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TRANSIONOSPHERIC DIFFERENTIAL DELAY MEASUREMENTS USING THE NTS --ETC(U)
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Transionospheric Differential Delay Measurements Using the NTS Satellites

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*Space Applications Branch
Space Systems Division*

April 1977

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TRANSIONOSPHERIC DIFFERENTIAL DELAY MEASUREMENTS USING THE NTS SATELLITES

Background

All radio signals transmitted through the ionosphere are subject to varying amounts of delay. With navigation satellites this delay can cause a significant portion of the error budget.

The NTS-1 satellite, launched on July 14, 1974 into a circular 8 hour orbit, is the first in the NAVSTAR GPS Program. This satellite transmits ranging signals at 335 and 1580 MHz. By correcting these signals to a common frequency and comparing the phase between these two signals the changes in delay can be measured as the satellite varies in elevation angle to the observer.

For an homogeneous ionosphere the differential delay is a relatively smooth function of the total electron content (TEC) of the ionosphere and the path length of the signals through the ionosphere (fig. 1). Two anomalies of importance to satellite navigation are depletion regions and the scintillation effect. The depletion regions are relatively large areas where the TEC is significantly less than surrounding areas. Gross variations in delay are observed when a satellite signal passes through these regions (fig. 2). The data for figures 1 and 2 was obtained using the Timation II satellite (ref. 1).

The scintillation effect is caused by small scale variations in the ionosphere and normally observed in equatorial and polar latitudes. During May 1975, the analog part of the equipment described in this report was used to obtain data near the magnetic equator (ref. 2). Figure 3 shows delay variations of approximately 2 nano-seconds and amplitude variations greater than 30 dBm. The amplitude fluctuations can cause serious power budget requirements for systems operating in these regions during periods of high scintillation activity.

It is hoped that the equipment described in this report can be used, in conjunction with the NTS-2

Note: Manuscript submitted April 5, 1977.

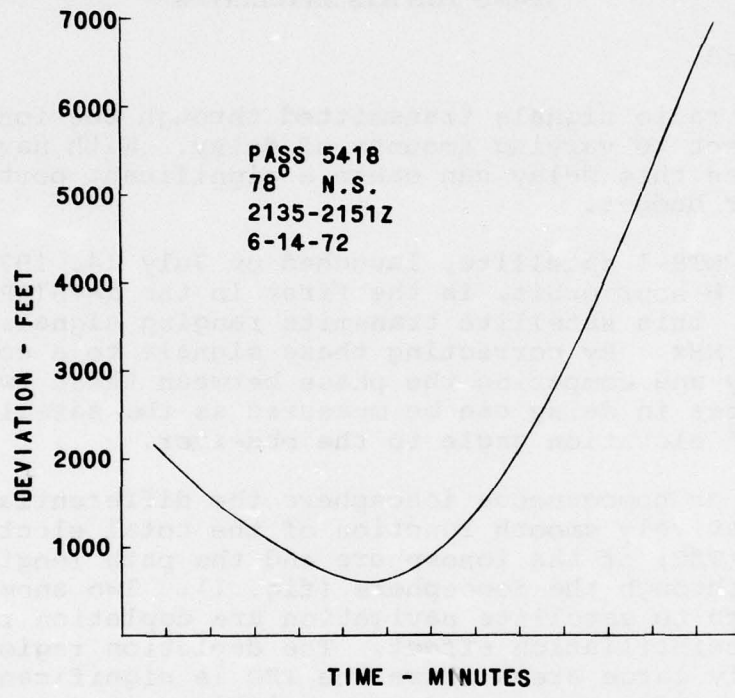


Fig. 1 - Normal delay

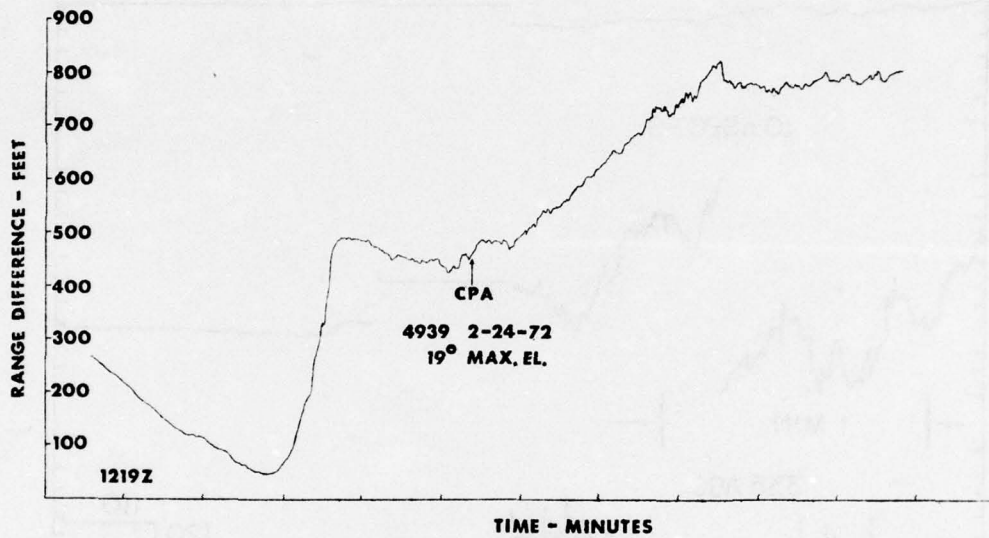
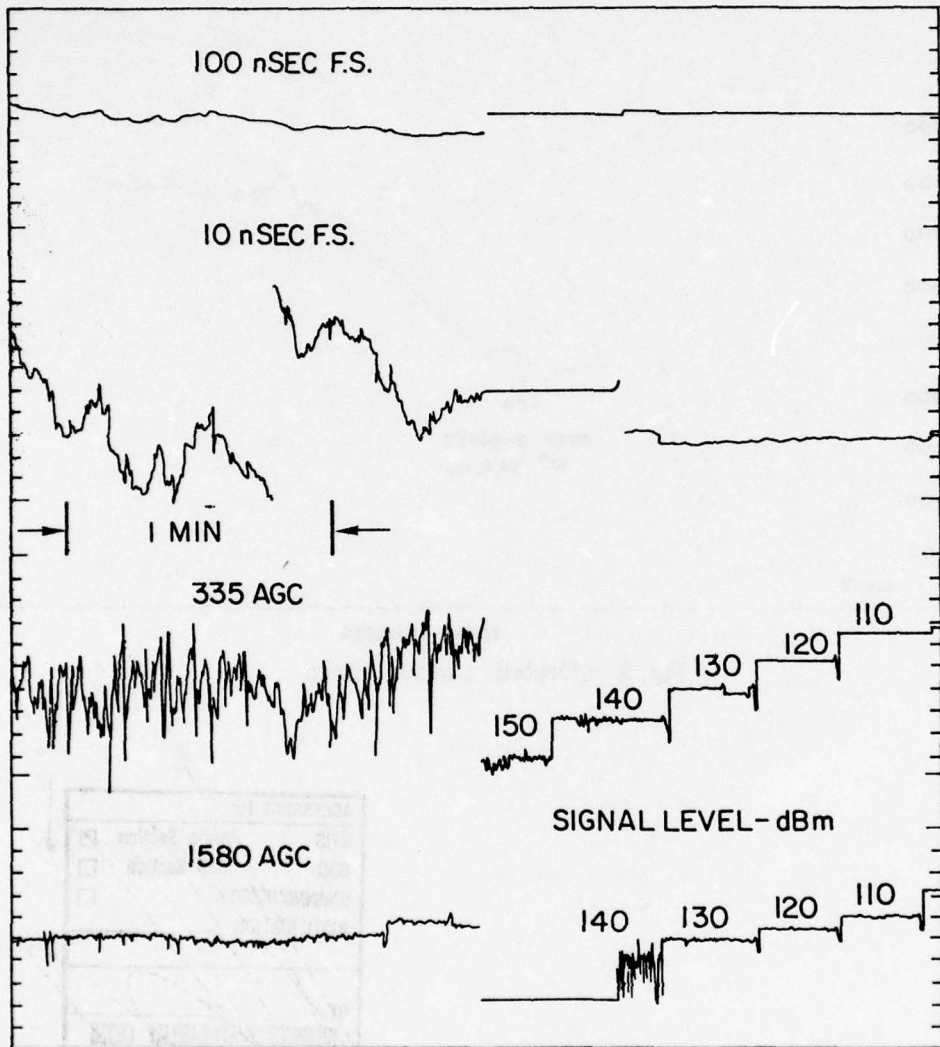


Fig. 2 - Depletion region effect

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Fig. 3 - Scintillation effect

satellite, to develop long term statistics on ionospheric scintillation.

Introduction

The system block diagram is shown in figure 4. MX780 doppler and MX760 ranging Magnavox receivers are used for signal acquisition. Since the outputs of the two models of receivers are different, two models of doppler converters were needed. The MX780 doppler receiver converts the beacon signals to 100 KHz signals with an equivalent doppler of 320 MHz. The MX760 ranging receivers convert the beacons to an equivalent 24 MHz with the doppler of 100 MHz. For the MX780 receivers a difference frequency of 100 MHz, which gives a range of 3 meters full scale and a precision of 3 centimeters, was chosen. Difference frequencies of 10 MHz and 1 MHz are also generated to examine coarser variations in delay. Because of the different outputs of the MX760 receiver, difference frequencies of 0.96 MHz, 9.6 MHz, and 96 MHz were chosen which give resolutions comparable to the MX780 system.

The outputs of the phase meters, along with the receiver AGC's, are displayed on a paper chart recorder. To facilitate data analysis the two higher frequency phase meters and the AGC's are digitized and recorded on a digital cartridge recorder. The digital portions of both systems are identical.

Doppler Converter for MX780 Receiver

The doppler converter (fig. 5) consists of the L.O. generator and the actual conversion circuitry. The L.O. generator, on P. C. Boards D-1 and D-2 (figs. 6 and 7) uses the 5 MHz station oscillator as a base frequency to synthesize 2.5 MHz, 900 KHz and 600 KHz L.O. frequencies. The L.O. output signals are buffered using low impedance line drivers. TTL level signals of 1 MHz and 100 KHz signals are also generated for use in the digital portion of the equipment.

The doppler converter for the 335 MHz signal is contained on boards D-3 and D-4 (figs. 8 and 9) which are duplicated for the 1580 MHz signal. The 100 KHz plus doppler signal is translated to 3.2 MHz in two stages. A single-shot is used to obtain a TTL level signal which is divided to produce 200 KHz plus 20 MHz doppler, 100 KHz plus 10 MHz doppler and 10 KHz plus 1 MHz doppler equivalent frequencies. The two lower frequencies are used directly by the phase meters. The 200 KHz signal is

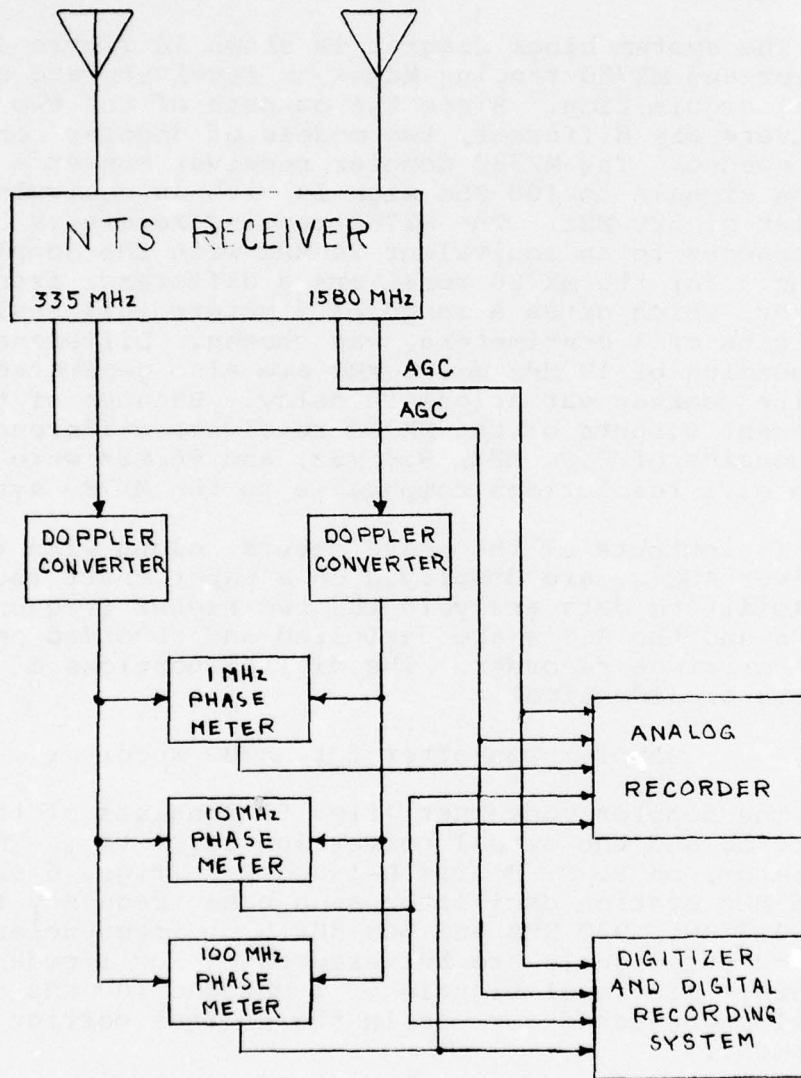


Fig. 4 - System block diagram

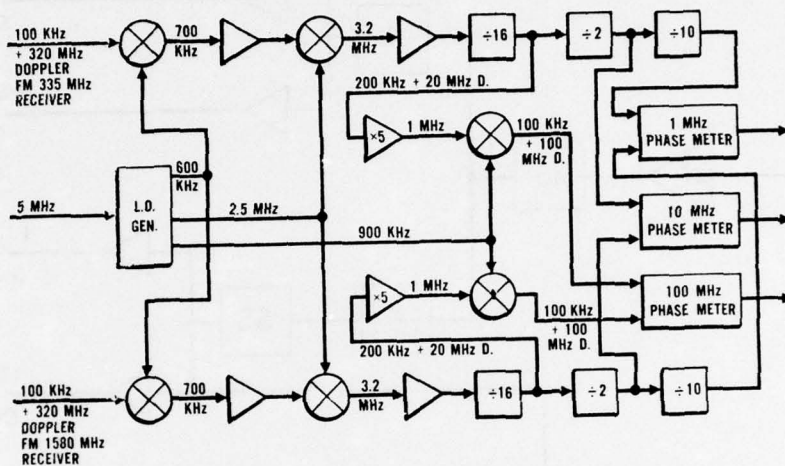


Fig. 5 — Doppler converter for doppler receiver

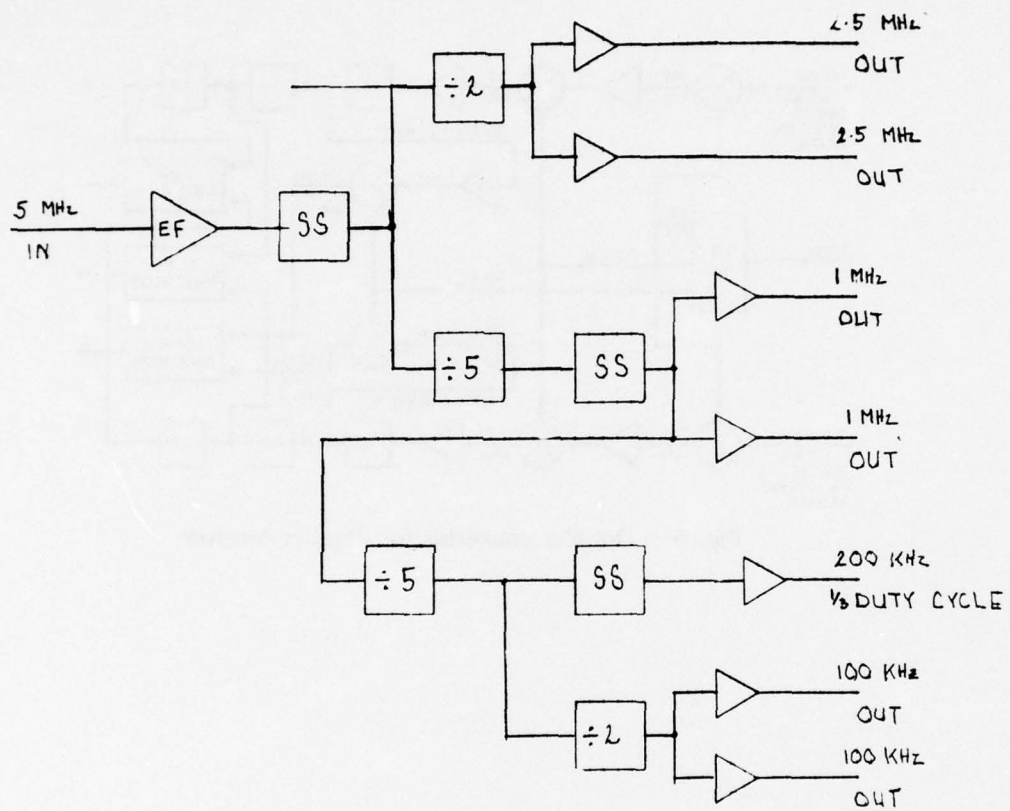


Fig. 6 - L. O. generator D-1

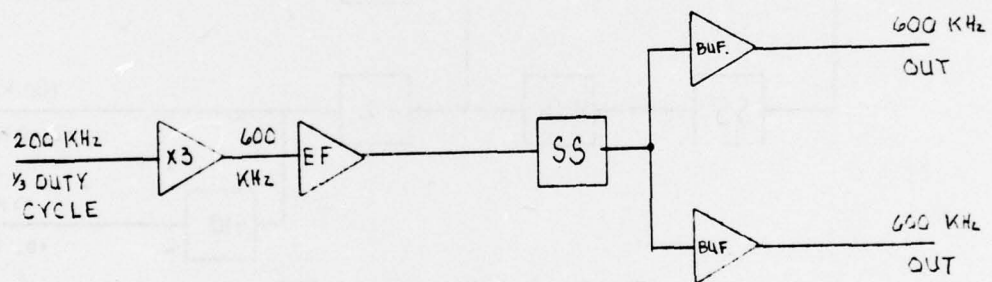
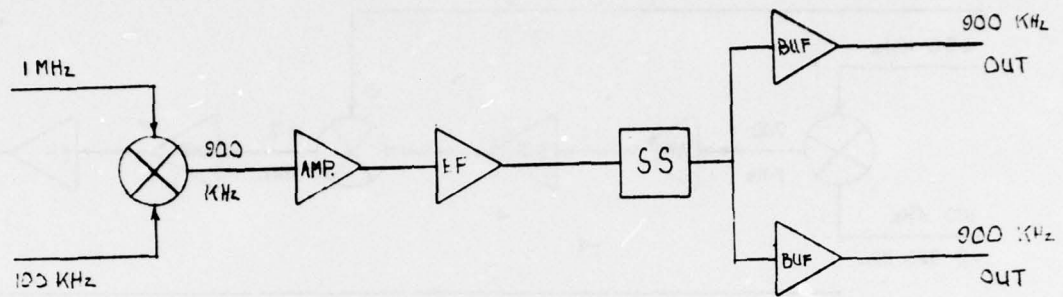


Fig. 7 - L. O. generator D-2

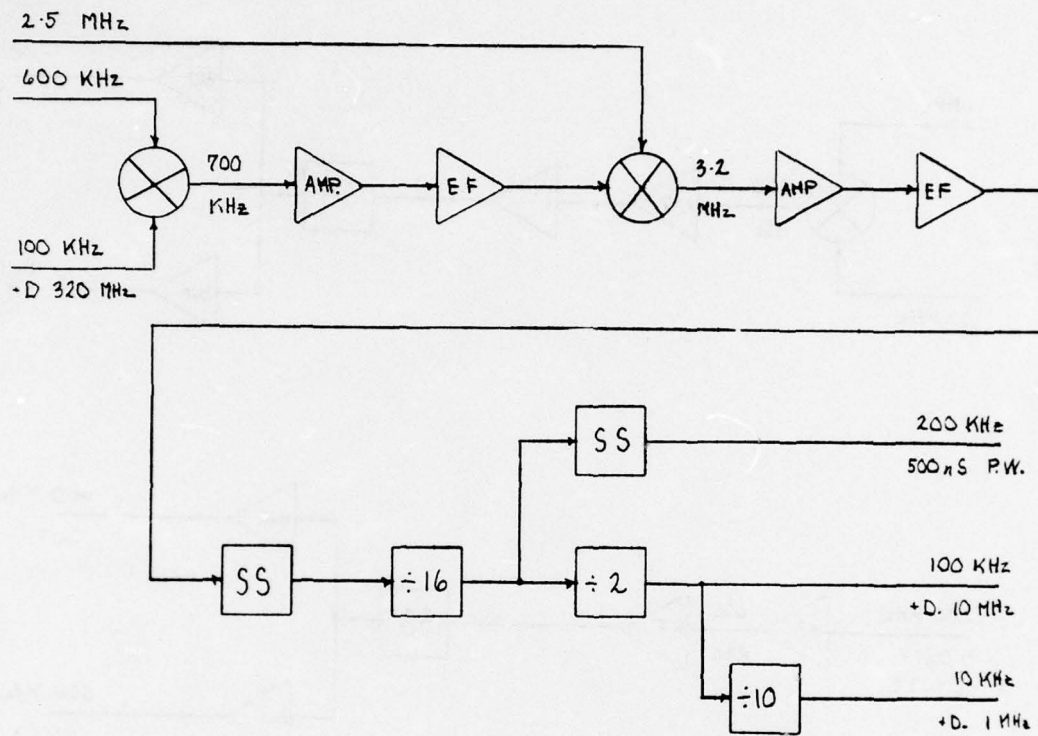


Fig. 8 — Doppler converter D-3

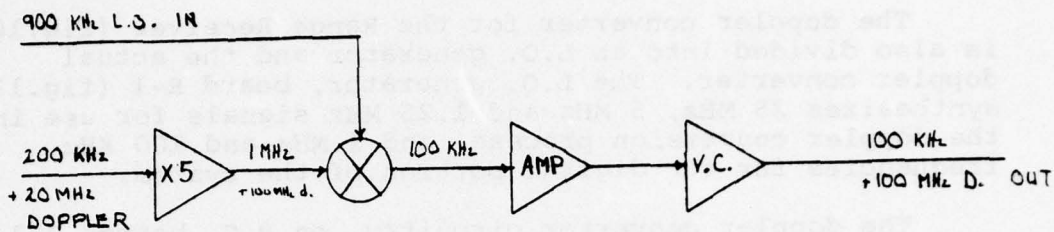


Fig. 9 - Doppler converter D-4

multiplied by 5 to generate a 1 MHz doppler signal which is translated to 100 KHz plus 100 MHz doppler for use in the phase meters.

Doppler Converter for MX760 Receiver

The doppler converter for the Range Receiver (fig.10) is also divided into an L.O. generator and the actual doppler converter. The L.O. generator, board R-1 (fig.11), synthesizes 25 MHz, 5 MHz and 1.25 MHz signals for use in the doppler conversion process, and 1 MHz and 100 KHz frequencies for the digital portion of the system.

The doppler converter circuitry, on P.C. boards R-2 and R-3 (figs. 12 and 13), converts the 24 MHz plus 24 MHz doppler signals from the receiver, to a 250 KHz plus 96 MHz signal. The 24 MHz is translated to 1 MHz and then multiplied by 4 to obtain the 96 MHz equivalent doppler. This signal is translated in two stages to the desired 250 KHz plus 96 MHz doppler. These two boards are duplicated, one set for each beacon signal, and all four boards are mounted in shielded boxes to reduce EMI between them. On board R-4, (fig. 14) voltage comparators are used to obtain TTL level signals which are divided to produce the 25 KHz plus 9.6 MHz doppler and 2.5 KHz plus 0.96 MHz doppler signals.

Phase Meters and Amplifiers

The phase meters (board B-5) and amplifiers (board B-6) are the same for both systems (figs. 15 and 16). A pulse width modulation (PWM) technique is used to measure phase. The equivalent doppler signals are fed through AND/OR gates to single shots which generate a narrow pulse on the rising edge of the input signal. Each signal derived from the 335 MHz beacon sets an R-S flip-flop while its corresponding doppler frequency from the 1580 MHz beacon resets the flip-flop to produce a signal whose pulse width is proportional to the difference in phase between the two equivalent doppler signals. The outputs of the flip-flops are integrated using an R-C network to give a varying DC voltage. These signals are amplified using 741 operational amplifiers and fed to the paper chart recorder. The PWM signals from the two highest resolution phase meters go to the amplifier board for use in the digital portion of the equipment.

The amplifier board performs two functions. First, the AGC's from the receiver are inverted and amplified to be displayed on the paper chart recorder. Secondly, the

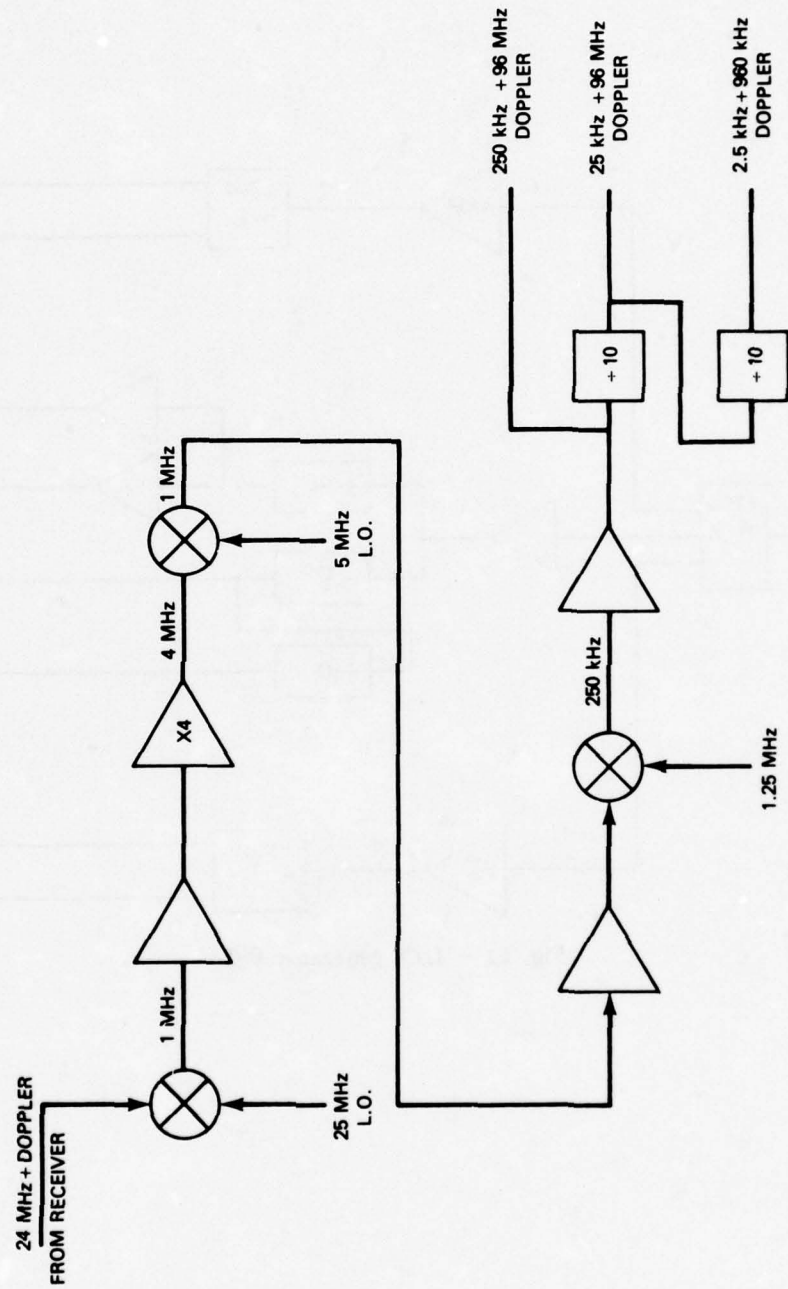


Fig. 10 — Range receiver doppler converter

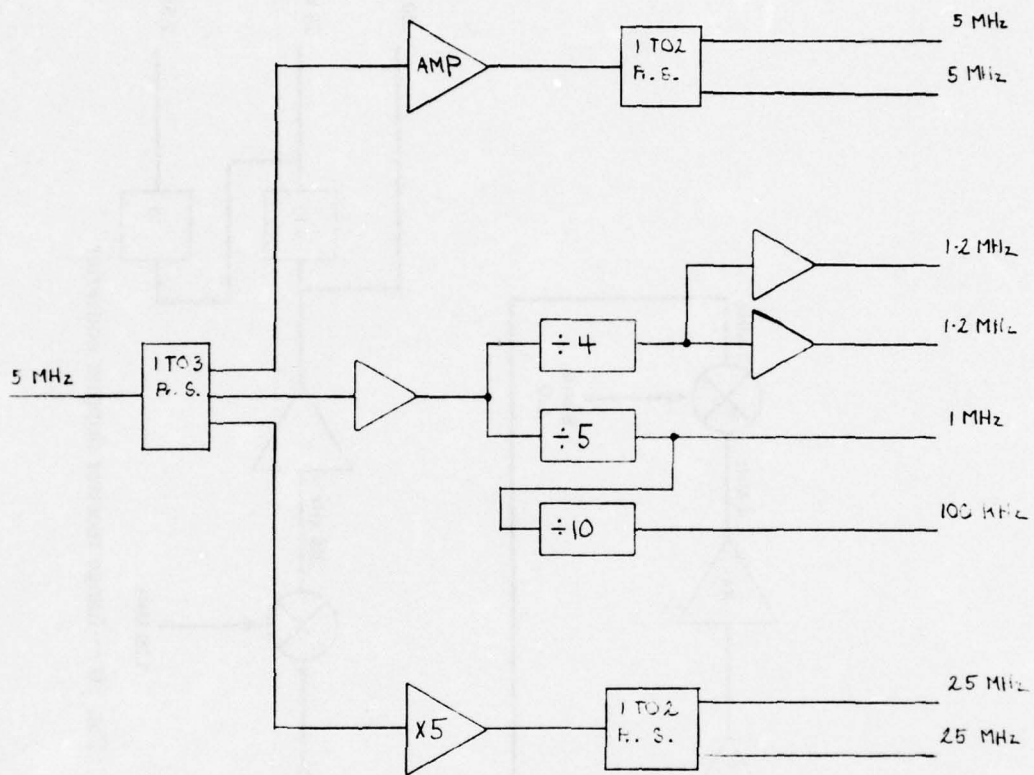


Fig. 11 - L.O. generator R-1

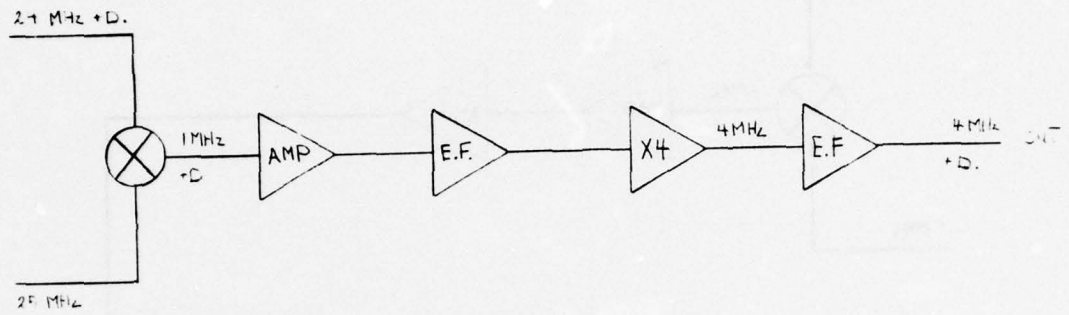


Fig. 12 — Doppler converter R-2

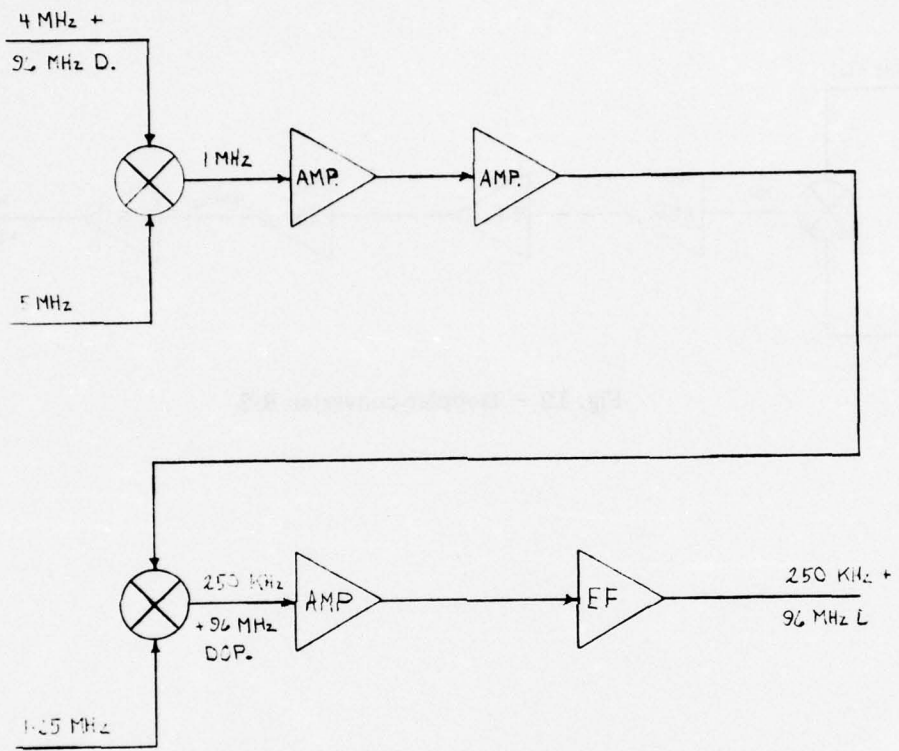


Fig. 13 — Doppler converter R-3

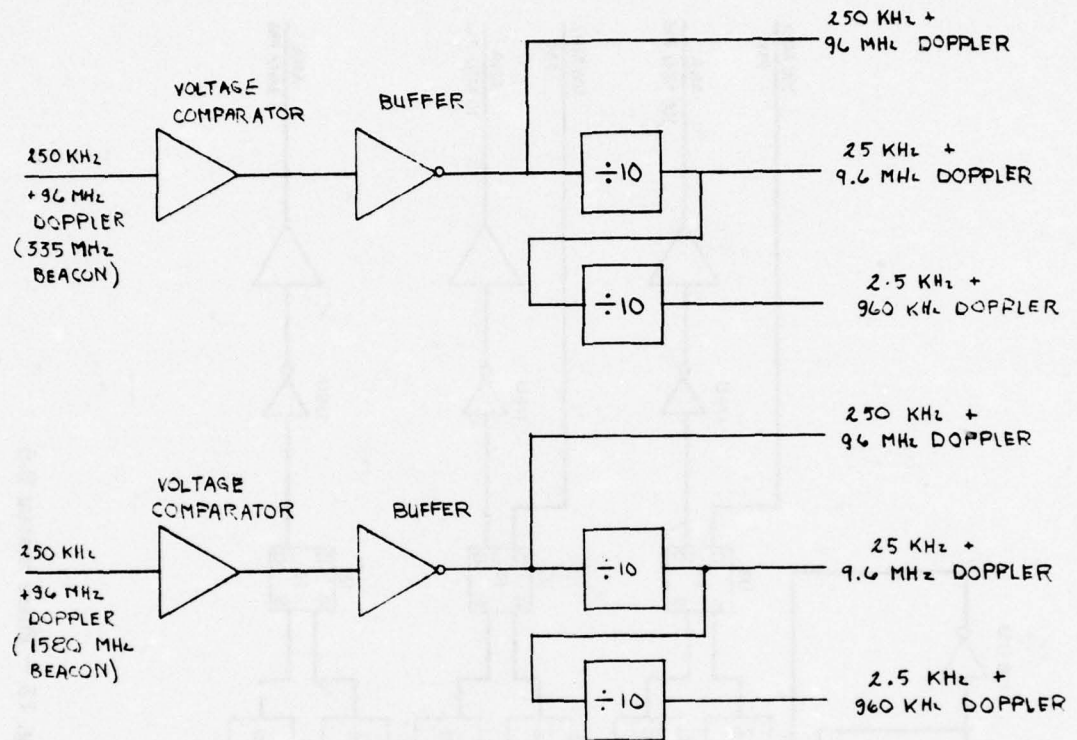


Fig. 14 - Doppler converter R-4

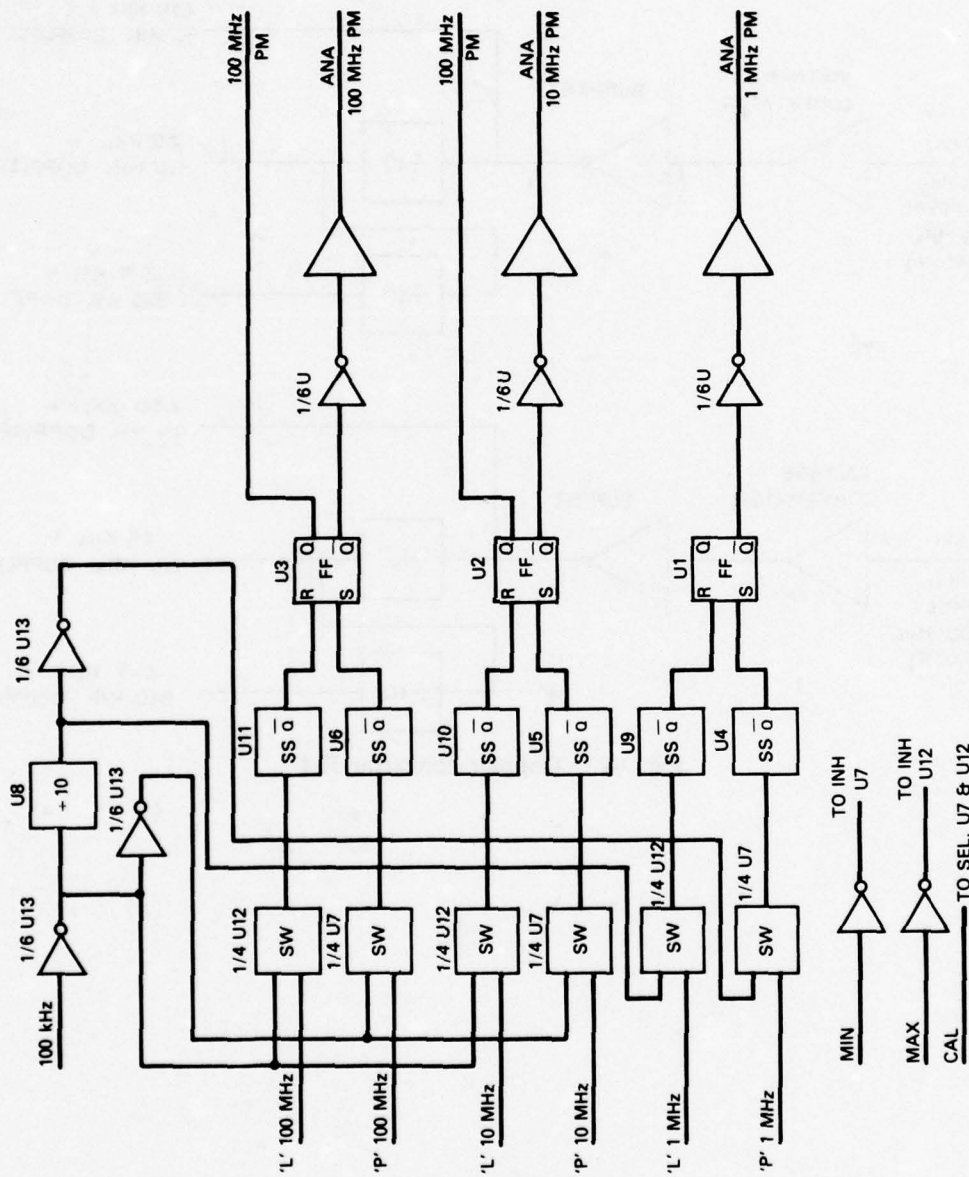


Fig. 15 — Phase meters B-5

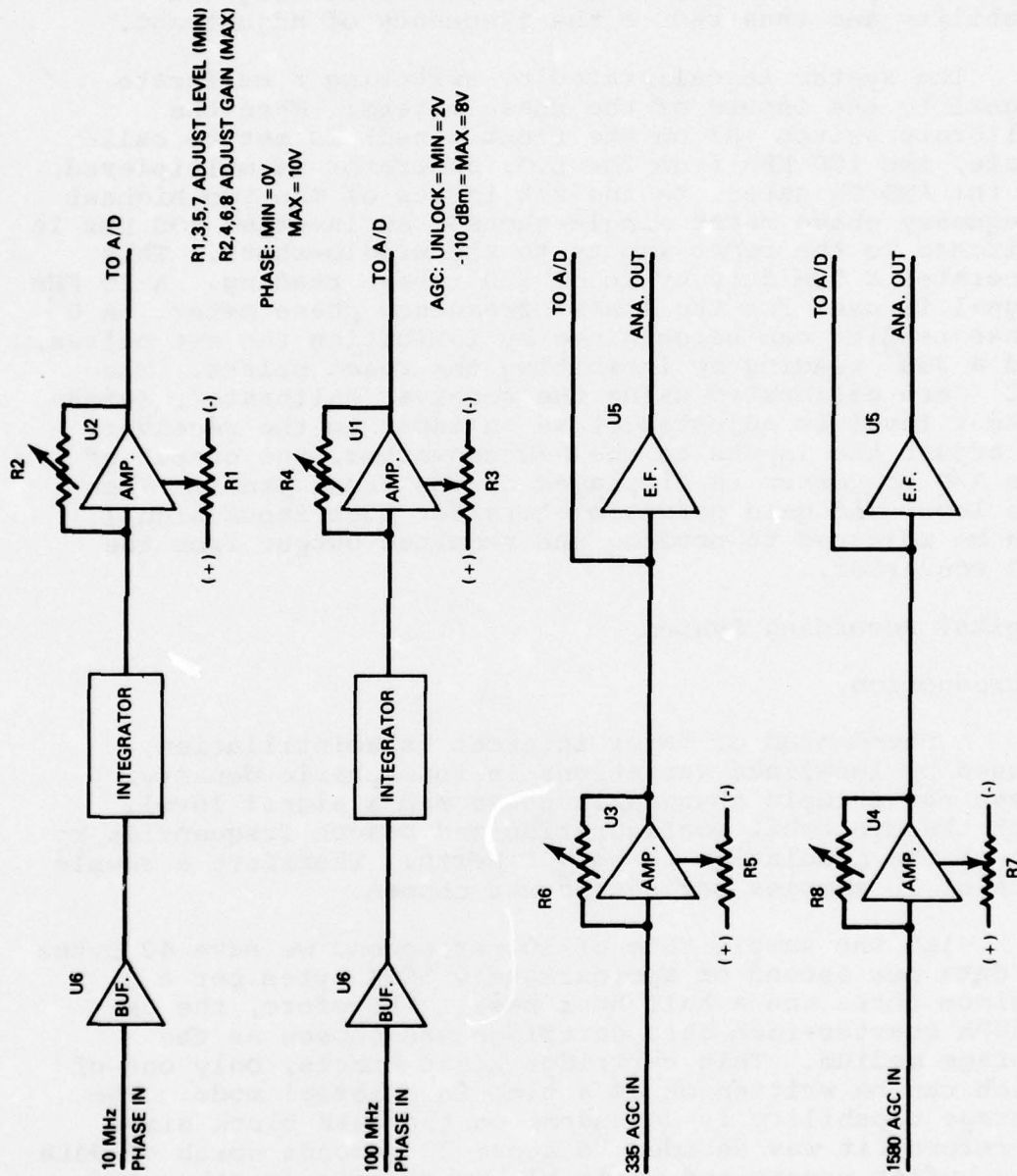


Fig. 16 — Amplifiers B-6

levels of the two highest phase meter and the AGC signals are adjusted to be compatible with the input requirements of the A/D converter (0-10 volts F.S.). Precision operational amplifiers are used to improve accuracy and stability and thus reduce the frequency of adjustment.

The system is calibrated by switching a calibrate signal to the inputs of the phase meters. When the calibrate switch (S3 on the front panel) is set to calibrate, the 100 KHz from the L.O. generator is multiplexed, by the AND/OR gates, to the set inputs of the two highest frequency phase meter single-shots. An inverted 100 KHz is switched to the reset inputs to the single-shots. This generates a 50% duty cycle or 180° phase reading. A 10 KHz signal is used for the lowest frequency phase meter. A 0° phase reading can be obtained by inhibiting the set pulses, and a 360° reading by inhibiting the reset pulses. The AGC's are calibrated using the receiver calibrator, (whose output level is adjustable) as an input to the receiver. To adjust the inputs to the A/D converter, the output of the A/D converter is displayed on the front panel. Then the level and gain potentiometers for each input signal can be adjusted to produce the required output from the A/D converter.

Digital Recording System

Introduction

A phenomenon of major interest is scintillation, caused by localized variations in ionospheric density. These cause rapid changes in phase and a signal level. With the NTS orbit configuration and beacon frequencies we expect the modulation to be ≤ 1 Hertz. Therefore a sample rate of 10 samples per second was chosen.

With the sample rate of 10 per second we have 40 bytes of data per second or approximately 500K bytes per a maximum three and a half hour pass. Therefore, the 3M DC300A quarter-inch data cartridge was chosen as the storage medium. This cartridge has 4 tracks, only one of which can be written on at a time in a serial mode. The storage capability is dependent on the data block size. Therefore, it was decided to store 30 seconds worth of data in a buffer memory and write blocks of this length. The time of the start of the block of data is stored in the first 3 bytes for an identification header giving a block size of 1203 bytes. For this block size the cartridge will store approximately 560K bytes (approx. 3½ hours worth of data) on a single track and 14 hours worth of data can be

recorded on one cartridge.

The digital system (1) digitizes the two highest resolution phase meters and the AGC's (2) stores 30 seconds worth of data in a buffer memory, (3) records the data on a cartridge recorder, (4) incorporates calibration and testing features. The system is divided into 5 major subsystems (fig. 17); the A/D converter, buffer memory, memory controller and memory test; clock and timing generator; tape recorder interface, controller and digital tape recorder; and the display and controller.

A/D Converter

Every 0.1 second the A/D converter subsystem (fig. 18) digitizes the four analog input signals; stores the data in a 32 bit shift register; notifies the memory controller that data is ready to be stored in the buffer memory; and, under command of the memory controller, serially transfers the data to the buffer memory in 8 bit bytes MSB first. The analog signals are digitized in the sequence: 100 MHz phase meter; 10 MHz phase meter; 335 MHz AGC, and, 1580 MHz AGC. The A/D converter is an 8 bit, 10 volts full scale converter with a 2 digit BCD output code. The BCD output code was selected to simplify interfacing to the display while giving the required precision, 1% full scale.

A 10 pps signal from the clock and timing system starts a conversion cycle. Upon receipt of a pulse the $\div 32$ and $\div 2$ counters are reset, the sample and hold amplifier samples the 100 (or 96) MHz phase meter and the A/D converter is activated. The A/D converter indicates end of conversion (EOC) by bringing the EOC line low. This triggers the pulse generator which causes the analog multiplexer to switch to the next input channel, the signal is sampled by the S/H amplifier, the output of the A/D is latched into a 8 bit parallel to serial shift register, and the A/D converter is restarted. A 8 cycle clock generator is also started, which transfers the data into a 32 bit serial shift register. The number of clock cycles is counted by the $\div 32$ counter. After 4 conversions the pulse generator is inhibited and the Q output of the $\div 2$ counter goes high. This signal (DRDY) goes to the memory controller to indicate data is ready to be stored in the buffer memory. The data is transferred to the memory 8 bits at a time by means of a clock (WCLK) generated by the memory controller. A combined lock (COMB LK) signal, which is generated by the receiver, indicates whether the receiver is locked onto both beacon frequencies. If not, a series of ones is clocked into the 32 bit shift register

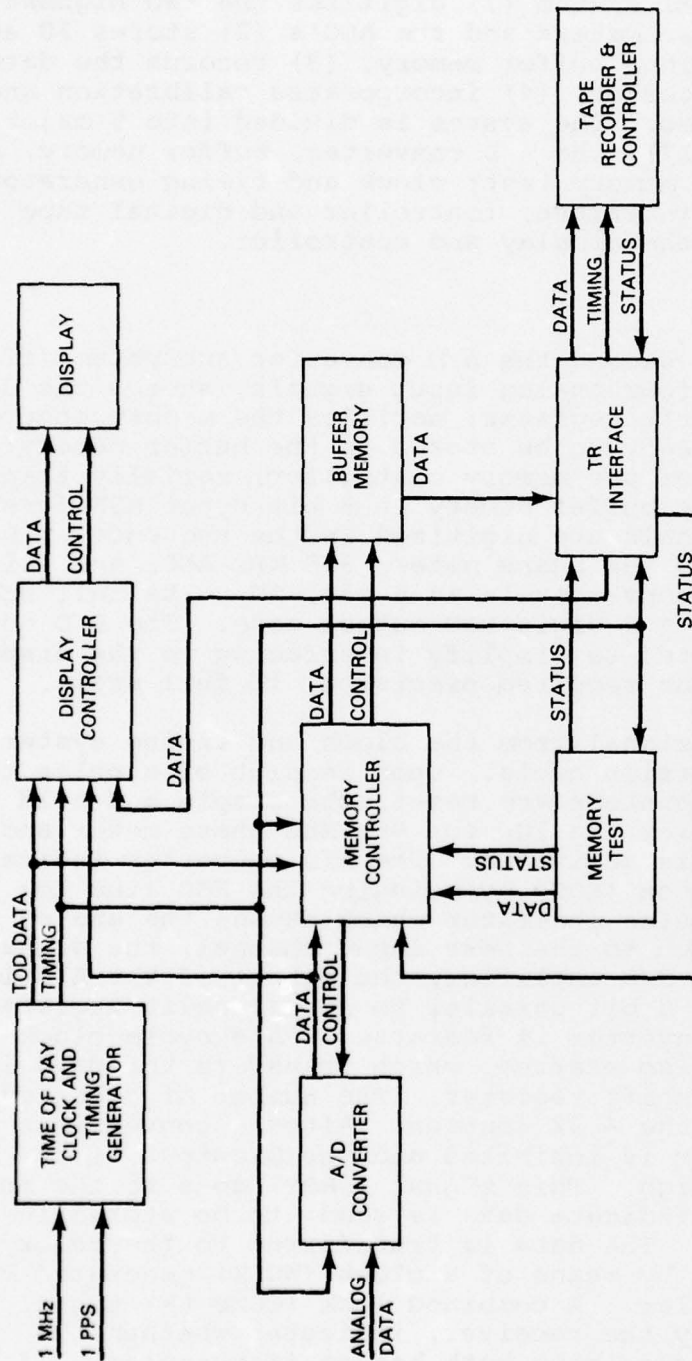


Fig. 17 -- Digital system

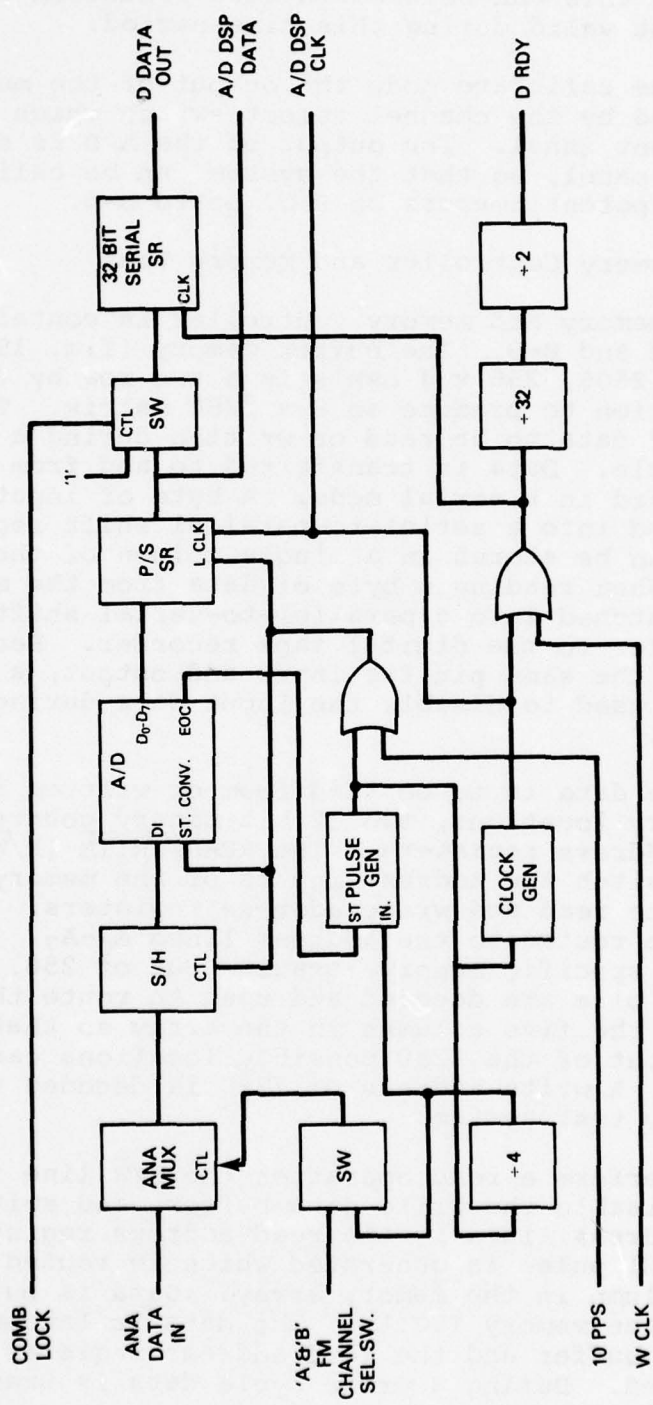


Fig. 18 - A-d converter B-7

instead of the output of the A/D converter. Since a data word of all ones is not a valid output for the A/D converter, this can be used in data reduction to indicate data is not valid during this time period.

In the calibrate mode the output of the multiplexer is selected by the channel select switch which is located on the front panel. The output of the A/D is displayed on the front panel, so that the system can be calibrated using the potentiometers on P.C. board B-6.

Memory, Memory Controller and Memory Test

The memory and memory controller is contained on P.C. boards B-8 and B-9. The buffer memory (fig. 19) uses ten Signetics 2606, 256 x 4 RAM's in a two row by five column configuration to produce an 8 x 1280 matrix. This allows one byte of data to be read or written during a single memory cycle. Data is transferred to and from the buffer memory board in a serial mode. A byte of input data is transferred into a serial-to-parallel shift register so that it can be stored in a single column of the memory matrix. When reading a byte of data from the memory, the data is latched into a parallel-to-serial shift register for transfer to the digital tape recorder. Because the 2606 uses the same pin for input and output, a tri-state buffer is used to disable the input data during a read operation.

Since data is to be read from or written into sequential memory locations, two 12 bit binary counters are used for the address registers. The READ/WRITE (R/W) line is used to switch the address inputs of the memory I.C.'s between the read and write address registers. The first 8 bits are routed to the address lines A₀-A₇. This chooses a specific memory location out of 256. The next 3 address bits are decoded and used to route the CE pulse to one of the five columns in the array so that a specific location out of the 1280 possible locations can be accessed. A write address of 1280 is decoded for use by the memory test system.

To perform a read operation the R/W line is pulled high to disable the write data buffers and switch the memory address lines to the read address register. A chip enable (CE) pulse is generated which is routed to the proper column in the memory array. Data is put on the I/O lines of the memory I.C.'s. The data is latched into the read data buffer and the read address register is incremented. During a write cycle data is transferred to

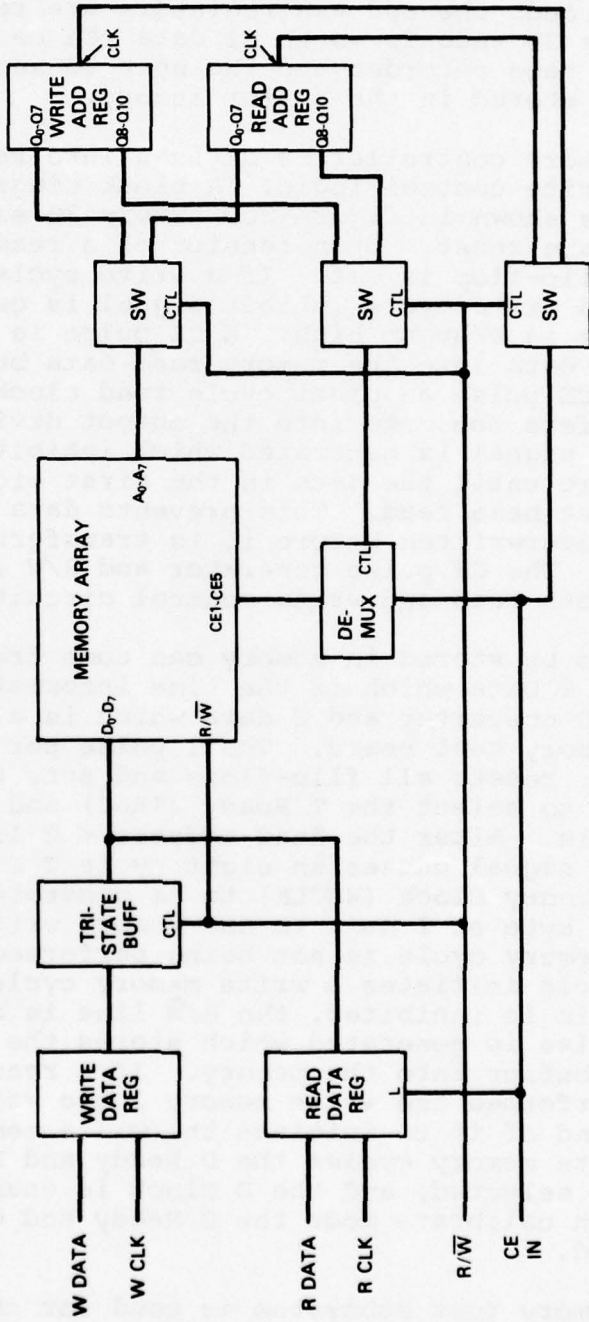


Fig. 19 — Buffer memory B-9

the write data register, the R/\bar{W} line goes low, the address lines are switched to the write address register, the write data buffers are enabled and the CE pulse stores data into the memory and increments the write address register. Every 30 seconds the address registers are reset, so that the previous 30 seconds worth of data can be transferred to the digital tape recorder and the next 30 seconds worth of data can be stored in the buffer memory.

The memory controller is divided into read control logic and write control logic. A block diagram of the read circuitry is shown in figure 20. Every 30 seconds all flip-flops are reset. Upon receipt of a read ready signal (RRDY), a flip-flop is set. If a write cycle is not being performed, a write cycle inhibit signal is generated and the R/\bar{W} line is brought high. A CE pulse is generated which loads data into the memory read data buffer. At the end of the CE pulse an eight cycle read clock is generated which transfers the data into the output device. A read address < 8 signal is generated which inhibits the write control logic until the data in the first eight memory locations has been read. This prevents data in the memory from being overwritten before it is transferred to the output device. The CE pulse generator and R/\bar{W} flip-flop are common to both read and write control circuitry.

Data to be stored in memory can come from 3 locations (fig. 21). T Data which is the time information, D Data from the A/D converter and C data which is a test pattern from the memory test board. The 1 pulse per 30 seconds reset pulse, resets all flip-flops and sets the dual 4-1 multiplexer to select the T Ready (TRDY) and T Data (TDAT) input signals. After the Read address < 8 line goes low, a TRDY true signal causes an eight cycle T Clock (TCLK) and Write Memory Clock (WMCLK) to be generated. This transfers a byte of T Data to the memory write data buffer. If a read memory cycle is not being performed, the last WM clock cycle initiates a write memory cycle. The read control logic is inhibited, the R/\bar{W} line is brought low, and a CE pulse is generated which stores the data in the write data buffer into the memory. If a read memory cycle is being performed the write memory logic waits until after the end of it to initiate the write memory cycle. After 3 write memory cycles the D Ready and D Data input signals are selected, and the D Clock is enabled. When the system is in calibrate mode the C Ready and C Data signals are selected.

The memory test subsystem is used for checking the operation of the buffer memory. In the calibrate mode the

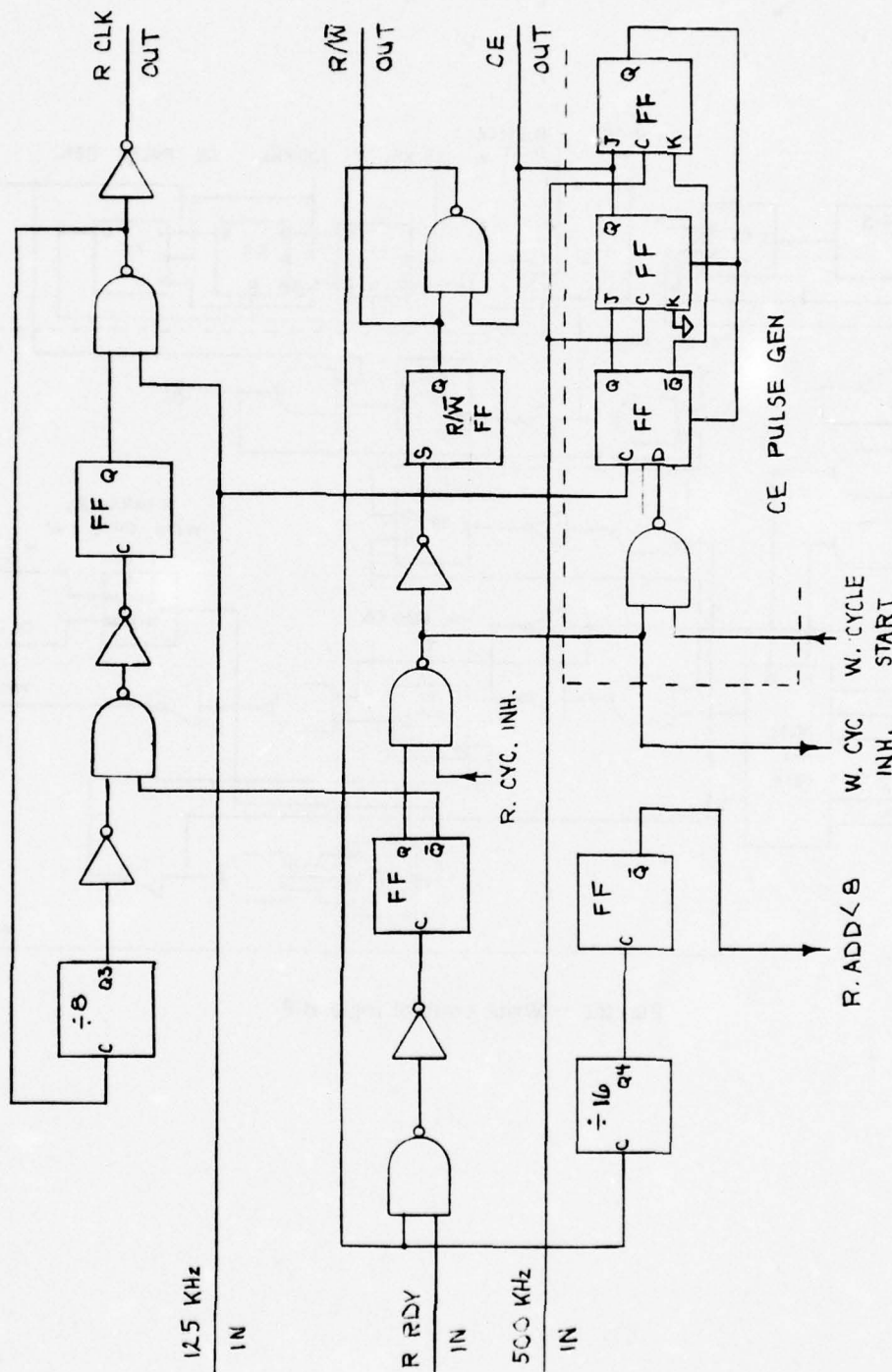


Fig. 20 — Read control logic B-8

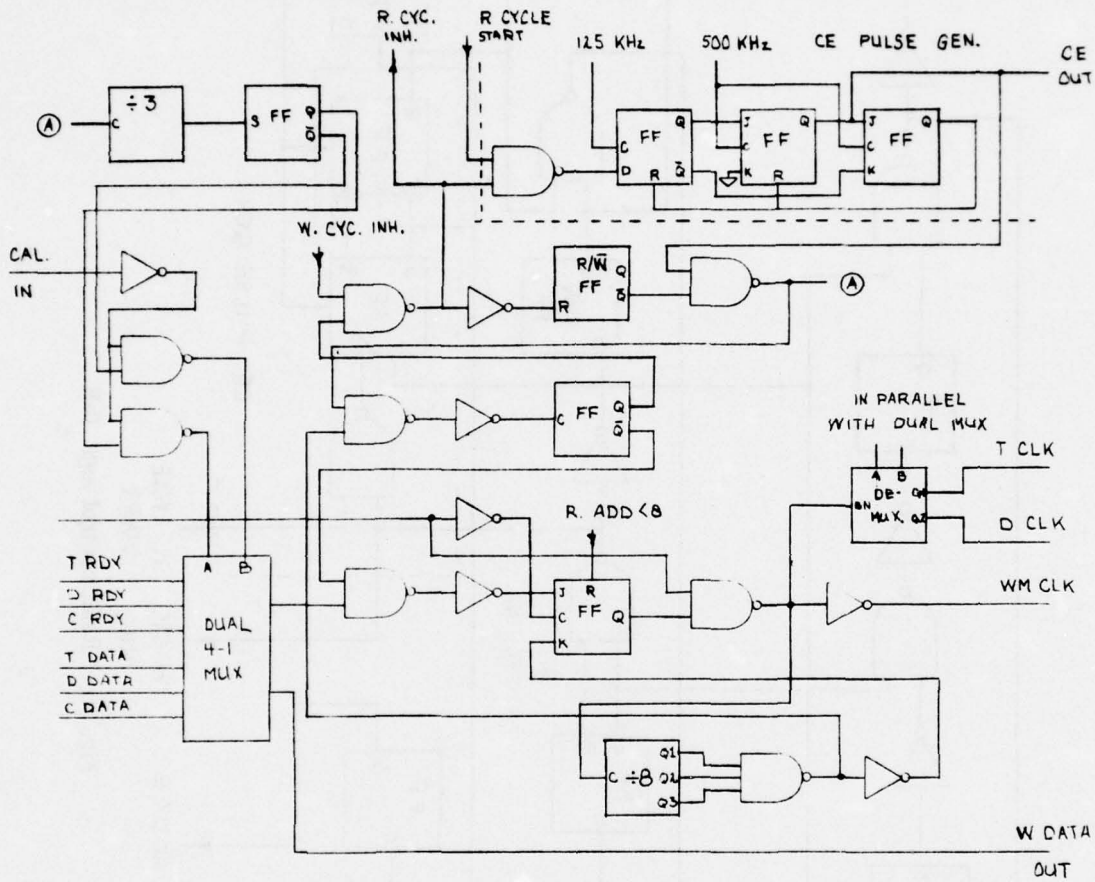


Fig. 21 - Write control logic B-8

buffer memory can be loaded with a sequence the BCD digits 00 through 99, and then the contents of the memory can be displayed on the front panel. This subsystem (located on P.C. board B-11) is divided into memory load and memory read electronics (figs. 22 and 23). In the operate mode the 1P/30 sec signal is passed through and used as the system reset. When the system is put into the calibrate mode, a single pulse is generated which resets the system and all flip-flops and counters on the memory test board.

When the system is set in the calibrate mode the memory test subsystem is automatically put in the memory load mode. When the memory load/read switch on the front panel is activated, a pulse is generated which sets C Ready (CRDY). This causes the data in the parallel/serial shift register to be transferred to the memory write data buffer. After eight clock pulses CRDY is reset. A write memory cycles is initiated by the memory controller. The CE pulse increments a \div 100 BCD counter and loads it outputs into the shift register. The falling edge of the CE pulse sets CRDY and the cycle is repeated until the 1280 W ADD line goes high. This indicates that the memory has been loaded and switches the memory test subsystem into the read mode. If the continuous/single switch is in the single position only one load cycle is performed for each activation of the memory load switch. This is useful for debugging the system.

Once the subsystem is in the read mode, another activation of the memory load/read switch starts to read the data in the memory and display it on the front panel. Every 0.2 seconds the DSP RDY is set (used as R RDY when in the calibrate mode). This starts a read memory cycle and transfers the data to the display controller. The display should show the digits 0 through 99 at a 0.2 second rate if the memory is operating properly. Again this can be done in a single cycle mode, for trouble-shooting.

Tape Recorder Interface and Controller

This subsystem (fig. 24) transfers data and control signals to and from the tape recorder interface. Differential line drivers and the optical coupled isolators are used as the line drivers and receivers for twisted pair lines. This eliminates ground loop problems, and reduces interference.

When the system is in calibrate or the front panel tape recorder on-off switch is in the off position, this signal is inhibited. When the TR RDY (used as R RDY in

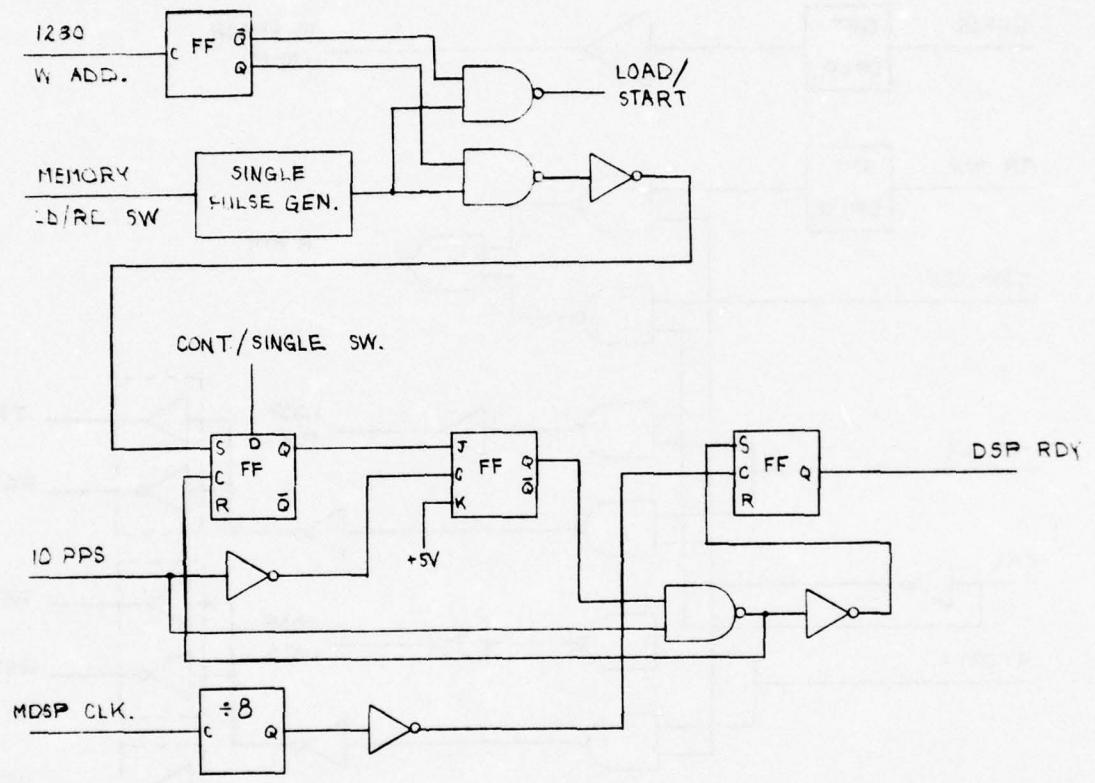


Fig. 23 — Memory test read logic B-11

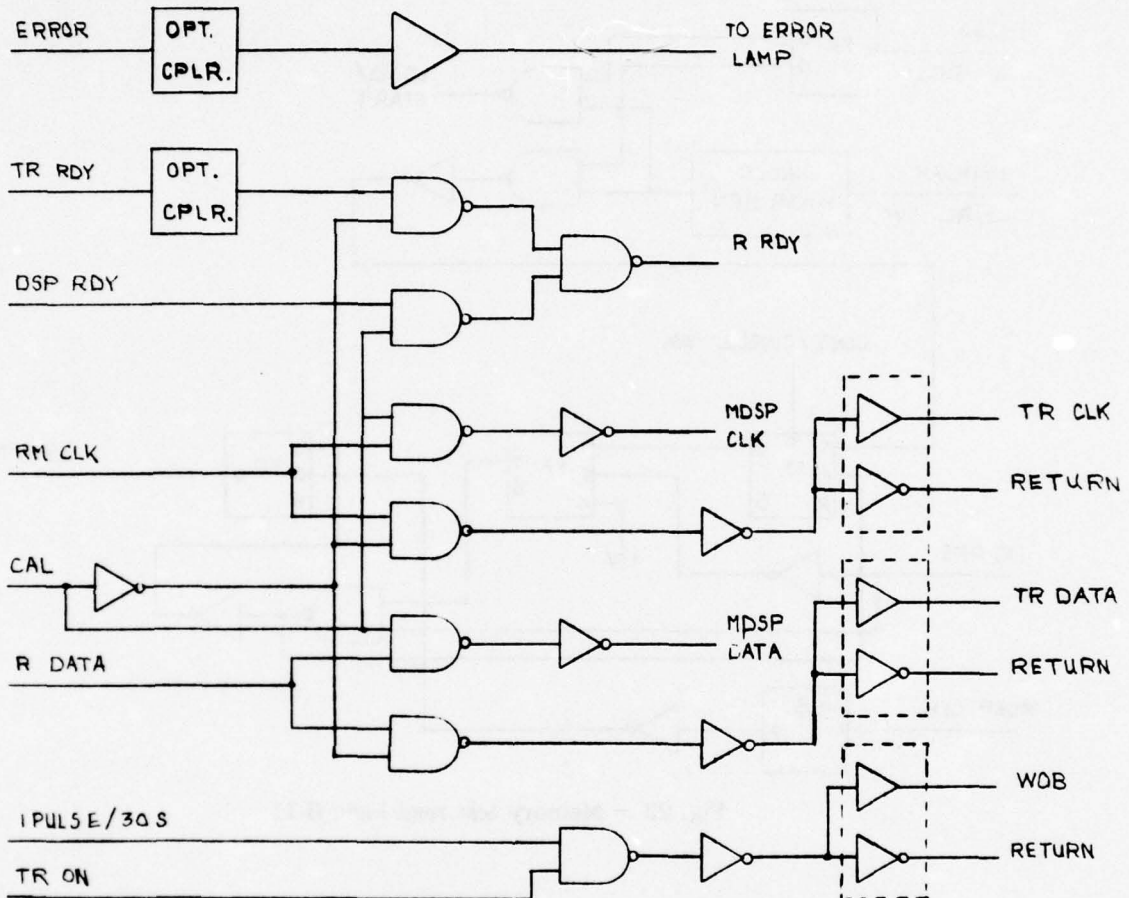


Fig. 24 - T.R. interface B-10

the operate mode) line goes high a read memory operation is performed and the data is serially transferred to the tape recorder by the TR Data and TR CLK lines.

In the calibrate mode the TR CLK and TR Data signals are inhibited and the DSP RDY signal from the memory test subsystem is used as R RDY. When DSP RDY goes high, a memory read operation is performed and the Data is transferred to the display via the MDSP Data and MDSP CLK. These lines are inhibited when the system is in the operate mode.

The tape recorder controller (fig. 25) is mounted in the tape recorder chassis. The 1P/30 sec signal is used to initiate a transfer of a block of data from the buffer memory to the tape recorder. This signal is inverted and sent to the tape recorder as the write one block (WOB) signal and it simultaneously sets the TR RDY flip-flop and resets all other flip-flops and counters. The TR RDY signal starts a memory read cycle and the transfer of one byte of data to a serial-to-parallel shift register on the controller P. C. board. The TR clock is divided by 8 to turn off the TR RDY signal when the shift register has been loaded. When the tape recorder is ready to record a data byte, it sends a data request strobe (DRS) which is buffered and returned to the recorder as the write data strobe (WDS). The DRS also sets the TR RDY flip-flop to initiate a read memory cycle and increments a $\div 1203$ counter. After 1203 bytes of data have been recorded the WDS is inhibited which indicates to the tape recorder the end of the data block. Two signals from the tape recorder ERROR and end of tape warning (EOTW) are used to turn on a lamp on the front panel when either signal is activated. Frequency activation of the ERROR signal would indicate to the operators a bad data tape or a malfunction in the tape recorder. Activation of the EOTW signal indicates to the operator to rewind the tape and switch to the next track. The EOTW signal also inhibits the WOB signal to prevent the equipment from attempting to write a data block beyond the end of the tape.

Time of Day Clock and Timing Signal Generator

The clock and timing subsystem (fig. 26) performs two functions; the 1 MHz signal from card 1 is divided down to produce necessary system clock and timing signals and 1 pps signal from the station clock is used to drive a 24 hour time of day clock. The division of the 1 MHz is straight forward using dual BCD counters. A single-shot is used to generate a 8 microsecond pulse 10 times per second. The

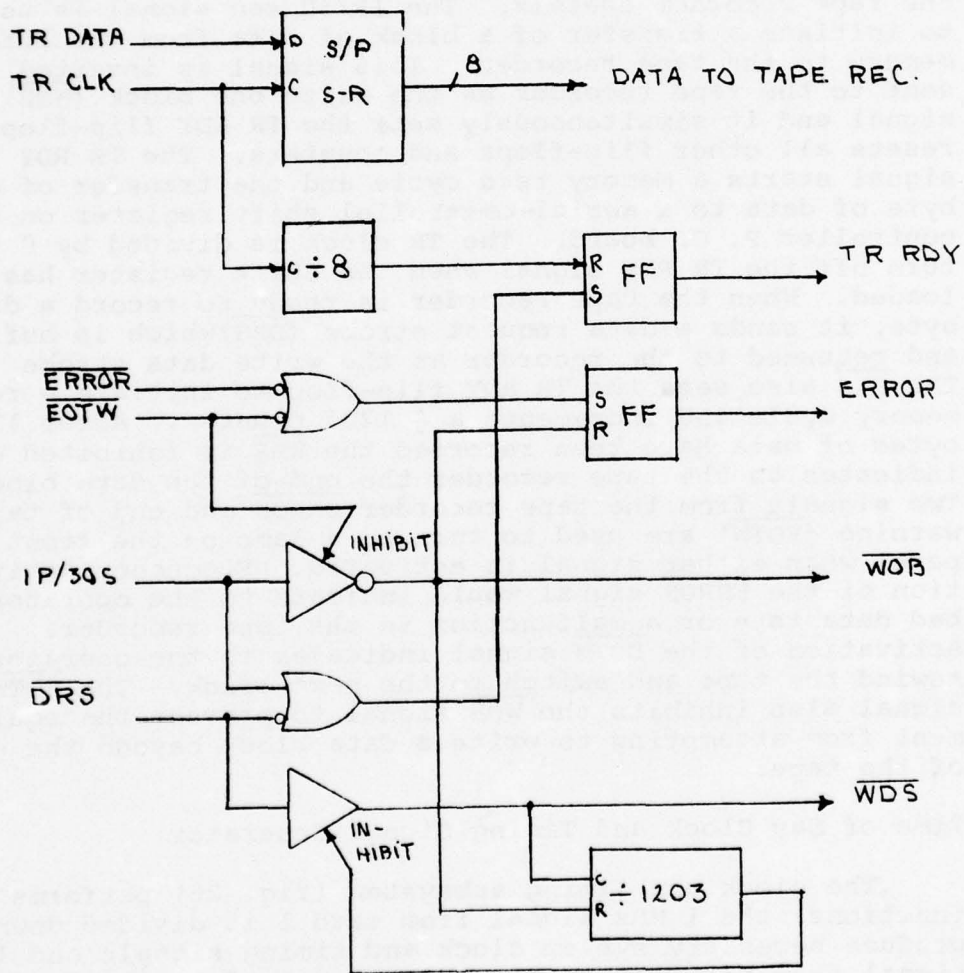
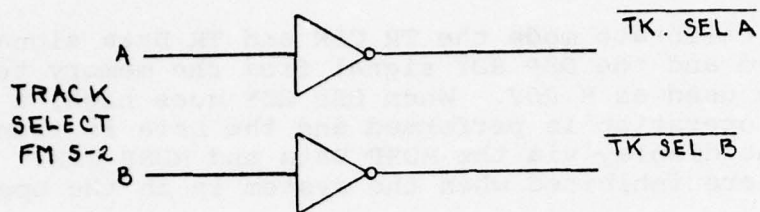


Fig. 25 — Tape recorder controller

1 pps resets the counters to synchronize the output signals.

The time clock consists of 3 dual BCD counters and associated decoding circuitry to produce the $\div 6$ counters for the 10's of seconds and 10's of minutes. The 24 hours condition is decoded to reset the hours and 10's of hours counters. The 00 and 30 second states are decoded to generate the 1P/30 seconds signal. To set the clock the appropriate counter is selected by the time set switch on the front panel. When the time set push button switch is activated a pulse is generated and routed to the selected counter through a demultiplexer. Every second the BCD outputs of the time clock are loaded into a 24 bit parallel serial shift register. A 24 cycle clock is started which transfers the time information to the display controller for display on the front panel. The 24 bit shift register is connected as a circular shift register so that the time information is re-entered. After the time has been transferred to the display, TRDY goes high so that the time data can be stored in the buffer memory once every 30 seconds.

Display and Display Controller

This section (figs. 27 and 28) is used to present necessary information to the operator. Three types of data can be selected; the output of the A/D converter, the output of the memory when using the memory test function, and the time of day, under control of a front panel thumb-wheel switch. Positions 0 through 3 selects one of the A/D channels, position 4 selects the memory display data; position 5 is the time of day data; and, position 6 disables the display. To reduce power consumption and the number of interconnections, the data is multiplexed to the display card which is mounted on the front panel. The selected data and clock are routed through a multiplexer to a 24 bit serial to parallel shift register. Each four bits corresponding to one digit is routed to a quad tri-state buffer. The outputs of the buffers are connected to a four line bus which transfers the data to the display card. A 1 KHz signal from the clock is used to develop the digit select control lines. The 1 KHz is divided by a $\div 8$ counter. The outputs of the first 3 stages of the counter are routed to the display card as the digit select lines. They are also fed to a one of ten decoder, the output of which is used to enable a particular tri-state buffer. The corresponding 7 segment display is enabled simultaneously. Since the data in positions 0 through 4 is only 2 digits, the $\div 8$ counter is reset on count 2. Thus only the first two 7 segment displays are enabled.

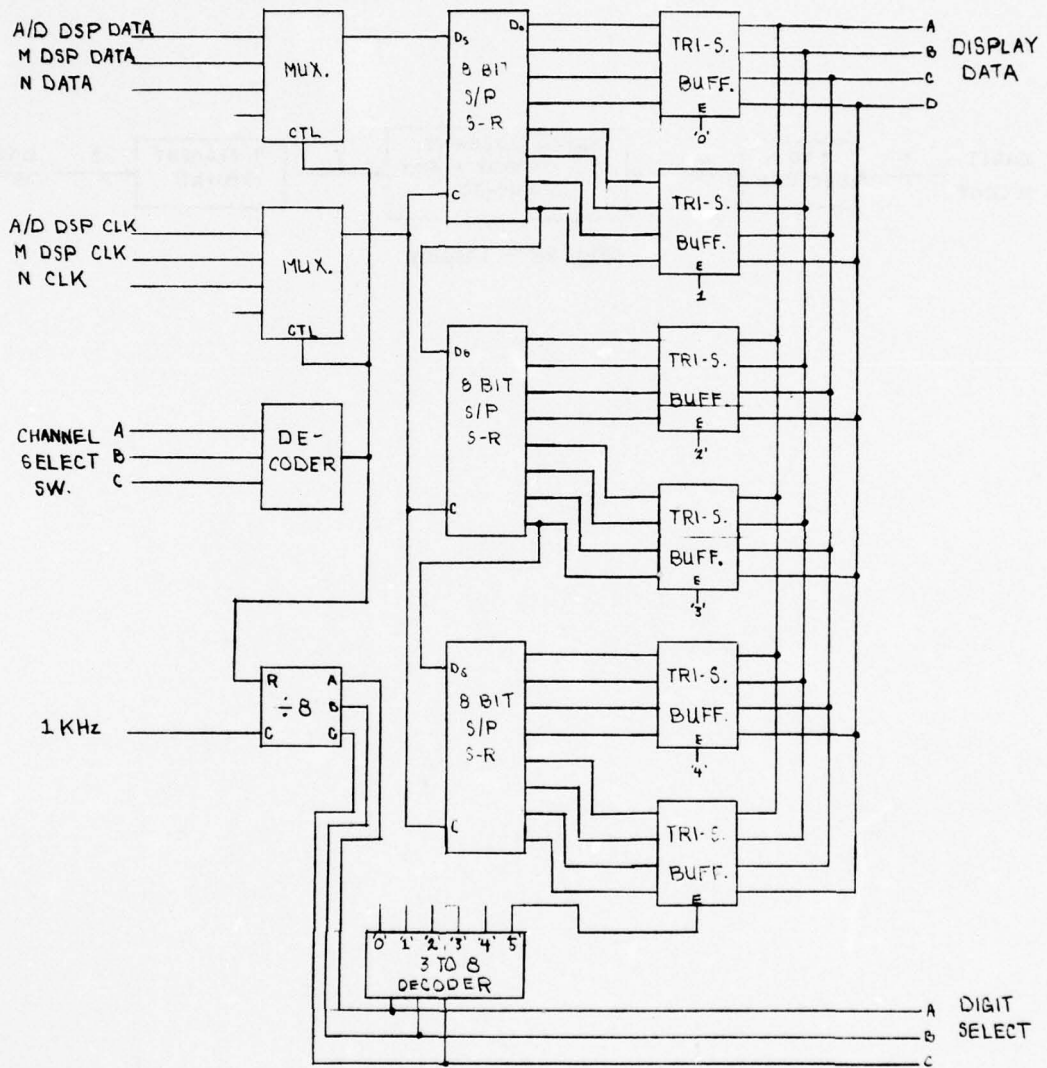


Fig. 27 - Display controller

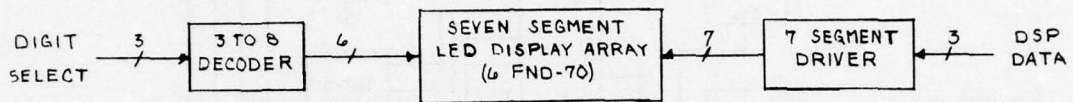


Fig. 28 - Display

In position 5 the counter is reset of 7 to enable all 6 displays. In position 6 the display is inhibited.

REFERENCES

1. R. R. Zirm, R. E. Brescia, and C. Morris, "Transionospheric Differential Delay Measurements from Timation II at 150 MHz and 400 MHz", NRL Report 7419, Aug. 24, 1972.
2. R. R. Zirm and J. M. Goodman, "Propagation Effects Observed in Connection with NTS-1 Observations Near the Magnetic Equator." Advisory Group for Aerospace Research and Development, AGARD-CPP-209.

Appendix
SCHEMATIC DIAGRAMS

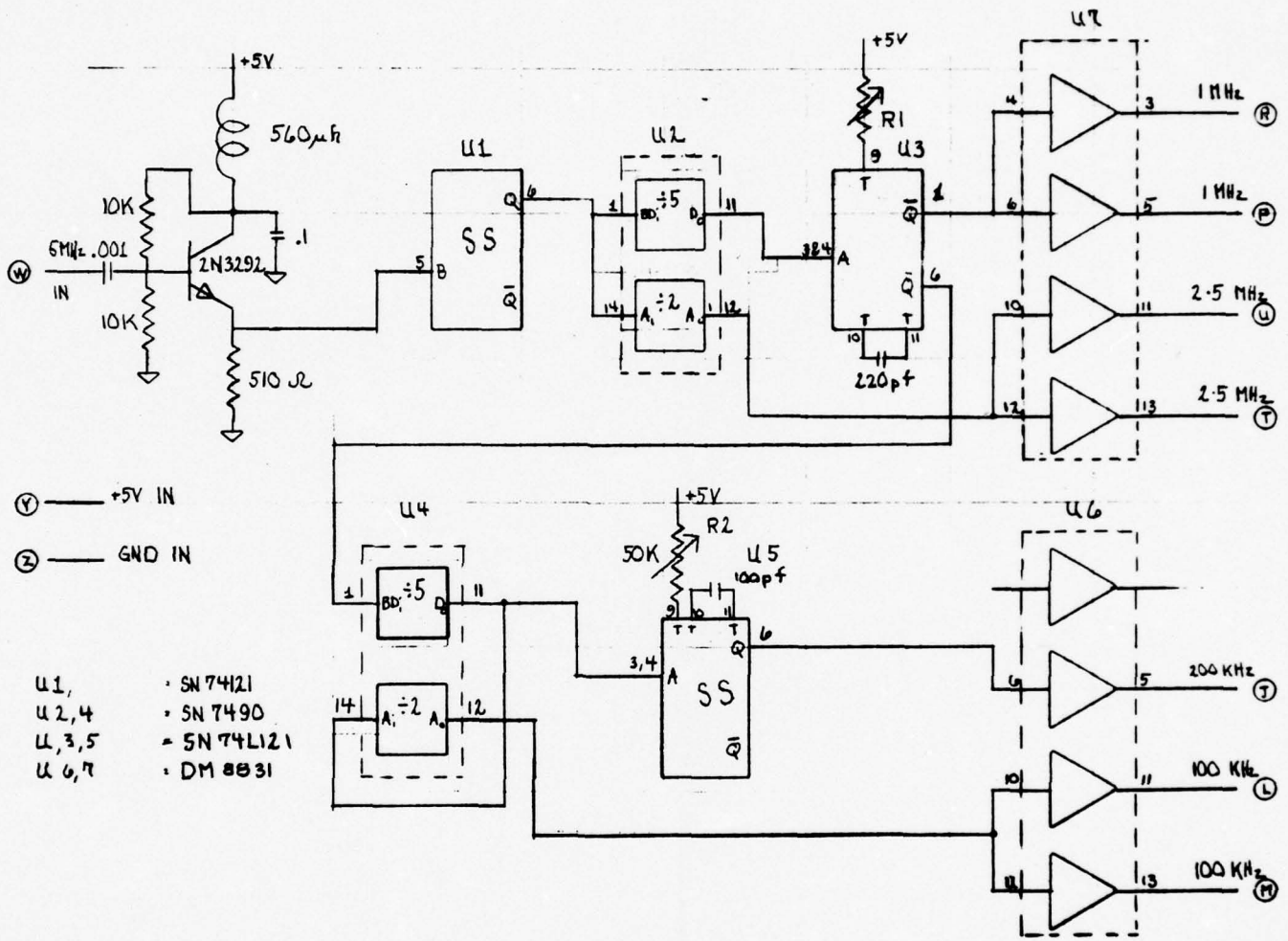


Fig. A-1 — L.O. generator D-1

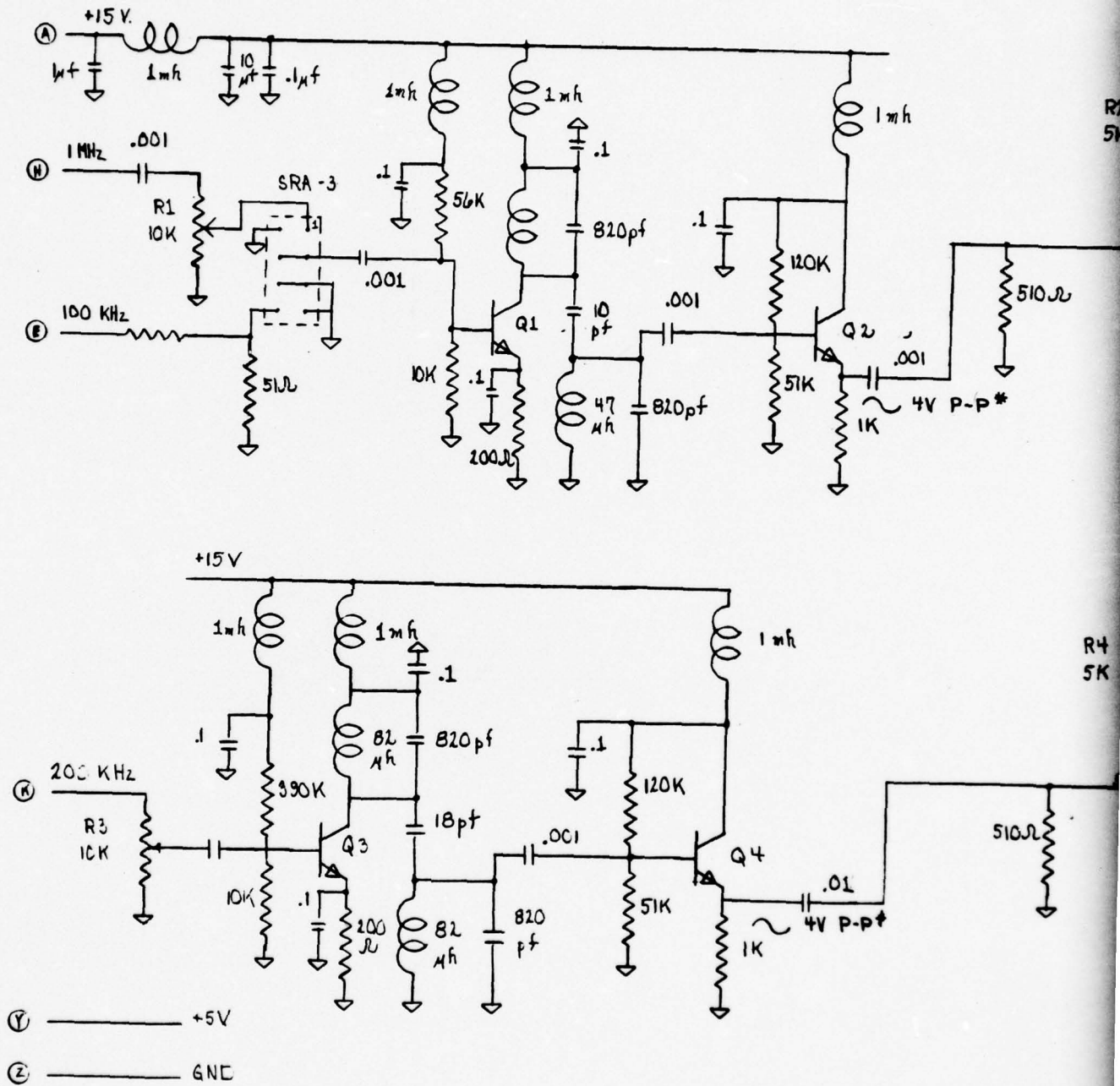
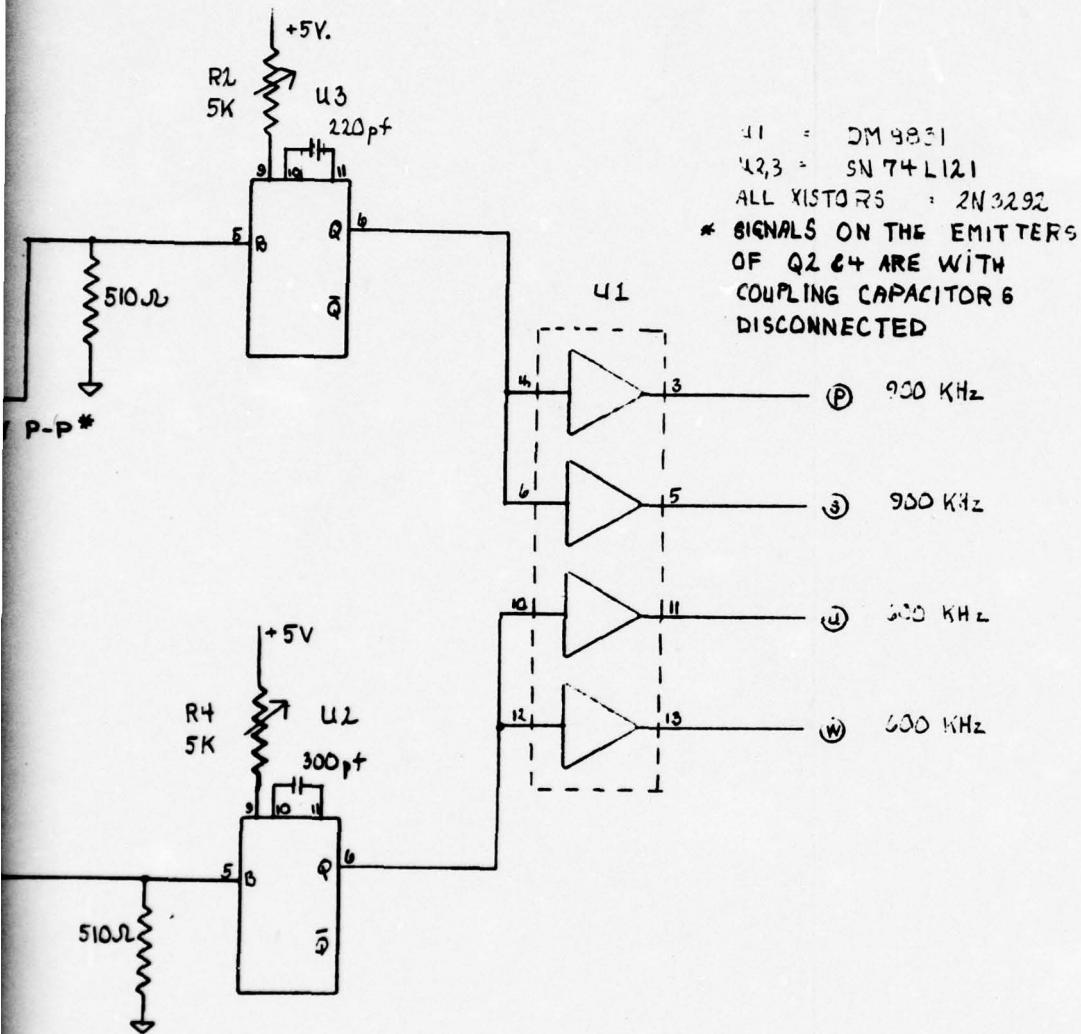


Fig. A-2 - L.O. generator D-2



U1 = DM 4851
 U2,3 = SN 74L121
 ALL XISTORS = 2N3292
 * SIGNALS ON THE EMITTERS
 OF Q2 & 4 ARE WITH
 COUPLING CAPACITOR 6
 DISCONNECTED

generator D-2

(blank)

2

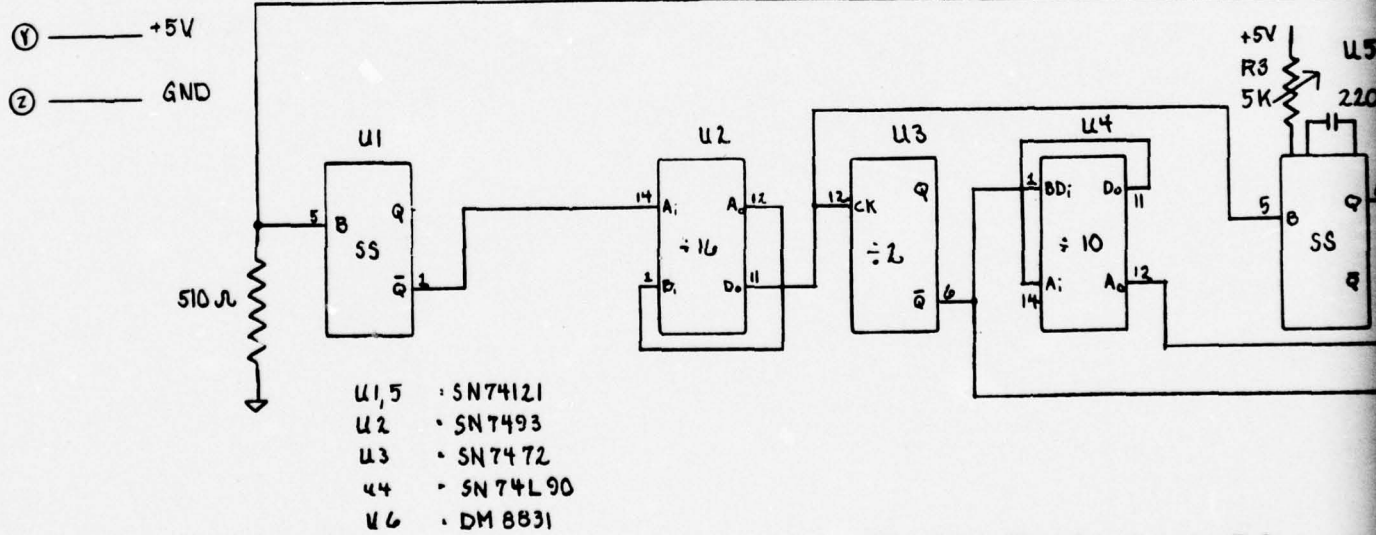
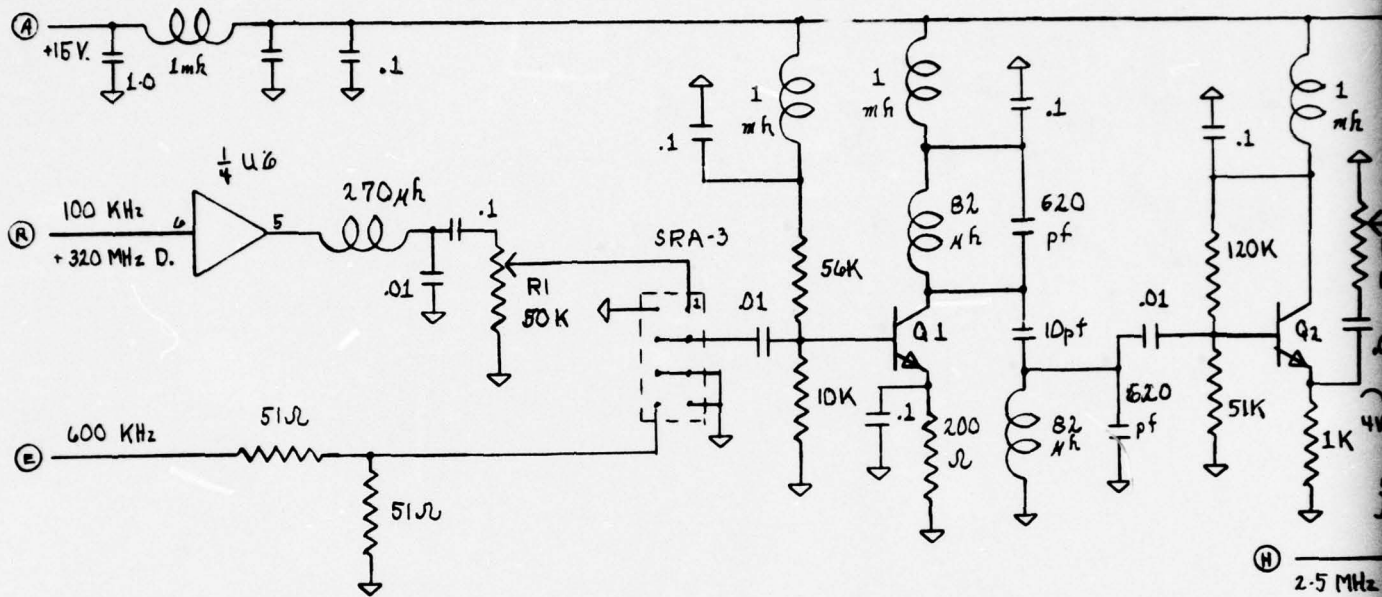
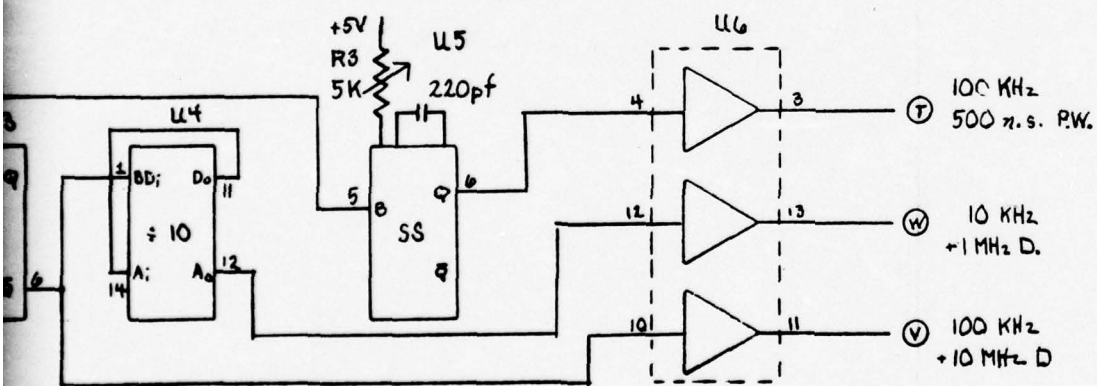
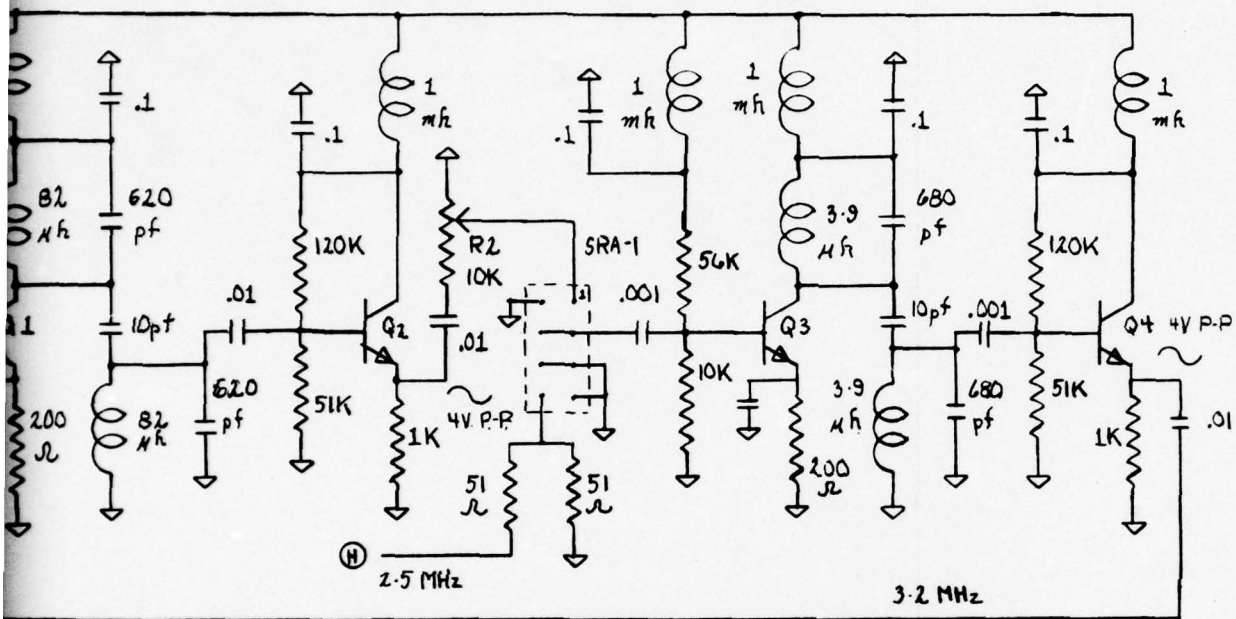
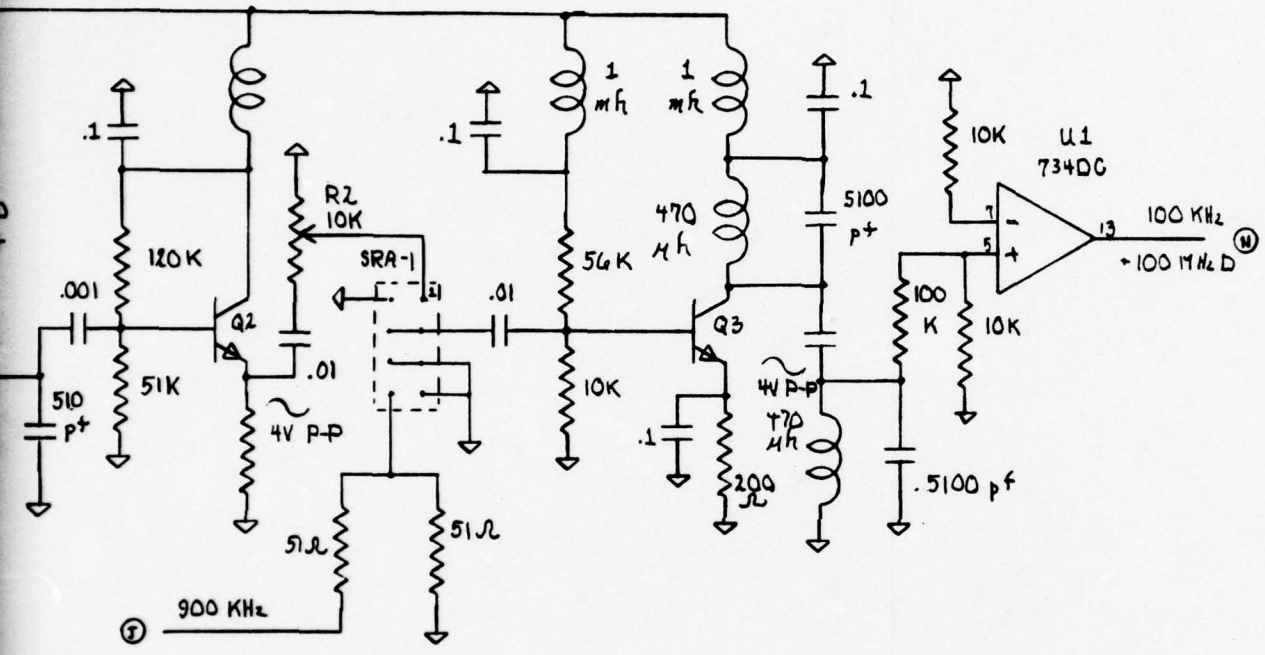


Fig. A-3 — Doppler converter D-3



A-3 - Doppler converter D-3

2



A-4 - Doppler converter D-4

2

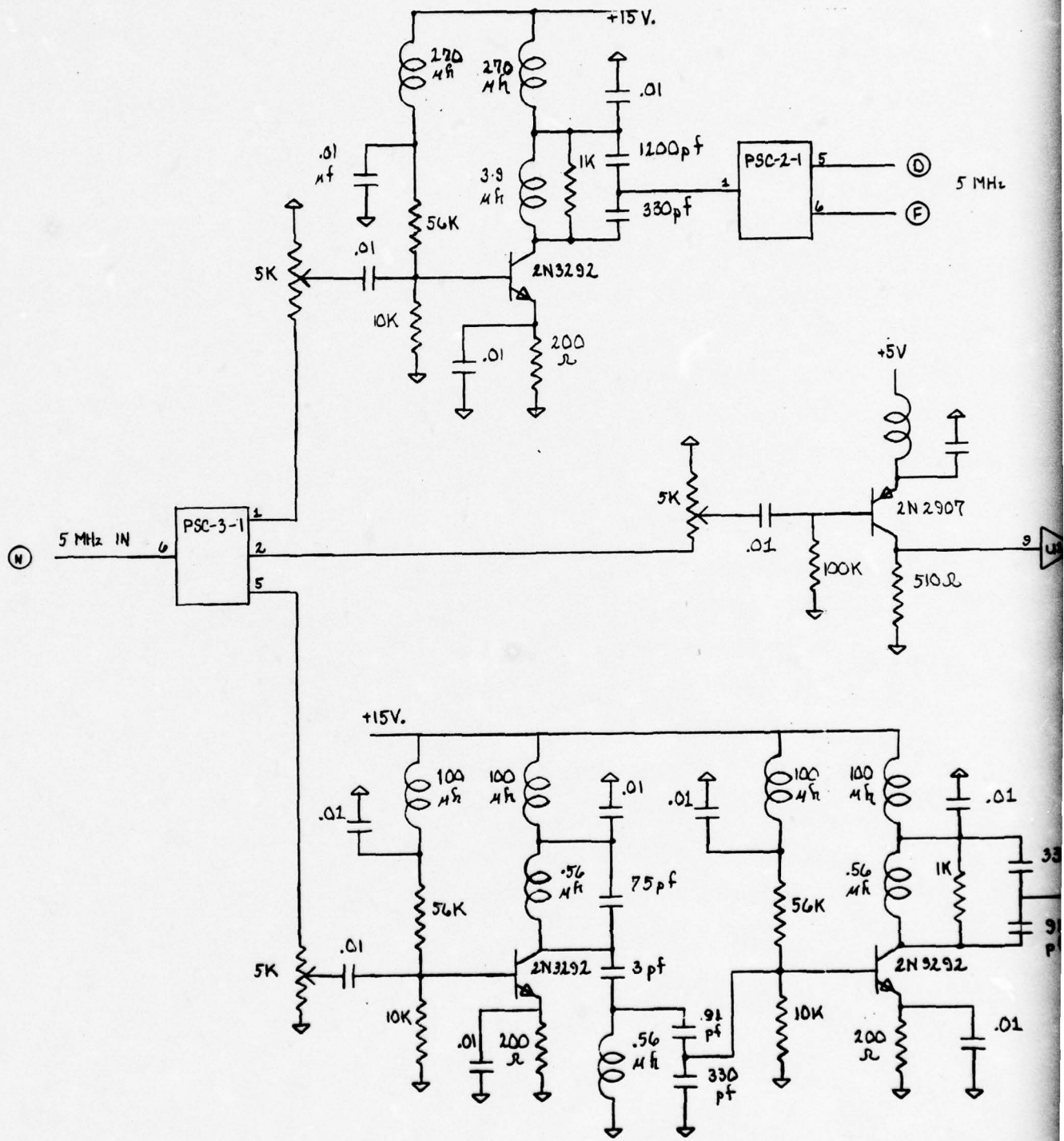


Fig. A-5 - L.O. generator R-1

U1 = 5N7404
 U2 = 5N7473
 U3,4 = 5N7490
 U5 = 5N7412B

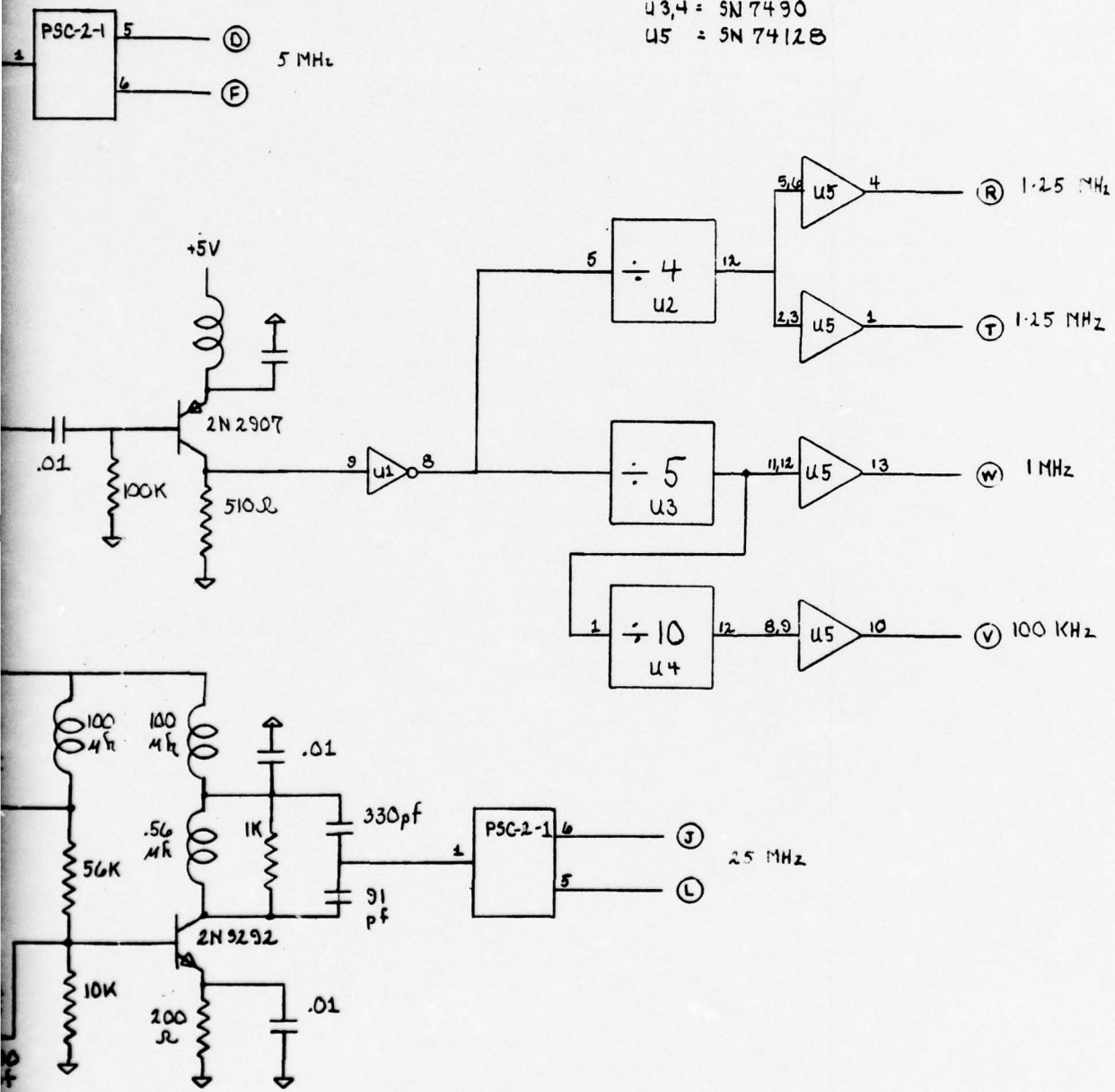


Fig. A-5 - L.O. generator R-1

2

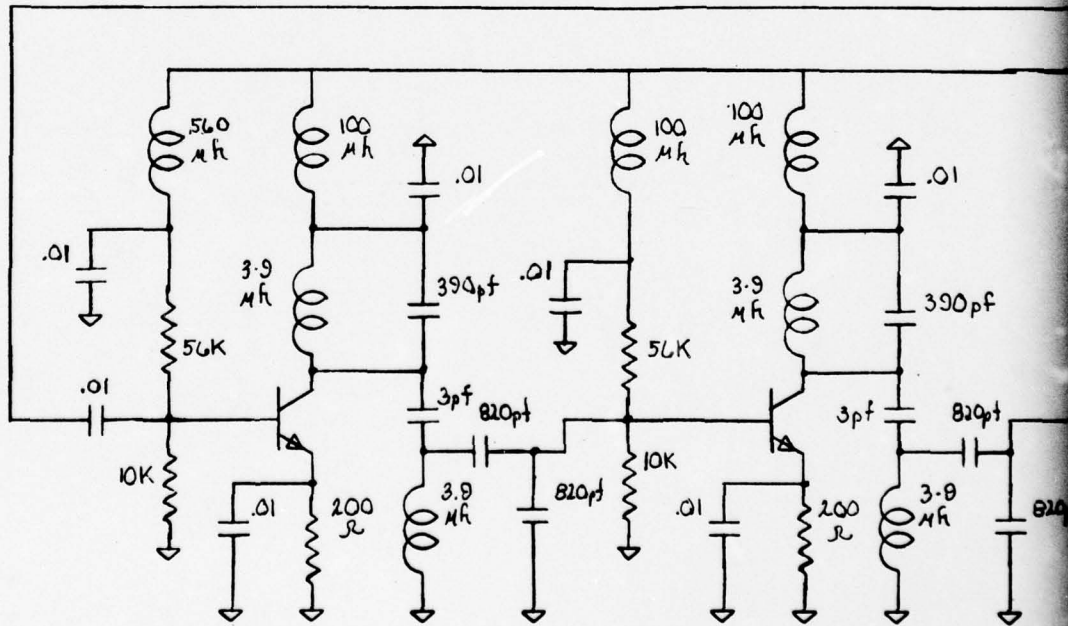
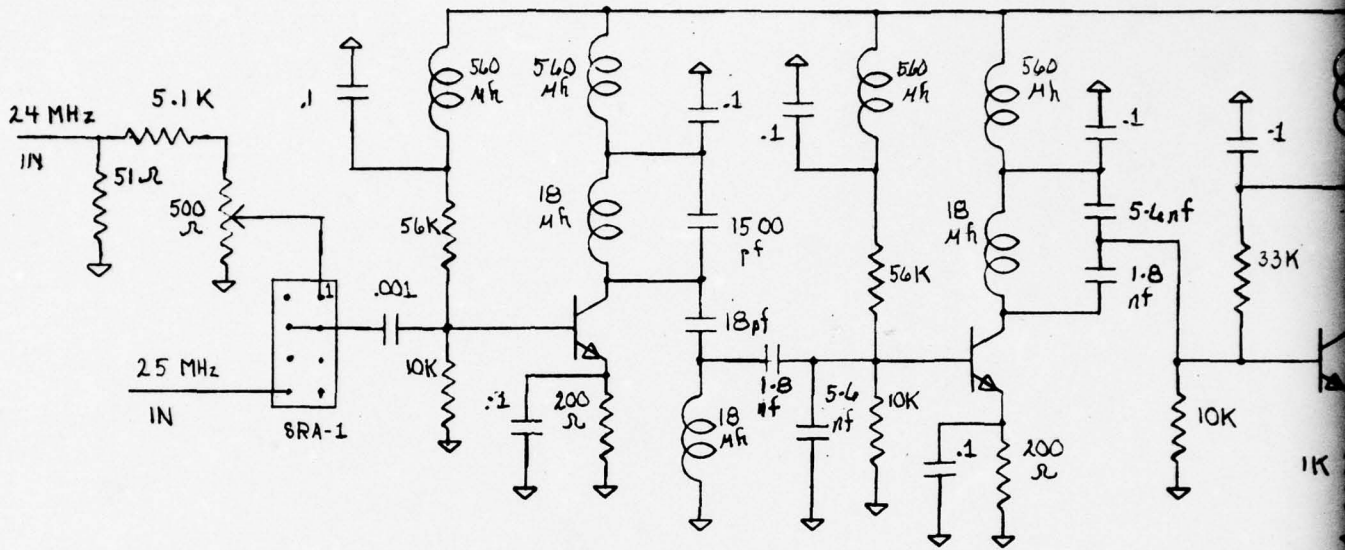
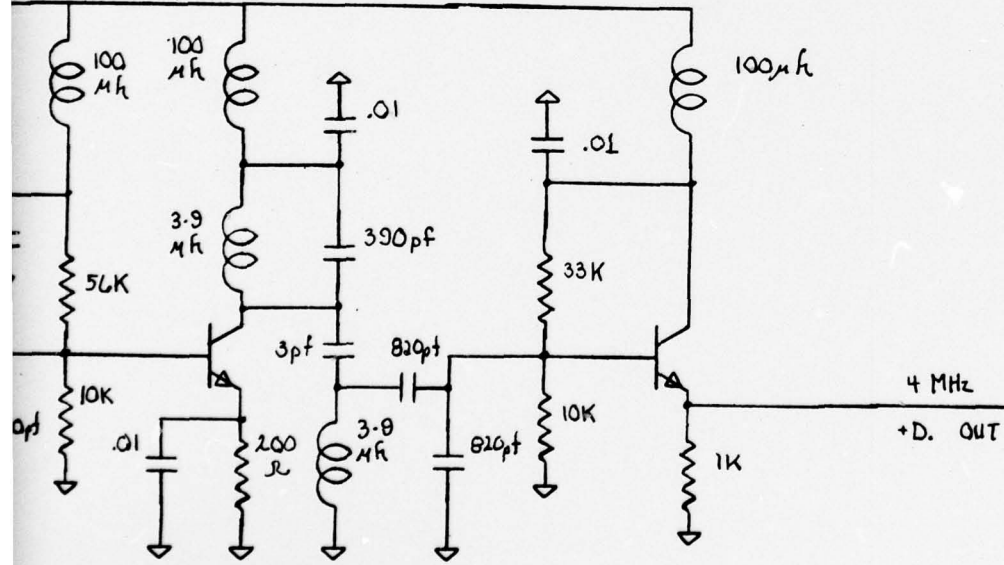
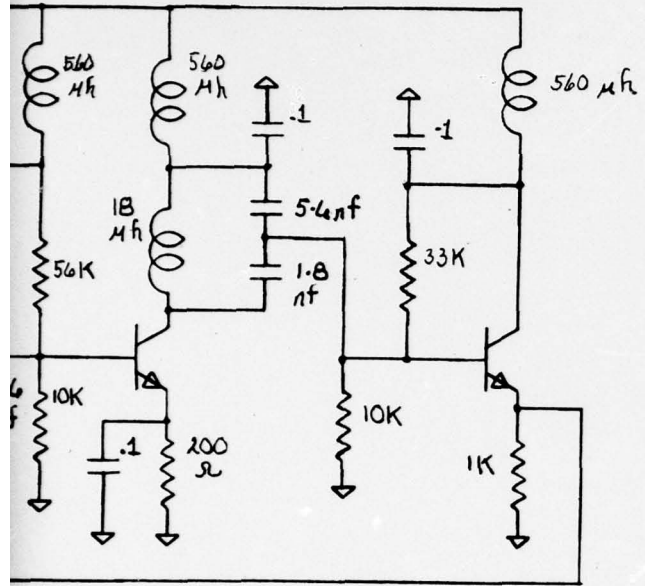


Fig. A-6 - Doppler converter R-2

ALL XISTORS-2N3292



Doppler converter R-2

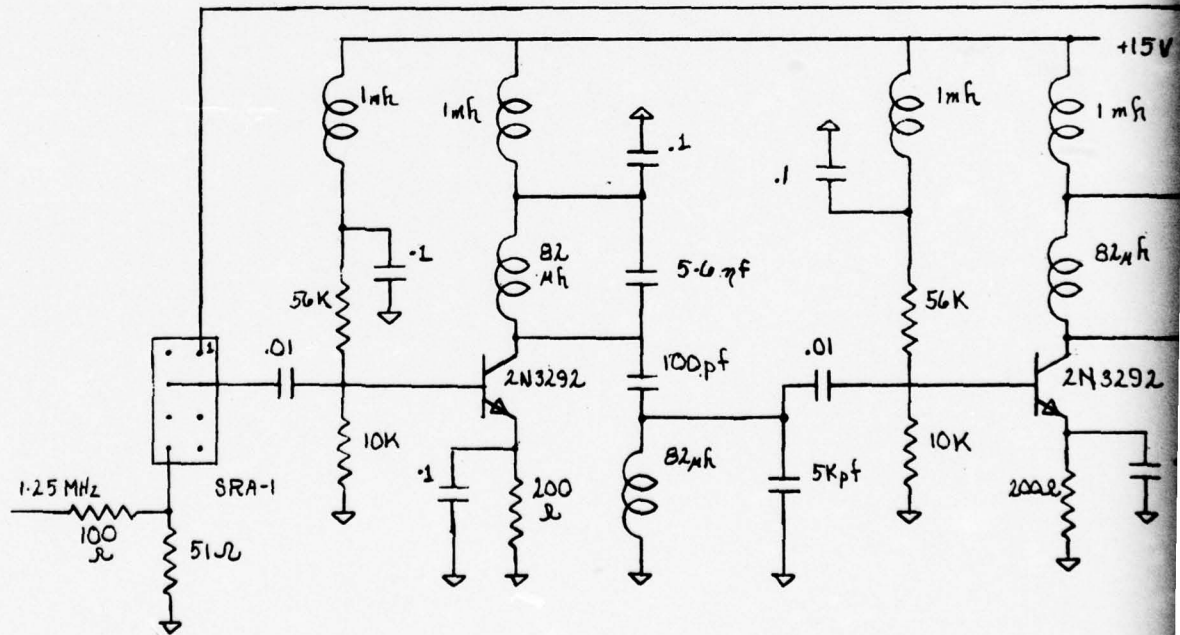
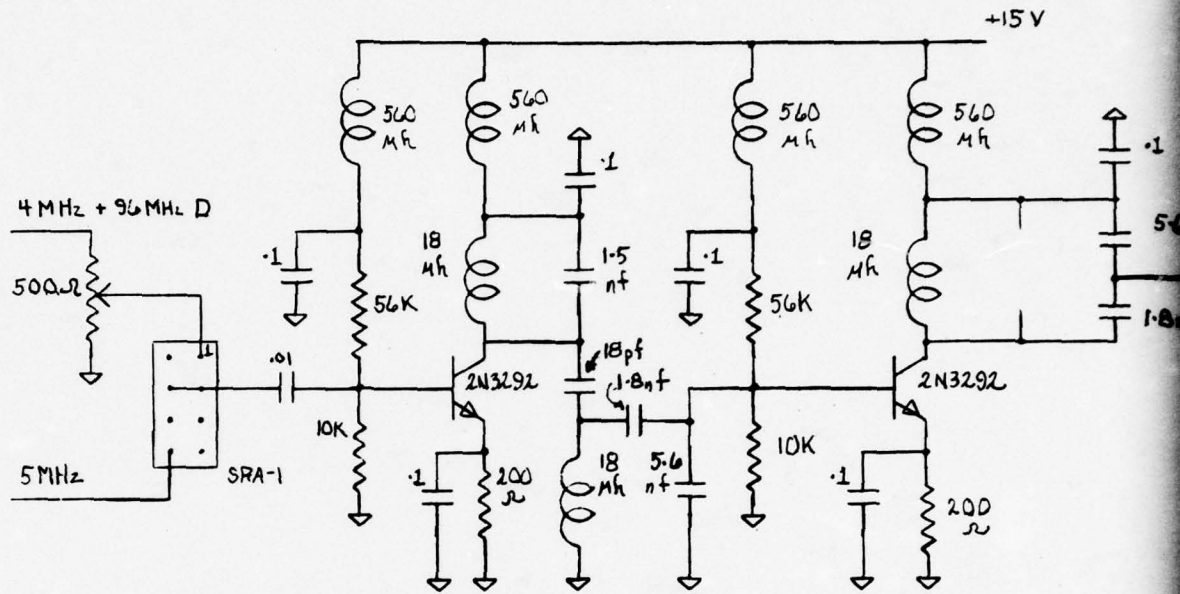


Fig. A-7 - Doppler converter R-3

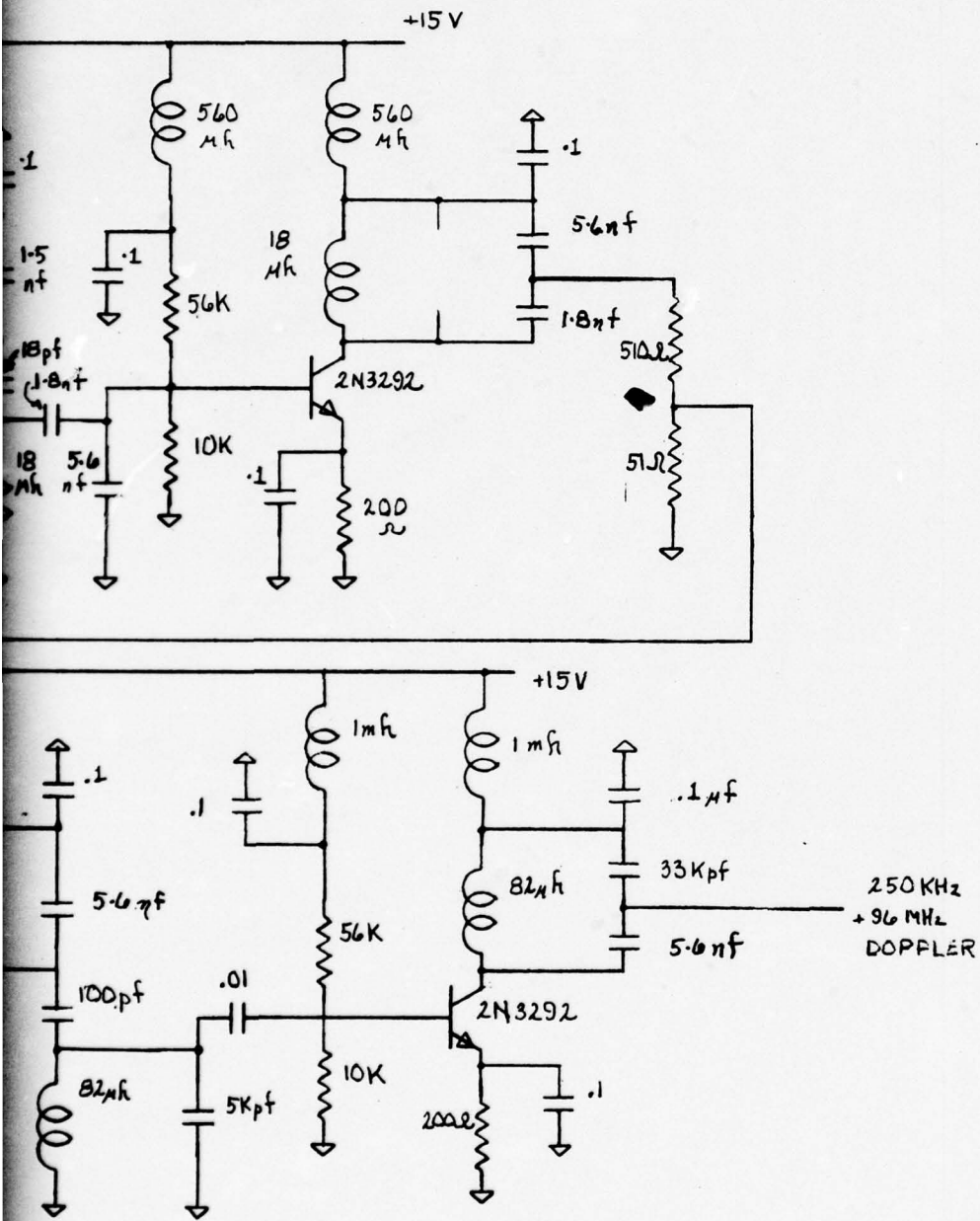


Fig. A-7 - Doppler converter R-3

2

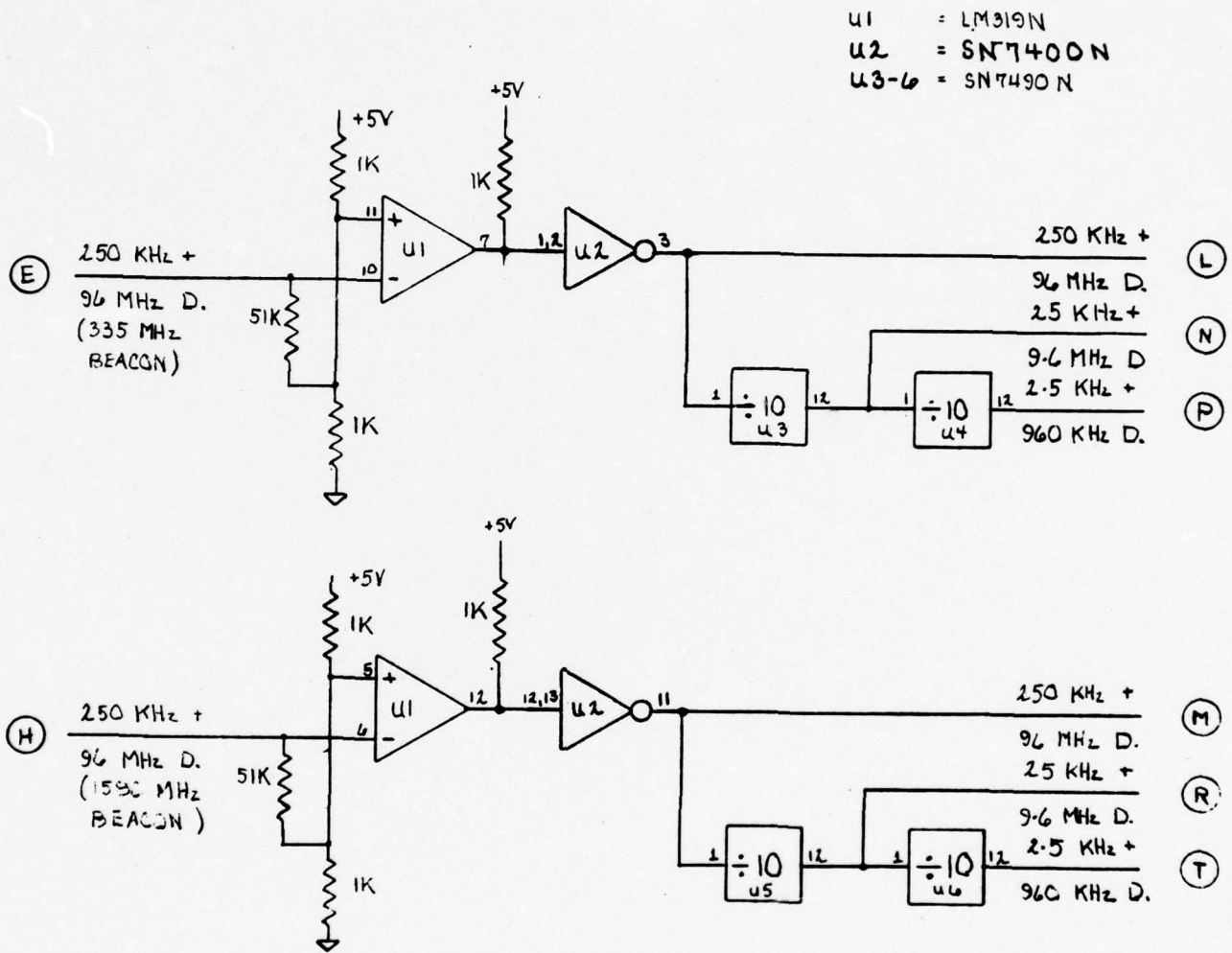


Fig. A-8 — Doppler converter R-4

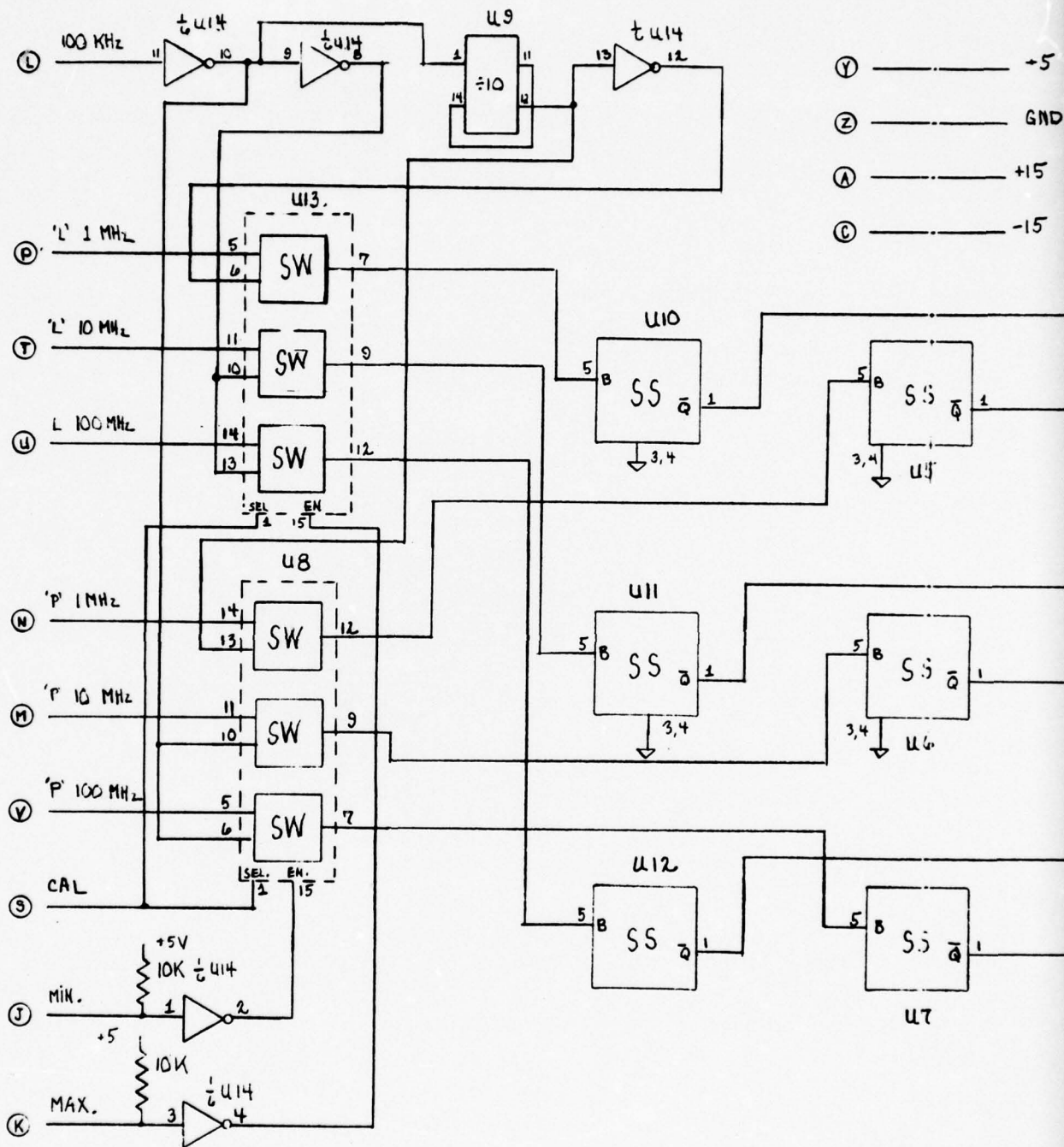


Fig. A-9 — Phase meters B-5

- ① ————— +5
- ② ————— GND
- ③ ————— +15
- ④ ————— -15

- U1, 2, 3, = SN7472
- U4, 14 = SN7404
- U5, 6, 7, 10, 11, 12 = SN74L121
- U8, 13 = SN74157
- U9 = SN7490
- U15, 16, 17 = 741 TC

74157's A' INPUTS
= DATA
'B' INPUTS
= CAL

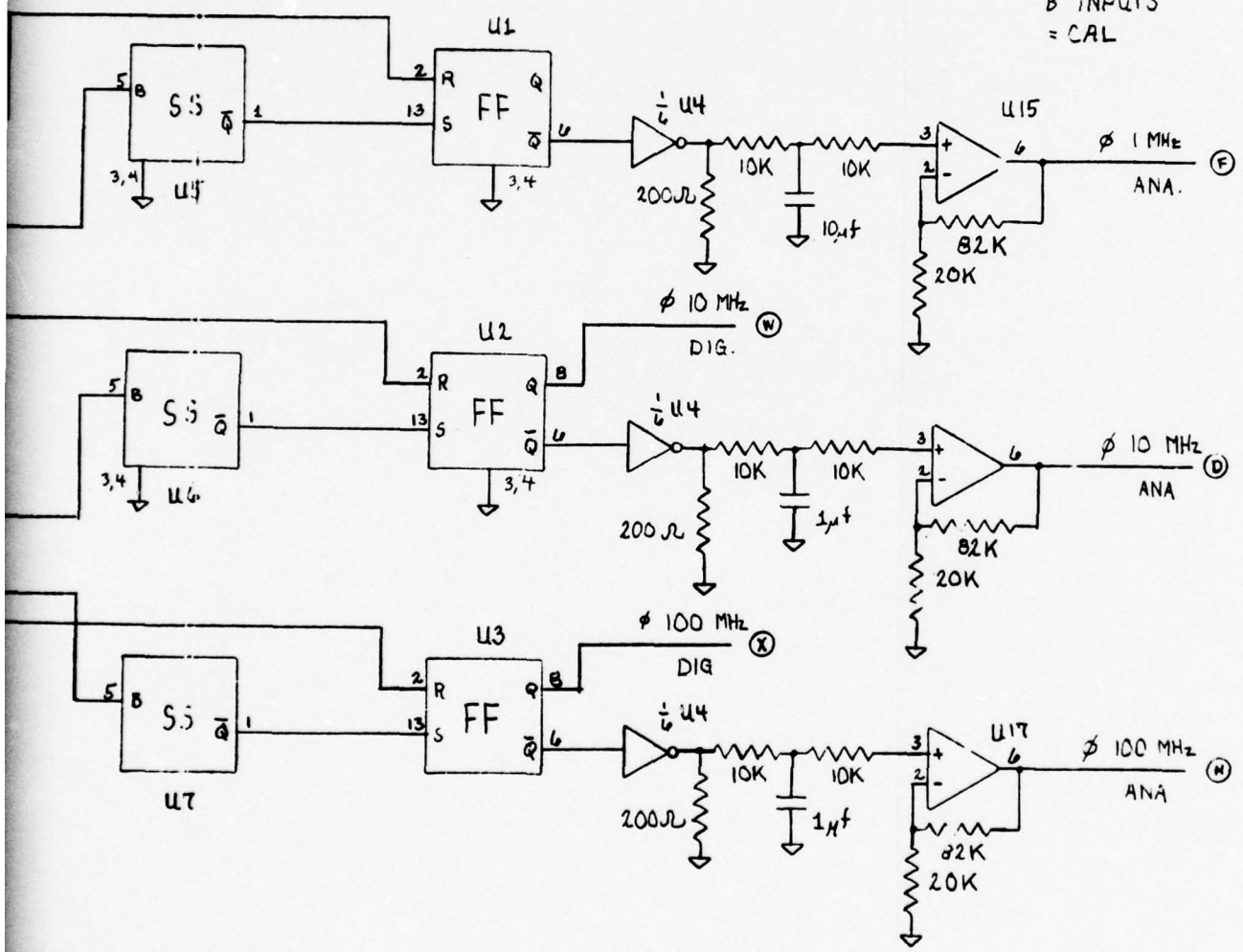


Fig. A-9 — Phase meters B-5

2

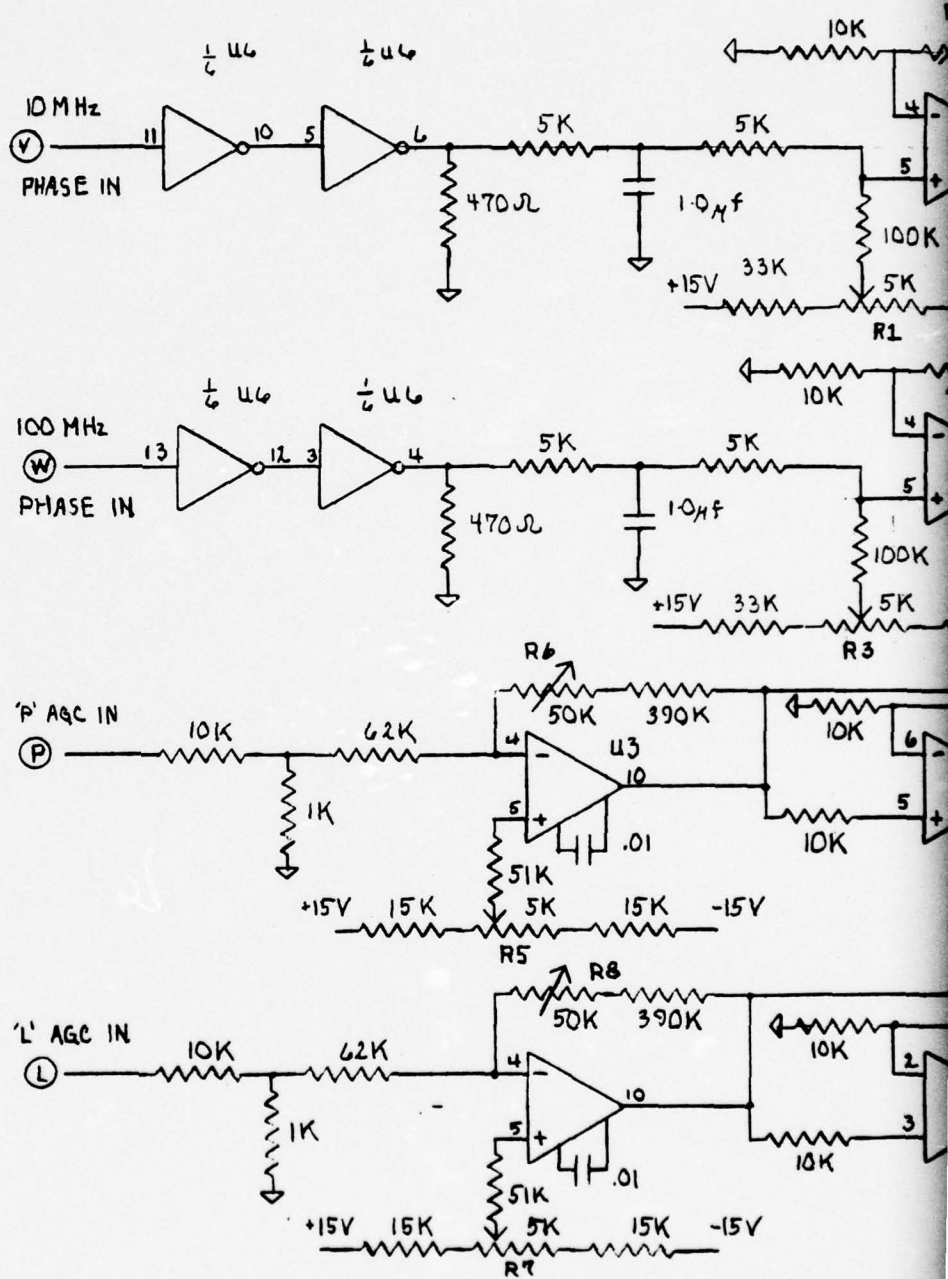
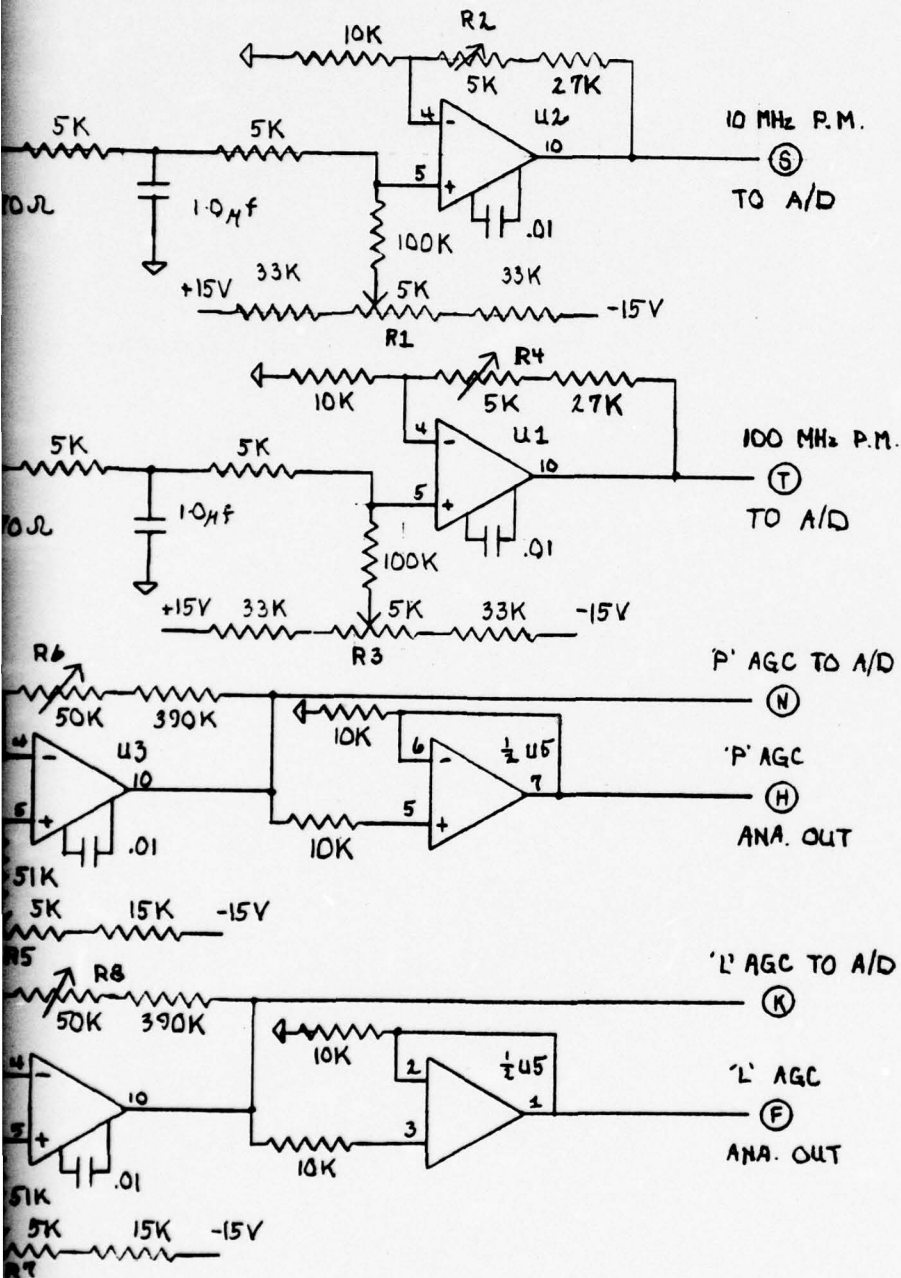


Fig. A-10 - Amplifiers B-6



U1-4 = 777DM
 U5 = MC1458
 U6 = SN 7404

Fig. A-10 - Amplifiers B-6

2

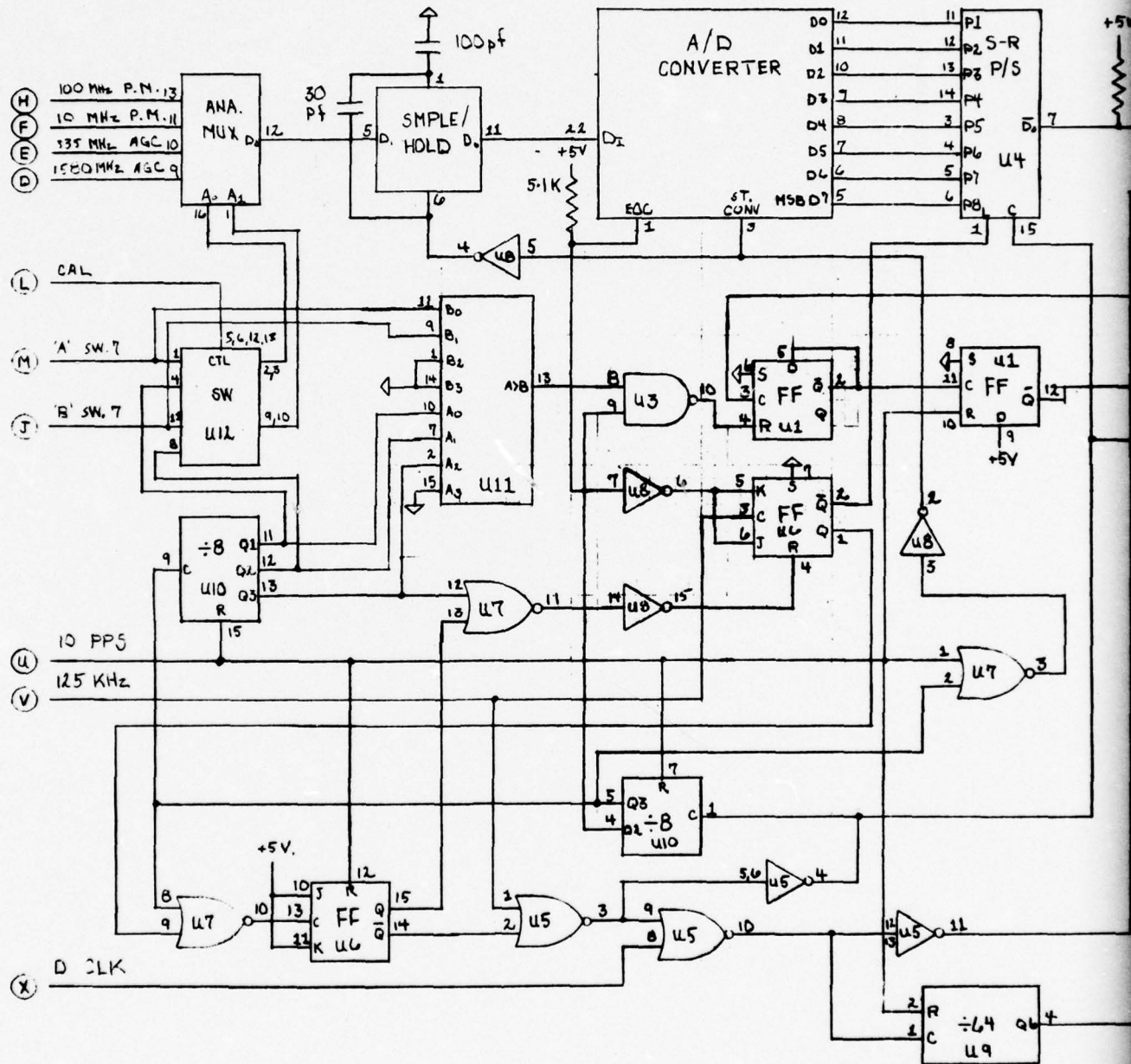
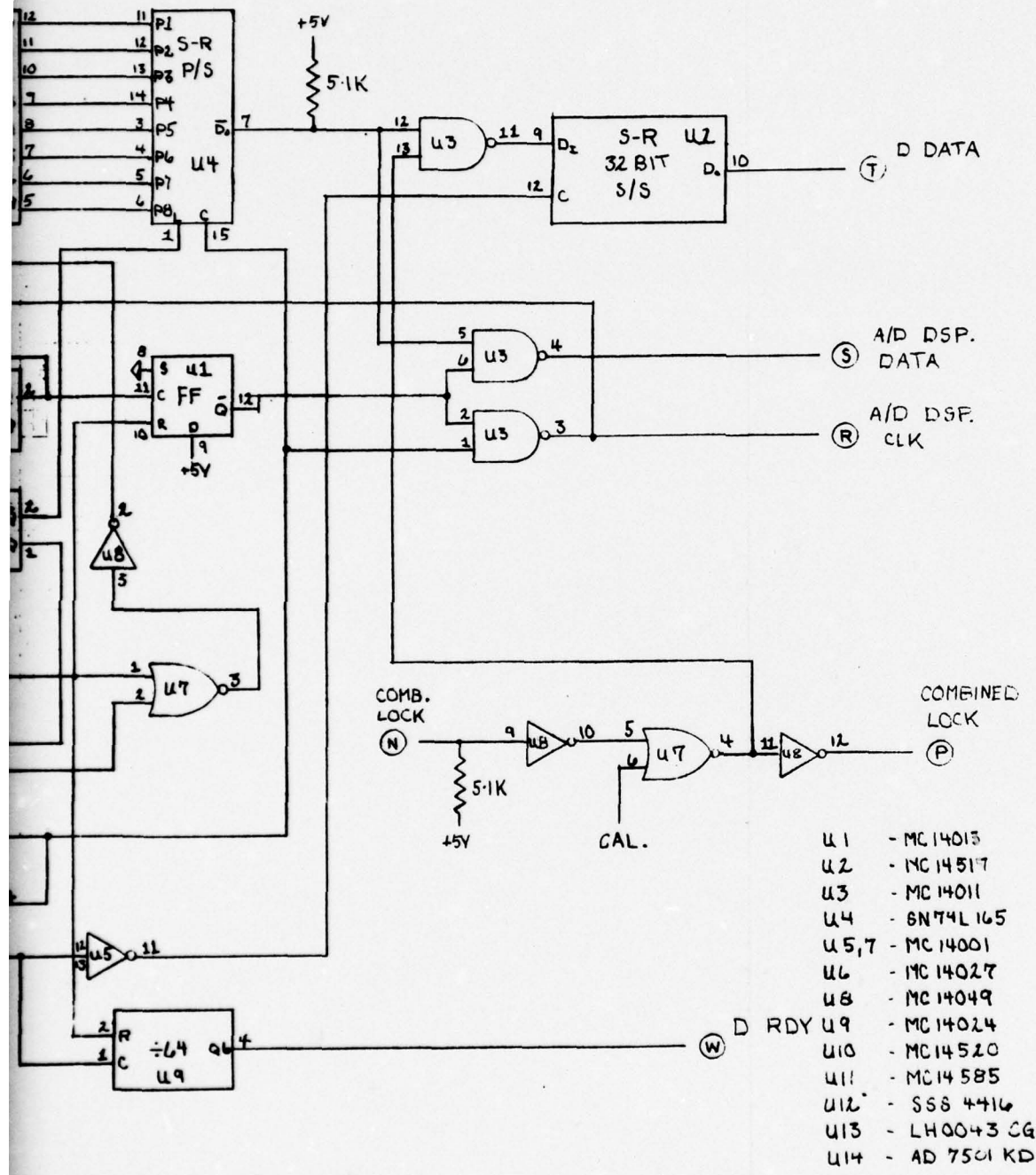


Fig. A-11 — A/D converter B-7



- U1 - MC14013
- U2 - MC14517
- U3 - MC14011
- U4 - 8N74L165
- U5,7 - MC14001
- U6,7 - MC14027
- U8 - MC14049
- U9 - MC14024
- U10 - MC14520
- U11 - MC14585
- U12 - S58 4416
- U13 - LH0043 CG
- U14 - AD 7501 KD

11 - A/D converter B-7

2

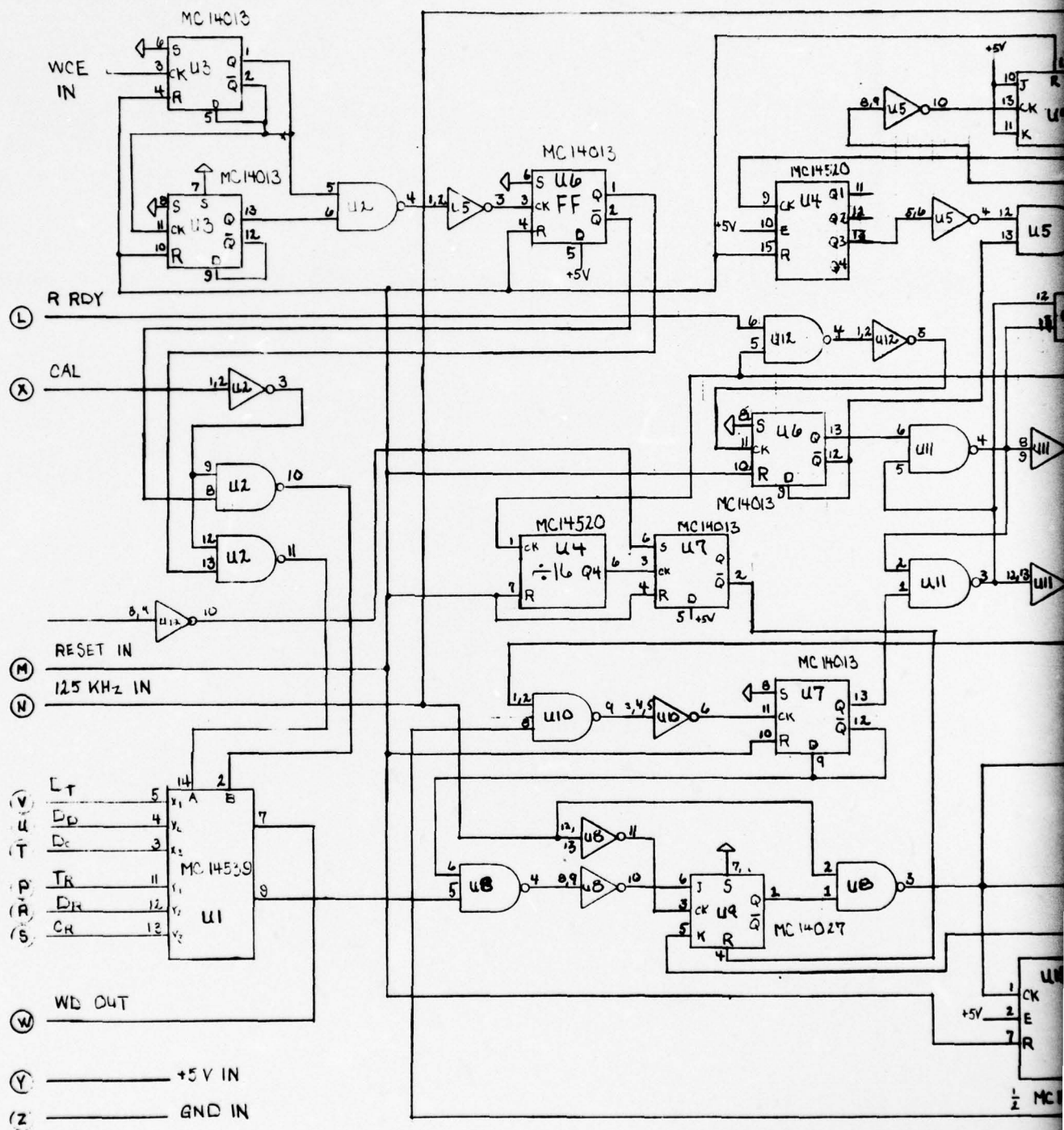
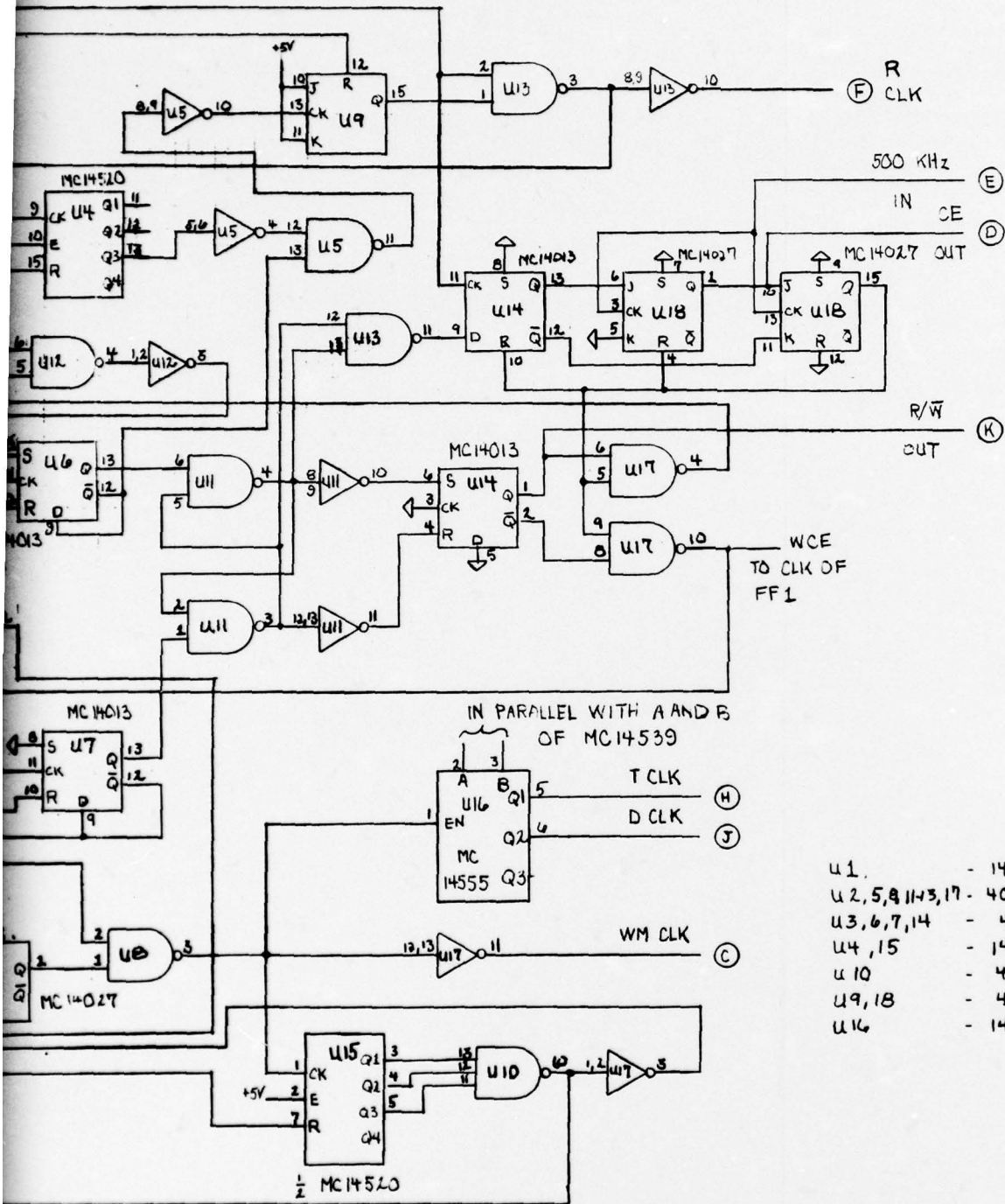


Fig. A-12 — Memory controller B-8



- U1 - 14539
- U2, 5, 8, 11, 13, 17 - 4011
- U3, 6, 7, 14 - 4013
- U4, 15 - 14520
- U10 - 4023
- U9, 18 - 4027
- U16 - 14555

A-12 - Memory controller B-8

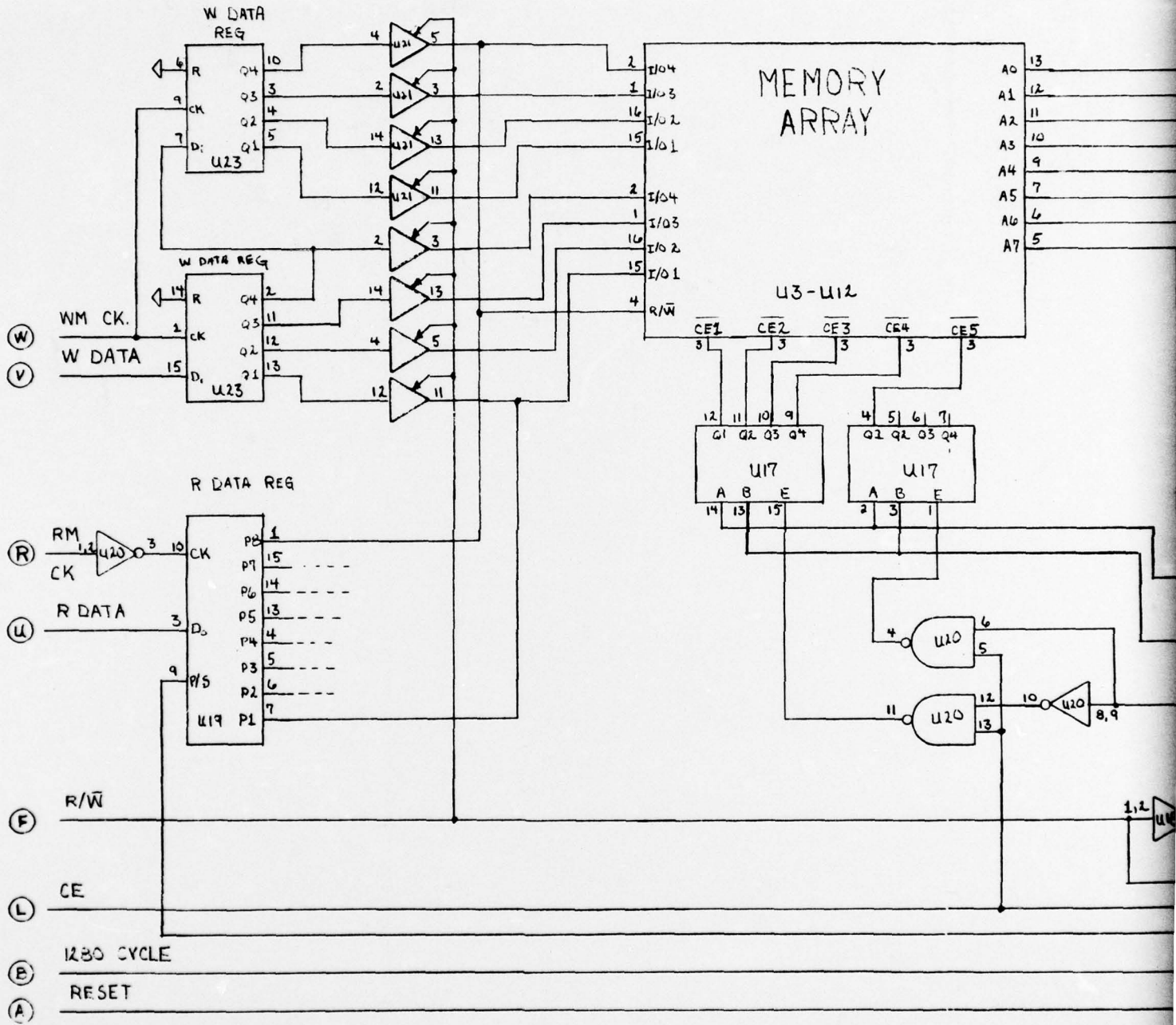
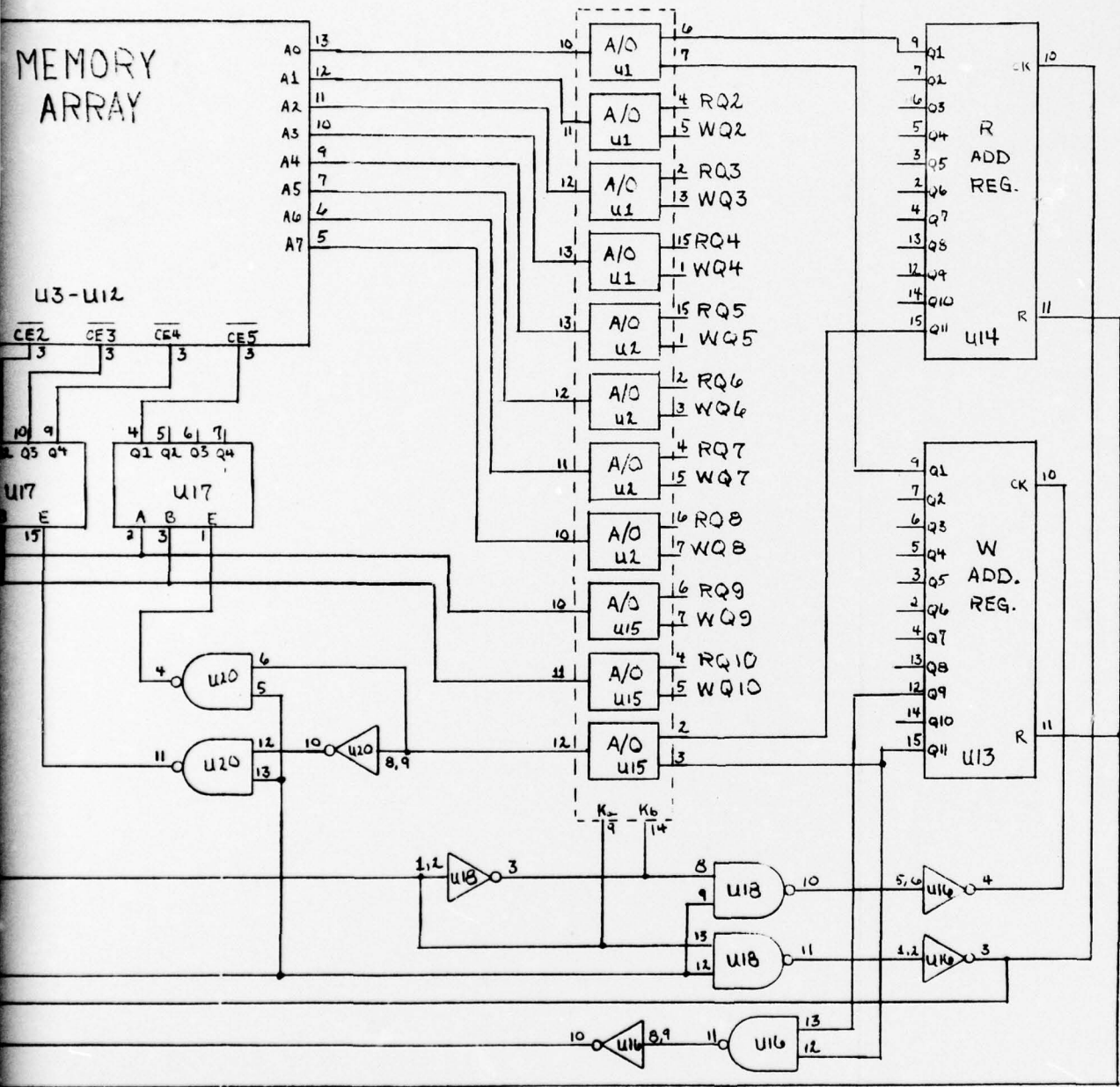


Fig. A-13 - Buffer memory B-9



- U1-2, 15 - 4014
- U3-12 - 2000
- U13-14 - 4040
- U16, 18, 20 - 4011
- U17 - 14556
- U19 - 4021
- U21-22 - 80075
- U23 - 4015

Fig. A-13 - Buffer memory B-9

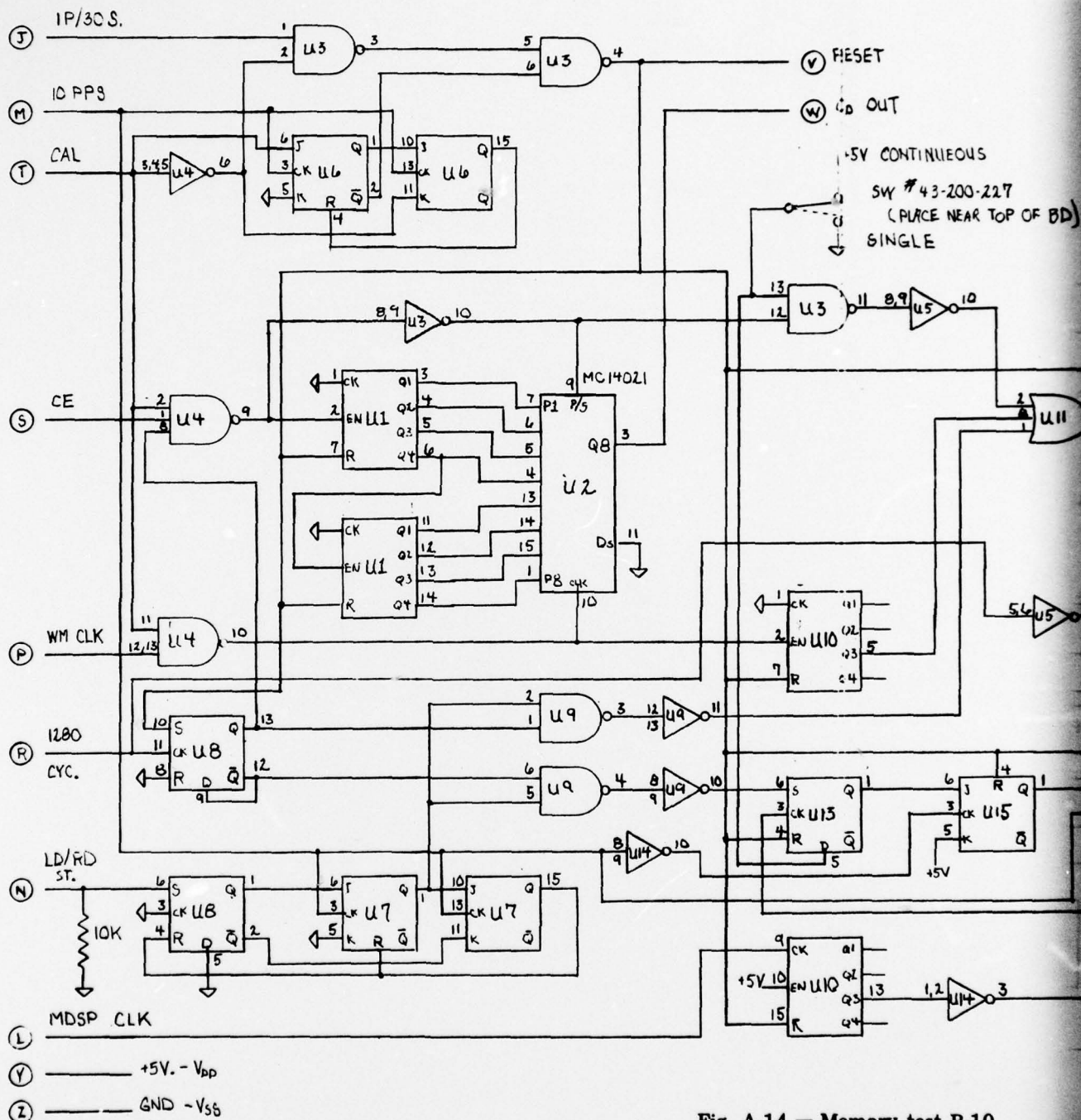


Fig. A-14 - Memory test B-10

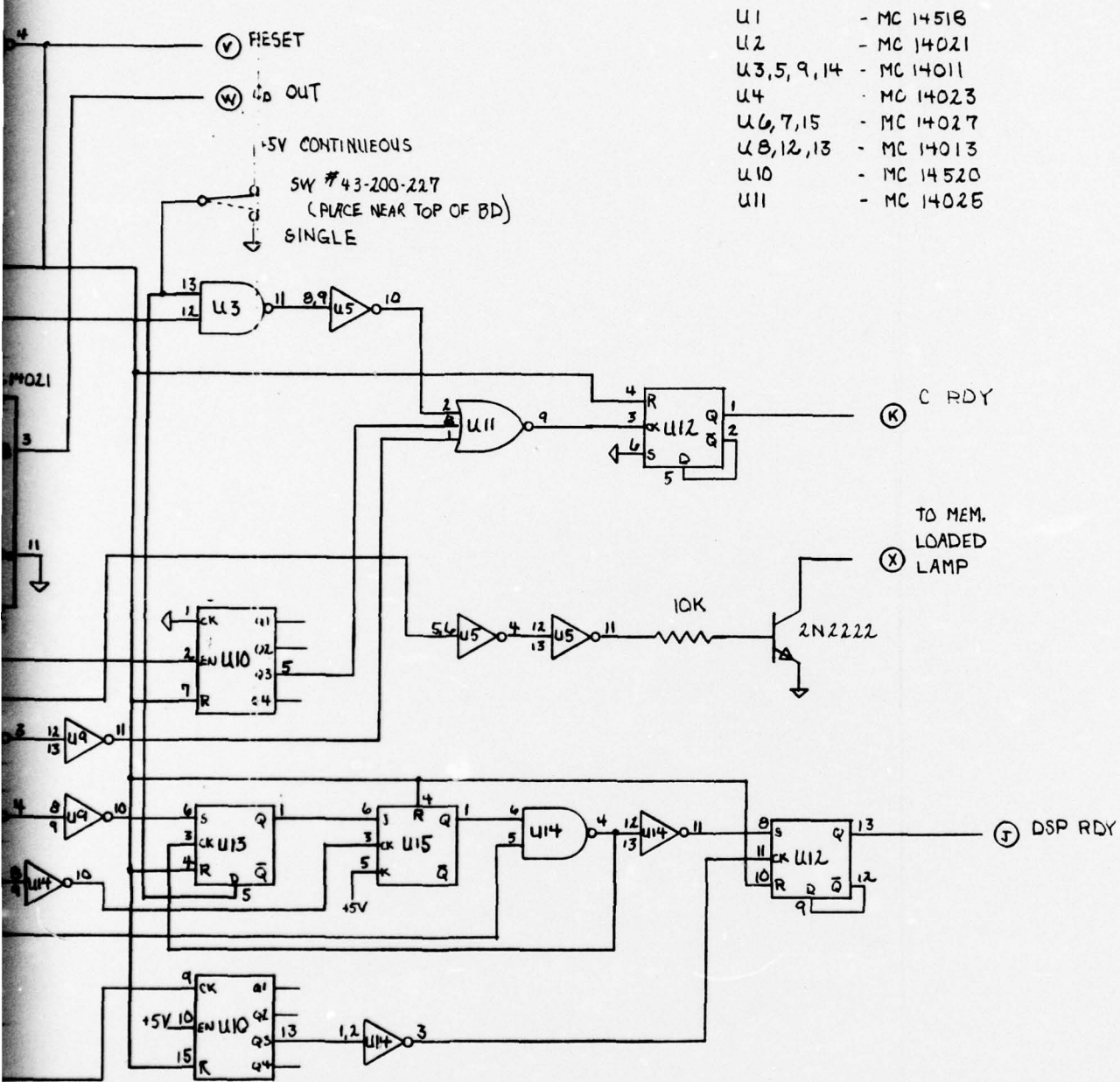


Fig. A-14 - Memory test B-10

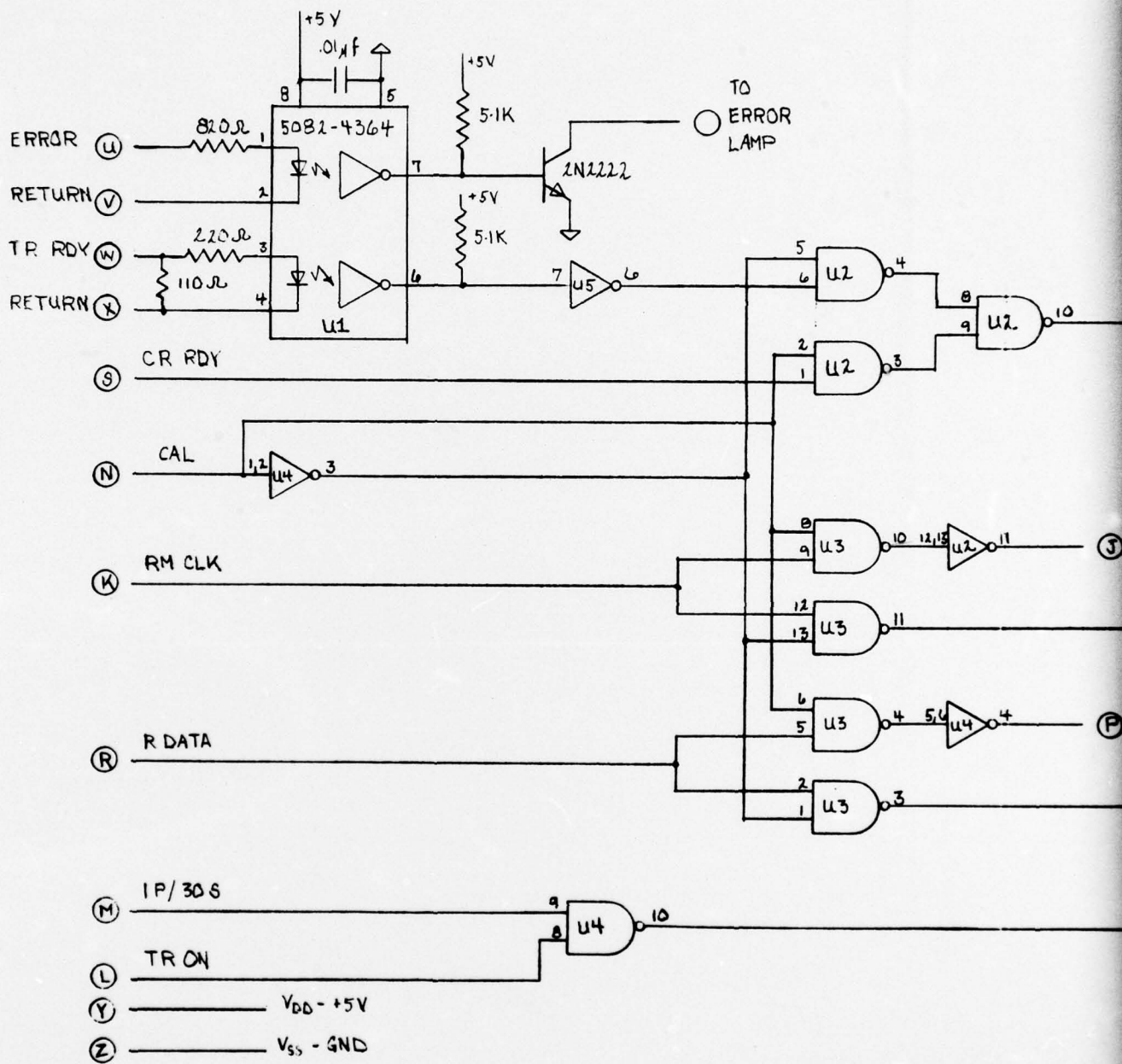


Fig. A-15 - TR interface B-11

TO
ERROR
LAMP

- U1 - 5082-4364
- U2,3,4 - MC14011
- U5 - MC 14049
- U6,7 - DM8331

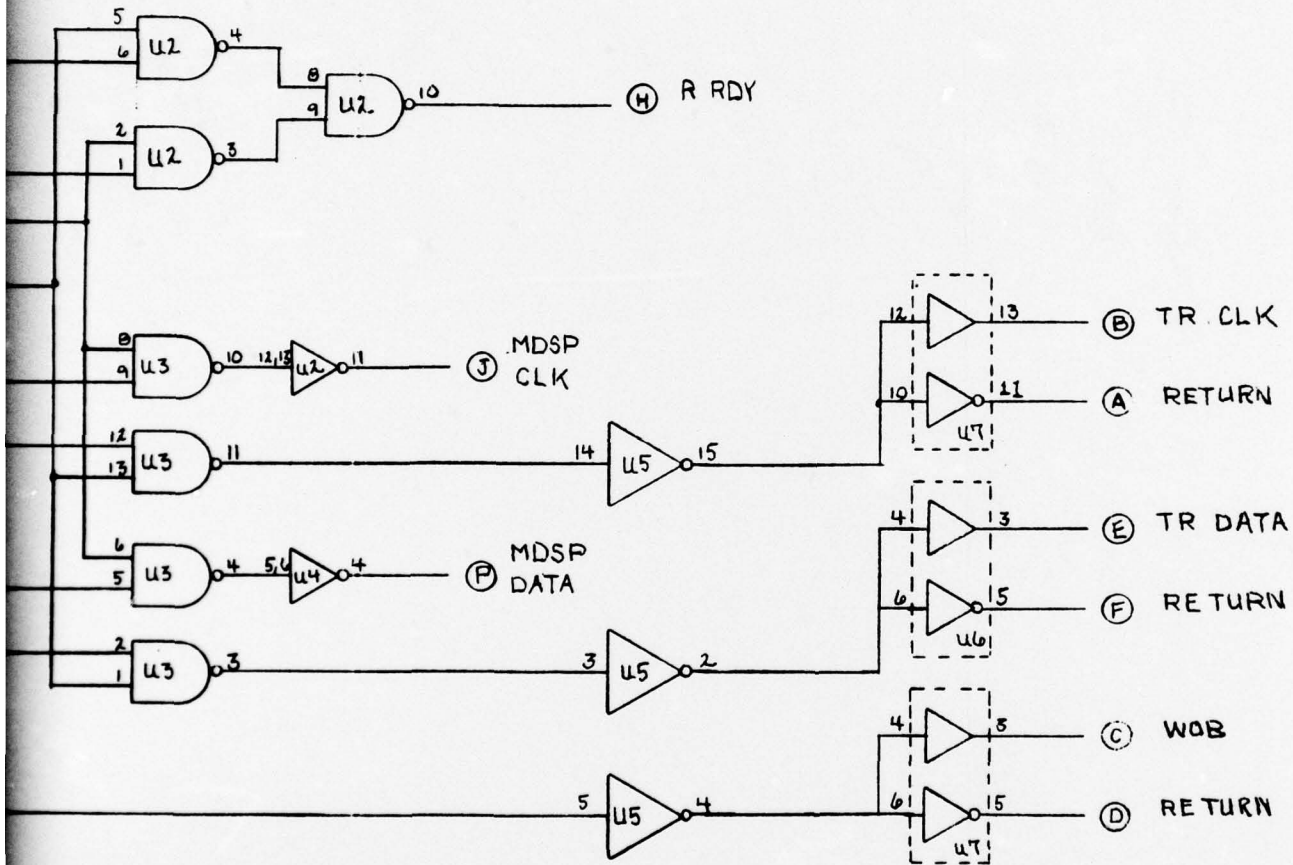
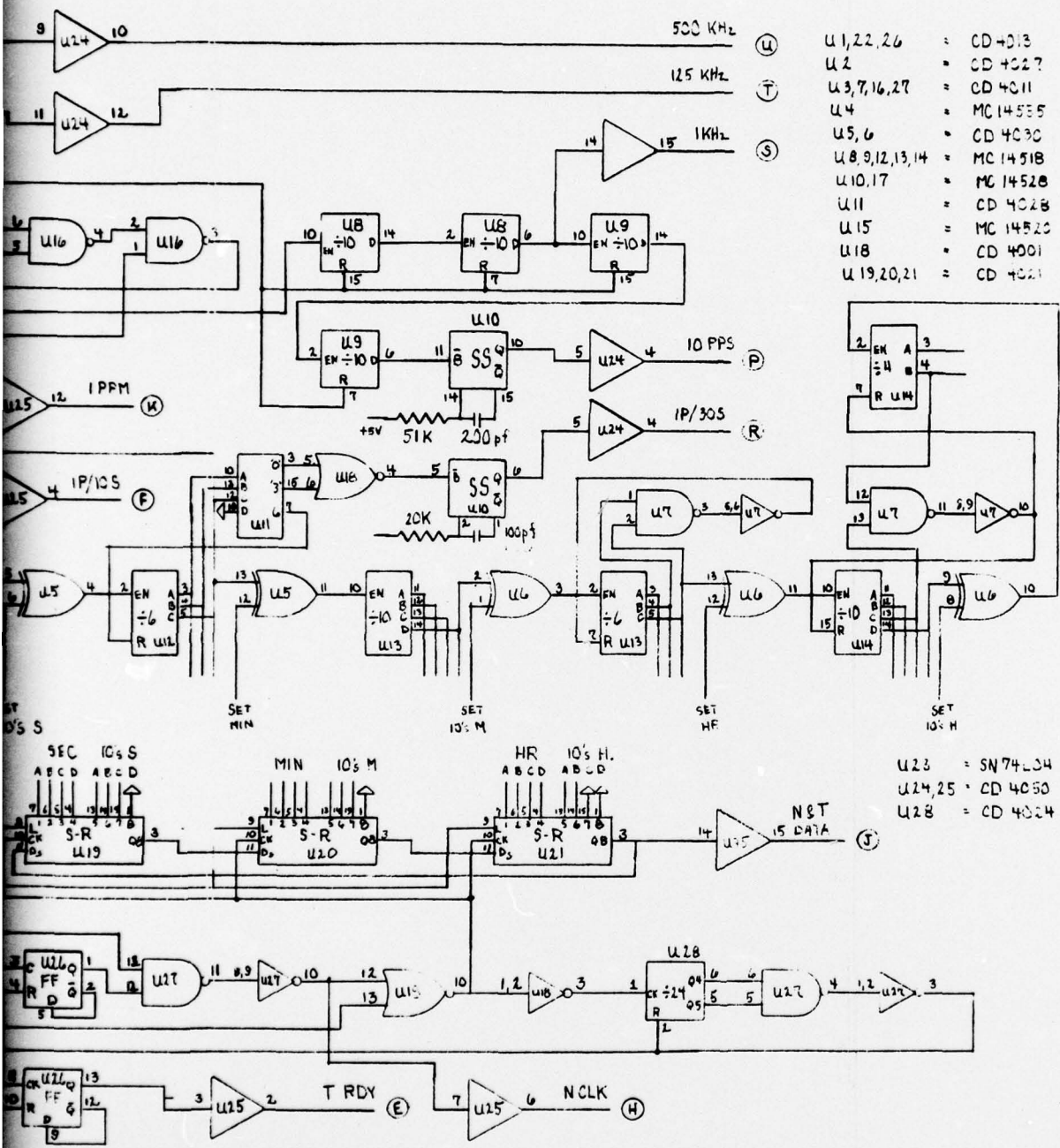


Fig. A-15 - TR interface B-11

9



- U 1,22,26 = CD 4013
- U 2 = CD 4027
- U 3,7,16,27 = CD 4011
- U 4 = MC 14555
- U 5,6 = CD 4030
- U 8,9,12,13,14 = MC 14518
- U 10,17 = MC 14528
- U 11 = CD 4028
- U 15 = MC 14520
- U 18 = CD 4001
- U 19,20,21 = CD 4021

- U23 = SN74LS4
- U24,25 = CD 4050
- U28 = CD 4024

A-16 - Clock and timing generator B-12

2

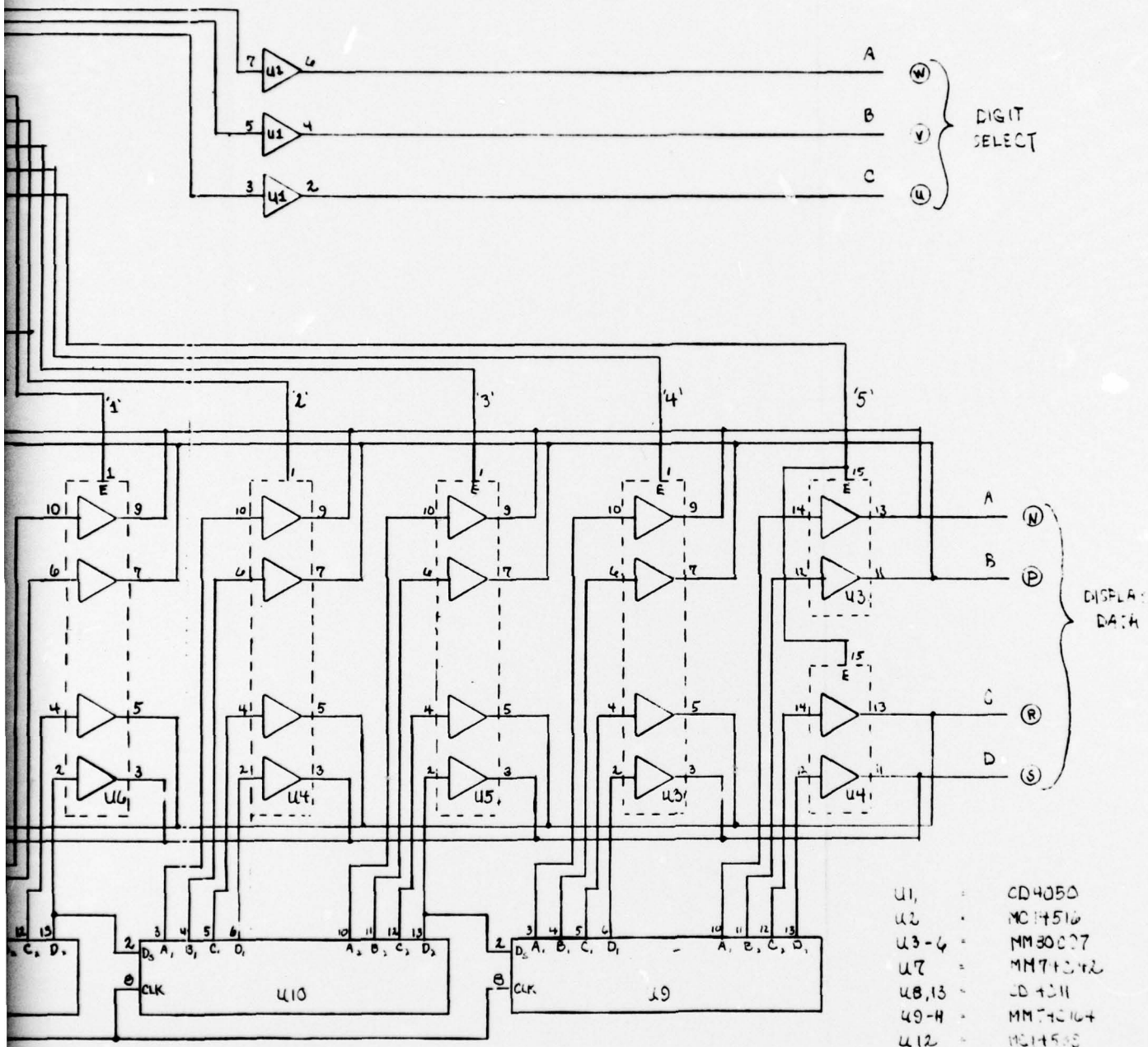
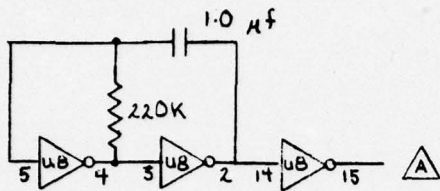
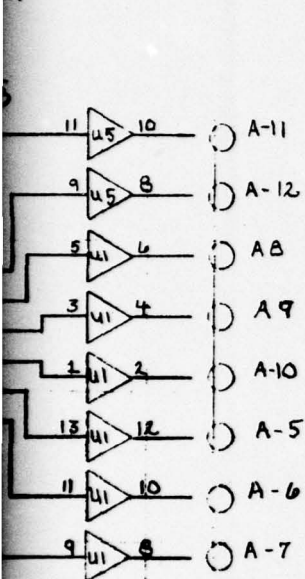


Fig. A-17 — Display controller B-13

2



U1,5	SN 7417
U2	SN 74164
U3,17	SN 7404
U4,6	SN 7400
U7	SN 7402
U8	MC 14049
U9	DM 8831
U10	SN 7474
U11,12,18,19	SN 7493
U13	SN 7430
U14,16	HP 5082-4364
U15	HP 5082-4360

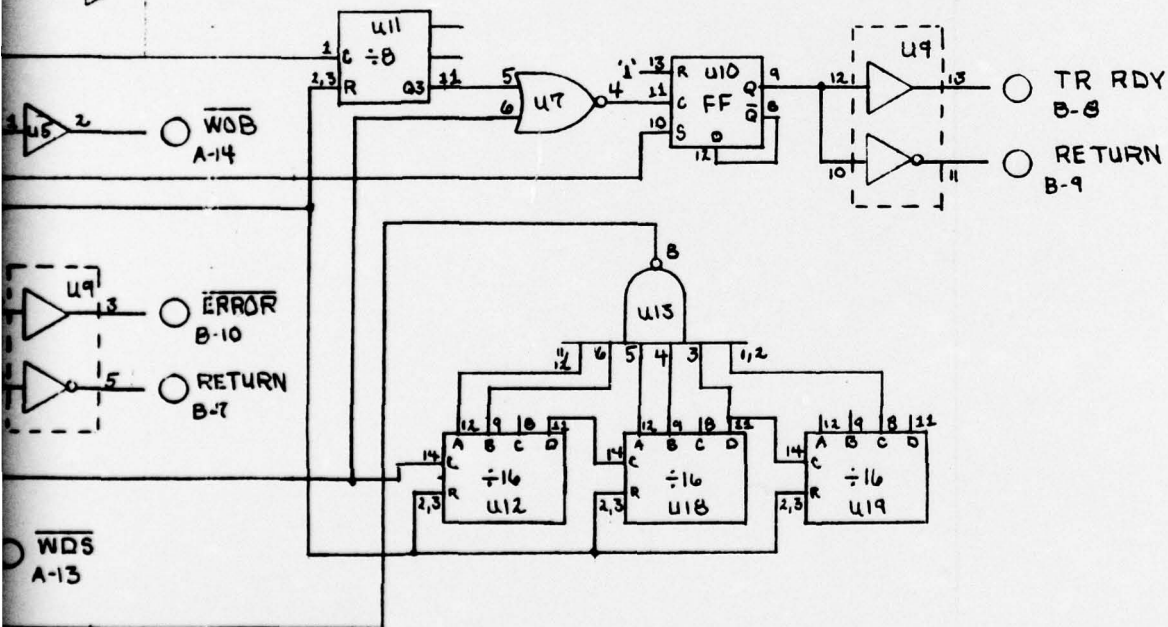
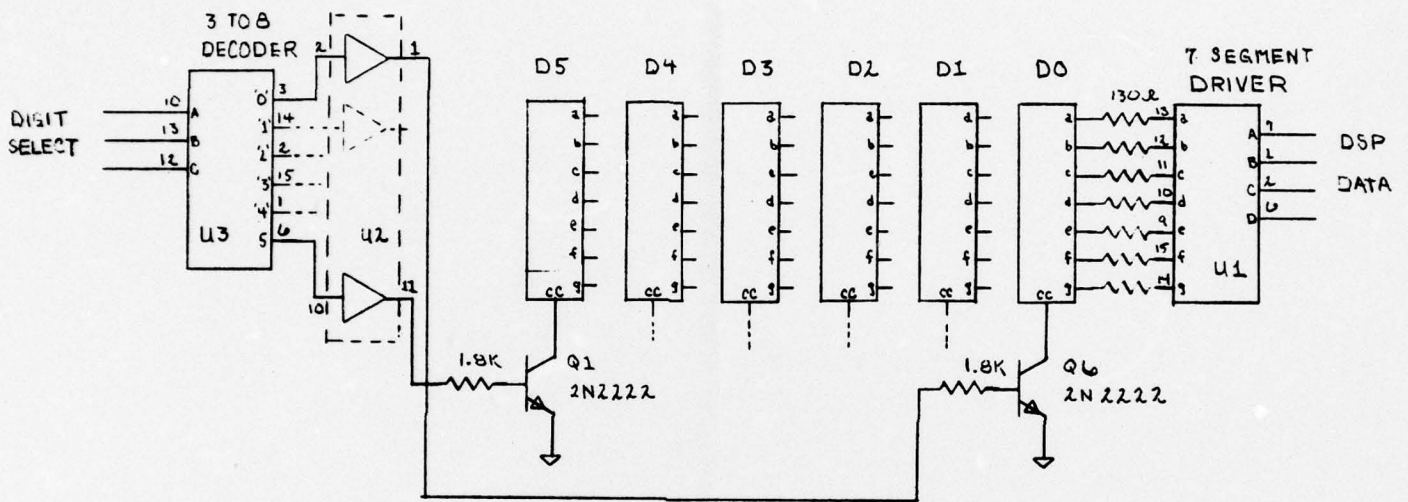


Fig. A-18 - Tape recorder controller

2



U1 = MC14511P
 U2 = MM80C95N
 U3 = MC1402B
 D0-D5 = FND 70

Fig. A-19 - Display