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Report Number N00014-75-C-0405

TOP COLLECTOR CONTACTED MICROWAVE POWER TRANSISTOR

Monolithic Microwave Lumped Element Integrated Circuit Program - Phase II

TRW Inc., Semiconductor Division
14520 Aviation Boulevard
Lawndale, California 90260

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March 1977

TECHNICAL REPORT, PHASE II

Final Report for Period 18 December 1975 - 24 February 1977

Approved for Public Release. Distribution Unlimited.

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This report covers the work on Naval Research Contract No. N00014-75-C-0405 (Top Collector Contacted Microwave Power Transistor). The objective of the contract is to investigate the monolithic integrated circuit approach for the fabrication of RF power transistors and associated matching networks to eliminate hand working, wire bonding and to provide improved uniformity, yield, reliability and ultimately, lower cost.

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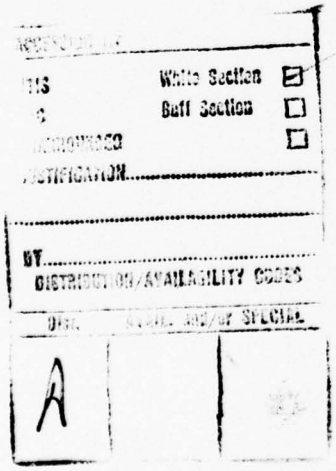
20. Abstract continued.

Specifically, Phase II of this work calls for an isolated all top contacted 30 watt, 1.5 GHz power transistor. The devices meet or exceed all the contract requirements (30 watt @ 1.5 GHz with 7 dB gain). The final processes used and the best results are discussed.



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SECTION 1

M^2 LEIC - PHASE II - FINAL REPORT

The objective of this research and development program is to examine the feasibility of producing the technology necessary to build microwave monolithic power transistors in the 1-10GHz range using silicon bipolar active transistor technology.

This report covers Phase II of a multi-phase program. The first phase developed the technology necessary for moving the collector contact from the back side of the chip to the top side with small resistive losses. In Phase II this top contacted structure was RF isolated from the back side of the chip, producing a microwave power transistor that is both laterally and vertically isolated on the silicon chip, while retaining the capability of heat sinking the transistor in a conventional manner. The next phase is to develop technology to integrate the hybrid matching networks, used in microwave power transistors, onto the isolated chip to produce a totally monolithic RF power transistor with "no hand wired" interconnect between active and parasitic elements.

This final report deals with the Phase II efforts where the all top contact technology of Phase I is utilized in isolated collector monolithic multicell devices. The issue for Phase II was RF collector isolation, both horizontal and vertical, in specific areas of a silicon substrate.

SECTION 2

COLLECTOR ISOLATION TECHNOLOGY

2.0 INTRODUCTION

A high power monolithic structure with isolated collectors which will operate in the 1.5GHz range at 30 watts output has been developed. The technology developed for the isolated collector RF power devices utilizes epitaxial P+/ν/n+/n- layers and the anisotropic etching of <100> oriented silicon to isolate the buried layers. Dielectric filling of the "V" groove isolation moats provides for planarization of the structure, which is required for fabrication purposes. "V"-groove etching also provides a method for producing low resistance vias to connect the buried collector regions.

The resultant N-P-N transistor is equivalent to those of today's hybrid transistor. Only, the collector is brought out from the top of the device and electrical isolation of the collector is provided by the P-I-N structure.

2.1 30W-1.5GHz ISOLATED TOP COLLECTOR CONTACT DEVICE

The objective of Phase II was to fabricate an RF power structure with an isolated top collector contacted configuration.

The transistor device was identical to that of the Phase I top contacted transistor, but with the addition of P-I-N isolation added to the device. The isolated structure (see Figure 1) objective was again 5 watts per cell with a minimum gain of 8 dB at 1.5GHz. Cell combining techniques were used to parallel the individual cells to obtain the required 30 watts at 1.5GHz with a minimum gain of 7dB.

One of the big problems encountered during the Phase II effort was obtaining the p+/ν/n+/n- epitaxy to our specifications. Epitaxial technology was developed to produce the required P-I-N structures. Another problem was the back polishing of polycrystalline silicon, which was solved by the acquisition of an R.H. Strasbaugh free wafer polisher. Other minor problems occurred during fabrication. The mask set we are using was designed and stepped almost two years ago (e.g., beginning of Phase I this contract). The mask set was designed for an approximately 26 micron isolation depth. "V"-grooving the epitaxial P-I-N material on hand required at least a 28 micron isolation groove to obtain complete isolation to the P+ substrate. Some channeling was found to occur between the two adjacent N+ collector regions when the "V"-groove did not extend clear through the intrinsic region to the P+. Varying degrees of dc leakage was the result. Some overetching, beyond that for which the mask set serif was designed,allowed some yield to produce and evaluate workable

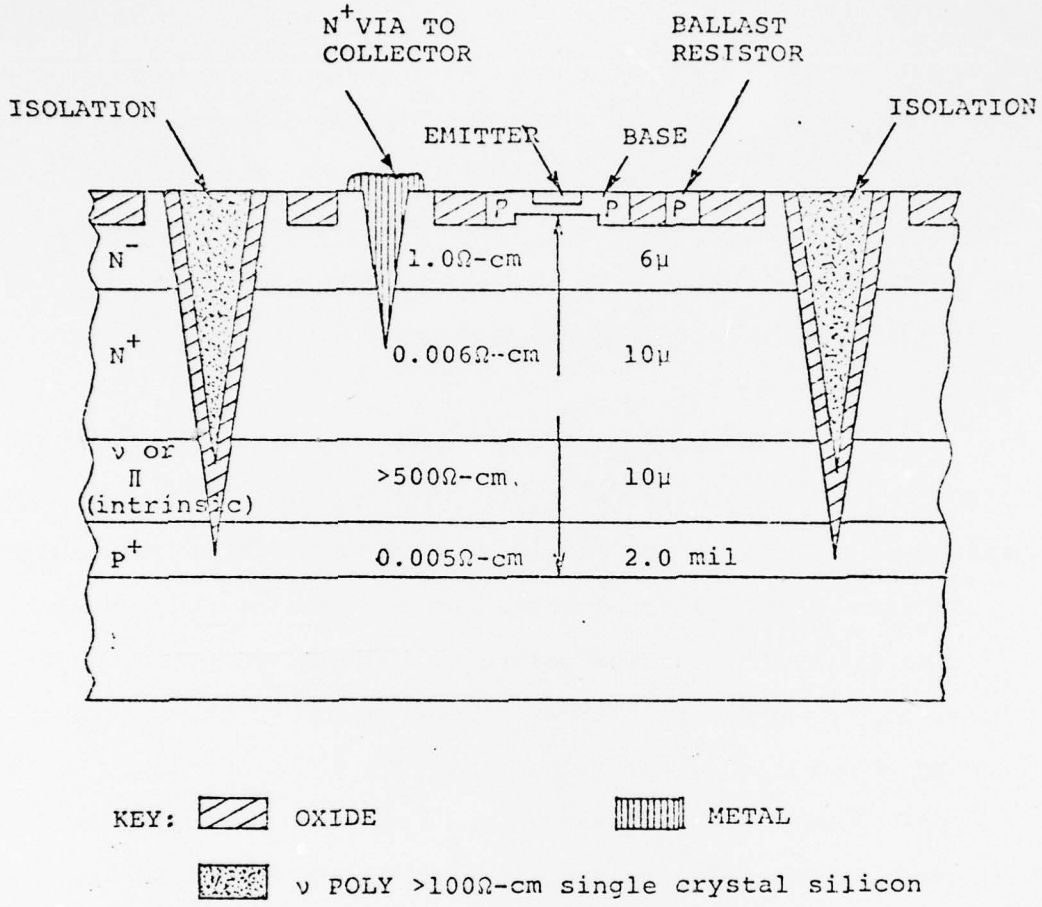

Figure 1. Side View of Isolated Structure (ISTCSB2000).

transistors.

2.2 P-I-N EPITAXIAL AND EVALUATION (VERTICAL ISOLATION)

The epitaxy specifications for the ISTCSB2000 transistor come from TRWS's epitaxial P-I-N deposition study, which includes theoretical calculations and extensive experimentation and measurements on the diffusion of the interfaces. Figure 2 indicates the desired specification for the multilayer epitaxial structures after all high temperature operations required for device processing.

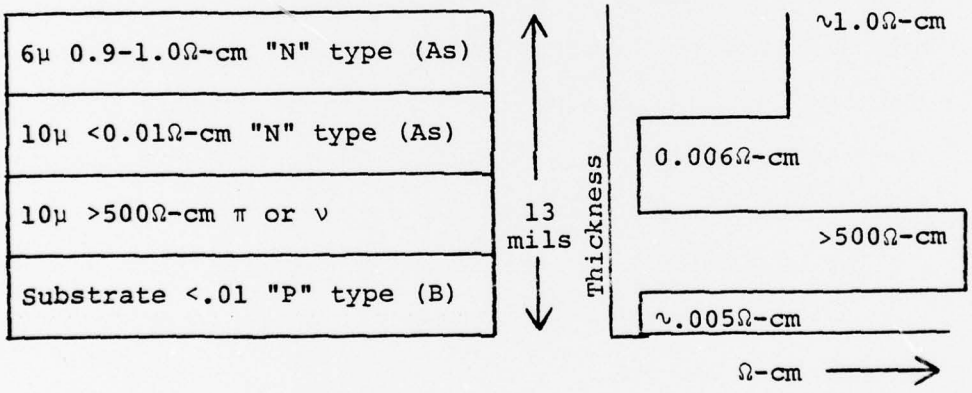

Figure 2. Thickness, Resistivity, Conductivity Type and Profile of Desired Multilayer Epitaxy.

The N- region serves as the collector region of a transistor. The low Ω-cm N+ layer is the buried collector contact layer. The intrinsic layer (ν) form the isolation between the collector

regions and the substrate (P+ region).

The substrate (P+) must be heavily doped to prevent surface channeling around the bottom of the grooves. A $\sim$1.0Ω-cm N- layer is the standard epitaxial collector material for TRWS production model SB2000 transistor.

Required specifications for the epitaxial layers, namely abrupt changes in doping density, imply that the epitaxy must be deposited rapidly at relatively low temperatures. The triple epitaxial layer can be grown continuously to give the same crystal quality as a single layer. An epitaxial reactor is programmed to give reproducible results by switching "on" and "off" the dopant (Arsenic) as the silicon grows continuously. Junction lags due to time taken to change reactor gases (concentration and type) are avoided. Thus, by using no dopant, followed by a high concentration of AsH_3 dopant, then lowering the AsH_3 concentration while utilizing a high flow rate (i.e., $\geq$ 50 l/min) vertical reactor, the abrupt resistivity layer requirements are met.

Dichlorosilane (H_2SiCl_2) is utilized in the reactor at a temperature of 1050^{o}C. This yields a growth rate of $\sim$1.2μ/min, so little difficulty occurs in controlling the growth of all three epitaxy layers in sequence. Sequential deposition also requires only one long hot HCl etch on the substrate so the

highest quality layers are processed. Spreading resistance probe (SRP) evaluation is made on all epitaxy runs. Typical SRP's are shown in Figures 3 and 4. The high temperature processes that the wafers experience during the fabrication cycle result in diffusion of the low resistivity epi layers into the higher resistivity layers. This diffusion changes the thicknesses of the layers and is commonly referred to as junction creep. Overall junction creep is held to a minimum by employing Arsine (AsH_3) for the N+ and N- regions. Junction creep that occurs during wafer fabrication demands the material to be specified as shown in Figure 5.

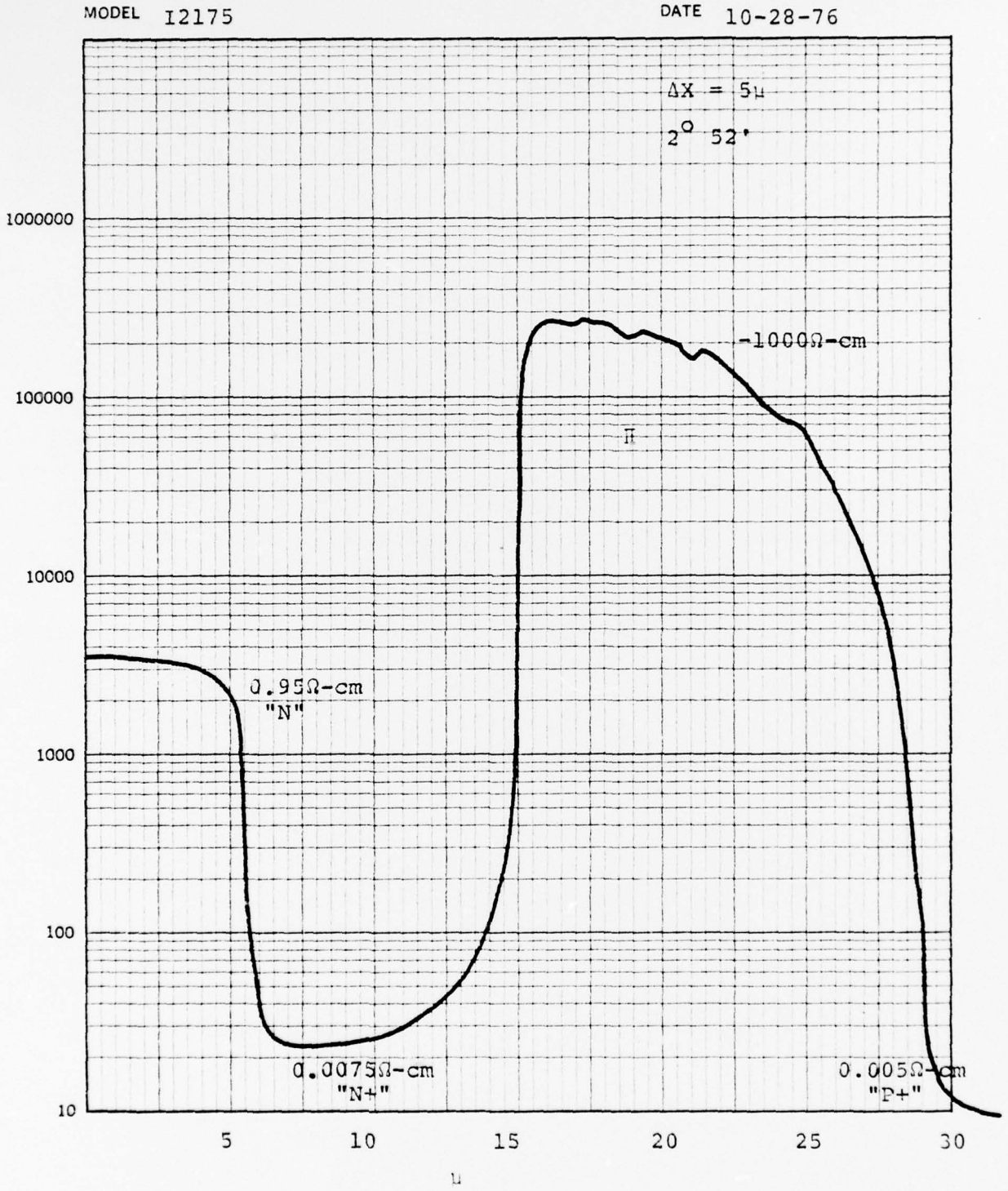

Figure 3. SRP of Substrate.

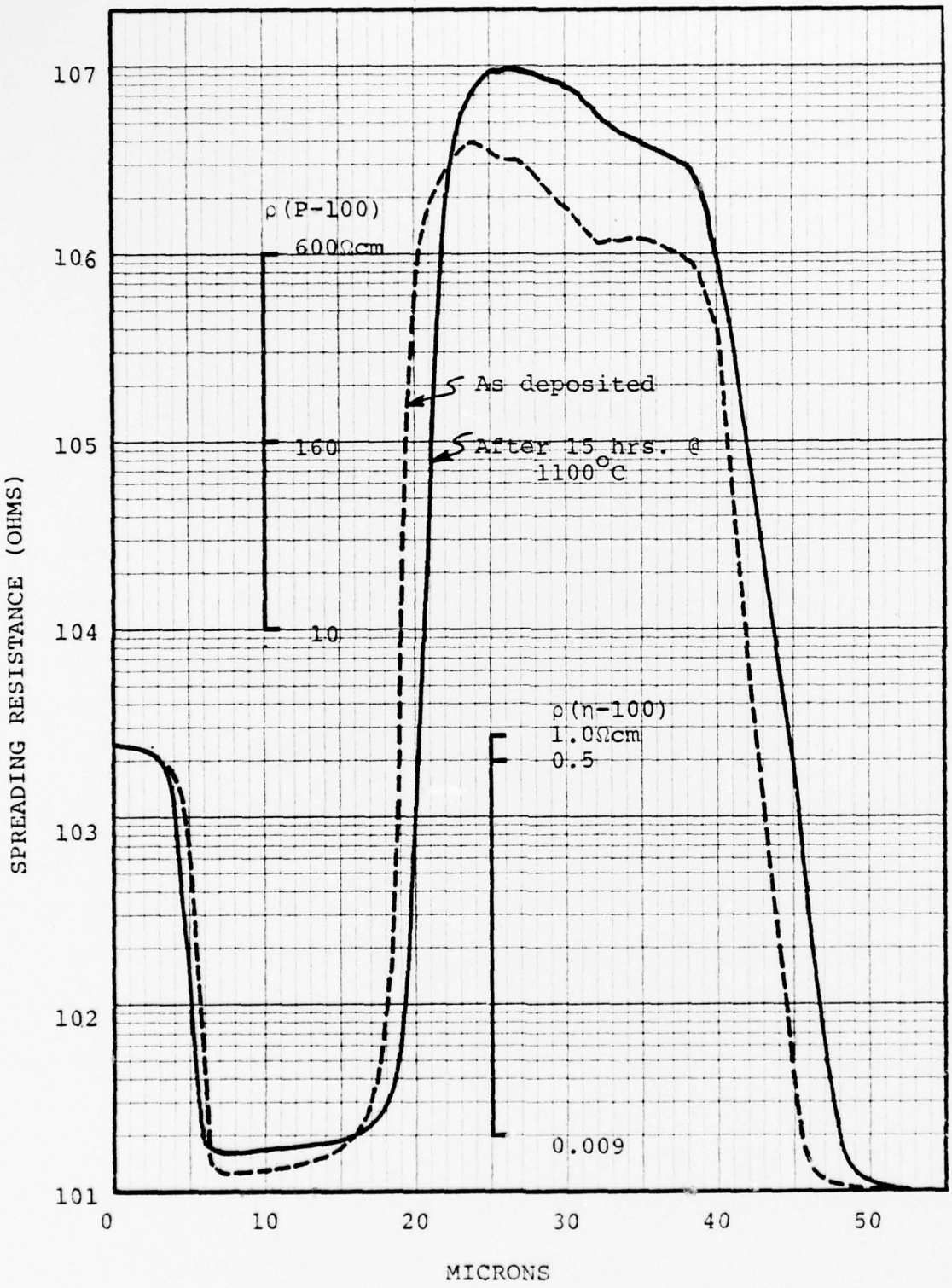

Figure 4. SRP of Material Before and After Junction Creep.

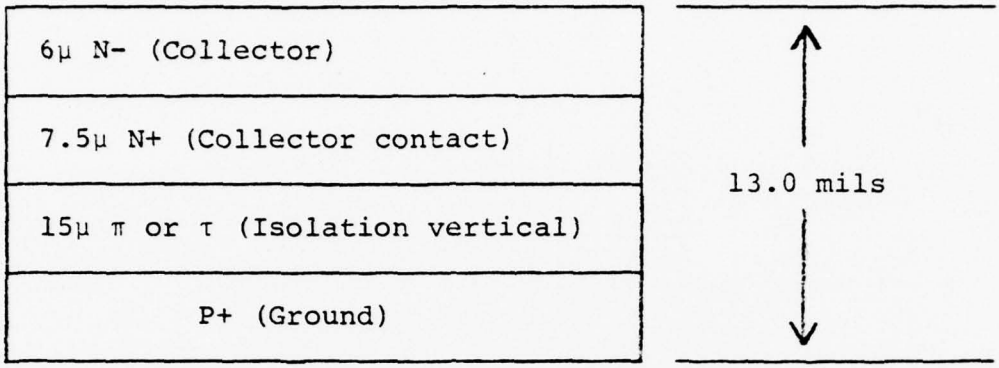

Figure 5. Epitaxial Growth Specifications

The 6 micron N- material chosen for the collector of the device is specified for 28V operation and ruggedness requirements. N+ material thickness and resistivity is determined by the required collector series resistance and saturation voltage. We have found that a direct top contact to the buried N+ layer improves V_{cc} (saturation) only to a point and that most of the V_{ce} (sat) is caused by current flowing through the N- collector layer. The saturation voltage cannot be reduced beyond a certain point by lowering the resistance of the buried layer. Any additional reduction in resistance is governed by the N- resistance between the base and buried layer. The N+ thickness is approximately 10μ for our geometry.

The intrinsic region is governed by two factors: minimum capacitance at the minimum collector voltage swing (i.e., ~1 volt)

and ample breakdown characteristics for the maximum collector voltage swing (i.e., >60 volts).

For the special case of P+IN+ abrupt planar junction diodes, the depletion width calculation is:

$$W_p = 0.509 \sqrt{\rho_c V}$$

where W_p = depletion width in microns (μ)

ρ_c = resistivity of intrinsic region in ohm-cm

V = voltage to obtain depletion maximum or minimum capacitance

If $W_p = 10\mu$ and $V = 1$ volt

$$\rho_c = \frac{10^2}{.259081} = 385\Omega\text{-cm}$$

minimum for the intrinsic layer.

The capacitance per unit area, C_s, of the junction if the intrinsic region is 10 microns thick and fully depleted is:

$$C_s = \frac{\varepsilon_s}{W_I}$$

C_s = device capacitance - farads/cm^2

$\varepsilon_s = \varepsilon_o \times \varepsilon$

ε_o = dielectric constant of free space

$= 8.85 \times 10^{-14}$ farads/cm

ε = relative permitivity of silicon

$= 11.7$

$\varepsilon_s \tilde{=} 1.0443$ pF/cm

W_I = junction width of intrinsic region abrupt junction

therefore:

$$C_s = \frac{6.73 \times 10^{-2}}{W_I(\mu)} \text{ pF/mil}^2$$

Hence, for a completely depleted 10μ region of $\tilde{\sim}400\Omega$-cm silicon, the capacitance is calculated to be:

$$C_s = 6.73 \times 10^{-3} \text{ pF/mil}^2$$

The P+IN+ reverse breakdown voltage is:

$$BV_{CS} = \frac{40.18}{\rho^{\frac{1}{8}}} W \frac{-3.8585W^2}{\rho}$$

where W = width depletion = 10μ

$\rho \tilde{\sim} 400\Omega$-cm

$BV_{CS} = 189.0$ volts

which is ample for any collector swing expected with a 28 volt power supply. The P+ will normally be held at ground potential.

This type of structure has the significant advantage in that the capacitance per unit area is very low even at low reverse voltages, so the collector to ground parasitics capacitance can be controlled.

The ISTCSB2000 mask set is designed to have a total of 146 mil^2 isolated collector region area. The C_s of this structure for

a 10μ intrinsic region is calculated to be:

$$C_s = 6.73 \times 10^{-3} \text{ (pf/mil}^2\text{)} \times 146 \text{(mil}^2\text{)}$$

$$= 0.98 \text{ pf}$$

Figure 6 shows a C-V plot of a typical reverse biased collector-substrate junction on a completed isolated collector ISTCSB2000 device. It can be seen that the experimental values are in close agreement with the theoretical calculation.

2.3 "V"-GROOVE FORMATION (HORIZONTAL ISOLATION)

Chemical V-grooving through the N-, N+ and intrinsic layers of a P-I-N structure into the P+ region form the horizontal isolation in the P-I-N substrate. Horizontal isolation requirements are the same as in the vertical situation with the exception that high thermal conductivity is not required. Air is the superior isolation medium at low voltages in the microwave region; however, air has a breakdown voltage significantly less than that of silicon dioxide, ceramics or polycrystalline mediums. A very high resistivity polysilicon fill in the isolation groove has proven effective in raising inter-device breakdown voltages. The total structure is shown in Figure 7.

The P-I-N design for a vertical isolation and V-groove design for horizontal isolation offers relatively simple processing, smaller isolation capacitances, and higher junction breakdown voltages than other techniques. Other process combinations

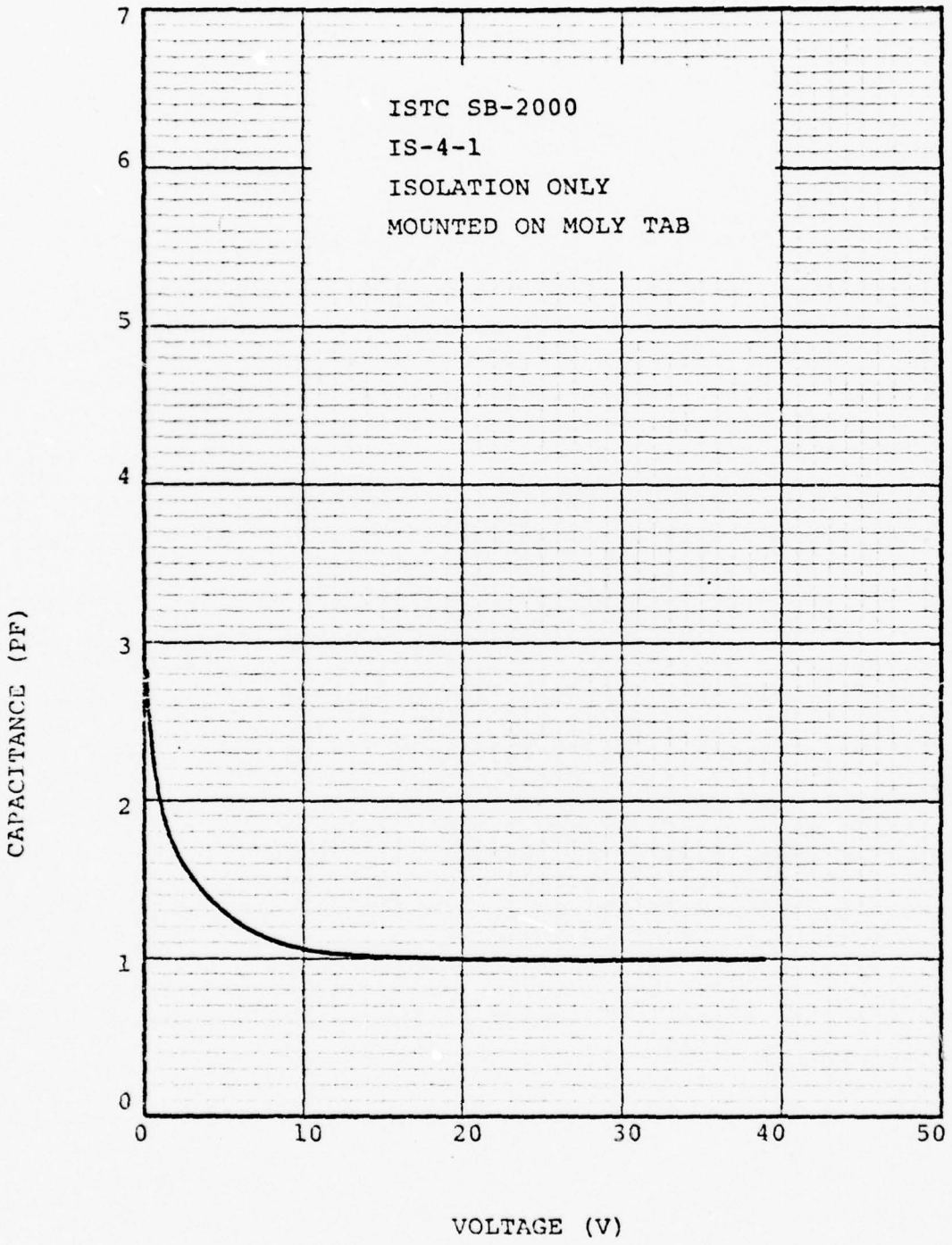

Figure 6. 10u Intrinsic Region.

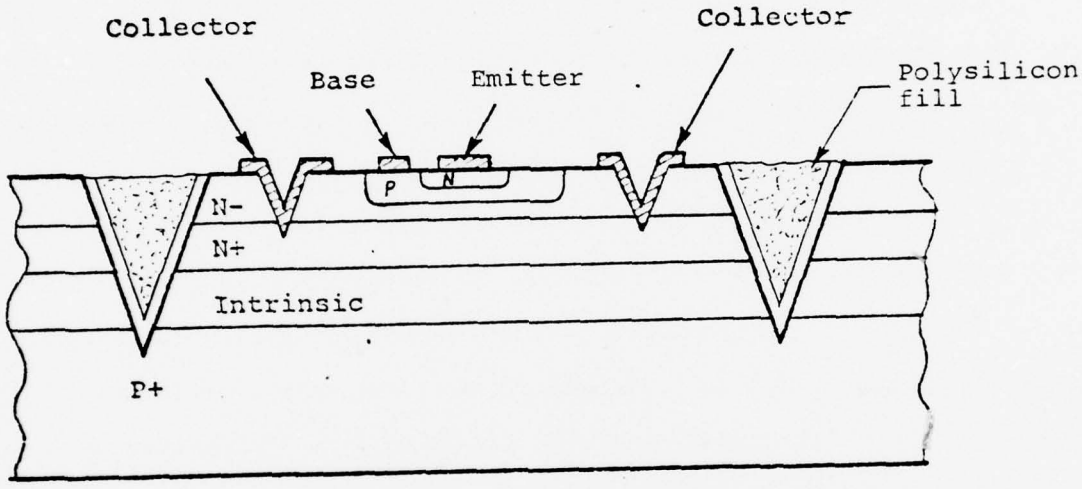

Figure 7. Cross Section of Final Device Fabrication.

are possible, but not without further fabrication complications, or degradation of the required properties.

The (100) orientation is utilized for the silicon substrates because it can be anisotropically etched (i.e., V-groove). Consequently, when stripes parallel to the (100) axis (parallel or perpendicular to the flat of a (100) wafer are opened through a SiO_2 or Si_3N_4 mask and anisotropically etched, a V-groove is formed.

A serif is required to control corner definition during anisotropic V-groove etching. Close packing is required for top contact design, isolation V-groove design, collector contact V-grooves and vias. Without a serif an outside corner etches very rapidly with respect to the fine line definition of anisotropic etching of (100) orientatin silicon. The "V"-groove utilized for horizontal isolation is identical in design concept as that used for the collector contact via in Phase I of this contract except the depth and width.

Passivation of the exposed P-I-N junction in the V-grooves (i.e., horizontal isolation) is done by thermal oxidation of the silicon. The V-groove is then filled with polycrystalline silicon.

2.4 POLYCRYSTALLINE SILICON FILL AND BACK POLISH

Polycrystalline filling of the "V"-groove formed to define the isolated collector regions is necessary to provide for planarization of the structure. Planarization is required for fabrication purposes and allows for metallization over the V-groove isolation.

The polycrystalline silicon is deposited over the wafer surface to a thickness that will fill the entire V-groove. The excess polycrystalline silicon is lapped and polished to the original oxidized surface of the wafer as shown in Figures 8, 9, and 10.

The SiO_2 acts as a polish stop. The filled V-groove now provides a surface that is planarized so the wafer can be processed through photoresist steps necessary for fine microwave geometries as shown in Figure 11.

For design purposes it is important to know the electrical characteristics of the polysilicon fill structure at high frequencies. Work done in the past on this type of structure has shown unacceptable loss tangent at frequencies above 500MHz. This work, however, was a study on polysilicon layers of much less than 100Ω-cm resistivity. Advances in CVD technology for polysilicon growth and the availability of reactants with low impurity levels produce polysilicon growth in the 1.1×10^5 Ω-cm range. Measurements on test structures with polysilicon resistivity

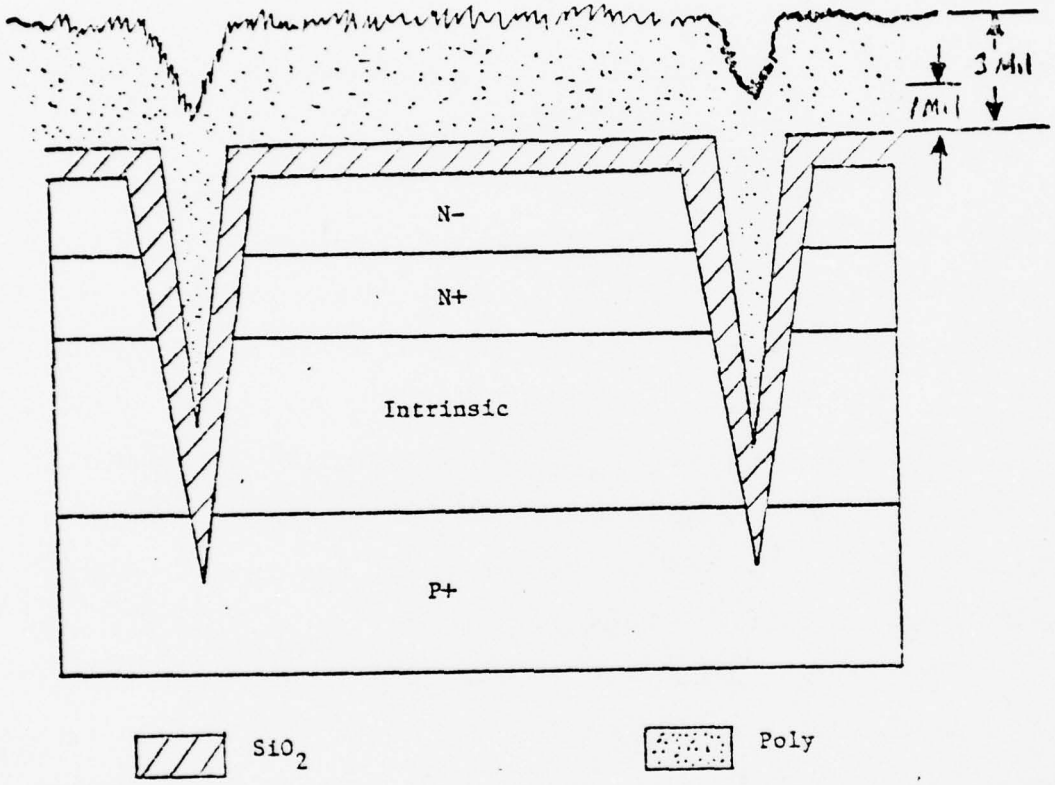

Figure 8. Dielectric Deposition and Polysilicon Backfill.

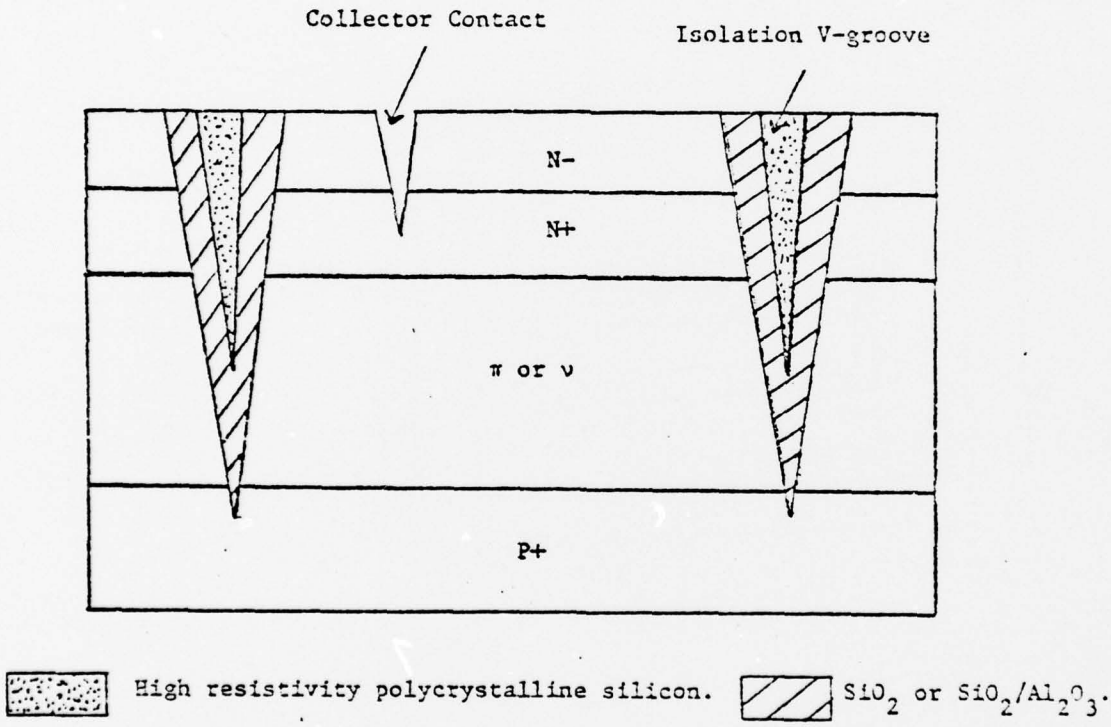

Figure 9. Side View of Back Polished Polysilicon Backfill.

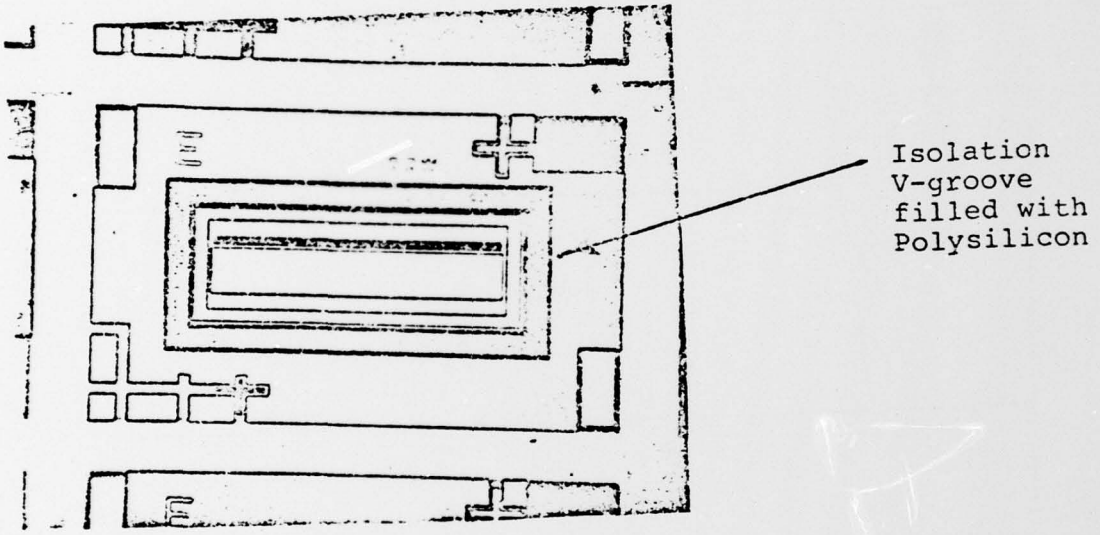

Figure 10. Top View of Back Polished Polysilicon Fill.

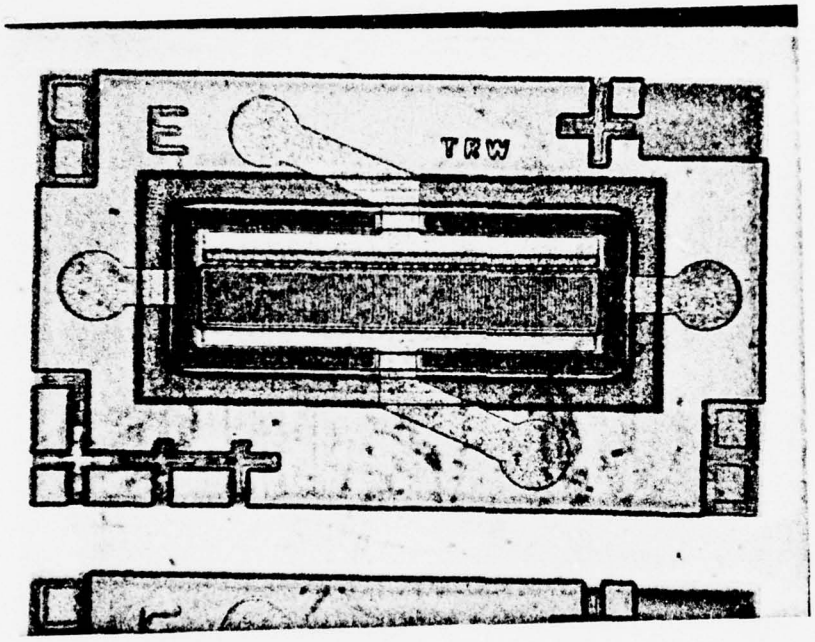

Figure 11. All Top Contacted Isolated Collector Power Transistor.

in this range have shown loss tangents which are acceptable at microwave frequencies.

There is no significant sidewall parasitics associated with the polysilicon fill structure. Thus, no significant capacitive effects are added to the P-I-N junction by this design concept.

Surfaces channeling at the bottom of the V-grooves between adjacent transistor collectors is eliminated because the P+ substrate is heavily doped. The heavily doped substrate (i.e., $3x10^{18}cm^{-3}$) acts as a channel stopper during the oxide passivation step.

One potential problem exists in utilizing the thermal oxide as the polish back stop. Thermal oxide has a polish rate that is approximately 10 times slower than that of polysilicon. If the wafers are warped or non-parallel, various areas polish back sooner, the oxide stop does not hold off long enough, and the underlying N- region of the epitaxial structure is destroyed.

The polish back process is one of the processes which has been under continuous development. At this time, the process has evolved to the point where process repeatability and yield are considered to be acceptable and where the existing problems and their solutions are understood.

Initial analysis of the polish back process indicated the possibility of problems and some approaches to their solution.

First, the polish process should preferably be chemical/mechanical in nature. A purely mechanical abrasive polish process would have a lower probability of success because abrasives readily attack the oxide or other dielectric layers used for the polish stop and, hence, would require a degree of polishing control not easily achievable. Secondly, the polishing should be carried out on a soft pad in order to take into account any warpage of the wafers. Ordinary silicon wafers used for p-n junction isolation are relatively free of warpage and their surfaces can be made quite parallel. This, of course, is not the case for the multilayer epitaxial silicon wafer. Because of the nature of the processing steps (the deposition of relatively thick polycrystalline silicon layers, etc.) some warpage and also some variation in the wafer thickness is certain to occur. Furthermore, the amount of warpage and the thickness gradients will not be the same from wafer to wafer. It is conceivable that these factors could be minimized through extensive substrate process study and optimization. However, complete process optimization is highly dependent on the characteristics of the equipment used for the high temperature processing and is, therefore, difficult to control from run to run. A better approach is to make the polishing process as insensitive to these factors as possible and to assume that as the epitaxial wafer substrate manufacturing technology matures, these factors will decrease in magnitude.

TRWS' first efforts were of an exploratory nature and were, in fact, a demonstration of polish back feasibility. In these experiments, standard silicon wafers with (100) crystal orientation were used, instead of multilayer epitaxial wafers. Some wafers were grooved to various depths while others were not. The surface of the wafers was protected by a thermally grown oxide or by an oxide plus other dielectric layers. Polycrystalline silicon was deposited and then polished back. The initial results are as follows: first, the polish back process was determined to be feasible, however, the polishing did not proceed uniformly over the wafer surface. Secondly, the polish rate of the oxide was about an order of magnitude less than that of the polycrystalline silicon. Therefore, once the oxide was reached at some point on the wafer surface, some additional time was available to polish the rest of the wafer before this oxide was completely removed. Thirdly, since the polishing was non-uniform over the wafer, it was difficult to devise experiments which would provide quantitative data on the parameters governing polish back. Finally, no high steps were observed at the edge of the isolation. A step or a dishing out of the polycrystalline silicon in the V-groove was expected because the chemical/mechanical polish process polishes the polycrystalline silicon at a faster rate than the surrounding oxide. This factor will be discussed later in more detail.

Although the standard wafers gave a good polish back yield, the results with the multilayer epitaxial wafers were not as encouraging. This result was expected on the basis of increased wafer warpage and thickness non-uniformity. Investigations were then carried out to determine the factors affecting polish back. Since it was difficult to arrive at quantitative results, useful area yield was used as a qualitative indication of an adequate polish back process.

The polish back process remains essentially the same as our initial setup, except for the method of mounting the wafers and equipment components. Initially the wafers to be polished were wax mounted on pistons. The polishing pad was mounted on a flat polishing table which slowly rotated. Since the polishing heads are off center, friction causes the heads to spin about their center. The heads are also free to tilt to accommodate slight differences in wafer thickness. The polishing slurry was pumped from a stirred reservoir and fed at a given rate onto the polishing pad.

The polishing slurry is a mixture of silica powder and water with the addition of a base such as KOH or NH_4OH. Such a solution is standard in semiconductor industry polishing applications, and it performs satisfactorily.

The requirement placed on the polishing pad is that it be sufficiently soft so that it follows the contour of a warped thin

wafer and yet be sufficiently stiff over a small area so that a polycrystalline-filled isolation groove will not be polished below the wafer surface. Pads of various thickness and softness were investigated. The yield was found to decrease as the pad thickness and softness decreased. Furthermore, there was an increasing tendency to overpolish those areas which cleared first (i.e., the high areas on the wafer). In the extreme case, where only a thin hard cloth was used on the polishing table, the yield became very poor.

The thickness of the wafer also plays a role in polishing; the thinner the wafer, the greater the resilience and, hence, a higher degree of flatness with which it can be mounted. However, the thinner the wafer, the greater the probability of wafer breakage during all processing steps. Experiments with various wafer thicknesses have verified the foregoing and at this time, it appears that a thickness of about 12 mils provides the best compromise between the requirements of resilience and strength.

Along these lines, a number of experiments were undertaken in which wafer planarization was attempted in order to insure parallelism. For wafer planarization, the wafer was mounted face down (device side down) after epitaxial growth, the back of the wafer was abraded, and about 1 to 3 mils of silicon material was removed in order to make the front and back faces of the wafer parallel prior to V-grooving and subsequent poly back fill. A

number of wafer runs were planarized and did show an improved yield through polish back. With stiff polish back polishing pads, planarizing is a necessity. With soft and thick polishing pads, planarizing does improve yield, but not to a degree which overcomes the added wafer breakage yield loss which occurs in the planarizing step.

Another obvious factor influencing the polish back yield was the thickness of the polycrystalline silicon layer filling the grooves. Since polishing occurs non-uniformity, even on flat standard wafers, the thinner this layer is, the greater the yield through polishing. However, the layer must be sufficiently thick to fill the grooves slightly above the original surface. Since the polycrystalline silicon also has a rough surface texture, this insures a smooth polished surface in the isolation region.

It is expected that since the polishing is partially chemical, there would be a tendency to propagate the surface profile as polishing continues. This would result in dishing out of the polycrystalline isolation, rounding of the single crystal silicon shoulder and perhaps, step down from the single crystal silicon to the polycrystalline region in the V-groove. Initial scanning electron microscope observations indicated very little dishing. Since then, however, it has been found that some dishing does occur and the shoulder of the single crystal island can be rounded, and the reasons for this are now apparent.

Oxidization of the horizontal isolation V-groove prior to poly deposition is typically 2.0μ in thickness for our process and affords a polish stopping ratio of 10 to 1. That is, the poly will polish approximately 10 times faster than the oxide polish stop on the substrate surface.

SECTION 3

ELECTRICAL DATA AND ANALYSIS OF 30 WATT ISOLATED COLLECTOR TOP CONTACTED SB2000.

3.0 INTRODUCTION

Once the isolated devices were completed through metalization they were thinned to 3.5 - 4.0 mils thick. They were then diced in single cell and triple cell combinations, mounted and evaluated. To determine the quality of each lot with respect to changes and variations in fabrication, several major performance areas were considered for evaluation. Test areas were dc response, capacitance versus voltage response, RF response at 1.5 and 2.0 GHz, in single and multiple cell configurations.

3.1 DC CHARACTERISTICS

The isolated device has the same dc characteristics as a normal non-isolated bipolar transistor with the exception of the addition of the PIN diode between the collector and the substrate. The dc characteristics of the isolated devices from lot 4 #1 are

shown in Table 1. The isolation layer breakdown voltage is very high ($\gtrsim$ 200V) and typically exhibits very small leakage (<10μA @ 28V) so that the isolation layer has very little effect on the dc characteristics of a transistor connected in the isolated mode.

TABLE 1. DC DATA - ISOLATED DEVICE.

Number of cells	h_{FE} 10V	BV_{ceo}	BV_{ces}	BV_{cbo}	BV_{ebo} Rev.	BV_{ebo} Fwd.	$V_{ce\ sat}$	$V_{be\ sat}$
1	29 @ 10ma	31 @ 10ma	48 @ 10ma	48 @ 10ma	5.9 @ 10ma	.77 @ 10ma	.27 @ .1A	1.0 @ .1A
3	13 @ 10ma	33 @ 10ma	47 @ 10ma	48 @ 10ma	5.9 @ 10ma	.72 @ 10ma	.24 @ .2A	.96 @ .2A
6	9 @ 10ma	38 @ 20ma	45 @ 20ma	46 @ 20ma	5.9 @ 20ma	.69 @ 20ma	.4 @ .5A	.98 @ .5A

3.2 CV CHARACTERISTICS

The capacitance versus voltage (C-V) characteristics of the isolation layer was measured to determine if the layer would actually be fully depleted by the collector bias supply. The PIN diode should fully deplete at a low collector to substrate voltage. The depletion region should not widen to any great extent at increased bias voltages. This effect should produce a nearly constant junction capacitance versus voltage above the voltage required to deplete the intrinsic layer. In fact the C-V plot showed this to be true. As shown in Figure 12 , the neutral capacitance of the isolation layer is 2.8 pf. The capacitance then reduced rapidly with increasing voltage to about 10V where the curve flattens out to a constant 1.0 pf to well past the normal operating voltage of 28V.

The C-V plot for the isolation layer in parallel with C_{ob} is shown in Figure 13. This is the normal connection for the isolated device. The total capacitance for both diodes is 2.95 pf @ 28V. This is only a 50% increase over the device in a non-isolated connection. As will be discussed later, this extra capacitance appeared to have no significant effect on the performance of the device.

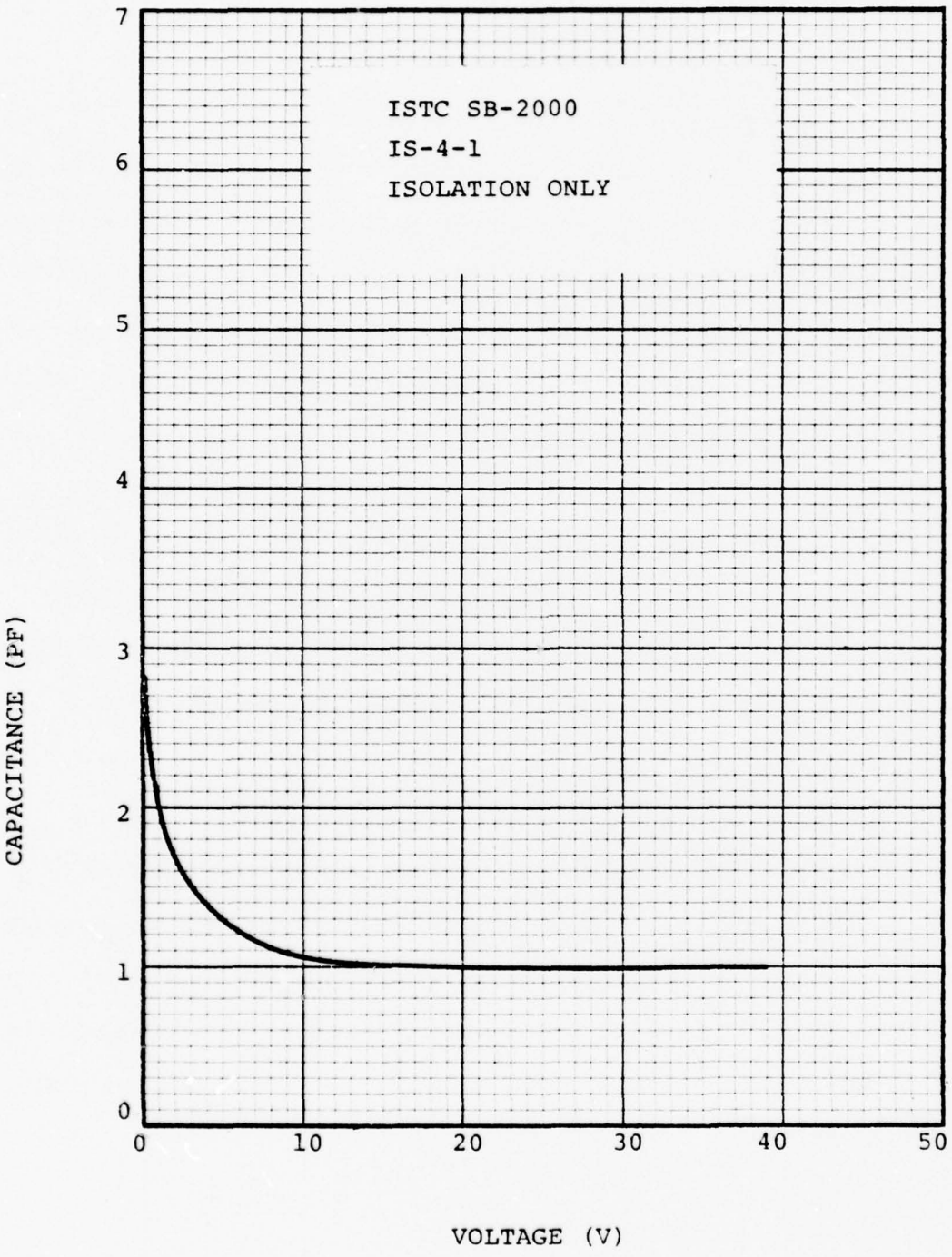

Figure 12. Isolation Capacitance.

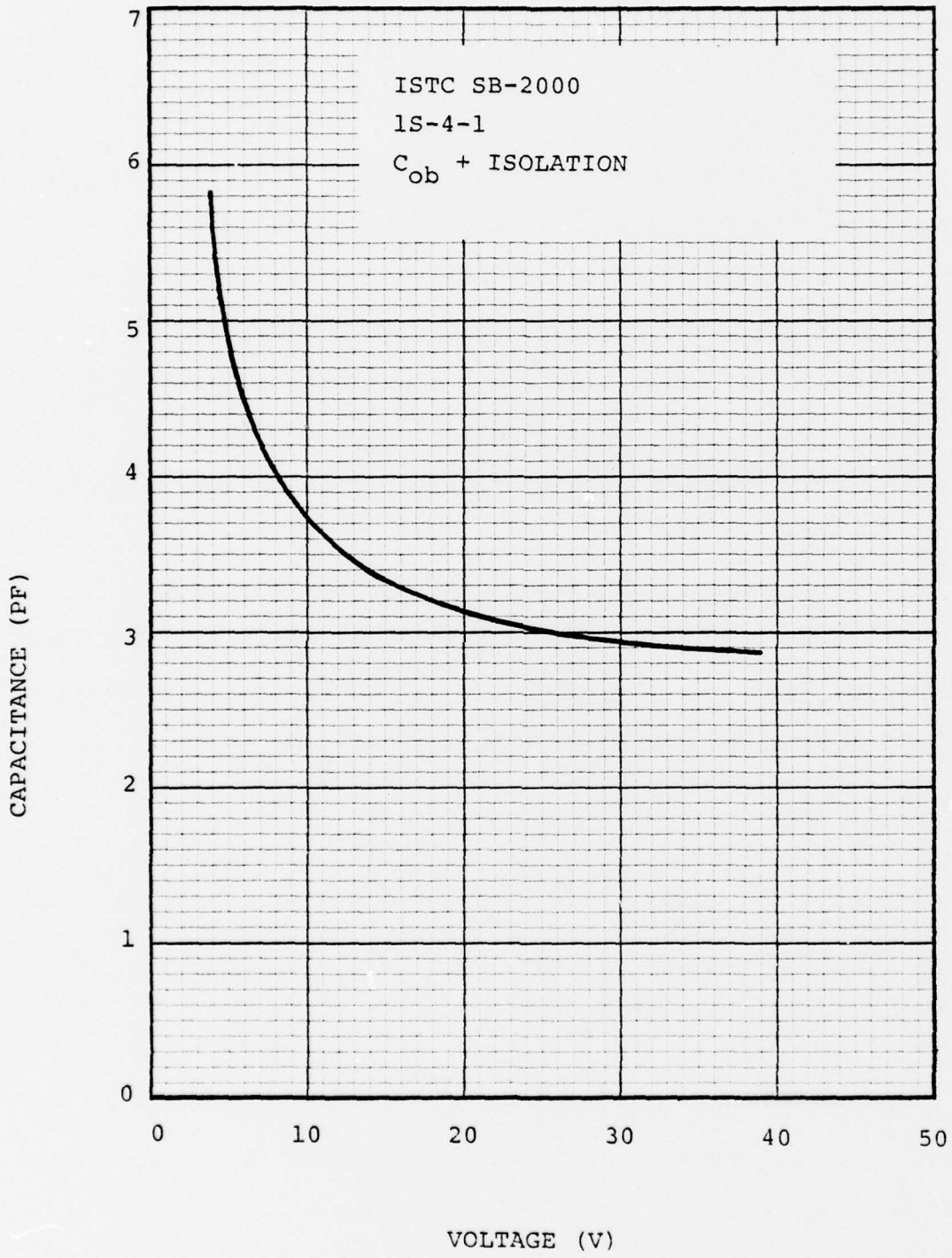

Figure 13. Total Device Capacitance.

3.3 RF PERFORMANCE

3.3.1 Introduction

To evaluate the isolated devices under RF operating conditions, several tests were performed. The tests were done on devices in the isolated mode and the non-isolated mode. Where applicable the tests were also performed on a conventional non-isolated production device of similar construction for performance comparison. These tests were:

1) Small signal S-parameter testing for the determination of F_{MAX},
2) Large signal testing of one cell devices in a package to determine output power, gain, and efficiency,
3) Multiple cell testing to check on the ability of the devices to be parallel combined.

3.3.2 Small Signal Testing

The small signal S-parameters were measured on an automatic network analyzer to determine F_{MAX}. The bias point was chosen to provide maximum small signal S_{21}. All the devices were mounted on a BeO 50Ω carrier for the measurements.

Two versions of the standard production SB-2000 were also characterized as control samples. The ISTCSB-2000 isolated device

has the same internal structure as the standard production SB-2000. The maximum frequency of oscillation, F_{MAX}, for the isolated device (as shown in Table 2) was slightly lower than the non-isolated device but the difference is not very significant. The ion-implanted SB-2000 showed a considerably higher F_{MAX} than any of the standard diffusion samples. The stability factor, K, is acceptable for any of the devices.

3.3.3 Large Signal Testing

Initial large signal testing was done on single cell samples of the isolated device and standard non-isolated devices in the common-base Class "C" mode. The testing was done in a standard BeO package.

The collector pad of the package could be shorted out electrically to allow the electrical characterization of the isolated device. Since the identical package was used in each case, the thermal resistance of each type of device would be the same so that only the electrical effects of the isolation would be studied.

The standard comparison device, an SB-2000 production chip in the GP-13 package, commercially available as the TRW 2003, is shown in Figure 14. The collector, bottom contact, of the device is isolated from ground by the collector pad metallized on the BeO.

The non-isolated top contact, ISTCSB-2000, device was wired in two configurations. First, to test the intrinsic device

TABLE 2: F_{max} COMPARISON

Bias 20V @ 200mA

Common Emitter

CHIP	LOT #	f_{max}	K (S-Band)
SB-2000 Std. Diffusion	107 #19	3.9GHz	1.25
SB-2000 Implanted Base	197 #2A	4.3GHz.	1.10
ISTC-SB-2000 Std. Diffusion Non-Isolated	IS4 #1	3.9GHz	1.15
ISTC-SB-2000 Std. Diffusion Isolated	IS4 #1	3.7GHz	1.20

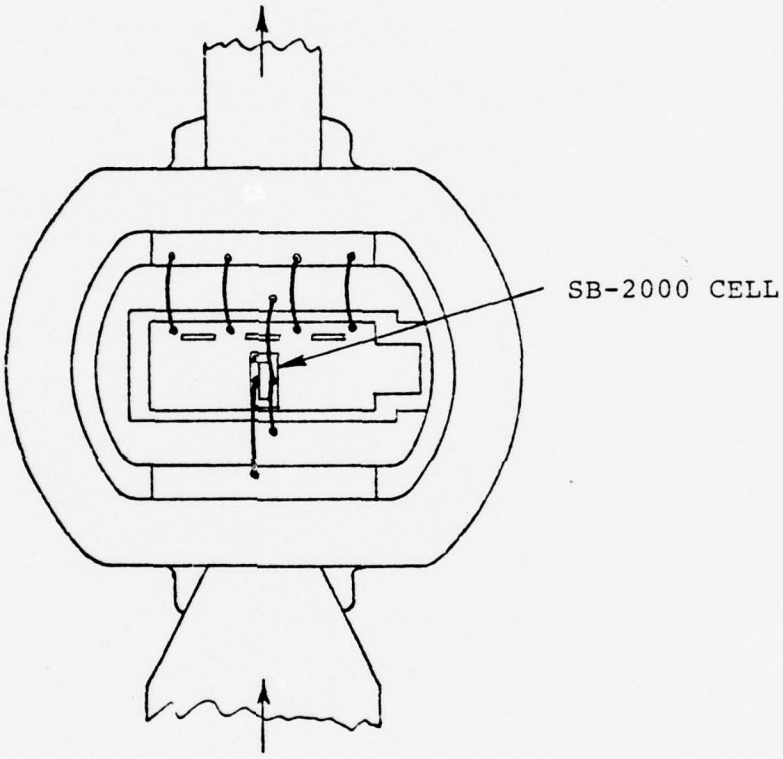

Figure 14. Standard Single Cell, SB-2000.

performance without the electrical effects of the isolation, the device was wired to short out the PIN isolation layer with bond wires from the top contact to the collector pad, Figure 15.

Second, the collector pad was shorted to ground on other test devices with a solder preform scrubbed across the insulating gap, Figure 16 . The top collector contact only was connected to the output lead. Other wiring remains the same as the non-isolated case.

All three types of devices were tested at 2.0 GHz for power output, gain and efficiency. As shown in Figure 17 the transfer characteristics of all three devices were virtually identical. The gain and efficiency curves, Figures 18 and 19 , also show very close similarity. All three devices also performed in the same fixed tuned test fixture which implies that the input and output impedance of the devices were very similar. Even though the isolated devices had an additional 1.0 pf of output capacitance caused by the PIN isolation layer, the total output capacitance remained nearly the same because the non-isolated devices have 0.66 pf of collector pad capacitance not present in the isolated device.

The isolated devices were tested for VSWR survival by the application of a sliding short to the output connector and the simultanious application of 2 dB overdrive (1W). The devices would survive with no apparent damage or degradation even after CW dissipation of 12.6W, (450mA @ 28V), at the highest current short

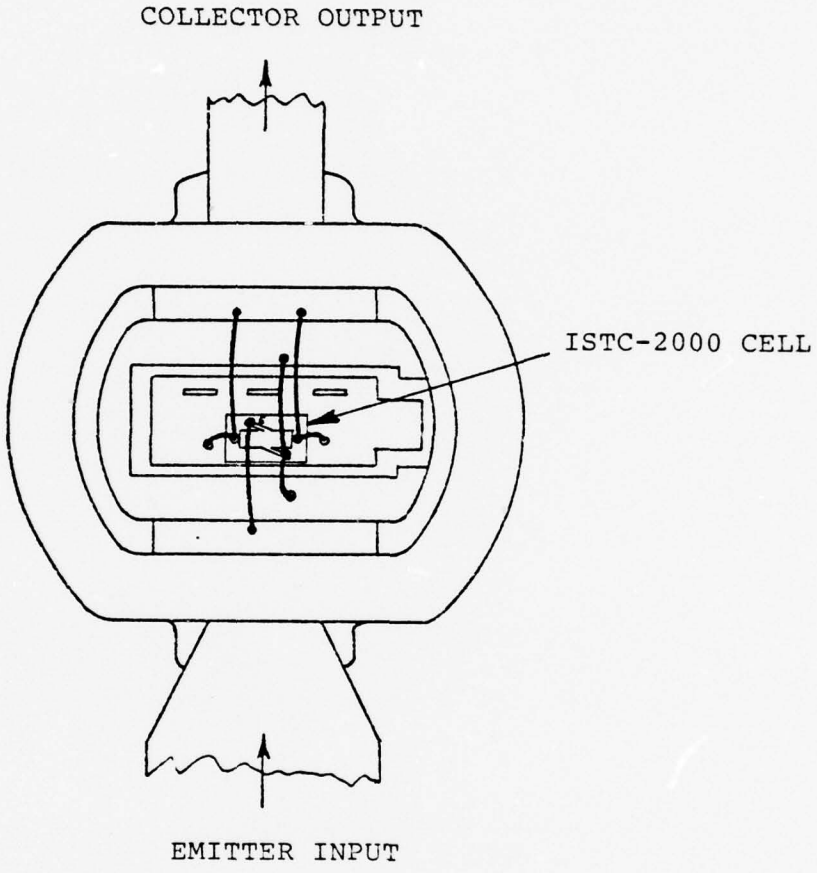

Figure 15. Non-Isolated Single Cell, ISTCSB-2000.

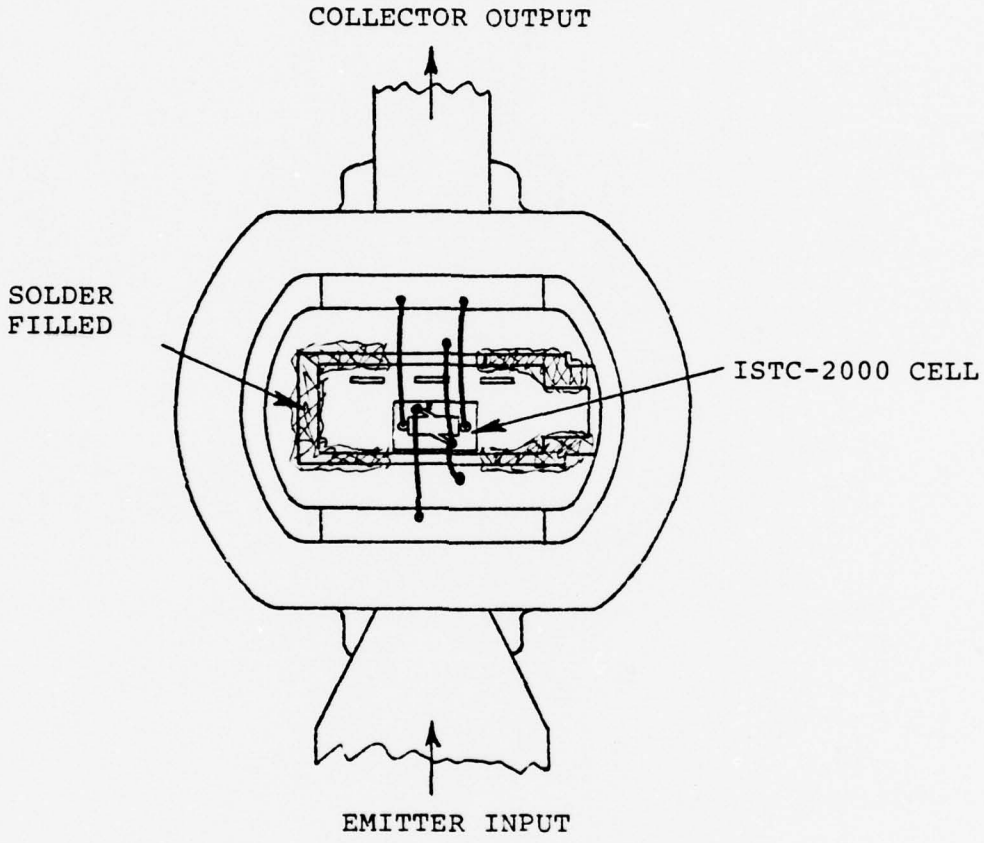

Figure 16. Isolated Single Cell, ISTCSB-2000.

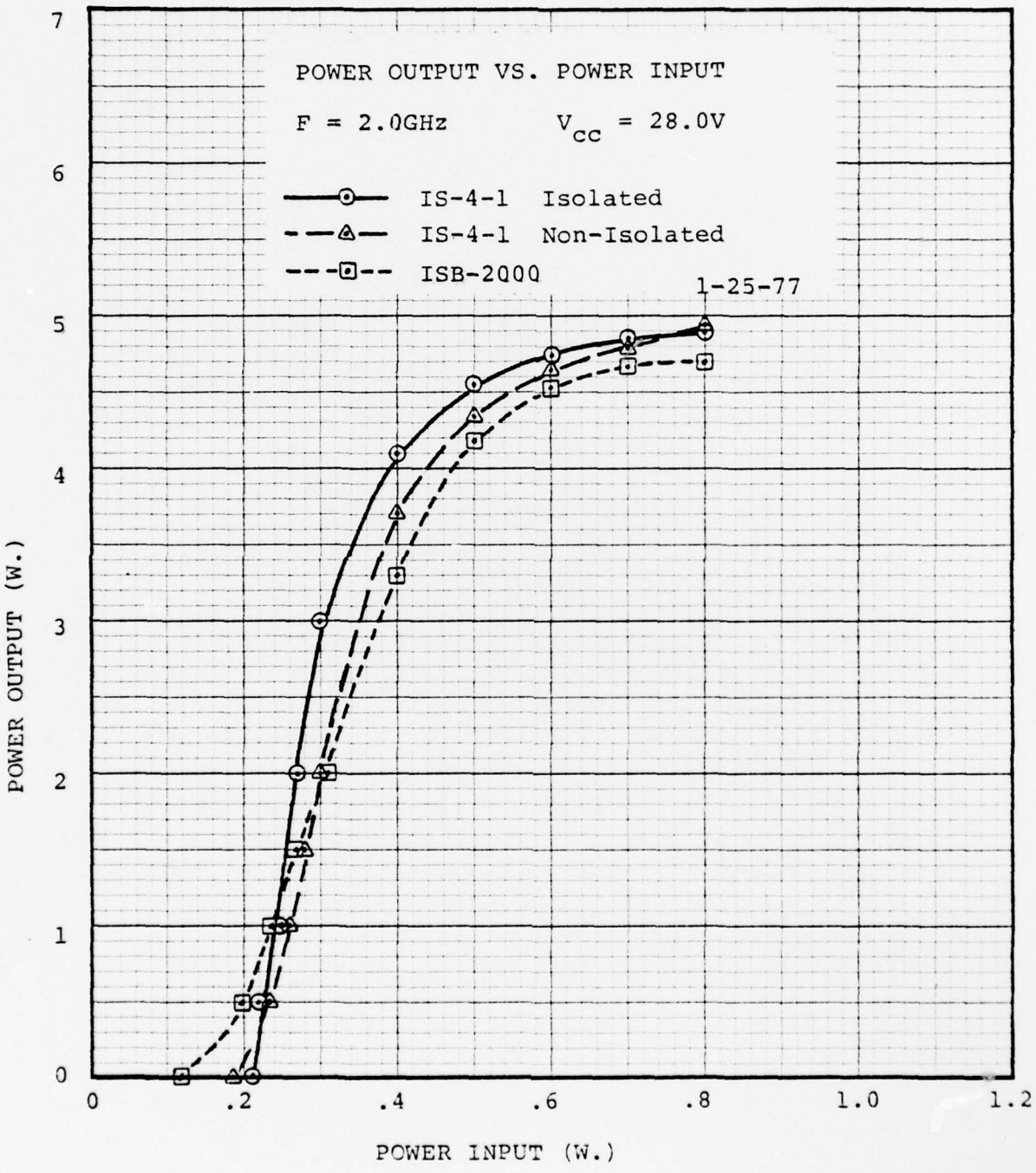

Figure 17. Power Output vs. Power Input.

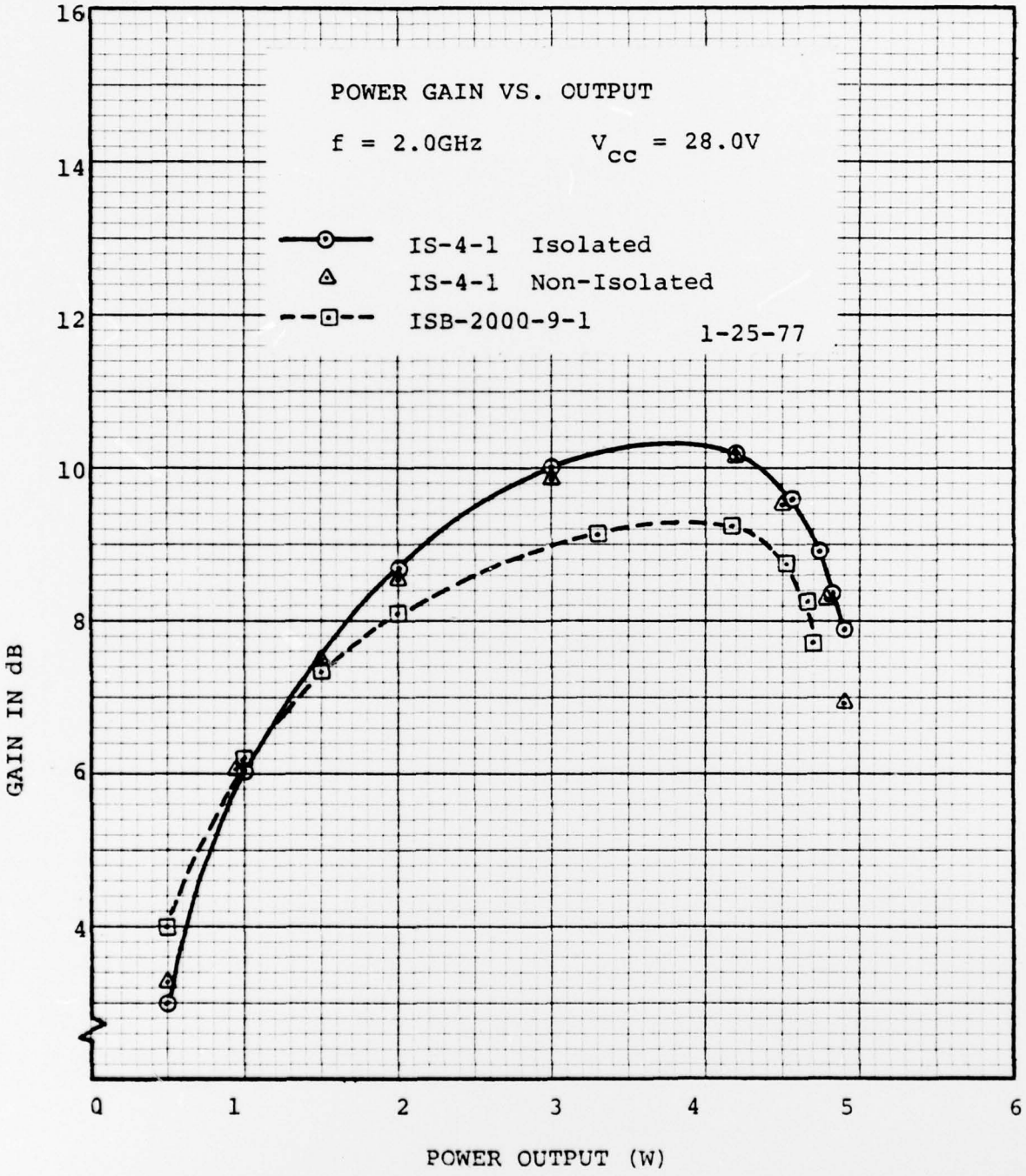

Figure 18. Power Gain vs. Output.

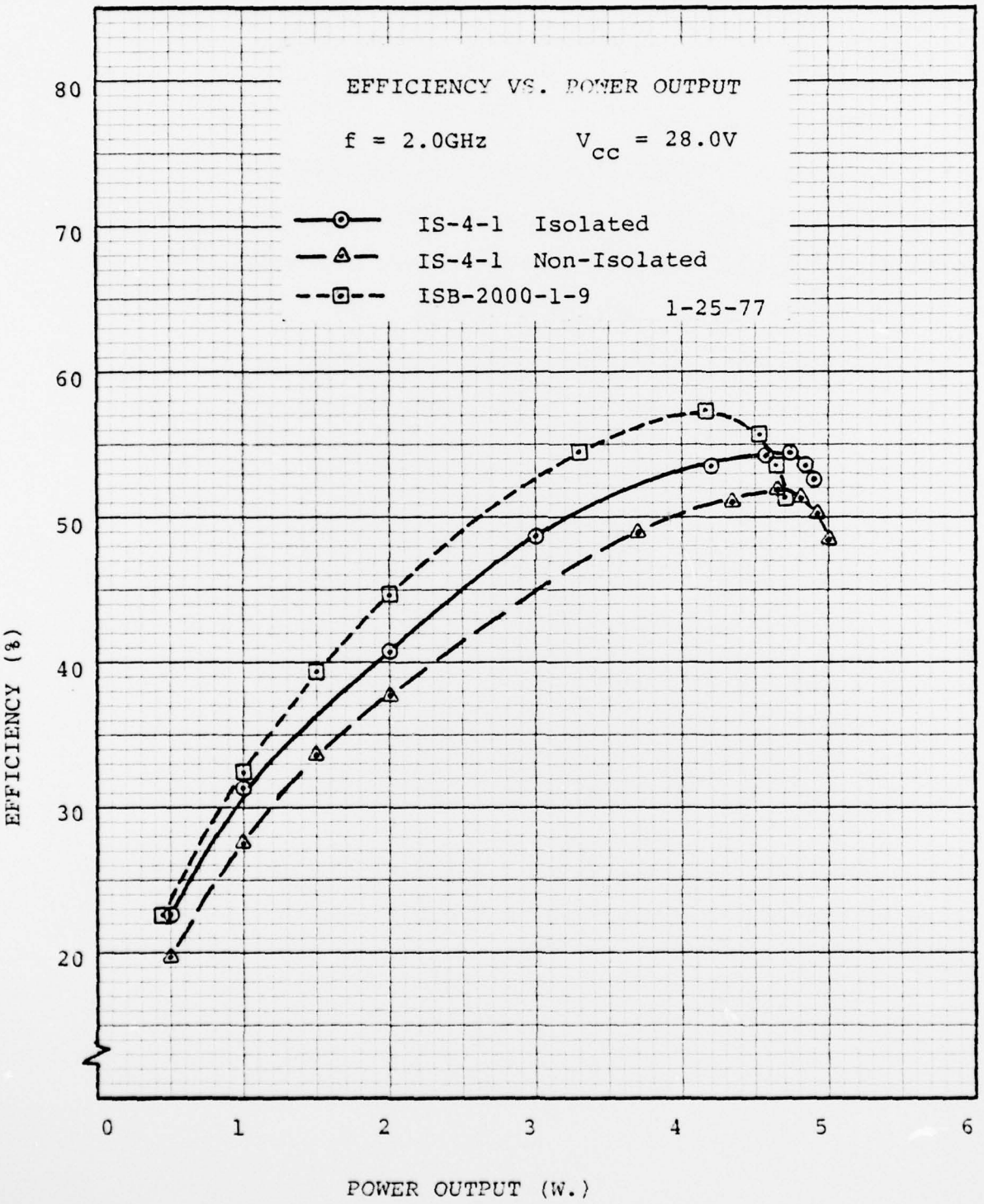

Figure 19. Efficiency vs. Power Output.

position. This dissipated power level is 3 times the normal operating dissipation.

3.3.4 Three Cell Device

In order to verify the ability of the isolated device to be parallel combined efficiently, a three cell version, Figure 20, was constructed and compared to the one cell version at 1.5 GHz. The devices were tested both CW and long pulse (500μs, 10%). The relative performance of the devices is characterized by a factor, η, not to be confused with collector efficiency, η_c .

$$\eta = \frac{P_{N\ SAT}}{N\left(P_{1\ SAT}\right)}$$

where

N = #of cells

$P_{1\ SAT} = P_{SAT}$ for a one cell device

$P_{N\ SAT} = P_{SAT}$ for a multicell device of N cells

For the one and three cell devices the performance is shown in Figure 21 and 22 and summarized in Table 3.

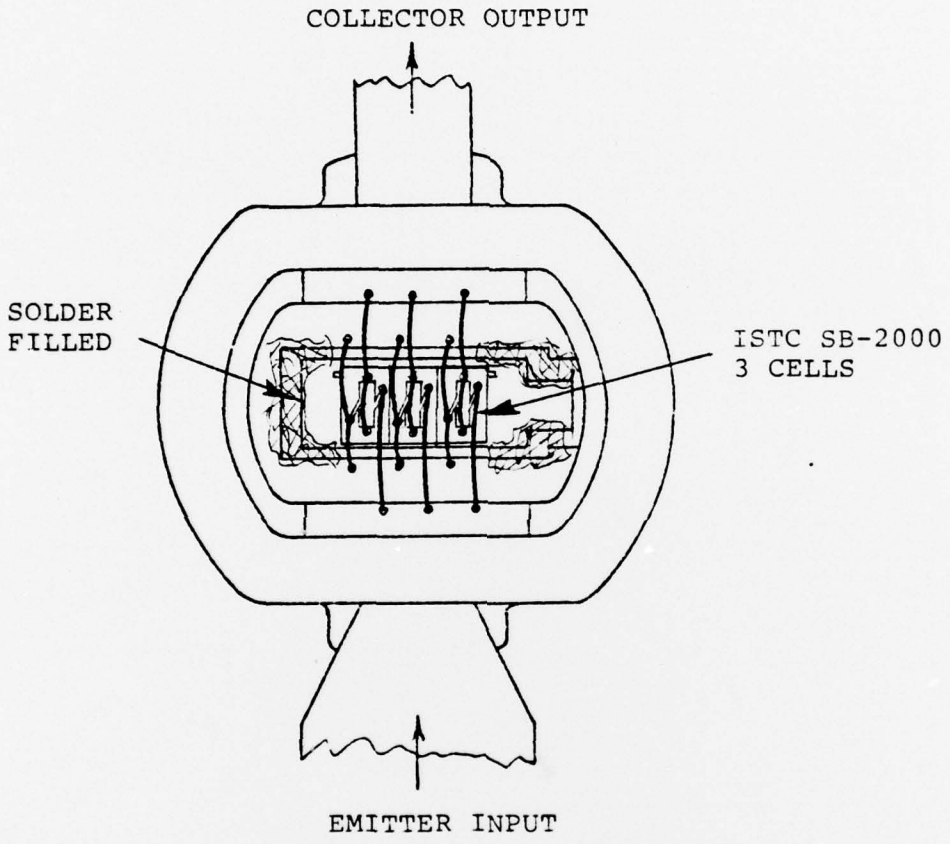

Figure 20. Isolated Three Cells, ISTC SB-2000.

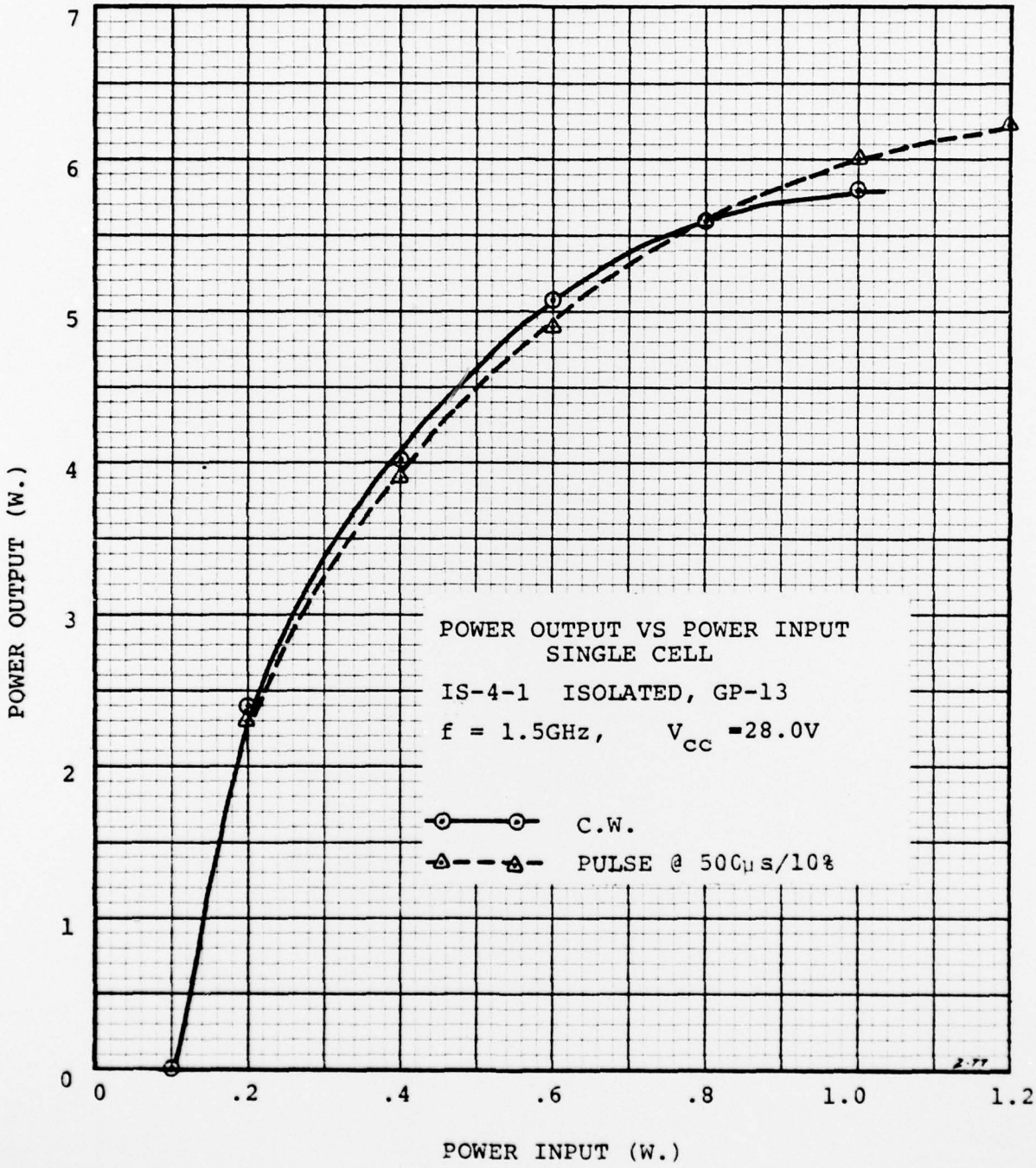

Figure 21. Power Output vs. Power Input Single Cell.

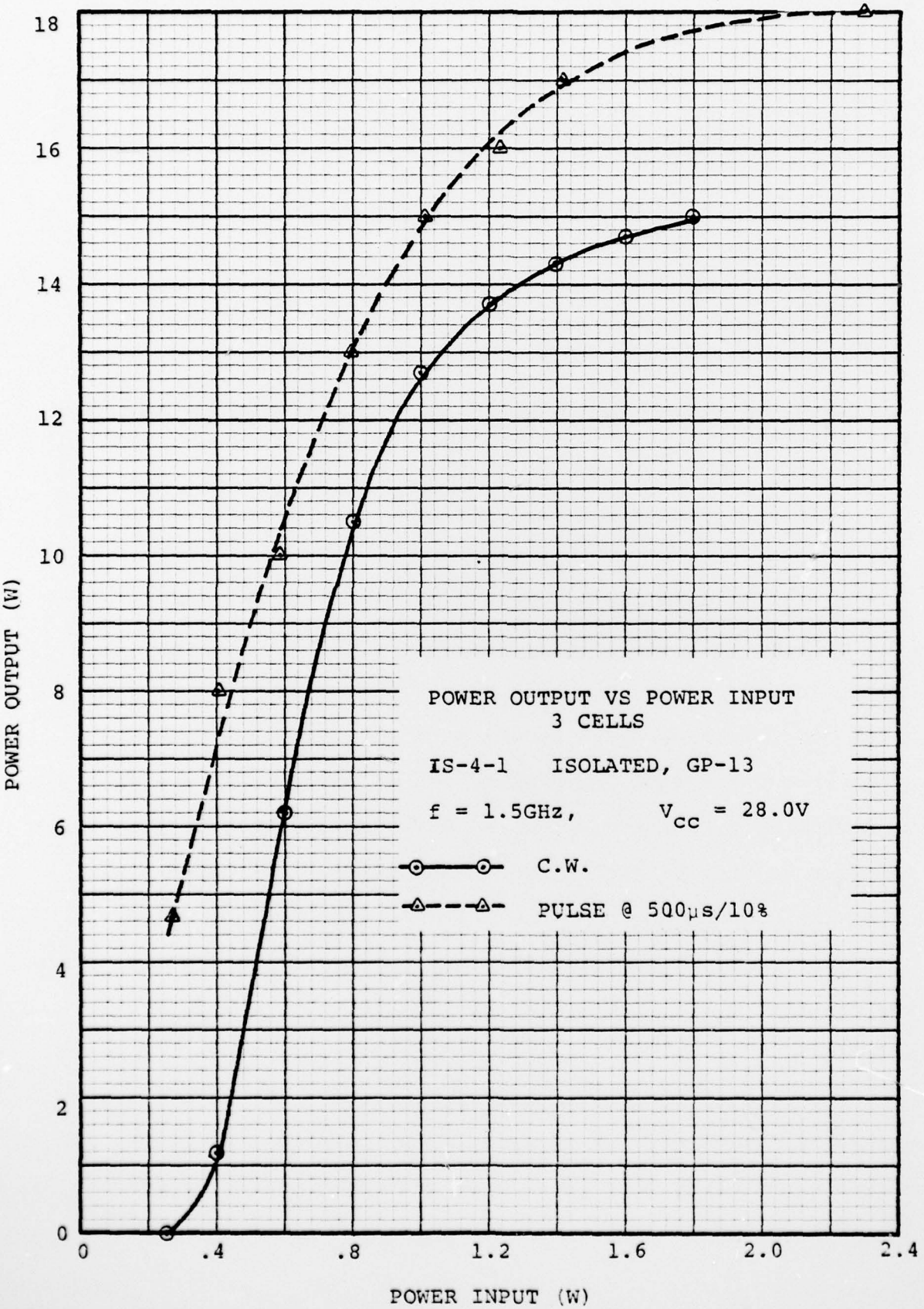

Figure 22. Power Output vs. Power Input 3 Cells.

TABLE 3. P_{SAT} AND RELATIVE POWER COMBINING EFFICIENCY.

V_{cc} = 28V f = 1.5 GHz

	CW	η	PULSE (500μs, 10%)	η
1 cell	5.8W	1.0	6.2W	1.0
3 cell	15W	.86	18W	.97

In pulse mode where junction temperature is reduced, the cells combine very well to produce 97% of the maximum available power. In the CW mode there is significant heat cone interference in the BeO substrate which causes additional thermal resistance and increased junction temperature in the three cell case causing the combining efficiency, η, to be 86%. This cell combining efficiency is as good or better than conventional devices.

3.3.5 Six Cell Device

The contract specification outlined a 30W long pulse device as a contract goal. The specifications for this device are listed in Table 4.

To produce 30W, six cells are required. These cells are arranged in two groups of three as shown in Figure 23 . The 30W devices were tested long pulse only and would typically produce 31W

TABLE 4. L-BAND SPECIFICATIONS.

Power	30 watts
Pulse Width	500 μsec
Duty Factor	10%
Efficiency	40%
Frequency Range	1.0 to 1.5GHz
Gain	7dB
Bandwidth	10%
Peak Hot Spot	$<180^{\circ}C$

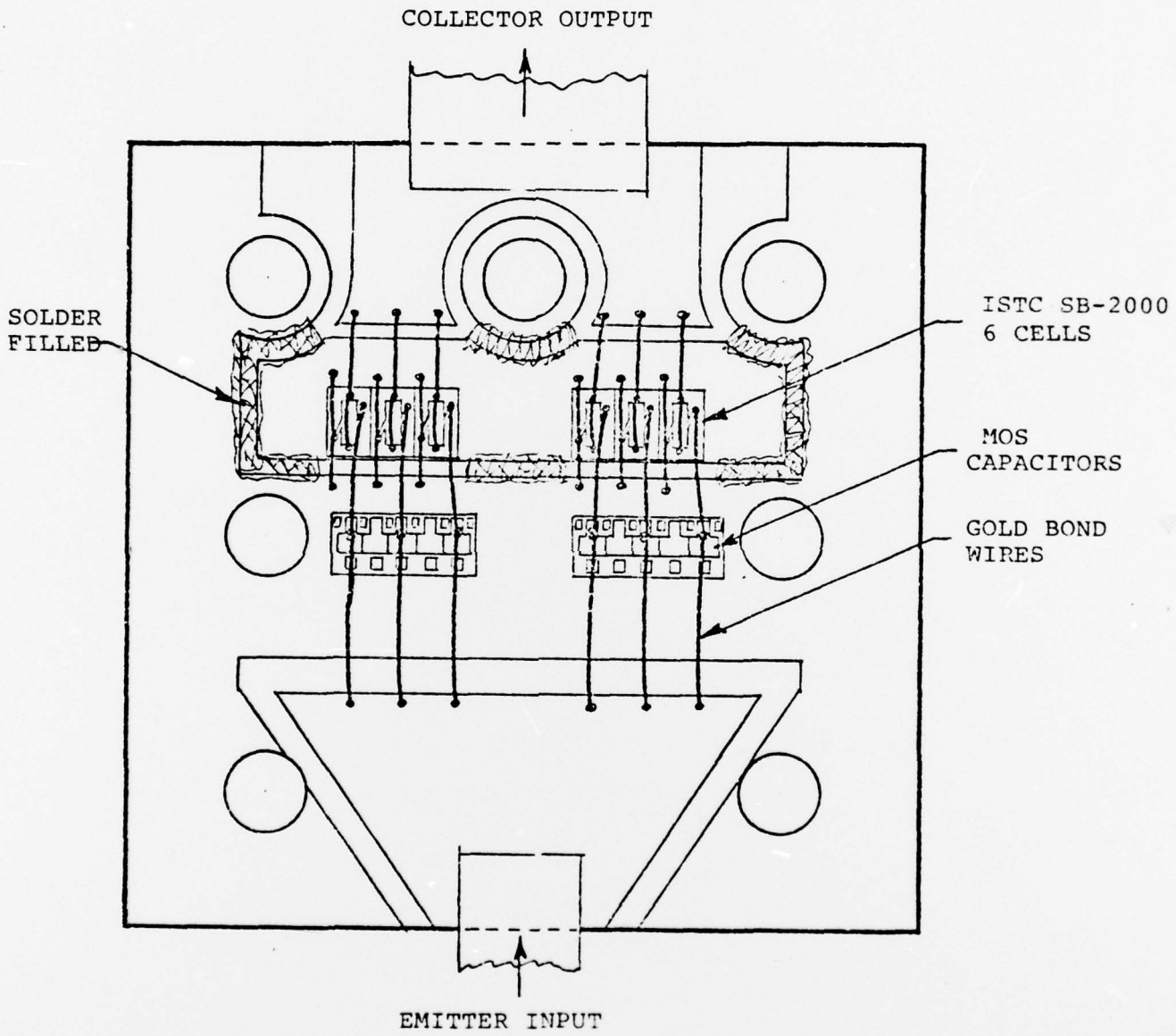

Figure 23. Isolated Six Cells, ISTC SB-2000.

peak power at a supply voltage of 28V dc with a gain of 8.2 dB and collector efficiency of 48% at a frequency of 1.5 GHz. The devices were mounted on a BeO carrier for ease of testing. Very slight (<0.2 dB) pulse droop was noted at the 30W level.

3.3.6 Junction Temperature and Thermal Resistance

To check the temperature and thermal resistance of the devices the single chip units were tested using the infrared microscope. Θ_{jf} for the devices in GP-13 package was 14°C/W, with maximum hotspot temperature of 99°C.

3.3.7 Monolithic Matching Networks

A Monolithic input matching network for a 5-cell SB-2000 transistor was fabricated during Phase I of this contract and described in Phase I Final Report - N00014-75-C-0405. The RF results obtained from the structure at that time, were quite poor as the material and process parameters had not been optimized. However, work continued on the networks as originally designed and much better results were obtained toward the completion of Phase II of this contract.

The original design called for a high Z_o air-dielectric transmission line to be used as an inductor. A polysilicon dielectric could be used for the inductor if the losses were not severly degraded. In the final result both air and polysilicon inductors were fabricated with excellent results. In fact, both types of network provided better performance than discrete network used as a control sample. Figure 24 shows the

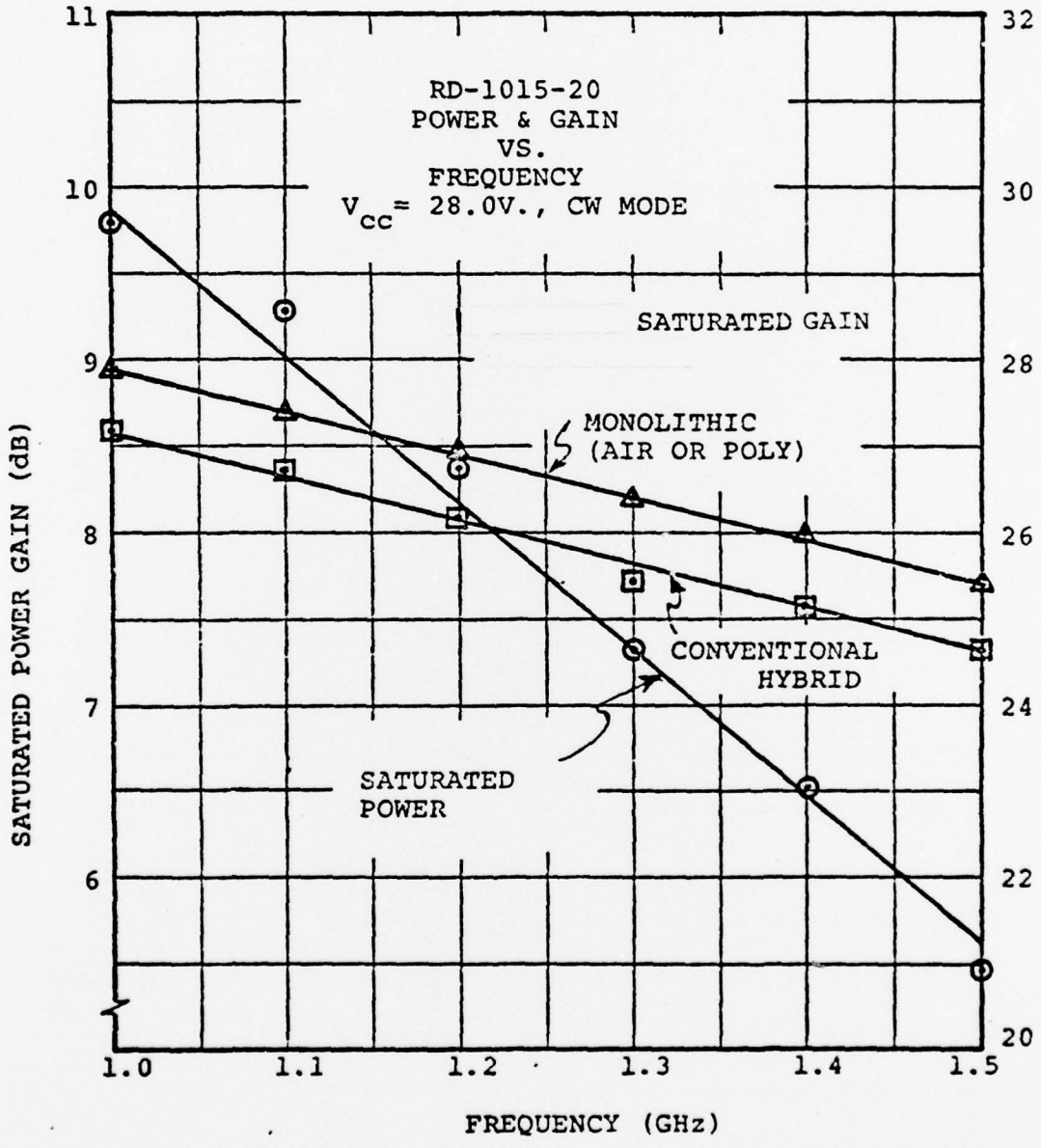

Figure 24. Power & Gain vs. Frequency RD-1015-20

performance obtained from the 5-cell SB-2000 as a broadband amplifier in the band 1.0 to 1.5 GHz. The monolithic networks provided 0.3 dB more gain than the conventional hybrid.

Small signal tests on a test structure of the polysilicon inductor have shown an attenuation of 0.4 dB/cm at 3.0 GHz for a 0.33 cm section of 80 ohm transmission line.

The excellent performance obtained from both the large signal and small signal tests demonstrates that both the losses and characteristic impedances of the polysilicon inductors are adequate for use as elements of future designs of silicon monolithic circuits.

SECTION 4

PHASE II CONCLUSIONS

4.0 CONCLUSION

High power monolithic transistors which will operate in the L-band range have been demonstrated. The monolithic transistor is a top collector contacted pulse transistor that is electrically isolated from the silicon substrate and is suitable for integrating into a single, monolithic, lumped element, internally matched structure. TRW Semiconductors has also demonstrated low loss monolithic matching inductors and capacitors on silicon substrates. Both the active and passive elements are batch fabricated by compatible processes, hence co-processing is possible.

As an added benefit, the electrically isolated monolithic transistor can be mounted into a package that no longer requires costly BeO for isolation. This improved packaging technique will be much less expensive and be potentially more reliable than the present hybrid on BeO techniques.

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