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HARDWARE TO INTERFACE A COMPUTEK GT-50 GRAPHIC TABLET WITH A DIGITAL COMPUTER

Report 77-0062

DAVID W. TAYLOR NAVAL SHIP RESEARCH AND DEVELOPMENT CENTER

Bethesda, Md. 20084

HARDWARE TO INTERFACE A COMPUTEK GT-50 GRAPHIC TABLET WITH A DIGITAL COMPUTER

by

James R. Carlberg

Matthew Yuschik

COMPUTATION, MATHEMATICS, AND LOGISTICS DEPARTMENT
RESEARCH AND DEVELOPMENT REPORT

January 1977

Report 77-0062

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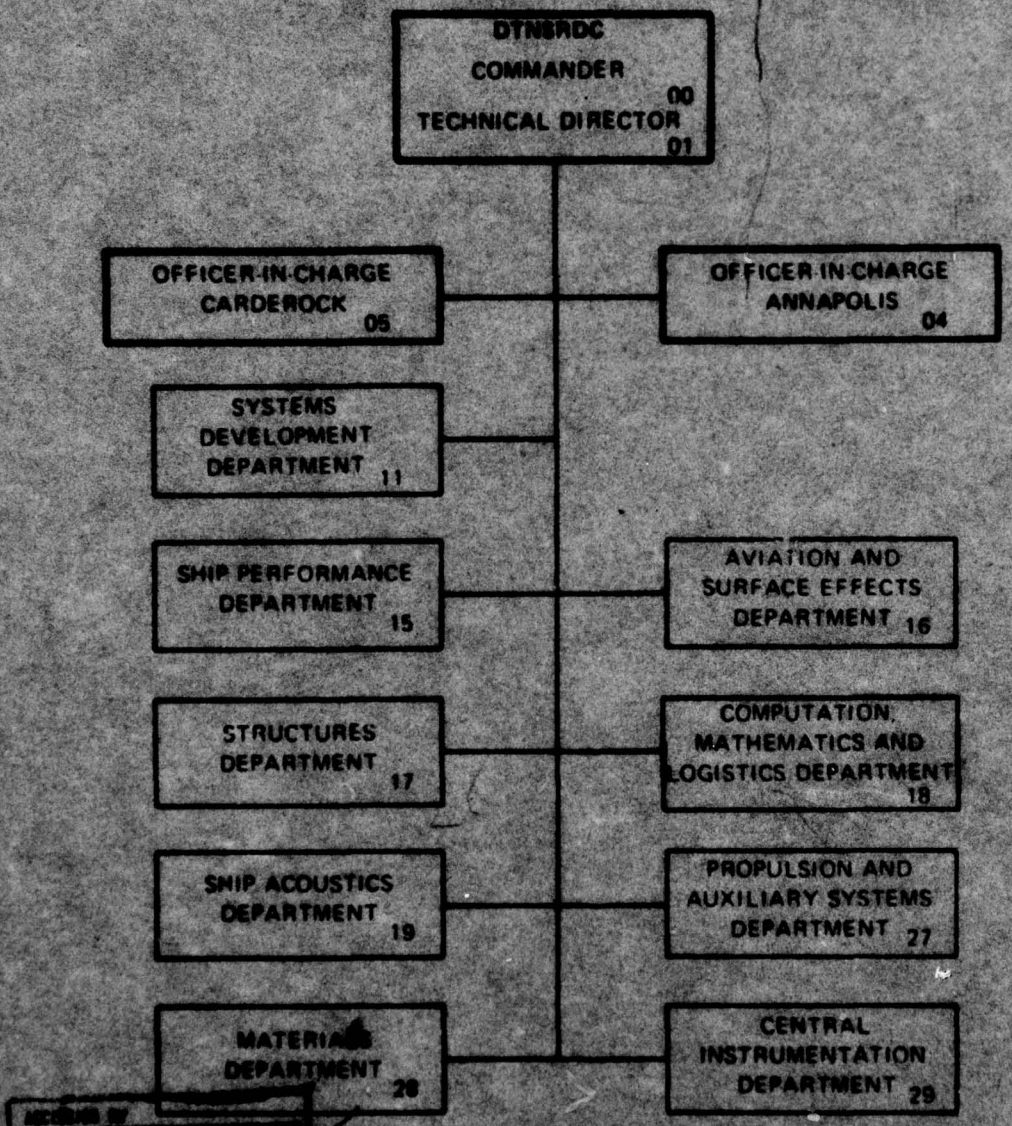

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Circuitry has been developed to permit a Computek GT-50 Graphic Tablet to be easily hooked up to any digital computer having an analog-to-digital converter. The Computek Tablet indicates the successive locations of a special pen traveling across the tablet surface as a series of digital coordinates. The circuity described represents each new set of digital coordinates. The circuitry described represents each new set of digital coordinates as a

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deviation from the previous set. Each deviation is represented as an analog voltage. The resulting analog signal is subsequently converted by an analog-to-digital converter into the binary representation required for use with a digital computer. This method of working with only the deviations of the successive pen positions allows the bandwidth needed to describe the movement of the pen across the table to be reduced. The accuracy of the signal describing the pen movement is assured by maintaining a large analog output signal-to-noise ratio.

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ABSTRACT

Circuitry has been developed to permit a Computek GT-50 Graphic Tablet to be easily hooked up to any digital computer having an analog-to-digital converter. The Computek Tablet indicates the successive locations of a special pen traveling across the tablet surface as a series of digital coordinates. The circuitry described represents each new set of digital coordinates as a deviation from the previous set. Each deviation is represented as an analog voltage. The resulting analog signal is subsequently converted by an analog-to-digital converter into the binary representation required for use with a digital computer. This method of working with only the deviations of the successive pen positions allows the bandwidth needed to describe the movement of the pen across the tablet to be reduced. The accuracy of the signal describing the pen movement is assured by maintaining a large analog output signal-to-noise ratio.

INTRODUCTION

A Computek Model GT-50 Graphic Tablet serves as the input device for the handprinted character recognition system developed by the Pattern Recognition Research Group at the David W. Taylor Naval Ship Research and Development Center (DTNSRDC). Special hardware and software has been developed within the Group to interface the Graphic Tablet with the Center's CDC 6700 computer.

The Graphic Tablet interprets the successive characters printed on the tablet face as a stream of digital positional information. The special circuitry described within this report transforms this digital positional information into a series of incremental movements which are then represented as an analog voltage and fed into the analog-to-digital (A/D) converter to be changed into the binary format which the computer requires.

The advantages of projecting successive pen-position locations as changes from the previously recorded pen locations rather than as a series of independent locations is that the signal bandwidth needed to transmit these changes is significantly reduced. This reduced bandwidth requirement enables an ordinary telephone line to be used to connect the graphic tablets with the computer so that it becomes practical to locate the graphic tablet some distance from the computer. Moreover, this analog representation allows the Computek Tablet to be hooked up directly to any general purpose computer having a three-channel A/D converter.

The handprinted character recognition system configuration is shown in Figure 1. The output from the interface is digitized by an A/D converter attached to the CDC 1700 digital computer and written onto magnetic disk. This disk information is then preprocessed on the CDC 1700 and transmitted to the CDC 6700 digital computer for further processing and eventual character recognition, using a recognition scheme* implemented with GIRL.[1]

The hardware components of the interface are described in the pages that follow. Diagrams of the various components are included in Appendix A. Logic gates used in implementing the interface are described in Appendix B. Appendix C describes the power supply and lists the wiring connections between the printed circuit boards and the connectors.

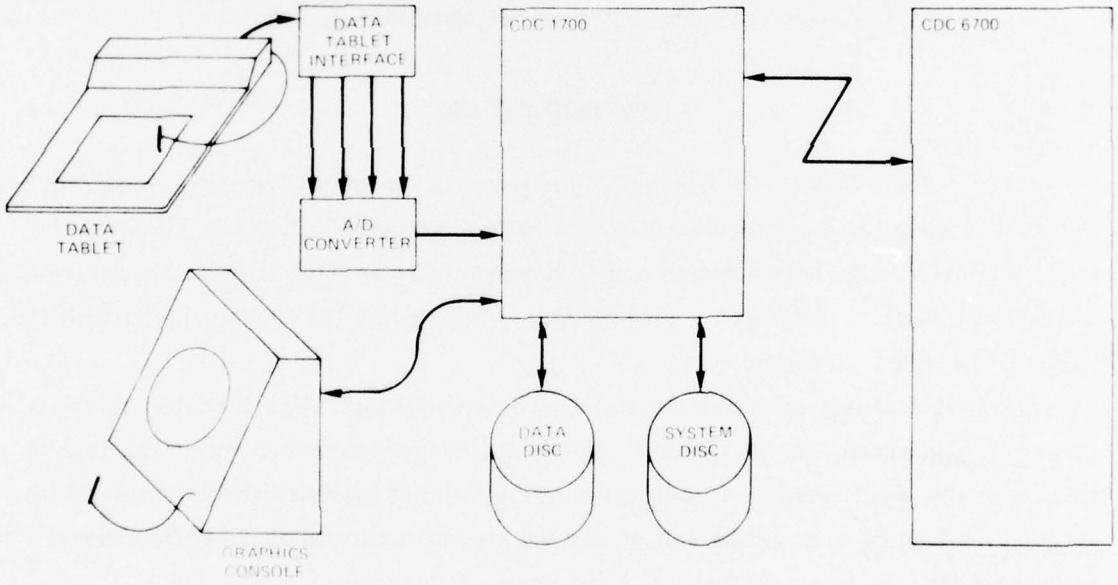

Figure 1 – Handprinting Recognition System Configuration

*Final documentation of the recognition scheme is in preparation.

[1] Berkowitz, S., *"Graph Information Retrieval Language: Programming Manual for FORTRAN Complement,"* David W. Taylor Naval Ship R&D Center Report 4137 (Jun 1973).

FUNCTION OF THE INTERFACE

GENERAL DESCRIPTION

The Computek Model GT-50 graphic tablet used for the recognition system is an electrical transducer that converts input which has been hand-drawn on the table surface into ten X-position bits and ten Y-position bits. Details of the Computek graphic tablet are available in the users manual from Computek, Inc.[2] This conversion is accomplished by encoding the electromagnetic signals that the writing pen has detected from the tablet surface. Signals that indicate pen proximity (PROX) and pen pressure (PRESS) are also available. These tablet outputs may be sampled at 800 μsec intervals when a sampling pulse (called FREE RUN) is presented by the tablet. A STROBE timing signal electrically identical to the FREE RUN signal appears simultaneously with the FREE RUN signal if the writing pen has moved since the last pulse of the STROBE signal.

The interface uses the ten coordinate bits put out by the graphic tablet to construct a 6-bit number that reflects the change in pen position from the previously recorded bits from the tablet. A block diagram of the hardware interface is shown in Figure 2. A block diagram of the difference calculator is shown in Figure 3. Since the physiological limit of normal writing speed (or equivalently, the high sampling rate of the tablet) is less than 1000 cm/sec (394 in./sec), the coordinate differences that occur between tablet output intervals can be exactly described using only five bits for the magnitude and one bit for the sign. The remaining four difference bits are always the same as the sign bit, and are thus irrelevant.

The use of the 6-bit difference approach reduces the likelihood of an error being made in the digitization by the A/D converter, since the dynamic range of the analog signal is extended and the signal-to-noise ratio improved about 16 times. The least significant bit (1sb) can be represented by a 10/64-volt signal instead of by the 1/100-volt signal required in the 10-bit approach.

The CDC-1700 computer accepts an input signal in the range of ±5 volts and converts it to a 12-bit digital word upon sampling. The sampling rate is limited to about 20,000 samples per second and may be either internally or externally controlled. When the computer is used in conjunction with the graphic tablet, the external sampling pulse is generated by the interface and it indicates the proper sampling time. The converted information is then written onto magnetic disk by the CDC 1700 and is subsequently processed for content on the CDC 6700. This scheme permits the use of a minimum amount of data to convey a maximum amount of information.

[2] *"User's Manual GT-50 Graphics Tablets,"* Bulletin GT-50M, Computek, Inc. (Sep 1970).

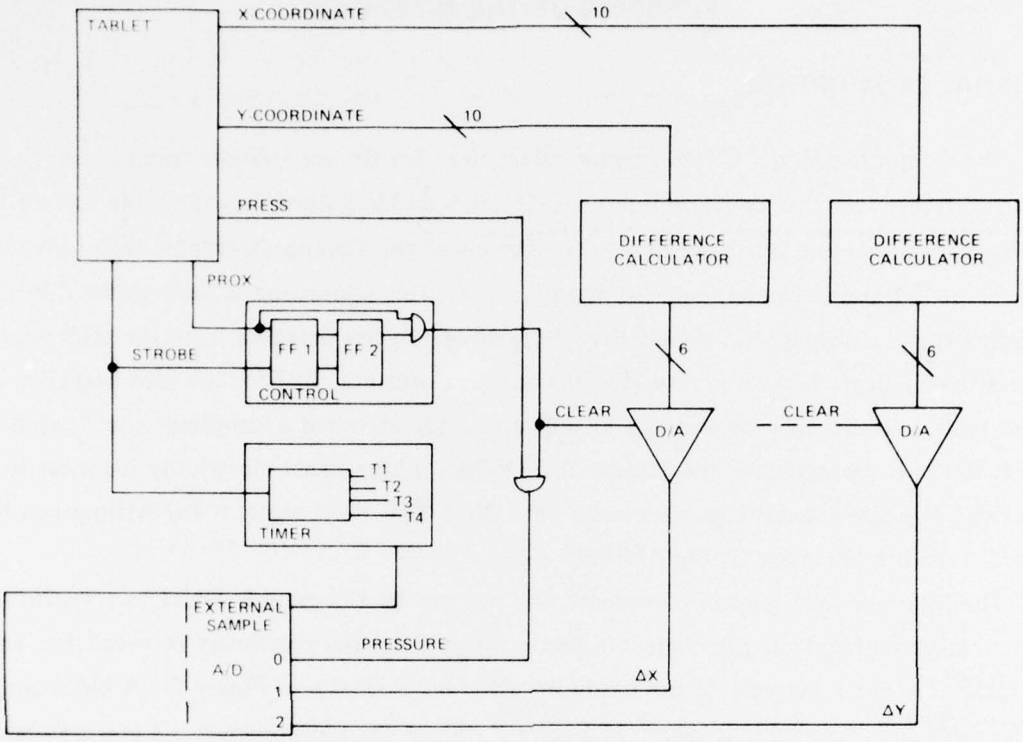

Figure 2 – The Hardware Interface

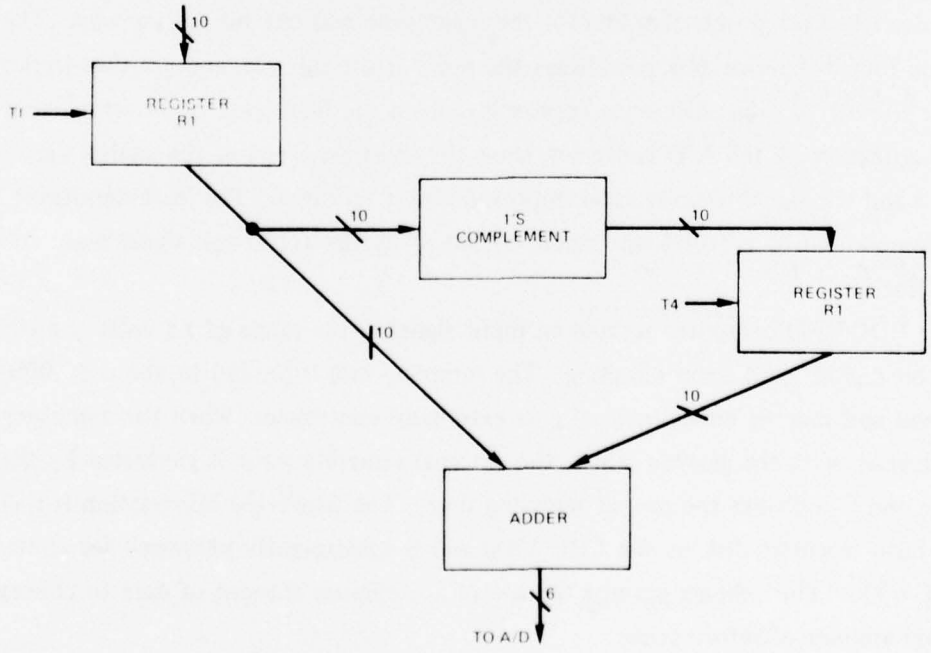

Figure 3 – Difference Calculator

Three other signals generated by the tablet - the STROBE, the PROX, and the PRESS - provide useful information, both explicitly and implicitly, about the state of the tablet. The STROBE and PROX signals are used for transmission control; the PRESS signal is transmitted along with ΔX and ΔY as a processing control.

The STROBE signal initiates the sequence of timing pulses that controls the transfer of data to the interface registers. The STROBE signal remains at a +5-volt level until a change in the position of either the X or the Y coordinate takes place, at which time the signal level drops to a 0-volt level for the duration of the tablet cycle time (FREE RUN signal). This indication from the STROBE signal is very useful, since it allows suppression of a large amount of redundant information that would otherwise be routinely generated under continuous sampling even though no change in coordinates had taken place.

During the processing of data for content, cues are useful for isolating individual characters and individual statements. Such cues are provided by the PROX signal, which is activated when the writing instrument is brought within 1 cm (1/3 in.) of the tablet surface, and by the PRESS signal, which is activated when 100 or more grams (3 oz) of pen pressure are applied (and the STROBE signal has been activated). The STROBE signal initiates a sequence of timing pulses in the interface which trigger the following actions:

1. Transfer of the tablet pen position coordinates to register R1.
2. Transfer of the sum of Register R1 and Register R2 to the input of the D/A converter.
3. Generation of a sample pulse for the CDC 1700 A/D converter.
4. Transfer of the complement of Register R1 to Register R2.

Only after the PROX signal is activated will the difference circuit obtain significant X and Y values, and only after a new STROBE signal is activated will a non-zero ΔX and/or ΔY be presented as input to the D/A converters. Note that the PRESS signal may or may not have been activated at this time. As long as the STROBE and PROX signals continue, the triplet (ΔX, ΔY, PRESSURE) will be sampled and transferred to the CDC 1700. At the same time the difference registers (R1, R2) will be updated. When the PROX signal is deactivated, the ΔX and ΔY signals are forced to a zero level, even though the STROBE signal may still indicate that sampling should take place. Just as the presence (or absence) of the PRESS signal provides a cue for the isolation of strokes, the PROX signal provides information for the isolation of entire lines of printing, providing that the user maintains the pen no more than 1 cm from the tablet while the line is being printed.

TIMING AND LOGIC DETAILS

When the STROBE signal is generated by the data tablet, indicating pen position changes, the interface must generate appropriate timing pulses and control signals. Under control of the timing pulses, data transformation takes place as follows: the present coordinate position from the tablet must be entered into register R1, and added to the complement of the previous coordinate (register R2) to construct a difference which is gated into the D/A converter and finally sampled by the CDC 1700. Four timing pulses are used to transform the coordinate positions into analog differences. Each of these pulses lasts 15 μsec; thus, the analog signal can be sampled as soon as 60 μsec after the coordinate position has been obtained from the tablet. Since the interface can generate coordinate differences at 60 μsec intervals, a sampling rate as high as 16,666 coordinates/sec can be achieved, although the tablet limits the actual rate to 1250 coordinates/sec (3750 samples/sec).

The control circuitry uses the STROBE and PROX signals from the tablet to properly gate the tablet information and sampling signals as described in the previous section. The use of two flip-flops (FF1 and FF2) with each of these signals forces the difference circuit to zero unless relevant position location is obtained. It also permits the beginning and the end of a written line to be ascertained. Timing signals T1 through T4 are used for sequencing the data transfers, and T4 is used also as the external sample pulse for the A/D converter. Figure 4 shows the relative time relationships for the timing signals (T1 through T4), the STROBE pulse, and clock signals (CL).

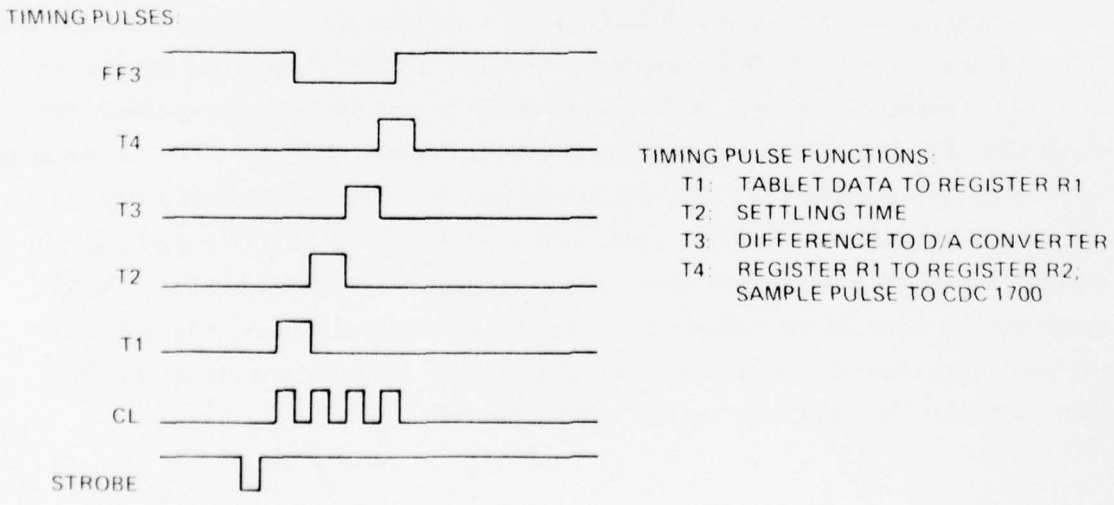

Figure 4 – Timing Pulses and Functions

CIRCUIT OPERATION

The interface consists of two functions per coordinate axis, each function located on a separate printed circuit card for each axis. One function contains the difference calculator which comprises the data storage registers and difference registers; the other contains the circuitry associated with the timing pulses and the logical control signals. The components for the interface are listed in Table 1 of Appendix A, and a functional description of the basic integrated circuit logic is presented in Appendix B.

When the tablet coordinate bits are ready to be transferred to the interface, the STROBE signal drops to zero volts, and a clock pulse T1 is sent to the data register R1 (Figure 5). This pulse gates the ten tablet coordinate bits (B1, least significant, through B10) into this register. The output of this register and that of Register R2 are directly connected to an adder register (Figure 6). Since Register R2 contains the negation of the previous tablet coordinate, the adder generates the 1's complement difference signal $\Delta X_i = X(t_i) - X(t_i - 1)$ as soon as the new position is gated into Register R1. This difference ΔX_i (and in another identical circuit, ΔY_i) is then immediately available to be transferred to its 8-bit D/A converter in 1's complement form.

The 6-bit difference (indicated by D1 through D6 in Figure 6) is transmitted to the D/A converter. The remaining two low-order bits transferred to the 8-bit D/A converter are logically identical to the sign bit. At the timing pulse T3, the differences ΔX_i and ΔY_i are gated into their D/A input buffers; at the timing pulse T4, the transformed tablet outputs of the D/A converters are sampled by the CDC 1700 computer through interface control. When pulse T4 occurs, the 1's complement of Register R1 is transferred into Register R2 where it is available to be added to the tablet coordinate position to be transferred into Register R1 at time T1 after the next STROBE signal. The fact that the outputs of the difference register are identically zero at time T4 (X_i is in R1 and $-X_i$ is in R2) is inconsequential, since no other pulse T3 will be generated until a new pulse T1 has already transferred the tablet output into Register R1. The inverted pulses $\overline{T1}$ and $\overline{T4}$ produced by the timer are used to distribute the electrical loading of the timer per se to other inverters on the data register circuit boards (Figure 5).

The sequence of signals generated by the timing and control section of the interface are initiated whenever a STROBE signal is received from the tablet. When the PROX signal is logically false, the control circuit clears (CLEAR) the D/A converter register for both ΔX and ΔY, forcing the analog voltages to represent a zero difference. Since no sample pulses (T4) will be generated during this period, the CDC 1700 A/D converter will not digitize.

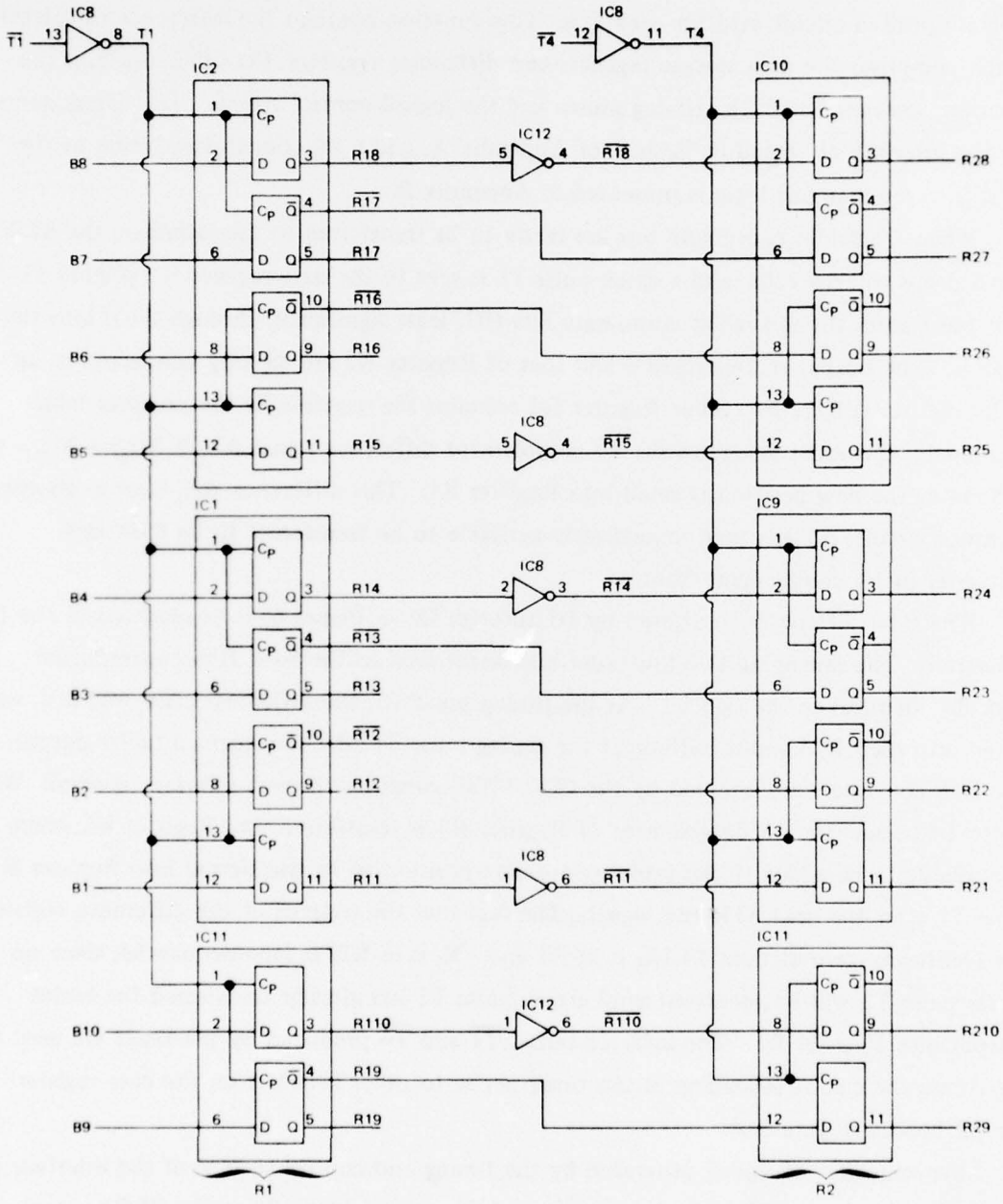

Figure 5 – Difference Calculator Registers

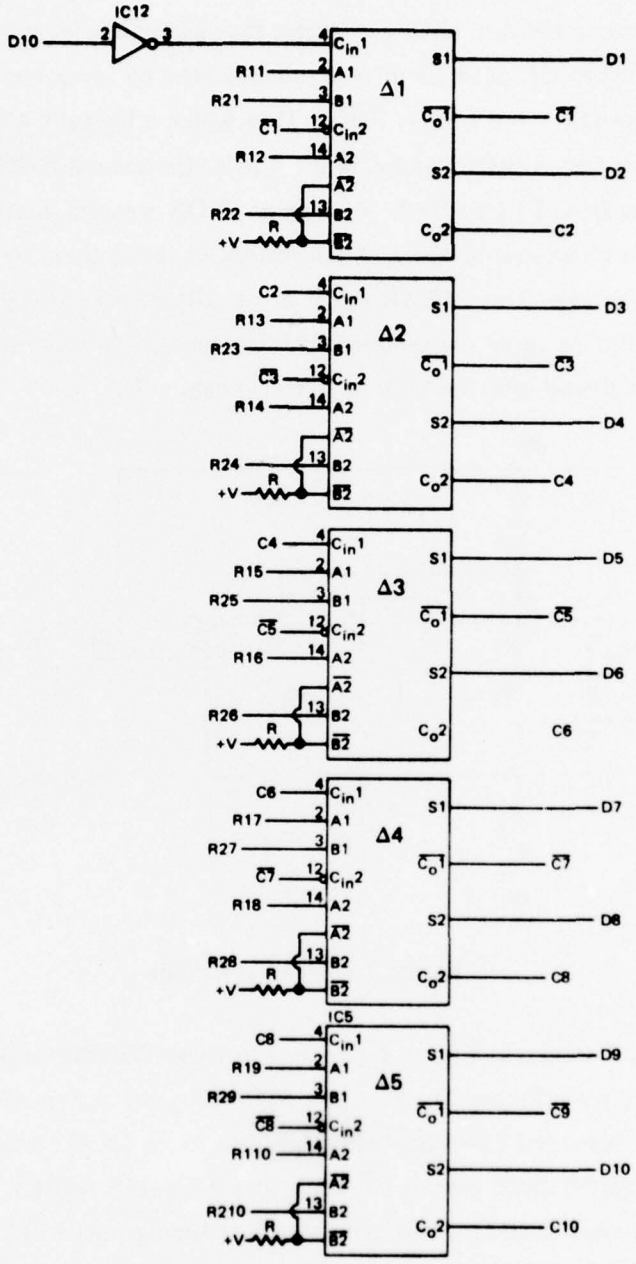

Figure 6 – Difference Calculator Adder

When the PROX signal is logically true, the timing and control circuits generate the signals necessary to produce ΔX and ΔY and to convert ΔX and ΔY into analog voltages. The control signal requires that at least two STROBE pulses be generated before it will allow ΔX and ΔY to be converted into analog voltages; thus generation of only relevant ΔX's and ΔY's is assured. A STROBE pulse counter is implemented by using two directly coupled master-slave flip-flops (FF1 and FF2 in Figure 7) in which a logically true PROX signal, in conjunction with the first STROBE pulse, will set FF1; the second STROBE pulse will transfer the set state from FF1 to FF2. As long as PROX remains in a true state, a logically true CLEAR signal will be sent to the D/A converters, enabling them to accept the input data from their storage buffers. This CLEAR signal is logically combined (by an AND gate) with the PRESS signal so as to allow the sampled PRESS signal to be true only if relevant ΔX's and ΔY's have been passed into the D/A converters (Figure 7).

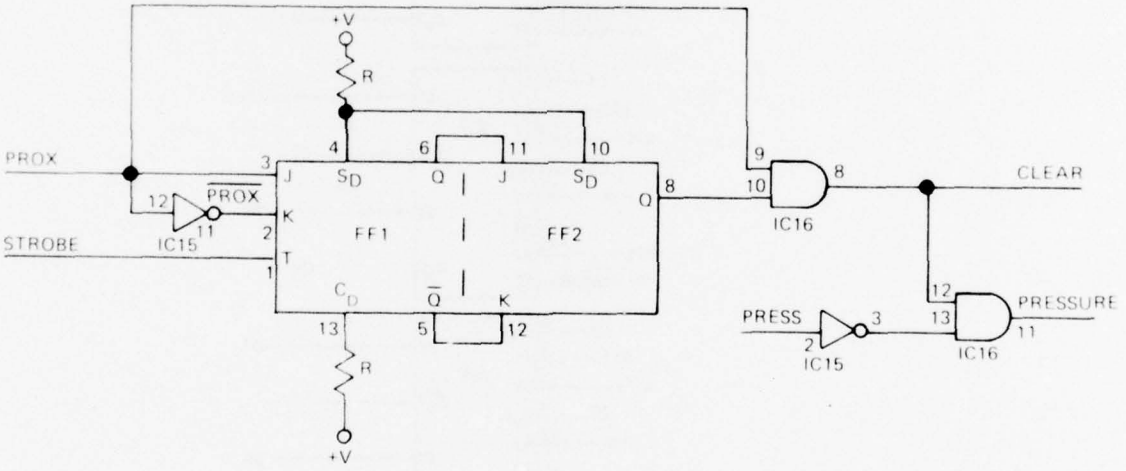

Figure 7 – Control Circuit

The timer circuit shown in Figure 8 responds to each STROBE pulse by generating a sequence of timing pulses (Figure 4). First the STROBE pulse is expanded by IC17. The trailing edge of the expanded STROBE pulse starts the clock (IC23) which generates outputs CL and $\overline{CL}$. The negated clock output $\overline{CL}$ controls a 4-bit shift register. Each of the four outputs of the shift register (Q1 to Q4) generates four timing pulses (T1 to T4, respectively). The counter and FF3 provide a logical "true" signal at the shift register input (D_S) so that one, and only one, pulse may be serially shifted through the register for each STROBE pulse occurring when the PROX signal is true (i.e., the pen is within 1 cm of the tablet). The functions that take place during each timing pulse are as follows:

T1 Tablet data is transferred to Register R1;

T2 Transients are allowed to settle;

T3 Difference is transferred to D/A converter;

T4 Register R1 is negated and its contents transferred to Register R2, and a sample pulse is generated for the A/D converter.

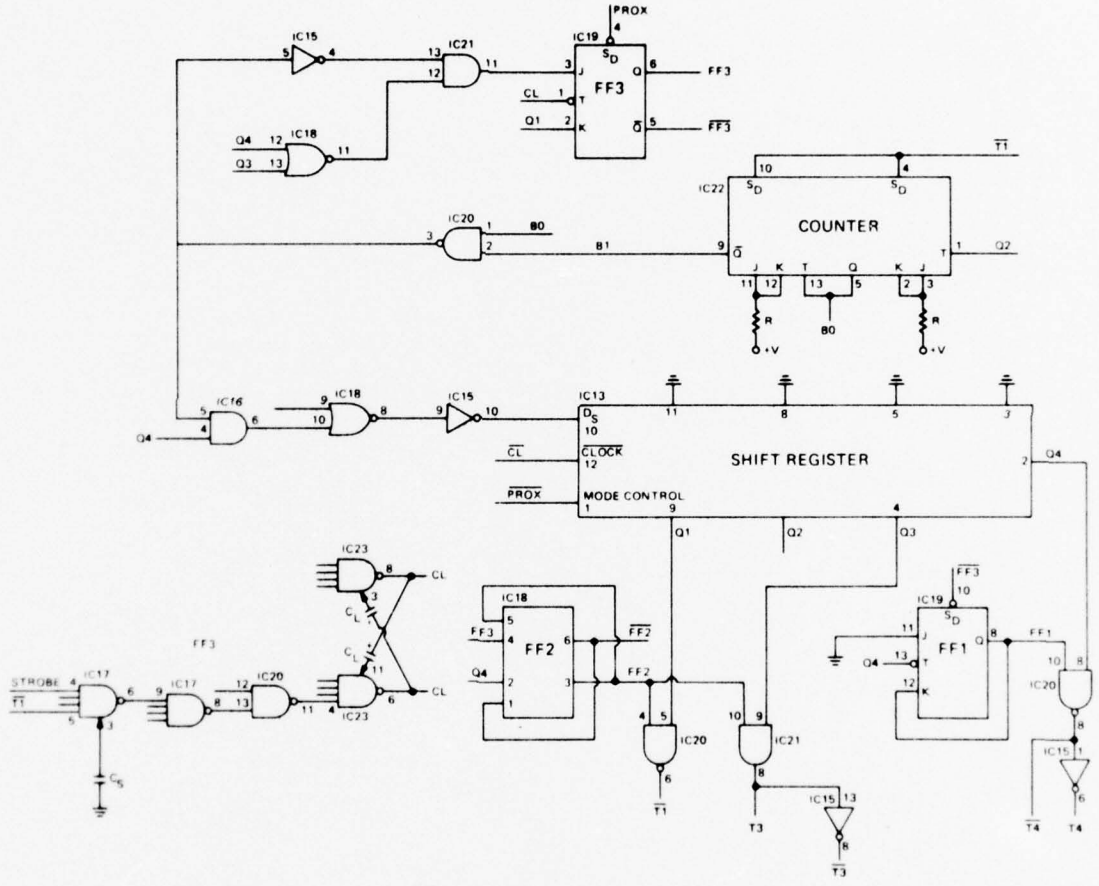

Figure 8 – Timer Circuit

ACKNOWLEDGMENTS

The authors are indebted to Dr. Sidney Berkowitz for his valuable suggestion that the difference in coordinate positions form the basis for the representation of the tablet pen movement; this technique significantly decreases the percentage of error associated with transmitted analog data.

APPENDIX A

PHYSICAL LAYOUT OF COMPONENTS

Table 1 lists the components required by the interface. Figures 9 through 12 show the relative locations of the components that make up the hardware interface. Figures 9 and 10 show the integrated circuit component layouts of the Difference Calculator and the Timer/ Control Circuit, respectively. Figure 11 shows the component layout of the D/A converter. Figure 12 shows the chassis locations of the power supplies and of the cards shown in Figures 10 through 12.

TABLE 1 – COMPONENT LIST

Circuit	Component	No. of Components
Data and Difference Circuit: (one per coordinate)		
R1 and R2	MC1814	5
△1 through △5	MC8304	5
Inverters	MC834	2
Resistors – logic	R=1kΩ	5
pull-up	R=1kΩ	10
Timing and Control Circuit:		
F1-F2	MC852	1
FF1	MC853	1
Counter	MC853	1
Shift Register	MC4012	1
Clock	MC832	1
Pulse Expander	MC830	1
AND Gates	MC1806	2
NOR Gates	MC1810	1
NAND Gates	MC846	1
Inverters	MC834	1
Resistors – logic	R=1kΩ	4
pull-up	R=1kΩ	3
Capacitors – C_L	.003μfd	2
C_S	.0022μfd	1
A/D Converter: (one per coordinate)		
Analogic	AN1808MBAL-3-C	1
Power Supplies:		
Tele-dynamics-Wanlass	7WS-1000 V=5	2
Technipower	M-14.5-0.1A V=± 15	2

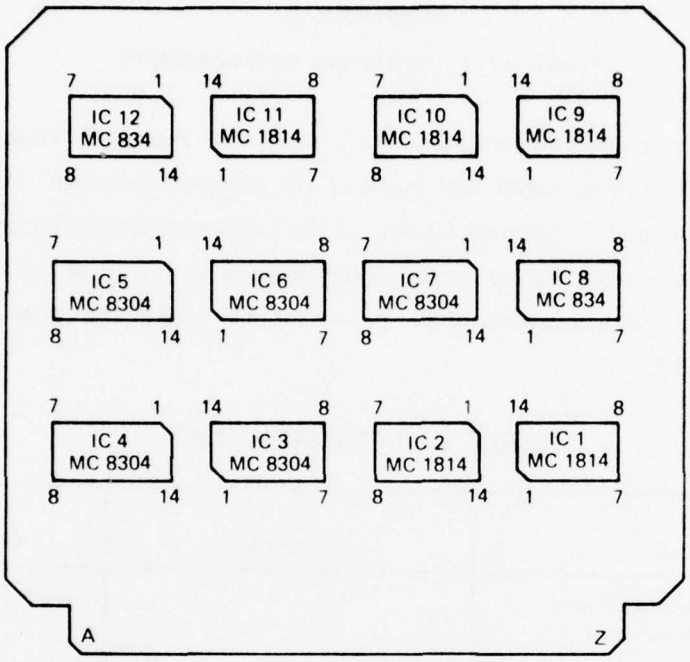

Figure 9 – Difference Calculator, Card Layout

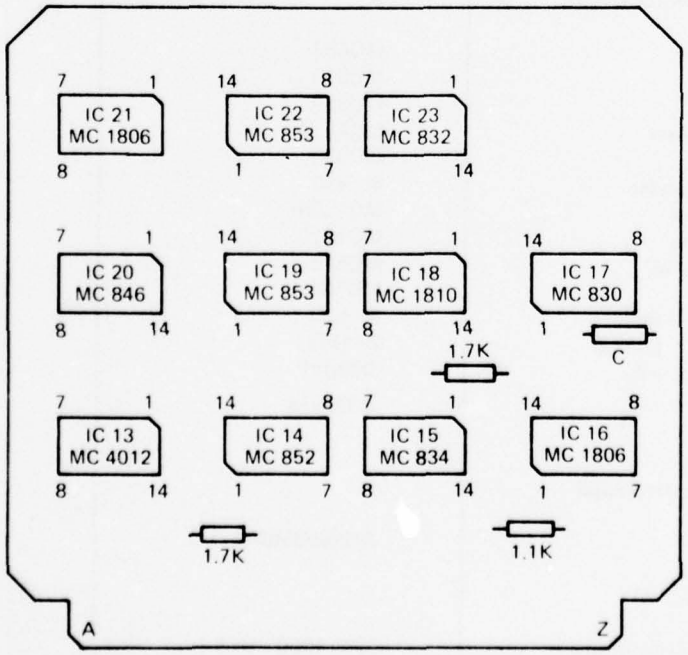

Figure 10 – Timer/Control, Card Layout

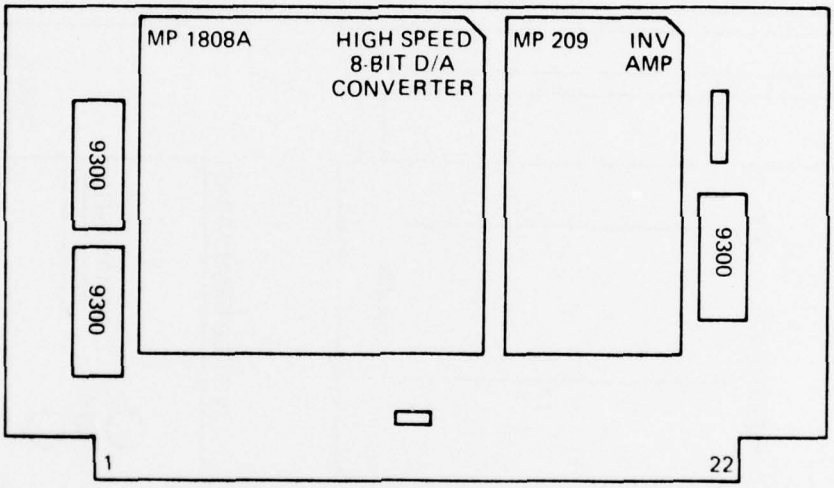

Figure 11 – D/A Converter Circuit, Card Layout

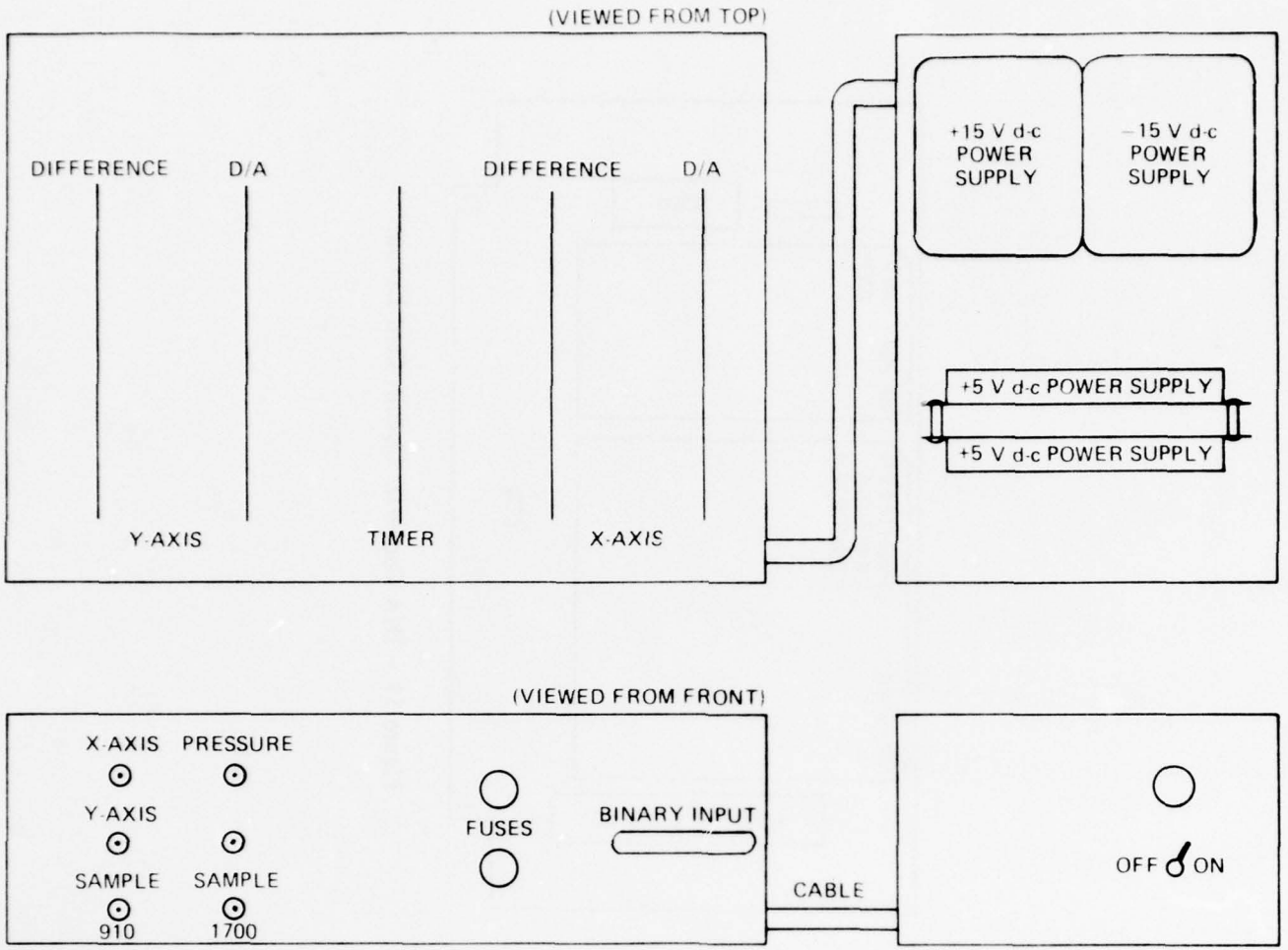

Figure 12 – Interface Chassis

APPENDIX B
LOGIC GATES

The logic gates are either diode-transistor-logic (DTL) or transistor-transistor-logic (TTL) integrated circuits. Both logics are of the general purpose type with moderate speed, good noise immunity, low noise generation, a high degree of flexibility, and economy. Typical propogation delay is about 35 nsec for a DTL gate and about 20 nsec for a TTL gate. The normal operating voltage for both types of logic is 5-volts d-c. The integrated circuits used are packaged in either 14-pin or 16-pin dual in-line packages. The component numbers indicated in the integrated circuit description are Motorola parts numbers. Figures 13 - 22 show the logic of the components and indicated pin identification numbers and logical functions.

Expandable Dual 4-Input Gate

This DTL gate (Figure 13) consists of two expandable 4-input NAND gate circuits. The integrated circuit component is an MC830.

Expandable Dual 4-Input Buffers

This DTL buffer element (Figure 13) is similar to the MC830 gate. The buffer element has triple the load driving capability of the MC830 gate. The integrated circuit element for the buffer gate is an MC832.

Hex Inverter

This DTL element (Figure 14) consists of six inverter circuits. The integrated circuit component is an MC834.

Quad 2-Input Gates

This DTL gate element (Figure 15) consists of four 2-input NAND gate circuits. The integrated circuit component is an MC846.

Dual J-K Flip-Flops

This DTL element consists of two J-K clocked flip-flops. Each flip-flop consists of two directly coupled flip-flops operating on the "master-slave" principle. Two variations of dual flip-flop elements are used in the interface hardware: one, the MC852, is shown in Figure 16; and, the other, the MC853, is shown in Figure 17.

Quad 2-Input AND Gates

This DTL gate element (Figure 18) consists of four 2-input gates, each performing the logical AND function. The integrated circuit component is an MC1806.

Quad 2-Input NOR Gates

This DTL gate element (Figure 19) consists of four 2-input gates, each performing the logical NOR function. The integrated circuit component is an MC1810.

Quad Latch

This DTL element (Figure 20) consists of four D flip-flops. When the clock C_p is high (logic state "1"), information (logic states) present at the data input D is transferred to the Q output. When the clock is low (logic state "0"), information present at the Q output will be retained. The integrated circuit component is an MC1814.

4-Bit Shift Register

This TTL element (Figure 21) is a 4-bit shift register that can be operated in either the parallel or the serial mode, the mode used being determined by the logic state of the mode control input. For parallel operation, the mode control is set to the logic state "1" and information at the D_p inputs is strobed into the register. For serial right-shift operation, the mode control is set to the logic state "0" and information is clocked into the register from the D_S input.

Dual Full Adder

This TTL element (Figure 22) consists of two full adders, each to perform the binary addition of two 1-bit numbers and the previous carry. Sum (S) and carry (C) outputs are provided from each adder. The integrated circuit component is an MC8304.

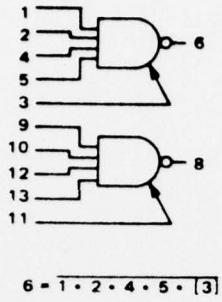

Figure 13 – Expandable Dual 4-Input Gates and Buffers (MC830 and MC832, respectively)

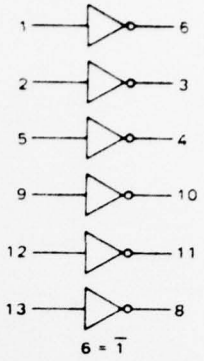

Figure 14 – Hex Inverter (MC834)

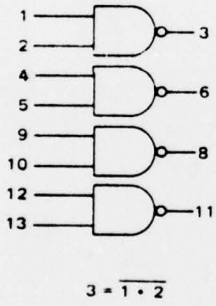

Figure 15 – Quad 2-Input NAND Gate (MC846)

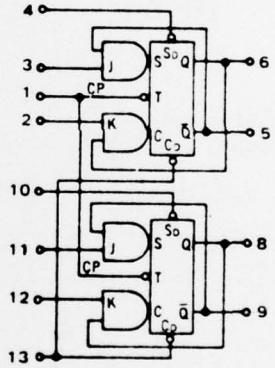

Figure 16 – Dual J-K Flip-Flop (MC852)

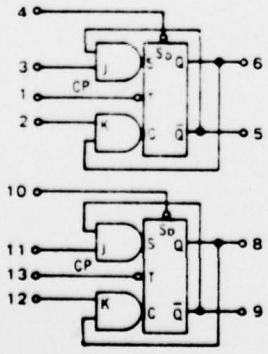

Figure 17 – Dual J-K Flip-Flop (MC853)

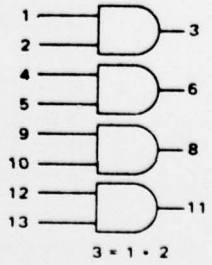

Figure 18 – Quad 2-Input AND Gate (MC1806)

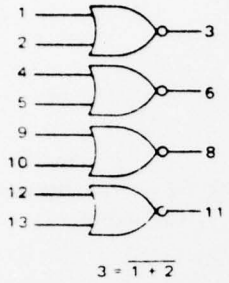

Figure 19 – Quad 2-Input NOR Gate
(MC1810)

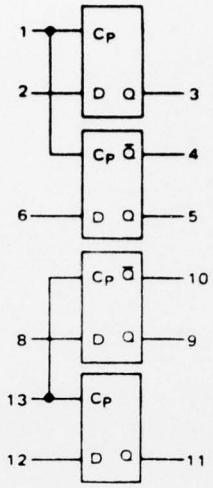

Figure 20 – Quad Latch
(MC1814)

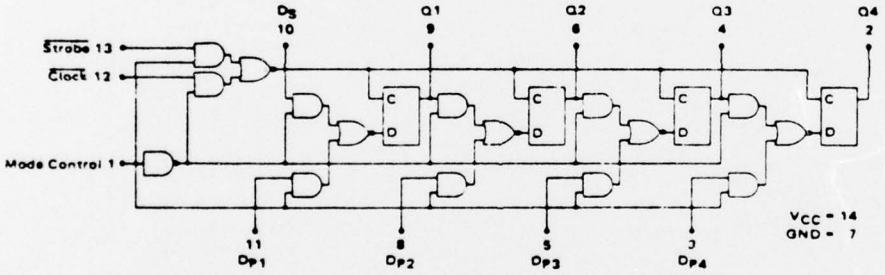

Figure 21 – 4-Bit Shift Register
(MC4012)

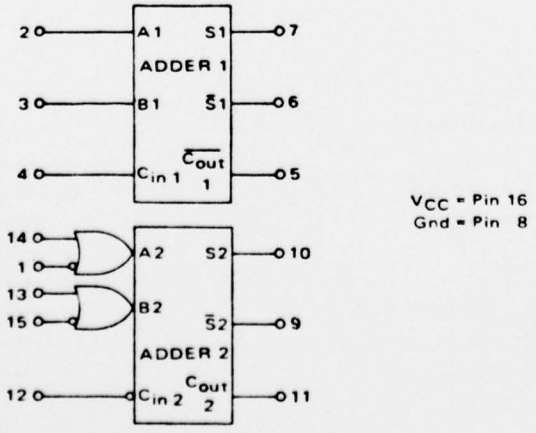

Figure 22 – Dual Full Adder
(MC8304)

APPENDIX C
WIRING LISTS AND POWER SUPPLY

POWER SUPPLIES

The power supplies used to generate the necessary direct current (d-c) bias voltage needed for the hardware interface are prepackaged units which generate d-c signals of +15volts d-c, – 15-volts, and +5-volts, using 115-volt 60-cycle input. Figure 23 shows the power supply connections. Two +5-volt d-c power supplies are used to distribute the load for the logic gates. The +15-volt d-c signal and the -15-volt d-c signal provide the biases for the D/A converter.

WIRING LISTS

The wiring lists for the Hardware Interface are presented in Tables 2 through 7. Table 2 describes the wiring from the data tablet cable connector to the circuit card connectors for the X and Y difference calculators, and for the Timer/Control circuit. Table 3 describes the wiring from the Timer/Control circuit card connector to the circuit card connectors for the difference calculators and D/A converters, and to the cable connector for the data tablet. Table 4 describes the wiring for the X-axis difference calculator, and Table 5 describes the wiring list for the X-axis D/A converter. Tables 6 and 7 describe the wiring for the Y-axis difference calculator and the Y-axis D/A converter, respectively.

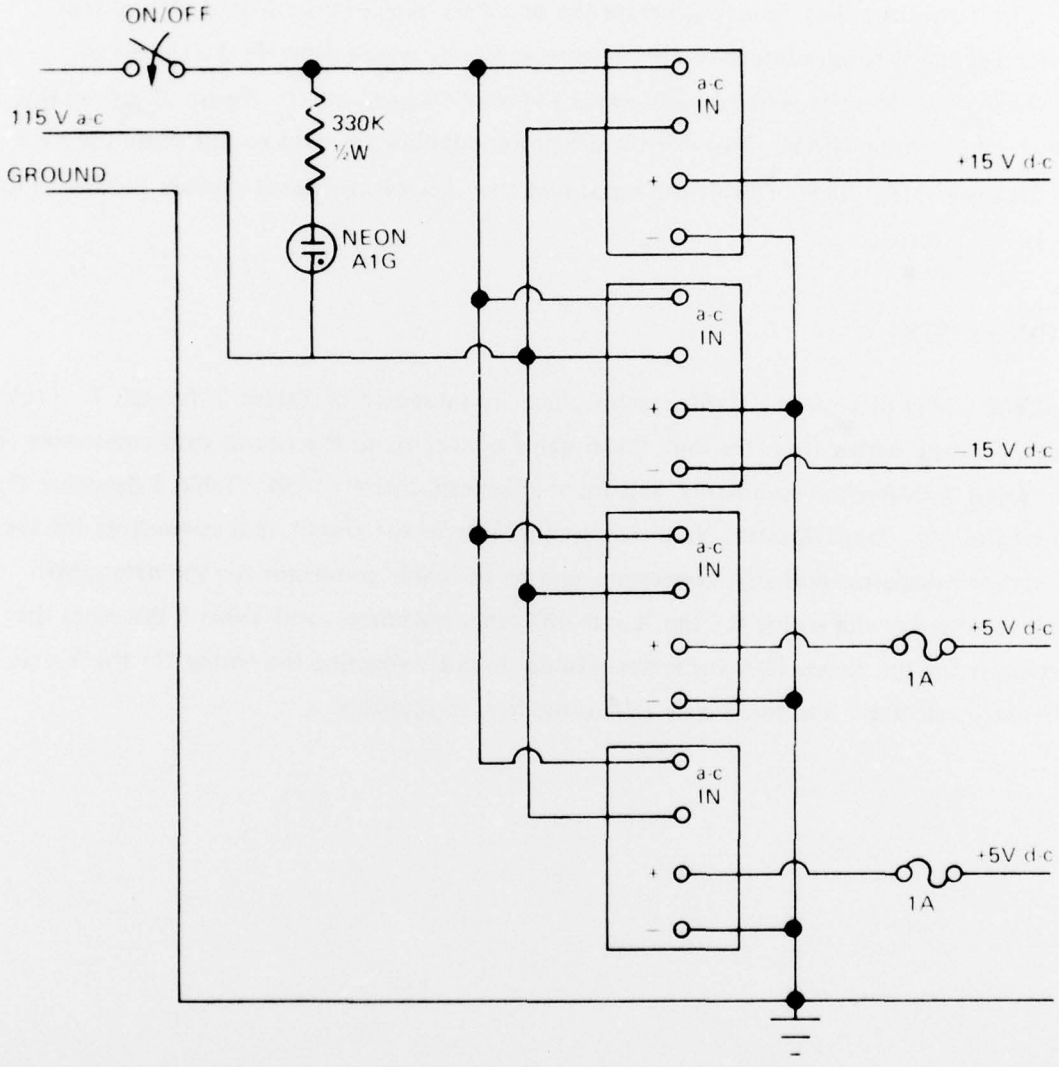

Figure 23 – Power Supply Circuit

TABLE 2 – WIRING LIST, DATA TABLET CABLE CONNECTOR

From	To	Color	Function
TABLET– 1		Blue/White	
– 2	GND	Orange/White	
– 3	GND	Green/White	
– 4	GND	Brown/White	
– 5	GND	Grey/White	
– 6	GND	Blue/Red	
– 7	GND	Orange/Red	
– 8	GND	Green/Red	
– 9	GND	Brown/Red	
–10	GND	Grey/Red	
–11	GND	Blue/Black	
–12	GND	Orange/Black	
–13	GND	Green/Black	
–14	GND	Brown/Black	
–15	GND	Grey/Black	
–16	GND	Blue/Yellow	
–17	GND	Orange/yellow	
–18	GND	Green/Yellow	
–19	GND	Brown/Yellow	
–20		Grey/Yellow	PB - 1
–21		Blue/Violet	PB - 2
–22		Orange/Violet	PB - 3
–23	Y - 3	Green/Violet	y_1 (LSB)
–24	Y - 4	Brown/Violet	y_2
–25	TIMER - 7	Grey/Violet	Pen pressure
–26	TIMER - 9	White/Blue	Proximity
–27	Y - 7	White/Orange	y_5
–28	Y - 6	White/Green	y_4
–29	Y - 8	White/Brown	y_6
–30	Y - 9	White/Grey	y_7

From	To	Color	Function
TABLET–31	Y - K	Red/Blue	y_8
–32	Y - L	Red/Orange	y_9
–33	Y - 10	Red/Green	y_{10} MSB
–34	X - 5	Red/Brown	x_3
–35	X - 6	Red/Grey	x_4
–36	X - 7	Black/Blue	x_5
–37	X - 8	Black/Orange	x_6
–38	X - 9	Black/Green	x_7
–39	X - K	Black/Brown	x_8
–40	X - L	Black/Grey	x_9
–41	X - 10	Yellow/Blue	x_{10} MSB
–42	Y - 5	Yellow/Orange	y_3
–43		Yellow/Orange	Free-run
–44	TIMER - 5	Yellow/Brown	Strobe
–45		Yellow/Grey	Function switch A
–46		Violet/Blue	Function switch B
–47		Violet/Orange	Keyboard switch
–48		Violet/Green	Ready
–49	X - 3	Violet/Brown	x_1 LSB
–50	X - 4	Violet/Grey	x_2

TABLE 3 – WIRING LIST, TIMER/CONTROL CARD CONNECTOR

From	To	Function
TIMER – 1	X-1, Y-1, GND	Ground
– 2		
– 3	X-2, XDAC-11	+5 V d-c
– 4		
– 5	TABLET-44	Strobe
– 6		
– 7	TABLET-25	Pen pressure
– 8		
– 9	TABLET-26	Proximity
–10		
–11		
–12	XDAC-B, YDAC-B	Clear Signal
–13		
–14	BNC–PRESSURE	Pressure Signal
–15		
–16	X-11, Y-11	$\overline{T1}$
–17		$\overline{T3}$
–18	XDAC-2, YDAC-2	T3
–19	X-12, Y-12	$\overline{T4}$ (also connected to TIMER-W)
–20	BNC – Sample 910	T4 Sample pulse for 910
–21		
–22	X-22, Y-22, GND	Ground

From	To	Function
TIMER – A		
– B		
– C		
– D		
– E		
– F		
– H		
– J		
– K		
– L		
– M		
– N		
– P		
– R		
– S		
– T		
– U		
– V		
– W	BNC–Sample 1700	$\overline{T4}$ Sample pulse for 1700
– X		
– Y		
– Z		

TABLE 4 – WIRING LIST, X-AXIS DIFFERENCE CALCULATOR CARD CONNECTOR

From	To	Function
X – 1	TIMER-1, Y-1	Ground
– 2	TIMER-3, XDAC-11	+5V d-c
– 3	TABLET-49	B1 (X_1) LSB
– 4	TABLET-50	B2 (X_2)
– 5	TABLET-34	B3 (X_3)
– 6	TABLET-35	B4 (X_4)
– 7	TABLET-36	B5 (X_5)
– 8	TABLET-37	B6 (X_6)
– 9	TABLET-38	B7 (X_7)
–10	TABLET-41	B10 (X_{10}) MSB
–11	TIMER-16	$\overline{T1}$
–12	TIMER-19	$\overline{T4}$
–13		
–14	XDAC-M	D1
–15	XDAC-13	D2
–16	XDAC-14	D3
–17	XDAC-15	D4
–18	XDAC-16	D5
–19	XDAC-17	D6
–20	XDAC-18	D7
–21	XDAC-Y	D8
–22	TIMER-22, GND	Ground

From	To	Function
X – A		
– B		
– C		
– D		
– E		
– F		
– H		
– J		
– K	TABLET-39	B8 (X_8)
– L	TABLET-40	B9 (X_9)
– M		
– N		
– P		
– R		
– S		
– T		
– U		
– V		
– W		
– X		
– Y		
–Z		

TABLE 5 – WIRING LIST, X-AXIS D/A CONVERTER CIRCUIT CARD CONNECTOR

From	To	Function
XDAC – 1		
– 2	TIMER - 18	T3
– 3		
– 4		
– 5		
– 6		
– 7		
– 8		
– 9		
–10		
–11	X-2, Fuse	+5 V d.c
–12	GND	Ground
–13	X-15	D2 (B7 IN)
–14	X-16	D3 (B6 IN)
–15	X-17	D4 (B5 IN)
–16	X-18	D5 (B4 IN)
–17	X-19	D6 (B3 IN)
–18	X-20	D7 (B2 IN)
–19	GND, YDAC-19	
–20	–15 V Power Supply	–15 V d.c
–21	+15 V Power Supply	+15 V d.c
–22	BNC-X AXIS	DAC Out

From	To	Function
XDAC – A		
– B	TIMER - 12	Clear Signal
– C		
– D		
– E		
– F		
– H		
– J		
– K		
– L		
– M	X-14	D1 (B8 IN)
– N		
– P		
– R		
– S		
– T		
– U		
– V		
– W		
– X		
– Y	X-21	D8 (MSB) (B1 IN)
– Z		

TABLE 6 – WIRING LIST, Y-AXIS DIFFERENCE CALCULATOR CARD CONNECTOR

From	To	Function
Y – 1	TIMER-1, X-1	Ground
– 2	YDAC-11	+5 V d-c
– 3	TABLET-23	B1 (Y_1) LSB
– 4	TABLET-24	B2 (Y_2)
– 5	TABLET-42	B3 (Y_3)
– 6	TABLET-28	B4 (Y_4)
– 7	TABLET-27	B5 (Y_5)
– 8	TABLET-29	B6 (Y_6)
– 9	TABLET-30	B7 (Y_7)
–10	TABLET-33	B10 (Y_{10}) MSB
–11	TIMER-16	$\overline{T1}$
–12	TIMER-19	$\overline{T4}$
–13		
–14	YDAC-M	D1
–15	YDAC-13	D2
–16	YDAC-14	D3
–17	YDAC-15	D4
–18	YDAC-16	D5
–19	YDAC-17	D6
–20	YDAC-18	D7
–21	YDAC-Y	D8
–22	GND, TIMER-22	Ground

From	To	Function
Y – A		
– B		
– C		
– D		
– E		
– F		
– H		
– J		
– K	TABLET-31	B8 (Y_8)
– L	TABLET-32	B9 (Y_9)
– M		
– N		
– P		
– R		
– S		
– T		
– U		
– V		
– W		
– X		
– Y		
– Z		

TABLE 7 – WIRING LIST, Y-AXIS D/A CONVERTER CIRCUIT CARD CONNECTOR

From	To	Function
YDAC – 1		
– 2	TIMER-18	T3 (DAC Strobe)
– 3		
– 4		
– 5		
– 6		
– 7		
– 8		
– 9		
–10		
–11	Y-2, Fuse	+5 V d-c
–12	GND	Ground (DIG RTN)
–13	Y-15	D2 (B7 IN)
–14	Y-16	D3 (B6 IN)
–15	Y-17	D4 (B5 IN)
–16	Y-18	D5 (B4 IN)
–17	Y-19	D6 (B3 IN)
–18	Y-20	D7 (B2 IN)
–19	XDAC-19, GND	ANA GND
–20	–15V Power Supply	–15 V d-c
–21	+15V Power Supply	+15 V d-c
–22	BNC-Y AXIS	DAC Out

From	To	Function
YDAC – A		
– B	TIMER-12	Clear
– C		
– D		
– E		
– F		
– H		
– J		
– K		
– L		
– M	Y-14	D1 (B8 IN)
– N		
– P		
– R		
– S		
– T		
– U		
– V		
– W		
– X		
– Y	Y-21	D8 (MSB) (B1 IN)
– Z		

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