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500 MHz ANALOG-TO-DIGITAL CONVERTER DEVELOPMENT PROGRAM

FINAL REPORT

MARCH 1972

AEROSPACE GROUP
HUGHES
HUGHES AIRCRAFT COMPANY
CULVER CITY, CALIFORNIA

500 MHz Analog-to-Digital Converter Development Program
Final Report

March 1972

Radar Division
AEROSPACE GROUP
Hughes Aircraft Company • Culver City, California

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INTRODUCTION

The results of a high-speed Analog-to-Digital Converter (ADC) development program are described in this report.

The report is divided into four sections as outlined below:

1. In the first section "Program Description and Results," a brief program description, the important conclusions, and results of the study are provided.
2. In the second section "Technical Discussion," the basic principle of ADC operation, terminology, basic components, and ADC configurations are described. A brief summary of the Hughes ADC philosophy is included.
3. The third section, "Breadboard Hardware Development," contains a detailed description of the hardware and its development.
4. In the last section, "Testing and Test Procedures," the testing techniques used and the performance results are presented.

PROGRAM DESCRIPTION AND RESULTS

The primary objective of this study was to establish the feasibility through analysis and laboratory experiments of a 4-bit A/D converter that could encode 500 MHz bandwidth radar signals. The study was restricted to the use of state-of-the-art solid-state devices because it appears that feasibility could be established using only this type of components.

The program was conducted in two phases. In the first phase, the high-speed conversion techniques were studied. These studies resulted in a conceptual A/D design. The conceptual paper design defined the performance criteria for the functional parts of the converter. During this phase, it was concluded that a single 500 megasample per second (Ms/sec) ADC was not feasible with the current (early 1971) technology. However, these investigations showed the feasibility of multiplexing ADCs that operate in the near 200 Ms/sec range to achieve a sample rate of 500 Ms/sec. Three ADCs each operating with a 6 ns sample period are required.* Each ADC is required to sample 250 MHz video at rates up to 170 Ms/sec. The 200 Ms/sec converter was developed during the second phase of the study.

Two breadboard A/D converters were built during the second phase of the study. Photographs of the hardware are shown in Figures 1 and 2. Block diagrams of the two converters are included in the report.** Photographs and a discussion of the digital to analog (D/A) converter ADC output observed during the "time domain test" are included in the Testing section.† This test shows the ADCs response to a maximum bandwidth video pulse input.

*See Figure 10 in the Breadboard Development Section.

**See Figure 12 in the Breadboard Development Section.

†See Figures 30 and 31.

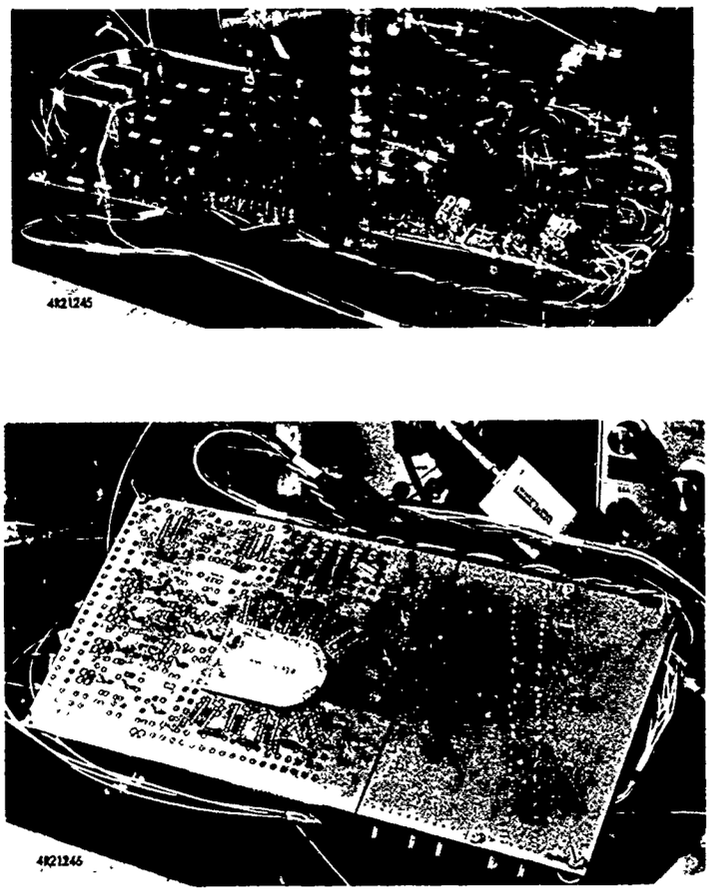


Figure 1. Model A breadboard A/D converter.

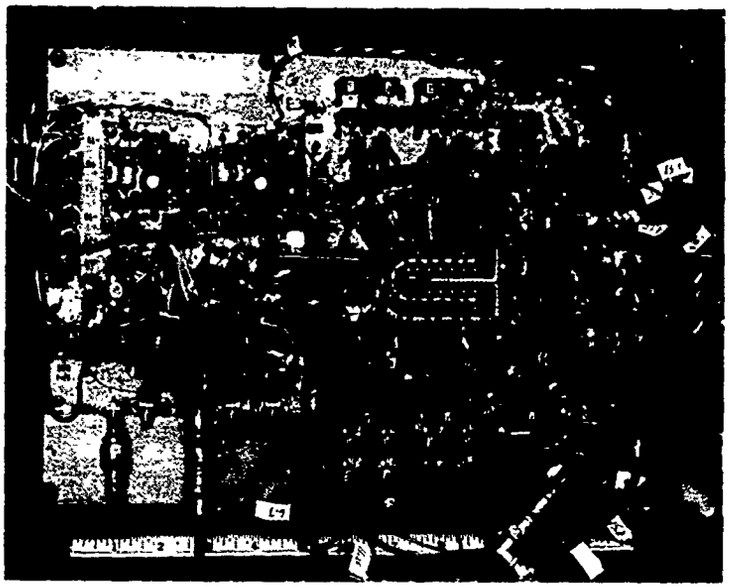


Figure 2. Model B breadboard A/D converter.

When the ADCs built in this study were tested, it was found, that the maximum complete unambiguous (to testing limits) sample rate per ADC, using standard Mecl III logic elements, was ≈150 Ms/sec. Operation to 170 Ms/sec. at 4 bits showed on the average, less than 0.5 percent of the samples were in error by more than 1 Least Significant Bit. The maximum encoding rates achieved (before gross distortions in the input signal reproduction occurred) for the first and second versions of the ADC were 195 and 255 Ms/sec, respectively. The upper speed bound was caused by a comparator response limitation. The response limitation was characterized by nondigital or ambiguous voltages at the comparator outputs (not latched to either a "1" or "0"). After thorough testing, it was concluded that substantial redesign or development of a new comparator would be required to achieve faster nonambiguous response times.

The sample-and hold circuits, driver amplifier and distribution network designs met the requirements for a 500 MHz A/D converter. The measured "aperture uncertainty" (aperture time) of the breadboard design "sample-and-hold" was less than 2.7 picoseconds rms. This low aperture time implies that the Sample-Hold could achieve 6 to 7-bit resolution at sample

rates as high as 500 Ms/sec. The experimental data also indicated that the short time stability of the timing reference generator caused most of the time jitter associated with a particular system aperture time performance.

With current "state-of-the-art" timing reference sources (≈5-10 picoseconds rms short term stability), A/D converters with 6 to 7-bit resolution capable of encoding video bandwidths of 250 MHz at sample rates of up to 500 Ms/sec appear to be feasible within the next year or so. A 6 to 7-bit converter initially would consist of several (8 to10) A/D converters connected in a parallel time-displaced multiplexed configuration. Additional effort is required to achieve hybrid implementations of present sample-and-hold encoder designs (e.g., Hughes 6-bit 65 Ms/sec, 4-bit 170 Ms/sec). As faster comparators are developed, the number of parallel converters required to achieve a given bandwidth capability can be reduced. The resulting designs would offer practical advantages such as reduced weight, power, and improved reliability and accuracy.

TECHNICAL DISCUSSION

GENERAL

The basic internal structure and operation of the high performance converters developed at Hughes are described in this section. Structurally, the ADCs of interest have two main sections: the sample-hold (S/H) section and the analog-to-digital word encoder (encoder) section.

An ADC block diagram is shown in Figure 3. The Sample-Hold section is an integral part although it is sometimes considered as a separate unit. The overall performance of the ADC is vastly improved by the construction of the two sections together. This approach minimizes delay uncertainties and matching problems by the application of a more nearly stationary input to the comparator bank in the encoder section. The high sample rates achieved by the Hughes encoders are made possible by the combined S/H and Encoder designs used.

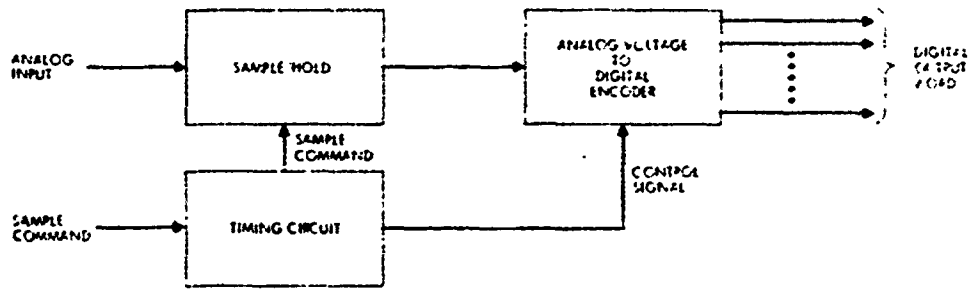


Figure 3. High speed analog-to-digital converter.

SAMPLE-HOLD UNIT

The Sample-Hold unit block diagram is shown in Figure 4. The unit consists essentially of a sample gate driven by an input amplifier. The sample gate is followed by a hold capacitor which, in turn, feeds an output driver amplifier. Its operation is as follows. A sequence of sample command pulses is applied to the sample gate. The switch (in the sample gate) is open except when a command pulse is present. The sample time is defined as that time (exactly) when the command pulse falls and the switch is caused to open. While the switch is open, the hold capacitor remains at its constant stored voltage.

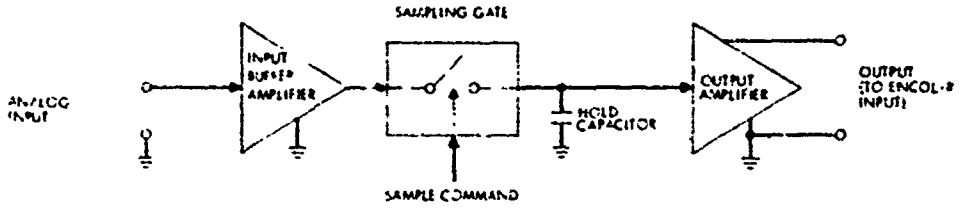


Figure 4. Sample-hold block diagram.

The held value is picked up by the comparator bank in the encoder section during this hold time in each cycle. Hence one important design consideration is to assure that the hold period is long enough for the comparators to respond to each held level before it is changed on the next cycle. A theoretical maximum sample rate achievable by the converter is the reciprocal of this hold time; achievement of this maximum rate would require an ideal S/H that acquired the analog signal input instantaneously. In practice a finite time is required for the hold capacitor to attain the input analog level.

Viewing each sample cycle in somewhat more detail, it is noted that each sample is subdivided into two series time increments:

1. Acquisition phase (while the switch is closed)
2. Hold time (while the switch is open.)

During the acquisition phase, the gate is closed and the capacitor voltage slews from its previously held level toward the new input voltage. The time required for the hold capacitor voltage to attain the input voltage (plus or

minus a defined maximum error) is the acquisition time. The remainder of the switch-closed duration, after acquisition, is the track time; during this time the hold capacitor voltage tracks the input voltage with a known phase lag or time delay. Waveforms that exemplify the operation of a track and hold function are shown in Figure 5.

From a design standpoint, the minimum switch-closed duration will permit acquisition with zero subsequent track-time, under worst case conditions. In a worst case, the initially held voltage might be as high as possible and the input might have achieved maximum negative slew rate immediately after the previous sample; it might have continued slewing at this rate

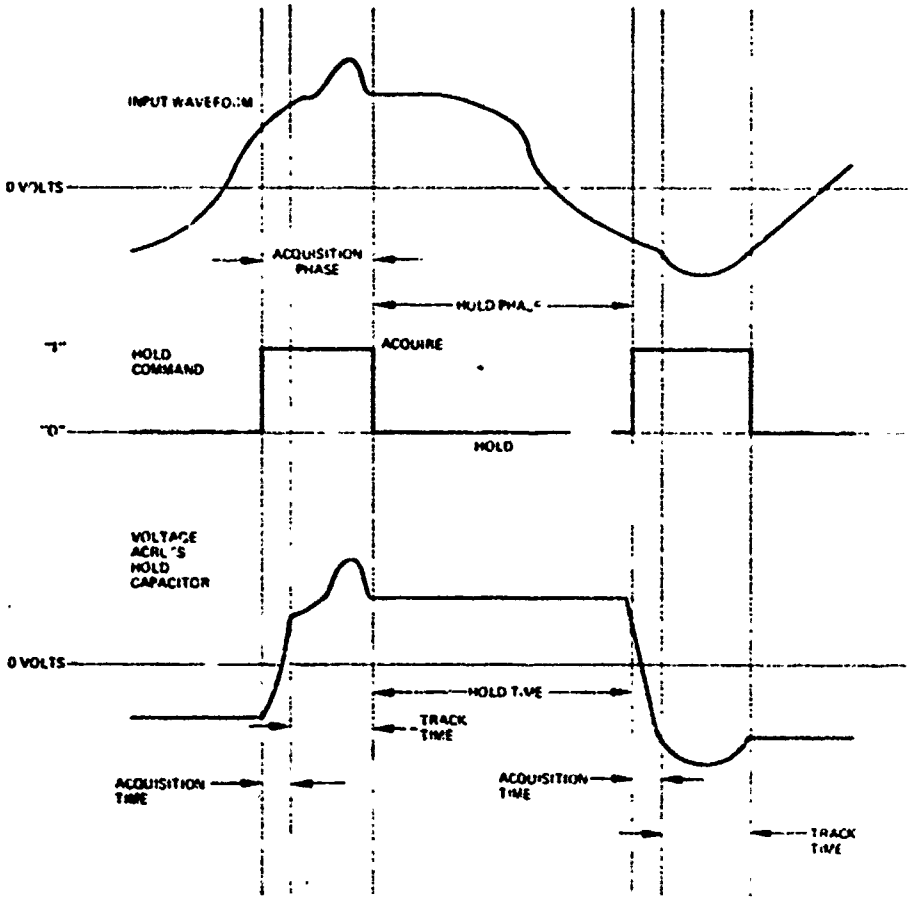


Figure 5, Waveforms exemplifying track and hold operations.

thereafter. Hence when the sample switch was later closed, the input voltage was as far from the held level as possible and moving further away at its maximum possible rate. The length of the period during which the switch must be closed must be long enough to permit acquisition even under the above worst case condition and all other equivalent to it. The reciprocal of this maximum acquisition time plus the maximum held time is the ideal ADC input word rate. The maximum acquisition time is inversely proportional to the S/H circuit performance; the maximum hold time is inversely proportional to the performance of the circuitry in the comparators and other encoder parts.

Unfortunately, even with ideal S/H (and Encoder) components, the maximum sample rate would still be limited. Time jitter in the sample command pulse train and in the control signals to the encoder corrupts ideal behavior. Jitter, component noise, etc., are treated as active and evaluated together statistically in the measurement of a specially defined quantity, aperture time. Its definition is implicit in the conditions under which it is measured, which simulate a combined worst case condition. This situation is derived as follows. In an ideal S/H, if an input signal is periodic and phase locked to the sample command pulse train, then the held level will be the same for each sample. This case would be ideal even if the sample is taken, each time, at a point of maximum input slew rate. With the samples taken at a maximum input signal slew rate point, any time jitter from sample point to sample point will correspond to a maximum proportional deviation of the held level. Any other noise in the circuitry causes still further variation of the held level, superimposed on variation caused by jitter. All such cumulative variation is artificially assumed to be caused just by timing jitter. Further, the maximum slew rate input signal is applied with the slew rate held constant during sampling. Then the total hold voltage variation can be measured and later translated back to an equivalent total time jitter (via the constant maximum input slope). A "statistical fraction" of this equivalent jitter (e.g. rms - 1σ) is defined as the aperture time. An aperture time can be defined for the S/H alone and/or for the tandem connection of the S/H and encoder; in either case, aperture time measurement provides a very useful figure of merit of total sampling uncertainty in either the S/H or the entire ADC.

Aperture time requirements can be calculated from the simple expression given in Equation (1). This equation was derived by calculating the change in sample-time required to yield a 1/2 LSB change in the hold voltage output while sampling a maximum slew rate portion of a waveform. The expression for the rms aperture time requirement (t_a) in terms of the input signal bandwidth (f) and the number of bits (N) is

$$t_a = \frac{1}{\pi f\left(2^{N+1}\right)} \tag{1}$$

This expression for t_a was derived for the total equivalent sample time jitter. Thus, the square root of the sum of the squares of the sample-hold aperture time (t_{as}) and the reference time jitter (t_{jr}) must be less than or equal to t_a as shown in Equation (2) below:

$$\left[(t_{as})^2 + (t_{jr})^2\right]^{1/2} < t_a \tag{2}$$

By rearranging Equation (2) the controlling relationship determining the sample-hold aperture time is as shown in Equation (3).

$$t_{as}^2 \leq t_a^2 - t_{jr}^2 \tag{3}$$

ENCODER UNIT

The encoder section, the second main ADC unit, receives a sequence of held analog signals from the S/H. It quantizes and encodes these input signals producing binary words that correspond to the quantized values.

Inside the Encoder, an analog reference is subdivided forming a discrete set of 2^N-1 reference levels. These levels are separated by a voltage, Q, the quantizing level. Each of these reference voltages is fed to a comparator circuit. This circuit compares the analog input to the reference level supplied to it. If the input level is above the reference, it produces a logical "1" at its output. If the reverse situation occurs, then the opposite output, a logical "0", is produced. This comparator is used in many circuit configurations to form a digital encoder function. In all configurations the output of

the comparator or comparators (as in a parallel comparator bank encoder) is/are used in a decoder to form a binary number at the encoder output. This binary number is uniquely generated for each quantizing level. The least significant bit in each binary number output corresponds to a quantizing level increment Q. In most A/D encoder configurations, the comparator is a key element. In many cases it is the limiting factor that prevents attainment of higher speed and/or accuracy-performance.

All A/D encoder configurations can be classified as one of three types: (1) Single stage parallel comparator bank encoders, (2) multistage cascaded comparator bank encoders, and (3) sequential feedback encoders. The relative advantages of these types of encoders for high speed encoding are discussed in this section. The first two encoding techniques are implemented as open loop configurations; the last technique includes the category of closed loop encoders. Because the excessive delay involved in a closed loop encoder design, it is typically not applicable to high speed A/D encoding.

The single stage parallel comparator bank encoder design provides the minimum time delay. Figure 6 is a block diagram showing this circuit configuration. It has several performance advantages over the other types of encoders. Some of its advantages are the result of the direct static control of the reference level subdivision. Another important advantage is the absence of cascaded active circuitry between the sample-hold output and the comparator inputs. This encoder uses 2^N-1 comparators and DC reference sources, where N is the number of binary bits of resolution. Each comparator

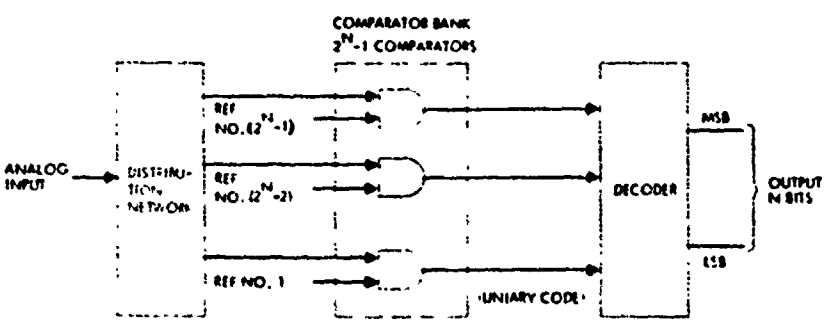


Figure 6. Parallel comparator bank A/D encoder block diagram.

is connected to a unique reference level. The operation of this encoder is described as follows.

The analog input to the encoder is applied simultaneously to every comparator analog input through a typically passive distribution network. For a given input voltage level, all comparators with reference inputs below the input signal level produce an identical output (say logical one) while those with reference levels above the input held-level, produce an identical, opposite output (say logical zero). This uniary code array formed across the ensemble of the comparator outputs is then converted to a different binary code, via the decoding network, driven by the comparators. The binary code output corresponds to a binary number proportional to the analog voltage reference level just below and nearest the input level.

Currently, comparator bank size has a practical limit due to the physical constraints of present packaging techniques. This limit is about 32 packages or 64 comparators. Therefore, at present 6 bits is a maximum resolution for the parallel comparator bank encoders. Since the number of comparators required is 2^N-1 (N = number of bits), 6 to 7 bits will probably be a practical limit for some time. For higher resolution, at high encoding rates, other encoding techniques must be used.

A second design approach, "multistage cascaded comparator/comparator bank encoders" has been used to overcome the above limitation. A block diagram of the design is shown in Figure 7.

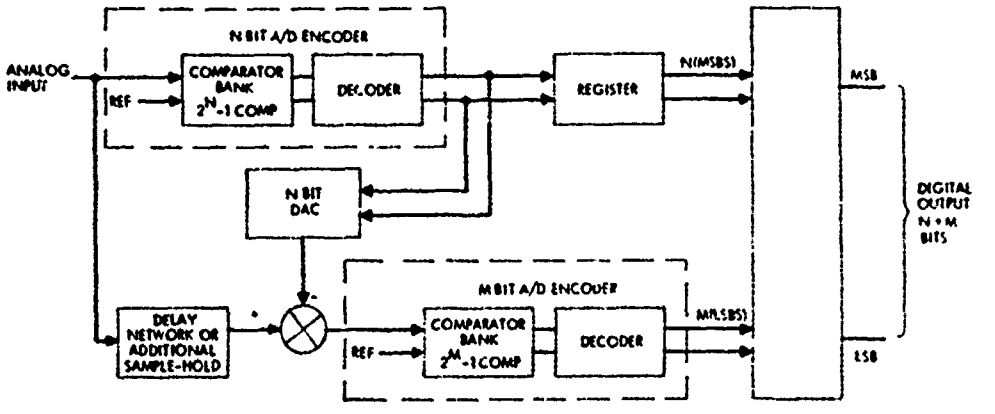


Figure 7. Two-stage cascaded [N+M] bit A/D encoder without overranging, block diagram.

The encoding process takes place in as many encoding steps as there are cascaded stages. This process is sometimes called a subranging technique, because each cascaded stage encodes a subrange or fraction of the analog input applied to the previous stage. This subranging process results in the resolution for this type of encoder as the sum of the number of bits in each encoder stage. Its operation is as follows. An analog input is applied at the input to both a delay network and a parallel comparator bank encoder of N bits resolution (encoder No. 1). This first level encoder converts this input into a first (coarse) digital estimate (N-bit resolution) of the input level. This digital estimate is applied to a N-bit DAC that provides an analog output proportion to this coarse estimate. This DAC output is subtracted from the delayed analog input in an analog summing network. The resultant difference voltage from the summing network is applied to the input of the second M bit encoder. At this time the fine (or subranged) second level measure of the analog input is encoded. The first level N bits form the most significant bits (MSBs) of the final digital word. These bits are shifted through an extra register so that they will be loaded into the output register at the same time as the M-bit output of the second level encoder. The second level encoder produces the M least significant bits (LSBs). These M + N bits are loaded into the correct order into the output register becoming the final encoded binary output.

Theoretically this subranging process could be performed for any number of encoding stages. Practically, however, some inherent problems in the implementation of the technique pose definite limits. To enable the entire encoder to function properly, the first level encoding must occur with an accuracy greater than required for the specified resolution of the encoder because small errors in the first encoding process add with analog errors in the D/A conversion process. Those errors, in turn, add to small analog errors in the delay and summing processes that often result in an incorrect second level encoding. These types of interstage "Tracking" errors cause both monotonicity errors and missing level errors in the ADC high speed transfer characteristic. Often small dynamic or settling errors can cause the above type of errors to exist only under the dynamic high speed conditions found when encoding radar video.

Hughes has adopted a design technique that can eliminate or minimize "Tracking" errors in a cascaded comparator bank encoder. This technique is often described as an overranging error correction process. A block diagram of a cascaded comparator bank encoder with overrange error correction is shown in Figure 8. This feature is implemented as follows. Basically the encoder functions as before; the scale factors, however, are adjusted so that the encoding range of the second ADC "overlaps" the worst case quantizing level of the first encoder. This overlapping feature allows correction of the first level estimate. This correction is accomplished by incorporation of an error correcting circuit; this circuit measures the size of the error in the first estimate as measured in the second (overlapping) encoder. The circuit then using that information is designed to correct all output data bits affected by that error producing a correctly encoded binary output.

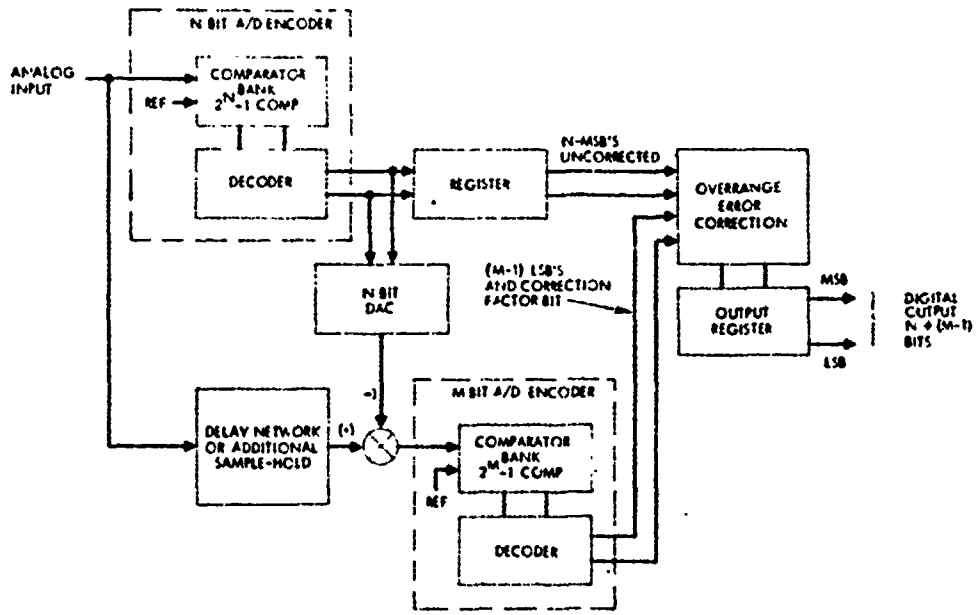


Figure 8. Two-stage cascaded [N+(M-1)] bit A/D encoder with overranging error correction, block diagram.

ENCODER DESIGN PHILOSOPHY

During the high speed ADC development, Hughes evolved several basic design philosophies. These were derived after observing common problems that recurred in many encoder configurations (designed to achieve reliable high speed encoding of radar video).

Two of the most common problems that occur in high speed ADCs are missing levels and monotonicity errors. These errors typically appear when the ADC (operating at or near maximum sample rates) is being exercized by encoding input signals that exhibit nearly full scale level change from sample to sample as well as a large slew rate (slope) during sampling. (These signals occur in real operating environments but are simulated in the laboratory during beat frequency tests; see Testing Test Procedures, p. 41).

A monoticity error is defined as an abrupt change in sign of the rate of change of digitally encoded output that is not present at the input. This change usually occurs at particular points throughout the transfer characteristics (Figure 9). Encoding techniques were then developed that eliminated or minimized these encoding errors plus others. Design philosophies evolved to prevent these errors are described in this section.

A first design philosophy suggests using parallel comparator bank encoders; if possible, a single comparator bank with 2^N-1 comparators and reference sources should be used. With this design structure, missing levels or monotonicity errors can occur only if a comparator malfunctions (if reasonable peripheral design is used). This structure also eliminates an existing

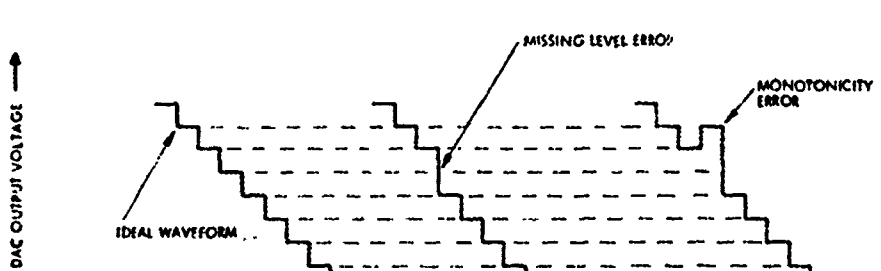


Figure 9. Portion of D/A converted ADC output waveform demonstrating common types of A/D encoder errors.

"tracking error" problem in cascaded comparator bank designs that do not have an overranging feature and the need for complicated analog circuitry in the delay network, D-A, and summer.

Another design philosophy in which available circuit components are used has the advantages of the reproducibility of a design, reliability of proven components, and lower cost of components. However, other problems including the size of parallel comparator banks are introduced. The package size of the currently used comparator as well as its input capacitance (of which the package is a large portion) causes a practical comparator bank size limitation of 32 packages or 64 comparators. (This bank is suitable for 6-bit operation.) Also these available comparators have several inherent electrical deficiencies that greatly limit the speed, such as the inherent settling time and lock of a non-ambiguous latch operation. The comparator also introduces input hysteresis that grows with increased operating speed. Available comparators can perform 6-bit encoding at up to 65 megasamples per second rates. In the future, hybrid and/or new state-of-the-art monolithic circuits probably will be used to permit improved speed and accuracy. For the present, however, an ADC requiring more than 7 bits encoding a single comparator bank encoder is not feasible.

A design philosophy has been evolved to handle the requirement for greater than 6-bit accuracy at high speed. In this technique, the number of cascaded encoder stages is minimized, and an overrange error correction scheme is employed. This eliminates interstage tracking error problems and reduces the accuracy requirements for the first level encoder. This approach necessitates the use of as large a comparator bank as possible to minimize the number of cascaded encoder stages. Further study of each design's requirements is needed to define the tradeoff between the number of bits encoded first and the number of bits encoded second. The overrange correction scheme is included as a requirement because it has been observed that no high speed high accuracy (greater than 8 bits at 4 megasamples per second) multistage ADC has ever been built that would meet specified performance over any reasonable temperature range that did not incorporate this feature. This program was devoted to the development of an A/D converter of less than

6-bit resolution. Also, the emphasis was to obtain the maximum conversion speed. For these reasons, a parallel comparator bank encoder design was used, since it minimizes the analog sources of errors that exist in other encoder techniques.

BREADBOARD HARDWARE DEVELOPMENT

INTRODUCTION

Initial investigations into the feasibility of a single 500 Ms/sec ADC showed that it was not feasible with the current (early 1971) technology. However, these investigations showed feasibility of an ADC in the near 200 Ms/sec range. For this reason an approach using several ADCs to achieve the sample rate of 500 Ms/sec was selected. This approach uses three ADCs each operating at a 6 ns sample period (see Figure 10). The

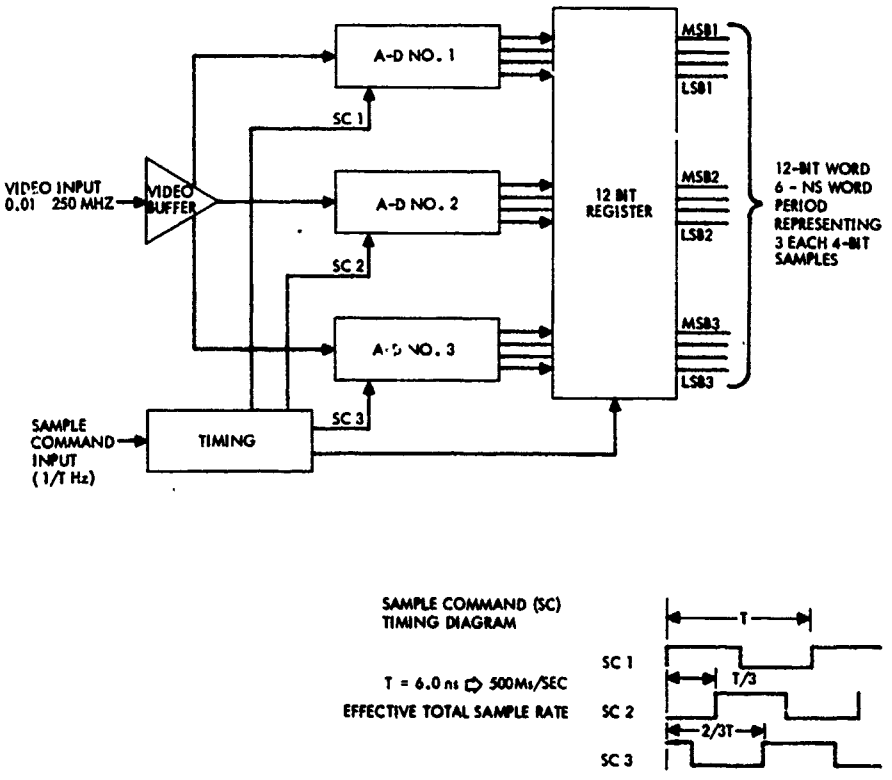


Figure 10. "Parallel" 500 Ms/sec A/D converter block diagram.

individual sample commands are interlaced so that the effective sample times are 2 ns apart. That is, ADC marker 1 samples the input video and starts encoding it at time t = 0; 2 ns later ADC number 2 samples the video; then another 2 ns later, ADC number 3 samples the video completing the cycle; 2 ns later the cycle starts again. This operation cycle continuously repeats itself. With this approach the output data are staggered in delay. A 12-bit register is used to synchronize the output data to the same time.*

Using the above technique, an ADC capable of sampling 250 MHz video at rates up to 200 Ms/sec was required. The remaining portion of the study was spent developing this converter.

Two complete A/D converter breadboards (versions 1 and 2) were constructed and tested. Both converter assemblies used the same sample-hold circuitry; however, two different encoder designs were used.

The Sample-Hold circuitry performed satisfactorily and achieved a remarkably low aperture time of <2.7 picoseconds rms. This low aperture time implies that Sample-Hold could achieve 6 to 7-bit resolution at sample rates as high as 500 Ms/sec.

Block diagrams of the two A/D encoders used in this study are shown in Figures 12. The first encoder (version 1) was designed with a clocked

*To minimize the processing errors created by the minute quantizing level differences in the ensemble of converters, a special sample timing format should be used. The sample command timing should be supplied so that repetitive samples of each A/D converter are always in the same time relationship to a master trigger or prf trigger as shown in Figure 11.

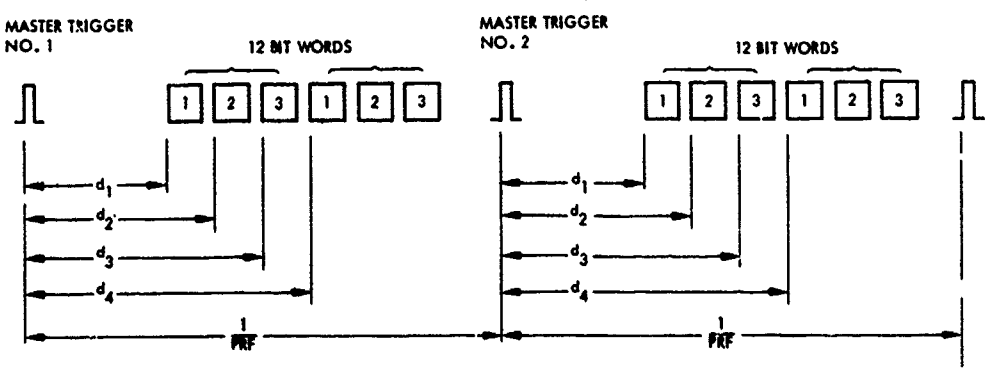
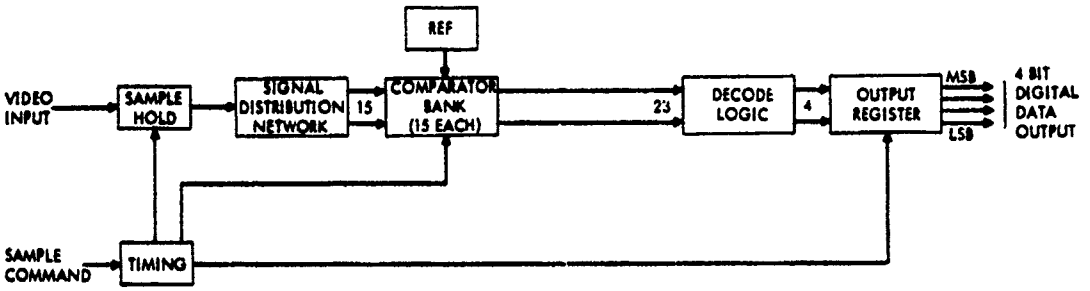
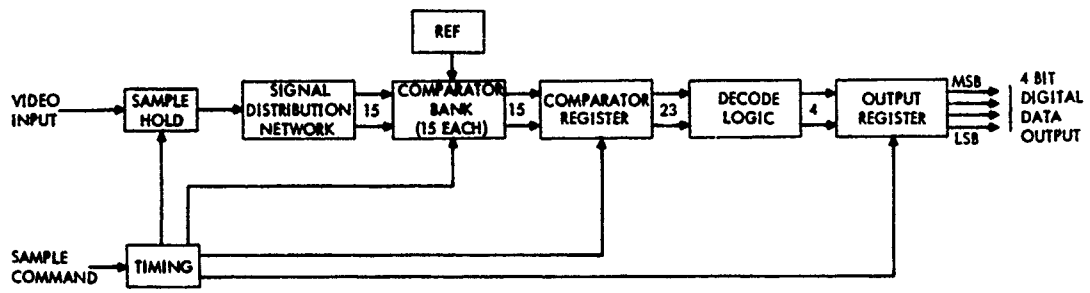


Figure 11. Time relationship of repetitive samples to master trigger or prf trigger.



a. Version 1



b. Version 2

Figure 12. ADC block diagrams.

comparator bank driving the decoder stage directly. The second encoder (version 2) was designed with a data register (consisting of 15 each "D" master-slave flip flops) used to interface between the comparator bank and the decoder stage. Also, version 2 used discrete clock drivers to improve the speed and uniformity of the critical timing signals used in the encoder.

At the conclusion of these experiments, ≈150 Ms/sec were found to be the maximum completely unambiguous (to testing limits) sample rate per ADC using standard Mecl III logic elements. Operation to 170 Ms/sec at 4 bits appeared quite reasonable, however, since on the average less than ≈0.5 percent of the samples were in error by more than 1 LSB. The maximum encoding rates achieved (before gross distortions in the input signal

reproduction occurred) for the first and second versions of the ADC were 195 and 255 Ms/sec, respectively.

Both ADCs exhibited similar encoding problems at high sample rates. Eventually these were traced back to response limitations of the MECL III comparators and "D" master slave flip flops (see "Comparator" discussion in the "ENCODER" section).

A technical description of the actual breadboard hardware and the experiments used in their development is given in this section.

SAMPLE-HOLD

A detailed block diagram of the Sample-Hold is shown in Figure 13.

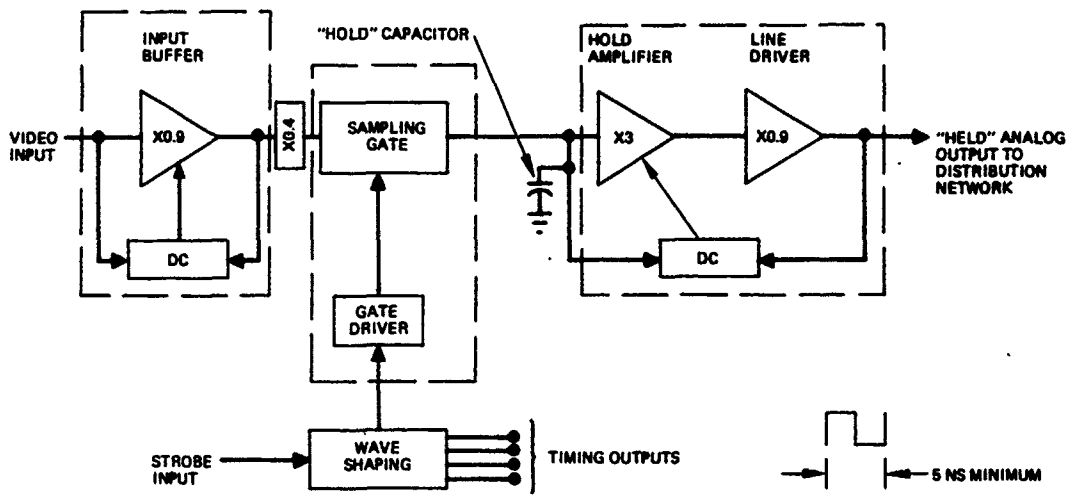


Figure 13. Sample-hold block diagram

This unit consists of an input buffer amplifier, sampling gate/hold capacitor, and an output "hold" amplifier. This ensemble of circuits operates (as described in the general description under "Sample-Hold") in a track and hold mode. The held level output represents the sample voltage to be encoded.

The circuit performance is summarized below:

1. Input bandwidth ≈ 400 MHz
2. Maximum acquisition time <1 ns to within ±3 percent
   <2 ns to < ±1 percent

3. Input signal 1.5V pp into 50Ω (SWR <1.02 to 250 MHz)
4. Output "hold" signal 1.8V pp into 13Ω resistive (distribution network input impedance)
5. Aperture time < 2.7 picoseconds rms
6. Delay time (sample command fall (50 percent to stable hold output ≈ 4.0 ns.

Photographs of typical voltage waveforms observed while sampling an input pulse and varying the delay of the sample command gate are shown in Figure 14.

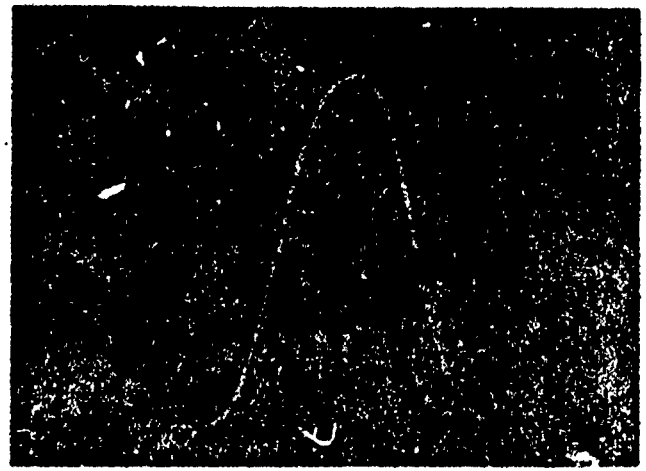
The following is a detailed description of the Sample-Hold circuitry.

Input Buffer Amplifier

A diagram of the input buffer is included in Figure 13. This amplifier stage consists of two signal paths. The first, a low frequency (τ = 2 second) path, consists of a μA725 operational amplifier that is connected as a differential integrator. The second path is a high frequency stage. It consists of a FET input negative feedback voltage follower and has a 400 MHz bandwidth and a voltage gain of 0.95. The low frequency stage compares the input and output waveforms and adjusts the DC difference so that it is the same as the offset voltage generated at the input of the operational amplifier. This function was accomplished by applying the μA725 output voltage to a DC offset control input to the wideband stage. This input buffer provides the necessary isolation for the input from the sampling gate transients and adequate output current to drive the 50 ohm input impedance of the sampling gate. The FET voltage follower input buffer also provides the very low input reactance necessary to provide a good transmission line termination (i.e., low SWR or reflection coefficient at the required bandwidth of operation).

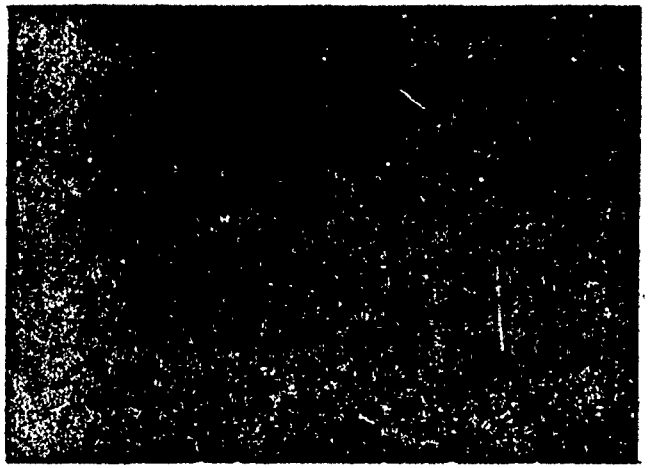
Sampling Gate and Gate Driver

The block diagram of the sampling gate and gate driver is included in Figure 13. The sampling gate is a classical six-diode bridge configuration using hot-carrier diodes. The bridge is biased "off" by a DC current. It is driven to the "on" state by a balanced current pulse. This pulse is generated by a two-stage differential current switch emitter follower (CSEF) using



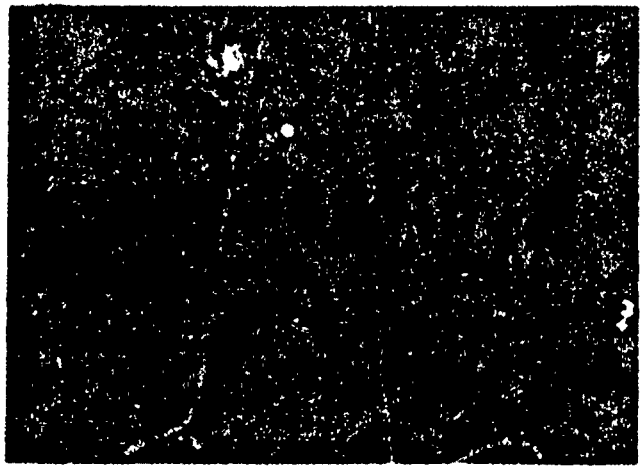
H = 1 nsec/div V = 200 mV/div

a. Input video



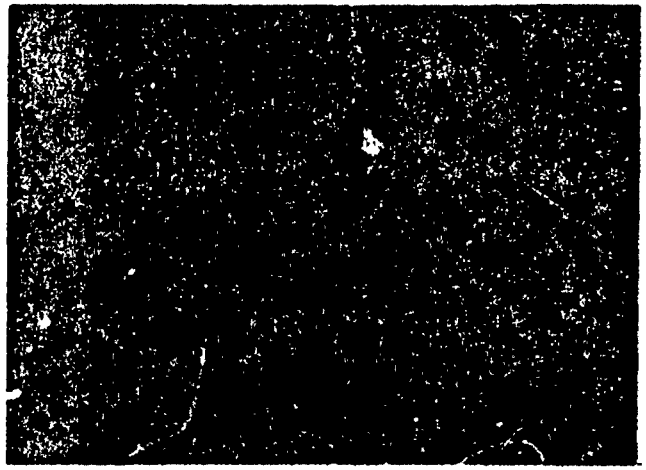
H = 2 nsec/div V = 200 mV/div

b. Output sample of rising edge of input



H = 2 nsec/div V = 200 mV/div

c. Output sample of peak of input



H = 2 nsec/div V = 200 mV/div

d. Output sample of falling edge of input

Figure 14. Photographs showing the input video pulse and the sample hold output (observed at the center of the distribution network) for several different sample command delays.

2N5841 transistors. The pulse is coupled to the sampling gate and isolated from the CSEF pulse generator by a wideband transformer coupling network. This pulse generator and coupling network provide a current pulse that has a 600 picosecond rise and fall time. The current pulse drive is adequate to provide enough "on" gate current to be able to slew the 10 pf hold capacitance (the full scale signal of 0.5 V p-p is less than 0.5 ns) and to provide low distortion in the track mode of operation. The actual turn off time of the sampling gate is approximately 400 picoseconds. This turn-off time is sufficiently small relative to the period of a maximum frequency input sine wave to allow accurate (low distortion) sampling of such an input. When the gate is "on" it forms (in combination with the hold capacitor) a low pass network with a bandwidth 500 MHz. This network has approximately 10 percent overshoot to a step input and settles to < 0.5 percent of its final value in < 2.0 ns. The bandwidth and transient response of the cascaded sampling gate ("on") and input buffer are adequate to accurately sample (to ≈ 6 bit accuracy) a 250 MHz BW video input signals.

Hold Amplifier and Line Driver (Output Amplifier)

The block diagram of the hold amplifier line driver is included in Figure 13. This amplifier also consists of two signal paths as used in the input amplifier configuration. This stage, however, instead of a voltage gain of 0.95 has a voltage gain of 3.0. The input of this amplifier is also a FET stage thus providing the necessary low input current to minimize "droop" on the hold capacitor during the "hold" phase. The FET is connected to a three-transistor negative feedback amplifier that provides the necessary voltage gain. This FET amplifier uses a 2N4416 FET, and HP35821E transistor. It has an 1800 MHz, 3 dB bandwidth and provides enough signal current to drive the line driver input impedance of 100 ohms. The output amplifier is the line driver. This stage provides the current gain necessary to provide unity voltage gain from the output of the X3 FET buffer into the 13 ohm load that is presented by the comparator distribution network. The two-stage hold amplifier/line driver combination provides a net 3 ns settling time and a 600 picosecond rise time response to a step input with the 13 ohm distribution network as its load while delivering a full scale 1.6 V p-p output voltage signal.

ENCODER

Both encoder designs used in this study are single-stage parallel comparator bank encoders and perform as described in the first part of this report.

A detailed description of the designs of each portion of the encoders used in this study is given in this section along with a more detailed presentation on the critical device response limitation.

Signal Distribution Network

Transmission lines are used to distribute analog signal to each of the 16 comparators with minimum reflection.

Microstrip and strip line techniques are used with printed circuit boards to form transmission lines. The microstrip is formed by a constant-width conductor on one side of a circuit, with a ground plane on the other side (Figure 15). The characteristic impedance is determined by the width and thickness of the conductor and by the thickness and dielectric constant of the circuit board material. The stripline consists of a constant width conductor between two ground planes.

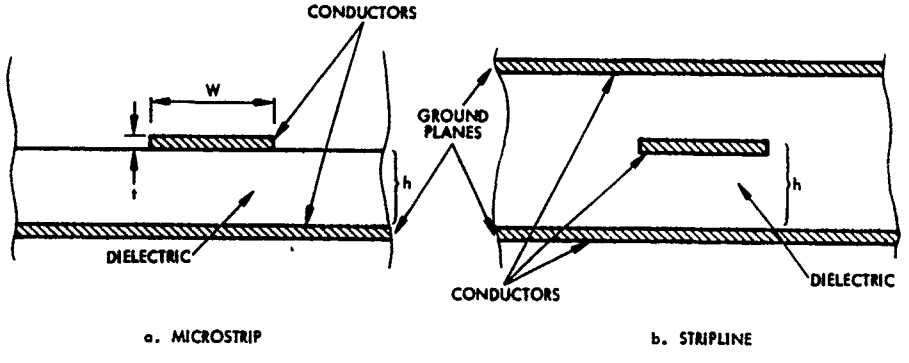


Figure 15. Printed circuit transmission lines.

The characteristic impedance of a microstrip line is given by Equation (4).

$$Z_o = \frac{60}{\sqrt{\epsilon_{re}}} \ln \frac{5.98h}{0.8w + t} \text{ ohms} \qquad (4)$$

where $h > 0.8w$, and $t < w$, where h, w, and t are as indicated in Figure 15.

The term ϵ_{re} represents the effective dielectric constant. The compound dielectric in a microstrip is considered in which air serves as dielectric on one side of the conductor to cause the microstrip to be faster than if it were completely buried in one dielectric materials. The value of the effective dielectric constant is

$$\epsilon_{re} = 0.475\epsilon_r + 0.67 \qquad 1 \leq \epsilon_r \leq 15 \qquad (5)$$

where ϵ_r is the relative dielectric constant. The delay of this type of line is found to be

$$T_D = 1.017\sqrt{\epsilon_{re}} \qquad (6)$$

Reflections occur whenever a transmission line encounters a discontinuity i.e., characteristic impedance that is different from the original line. The discontinuity can be another transmission line, a circuit or a load. The reflected voltage is $V_R = \rho V_i$ where V_i is the incident voltage. The reflection coefficient for a waveform traveling along a transmission line with characteristic impedance Z_1 and encounters a discontinuity with impedance Z_2 is

$$\rho = \frac{Z_1 - Z_2}{Z_1 + Z_2} \qquad (7)$$

When a transmission line is loaded at several points along the line, its characteristic impedance is altered. If the loads are capacitive of equal magnitude and they are distributed uniformly along the transmission line, the net characteristic impedance is lowered. Uniform distribution with small

spacing between loads enable the resulting characteristic impedance (Z) to be approximated by:

$$Z \cong \frac{Z_o}{\sqrt{1 + \frac{Cd}{C}}} \tag{8}$$

where

Z_o = original impedance
C = capacitance per unit length of the original transmission line
Cd = added capacitance per unit length.

In regard to coupling problems, the magnetic field decays at a rate inversely proportional to distance from the center of the line. In experiments performed by Sanders Associates, it was found that if two lines are separated by 2.5 times the line width then the coupling between lines is less than -70 dB. In most cases, a line has been separated from another or from a ground plane by about three times the line width. The results have been quite satisfactory.

Experiment

Several experimental microstrip lines were constructed to measure the effect of capacitive loading by the comparator input impedance.

The comparators SC8372, (re-metallized MC1650) exhibit an average of 3.3 pf capacitance at the input.

A microstrip line was loaded as shown in Figure 16. Each capacitor represents a comparator input capacitance and they are spaced 1/4 inch from each other. The 47 ohm resistors help damp out a small amount of high frequency oscillation. This test line represents one half the actual video distribution line. For a 4-bit A/D, another identical line is connected in parallel.

The microstrip line is 0.1 inch wide by 0.0015 inch thick. The dielectric material is epoxy glass, whose ϵ_r is 5, and its thickness is 0.250 inch. Its original characteristic impedance is calculated and experimentally verified to be 100 ohms. When loaded as shown in Figure 16, the characteristic impedance is verified to be about 27.8 ohms as determined by

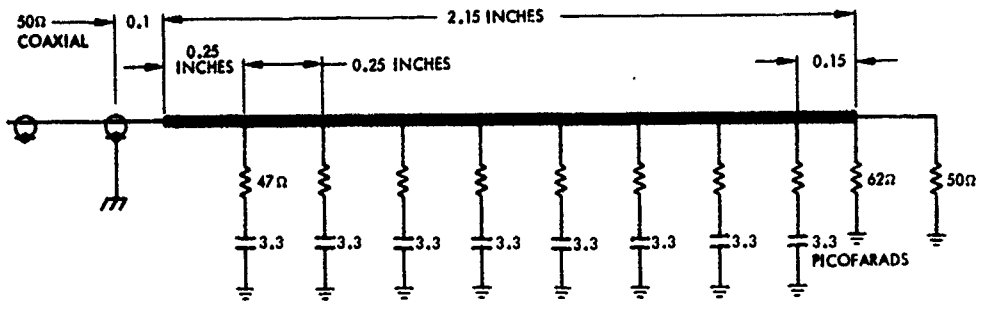


Figure 16. Loaded microstrip line.

the value of the termination resistor that shows least amount of reflection. The HP1415A time domain reflectometer was used in all tests.

The summary of experimentally determined parameters from the microstrip line shown in Figure 16 is given below.

Z = 27.8 ohms

Delay = 0.419 ns/in

T_r = 1.1 ns (settles to <1 percent in 2 ns)

Final Configuration

In the actual A/D comparator assembly, the comparators are loaded on both sides of "horseshoe" microstrip line as shown in Figure 16. This configuration is the equivalent of having two of the lines discussed previously in parallel. The delay between the source and termination is cut in half as compared with the delay in the case in which the line is driven from one end. About three travels by the reflected waveforms between the source and the termination are allowed before the comparator outputs are considered to be accurate. The delay is about 0.84 ns after a waveform leaves the source. In this way error introduced due to reflection is reduced to a negligible amount. The video amplifier at the source, however, must now drive one half of 27.8 or 13.9 ohms.

Circular bends are used as opposed to 90 degree rectangular bends. Thus large reflections are eliminated because the line width is constant throughout.

Effects of line width variation and dielectric material thickness on characteristic impedance are 0.24 and 0.55 percent worst case, respectively. In line width variation both artwork and printed circuit process errors are considered.

Because of layout problems, a short transmission line was needed between the video buffer and the center of the "horseshoe" microstrip where the signal is inserted. This line would see a net impedance of 13.9 ohms. Therefore, a stripline with characteristic impedance of about 13.9 ohms is used. Such low impedance microstrip becomes quite wide for 0.25 inch thick dielectric; hence, stripline was used. Small mismatch that most likely exists between this stripline and the "horseshoe" microstrip will not contribute any significant error because the stripline is quite short (1.6 inches).

Reference Generator

The reference generator is a 16-element resistive divider that is driven by two positive voltage sources and by two negative voltage sources and grounded in the cneter. Four μA747 dual operational amplifiers are used as the voltage sources. They are connected to supply the four reference voltages from a single 1N827 temperature compensated zener reference. Each voltage output is adjustable by external offset potentiometers. The resistive voltage divider uses 30 and 15 ohms, 1 percent film type resistors. This voltage generator supplies all of the 16 required reference voltages to a 0.30 percent worst case accuracy over a temperature range of 0 to 50°C. Each tap on the resistive reference divider is bypassed with 0.1 μf chip capacitors to minimize transients caused by the switched input currents of the comparators. Also, a small RC network is connected from the reference string taps to each comparator reference input. The total resistance as seen by each comparator is calculated to be the same as that seen by the analog input to provide temperature compensation for the comparator offset currents. The reference generator was designed to a close tolerance to eliminate any significant contribution reference errors from the converter error budget. A block diagram of the reference is shown in Figure 17.

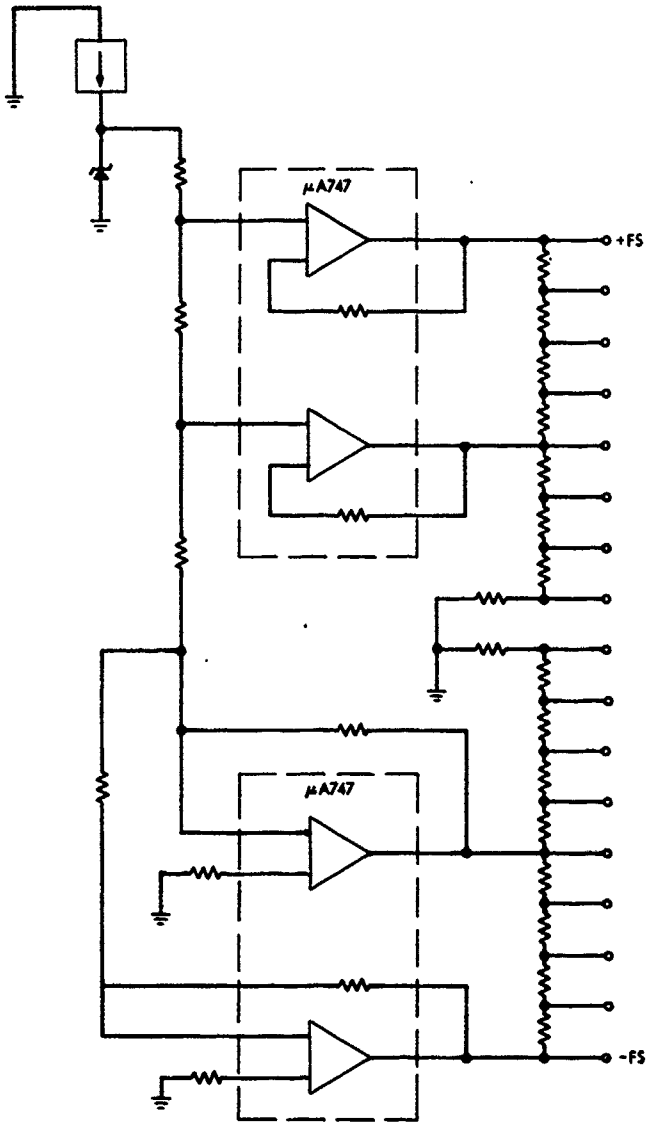


Figure 17. Reference generator block diagram.

Comparator

The comparator is the key circuit of the analog-to-digital encoding process. It compares the reference voltage with the analog input signal (from the sample hold via the distribution network) and then generates a digital output corresponding to their relationship. If the analog voltage is above the reference, a logical "1" voltage (≈-0.9V) is generated at the output. If the analog input is less than the reference, a logical "0" voltage (≈-1.75V) is generated at its output.

A survey of available comparator circuits suitable for the very high speed operation showed only one basic IC comparator circuit available — the Motorola MC1650. Initial testing, however, exposed a serious deficiency in its high speed performance — an input slew rate limit (-200V/μs) in the negative going direction (input voltage slewing from a positive value to a negative value). This deficiency caused an unacceptably large error in the very high speed operation of the device. A remetalized version of the MC1650 obtained from Motorola* (an SC8372), eliminated the source of the problem. This device showed performance that was adequate for 170 Ms/sec operation and for the approximately 5-bit resolution and accuracy.

The performance of the comparators was measured as follows. Figure 18 is a schematic showing the test circuit and equipment configuration. An accurate voltage pulse waveform was supplied to one of the comparator inputs, and a DC reference voltage was applied to the other input. Then the comparator response to the input pulse waveform was observed as the reference voltage was varied. The comparator performance was interpreted by recording the reference voltages that corresponded to distinct changes in the comparators pulse response (such as the reference voltage that corresponded to the change from a pulsing to a non-pulsing output). The data measured were tabulated for a large variety of input pulsewidths and amplitudes for several samples of both type of comparators. Then the results were plotted to see if trends existed.

* Presently known as MC 1651

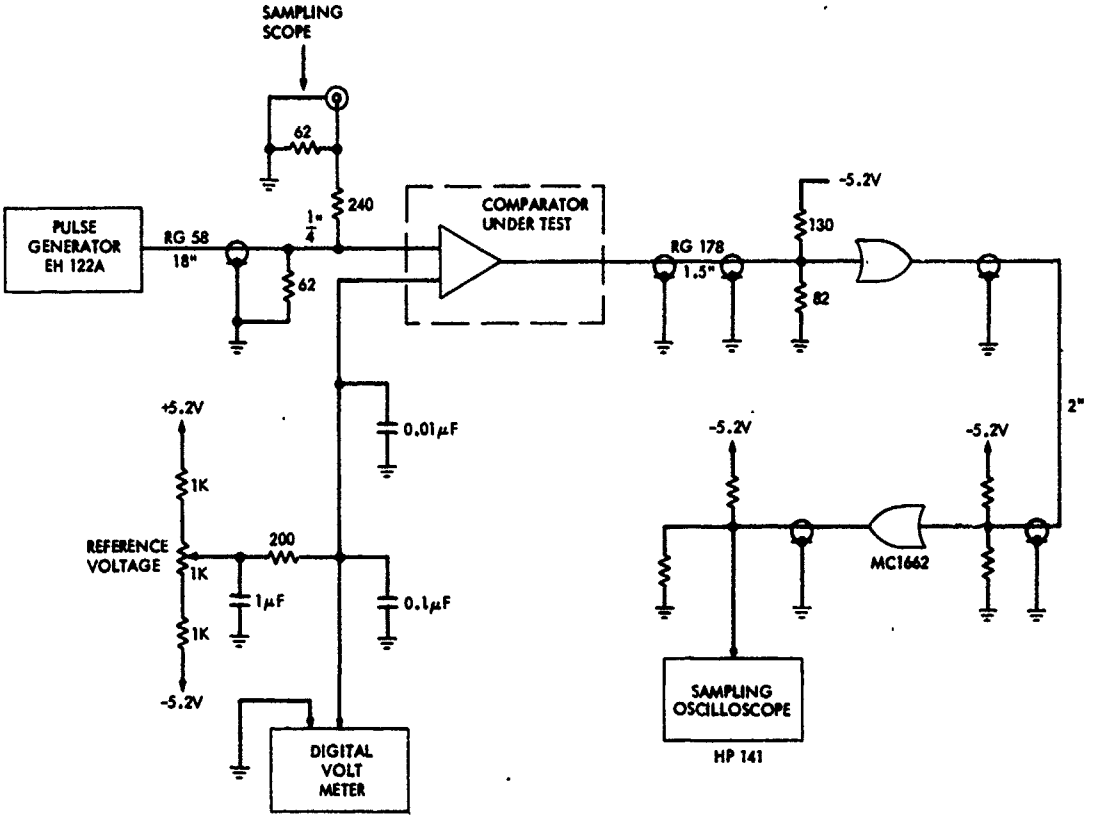
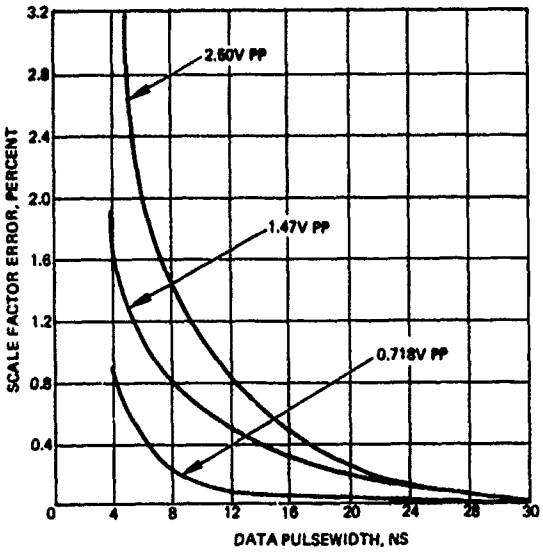


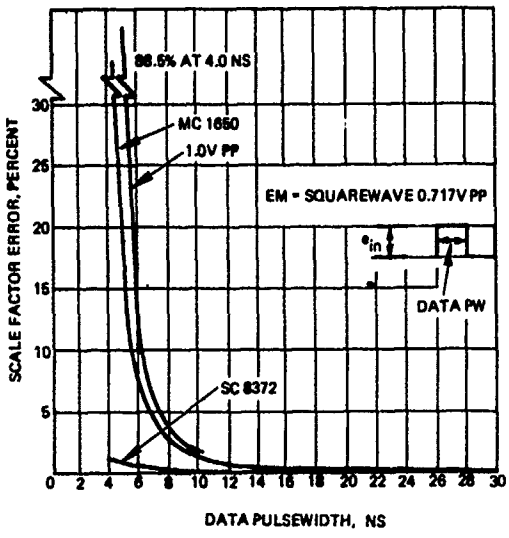
Figure 18. Comparator performance test setup.

Figures 19 through 21 are curves in which the performance of the two types of comparators are compared. Table I is a summary of the potential comparison accuracy versus the maximum analog signal (peak-to-peak) and the conversion rate. From the comparator performance data that were measured, an analog input signal of ≈1.8 V p-p was shown to provide near optimal accuracy at up to 170 Ms/sec. A summary of the various comparator parameters that were measured, then used in the high speed 4-bit design is given in Table II.

During the evaluation of the A/D performance another problem caused by the high speed comparator performance was discovered. The problem became more noticeable as the encoding rate was increased. It was observed that the encoding process during the transition from one word to the next

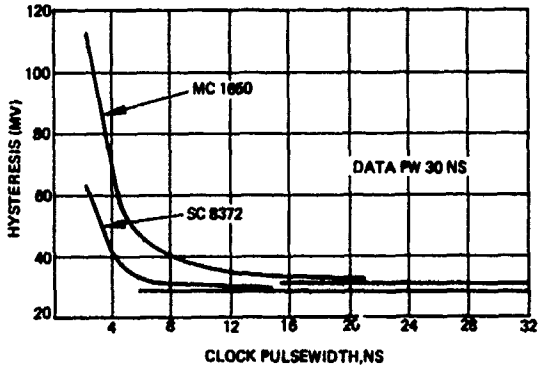


a. Versus data pulsewidth for different input voltages SC 8372 (Motorola) comparator.

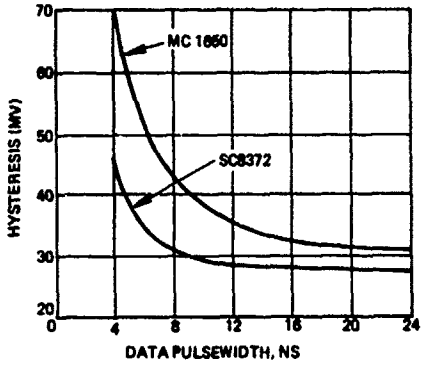


a. Versus data pulsewidth comparing MC 1650 SC 8372.

Figure 19. Scale factor error.



a. Versus data pulsewidth



b. Versus clock pulsewidth

Figure 20. Comparator input hysteresis errors.

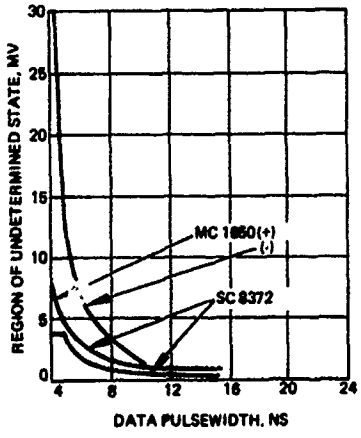


Figure 21. Region of undetermined state versus data pulsewidth for MC 1650 and SC 8372.

TABLE I. MEASURED ERROR DATA FOR MC1650 AND SC8372 COMPARATORS AT 6 ns DATA RATE

Errors, percent	SC8372 (Motorola), Percent	MC1650, percent
1. Scale Factor		
0.72V	0.4	7
1.0 V	0.8	13
1.47V	0.9	33
1.77V	1.0	54
2.50V	1.9	
2. 1/2 Hysteresis		
0.72V	2.4	3.5
1.0 V	1.75	2.5
1.47V	1.2	1.6*
1.77V	1.0	1.5*
2.50V	0.8	
3. Offset		
0.72V	0.7	1.0
1.0 V	0.5	0.7
1.47V	0.34	0.46
1.77V	0.28	0.40
2.50V	0.15	
Total Error		
0.72V	3.5	11.5
1.0 V	3.05	16.2
1.47V	2.44	35.1
1.77V	2.28	55.9
2.50	2.28	
*Estimated		

TABLE II. COMPARATOR INPUT CHARACTERISTICS

MC1650

Z_{in} = -60 Kohm//2.0 pf measured @ 10 MHz

I_{in} = 10 μa maximum

SPECIAL COMPARATOR

Z_{in} = 3 pf//22 Kohm/ 4 pf//5 Kohm in active region ($e_{in} = V_{ref} \pm 50$ mV) measured at 10 MHz

I_{in} = 50 μa maximum

became more noticeable as the encoding rate was increased. It was observed that the encoding process during the transition from one word to the next sometimes produced large (MSB size) errors for a fairly small fraction of the samples. The errors were traced to the comparators and revealed that a nondigital or ambiguous level output (not latched to either 1 or 0) from comparators appeared to be the prime source of the problem. Because of this problem, a bank of MECL III "D" master slave flip-flops were incorporated in the second breadboard at the comparator outputs to eliminate the digital ambiguity. However, it was discovered that these flip-flops respond very slowly (i.e., ≈10 ns to latch) to marginal level digital input signals. At these encoding speeds, quasi-stable non-digital voltage levels at their outputs still resulted.

Further investigation of the above problem revealed that it can be overcome by placing a high speed "latch" stage on critical comparator outputs. This device would behave as a Schmitt trigger. Thus, after a short settling time, "latched" digital outputs that can be interpreted unambiguously in a decoder or register that would be provided. A discrete latch stage using 2N5841, (2.5 GHz devices) was built and exhibited a 3 ns time-to-latch. After this stage, an unambiguous digital sample can be taken by devices such as the MECL III "D" master slave flip-flop and fed to the decoder section.

Hughes has built ultrahigh speed logic gates which exhibited approximately 250 pico-seconds propagation delay using discrete HP35901E (4.0 GHz devices). A Schmitt trigger "latch" could be constructed that would provide approximately 1.5 to 2 ns time-to-latch. This latch could also greatly increase the usable speed of a particular comparator.

The current discrete assembly techniques make use of this added latch impractical for large (5 bit) encoder comparator banks. Hybrid assemblies could reduce this problem. A monolithic chip comparator incorporating this feature would physically allow a higher speed, high bit resolution comparator bank.

New comparator designs for the development of a dual, triple, or quad ultrahigh speed monolithic comparator that incorporates a latch and hold feature ~~should be investigated.~~ This device must be several times more sensitive and faster than the Motorola MC1650 or SC8372. This type of design probably would consist of a pair of cascaded low gain, high bandwidth current limited amplifiers (such as a pair of differentially cascaded interstages, etc.) to drive a sensitive Schmitt trigger. The Schmitt trigger would then drive, or could be incorporated in, a clocked latch, that would enable track and hold operation or sample-hold (as in a master slave flip-flop design) operation. The Motorola MC1650 design appears to be a good first cut, but closer inspection shows many speed limiting features that were incorporated to make the input impedance high and to keep the power low.

To achieve the high speed operation required, the design rules have to be changed to optimize the speed. This change is mandatory, since at present, the comparator bank is the major stumbling block that prevents 250 mega-samples per second unambiguous A/D conversion. The input characteristics should be considered, of course, but at present these are not the limitation of performance. The sample-hold driver portion has only scratched the surface of the potential performance of these circuits, and other comparator input impedances can be adapted. Another idea that may enable more rapid development of practical high speed comparators would be the use of hybrid assemblies of several special IC chips. If used, considerable flexibility

would be allowed in the choice of devices for specific performance requirements at the various stages of the circuit. Possibly some of these stages might be designed by using new metal masks on existing MECL III/IV or other high speed logic chips. New high speed techniques that reduce parasitic capacitance such as ion implanted resistors and Shotky diodes could greatly improve the speed of exising chip designs.

Availability of faster comparators will permit the reduction in the number of parallel A/D encoders and sample and hold circuits that are required to presently perform the required encoding task. Increased reliability, lower power, greater accuracy, and ease of use (due to the reduced tracking problem between the fewer number converters) will result. At present, it appears feasible to accurately encode an unknown input voltage sample every 3 to 4 ns within the next year, for each A/D encoder at accuracies approaching 7 bits.

Decoder

The analog input to the encoder is applied simultaneously to every comparator. For a given input voltage level, all comparators with reference inputs below the input signal level produce logic one level outputs while those with reference levels above the input produce logic zero level outputs. This uniary code array formed across the ensemble of comparator outputs is then converted to a different binary code by the decoder network. The binary code output corresponds to a binary number proportional to the analog voltage reference level just below and nearest the input level. The A/D transfer function is shown in Figure 22.

The comparator bank output is latched, and an unambiguous digital sample is presented to the decoder network via MECL III master slave "D" flip flops.

The decoder logic to generate an n-th bit output works as follows. Outputs of two comparators, whose reference levels define limits of the range in which logic 1 is to exist at the decoder output, are used to generate an output $C_{Lower} \cdot \overline{C}_{Upper}$. (The term C_{lower} is the true output of the comparator whose reference level is that of the lower limit of the particular

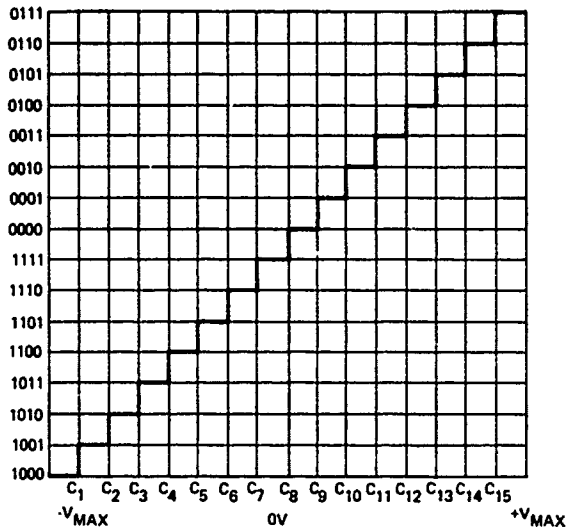


Figure 22. A/D transfer function.

range in question. $\overline{C}_{Upper}$ is the not-true output of the upper limit comparator.) Then $2^{N-(n+1)}$ such outputs are logically ORed to produce the final output for the n-th bit. For example, for the 4-bit case (N=4), the least significant bit output (2 degrees) is the result of eight such outputs ORed together.

The output is in "2's complement" format.

Logic equations for each of the four bits are (Refer to Figure 22; C_i is the i-th comparator output.)

$$2^0 = C_1 \cdot \overline{C}_2 + C_3 \cdot \overline{C}_4 + C_5 \cdot \overline{C}_6 + C_7 \cdot \overline{C}_8 + C_9 \cdot \overline{C}_{10} + C_{11} \cdot \overline{C}_{12} + C_{13} \cdot \overline{C}_{14} + C_{15} \cdot \overline{C}_{16}$$

$$2^1 = C_2 \cdot \overline{C}_4 + C_6 \cdot \overline{C}_8 + C_{10} \cdot \overline{C}_{12} + C_{14}$$

$$2^2 = C_4 \cdot \overline{C}_8 + C_{12}$$

$$2^3 = \overline{C}_8$$

Each of these outputs is then latched using MECL III master-slave D flip-flops. In this way, the four outputs change their state simultaneously at the output and minimize ambiguity.

Computer study of various parallel decoding schemes has revealed that the decoder scheme discussed here gives the least amount of error.

To maximize the conversion speed, the logic signals from the comparator bank are fed to the decoder through striplines having appropriate different insertion delays. Each signal is delayed by the time necessary to compensate for the analog signal delay in the distribution network. Hence all comparator output signals arrive at the decoder almost instantaneously.

ADC ERROR BUDGET

The error budget allocation to the key components of the A/D converter are summarized in Table III. The allocation for hysteresis is included in the first set of numbers.

TABLE III. A/D CONVERTER ERROR BUDGET (6 ns SAMPLE RATE)

Absolute Worst Case Accuracies		
Comparator	—	2.3 percent (includes hysteresis)
Sample Hold	—	0.6 percent
Reference	—	0.25 percent
		3.15 percent
Comparator	—	1.3 percent (without hysteresis considered)
Sample Hold	—	0.6 percent
Reference	—	0.25 percent
		2.15 percent

TESTING AND TEST PROCEDURES

The utilization of test data and the isolation and rectification of design deficiencies have been essential in high performance ADC design. Much study, a literature search, and analysis have been performed in deriving appropriate tests and devising and fabricating test equipment. Further, Hughes has compiled considerable experience in the testing and evaluation of ADCs for high performance applications. Beat frequency tests (described in this section) have been found to produce results that most meaningfully describe ADC performance in the following sense. ADCs that have demonstrated satisfactory performance while undergoing such tests subsequently have been found to exhibit nearly theoretical or ideal behavior when used in conjunction with radar signal processors to convert radar video.

Recently, Hughes conducted tests on most commercially available ADCs using manufacturers' specifications in which greater than or equal to 10 mega-samples per second conversion rates with a resolution of 6 bits or greater (the maximum resolution available was 8 bits) were claimed. These tests were witnessed by technical representatives of the Air Force; a higher performance ADC was required to replace units used in the Forward Looking Advanced Multimode Radar (FLAMR) signal processor. Results indicated that few could meet a requirement of properly encoding a radar video type of input signal even at room temperature. (Typical problems discovered were quantizing level and monotonicity errors that were much greater than an LSB of the provided resolution; also poor recovery times under overdrive conditions.) No units manufactured outside Hughes could pass the required tests during cycling through a 0 - 50°C temperature environment.

The tests used in the breadboard development phase of this study are described in the remainder of this section.

DC TESTS

Conventional test procedures are used to provide the plot of DC input voltage versus output code (Figure 23).

SAMPLE-HOLD APERTURE TIME TEST

During the final evaluation phases of the study, emphasis was placed on the measurement of the actual aperture time of the sample-hold circuitry. The sample hold aperture time was measured as follows. First all sources of time jitter in the test equipment setup were determined and their total time jitter was measured. Next an equivalent sample-hold and test setup time jitter ($J_{SH + TS}$) was calculated from measured sample-hold held level output variations obtained while sampling a known input signal slew rate.** The value for the aperture time or net equivalent time jitter for the sample hold was then found by subtracting the test equipment jitter contribution from ($J_{SH + TS}$) as shown in Equation (13).

A sampling scope was used to measure time jitter and noise levels of the high speed wave forms used in this study. A "Tangential Trace" technique was used to provide accurate repeatable measurements. This technique was described in the April 1969 and February 1970 issues of Tekscope.* In this technique, two traces are produced by adding a slow

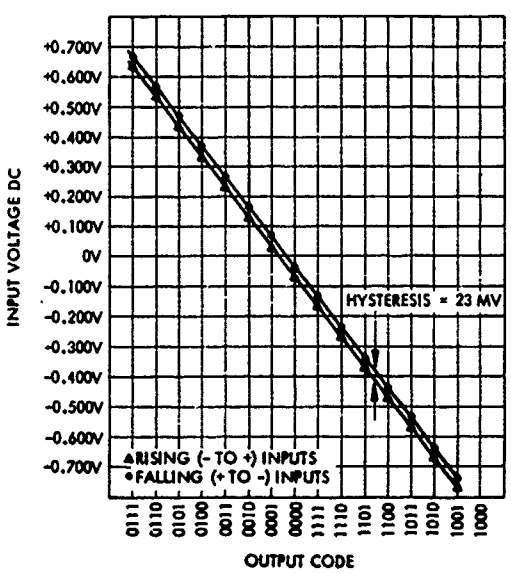


Figure 23. A. D output code versus DC input voltage.

*Tekscope - A monthly publication of Tektronics, Inc.

**See "Sample Hold" discussion pages 8 through 11 for details.

square wave to the vertical (for noise measurements) or horizontal (in jitter measurements) signals. By adjusting this square wave amplitude to achieve "tangency" of the two traces, fairly accurate and repeatable measurements of noise jitter can be made. For a Gaussian distribution, tangency is achieved when the square wave peak amplitude (N_{sw} or J_{sw}) is exactly twice the rms noise or jitter value.* As shown in Figure 24 the displayed noise or jitter value (N_D or J_D), containing 90 percent of the samples, is approximately three times the rms noise or jitter value (N_{rms} or J_{rms}). These relationships are summarized by expressions (9) and (10):

$$N_D \approx 3N_{rms} = 3/2N_{sw} \tag{9}$$

$$J_D \approx 3J_{rms} = 3/2J_{sw} \tag{10}$$

From Equations (9) and (10) it can be seen that accurate measurement of N_{sw} or J_{sw} allows direct calculation of N_{rms} and J_{rms}. The scale factors of N_{sw} and J_{sw} were measured by first determining the N_{sw} or J_{sw} amplitude that provides a deflection of several major divisions in height or width. Then by comparing the N_{sw} or J_{sw} amplitude to the N_{sw} or J_{sw} amplitude required for tangency, a factor directly relating the measurement

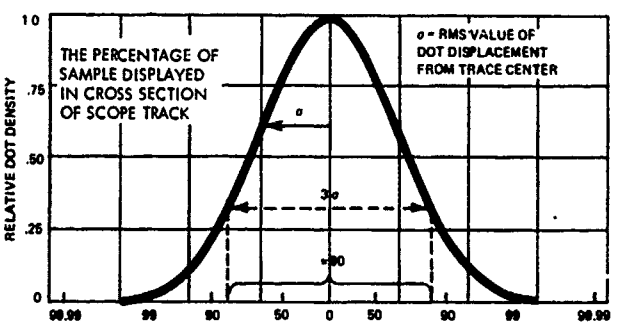
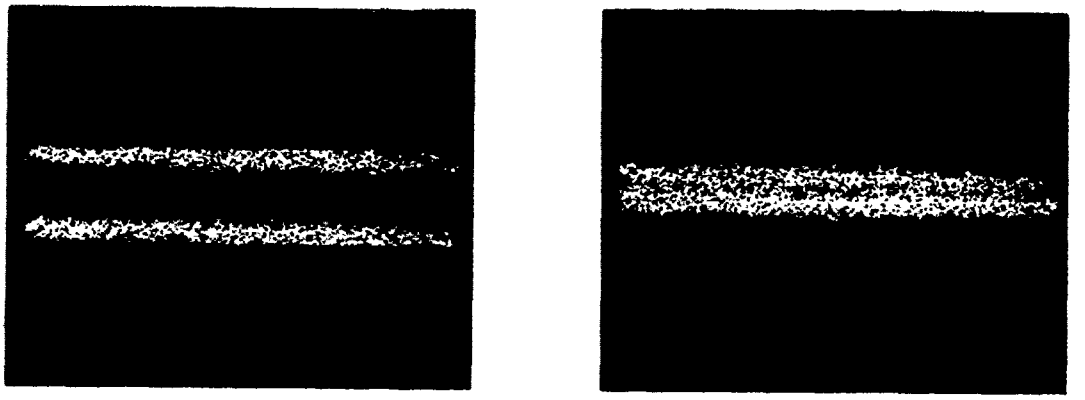


Figure 24. Sample density versus percent of trace width.

*Garuts, V., "A Simple Method for Measuring Preamp Noise", Tektronics Engineering Instrument Specification guidelines.



a. Initial setup

b. Final adjustment (dark band between noise bands has just vanished).

Figure 25. Typical waveforms used in tangency measurement technique.

to the horizontal or vertical scale factor was obtained. Photographs of typical waveforms involved in the tangency measurement technique are shown in Figure 25. In all the jitter measurements performed in this study the noise (vertical component of displayed waveform) on the waveforms was small enough to not contribute to the measurements.

To establish accurate and repeatable results the following procedures were instituted:

1. Always select horizontal scale factors to provide similar sample densities
2. Always use a sensitive vertical scale factor to minimize the effect of the limited oscilloscope resolution (usually noise levels or jitter levels of greater than 1/2 major div. p-p observed are required
3. Keep the intensity settings approximately the same for all measurements
4. Use great care not to introduce ground loops in any of the input signals.

A brief outline of the tests that are required to evaluate the sample hold aperture time are listed on the next page.

1. Measure jitter (J_s) and noise (N_s) of scope and sync circuit
2. Measure analog source jitter (J_{as}) and noise (N_{as})
3. Measure sample hold apparent aperture time
   a. Measure "held" output slew rate by measuring ΔV of held voltage versus a change in the sample delay ΔT (passive adjustable delay line) symmetrically displaced above and below the measuring point on the hold voltage
   b. Measure held level noise level at testpoint (N_{HSW})
   c. Measure held level noise at positive and negative peak outputs.

The scope and sync jitter are used to determine the true source jitter in Equations (11), (12), and (13). The apparent S and H jitter time ($J_{SH + TS}$) is calculated by using the sample-to-sample slope measured in 3a and by Equation (11) held level noise measured in 3b using Equation (11). The true source jitter (J_{st}) is formed by (12)

$$(J_{SH + TS}) = \left(\Delta T(N_{HSW})\right)/2\,\Delta V \tag{11}$$

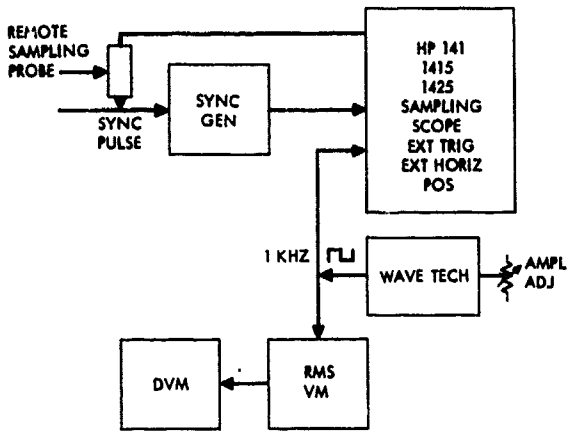
$$J_{st} = \left((J_{as})^2 - (J_s)^2\right)^{1/2} \tag{12}$$

The true aperture time (T_{at}) is found by (13)

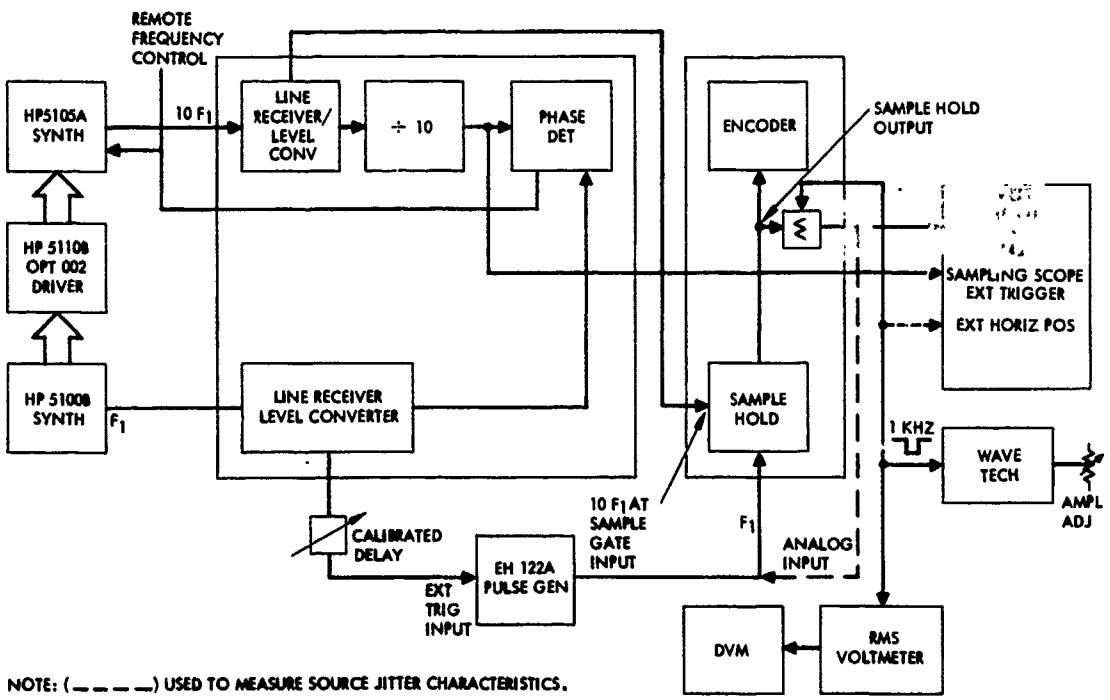
$$T_{at} = \left((J_{SH + TS})^2 - (J_{st})^2\right)^{1/2} \tag{13}$$

Figure 26 a and b shows the test equipment configuration used to perform these measurements. The tabularized results of the measurements are given in Table IV.

In conclusion, the results showed that the individual tangency measurements varied about ±6 percent from their mean value. By averaging many samples, a reasonable estimate of the true tangency values were obtained. The ≈±1 percent calculated values in Table IV show that a sample hold jitter of <2.7 picoseconds rms is a reasonable upper bound. Because of the relatively large test equipment jitter ≈12 picoseconds rms, however, it is still hard to firmly justify the bound. It is important that the sample hold aperture time is small in comparison to the short term stability of the time references; e.g., $(T_{at})^2 \ll (12_{ps})^2$.



a. For sampling scope and synch – jitter measurement



b. For sample-hold aperture time measurements

Figure 26. Test equipment configuration

TABLE IV. RESULTS OF APERTURE TIME TESTS

1. Scope + sync jitter = 3.06 picoseconds rms

   Vertical 10 mV/div.
   Horizontal 20 picoseconds/div.

2. Analog source jitter = 12.2 picoseconds rms

   Vertical 20 mV/div.
   Horizontal 20 picoseconds/div.

3. Sample hold measurements

   Delay line scale factor = 0.174 ns/inch
   8 div. deflection length change = 1.093 inches
   Sample-to-sample slope = 0.190 ns/8 div.
   Apparent aperture time = 11.9 picoseconds rms
   Vertical 10 mV/div.
   Horizontal 50 picoseconds/div.

$$\text{Actual aperture time} = \sqrt{11.9^2 - (12.2^2 - 3.06^2)}$$

$$= 1.4 \text{ picoseconds rms calculated}$$

allowing for ± 1 percent errors in 2 and 3 above

$$T_a < 2.7 \text{ picoseconds rms}$$

DYNAMIC TEST - SINEWAVE BEAT FREQUENCY TEST

The test equipment configuration (Figure 27) is used to exercise the ADC under full dynamic conditions and measure its response with a maximum frequency sinusoidal input signal (at approximately 1/2 the sample frequency). The sample point is moved continuously through a sequence of time points across the input signal period. This test permits oscilloscope observation and spectral analysis of the ADCs response at all points of critical behavior. It also exercises the ADC in a manner closely resembling the unique

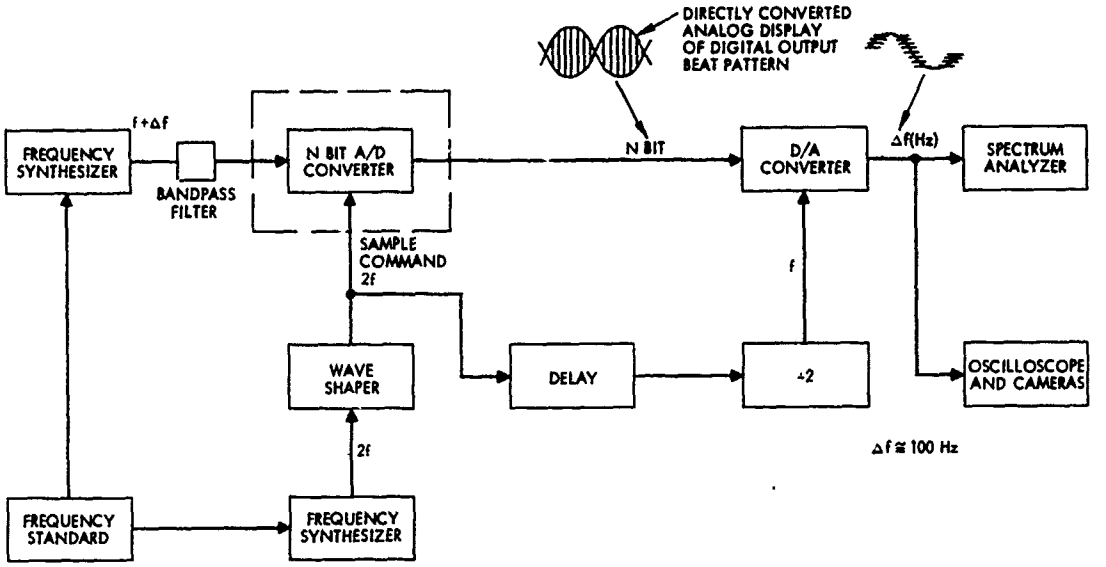


Figure 27. A/D dynamic test setup.

characteristics of Radar Video (encoding of input levels that have up to full scale changes from sample to sample as well as the possibility of a large slew rate at the sample time).

A single frequency standard that drives two frequency synthesizers is used. The sample command pulse train is derived from the first synthesizer through a wave shaper. The other frequency synthesizer is filtered to insure its spectral purity and thereafter applied as an analog input to the ADC under test. The sample command pulse train is further delayed, divided by two in frequency, and "mixed" (demodulated) in a D/A converter with the ADC output. The resultant analog signal (the beat pattern output from the DAC) is fed in parallel to a spectrum analyzer and an oscilloscope, where the beat frequency signal is observed in both the time and frequency domains.

When the equipment is operating, the sample command repetition rate is set at f_{sample}. The analog input signal, coherently locked to the sample command signal, is set at a frequency of $f_{sample}/2 \pm \Delta f$. Here, Δf (e.g., 100 Hz) is the desired beat frequency. Then the sample point moves through one complete input cycle every $(1/\Delta f)$ second (e.g., 10 ms). The response at the ADC output, were it D/A converted directly at the ADC word rate, would be as illustrated in Figure 27.

The beat frequency corresponds to a phase shift or increment in delay proportional to time. With the input frequency set at approximately half the sample rate, each ADC sample is taken at approximately 180 degree phase intervals on the input waveform. The analog beat frequency results since the sample point pair slides through the input signal cycle periodically. With samll DAC errors the setup, as used permits response measurement under repetitive sequences of all worst case conditions including: sampling at zero crossings (maximum slew rate), sampling at alternate positive and negative signal peaks, etc. Furthermore, since the spectral integrity of the input signal is insured by filtering, spectral analysis of the DAC output provides information about high speed linearity that is measured in terms of the relative power of distortion induced harmonics. Careful analysis of the time domain response permits detection of monotonicity errors, missing quantizing levels, and high frequency quantizing errors.

TIME DOMAIN TEST

The appropriate test equipment configuration is illustrated in Figures 28 and 29. The test is similar to the dynamic test described (since it also utilizes beat frequency procedures). In this case, however, a video pulse is used that simulates the impulse response of the equipment which will feed the ADC. This approach permits measurement of rise time, fall time, settling time, delay, etc., through the ADC under conditions that duplicate those which will be the worst case conditions in its intended application.

The input pulse is applied once every N sample pulses; therefore, the output is again a beat frequency pattern (see Figure 29).

Photographs of waveforms obtained for this test are shown in Figures 30 and 31.

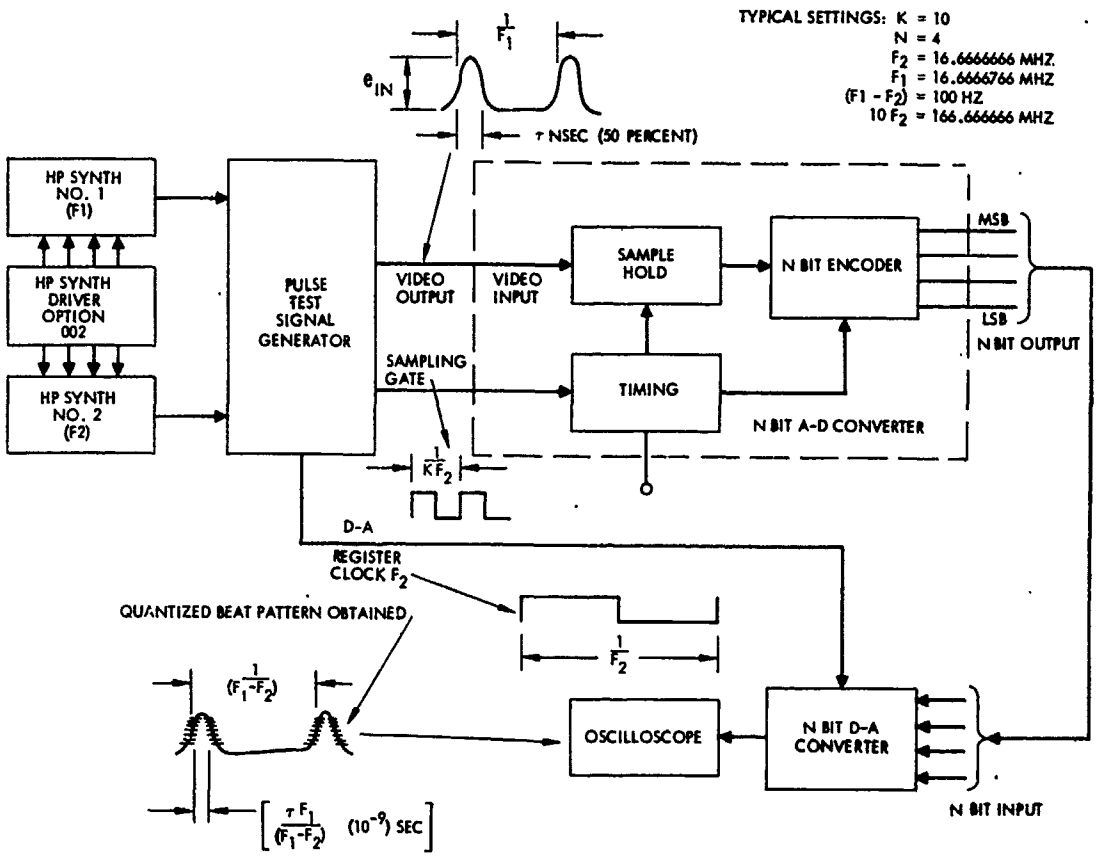


Figure 28. Beat frequency pulse test block diagram.

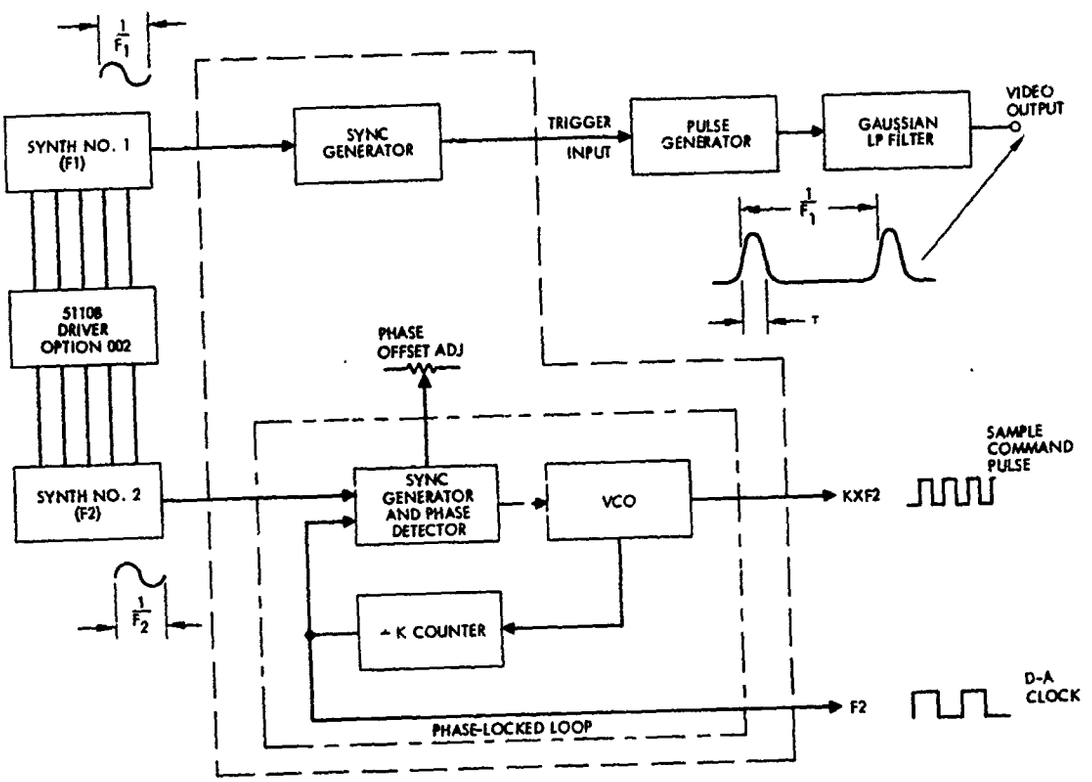
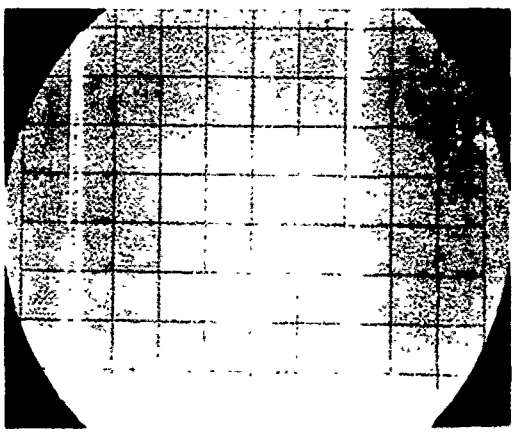
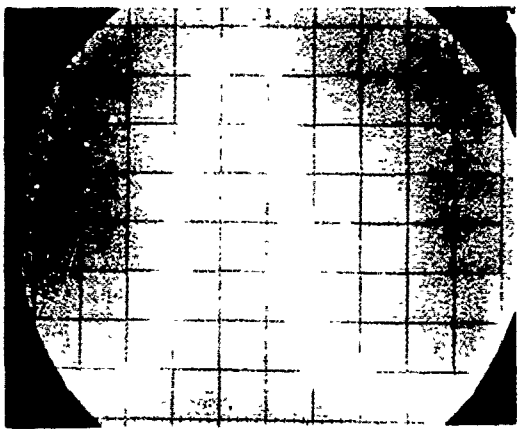


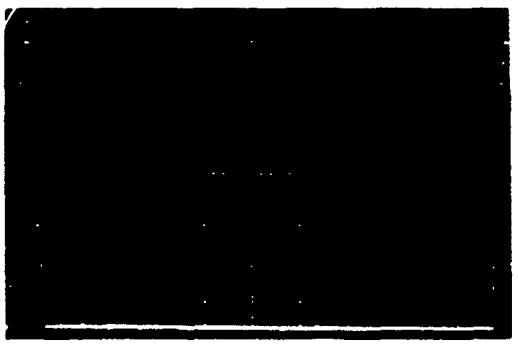
Figure 29. Pulse test signal generator block diagram.



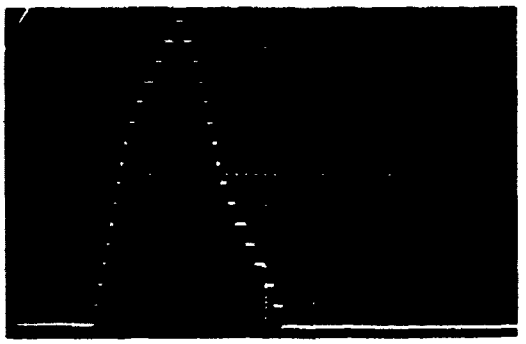
INPUT VIDEO PULSE TRAIN
SCALE 190 MV/CM
10 NSEC/CM



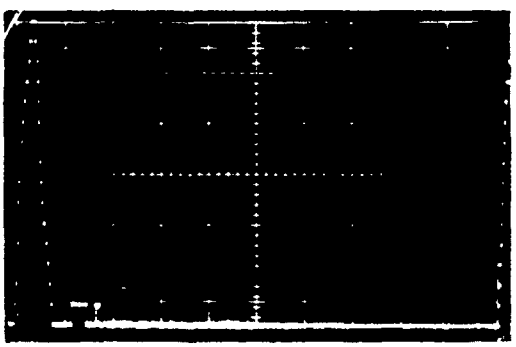
INPUT VIDEO PULSE
SCALE 200 MV/CM
1 NS/CM



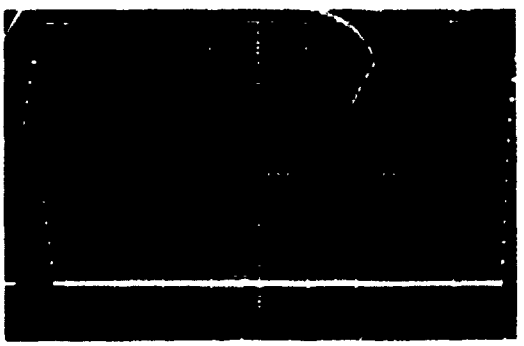
OUTPUT (D/A) FOR PULSE IN PICTURE (4)
BEAT FREQUENCY (100HZ)
SCALE 1 0 MS/CM



OUTPUT (D/A)
BEAT FREQUENCY (100HZ)
SCALE 0.2 MS/CM



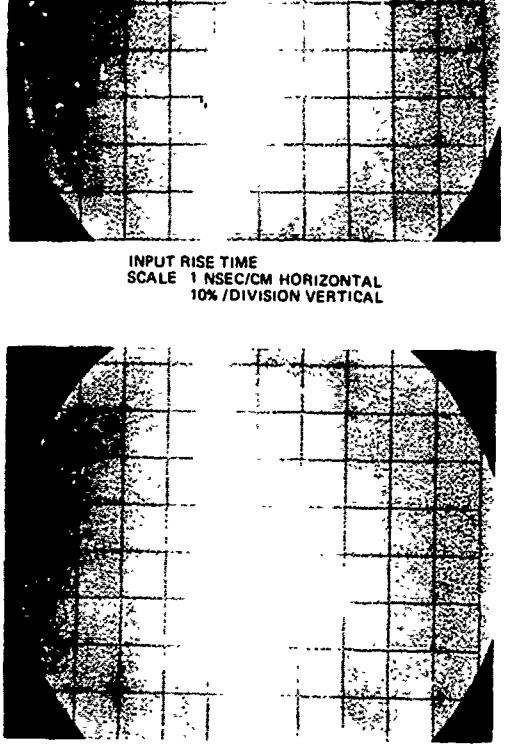
OUTPUT (D/A) (SLIGHT INPUT DC OFFSET)
BEAT FREQUENCY (100HZ)
SCALE 1 MS/CM



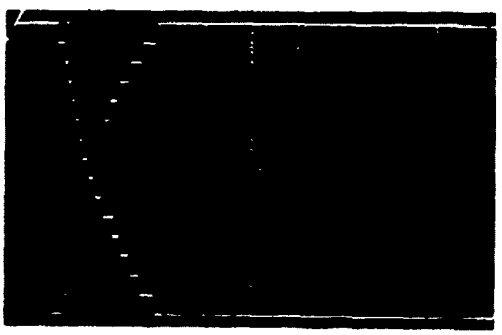
OUTPUT (D/A) INPUT LEVEL REDUCED
(INCLUDING DC OFFSET)
BEAT FREQUENCY (100 HZ)
SCALE. 1 MS/CM HORIZONTAL

Figure 30. Wave forms for time domain test, video pulse train and video pulse.

INPUT RISE TIME
SCALE 1 NSEC/CM HORIZONTAL
10% /DIVISION VERTICAL



INPUT FALL TIME
SCALE. 1 NSEC/CM HORIZONTAL
10%/DIVISION VERTICAL



OUTPUT (D/A) RISE AND FALL OF THE PULSE (100Hz BEAT FREQUENCY)
SCALE: 0 2 MSEC/CM →1.2 NSEC/DIVISION HORIZONTAL

NOTE: 10 TO 90 RISE AND FALL TIME OF A-D CONVERTER CALCULATED TO BE 1.18 NSEC.

Figure 31. Input rise and fall times for time domain test.