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SECOND QUARTERLY PROGRESS REPORT

1 OCTOBER 1976 TO 31 DECEMBER 1976

MANUFACTURING METHODS AND TECHNIQUES FOR MINIATURE HIGH VOLTAGE HYBRID MULTIPLIER MODULES

CONTRACT DAAB07-76-C-0041

PLACED BY:

PROCUREMENT & PRODUCTION DIRECTORATE

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The progress of the Manufacturing Methods and Technology Program for Miniature High Voltage Multiplier Modules is described in this Second Quarterly Report.

Work was concentrated on the design of the module's components - the capacitors, substrates and rectifiers. Rectangular multipliers were fabricated and tested.

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SECOND QUARTERLY PROGRESS REPORT

1 OCTOBER 1976 TO 31 DECEMBER 1976

MANUFACTURING METHODS AND TECHNIQUES FOR MINIATURE HIGH VOLTAGE HYBRID MULTIPLIER MODULES

CONTRACT NO. DAAB07-76-C-0041

PREPARED BY: DR. MICHAEL KORWIN-PAWLOWSKI

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ABSTRACT

The progress of the Manufacturing Methods and Technology Program for Miniature High Voltage Multiplier Modules is described in this Second Quarterly Report.

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PURPOSE

This Contract covers component designs, mounting and interconnection techniques, tooling and test methods and other manufacturing methods and techniques required for production of rectangular and curved miniature high voltage multiplier modules. These units are to be used in low cost power supplies for second generation image intensifier tubes. The full scope and details of the specification are given in SCS-495, Appendix A to the First Quarterly Report.

Major milestones in this program consist of delivery of the following items:

(1) First and second engineering samples and test data.

(2) Production line layout and schedule.

(3) Confirmatory samples and test data.

(4) Production line set-up.

(5) Pilot production run.

(6) Production rate demonstration.

(7) Preparation and publication of a final report.

The general approach is to design and set-up a cost-effective production capability, utilizing already established device technologies and materials, and to demonstrate the production line capability to fabricate at the rate of 125 acceptable units per 40 hour week.

GLOSSARY OF SPECIAL TERMS

Capacitor bank:	- Ceramic wafer with metallizations which perform the function of a number of capacitors connected in parallel (parallel bank) or in series (series capacitor bank).
Cure:	- To change the physical properties of a material by chemical reaction or by the action of heat and catalyst.
Flash test:	- Test consisting of instantaneous application of voltage at its specified value to the part.
Hybrid:	- Technology combining thick-films (capacitor banks) with discrete devices (rectifiers).
Multiplier modules:	- Device consisting of capacitor banks and rectifiers connected and packaged to perform voltage multiplication and rectification.
Pad:	- The metallized area on the ceramic bank acting as a plate of a capacitor and used to make an electrical connection to it.
Rectifier:	- Semiconductor device with one or more p-n junctions connected in series.

Rectifier-substrate assembly:	- A substrate with rectifiers placed and secured within it.
Substrate:	- Part of a multiplier module consisting of a piece of insulating material machined to accommodate the rectifiers and support the capacitor banks.

LIST OF SYMBOLS AND ABBREVIATIONS

ic	-	charging current (μA)
C_x	-	measured capacitance (pF)
D.F.	-	dissipation factor (%)
f	-	frequency (KHz)
C_i	-	input capacitance (pF)
I_L	-	load current (nA)
v_r	-	ripple voltage (V)
V_B	-	breakdown voltage (V)
V_i	-	input voltage (Vp-p)
V_o	-	output voltage (V d.c.)
η	-	efficiency (%)

1. INTRODUCTION

This report describes briefly the progress made during the period from 1 October to 31 December 1976.

In the initial effort on this program, described in the First Quarterly Report, it was possible to establish capacitor pad design that would reduce stray capacitance. Manufacture of prototype substrates assemblies demonstrated the unsuitability of the originally proposed design regarding diode pellet assembly and the complexity of jigging required in the assembly operation. A new substrate design was proposed. All effort is on the rectangular multiplier and once the major problem areas are identified and resolved, evaluation of the curved multiplier components will proceed.

2. MULTIPLIER DESIGN AND CHARACTERISTICS

The multiplier design adopted to meet this program's specifications was described in the First Quarterly Report.

Current work was concentrated on the individual components of the multiplier: the capacitors, substrate, and rectifiers.

2.1 Capacitors

The first prototype sample batch of capacitors, designated TSK 25-250 and TSK 25-251, was electrically tested for the following parameters:

(a) Capacitance and Dissipation Factor

(b) Leakage Current at bias

(c) Voltage breakdown and Flash-test.

For results see Tables 1 and 2.

The capacitance, dissipation factor and leakage were found satisfactory. Because of the stray capacitance of the test equipment it was not possible to measure the capacitance values at 6KV. Consequently, capacitance values were calculated using the voltage depression factor of -30% at 6KV for the K-1200 ceramic supplied by the Capacitor Manufacturer (Erie Technological Products, Inc., Erie, PA).

The flash test and breakdown voltage values indicate that the capacitors were unable to meet the expected volts/mil rating (9KV). Examination of the failed capacitors revealed that all breakdowns were a direct puncture through the ceramic. Failures were sent back to the manufacturer for further examination and analysis. The leakage currents measured at 6KV were found acceptable.

The flash test is more severe than the gradual increase of voltage on the capacitor to the same nominal value probably due to generated transients. While passing the flash test is very desirable, the failure of one or even more pads to withstand the flash test voltage does not necessarily mean that the capacitor will not operate satisfactorily in the multiplier. We have chosen 9KV as the flash test voltage which is in excess of what any capacitor will be subjected in operation or in acceptance testing.

In the first approximation, the maximum voltage on a TSK 25-251 capacitor will be on the pad connected to the output lead and will be equal to the output voltage. The highest values of the output voltage will be reached during over-voltage tests and according to SCS495 paragraph 3.3.4 will be 9KV for multipliers with efficiencies less than 88% and 7.8KV for multipliers with higher efficiencies. We aim in our design to achieve efficiencies above 88%. Other pads in the capacitor bank will have voltages lower by 1.3KV per stage away from the output stage, i.e. 6.5KV, 5.2KV, and so on. Assuming the efficiency exceeds 88% the highest voltage on a TSK 25-250 capacitor will be equal to the output voltage of 7.8KV reduced by the last diode reverse voltage drop of 1.3KV, i.e. 6.5KV. Pads farther away from the output will have lower maximum voltages across them: 5.2KV, 3.9KV, and so on.

Basing on the results of the present tests and on the results of testing the multipliers (Section 2.3), the TSK 25-250 and TSK 25-251 capacitors are acceptable. It would be however, interesting to see if any improvement in breakdown voltages could be achieved by redesigning the pad layout, without increasing the capacitor's thickness.

The capacitors TSK 25-254 and TSK 25-255 are of a version redesigned to improve dimensional conformity. The result is a slight reduction in pad length compared with previous design (Fig. 1 and 2). A capacitor bank pair, TSK 25-252 and TSK 25-253 was designed to improve the breakdown voltages (Fig. 3 and 4). In all four new capacitor banks the common electrode was redesigned so as to increase the tracking distance from the high-voltage output lead. The TSK 25-252 and TSK 25-253 banks have U-shape strip back electrodes offset toward the edges from the capacitor pads on the other side. This is to increase the effective dielectric thickness between the pads on each side of the capacitor bank.

Samples of rectangular capacitors of the original and new designs, as well as first curved capacitor samples, were ordered from Erie Technological Products, Inc., Erie, PA with an expected delivery of 4 to 5 weeks.

2.2 Rectifiers

The rectifiers are manufactured in-house by an established process for high-voltage rectifiers of the HV series.

Due to the substrate thickness limitation of approximately 0.040 inches, the originally proposed four-junction rectifiers were found dimensionally unsuitable. Consequently, two batches of fifty rectifiers per batch were fabricated as single and double-junction rectifiers. The body length of the single-junction device was 0.020 - 0.025 inches and for the two-junction device it was 0.030 - 0.035 inches. Both types of rectifiers were electrically tested at 3KV dc and 10nA maximum reverse leakage current. The tests were carried out at room temperature and devices with leakages in excess of 10nA were classed as rejects.

The single-junction rectifiers yielded 25% of good devices and two-junction rectifiers yielded 45% of good devices. Because of poor yields, it was decided to discontinue all further work with the single-junction devices.

A batch of fifty pieces was manufactured as three-junction rectifiers. The yield of devices with reverse leakage at 2000V below 2nA was 85%. The rectifier body length was between 0.038 to 0.042 inches. The three-junction rectifiers would appear to be most suited for this application regarding voltage rating and yields, but it does not allow to meet the originally proposed substrate thickness specification of 0.040 inches.

2.3 Substrates

A small number of substrates (3) was assembled using the two-junction rectifiers. The substrate material was glass-filled epoxy board 0.060 inches thick, type G-10, supplied by Warehouse Plastics, Toronto, Ont. The rectifiers were encapsulated in the substrate using thermosetting epoxy, (Waterford Specialties type X-7902.). The assembled substrates were lapped, by hand, on 400 grade carborundum paper. The object of this exercise was to evaluate the assembly technique and to determine the optimum substrate thickness after lapping. The final thicknesses were (1): 0.038 inches, (2): 0.041 inches, (3): 0.041 inches.

Three rectifier-substrate assemblies were manufactured using three-junction rectifiers. The final lapped thickness of the assemblies were (1): 0.052 inches, (2): 0.051 inches, (3): 0.052 inches.

A sample of machinable glass-ceramic (Macor, Code 96581) manufactured by Corning Glass was ordered for evaluation purposes and as an alternative to glass epoxy board presently used.

2.4 Multipliers

Three multipliers (units 1 to 3) were assembled in a way described in detail in the First Quarterly Report, using TSK 25-250 and TSK 25-251 capacitor banks and standard four-junction high voltage rectifiers soldered to the capacitor pads. One (unit #4) multiplier was assembled using capacitor banks and a prototype substrate made with two-junction high voltage rectifiers. Connections between the substrate and the capacitor pads were made using electrically conductive epoxy (EPO-TEK 410 of Epoxy Technology Inc., Watertown, Mass.).

The multiplier efficiency (at no load) was determined at different levels of input voltage at frequencies of 25 and 40KHz. After completion of those tests, multiplier voltage breakdown levels were determined.

Under test, the anode of the input rectifier was connected to ground and the units were tested in Fluorinert FC-43. The test circuit is given on Fig. 5 and the test results in Table 3.

The no-load efficiency readings on all multipliers were much better than anticipated. The breakdown on units 1, 2 and 3 occurred in all cases above the maximum voltage given in Table 4. In all cases the breakdown occurred in the last stage of the multiplier and manifested as a distinct puncture through the dielectric material. Unit No. 4 withstood an input voltage of 2000 volts and no physical defects could be detected after the tests.

The multiplier efficiency under load was measured on the unit No. 4 that survived breakdown tests carried out on prototype multipliers manufactured. The input voltage was 1000V peak-to-peak with a frequency of 40KHz. The results are given in Table 5.

The multiplier efficiency under load conditions was much better than anticipated. However, the construction of the tested multiplier did not conform to the proposed design, therefore, the efficiency results are not necessarily representative of what will be achieved with actual parts.

3. CONCLUSIONS

1. The first prototype sample batch of capacitors was electrically tested and found generally satisfactory, but further improvement is expected with design modifications.

2. A three-junction high-voltage rectifier has been chosen for the multiplier module as optimal from the point of view of performance and cost.

3. Rectangular multipliers were fabricated and tested with good results.

4. PROGRAM FOR NEXT QUARTER

1. Evaluate the redesigned rectangular capacitor banks.

2. Manufacture prototype multipliers with different capacitor banks and rectifier-substrate-assemblies.

3. Manufacture a large batch of three-junction rectifiers.

4. Evaluate the curved capacitor banks.

5. PUBLICATION AND REPORTS

No reports or publications were made on the work associated with this program during the current quarter.

6. IDENTIFICATION OF PERSONNEL

A brief description of the background of technical personnel involved is included in the First Quarterly Report. Background of personnel added to the program during the second quarter follows.

During the second quarter of this program the following persons worked in their area of responsibility:

Individual	Responsibility	Hours Spent
P. Ransom	General Manager, High Voltage Products	2
A. Kennedy	Program Manager (until March 25/77)	356
G. Gordon	Senior Electronic Engineer	13
D. Platt	Manager, Quality Assurance & Control	28
D. Archard	Q.C. Test Technician	58
D. Regan	Senior Engineering Technician	35
V. Glenn	Q.A. Assistant	32

D. ARCHARD Senior Test Technician

PROGRAM RESPONSIBILITY

Design and construction of electrical test equipment and related fixtures.
Test and evaluation of special multiplier designs.
Q.A. functions related to Engineering samples and acceptance evaluations.

CURRENT ASSIGNMENT

Responsible for the Q.C. Test and Inspection Audit of all products currently being manufactured by the High Voltage Rectifier group.
Q.C./Q.A. related duties such as special test applications and the fabrication of equipment and fixtures.

ACADEMIC AND PROFESSIONAL BACKGROUND

1969	Electronic Technician Diploma, Loyalist College, Ontario
	Various Q.C. Related Courses.
1971 - present	Employed by Erie Technological Products of Canada Ltd., as a Q.C./Q.A. Test Technician.

V. GLENN Q.C. Inspector

PROGRAM RESPONSIBILITY

Test and evaluation of procured materials and assemblies.
Clerical Duties.

CURRENT ASSIGNMENT

Responsible for the Q.C. Receiving Inspection and Test of Procured Materials.
Secretarial duties to both Q.C./Q.A. and Engineering Departments.
Assistant to the Q.C./Q.A. Manager.

ACADEMIC AND PROFESSIONAL BACKGROUND

1969	Completed Business Course - Bookkeeping, Typing, Accounting experience.
1973	Various Data Processing Courses, Loyalist College, Ontario.
1974	Various Q.C. Related Courses.
1974	Electrical Fundamentals Course, Loyalist College, Ontario.
1972 - present	Employed by Erie Technological Products of Canada Ltd., as: 1972 - Production Assembler 1973 - Q.C. Inspector 1975 - Q.C. Inspector - Lead Hand 1976 - Assistant to the Q.C./Q.A. Manager.

D.P. REGAN Senior Engineering Technician

PROGRAM RESPONSIBILITY

Production of substrate for voltage multiplier modules plus manufacture of jigs and fixtures required for Production use.

CURRENT ASSIGNMENT

Manufacture or modification of material and components for use by High Voltage Engineering and Production Departments. Manufacture or modification of tooling, jigs and fixtures for use by High Votlage Production Departments. Manufacture of book molds for making components or assemblies for High Voltage Engineering and Production Departments.

ACADEMIC AND PROFESSIONAL BACKGROUND

Completed 4 year S.T.&T. course at East Northumberland High School, 1965.
Certified Machinist by Ontario Dept. of Labour, 1970.

1974 - present	Employed as Sr. Eng. Technician by Erie Technological Products of Canada Ltd.
1973-1. +	Machine Operator, L.C. Shewman Co., Wooler, Ont.
1970-1973	Machine Operator, Bata Engineering, Batawa, Ont.
1970	Finishing Lathe Operator, Canadian Flight Equipment, Trenton, Ont.
1966-1970	Apprentice, Bata Engineering, Batawa, Ont.

ACCEPTANCE OF MATERIAL SUBJECT TO APPROVAL OF PRODUCTION SAMPLES BY ENGINEERING DEPARTMENT
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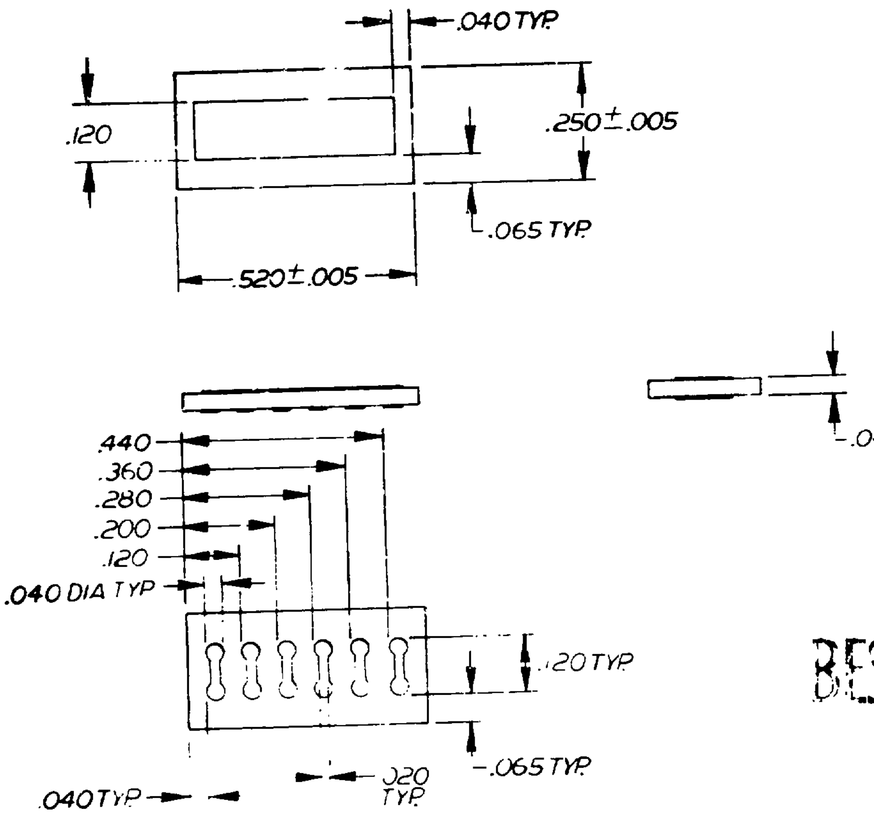

ELECTRICAL SPECIFICATION

1.1

WORKING VOLTAGE	OPERATING TEMPERATURE	CAP. (PF.) & TOL. / SECT.
6.0 K.V.	+ 25°C	55 PFD ± 20%

1.2 TEMPERATURE CHARACTERISTICS (X5R)
1.3 DIELECTRIC STRENGTH TEST VOLTAGE 9.0 K.V. AT 25°C.
1.4 INSULATION RESISTANCE AT TEST VOLTAGE + 25°C.
— 100 KM. OR 1000 M.Ω MFD.
1.5 CAPACITANCE AT 25°C. & 1 KHZ., 1 V. RMS. & WORKING VOLTAGE. — SEE TABLE ABOVE.
1.6 D.F. UNDER SAME CONDITION AS REF. 1.5 SHOULD BE < 2.5%.
1.7 SCHEMATIC

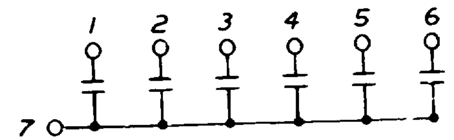

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FIG. 1

SCALE : 4 = 1

[redacted]

ERIE

PARALLEL BANK CAPACITOR

TOLERANCES UNLESS OTHERWISE SPECIFIED		DWN. 25/APR/77	CKD.
FRACTIONS	—	MATERIAL	
DECIMAL	.002	BTSK-25-254	REV
ANGLES	0°30'		

BTSK-25-254 | REV.

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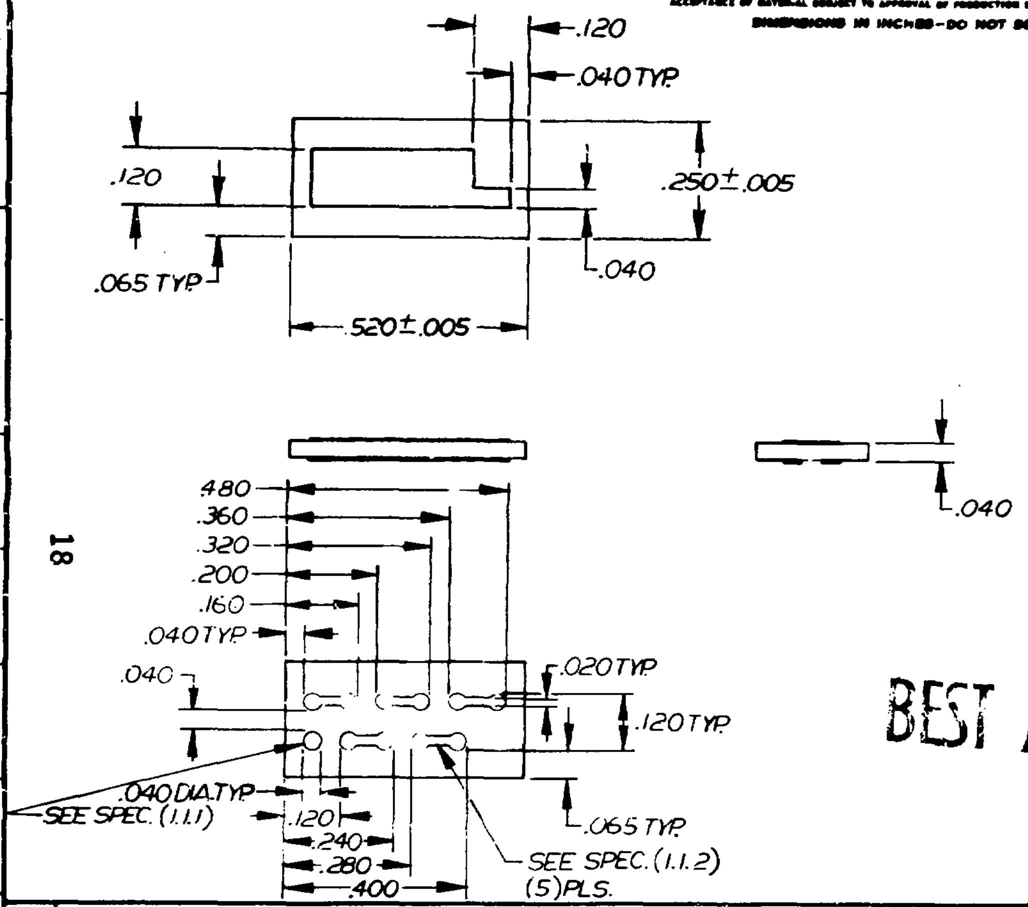

ELECTRICAL SPECIFICATION

1.1

	WORKING VOLTAGE	OPERATING TEMPERATURE	CAP. (P.F.) & TOL. / SECT.
(1.1.1)	6.0 K.V.	+ 25°C	25PFD ± 20%
(1.1.2)	6.0 K.V.	+ 25°C	55PFD. ± 20%

1.2 TEMPERATURE CHARACTERISTICS (X5R)
1.3 DIELECTRIC STRENGTH TEST VOLTAGE 9.0 K.V. AT 25°C.
1.4 INSULATION RESISTANCE AT TEST VOLTAGE + 25°C — 100 KM. OR 1000 M.Ω MFD.
1.5 CAPACITANCE AT 25°C. & 1 KHZ. 1 V. RMS. & WORKING VOLTAGE. — SEE TABLE ABOVE.
1.6 D.F. UNDER SAME CONDITION AS REF. 1.5 SHOULD BE < 2.5%.
1.7 SCHEMATIC

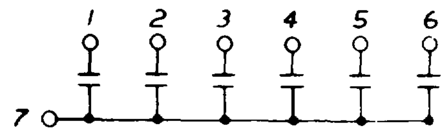

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FIG. 2

SCALE 4=1

PARALLEL BANK CAPACITOR

TOLERANCES		DWN	24/APR/77
FRACTIONS		MATERIAL	—
DECIMAL	.02		
ANGLE	0°30	BTSK-25-255	REV

BTSK-25-255

REV.

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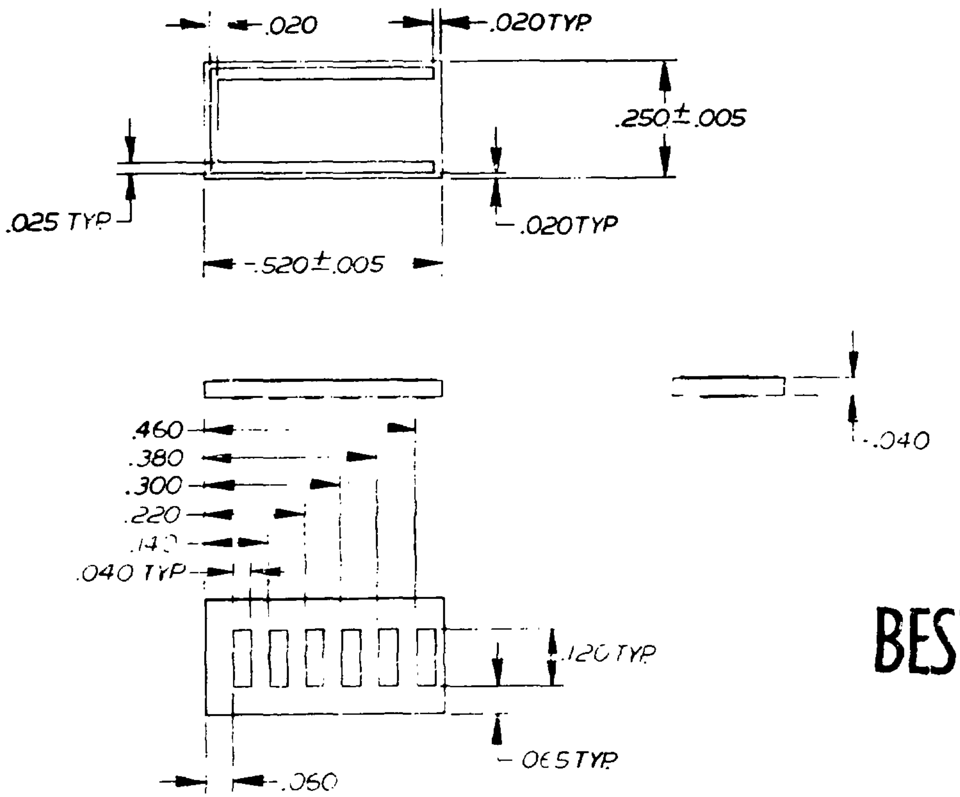
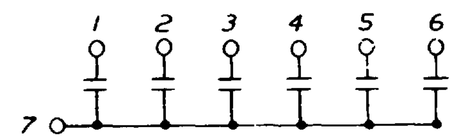


ELECTRICAL SPECIFICATION

1.1

WORKING VOLTAGE	OPERATING TEMPERATURE	CAP. (P.F.) & TOL. / SECT.
6.0 K.V.	+ 25°C	50PFD ± 20%

1.2 TEMPERATURE CHARACTERISTICS (X5R)
1.3 DIELECTRIC STRENGTH TEST VOLTAGE 9.0 K.V. AT 25°C.
1.4 INSULATION RESISTANCE AT TEST VOLTAGE + 25°C. — 100 K.M. OR 1000 M.Ω MFD.
1.5 CAPACITANCE AT 25°C. & 1 KHZ., 1 V. RMS & WORKING VOLTAGE. — SEE TABLE ABOVE.
1.6 D.F. UNDER SAME CONDITION AS REF. 1.5 SHOULD BE $< 2.5\%$.
1.7 SCHEMATIC



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SCALE : 4 = 1

FIG. 3

PARALLEL BANK CAPACITOR

ERIE

TOLERANCES	
FRACTIONS	—
DECIMAL	.002
ANGLES	0°30'

DWN. L. MAYLIN 2_ APR. 77
CKD.
MATERIAL

BTSK-25-252

REV.

BTSK-25-252

REV.

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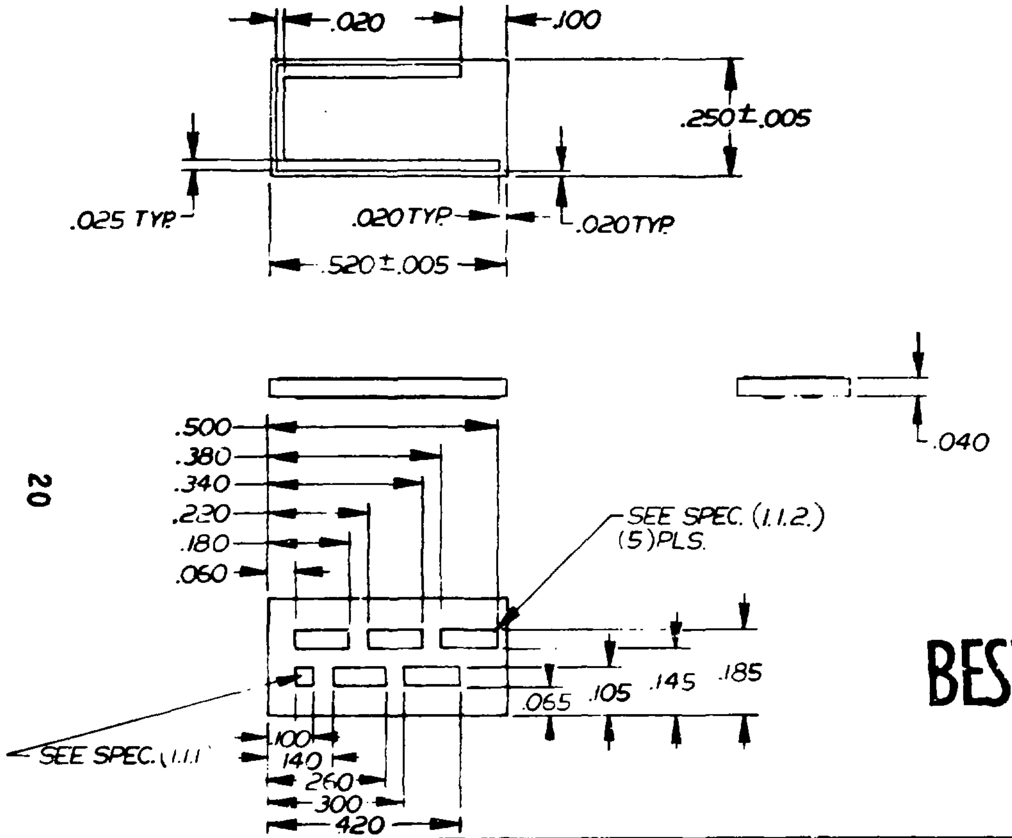

ELECTRICAL SPECIFICATION

1.1

	WORKING VOLTAGE	OPERATING TEMPERATURE	CAP. (P.F.) & TOL. / SECT.
(1.1.1)	6.0 K.V.	+ 25°C	20 PFD ± 20%
(1.1.2)	6.0 K.V.	+ 25°	50 PFD ± 20%

1.2 TEMPERATURE CHARACTERISTICS (X5R)
1.3 DIELECTRIC STRENGTH TEST VOLTAGE 9.0 K.V. AT 25°C.
1.4 INSULATION RESISTANCE AT TEST VOLTAGE + 25°C. — 100 K.M. OR 1000 M.Ω MFD.
1.5 CAPACITANCE AT 25°C. & 1 KHZ., 1 V. RMS. & WORKING VOLTAGE. — SEE TABLE ABOVE.
1.6 D.F. UNDER SAME CONDITION AS REF. 1.5 SHOULD BE < 2.5 %.
1.7 SCHEMATIC

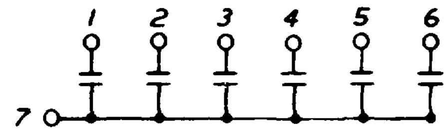

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FIG. 4

SCALE: 4 = 1

PARALLEL BANK CAPACITOR

TOLERANCES UNLESS OTHERWISE SPECIFIED

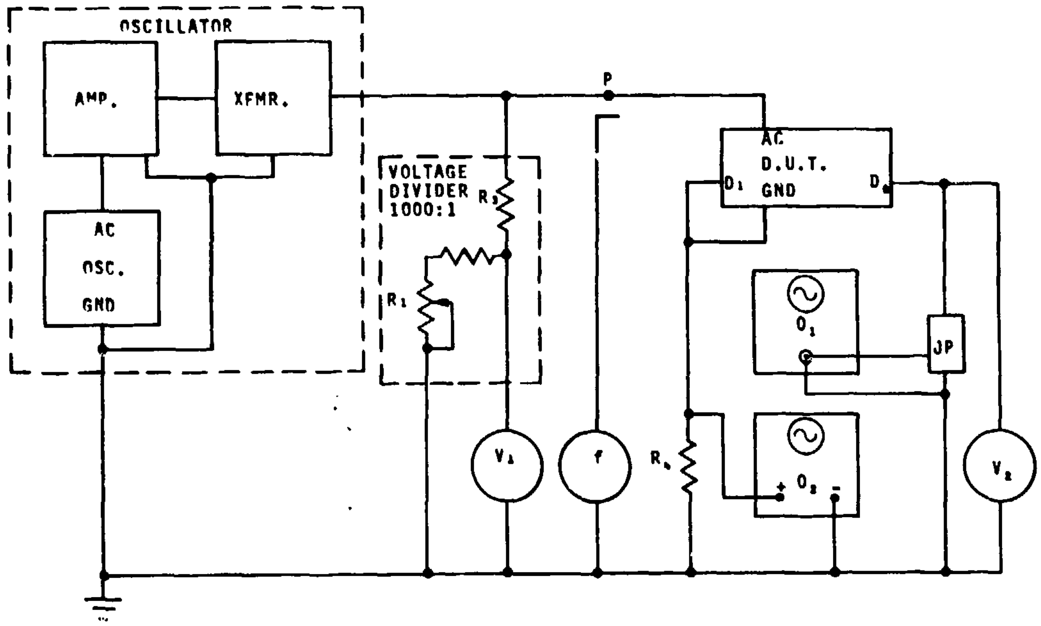
FRACTIONS	± —
DECIMAL	±.002
ANGLES	±0°30'

DWN. L. MACKLIN 25 APR '77
CKD.
MATERIAL

BTSK-25-253

REV.

MULTIPLIER OPERATIONAL TEST CIRCUIT



NOTE:

(1) Point P is the location of the proximity electromagnetic coupling of the electronic (frequency) counter.

(2) Dotted lines represent functional blocks.

EQUIPMENT:

OSC.	-	Oscillator, Hewlett Packard Model #200CDR
AMP.	-	Amplifier, Bogen Model #MO-100A
XFMR.	-	Horizontal Output Transformer; Chicago Stadard Transformer Corp., Model #AB127.
V_1	-	Voltmeter, Digitec Model #201
f	-	Electronic Counter, Hewlett Packard Model #5321A
O_1	-	Oscilloscope, Tektronix Model #536
O_2	-	Oscilloscope, Hewlett Packard Model #120AR
JP.	-	Jennings Probe, Erie Model #TEX-105-300
V_2	-	Taunt Band Electrostatic Kilovoltmeter, High Voltage Measurement Inc., Model KVE (5, 15, 30 KV ranges)
D.U.T.	-	Device Under Test (i.e. Voltage Multiplier)
R_1	-	1.0 Megohm Variable, 10 Turn Potentiometer for calibration adjustment
R_2	-	1.0 Megohm, 10%
R_3	-	1.0 Gigohm, 15%, 15KV
R_4	-	1.0 Kilohm, 10%, 2W

FIG. 5.

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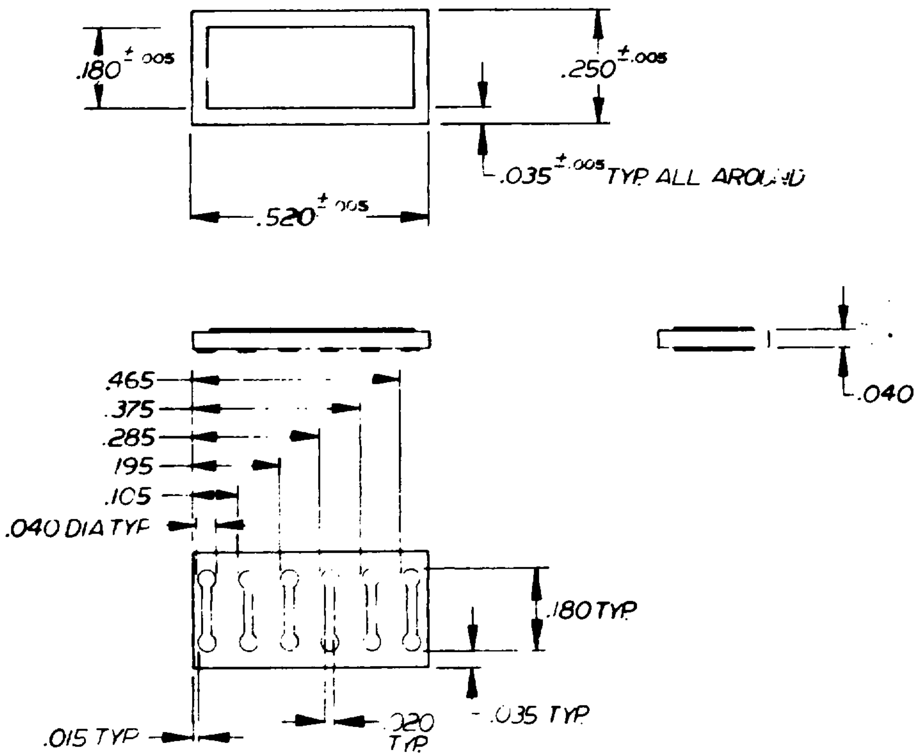


ELECTRICAL SPECIFICATION

1.1

WORKING VOLTAGE	OPERATING TEMPERATURE	CAP. (PF.) & TOL. / SECT.
6.0 K.V.	+ 25°C	55 pF ±20%

1.2 TEMPERATURE CHARACTERISTICS (X5R)
1.3 DIELECTRIC STRENGTH TEST VOLTAGE [illegible] K.V. AT 25°C.
1.4 INSULATION RESISTANCE AT TEST VOLTAGE + 25°C. — 100 KM. OR 1000 M.Ω MFD.
1.5 CAPACITANCE AT 25°C. & 1 KHZ., 1 V. RMS. & WORKING VOLTAGE. — SEE TABLE ABOVE.
1.6 D.F. UNDER SAME CONDITION AS REF. 1.5 SHOULD BE < 2.5%.
1.7 SCHEMATIC

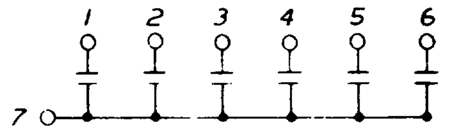


FIG. 6

SCALE: 4=1

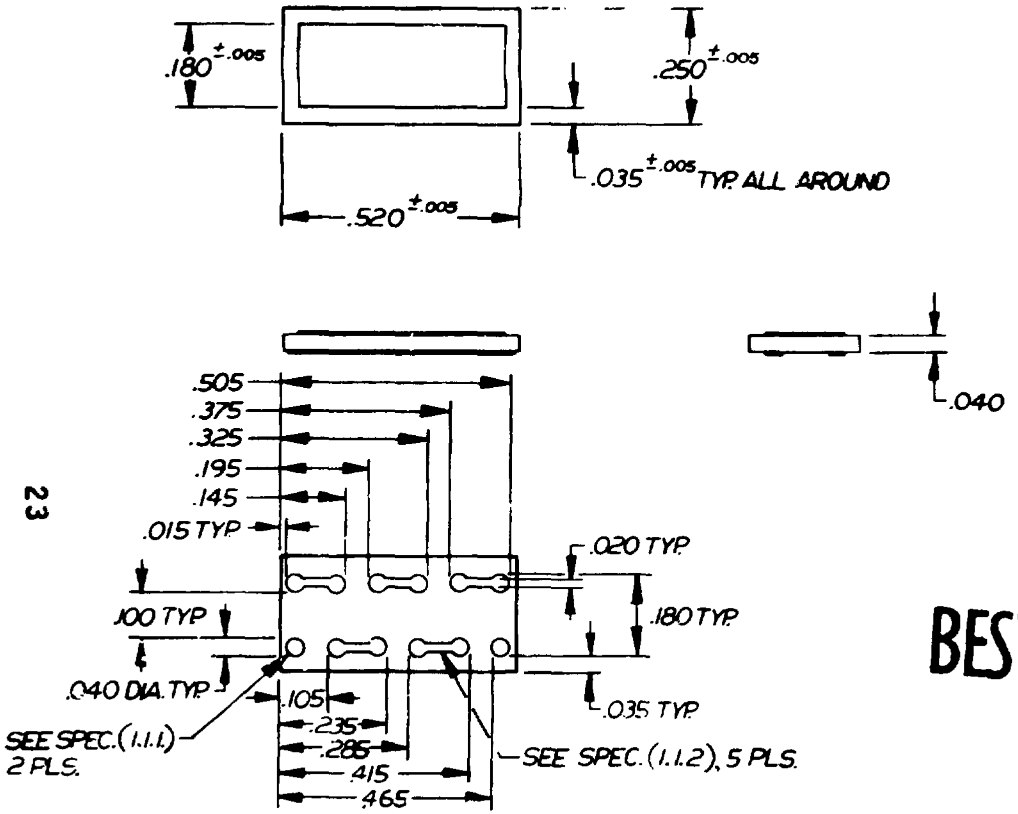
PARALLEL BANK CAPACITOR

TOLERANCES UNLESS OTHERWISE SPECIFIED	
FRACTIONS	± —
DECIMAL	±.002
ANGLES	±0°30'

DWN. 5/MAY/77
CKD.
MATERIAL

BTSK-25-250 REV.

ERIE

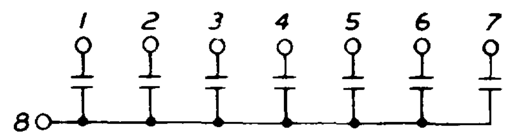


ELECTRICAL SPECIFICATION

1.1

	WORKING VOLTAGE	OPERATING TEMPERATURE	CAP. (PF.) & TOL. / SECT.
(1.1.1)	6.0 K.V.	+ 25°C	20 pF ±20%
(1.1.2)	6.0 K.V.	+ 25°C	45 pF ±20%

1.2 TEMPERATURE CHARACTERISTICS (X5R)
1.3 DIELECTRIC STRENGTH TEST VOLTAGE 9.0 K.V. AT 25°C.
1.4 INSULATION RESISTANCE AT TEST VOLTAGE + 25°C. — 100 KM. OR 1000 M.Ω MFD.
1.5 CAPACITANCE AT 25°C. & 1 KHZ., 1 V. RMS. & WORKING VOLTAGE. — SEE TABLE ABOVE.
1.6 D.F. UNDER SAME CONDITION AS REF. 1.5 SHOULD BE < 2.5%.
1.7 SCHEMATIC



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SCALE 4=1

FIG. 7

PARALLEL BANK CAPACITOR

TOLERANCES

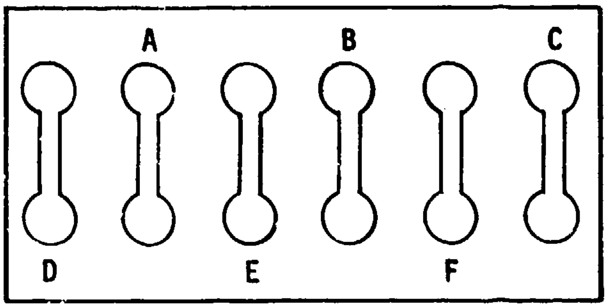
FRACTIONS	±
DECIMAL	± .002
ANGLES	± 0°30'

BTSK-25-251

REV

23

CHARACTERISTICS OF TYPE TSK-25-250 CAPACITOR

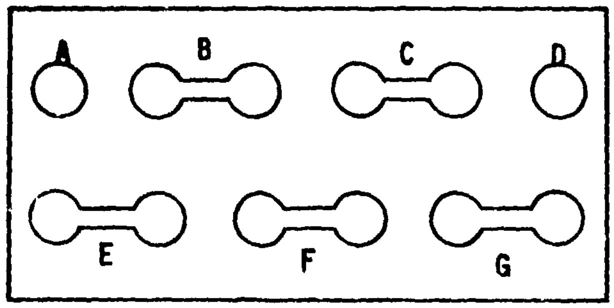


Bottom Pad Grounded

PAD	C_x @ no bias (pF)	D.F. (%)	C_x @ 6KV (pF)	LEAKAGE CURRENT @ 6KV (nA)	V_B (KV)	FLASH-TEST @ 9KV
A	88.7	0.36	62.1	10	7.9	FAIL
B	88.3	0.36	61.3	12	7.9	FAIL
C	51.0	0.22	35.7	12	8.1	FAIL
D	58.0	0.23	40.6	11	7.9	O.K.
E	90.0	0.37	63.0	13	7.5	FAIL
F	84.1	0.32	58.9	13	8.5	FAIL

TABLE 1

CHARACTERISTICS OF TYPE TSK-25-251 CAPACITOR



Bottom Pad Grounded

PAD	C_x @ no bias (pF)	D.F. (%)	C_x @ 6KV (pF)	LEAKAGE CURRENT @ 6KV (nA)	V_B (KV)	FLASH-TEST @ 9KV
A	23.5	0.12	16.5	8	> 9	FAIL
B	64.6	0.25	45.2	9	> 9	FAIL
C	65.4	0.28	45.8	10	> 9	FAIL
D	23.6	0.15	16.5	10	> 9	FAIL
E	51.2	0.21	35.8	10	> 9	FAIL
F	63.8	0.27	44.7	11	> 9	FAIL
G	54.0	0.30	37.8	10	> 9	FAIL

TABLE 2

MULTIPLIER EFFICIENCY

(units tested in Fluorinert FC-43)

		UNIT #1		UNIT #2		UNIT #3		UNIT #4	
V_i (Vpp)	f (KHz)	V_o (KV)	η (%)	V_o (KV)	η (%)	V_o (KV)	η (%)	V_o (KV)	η (%)
200	25	1.12	93	1.10	92	1.11	93	1.14	95
200	40	1.14	95	1.10	92	1.11	93	1.12	93
300	25	1.75	97	1.77	98	1.77	98	1.76	98
300	40	1.75	97	1.78	99	1.78	99	1.78	99
500	25	2.90	97	2.90	97	2.90	97	2.91	97
500	40	2.89	96	2.90	97	2.90	97	2.90	97
700	25	3.96	94	3.95	94	4.02	96	4.03	96
700	40	3.98	95	3.93	94	4.01	95	4.00	95
800	25	4.53	94	4.52	94	4.60	96	4.59	96
800	40	4.54	95	4.50	93	4.58	95	4.60	96
900	25	5.10	94	5.10	94	5.20	96	5.20	96
900	40	5.10	94	5.10	94	5.20	96	5.20	96
1000	25	5.70	95	5.50	92	5.75	96	5.75	96
1000	40	5.70	95	5.50	92	5.75	96	5.75	96
1200	25	6.80	94	6.70	93	6.90	96	6.95	97
1200	40	6.80	94	6.70	93	6.90	96	6.95	97
1500	25	8.60	95	8.60	95	8.70	96	8.70	96
1500	40	8.60	95	8.60	95	8.70	96	8.70	96

TABLE 3

MULTIPLIER BREAKDOWN VOLTAGES

Unit No.	1	2	3	4
VB (KV)	9.3	10.8	9.8	11.5

TABLE 4

NOTE: Input frequency: 40KHz
Devices immersed in Fluorinert FC-43

MULTIPLIER UNIT #4 EFFICIENCY UNDER LOAD

Test Conditions: Input Voltage: 1000 Vp-p

Frequency: 40KHz

LOAD CURRENT (nA)	OUTPUT VOLTAGE (KV dc)	EFFICIENCY (%)
0	5.80	96.75
10	5.78	96.40
50	5.78	96.40
100	5.77	96.20
300	5.76	96.00
500	5.75	95.80
700	5.75	95.80

TABLE 5

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