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HIGH-RELIABILITY, LOW-COST INTEGRATED CIRCUITS.(U)
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FIFTH QUARTERLY DEVELOPMENT REPORT

FOR

HIGH-RELIABILITY, LOW-COST INTEGRATED CIRCUITS

3 FEBRUARY 1977 TO 3 MAY 1977

Prepared By
RCA Solid State Divison
Route 202, Somerville, N.J. 08876

For

DEPARTMENT OF THE NAVY
NAVAL ELECTRONICS SYSTEMS COMMAND
Washington, D.C.

Contract No. N00039-76-C-0240
Project No. 62762N
Subproject No. XF54586
Task No. 002

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SECTION I

ABSTRACT

Wafer fabrication for the CA741, 5420, 54S20, 5470, 5472, CD4012B, CD4027B, and CD4014A has been initiated. Lead wafers for most of the circuits are in the metallization process. The required array of life-test sockets for each type has been ordered, and samples of CD4012B and CA741 are being assembled for accelerated life test and step-stress testing. Initial reliability data obtained on CA741 devices indicate that the contract goal of less than 0.005% failures per 1000 hours at 125°C operating life is attainable.

SECTION II
PURPOSE

The objective of this program is to investigate alternate approaches to MIL-M-38510 for achieving high reliability integrated circuits at low cost. Emphasis is on adapting existing technology to industry mainstream products to achieve semiconductor reliability which will meet military requirements without a severe cost penalty.

The approach to achievement of the goals of this program will be the integration and application of existing sealed-chip integrated-circuit processing with automated plastic packaging. The program will be carried out in three phases.

Phase I - Completed

(a) Process Feasibility - The required photomasks were generated using existing masks to the maximum extent possible. Then, small quantities of each device type were fabricated to assure that the masks and processes were available for the production runs of Phase II. Also, each device type was fabricated using a matrix of carefully varied process parameters to assess their impact on yields and reliability.

(b) Process Development - The processes required to fabricate the eight integrated-circuit types to be produced in Phase II were defined and documented. Silicon nitride passivation and the titanium-platinum-gold metallization system were used to achieve chip hermeticity and a corrosion-free metallization system. In addition, a silicon nitride overcoat layer was applied for protection of the metallization. A series of experiments was completed at each critical processing step to

assure repeatability. Real-time indicators and accelerated life tests were used to assess the effects of process changes on reliability and to measure progress in achieving the required failure rate.

(c) Automated Assembly - The technology to be used in Phase II was defined and documented. The effect of assembly process parameters on cost and yield was assessed. Bonding tapes and lead-frames compatible with each of the device types were designed and fabricated. A number of devices of each type were assembled using the automated assembly system. Reliability was monitored continually by means of accelerated life tests.

The photomasks, wafer process, and assembly process required to fabricate the eight integrated-circuit types in the low-cost high-reliability device-fabrication phase have been defined and documented and sample devices of each type were fabricated. Additionally, preliminary reliability data have been generated to demonstrate the soundness of the chosen approach.

At this time, the production runs of Phase II have begun.

Phase II - Fabrication

The low-cost high-reliability device fabrication phase of the program will involve significant quantities of each of the eight selected integrated-circuit types to be fabricated according to the processes defined in Phase I. Both silicon nitride passivated, titanium-platinum-gold metallized integrated circuits and conventional silicon dioxide, aluminum-metallized integrated circuits will be constructed in both plastic and ceramic packages. This will permit a detailed comparison to be made of the new and conventional processes. During these production runs, any significant differences between the two processes will be defined and documented. The utilization of existing equipment and mask sets will be demonstrated, and the cost impact of converting to this type of processing will be estimated. In-process quality controls, real-time indicators, and parameter distributions

at wafer probe and final test will be used to monitor the production run and to assure process reproducibility. All devices produced in this phase of the program will be utilized in Phase III for reliability testing and delivery to the Navy. Finally, the testing facilities for the Phase III program will be defined and asembled.

Phase III - Reliability

The reliability of the devices produced in Phase II will be demonstrated. The conventional aluminum-metallized integrated circuits, packaged and tested to military high-reliability requirements, will be used as the baseline from which to appraise the new process developed under the program. In addition, the level of testing required over and above commercial screening to assure a reliable product for military end use will be determined, and the cost impact of this testing will be analyzed and verified.

SECTION III
PHASE II PROGRAM

Phase II, the low-cost high-reliability device-fabrication phase of the program, will involve significant quantities of each of the eight selected integrated-circuit types to be fabricated according to the processes defined in Phase I. Both silicon nitride passivated, titanium-platinum-gold metallized integrated circuits and conventional silicon dioxide, aluminum-metallized integrated circuits will be constructed in both plastic and ceramic packages. This plan will permit a detailed comparison to be made of the new and conventional processes. During these production runs, any significant differences between the two processes will be defined and documented. The utilization of existing equipment and mask sets will be demonstrated, and the cost impact of converting to this type of processing will be estimated. In-process quality controls, real-time indicators, and parameter distributions at wafer probe and final test will be used to monitor the production run and to assure process reproducibility. Devices produced in this phase of the program will be utilized in Phase III for reliability testing and delivery to the Navy. Finally, the testing facilities for the Phase III program will be defined and assembled. The milestone chart for Phase II is shown in Fig. III-1.

As shown in Fig. III-2, the minimum quantity of units required for delivery to the Navy and for the Phase III test plan is 5165 devices per type. Reliability testing during Phase II will require additional units, and other needs will surface during the course of the contract. It is anticipated, therefore, that approximately 10,000 units of each type will be fabricated during Phase II.

In addition to initiating the long-term 125°C life tests during Phase II, a program of accelerated life testing is planned for two circuits,

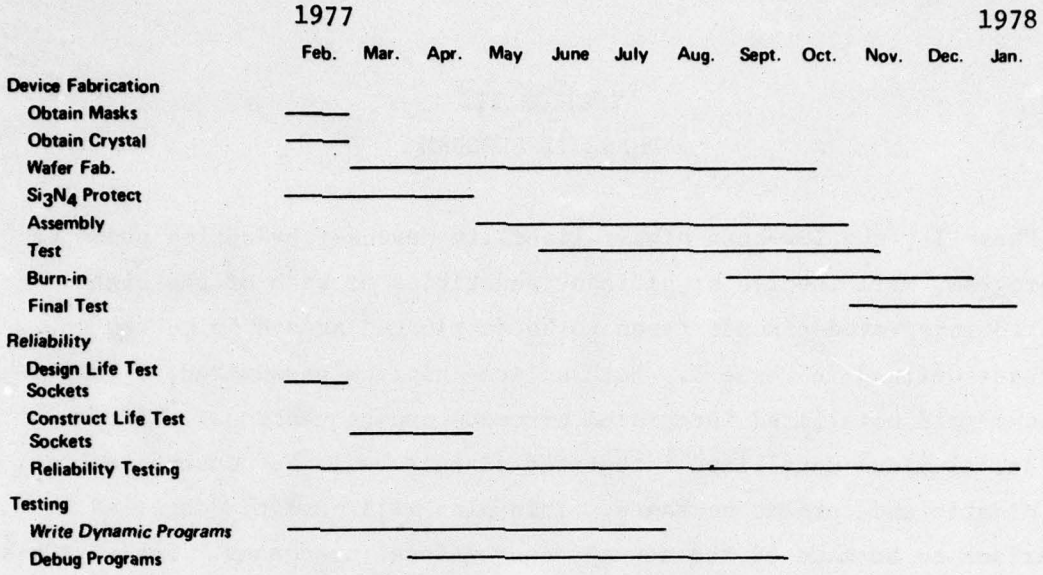

Fig. III-1 - Phase II Milestone Chart

Type	CD4012B	CD4014A	CD4027B	CA741	5420	54S20	5470	5472
Technology	COS/MOS	COS/MOS	COS/MOS	Bipolar Linear	Au-T^2L	Schottky	Au-T^2L	Au-T^2L
Wafer Lot Size	25	25	25	25	25	25	25	25
Net Units Required								
Internal								
Al DIP	115	→						
Al DIC	145	→						
Trimetal DIC	155	→						
Trimetal DIC (Unencapsul.)	25	→						
Trimetal DIP	725	→						
To Be Delivered	4000	→						
Total	5165	→						

Fig. III-2 - Phase II Device Fabrication Plan.

the CA741 and the CD4012B. This program will verify that the reliability goals of the program are being met, compare the encapsulation techniques, and compare the results achieved with devices in dual-in-line ceramic packages. The planned test matrices are shown in Fig. III-3.

Life Tests	Encapsulation Technique				
	Silicone	Epoxy Novolac	Epoxy Novolac With Junction Coat	DIC	Non-Hermetic DIC
Bias					
150°C	20	20	20	15	15
175°C	20	20	20	15	15
200°C	20	20	20	15	15
225°C	20	20	20	15	15
250°C	20	20	20	15	15
Storage					
150°C	15	15	15	10	10
175°C	15	15	15	10	10
200°C	15	15	15	10	10
225°C	15	15	15	10	10
250°C	15	15	15	10	10
Step Stress					
150°C	20	20	20	15	15

Types: CD4012B, CA741

Fig. III-3 - Phase II Test Plan.

SECTION IV

DETAILED FACTUAL DATA

TECHNICAL DISCUSSION

Product Generation

Masks and wafers for the eight integrated circuit types have been ordered. Wafers of all eight circuits are currently being processed. A by-type status report of wafers in the production line is shown in Table IV-1.

Gold Plating Process Refinement

Tests have been run which indicate that improved conformity of the silicon nitride protective layer is obtained if the walls of the gold interconnect metallization are only minimally reentrant. The use of positive photoresist to plate the gold lines results in more nearly vertical gold sidewalls. The scanning electron microscope photo in Fig. IV-1 shows a gold line which has been plated using negative photoresist. Fig. IV-2 shows a similar plated gold line using positive resist. As a result of this improvement in line contour, the process has been converted to the use of positive photoresist.

Junction Seal Integrity Testing

Junction seal integrity testing of the 200 Å Si_3N_4 layer used on the CMOS circuits and the 2000 Å Si_3N_4 layer used on the bipolar circuits was performed using small signal n-p-n transistors incorporating these layers. The samples for JSI testing were contaminated in open DIC packages with a 10% solution of sodium chloride and then dried. The devices were then subjected to 250°C bias life with 30 volts for the bipolar Si_3N_4 thickness and 12 volts for the CMOS 200 Å Si_3N_4 layer. A summary of the test is shown in Table IV-2.

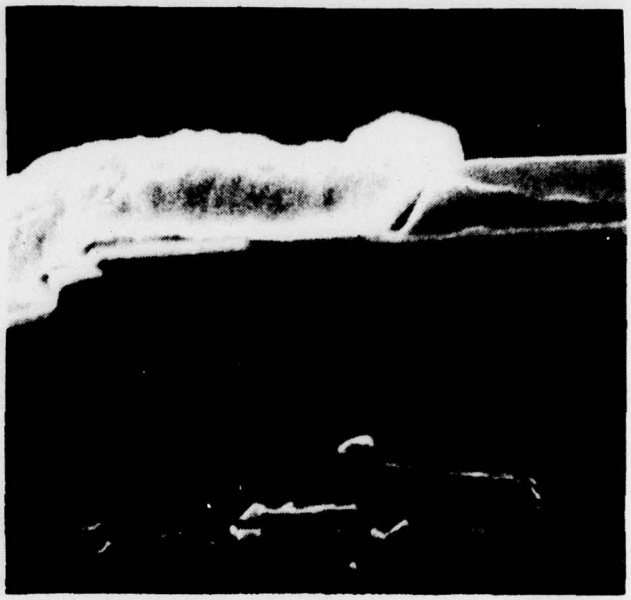

Fig. IV-1 - SEM photograph of a gold line (∿15 kA thick) plated by means of negative photoresist.

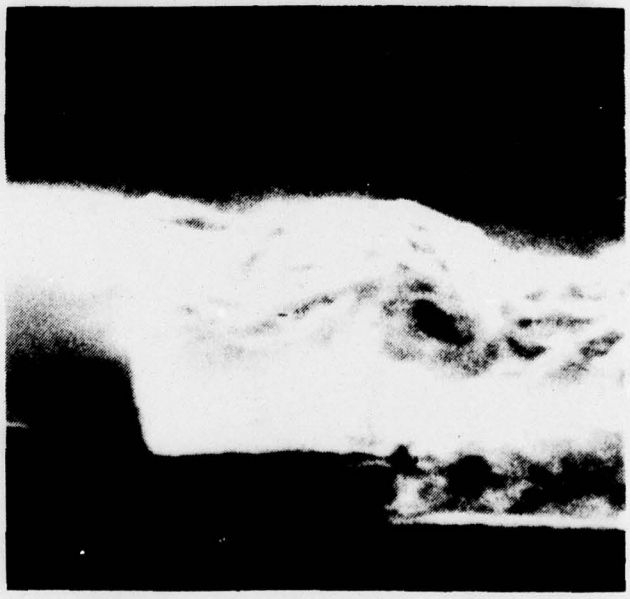

Fig. IV-2 - SEM photograph of a gold line (∿15 kA thick) plated by means of positive photoresist.

TABLE IV-2

SUMMARY OF JSI TESTS

Device Conditions	Si_3N_4 Thickness	Voltage Stress	Sample Size	Failures At 3 Hrs	Failures At 8 Hrs
CMOS	200 Å	12 Volts	13	0/13	0/13
CA741 Bipolar	2000 Å	30 Volts	8	1/8*	0/7

* Opened Package, Handling Related Failure

JSI Test - 8 Hours Bias Test, NaCl Contaminant, Forming Gas Atmosphere, 250°C

Radioactive Tracer Comparison of Plasma-Deposited Si_3N_4 and Commonly Used SiO_2 Layers

Radioactive-tracer evaluations are used to determine the effectiveness of deposited silicon nitride films as alkaline barriers. Test wafers are coated with a layer of Si_3N_4, 2000 Å for bipolar circuits and 200 Å for COS/MOS circuits, over a 3000 Å layer of SiO_2. A 0.2-mil solution containing 1.31×10^{-6} atoms Na and 4 microcuries Na_{22} is used to coat a nickel electrode, which is dried under a heat lamp. The wafers are coated with this tracer element by evaporation at a pressure of 10^{-6} torr and subsequently annealed at 600°C for 22 hours. At this point, the surface radioactivity (R) of Na_{22} is determined. The test wafers are then etched to remove approximately 10 Å of Si_3N_4, and the surface radioactivity of the fresh surfaces determined.

Results of radioactive tracer measurements for plasma deposited silicon nitride, chemical vapor deposited phosphorus silicate glass, thermally grown SiO_2, and CVD Si_3N_4 are shown in Fig. IV-3. The results show the plasma deposited nitride to be an effective sodium barrier relative to PSG and thermally grown SiO_2 layers.

Reliability Data

A summary of reliability data taken on gold metallized, silicon nitride overcoated CA741 circuits is shown in Table IV-3.

Samples of CA741 and CD4012B for accelerated life tests and step stress tests are currently in the assembly area.

Status of Life Test Sockets

The status of life test sockets for CA741, CD4012B, and 5420 is shown in Table IV-4.

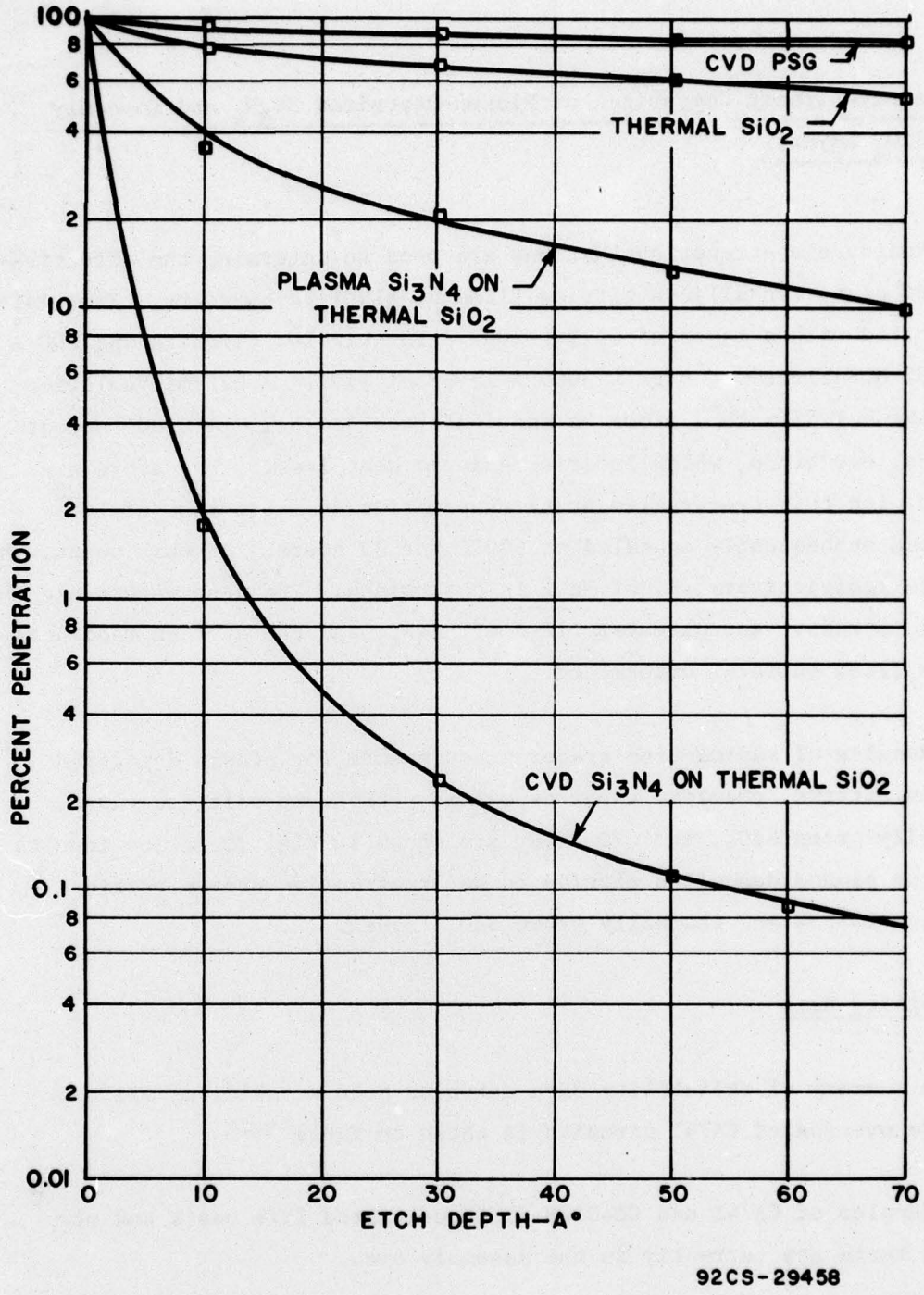

Fig. IV-3 - Results of radioactive tracer measurements for plasma deposited silicon nitride, chemical vapor deposited phosphorus silicate glass, thermally grown SiO_2, and CVD Si_3N_4.

TABLE IV-3

RELIABILITY DATA

TRIMETAL TYPE CA741 DEVICES - Si_3N_4 DIELECTRIC OVERCOAT

Molding Compound	Assembly	Exposure	Duration (hrs)	Fail/Pass
DC 480	Beam Tape	Salt Atmosphere	72	0/25
DC 480	Beam Tape	Salt Atmosphere	48	
		+		0/12
		85°C/85% RH/30V	168	
DC480	Beam Tape	250°C Life 30V	786	4/45*
Open Ceramic	Wire	85°C/85% RH/30V	1000	0/10

* At 1.1 ev, 60% Confidence Level - Failure Rate = 0.0026%/1000 hours @ 125°C

At 1.74 ev, 60% " " " " = 0.00002%/1000 hours @ 125°C

TABLE IV-4

STATUS OF LIFE-TEST SOCKETS

Type	Life Test	On-Hand	Ordered	Schedule Delivery
CA741	125°C Operating	54	135	5/20
	200°C Bias	48		
	125°C Bias	54	162	6/10
	85°C/85% RH Bias	48		
	175°C Bias		96	7/1
	150°C Bias		81	8/12
	250°C Bias		240	5/20
CD4012B	125°C Operating	54	78	7/15
	200°C Bias	48		
	125°C Bias	54	130	7/8
	85°C/85% RH Bias	48		
	175°C Bias		104	6/24
	250°C Bias		240	6/3
	150°C Bias		104	6/17
5420	125°C Operating	54	126	8/12
	200°C Bias	48		
	125°C Bias		170	8/19

A total of 1820 additional life-test sockets, to be equally divided among the CD4027B, CD4014A, 54S20, 5470, and 5472 for 125°C operating life and 125°C bias life tests has been ordered. Delivery data commitments for these sockets have not yet been obtained.

SECTION V

RCA PROPOSAL UTILIZING CONTRACT RELATED TECHNOLOGY

Presentation - Application of Beam Tape Bonded Devices to Multichip Circuits, Lockheed Missile & Space Corp, Sunnyvale, CA, April 12, 1977 - A. S. Rose.

SECTION VI

TECHNICAL PRESENTATION RELATED TO CONTRACT TECHNOLOGY

Reliability of Trimetal Plastic Integrated Circuit Packages by H. Khajezadeh and A. S. Rose.

Paper presented at International Reliability Physics Symposium, April 14, 1977 Las Vegas, Nevada.

SECTION VII
CONCLUSIONS

1. The required Phase II wafer-fabrication program is on schedule.

2. Process refinement has resulted in conversion to positive photoresist at gold interconnect plating.

3. All required life-test sockets have been ordered.

4. Reliability data to date on the CA741 have been excellent.

SECTION VIII

PROGRAM FOR THE NEXT INTERVAL

1. Continue wafer fabrication.

2. Obtain reliability data for accelerated testing and step-stress testing of the CA741 and CD4012B.

3. Initiate long term life testing.

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