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NEW MEMORY DEVICE STRUCTURES.(U)
JUL 74 G A HARTSELL

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(15) by
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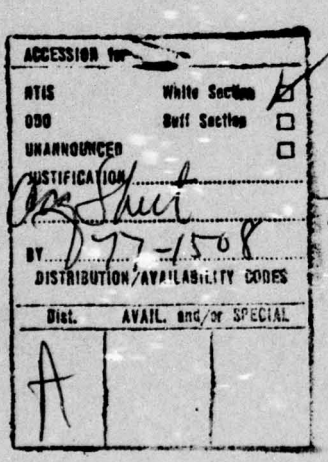

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SECTION I

INTRODUCTION

A. Program Goals

The Air Force has requirements for a radiation-hardened shift register analog memory device for applications such as data storage, data re-formatting, and signal delay. The device must have low power consumption and a wide dynamic range, but nonvolatility is not required because of the nature of the real-time system application. The objective of the program carried out under Contract No. F33615-74-C-1054 is to investigate new semiconductor analog memory structures having the potential for extreme radiation hardness. Device performance goals are (1) sample rate of 10 MHz, (2) dynamic range of 10^3, (3) maximum power dissipation of 40 microwatts per bit, (4) total dose hardness to ionizing radiation of 10^6 rad (Si), and (5) recovery within 10 milliseconds after exposure to a pulse of ionizing radiation.

B. Summary of Program Plan

Double-level metal, coplanar electrode, anodized aluminum CCD's previously developed at Texas Instruments have demonstrated the feasibility of meeting the first three of the performance goals listed above. This structure also has several potentially good features for radiation hardness. Therefore, Texas Instruments proposed a program to determine and improve the radiation hardness of double-level, anodized aluminum CCD's. Other types of CCD's will be studied as possible backups to this structure. Figures 1 and 2 show layouts of 3 ϕ, double-level metal CCD's in which the top surface of the first-level aluminum is anodized to provide interlevel insulation. Layout details and advantages of this 3 ϕ, double-level design are discussed in Appendix A. The CCD's shown in Figure 3 are 3 ϕ devices that have this structure and are of the same design as samples delivered to AFAL in May 1974.

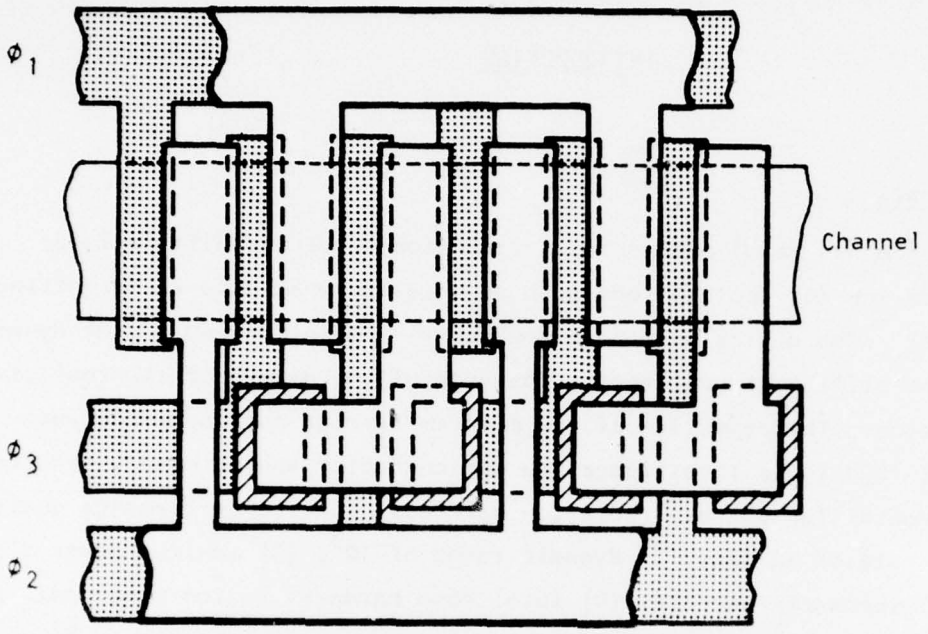


Figure 1 Double-Level, 3 ϕ CCD Layout - Parallel Section

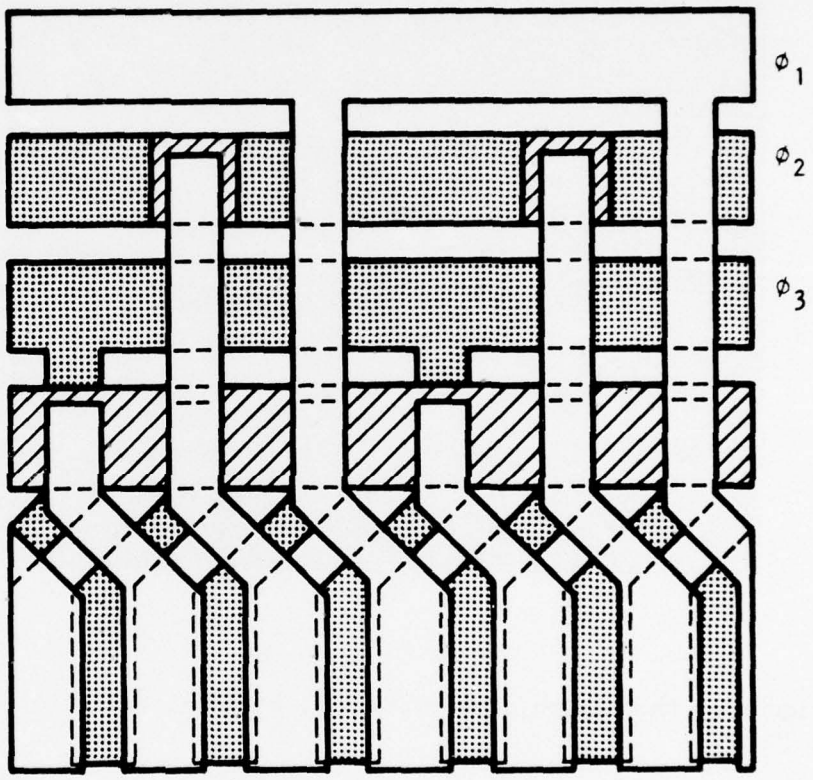


Figure 2 Double-Level, 3 ϕ CCD Layout Serial Section (All Clocks From One Side)

- top level
- bottom level
- via hole

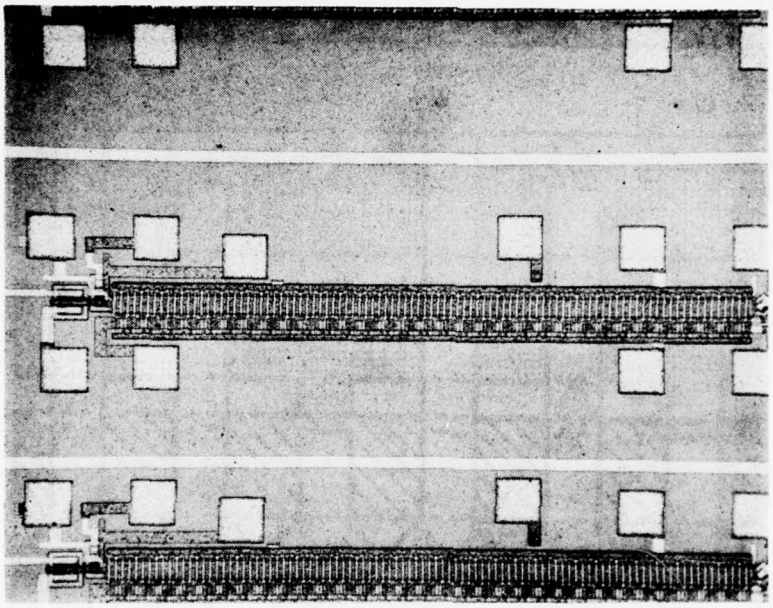


Figure 3 Photograph of 64-Bit, 3 ϕ, Double-Level Metal CCD

The basic plan for this program is to fabricate and test three groups of CCD test devices, with a period of time after each test for evaluation of results and selection and possible modification of the most promising structures before the next group of test devices is fabricated. After the final group of test devices is tested, a group of 16 K bit analog memory devices will be fabricated using the optimum structure and processes.

At the time of this report, the first group of test devices had been fabricated and tested. Most of the post-irradiation testing has been completed, and evaluation of the test results is progressing. The next three sections of this report describe the fabrication, characterization, radiation testing, and post-irradiation characterization of these devices. The remaining sections dis other program efforts and plans for the next six months.

SECTION II

FABRICATION OF TEST DEVICES

A. Description of Test Bar

Because a suitable CCD test bar design and masks were available at the start of this contract, it was possible to begin fabrication of devices for the first radiation test within one month. Finished, characterized devices were ready for testing in four months. Figure 4 is a photograph of a bar of this design. This test bar contains the following devices, which were bonded and tested for use in the first radiation test:

(1) 150-bit, 4 ϕ, double-level gate CCD serial register with precharge diffusion and source follower output detector.

(2) 150-bit, 4 ϕ, double-level gate CCD serial register with reverse bias diode output detector.

(3) MOSFET transistor.

(4) MOS gate oxide capacitor.

(5) Gated diode.

The CCD's on this design were the 4 ϕ, double-level metal, overlapping electrode type instead of the 3 ϕ design that would be used for an actual memory where high bit density is desired. However, the MOS structure and biasing are the same for both 3 ϕ and 4 ϕ so that the radiation effects should be the same for both when they are evaluated on a per-transfer basis. Previous measurements on non-irradiated devices showed comparable performance is obtained from 3 ϕ and 4 ϕ devices of the same MOS structure.

B. Processing Variations

Devices for this test came from five different process lots. Each lot was divided into two or more groups so that 15 different process combinations were

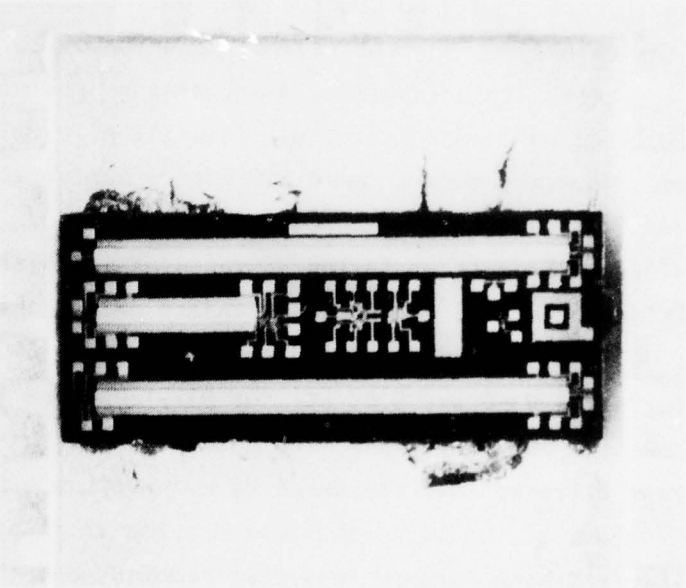


Figure 4 Photograph of CCD Test Bar

included. Table I lists the lot and slice number of slices from which the test samples came, along with the process variation that each slice represents. In all, 43 units were tested. Each had at least one of the 150-bit CCD's connected, in addition to the other test structures listed in the previous section, except the devices from lot 97, which had no CCD's connected. Because of the time required to develop the chrome doping process, only one lot of this material was completed in time for test. Unfortunately, a processing problem with this chrome-doped lot resulted in a poor interlevel insulation layer, and no good CCD's were obtained. However, chrome-doped MOS test structures were included.

The most significant process variation represented in these devices is oxide growth conditions. Lots 28 and 98 had standard oxide, that is, oxide grown in steam at 950°C. Slices 93-6 and 93-7 had oxide grown at 1100°C with HCℓ gettering (2.5% HCℓ for slice 93-6 and 5.0% HCℓ for 93-7). Slice 97-9 also had 2.5% HCℓ gettered oxide. For slice 93-4, the gate oxide was grown dry at 1100°C. In lot 97, chrome was diffused into the oxide by evaporating a 500 Å layer of chromium over the surface of the slice and then driving it in at 450°C in a nitrogen atmosphere. The remaining chromium was then removed, and the normal aluminum metallization process was used.

Another significant process variation was in the manner of forming the buried channel layer. Slices from all lots except lot 98 had phosphorus ions implanted in half the slice to form the buried channel layer. All implants were made through the gate oxide at a dose of 1.5×10^{12} per cm^2, except for slice 28-1. This slice represents an experiment in which a heavier dose was implanted into an oxide layer and then thermally diffused into the silicon in an attempt to avoid implant dislocation damage in the silicon surface. Unfortunately, the final n-type surface layer doping was so high it was not possible to deplete the buried layer completely, and normal buried channel operation could not be obtained.

TABLE I

OXIDE GROWTH CONDITIONS FOR TEST DEVICES

LOT	SLICE	OXIDE TYPE
28	1	950°C, steam
28	6	950°C, steam
93	4	1100°C, dry
93	6	1100°C, 2.5% HCℓ
93	7	1100°C, 5.0% HCℓ
97	9	1100°C, 2.5% HCℓ; chrome doped
98	6	950°C, steam
98	9	950°C, steam

Note: All slices contained both surface channel and implanted layer buried channel devices except 98-6 and 98-9, which have all epitaxial layer buried channel devices.

The surface n-type layer on slices from lot 98 was formed epitaxially on the initial substrate so that a uniform n-layer exists over the whole device surface. Consequently, all devices from this lot were buried channel type.

C. Pre-Irradiation Testing and Characterization

Before irradiation, all test samples received the normal CCD dc and functional tests, after which more detailed characterization data were taken. The following types of measurements were made:

(1) CTE of both CCD's at 1 MHz and a clock voltage of 15 volts for surface channel and 8 volts for buried channel devices.

(2) Input bias level required for a given fat zero level.

(3) Dark leakage current of the CCD at clock levels as in (1).

(4) CV and GV plots of surface channel MOS capacitors.

(5) Plots of gate capacitance versus gate voltage at various substrate biases for buried channel gated diodes.

(6) Plot of diode leakage current versus gate voltage for gated diodes.

Additional nonirradiated samples of devices from the same slices are available so that additional pre-irradiation characteristics can be examined if it becomes desirable to do so.

D. Test Samples for AFAL

Five representative nonirradiated test devices were shipped to AFAL on 7 June 1974 with a second test fixture and test and operating information. A similar test fixture was sent to AFAL with the 3 ϕ devices shipped in May 1974. Both fixtures can be used for both 3 ϕ and 4 ϕ CCD's.

SECTION III

DISCUSSION OF RADIATION TESTING

The sample devices described previously were irradiated in the North Cell of the Gamma Irradiation Facility of Sandia Laboratories in Albuquerque, New Mexico, on 13 May 1974. This is a cobalt-60 source with a present strength of about 94 kilocuries and maximum dose rate of about 0.9×10^5 rad (Si) per minute. A test fixture was made which allows separate bias condition to be applied to two groups of 10 devices wired in parallel. To simulate operating bias conditions as nearly as practical without having to supply four-phase clocks and input signals, the following bias levels were chosen:

(1) All gate electrodes in each group were connected together. Clock pulses of 50% duty cycle and 200 kHz were applied to the gates. The amplitudes were 8 volts for buried channel and 15 volts for surface channel.

(2) All diodes and transistor sources and drains were tied together to a bias of +24 volts for buried channel and +15 volts for surface channel.

(3) A substrate bias of -2 volt was used for all devices.

The 43 samples were divided into three test groups, with each process variation being represented in each group if possible. The three groups were irradiated sequentially. The position of the test fixture relative to the source was chosen to provide dose levels of approximately 10^5, 10^6, and 3×10^6 rad (Si) in reasonable times. Cobalt glass dosimetry pellets were attached to the test fixture for each test. The actual dose levels were determined by this means to be 0.79×10^5, 0.96×10^6, and 3.05×10^6 rad (Si).

SECTION IV

POST-IRRADIATION CHARACTERIZATION AND EVALUATION OF RESULTS

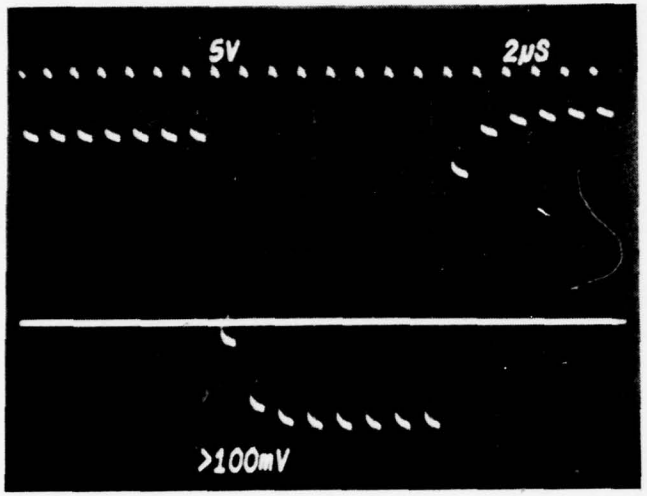
A. Present Status

The first step in the post-irradiation characterization consisted of making the same types of measurements on the test devices as those made before irradiation. These have been completed except for the GV and gated diode leakage measurements, which are presently being done. Some very significant results have been obtained thus far, as discussed below. Of course, more work must be done to explain all the observed phenomena, and additional measurements are being made on these devices.

B. Evaluation of Results

We will consider first the observed results in terms of CCD operation and then the more basic parameters such as flatband voltages. The most significant result is that buried channel, double-level anodized aluminum CCD's can survive a total gamma dose of at least 3×10^6 rad (Si) with little or no change in CTE or full well charge capacity and only moderate increases in dark current. It is emphasized that this is true in spite of the fact that very large flatband voltage shifts and surface state density increases were observed on surface channel devices from the same slices. This shows that the operation of these buried channel devices is relatively insensitive to the oxide charge buildup and surface state density increases that have caused the low radiation tolerance of most previous MOS devices. This, in turn, implies that hardened CCD memory and imager devices can be manufactured using conventional oxide processes.

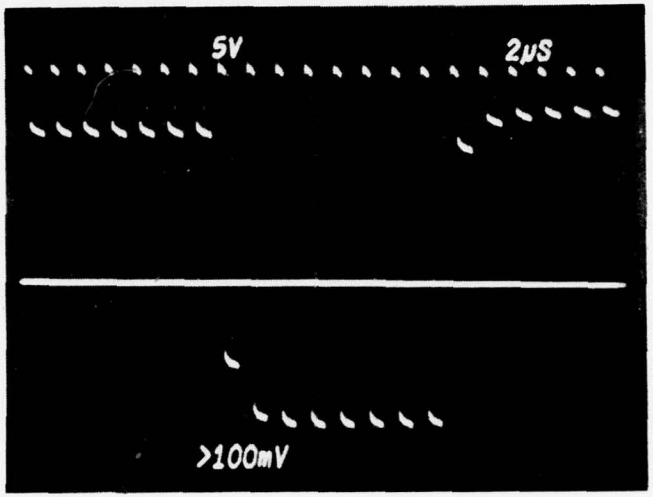
Output waveforms of a typical buried channel device before and after irradiation to a level of 3.0×10^6 rad (Si) are shown in Figure 5 along with values for dark leakage current and input bias levels. Equally good results were observed for the devices irradiated at the lower levels. Also, no significant difference



Before Irradiation

I_L = 0.65 nA

V_{in} = 14.0 volts



After Irradiation

I_L = 4.8 nA

V_{in} = 17.5 volts

Figure 5 Output Waveforms of Buried Channel CCD Test Unit 93-6-10 Before and After Irradiation under Bias with a Dose of 3×10^6 rad (Si)

in hardness was found between implanted buried layer devices and epitaxial buried layer devices. It can be seen that the input level required for a given output increased by about 4.0 volts for the input technique used for these measurements, which is dependent on the MOS gate threshold voltage. A similar change in threshold voltage was also seen in the gated diode characteristics; however, by using the technique described in Appendix B, it is possible to introduce the signal charge into the CCD in a manner independent of the gate threshold voltage for moderate threshold variations.

Although the normal tests for CTE evaluation use pulsed inputs signals, these devices are basically linear analog devices, as shown by Figure 6.

The radiation hardness of the surface channel CCD's is much lower, as indicated by the pre- and post-irradiation output waveforms of a typical surface channel CCD that received a total dose of 0.8×10^5 rad (Si) (Figure 7). A flatband voltage shift of 13.6 volts was measured for this device. However, the nonsymmetrical shape of the output pulse indicates that the main cause of the CTE degradation is a large increase in surface state density. This is also indicated by the fact that a large fat zero is required before a small pulse can be transmitted through the device at all. Initial G-V measurements on some of the devices that received 10^6 rad show an increase in surface state density by a factor of 2000 to 3000 X. The performance of the surface channel devices irradiated to 10^6 and 3×10^6 rad (Si) was degraded even more than that shown in Figure 7. The observed changes in flatband voltage for the different types of oxide shown in Table II generally match previously reported results. That is, the HCℓ oxides had larger shifts than the steam and dry oxides. However, in these tests, the 1100° dry oxide was no better than the 950° steam oxide. No definite conclusions have been reached to date on the hardness of the chrome-doped oxide because the chrome doping was inadvertently implemented on slices that had HCℓ gettered oxide. The surface channel MOS capacitors from this material showed large flatband shifts, but this may be due to the effects of the HCℓ gettering.

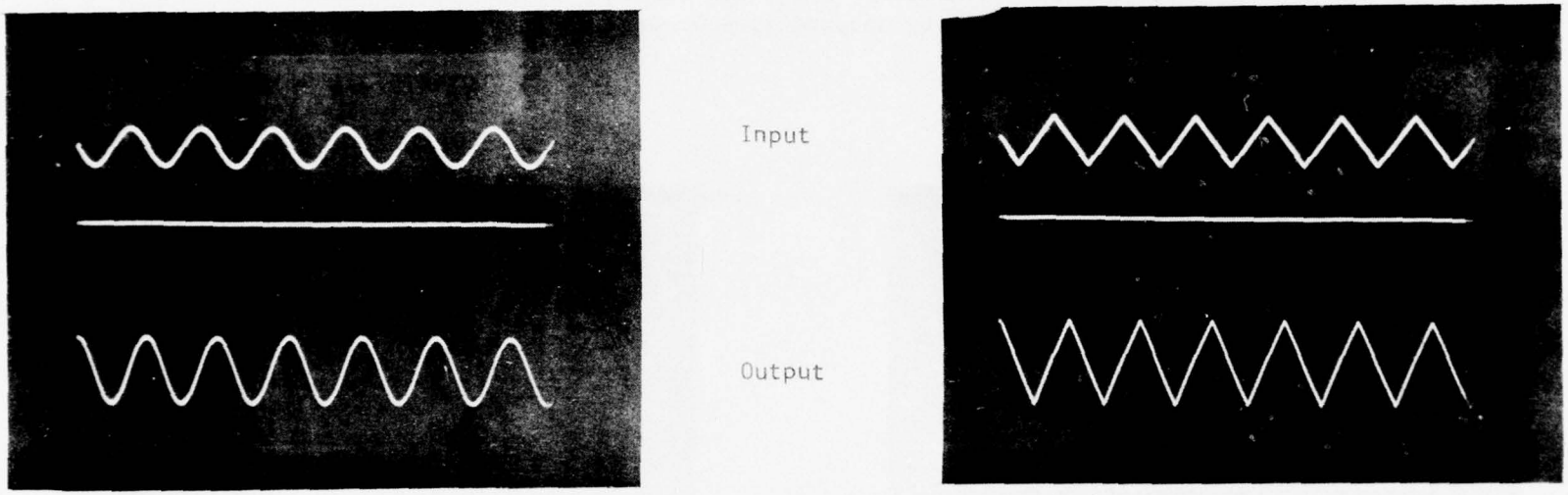
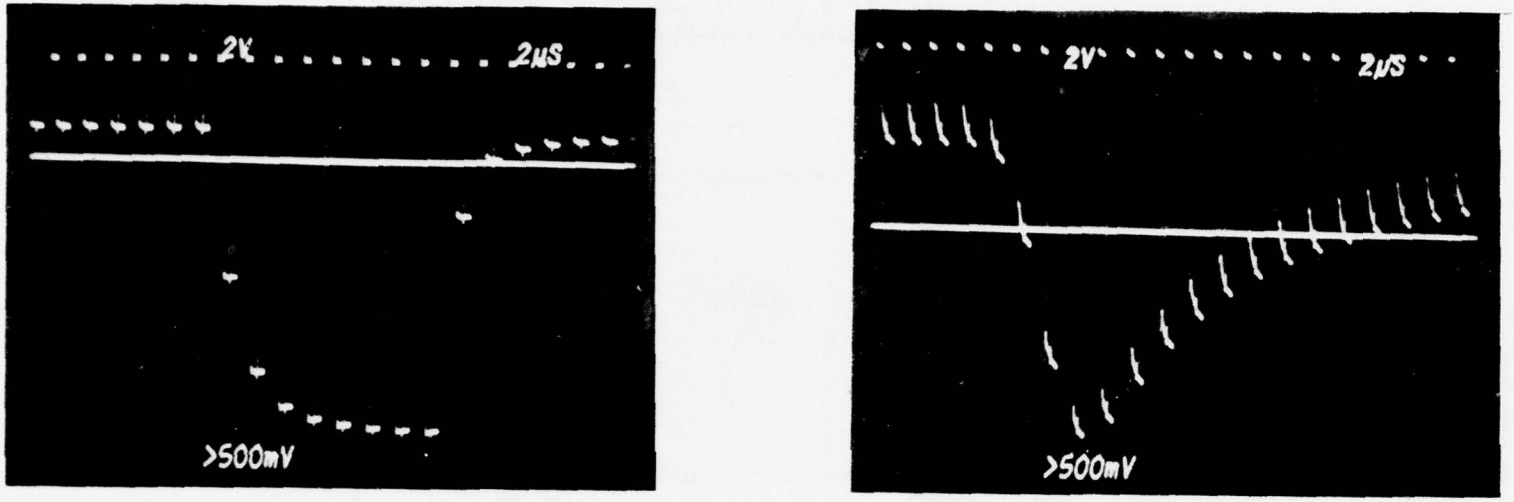


Figure 6 Input and Output Waveforms of Buried Channel CCD Irradiated with 3×10^6 rad (Si), Demonstrating Linear Operation



Before Irradiation

After Irradiation

Figure 7 Output Waveforms of Surface Channel CCD Test Unit 93-6-3 Before and After Irradiation Under Bias with a Dose of 0.79×10^5 rad (Si)

TABLE II

FLATBAND VOLTAGE SHIFTS FOR SURFACE CHANNEL MOS CAPACITORS

Dose Level	Slice Number				
	28-6	93-4	93-6	93-7	97-9
0.79×10^5 rad (Si)	3.3	3.8	11.5	13.6	--
0.96×10^6 rad (Si)	11.6	13.0	> 65	48	62
3.05×10^6 rad (Si)	--*	12.3	26	--	53

*No data for this combination.

The dark leakage currents of the devices in this test were higher than those of more recently processed CCD's. Significant process developments made in the last four to five months provide devices with reduced dark leakage currents. However, the CCD's included in this test were processed without these improvements and had leakage currents that typically were 100 to 200 nA/cm^2. Though there were wide variations, the CCD leakage current changes were approximately the same for both surface and buried channel devices and for all three dose levels. Typical changes were increases of from two to eight times. Further testing must be done to determine if the increased leakage is occurring in the CCD itself, in the output detector circuit, or both.

SECTION V

DESIGN OF AN ON-CHIP LOW NOISE OUTPUT CIRCUIT

We have completed the design and layout of an output circuit that implements the double-sampling technique of precharge noise reduction described by White,* et al., and that is compatible with the fabrication processes for the ion-implanted, buried channel, double-level metal CCD described earlier in this report. This circuit is being fabricated first as a test circuit on a CCD for another program at TI. Its operation should be verified in time for inclusion on the first mask designed under this contract. The operation of this circuit is described in the remainder of this section.

- Operation of Double Sampling Output Circuit

A schematic of the double sampling output circuit is shown in Figure 8. This circuit is designed to reduce the magnitude of "kTC" noise introduced at the output of the CCD, that is, noise resulting from the uncertainty in the voltage level to which the output diode of the CCD may be precharged prior to the arrival of a signal charge packet. The circuit function is based on the common television circuitry concept of dc restoration, whereby an ac-coupled signal is periodically "restored," or clamped, to a dc reference voltage. The clamping operation consists of charging the coupling capacitor to a voltage which is the difference between the dc reference voltage and the input voltage applied to the capacitor. The noise introduced by the dc restoration process is just the uncertainty in the voltage to which a capacitance C may be preset, namely, $\sqrt{kT/C}$.

The use of dc restoration to reduce output noise in a CCD depends on performing the clamping operation in synchronization with the pulse sequence used to precharge the output diode of the CCD. Referring to Figure 8, MOSFET Q_1 is pulsed on momentarily, presetting the CCD output diode to $V_{REF} + \Delta V_1$, where ΔV_1 is the deviation of the voltage from V_{REF} resulting from kTC noise on the

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* M. H. White, D. R. Lampe, F. C. Blaha, and I. A. Mack, "Characterization of Surface Channel CCD Image Arrays at Low Light Levels," IEEE J. Solid State Circuits SC-9, 1 (1974).

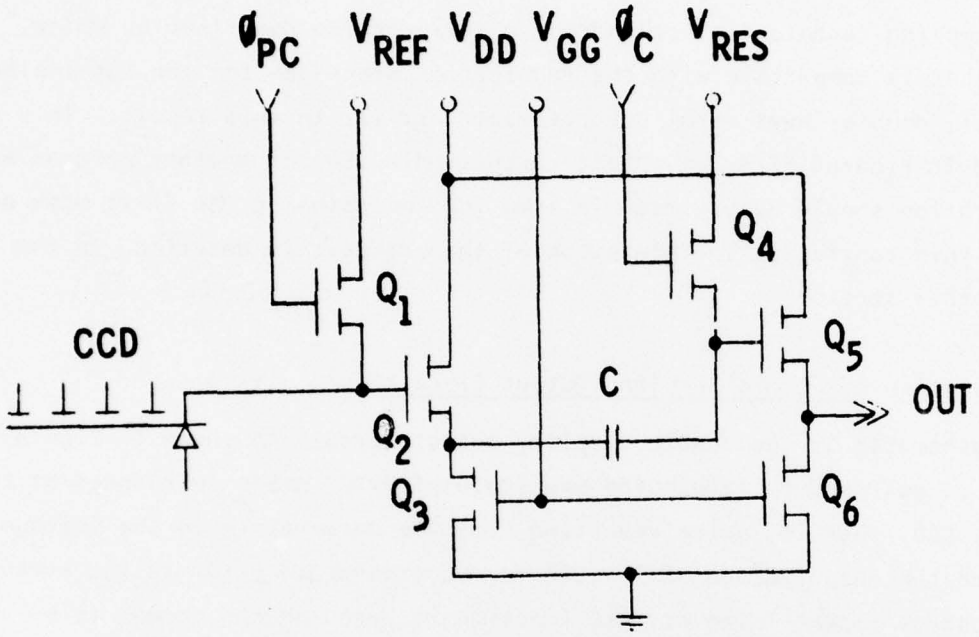

Figure 8 Schematic Diagram of Double Sampling Output Circuit

precharge operation. Q_2 acts as a source-follower, with Q_3 its load device. Once Q_1 has returned to its off state, the clamp gate Q_4 is pulsed on momentarily, charging the coupling capacitor C to a voltage V_C. If we assume for simplicity that the threshold voltage of Q_2 is zero and that the Q_2-Q_3 source-follower has unity gain, then V_C will be given by

$$V_C = V_{REF} + \Delta V_1 - V_{RES} - \Delta V_2,$$

where ΔV_2 is the deviation of the voltage on the gate of Q_5 resulting from kTC noise on the operation of charging capacitor C. MOSFET Q_5 functions as a source-follower with load device Q_6. If its threshold voltage is assumed to be zero and the gain of the combination is assumed to be unity, the output voltage after clamping will be $V_{RES} + \Delta V_2$, independent of ΔV_1.

If now the CCD is clocked to dump the next signal charge packet onto the output diode, the voltage on the gate (and source) of Q_2 will change by a voltage ΔV_S proportional to the magnitude of the charge in the packet. As Q_4 is now off, the voltage across C must remain at V_C, so the gate (and source) of Q_5 also change by ΔV_S. The final output voltage is thus $V_{RES} + \Delta V_2 + \Delta V_S$, independent of ΔV_1. The noise on the output signal is the rms fluctuation in ΔV_2, namely, $\sqrt{kT/C}$. The noise introduced by the output diode precharge operation is the rms fluctuation in ΔV_1, namely $\sqrt{kT/C_o}$, where C_o is the parasitic capacitance of the output diode node. This component of noise is completely removed by the clamp circuit, so the noise voltage is reduced by the factor $\sqrt{C_o/C}$.

In the actual implementation of the circuit on the CCD chip, C_o is approximately 0.25 pF and C is approximately 25 pF, resulting in a noise voltage reduction by a factor of 10. In terms of absolute noise voltage, the rms kTC noise voltage on a 25 pF capacitor is approximately 13 μV. In terms of effective rms number of noise electrons at the output of the CCD, the noise resulting from the clamping procedure is approximately 20 electrons.

SECTION VI

PLANS

Plans for the next six months of contract effort include:

(1) Further evaluation of devices from the first radiation test.

(2) Further development of chrome doping process.

(3) Fabrication of test samples for the second radiation test.

(4) Design and fabrication of test fixtures and circuits for gamma pulse recovery testing.

(5) Investigation of dark current increases and noise.

Specific items from the results of the first test that need further evaluation include surface state density, causes of leakage current increases, and noise levels. Some low temperature ($\leq 350°C$) annealing experiments on selected devices may also be useful. Chrome doping by ion implantation and thermal diffusion will be evaluated, as will thermally deposited metal. There may be somewhat less emphasis than originally expected on oxide hardening techniques, since buried channel CCD's are relatively insensitive to surface charge and surface state density increases. However, dark leakage current and the noise it produces are more important in buried channel devices because of the smaller charge capacity than that of surface channel CCD's.

SECTION VII

CONCLUSIONS

Buried channel, double-level anodized aluminum CCD's with ordinary oxide processing have been found to withstand total doses of ionizing radiation of at least 3×10^6 rad (Si) without significant changes in CTE or full well capacity and with only moderate increases in dark leakage current. This exceeds the program goals for total dose hardness by a factor of three. However, surface channel CCD's were found to have greatly degraded CTE at dose levels of 0.8×10^5 rad (Si). HCℓ gettered oxides had significantly worse flatband voltage shifts than either steam or dry oxides, both of which showed about the same shifts. The tests of chrome doping of the oxide were inconclusive due to its inadvertent combination with HCℓ gettering.

APPENDIX A

DESCRIPTION OF 3ϕ, DOUBLE-LEVEL METAL CCD's WITH COPLANAR ALUMINUM ELECTRODES

APPENDIX A

DESCRIPTION OF 3ϕ, DOUBLE-LEVEL METAL CCD's WITH COPLANAR ALUMINUM ELECTRODES

Texas Instruments has developed and fabricated CCD's using the Aℓ-$Aℓ_2O_3$-Aℓ double-level metalization system with only three electrodes per bit. This three electrodes per bit technique in a double-level metalization structure has significant advantages over four electrodes per bit systems in both area per bit and number of transfers required.

Double-level metal CCD's have generally been constructed either as 4 ϕ, or as 2 ϕ with two electrodes per phase, because the even symmetry of the structure suggests a clocking scheme with an even number of clocks per bit. However, either of the above-mentioned schemes has four gates per bit and inherently requires more area per bit than a 3 ϕ clocked system. A double-level layout scheme has been developed at TI that permits 3 ϕ clocking and three gates per bit without requiring an excessive number of interlevel connections. Figure A-1 shows the layout of a 3 ϕ, double-level, anodized aluminum CCD register where clock electrodes are bussed together on both sides of the register. This is typical in the case of a single linear register or several adjacent parallel registers. It can be seen that the clock electrodes for a given phase are on alternate levels in adjacent bits. This is a consequence of having an odd number of clock phases and an even number of metal levels. Note that the ϕ_1 clock electrodes in odd-numbered bits are all on first level and are interconnected by a first level ϕ_1 bus. The ϕ_1 electrodes in even-numbered bits are all on second level and are interconnected by a second level ϕ_1 bus which runs directly on top of the first level ϕ_1 bus. The first level ϕ_1 bus may be left unanodized so that the two buses are connected all along their length; otherwise, they may be interconnected at one or both ends of the register. The ϕ_2 electrodes are connected in the same way on the other side of the register. However, the ϕ_3 electrodes are trapped in by the double-level ϕ_1 and ϕ_2 buses and can be connected only by going alternately over and under the ϕ_2 (or ϕ_1) electrodes.

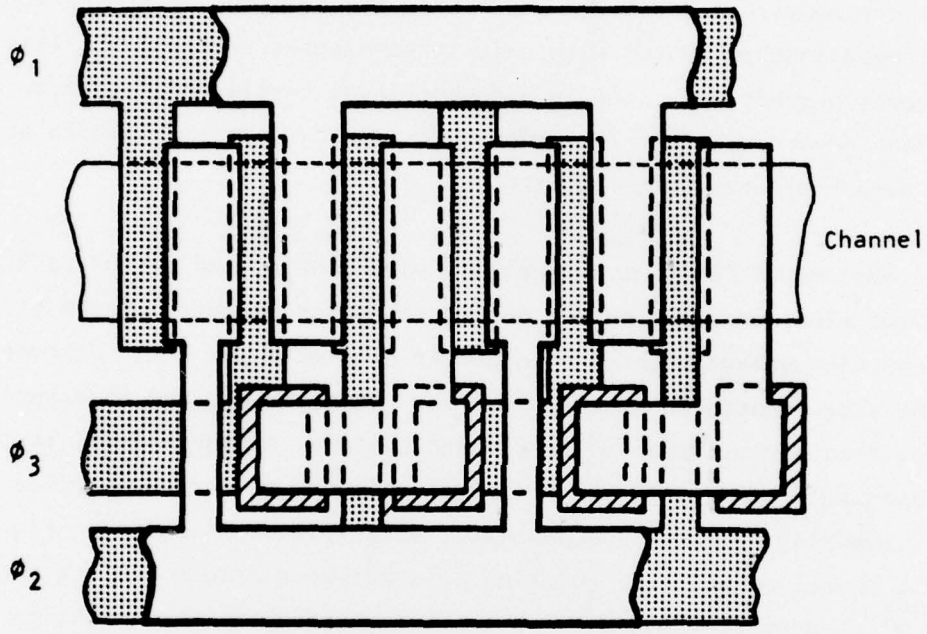

Figure A-1 Double-Level, 3 ϕ CCD Layout - Parallel Section

This scheme requires only one interlevel interconnection per bit in a single register, or one per row of bits in an array of several parallel registers.

The layout of a serial register having all clock buses on the same side is shown in Figure A-2. This is the typical case for a serial CCD register used as a multiplexer or demultiplexer, as in the input and output registers of a serial-parallel-serial (SPS) area array. In this case, electrodes of the same clock phase in adjacent bits are first connected together, and then a single lead is used to connect each pair of electrodes to the clock bus. This arrangement requires four interlevel contacts for each pair of bits for an average of two per bit. This is one less interlevel contact per bit than is required for a 4 ϕ, double-level register of the same type.

The use of 3 ϕ phase clocking instead of 4 ϕ phase reduces the area per bit by 25% for serial arrays and by 44% for SPS area arrays. It also reduces the number of transfers per bit from four to three. Thus, if register length is limited by CTE, 3 ϕ clocking allows serial registers to be 33% longer and SPS registers to be 78% longer than is possible for 4 ϕ systems. The reduced number of transfers per bit is especially important for analog memory applications, since the signal dispersion due to imperfect transfer cannot be simply removed by use of a threshold detector-regenerator, as in a digital system.

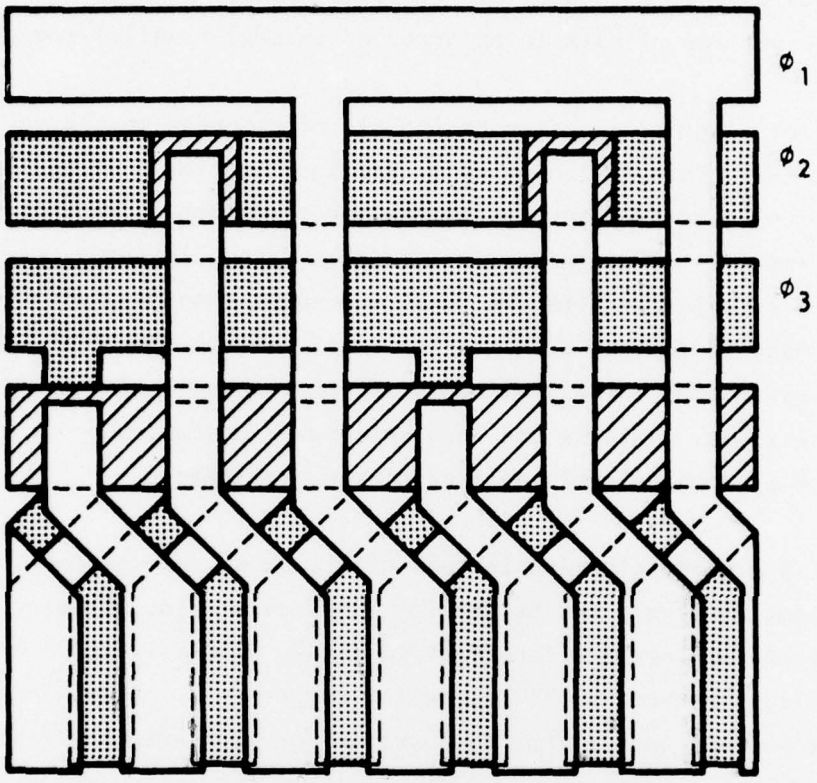

Figure A-2 Double-Level, 3 ϕ CCD Layout Serial Section (All Clocks From One Side)

- top level
- bottom level
- via hole

APPENDIX B

METHOD OF INTRODUCING A SIGNAL INTO A CCD INDEPENDENTLY OF GATE THRESHOLD VARIATIONS

APPENDIX B

METHOD OF INTRODUCING A SIGNAL INTO A CCD INDEPENDENTLY OF GATE THRESHOLD VARIATIONS

The signal introduction technique illustrated by Figure B-1 has been described by Emmons and Buss,* who were particularly interested in its low noise advantages. However, it will be shown that it also has the advantage of making the signal introduction independent of the gate threshold level and therefore may be useful in applications in which the gate threshold voltage may change due to the effects of ionizing radiation.

To understand the operation of this method, consider the potential diagrams of Figure B-1. If the signal voltage is applied to the input gate and the input diode is pulsed on while ϕ_1 is on, the ϕ_1 well will be filled. If the diode is then pulsed off (before ϕ_2 comes on), the charge remaining in the ϕ_1 well will be determined by the difference in the potentials under the input gate and ϕ_1. So long as changes in the gate threshold affect the potential under both equally, the difference in potential, and hence the charge in the ϕ_1 well, are not affected by such changes.

* "The Performance of CCD's in Signal Processing at Low Signal Levels," S. P. Emmons and D. D. Buss, CCD Applications Conf., San Diego, California, Sept. 18-20, 1973.

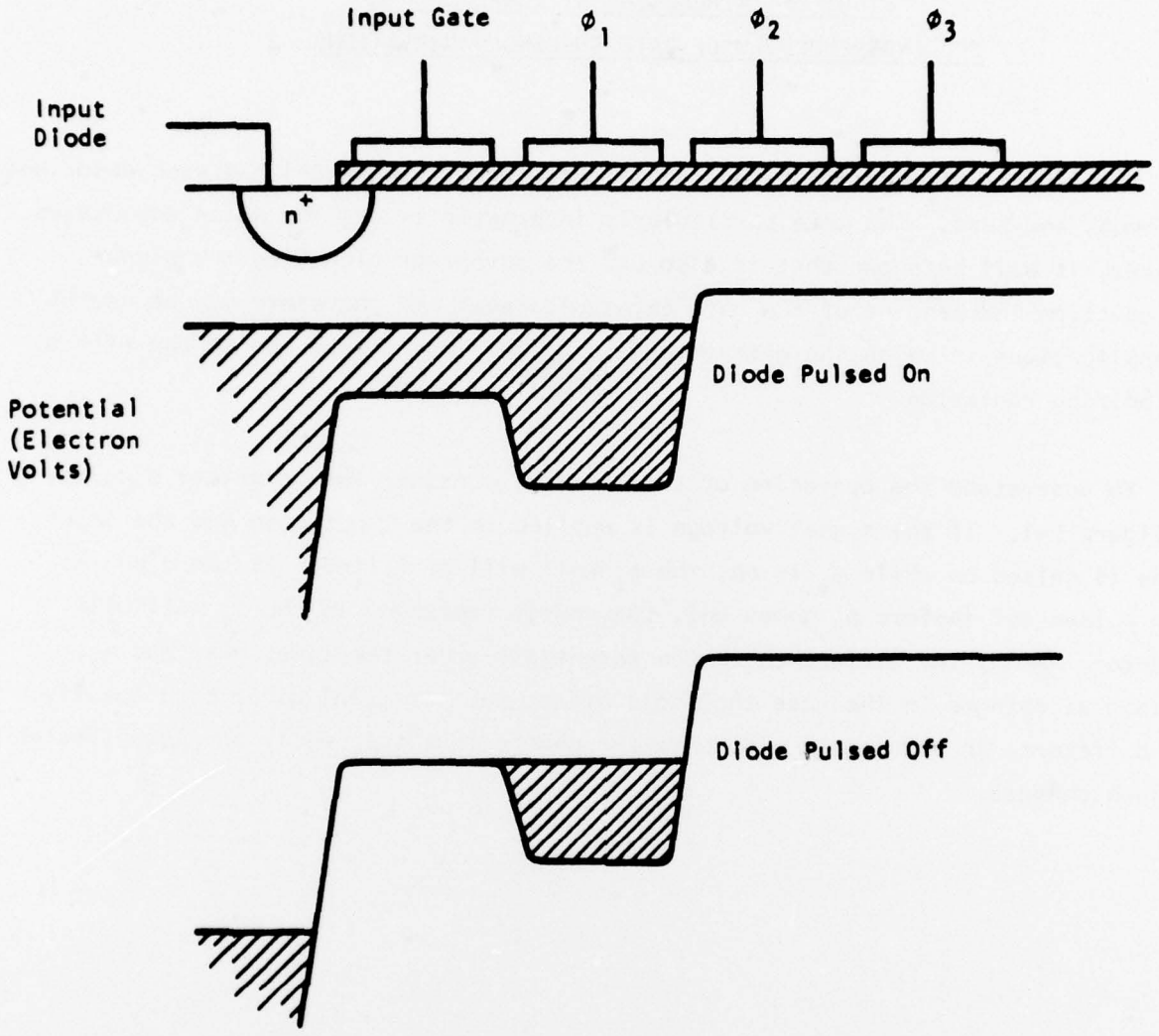

Figure B-1 Diagrams Illustrating Technique for Introducing a Signal into a CCD Independently of the Gate Threshold Voltage

APPENDIX C

SUMMARY OF THE STATUS OF RIDGE-GUIDED ACOUSTIC SURFACE WAVE DEVICE DEVELOPMENT

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SUMMARY OF THE STATUS OF RIDGE-GUIDED ACOUSTIC SURFACE WAVE DEVICE DEVELOPMENT

Work under Texas Instruments sponsorship in the areas of acoustic waveguide fabrication and analysis has continued at a moderate level. Various techniques for waveguide formation have been examined, and it is believed that usable procedures have been found.

We have added to our analytic capabilities a comprehensive finite-element computer program. This program is capable of analyzing the propagation of modes in waveguides of completely arbitrary cross section and general anisotropy and piezoelectricity.

These two capabilities bring the acoustic ridge waveguide technology at Texas Instruments to a level where the pursuit of an acoustic memory program should be seriously considered.