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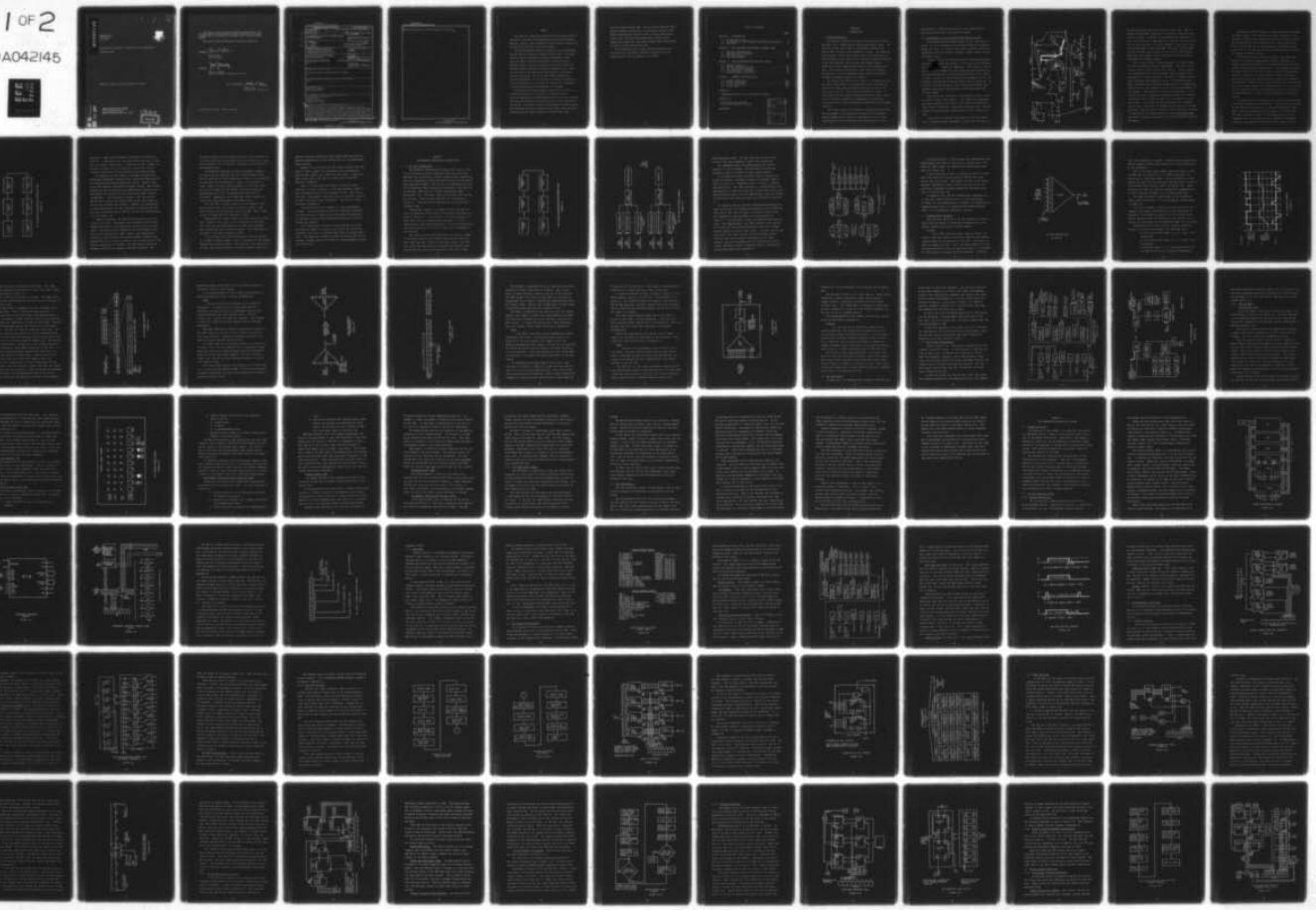

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PHASE REPORT
June 1977

MICROPROCESSOR UTILIZATION IN COMMUNICATIONS SYSTEM MONITORING

Clarkson College

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This report illustrates how a microprocessor may be used to monitor the operating performance of the Frankfurt-Koenigstuhl-Vaihingen (FKV) area of the European Defense Communications System (EDCS). Specifically described are the interfaces and software routines necessary to carry out the monitoring function and the advantages and limitations of the proposed microprocessor system. Background information is also given which describes various monitoring methods previously suggested for EDCS. Also described are the various communications devices which are deployed in the FKV area and a non-microprocessor-controlled

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monitoring system which is currently proposed for that area.

PREFACE

This effort was conducted by Clarkson College of Technology under the sponsorship of the Rome Air Development Center Post-Doctoral Program for RADC/DCLD. Charles N. Meyer of RADC/DCLD was the task project engineer and provided overall technical direction and guidance.

The RADC Post-Doctoral Program is a cooperative venture between RADC and some sixty-five universities eligible to participate in the program. Syracuse University (Department of Electrical Engineering), Purdue University (School of Electrical Engineering), Georgia Institute of Technology (School of Electrical Engineering), and State University of New York at Buffalo (Department of Electrical Engineering) act as prime contractor schools with other schools participating via sub-contracts with the prime schools. The U.S. Air Force Academy (Department of Electrical Engineering), Air Force Institute of Technology (Department of Electrical Engineering), and the Naval Post Graduate School (Department of Electrical Engineering) also participate in the program.

The Post-Doctoral Program provides an opportunity for faculty at participating universities to spend up to one year full time on exploratory development and problem-solving efforts with the post-doctorals splitting their time between the customer location and their educational institutions. The program is totally customer-funded with current projects being undertaken for Rome Air Development Center (RADC), Space and Missile Systems Organization (SAMSO), Aeronautical Systems Division (ASD),

Electronics Systems Division (ESD), Air Force Avionics Laboratory (AFAL), Foreign Technology Division (FTD), Air Force Weapons Laboratory (AFWL), Armament Development and Test Center (ADTC), Air Force Communications Service (AFCS), Aerospace Defense Command (ADC), HQ USAF, Defense Communications Agency (DCA), Navy, Army, Aerospace Medical Division(AMD), and Federal Aviation Administration (FAA).

Further information about the RADC Post-Doctoral Program can be obtained from Mr. Jacob Scherer, *RADC/RBC, Griffiss AFB, NY, 13441,* telephone Autovon 587-2543, Commercial (315) 330-2543.

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CHAPTER 1

INTRODUCTION

1.1 Problem Definition

This report examines the problem of incorporating a microprocessor into a communications network monitoring system. The specific network under study is the Defense Communications System (DCS) located on the continent of Europe. The proposed microprocessor system would perform some of the functions currently planned in the digital ATEC (Automated Technical Control) system which monitors various alarm and voltage signals emanating from the communications devices of the defense network. Specifically investigated is the task of utilizing a microprocessor to scan equipment alarms, measure selected DC voltages and monitor certain TTL signals.

The overall objective of this effort is to demonstrate the process of interfacing a microprocessor to the system and to indicate the long range advantages which may be realized by using such a device. Some of these advantages include: a distribution of the monitoring system processing load, a reduction of telemetry bandwidth, an enhancement of monitoring system flexibility and an expansion of monitoring system sophistication.

This report consists of background information describing the development of the monitoring concept for the European Defense Communications System, a description of the present communications system into which the microprocessor is to be

incorporated, a detailed description of the proposed microprocessor system, and a conclusion and summary.

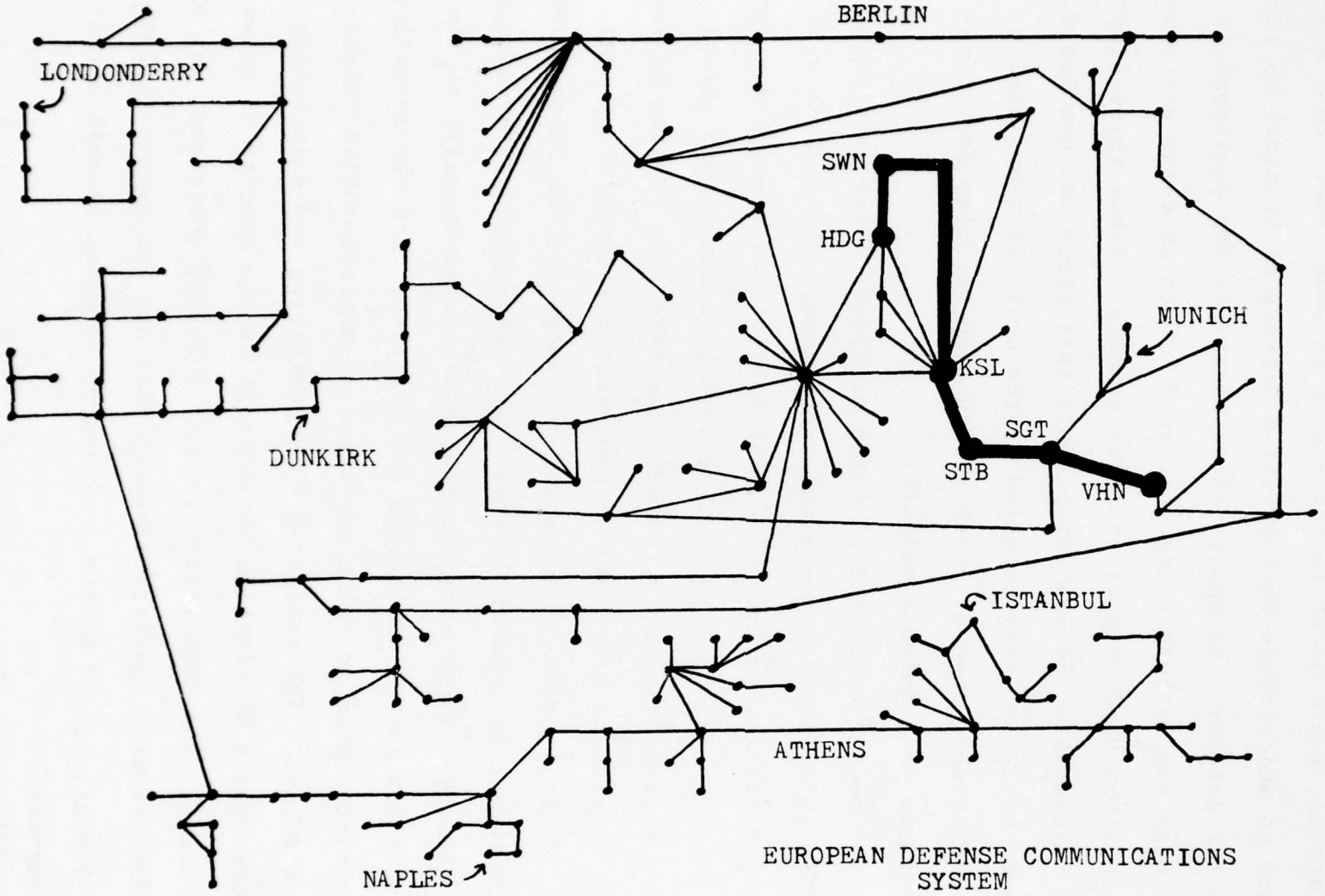
1.2 Development of the European DCS Monitoring Concept

The European Defense Communications System, illustrated in Figure 1-1, is an extremely large network consisting of approximately 225 sites. It connects such widely separated cities as: Londonderry, Northern Ireland; Istanbul, Turkey; Athens, Greece; and Naples, Italy.

A network of such size gives rise to a significant problem of network monitoring and control. In the case of the European DCS, however, the problem is compounded. The reason for this is that the network, rather than being designed and constructed as a system, has evolved in a piece-by-piece fashion over a number of years. During its initial period of development and use, the problem of network monitoring and control was not addressed. As a result, with the passage of time, significant problems arose regarding maintenance coordination, circuit degradation and circuit outages.

One flaw in the system was its maintenance concept, which was that of repair after failure. This meant that maintenance operations commenced only after a user, who was dissatisfied with service, complained. Conditions prompting such a complaint usually involved extreme degradation of or total failure of a line.

There were two problems associated with this philosophy. First, assuming fallible equipment, it meant that failures, by



EUROPEAN DEFENSE COMMUNICATIONS SYSTEM

FIGURE 1-1

definition, would occur in the system at some time. This was deemed an undesirable feature for a network as critical as one used for defense. Secondly, it was possible for equipment to fail with the failure going unnoticed. Such an event was possible in lines used only at critical moments. Since these lines were seldom used, it was conceivable that their failure would, on some occasion, only be noted at the critical times during which they were needed. Such a situation was also deemed unacceptable in a defense network.

Due to the existence of these problems, a research effort to find an alternate system was undertaken. The goal of this research effort, called SYPAC, was to devise a network monitoring scheme which would detect network problems before severe degradation or failure occurred. The SYPAC [1] (System Performance Assessment and Control) program, in accomplishing that goal, identified those operating parameters of the European DCS which served as good indicators of the operating performance of the network. These parameters were monitored manually at the various DCS sites, collected, and analyzed, with the resulting information used to guide personnel in a preventative maintenance effort. The result of this monitoring and maintenance process was a distinctive improvement in the quality of network operation. The significant result of SYPAC, therefore, was that it demonstrated the effectiveness of a new fix-before-failure philosophy, guided by the analysis of selected network operating parameters.

Following the SYPAC program, an effort was made to automate the SYPAC scheme. This involved three basic operations: the automatic collection of parameters previously selected by SYPAC, the transmission of those parameters to a central processing point, and the analysis of such parameter information at that central site. The name given to the automation effort was ATEC or Automated Technical Control.

The ATEC system was designed to monitor the operational quality of an analog communications network. Therefore, as digital technology developed and a trend toward digital communications emerged, another problem arose. This problem concerned the applicability of the ATEC system to digital communications systems. The ATEC system was designed to monitor parameters which indicated the performance quality of an analog communications network. However, this set of parameters was not appropriate for a similar analysis of a digital system. As a result, as digital communications became established in parts of the DCS, it became necessary to adapt the ATEC equipment to the digital system.

The program which investigated this general problem was the ATEC Digital Adaptation Study [2]-[4]. This study was an effort to determine the applicability of already-designed ATEC equipment to digital communications monitoring. In this program, those new parameters thought to be appropriate for digital communications system monitoring were selected, and changes, deletions, and additions to the former ATEC system, for the

purpose of upgrading the system for digital monitoring, were proposed.

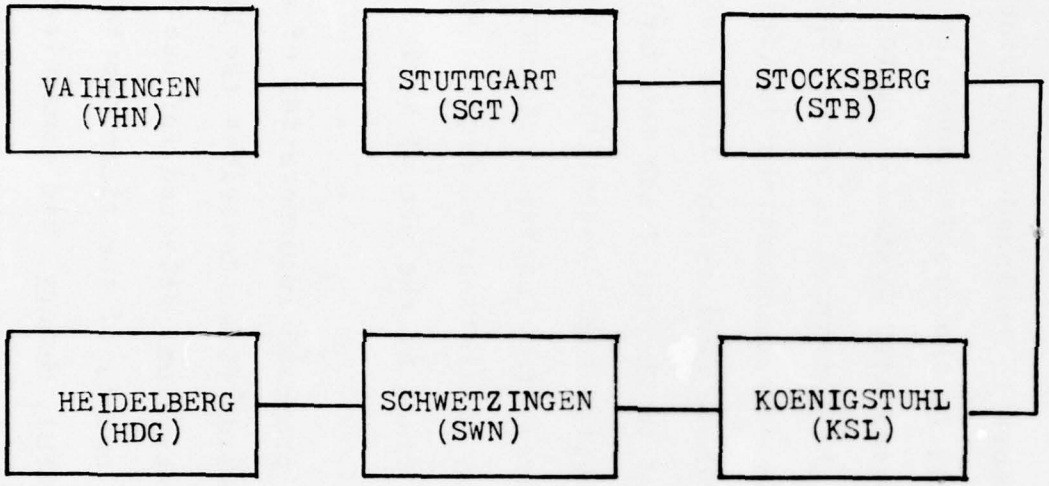
The Digital ATEC Adaptation Study addressed a particular part of the European DCS known as the Frankfurt, Koenigstuhl, Vaihingen (FKV) area which is illustrated in Figure 1-2. The FKV area had been previously upgraded to a digital communications network and was therefore judged to be suitable for the ATEC adaptation program.

The digital ATEC system configuration, as proposed in ATEC Digital Adaptation Study documentation, consists of a main monitoring node (Nodal Control Site) supplemented by five subordinate nodes (Remote Sites). The ATEC devices located at the subordinate nodes measure various network operating parameters and telemeter this information to the main node for analysis; thus, the system is highly centralized with nearly all processing done at the nodal control site and very little processing done at the remote sites.

1.3 Overview

The purpose of this report is to investigate the incorporation of a microprocessor into the digital ATEC system. Specifically discussed is the problem of interfacing between the microprocessor and those digital network parameters which must be monitored in order to determine the operating performance of the digital communication network.

The fact that remote sites lack a local processing device makes the prospect of having a microprocessor at these sites



THE FRANKFURT-KOENIGSTUHL-VAIHINGEN AREA

FIGURE 1-2

attractive. Some possible benefits of remote site processing would be: a reduction in the main node processing load; a reduction in telemetry requirements; a reduction in ATEC hardware, resulting in reduced size, cost and power requirements; and an increase in monitoring system flexibility and sophistication.

The remainder of this report is intended to provide more background information relating to the problem and then describe the proposed microprocessor-based ATEC system. Chapter 2 discusses the Frankfurt-Koenigstuhl-Vaihingen network. Specifically examined are the various types of communications devices used in the network, the function of those devices and their relative configuration. Also discussed in Chapter 2 are the various devices which comprise the digital ATEC system, their function and the ways in which they interact. Chapter 2 is concluded by a section which points out the limitations of digital ATEC and how those limitations may be eased by the use of a microprocessor at an FKV remote site.

Chapter 3 discusses the proposed incorporation of a microprocessor into ATEC. The chapter first describes the Motorola MC6800 microcomputer system which was selected for use in this report. Discussed are the elements of the microcomputer which include the microprocessor (MPU), memory, and communication interfaces, with particular descriptive emphasis placed on the Motorola Peripheral Interface Adapter (PIA) through which all FKV monitor signals pass to the MPU. Also described in the microcomputer section is the computer interrupt structure. The

interrupt structure plays an important role in the execution of a function which must be performed at precise intervals of time and is necessary to call the MPU's attention to the arrival of asynchronous pulses.

Following the discussion of the microcomputer, Chapter 3 then describes the different FKV alarms and parameters which must be monitored by the microprocessor system. It is shown that all pertinent FKV alarm/parameter signals are available as either contact closures, analog voltages, or TTL levels, and that the TTL signals may be further classified as Slow TTL, Medium Speed TTL or Fast TTL depending on their rate of occurrence. Depending on the signal type, these signals are interfaced to the microcomputer in different ways.

Fast TTL (FTTL) signals, which are to be counted in the digital ATEC system, are counted in external counters, and these counters are periodically read by the MPU. This is done on what is called the FTTL Interface or FTTLI.

Medium Speed TTL (MTTL) signals are also counted in digital ATEC. However, since their rate of occurrence is less than FTTL, they are read individually by the MPU on an interrupt basis without the use of external counters. This operation is performed via the MTTL Interface or MTTLI.

It is necessary that the microprocessor read the voltage of a number of analog signals. This is performed via the Analog Voltage Scan Interface (AVSI). The function of the interface is to scan, under program control, 32 analog voltages, perform an

analog to digital conversion of the voltage value and send the digital representation of the voltage value to a microprocessor input register.

Chapter 3 also describes how FKV contact closures (CC) and Slow TTL (STTL) signals are interfaced to the microcomputer. These CC/STTL signals are latched (in some cases), scanned and their status sent to the MPU via Contact Closure/Slow TTL Interface (CC/STTLI).

Since it is necessary for the MPU to perform various functions at precise intervals, a Time Base Generator (TBG) is also incorporated into the microcomputer system. This device, which has a programmable time base, sends an interrupt signal to the MPU at the end of each time period. This device is also discussed in Chapter 3.

Described at the end of Chapter 3 is the microcomputer software. The main programs and various interrupt subroutines are listed and their functions and interaction are explained. In addition, various timing considerations and worst case conditions are examined.

It is the overall function of the microprocessor system described in Chapter 3 to monitor the various FKV alarms and parameters and store the alarm/parameter data in a memory data list. This makes the information readily accessible for use by software packages which may be added to the microcomputer system at a later date.

CHAPTER 2

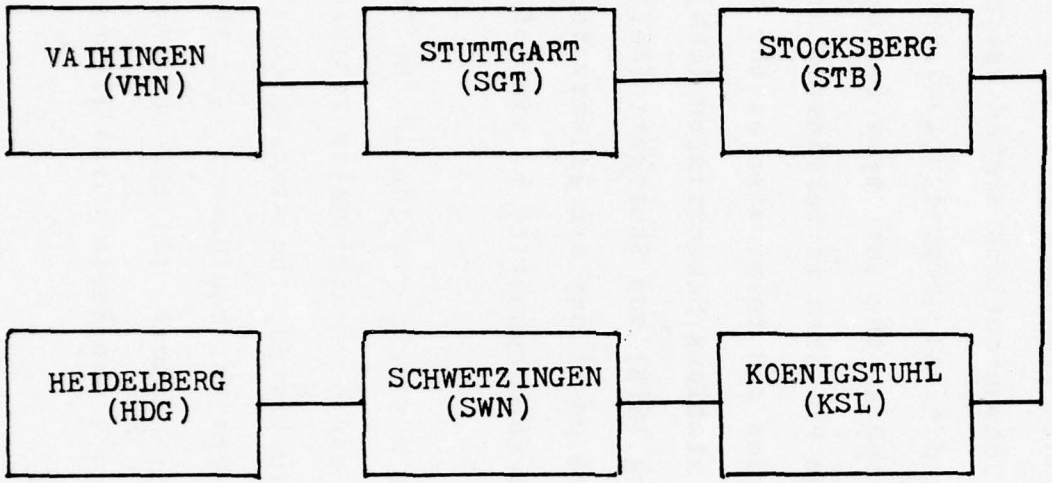
THE FRANKFURT-KOENIGSTUHL-VAIHINGEN AREA

2.1 FKV Area Configuration

The Frankfurt, Koenigstuhl, Vaihingen (FKV) area is a subset of the European Defense Communications System which was upgraded from an analog to a digital communications network and which was subsequently selected as the test area for the Digital ATEC Adaptation Program. The FKV area is terminated at one end by the Heidelberg (HDG) station and terminated at the other end by Vaihingen (VHN) with the stations Schwetzingen (SWN), Koenigstuhl (KSL), Stocksberg (STB) and Stuttgart (SGT) between the two ends. Their relative positions are illustrated in Figure 2-1. These nodes are interconnected by line-of-sight microwave links.

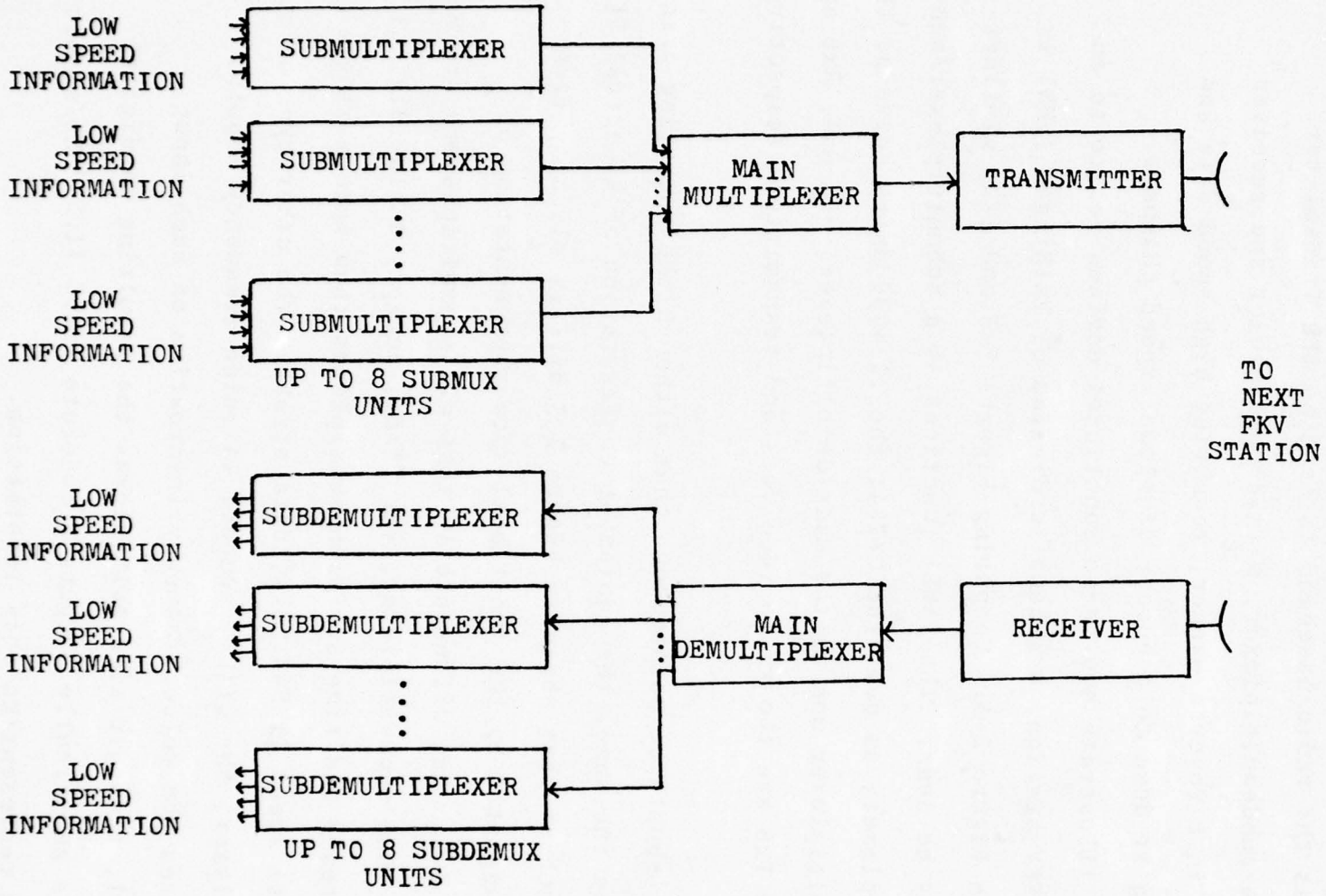
Looking more closely at a single station in the FKV network, an individual station may be functionally represented as shown in Figure 2-2. As illustrated, the station consists of three basic types of communications equipment: (1) the submultiplexers and subdemultiplexers, (2) the main multiplexer and main demultiplexer, and (3) the radio units (transmitter and receiver).

The function of the submultiplexer is to take in a number of low-speed communications channels and time-division multiplex (TDM) them into a moderate-speed data stream. The function of the main multiplexer is to accept the moderate speed data streams and time division multiplex them into a single



THE FRANKFURT-KOENIGSTUHL-VAIHINGEN AREA

FIGURE 2-1



FKV STATION FUNCTIONAL DIAGRAM

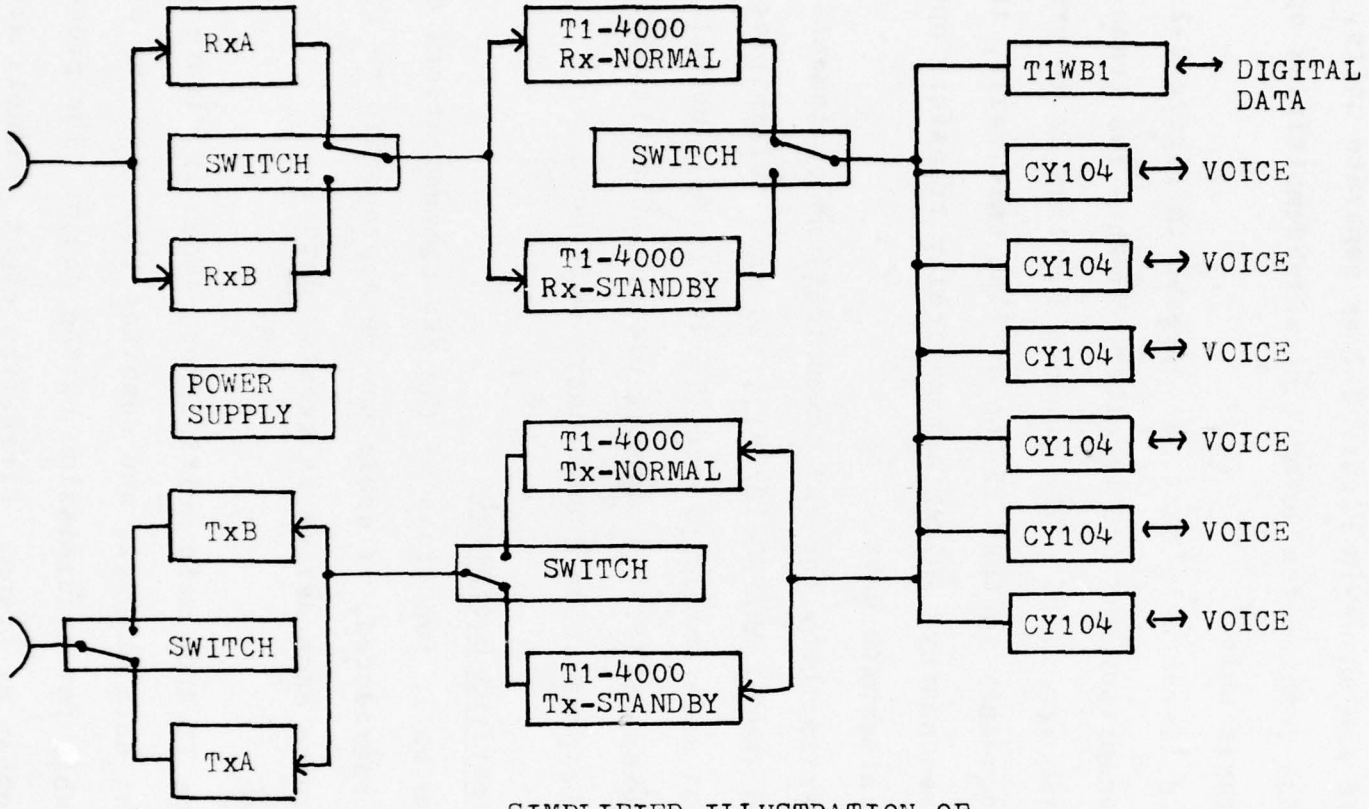
FIGURE 2-2

high speed data stream. The high speed data stream, which serves as the radio baseband is sent to the transmitter.

The subdemultiplexer, main demultiplexer and receiver operate in a reverse manner, receiving high speed data and breaking it down to a number of slower speed channels.

To illustrate how these functional devices relate to an actual FKV station, a schematic diagram of Vaihingen (VHN) is shown in Figure 2-3. Comparing Figures 2-3 and 2-2, similarities may be seen. The T1WB1 functions as a submultiplexer/subdemultiplexer, as does the CY104; the T1-4000 units serve as the main multiplexer and as the main demultiplexer; and RxA, RxB and TxA and TxB are the radio receivers and transmitters respectively.

It should be pointed out that although the operating principle is the same, the equipment configuration of an actual FKV site such as that shown in Figure 2-3 differs slightly from that suggested by the functional site representation of Figure 2-2. One difference is that all submultiplexers are not alike. One submultiplexer, the T1WB1, accepts 8 slow digital bit streams and time division multiplexes them into a single moderate speed (1.544 Mb/s) data stream. The other type of submultiplexer, the CY104, accepts 24 voice frequency inputs, digitizes the voice frequency information on each input channel, time division multiplexes the resulting 24 digital signals and finally outputs a moderate speed (1.544 Mb/s) bit stream representing this information.



SIMPLIFIED ILLUSTRATION OF
VHN SITE

FIGURE 2-3

A second difference is that although the submultiplexes and submultiplexer are shown in Figure 2-2 as separate units, the CY104 and T1WB1 combine the submultiplex/subdemultiplex operations in a single unit.

A third difference is that, as opposed to Figure 2-2 which shows one transmitter and one receiver, VHN has two transmitters and two receivers. The purpose for this is to provide equipment redundancy so that if the on-line unit fails, the protection (redundancy) switch automatically transfers operations to the alternate unit.

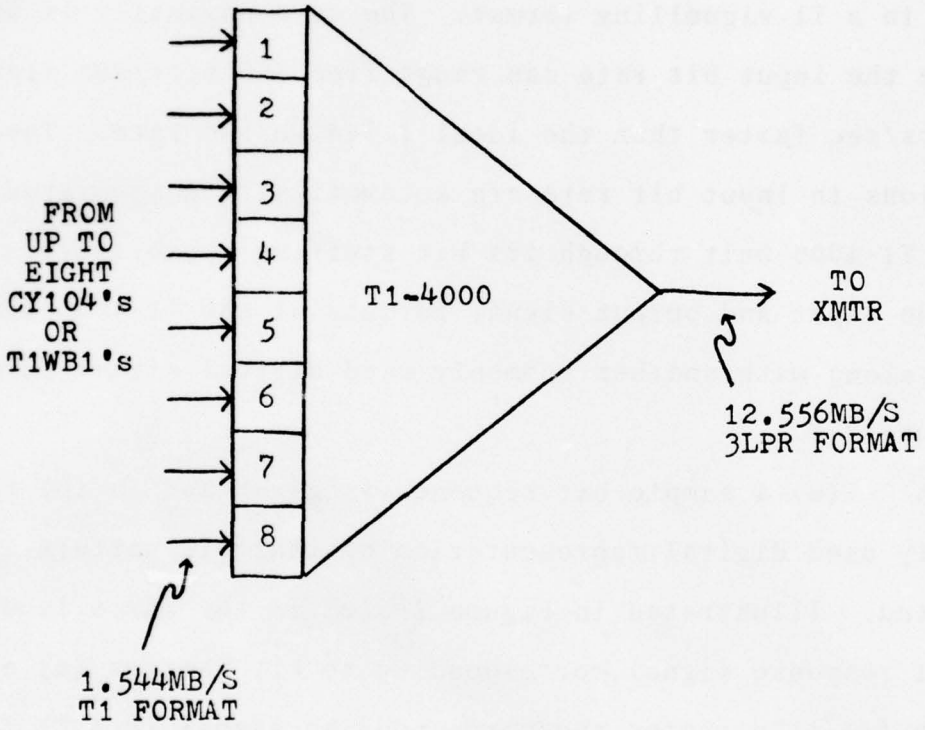
To summarize then, the FKV communications equipments are: (1) the radio (Model AN/FRC-162(V)); (2) main multiplexer (T1-4000); (3) main demultiplexer (T1-4000); (4) submultiplexer/subdemultiplexer CY104; (5) submultiplexer/subdemultiplexer T1WB1; (6) the protection (redundancy) switches.

2.2 Communications Equipment

With the basic functions of the FKV communications devices having been introduced, it would now be appropriate to individually examine each device in greater detail.

T1-4000

The T1-4000 main multiplexer, shown in Figure 2-4, accepts eight data channels and combines them into one digital signal suitable for transmission by the radio. The process is done in a number of steps. First, the eight channels are time division multiplexed; then, the resulting sequence is scrambled for the purpose of frequency spectrum smoothing. Following



T1-4000 TRANSMIT UNIT

FIGURE 2-4

this, the scrambled bit sequence is converted into a three level partial response (3LPR) signal format and is then finally sent to the transmitter.

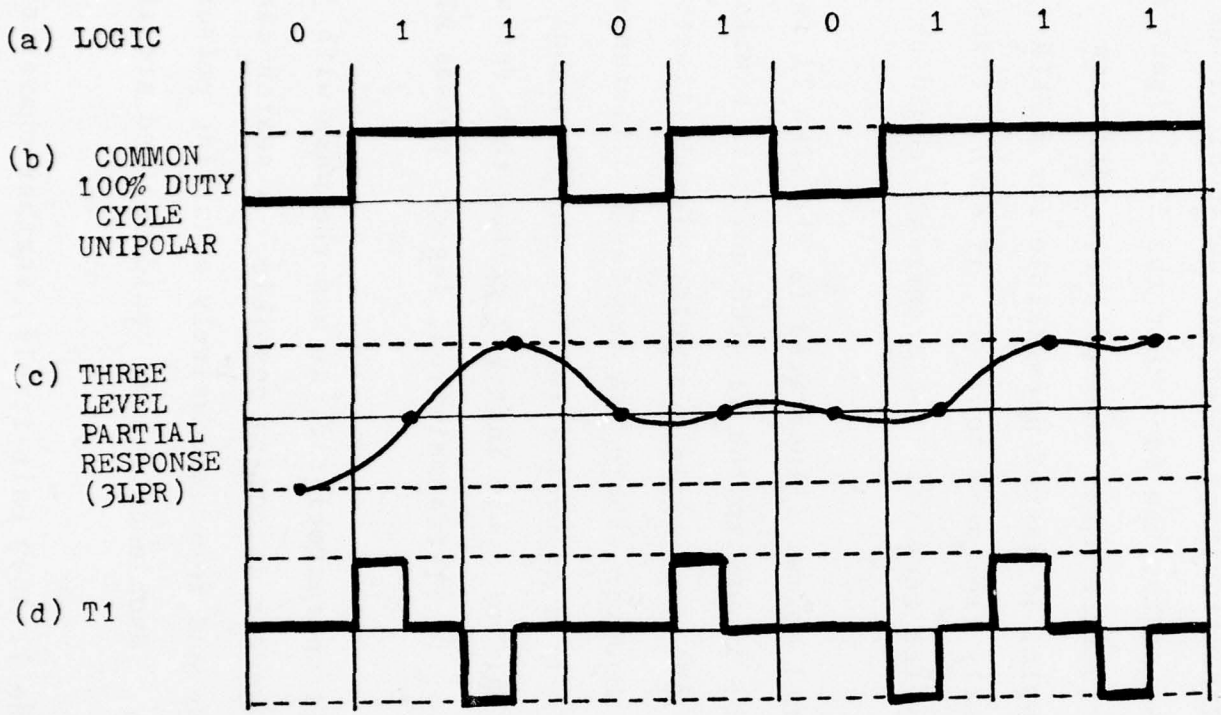
Each of the eight input signals comes from either a CY104 or T1WB1 unit and consists of a 1.544 Mb/s (nominally) bit stream in a T1 signalling format. The word nominally is used because the input bit rate can range from 300 bits/sec slower to 150 bits/sec faster than the ideal 1.544 Mb/sec rate. These variations in input bit rate are automatically compensated for by the T1-4000 unit through its bit stuffing capability.

The input and output signal formats of the T1-4000 are shown, along with another commonly used digital signal format, in Figure 2-5.

In 2-5(a) a sample bit sequence is given and in (b) the commonly used digital representation of that bit pattern is presented. Illustrated in Figure 2-5(c) is the three level partial response signal corresponding to bit pattern (a) and finally (d) illustrates the corresponding signal in a T1 format.

Regarding the three level partial response signalling format, it is decoded according to the following rules:

- if the received 3LPR signal is a +1, a logic 1 was transmitted;
- if the received 3LPR signal is a -1, a logic 0 was transmitted;
- if the 3LPR signal is a 0, the transmitted bit was the opposite of the bit previously transmitted.



FKV SIGNALLING FORMATS

FIGURE 2-5

It can be seen that the 3LPR signal has a number of attributes. First, its bandwidth, as compared with (b) or (d), is greatly reduced. This is evident by noting that the 3LPR signal lacks the discontinuities which are apparent in the other waveforms. Secondly, the fact that the 3LPR signal must follow a certain structure makes limited error detection possible. For example, it is not permissible for a 3LPR signal to transition directly from a +1 to a -1. If such a transition were to be noted by the receiver, the occurrence could be tagged as an error.

The other signal format illustrated is T1. The T1 format, which is used at the inputs to the T1-4000 unit, is similar to the commonly used 100% duty cycle, unipolar signal illustrated in Figure 2-5(b). However, there are two basic differences. First, when a logic 1 is to be transmitted, the T1 signal goes high for only one-half of a bit interval rather than for a full bit interval. Also, in T1 transmission, logic 1 pulses alternate in polarity.

This second T1 characteristic, as was the case with 3LPR, also makes limited error detection possible. A search can be made at the receive end for consecutively occurring pulses of identical polarity. Such occurrences could be (and are in FKV) tagged as errors.

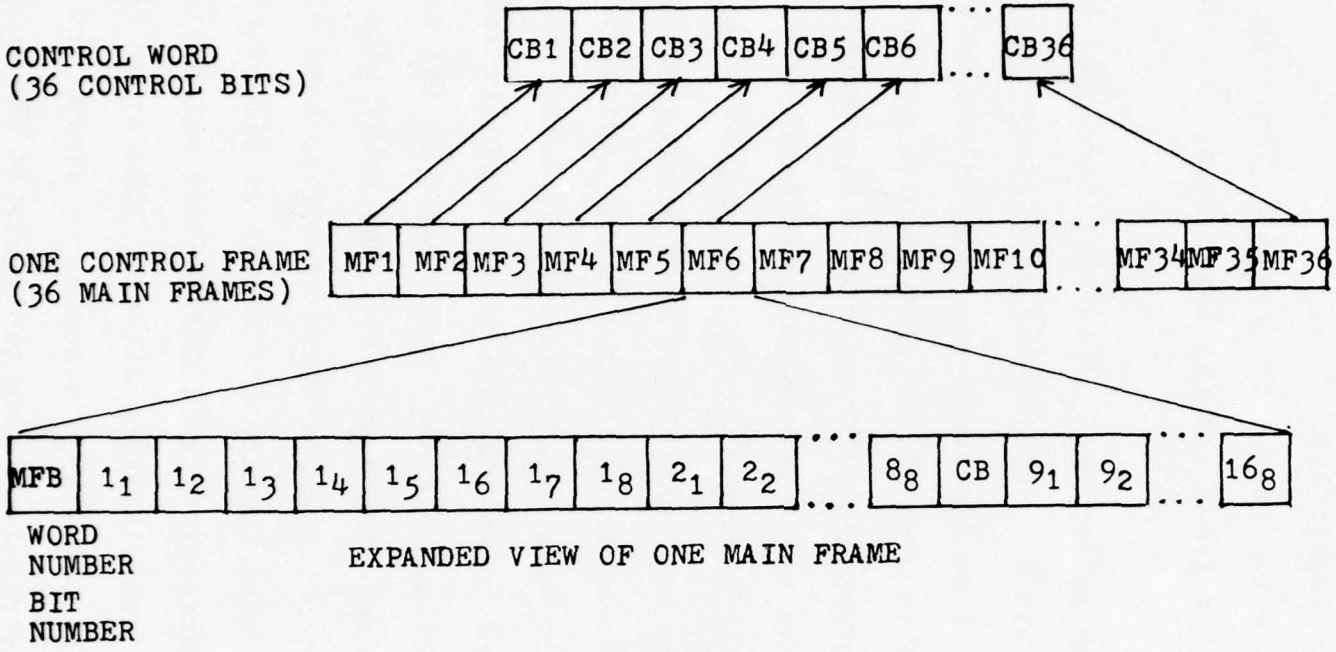
Concerning the T1-4000 unit itself, another characteristic of interest is its output TDM framing scheme. For decoding purposes, the time division multiplexed information is

organized in precise structures called frames. This frame structure has particular relevance to this report and is therefore illustrated in Figure 2-6.

The T1-4000 has two levels of framing. The higher level is called the control frame and the lower level is referred to as the main frame.

The main frame is composed of 130 bits arranged in the following order. Bit 1 is called the main frame bit. It signals the start of each main frame, alternating between a 1 and a 0 from frame to frame. The next 64 bits (#2 to #65) are information bits organized as 8 words of 8 bits each. Each bit of a word represents one bit from each of the T1-4000 input channels. The next bit (#66) is called the control bit. The receiver takes this one control bit from 36 consecutive main frames (36 main frames are contained in one control frame) and constructs a 36 bit word called the control word. The function of the control word is to indicate to the receiver whether or not the transmitter added dummy "stuff bits" to the data. If the control word does indeed indicate that stuff bits were added, the receiver disregards them. Finally, bits 67-130 contain more data bits in the same format as bits 2-65.

One final characteristic of the T1-4000 which will be considered is the fact that the T1-4000, like other FKV communications devices, has available a number of alarms and parameters which are useful for determining the state of the network. These are the alarms and parameters which go to the automatic



T1-4000 FRAME STRUCTURE

FIGURE 2-6

monitoring system, ATEC, which will be described in detail in the latter section of this chapter.

A list and description of the T1-4000 alarms/parameters, which are measured by ATEC, are given in Appendix A1.

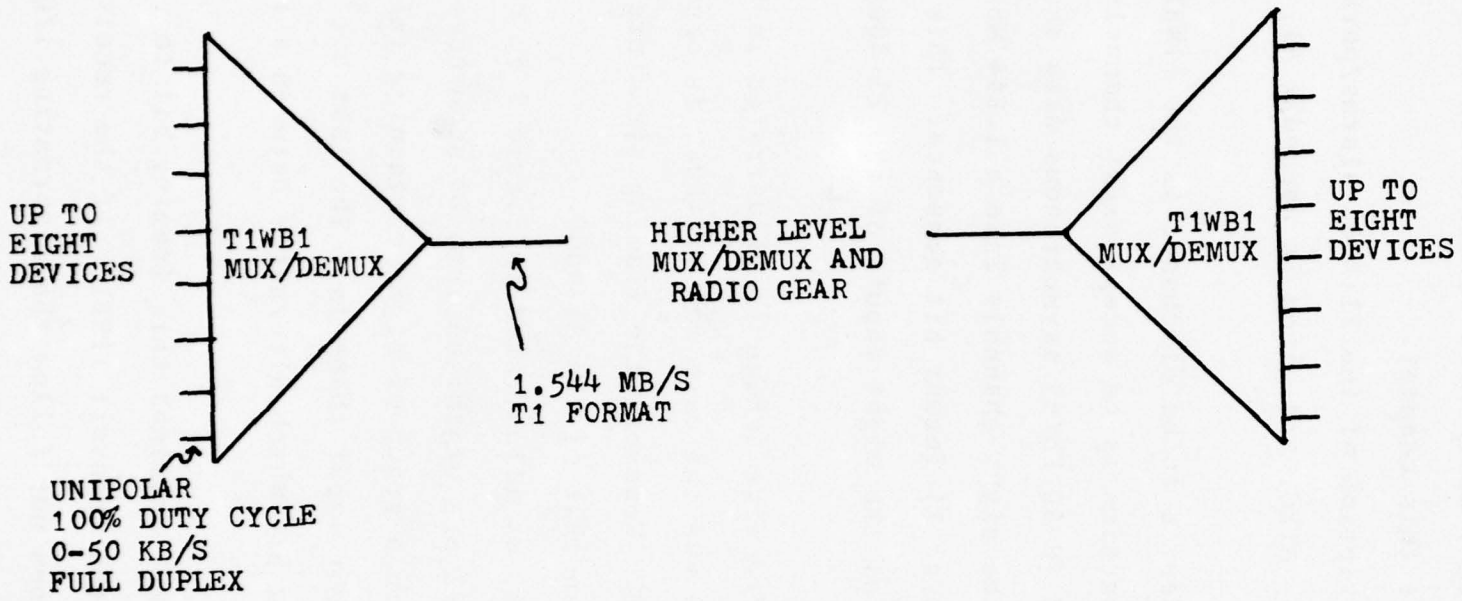
T1WB1

The next device to be discussed is the T1WB1 sub-multiplexer. Its function is to accept eight channels of relatively low speed (0-50 Kb/s) asynchronous data and time division multiplex the eight channels into a 1.544 Mb/s (-300 b/s to + 150 b/s) T1 format bit sequence. This sequence is then sent to one of the eight inputs of the T1-4000 main multiplexer.

The T1WB1 send/receive scheme is illustrated in Figure 2-7. The T1WB1 output, as was the case for T1-4000, is organized in a frame structure. However, the framing structure of the T1WB1 is simpler than that of the T1-4000.

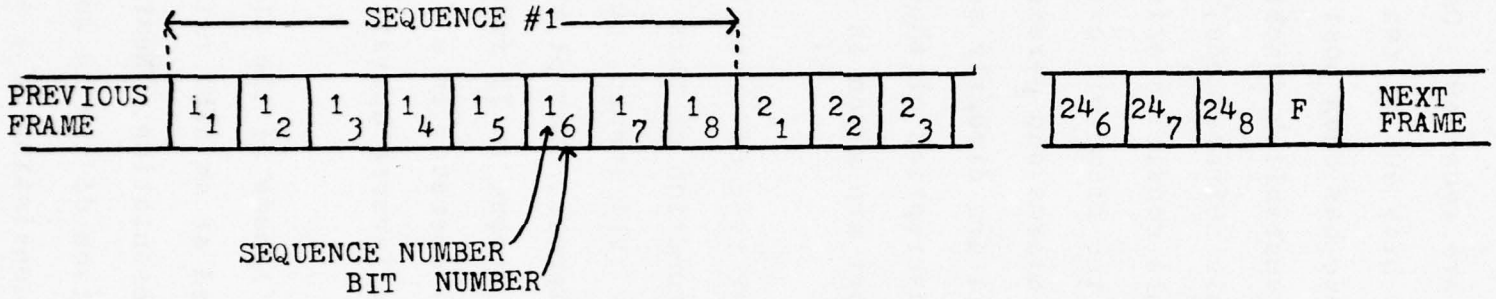
The T1WB1 frame, as illustrated in Figure 2-8, consists of 193 bits. Bits 1-192 are organized into 24 sequences of eight bits with each bit in a group of eight containing information about one of the eight input channels. The last bit of the frame is the Framing Bit which alternates between a 1 and a 0 from frame to frame.

The receive T1WB1 examines this framing bit to verify that it is in sync with the transmit T1WB1. If the receiver detects a frame bit which does not follow the alternating 1/0 format, it generates an error signal.



T1WB1 SEND/RECEIVE
CONFIGURATION

FIGURE 2-7



T1WB1 FRAME STRUCTURE
FIGURE 2-8

The receiver is considered to be in frame sync after seven consecutive correct frame bits are received. Once in this state, if three incorrect frame bits out of ten are received, the T1WB1 assumes that frame sync has been lost and enters a reframe mode in an attempt to reestablish synchronization with the transmit T1WB1. When in this reframe mode, an alarm signal is generated indicating that this condition exists.

The T1WB1, in addition to the frame bit error and reframe signals, has a number of other alarms and parameters available for monitoring (although not all are directly scanned by the ATEC system). A listing and description of those parameters which are relevant to this report are given in Appendix A2.

CY104

The CY104 is the other type of submultiplexer/subde-multiplexer used in FKV. The function of this device is to accept up to 24 voice frequency (VF) inputs, pulse code modulate and multiplex these signals, encrypt the resulting TDM bit stream and convert the bit stream to T1 format for output to the T1-4000 unit. The CY104 operates in a full duplex mode, thus enabling it to perform the inverse operations on received signals.

The fundamental operating scheme of the CY104 is this. Each input VF channel is sampled at an 8KHz rate and then converted to an 8 bit binary representation. Next, the 24 8-bit words representing the information of the 24 input channels are arranged in a frame structure consisting of a single frame bit

followed by the 24 8-bit words. This signal is then encrypted, converted to T1 format, and sent to the T1-4000 unit.

It should be pointed out that, as shown in Figure 2-9, the CY104 actually consists of 3 sub-units: the VICOM D2, KG-34 and HN-74. The VICOM D2 performs the sampling, A/D conversion, PCM and TDM operations, and also organizes the frame structure. The KG-34 does the encryption/decryption, and the HN-74 converts the signal to T1 format.

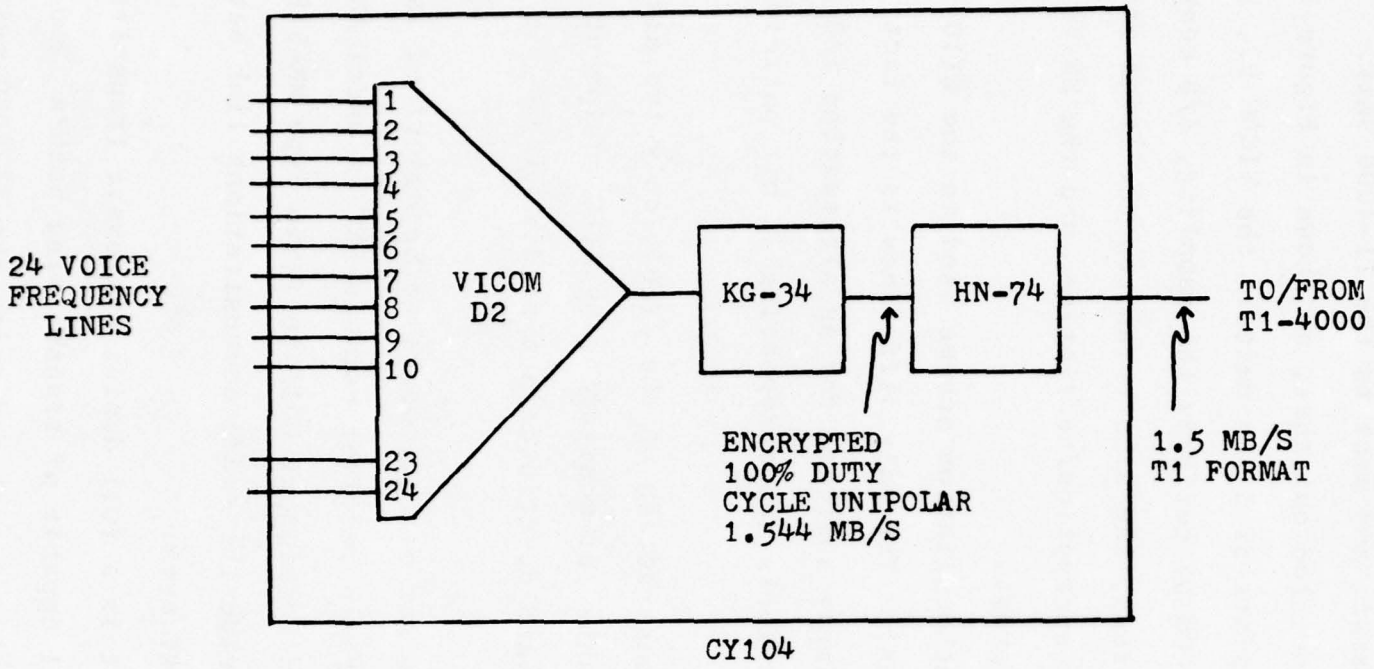
The frame synchronization scheme used in the CY104 is similar to the T1WB1. The only difference is the fact that while the T1WB1 simply searches for an alternating 1/0 frame bit pattern, the CY104 looks for a repeating 12 bit pattern (100011011100).

Due to the construction of the CY104, only two alarm signals are available for monitoring by ATEC equipment. These alarms are listed and described in Appendix A3.

Radio

The next set of equipments to be described is the radio unit. The radio receiver used in FKV is model AN/FRC-162(v), a modified version of Collins radio type MW-518. Its purpose is to provide the radio communications link between stations in the FKV area.

The radio set is a full duplex microwave transmitting and receiving terminal capable of transmitting both a 12.6 Mb/s data stream (the data that enters and exits the T1-4000 main multiplexer units) and also a network orderwire channel which



THE CY104 UNIT

FIGURE 2-9

consists of a voice maintenance circuit and the ATEC telemetry data.

The FKV radio consists of six basic devices: normal (main) transmitter, standby transmitter, normal (main) receiver, standby receiver, transmitter switchover unit and receiver switchover unit. This scheme makes it possible to switch from the main transmitter or receiver to the standby transmitter or receiver in case of equipment failure.

The alarms/parameters which emanate from the radio set are listed and described in Appendix A4.

Switches

It is the task of the switches to automatically transfer operations from the normal to standby unit or vice-versa if the currently operating unit fails. As can be seen in the previously presented schematic diagram of VHN, in Figure 2-3, a switchover unit provides this normal to standby and standby to normal transfer capability to the radio transmitter, radio receivers, T1-4000 transmitters and T1-4000 receivers.

One aspect of switch operation which is relevant to this report is that the switch units provide a status signal output. This status signal indicates which of the units under switch control (normal or standby) is currently on line. This signal is of great significance in fault detection and fault isolation efforts and is thus monitored by ATEC.

2.3 The ATEC System

In addition to the communications equipment, each FKV site

houses what is called ATEC equipment. The collective function of this ATEC hardware is to monitor the alarms and parameters output by FKV communications equipment and telemeter the status of these alarms and parameters to a central control point for display and analysis. Illustrated in Figure 2-10, which is actually an update of Figure 2-3, is an FKV station with both the communications and ATEC devices shown.

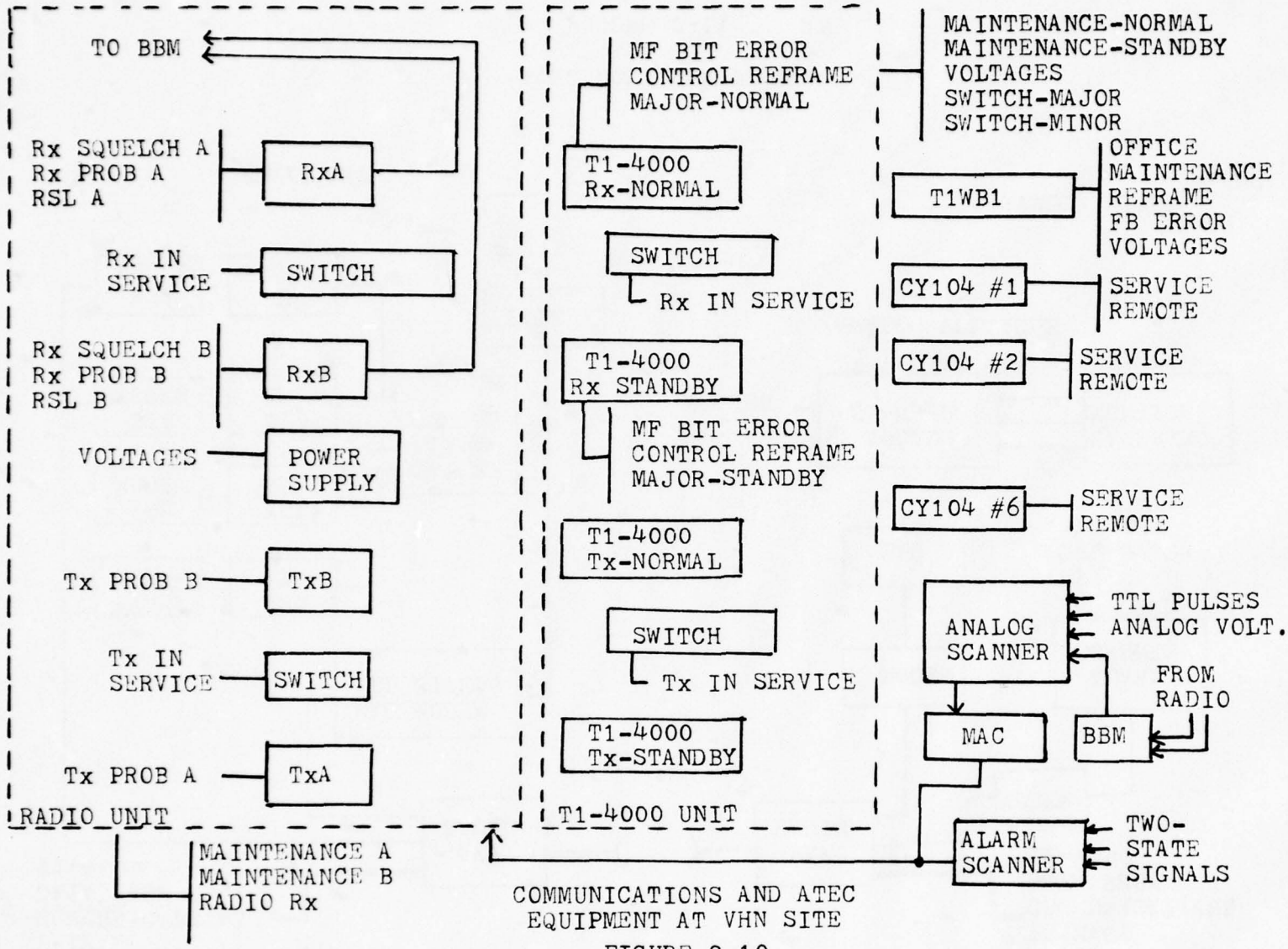
As can be seen, the ATEC monitoring devices at VHN station are the following: the Measurement Acquisition and Control Unit (MAC), the Alarm Scanner (AS), the Analog Scanner (ANS) and the Baseband Monitor (BBM).

The next few sections of this report will first introduce the configuration of the ATEC monitoring system elements, then describe each element individually and finally explain the operation of the ATEC system as a whole.

2.3.1 ATEC System Configuration

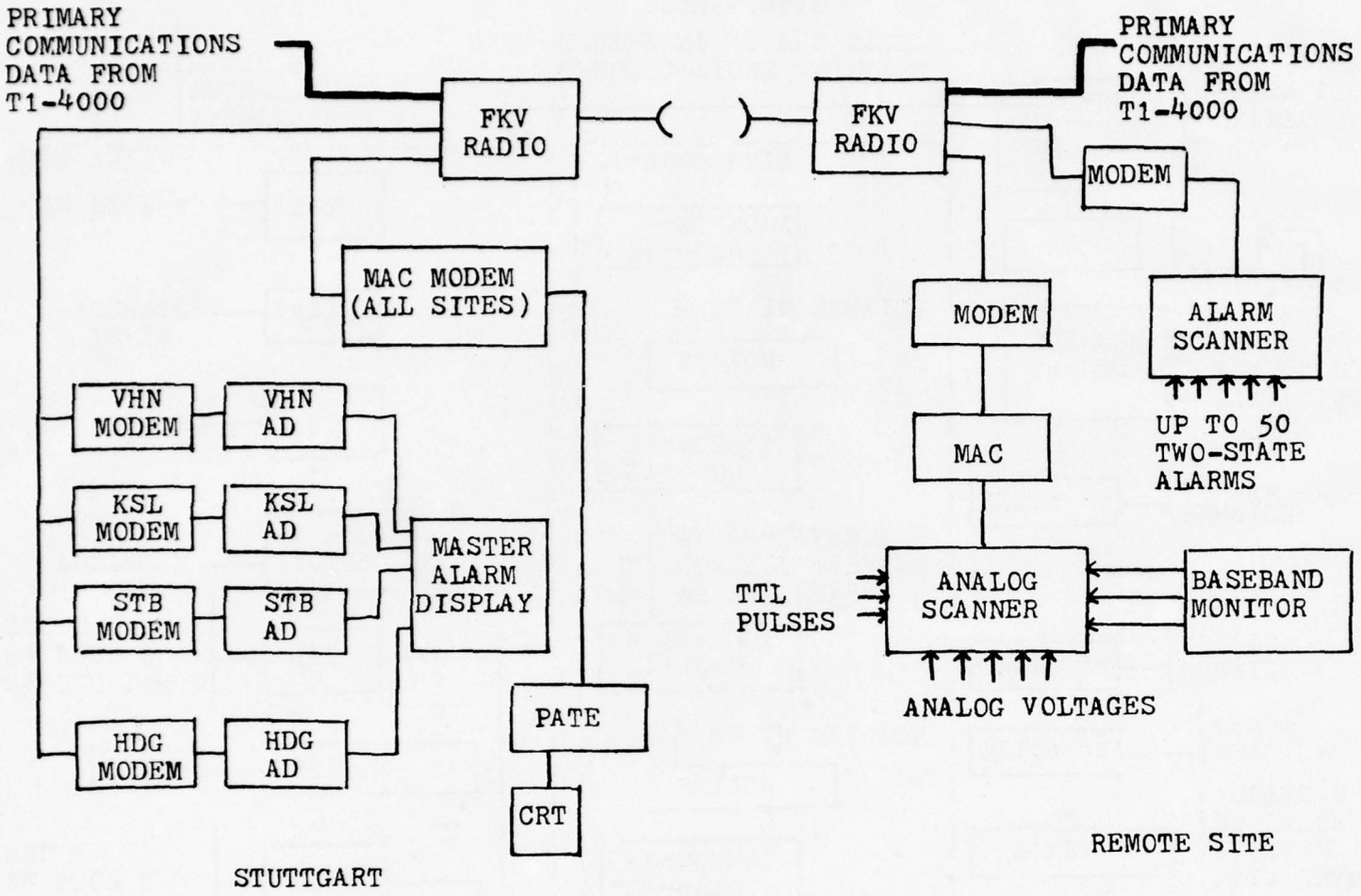
Shown in Figure 2-11 is the overall configuration of the elements in the ATEC system. In this diagram are shown the two types of ATEC sites: the Remote Site (there are 5 in FKV), where the automatic scanning of alarms and parameters takes place, and the Nodal Control Site where information from all the remote sites is received, processed and displayed. The five ATEC remote sites are HDG, SWN, KSL, STB and VHN; the single Nodal Control Site is SGT.

It should be pointed out that Stuttgart (SGT) also houses the standard complement of FKV communications gear and standard



COMMUNICATIONS AND ATEC EQUIPMENT AT VHN SITE

FIGURE 2-10



ATEC CONFIGURATION

FIGURE 2-11

ATEC monitoring devices found at remote sites. The Control Site processing equipment monitors the equipment as it would monitor the equipment at any other FKV station, considering it as just another remote site.

2.3.2 ATEC Equipment

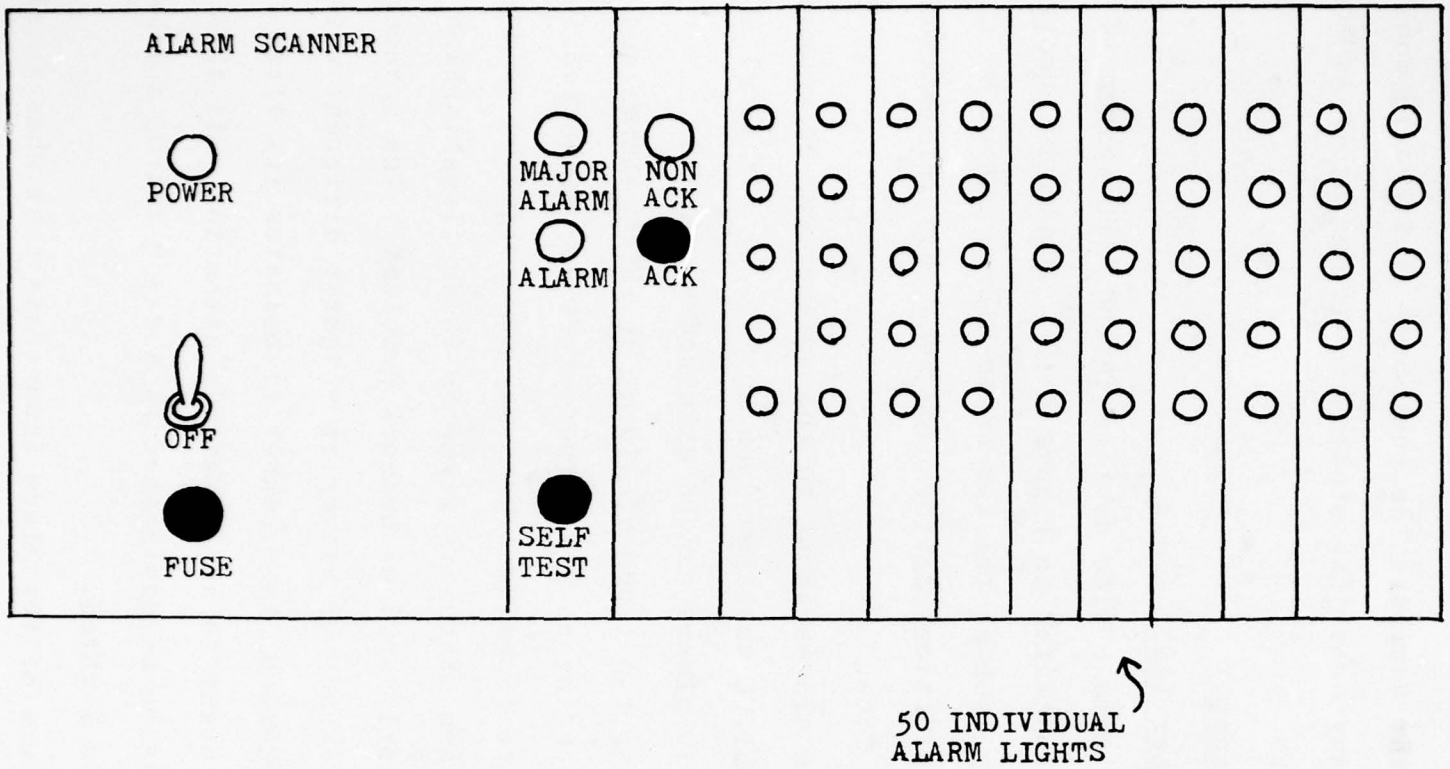
Alarm Scanner (AS)

One of the remote site devices in the ATEC system is the Alarm Scanner, illustrated in Figure 2-12. Its basic function is to sequentially look at the two-state alarms output by the various FKV communications devices and send this information to the Nodal Control Site.

The two-state alarms input to the scanner may be contact closures, two-level DC voltages such as TTL, or two level AC voltages. Up to 50 alarms can be examined by the AS.

There are also two types of alarms in FKV: Alarms and Major Alarms; depending on how jumper wires are connected in the AS, any one or more incoming alarms may be designated as Major Alarms. Major alarm status is given to those signals which indicate particularly serious network problems. The scanner handles the two classes of alarms in slightly different ways. If an alarm is received, the scanner illuminates its Alarm lamp to call the event to an operator's attention. If this alarm also happens to be designated as a major alarm, the Major Alarm lamp is also lighted.

Another feature of the Alarm Scanner is that when an alarm is received, the lamp for that particular alarm blinks and the



FKV ALARM SCANNER

FIGURE 2-12

alarm non-acknowledged (NON ACK) lamp lights. This indicates that an individual who is monitoring the alarm scanner has not yet acknowledged the event by depressing the acknowledge (ACK) button. When this button is pushed, the blinking stops and the NON ACK lamp goes off.

Also included in the Alarm Scanner is a self-test feature. Pressing the Self Test button tests the panel of lights and tests some of the internal logic of the AS. This test can also be activated by remote control from the Nodal Control Site.

The Alarm Scanner keeps track of major alarms, alarms, and alarm acknowledgments and sends this information to the Nodal Control Site via a 75 baud FKV radio subchannel.

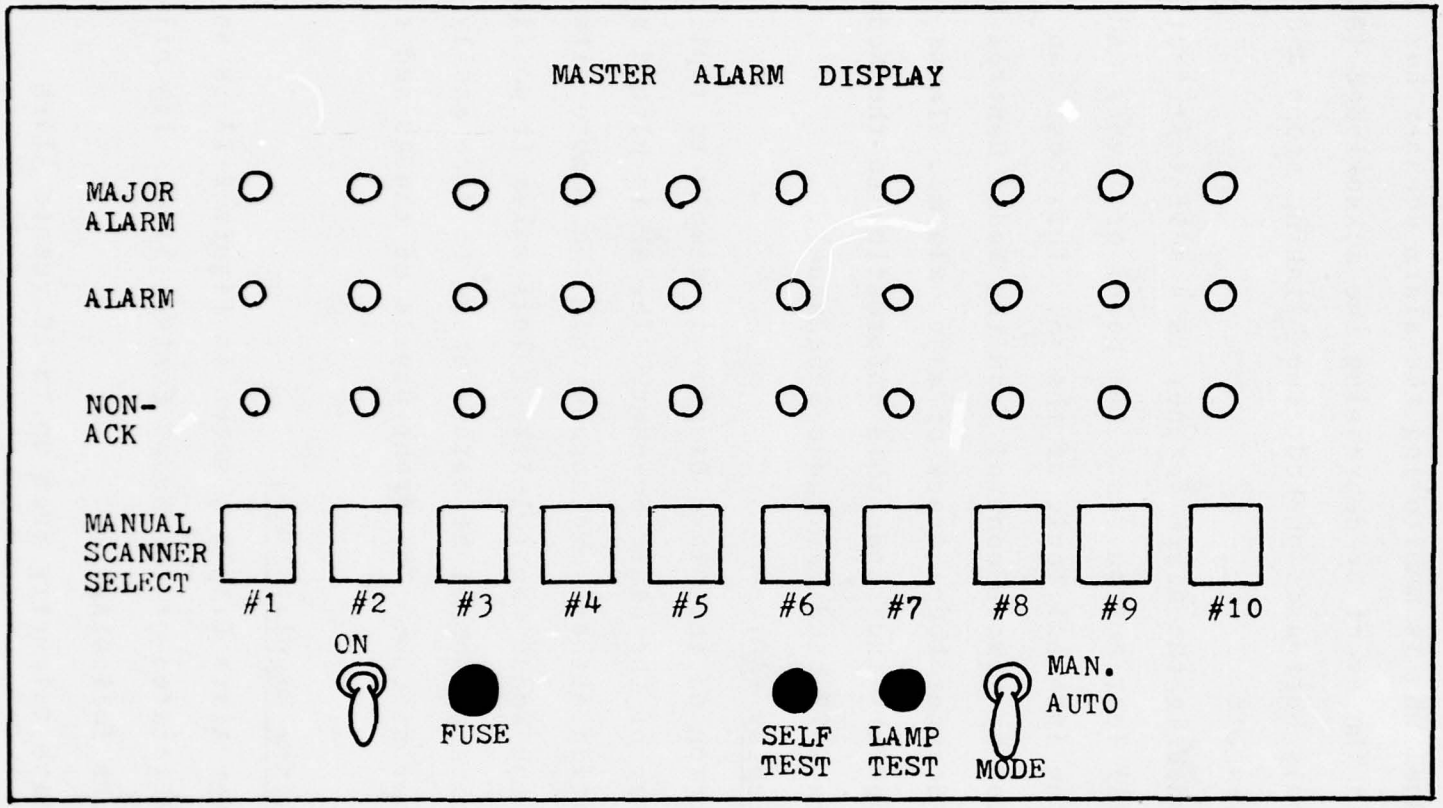
Alarm Display (AD)

The function of the Alarm Display is simply to replicate the front display of the Alarm Scanner. The AD is placed at a convenient location either somewhere within the remote site building or at the Nodal Control Site. This makes it possible for the monitoring personnel at either areas to more easily view the alarm scanner status. The front panels of the AD and the AS are identical.

Master Alarm Display (MAD)

The Master Alarm Display, shown in Figure 2-13 is an ATEC device which is located at the Nodal Control Site. Its primary functions are the following:

a) receive telemetry from up to 10 remote Alarm Scanners;



FKV MASTER ALARM DISPLAY

FIGURE 2-13

b) indicate whether or not each of the individual remote sites has

1) a Major Alarm

2) an alarm

3) an unacknowledged alarm;

c) generate control signals to activate a remote alarm scanner's self-test sequence.

The MAD can automatically and sequentially scan each alarm scanner or can be manually controlled for the purpose of viewing the status of a particular alarm scanner. The latter is done by depressing the desired Manual Alarm Scanner Select button and placing the Manual Select/Auto switch in the manual select position.

The MAD also functions as the Alarm Scanner-Computer interface, communicating with the CPU on a full duplex 150 baud line. The computer periodically makes inquiries of the MAD, commanding the MAD to transmit either the major alarm status of all alarm scanners or the complete status of a particular alarm scanner.

Measurement Acquisition and Control Unit (MAC)

Another device located at the remote site is the Measurement Acquisition and Control Unit (MAC). The major functions of the MAC are:

a) measure analog DC test voltages which come from FKV communications gear;

b) measure voice frequency (VF) voltages on selected FKV communications lines;

c) inject test tones on selected FKV communications

lines;

d) control the switching unit (Analog Scanner) which selects the voltages to be measured and routes them to the MAC and which also connects the MAC test tone output signal to selected lines.

When MAC performs a DC or VF parameter measurement, the result of the measurement is coded and telemetered to the nodal control site for analysis. When MAC is commanded to inject a test tone on a line, the MAC causes the Analog Scanner to connect the proper line to the MAC's tone output. While doing this, a MAC at the other end of the communications line measures the received tone and sends that measurement information to the nodal control site. Before measuring the AC voltage value of this received VF test tone, the MAC can switch various filters onto the VF line and terminate the receive end of the line with various terminating resistances.

Analog Scanner (ANS)

The Analog Scanner is the switching unit which is controlled by the MAC and is located, along with the MAC, at the remote sites.

As was mentioned in the last section, a primary function of the ANS is to either route DC or VF parameters from the parameter monitoring point to the MAC or connect the MAC test tone generator to an FKV communications line which is to be tested. However, this is not the only purpose of the Analog Scanner.

Another of its functions is to count the occurrences of

TTL pulses emitted by certain communications devices. For example, it counts the number of Frame Bit Error pulses emitted by the T1WB1. It then sends a representation of the count in the form of an analog DC voltage to the MAC for measurement.

The Analog Scanner also has the capability of latching the occurrence of short-duration pulses. For example, it latches the Rx Squelch Alarm signal emitted by the radio. This capability is provided to insure that some signals which may appear and disappear quickly do not elude detection.

Some signals, in addition to being latched by the ANS, are also scanned by the Alarm Scanner. This provides system controllers with two important bits of information. The Alarm Scanner data will inform the controller if the alarm currently exists and the ANS-MAC data will indicate whether the alarm condition existed at any time since the latch was last cleared.

Baseband Monitor (BBM)

The Baseband Monitor, located at all remote sites, examines the received high speed digital data signal coming from the radio for the three measures of quality: signal amplitude, average noise amplitude and noise bursts. The results of these three measurements are represented in 3 DC analog voltages which are sent to the Analog Scanner and thence to the MAC.

Programmable ATEC Terminal Element (PATE)

At the nodal control site, in addition to the already mentioned MAD and AD's, is the central computer system referred to as PATE or Programmable ATEC Terminal Element. The PATE

assimilates the Alarm Scanner and MAC information, computes trends, searches for out-of-tolerance conditions, stores data in history files and outputs relevant information to the system operator on a CRT or on paper.

The PATE is primarily a monitoring rather than a control device. This is to say that the PATE receives many signals from remote devices but sends few signals back. The only signals sent by PATE to the remote sites are relatively simple command signals to the MACs requesting the measurement of a particular parameter, requesting a test tone to be sent, or requesting interconnection, breaking, or bridging of certain VF communications lines. By sending these commands, PATE can effectively isolate system faults and can coordinate tests on communications lines between FKV sites.

2.3.3 ATEC Functional Summary

The following is a description of how the various ATEC equipments are interconnected to form a functional ATEC system. The ATEC devices and their relative configuration are shown in Figure 2-11 which was previously presented in this chapter. For the purpose of clarity, only the Nodal Control Site and one of the 5 Remote Sites are shown.

The Alarm Scanners at each remote site send information, via the modems and FKV radio subchannel, to the Nodal Control Site (NCS). At the NCS, the Alarm Scanner information is then received by an Alarm Display (one alarm display per alarm scanner) which displays the status of the remote site Alarm

Scanner.

The Master Alarm Display monitors up to ten AD's, scanning each for the presence of alarms, major alarms or unacknowledged alarms. Should one of these conditions be detected, an appropriate light on the MAD is illuminated.

At the remote site, the Analog Scanner (ANS) scans selected analog voltages, counts certain TTL signals and latches some TTL signals. It also scans the three baseband quality parameters output by the BBM. The ANS sends these signals in sequence to the MAC which in turn performs the actual measurement of the signals and telemeters the information to the Nodal Control Site. Once at the NCS, this MAC telemetry, along with the MAD data, is input to the PATE where it is processed, displayed and stored for future reference.

The MACs from all remote sites share a common 150 BPS party line frequency slot in the FKV radio subchannel; each remote Alarm Scanner communicates with the Nodal Control Site on a separate 75 BPS line.

2.4 ATEC Shortcomings

The ATEC system has a number of shortcomings, some of which could be solved by incorporating a microprocessor into the system.

One disadvantage of ATEC lies in its processing scheme. The vast majority of ATEC system processing is done at the Nodal Control Site with little processing done at the remote sites. This is a significant drawback because it is therefore necessary

to send all monitoring information to the NCS, burdening the NCS with a significant amount of processing work. By pre-processing data before it leaves the remote site, less raw data need be telemetered. An example of some possible remote pre-processing tasks are computation of parameter trends and selective transmission of only those alarms which had changed state since last being scanned. This remote site to NCS data reduction has two advantages. First, the telemetry bandwidth requirement is reduced and secondly, the NCS processing burden is relieved. Though these advantages may not be of immediate concern, their significance as the present FKV system expands may be much greater.

Other advantages of this preprocessing scheme are the following. With the amount of data being sent by remote sites to NCS reduced, given a certain amount of PATE processing capability, more remote sites may be added to the system. In addition, with processing capability at the remote site, the remote site could be programmed to store telemetry data should the telemetry link to NCS be lost.

A second disadvantage of the present ATEC system is its heavy reliance on hardware for the implementation of its monitoring functions. Many of the functions now performed in hardware may be replaced by software operations with some resulting benefits. Two such benefits are size reduction and power reduction. Size reduction is apparent by the fact that the functions of a relatively large number of discrete devices

may be replaced by a single large scale integration device. Power reduction is also realized because in many cases, TTL type hardware is replaced by a low power MOS microprocessor.

Another advantage of software systems over hardware systems is their flexibility. Substantial functional changes may be made in microprocessor-based software systems merely by replacing the Read Only Memory chips containing the system program. Corresponding changes in a hardware-based system would require significant physical equipment alteration.

Two final advantages of a microprocessor system include low cost and less maintenance. While the sophistication of microprocessor systems has increased dramatically over recent years, the cost has continually decreased. Many of the maintenance problems in digital systems relate to device interconnection failures. The fact that the microprocessor is fabricated by large-scale integration reduces the number of connections necessary and therefore reduces the number of maintenance problems.

Another ATEC disadvantage is that in some respects, its monitoring scheme is inflexible. This is evident in the system's alarm-monitoring strategy. For example, the scanning sequence and scanning rate of the Alarm Scanner cannot be changed except by hardware alteration. In addition, the PATE has no control over the alarm scanning process.

One advantage which could be gained by performing on site processing is an increase in this alarm scanning flexibility.

The scanning sequence and scanning rate could be made automatically adaptive to existing network conditions or could be brought under the control of the Nodal Control Site. Such capabilities could make network analysis or fault isolation procedures more efficient.

These previously mentioned facts have prompted this report which investigates the feasibility of incorporating a microcomputer system at the remote sites. The object of this study is not to attempt to immediately eliminate those ATEC shortcomings which have been discussed, but to describe the first step in the process which is to interface the microprocessor to the various FKV communications devices.

CHAPTER 3

THE MICROPROCESSOR-BASED ATEC SYSTEM

3.1 Chapter Objective

The objective of this chapter is to describe a microprocessor implementation of a subset of those functions monitored as part of the digital ATEC system. Specifically, this chapter proposes to replace all of the operations of the alarm scanner and some of the functions of the MAC with a microprocessor-based system. This proposed microprocessor-based ATEC system will hereafter be referred to as M-ATEC.

The rationale for utilizing the microprocessor in this particular way is the following. Given that the fundamental objective of this work was to illustrate how a microprocessor may be used in ATEC, and given that the system was extremely centralized with regard to processing, it was decided to locate a microprocessor at a remote site to decentralize the network. Furthermore, since the primary remote site function is that of parameter/alarm scanning, and since a microprocessor is very capable of performing such scanning, it was decided to utilize the microprocessor in such a scanning capacity.

3.2 The Microcomputer System

3.2.1 System Architecture

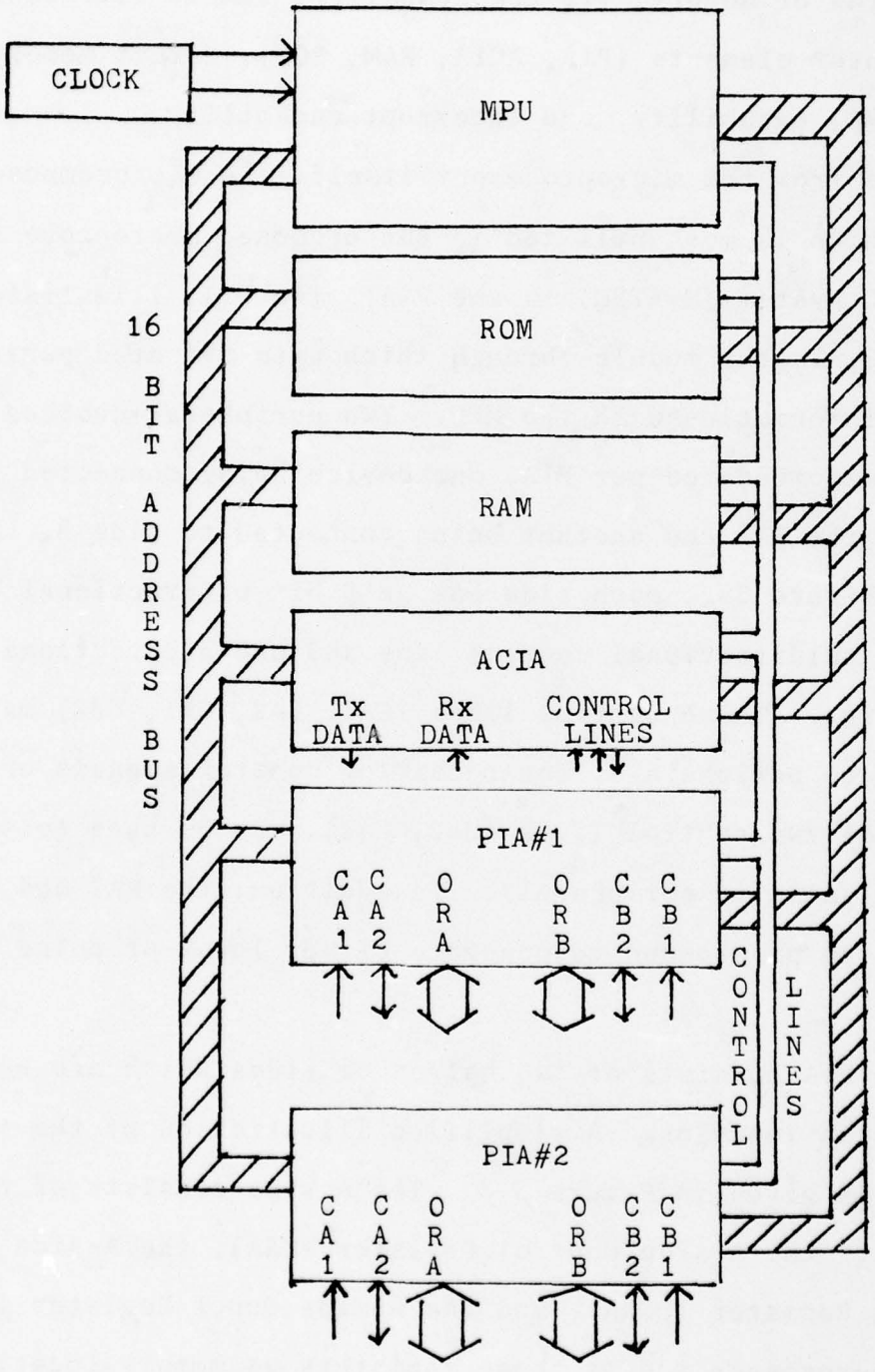
The microprocessor (MPU) selected for use was the Motorola MC6800 [5]-[6]. Selection was based on the versatility of the device, the ease of interfacing with the external

environment and the availability of good documentation.

Along with the microprocessor chip, four other types of devices were selected for use. These devices, which are simply interfaced with each other, comprise an MC6800 microcomputer system which is illustrated in Figure 3-1. An MC6800 microcomputer system consists, therefore, of the Microprocessor, Read Only Memory (ROM), Random Access Memory (RAM), a Peripheral Interface Adaptor (PIA), and an Asynchronous Communication Interface Adaptor (ACIA).

The Read Only Memory (ROM) is a 1024x8 memory device which contains information programmed into it at the time of manufacture. It contains the sequential operating instructions for the computer system. Though the contents of ROM cannot be changed under program control, the microcomputer operating sequence may be changed by merely installing new ROM chips. The Random Access Memory (RAM) is that section of the microcomputer memory in which information can be stored or from which information may be retrieved. In contrast to the ROM, the contents of RAM are easily alterable under program control. The Asynchronous Communication Interface Adaptor (ACIA) transfers serial, asynchronous information between the microcomputer and the external environment. The Peripheral Interface Adaptor (PIA) serves as an interface between the microprocessor and byte-oriented peripherals.

Some of the significant features of this Motorola microcomputer system include: the capability of addressing up to



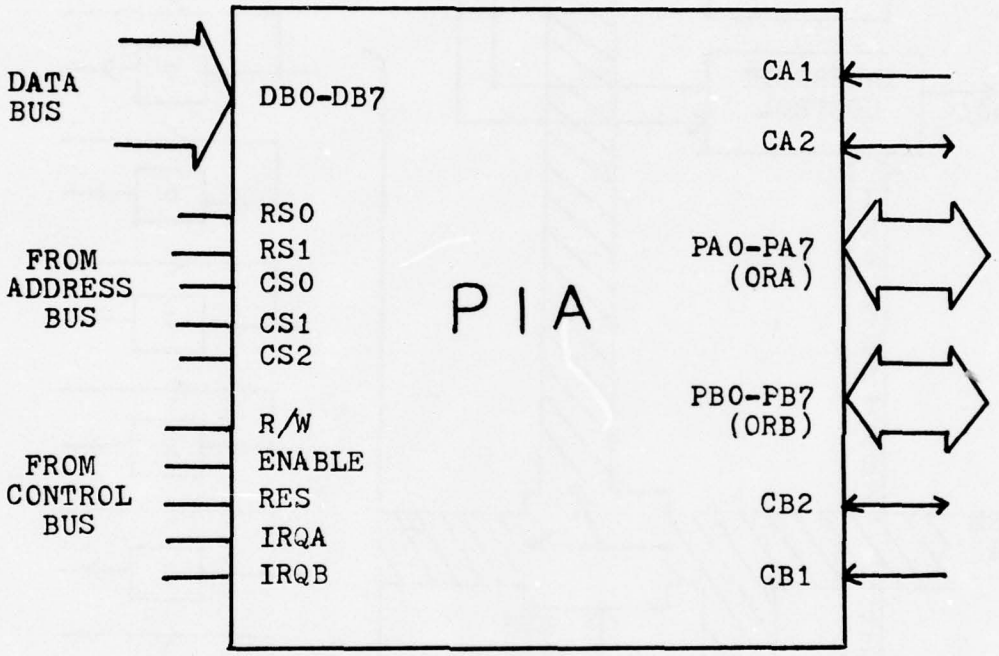
MC6800 MICROCOMPUTER SYSTEM

FIGURE 3-1

65,536 words of memory, TTL compatability, simple interfacing of microcomputer elements (PIA, ACIA, RAM, ROM), direct memory access (DMA) capability, and interrupt capability.

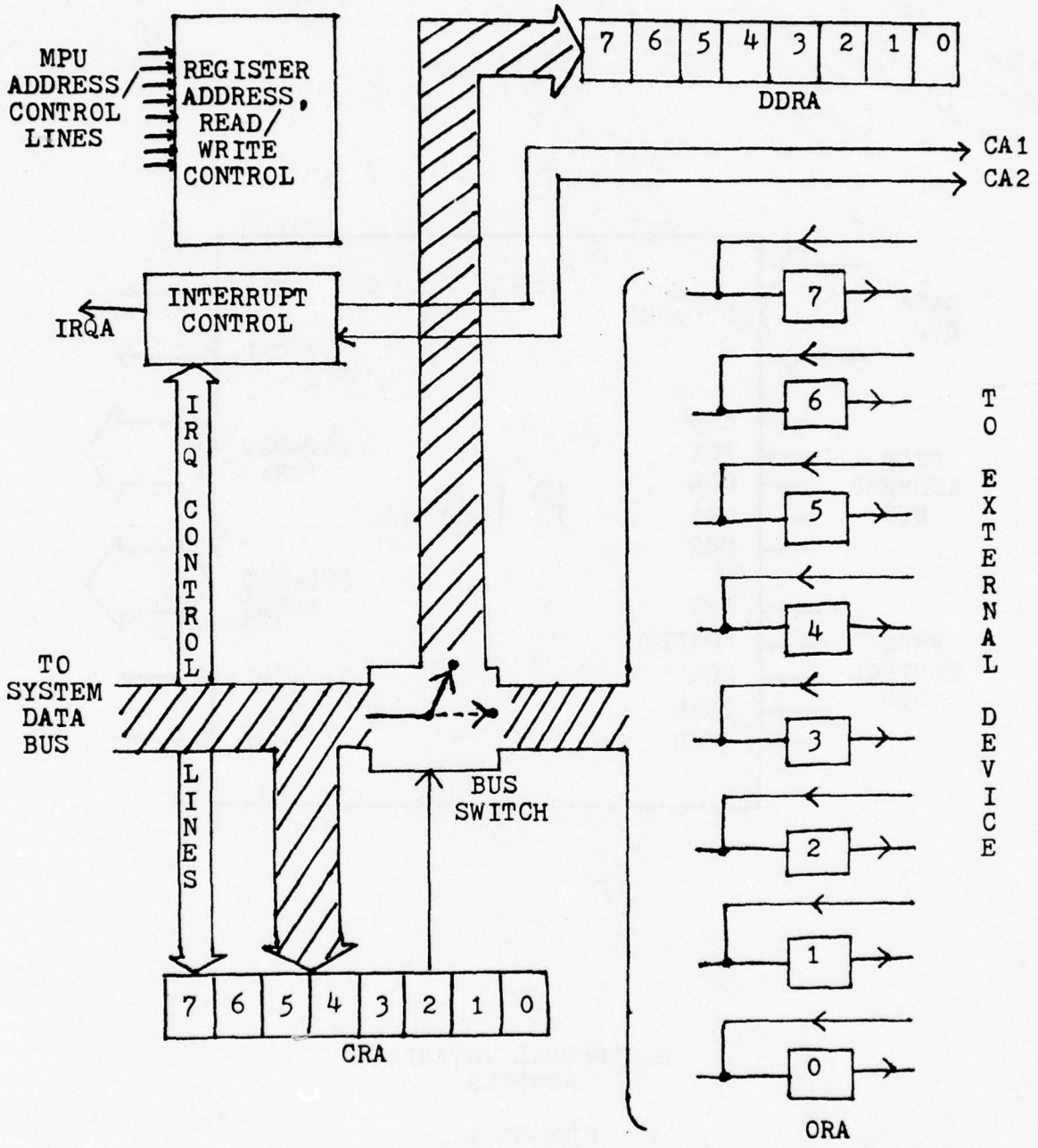
Aside from the microprocessor itself, the microcomputer element which is most utilized in the proposed microprocessor-based ATEC system (M-ATEC) is the PIA. The PIA, illustrated in Figure 3-2, is the module through which byte-oriented peripherals exchange information with the MPU. Two peripheral devices are normally accommodated per PIA, one device being connected to side A of the PIA and another being connected to side B. As shown in Figure 3-2, each side has an 8 bit bidirectional data port, one unidirectional control line and one bidirectional control line. These control lines (CA1, CA2, CB1, CB2) may be connected to peripherals, for receiving control signals or, in the case of two control lines (CB2, CA2), may be used to send control signals to peripherals. In addition, the CA2 and CB2 lines may be programmed to generate either level or pulse output signals.

Each PIA consists of two halves or sides which are nearly identical in function. A simplified illustration of the A side of a PIA is given in Figure 3-3. The A side consists of three registers: the A-side Control Register (CRA), the A-side Data Direction Register (DDRA), and the A-side Ouput Register (ORA). The microprocessor treats these registers as memory locations with the implication being that they may be written into or read by standard MC6800 memory reference instructions.



PERIPHERAL INTERFACE
ADAPTER

FIGURE 3-2



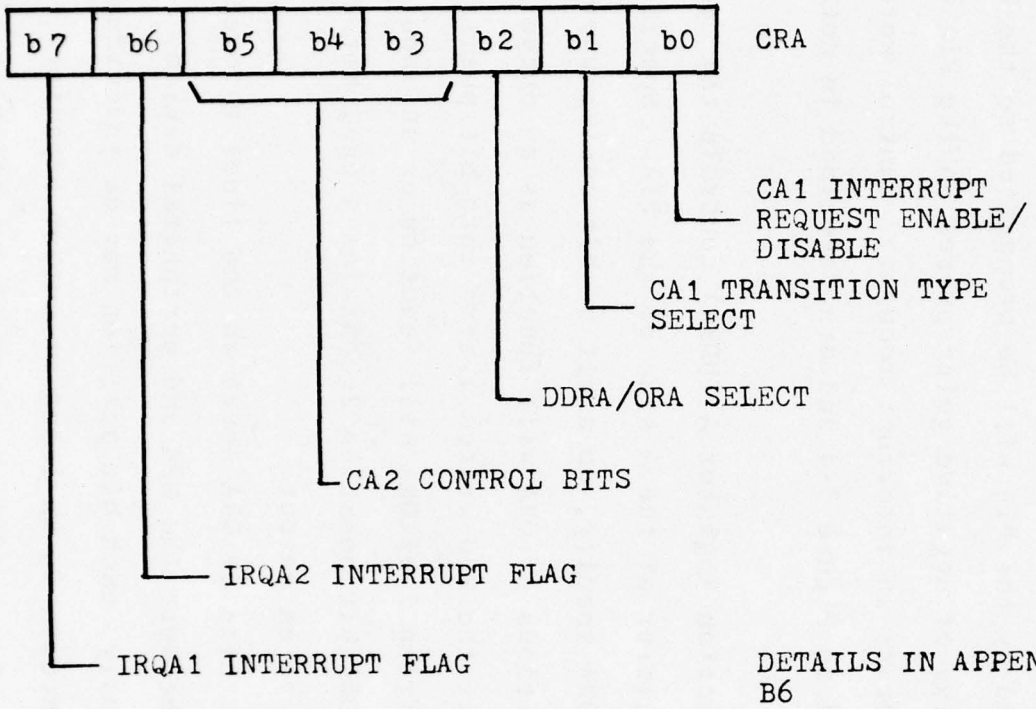
PERIPHERAL INTERFACE ADAPTER (PIA)
SIDE A

FIGURE 3-3

The CRA is a register which contains a coded control word establishing the various operating modes of the A side of the PIA. For instance, the contents of CRA establish whether CA2 will function as an output or an input, whether interrupt requests received by the PIA will be propagated to the MPU, and whether positive or negative-going pulses on the PIA control lines may generate an interrupt request. Control word options are summarized in Figure 3-4 and are described in detail in Appendix B6.

Data Direction Register A (DDRA) controls the operation of the output register of the A side of the PIA. Specifically, the contents of DDRA specify, on a bit-by-bit basis, whether each of the 8 bit positions of ORA will function as an output or input. For example, if the MPU writes a zero into bit position 2 of DDRA, bit position 2 of ORA will function as an input. Conversely, if DDRA bit position 2 contains a one, bit 2 of ORA will function as an output.

The eight bits of ORA serve as the lines through which data is exchanged between the MPU and peripheral devices. As mentioned previously, each bit position may be individually programmed to function in an input or output capacity. When programmed for input, data present at a particular bit position will be read into the MPU during a read output register command; when programmed for output, data written into a certain bit position by the MPU during a write to output register command, will be stored in that bit position, available for access by a



PIA SIDE A CONTROL REGISTER FORMAT

FIGURE 3-4

peripheral device.

3.2.2 Interrupt

Another feature of the MC6800 microcomputer system which deserves closer scrutiny is its interrupt system. Interrupt is the name given to a situation in which the MPU temporarily suspends the execution of the current program and transfers control to another program. When this second program is concluded, control then reverts back to the main program. Of interest in this report, is how an interrupt is initiated by a peripheral device.

In the proposed M-ATEC system, as is the case with most computer systems, interrupt requests are generated by peripheral devices. The request comes in the form of a pulse or voltage level sent by a peripheral to one of the PIA control signal inputs (CA1, CA2, CB1, CB2). The PIA examines the signals at the control inputs and, if the appropriate signal arrives, it sends an interrupt request signal to the MPU.

With regard to interrupts, the PIA is an extremely versatile device. As specified by the control word resident in CRA of the PIA, the PIA will recognize only certain signals as being valid interrupt requests. For example, considering side A of the PIA and referring back to Figure 3-4, if bit 1 of CRA is set equal to one, only low to high transitions on control input CA1 will be recognized by the PIA as being valid interrupt requests. In addition, upon the receipt of the proper CA1 interrupt signal, the PIA may be programmed to generate an MPU interrupt or not

generate an MPU interrupt, as specified by bit 0 of CRA.

The method by which the PIA deals with a sample interrupt signal may be described as follows. Assume that the interrupt signal arrives on CA1. Assume also that CRA bit 1 is set equal to 1 and CRA bit 0 is set to 1. With bit 1 of the CRA set, then in order to be recognized, it is necessary that the interrupt signal be characterized by a low-to-high transition. When the proper signal arrives, bit 7 of CRA, which serves as an interrupt flag, is set. Since CRA bit 0 is set to 1, this signal arrival also causes the PIA to send an interrupt request to the MPU.

Bits 7 and 6 of CRA serve as interrupt flags; bit 7 is set by the appearance of an appropriate interrupt signal on CA1 and bit 6 is set by the appearance of an appropriate signal on CA2. Should an interrupt occur, the MPU may determine which line (CA1 or CA2) had been active by examining the state of bits 6 and 7 of CRA. Reading CRA automatically clears these flag bits.

If CA2 is programmed as an input, by setting CRA bit 5 equal to zero, it functions in the same way as CA1. When CA2 is used for input, bits 3 and 4 control CA2 operation in the same way that bits 0 and 1 control CA1 operation.

3.3 FKV Alarms and Parameters

At a typical FKV remote site there are a number of alarms and parameters which are to be monitored by digital ATEC. These alarms and parameters, listed in Figure 3-5, are those which originate in FKV communications equipment. Although more signals

ALARM SCANNER INPUTS

Rx SQUELCH A
Rx PROBLEM A
Rx SQUELCH B
Rx PROBLEM B
RADIO Rx
MAINTENANCE A (RADIO)
MAINTENANCE B (RADIO)
Tx PROBLEM A
Tx PROBLEM B
MAJOR-NORMAL
MAJOR-STANDBY
SWITCH MAJOR
SWITCH MINOR
MAINTENANCE-NORMAL (T1-4000)
MAINTENANCE-STANDBY (T1-4000)
Rx IN SERVICE (RADIO)
Tx IN SERVICE (RADIO)
Rx IN SERVICE (T1-4000)
Tx IN SERVICE (T1-4000)

OFFICE
MAINTENANCE (T1WB1)
REFRAME
SERVICE (CY104 #1)
REMOTE (CY104 #1)
SERVICE (CY104 #2)
REMOTE (CY104 #2)
SERVICE (CY104 #3)
REMOTE (CY104 #3)
SERVICE (CY104 #4)
REMOTE (CY104 #4)
SERVICE (CY104 #5)
REMOTE (CY104 #5)
SERVICE (CY104 #6)
REMOTE (CY104 #6)

ANALOG SCANNER INPUTS

RSL A
RSL B
BBM OUTPUT #1
BBM OUTPUT #2
BBM OUTPUT #3
MAIN FRAME BIT ERROR-NORMAL
CONTROL REFRAME-NORMAL
MAIN FRAME BIT ERROR-STANDBY
CONTROL REFRAME-STANBBY
Rx IN SERVICE (RADIO)
Rx SQUELCH A
Rx SQUELCH B
Rx IN SERVICE (T1-4000)
FRAME BIT ERROR
REFRAME

EIGHT RADIO POWER SUPPLY VOLTAGES
FIVE T1-4000 POWER SUPPLY VOLTAGES
SIX T1WB1 POWER SUPPLY VOLTAGES

ALARM SCANNER AND ANALOG SCANNER INPUTS

FIGURE 3-5

are available for monitoring, the ATEC system only scans those which were deemed necessary for monitoring by the ATEC Digital Adaptation Study. These are the same signals scanned by the proposed M-ATEC system.

Presented in Figure 3-6 is a schematic diagram of the VHN station. This figure shows the various FKV communications devices and indicates the alarms/parameters extracted from each device for monitoring purposes.

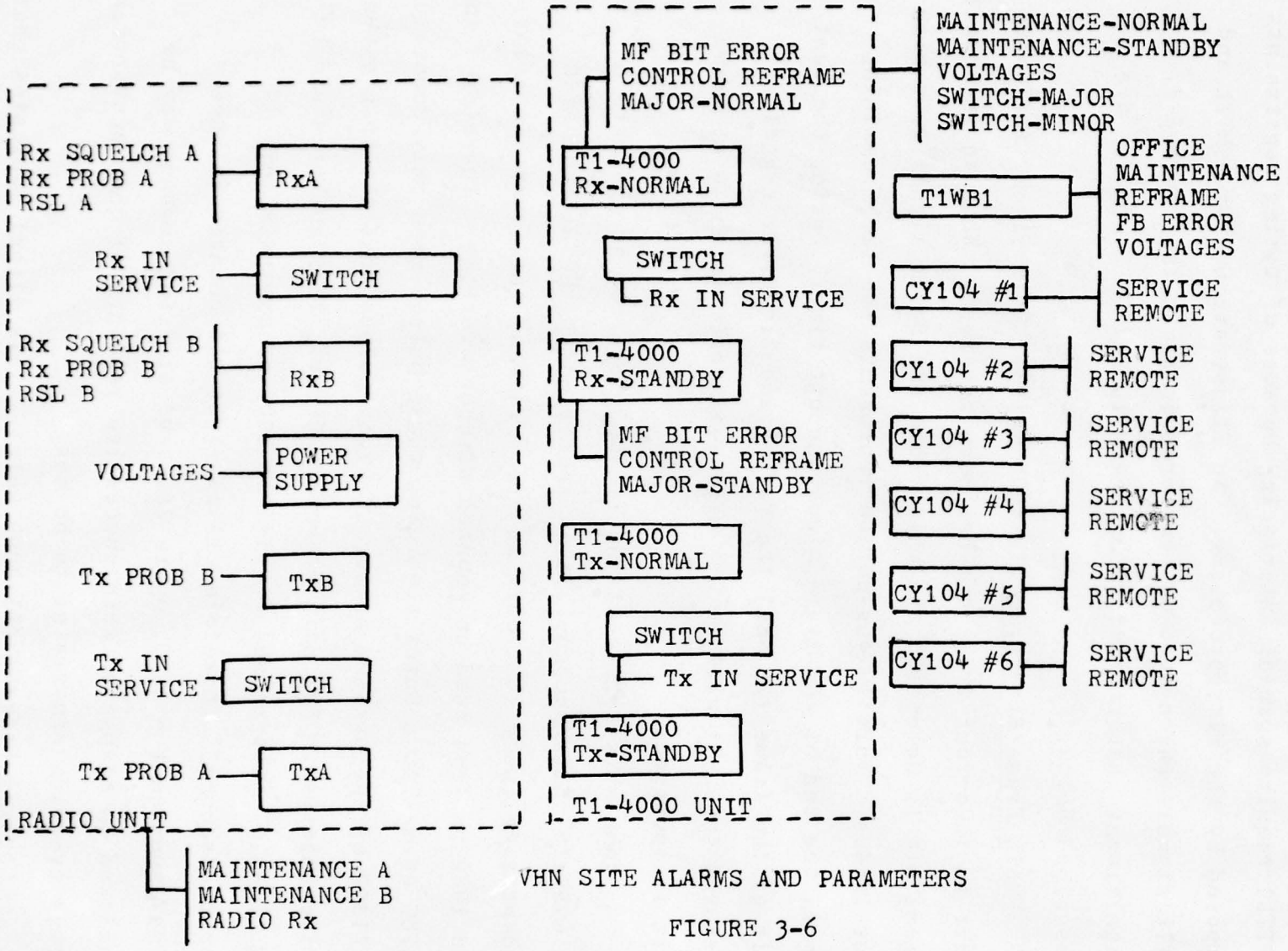
The alarms and parameters monitored at VHN may be classified as one of the following types:

Contact Closure. These signals appear as either normally open or normally closed circuit paths to ground.

TTL Voltages. These are conventional logic signals which may be further classified according to their repetition rate. Slow TTL (STTL) signals are those with a minimum repetition period greater than one second. Medium speed TTL (MTTL) signals are those with a repetition period between 50μs and one second. Fast TTL (FTTL) signals are those with a repetition period of less than 50μs.

Slowly Varying Analog Voltages. These are voltages of near-zero frequency such as a power supply voltage.

Of particular interest are the TTL signals. Depending on the repetition rate of the TTL, different techniques must be developed to interface these signals to the microcomputer system. Slow TTL (STTL) signals may be monitored in the same way as contact closures. However, medium speed TTL (MTTL) and fast TTL



VHN SITE ALARMS AND PARAMETERS

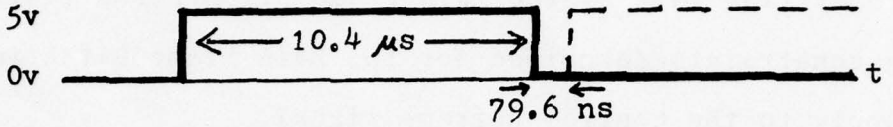
FIGURE 3-6

(FTTL, require special interfacing because of timing constraints imposed by the microprocessor. An illustration of the MTTL and FTTL signals which must be monitored is given in Figure 3-7. Significant characteristics of the MTTL and FTTL signals are described below.

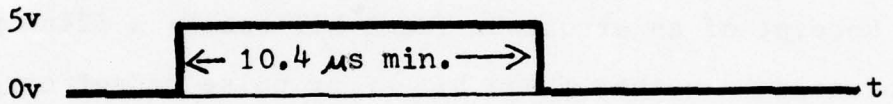
Main Frame Bit Error (T1-4000 unit). This signal indicates that an incorrect frame bit has been received. When an incorrect frame bit is detected, the Main Frame Bit Error signal goes high for 10.4μs. This 10.4μs period represents the time remaining until the end of the frame minus one bit time. During the last bit of the frame (79.6ns) the Main Frame Bit Error signal returns low. It will return high again only if the next frame bit is incorrect.

Frame bits arrive at the T1-4000 receiver at the rate of 9.6558×10^4 bits/second. It is specified in the Digital ATEC Adaptation Study that only an error rate of one frame bit error in 1000 or less need be counted without overflow. Therefore, an ATEC or M-ATEC counter recording these pulses need only count to 1/1000 of the maximum number of error pulses possible in a given time interval. For Main Frame Bit Errors, this number would be 9.6558×10^4 bits/second divided by 1000 or approximately 97 errors/second. Therefore, if an eight bit counter is used (maximum count = 255), up to 255 ÷ 97 or 2.628 seconds may be allowed to elapse between successive readings of the counter for this overflow constraint to be met.

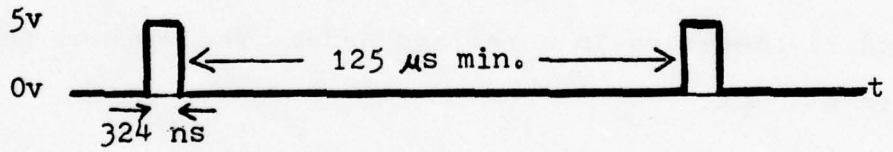
Control Reframe (T1-4000 unit). This signal indicates that



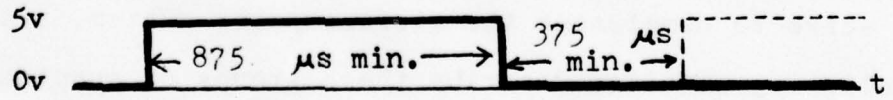
(a) MAIN FRAME BIT ERROR (T1-4000) - FTTL



(b) CONTROL REFRAME (T1-4000) - FTTL



(c) FRAME BIT ERROR (T1WB1) - MTTL



(d) REFRAME (T1WB1) - MTTL

FKV MTTL AND FTTL SIGNALS

FIGURE 3-7

a receive T1-4000 has lost control frame synchronization with its transmitting counterpart. The minimum Control Reframe pulse length is 10.4μs. Since, at worst case, this signal has the same repetition rate as the Main Frame Bit Error signal, the timing constraints described for the Main Frame Bit Error signal also apply to the Control Reframe signal.

Frame Bit Error (T1WB1 unit). This signal indicates that a receive frame bit violates the proper frame bit sequence format. Receipt of an erroneous frame bit causes a 324ns pulse to be generated. Another frame bit error pulse cannot occur until the next frame bit is received, 125μs later.

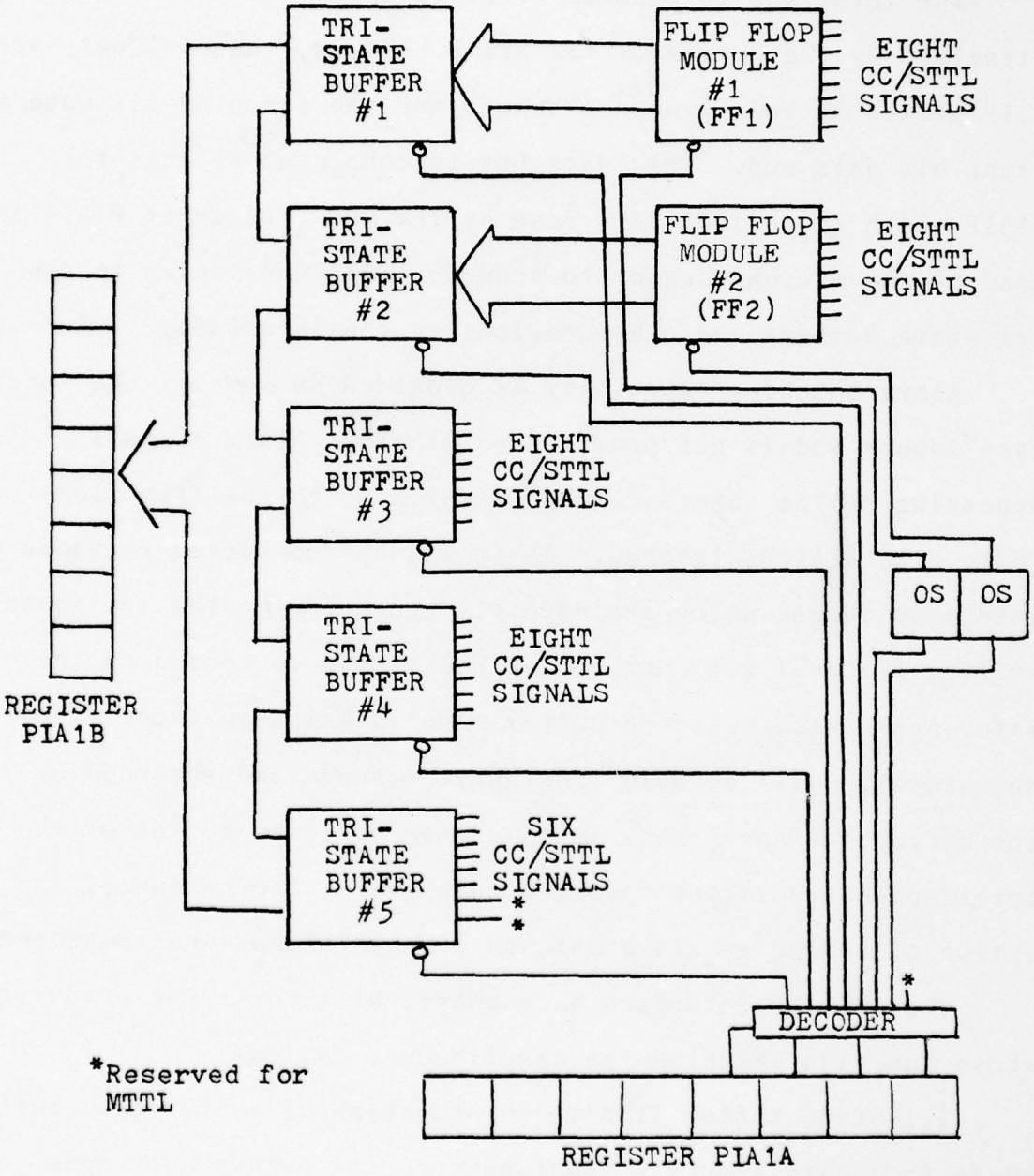
Reframe (T1WB1). This is a TTL signal indicating that the receive T1WB1 has lost frame synchronization with the transmitter and is therefore in a reframe node. The minimum reframe time is 875.0μs.

3.4 Alarm/Parameter Interfaces

In the proposed M-ATEC system various groups of devices, which serve to complement the microcomputer system, are required. The following sections describe these groups of supplementary circuits.

3.4.1 CC/STTL Interface

The Contact Closure/Slow TTL Interface (CC/STTLI), shown in Figure 3-8, is that group of devices in the M-ATEC system which permits the microprocessor to perform a scan of two-state FKV equipment alarms and parameters. Thus, it accomplishes the primary function performed by the Alarm Scanner used in the ATEC



CONTACT CLOSURE/SLOW TTL INTERFACE

FIGURE 3-8

system.

The interface is capable of accepting up to 38 CC/STTL signals. By the action of tri-state buffers, these signals are multiplexed in four groups of eight and one group of six onto an eight bit data bus. This data bus is connected to register PIA1B which is periodically read by the MPU. Register PIA1A is used by the microprocessor to send control information to the tri-state buffers and other devices on the interface.

Alarm latching capability is provided on some of the interface inputs and is not provided on others. Alarm signals appearing on the interface inputs which go to the flip flops (FF1, FF2) will be latched. Alarm signals connected to those interface inputs which are directly connected to the Tri-State Buffers (TSB3-5) will not be latched. When connected to the latching inputs, alarm/parameter signals which go true, even momentarily, will be held true until scanned and recorded by the microprocessor. This latching/non-latching option of the interface board is incorporated to allow system personnel the option of having an alarm latched or not latched when detected.

The CC/STTL Interface is composed of three types of devices whose function which may be described as follows:

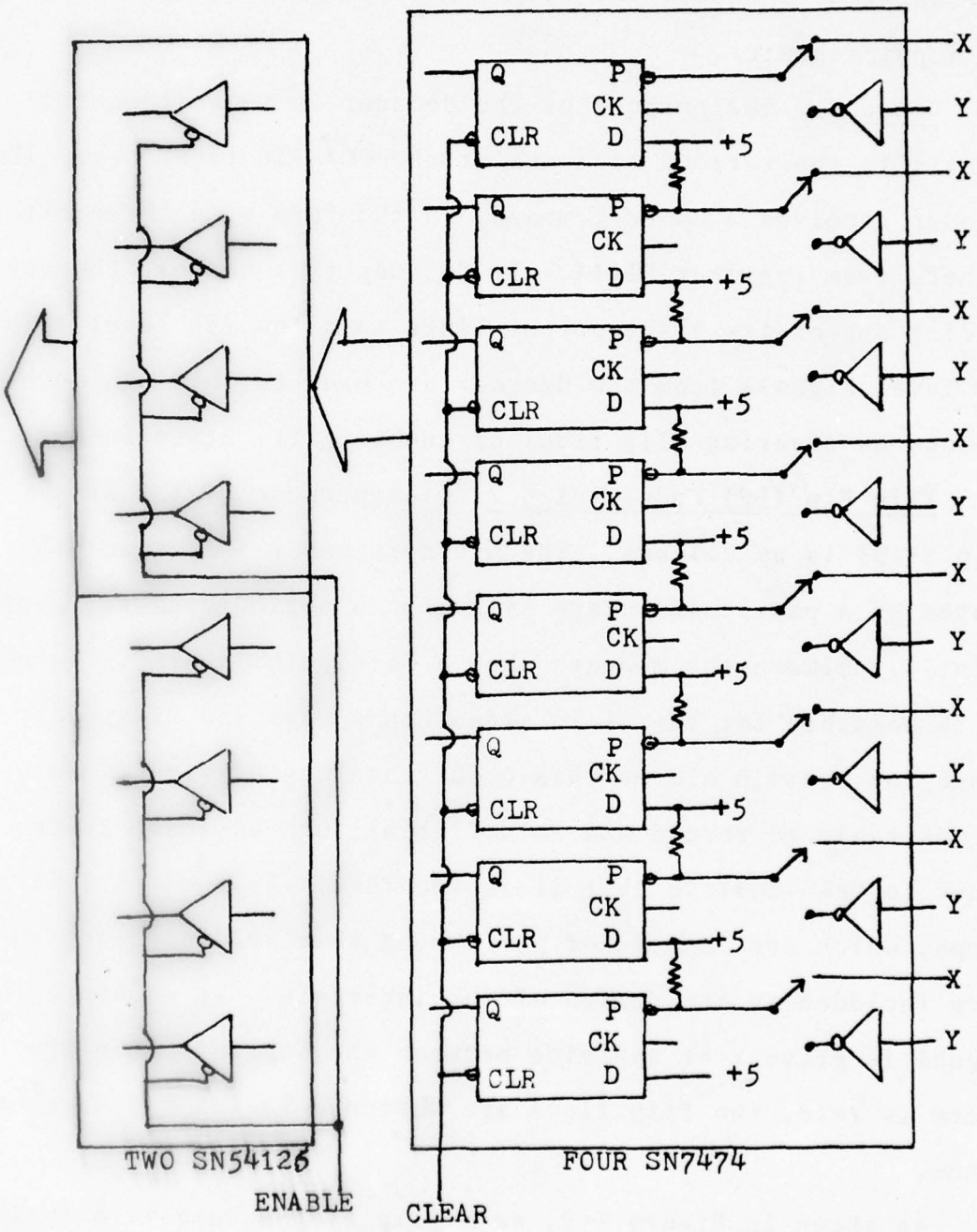
Tri-State Buffer (TSB). The function of a tri-state buffer is to pass data from its input port to its output port upon receipt of an enable pulse, and to assume a high impedance state at its output terminal when this enable signal is absent. Its fundamental function in the interface is that of a switch which,

when enabled, connects the flip flops or CC/STTL signals to the PIA input register.

Decoder. The purpose of the decoder is to emit control signals to the various elements of the CC/STTL interface. The decoder receives a coded command, in the form of a three-bit number, from register PIA1A. It decodes this number, thereby forcing one of its eight output lines to a low TTL level. These low level signals from the decoder are used to initiate such actions as clearing flip flops or enabling tri-state buffers.

Flip Flp (FF) Modules 1 & 2. The purpose of the set of flip flops is as follows. The microprocessor only scans the states of a particular alarm signal on a periodic basis. Consequently, between the moments when a particular alarm is examined, it is possible for the alarm signal to appear and disappear. Since for certain alarms this occurrence may be significant, it is desirable to record and hold (latch) such an alarm state in order to make certain that it is recorded. As a result, flip flops, which are capable of performing this holding function were included in the design of the interface. If an alarm signal is present at any time between the instants when that alarm is read, the flip flops are designed to latch its occurrence.

As shown in Figure 3-9, each flip flop module is actually composed of 4 D-type positive edge-triggered flip flops with preset and clear. Each flip flop is connected in such a way that a negative level applied to its preset (P) input will



FLIP FLOP/TRI-STATE BUFFER PAIR
ON CC/STTL INTERFACE

FIGURE 3-9

cause its output (Q) to assume a high state. Thus, the flip flop performs a type of latching function.

There are four types of signals to be monitored by the interface: normally low and normally high Slow TTL, and normally open and normally closed contact closures. By merely connecting a pull up resistor to the contact closure line, the contact closure signal takes on a TTL characteristic. Therefore, in actuality, only two types of signals must be accommodated by the interface: normally low TTL and normally high TTL. As previously stated, a flip flop will assume a high state when a negative level is applied to its preset input. Therefore, normally high TTL signals, which go low when an alarm state exists, should be connected to the preset input. This will insure that the low level alarm states will be latched. For normally low TTL signals which go high when an alarm state exists, the same latching function may be performed by first passing the signal through an inverter and then connecting the inverter output to the preset (P) input of the flip flop. Consequently, referring to Figure 3-9, normally high TTL or normally open contact closures should be applied to input X, and normally low TTL or normally closed contact closures should be applied to input Y.

One Shot Multivibrators. Due to system software which is discussed later, the flip flop clear signal emitted by the decoder is of long duration. To shorten this pulse length, a one shot multivibrator is used.

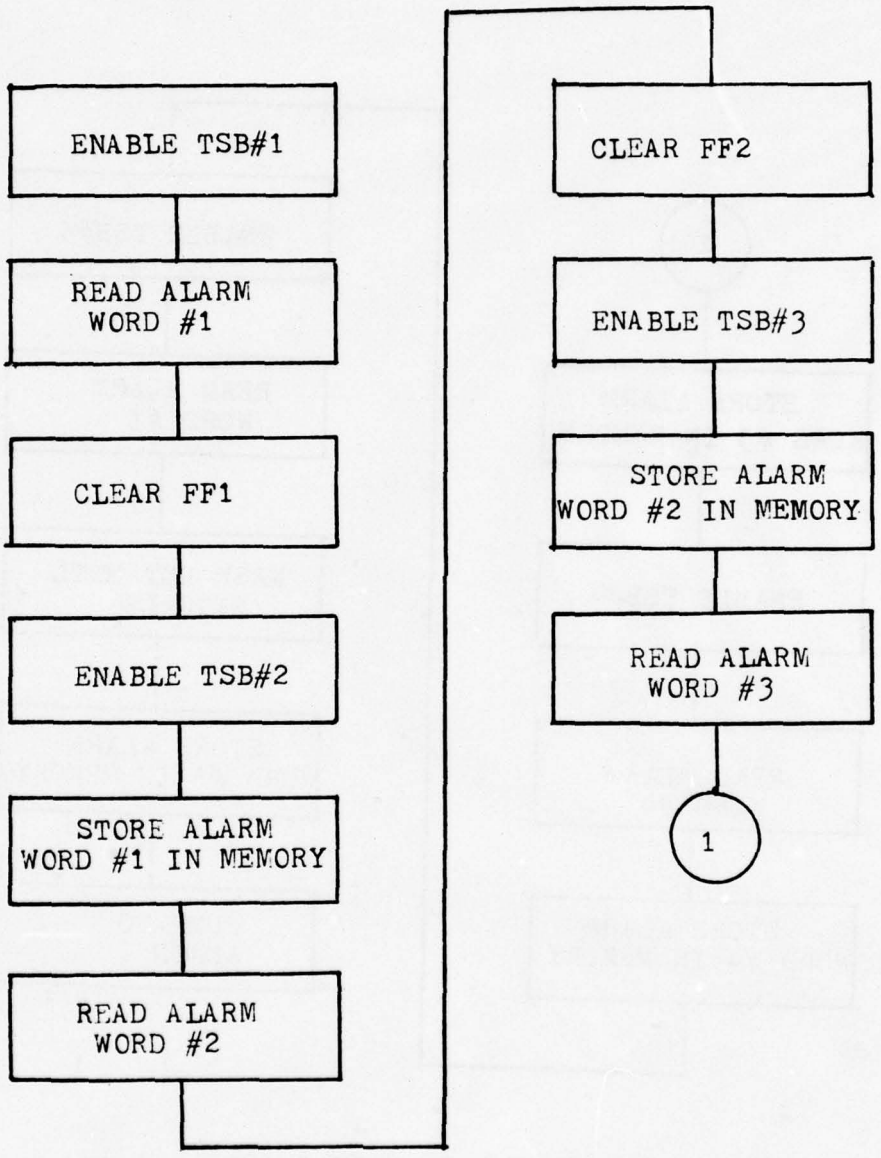
The flowchart given in Figure 3-10 describes the operation of the interface. The corresponding MC6800 assembly program is presented in Appendix B1.

3.4.2 Fast TTL Interface

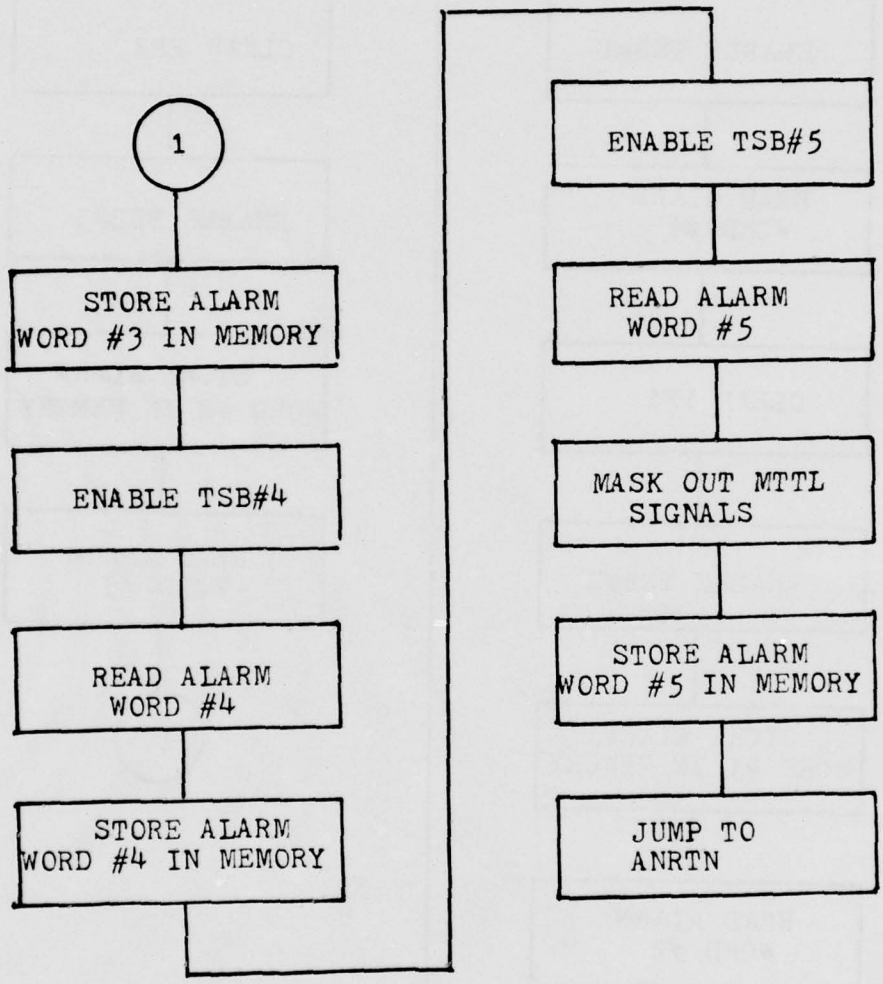
The Fast TTL (FTTL) interface, shown in Figure 3-11, performs the counting function done by the Analog Scanner in ATEC. The FTTL pulses, which are to be monitored by M-ATEC, occur so rapidly that the microcomputer system is unable to count them without some sort of buffering. Consequently, an FTTL interface is needed to count each of the incoming FTTL pulses in separate 8 bit counters and to provide the means by which each of these counters may be periodically queried by the MPU.

The FTTL interface counts pulses on four separate FTTL lines using four eight-bit counters. Periodically, at the request of the time base generator, a device which will be discussed in Section 3.4.5, the microprocessor is interrupted and control is transferred to a routine which reads one of the four counters. After the counter is read by the MPU, the counter is cleared and the interrupt is terminated. Each time the interrupt routine is executed, a different one of the group of four counters is serviced.

The A side output register of PIA#2 (PIA2A) is used to output various control instructions to the interface. The B side output register of PIA#2 (PIA2B) is used to receive the data from the counters.

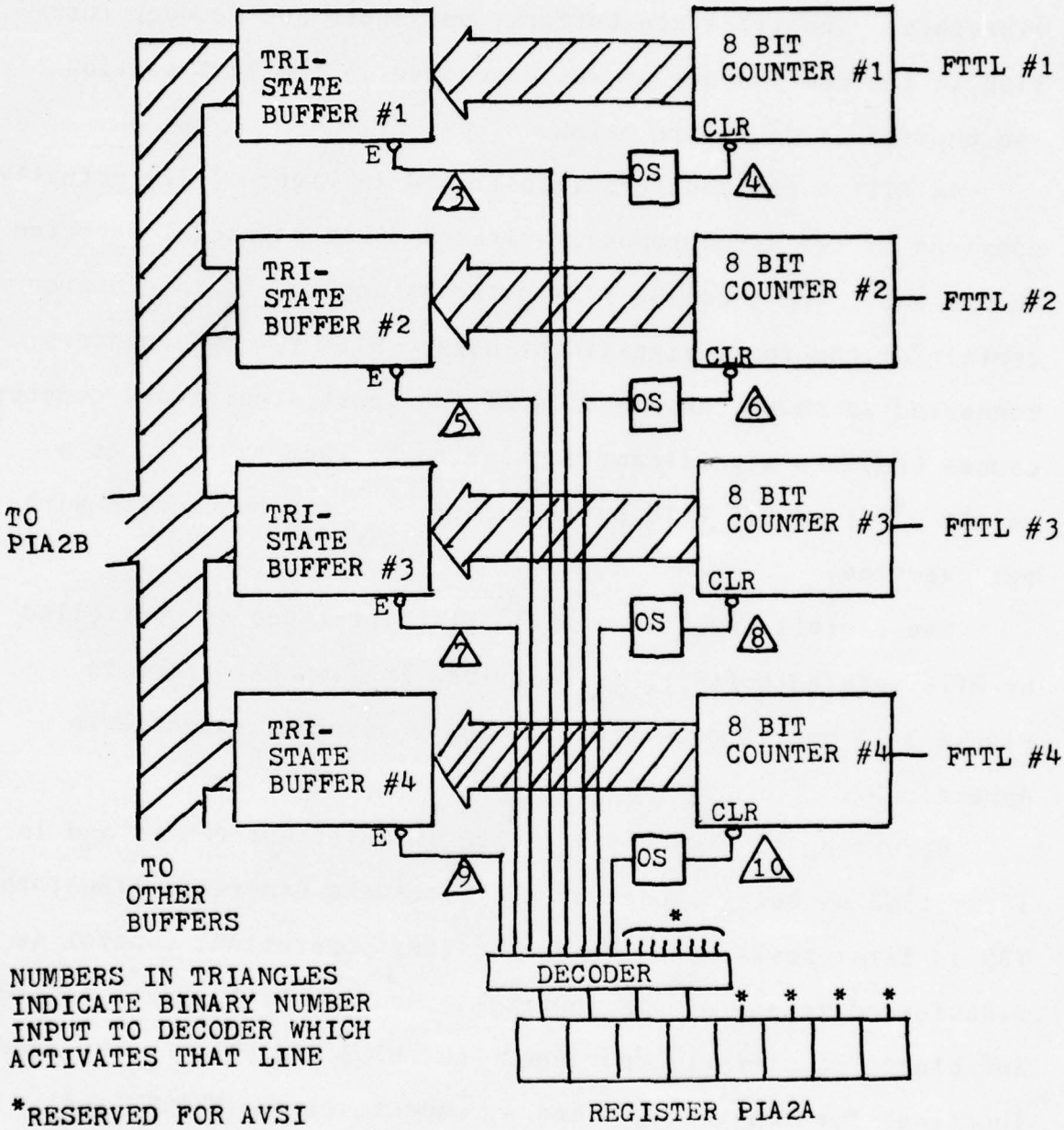


CC/STTL FLOW CHART
FIGURE 3-10(a)



CC/STTL FLOW CHART
(CONTINUED)

FIGURE 3-10(b)



FAST TTL INTERFACE

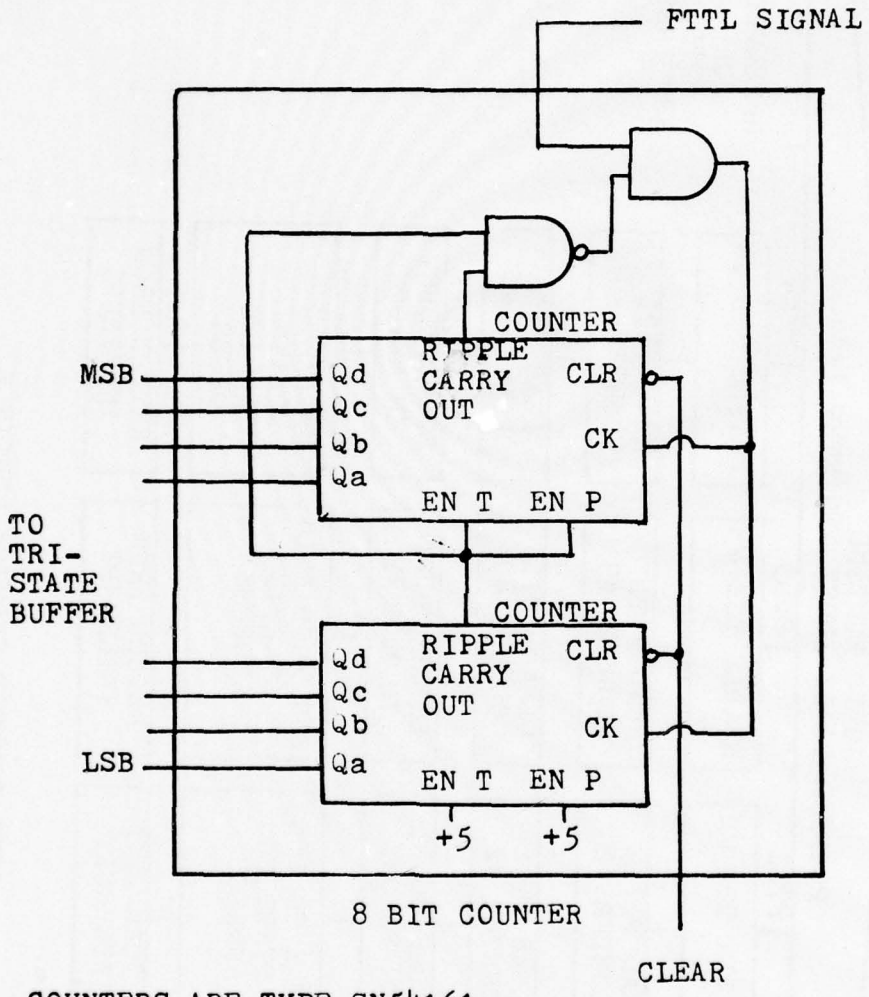
FIGURE 3-11

The interface is constructed of four types of devices: tri-state buffers, counters, a decoder and one shot multivibrators. The tri-state buffers, one shots and decoder function in the same manner as was described in the last section. The counter is described below.

An FTTL 8 bit counter, illustrated in Figure 3-12, actually consists of two asynchronously cleared 4 bit counters connected in cascade. The incoming FTTL pulse is applied to the counter containing the least significant bits. With the two counters connected as shown, an overflow of the least significant counter causes the more significant counter to be incremented. As a result 2^8 -1 or 255 FTTL pulse occurrences may be counted without overflow.

The overall operation of the FTTL interface as controlled by FTTL-related software is described in flowchart form in Figure 3-13 and is presented in MC6800 assembly language in Appendix B2.

Referring to Figure 3-13, when an interrupt occurs and is identified as being caused by the Time Base Generator (TBG), the TBG is first reset. Following the reset operation, control is transferred to one of six routines. Routine FTL1 reads, records, and clears counter #1; routines FTL2, FTL3 and FTL4 do the same functions for counter 2, 3 and 4 respectively. (MTL1TM and MTL2TM are reserved for purposes to be described in Section 3.5.1). Each time the TBG interrupts, a different one of the six routines is executed on a rotating basis.

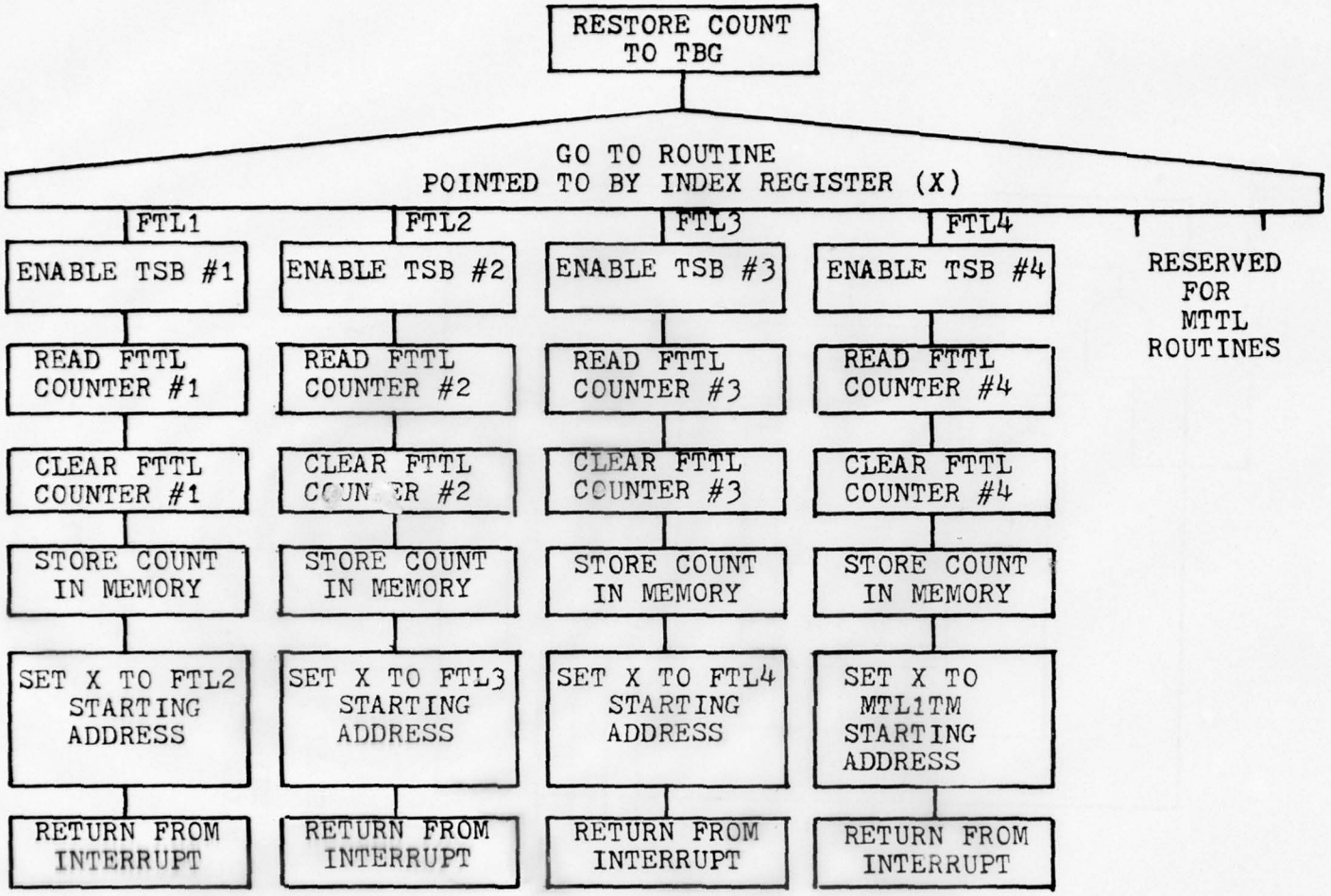


COUNTERS ARE TYPE SN54161

GATES INHIBIT FURTHER COUNTING
ONCE MAXIMUM COUNT IS REACHED

SAMPLE FTTL 8 BIT COUNTER

FIGURE 3-12



FTTL COUNTER SERVICE ROUTINES

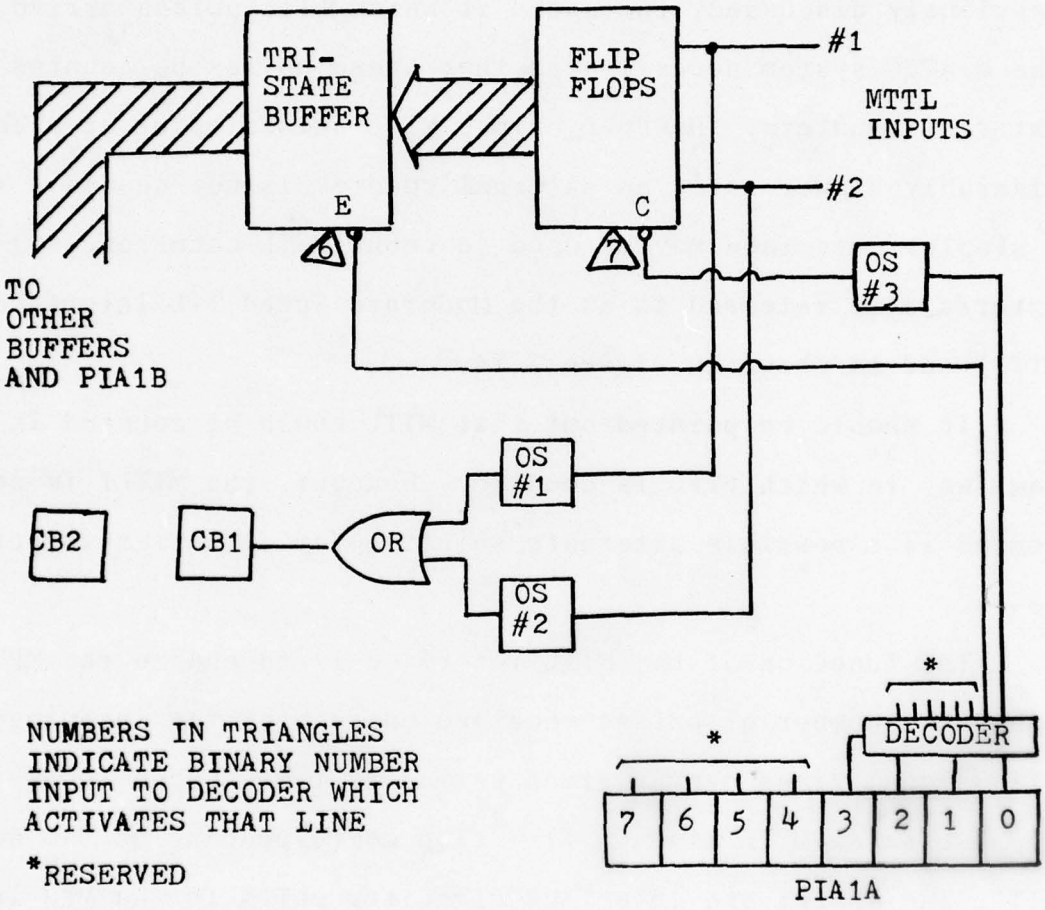
FIGURE 3-13

3.4.3 MTTL Interface

In FKV there are two types of TTL pulses that need to be counted, Fast TTL (FTTL) and Moderate Speed TTL (MTTL). As was previously discussed, the speed at which FTTL pulses arrive at the M-ATEC system necessitates that these pulses be counted in external counters. However, since MTTL pulses occur at a considerably slower rate, an external counter is not needed. Thus, a simpler interface may be used to count MTTL occurrences. This interface is referred to as the Moderate Speed TTL Interface or MTTLI and is shown in Figure 3-14.

It should be pointed out that MTTL could be counted in the same way in which FTTL is counted. However, the MTTLI is presented as a possible alternate solution for illustrative purposes.

The function of the MTTL interface is to enable the MPU to count the number of pulses received on each of two incoming MTTL signal lines over a given period of time. Upon receipt of a pulse on an MTTL line, a flip flop corresponding to the active MTTL line is set and interface circuitry calls for an MPU interrupt. When an interrupt occurs, the microprocessor identifies the line on which the pulse was received by reading the state of the flip flops. The MPU then increments a counter in memory corresponding to the active MTTL line. To record the number of MTTL pulses arriving in a certain period, the MPU, at precise time intervals, transfers the current value of each MTTL count to another memory location for storage and resets the current



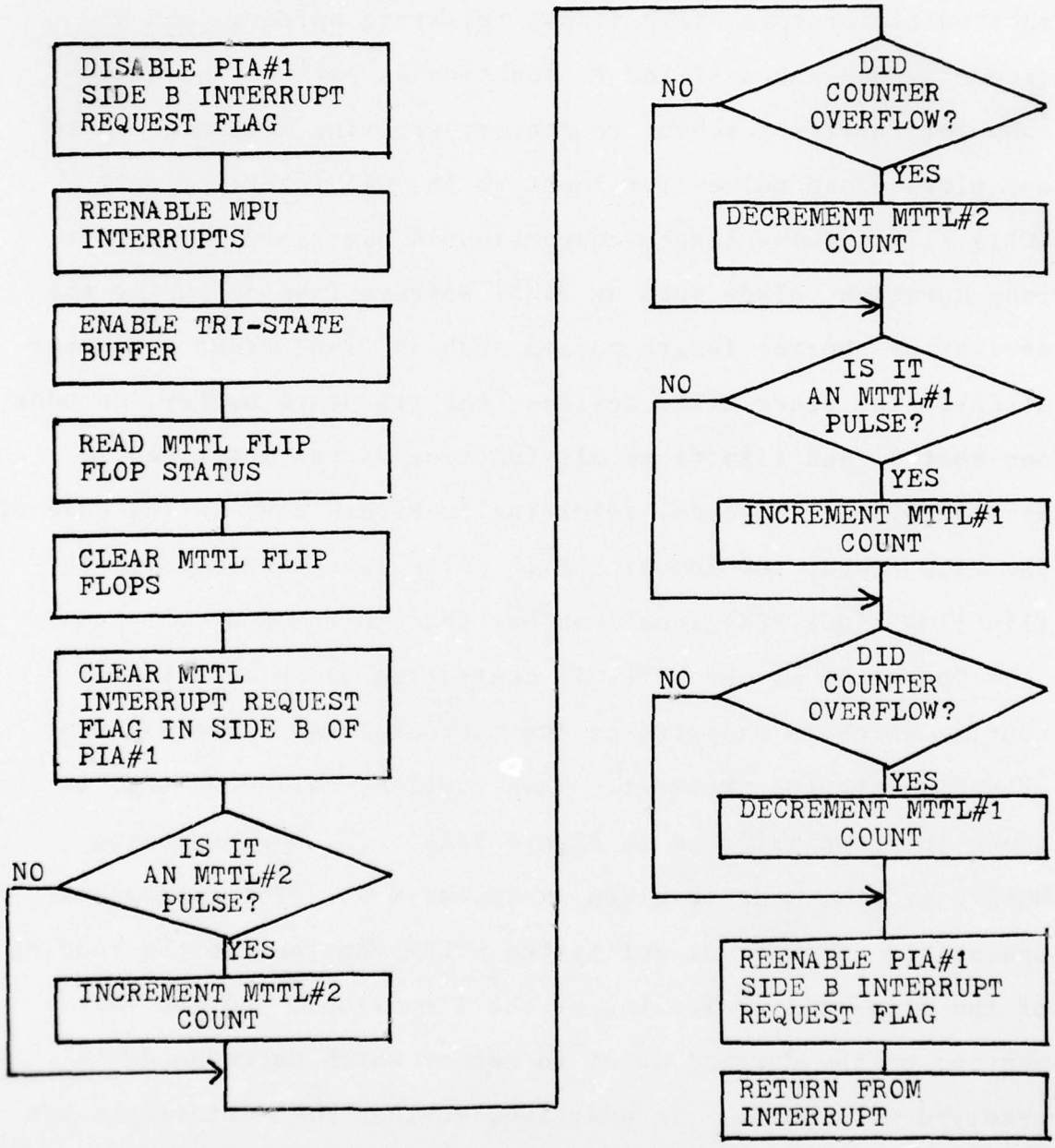
MODERATE SPEED TTL (MTTL)
INTERFACE

FIGURE 3-14

count to zero.

The MTTLI is composed of four major types of devices: one-shot multivibrators, flip flops, tri-state buffers, and a decoder. One-shots #1 and #2 function as part of the microcomputer interrupt scheme to convert arriving MTTL signals to one microsecond pulses for input to the PIA interrupt port (CB1). This pulse length conversion is necessary to prevent long duration pulses such as T1WB1 Reframe from obscuring the arrival of shorter length pulses such as T1WB1 Frame Bit Error at CB1. The other MTTLI devices, the tri-state buffer, decoder, one-shot #3 and flip flops all function as was described in Section 3.4.1. However, referring to Figure 3-9, in the case of the flip flops, the incoming MTTL pulses are connected to the flip flop clock (CK) inputs rather than to the X or Y inputs.

Operation of the MTTLI is controlled by an interrupt routine which is executed by the microprocessor after receipt of a PIA interrupt request. This routine, called MTTLSR, is shown in flowchart form in Figure 3-15. The corresponding MC6800 program code is given in Appendix B3. The fundamental operations which occur during the MTLSR routine are the reading of the flip flops, clearing of the flip flops, and the incrementing of the current count in memory which corresponds to received MTTL pulse. In addition, further MTTL interrupts are inhibited at the outset of the routine and reenabled at the conclusion of the routine. The purpose of this is twofold. First, it allows the MPU interrupt system to be reenabled



MTTL SERVICE ROUTINE (MTLSR)
FIGURE 3-15

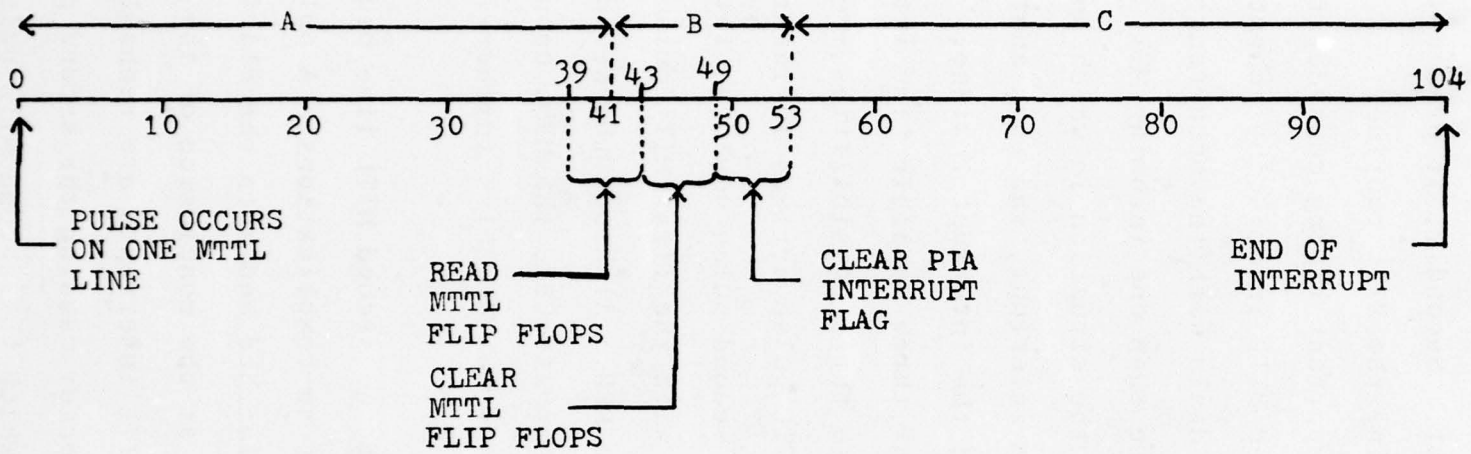
without having the still-present MTTL interrupt flag cause a second false interrupt. Secondly, it prevents another MTTL pulse from interrupting the MTTL routine.

There are two important timing considerations to be made regarding the proposed MTTL interfacing scheme. The first of these considerations deals with the occurrence of near-simultaneous pulses on more than one incoming MTTL line. Specifically of interest is the situation in which an MTTL signal arrives and causes an interrupt, and then another MTTL line becomes active during the interrupt routine. The second pulse might arrive in one of three possible time intervals as shown in Figure 3-16. These three possibilities are discussed below.

If the second MTTL pulse arrives in interval A, no complications result. The second pulse would be latched by the flip flops and read along with the first MTTL pulse when the flip flops are read by the MPU. Although the second arrival of an MTTL signal will reactivate CB1, the MPU, upon entering the interrupt handling routine, disables further interrupts from being recognized.

In the case that the second MTTL line becomes active in interval C, there are no complications. A pulse occurring in this time period is latched and sets the PIA interrupt request flag. Consequently, at the conclusion of the current MTTL interrupt routine, MTTL interrupts are reenabled, and another MTTL interrupt will occur causing the second pulse to be read.

In the case in which the second MTTL pulse arrives during



POSSIBLE TIMES OF ARRIVAL
FOR MULTIPLE MTTL PULSES

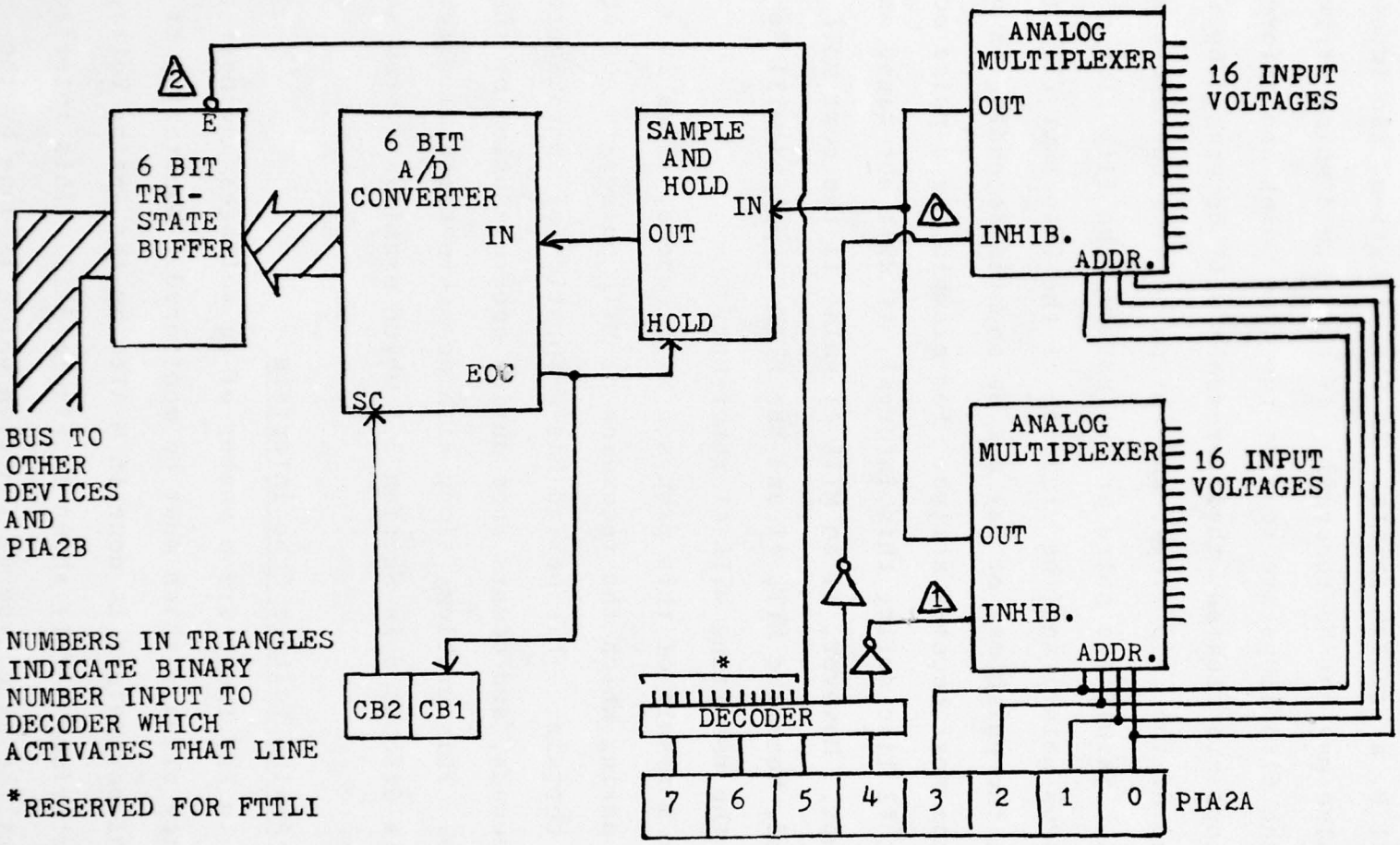
FIGURE 3-16

interval B, a problem exists. In the situation, the incoming MTTL pulse may not be recorded. If the second pulse arrives after the flip flops are read at the 41μs point and before the flip flops are cleared, their presence will be erased by the clearing of the flip flops, and the pulse will therefore not be counted. Should the pulse arrive between the flip flop clearing time (49μs point) and the clearing of the interrupt flag (53μs point), the pulse may or may not be counted depending on which MTTL line next becomes active. For example, if a pulse occurs on MTTL #2 line during this interval, it will not cause an interrupt. However, if an MTTL #1 pulse is the next MTTL signal received, both the MTTL #1 and the MTTL #2 pulses will be read during the resulting MTTL #1 interrupt.

As a result of this proposed MTTL scheme, there is a time period during which the recording of MTTL pulses is not absolutely certain. This period has a duration of approximately 12 microseconds, and occurs once during each execution of the MTTL routine. This problem, along with possible remedial alternatives is discussed in Section 3.5 which examines system software.

3.4.4 Analog Voltage Scan Interface

In FKV there are a number of dc voltages and near-zero frequency signals which must be monitored. Monitoring of these types of parameters is done in M-ATEC by the Analog Voltage Scan Interface (AVSI) shown in Figure 3-17. This interface performs the same type of function which is done by the



ANALOG VOLTAGE SCAN INTERFACE

FIGURE 3-17

MAC/Analog Scanner combination in ATEC. The Analog Voltage Scan Interface accepts up to 32 dc or near-dc voltage inputs and, in sequence, selects a particular input voltage, performs an analog to digital conversion and sends the digital representation of the voltage level to the PIA for input to the microprocessor.

The A side of PIA2 serves to emit control signals to the devices on the interface; the B side of the PIA reads the result of the A/D conversion. Control ports CB1 and CB2 monitor and control the analog to digital conversion process.

The interface contains five major types of devices which may be described as follows.

Analog Multiplexer. This device accepts up to 16 voltage signals, and in accordance with the digital address code applied to its address inputs, connects one of the 16 input signals to its output terminal.

Sample and Hold Module (SHM). The SHM normally allows voltages at its input terminal to pass to its output terminal. However, when the SHM Hold input is brought to a high TTL level, the voltage present at the SHM output port will cease following the input and will be held constant. This is done to insure that the A/D converter receives a constant voltage during the A/D conversion process. When the SHM Hold input is returned low, the SHM ouput voltage will once again follow its input voltage.

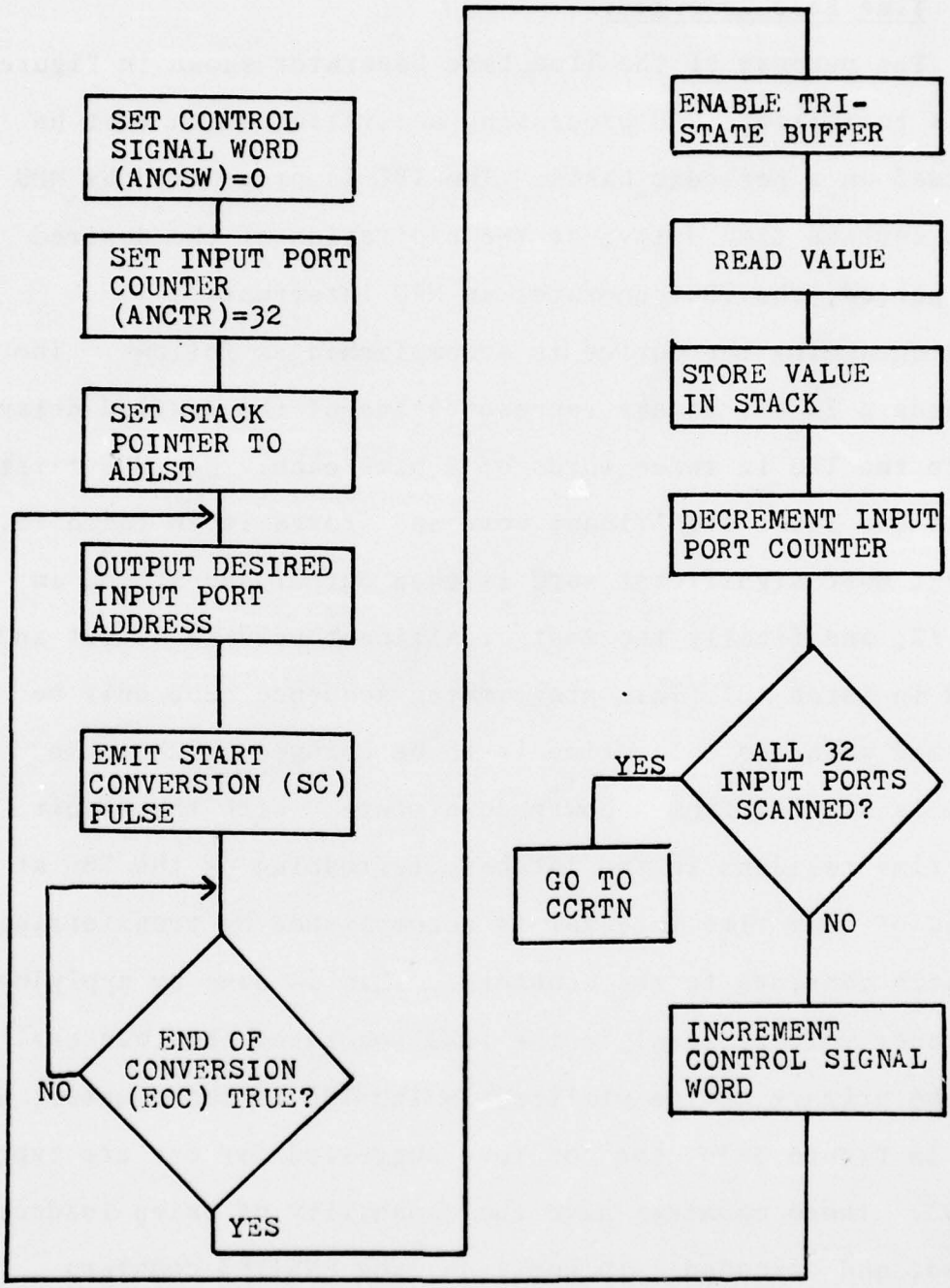
Analog to Digital (A/D) Converter. The function of the

A/D module is to determine the value of the voltage present at its input terminal and output a binary number representing the input voltage value. The microprocessor initiates the conversion process by emitting a pulse from CB2. This causes the EOC output of the A/D module to go high, thereby placing the Sample and Hold in its hold mode. At the same time, the A/D conversion process begins. When the conversion is completed, the A/D module returns EOC to a low state, thereby returning the Sample and Hold to its normal state and causing a negative transition to be sent to CB1. This negative transition on CB1 indicates to the microprocessor that the conversion is complete. Consequently, the microprocessor enables the six bit tri-state buffer and reads the binary value from the A/D into memory.

Tri-State Buffer and Decoder. These devices function as previously described in Section 3.4.1.

The operation of the Analog Voltage Scan Interface is described in flowchart form in Figure 3-18. The AVSI control program is shown in MC6800 assembly language in Appendix B4.

Referring to Figure 3-18 the control word, ANCSCR, is that word output to PIA2A which causes the generation of various control signals on the AVSI. The input port counter, ANCTR, counts down as each input port is scanned and causes an exit from the routine after the last input signal has been serviced. The memory list pointer points to those successive locations in memory in which the value of each input signal is to be stored.



CONTROL SIGNAL WORD IS THE BINARY NUMBER SENT TO THE DECODER

ANALOG VOLTAGE SCAN ROUTINE

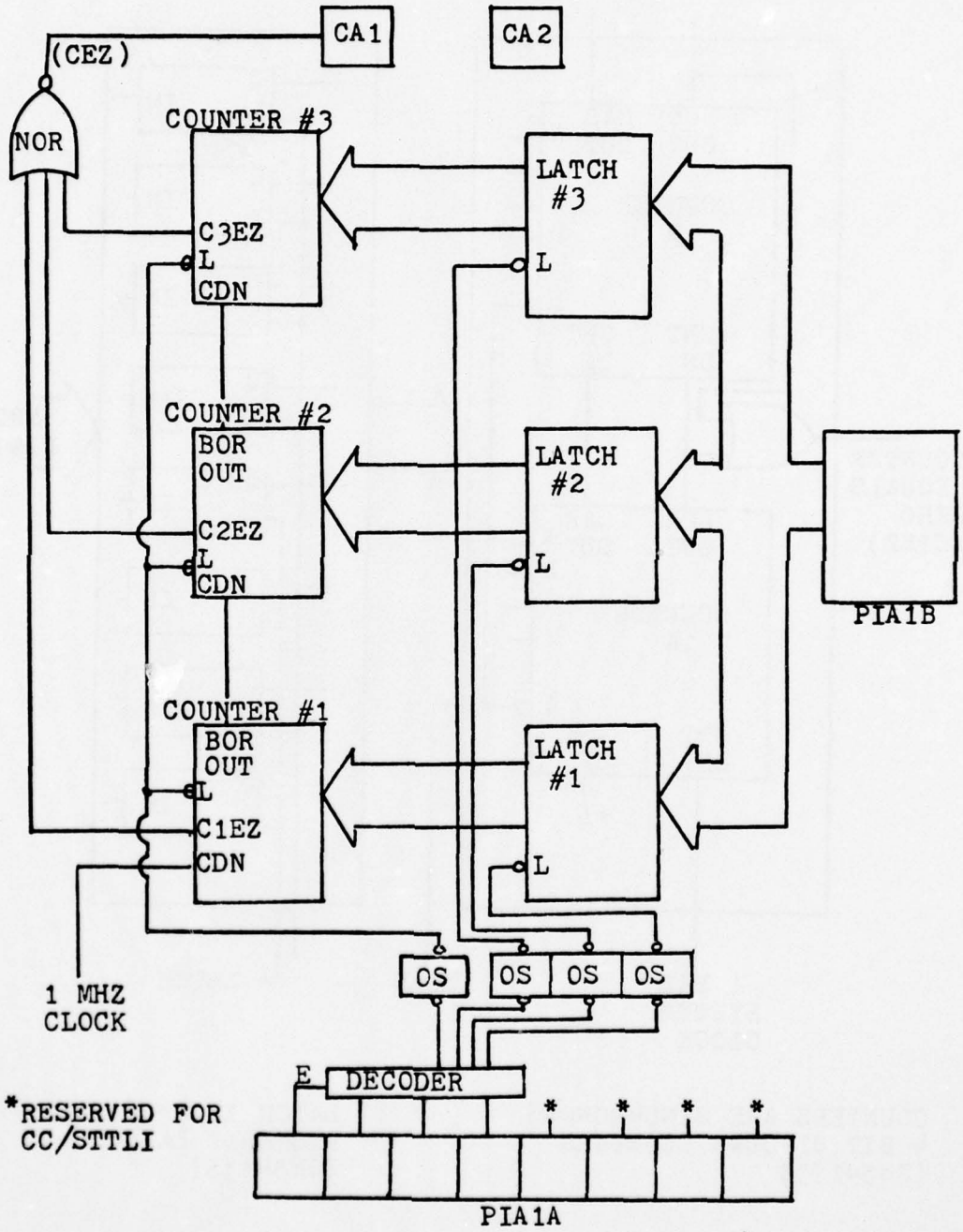
FIGURE 3-18

3.4.5 Time Base Generator

The purpose of the Time Base Generator shown in Figure 3-19 is to initiate MPU processing activities which must be performed on a periodic basis. The TBG is programmed by MPU to have a certain time delay; at the expiration of the desired delay period, the TBG generates an MPU interrupt.

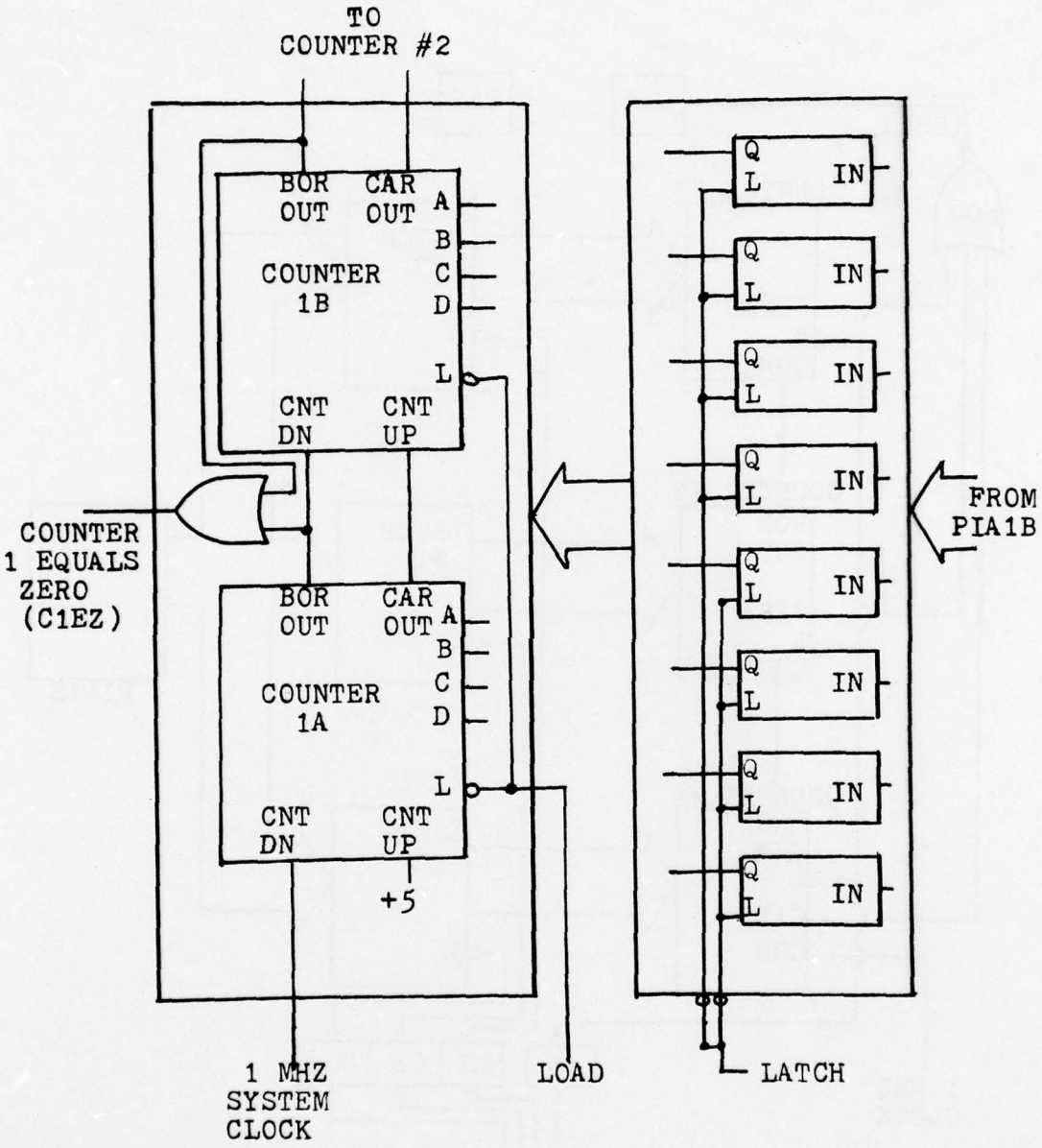
Programming the device is accomplished as follows. The MPU sends a 24 bit binary representation of the desired delay time to the TBG in three words of 8 bits each. The MPU first outputs the least significant word and stores it in latch #1; the next most significant word is then output and stored in latch #2, and finally the most significant word is output and stored in latch #3. This programming sequence need only be performed when the delay time is to be changed or when the system is started from a power down state. With the 24 bit delay time resident in the latches, refreshing of the TBG at the end of each time interval is accomplished by transferring the latch contents to the counters. This is done by applying the proper voltage level to the load inputs of the counters.

The primary device utilized in the TBG is the counter; as shown in Figure 3-20, the counters suggested for use are type SN54193. These counters have the capability of being loaded, cleared, and cascaded. In addition, the SN54193 counters output a borrow out signal which goes true when the count equals zero. The borrow out signal is used for two purposes. First, it is used to cascade the counters, and secondly the



TIME BASE GENERATOR (TBG)

FIGURE 3-19



COUNTERS ARE SYNCHRONOUS
4 BIT UP/DOWN COUNTERS
(SN54193)

LATCH IS AN 8 BIT
BISTABLE LATCH
(SN54116)

TBG COUNTER #1 AND LATCH #1

FIGURE 3-20

borrow out signals from each of the three counters are gated together to form a signal (CEZ) which indicates that the 24 bit count is equal to zero. The CEZ signal is sent to CA1 and causes an interrupt when true.

A flowchart which illustrates the programming sequence for the Time Base Generator is given in Figure 3-21. This sequence is coded in MC6800 assembly language in Appendix B5.

3.4.6 Overall Interface Hardware Configuration

Shown in Figures 3-22 and 3-23 is the configuration of the various M-ATEC interfaces, the Time Base Generator, and the four PIA registers. Two PIAs are used. The TBG, MTTL and CC/STTL devices communicate with the MPU via PIA1; the FTTL and analog scan interfaces communicate with MPU via PIA2.

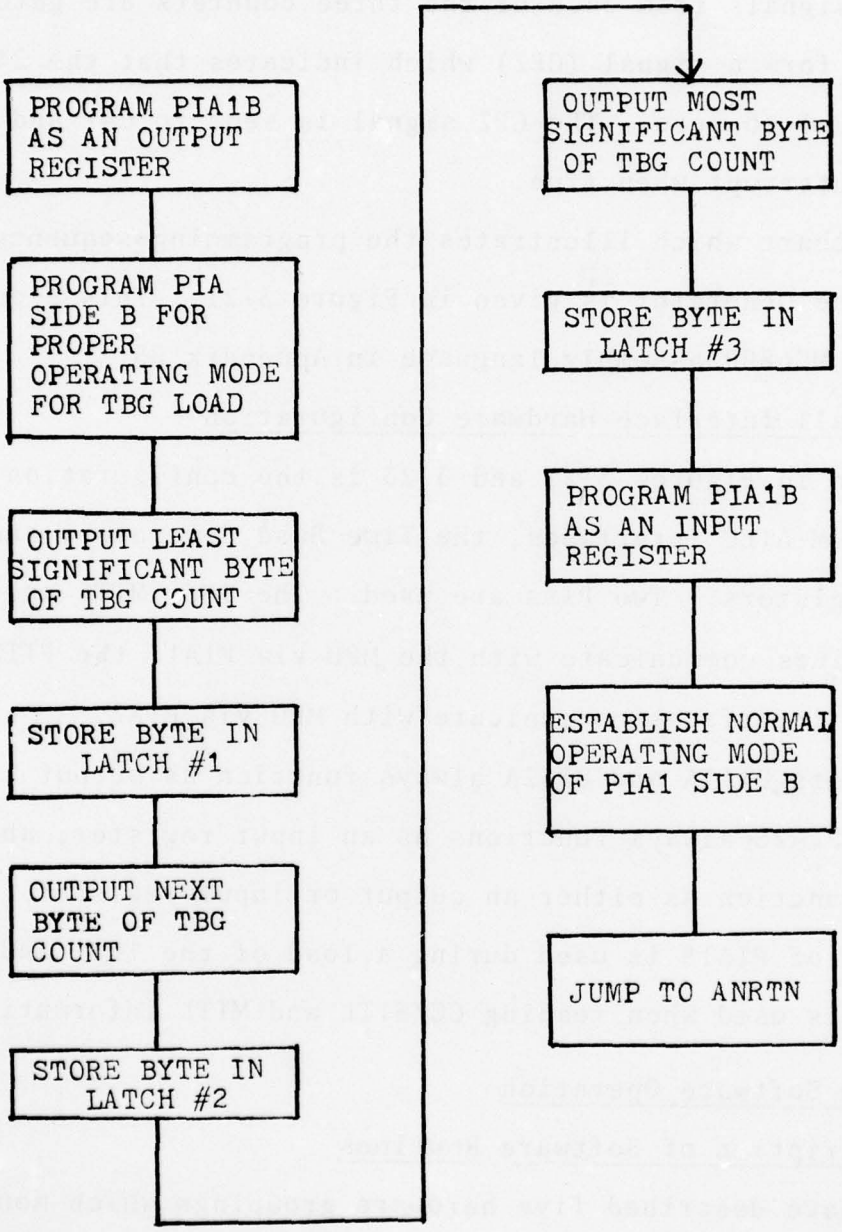
Registers PIA1A and PIA2A always function as output registers; PIA2B always functions as an input register, and PIA1B may function as either an output or input register. The output mode of PIA1B is used during a load of the TBG, and its input mode is used when reading CC/STTL and MTTL information.

3.5 System Software Operation

3.5.1 Description of Software Routines

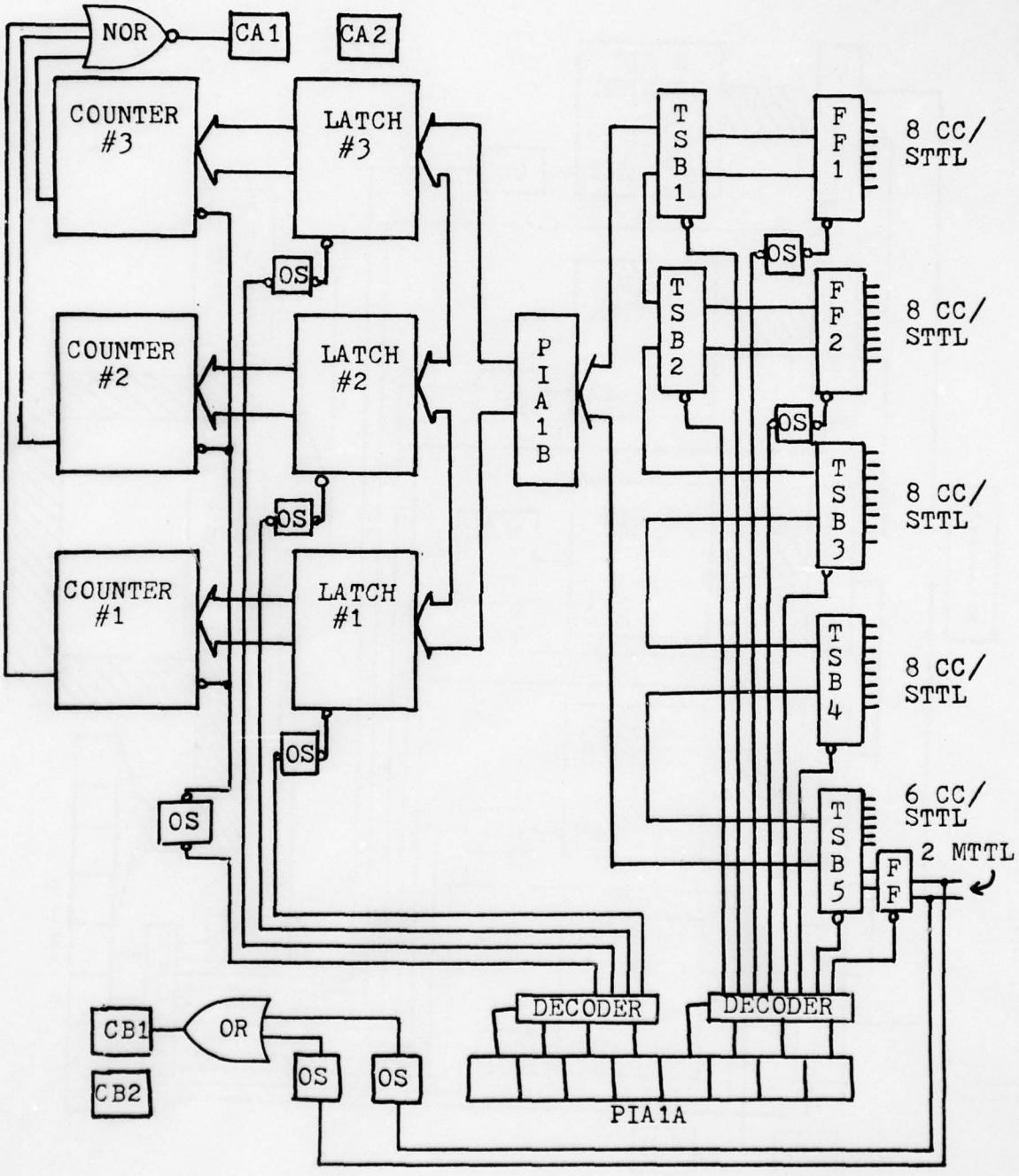
We have described five hardware groupings which monitor the various FKV alarms and parameters and generate an MPU time base. These devices are controlled by the software routines described below.

Analog Scan Routine (ANRTN). This routine controls the Analog Voltage Scan Interface and regulates voltage scanning,



TIME BASE GENERATOR LOAD NEW COUNT ROUTINE (TBGLNC)

FIGURE 3-21



DEVICES SERVICED BY PIA#1
(CC/STTL, MTTL, TBG)

FIGURE 3-22

AD-A042 145 PURDUE UNIV LAFAYETTE IND SCHOOL OF ELECTRICAL ENGI--ETC F/G 9/2
MICROPROCESSOR UTILIZATION IN COMMUNICATIONS SYSTEM MONITORING.(U)
JUN 77 J J KIRBY, R A MEYER, S C CRIST F30602-75-C-0082
UNCLASSIFIED RADC-TR-77-218 NL

2 OF 2
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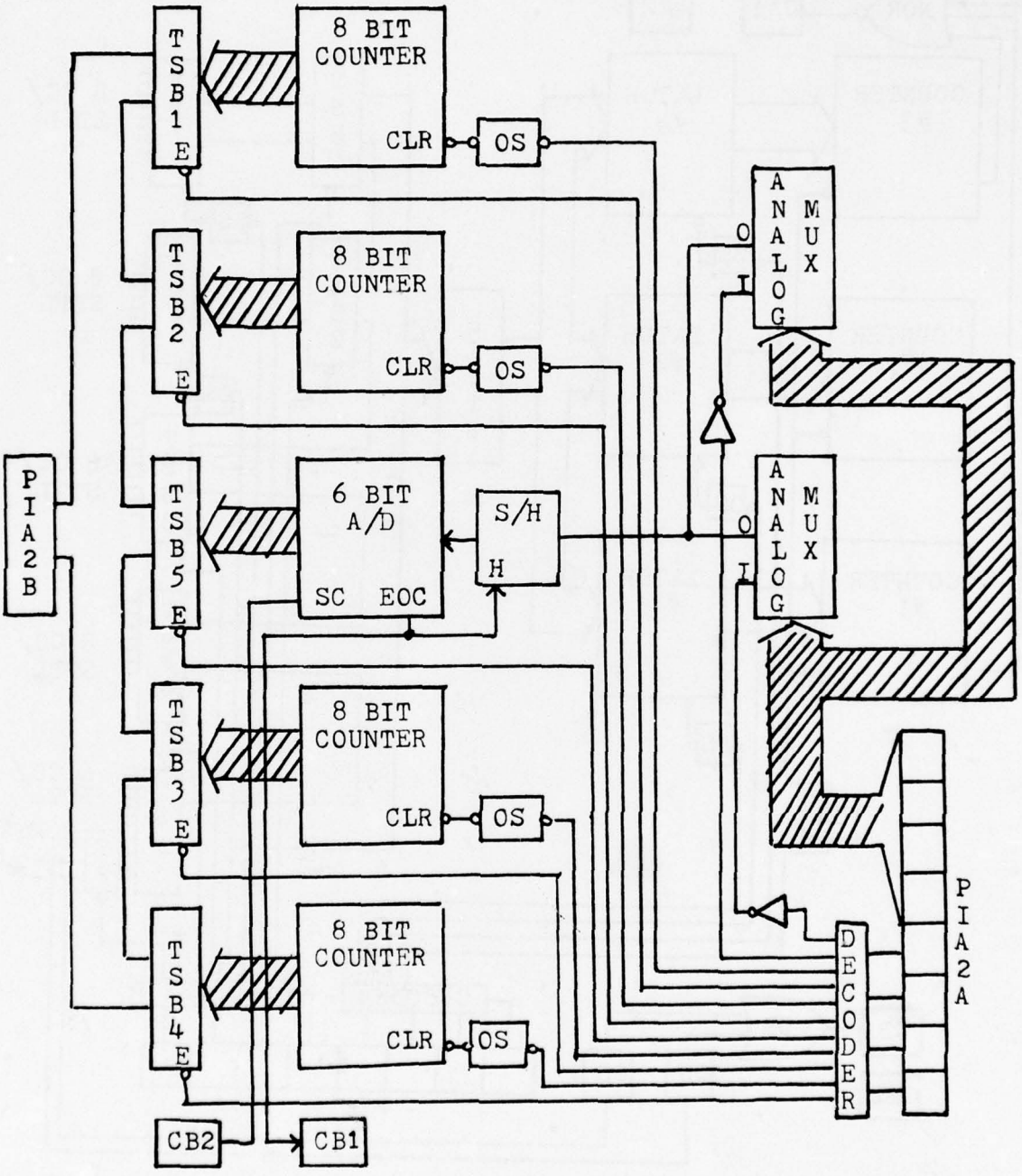


DEVICES SERVICED BY PIA#2
(FTTL, ANALOG)

FIGURE 3-23

A/D conversion, data input and data storage.

Contact Closure/Slow TTL Scan Routine (CCRTN). The CCRTN routine reads the contact closure/slow TTL alarm states which are sent to the CC/STTL interface and stores the resulting data in five 8 bit words.

Medium Speed TTL Service Routine (MTLSR). This interrupt routine provides for the detection and counting of MTTL pulses which arrive at the MTTL interface.

Fast TTL Counter Service Routines 1 thru 4 (FTL1, FTL2, FTL3, FTL4). Each of these routines services a particular counter on the FTTL interface. Execution of one of the routines causes the MPU to read a counter, store the counter contents in memory and clear the counter. Program FTL1 services FTTL counter #1; program FTL2 services FTTL counter #2, etc.

MTTL#1 Count Transfer Routine (MTL1TM). The MTL1TM program is a periodically executed routine which transfers the contents of the MTTL#1 software counter located in memory to another section of memory. The transferred data represents the number of pulse occurrences recorded over the previous time base interval.

MTTL#2 Count Transfer Routine (MTL2TM). This interrupt routine is identical to MTL1TM except that the MTTL#2 count is transferred.

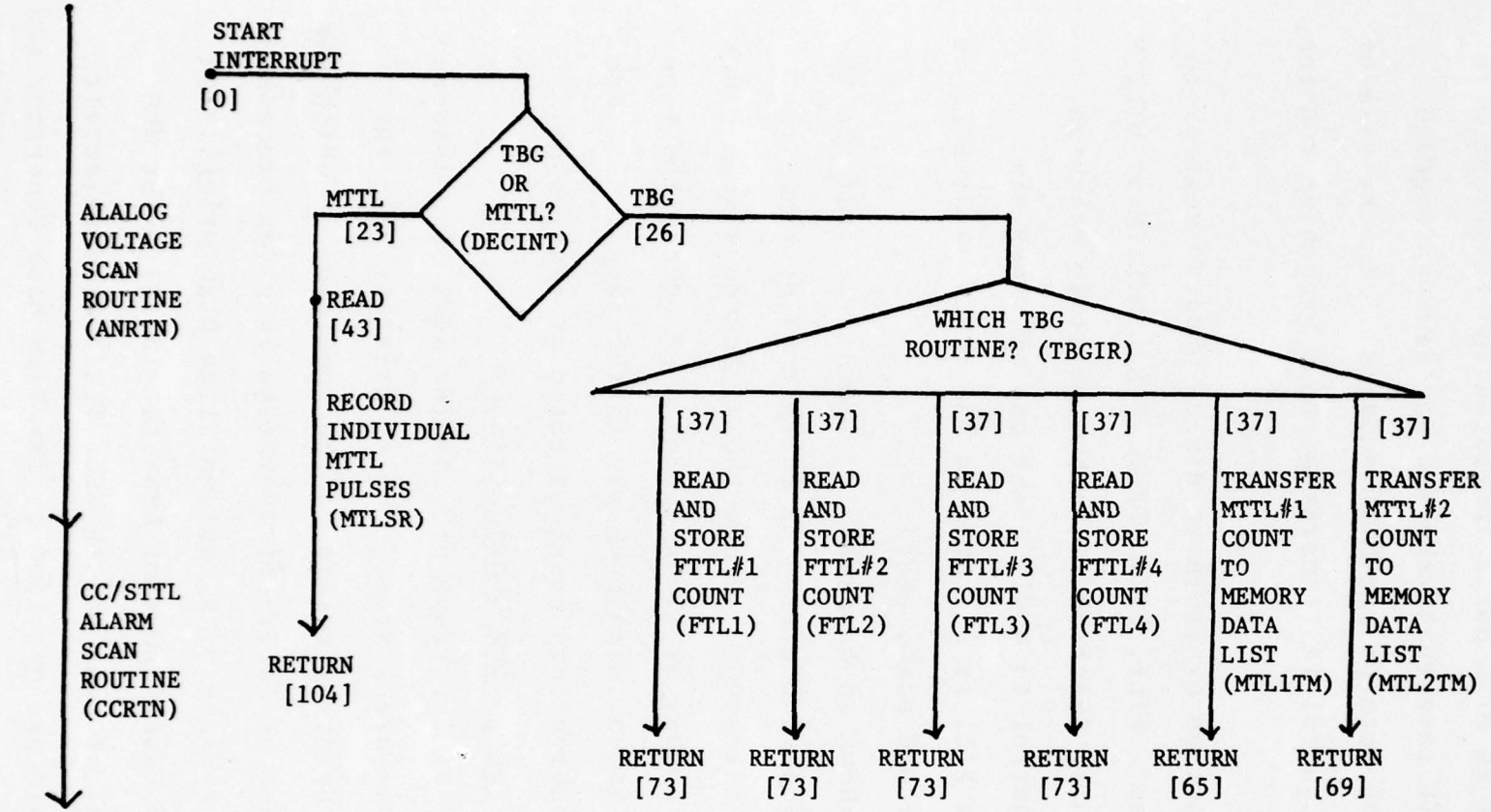
Time Base Generator Load New Count Routine (TBGLNC). The TBGLNC program controls the process of loading a new time base

value into the TBG. This program is executed on an irregular basis.

3.5.2 Program Flow

It is necessary that the individual routines previously described be linked in some manner. This linking is illustrated in Figure 3-24. The routines shown in the figure may be classified as one of two types of programs: main programs or interrupt routines. The main programs are those which are executed when the microprocessor is in its normal or non-interrupted state. These main programs are the Analog Voltage Scan Routine (ANRTN) and the CC[illegible] Scan Routine (CCRTN). The interrupt routines are those which are executed only upon an MPU interrupt condition. Those programs which fall into this category are: MTLSR, FTL1, FTL2, FTL3, FTL4, MTL1TPM and ML2TPM. The Time Base Generator Load New Count Routine (TBGLNC) is a special program executed as part of a system start or system reset routine.

Program flow in the M-ATEC microprocessor may be described in the following way. Referring to Figure 3-24, during its uninterrupted state, the MPU continuously executes ANRTN and CCRTN. Upon receipt of an interrupt signal, if its interrupt system is not disabled, the MPU completes the current instruction and then carries out preparations for interrupt. These preparations include storing the current contents of MPU registers in memory and disabling further interrupts. Program control is then transferred to routine DECINT which determines



- ACTUAL PROGRAM NAMES ARE GIVEN IN PARENTHESES
- NUMBERS IN BRACKETS INDICATE ELAPSED TIME IN MICROSECONDS SINCE RECEIPT OF INTERRUPT (ASSUMING) 1 MHz CLOCK RATE)
- PROCESSING TIME OF ANRTN IS APPROXIMATELY 2439 μs
- PROCESSING TIME OF CCRTN IS 120 μs

SYSTEM PROGRAM FLOW

FIGURE 3-24

whether the TBG or an MTTL pulse initiated the interrupt. In the case of an MTTL interrupt, the MPU proceeds to execute routine MTLSR which records the MTTL pulse(s). In the case of a TBG interrupt, control is transferred to a branching routine, TBGIR.

It is the function of TBGIR to direct program control to one of six routines: FTL1, FTL2, FTL3, FTL4, MTL1TM or MTL2TM which were previously described. Each time it is executed, TBGIR transfers control to a different one of those six routines. Program FTL1 is executed on the first pass; FTL2 is executed on the second pass, etc.

The numbers shown in brackets in Figure 3-24 indicate the number of clock cycles occurring up to that point since the initiation of the interrupt. Since the suggested system clock rate is 1MHz, the number of clock cycles also equals the time in microseconds. Shown in parenthesis in the same figure are the names of the subroutines being executed at that point.

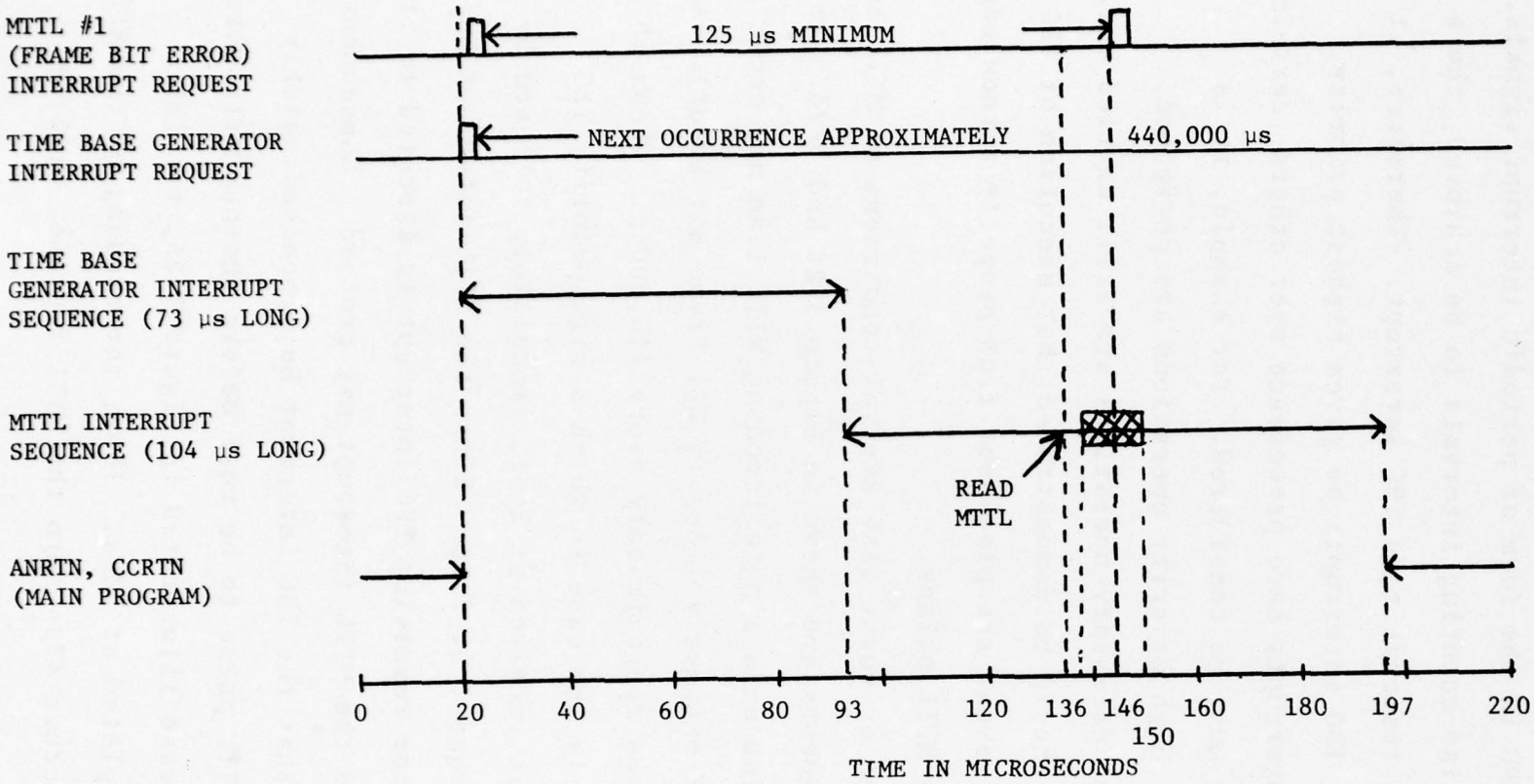
3.5.3 Interrupt Programming Considerations

Two aspects of interrupt programming must be considered in the proposed software system. One is priority, and the other is timing. Priority refers to the condition in which the handling of one type of interrupt operation is given precedence over another. An example of a routine given high priority in M-ATEC is the Time Base Generator Routine (TBGIR). The MPU records the arrival of many pulses over fixed time intervals. These time intervals are provided by the Time Base Generator and

are sent to the MPU in the form of periodic interrupt signals. In order for precise counting intervals to be achieved, there should be a quick response to a TBG interrupt. Therefore, it is necessary that TBG interrupts be given highest priority.

Since TBG interrupts have precedence over others, certain aspects of timing must be considered. For example, it is necessary that if high priority operations are performed, lower priority but necessary operations are still carried out. Specifically, it should be demonstrated that execution of TBG routines do not prevent the processor from properly acknowledging and recording MTTL pulses.

Illustrations of worst case arrival conditions of MTTL and TBG interrupt requests are shown in Figure 3-25 and 3-26. At worst case, a pulse on a single incoming MTTL line may occur at a maximum rate of one every 125μs (T1WB1 Frame Bit Error). A TBG request arrives approximately every 440,000μs. Shown in the first figure is the case in which a high priority TBG interrupt pulse is received at 20μs, immediately followed by an MTTL interrupt request at 21μs. Since the MTTL interrupt has lower priority, the resulting TBG interrupt is executed to its conclusion before the MTTL interrupt may proceed. Consequently, it is important that the TBG interrupt be processed quickly enough for the MTTL pulse to be read before another MTTL pulse occurs. In the case illustrated in Figure 3-25, the TBG interrupt is completed at 93μs. Thus, the reading of the MTTL latches, which occurs 43μs into the MTTL routine, will be

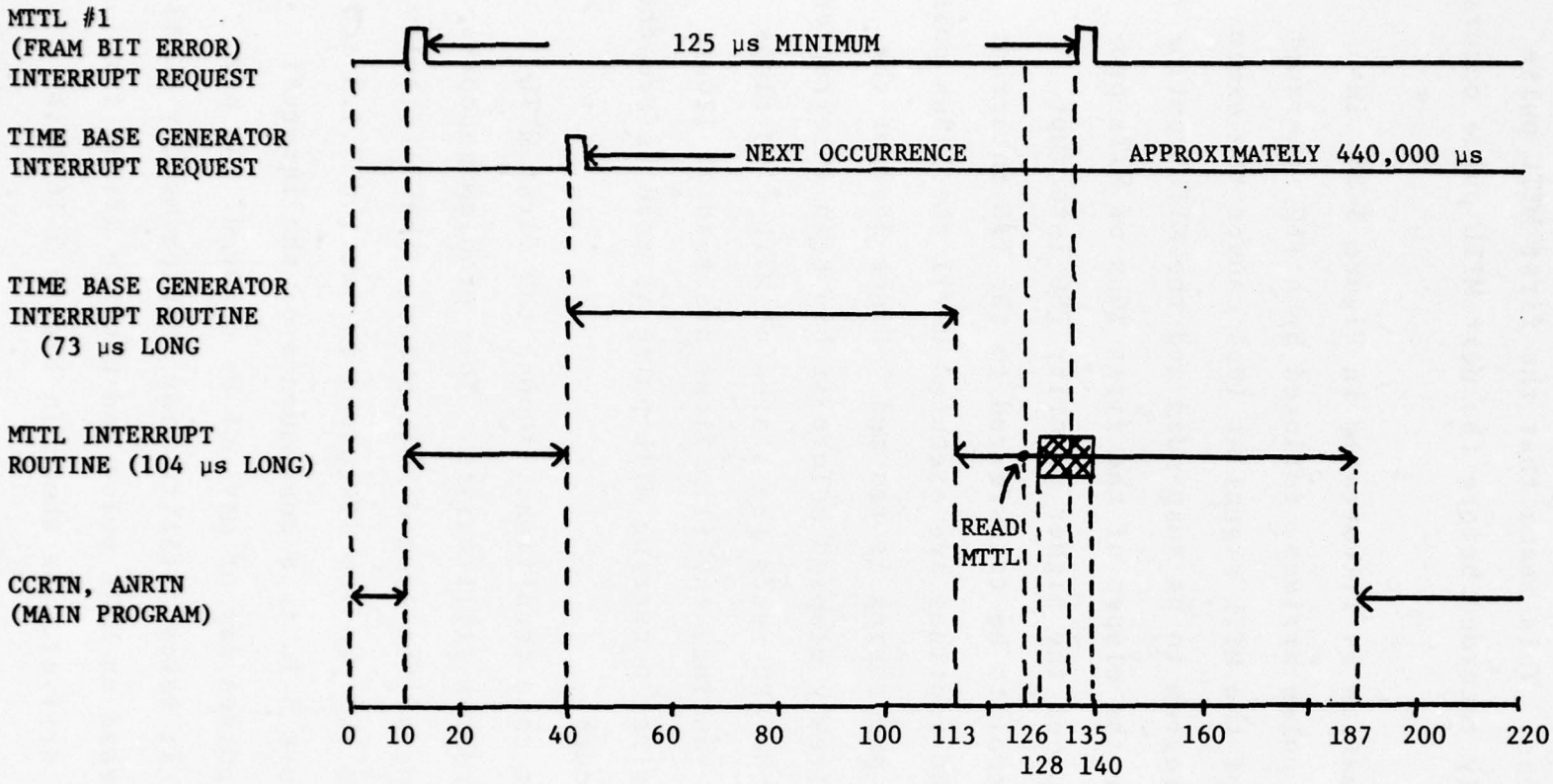


CROSSHATCH INDICATES
READ UNCERTAINTY INTERVAL

READ INSTRUCTION BEGINS AT
136 µs; ACTUAL READING OF
FLIP FLOPS OCCURS AT 138 µs.

INTERRUPT REQUEST ARRIVALS AND
PROGRAM STATUS - MTTL OCCURS
AFTER TBG

FIGURE 3-25



CROSSHATCH INDICATES
READ UNCERTAINTY INTERVAL

READ INSTRUCTION BEGINS AT
126 μs; ACTUAL READING OF
FLIP FLOPS OCCURS AT 128 μs.

TIME IN MICROSECONDS

INTERRUPT REQUEST ARRIVALS AND
PROGRAM STATIS - MTTL OCCURS
AFTER TBG

FIGURE 3-26

accomplished at 136μs. This means that the first MTTL pulse will be successfully recorded before the next MTTL pulse occurs at 146μs.

A similar situation is illustrated in Figure 3-26, in which case an MTTL pulse arrives, followed by a TBG interrupt request. Receipt of the MTTL signal at 10μs causes the execution of the main program to be suspended and the MTTL routine to commence. After the elapse of the first 30μs of MTTL processing, the receipt of the higher priority TBG interrupt request causes control to be transferred to the TBG interrupt routines. The TBG routines are executed until the 113μs point at which time MTTL processing is resumed. Since 30μs of the MTTL routine had already elapsed before it had been interrupted by TBG, and since the MPU reads the states of MTTL flip flops 43μs into the MTTL routine, the flip flops are read at 126μs. Consequently, the first occurring MTTL pulse is read before the next MTTL pulse occurs.

In these worst case conditions, though the first MTTL pulse is read, a problem still exists. This problem concerns the proper recording of the second MTTL pulse. The difficulty, which is related to the problem discussed in Section 3.4.3 and illustrated in Figure 3-16 is a consequence of the interval during which MTTL pulses may or may not be counted. As previously explained, it takes a finite time (approximately 12μs) for the system to read an MTTL pulse and prepare itself for another MTTL pulse arrival. As shown in Figure 3-16 this

period begins two cycles into the read instruction and ends at the conclusion of the clear interrupt flag instruction. In Figure 3-25 this interval extends from 138μs to 150μs, and in Figure 3-26, the corresponding interval is from 128μs to 140μs. In both of these cases, the second MTTL pulse occurs during the 12μs uncertainty period. As a result, this second MTTL pulse may not be recorded properly.

Therefore, considering this situation and the discussion of multiple line MTTL activity in Section 3.4.3, it can be said that the presence of the 12μs uncertainty interval may give rise to problems in two different cases. The first case occurs when the TBG routine interferes with the MTTL service routine, and the second case occurs when an MTTL pulse arrives during the servicing of another MTTL interrupt request. Proposed alterations to the MTTL monitoring strategy, which would improve M-ATEC MTTL monitoring capabilities, are given below.

Problems related to the first case could simply be solved by altering the system clock rate slightly. Referring to Figure 3-25, if the time from the beginning of the TBG routine to the Read MTTL instruction could be reduced, the interval of uncertainty would also be shifted in such a way that it would occur before the next possible MTTL arrival. This reduction in execution time could be attained by increasing the rate of the system clock. A ten percent increase in the clock rate to 1.1MHz would cause the uncertainty interval to terminate at approximately 137μs, meaning that the second MTTL pulse

occuring at 146μs will be properly recorded. It should be pointed out that this solution does not alleviate the problem relating to multiple MTTL line activity.

In the second case, difficulties arise specifically when a second MTTL pulse arrives during the 12μs uncertainty interval of a currently executing MTTL routine. This problem could be eliminated by supplying each incoming MTTL line with a separately cleared flip flop and a separate interrupt request line. In the proposed MC6800 microcomputer system, separate MTTL interrupt capability could be achieved by allowing only one MTTL signal to be connected per each side of a PIA since each side has a separate interrupt request output to MPU.

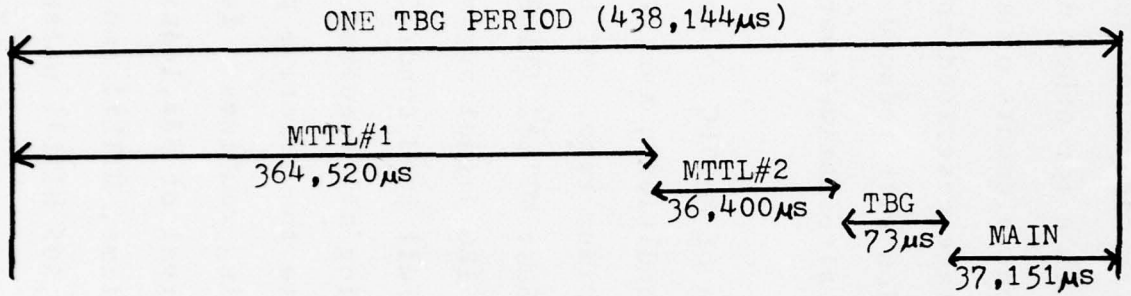
Another solution to the problem illustrated in Figure 3-26 would be to inhibit the servicing of TBG interrupts until after the read uncertainty interval ends, a maximum delay of 57μs. This would cause the uncertainty period shown in Figure 3-26 to terminate at the 67μs point. Such a solution would also eliminate the possibility of another condition occuring, namely, the receipt of a TBG interrupt during the read uncertainty interval. A TBG arrival during that period would cause an extension of the uncertainty interval. It should be pointed out that occasionally delaying the start of the TBG interrupt routine produces an error of 57/440,000 or approximately 0.01% in the time base interval.

A final solution to the MTTL read problem would be to eliminate the MTTL interface and count MTTL in the same way that

FTTL is counted. This would eliminate both the multiple-line MTTL activity problem and the difficulty related to TBG interference of the MTTL routine. It would also significantly reduce the computational load under worst case conditions, thus making available additional processing time for other uses.

All above proposals represent elements of a cost/performance tradeoff. The MTTL interface described in Section 3.4.3 represents an inexpensive solution with reduced capabilities while the three above-mentioned alternatives work more effectively but at higher cost.

A final operating condition of M-ATEC to be considered is its operation under full load conditions, that is, when all pulses are received at their maximum rate. MTTL#1 (T1WB1 Frame Bit Error) is received every 125μs; MTTL#2 (T1WB1 Reframe) is received every 1,250μs, and the TBG signal arrives every 438,144μs. To show that under full load conditions the microprocessor is capable of performing all required processing, Figure 3-27 is used to illustrate the relative processing time requirements of various processing routines. In Figure 3-27, a single time base generator interval of 438,144μs is shown. If it is assumed that during this time, MTTL#1 and MTTL#2 pulses arrive at their maximum rate, 3,505 MTTL#1 pulses and 350 MTTL#2 pulses will occur. Since the processing time for a single MTTL#1 pulse is 104μs and the processing time for a single MTTL#2 pulse is 104μs, the resulting processing time for MTTL#1 and MTTL#2 pulses is 364,520μs and 36,400μs respectively.



RELATIVE TIMES NOT
DRAWN TO SCALE

RELATIVE PROCESSING TIME ALLOCATION
AT WORST CASE INTERRUPT RATE

FIGURE 3-27

Taking into account the 73μs needed to service the single TBG interrupt which occurs during this period, 37,151μs remain available during which the main programs, ANRTN and CCRTN, may be executed. At worst case, the execution time for the main program is 3,403μs. As a result, the main programs are executed at a very satisfactory rate of at least 11 times per 438,144μs or, equivalently, 25 times per second.

3.5.4 Alarm/Parameter Data Storage

As a result of the various scan routines, the collected alarm/parameter data is placed in 43 locations in random access memory (RAM). The structure of the list is illustrated in Figure 3-28. Thirty-two locations ending at address ADLST are reserved for the values of the 32 analog voltages scanned by the Analog Voltage Scan Interface; four locations starting from FTLLST contain the values read from the four FTTL counters during the FTL1, FTL2, FTL3, and FTL4 routines. Contained in the two locations MTLLS1 and MTLLS2 are the counts of pulse occurrences, during one TBG interval, on lines MTTL#1 and MTTL#2 respectively. The five locations beginning with CCLST contain five alarm words of eight bits each. Each bit of an alarm word represents the state of one alarm.

The information in this data list may be directly sent to the Nodal Control Site (NCS) or, what is more desirable, may be first processed by additional software routines and then telemetered to NCS.

LOCATION	CONTENTS
ADLST-31	ANALOG VOLTAGE VALUE #32
ADLST	ANALOG VOLTAGE VALUE #1
FTLLST	FAST TTL #1 COUNT
FTLLST+3	FAST TTL #4 COUNT
MTLLS1	MODERATE SPEED TTL #1 COUNT
MTLLS2	MODERATE SPEED TTL #2 COUNT
CCLST	ALARM WORD #1
CCLST+4	ALARM WORD #5

POST-SCAN MEMORY CONTENTS

FIGURE 3-28

CHAPTER 4

SUMMARY AND CONCLUSIONS

4.1 M-ATEC Capabilities

In summary, the M-ATEC system described in this report illustrates how a microprocessor may monitor the operating performance of the Frankfurt-Koenigstuhl-Vaihingen (FKV) area of the European Defense Communications system. Specifically, M-ATEC monitors various equipment alarms and parameters output by FKV communications devices and stores the monitoring data in the memory of the M-ATEC microcomputer system. The data stored in memory is therefore available for use by additional processing routines or may be telemetered to the central ATEC monitoring site known as the Nodal Control Site (NCS).

The M-ATEC system monitors a number of different signal types; these are Contact Closures (CC), slowly varying analog voltages, Slow TTL (STTL) signals (repetition period greater than one second), Moderate Speed TTL (MTTL) signals (repetition period between 50μs and one second), and Fast TTL (FTTL) signals (repetition period less than 50μs). The state of CC and STTL signals, some of which may be latched, are examined by a periodically executed scanning sequence. Signals of the FTTL type are counted in external counters which are periodically read and cleared by the microprocessor. MTTL signals are counted as they arrive and recorded in software counters internal to the microprocessor.

The M-ATEC system has the capability of accepting up to

38 CC or STTL signals, two MTTL signals and four FTTL signals. At worst case, the status of CC and STTL signals and the values of analog voltages are monitored by the microprocessor approximately every 30 milliseconds. FTTL and MTTL counts are read approximately every 2.6 seconds.

Concerning M-ATEC hardware requirements, the overall proposed M-ATEC system consists of 69 circuit modules. Seven modules comprise the microcomputer system, itself; 35 modules, which are connected to PIA#1, comprise the Time Base Generator and MTTL and CC/STTL Interfaces, and 27 modules, connected to PIA#2, make up the FTTL and Analog Voltage Scan Interface. The modules range in complexity from small scale integration NOR gates to large scale integration devices such as the MPU chip.

4.2 M-ATEC Advantages

With a microprocessor incorporated into the ATEC system at a remote site, various short range and long range advantages may be realized. Examples of some immediate advantages are system programmability, reduced size, reduced power consumption and reduced maintenance.

Programmability of the ATEC system is a result of the fact that a Read Only Memory (ROM) controls system operations. Should a change in the operating sequence of M-ATEC be desired, such a change could be made simply by replacing the present ROM with a new ROM containing the desired program. This is advantageous because a comparable change in a non-microprocessor controlled system would require significant hardware alterations

to be made.

The reduced size and power requirement of M-ATEC is a consequence of M-ATEC's extensive utilization of large scale integration (LSI) technology. Since LSI incorporates a number of discrete devices onto a single chip, size reduction is an automatic result. Also, since the microcomputer chips utilize MOS technology, system power requirements are reduced. The feature of system programmability, also a consequence of the use of LSI, allows many system functions, previously done in hardware, to be done in software. An example of this is M-ATEC's MTTL counting scheme in which a software counter rather than a hardware counter is used to record incoming MTTL pulses. By performing certain functions in software, a number of hardware devices may be replaced by a single memory device which contains an appropriate software routine. As a result additional power and size reduction is realized. It should be pointed out that the future trend of microprocessor technology is toward greater sophistication, higher speed and lower power consumption.

Reduced maintenance is another immediate advantage of the M-ATEC system. Many maintenance problems are related to device interconnection failure. Since the LSI technology used in M-ATEC reduces the number of discrete devices used in FKV monitoring, a reduction in maintenance time and expense should occur.

Various long range advantages may also be realized with the introduction of processing capability at FKV remote sites.

For example, given the development of appropriate software in the future, M-ATEC monitoring sequences could be made adaptive to network conditions existing at a particular moment. Monitoring data could be processed before being telemetered to the remote site, and increased nodal control site-remote site interaction could be made possible. A consequence of making monitoring sequences adaptive and increasing NCS-Remote site interaction would be increased fault isolation and fault detection efficiency. Preprocessing data before transmission to the NCS would reduce telemetry bandwidth and reduce NCS processing requirements. Given a fixed telemetry bandwidth and a fixed NCS processing capability, this would allow more remote sites to be connected to a single nodal control site.

4.3 M-ATEC Limitations

Though the proposed M-ATEC system offers many beneficial features, M-ATEC does have some limitations. First, M-ATEC is limited in the number of asynchronous interrupts it can handle. The fundamental difficulty is time. Since it takes a finite time to process an interrupt and since many interrupt requests must be processed in a limited amount of time, the result is that a microprocessor can process only a limited number of independent interrupt signals. Also, in M-ATEC, since MTTL pulse arrivals are recorded on an interrupt basis, during periods of high MTTL activity, the MPU processing time is almost fully utilized. This means that additional processing routines would require a second microprocessor at the remote site.

Another limitation of the proposed M-ATEC system is that it lacks the displays which are available on digital ATEC devices such as the Alarm Scanner. These displays could, however, be incorporated into the system without major difficulty.

One final limitation of M-ATEC is that, at the present level of design, it does not perform all of these remote site monitoring and switching functions described in the ATEC Digital Adaptation Study. An expansion of M-ATEC to encompass some of these functions is discussed in the next section of this report.

4.4 Future Work

The function of the M-ATEC system proposed in this report is to monitor a number of TTL levels, contact closures and low frequency analog voltages and to store the results of these measurements in the microcomputer memory. Of future concern could be the expansion of M-ATEC monitoring capability and the development of additional system software.

One aspect of M-ATEC monitoring which could be investigated is the addition of voice frequency (VF) monitoring capability. At present, the M-ATEC system has no provisions for the monitoring of FKV voice frequency (VF) signals. However, it is possible for a microprocessor to scan, filter and measure VF signals. Scanning could be accomplished in a manner similar to that used by M-ATEC to scan low frequency analog signals, and filtering could be done internal to the microprocessor by utilizing digital filtering techniques. Since an appreciable amount of processing time is required to perform these

functions, it would be necessary to add a second microprocessor to the system to provide this capability.

Another function which could be incorporated into M-ATEC is control over the breaking, interconnection and termination of VF lines. This is a function performed in digital ATEC by the MAC/Analog Scanner combination.

Development of additional system software would be a particularly worthwhile area of future work. Since the presence of processing capability at remote sites is a significant result of the M-ATEC development effort, the efficient utilization of this capability should be a primary goal. Development of appropriate system software would make it possible to implement a number of valuable functions which were previously mentioned, including: adaptive alarm/parameter scanning, increased NCS-Remote Site interaction, data preprocessing at remote sites, and digital filtering.

APPENDIX A1

T1-4000 ALARMS AND PARAMETERS

1) Major Alarm - An alarm generated when one or more of the following events occurs:
   a) loss of +20VDC power supply
   b) T1-4000 Remote Alarm received. Remote Alarm indicates that a receive T1-4000 has noted that its transmitting counterpart has lost main frame or control frame synchronization for more than 250 milliseconds.
   c) Minor Alarm present. A receive T1-4000 generates a minor alarm if it determines that the three level partial response signal has a format error rate of 10^{-5} or greater.
2) Main Frame Bit Error - A pulse generated by the T1-4000 unit indicating that an incorrect framing bit has been received.
3) Control Reframe - A TTL level which indicates that the receiver has lost control frame synchronization and is attempting to resynchronize.

The following alarms/parameters do not emanate directly from the T1-4000 unit but are related to T1-4000 operation.

4) Maintenance Indicator - A signal (actually a manual switch closure) generated by maintenance personnel to indicate that maintenance relating to the T1-4000 units is in progress.
5) Switch-Major - An alarm, emitted by the T1-4000 switchover unit, which indicates that one or more of the following

conditions exist:

a) A switchover (transfer) attempt from main to standby unit or vice versa has failed.

b) The standby T1-4000 had a local alarm when it was switched on line.

c) A remote alarm has been received.

d) The switch unit is in the standby mode and is thus inoperative.

6) Rx In Service - A TTL level which indicates to the ATEC devices which of the T1-4000 receivers (main or standby) is currently on line.

7) Tx In Service - A TTL level which indicates to the ATEC devices which of the T1-4000 transmitters (main or standby) is currently on line.

It should be noted that there are two each of the following alarms/parameters at VHN: Major Alarm, Main Frame Bit Error, Control Reframe, and T1-4000 Maintenance. One set of alarms/parameters comes from the main (normal) T1-4000 and the other set comes from the standby T1-4000 unit.

APPENDIX A2

T1WB1 ALARMS/PARAMETERS

1) Local Alarm - indicates either of the following conditions exists:
   a) loss of receiver synchronization for more than 5 milliseconds or
   b) failure of the +5v, +12v or +9v power supplies.
2) Loop Alarm - By switch control, the T1WB1 can be operated in such a way that it will immediately re-receive information which it transmits. This is called loopback mode and is primarily used as a maintenance aid. Operating in this way, the T1WB1 is essentially disconnected from the system. To prevent accidental operation of the T1WB1 in loopback mode, an alarm is generated by the T1WB1 when operating in this way.
3) Bipolar Violation Rate Alarm - A signal indicating that bipolar errors in the received T1 format exceed a certain threshold.
4) Fuse Alarm - A signal indicating that a fuse in the -48v power supply has blown.
5) Outgoing Alarm - An alarm, which is sent to a remote T1WB1, indicating that the local T1WB1 has one of the following alarm conditions:
   a) Fuse Alarm
   b) Bipolar Violation Rate Alarm
   c) Local Alarm

d) Loop Alarm.

6) Remote Alarm - indicates that the remote T1WB1 is sending an outgoing alarm.

7) Office Alarm - A consolidated alarm indicating that the local T1WB1 is in one of the following states:

   a) Remote Alarm

   b) Local Alarm

   c) Bipolar Alarm

   d) Fuse Alarm

   e) Loop Alarm

   f) loss of power

   g) outgoing alarm manually disabled.

8) Maintenance Alarm - A signal generated by a switch closure indicating that maintenance is being performed on T1WB1 equipment.

9) Power Supply Voltages - Six of the T1WB1 power supply voltages are monitored.

Of those T1WB1 alarms/parameters mentioned, the following are measured by the ATEC monitoring system:

   a) Office Alarm

   b) Maintenance Alarm

   c) Reframe Signal

   d) Frame Bit Error Signal

   d) Power Supply Voltages.

APPENDIX A3

CY104 ALARMS

1) Remote Alarm - indicates that the CY104 at the other end of the communications link is in a Local Alarm state. A Local Alarm is an indication that a fuse has blown or that there has been a loss of frame synchronization for more than 300 milliseconds.

2) Service Alarm - A combined alarm indicating that the CY104:

   a) is in a Local Alarm state

   b) is in a Loop Alarm state

   c) has lost power

   d) is receiving a Remote Alarm.

APPENDIX A4

RADIO SET ALARMS/PARAMETERS

1) Rx Squelch Alarm - indicates that the received signal level has gone below a preset value.

2) Received Signal Level (RSL) - (Sometimes referred to as Receiver Automatic Gain Control Voltage - AGC). An analog voltage ranging from +2 to +8 VDC which gives an indication of the relative strength of the received signal.

3) Rx Problem - A combined alarm indicating that one or more of the following conditions exist:
   a) Rx Phase Lock Alarm - receiver local oscillator has lost phase lock with reference oscillator.
   b) Rx Pilot Alarm (also called Receive Switch Signal) - received pilot signal has gone below a predetermined threshold.

4) Tx Problem - A combined alarm indicating that one or more of the following conditions exist:
   a) Transmit Power Alarm - transmit power has gone below a predetermined threshold.
   b) XMIT AFC Alarm - Automatic Frequency Control (AFC) voltage is outside of a +5 to +15 volt DC range or phase lock in AFC reference unit is lost.
   c) Transmit Pilot Alarm - transmit pilot level is below a predetermined threshold.

5) Radio Rx Alarm - indicates that both of the following conditions exist:

a) Rx Pilot Alarm (A) - received pilot level in receiver A, the normal receiver, is below a preselected threshold.

b) Rx Pilot Alarm (B) - received pilot level in receiver B, the standby receiver, is below a preselected threshold.

6) Maintenance Indicator A - signal generated by a manual closing of a contact by maintenance personnel indicating that receiver or transmitter A is undergoing maintenance work.

7) Maintenance Indicator B - same as 6 except applies to receiver or transmitter B.

8) Power Supply Voltages - 8 DC power supply voltages are available for external monitoring.

All eight of the just-mentioned alarms/parameter types are monitored by ATEC.

APPENDIX B1

CC/STTL READ ROUTINE

# of Bytes				# of Cycles
2	CCRTN	LDAA #08		2
3		STAA PIA1A	enable TSB#1	5
3		LDAB PIA1B	read alarm word #1	4
3		INC PIA1A	clear flip flop #1	6
3		INC PIA1A	enable TSB#2	6
3		STAB CCLST	store alarm word #1 in memory list	5
3		LDAB PIA1B	read alarm word #2	4
3		INC PIA1A	clear flip flop #2	6
3		INC PIA1A	enable TSB#3	6
3		STAB CCLST+1	store alarm word #2 in memory list	5
3		LDAB PIA1B	read alarm word #3	4
3		STAB CCLST+2	store alarm word #3 in memory list	5
3		INC PIA1A	enable TSB#4	6
3		LDAB PIA1B	read alarm word #4	4
3		STAB CCLST+3	store alarm word #4 in memory list	5
3		INC PIA1A	enable TSB#5	6
3		LDAB PIA1B	read alarm word #5	4
2		ANDB #$CO	mask out MTTL information	2
3		STAB CCLST+4	store alarm word #5 in memory list	5
3		JMP ANRTN	jump to Analog Voltage Scan Routine	3

Symbol Interpretation

PIA1A: Side A Output Register of PIA#1
PIA1B: Side B Output Register of PIA#1
CCLST: first of five memory locations into which the five alarm words are stored

Total Execution Time: 93 cycles

Total Memory Requirements: 58 bytes of ROM
5 bytes of RAM

APPENDIX B2

TIME BASE GENERATOR INTERRUPT ROUTINES

#of Bytes				# of Cycles
2	TBGIR	LDAA	#B0	2
3		STAA	PIA1A reload TBG	5
2		BRA	X	4
3	RFTLX	LDX	*+4 point index register to start of FTL1 routine	3
1		RTI		10
2	FTL1	LDAA	#$30	2
3		STAA	PIA2A enables tri-state buffer #1	5
2		LDAA	#$40 prepare clear signal	2
3		LDAB	PIA2B read in count	4
3		STAA	PIA2A emit clear signal	5
3		STAB	FTLLST store count in memory	5
3		LDX	#*+4 arrange index register so that FTL2 will be executed on next pass	3
1		RTI		10
2	FTL2	LDAA	#$50	2
3		STAA	PIA2A enable tri-state buffer #2	5
2		LDAA	#$60 prepare clear signal	2
3		LDAB	PIA2B read in count	4
3		STAA	PIA2A emit clear	5
3		STAB	FTLLST+1 store count in memory	5
3		LDX	#*+4 arrange index register so that FTL3 will be executed on next pass	3
1		RTI		10
2	FTL3	LDAA	#$70	2
3		STAA	PIA2A enable tri-state buffer #3	5
2		LDAA	#$80 prepare clear signal	2
3		LDAB	PIA2B read in count	4
3		STAA	PIA2A emit clear signal	5
3		STAB	FTLLST+2 store count in memory	5
3		LDX	#*+4 arrange index register so that FTL3 will be executed on next pass	3
1		RTI		10
2	FTL4	LDAA	#$90	2
3		STAA	PIA2A enable tri-state buffer #4	5
2		LDAA	#$A0 prepare clear signal	2
3		LDAB	PIA2B read in count	4
3		STAA	PIA2A emit clear	5
3		STAB	FTLLST+3 store count in memory	5

# of Bytes				# of Cycles
3		LDX *+4	arrange index register so that MTL1TM will be executed on next pass	3
1		RTI		10
3	MTL1TM	LDAA MTLTM1	read MTTL counter #1	4
3		CLR MTLTM1	clear counter	6
3		STAA MTLLS1	store count in data list	5
3		LDX #*+4	arrange index register so that MTL2TM will be executed on the next pass	3
1		RTI		10
3	MTL2TM	LDAA MTLTM2	read MTTL counter #2	4
3		CLR MTLTM2	clear counter	6
3		STAA MTLLS2	store count in data list	5
2		BRA RFTLX	branch to index register reset routine	4

Symbol Interpretation

PIA1A: side A output register of PIA#1
PIA2A: side A output register of PIA#2
PIA2B: side B output register of PIA#2
FTLLST: first of four consecutive memory locations into which the four FTTL counts are written
MTLTM1: memory location which is incremented upon receipt of an MTTL#1 pulse
MTLTM2: memory location which is incremented upon receipt of an MTTL#2 pulse
MTLLS1: memory location into which the MTTL#1 count over one TBG period is written
MTLLS2: memory location into which the MTTL#2 count over one TBG period is written

Total Execution Time from Receipt of Interrupt:

FTL1 73 cycles
FTL2 73 cycles
FTL3 73 cycles
FTL4 73 cycles
MTL1TM 54 cycles
MTL2TM 59 cycles

Memory Requirements: 115 bytes of ROM
6 bytes of RAM

APPENDIX B3

MTTL INTERRUPT ROUTINES

# of Bytes				# of Cycles
2	DINT	LDAA #$80	prepare mask for interrupt indentification	2
3		BITA CR1A	test for IRQA1 (TBG interrupt)	4
2		BEQ MTLSR	service MTTL routine if IRQA1 not set	4
3		JMP TBGIR	service TBG routine otherwise	3
2	MTLSR	LDAA #06		2
3		STAA CR1B	disable the PIA1 side B IRQ output	5
1		CLI	reenable MPU interrupt system	2
2		LDAA #$0E	prepare to output TSB enable pulse	2
3		STAA PIA1A	output TSB enable pulse	5
3		LDAB PIA1B	read MTTL byte	4
3		INC PIA1A	clear MTTL latch	6
3		LDAA CR1B	dummy instruction-clears MTTL interrupt flag inside PIA	4
2		LDAA #02	generate mask to determine if MTTL#2 flip flop is set	2
2		BITA B		3
2		BEQ LP1	if MTTL#2 flip flop is not set jump to LP1	4
3		INC MTLTM2	increment MTTL#2 counter	6
2		BNE LP1	if no overflow, jump to LP1	4
3		DEC MTLTM2	if counter overflow occurred, reset count to maximum	6
2	LP1	LDAA #$01	generate mask to determine if MTTL#1 flip flop is set	2
2		BITA B		3
2		BEQ LP2	if MTTL#1 is not present, jump to LP2	4
3		INC MTLTM1	increment MTTL#1 counter	6
2		BNE LP2	if no overflow, jump to LP2	4
3		DEC MTLTM1	if counter overflow occurred, reset count to maximum	6
2	LP2	LDAA #07		2
3		STAA CR1B	reenable the PIA#1 side B IRQ output	5
1		RTI	return from interrupt	10

Symbol Interpretation

CR1A:	control register A of PIA#1
CR1B:	control register B of PIA#1
PIA1A:	output register of PIA1 side A
PIA1B:	output register of PIA1 side B
MTL2TM:	memory location incremented upon receipt of an MTTL#2 pulse
MTL1TM:	memory location incremented upon receipt of an MTTL#1 pulse

Worst case MTTL execution time from receipt of interrupt:

- One MTTL line read - 104 cycles
- Two MTTL lines read - 120 cycles

Memory Requirements: 64 bytes of ROM

2 bytes of RAM

APPENDIX B4

ROUTINE TO READ 32 ANALOG VOLTAGES

# of Bytes				# of Cycles
2	ANRTN	LDAA #00		2
3		STAA ANCSW	set analog control signal word equal to zero	5
2		LDAA #32		2
3		STAA ANCTR	configure counter to count off the 32 input signals	5
3		LDS #ADLST	set stack pointer to ADLST	5
2	LOOP1	LDAA ANCSW		2
3		STAA PIA2A	select the desired input port	5
2		LDAA #$3D		2
3		STAA CR2B	set CB2 (start conversion)	5
2		LDAA #$35		2
3		STAA CR2B	clear CB2	5
2		LDAA #$80		2
3	LOOP2	BITA CR2B	test for end of conversion (EOC)	4
2		BEQ LOOP2	if EOC not received jump to LOOP2	4
2		LDAA #$20		2
3		STAA PIA2A	enable A/D tri-state buffer	5
2		LDAB PIA2B	read A/D value	2
1		PSHB	store A/D value in stack	4
3		DEC ANCTR	decrement counter	6
3		TST ANCTR	have all 32 inputs been read?	6
2		BEQ CCRTN	if done, jump to CC routine	4
3		INC ANCSW	increment control signal word	6
2		BRA LOOP1	service next input	4

Symbol Interpretation

ANCSW: location which contains the control signal word sent to the control signal decoder
ANCTR: counter in memory which decrements as each of the input ports is read
ANCTR=0 signifies the end of the routine
PIA2A: output register of side A of PIA#2
CR2B: side B control register of PIA#2
PIA2B: output register of side B of PIA#2
ADLST: first of 32 successive memory locations into which the analog voltage data is written

Total Execution Time: 3310 cycles (including A/D conversion time).

Total Memory Requirements: 56 bytes of ROM

34 bytes of RAM

APPENDIX B5

TIME BASE GENERATOR LOAD NEW COUNT ROUTINE

# of Bytes				# of Cycles
2	TBGLNC	LDAA #$00		2
3		STAA CR1B	causes DDRB of PIA1 to be addressed	5
2		LDAA #$FF		2
3		STAA DDR1B	program OTR of PIA1B as output	5
2		LDAA #$03		2
3		STAA CR1B	select OTR of PIA1B, IRQB1 set by low to high transition, IRQB1 enabled	5
3		LDAA TBGCT1		4
3		STAA PIA1B	output LS byte of TBG count	5
2		LDAA #$80		2
3		STAA PIA1A	strobe LS byte latch	5
3		LDAA TBGCT2		2
3		STAA PIA1B	output next higher byte of TBG count	5
2		LDAA #$90		2
3		STAA PIA1A	strobe next higher byte latch	5
3		LDAA TBGCT3		2
3		STAA PIA1B	output MS byte	5
2		LDAA #$A0		2
3		STAA PIA1A	strobe MS byte latch	5
2		LDAA #$00		2
3		STAA CR1B	address DDRB of PIA1	5
3		STAA DDR1B	return PIA1B to input mode	5
2		LDAA #$07		2
3		STAA CR1B	address OTR, control register reprogrammed for normal operating mode	5
3		JMP ANRTN	jump to Analog Voltage Scan Routine	3

Symbol Interpretation

CR1B:	Control Register of B side of PIA#1
DDR1B:	Data Direction Register of B side of PIA#1
PIA1B:	Output Register of B side of PIA#1
PIA1A:	Output Register of A side of PIA#1
TBGCT1:	Location in RAM which contains the least significant byte of the desired TBG count
TBGCT2:	Location in RAM which contains the next more significant byte of the desired TBG count
TBGCT3:	Location in RAM which contains the most significant byte of the desired TBG count

Total Routine Execution Time: 85 cycles.

Total Memory Requirements: 65 bytes of ROM

3 bytes of RAM

APPENDIX B6

PIA CONTROL WORD OPTIONS

Bit 0-1: CA1 control bits

- If bit 1 is a 1, the CA1 input is sensitive to low to high transitions.
- If bit 1 is a 0, CA1 is sensitive to high to low transitions.
- If bit 0 is a 1, the proper transition on CA1 will cause the PIA IRQA (interrupt request) output, which is connected to the MPU interrupt request line, to request an MPU interrupt.
- If bit 0 is a 0, the request will be temporarily inhibited but will be generated at that time when bit 0 is reset to 1.

Bit 2: DDRA/ORA select bit

DDRA and ORA share a single memory address.

To select between the two registers, a one or a zero is written into CRA bit 2 prior to addressing the DDRA/ORA location.

- If CRA bit 2 equals 0, DDRA is addressed.
- If CRA bit 2 equals 1, ORA is selected.

Bits 3-5: CA2 control bits

- If bit 5 is set equal to zero, CA2 functions as an input and bits 3 and 4 affect CA2 in the same way as bits 0 and 1 affect CA1.
- If bit 5 is set equal to 1, CA2 functions as an output and may operate in one of the following ways:
  a) as a strobe output, going low when a read output register command is completed and returning high by an active CA1 transition
  b) as a strobe output, going low on a read output register command and automatically returning high in approximately one microsecond
  c) as an output which duplicates what is written into bit 3 of CRA.

Bits 6-7: IRQA2 and IRQA1 flags

These flags are set by transitions on inputs CA2 and CA1 respectively and indicate that an interrupt signal was received on the respective input. These flags may be read by a read CRA command and are automatically cleared when read.

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