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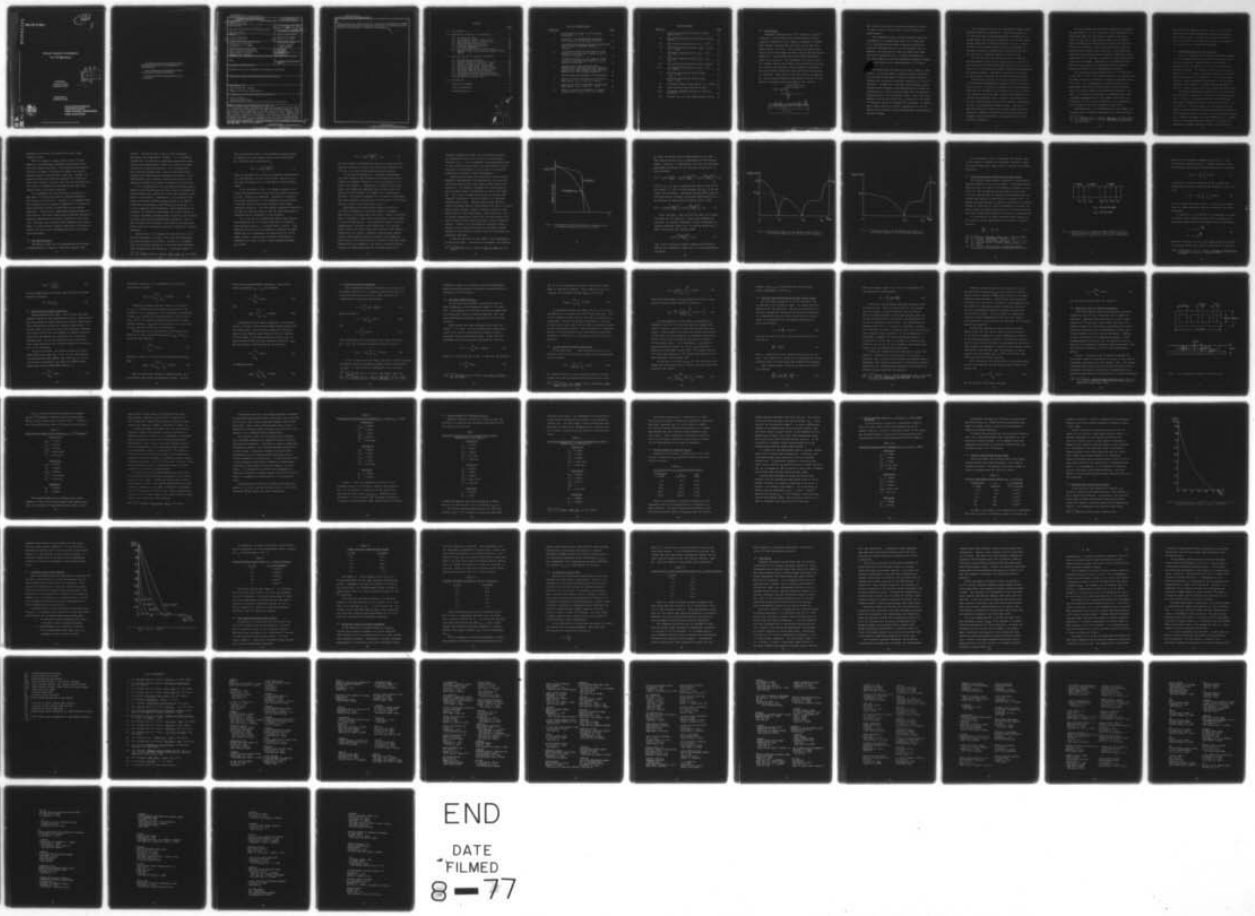

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Vertical Transistor Investigation For I^2L Structures

Prepared by
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U.S. Army Materiel Development and Readiness Command
HARRY DIAMOND LABORATORIES
Adelphi, Maryland 20783

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A one-dimensional mathematical model is presented for the vertical transistor associated with an I^2L semiconductor device. This particular model represents a modification of similar models used for bipolar transistor operation; it requires little computer time and has been subjected to extensive verification over past years. Although incomplete in its present form, the model suggested here is based upon the physical mechanisms encountered during semiconductor device operation. For this reason, it is suggested that

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little additional effort would be required to complete this model, including the physical mechanisms associated with damage arising from an ionizing type of radiation environment.

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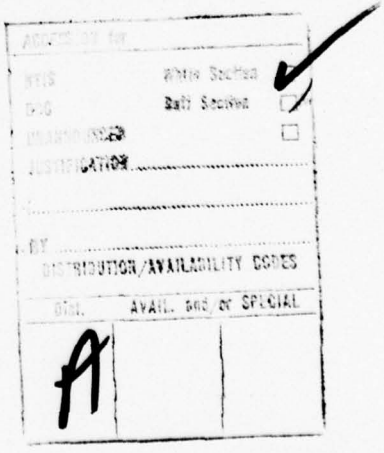

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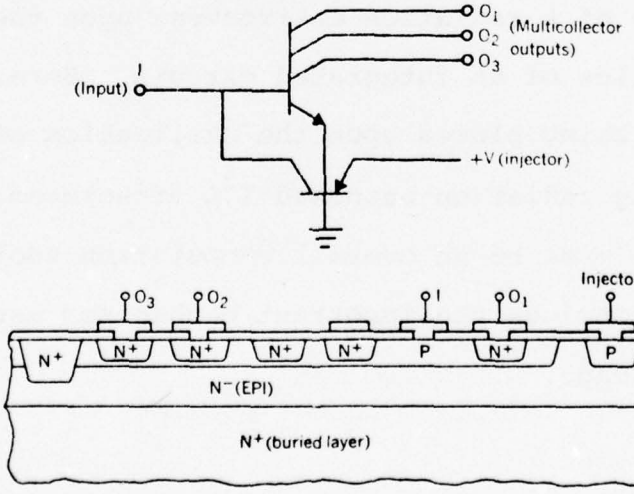
1.0 Introduction

Integrated injection logic (I^2L) gates are a class of integrated circuits which can be fabricated on bipolar transistor production lines, making it possible to combine other bipolar circuitry with I^2L logic on the same integrated circuit (IC) chip. They promise high packing densities and low delay-power products, making them potentially competitive with conventional metal-oxide-semiconductor (MOS) logic circuitry. The fundamental I^2L logic circuit is a simple inverter (see sketch) which physically consists of a vertical npn multiple emitter transistor operated in the inverse mode so that the conventional emitters perform as collectors. Base drive to the npn inverter is supplied by a lateral pnp transistor whose p-type collector is integrated (or merged) with p-type base of the inverter.



The inverse active mode of operation inherent in such an I^2L gate is one for which there is little theoretical understanding.

This program of effort has been directed toward the development of a mathematical model for I^2L operation. It is intended that this model accurately predict the electrical characteristics of an I^2L structure and, in addition, the influence of radiation damage upon these electrical characteristics. A further requirement is that this model also yield the important parameters needed for an equivalent circuit representation of I^2L device operation.

The engineering applicability of such a model is self-evident. Using this model, a design engineer could study and evaluate the necessary "trade-off" between radiation hardness and the overall electrical properties of a new I^2L structure. In addition, this model would provide a means whereby design engineers could quantitatively evaluate the consequences of a radiation environment upon the operating characteristics of an integrated circuit. Here, particular emphasis is being placed upon the utilization of this model for designing radiation hardened I^2L structures. In reality, such a model must be an overall computation tool for I^2L design--and include the important mechanisms associated with radiation damage.

The intended end use of this mathematical model places limitations upon its complexity. Physical mechanisms of I^2L operation must be approximated with the degree of accuracy needed for engineering purposes, yet the model must remain simple from a computational point of view. During I^2L design the engineer should be able to undertake an extensive program of computational experimentation, without involving an excessive amount of computer time.

The initial plan for this project was to complete the development effort over a two-year period. The first year was to be directed toward modeling the vertical transistor in an I^2L structure, without including the mechanisms of radiation damage. Thereafter, during the second year, it was planned to complete this model development effort.

During the first year it was also planned to develop a two-dimensional mathematical model for vertical transistor operation. For practical reasons, this two-dimensional model was not intended as an I^2L design tool but, instead, as a research tool to be used during the development of a simplified engineering model. Clearly, the funding level for this program would not permit the complete development of such a two-dimensional computer model. Therefore, it was our intention to modify an existing model for bipolar transistor operation; modifications that would permit an analysis of device operation, as encountered in the I^2L vertical transistor.

It can be stated that these modifications far exceeded our expectations. At the initiation of this program a two-dimensional model for the bipolar transistor was operational; it was not a good computer model, but it worked. After introducing the required modifications many difficulties were encountered. These difficulties were primarily associated with computational stability. Algorithms that worked for conventional bipolar transistor operation proved inadequate for I^2L operation, and many of these difficulties could not be overcome. Nonetheless, this difficulty did not alter the program of development directed toward an engineering model for this semiconductor structure.

The engineering model proposed here for I^2L operation is not new. In fact, this model represents a new application of models previously developed for bipolar transistor operation [1,2]. As a consequence, a large part of this proposed model has been used extensively for device design, and it has proven adequate for engineering purposes. Further, it is known that this model is computationally fast; a suitable implementation of this model would permit the analysis of an I^2L vertical transistor in an estimated 20 to 30 seconds of CPU time (assuming an IBM 360/85).

Described here is an implementation of this model, and its application to specific problems of I^2L device design.

---

[1] D.P. Kennedy and P.C. Murley, IBM Jour., 8, 482 (1964).
[2] D.P. Kennedy and P.C. Murley, Solid-State Electronics, 15, 203 (1972).

The discussions presented in this report are limited to those aspects of model development completed during the first contract year. Because this program of effort is not being funded to its completion, further developments of this model will be described elsewhere.

2.0 Mathematical Model for I^2L Operation

Figure 1 illustrates the vertical transistor assumed in this proposed model for the vertical transistor of an I^2L type structure. Simplification of this model is accomplished by its subdivision into two fundamentally different regions: an intrinsic region and an extrinsic region, Fig. 2. Clearly, this simplification ignores two important aspects of I^2L operation. First, this simplification ignores mechanisms encountered at the up emitter periphery, and, second, it ignores the two-dimensional flow of electric current within the transistor base region.

Peripheral mechanisms associated with this structure are recognized as important to vertical transistor operation. Further, it is recognized that these mechanisms are greatly influenced by the close proximity of the injector junction. For this reason, it was planned that the model for these peripheral mechanisms would be included in the second year effort, as a part of the horizontal transistor. Despite the absence of these mechanisms, it is shown that in its present form this model for a vertical I^2L transistor provides extensive insight and quantitative

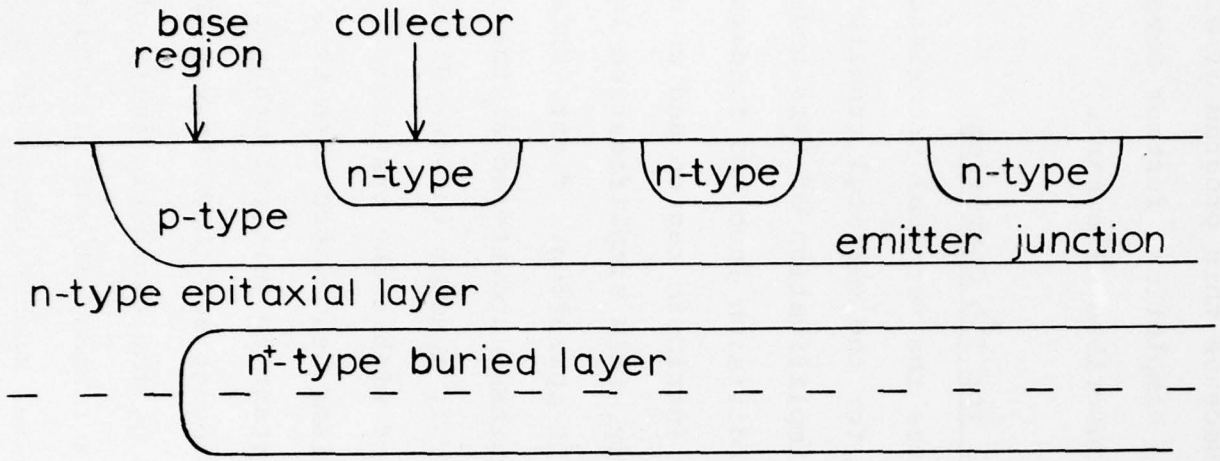


Fig. 1 Two-Dimensional Model of the Vertical Transistor.

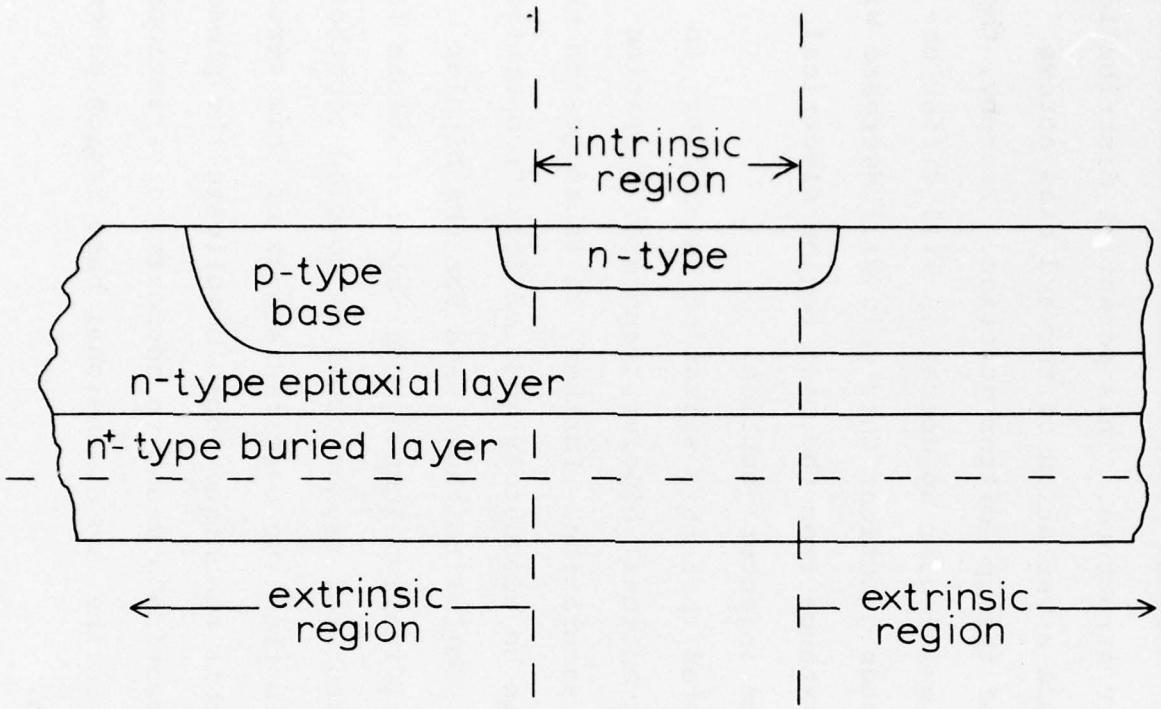


Fig. 2 Division of a Two-Dimensional Transistor into Intrinsic and Extrinsic Regions.

information concerning the operation of such a semiconductor device.

During up operation, base region electric current produces a two-dimensional potential distribution within this semiconductor structure. This potential distribution is known to produce a variation of forward bias across various regions of the up emitter junction. Thereby, the apparent current gain under up operation will differ between each collector junction; this gain will decrease with an increase of distance from the base region electrical contact and/or the injector junction.

It is suggested that this situation is similar, in many ways, to conventional bipolar transistor operation when driven into saturation. Further, it is suggested that this mechanism can be adequately modeled for I^2L operation using techniques similar to those used for the bipolar transistor. Specifically, lumped model approximations for each vertical transistor region could be coupled together by resistors approximating the base resistance of this structure. Although this technique would complicate the present model, it could provide a means to approximate variations of current gain due to the two-dimensional base region potential distribution.

2.1 The Physical Model

The physical model for this semiconductor device must be representable in terms of a specified impurity atom

profile. Therein we have a topic of much discussion throughout the semiconductor industry. It is frequently assumed that an inability to adequately approximate these impurity atom distributions limits the validity of models for bipolar transistor operation. It is proposed that this inability produces only a need to understand these inherent differences between experiment and theory. Such understanding, once attained, permits modification of the mathematical model in a fashion consistent with experiment.

It is recognized that few semiconductor devices contain impurity atom distributions that are ideally represented by closed mathematical expressions of the type derived in textbooks on this subject. Nonetheless, it is suggested that these experimental anomalies appear primarily in regions containing an exceedingly large impurity atom density. It is also suggested that tradiational closed mathematical expressions can adequately approximate the active regions of a bipolar transistor--assuming these expressions are modified to correct for the high concentration anomalies. Here we have the basis for our model of the impurity atom distributions within the intrinsic and extrinsic regions of a bipolar transistor.

Specifically, it is assumed the base region of an I^2L vertical transistor is p-type, and it has been fabricated by diffusing boron into silicon. Further, it is assumed that this diffusion process is of the traditional two-step type--predeposition and oxidation. It has been shown [3]

---

[3] D.P. Kennedy and P.C. Murley, Proc. IEEE, 52, 372 (1963).

that the oxidation phase of this diffusion process yields an impurity atom distribution that is well approximated by a Gaussian type of distribution,

$$C(x) = C_o \exp\left[-\left(\frac{K+X}{2L}\right)^2\right] , \qquad (1)$$

where C_o represents the impurity atom surface concentration, X is the distance from the silicon-oxide interface, K is the oxide thickness, and L is the impurity atom diffusion length.

In the derivation of Eq. 1 we neglect changes of impurity atom distribution arising from the dopant solubility in SiO_2. Because this mechanism introduces a relatively short-range modification of the impurity atom distribution, it has been found to have small influence upon bipolar transistor operation. For this reason, mechanisms influencing the impurity atom distribution near the oxide-semiconductor interface are not considered in this analysis.

Due to the initial predeposition phase (high impurity atom concentration) it has been found that the impurity atom diffusion length, L, is seldom known, a priori. Each different diffusion process produces a different diffusion length and, as a consequence, we seldom know C(x) at any given location. Despite this situation, when boron is diffused into n-type silicon of known background doping, C_B, we have

$$C(x) = C_o \exp\left[-\left(\frac{K+X}{2L_1}\right)^2\right] - C_B \ . \qquad (2)$$

For the analysis of semiconductor devices we need only know where the junction is located, and the surface concentration of boron, C_o, which can be determined experimentally.

It has been found that Eq. 2 adequately approximates the boron impurity atom distribution throughout the active regions of a bipolar transistor. This verification is indirect, but extensive. Specifically, numerous device parameters are exceedingly dependent upon the base region impurity atom distribution; for example, the reach-through voltages. Satisfactory agreement is attained with experiment when these parameter calculations are based upon a base region impurity profile of the type given by Eq. 2.

Approximating the down emitter impurity profile in this device represents a difficult problem of judgment. Specifically, the narrow base width used in today's technology makes it necessary to use a high concentration arsenic dopant to form the down emitter. This becomes necessary to prevent compensation of the base region impurities and, thereby, unduly reduce the overall base region impurity atom density. Phosphorous, for example, produces a substantially smaller impurity atom gradient than does arsenic, and phosphorous would restrict I^2L structures to a relatively large base width. Contrasting with phosphorous, the arsenic diffusing process produces an impurity atom profile for which there is no

available mathematical model [4]; the resulting profile is exceedingly steep in the vicinity of the collector junction, Fig. 3. As a consequence, any mathematical model of this diffusion process must be an approximation that is consistent with experiment, yet not alter the electrical properties of any device under consideration.

Experience has shown that this arsenic profile can be adequately approximated by a complementary error function, using an unrealistically large impurity atom surface concentration. For example, throughout this calculation we use an assumed surface concentration of about 10^{24} atoms/cm^3. This is not intended to imply that we believe 10^{24} atoms/cm^3 represents a realistic value; it is obviously unrealistically large. Nevertheless, by this means we attain the needed impurity atom gradient near the up collector junction and, thereby, produce a realistic amount of base region impurity atom compensation. This unrealistic value of surface concentration yields near the down emitter junction an impurity atom gradient typical of that produced by arsenic. Further, this approximation technique yields a similar type of impurity distribution throughout regions adjacent to this junction, regions that are associated with transistor operation.

A similar approach has been taken in our approximation of the buried layer. Specifically, throughout this analysis

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[4] D.P. Kennedy and P.C. Murley, Proc. of IEEE, 59, 335 (1971).

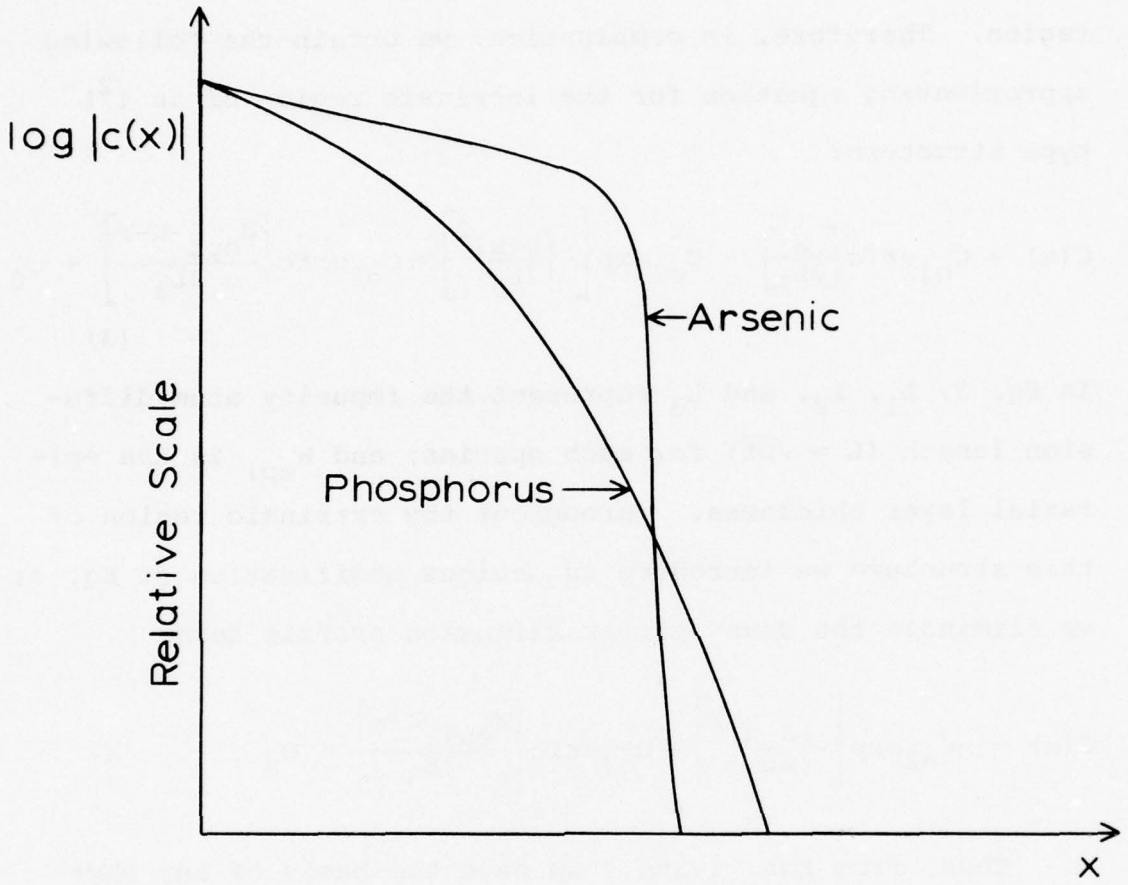

Fig. 3 Illustrative Difference Between a Phosphorus and an Arsenic Diffusion Profile in Silicon.

we assume the buried layer is approximated by the same type impurity profile used to approximate the down emitter region. Therefore, in combination, we obtain the following approximating equation for the intrinsic region of an I^2L type structure:

$$C(x) = C_{o1}\text{erfc}\left[\frac{x}{2L_1}\right] - C_{o2}\exp\left[-\left(\frac{K+x}{2L_2}\right)^2\right] + C_{o3}\text{erfc}\left[\frac{W_{epi}-K-x}{2L_3}\right] + C_B \ . \tag{3}$$

In Eq. 3, L_1, L_2, and L_3 represent the impurity atom diffusion length ($L = \sqrt{Dt}$) for each species; and W_{epi} is the epitaxial layer thickness. Throughout the extrinsic region of this structure we introduce an obvious modification of Eq. 3: we eliminate the down emitter diffusion profile term:

$$C(x) = -C_{o2}\exp\left[-\left(\frac{K+x}{2L_2}\right)^2\right] + C_{o3}\text{erfc}\left[\frac{W_{epi}-K-x}{2L_3}\right] + C_B \ . \tag{4}$$

Thus, from Eqs. 3 and 4 we have the basis of our physical model for I^2L operation. Using these mathematical relations, an iterative procedure is used to establish the junction locations (where $C(x) = 0$) and the buried layer edge is defined by that location where

$$C_{o3}\text{erfc}\left[\frac{W_{epi}-K-x}{2L_3}\right] = C_B \ . \tag{5}$$

Figs. 4 and 5 illustrate typical impurity atom profiles used in this mathematical model for an I^2L type semiconductor device.

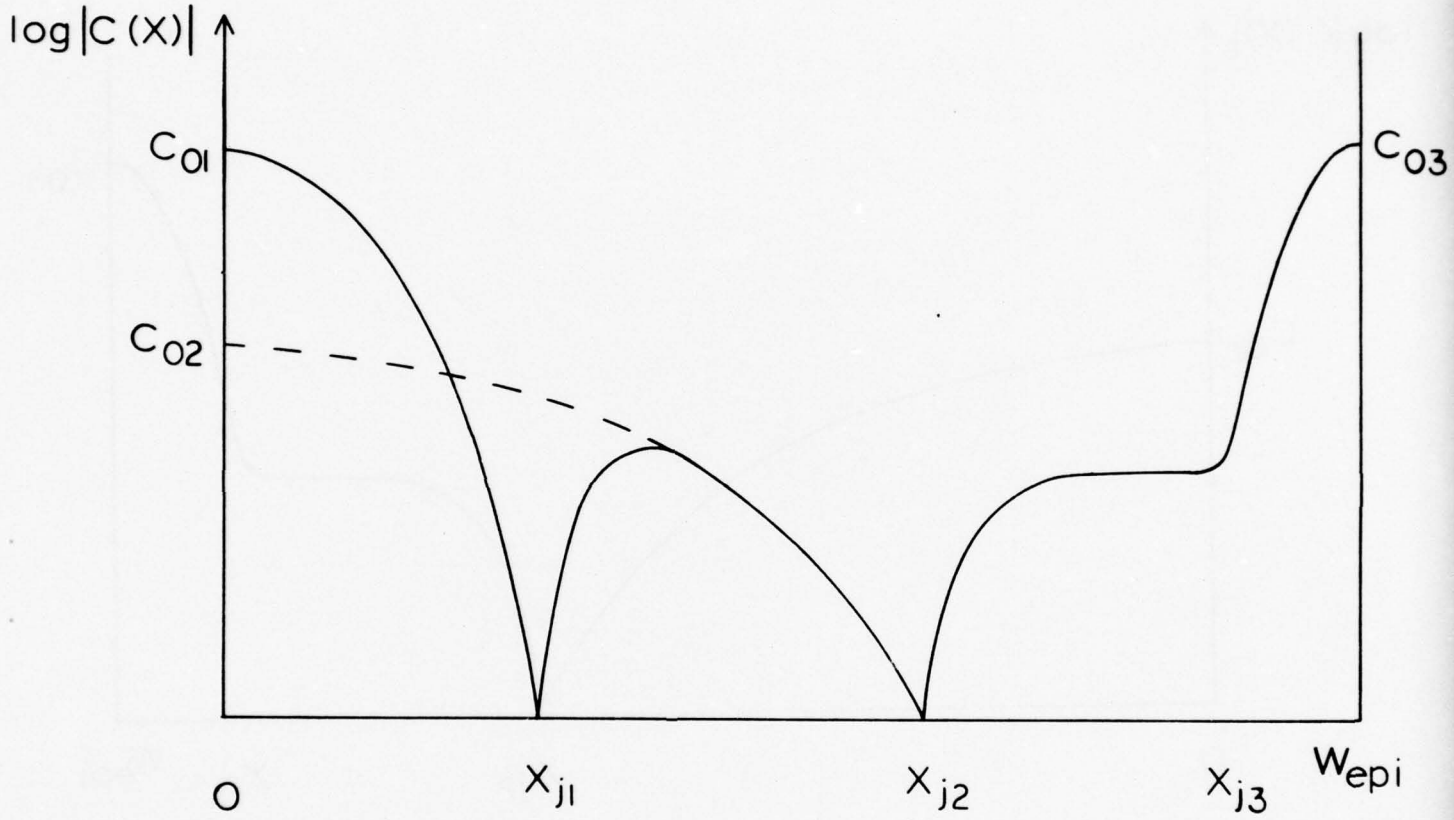

Fig. 4 Illustrative Model for the Impurity Atom Profile in the Intrinsic Region of an I^2L Vertical Transistor.

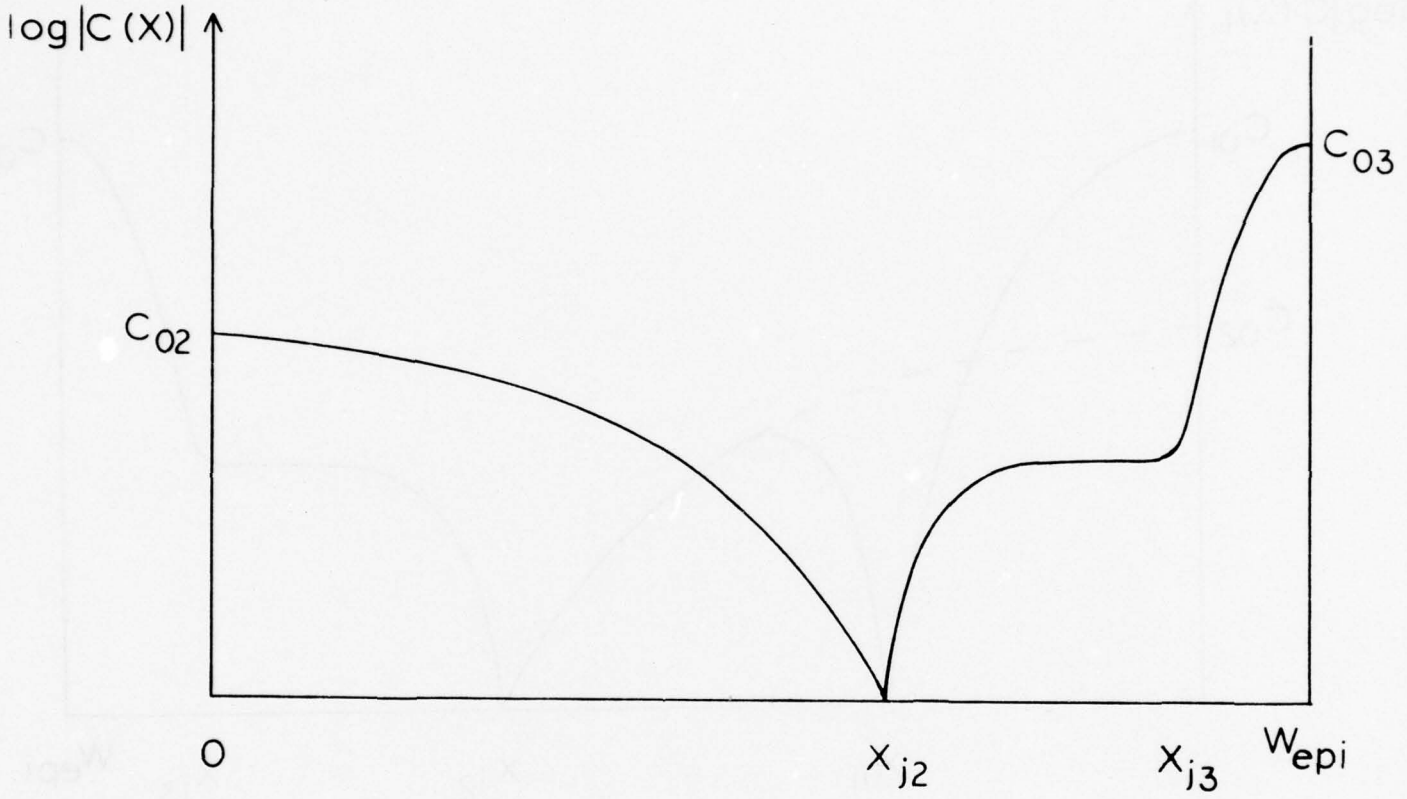

Fig. 5 Illustrative Model for the Impurity Atom Profile in the Extrinsic Region of an I^2L Vertical Transistor.

For convenience, Fig. 6 illustrates the notation used in this report to identify the junctions, and their respective space-charge layer edges, within a typical I^2L vertical transistor.

2.2 Space-Charge Layer Characteristics--Equilibrium

The depletion approximation represents a traditionally important aspect of p-n junction theory. This approximation technique was first used in the analysis of abrupt p-n junctions [5], and its application continued for many years. It is now realized that the depletion approximation has only limited applicability for the abrupt p-n junction [6-7], although this approximation is generally applicable to linearly graded p-n junctions [8], and to diffused p-n junctions [9]. Here we model the space-charge regions of diffused junctions based upon traditional concepts of the depletion approximation.

At equilibrium, we assume the space-charge regions of I^2L junctions can be represented by solutions of Poisson's equation:

$$\frac{d^2\psi}{dx^2} = - \frac{q}{\kappa\varepsilon_o} C(x) \ , \qquad (6)$$

---

[5] W. Shockley, Bell Syst. Tech. Jour., 28, 435 (1949).
[6] D.P. Kennedy, IEEE Trans., ED-22, 11 (1975).
[7] D.P. Kennedy, Solid State Electronics, 20, 311 (1977).
[8] D.P. Kennedy and R.R. O'Brien, IBM J. of Res., 11, 252 (1967).
[9] D.P. Kennedy, Math. Invest. of Semicond. Devices, Final Report AF 19(628)-5072, AFCRL-66-358(11), 1967.

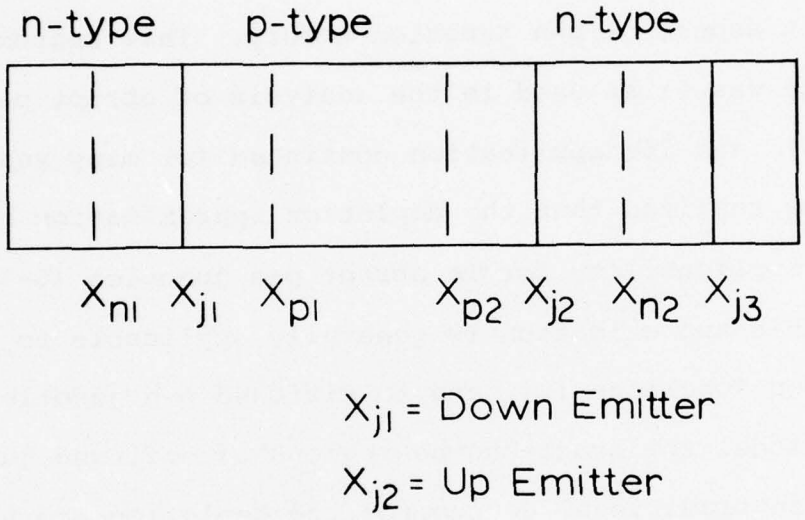

Fig. 6 Illustration of the Notation Used to Identify Each Junction (and its respective space-charge layer edges) in the Intrinsic Region of an I^2L Vertical Transistor.

where C(x) for intrinsic regions is given by Eq. 3 and for extrinsic regions by Eq. 4. Further, from Eq. 6 the space-charge layer electric field distribution is given by

$$\xi(x_1,x) = \frac{q}{\kappa\varepsilon_o} \int_{x_1}^{x} C(t)dt \ , \tag{7}$$

In addition, a second integration of Eq. 7 yields the electrostatic potential distribution throughout a p-n junction,

$$\psi(x) = - \frac{q}{\kappa\varepsilon_o} \int_{x_1}^{x} \int_{x_1}^{\eta} C(t)dtd\eta \ . \tag{8}$$

It can be shown [10] that both Eq. 7 and Eq. 8 are expressible in closed analytical form and, therefore, are easily calculated.

In addition, at equilibrium it is reasonable to assume all mobile carrier densities within the p-n junction are adequately approximated by a Boltzmann type of distribution,

$$\begin{aligned} &\text{a)} \quad p = C_1 e^{-\frac{q\psi}{kT}} \\ &\text{b)} \quad n = C_2 e^{\frac{q\psi}{kT}} \end{aligned} \tag{9}$$

From Eq. 9a and Eq. 9b, the total voltage across a diffused p-n junction space-charge layer at equilibrium is given by:

---

[10] M. Abramowitz and J.A. Stegum, Handbook of Mathematical Functions, U.S. Dept. of Commerce, 1964.

$$V_{eq} = \frac{kT}{q} \ell n \left[\frac{p(x_{pe}) n(x_{ne})}{n_i^2} \right] \qquad (10)$$

where

$$n(x) = p(x) = \frac{C(x) + \sqrt{C(x)^2 + 4n_i^2}}{2} \qquad (11)$$

In Eq. 10, x_{pe} and x_{ne} designate the space-charge layer edges in the n-type and p-type material, respectively, at equilibrium.

Thus, in combination, Eqs. 7, 8, and 10 yield the equilibrium conditions for a diffused p-n junction:

$$\text{a)} \quad 0 = \frac{q}{\kappa \varepsilon_o} \int_{x_{ne}}^{x_{pe}} \int_{x_{ne}}^{\eta} C(t)\,dt\,d\eta - \frac{kT}{q} \ell n \left[\frac{p(x_{pe}) n(x_{ne})}{n_i^2} \right] \qquad (12)$$

$$\text{b)} \quad 0 = \frac{q}{\kappa \varepsilon_o} \int_{x_{ne}}^{x_{pe}} C(t)\,dt \ .$$

This mathematical model has been used to calculate the equilibrium space-charge layer edges for both the up and down emitters of an I^2L type structure.

Using this model, we locate in a given device the space-charge layer edges of both p-n junctions, and their respective "built-in" or equilibrium diffusion voltages,

$$V_{eq} = \frac{kT}{q} \ell n \left[\frac{p(x_{pe}) n(x_{ne})}{n_i^2} \right] \ . \qquad (13)$$

From a knowledge of these space-charge layer edge locations, (x_{ne}, x_{pe}) we also calculate the equilibrium space-charge layer capacitance of each junction,

$$C_{eq} = \frac{\kappa\varepsilon_o}{|x_{ne}-x_{pe}|} \quad . \tag{14}$$

In addition, a knowledge of these locations provides a means to readily establish the equilibrium electrical base region width within an I^2L transistor,

$$W_e = \left(x_{pe_2}-x_{pe_1}\right) \quad . \tag{15}$$

2.3 Space-Charge Layer Characteristics--Reverse Bias

Equation 7 and Eq. 8 are also used to calculate the reverse biased characteristics of a diffused p-n junction. With a knowledge of the "built-in" equilibrium voltage (Sec. 2.2), the reverse bias space-charge layer edges are located by satisfying the relations

$$\begin{aligned} \text{a)} \quad 0 &= \frac{q}{\kappa\varepsilon_o}\int_{x_n}^{x_p}\int_{x_n}^{\eta} C(t)\,dt\,d\eta - V_{eq} - V_a \\ \text{b)} \quad 0 &= \frac{q}{\kappa\varepsilon_o}\int_{x_n}^{x_p} C(t)\,dt \quad . \end{aligned} \tag{16}$$

In Eq. 16, V_{eq} represents the equilibrium junction barrier potential and V_a is an applied reverse biasing voltage.

As used for the equilibrium case (Sec. 2.2), the calculation establishes the space-charge layer edges (x_n, x_p) for each p-n junction. Similarly, after calculating these locations we establish the space-charge layer capacitances for each individual junction,

$$C(V_a) = \frac{\kappa\varepsilon_o}{\left|x_n - x_p\right|} \tag{17}$$

and the nonequilibrium electrical base width for this semiconductor structure

$$W_e = \left|X_{p_2} - X_{p_1}\right| . \tag{18}$$

2.4 Reach-Through Voltage Calculations

Another application of Eqs. 7 and 8 yields the reach-through voltages for this semiconductor device. Specifically, the reverse biasing voltage required to produce space-charge layer reach-through within the transistor base region. It has been shown [2] that this particular electrical parameter offers many difficulties with respect to bipolar transistor fabrication reproducibility, particularly in narrow-base configurations. It will be shown here that space-charge layer reach-through can be a similar problem in the fabrication of I^2L structures.

During up operation, the reverse biased up collector space-charge layer edge (X_{p_1} in Fig. 6) can reach-through to the up emitter space-charge layer edge (X_{p_2} in Fig. 6). In this type of situation, the total up collector space-charge layer can be established using Eq. 7,

$$0 = \int_{X_{n_1}}^{X_{p_2}} C(x)dX . \tag{19}$$

Thereafter, using Eq. 8, we establish the up collector punch-through voltage,

$$V_{RT} = \frac{q}{\kappa\varepsilon_o} \int_{X_{n_1}}^{X_{p_2}} \int_{X_{n_1}}^{\eta} C(t)dtd\eta \qquad (20)$$

Substantial changes have been found in the location of X_{p_2} for forward bias and equilibrium operation of the up emitter. As a consequence, the up collector reach-through voltage, V_{RT}, changes for these two modes of device operation, and it is necessary to specify two different reach-through voltages: V_{RTO} when the up emitter is at zero bias and V_{RTU} when the up emitter is operational.

Assuming the up emitter junction space-charge layer edges are at their equilibrium locations (X_{pe_2} and X_{ne_2}), we satisfy the relation:

$$0 = \int_{X_{n_1}}^{X_{pe_2}} C(t)dt \ . \qquad (21)$$

Thereafter, from Eq. 8 we have the reach-through voltage, V_{RTO},

$$V_{RTO} = \frac{q}{\kappa\varepsilon_o} \int_{X_{n_1}}^{X_{pe_2}} \int_{X_{n_1}}^{\eta} C(t)dtd\eta \ . \qquad (22)$$

When the up emitter junction is forward biased its space-charge layer width is exceedingly narrow. For pur-

poses of this punch-through calculation, little error arises by assuming $X_{p_2} = X_{j_2}$ and therefore,

$$0 = \int_{X_{n_1}}^{X_{j_2}} C(t)dt \ , \tag{23}$$

and

$$V_{RTU} = \int_{X_{n_1}}^{X_{j_2}} \int_{X_{n_1}} C(t)dtd\eta \tag{24}$$

Contrasting with up emitter operation, little change arises in the down emitter space-charge between equilibrium and forward bias. This situation arises from the large impurity atom gradient associated with this p-n junction. For this reason, it becomes necessary to define only one reach-through voltage for down transistor operation, V_{RTD}, and this voltage is approximated by the equations

$$0 = \int_{X_{n_2}}^{X_{j_1}} C(x)dx \tag{25}$$

in combination with

$$V_{RTD} = \int_{X_{n_2}}^{X_{j_1}} \int_{X_{n_2}}^{\eta} C(t)dtd\eta \tag{26}$$

2.5 Junction Avalanche Breakdown

The avalanche breakdown of a diffused p-n junction can be readily modeled for any arbitrary space-charge layer impurity atom distribution [11-13]. This calculation is accomplished by satisfying the relation

$$1 = b \int_{X_n}^{X_p} \exp\left(- \frac{a}{\xi(\eta)}\right) d\eta \tag{27}$$

where, from Eq. 8,

$$\xi(\eta) = \frac{q}{\kappa\varepsilon_o} \int_{X_n}^{\eta} C(t)dt \tag{28}$$

and

$$0 = \int_{X_n}^{X_p} C(t)dt \ . \tag{29}$$

After establishing the space-charge layer edges satisfying Eqs. 27-29, the avalanche breakdown voltage is given by

$$V_{av} = - \frac{q}{\kappa\varepsilon_o} \int_{X_n}^{X_p} \int_{X_n}^{\eta} C(x)dxd\eta \ . \tag{30}$$

It will be shown that the "down" operation collector junction will sometimes undergo avalanche breakdown before reach-through $V_{av}<V_{RTD}$. In this situation, measurement of the collector

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[11] D.P. Kennedy and R.R. O'Brien, IRE Trans., ED-9, 478 (1962).
[12] D.P. Kennedy and R.R. O'Brian, IBM Jour., 9, 422 (1965).
[13] D.P. Kennedy and R.R. O'Brien, IBM Jour., 10, 213 (1966).

breakdown voltage will be shown to offer an experimental means for gaining valuable information concerning physical properties of an I^2L device.

2.6 Open-Base Breakdown BV_{EBO}

As yet, open-base breakdown calculations have not been implemented in our mathematical model for I^2L operation. Nevertheless, this has been previously accomplished for conventional bipolar transistor operation [14], and these techniques are directly applicable to the I^2L type structure.

Specifically, open base breakdown occurs when $\alpha M = 1$ (hence $\beta = \infty$), where α is the grounded base current gain, and M is the current multiplication occurring within a collector junction space-charge layer. Thus, open-base breakdown can be calculated by satisfying the relation,

$$(1-\alpha) = b \int_{X_n}^{X_p} \exp - \frac{a}{\xi(\eta)} \, d\eta \ , \tag{31}$$

where $\xi(\eta)$ is given by Eq. 28 and, in addition, the relation

$$0 = \int_{X_n}^{X_p} C(t)dt \ . \tag{32}$$

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[14] D.P. Kennedy and R.R. O'Brien, Int. Jour. of Elect., 18, 133 (1965).

Eqs. 31 and 32 establish the junction space-charge layer edges at open-base breakdown. After completing this calculation, the breakdown voltage (BV_{CEO}) is given by

$$BV_{CEO} = \int_{X_n}^{X_p} \int_{X_n}^{\eta} C(t)dtd\eta \ . \qquad (33)$$

As previously stated, this model has not, as yet, been implemented in our analysis of the I^2L type structure. This is not intended to imply that we feel such a calculation is unimportant. During "up" operation substantial collector multiplication could occur; even at the low operating voltages of this semiconductor device. This calculation is suggested because a recent publication [15] indicated that open-base breakdown in I^2L devices is a problem of concern for device designers.

2.7 V_{EB} and Stored Intrinsic Base Charge

It has been shown that the minority carrier distribution within an intrinsic base layer can be approximated by the relation:

$$n(x) = \frac{J_n}{q\overline{D_n}C(x)} \int_{X_{p_1}}^{X} C(x)dx \ . \qquad (34)$$

For greater accuracy, we have introduced into Eq. 34 the average base region electron diffusion coefficient, where

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[15] J.L. Saltich, W.E. George, and J.G. Soderberg, IEEE Trans., SC-11, 478 (1976).

$$\overline{D_n} = \frac{kT}{q\left|X_{p_1} - X_{p_2}\right|} \int_{X_{p_1}}^{X_{p_2}} \mu_n(h)\,dh \ . \qquad (35)$$

From these expressions, the V_{EB} required to attain a given emitter junction current density is given by

$$V_{EB} = \frac{kT}{q}\, \ell n\left\{\frac{J_n}{q\overline{D_n} n_i^2} \int_{X_{p_1}}^{X_{p_2}} C(x)\,dx + 1\right\} . \qquad (36)$$

Our implementation of this model was based upon an assumption that I^2L "up" operation does not produce high minority carrier injection levels into the transistor base region. After studying the results of several calculations it was found that this assumption is sometimes unjustified; further details of this study are presented in Section 3. of the present report. As a consequence, a new model is being developed to replace Eq. 34 for V_{EB} calculations. Despite this deficiency in our model, it is shown (Section 3.3) that other concerns of I^2L analysis and design are far more important at the present time.

In addition to calculating V_{EB} (Eq. 36) this model also yields the stored charge due to minority carriers within the intrinsic base region:

$$\rho_{int} = \frac{J_n}{\overline{D_n}} \int_{X_{p_1}}^{X_{p_2}} \frac{1}{C(\eta)} \int_{X_{p_2}}^{\eta} C(t)\,dt\,d\eta \ . \qquad (37)$$

Further, from ρ_{int} we also obtain the intrinsic base region recombination current J_{ri}.

2.8 Extrinsic Base and Up Emitter Region Stored Charge

We next model a property of the I^2L transistor that is important to its switching speed: the stored extrinsic charge during "up" operation. Here we use relatively conventional assumptions concerning the associated mechanisms. It is assumed the extrinsic base region minority carrier current is attributable to the combined mechanisms of drift and diffusion,

$$J_n = qD_n \frac{dn}{dx} + q\mu_n n\xi(x) \ , \tag{38}$$

and that continuity of this injected electron current is governed by

$$\frac{dJ_n}{dx} = \frac{qn(x)}{\tau_n} \ , \tag{39}$$

where τ_n represents the base region minority carrier lifetime. This condition of continuity is recognized as the low injection limit of conventional SRH recombination processes.

After combining Eqs. 38 and 39 we obtain the differential equation

$$\frac{d^2n}{dx^2} + \frac{1}{C(x)} \frac{dC}{dx} - \frac{n(x)}{L_n^2} = 0 \ , \tag{40}$$

where the electric field $\xi(x)$ in Eq. 38 is obtained from the quasi-neutral approximation

$$\xi(x) = \frac{kT}{q} \frac{1}{C(x)} \frac{dC(x)}{dx} . \qquad (41)$$

In the past, two different approaches have been used to solve Eq. 40: first, an infinite series type solution [16] and, second, a finite difference type of solution. The first method requires a little more computer time, yet it does not exhibit the errors known to be encountered in any finite-difference type solution. The second method is computationally fast, it is easier to implement, although this technique can lead to round-off error, and instabilities, that sometimes produce problems. In our implementation of this model we adopted the finite-difference approach. It is planned at a later time to implement an infinite series method for solving Eq. 40 and, thereafter, draw comparisons between these two computational techniques.

Conventional methods have been employed to obtain this solution. Equation 40 is first written in its finite-difference form, yielding the well-known tri-diagonal matrix. Thereafter, this system of equations is solved using Gaussian elimination [17], and backward calculation of the resulting minority carrier (electron) distribution.

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[16] D.P. Kennedy and P.C. Murley, IRE Trans., ED 9, 136 (1962).
[17] C.E. Pearson, Handbook of Applied Math, Van Nostrand Reinhold, New York (1974).

Boundary conditions used for our solution of Eq. 40 are based upon an applied V_{EB} at the up emitter junction, and an infinite surface recombination velocity at the semiconductor-oxide interface. From previous calculations of this type [17], during "up" operation it was suspected that the "built-in" base region electric field was sufficient to keep an appreciable number of minority carriers from this interface region. For this reason, by assuming an infinite surface recombination velocity we are taking a most pessimistic view concerning the influence of the surface upon device operation.

An identical approach is used to calculate stored charge within the "up" emitter region of this structure. In our model we assume an infinite recombination velocity at the substrate-epitaxy interface. Calculations indicate that the quasi-neutral electric field produced by the buried layer negates any assumption concerning this interface region. Calculations indicate that near this interface we obtain minority carrier density that is 10^{40} to 10^{50} below that found near the "up" emitter junction.

After solving Eq. 40 and obtaining a predicted minority carrier distribution, the base region stored charge is obtained from

$$\rho_{ext} = q \int_{X_{p_2}}^{0} n(x)dx \qquad (42)$$

for the extrinsic base layer, and from

$$\rho_e = q \int_{X_{n_2}}^{W_{epi}} p(x)dx \qquad (43)$$

for the emitter region under "up" operation.

3.0 Analysis of the I^2L Vertical Transistor

Using the foregoing model, many important electrical properties of an I^2L type transistor can be readily established. Resulting from this study is a better understanding of I^2L operation, some insight into basic differences between this type device and conventional bipolar transistor operation, and an understanding of many associated problems relating to device fabrication. Thereby, a view is obtained of the capabilities inherent in this proposed modeling technique, and its potential value for modeling the influence of radiation induced mechanisms upon the electrical properties of an I^2L type semiconductor device.

Figure 7 illustrates the I^2L structure adopted for the present study; this structure is similar to that used in a previous investigation of I^2L operation [18]. The changes introduced here resulted from an initial evaluation of the previously used model; calculations indicated emitter to collector reach-through at equilibrium, a situation considered

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[18] J.A. Niehaus, Computer Aided Analysis of I^2L, Univ. of Ill. Report UILU-ENG 75-2224, Joint Services Contract DAAB-07-72-C-0259, Sept. 1975.

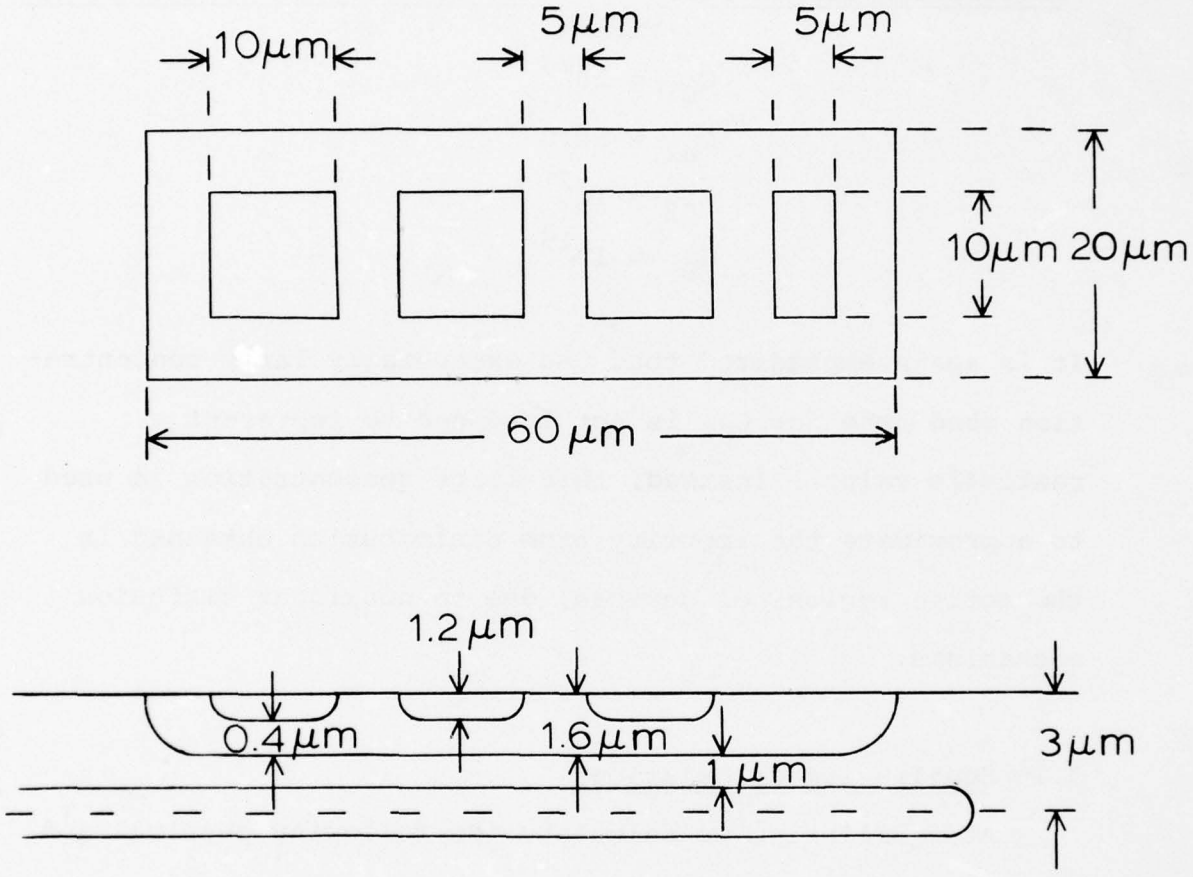

Fig. 7 Device Dimensions Assumed in this Analysis.

impractical. For purposes of illustration we have adopted the following impurity atom concentrations (atom/cm^3):

TABLE I

Fabrication Process Parameters Assumed for the Design-Center Device

$$C_{01} = 10^{23}$$
$$C_{02} = 5x10^{19}$$
$$C_{03} = 10^{21}$$
$$C_B = 10^{15}$$

It is again emphasized that the exceedingly large concentration used here for C_{01} is not intended to represent a realistic value. Instead, this large concentration is used to approximate the impurity atom distribution obtained in the active regions of devices, due to nonlinear diffusion mechanisms.

3.1 Equilibrium Calculations

At equilibrium we calculate the following physical and electrical characteristics for this illustrative I^2L transistor:

TABLE II

Equilibrium Characteristics for the Design-Center Device

Junction #1

X_{ne_1} = 1.149μm

X_{j_1} = 1.200μm

X_{pe_1} = 1.297μm

V_{eq_1} = 0.834 volts

C_1 = 0.014 Pfd

Junction #2

X_{pe_2} = 1.440μm

X_{j_2} = 1.600μm

X_{ne_2} = 1.960μm

V_{eq_2} = 0.695 volts

C_2 = 0.239 Pfd

Transistor

W_p = 0.400μm

W_e = 0.143μm

An observation from this calculation is the difference between the physical base width (W_p) and the electrical base width (W_e). In this particular structure only about 35% of the physical base region is charge neutral. This situation could produce a substantial fabrication reproducibility problem. For this reason, additional equilibrium calculations provide insight into the factors influencing these particular device parameters.

First, a design change was introduced by reducing C_{02} to 10^{19} atoms/cm^3, and maintaining all other parameters at their design center values, Table I. Resulting from this modification are the following characteristics.

TABLE III

Equilibrium Characteristics Assuming $C_{02} = 10^{19}$ atoms/cm^3

Junction #1

X_{ne_1} = 1.142μm

X_{j_1} = 1.200μm

X_{pe_1} = 1.325μm

V_{e_1} = 0.812 volts

C_1 = 0.011 Pfd

Junction #2

X_{pe} = 1.423μm

X_{j_2} = 1.600μm

X_{ne_2} = 1.950μm

V_{e_2} = 0.695 volts

C_2 = 0.236 Pfd

Transistor

W_p = 0.400μm

W_e = 0.098μm

This proposed modification produces only a small reduction of the junction space-charge layer capacitances (due to an increase of space-charge layer width), but it

does produce a large change of electrical base width. Specifically, reducing C_{02} from 5×10^{19} (atoms/cm^3) to 10^{19} (atoms/cm^3) reduces the equilibrium electrical base region from .143μm to 0.098μm; a reduction of about 31%.

It has been shown [19] that in an "up" direction of operation, emitter region back injection represents an important source of difficulty. In addition, it was shown that a buried layer can be used to minimize operating difficulties in this region; this layer reduces minority carrier recombination at the substrate-epitaxy interface. As a consequence, there is a tendency for I^2L engineers to move this buried layer very close to the adjacent p-n junction; this design method is intended to improve emitter injection efficiency in the "up" direction. For this reason, the consequences of such a design modification are established for this device at equilibrium.

Calculations were performed assuming the previously stated design-center fabrication parameters of this illustrative device, Table I, except the buried layer location was changed to 1.80μm. This design modification was accomplished by assuming in our model a reduction of epitaxial layer thickness--from 3.0μm to 2.2μm. Such a change would locate the buried layer close to the emitter junction space-charge layer edge during "up" operation.

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[19] F.M. Klaassen, IEEE Trans., ED-22, 145 (1975).

Calculations show that this change produced an increase of equilibrium space-charge layer capacitance (from 0.244 Pfd to 0.36 Pfd), with little significant change of electrical base width. Hence, from a device design point of view, a reduction of epitaxial layer thickness (from 3.0μm to 2.2μm) appears to be a reasonable design modification.

In a previous study [2] it was shown that epitaxial layer thickness represents an important source of fabrication process variability. From wafer to wafer an observable difference is found in the epitaxial thickness produced by a given reactor. Similarly, changes of epitaxial layer thickness can also be observed across any given slice of silicon produced in a given reactor. In this previous study a ±10% thickness change could be observed in measurements taken upon a large number of epitaxial layers. For this reason, it is important to consider the consequences of inadvertent epitaxial thickness changes upon this I^2L device, when it is assumed to be fabricated on a 2.2μm epitaxial layer.

Calculations were performed assuming the buried layer starts at X_{j_2} (1.6μ) and the epitaxial layer is 2.0μm thick. Following are the results of these calculations.

TABLE IV

Equilibrium Characteristics Assuming $W_{epi} = 2.0\mu m$; $X_{j_2} = 1.6\mu m$

Junction #1

$X_{ne_1} = 1.449\mu m$

$X_{j_1} = 1.200\mu m$

$X_{pe_1} = 1.297\mu m$

$V_{eq_1} = 0.834\mu m$

$C_1 = 0.014$ Pfd

Junction #2

$X_{pe_2} = 1.466\mu m$

$X_{j_2} = 1.600\mu m$

$X_{ne_2} = 1.621\mu m$

$V_{eq_2} = 0.732\mu m$

$C_2 = 0.799$ Pfd

Transistor

$W_p = 0.400\mu m$

$W_e = 0.169\mu m$

Table IV shows the reduction of epitaxial layer thickness produces an increase of impurity atom gradient and, as a consequence, a reduction of the equilibrium space-charge layer width ($X_{ne_2} - X_{pe_2}$). Therefore, this modification of the epitaxial layer thickness produces an increase of electrical base width (from 0.143μm to 0.169μm).

3.2 Reverse Biased "Up" Collector (V_{EB}=0)

Assuming a biasing voltage of 1.5 volts on the "up" collector, we calculate the following characteristics for this design center device:

TABLE V

Calculated Characteristics for Design-Center Device Assuming V_{CB} = 1.5V; V_{EB} = 0

Junction #1

X_{n_1} = 1.135μm

X_{j_1} = 1.200μm

X_{p_1} = 1.385μm

V_{CB} = 1.5 volts

C_1 = 0.008 Pfd

Junction #2

X_{p_2} = 1.440μm

X_{j_2} = 1.600μm

X_{n_2} = 1.960μm

V_{EB} = 0.000 volts

C_2 = 0.239 Pfd

Transistor

W_p = 0.400μm

W_e = .056μm

It should be observed that this calculation is based upon an "up" emitter that is at equilibrium (V_{EB} = 0).

The biasing voltage assumed on this "up" collector junction (V_{CB} = 1.5V) produces an electrical base width

that may be too small. One consequence of this situation is the overall reproducibility problem in the diffusion process [20]. For this reason, similar calculations have been made for this device assuming an "up" collector bias of 1.0 volts. Following are the results of such calculations:

TABLE VI

Calculated Characteristics for the Design-Center Device Assuming $V_{CB} = 1.0V$; $V_{EB} = 0$

Junction #1

$X_{n_1} = 1.138\mu m$

$X_{j_1} = 1.200\mu m$

$X_{p_1} = 1.355\mu m$

$V_{CB} = 1.000$ volts

$C_1 = 0.009$ Pfd

Junction #2

$X_{p_2} = 1.440\mu m$

$X_{j_2} = 1.600\mu m$

$X_{n_2} = 1.960\mu m$

$V_{EB} = 0$

$C_2 = 0.239$ Pfd

Transistor

$W_p = 0.400\mu m$

$W_e = 0.086\mu m$

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[20] D.P. Kennedy, IBM Journ., 5, 331 (1961).

From these calculations, a reduction of 0.5 volts bias on the up collector produces an increase of electrical base width (assuming $V_{EB} = 0$) from 0.056μm to 0.086μm. In a practical device fabrication situation it is indeed questionable that such a device would represent a practical design. Small inadvertent variations of boron impurity atom surface concentration could produce a condition of reach-through in this mode of operation.

3.3 Reverse Biased Up Collector--$V_{EB} \neq 0$

Assuming an up collector junction bias of 1.0 volts, we next calculate the V_{EB} required to attain a specified collector current.

TABLE VII

V_{EB} Calculations for the Design-Center Device

I_C/collector (μ-amps)	J_C (amps/cm^2)	V_{EB} volts
5.0	25.0	0.603
10.0	50.0	0.621
50.0	250.0	0.663
100.0	500.0	0.681
200.0	1000.0	0.699

Table VII illustrates a situation encountered in I^2L transistors that is not characteristic of traditional bipolar operation. The small impurity atom gradient at the up direction emitter places a limitation upon the minority

current density obtainable from this junction. This limitation arises from the small equilibrium voltage (V_{e_2} = 0.695 volts in our illustrative example). In recent publications [18-19] it was assumed that the up direction emitter junction would yield a current density of 1000 Amps/cm^2 with an applied V_{EB} of about 0.750 volts; these assumptions would be typical of the down direction emitter junction. In the up direction a similar current density might not be attained without specific design modifications.

In addition to the equilibrium junction voltage, another factor must be taken into consideration: up emitter junction space-charge layer contraction, due to an applied forward bias. A substantial increase of electrical base width results from the V_{EB} applied to the up emitter junction and, as a consequence, the up electrical base width is substantially wider than the down electrical base width.

Calculations show that by moving the buried layer slightly into the equilibrium space-charge layer of the up emitter junction, an increase is obtained in the built-in voltage. For example, from TABLE II, the equilibrium up emitter junction terminates at X_{n_2} = 1.96μm. A design modification placing X_{j_3} = 1.7μm (slightly inside the equilibrium space-charge layer), the equilibrium junction voltage is increased from 0.695 volts to 0.768 volts.

3.4 Electrical Base Width (V_C = 1.0 volt; J_C = 100 μ-amp/ Collector)

It was previously stated that a substantial change of electrical base width results from forward biasing the emitter junction. Assuming a collector current of 100 μ-amps, the following physical and electrical characteristics were calculated for this proposed design-center device (TABLE I):

TABLE VIII

Calculated Characteristics Assuming V_{CB} = 1.0 V; J_C = 100μa

Junction #1

X_{n_1} = 1.138μm

X_{j_1} = 1.200μm

X_{p_1} = 1.355μm

V_{CB} = 1.00 volts

C_1 = 0.009 Pfd

Junction #2

X_{p_2} = 1.596μm

X_{j_2} = 1.600μm

X_{n_2} = 1.610μm

V_{EB} = 0.681 volts

C_2 = 85.7 Pfd

Transistor

W_p = 0.400μm

W_e = 0.241μm

From TABLE VIII, when this I^2L device is operating in the up direction (J_c = 100μa) we have an electrical base width of 0.298μm, which is larger than encountered in traditional bipolar operation.

It should also be noted that this up emitter junction has a very large space-charge layer capacitance at this particular biasing voltage. It is suggested that this capacitance could have a significant influence upon the switching speed of an I^2L structure.

3.5 Intrinsic Base Region Stored Charge

Using this model, the intrinsic base region stored charge has been calculated throughout a wide range of collector currents. As expected, this stored charge is linearly dependent upon the collector current:

TABLE IX

Intrinsic Base Region Stored Charge (V_{CB} = 1.0 volts)

I_C/Collector (μ-amps)	J_C (amps/cm^2)	ρ_{int}/Collector (Pico-Coulombs)
5.00	25.0	3.1×10^{-5}
10.0	50.0	6.2×10^{-5}
50.0	250	3.1×10^{-4}
100	500	6.2×10^{-4}
200	1000	1.2×10^{-3}

Included in this model is the capability of calculating the minority carrier distribution between the emitter and

collector junctions. Figure 8 illustrates this calculated minority carrier distribution assuming a collector current of 100 μ-amps.

Figure 8 provides substantial insight into the influence of the "built-in" base region electric field. It has been suggested [21] that during up operation the "built-in" electric field in this device is directed to oppose carrier transport from the emitter to the collector. As a consequence, this "built-in" field is believed to produce excessive base region charge storage and, therefore, reduce the switching speed of I^2L structures. Figure 8 indicates that the stored charge in this intrinsic base region differs little from that of a homogeneous base device. As a consequence, it is difficult to understand how this particular stored charge mechanism could contribute to the switching speed problems associated with the I^2L technology.

3.6 Extrinsic Base Region Stored Charge

In the device we have selected for analysis, the "built-in" extrinsic base region electric field appears to be of significant advantage. In particular, this electric field tends to reduce the extrinsic base region stored charge and, thereby, reduces the base region recombination current. As a consequence, the extrinsic base region

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[21] C. Thornton, ECOM (private communication).

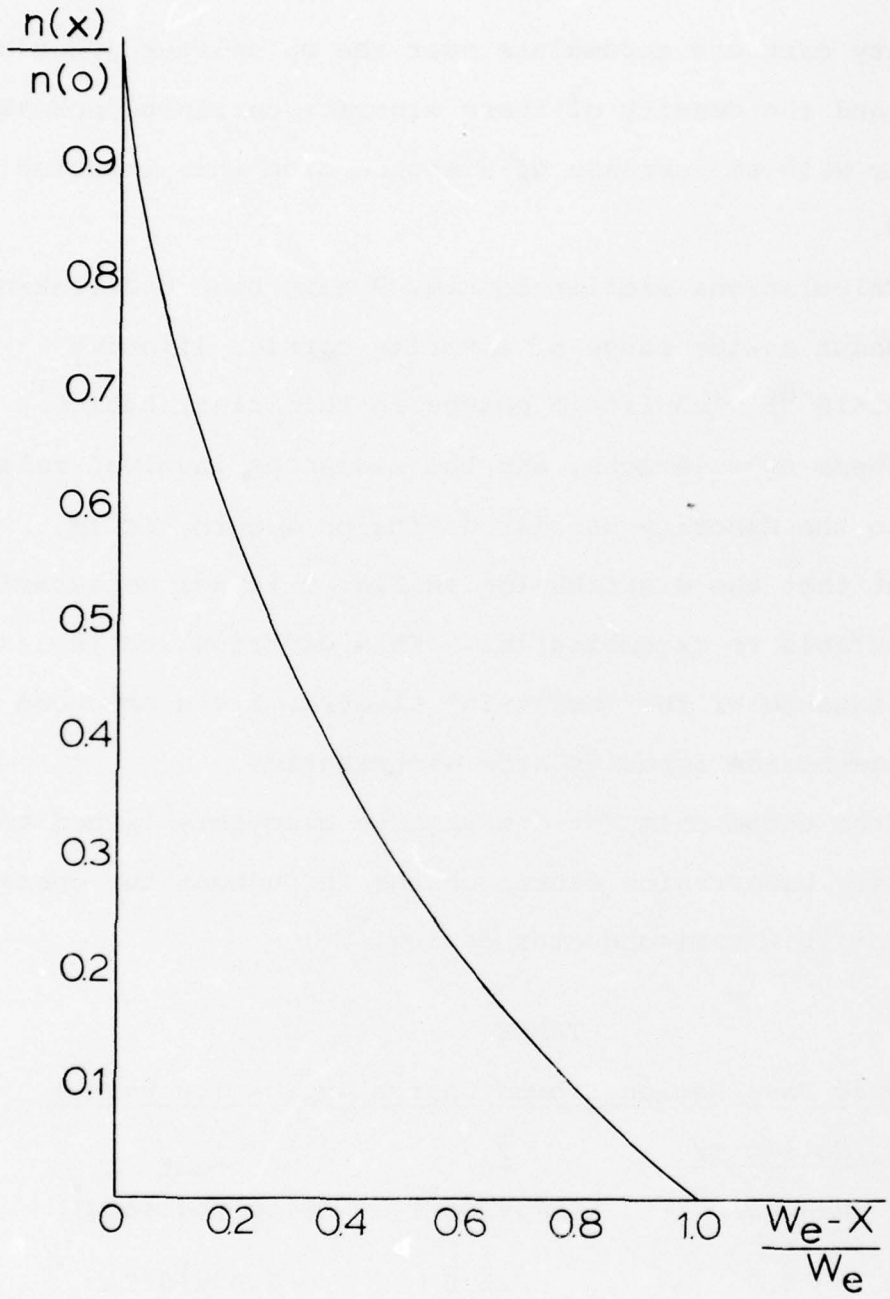

Fig. 8 Minority Carrier Distribution in Intrinsic Base Region during Up Operation (V_{CB} = 1.0V; J_C = 500A/cm^2).

minority carriers accumulate near the up emitter junction face, and the density of these minority carriers decreases rapidly with an increase of distance from this location, Fig. 9.

Calculations similar to Fig. 9 have been undertaken throughout a wide range of minority carrier lifetime ($10^{-8}<t<10^{-6}$) with little change in this distribution. From these calculations, and the distances involved relative to the minority carrier diffusion length, it is evident that the distribution in Fig. 9 is not necessarily attributable to recombination. This distribution is assumed a consequence of the "built-in" electric field produced by the base-region impurity atom distribution.

From these calculations we have also established the extrinsic base region stored charge throughout the operating range of this semiconductor device:

TABLE X

Extrinsic Base Region Stored Charge (V_{CB} = 1.0 Volts)

J_C/Collector (μ-amps)	J_C (amps/cm^2)	ρ_{ext} (Pico-Coulombs)
5.0	25.0	2.07×10^{-3}
10.0	50.0	4.15×10^{-3}
50.0	250.0	2.07×10^{-2}
100.0	500.0	4.15×10^{-2}
200.0	1000.0	8.314×10^{-2}

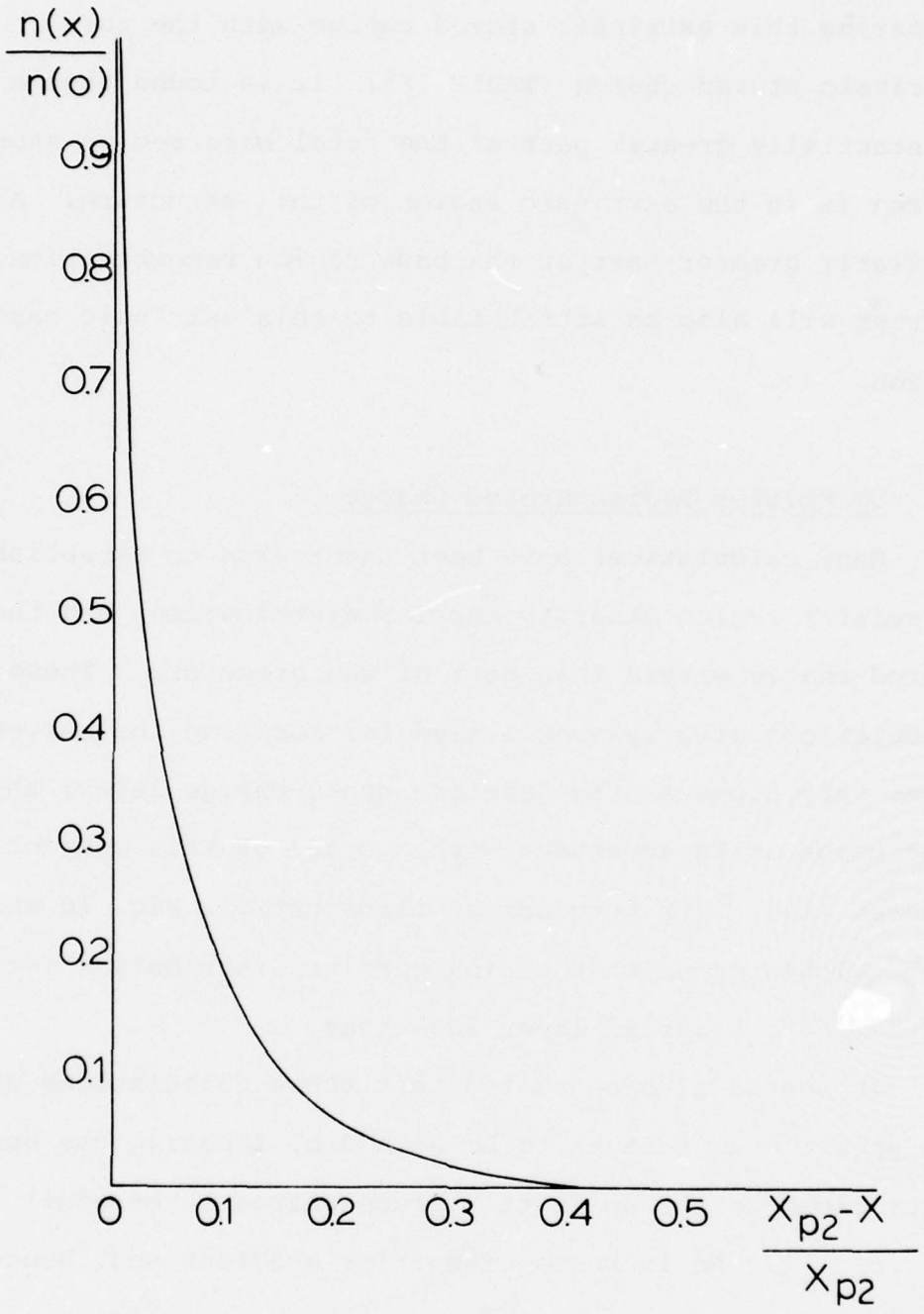

Fig. 9 Minority Carrier Distribution in the Extrinsic Base Region during Up Operation (V_{CB} = 1.0V; I_C = 100μa).

Comparing this extrinsic stored charge with the total intrinsic stored charge (TABLE IX), it is found that a substantially greater part of the total base region stored charge is in the extrinsic region of this structure. A similarly greater part of the base region recombination current will also be attributable to this extrinsic base region.

3.7 Up Emitter Region Stored Charge

Many calculations have been undertaken to establish the up emitter region minority carrier distribution, and the stored charge within this part of the structure. These calculations clearly show a need for locating the buried layer very close to the junction space-charge layer; this conclusion is in agreement with a study of this subject by Klaasen [19]. For purposes of illustration, Fig. 10 shows this calculated emitter region carrier distribution for four different buried layer locations.

It should also be stated that these calculations show two specific advantages to be gained by locating the buried layer close to the up emitter space-charge layer edge:

1. An increase of carrier gradient and, hence, a decrease in their integrated density.
2. Some decrease in the density of carriers at the space-charge layer edge, due to an increase of doping at that location.

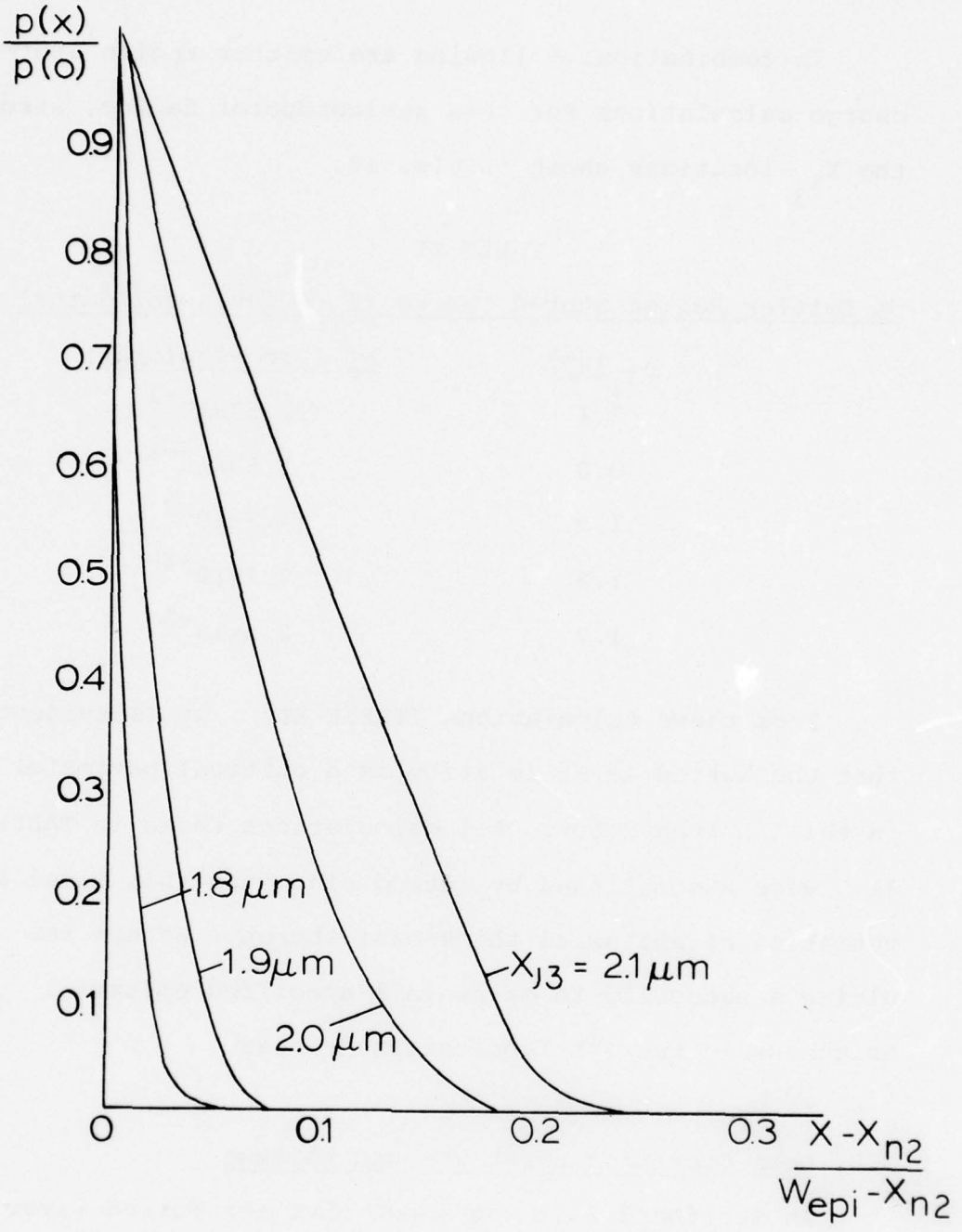

Fig. 10 Minority Carrier Distribution in the Up Emitter Region (V_{CB} = 1.0V; I_C = 100μa).

In combination, following are emitter region stored-charge calculations for this semiconductor device, assuming the X_{j_3} locations shown in Fig. 10.

TABLE XI

Up Emitter Region Stored Charge (I_c = 100μa/collector)

X_{j_2} (μm)	ρ_e (Pico-Coulombs)
2.1	2.57×10^{-1}
2.0	1.50×10^{-1}
1.9	4.7×10^{-2}
1.8	8.7×10^{-4}
1.7	2.2×10^{-5}

From these calculations (TABLE XI) it is evident that the buried layer location is a critical parameter in the I^2L transistor. All calculations shown in TABLE 11.0 were accomplished by introducing into this model a variation of epitaxial thickness; thereby, we are implying a necessity to maintain a specified epitaxial thickness in the I^2L fabrication process.

3.8 Down Operation Reach-Through Voltage

In Section 3.5 it was shown that the buried layer in an I^2L transistor must be maintained at a location that is relatively close to the up emitter junction. This particular requirement will significantly influence the down operation reach through voltage. For this reason, TABLE XII shows this calculated voltage throughout a range of buried layer locations:

TABLE XII

"Down" Operation Reach-Through Voltage

X_{j_3} (μm)	V_{RT} (volts)
2.1	16.3
2.0	14.1
1.9	12.6
1.8	10.9
1.7	9.51

From TABLE XII, there appears to be little difficulty associated with the down collector reach-through voltage. Throughout the range of interest for locating the buried layer, this reach-through voltage is shown to always remain above the normal operating voltage for this I^2L structure.

From this reach-through calculation, one might be tempted to use measurements of this parameter as an indicator of the distance $X_{j_3} - X_{j_2}$. It can be shown that this voltage is also dependent upon the base region impurities and, therefore, reach-through measurements are of little value for this particular evaluation technique.

3.9 Up Emitter Junction Avalanche Breakdown

In the particular structure chosen for analysis, reverse bias avalanche breakdown will not be observed; reach through to the up collector occurs at a lower voltage than avalanche breakdown. Nonetheless, avalanche breakdown measurements, in conjunction with their calculated values,

can yield important information. Such measurements are not undertaken on completed I^2L devices but, instead, upon test devices containing no up collector junction. Test devices of this type are usually constructed by subjecting them to all heat cycles used for completed device fabrication, yet without introducing the n-type up collector impurities. Table XIII shows the calculated reverse breakdown voltage for this type of I^2L test structure.

TABLE XIII

Avalanche Breakdown Voltage for I^2L Test Structures

X_{j_3} (μm)	V_{av} (volts)
2.6	30.2
2.1	26.0
2.0	23.1
1.9	20.1
1.8	17.3
1.7	17.2

These calculations show that the avalanche breakdown voltage is exceedingly dependent upon the buried layer location, relative to X_{j_2}. It can also be observed from these calculations that when $X_{j_3} \leq 1.8\mu m$, approximately, the structure undergoes breakdown in a manner similar to an abrupt junction--V_{av} is nearly independent of X_{j_3}.

Similar breakdown calculations throughout a range of base impurity atom density (and background doping) will

show the particular value of this type I^2L test structure. Specifically, calculations show that the up emitter avalanche breakdown voltage is relatively insensitive to all fabrication parameters except the distance $X_{j_3} - x_{j_2}$. As a consequence, this technique can be used to estimate the distance $X_{j_3} - X_{j_2}$ in experimental I^2L devices.

3.10 Up Operation Current Gain

Current gain calculations seldom offer the accuracy obtained from other device calculations. Little (or no) information is available concerning the minority carrier lifetime in any active region of a bipolar transistor. Therefore, for the present I^2L analysis a guess must be made concerning the minority carrier lifetime, although this guess can be drawn from experience with similar calculations for bipolar transistor operation. During bipolar transistor calculations, agreement between experiment and theory is seldom obtained without assuming a minority carrier lifetime of about 10^{-8} seconds. For this reason, a similar guess has been made for all active regions of the I^2L structure under consideration.

In our calculation of current gain we assume all collector junctions are connected together. Thus, the total current gain for this device is given by

$$\beta = \frac{3I_C}{I_B}$$

where I_C is the electric current/collector, and I_B is the total base current. In our calculation of I_B we take into account the total base region recombination current and the back injection current of the "up" emitter junction. Table XIV lists the results of this current gain calculation.

TABLE XIV

Current Gain for this Semiconductor Device (I_C = 100μa/collector)

X_{j_3} (μ-m)	β
2.6	2.1
2.1	11.0
2.0	15.6
1.9	34.5
1.8	67.7
1.7	69.0

Table XIV shows the reason particular emphasis has been placed upon the location of an I^2L buried layer, relative to the up emitter junction. These calculations clearly show that the current gain during up operation is critically dependent upon this buried layer location, and that this location must be controlled during device fabrication.

The foregoing calculations are not intended to imply that the present model considers all mechanisms influencing current gain in an I^2L structure. It is indeed obvious that peripheral regions of the up emitter will significantly influence this important device parameter. Nonetheless, these calculations do offer substantial insight into pro-

blems inherent to the design, development, and fabrication of I^2L type semiconductor devices.

4.0 Conclusions

Numerous conclusions can be drawn from the foregoing calculations of I^2L vertical transistor operation. These conclusions can be directed toward many aspects of modeling this semiconductor device; toward problems associated with device fabrication; and toward additional model developments for I^2L operation. It is suggested that these conclusions offer a greater level of accuracy than would be realized for other, new, semiconductor devices; this increased accuracy arises from the similarity between an I^2L vertical transistor and the conventional bipolar transistor. Many of the calculated properties for I^2L vertical transistor operation have been previously encountered during mathematical studies of the bipolar transistor.

From this analysis, in conjunction with similar studies for bipolar operation, it is suggested that the I^2L technology could introduce a greater level of engineering difficulty than the bipolar technology. It is also suggested that this increased level of difficulty could be particularly evident in the design and development of high-speed structures, containing a narrow base width. During down operation the I^2L vertical transistor is similar to a conventional bipolar transistor. For this reason, there is little reason to expect a significant simplification of the known problems associated with bipolar design, develop-

ment, and fabrication. In addition to these problems, many additional difficulties appear evident when considering the required operating characteristics for I^2L up operation.

The foregoing analysis implies that formidable problems could arise from the small "built-in" voltage associated with an up emitter junction. This "built-in" voltage is substantially less than that encountered at the down emitter and, in addition, the up emitter area is substantially greater than that of the down emitter. In combination, these inherent properties could produce important limitations in the electric current obtainable from a forward biased up emitter. An excessive forward bias of the up emitter, relative to its "built-in" voltage, could produce a reduced up emitter injection efficiency, and an excessive emitter junction space-charge layer capacitance.

Conclusions drawn from current gain calculations for up operation are consistent with other published investigations of this subject, both experimental and theoretical. These calculations indicate the up operation current gain of an I^2L structure will be greatly influenced by the distance between its up emitter and its buried layer. These calculations indicate that a relatively small increase of distance between the up emitter and buried layer could produce a substantial decrease of current gain.

As in bipolar transistor operation, the up emitter to buried layer distance also influences the reach-through

voltage during down operation, assuming space-charge layer interference. Therein a basic problem could be encountered in I^2L design. The need for a close proximity between the up-emitter and the buried layer (for up emitter injection efficiency) could produce an excessively small down operation reach-through voltage. Clearly, an extensive analytical study might be required during I^2L design as a means to obtain the necessary "trade-off" for satisfactory device operation.

Unlike the bipolar transistor, during up operation an I^2L vertical transistor exhibits large changes of electrical base width, with changes of emitter junction biasing voltage. This situation is attributable to the relatively small impurity atom density gradient associated with this junction. A small p-n junction impurity atom density gradient implies a relatively large equilibrium space-charge layer width; hence, forward biasing the up emitter junction produces a reduction of space-charge layer width, and an associated increase of electrical base width.

It is also suggested that an excessively small open-base breakdown voltage (BV_{CEO}) could represent an inherent difficulty associated with I^2L up operation. Although this parameter has not, as yet, been included in the present model, extensive understanding of this problem has been gained from previous studies of bipolar transistor operation. Briefly, open-base breakdown arises when carrier multiplication in the up collector, M, becomes excessive; instability usually occurs if

$$M = \frac{\beta+1}{\beta} , \qquad (44)$$

approximately. In bipolar transistor operation, Eq. 44 is usually satisfied when the applied collector junction biasing voltage is about 24% to 28% of the collector junction avalanche breakdown voltage.

The up operation collector junction usually exhibits a breakdown voltage of about 4.5 volts. As a consequence, an up collector biasing voltage of 2.0 volts could produce a substantial amount of carrier multiplication and, hence, a reduced BV_{CEO}. For example, Eq. 44 indicates that an M of only 1.5 would produce instability in an I^2L device exhibiting a current gain of 2; this magnitude of M could be very close to the operating range for an I^2L structure.

This model for I^2L operation has been used to emphasize the calculated properties during up operation. This model remains incomplete, yet in this incomplete stage of development substantial insight can be gained concerning problems of I^2L design and development. Because the model discussed here was drawn from previous studies of bipolar transistor operation, it is equally applicable to a similar study of down operation for an I^2L structure. It is suggested that all work necessary for such an extension could be completed in about two months of effort.

Including in this model the mechanisms associated with open-base breakdown (both up and down operation) represents a relatively trivial task. The computational tools needed

to calculate space-charge layer multiplication are already operational; one need only couple this calculation with the current gain.

As previously stated, during up operation the base region potential distribution is known to produce lateral variations of up emitter biasing voltage. This problem was previously encountered in the analysis of bipolar transistor operation: during studies of emitter crowding and collector junction saturation. A consequence of this previous experience is a knowledge of how to implement such mechanisms into a model of I^2L operation. Briefly, it is suggested that by coupling through base resistances one-dimensional lumped models for each intrinsic I^2L region, an adequate model could be obtained for variations of current gain between each up collector junction.

Although complicated in appearance, this proposed model is computationally simple and requires very little computer time. In reality, the entire model has been implemented on a small, programmable, desk calculator. Through previous experience with this model, in conjunction with a knowledge of relative computer speeds, it is estimated that the present model would require about 15-20 seconds CPU time on a large computer facility (typically IBM 360/85).

It is also suggested that this model is based upon important physical mechanisms associated with semiconductor device operation. For this reason, introducing into this model mechanisms associated with radiation damage would

not represent an unreasonable engineering problem. In combination, this model would offer an ability to inexpensively calculate the electrical and radiation properties of an I^2L vertical transistor. It is suggested that a computational tool of this type could be completed and made available to the semiconductor industry with about one additional year of development effort.

Glossary of Symbols

BV_{CEO}	Open base breakdown voltage
α	Common base current gain
β	Common emitter current gain
$C(x)$	Impurity concentration profile
C_o	Surface impurity concentration
C_B	Epitaxial layer impurity concentration
$C_{1,2}$	Junction capacitances
C_{eq}	Equilibrium junction capacitance
D_n	Electron diffusion coefficient
$\bar{D}_n$	Average electron diffusion coefficient in base region
$\mathcal{E}$	Electric field intensity
ε_o	Permittivity of free space
J_c	Collector current density
J_n	Electron current density
J_{ri}	Recombination current density in the intrinsic base region
k	Boltzmann's constant
K	Oxide thickness
κ	Relative permittivity of silicon
L	Impurity atom diffusion length
M	Carrier multiplication factor
μ_n	Electron mobility
n	Electron density
n_i	Intrinsic density
p	Hole density
ψ	Electrostatic potential
q	Electron charge (magnitude)
ρ_e	Stored minority charge in the "up" emitter region
ρ_{ext}	Stored minority charge in the extrinsic base region
ρ_{int}	Stored minority charge in the intrinsic base region
T	Absolute temperature
τ_n	Electron lifetime in the base region
V_a	Applied reverse bias voltage
V_{av}	Avalanche breakdown voltage

V_{CB}	Collector-base bias voltage
V_{EB}	Emitter-base bias voltage
V_{eq}	Equilibrium junction voltage
V_{RTO}	Reach through voltage, "up" emitter unbiased
V_{RTU}	Reach through voltage, "up" emitter forward biased
V_{RTD}	Reach through voltage, "down" emitter forward biased
W_e	Electrical base width
W_p	Physical base width
W_{epi}	Epitaxial layer thickness
x_{pe}, x_{ne}	Space-charge boundaries at equilibrium
x_{j1}	Location of "down" emitter-base junction
x_{j2}	Location of "up" emitter-base junction
x_{j3}	Location of buried layer edge
x_{n1}, x_{p1}	Space-charge layer boundaries of "down" emitter junction
x_{n2}, x_{p2}	Space-charge layer boundaries of "up" emitter junction

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