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X-BAND SOLID-STATE MODULE FOR AIRBORNE ARRAY RADAR APPLICATIONS--ETC(U)

MAY 77 R L ERNST, H C HUANG N00173-76-C-0383

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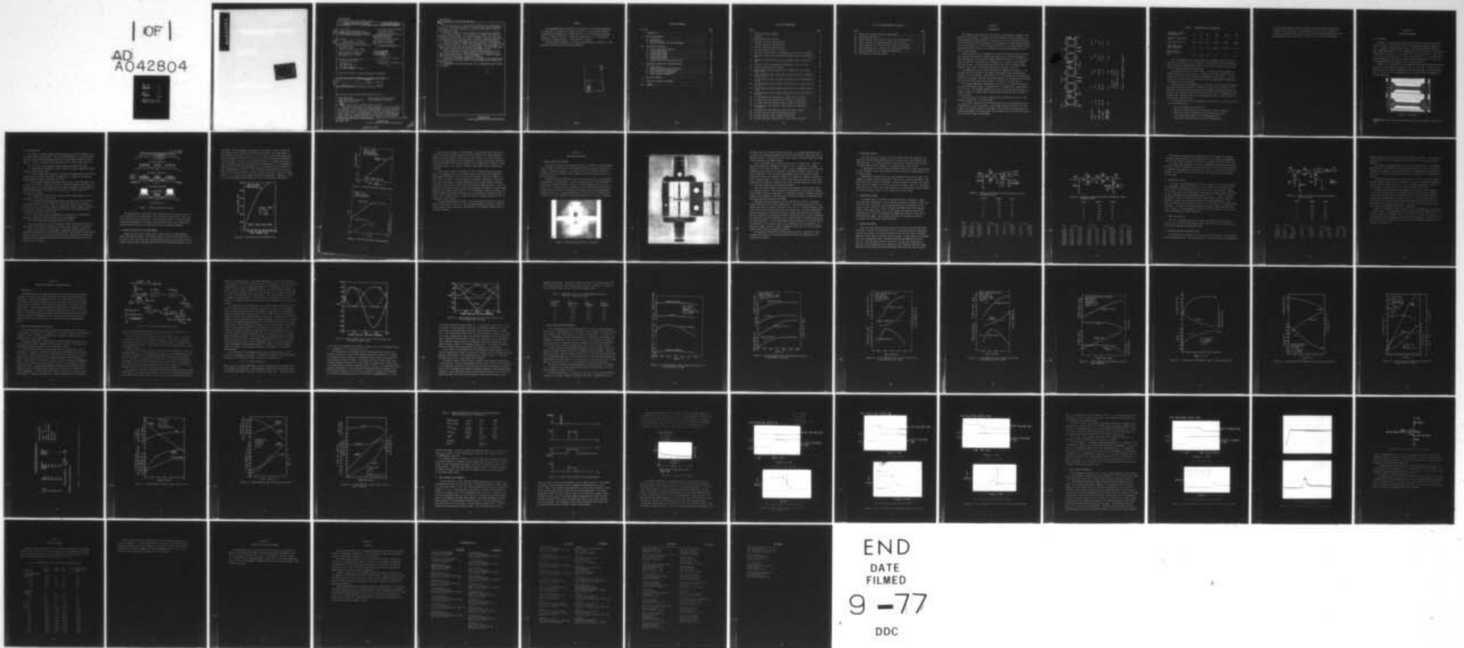

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This report describes the progess during the first six months of an 18-months' research program to develop amplifier modules suitable for airborne, active array radar applications. Using GaAs FETs as the active device, the design goal of these amplifier modules is an output power of 5 W with 25-dB gain over the 9- to 10-GHz frequency band. Extensive characterization of the amplifiers during pulsed operation is also part of this program.

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It is projected that the amplifier module will be configured as a cascade of five balanced stages. To achieve high overall amplifier efficiency, the output power of the FETs will be tailored to each of the amplifier stages.

New device types have been developed to the point of achieving greater than 1-W output. In particular, the 16-gate (16G) FET has achieved 1.03 W at 8 GHz, the 32G FET achieved 1.82 W at 8 GHz, and the 48G FET achieved 3.2 W at 4 GHz. Material parameters and processing techniques are being improved to give even better performance.

Amplifier stages have been fabricated using 2G, 4G single-cell, and 4G two-cell devices. When used as balanced pairs, more than 500 mW have been generated over the 9- to 10-GHz band. The development of higher power stages and the efficient packaging of a multistage amplifier will be major goals for the next six-months' period.

Phase sensitivity and phase transient measurements on the low-level stages indicate that FET amplifiers are good candidates for phase array applications. Phase measurements on a cascade of amplifiers will be done during the next six months.

Modulation techniques permitting a pulse to be superimposed upon the gates of the individual FETs in a cascade of balanced stages have been developed.

Twenty FETs have been delivered to the contracting agency during this period.

PREFACE

This Semiannual Report describes the progress of the research performed for the period 1 October 1976 through 31 March 1977, under Contract N00173-76-C-0383 at RCA Laboratories, Princeton, N.J., in the Microwave Technology Center, F. Sterzer, Director. The Project Supervisor is S. Y. Narayan and the Project Scientists are R. L. Ernst and H. C. Huang.

The Navy Project Engineer is E. Cohen of Naval Research Laboratory. This program is funded by Naval Air Systems Command.

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SECTION I

INTRODUCTION

The progress during the first six months of an 18-months' program is summarized in this report. The object of this 18-months' research program is to develop amplifier modules suited to airborne, active array radar applications. Using GaAs FETs as the active device, the design goal of these amplifier modules is an output power of 5 W with 25-dB gain over the 9- to 10-GHz frequency band. Extensive characterization of the amplifiers during pulsed operation is also part of this program.

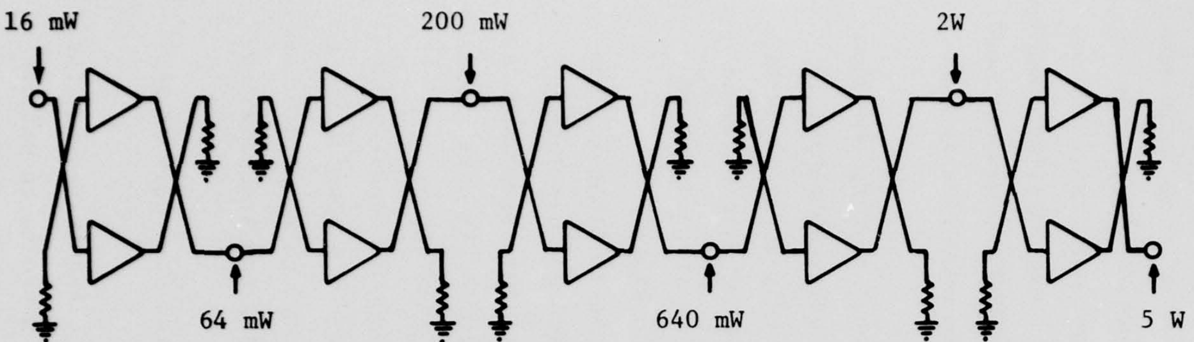
Based upon the current performance of devices developed so far, and upon the predicted performance of higher power FETs which are being developed in this program and in a concurrent program (#F33615-76-C-1144), it is projected that the amplifier module would be configured as a cascade of five balanced amplifier stages. The anticipated FET device types and the stage-by-stage budget of gain, power levels and efficiencies are shown in Fig. 1.

The dimensions of the various type FETs are summarized in Table 1. The two-gate (2G) and 4G devices use designs established by RCA and previously reported in the literature. The 8G device is a new design for which masks are currently being made. The 16G, 32G and 48G devices are currently under development, and the latest data will be given in Section II of this report.

The output stage power requirements shown in Fig. 1 should be satisfied by using two 48-gate devices. These devices are designed for a power level of 4 W at 10 GHz. An alternate approach is to use two 32G devices which are designed to operate at higher bias voltage levels, permitting the attainment of 3 W per device.

The 2-W output of the fourth stage should be satisfied by a pair of 16G devices designed for a 1-W power level.

Low current versions of the 16G devices are also good candidates for the 640-mW output of the third stage. An alternate approach would be to utilize a pair of 4G two-cell devices. Currently, these devices are giving more consistent performance than the 16G FET, which reflects the fact that the 16G FET is in an early stage of development.



DEVICE TYPE	2G	4G	16G	16G	48G
GAIN	6 dB	5 dB	5 dB	5 dB	4 dB
ADDED POWER	48 mW	136 mW	440 mW	1.36 W	3.0 W
DC POWER	267 mW	680 mW	2.2 W	5.44 W	12.0 W
POWER ADDED EFFICIENCY	18%	20%	20%	25%	25%

Total Gain : 25 dB
DC Power : 20.6 W
PA Efficiency: 24.3%

Figure 1. Overall amplifier approach.

TABLE 1. COMPARISON OF FET GEOMETRIES

Designation (number of gates/cell)	2G	4G	8G	16G	32G	48G
Number of cells/pellet	1	5	1	1	1	1
Gate width/cell (μm)	300	600	1200	2400	4800	9600
Gate length (μm) (mask dimension)	1.0	1.0	1.0	0.8,1.0	0.8,1.0	1.0,1.5
Design output power at V_{DS} = 8V (W)	0.15	0.25	0.5	1.0	2.0	4.0

The requirements of the second stage for a 200-mW output can ideally be satisfied by a single cell of a 4G device. Historically, these devices have had the greatest developmental effort, and can often be expected to achieve twice the power required for this stage.

The prime device for the first stage is a special 2G type designed to operate efficiently at low levels. A selected low current version of a 4G single-cell device is also a possible candidate for this stage. It is also feasible that devices which have recently become commercially available may find application in this stage.

Besides requiring development of new FET types and new amplifier modules, extensive efforts are needed to determine the pulse characteristics of the amplifiers with special attention to the intrapulse and interpulse phase properties. The amplifier rf and bias circuitry must then be configured to have optimal pulse characteristics for pulse widths between 0.2 and 20 μs and for duty factors as great as 50%.

This semiannual report will summarize the efforts for the last six months in the following areas:

- Device development and fabrication.
- Amplifier design techniques and measured circuit performance.
- Pulse measurement techniques for both amplitude and phase.
- Pulsed phase measurements of individual amplifiers.
- Bias circuit considerations for pulsed FET amplifiers.

Both the progress made in these areas and the problems which have been encountered will be detailed. The program plan for the next six months to alleviate the problem areas and to assure the satisfactory completion of the program design goals by the end of the contract will also be described.

SECTION II

DEVICE DEVELOPMENT

A. FET DESIGN

In order to achieve high overall amplifier efficiency, the output power of the FETs must be tailored for each of the amplifier stages as shown in Fig. 1. There are five different types of FETs being developed under this and a concurrent program.* The FET geometry was listed in Table 1. The design output power for the 2, 4, 8, 16, 32 and 48G structures are 0.15, 0.25, 0.5, 1, 2 and 4 W, respectively, for a drain bias voltage of 8 V. At higher drain bias voltages the output power increases almost proportionally to the drain voltage provided the performance is not thermally limited.

Figure 2 is a photograph of the largest FET which has 48 gates in parallel. There are 25 source pads, one gate pad, and one drain pad. Gold posts are plated on all the pads to accommodate flip-chip packaging, as will be shown in Fig. 7. The other FET configurations have a similar contact arrangement as the 48G FET device.

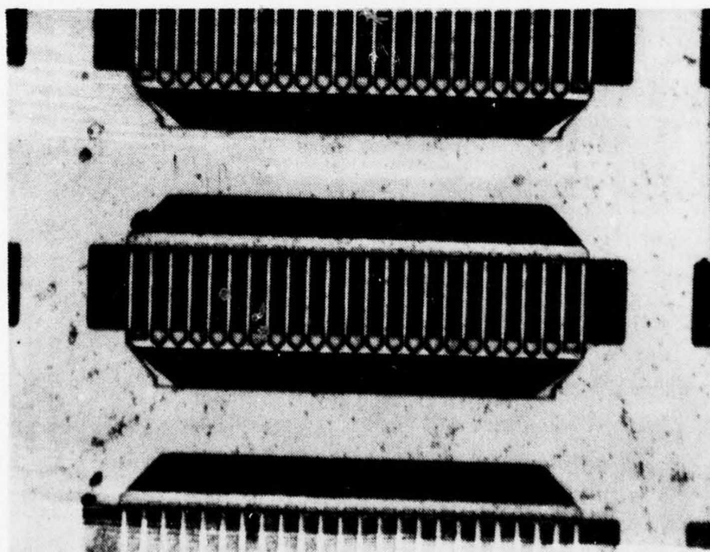


Figure 2. 48G FETs.

*"X-Band Power FET," Air Force Avionics Laboratory, Contract No. F33615-76-C-1144.

B. FET PROCESSING

The process technique employed at RCA Laboratories for FET fabrication is the self-aligned gate technique. The processed FET pellets are flip-chip packaged with sources thermocompression-bonded to a gold-plated copper heat sink (Fig. 7). Figure 3 summarizes the processing steps. The salient steps are:

(1) The n^+-face is metallized using titanium, platinum, and gold.

(2) Photoresist patterning is used to define the mesa. Mesas are formed using ion beam etching (IBE).

(3) A second photoresist pattern is defined which splits mesas into alternating source and drain electrodes. Openings (i.e., channels) in the photoresist between adjacent electrodes are 1.0 μm.

(4) The channels formed in the photoresist are cut using IBE down to the n-layer of the wafer. During IBE, source to drain saturation current (I_{DS}) is monitored and the process stopped when the channel thickness is appropriate for good FET performance. Typically, the value of I_{DS} at this point is 5 to 15 A/cm of gate width.

(5) A chemical "touch-up" etch is used to give enough undercut to prevent short circuiting in later steps.

(6) A second Ti/Pt/Au evaporation places the gate stripes into the channel formed by earlier steps. Since the source and drain pads are undercut, there is no short circuiting of gate to either pad. Also, because the material in the active channel is lightly doped ($\sim 10^{17}$ cm^{-3}), the titanium forms a Schottky-barrier contact [Fig. 3(c)].

(7) A protective layer of photoresist is deposited on the FET wafer. Holes are opened over the source region for post formation.

(8) 25-μm-thick gold is plated in the post region.

Excess metallization layers are removed. Figure 3(d) shows posts on our power FETs. The adhesion between the post and source contacts is excellent.

The n^+ layer thickness of the wafer is carefully chosen to allow gate metallization thickness of between 4000 to 6000 Å. About 5000 Å of gate metallization is desirable to decrease the effects of gate metallization resistance. Excessive gate metallization can lead to short circuits between the gate and source or drain contacts.

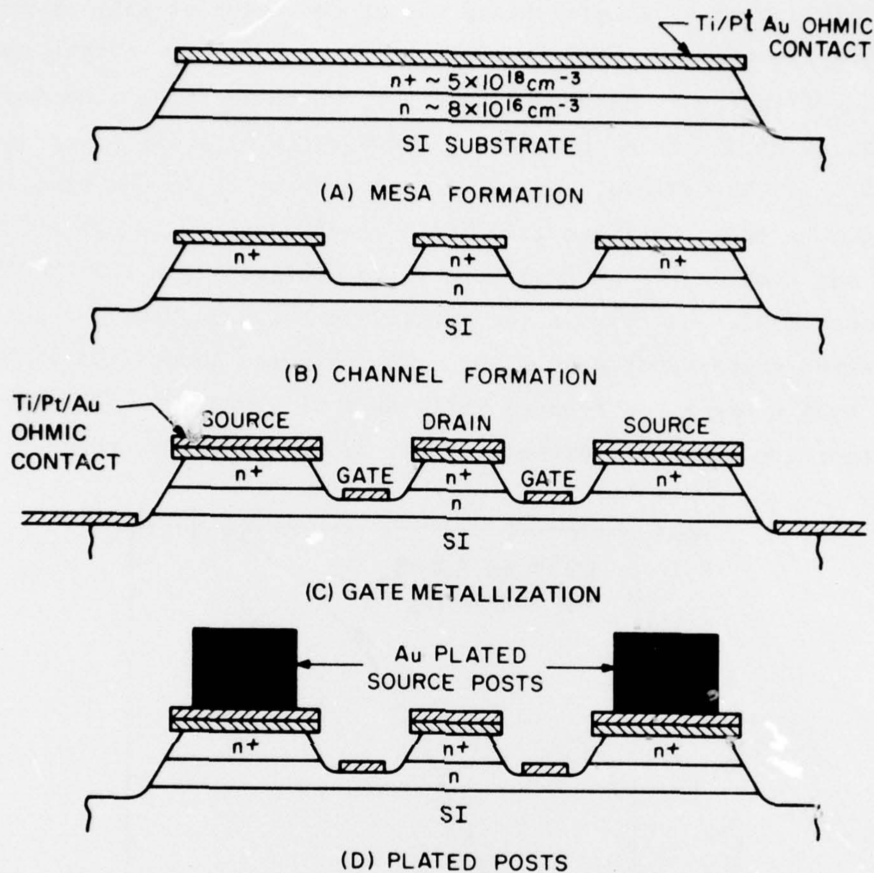


Figure 3. MESFET fabrication process.

The smallest gate length which can be achieved by this process is that set by the resolution of the photomask. Since ion-beam etching does not undercut, we can obtain 1:1 mask resolution to metal definition ratio. We have obtained excellent photomasks with 1-μm gate stripes and with these have obtained gate lengths between 0.5 and 1 μm by precise control of exposure parameters.

C. RESULTS AND PLANS FOR FET DEVELOPMENT

During the period from October 1976 to April 1977, more than 100 GaAs wafers have been processed. The 4G FETs provide a gain of about 8 dB, an output power of 150 to 300 mW, and a power-added efficiency up to 30% in the 9- to 10-GHz frequency band. The best gain observed from a 16G FET was about 7 dB in

this band. The power-added efficiency was of the order of 15%. Recently we have improved the efficiency of 16G FETs to about 20%. The output power of the 16G FET was typically about 0.7 to 1.2 W, which is within the design goal. The performance of 32G FETs thus far is about 1.8 W with 14% power-added efficiency at 8 GHz. The gain of the 48G FETs in the 9- to 10-GHz band is quite low. We believe that the large gate width of 48G devices is not a fundamental limitation and that useful performance can be achieved from the 48G FETs in this frequency band. Because of the relatively low gain from our initial 48G FETs, we tested those devices at 4 GHz. The gain was about 7 dB with an output power of 3 to 4 W and a power-added efficiency of about 30%. Figures 4, 5 and 6 are the representative performance of 16, 32 and 48G FETs, respectively.

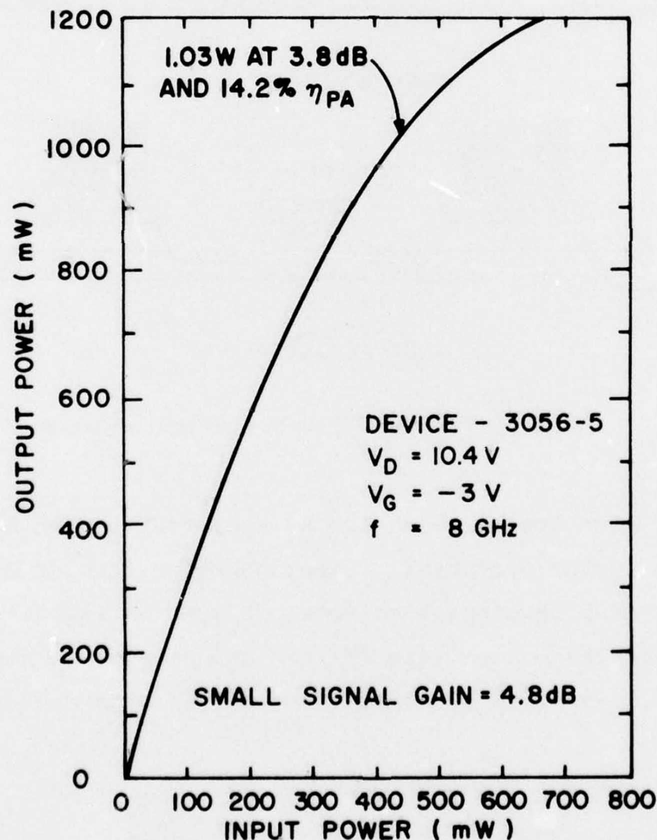


Figure 4. 16G FET saturation characteristic.

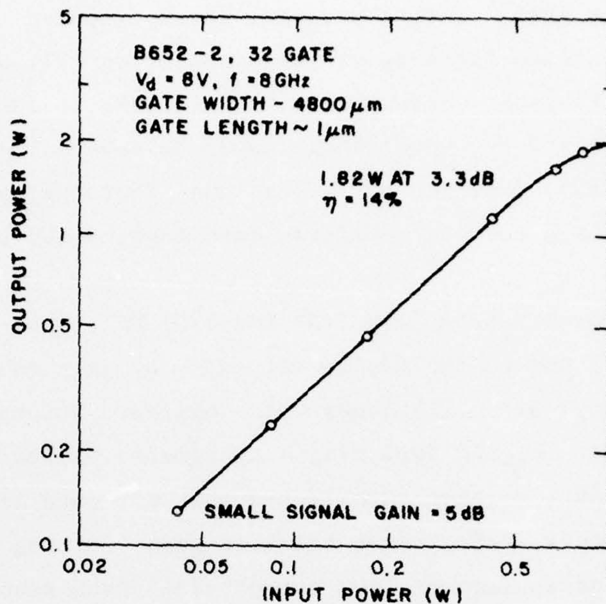


Figure 5. 32G FET saturation characteristic.

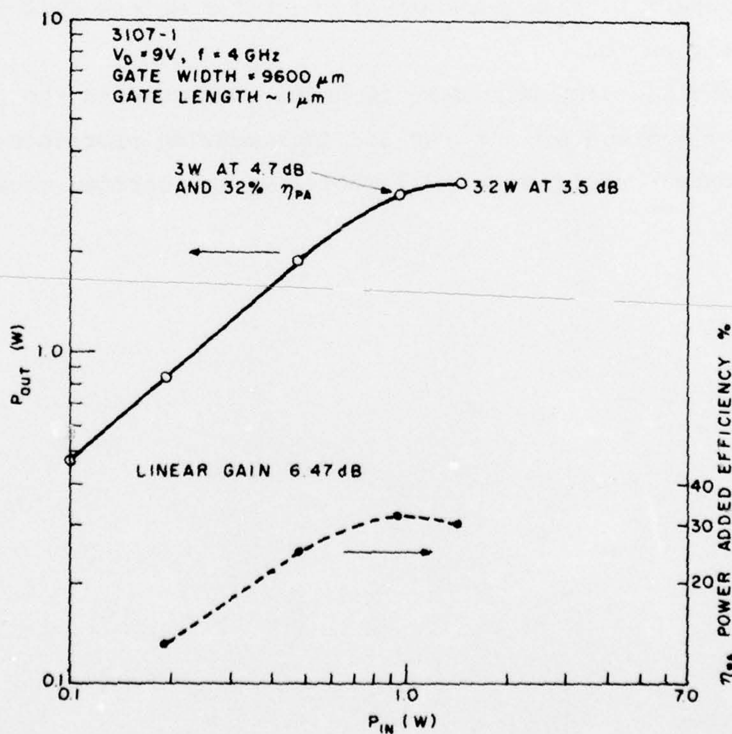


Figure 6. 48G FET saturation characteristic.

During the early phase of this program, we experienced some difficulties caused by the poor surface flatness of semi-insulating (SI) GaAs substrates. When the surface flatness is worse than a few microns, it is very difficult to define a 1-μm gate length by photolithography. We have solved this problem by carefully polishing the substrate surface at RCA Laboratories instead of using an outside vendor. As a result, submicron gate lengths can be consistently achieved.

These initial results from large (32 and 48G) FETs show that the output power is reasonably close to the design values. The gain (and consequently, power-added efficiency) are still lower than desired. The exact reason for this is not yet clear. We are beginning a systematic evaluation to determine the cause for low gain. We have established that our gate length is between 0.7 and 1.0 μm, and thus, this is not the main gain-limiting factor. Until recently, the best wafer surface quality was obtained from reactor B, while higher mobility was achieved with reactor A. By the addition of gas line filters, the wafer surfaces now obtained with reactor A are comparable to those obtained in reactor B. We expect to have a number of reactor A wafers evaluated by the end of the next report period.

The gate metallization thickness is being increased in the next series of wafers to between 0.6 and 0.8 μm. We are implementing procedures to routinely monitor ohmic contact resistance, Hall mobility, and carrier concentration in all device wafers.

SECTION III

AMPLIFIER DEVELOPMENT

A. OVERALL AMPLIFIER APPROACH

The overall amplifier configuration proposed to satisfy the program design goals consists of a cascade of five balanced amplifier stages as discussed in Section I and shown in Fig. 1. The device types which have been available during the first six months of this program for amplifier design are the 2, 4 and 16G varieties.

To design any given amplifier stage, the selected device is characterized by measuring its S-parameters. The carrier mounted device, shown flipped and mounted onto a copper pedestal in Fig. 7, is placed between two 50-Ω microstrip lines. The most accurate measurements are obtained when the microstrip characterization fixture incorporates a waveguide below cutoff configuration, as shown in Fig. 8, to suppress propagation in other than the quasi-TEM mode of microstrip. The S-parameters are then measured as a function of frequency

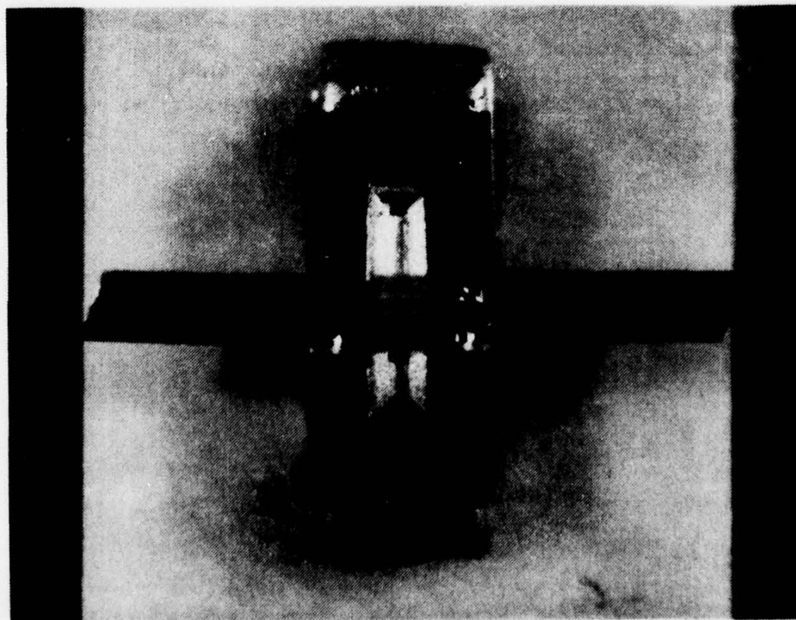


Figure 7. Flip-chip mounted FET on a carrier.

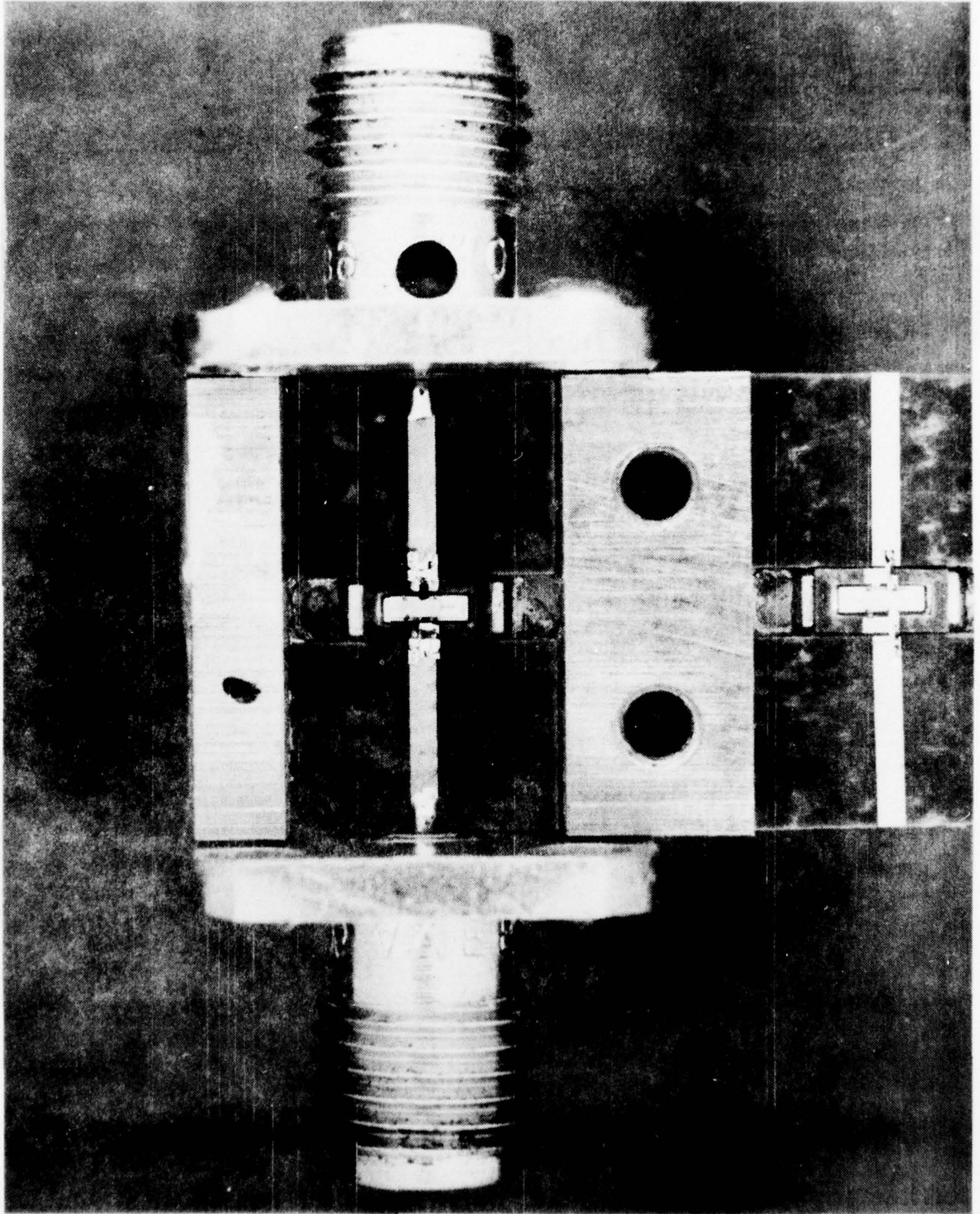


Figure 8. Flip-chip mounted FET in a waveguide below cutoff test fixture.

and gate bias by an automatic network analyzer. The computer-generated printout shows the scattering parameters and the predicted small signal gain for the measured device. These data are then used to select the proper amplifier stage network topology and element values.

First, the values of s_{11} and s_{22} are plotted on a Smith chart. Then the matching networks are designed for a match to 50 Ω, usually at the highest frequency in the band of interest. This is done to compensate for the intrinsic 6-dB/octave gain variation of the FET by introducing mismatch losses at the lower frequencies. The resulting higher VSWRs at input and output are compensated by the use of quadrature couplers to combine two identical amplifiers into a balanced stage. In this way each stage will have good input and output VSWRs and can be directly cascaded to the other balanced amplifier stages without interstage interactions and detuning effects.

Once the initial element values have been designed from the Smith chart, the complete network is then analyzed and optimized by an RCA computer program called COSMIC (Computer Optimization of Simulated Microwave Integrated Circuits). Usually the optimization constraints are selected to produce an amplifier with high flat gain and reasonably low VSWRs.

Amplifier protytype circuits are then fabricated on either 25-mil-thick alumina substrates or on 10-mil-thick Duroid. The alumina substrates are more durable and result in smaller circuitry, but in the 9- to 10-GHz frequency range some circuit elements may be too short to be practical. By using 10-mil-thick Duroid substrates, more reasonable circuit element dimensions can be achieved and the probability of dispersion effects in microstrip are virtually eliminated. The amplifier circuitry developed in this program utilizes alumina substrates as the preferred media. As the higher power stage utilizing the 16 and 48G devices are developed, it is possible that the low impedance levels presented by the device may demand the wider range of impedance levels that can be more readily achieved with the Duroid substrate approach.

The design and performance achieved during the first six months of this program with several of the required amplifier stages are summarized in the following subsections.

B. FIRST-STAGE DESIGN

The first stage is intended to achieve 64-mW output with 6-dB gain. An amplifier has been fabricated utilizing a 2G device which has achieved 25 mW with 5-dB gain. It is believed that by proper device selection two devices in a balanced amplifier will generate the needed power and gain levels.

In developing the second stage utilizing 4G FETs, low current devices which are not suitable in that stage would be ideally suited as a backup approach for the first stage.

Commercially available FETs also show potential for the first stage. For example, according to the manufacturer's data sheet, the Dexcel DXL-501 is capable of 50 mW at 12 GHz with 9-dB gain. Initial attempts to utilize this device show that it is capable of high flat gain, but its power output is a disappointingly low 10 mW. If this low output condition is consistent for several samples of this type number, then it is not usable in the first stage.

C. SECOND-STAGE DESIGN

The second stage is intended to provide 200 mW with 5-dB gain. Amplifiers have been fabricated on 25-mil alumina substrates utilizing a single cell of the 4G FET. The design and the computer-predicted performance for this stage are shown in Fig. 9. About 7-dB gain and 100-mW output have been obtained from a single stage. Two of these stages have been fabricated and integrated with a pair of interdigitated quadrature couplers to form a balanced amplifier stage. This balanced amplifier has achieved 204 mW with 6.6-dB gain and 10.3% power-added efficiency.

D. THIRD-STAGE DESIGN

The third stage should provide 640 mW with 5-dB gain and 20% power-added efficiency. Because the 16G devices are in a very early stage of development, the two-cell version of the more developed 4G FET has been used to fabricate amplifiers which might be suitable for this stage. Single stages of this amplifier use a topology and have a computer-predicted performance as shown in Fig. 10. The fabricated amplifier has about 7-dB gain and 270-mW output. When two of these amplifiers are combined to form a balanced amplifier stage, 518 mW with 6.9-dB gain and 19.8% power-added efficiency have been obtained.

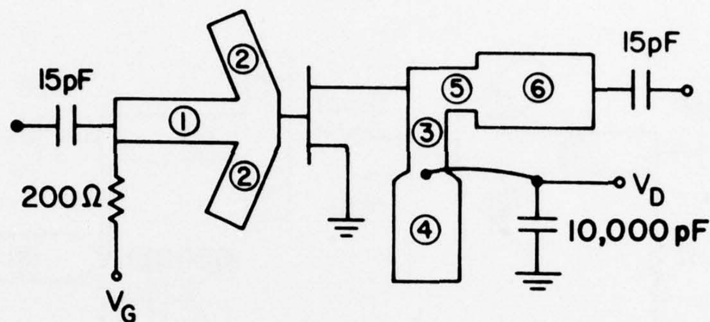


Figure 9. Amplifier design and predicted performance using a 4G-single-cell FET.

LINE #	LENGTH	WIDTH
1	175	27
2	64	12
3	30	6
4	117	50
5	30	30
6	80	40

FREQ	FGAIN PH		FLATNESS		S11,I.RC		S22,O.RC	
	X	1.000DB	X	1.000DB	X	1.000*	X	1.000*
9.000	8.408	166.51	.000	.00	.585	-148.91	.293	-149.19
9.200	8.609	146.85	.202	.20	.551	-174.58	.211	-175.36
9.400	8.628	127.69	.220	.02	.497	164.11	.165	136.46
9.600	8.544	106.61	.220	-.08	.471	136.71	.193	87.05
9.800	8.615	91.19	.220	.07	.478	121.87	.278	54.71
10.000	8.252	70.61	.376	-.36	.475	98.04	.326	32.82

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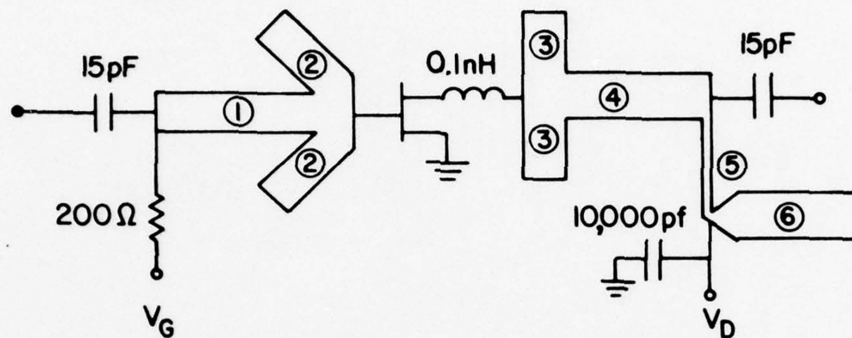


Figure 10. Amplifier design and predicted performance using a 4G-two-cell FET.

LINE #	LENGTH	WIDTH
1	190	18
2	65	24
3	66	39
4	144	53
5	127	5
6	117	50

FREQ	FGAIN PH		I VSWR O		S11,I.RC		S22,O.RC	
	X	1.000DB	X	1.000	X	1.000*	X	.977*
8.600	6.826	71.24	4.576	2.19	.641	-125.48	.364	3.30
8.800	7.605	53.14	3.867	1.85	.589	-151.34	.292	-10.40
9.000	7.979	37.28	3.503	1.63	.556	-170.66	.234	-25.96
9.200	7.986	17.61	2.775	1.40	.470	160.05	.163	-35.43
9.400	8.271	5.91	3.200	1.28	.524	150.23	.118	-45.92
9.600	8.525	-19.09	3.498	1.08	.555	104.51	.038	-23.86
9.800	7.873	-34.44	2.233	1.12	.465	82.72	.057	34.82
10.000	8.236	-51.26	3.540	1.22	.555	64.38	.097	44.52
10.200	7.890	-68.61	3.784	1.48	.582	44.37	.190	32.66
10.400	6.665	-86.79	3.286	1.67	.583	13.80	.244	12.89

This balanced stage has been cascaded with the 2G single-cell balanced amplifier stage developed for the second stage. This cascade has generated an output of 501 mW with 13-dB gain and 13.1% power-added efficiency at 9.25 GHz.

The power levels generated to date are slightly below the desired level of 640 mW. As more 4G wafers are processed, devices will be selected which should be capable of generating the desired output. Also, as the 16G devices are developed, low current versions should be excellent candidates for application on this stage.

E. FOURTH-STAGE DESIGN

The fourth stage should generate 2W with a gain of 5 dB. The representative performance reported in Section II for a 16G FET is 1.03 W with 4.8-dB gain and 14.2% power-added efficiency at 8 GHz. One of the earliest samples of this device has been incorporated into an amplifier design having the topology and computed-predicted performance shown in Fig. 11. Hoping to exploit the highest frequency potential of this device, a Duroid ring was used with the device carrier, and a Duroid substrate in the amplifier design. This earliest amplifier achieved 300 mW output with 6.5-dB gain and 5.5% power-added efficiency. As newer devices are being made available, newer amplifiers are being designed. If the impedance levels permit, this amplifier will be fabricated on 25-mil-thick alumina substrates.

F. FIFTH-STAGE DESIGN

The best performance for both 32 and 48G devices has been reported in Section II. As these devices become suitable for use in the 9- to 10-GHz frequency range, amplifier designs will begin.

G. PROBLEM AREAS AND ANTICIPATED GOALS

In designing the amplifiers for the second and third stages, one consistent problem became apparent. When the amplifiers are first turned on, the amplifier

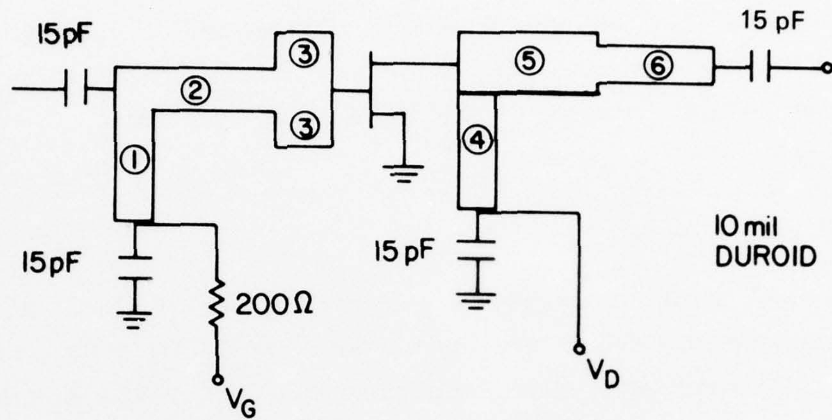


Figure 11. Amplifier design and predicted performance using a 16G FET.

LINE #	LENGTH	WIDTH
1	156	6
2	166	51
3	110	60
4	150	36
5	250	80
6	250	49

```
FREQ      S11,1.RC          FGAIN PH             FGAIN PH           FLATNESS
          X      1.000*     X       1.000DB      X      1.000DB     X     1.000DB
 8.500   .621     65.16    .292     -145.75     3.667   140.67     .000     .00
 9.000   .524     37.58    .349     -164.51     4.248   112.54     .581     .58
 9.500   .355      3.26    .350      167.03     4.053    79.39     .581    -.20
10.000   .306    -70.59    .314      157.80     3.673    45.50     .581    -.38
10.500   .571   -127.43    .198      116.26     3.893     4.84     .581     .22
NEXT?   (PAUSE):  *GO,??
```

response appears to be tuned about 1 GHz too high in frequency. This has been corrected by retuning the amplifiers with external chips to get the reported results.

This mistuned response may be due to any of several causes. The designs were based upon S-parameters of devices which have since burned out, and other devices which appeared to have almost identical S-parameters were substituted in the circuit. The difference in devices may be a major cause of the detuned response.

In characterizing the FETs, it is necessary to specify a reference plane extension from the location of an SMA short circuit used during the calibration of the automatic network analyzer. If the specified extension is a little shorter than the correct value, the observed detuning will occur.

Another area for amplifier improvement is that of efficient packaging. So far, all alumina stages use substrates which are 300 mil wide. Balanced stages therefore must be at least 600 mil wide. The way we have initially packaged the cascaded balanced stages results in a total amplifier width of two inches. Our review of this package shows many wasted areas, and it is believed that an overall width closer to one inch should be realizable, and that some of the mounting plates can be eliminated.

Amplifier development efforts during the next six months will concentrate on several areas: the amplifiers which have already been developed will be optimized by selection of better devices; reduction of the need for tuning of the amplifiers; and, packaging in the most efficient manner. As the 16, 32 and 48G devices become available, the fourth and fifth amplifier stages will be designed and fabricated.

SECTION IV

AMPLIFIER PULSED PHASE CHARACTERIZATION

A. INTRODUCTION

The application of FET amplifier modules to airborne, active array radar applications requires that these modules have extensive pulsed phase characterization. Because the microwave power FET is a new device, it is necessary to determine if any phase limitations in the pulse mode exist which would make these devices not suitable for the intended application. To obtain these required data, a pulsed phase measurement technique which has high resolution, high accuracy under a variety of amplitude conditions, and a fast rise time is needed. Once the extensive pulsed phase measurements have been done, biasing and pulse modulation techniques must be developed which permit the FETs to operate at their full potential and are compatible with the program design goals.

B. PULSED PHASE MEASUREMENT TECHNIQUES

Any phase measurement technique requires that the phase of an rf signal at the output of an amplifier be compared to a reference signal at the identical frequency. This is usually accomplished by coupling the reference and test signals from the same rf generator.

The phase bridge used in this program is shown schematically in Fig. 12. Using standard waveguide components, this bridge is capable of measuring both amplitude and phase responses in both pulsed and cw modes.

In the particular phase bridge fabricated at RCA Laboratories, the rf generator is a klystron. Because all pulsed phase measurements are done with a cw carrier, sweep oscillators and traveling-wave-tube amplifiers are dedicated to test benches used for swept amplitude response and power measurements. The output of the klystron is pulsed by using a standard PIN modulator because direct modulation of the klystron reflector causes frequency changes during the pulse. A high-quality isolator is used at the klystron output to guarantee that the frequency remain absolutely constant and is unaffected by the PIN modulator. A 10-dB directional coupler is used at the output of the PIN modulator to monitor frequency and rf pulse amplitude on an oscilloscope.

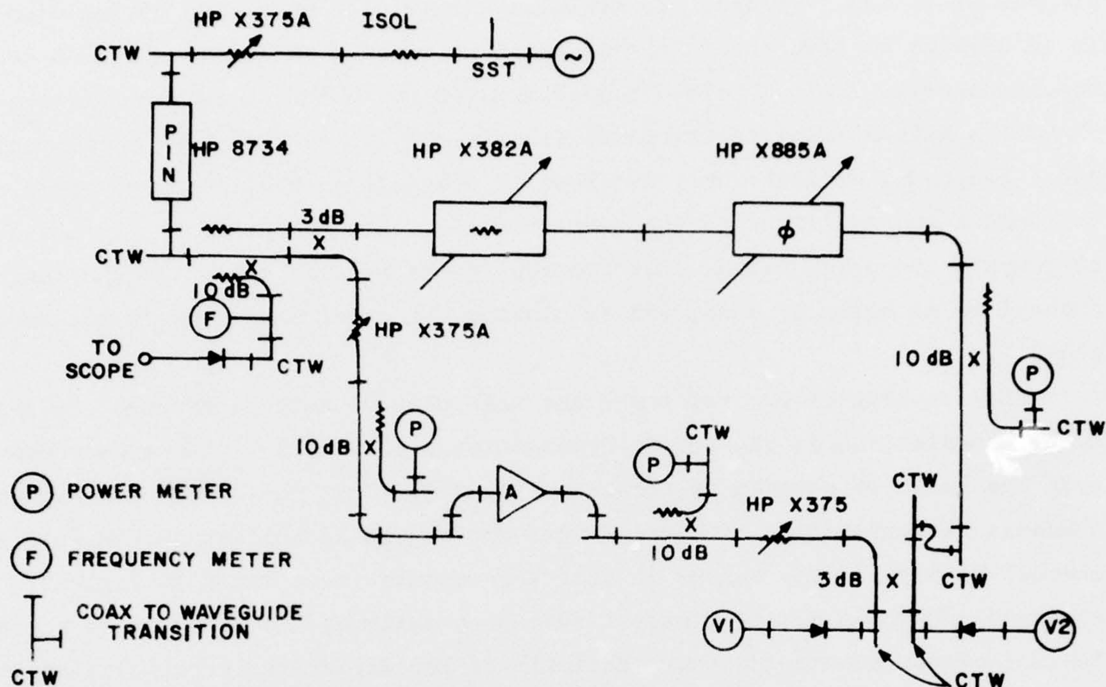


Figure 12. Pulsed phase measurement bridge.

By simply disconnecting the modulator from its pulse driver, which is not shown in Fig. 12, the bridge can be used in a cw mode.

The rf is split into two channels by using a 3-dB coupler in the form of a short-slot hybrid. One output, to be used as the "reference channel," goes through a rotary vane attenuator and a phase shifter to provide any desired amplitude and phase. This reference power is monitored through a 10-dB directional coupler.

The other 3-dB coupler output is used as the "test channel" to drive the amplifier under test. Ten-dB directional couplers are used immediately before and after the amplifier to respectively monitor its input and output power levels. The gain is calculated from these data. Level-setting attenuators used before and after these couplers permit the power input to the amplifier to be varied as desired, while ensuring that the power rating of the crystal detectors used at the end of the phase bridge is not exceeded.

The outputs of the test and reference channels are combined through another 3-dB coupler. The outputs of the coupler are detected, and these detected outputs, shown as V1 and V2 in Fig. 12, are connected to a differential amplifier

plug-in of an oscilloscope. To minimize ambiguities on the resulting display, it is helpful to have the reference and test signals arrive at the 3-dB coupler simultaneously. This is closely approximated by including in the reference channel a pair of coax to waveguide transitions, denoted as CTWs in Figure 12, and a length of coaxial cable as close as possible to the length of cable used to connect the amplifier to the test channel. This feature makes it possible to compare the phase response of two amplifiers by placing one in the test channel as is normally done, and by placing the other amplifier in the reference channel.

The coupling of the reference and test channel outputs through the 3-dB hybrid coupler causes the two detector outputs at V_1 and V_2 to be dependent upon the relative phasing of these two signals. When the test and reference channels are maintained at equal levels and the phase shifter in the reference channel is varied, the change in detector outputs is as shown in Fig. 13. As expected, when one detector output reaches a maximum, the other is at a minimum. Because of the square-law characteristic of the detectors, especially at small signal levels, the minimums are very broad, and the determination of the phase shifter setting which gives the exact minimum is very uncertain. If the difference in detector outputs is measured, which is accomplished by the differential plug-in of the oscilloscope, the zero voltage setting can be determined with high precision. As Fig. 13 shows, the minimum output of a single detector occurs at a point of zero slope, while the zero crossing of the differential output occurs at a point of maximum slope. Thus, the differential output measurement gives maximum sensitivity to phase variations, whether caused by changes in phase shifter settings or by changes in the amplifier phase response.

The differential phase bridge method has the advantage that it is not sensitive to amplitude variations. A theoretical analysis of the phase bridge shows that its differential output is given by the expression:

$$V_1 - V_2 = 4V_rV_t \sin(\theta_1-\theta_2),$$

where V_r and V_t are the magnitudes of the rf voltages from the reference and test channels, respectively. This expression shows that the difference output can be zero when either V_r or V_t or $\sin(\theta_1-\theta_2)$ equals zero. This shows that

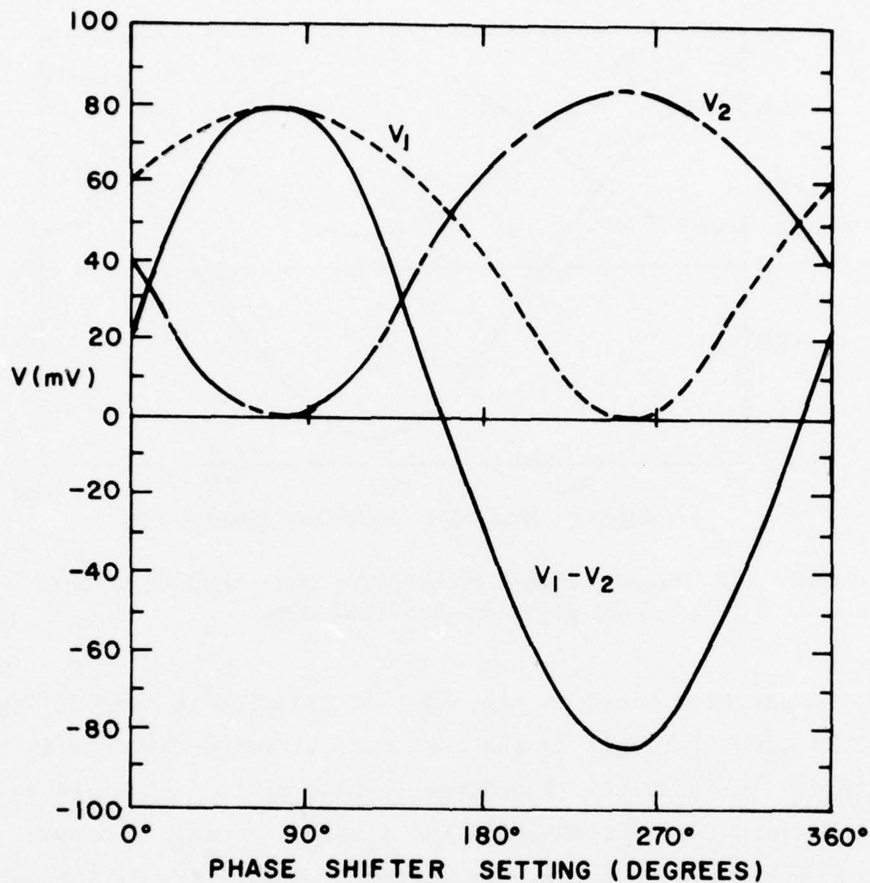


Figure 13. Phase bridge detector outputs with reference and test arms at equal levels.

a null will occur whenever the difference angle, $\theta_1-\theta_2$, is an integer multiple of π, independent of the values of V_r or V_t.

The independence of the phase bridge to amplitude variations has been tested by varying one of the level setting attenuators in Fig. 12. By using an automatic network analyzer, the variation of phase shift as a function of the attenuator setting is known. The change in detector outputs when the attenuator immediately ahead of the 3-dB coupler is changed from a 0-dB setting to a 10-dB setting is shown by comparing Figs. 13 and 14. From separate network analyzer measurements, it is known that the amplitude really changes 7.52 dB and the phase changes by 57.3° for this particular attenuator and frequency. All the detector patterns in Fig. 14 are shifted by approximately 57° to the

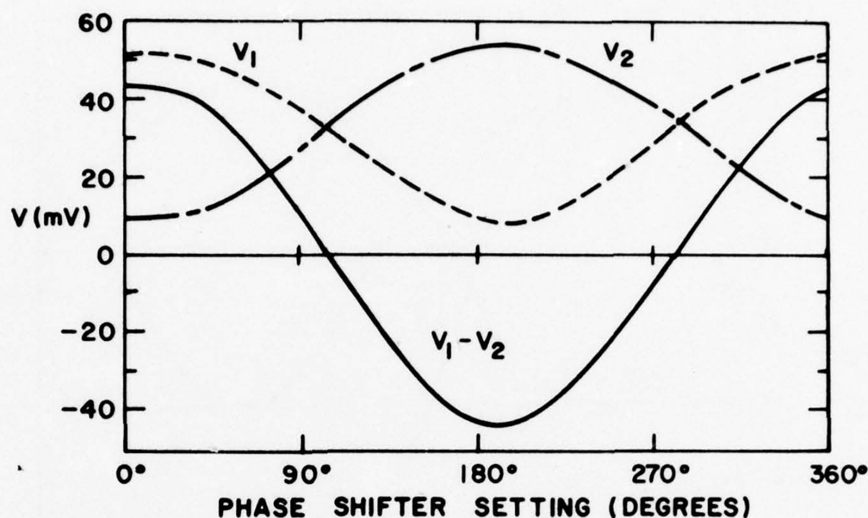


Figure 14. Phase bridge detector outputs with reference arm 7.5 dB greater than test arm.

left from the patterns shown in Fig. 13. It can also be seen in Fig. 14 that the effect of unequal levels in the test and reference channels is to cause the outputs of the individual detectors to have minima which are no longer zero. The differential output still has a zero crossing. However, the slope at the zero crossing and, hence, the vertical sensitivity of the oscilloscope used to measure the differential output, is a function of the rf amplitudes. Thus, using the highest level of rf compatible with the limitations of the detector diodes results in the greatest sensitivity. The various attenuators within the phase bridge setup permit this criterion to be satisfied.

The rf amplitude independence of this differential phase bridge is verified by varying the attenuator settings and comparing with the automatic network analyzer measurements. The resulting data are shown in Table 2. Excellent agreement occurs over a wide range of attenuation.

The phase bridge can also be used to measure pulse amplitude response of an FET amplifier. This is accomplished by adjusting the rotary vane attenuator in the reference channel arm to the MAX setting, which corresponds to greater than 75 dB of attenuation according to separate automatic network analyzer measurements. This effectively turns off the reference channel so that the only signal arriving at the two crystal detectors comes from the output of the

amplifier under test. The function selector switch on the front panel of the differential amplifier oscilloscope plug-in is used to display the output of either detector rather than the difference between them.

TABLE 2. COMPARATIVE PHASE SHIFT MEASUREMENTS OF HP X375A (Inv. No. 3-5654) Attenuator

Attenuator Setting (dB)	True Attenuation (dB)	Δ Ø Bridge (degrees)	Δ Ø Analyzer (degrees)
1	0.84	9.5	10.5
5	3.59	33.5	33.4
10	7.52	59.0	57.3
15	11.67	80.2	77.7
20	16.01	97.0	94.5

C. PHASE SENSITIVITY MEASUREMENTS

For the intended phase array application, it is vital to know the phase sensitivity of the amplifiers to variations in such parameters as drain voltage, gate voltage, power input level, load VSWR, and temperature. It is also essential to determine that the phase sensitivities reproduce consistently from amplifier to amplifier. Thus, it will be assured that the phase tracking of amplifiers used in a phase array will be maximized by driving all amplifiers from the same gate and drain voltages and at the same input power levels.

To date, some phase sensitivity measurements have been done on prototype amplifier stages developed from 2G, 4G (single cell) and 16G FETs. This has been done to give early indication if there are any major phasing problems with the FET amplifier approach. The resulting data does not show any fundamental limitations with this approach. More detailed and finalized data will be taken when the final versions of the various amplifier stages are developed.

The details of the various measurements are plotted in Figs. 15 through 26. A summary of the various phase sensitivities with references to the relative figures is given in Table 3.

For the 2G amplifier, it is noted that the sign of the phase sensitivity relative to the drain voltage is dependent upon the rf signal level, as is

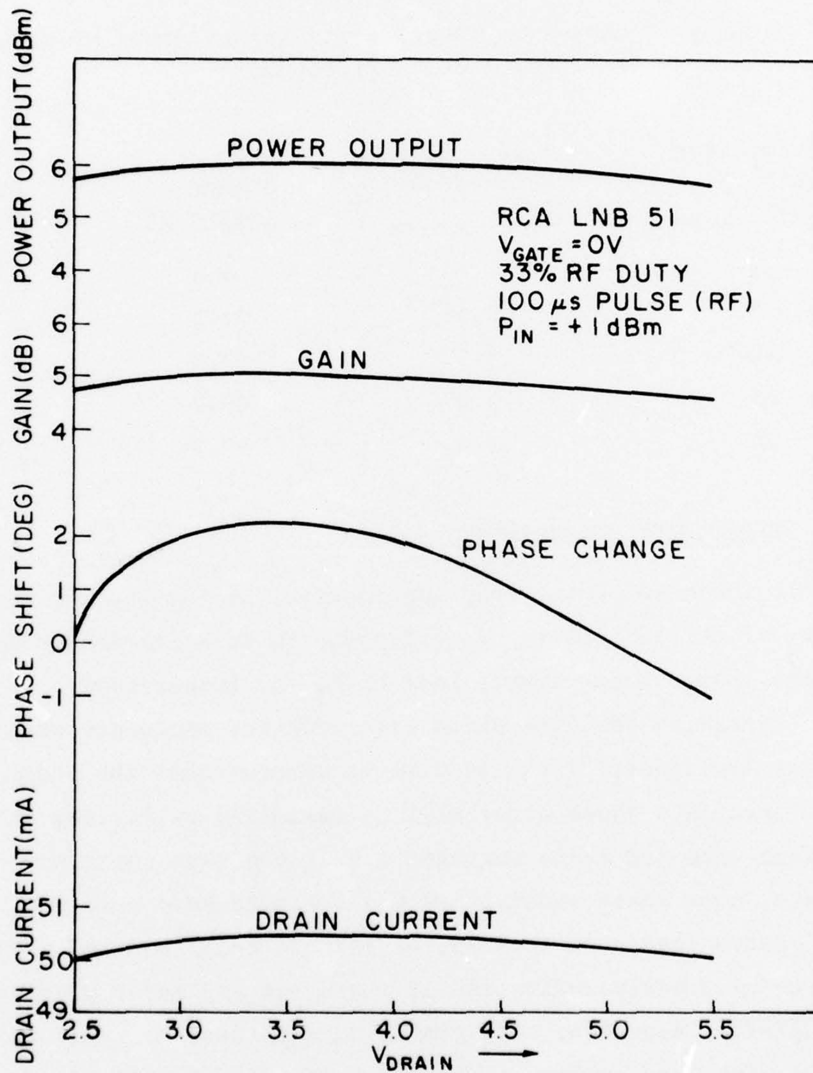


Figure 15. 2G FET amplifier drain voltage sensitivities at an input power of +1 dBm.

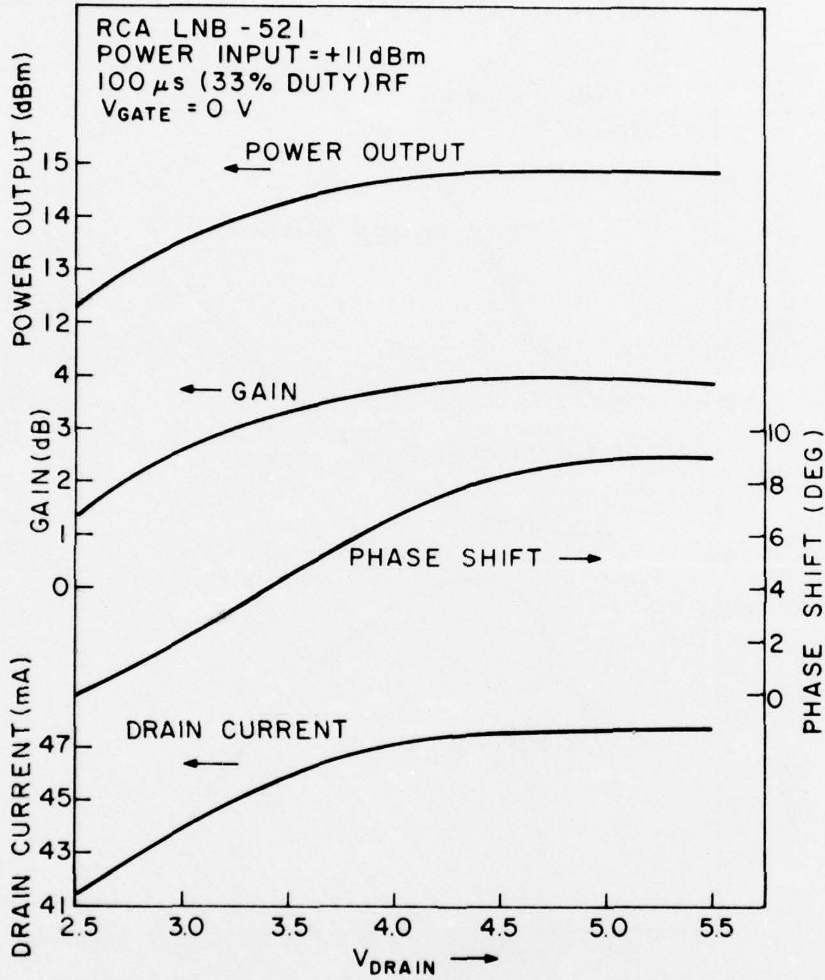


Figure 16. 2G FET amplifier drain voltage sensitivities at an input power of +11 dBm.

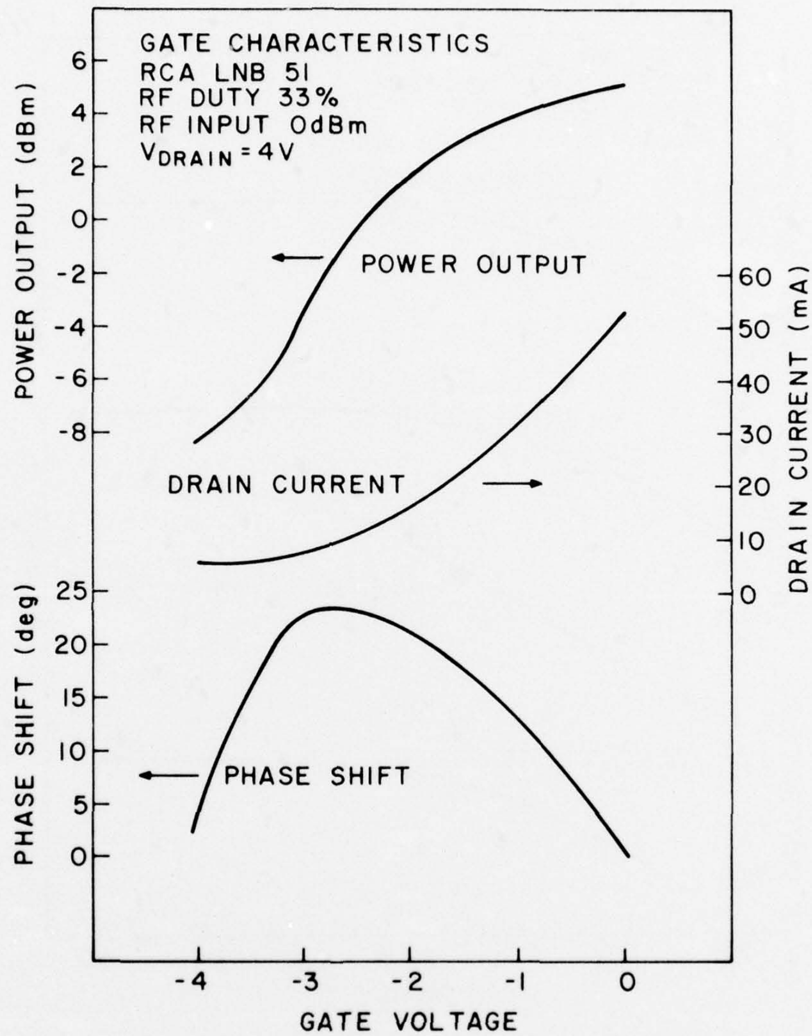


Figure 17. 2G FET amplifier gate voltage sensitivities at an input power of 0 dBm.

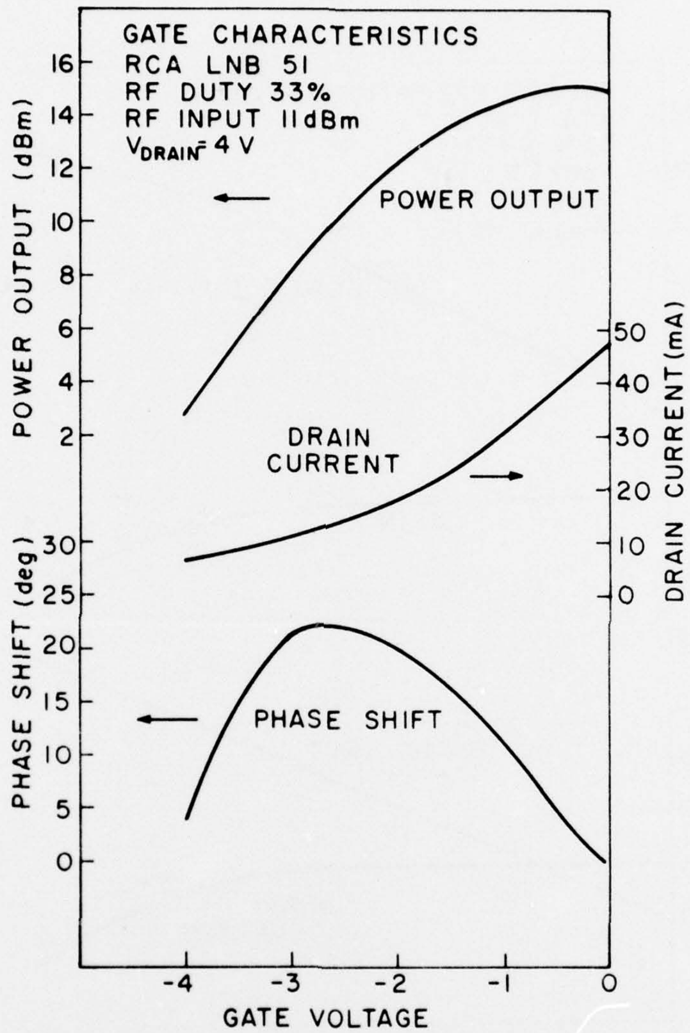


Figure 18. 2G FET amplifier gate voltage sensitivities at an input power of +11 dBm.

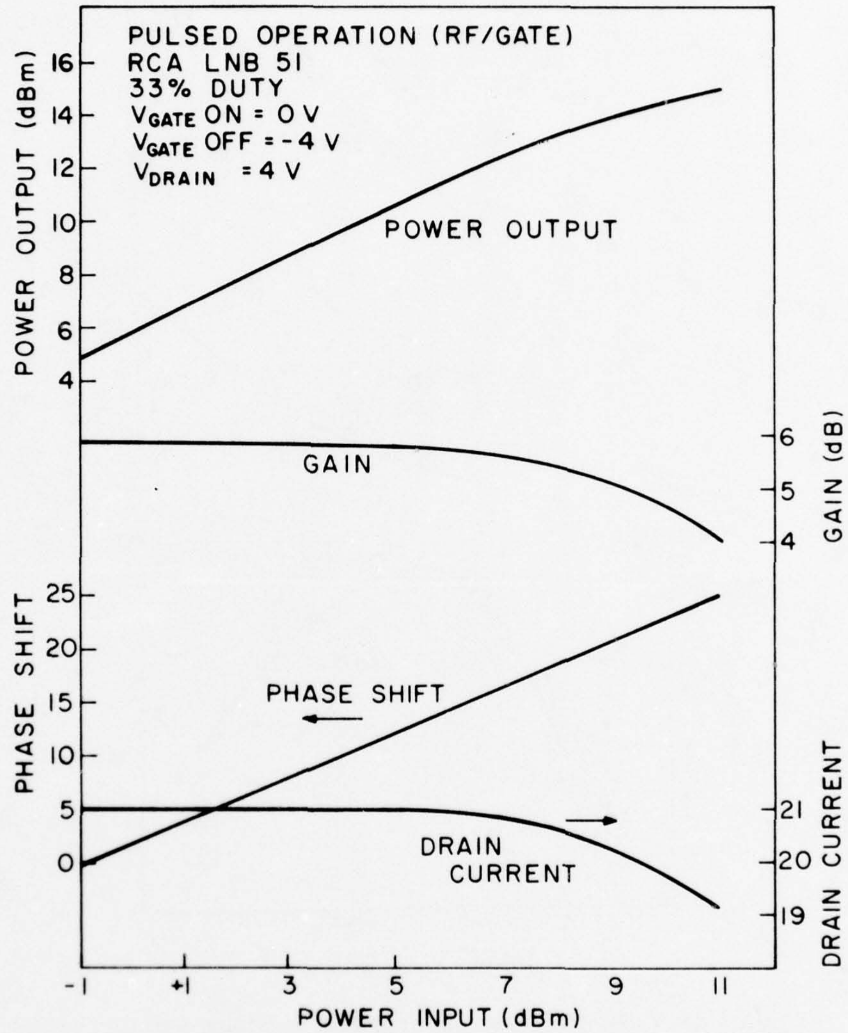


Figure 19. 2G FET amplifier sensitivities to input power variations.

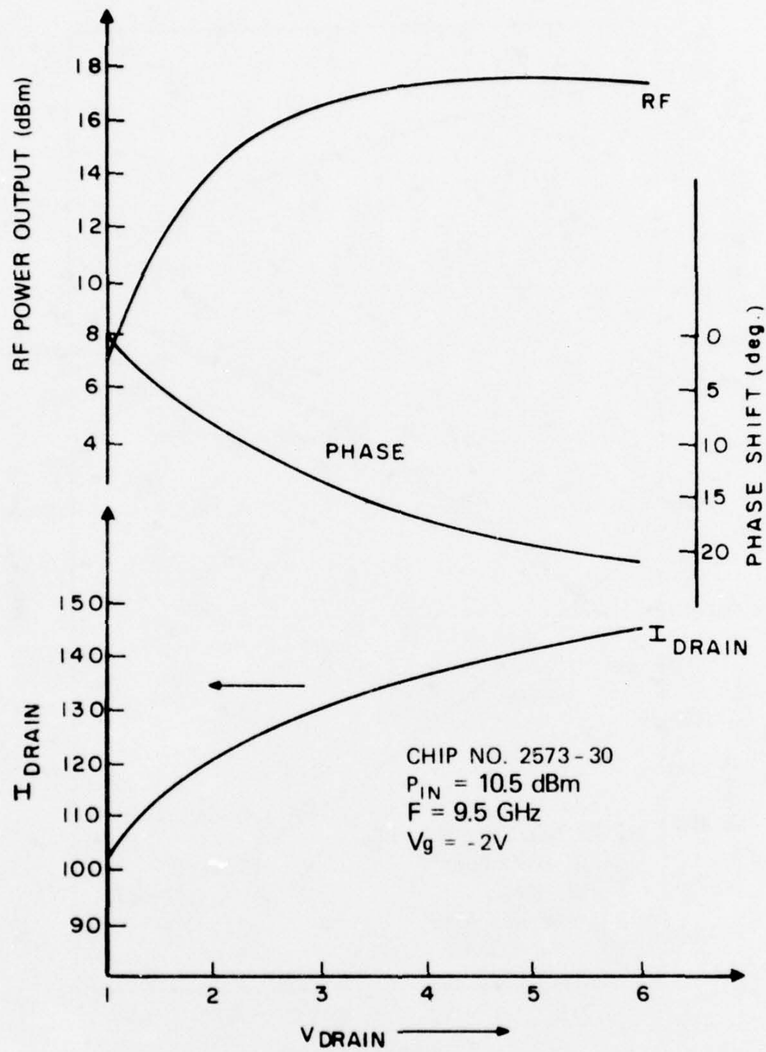


Figure 20. 4G single-cell FET amplifier drain voltage sensitivities.

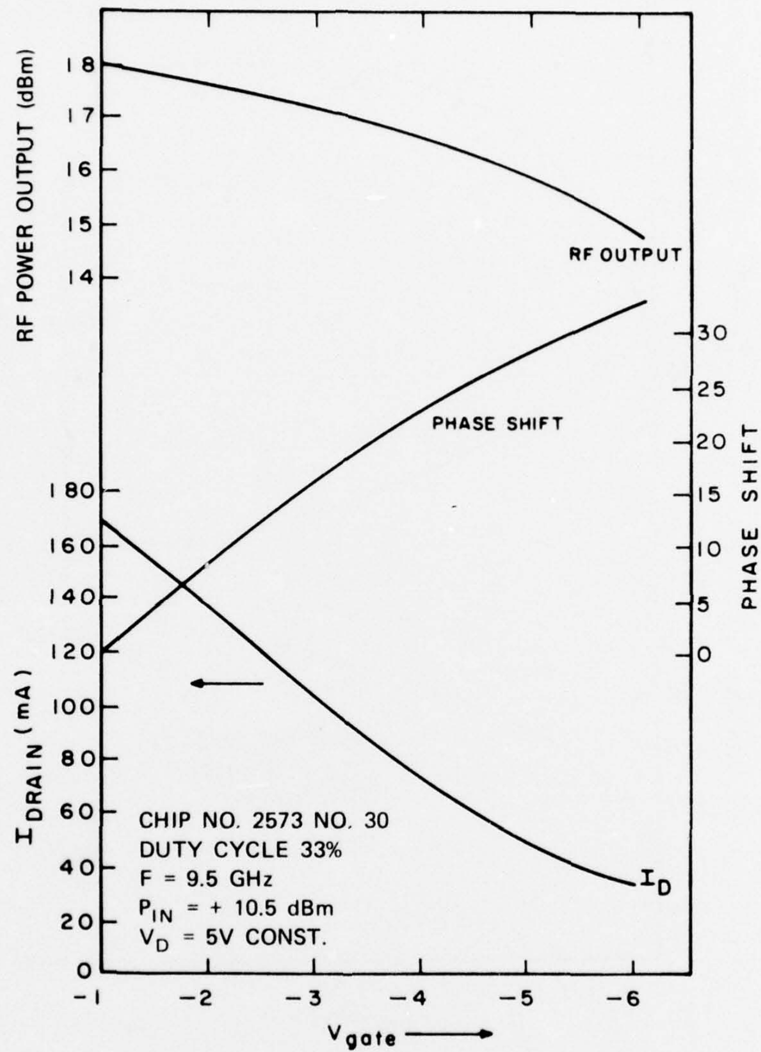


Figure 21. 4G single-cell FET amplifier gate voltage sensitivities.

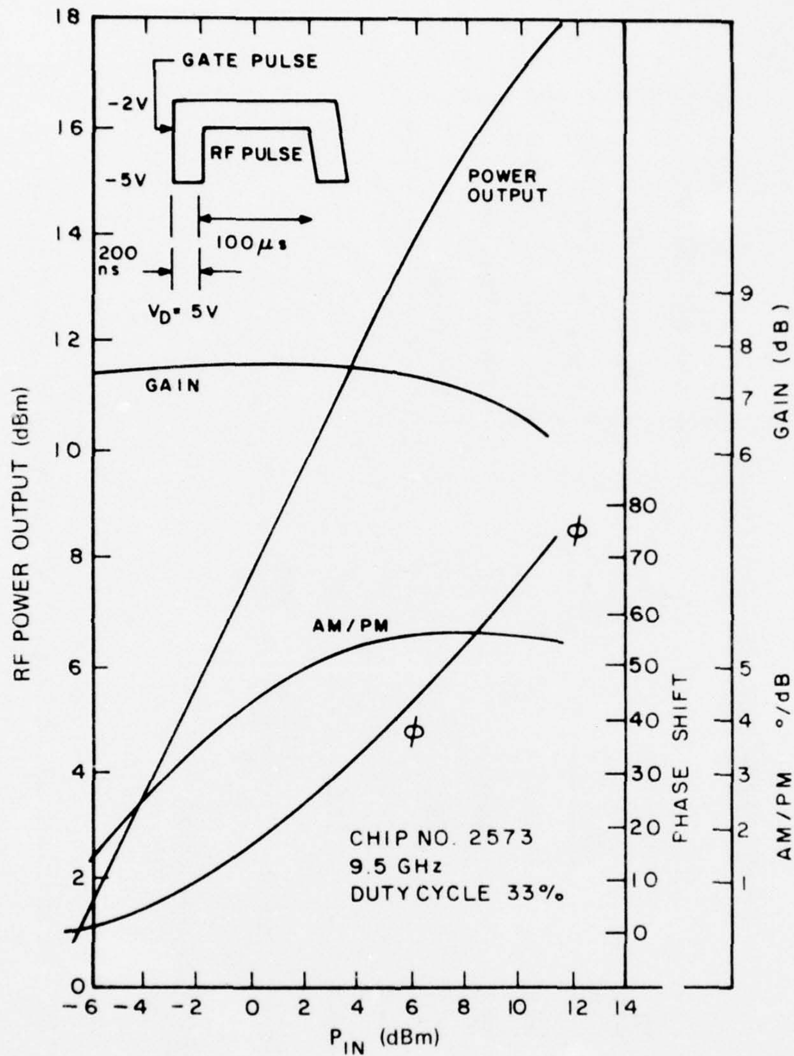


Figure 22. 4G single-cell FET amplifier sensitivities to input power variations.

PHASE-TEMPERATURE SENSITIVITY

Temp. (°C)	I_D Avg. (mA)	RF Power Output (dBm)	Relative Phase Shift*
15	36.6	18.2	0°
30	36.3	18.2	
40	35.7	18.0	1°
55	34.9	17.7	2°
70	34.4	17.5	3°

Temperature Sensitivity: $\frac{\Delta\ 3^\circ \text{ Phase}}{\Delta\ 45^\circ \text{ C}} = \frac{.066^\circ}{^\circ\text{C}}$

*Measured at end of intrapulse period.

Chip No. 2573-42
V_{drain} = 5 V
V_{gate} = −5 to −2 V
RF Input = 12.5 dBm
100 μs Pulse
33% Duty

Figure 23. 4G single-cell FET amplifier temperature sensitivities.

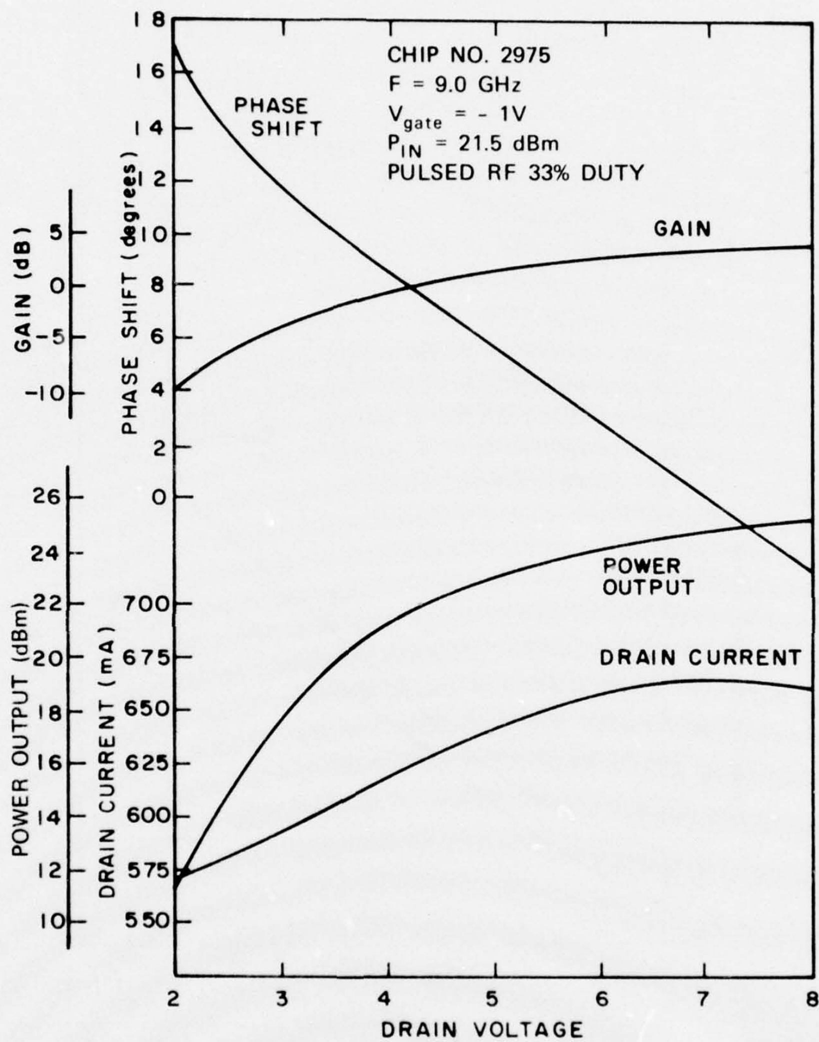


Figure 24. 16G FET amplifier drain voltage sensitivities.

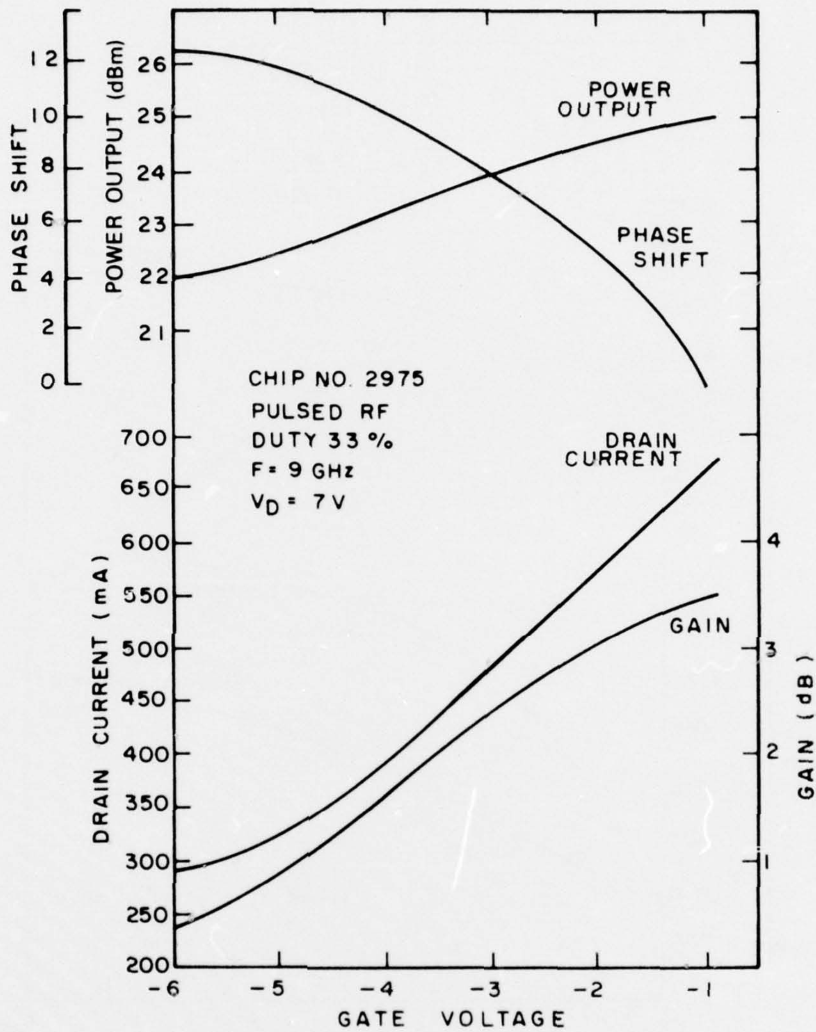


Figure 25. 16G FET amplifier gate voltage sensitivities.

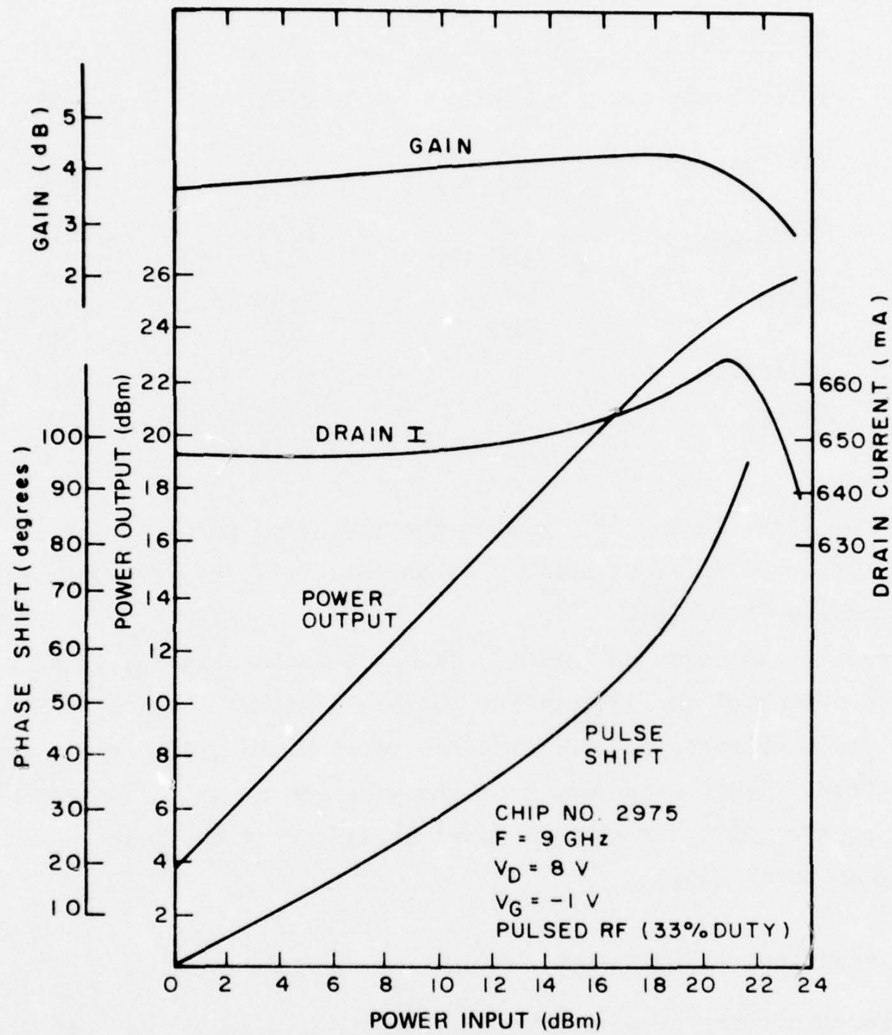


Figure 26. 16G FET amplifier sensitivities to input power variation.

TABLE 3. PHASE SENSITIVITIES OF PROTOTYPE FET AMPLIFIER STAGES (Figure Numbers Given in Parentheses)

Device Type	2G	4G	16G
Wafer Number	LNB51	2573	2975
$\Delta\phi/\Delta V_{drain}$	$\pm$ 1°/V (15,16)	-2°/V (20)	-3°/V (24)
$\Delta\phi/\Delta V_{gate}$	12°/V (17,18)	8°/V (21)	6°/V (25)
AM/PM	2°/dB (19)	5.5°/dB (22)	8°/dB (26)
$\Delta\phi/\Delta$VSWR		6°	
$\Delta\phi/\Delta T$		0.066°/°C (23)	

verified from Figs. 15 and 16. Around the operating point of 5 V on the drain, $\Delta\phi/\Delta V_{drain}$ is about -1°/V at small signals (Fig. 15), and is about +1°/V at 1 dB compression (Fig. 16).

By scanning the data in Table 3, it can be seen that the phase sensitivity to the gate potential is greatest for the small signal devices, while the sensitivity to drain voltages and the am/pm conversion are greatest for the larger signal devices. These data show that the greatest amount of voltage regulation is needed at the gate, and that rf level changes have the greatest influence on the higher power stages.

D. PHASE TRANSIENT MEASUREMENTS

The FET amplifier is most naturally pulsed between on and off states by superimposing a pulse upon the gate bias. Microwave power FETs normally operate at a gate bias between -1 and -2 V, and are normally pinched off at a gate bias around -5 or -6 V. To measure phase transients, a system of pulse generators is set up to generate the various waveshapes shown in Fig. 27. From the top, the first waveshape shown is a sync pulse used to synchronize all pulse generators, oscilloscopes, and peak power meters. The second waveshape is the rf pulse output of the PIN modulator shown in Fig. 12. The third waveshape is the pulse used to drive the gate of the FET amplifier under test. It is derived from a pulse generator which permits the two voltage levels of the

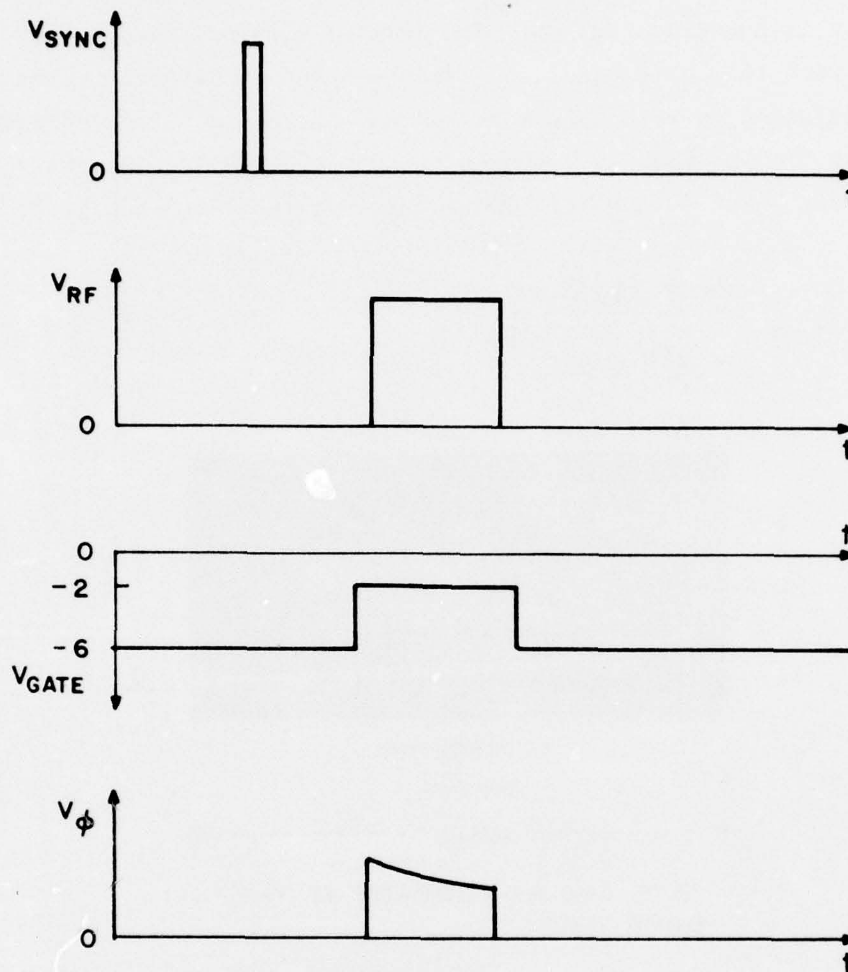


Figure 27. Pulses used in phase transient measurements.

pulse to be set at those values needed to turn the FET on and off. The timing and width of the gate pulse can be set completely independently of the rf pulse. Hence, the response of the amplifier to pulsing the gate before, after, or at the same time as the rf pulse can be readily determined. The bottom waveshape of Fig. 27 shows a typical output of the differential phase bridge. Because the FETs tested so far show a small transmission even when a cutoff voltage is applied to the gate, the timing and width of this pulse coincides with the rf pulse. This waveshape can be inverted depending upon which null of the differential phase bridge is used for measurements.

The intrapulse phase decay for a 100-μs rf and gate pulse applied to a 4G amplifier is shown in Fig. 28. The initial turn-on transient is too short to be seen with this time base, and will be discussed shortly. The phase bridge is adjusted to zero output at the end of the rf pulse, corresponding to the right side of Fig. 28. It can be seen that neglecting the turn-on transient, the phase during the 100-μs pulse varies less than 1.5°.

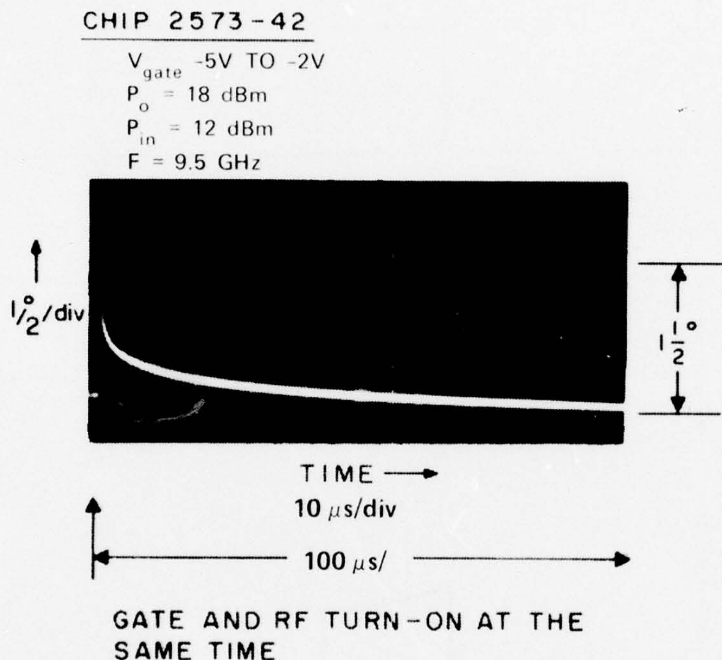
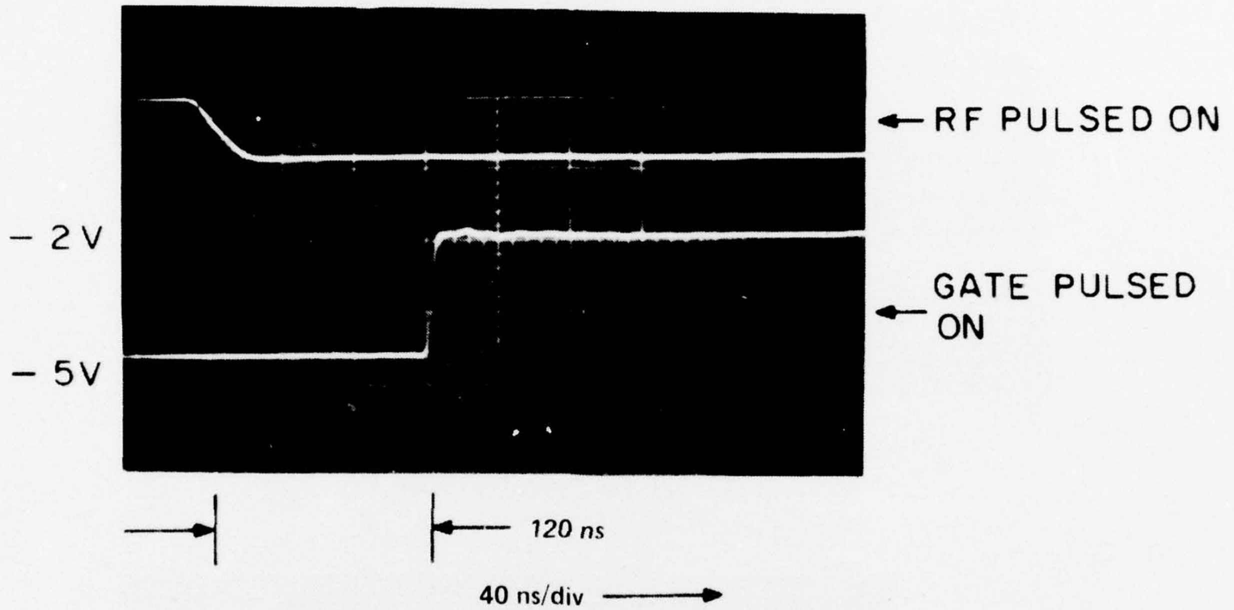


Figure 28. Intrapulse phase decay.

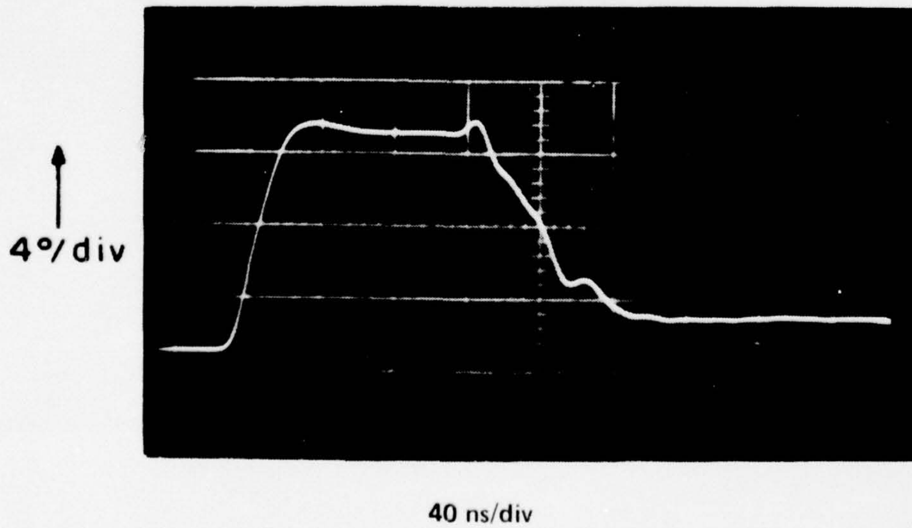
The turn-on transient is highly dependent upon the timing of the gate pulse relative to the rf pulse. When the rf is pulsed on well in advance of the gate pulse, a 13° turn-on transient is seen as shown in Fig. 29. However, the rf pulse seems to act as a window showing the FET response to the gate pulse. Delaying the rf pulse in progressive steps from the condition shown in Fig. 29, shows less of the gate turn-on phenomenon. Thus, when the rf and gate are pulsed *simultaneously*, the full 13° transient still is seen as shown in Fig. 30. When the rf is turned on 40 ns after the gate pulse, only a 4°-transient representing the trailing end of the full transient occurs. This transient is shown in Fig. 31. When the rf pulse is delayed even further, less

P_O = 17 dBm
P_{IN} = 12 dBm
33% DUTY
PULSE WIDTH = 100 μs
V_{DRAIN} = 5V

FET CHIP NO. 2573-42

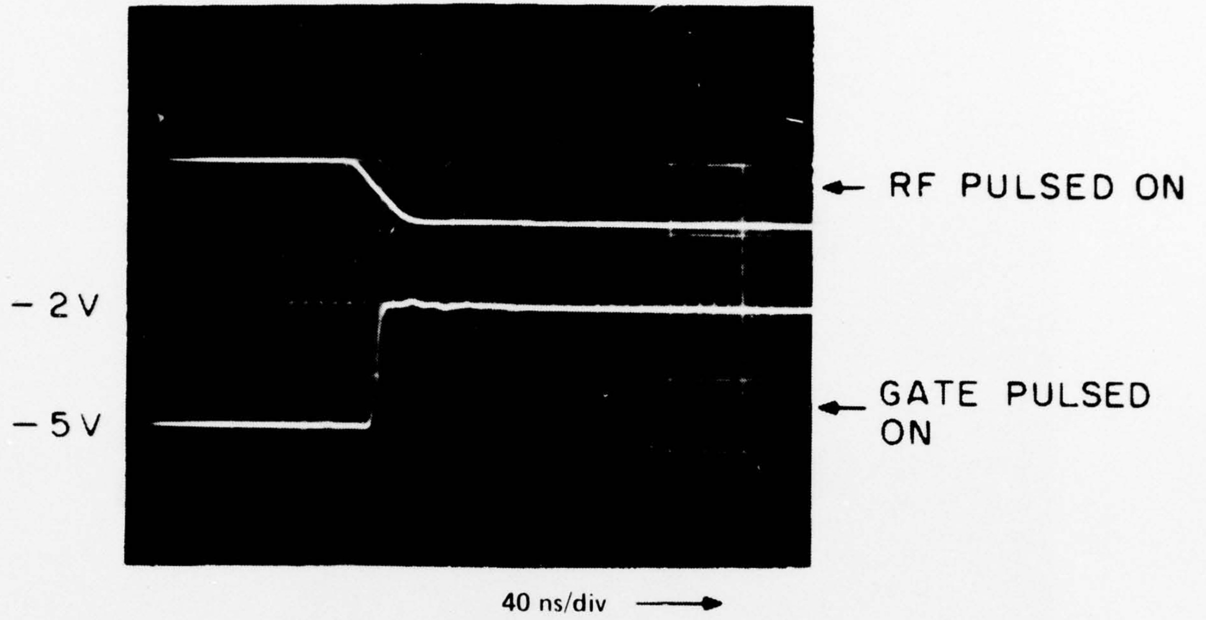


(a) RF and gate pulses

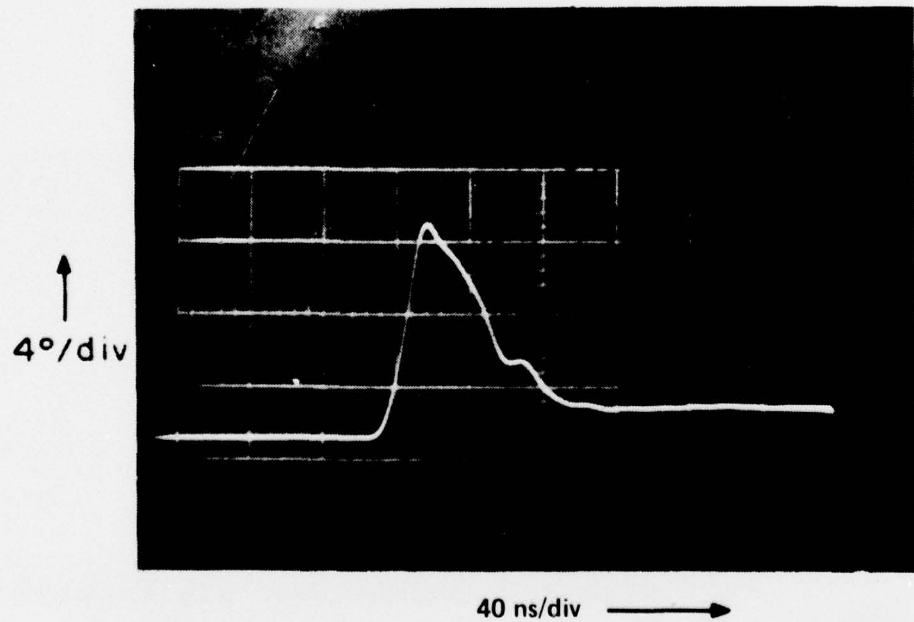


(b) Resulting unbalance phase transient

Figure 29. Phase transient for rf turn-on 120 ns before gate turn-on.

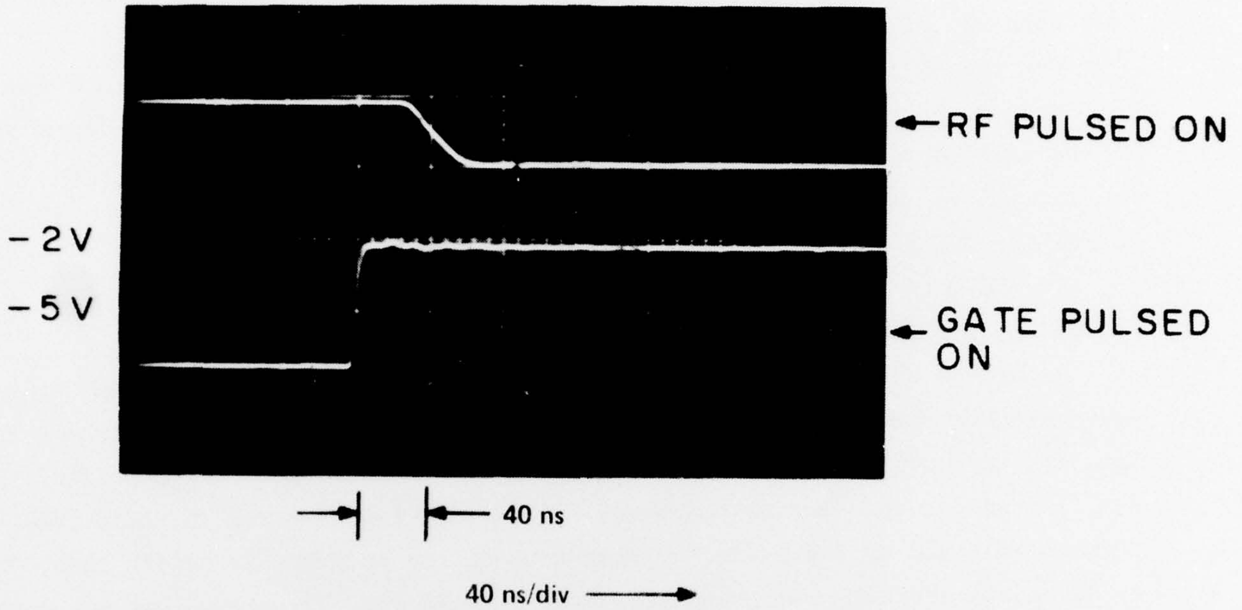


(a) RF and gate pulses

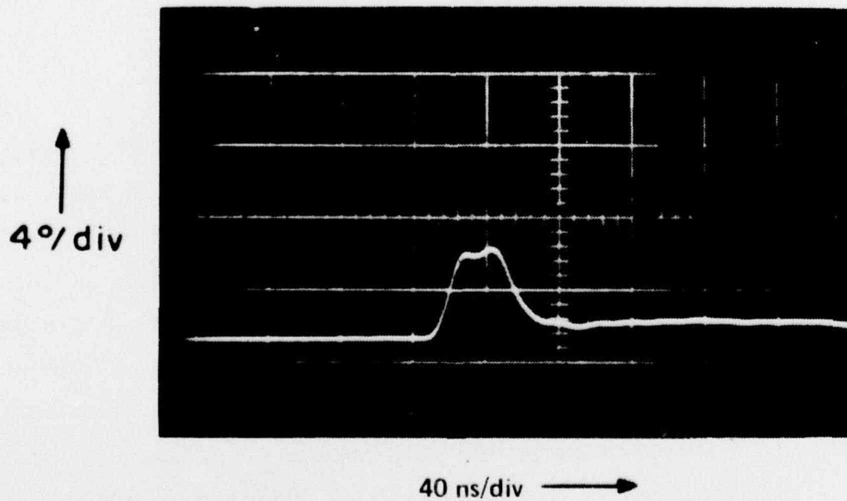


(b) Resulting unbalanced phase transient

Figure 30. Phase transient for simultaneous gate and rf turn-on.



(a) RF and gate pulses



(b) Resulting unbalanced phase transient

Figure 31. Phase transient for rf turn-on 40 ns after gate turn-on.

than a 4°-transient is seen, as shown in Fig. 32. It is suspected that this response is caused by slight inequalities in the length of the reference and test channels of the phase bridge.

For the 4G device tested, these measurements show that a maximum turn-on transient of 13° occurs when the rf and FET gate are pulsed on simultaneously. If the rf is delayed by 40 ns, the turn-on transient is reduced to 4°. After the initial transient, which lasts for about 80 ns after the gate pulse, the intrapulse phase decays by about 1.5° over a 100-μs pulse width.

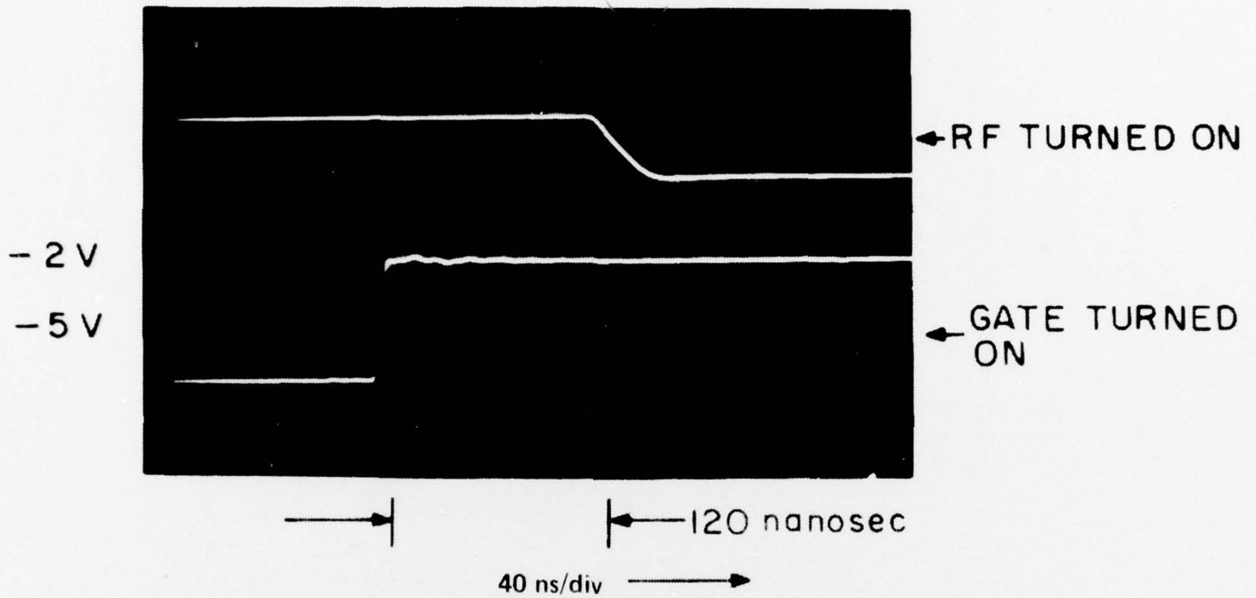
If the gate is not pulsed so that the FET is constantly biased on, no variation in phase response is seen as the rf is pulsed.

Amplitude and ph - transient response measurements on an amplifier stage using another sample of a 4G device show even better performance. As shown in Fig. 33, the amplitude reaches its final value within 40 ns. The amplifier may, in fact, have a better response, but further improvements in measurement techniques, such as improving the rise time of the rf pulse to better than 30 to 40 ns are needed. The phase response, also in Fig. 33, shows that after an initial overshoot of 7°, the phase shift 60 ns after pulse turn-on is 1.5°. When inspecting the two responses in Fig. 33, realize that they are not synchronized horizontally to each other.

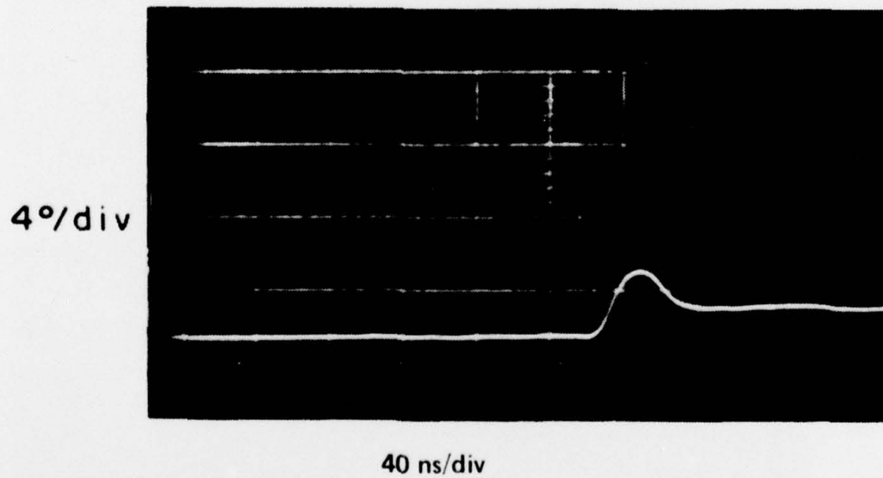
E. PULSE BIASING TECHNIQUES

The measurements described so far were on single amplifier stages utilizing a pulse generator having a dc offset capability. This permitted both levels of the gate pulse to be set to those values which turn the FET on and off.

A multistage FET amplifier should be operated from a single gate bias supply and a single pulse input. However, it is expected that the various stages may each require different individual potentials for the on and off conditions. For fixed duty factors, it is conceivable that dc levels can be set by a system of potentiometers, and that pulses could be coupled to the gates capacitively. However, as the duty factor of the pulses vary, the resulting levels at the gates would also vary. Rather than incorporate a complex scheme of diodes into a dc restoration network, a dc coupled network for injecting pulses onto a biased FET gate has been developed. This network, shown in Fig. 34, is not duty-factor sensitive. It can be seen that when there is no voltage on the base, the illustrated transistor is turned off, and the emitter

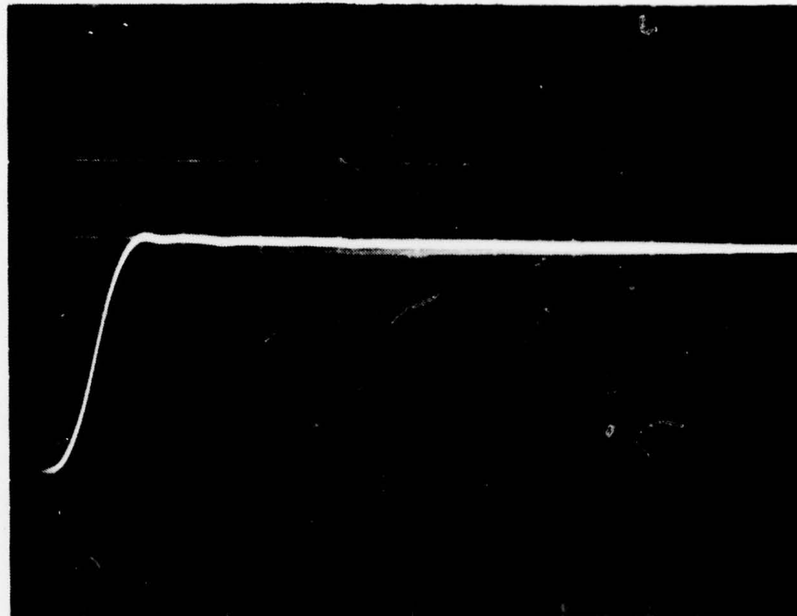


(a) RF and gate pulses



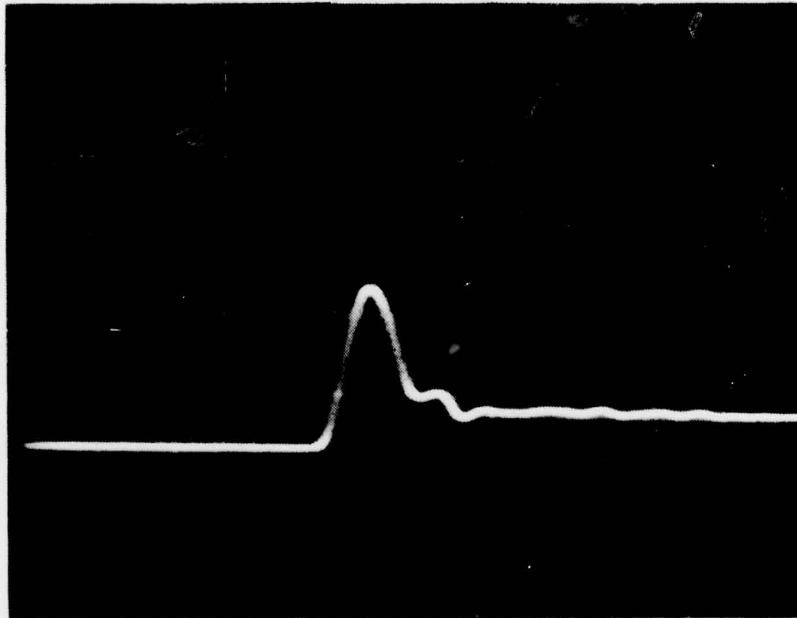
(b) Resulting unbalanced phase transient

Figure 32. Phase transient for rf turn-on 120 ns after gate turn-on.



40 ns/cm

(a) Amplitude response



40 ns/cm

(b) Phase response

Figure 33. Pulse responses of a 4G single-cell amplifier.

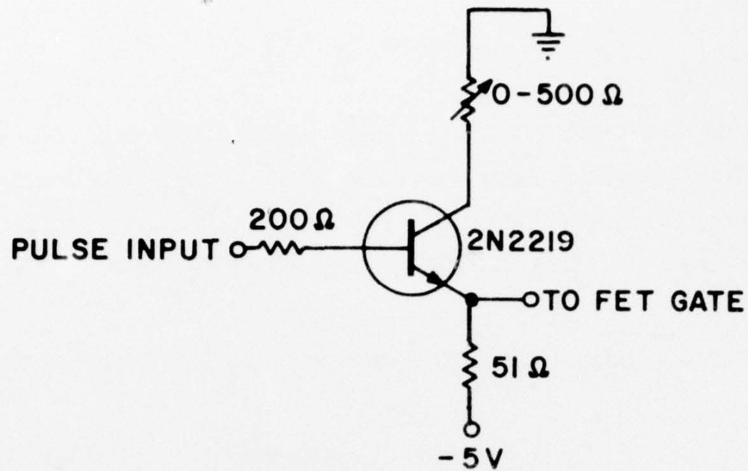


Figure 34. Gate-bias pulse modulator stage.

output is maintained at -5 V. When a voltage does appear at the base, the transistor conducts, causing the emitter voltage to assume a value dependent upon the collector resistance. The selected transistor has a high-frequency response to minimize pulse distortion.

A complete pulse distribution network would incorporate a transistor pulsing stage for each stage of the rf amplifier which is to be pulsed. For the amplifier module shown in Section I, the last two or possibly three stages would be pulsed to yield high overall efficiency.

In principle, the FETs can also be pulsed at the drain supply. Because a substantial current is supplied at the drain, an elaborate modulator network would be needed to switch the FETs on and off at the required fast speeds. Because the gates of the FETs draw no current, it is, by comparison, a simple matter to apply pulse modulation to these terminals.

SECTION V

DEVICE DELIVERIES

During the first six months of this program two deliveries of ten devices each were made. Complete data sheets showing the rf performance of these devices as a function drive level has been delivered with the devices. A summary of the device characteristics is tabulated in Table 4.

TABLE 4. CHARACTERISTICS OF DELIVERED FET DEVICES AT 8GHz

Device No.	Power Out (mW)	Gain (dB)	η_{PA} (%)	Gain (Small Signal) (dB)
4G Two-cell types				
B327B-112	209.4	4.5	6.7	6.0
-113	243.9	5.2	8.2	6.3
-147	211.8	4.6	5.2	5.7
-294	327	5.0	16.8	5.9
-322	256	3.9	15.7	5.95
16G types				
B390-11	417	5.0	7.2	5.4
-29	315	4.3	15.2	4.7
-30	220	3.3	3.7	3.3
-32	298	4.0	9.3	4.1
2975-72	393	4.7	9.75	5.4
B620-5	761.6	3.14	10.6	5.07
-9	654.5	2.48	6.43	4.62
-11	737.8	3.00	12.1	4.96
-17	714.0	2.85	11.88	3.68
-18	821.1	3.46	15.16	5.18
-26	642.6	2.40	6.48	4.66
-32	773.5	3.20	11.36	4.97
-33	654.5	2.48	9.05	3.97
-34	749.7	3.07	12.10	4.96
-40	690.2	2.71	7.38	4.85

The last ten rows of this table show the devices that were delivered in the second shipment. It can be seen that, on the average, the output power of these 16G devices is more than double the output power of the five 16G devices delivered in the first shipment, which was two months earlier. This is indicative of the progress being made in device development.

SECTION VI

PLANS FOR THE NEXT SIX MONTHS

Development of 16, 32, and 48G devices will continue in the next six months. During this time frame, a multistage amplifier consisting of the first four stages shown in Fig. 1 will be fabricated. This will consist of a cascade of four balanced amplifier stages with output power approaching the 2-W level. This amplifier module will be used for extensive phase characterization testing.

SECTION VII

SUMMARY

The first six months of this program show advances being made in the areas of device development, fabrication of single amplifier stages, and characterization of pulsed phase responses of FET amplifiers.

New device types, namely the 16, 32 and 48G FETs have been developed to the point of achieving greater than 1-W output. In particular, the 16G FET has achieved 1.03 W at 8 GHz, the 32G achieved 1.82 W at 8 GHz, and the 48G achieved 3.2 W at 4 GHz. Material parameters and processing techniques are being improved to give even better performance.

Amplifier stages have been developed, which when used as balanced pairs, are capable of over 500 mW over the 9- to 10-GHz band. Efforts will concentrate on reducing the need for tuning chips, improving the packaging efficiency of a complete amplifier module, fabricating higher power stages, and assembling a multistage amplifier.

Pulsed phase measurement techniques have been developed which are accurate, have high resolution, and are easily performed. Phase sensitivity measurements and phase transient measurements done on early prototypes of the low-level stages show no major limitations which would prohibit the use of FET amplifiers in phase array applications. Phase measurements on a cascade of amplifiers will be done in the next six-months' period.

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