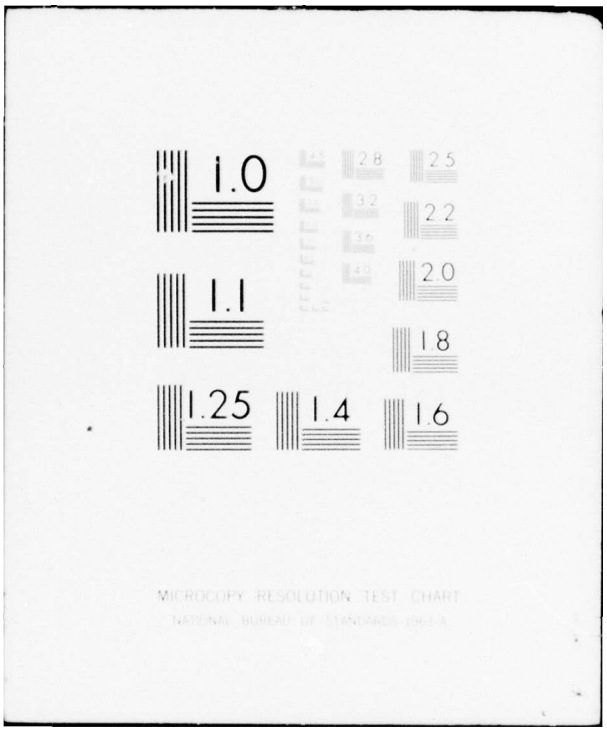
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RADC-TR-77-263, Volume II (of three)
Final Technical Report
August 1977

UNATTENDED/MINIMALLY ATTENDED RADAR STUDY
2-D (Unattended) Radar

General Electric Company

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The purpose of the Unattended/Minimally Attended Radar Study was to determine the exploratory and advanced development activities necessary to support the development of Unattended (2-D) and Minimally Attended (3-D) Radars. Volume II describes the several radar concepts that were considered for the 2-D unattended role, and the selection of the recommended design.

The 2-D Radar provides detection of low-flying aircraft to 60 nmi. The principle design ground rules include extremely high reliability and ease of maintenance, low life cycle cost, and very low prime power. → (cont)

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The study concludes the technology is available in 1977 to permit the design and implementation of radars which can operate unattended for periods of up to three months (with 90% confidence of full performance). The recommended design is an L-band cylindrical array, using either an analog or a digital signal processor and a distributed data processor. Prime power usage is from 400 W to slightly more than 1 kW, depending on the implementation scheme selected.

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PREFACE

This report, prepared by the General Electric Company for Rome Air Development Center under Contract No. F30602-76-C-0380 was compiled by T. B. Shields, the Study Director. Major contributors were S. E. Bell, M. I. Fox, L. D. Hayes, R. V. Jackson, R. D. King, J. W. Krueger, D. J. Murrow, J. A. Rougas, N. A. Schmitz, F. D. Shapiro, J. J. Stewart, and R. D. Wengenroth. B. Cameron was the General Electric Company Program Manager. R. A. Ackley and A. S. Briggs were the RADC Program Monitors.

TABLE OF CONTENTS

Section	Title	Page
I	INTRODUCTION	1-1
II	DESIGN GOALS/REQUIREMENTS	2-1
	1. Prime Power	2-1
	2. Coverage	2-3
	3. Accuracy	2-5
	4. Resolution	2-5
	5. Automatic Detection and Tracking	2-5
III	SYSTEM DESIGN	3-1
	1. Requirements Allocation	3-1
	2. System Synthesis	3-36
	3. Sensor Subsystem	3-58
	4. RF Design	3-71
	5. IF Design	3-86
IV	SIGNAL PROCESSOR	4-1
	1. Introduction	4-1
	2. Signal Processor Requirements	4-7
	3. Digital Signal Processor	4-10
	4. Charge Coupled Device Signal Processor	4-26
	5. Rejected Designs	4-42
V	DATA PROCESSING SUBSYSTEM REQUIREMENTS	5-1
	1. Summary Description	5-1
	2. Radar Data Input Processor	5-3
	3. Radar Target Processor	5-13
	4. IFF Data Controller and Data Processor	5-23
	5. Radar Control Processor/Synchronizer	5-31
	6. Remote Site Control Processor	5-42
	7. Performance Monitor/Fault Detection and Location	5-42
	8. Data Processor Architecture	5-46
	9. Data Communication Link	5-64
	10. Radar Synchronizer	5-65
	11. IFF Data Controller Implementation	5-71

TABLE OF CONTENTS (Cont)

Section	Title	Page
VI	RELIABILITY AND MAINTAINABILITY	6-1
	1. Objectives	6-1
	2. Reliability Analysis	6-4
	3. Maintainability Analysis	6-20
VII	BUDGETARY 2-D RADAR PROCUREMENT SCHEDULE AND COSTS	7-1
	1. Development and Acquisition	7-1
	2. Operations and Maintenance Costs	7-3

LIST OF ILLUSTRATIONS

Figure	Title	Page
2-1	Range/Elevation Coverage Requirements for 5000-ft Site Elevation	2-4
3-1	Frame Time and Coverage Tradeoff Relationship	3-2
3-2	Sequential Lobing Beam Crossover Accuracy	3-4
3-3	Accuracy Degradation vs Target Angle	3-5
3-4	M-Out-of-N Detection Performance	3-7
3-5	Effect on Diversity on Detection Requirements ($P_{FA} = 10^{-6}$)	3-7
3-6	Variation of the Probability of a False Track Initiate with Single Cell/Scan P_{FA} on a No Scan-to-Scan Motion Target	3-8
3-7	Effect of Diversity on Detection Requirements ($P_{FA} = 10^{-4}$)	3-10
3-8	Required SNR for Desired False Track Initiation Rates	3-10
3-9	Position Accuracy vs Time During Track Initiation, N = 4	3-11
3-10	Velocity Accuracy vs Time During Track Initiation	3-11
3-11	Target Track Example	3-13
3-12	Radar Horizon vs Site Elevation	3-15
3-13	Multipath F-Factor for a 500-Ft Target Height and a 1000-Ft Radar	3-16
3-14	Comparative L-Band/UHF Multipath Performance	3-18
3-15	Three-Out-of-Four Cumulative Detection for a 150-Ft Radar and a 500-Ft Target Height	3-19
3-16	Three-Out-of-Four Cumulative Detection for a 4500-Ft Radar and a 500-Ft Target Height	3-19
3-17	One-Out-of-Four Cumulative Detection for a 150-Ft Radar and 500-Ft Target Height	3-20
3-18	One-Out-of-Four Cumulative Detection for a 4500-Ft Radar and 500-Ft Target Height	3-20
3-19	Coverage Pattern in the Presence of Severe Multipath	3-21
3-20	Clutter and Signal RCS After Pulse Compression	3-23
3-21	Clutter Attenuation Factors	3-26
3-22	Ideal $\csc^2$ Radar Elevation Pattern	3-28
3-23	Weather Clutter Beam Filled Area*(Zero Radar Height)	3-30
3-24	Mean Clutter Velocity (Zero Radar Height)	3-31
3-25	Clutter Velocity Spread (Zero Radar Height)	3-32

LIST OF ILLUSTRATIONS (Cont)

Figure	Title	Page
3-26	Weather Clutter Beam Filled Area* (4500 Ft Radar Height)	3-33
3-27	Mean Clutter Velocity (4500 Ft Radar Height)	3-34
3-28	Clutter Velocity Spread (4500 Ft Radar Height)	3-35
3-29	Matrix-Switched Transmitter/Receiver Candidate Concept	3-37
3-30	RF Power Variation With Frequency	3-40
3-31	UHF RF Power Variation With Beamwidth	3-41
3-32	L-Band RF Power Variation With Beamwidth	3-42
3-33	Candidate Waveform	3-44
3-34	8-Pulse Doppler Processor Response	3-46
3-35	Weighting Effect on Doppler Filter Response	3-48
3-36	Doppler Filter Response in Null Region (of Second Null)	3-49
3-36A	Single-Scan Probability of Detection as Function of Target Velocity, Aligned Doppler Channels, Both Ground and Weather Clutter Present	3-54
3-37	Single Scan Probability of Detection as Function of Target Velocity, Unaligned Doppler Channels, Both Ground and Weather Clutter Present	3-54A
3-37A	Single-Scan Detection Probability	3-56
3-38	Binary Detection Over Four Scans	3-58
3-39	Type A Candidate Approaches	3-60
3-40	Baseline Unattended Radar Design	3-62
3-41	Unattended Radar Replacement	3-63
3-42	Alternate Unattended Radar Design	3-65
3-42A	Horn Antenna Inertialess Unattended Radar Design	3-65A
3-43	Simplified Block Diagram for Ring Array	3-66
3-44	Cylindrical Arrays	3-66
3-45	Frequency-Scanned Planar Array	3-67
3-46	Organ-Pipe Scanned Cylindrical Array	3-67
3-47	Cylindrical Array Patterns	3-68
3-48	Sample Beamshapes for a Type A Growth Option	3-70

LIST OF ILLUSTRATIONS (Cont)

Figure	Title	Page
3-49	Delay-Bit Steered Cylindrical 1-64-256 Array, RF Block Diagram, Unattended Radar	3-72
3-50	Matrix Switched Cylindrical 1-64-256 Array	3-74
3-51	Organ-Pipe Scanner Cylindrical Array, RF Block Diagram, Unattended Radar	3-75
3-52	Tapered Drive Matrix-Switched Cylindrical 1-64-256 Array, RF Block Diagram, Unattended Radar	3-76
3-53	Frequency Scanner Planar Array, RF Block Diagram, Unattended Radar	3-77
3-54	Parabolic Torus Mechanically-Scanned Antenna, RF Block Diagram, Unattended Radar	3-79
3-55	Solid-State 4.5 W Amplifier Chain	3-82
3-56	8-W L-Band Amplifier Made for NADC	3-82
3-57	Voltage Controlled Power Amplifier Performance	3-83
3-58	Controlled Modulator	3-84
3-59	Typical Driver Circuit	3-87
3-60	Exciter Waveform Generator	3-89
3-61	Measured Short-Term Frequency Stability of 80-MHz STALO	3-90
3-62	Frequency Divider/IFF Transmit Pulse Generator (Part of Exciter/Waveform Generator)	3-93
3-63	Unattended/Minimally Attended Radar Waveform Generator	3-94
3-64	Unattended Radar Receiver	3-96
3-65	Unattended/Minimally Attended Radar Receiver Synchronous Detector	3-97
4-1	Processor Block Diagram	4-2
4-2	Signal Processor Block Diagram	4-11
4-3	Signal Processor Time Line	4-14
4-4	A/D Converter and Dc Correction Loop Block Diagram	4-17
4-5	Dc Correction Loop (1 of 2)	4-18
4-6	Pulse Compressor BT = 32, 2 Channels	4-19
4-7	Serial Arithmetic Equalizer	4-20
4-8	Doppler Processor Block Diagram	4-22

LIST OF ILLUSTRATIONS (Cont)

Figure	Title	Page
4-9	Decimation-in-Frequency FFT 8 Using FFT 2's	4-23
4-10	Magnitude Calculator	4-24
4-11	Normalizer	4-25
4-12	CCD Signal Processor	4-27
4-13	Serial CCD Pulse Compression Filter (One Board)	4-28
4-14	CCD Matched Filter Response and Impulse Response At 500 kHz Clock Rate After S/H	4-29
4-15	Experimental Transfer Function of CCD Sine Chirp Matched Filter	4-30
4-16	CCD Sine Chirp-Matched Filter Output Waveform	4-32
4-17	CCD Doppler Processor	4-33
4-18	Magnitude Estimation Circuit, CCD Normalizer and Digital Data Interface	4-36
4-19	Magnitude Detection Circuit	4-37
4-20	Redundant CCD Signal Processor	4-41
4-21	16-Bit Signal Processing Element (2 MHz, 400-ns Cycle Time)	4-43
4-22	Serial Complex Multiplier	4-44
4-23	One-of-Eight Serial Arithmetic DFT Doppler Processors	4-45
4-24	A Squaring Magnitude Calculator	4-45
5-1	Unattended Radar Configuration	5-2
5-2	Data Processor and Control	5-4
5-3	Nominal Transmit Waveform	5-6
5-4	Radar Data Input Processor Aligned System	5-7
5-5	Radar Data Input Processor Buffer Management Aligned System	5-10
5-6	Radar Data Input Processor Unaligned System	5-12
5-7	Radar Data Input Processor Buffer Management	5-15
5-8	Radar Target Processor	5-16
5-9	IFF Transponder Return	5-25
5-10	IFF Functional Block Diagram of IFF Processing	5-26
5-11	IFF Data Controller	5-28
5-12	IFF Data Processor	5-30

LIST OF ILLUSTRATIONS (Cont)

Figure	Title	Page
5-13	Matrix-Switched Cylindrical Array	5-35
5-14	Delay-Bit Steered Cylindrical Array	5-38
5-15	Delay Bit Steered Drive Table Definition	5-39
5-16	Processor Network	5-46
5-17	Overall Data Processor Configuration	5-48
5-18	CMOS PE Architecture	5-50
5-19	LS-TTL PE Architecture	5-53
5-20	FIFO Block Diagram	5-56
5-21	Program Memory Block Diagram	5-60
5-22	Clutter Map Memory	5-62
5-23	Data Communication Link Block	5-64
5-24	Synchronizer	5-66
5-25	Synchronizer Output Logic	5-70
5-26	IFF Data Controller	5-72
6-1	Overall 2-D Radar Reliability Block Diagram	6-5
6-2	Probability of Successful System Operation	6-6
6-3	Unattended Radar Reliability Block Diagram	6-9
6-4	CCD Signal Processor Reliability Block Diagram	6-11
7-1	2-D — Development and Acquisition Schedule	7-2
7-2	Probability of Operation for Four Reliability Options	7-8
7-3	Power Cost as a Function of Rate	7-17

LIST OF TABLES

Table	Title	Page
2-1	General Design Goals	2-2
2-2	Clutter and Environment Data (Guide)	2-6
3-1	Automatic Target Detection and Track Parameters	3-9
3-2	Dew Line Site Altitudes	3-14
3-3	Pulse-Radar Range-Calculation Work Sheet	3-39
3-4	Prime Power Requirements Summary	3-42
3-5	Typical Frequency and Pulse Period for 4-Diversity Channel, Aligned Doppler System	3-45
3-6	SNR Per Dwell at Maximum Range	3-50
3-7	Signal-to-84th-Percentile-Ground-Clutter Per Dwell at Maximum Range	3-52
3-8	Signal-to-Weather-Clutter in Doppler Sidelobes at Maximum Range	3-53
3-9	Dc Power Requirements L-Band	3-80
3-10	RF Technology Development Status	3-80
4-1	Signal Processor Detection Losses	4-10
4-2	Signal Processor Power and Logic Estimates	4-15
4-3	CCD Signal Processor Implementation/Power Consumption Summary	4-40
5-1	Radar Data Input Processor Loading and Storage	5-9
5-2	Radar Data Input Processor Loading Unaligned System	5-14
5-3	Track Prediction and Smoothing Algorithm	5-18
5-4	Track Filter Initialization	5-20
5-5	Track Data Base	5-21
5-6	Process Load and Storage Requirements for Radar Target Processor	5-22
5-7	Integrated IFF Mark X System Performance	5-24
5-8	Process Load and Storage Requirements for IFF Data Processor	5-32
5-9	Radar Control Processor/Synchronizer Functions Normal Radar Scan	5-34
5-10	Process Load and Storage Requirement for Matrix Steered Cylindrical Array	5-37

LIST OF TABLES (Cont)

Table	Title	Page
5-11	Processor Load and Storage Requirements for Delay-Bit Steered Cylindrical Array	5-40
5-12	Synchronizer Drive Commands	5-41
5-13	Data Link Controlled Requirements	5-43
5-14	Hardware PM and FD/L Design Requirements	5-43
5-15	PM and FD/L Approach Software/Firmware Design	5-45
5-16	Power and Device Summary	5-47
5-17	Parts List for CMOS PE	5-52
5-18	Parts List for LS-TTL PE	5-54
5-19	Parts for FIFO Buffer	5-58
5-20	Parts List for Program Summary	5-61
5-21	Parts List for Clutter Map	5-63
5-22	Parts List for Data Communications	5-65
5-23	Parts List for Radar Synchronizer	5-70
5-24	IFF Data Controller Component Summary	5-73
6-1	Analyzed System Configurations for 2-D Radar	6-2
6-2	R/M Summary Requirements	6-3
6-3	Subsystem Reliability for Aligned Models vs PM Frequency	6-8
6-4	Representative Component Environmental/Quality Factors	6-19
6-5	AN/TPS-59 Reliability Failure Rate Data	6-19
6-6	Replaceable Units	6-23
7-1	System Component Parameters (2-D)	7-4
7-2	Test Equipment Costs	7-7
7-3	Cost Variables and Parameters	7-11
7-4	Component Parameters	7-12
7-5	Cost Variables and Parameters - Overall Costs	7-12
7-6	Overall Operations and Maintenance Costs	7-15
7-7	Operations and Maintenance Costs	7-16
7-8	Total Per Year Per System Manhours	7-22

GLOSSARY

A	Ampere
A/D	Analog-to-Digital
ALU	Arithmetic Logic Unit
AMPL	Amplifier
Az	Azimuth
BLR	Base Labor Rate
BT	Bandwidth Time
CCD	Charge Coupled Device
CE	Combination - Exponentation
CFAR	Constant False Alarm Rate
CkW	Cost per kilowatt
CMCR	Material Cost of Repair
CMOS	Complementary Metal Oxide Semiconductor
CNR	Clutter-to-Noise Ratio
COHO	Coherence Oscillator
COMB	Combiner
CPP	Cost of Prime Power
CPU	Central Processor Unit
CPT	Cost per Trip
csc^2	Cosecant Squared
CSR	Clutter-to-Signal Ratio
CT	Cost of Transportation
CW	Continuous Wave
D/A	Digital-to-Analog
dBm	Decibel referenced to a milliwatt
dc	Direct Current
DEW	Distant Early Warning
DFT	Discrete Fourier Transform
DIP	Dual In-Line Package
DIV	Division
DLR	Depot Labor Rate
DMI	Data Memory Interface
DP	Digital Processor

ECM	Electronic Countermeasures
FAA	Federal Aviation Administration
FET	Field-Effect Transistor
FFT	Fast Fourier Transform
FIFO	First-In First-Out
FIR	Finite Impulse Response
GF	Ground Fixed
h	hour
H	Horizontal
IC	Integrated Circuit
IF	Intermediate Frequency
I/O	Input/Output
ISLS	Interrogation Sidelobe Suppression
IV	Inverter
kWh	kilowatt hour
LARAM	Line-Addressed Random Access Memory
LC	Inductance Capacitance
LCC	Life Cycle Cost
LFM	Linear Frequency Modulated
LO	Local Oscillator
LS	Schottky Logic
LSI	Large Scale Integration
LSTTL	Schottky Logic Transistor-to-Transistor Logic
m	meter
M	Magnitude
mA	milliampere
MC	Memory Controller
mh	manhour
mm	millimeter
MOS	Metal Oxide Semiconductor
mrad	milliradian

MSI	Medium Scale Integration
MTBF	Mean Time Between Failures
M (ct)	Maintenance Corrective Time
MTI	Moving Target Indicator
MTTR	Mean Time to Repair
MUX	Multiplier
mW	milliwatt
μ	microsecond
NADC	Naval Air Development Center
NDEPOT	No. of Depots
NF	Noise Figure
nmi	nautical miles
NT	No. of Trips
O&M	Operational and Maintenance
OV	Outside Vendor
PC	Pulse Compression
PCB	Printed Circuit Board
PE	Program Element
PM	Preventive Maintenance
PM	Performance Monitor
PM/FD&L	Performance Monitor/Fault Detection and Location
PM/FL	Performance Monitor/Fault Location
p-p	peak-to-peak
PRF	Pulse Repetition Frequency
PRI	Pulse Repetition Interval
PROM	Programmable Read-Only Memory
PRP	Pulse Repetition Period
PS	Power Supply

RAM	Random Access Memory
RCS	Radar Cross Section
REG	Register
RF	Radio Frequency
R/M	Reliability/Maintainability
rms	Root-mean-square
ROM	Read Only Memory
R/W	Read/Write
s	second
SCR	Signal-to-Clutter Radio
S/H	Sample/Hold
SIF	Selective Identification Features
SIN	System Initialization
SIR	Signal-to-Interference Ratio
SLS	Sidelobe Suppression
SNR	Signal-to-Noise Ratio
SOS	Silicon-On-Sapphire
SOW	Statement of Work
SP	Signal Processor
SPDC	Signal Processor Data Conditioner
SSI	Small Scale Integration
STALO	Stabilized Local Oscillator
STC	Sensitivity Time Control
STR	Systems Technology Radar
TBD	To Be Determined
T^2L (TTL)	Transistor-to-Transistor Logic
T/R	Transmit/Receive
UART	Universal Asynchronous Receiver-Transmitter
UHF	Ultra High Frequency
V	Vertical
VSWR	Voltage Standing Wave Ratio
W	Watt
WFG	Waveform Generator
yr	Year

SECTION I

INTRODUCTION

This volume of the report describes the study effort that led to the selection of feasible designs for the 2-D Unattended Radars. The primary considerations were high-reliability, low-life cycle cost, very low prime power, and existing or near-term technology. The goal was to identify those advance development activities which are needed to support the development of a short range (60 nmi) 2-D radar which can operate unattended for periods of 3, 6, and 12 months with a 0.9 probability of successful operation at the end of that period.

Many different designs were considered, including rotating and fixed antenna systems, at frequencies from UHF to S-band. Signal processing concepts included both analog and digital implementations. Each of the various designs was subjected to reliability and prime power analyses to narrow the concepts considered in detail to a manageable number which had the best chance of meeting the study objectives.

The conclusion of the study is that the technology is available now to permit the development of unattended radars. The recommended system is an L-band cylindrical array, totally solid-state including the Transmitter, with an analog charge-coupled-device (CCD) signal processor and a distributed digital data processor. This report describes these subsystems in detail, along with alternate designs that permit trade-offs between performance, prime power, life-cycle cost, and technical risks.

SECTION II

DESIGN GOALS/REQUIREMENTS

The considerations which have been used in developing baseline requirements and design goals and allocating them to subsystems of the 2-D Unattended Radar are discussed herein. Major tradeoffs which have been performed in the course of this study are identified and discussed. Radar parameters having a secondary effect on the radar cost, reliability, and/or performance have been accepted directly from the Statement of Work (SOW) in order to concentrate attention on optimization of the higher payoff parameters. This approach places the emphasis where it should be for this study - on technology and reliability developments for the demonstration of the feasibility of unattended radar operation.

A summary of the radar design goals is presented in Table 2-1. They are interpreted and discussed further in the following paragraphs.

1. PRIME POWER

The 500-W prime power goal is based on the total long-term prime power capability of 2 kW (NASS Power System Requirement, NRS-RFP-76-35-CAO) for the unattended site. The preliminary budget is as follows:

Environmental	1.0 kW
Radar/Processor	0.5 kW
Security	0.4 kW
Communications	0.1 kW
	2.0 kW

This does not include the power generated in the form of heat from, for example, an isotope or fossil fuel approach. Therefore, in addition to the 1.0 kW available for environmental control, the thermal by-product may also be available for this use. Thus, it is possible that somewhat more than 500 W can be available for the radar.

A serious design effort toward the 500-W goal was carried out. The design was dominated by this goal in that it led to a different overall sensor form factor than would have otherwise resulted.

TABLE 2-1. GENERAL DESIGN GOALS

RF Bandwidth	10%
Site Altitude	50 to 4500 ft
Radar Prime Power	500 W
Frame Time	4 s
Growth	3-D
Target Characteristics	
RCS	1 to 16 m^2
Speed	80 to 2400 knots
Detection Range	30 nmi (1 m^2)/60 nmi (16 m^2)
No. of Tracks	20
Special Features	ECM Warning Zero Doppler Detection Anticlutter Processing CFAR
Coverage	
Max. Range	60 nmi
Min. Range	TBD
Max. Altitude	100 kft
Max. Elevation Angle	50°
Min. Elevation Angle	R_{min} at 0 kft
Azimuth Coverage	360°
Resolution/Accuracy	
Range	0.5 nmi/0.25 nmi
Azimuth	3°/0.5°
Height Accuracy	NA
Angle Sidelobes	
Transmit	≤ -20 dB (First) ≤ -30 dB (Others)
Receive	≤ -30 dB

TABLE 2-1. GENERAL DESIGN GOALS (CONT'D)

Detection	
P_D (3 out of 4 scans)	0.95
P_{FA}	10^{-6}
Tracking	
P (Track Initiate and Maintenance)	0.95
P (Drop Track Exiting Coverage)	0.999
False Track Initiation	one per hour
Track Initiate Time	16 s
Track Drop Time (Exiting Target)	12 s

2. COVERAGE

The radar must detect, locate, and report all valid targets in the coverage, and track up to 20 of these. Expected aircraft vary in size and spread from Piper Cubs (e.g., bush pilots) to fighter-type aircraft. For design purposes, the smaller aircraft are assumed to possess 1 m^2 radar cross-section (RCS) with a Swerling I type fluctuations, and are to be detected to 30 nmi. The larger aircraft with 16 m^2 RCS, also fluctuate as in the Swerling I model and are to be detected to 60 nmi. Target speeds range from 80 to 2400 knots. The time required for a scan of the normal surveillance sector is nominally 4 s and variations up to 8 s were considered in this study. Frame time has a major impact on the ultimate sensor size and was traded off with power aperture.

The maximum instrumented range of the unattended type A radar is 60 nmi. The minimum range of the radar was to be determined consistent with the shortest pulse duration and with tracking targets through the coverage volume.

The antenna gain and pattern will be such as to allow detections of aircraft with altitudes up to 100 kft. The nominal range vs elevation coverage contour provided by the antenna pattern will be at least 60 nmi from the horizon to an elevation angle of 15° (100 kft) and approximate cosecant-squared (csc^2) in shape from 15° to 50°) (at 100 kft), as illustrated in Figure 2-1. The 3-D coverage of the type B radar is also given for reference. The radar beam will provide low elevation coverage to the ground from -10° to the horizon for higher elevation sites.

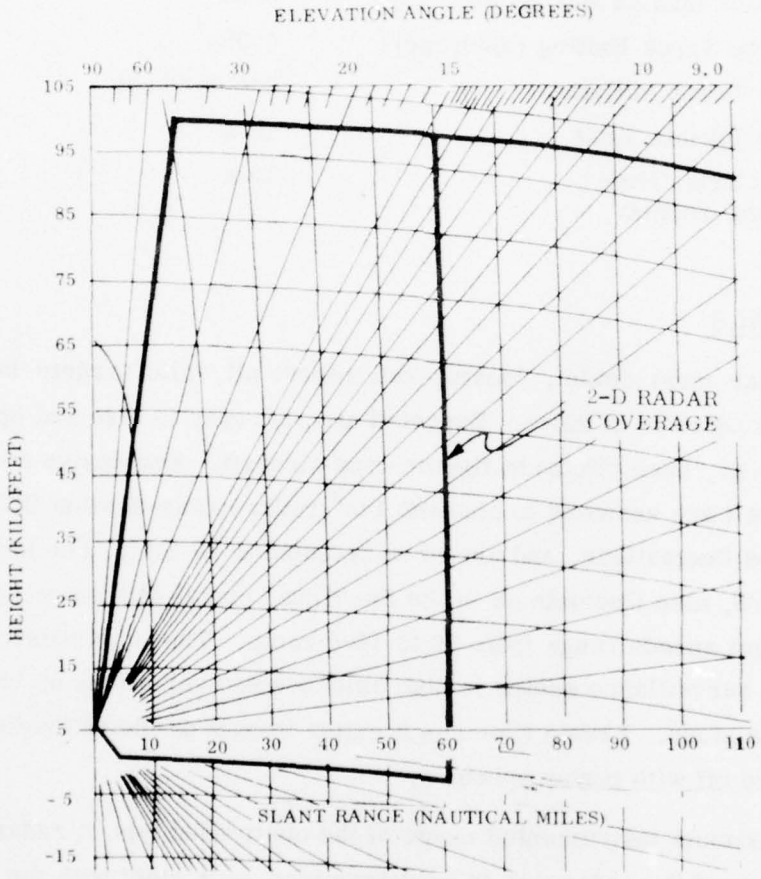


Figure 2-1. Range/Elevation Coverage Requirements for 5000 ft Site Elevation

The radar will have the capability of sector of full 360° scan azimuth coverage, automatically controlled by the radar data processor or via a communication link by the manned site. Target tracking and reacquisition will be accomplished over the full 360°.

3. ACCURACY

The accuracy (rms error) with which the radar determines the range to a target in the coverage based on four scans of data will be 0.25 nmi (1519 ft) or better.

The accuracy in the azimuth estimate of target position after 4 scans of data on a target in the coverage will be 0.5° (8.7 mrad) or better.

4. RESOLUTION

The type A radar will declare 2 targets and initiate 2 tracks with at least 50% probability for two targets separated in range by more than 0.5 nmi.

The radar will declare two targets and initiate two tracks with at least 50% probability, for two targets separated in azimuth by more than 3° in the -10 to 15° elevation interval.

The angle sidelobe adjacent to the main beam on transmit should be at least 20-dB down from the main transmit beam boresight response. Transmit sidelobes further out should be kept at least 30-dB down. All receive sidelobes should be at least 30 dB down from the main receive boresight response.

5. AUTOMATIC DETECTION AND TRACKING

Target detection (track initiation) and tracking will be fully automated in the type A radar, with automatic correlation of radar and Identification Friend or Foe (IFF) returns.

The radar will achieve a 0.95 probability of detection and track initiation on a 1 m^2 RCS target within 30 nmi (or on a 16 m^2 RCS target within 60 nmi) within 16 s after it enters the respective surveillance volumes defined by those maximum ranges. The probability will be at least 0.95 that the radar will maintain (not drop) a track on a valid target in the coverage during the present scan. The probability will be at least 0.999 that the radar will drop a track on a valid target within 12 or 16 s of it exiting

the coverage. The radar will initiate false tracks at an average rate of less than one per hour. The radar will develop a smoothed estimate of the heading of all tracks in the coverage to at least ±5°. The radar will develop a smoothed estimate of the range-azimuth velocity magnitude of a target in the coverage accurate to better than 10% of its actual velocity for nonmaneuvering targets.

The radar design will accommodate the effects of strong multipath returns with respect to initiation and maintenance of tracks. The radar design will accommodate the returns from clutter and provide a clutter improvement factor sufficient to maintain detection and tracking when target and clutter are resolvable. The clutter model should include reflectivities from land, sea, snow, ice and aurora applicable to prevailing environmental conditions anticipated at the sites. The models given in Table 2-2 are to be used for performance evaluation. A clutter improvement factor of 50 dB with respect to ground clutter and 30 dB with respect to weather clutter is the design-to-performance guide.

TABLE 2-2. CLUTTER AND ENVIRONMENT DATA (GUIDE)

	Reflectivity (dB)					
	UHF		L-Band		S-Band	
Land Clutter						
Median	-39		-34		-32	
84th Percentile	-29		-24		-22	
Sea Clutter (Sea-State)						
	(H)	(V)	(H)	(V)	(H)	(V)
1° Depression Angle	-72	-53	-55	-48	-42	-41
3° Depression Angle	-62	-51	-50	-43	-42	-39

(H) is horizontal polarization
(V) is vertical polarization

Weather - Rain up to 15 mm/h from 0 to 30 kft for a storm cell size up to 5 miles in horizontal extent. Wind shear 0 to 80 knots from 0 to 50 kft with an arbitrary shear distribution over this altitude range.

SECTION III

SYSTEM DESIGN

1. REQUIREMENTS ALLOCATION

a. COVERAGE

The range coverage requirements implies a maximum instrumented range of at least 60 nmi, which corresponds to a minimum receive listen time of 741 μs. The maximum practical pulse-repetition frequency (PRF) without interleaving is therefore about 1300 Hz.

The azimuth coverage requirement allows for sector scanning up to and including full 360°. For a fixed number of pulses per azimuth resolution cell, the PRF and azimuth coverage specifies the frame-time beamwidth product, i.e.,

$$T_F \theta_B = \frac{N\theta_c}{PRF \cdot K_{BP}} \tag{3-1}$$

where

θ_c = azimuth sector coverage

N = no. of pulses per azimuth resolution cell

PRF = pulse repetition frequency

θ_B = azimuth resolution (3-dB beamwidth)

K_{BP} = beam packing factor

This relationship is illustrated for 32 pulses in Figure 3-1 for various sector coverages.

Minimizing prime power requirements drives the designs toward narrow beam high gain antennas. Figure 3-1 illustrates, for example, that 4-s data rate is compatible with a 1.5° design, using approximately 240° sector search. It also illustrates that 360° coverage at a 4-s rate calls for a beamwidth of at least 2.3°. This is a major factor influencing the recommended radar design.

The elevation coverage principally affects the $\csc^2$ antenna pattern design. The desire to maintain 20 dB on the first transmit sidelobe and 30 dB on the rest dictates the taper efficiency, or loss, which must be taken as a result of the aperture illumination. For equivalent azimuth Taylor weighting of 30 dB, $\bar{n} = 6$ in a cylindrical array approximately 0.66-dB taper loss results. Accounting for element gain, mutual

coupling effects and taper efficiencies, antenna studies performed on this contract have shown that a $\csc^2$ elevation pattern covering up to 100 kft and -10° to about 50°, with a 15° corner angle and 1.5°, 3-dB nominal azimuth beamwidth results in a one-way directive antenna gain of about 28.5 dB at L-band. The one-way directive gain increases in proportion to the square of frequency, and inversely with the effective solid angle beamwidth.

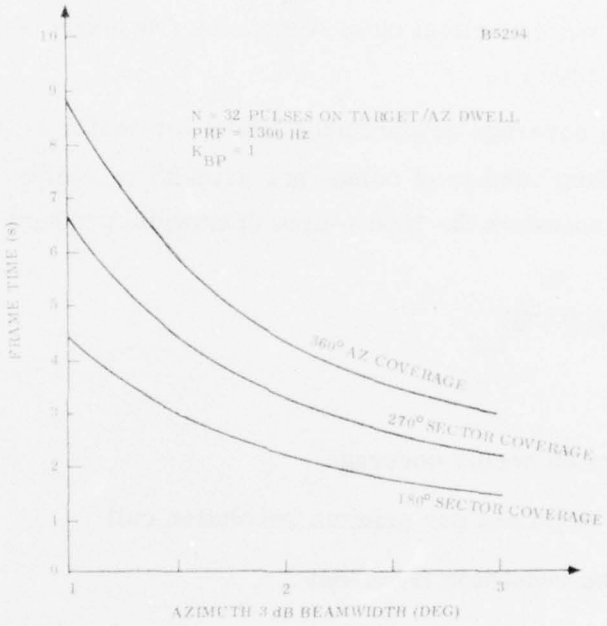


Figure 3-1. Frame Time and Coverage Tradeoff Relationship

b. RESOLUTION

The directive gain is fixed primarily by the pattern. The aperture dimensions increase in direct proportion to the effective solid angle beamwidth and inversely with the frequency. The cylindrical aperture dimensions for a 1.5° (3°) azimuth beamwidth L-band pattern providing the elevation coverage desired has been found in the antenna design studies to be about 44 (22) ft in diameter and 4.5-ft tall. The 1.5° (3°) design uses 64 (32) columns in a 90° arc of the cylinder to form the azimuth beam. The effective aperture for the 1.5° beam case is

$$A_e = \frac{\lambda^2}{4\pi} G \doteq 32 \text{ ft}^2 \qquad (3\text{-}2)$$

The projected physical area of the aperture is about 140 ft^2 (31.1 ft x 4.5 ft). The total taper loss, therefore, for the csc^2 elevation beam with 30 dB $\bar{n} = 6$ Taylor weighted 1.5° azimuth beam is approximately 6.4 dB.

The half-mile range resolution required dictates at least 162 kHz bandwidth waveforms and processing. A bandwidth of 250 kHz allows for range sidelobe control, if required, and nonideal performance. A pulse duration of 128 μs, consistent with reliable solid-state operation at about 15% duty factor, gives a reasonable LFM waveform/pulse-compression signal processor with a BT product of 32.

c. ACCURACY

The quarter-mile range accuracy requirement implies 2:1 range splitting, which is easily accommodated.

An azimuth accuracy of 0.5° requires at most about 6:1 beamsplitting. This level of accuracy can be easily and inexpensively achieved with a sequential lobing type of measurement procedure, in which a ratio is formed of the video 32 pulse integrated samples in adjacent azimuth cells and compared in the data processor to a stored table of beam pattern magnitude ratios vs azimuth arrival angle. It can be shown that this procedure yields a maximum likelihood estimate of angle of arrival in the absence of beam-to-beam echo coherence. Figures 3-2 and 3-3 show the accuracy (rms error) of such a scheme in the presence of thermal noise vs angle of arrival (in 3-dB beamwidths), signal-to-noise ratio (SNR), and number of pulses, as given by:

$$\sigma = \frac{\sigma_\theta}{\theta_B} = \frac{\gamma_\theta}{\sqrt{2(k-1)\, n\, \overline{SNR}}} \qquad (3\text{-}3)$$

where

σ_θ = actual rms error

σ = rms error normalized to 3-dB beamwidth

γ_θ = measurement sensitivity factor

θ_B = 3 dB beamwidth (rad)

k = number of diversity pulses noncoherently integrated per beam

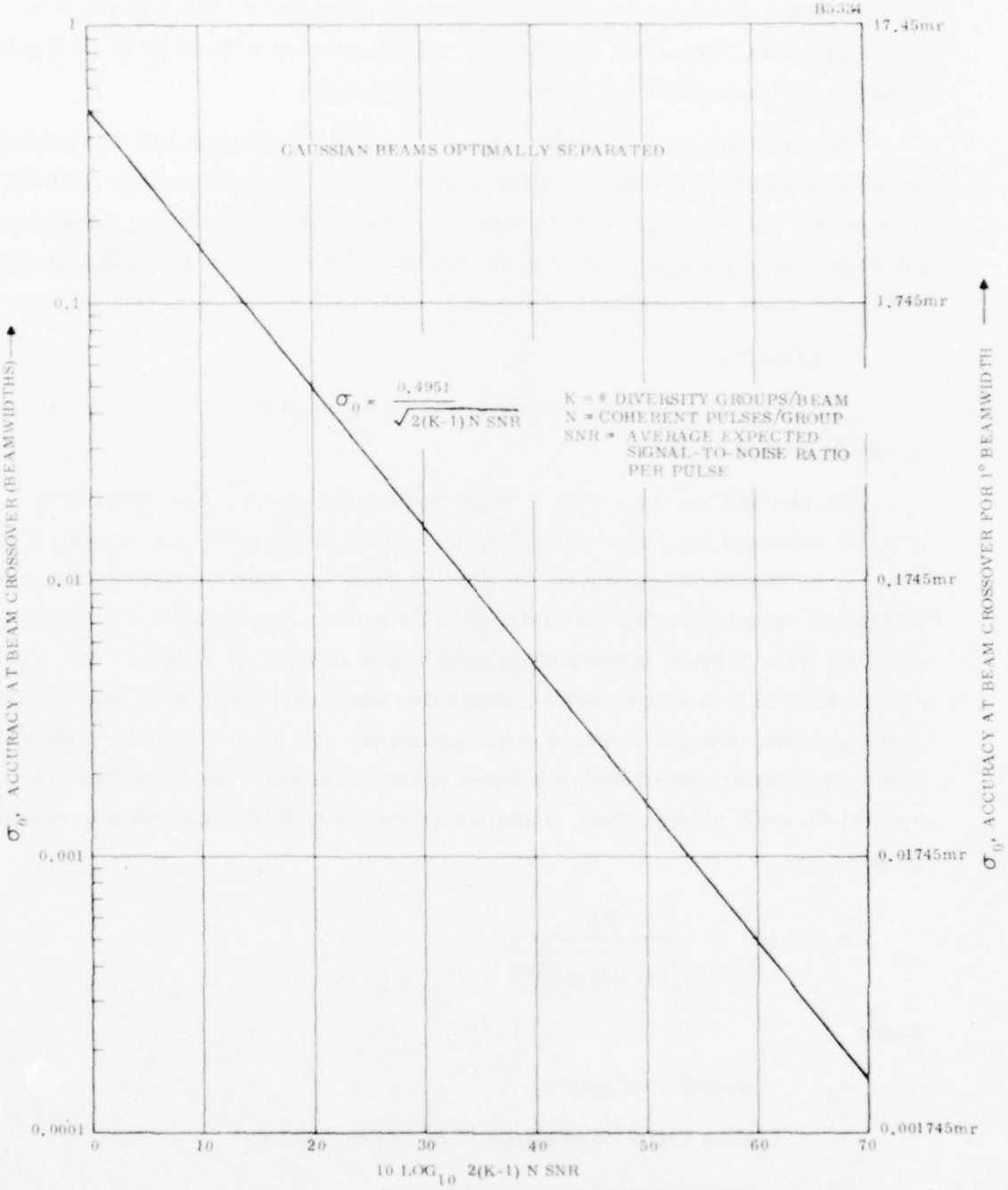


Figure 3-2. Sequential Lobing Beam Crossover Accuracy

n = number of pulses coherently integrated per beam

$\overline{SNR}$ = average expected boresight per pulse SNR

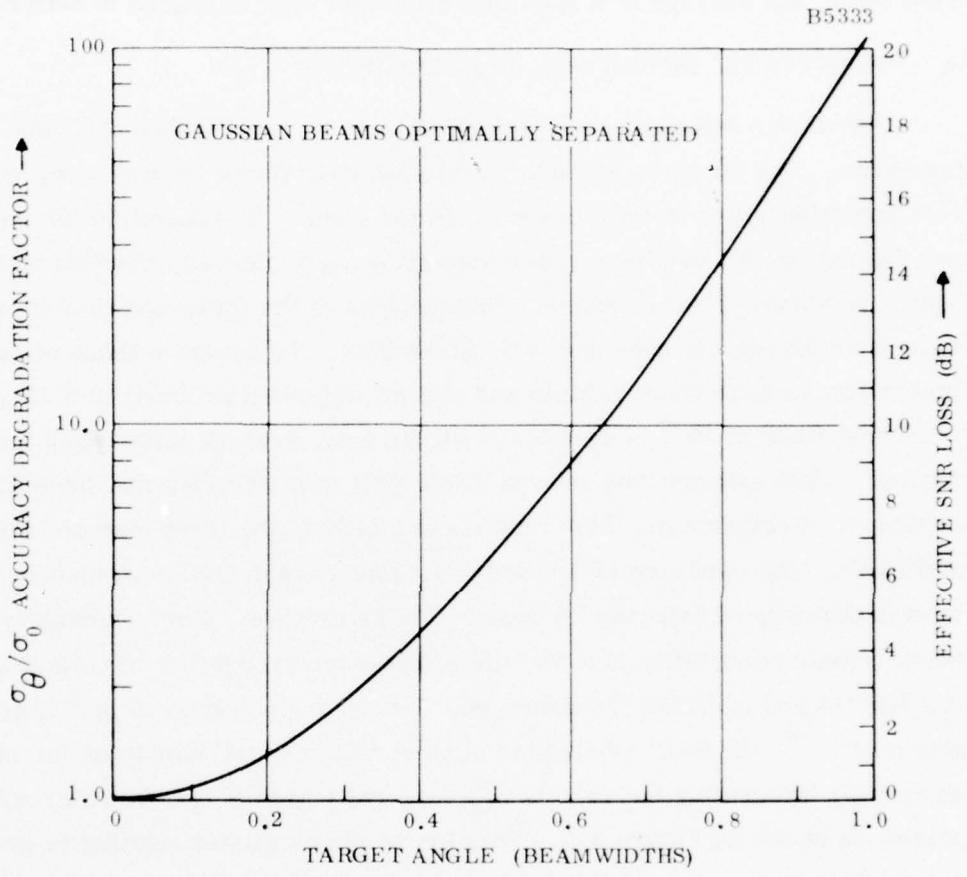


Figure 3-3. Accuracy Degradation vs Target Angle

This result assumes no significant target fluctuations from one azimuth dwell to the next and Swerling II type fluctuation from diversity pulse to diversity pulse. The beam packing is optimum when the distance between beams is 85% of the one-way 3-dB beamwidth.

For an average expected SNR on the order of 0 dB per pulse as required for a detection, Figure 3-2 shows that about 14:1 beam splitting is achieved on a target exactly at the crossover point between two azimuth beams. For a 1.5° (3°) beam,

this corresponds to an azimuth accuracy of about 0.1° (0.2°). Not accounting for the two estimates obtained on such a target, performance is worst when the target is on the peak of a beam. In this case, it degrades to about 0.35° (0.7°). Naturally, for closer or higher SNR targets, the per scan accuracy improves accordingly. For either beamwidth, the average accuracy overall target arrival angles is better than 0.5°.

d. AUTOMATIC DETECTION AND TRACKING

Automatic detecting and tracking of up to 20 simultaneous targets is required of the radar. The three-out-of-four (3/4) scan cumulative criterion represents a reasonable detection/track initiate criterion in the clear. It reduces the effect of false alarms per resolution cell per beam while also allowing a reduced detection probability per scan - and hence smaller radar. Alternatives to the three-out-of-four scan criterion were considered, viz one- and two-out-of-four. To compare these alternatives, the probability of false track initiate and overall detection probability 0.95 respectively, were held fixed at 10^{-6}, consistent with the unity average false track initiate rate desired. Both alternatives showed lower SNR required than the three-out-of-four criterion. Furthermore, both criteria outperform the three-out-of-four in clutter and multipath. The variation of 3/4 and 1/4 cumulative detection probability with single-scan probability of detection is depicted in Figure 3-4. For a cumulative detection/track initiate probability of 0.95, the single-scan probability of detection required is 0.9 for 3/4 and 0.53 for 1/4 detection. For a single cell/scan probability of false alarm of 10^{-6}, the SNR required to achieve this 0.9 probability of detection (by non-coherently integrating the results of K-diversity groups of N/K coherently integrated pulses) is shown in Figure 3-5. This figure shows a minimization in per pulse required SNR in the vicinity of four diversity channels. For 32 total pulses, the required average SNR associated with 4 diversity channels and 8-pulse Doppler processing is about 1.5 dB. However, it is not clear that 10^{-6} probability of false alarm per cell is reasonable. First, by reducing the per cell probability of false alarm, the single-scan radar threshold can be lowered thereby decreasing the average expected SNR/pulse required for detection to the 0.9 single-scan level. The question that is addressed in this study is "How small may the single scan/cell probability of false alarm be specified without significantly increasing the data processing load with noise tracks?" The answer to this question obviously depends rather strongly on the exact nature of the track initiate, maintenance, and dropping algorithms. The problem was analyzed in detail taking into account target motion, and scan-to-scan correlation window size. Considering a target with no scan-to-scan motion as a simple example, the variation of the probability of a false track initiate (i.e., initiate on noise only) with single cell/scan probability of false alarm is as shown in Figure 3-6.

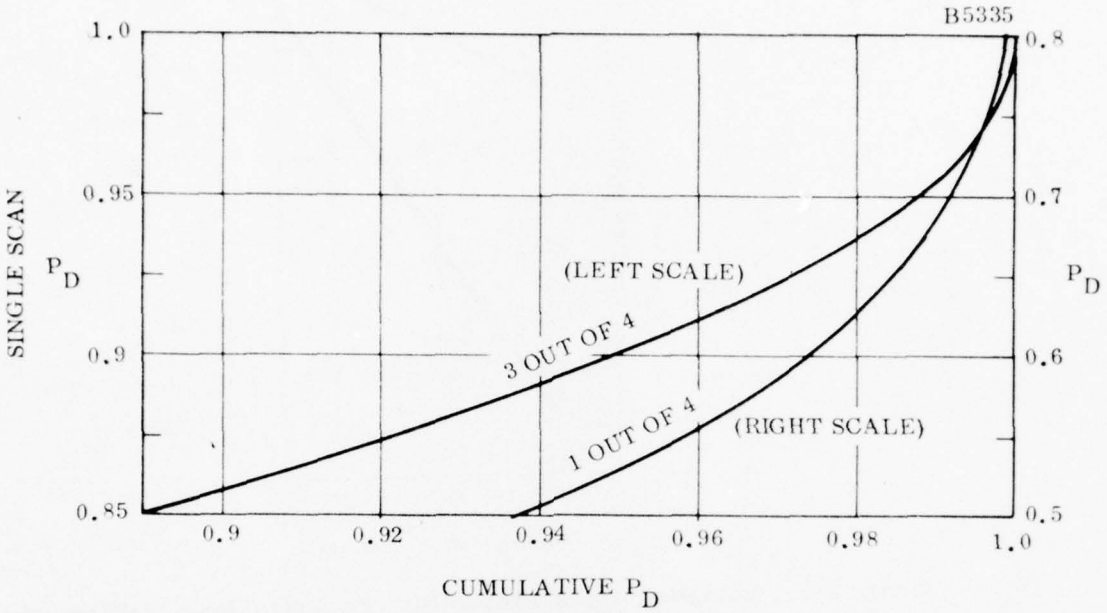


Figure 3-4. M-Out-of-N Detection Performance

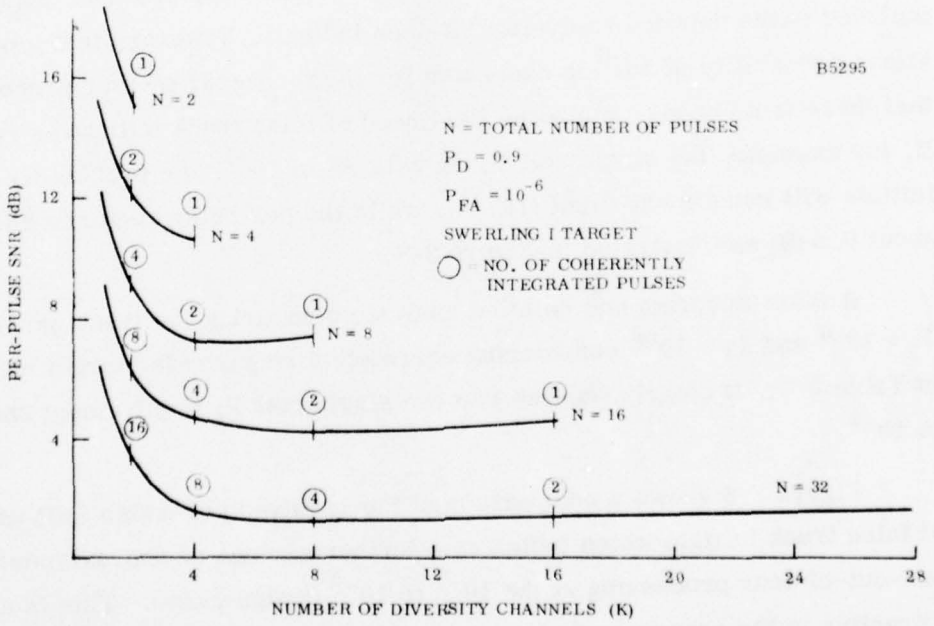


Figure 3-5. Effect on Diversity on Detection Requirements ($P_{FA} = 10^{-6}$)

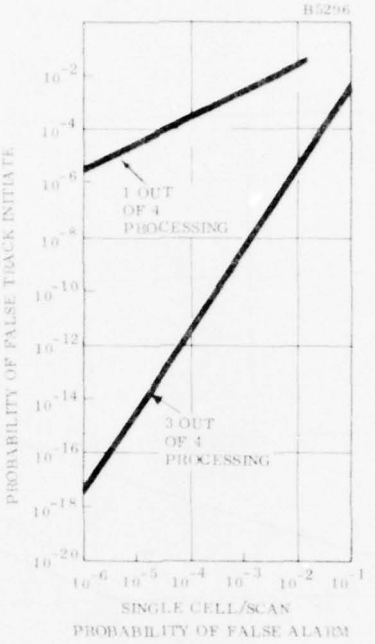


Figure 3-6. Variation of the Probability of a False Track Initiate with Single Cell/Scan P_{FA} on a No Scan-to-Scan Motion Target

This figure is somewhat optimistic in that it does not account for the independent chances of false alarm involved in searching a single-scan correlation "window" of range-azimuth resolution cells - necessary to allow for possible target motion (and included in the detailed analysis). It does indicate, however, that a per cell false alarm probability of 10^{-6} is excessive for the three-out-of-four processing in that there is no need to make the likelihood of false track initiate as remote at 10^{-17}. If, for example, the single cell P_f is relaxed to 10^{-4}, the probability of false track initiate will remain excellent (10^{-11}), while the per pulse required SNR reduces to about 0.2 dB as illustrated in Figure 3-7.

A more accurate and detailed analysis comparing the track parameters for $P_f = 10^{-4}$ and $P_f = 10^{-6}$ considering correlation required for target motion is included in Table 3-1. It clearly implies that the single cell P_f requirement should be relaxed to 10^{-4}.

Figure 3-8 shows a comparison of the required per-pulse SNR vs the probability of false track initiate which indicates a further savings of approximately 1 dB using one-out-of-four processing at the 10^{-7} to 10^{-8} design range. This is also more attractive in the presence of clutter and multipath as described below and, therefore, is the recommended track initiate algorithm.

TABLE 3-1. AUTOMATIC TARGET DETECTION AND TRACK PARAMETERS

	3/4 Processing		1/4 Processing	
False Alarm Probability	10^{-4}	10^{-6}	10^{-4}	10^{-6}
Per-Scan Detection Probability	0.9	0.9	0.54	0.54
SNR Required	0.2 dB	1.5 dB	-3.5 dB	-1.8 dB
P (False Track Initiate)	5×10^{-8}	5×10^{-14}	4×10^{-4}	4×10^{-6}
P (Correctly Drop Track)	0.927*	0.999*	0.856**	0.9984**
P (Correctly Maintain Track)	0.999*	0.999*	0.95**	0.95**

* 1 out of 3 track maintenance
** 1 out of 4 track maintenance

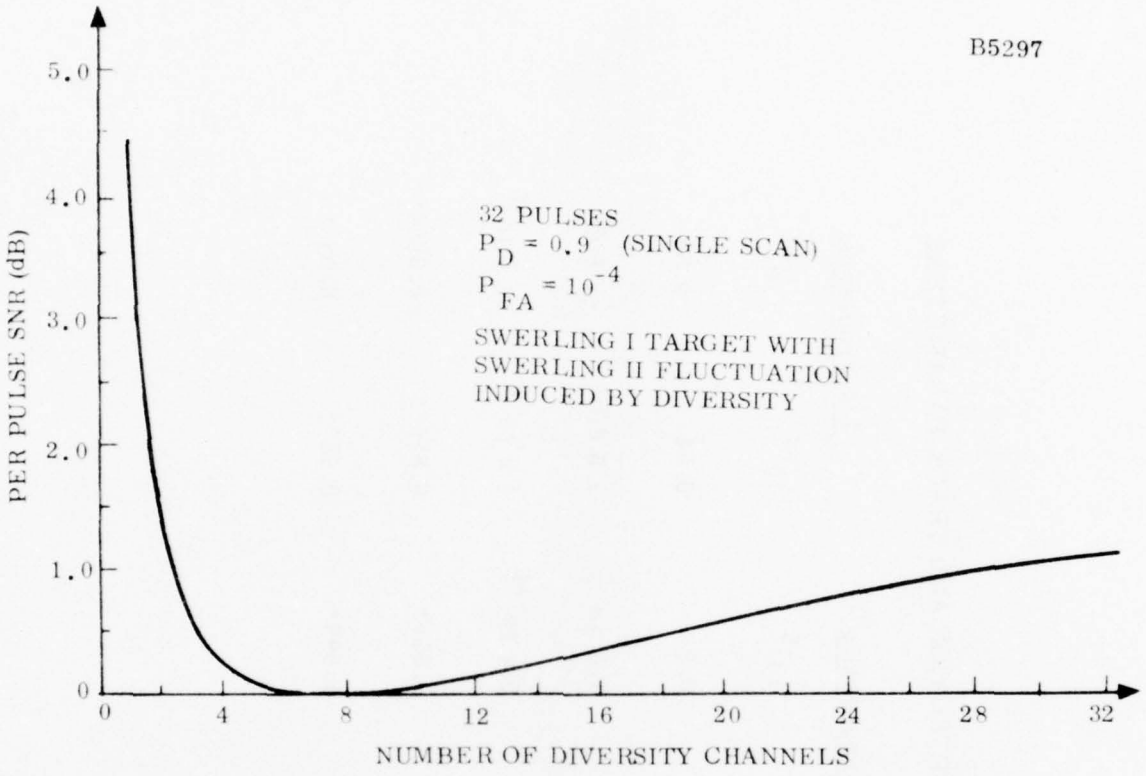


Figure 3-7. Effect of Diversity on Detection Requirements ($P_{FA} = 10^{-4}$)

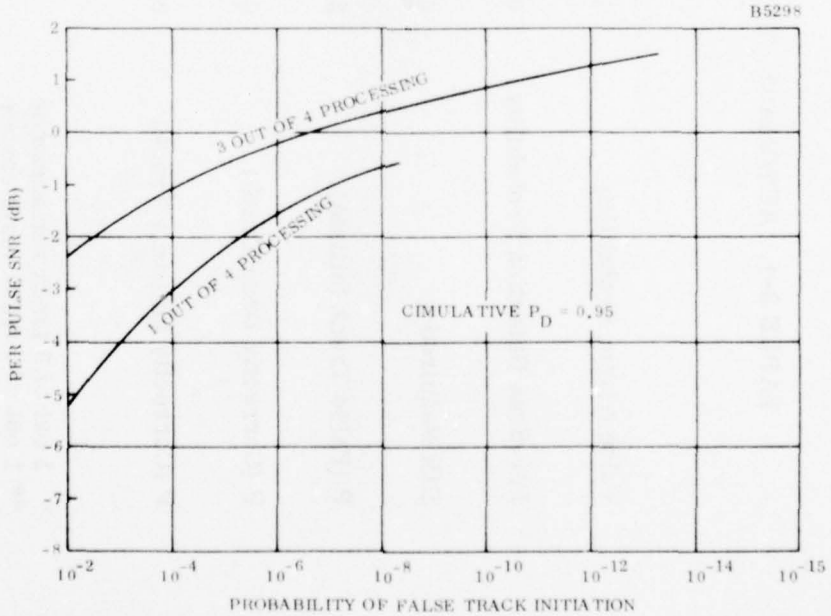


Figure 3-8. Required SNR for Desired False Track Initiation Rates

The purpose of track initiation is to establish a sufficiently accurate target state vector in order to initialize the tracking filters and minimize the probability of losing initial tracks. The "M-out-of-N" scheme is well suited to this role. For the 3-out-of-4 process used above to verify detections, the position vs time (normalized by the per-scan measurement accuracy, σ_m) is shown in Figures 3-9 and 3-10 for the Type 2-D and 3-D radars. The variation in the times reflect the 4-s and 12-s scan rates, respectively. It is seen that the prediction errors are substantially reduced in four scans (4-out-of-4 detections are shown) thus providing a reasonable state vector uncertainty for track filter initialization.

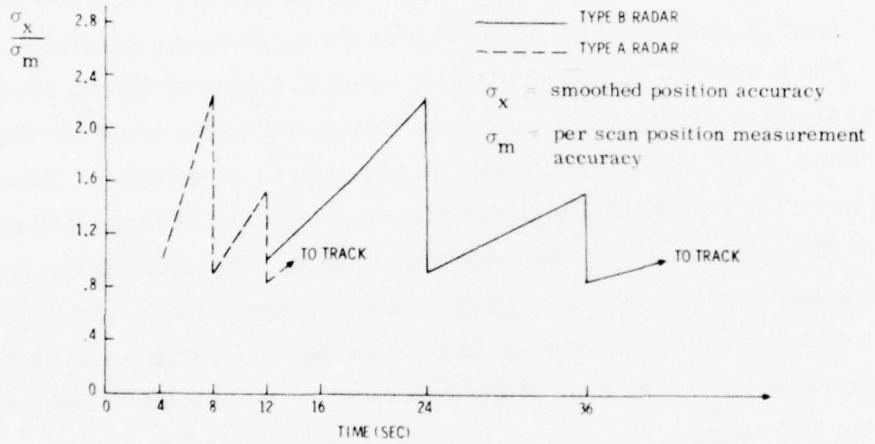


Figure 3-9. Position Accuracy vs Time During Track Initiation, N = 4

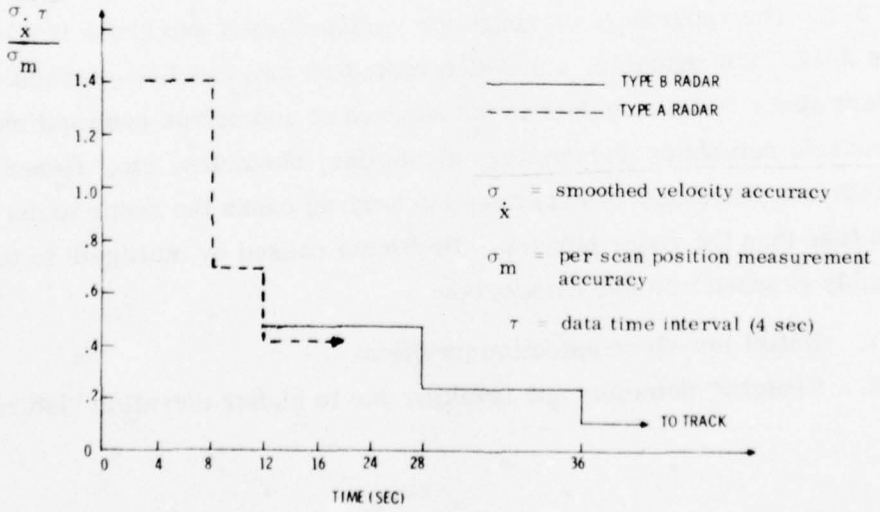


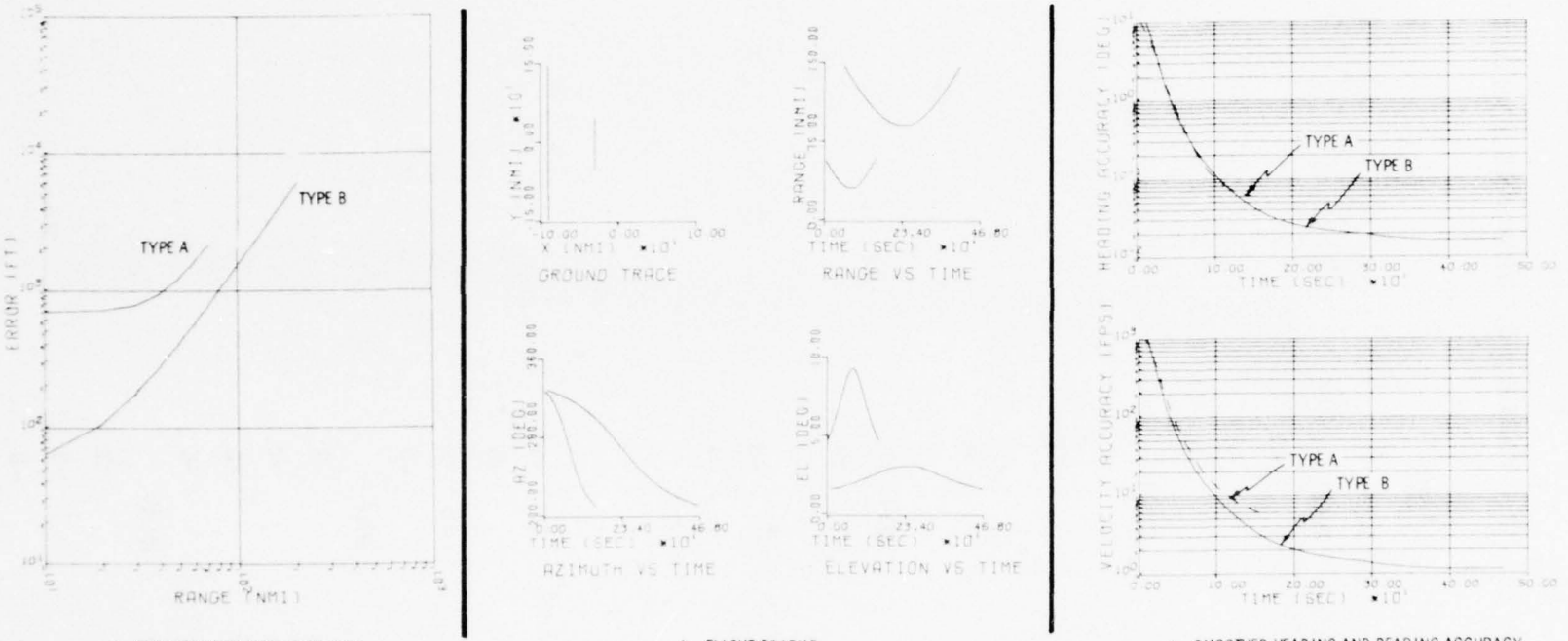
Figure 3-10. Velocity Accuracy vs Time During Track Initiation

The minimum tracking accuracy requirements of ±5° in heading and ±10% in speed are a function of target velocity, flight path through the coverage, and radar type. The following sample track assumes a 2400-knot target penetrating the radar coverage at a constant altitude in a north-to-south flight path laterally displaced west of the radar by one-half of its maximum range. Figure 3-11(b) illustrates this profile for the 60-nmi Type A radar and the 150-nmi version of the Type B radar. The per-scan measurement error vs range is shown in Figure 3-11(a) for each radar type. This error is dominated by the thermal angle error component except for short ranges for the Type A radar, which clearly shows the range-independent jitter error limitation. The resulting smoothed heading and velocity accuracy as a function of track time is shown in Figure 3-11(c) for the in-coverage durations of both the Type A and Type B radars. The specified accuracy is achieved shortly after track start (after three scans for the Type B radar and after seven scans for the Type A radar). As shown, the a priori state vector is assumed to be unknown. Therefore, the specified accuracy is essentially achieved upon completion of track initiation. Thus, the track filter problem is a relatively simple task. The error is the 2-D and 3-D uncertainty of the Type A and Type B radars, respectively, and which is representative of the error for a constant-altitude target or a variable-altitude target with high-quality IFF in the case of the 2-D radar or a constant/variable-altitude target for the 3-D radar.

e. PERFORMANCE IN MULTIPATH

Present DEW line sites range in elevation from 42 to 4720 ft, as tabulated in Table 3-2. The radar horizon range for various target and radar heights is shown in Figure 3-12. For example, a 500-ft target at 60 nmi has line-of-sight visibility only to radars above 700 ft in height in the absence of anomolous propagation affects such as excessive refraction and ducting, mountains, obstacles, etc. Generally speaking, multipath and diffraction effects near the horizon cause the radar to detect targets at ranges less than the radar horizon. Problems caused by multipath to the radar may be roughly grouped into two categories:

1. Initial low-flyer detection problem
2. "Patchy" detection and tracking due to higher elevation "lobing"



a. PER-SCAN ESTIMATION ERRORS

b. FLIGHT PROFILE

c. SMOOTHED HEADING AND BEARING ACCURACY

Figure 3-11. Target Track Example

TABLE 3-2. DEW LINE SITE ALTITUDES

Site	Height (ft)
BAR	42
BAR -1	84
-2	223
-3	100
-4	330
CAM	160
-1	160
-2	123
-3	190
-4	1104
-5	1297
DYE	2420
-1	4720
-2	
-3	
-4	1081
FOX	75
-2	571
-3	1642
-4	1330
-5	1947
LIZ -2	75
-3	130
PIN	361
-1	371
-2	97
-3	108
-4	408
ROW	60
-1	74
-2	59
-3	61

The first problem is attributable primarily to the diffraction phenomenon, which results in drastically attenuated signals below and near the radar horizon. The second cause arises because of in-phase and out-of-phase addition due to the path length difference between the direct and indirect paths of propagation for targets above the radar horizon.

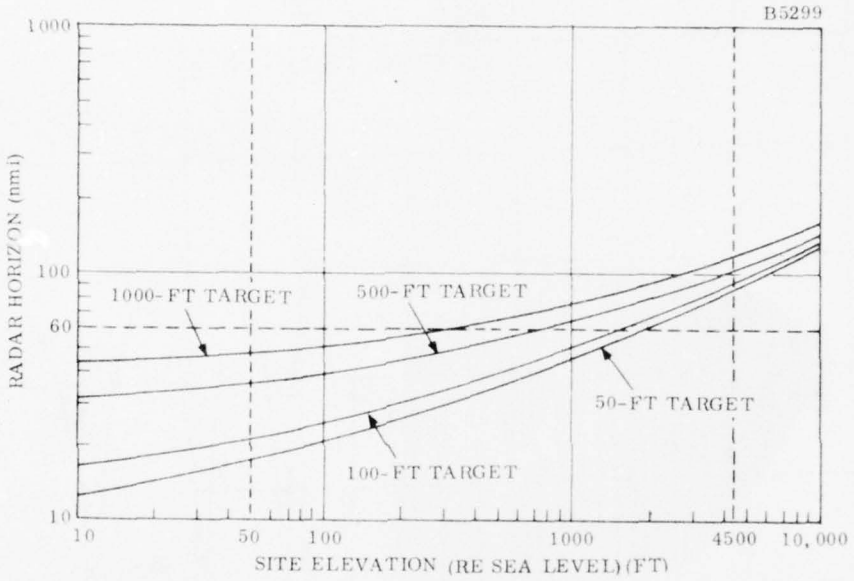


Figure 3-12. Radar Horizon vs Site Elevation

Figure 3-13 is a plot of the two-way multipath propagation factor* in dB vs range for a constant height target at 500 ft approaching an L-band radar at 1000 ft height. This factor directly adds to the SNR in free space, and so the range at which the SNR in the presence of multipath becomes equal to that required for detection in free space is that corresponding to the interaction of the two-way propagation factor and the 40 $\log_{10}$ r/r_{FS} curve. (r_{FS} = free space detection range of the radar). For example, Figure 3-13 illustrates that a 1000 ft L-band radar with a free space detection range of 60 nmi detects a 500 ft target at about 60 nmi. Curves such as Figure 3-13 have been used to compare UHF and L-band performance for 500-ft target vs

*By taking a sea-state of zero, the most severe multipath case results, corresponding to specular reflections.

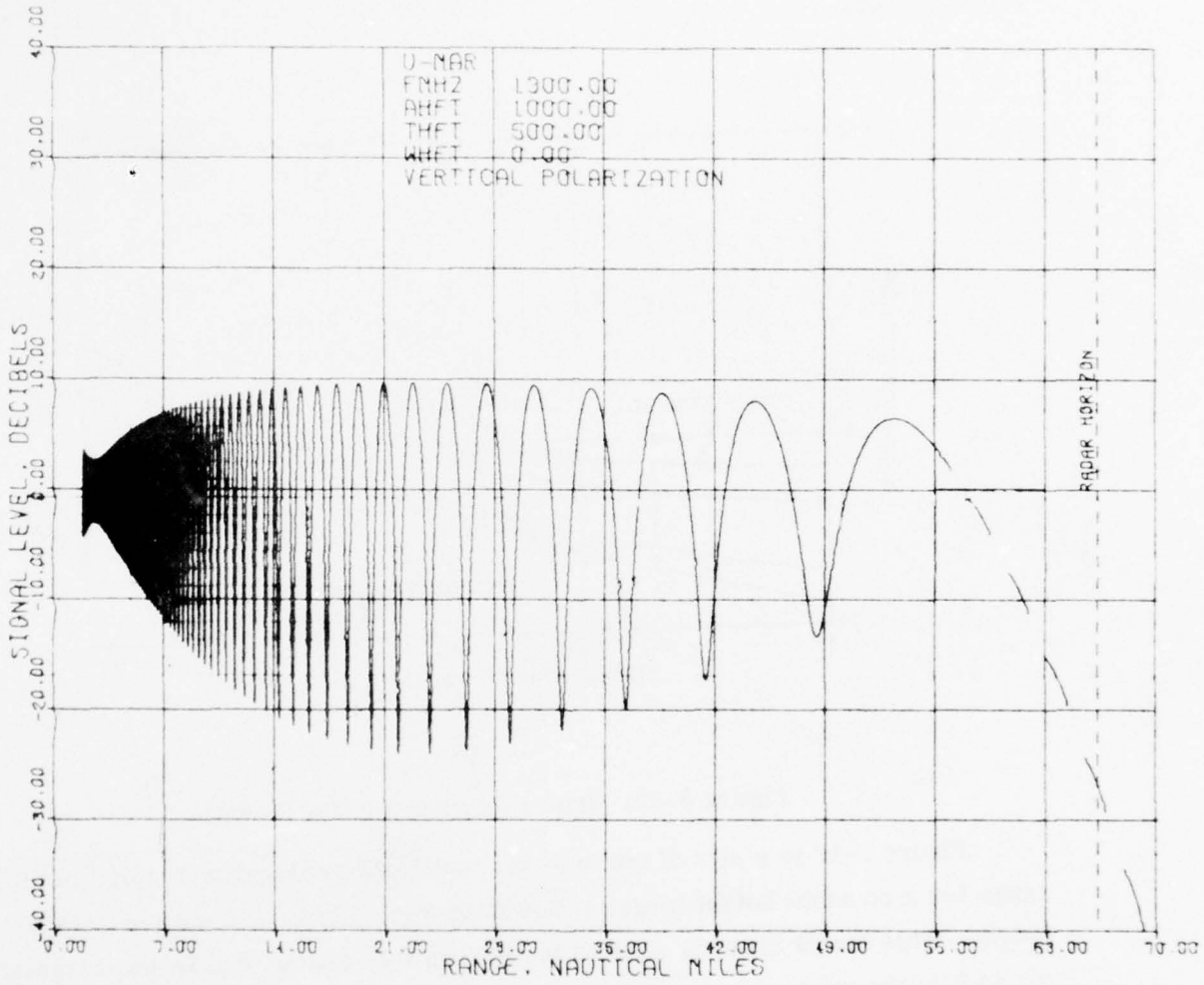


Figure 3-13. Multipath F-Factor for a 500-Ft Target Height and a 1000-Ft Radar

site elevation in multipath, the results of which are graphed in Figure 3-14. The L-band radar has a 5 to 15-mile advantage over a UHF radar, depending on the extent of additional tower mounting for the L-band antenna owing to its smaller size and lighter weight. This can represent up to about 10 dB SNR advantage for L-band over UHF for the low elevation sites.

The cumulative M-out-of-N detection of low flying targets is even more adversely affected by the diffraction multipath and diffraction. Figure 3-15 shows the cumulative detection probability for a 3-out-of-4 process of a 150-ft L-band 60-nmi range radar (single scan $P_D = 0.9$) against a constant 500-ft height 2400-knot target. The detection range is about 38 nmi for 0.95 cumulative probability of detection in multipath at 10^{-4} false alarm probability.

The "patchy" detection problem caused by interference region lobing can also be illustrated (Figure 3-16) by examining the performance of the same target against the same radar, only located at the highest site of 4500 ft. For this radar, a 60-nmi 500-ft target is well above the radar horizon. The radar would get an occasional track initiate to well beyond 60 nmi, but would not get a reliable track initiate until about 40 nmi. By contrast, the single-scan detection range indicated by Figure 3-14 is well beyond 60 nmi. Under these severe multipath conditions, the cumulative four-scan detection range is actually less than the single-scan detection range. This is because of the significant probability that the target will be in a null of the propagation factor on more than one of the four scans. Better cumulative detection in multipath results when the criterion is 1 or 2 out-of-four. The cumulative detection performance under the one-out-of-four criterion is shown in Figures 3-17 and 3-18. Scan-to-scan processing based on the one-out-of-four criterion is recommended for a baseline design because of its superior performance in-the-clear, in multipath, and in clutter.

Another manner of illustrating the lobing effect of multipath on the radar for targets in the interference region is to show single-scan detection contours on a range-height-angle chart. Figure 3-19 shows the coverage in multipath afforded by a first-cut synthesis of a "typical" 100-kft $\csc^2$ pattern on a 60-nmi radar. This pattern was synthesized by weighting six uniform sin x/x beams for the sole purpose of illustrating multipath effects. Also, the attempt was made to account for the decreasing atmospheric loss at higher elevations, which would increase the high angle appreciably over that indicated in Figure 3-19. More practical and detailed syntheses of the actual pattern were accomplished in the study, taking into account the array cylindrical geometry, elevation patterns, but were inconvenient to use in the multipath analysis.

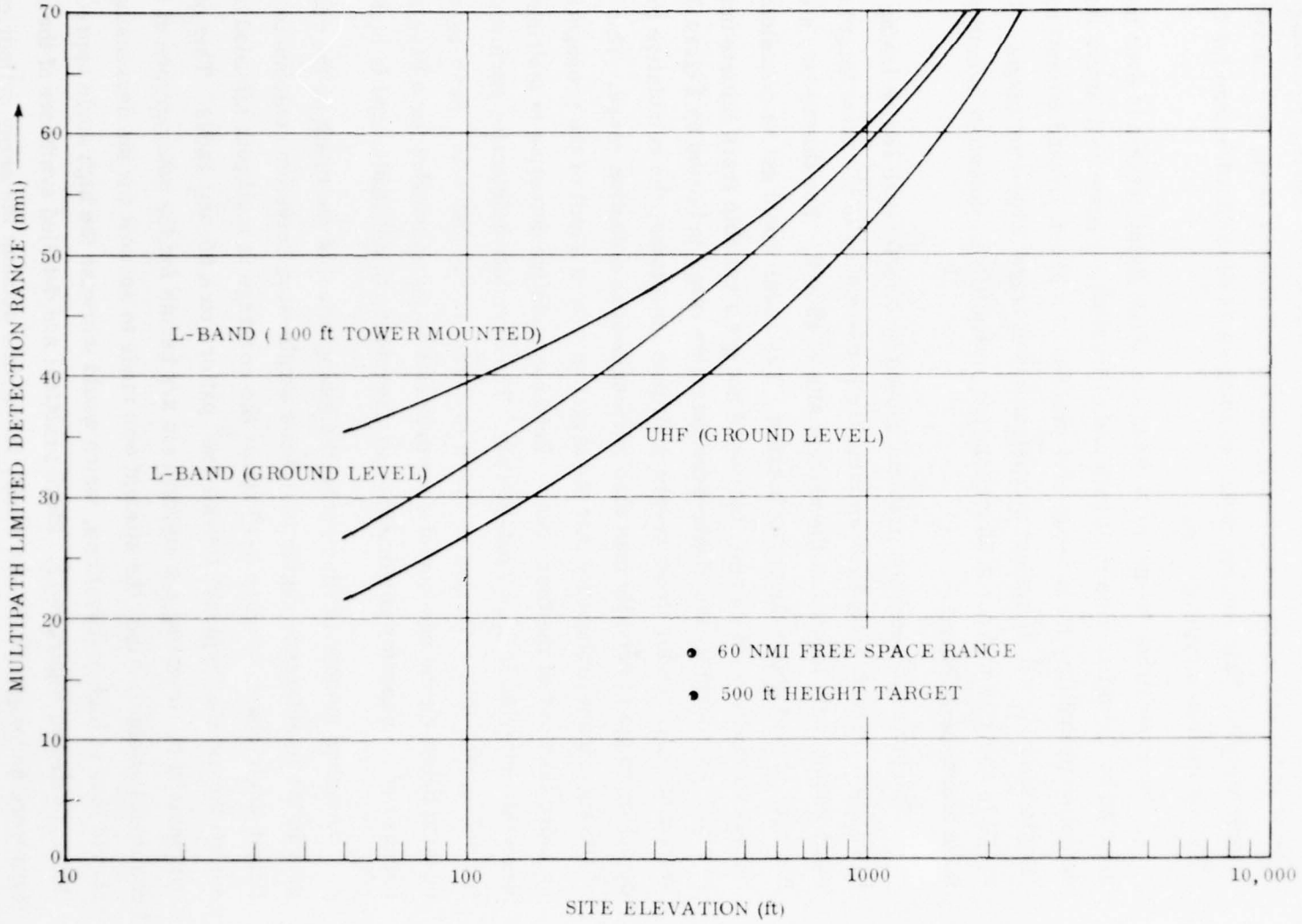


Figure 3-14. Comparative L-Band/UHF Multipath Performance

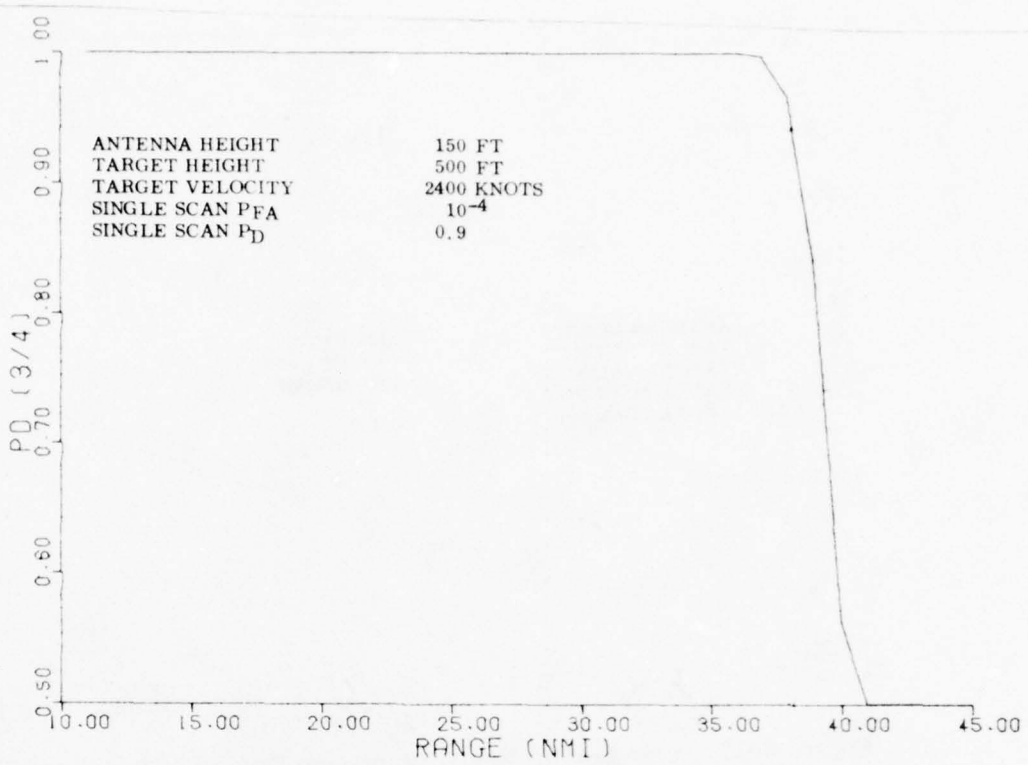


Figure 3-15. Three-Out-Of-Four Cumulative Detection for a 150-Ft Radar and a 500-Ft Target Height

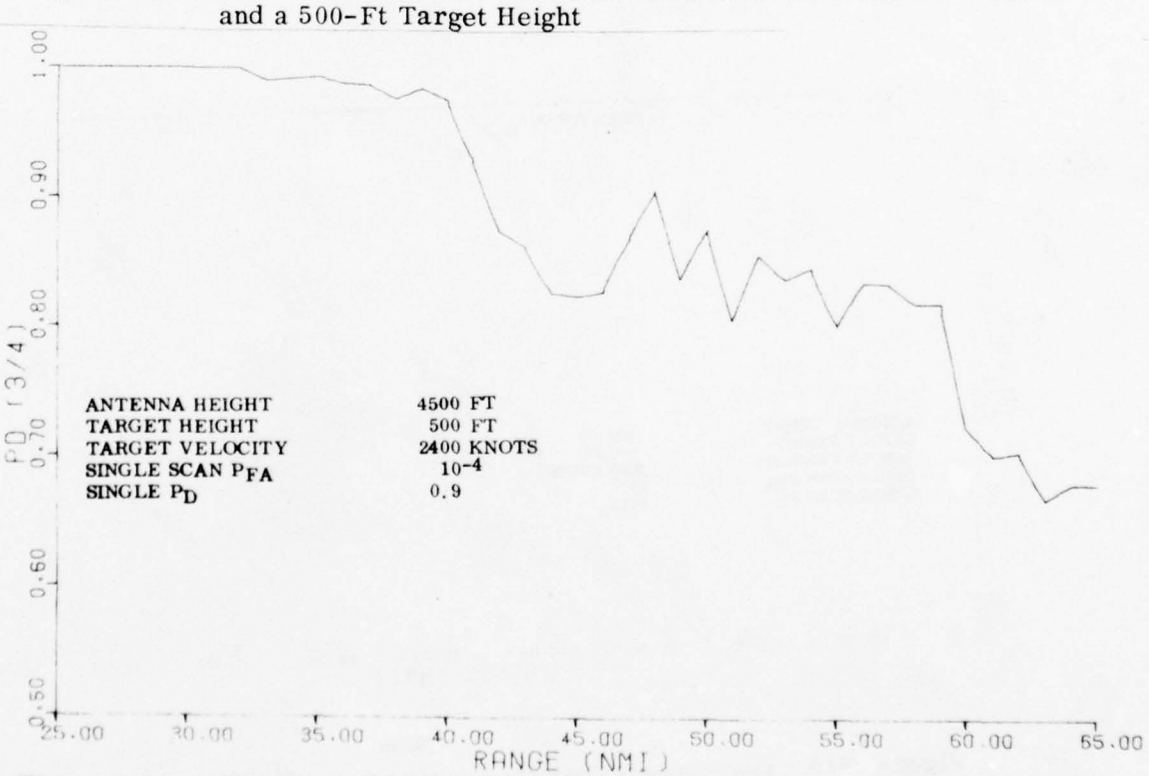


Figure 3-16. Three-Out-Of-Four Cumulative Detection for a 4500-Ft Radar and a 500-Ft Target Height

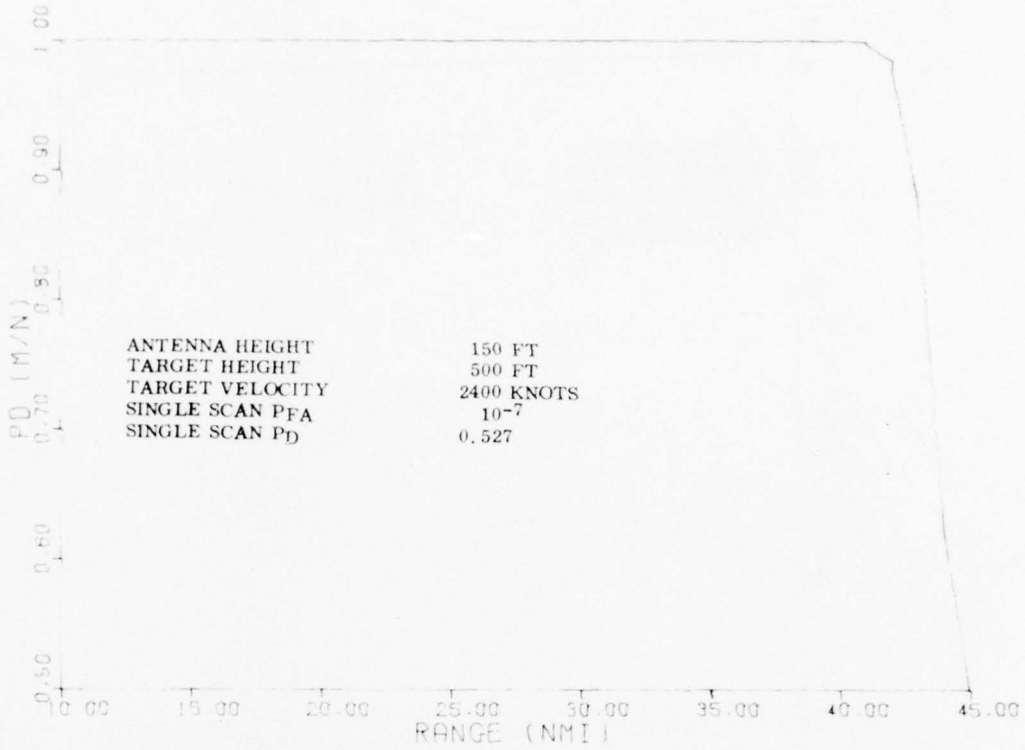


Figure 3-17. One-Out-of-Four Cumulative Detection For a 150-Ft Radar and 500-Ft Target Height

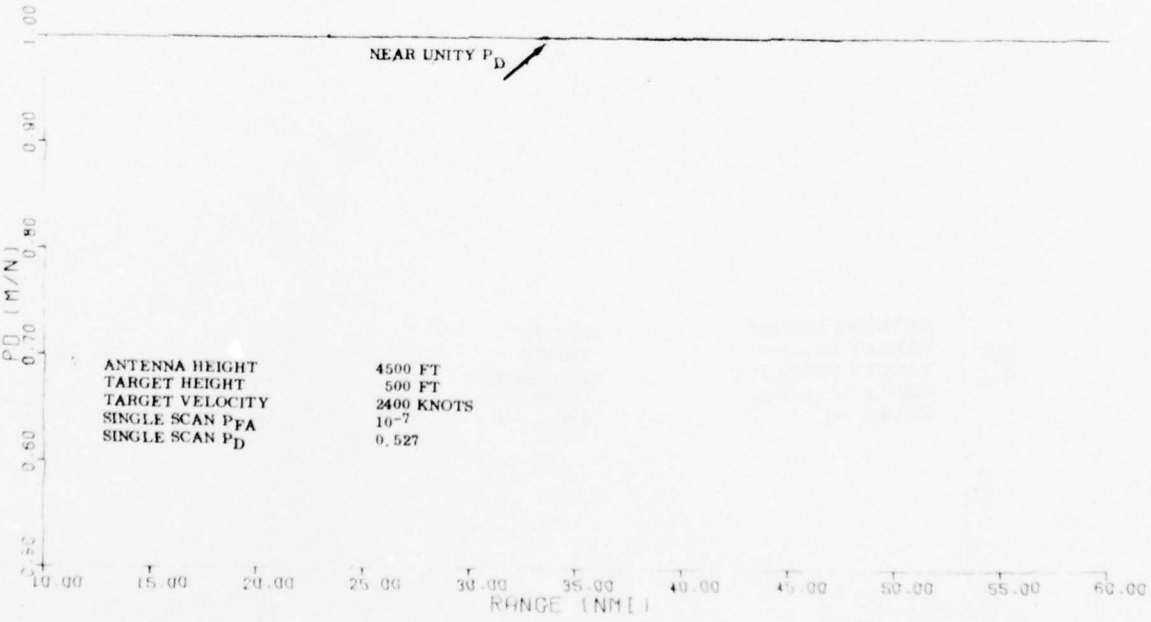


Figure 3-18. One-Out-of-Four Cumulative Detection for a 4500-Ft Radar and 500-Ft Target Height

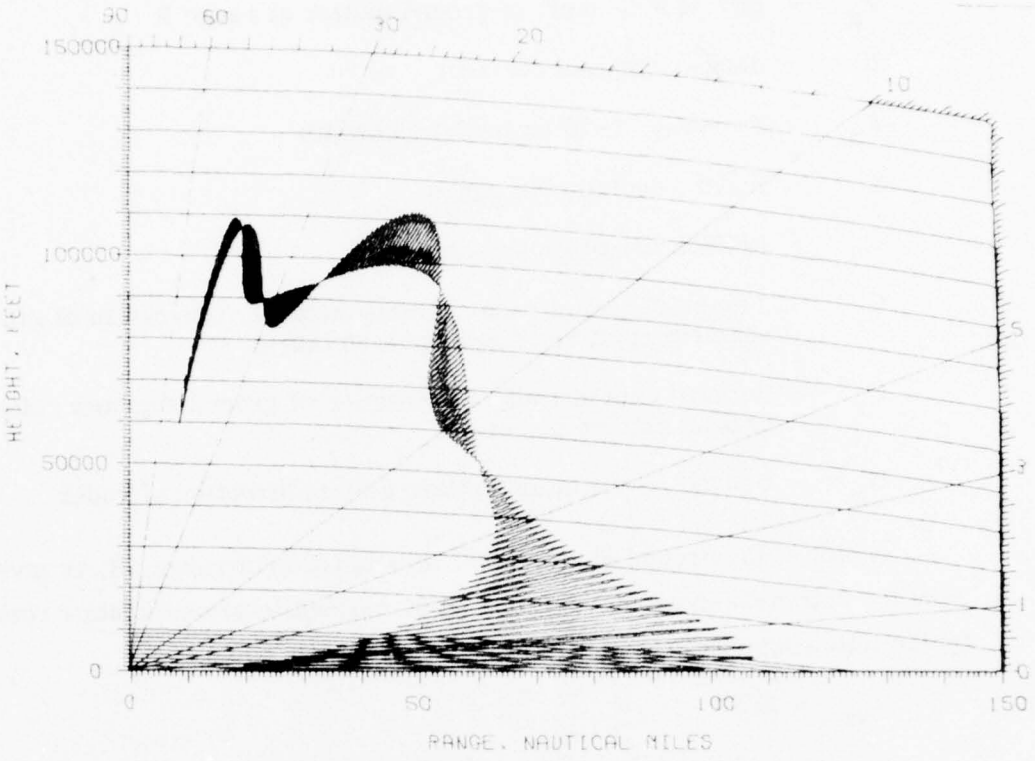


Figure 3-19. Coverage Pattern in the Presence of Severe Multipath

f. CLUTTER REQUIREMENTS

Design requirements for the Unattended Radar depend on the environment in which it must operate. A quantitative description of this natural environment, comprised of land, sea and weather clutter, will vary markedly over the possible radar site locations. Design specifications were established to permit the radar to meet performance requirements in the most severe site clutter environment and, thereby, exceed the requirements for most site locations. In accordance with this philosophy, a worst case environment was quantitatively defined and the radar design is based on this pessimistic model.

(1) Ground Clutter RCS

Ground clutter is assumed to enter the radar through the mainlobe. The RCS of this clutter relative to a target RCS is given by the expression:

$$\sigma_g = R\,\theta_{az}\, r\sigma_o\, G_t'\, G_r'\, G_g \qquad (3\text{-}4)$$

σ_g = RCS of a segment of ground clutter at range R

R = Range to ground segment

θ_{az} = Two-way, 3-dB azimuth beamwidth

r = Radar resolution in range

σ_o = Reflectivity of ground clutter

G'_t = Transmit gain of radar antenna pattern in direction of ground segment relative to peak gain on target

G'_r = Receive gain of radar in direction of ground segment relative to peak gain on target

G_g = Ground re-radiation pattern gain in direction of radar

A plot of the ground clutter RCS, as a function of range, R, is given in Figure 3-20 for both median ground clutter and 84 percentile ground clutter return as defined by the following conditions:

θ_{az} = 1.5°

r = 600 m corresponding to a 250-kHz signal bandwidth

σ_o = -34 dBm^2/m^2 for median ground reflectivity and -24 dBm^2/m^2 corresponding to the 84th percentile clutter as stated in the SOW

G_t = 1 (worst case assumption)

G_r = 1 (worst case assumption)

G_g = 1 (worst case assumption)

The ground clutter RCS shown in Figure 3-20 is highly pessimistic because the gain factor G_g and relative factors G_t, G_r were taken as unity. This would be correct for the case in which the radar beam is pointed perpendicular to the clutter as might occur when the radar beam is directed at a mountain or other prominance rising above the ground plane. More typically, the ground plane itself would be illuminated and the resulting clutter return would be received off the peak of the radar antenna pattern. It will be shown that this effect attenuates the ground plane clutter by 3 to 10 dB depending on the radar range and antenna height. The G_g term is a function of the grazing angle made by the radar beam. For an ideal diffuse scatterer the re-radiation pattern varies as the sine of reflected angle which equals the radar beam grazing

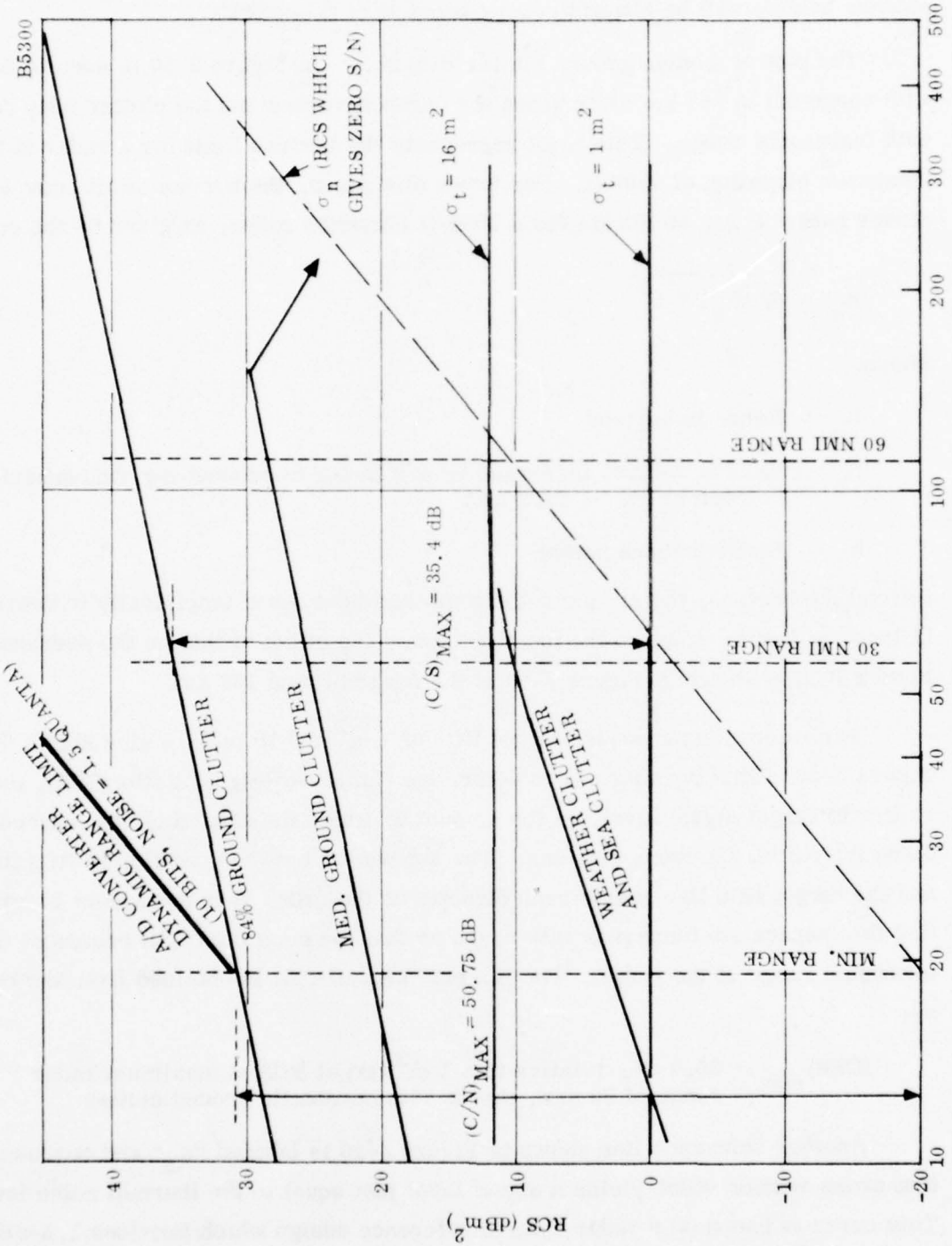


Figure 3-20. Clutter and Signal RCS After Pulse Compression

angle. Ground plane clutter attenuation of 10 to 30 dB, depending on radar range and antenna height, will be shown to occur because of this effect.

The plot of median ground clutter RCS shown in Figure 3-20 is seen to increase with range out to 153 km after which the curve reverses and the clutter falls rapidly with increasing range. This point represents the horizon limit for a radar at the maximum elevation of 4500 ft. For lower elevations, the horizon limit occurs at closer range; e.g., at 102 km for a 2000-ft elevation radar, as given by the equation:

$$R_h = \sqrt{2R_e h + h^2} \qquad (3\text{-}5)$$

where:

R_h = Range to horizon

R_e = Earth's radius, increased by 4/3 factor to account for atmospheric refraction (R_e = 8495 km)

h = Radar antenna height

Beyond the horizon, the ground reflectivity has been found empirically to decrease at least as fast as range to the fourth power. The effect of this on the average ground clutter RCS is shown in Figure 3-20 at the range beyond 153 km.

For reference purposes, target RCS of 1 m^2 and 16 m^2 are also shown in Figure 3-20. This permits one to determine Clutter-to-Signal Ratio (CSR), the clutter to target signal level, as the amount by which the ground clutter exceeds these typical target cross sections. The separation between the clutter RCS line and the target RCS line can be read directly as the CSR. It is seen from Figure 3-20 that this separation increases with range so that the maximum CSR occurs at the maximum range of the radar. The largest value of CSR is obtained from the curve as:

$(CSR)_{max}$ = 35.4 dB, relative to a 1 m^2 target RCS at maximum radar range of 30 nmi, due to 84th percentile ground clutter (3-6)

Another reference line shown in Figure 3-20 is labeled "σ_n" and corresponds to that cross section which yields a signal level just equal to the thermal noise level. This curve is based on a radar system reference design which provides 1.5-dB SNR from a 1 m^2 target at a 30-nmi range. In accordance with this design point, the 1 m^2

line in Figure 3-20 is 1.5-dB above to "σ_n" line at 30 nmi. Having obtained one point on the "σ_n" line, the line is drawn to compensate for a fourth power fall off of signal power with range as per the radar range equation.

The "σ_n" line provides a means of determining clutter and signal levels relative to noise. The amount by which an RCS exceeds the "σ_n" line gives the SNR or clutter-to-noise (CNR) directly. For example, the largest separation between the 84th percentile ground clutter line and the "σ_n" line is seen to occur at minimum range. The minimum range shown corresponds to a 128-μs pulsed radar. At this range of 19.2 km the CNR is:

$$(CNR)_{max} = 50.75 \text{ dB, due to 84th percentile ground clutter at minimum range} \quad (3\text{-}7)$$

(2) Grazing Angle and Off-Boresight Attenuation Effects

Ground clutter return is affected by the grazing angle, Ψ The return from the illuminated segment, "ΔA" will be decreased in proportion to the projection of "ΔA" in the direction of the radar. This term, designated as G_g in Equation (3-4) is given as:

$$G_g = \sin \Psi \quad (3\text{-}8)$$

where Ψ is a function of radar height, h, and range, R. The equation for sin Ψ is:

$$\sin \Psi = -\cos\left(\Psi + \frac{\pi}{2}\right) = \frac{(R_e + h)^2 - R^2 - R_e^2}{2R\,R_e} = \frac{R_h^2 - R^2}{2R\,R_e} \quad (3\text{-}9)$$

where R_h is the range to the horizon as given by Equation (3-5) and R_e is the effective earth radius.

The "sin Ψ" is plotted in Figure 3-21 as a function of radar range, R, for radar heights of 2000 and 4500 ft. Note that attenuation of 10 to 30 dB can be expected from this grazing angle effect on ground plane clutter return.

The second attenuation factor affecting the clutter return is the product of the radar transmit and receive gains in the direction of the clutter segment. This gain is dependent on the depression angle, δ,, and is given as:

$$\delta = E_h - \theta \quad (3\text{-}10)$$

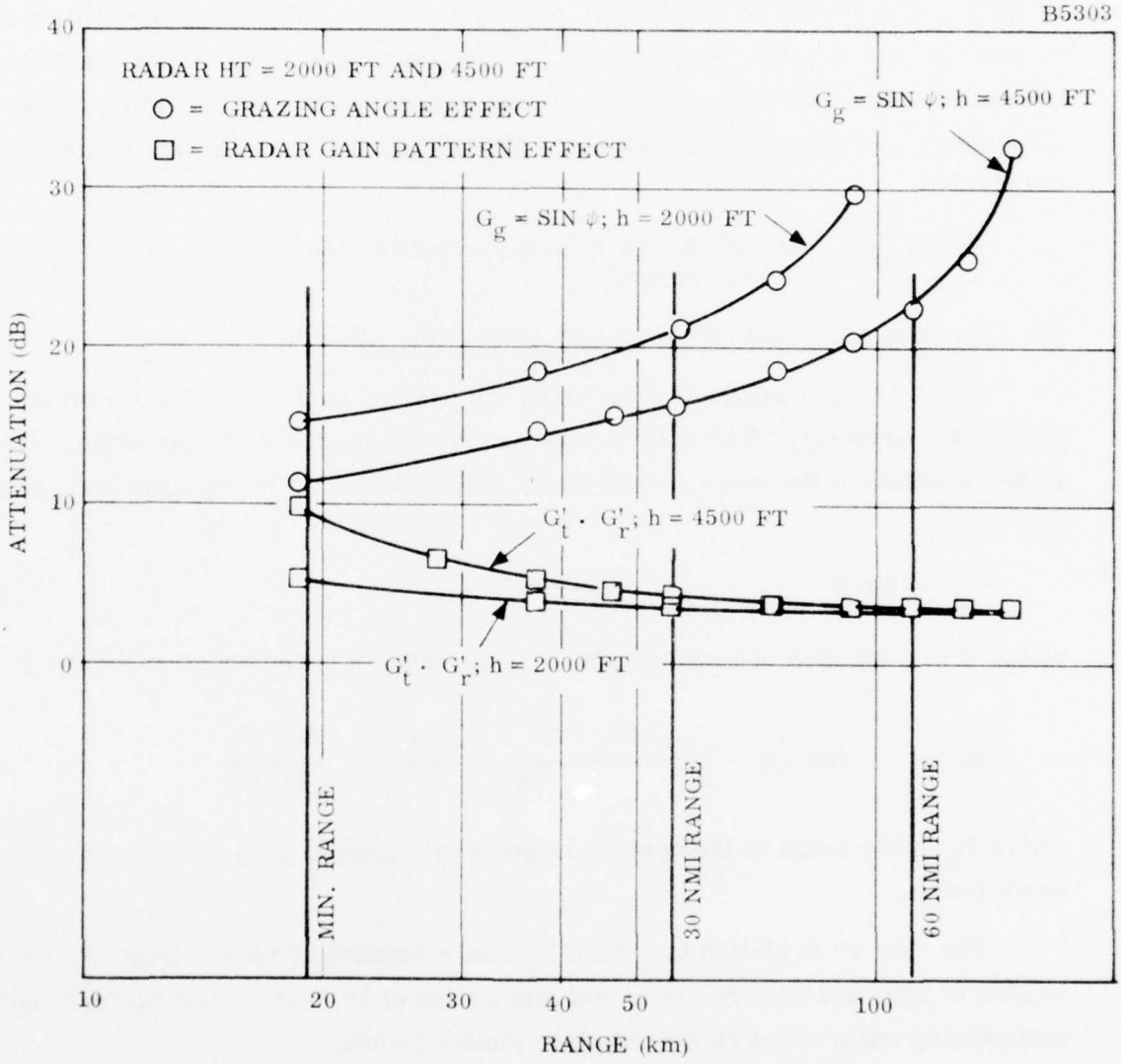


Figure 3-21. Clutter Attenuation Factors

where E_h is the elevation angle from the radar to the horizon, given by:

$$E_h = \sin^{-1} \frac{R_e}{R_e + h} = \begin{cases} 88.97°; \text{ for } h = 4500 \text{ ft} \\ 89.31°; \text{ for } h = 2000 \text{ ft} \end{cases} \quad (3\text{-}11)$$

and

$$\theta = \sin^{-1} \frac{R_e \sin(\Psi + \pi/2)}{R_e + h} = \sin^{-1} \frac{R_e \cos \Psi}{R_e + h} \quad (3\text{-}12)$$

The gain of the radar is determined assuming the beam shape shown in Figure 3-22. That is, a $\frac{\sin X}{X}$ pattern with a peak to null width of 15° is assumed up to an elevation angle of E_{max}, after which the gain falls off in $\csc^2$. For a worst case ground clutter condition, it is assumed that the radar beam is depressed so that the maximum gain angle, E_{max}, is placed 5° above the horizon. With this assumption, the product of transmit and receive gain in the direction of the ground clutter relative to peak gain is:

$$G'_t \cdot G'_r = \left(\frac{\sin X\pi}{X\pi} \right)^4 \quad (3\text{-}13)$$

where

$$X = \frac{5° + \hat{o} \text{ (deg)}}{15°}$$

A plot of $G'_t \cdot G'_r$ is shown in Figure 3-21. From 3 to 10 dB of clutter attenuation is seen to accrue from this factor.

(3) Weather Clutter

Weather clutter arises from the reflection of radar energy from rain droplets. These droplets tend to move horizontally with the local winds causing a Doppler effect. Because the winds vary with altitude, a radar beam may encompass low velocity droplets at the low end of the beam and high velocity droplets at the other end. A resulting Doppler spread and mean Doppler shift will occur from the accumulation of clutter over the entire beam.

A computer program was written to determine the clutter contained in a radar resolution cell. The radar cell is an elliptical beam in azimuth and elevation, which has a major axis of 1.5° in azimuth, corresponding to the two-way radar beamwidth and 70° in elevation. The elevation direction is weighted according to the pattern given

in Figure 3-22. The radar cell width in range was taken as 600 m, corresponding to a radar bandwidth of 250 kHz. The computer program was run for various elevation pointing angles, given by the elevation angle of E_{max}, where E_{max} as shown in Figure 3-22 is the angle at which maximum gain is achieved. Clutter is assumed to be uniform in density from sea level to 30-kft altitude, and have a reflectivity of 1.5×10^{-9} m^2/m^3 which corresponds to a rainfall rate of 15 mm/h.* Winds are assumed to vary uniformly from 0 to 80 knots over this 30-kft altitude band, and are directed horizontally. The radar azimuth is assumed to be pointing into the wind to give worst-case Doppler conditions.

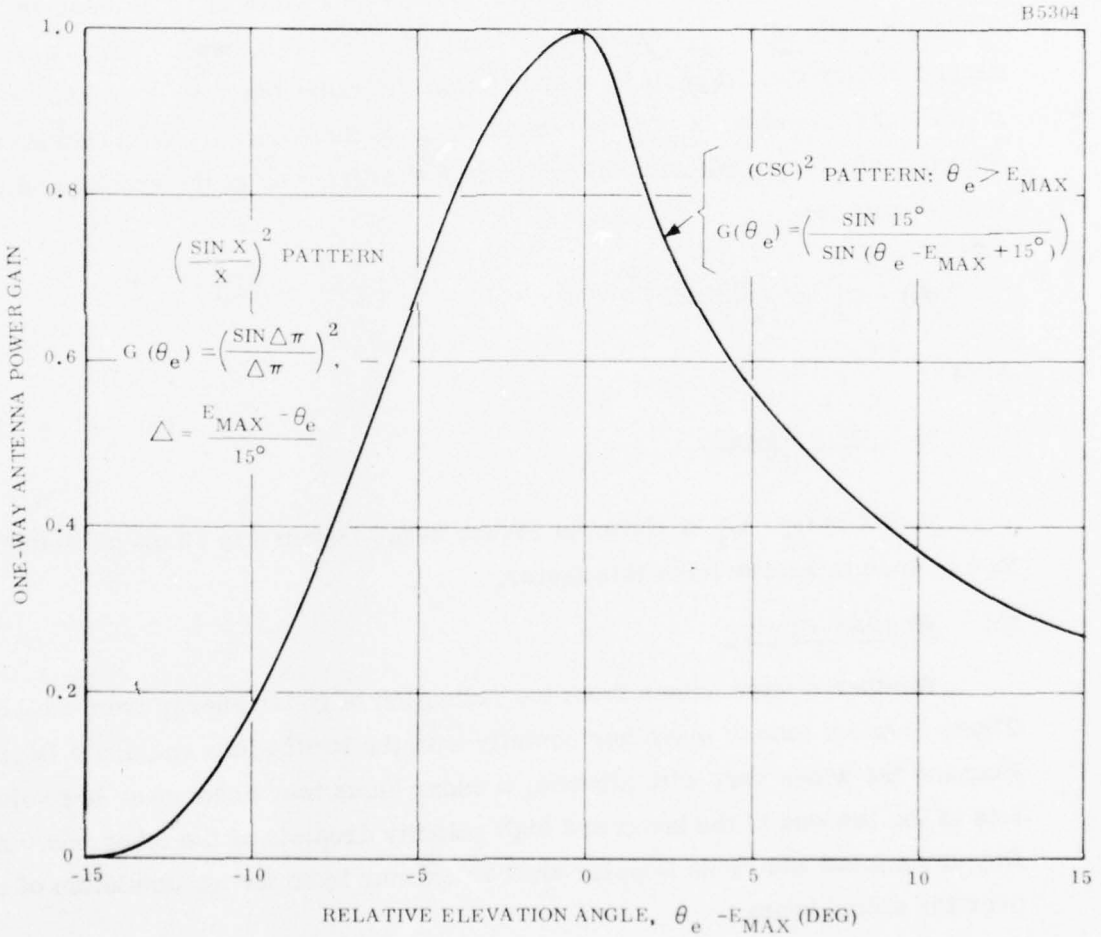


Figure 3-22. Ideal csc^2 Radar Elevation Pattern

*Radar Equations for Jamming and Clutter, D.K. Barton, IEEE Transaction on Aerospace and Electronic Systems, Vol. AES-3, No. 6, November 1967.

The results of this analysis provide clutter RCS, clutter mean velocity and clutter velocity spread as a function of range. These three results are given in Figures 3-23 through 3-25 for a radar at sea level and Figures 3-26 through 3-28 for a radar at 4500-ft altitude. For each set of results, the radar elevation pointing angle is given as a parameter.

Figures 3-23 through 3-26 show the amount of clutter increases with range as is expected since the azimuth and elevation cells each increase directly with range. However, beyond a certain point, the clutter starts falling off with range. This occurs since the clutter ceiling (30 kft) is reached by the radar cell.

Figures 3-25 and 3-28 show that the clutter spread is less than 10 m/s which might suggest that a 10 m/s velocity-matched filter could remove this clutter. This, however, is not true since the mean velocity given in Figures 3-24 and 3-27 shows a variation with range of from 0 to 40 m/s requiring the notched filter to either vary adaptively with range or else be wide enough to contain both the mean and the spread of the clutter.

The clutter RCS given in Figure 3-26 for the worst case condition; i.e., the lowest elevation pointing angle of the radar, is redrawn on Figure 3-20 so that the weather clutter can be conveniently compared to the ground clutter.

(4) Sea Clutter RCS

Sea clutter RCS is given by Equation (3-4) which was used to define ground clutter. Again, for determining worst conditions, the attenuation factors G_t and G_r will be omitted; i.e., set to unity. The reflectivity of sea clutter is a function of sea state. Reflectivity for sea state 4 is specified as -50 dB or less for grazing angles of 3° or less. This reflectivity already includes the previously described grazing angle effect term, G_g. The 3° limit covers the expected variation of grazing angles even for the worst case condition of a radar at 4500-ft altitude observing sea clutter at minimum range.

Since the same equation governs both sea and ground clutter, the sea clutter follows the same curve as the median ground clutter shown in Figure 3-20. Sea clutter is shown 16 dB below the median ground clutter because of its reduced reflectivity. The sea clutter RCS happened to coincide, within 1 dB, with the already drawn weather clutter curve and is, therefore, represented by a common curve.

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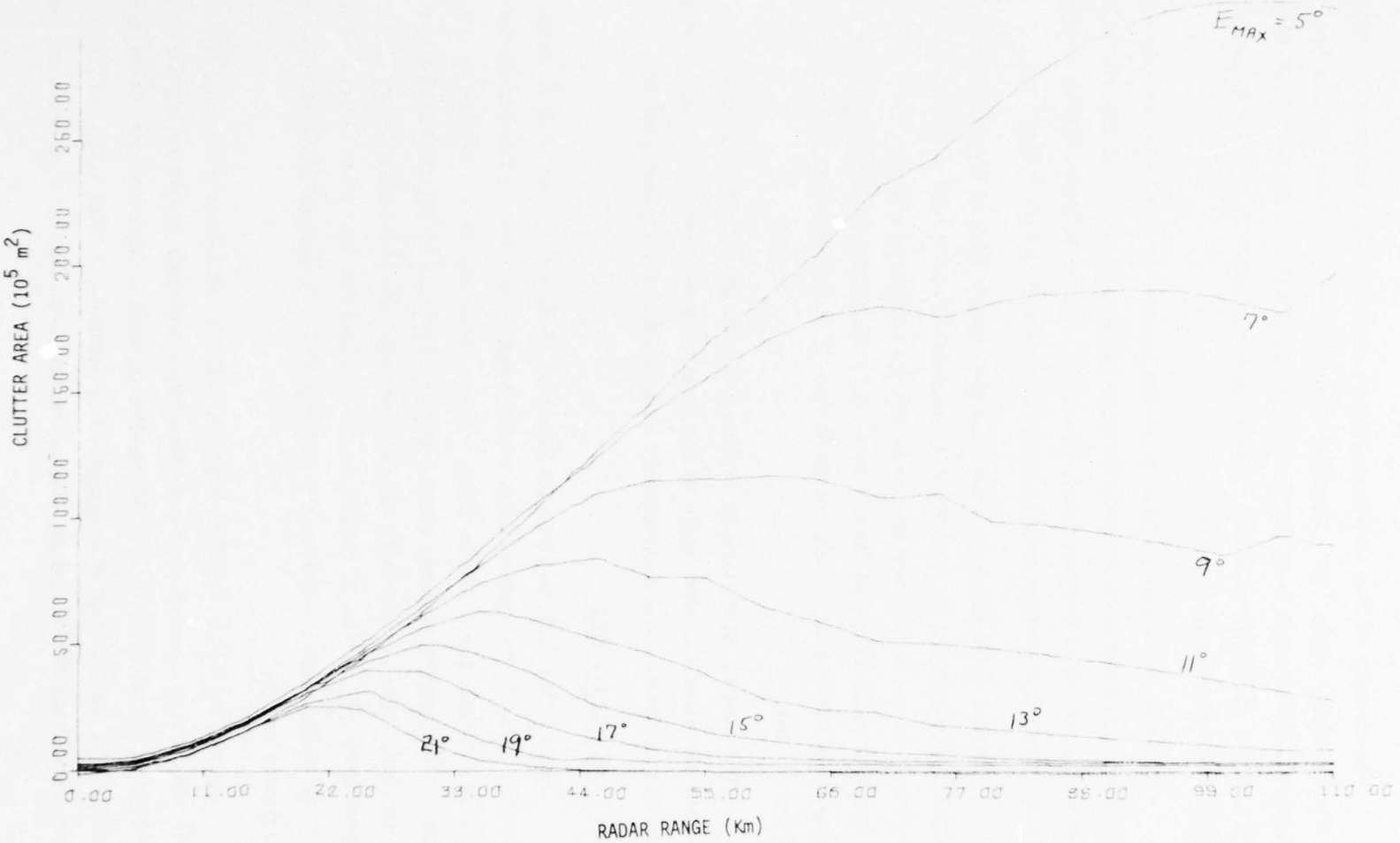
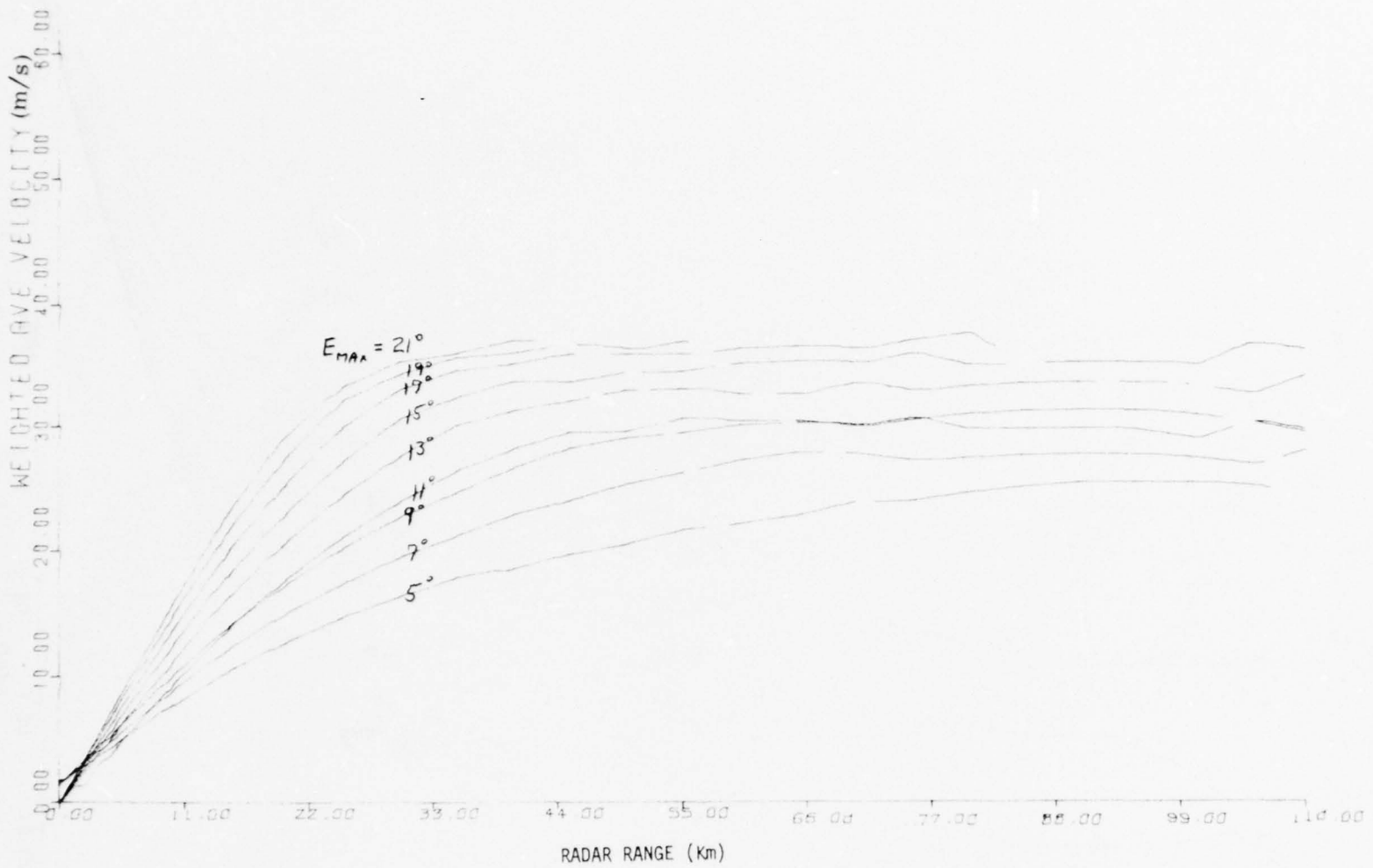


Figure 3-23. Weather Clutter Beam Filled Area* (Zero Radar Height)

*To convert to clutter RCS, multiply by range resolution (m) and by the weather reflectivity.



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Figure 3-24. Mean Clutter Velocity (Zero Radar Height)

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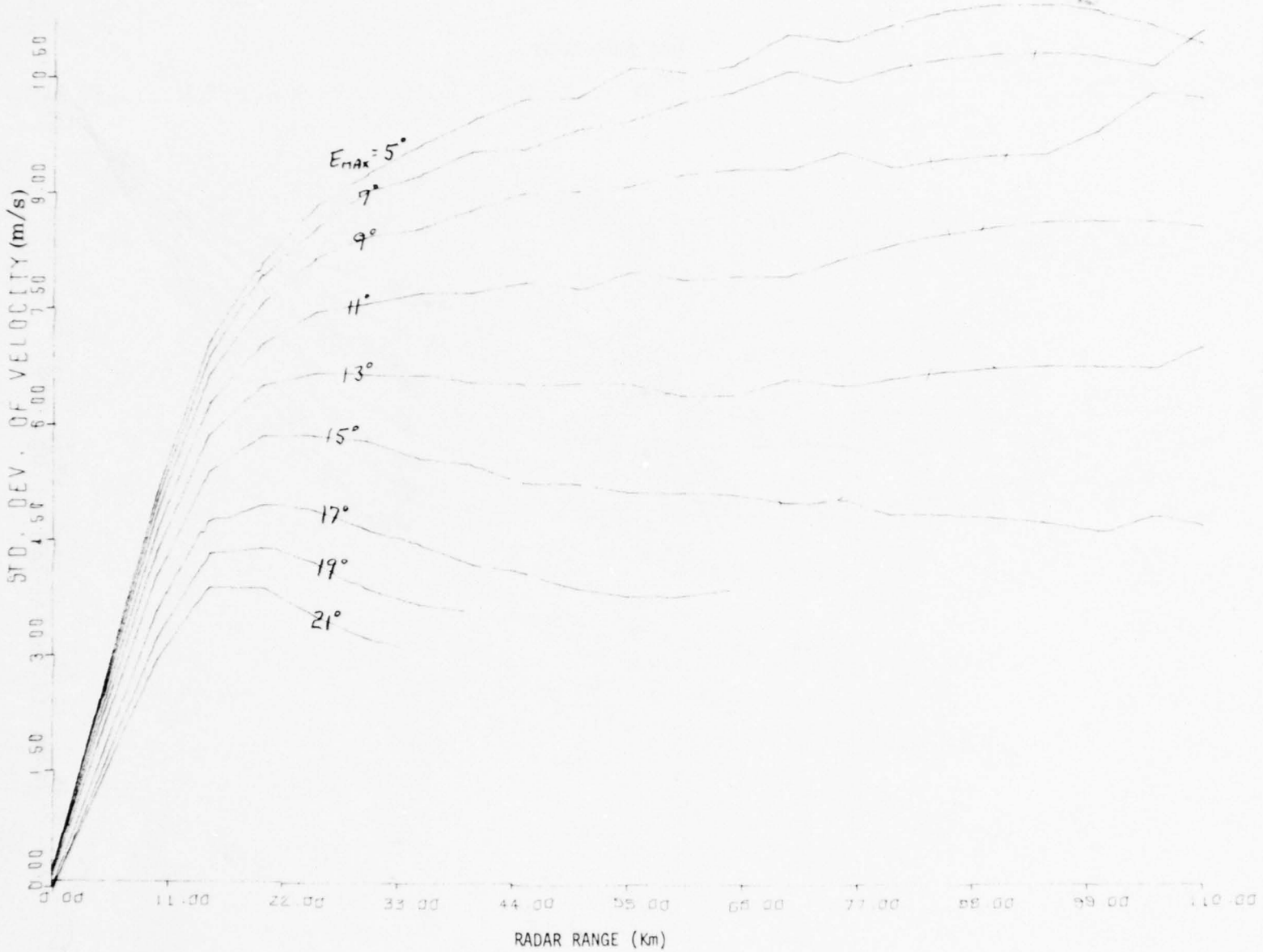


Figure 3-25. Clutter Velocity Spread (Zero Radar Height)

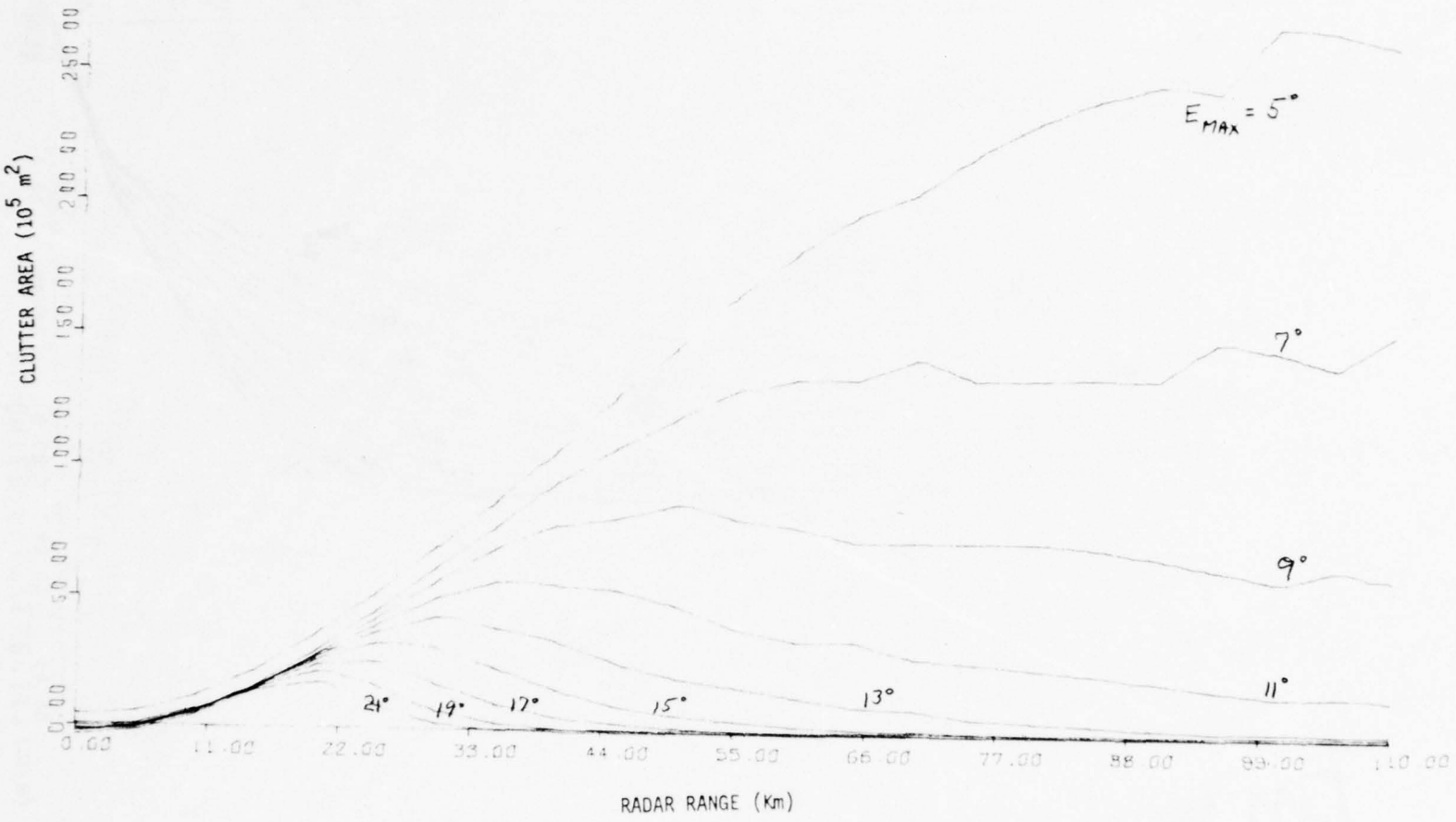


Figure 3-26. Weather Clutter Beam Filled Area* (4500 Ft Radar Height)

*To convert to clutter RCS, multiply by range resolution (m) and by the weather reflectivity.

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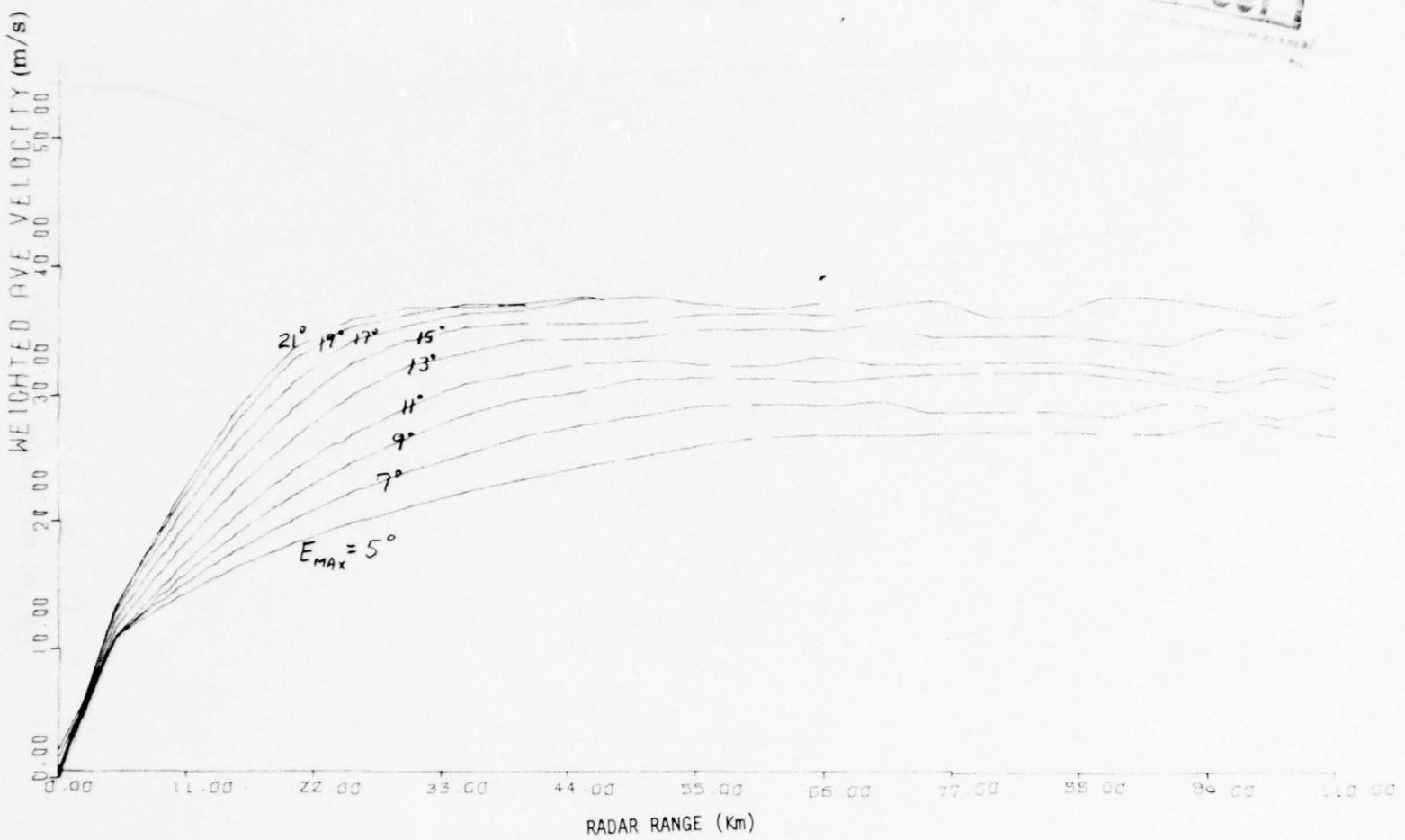


Figure 3-27. Mean Clutter Velocity (4500 Ft Radar Height)

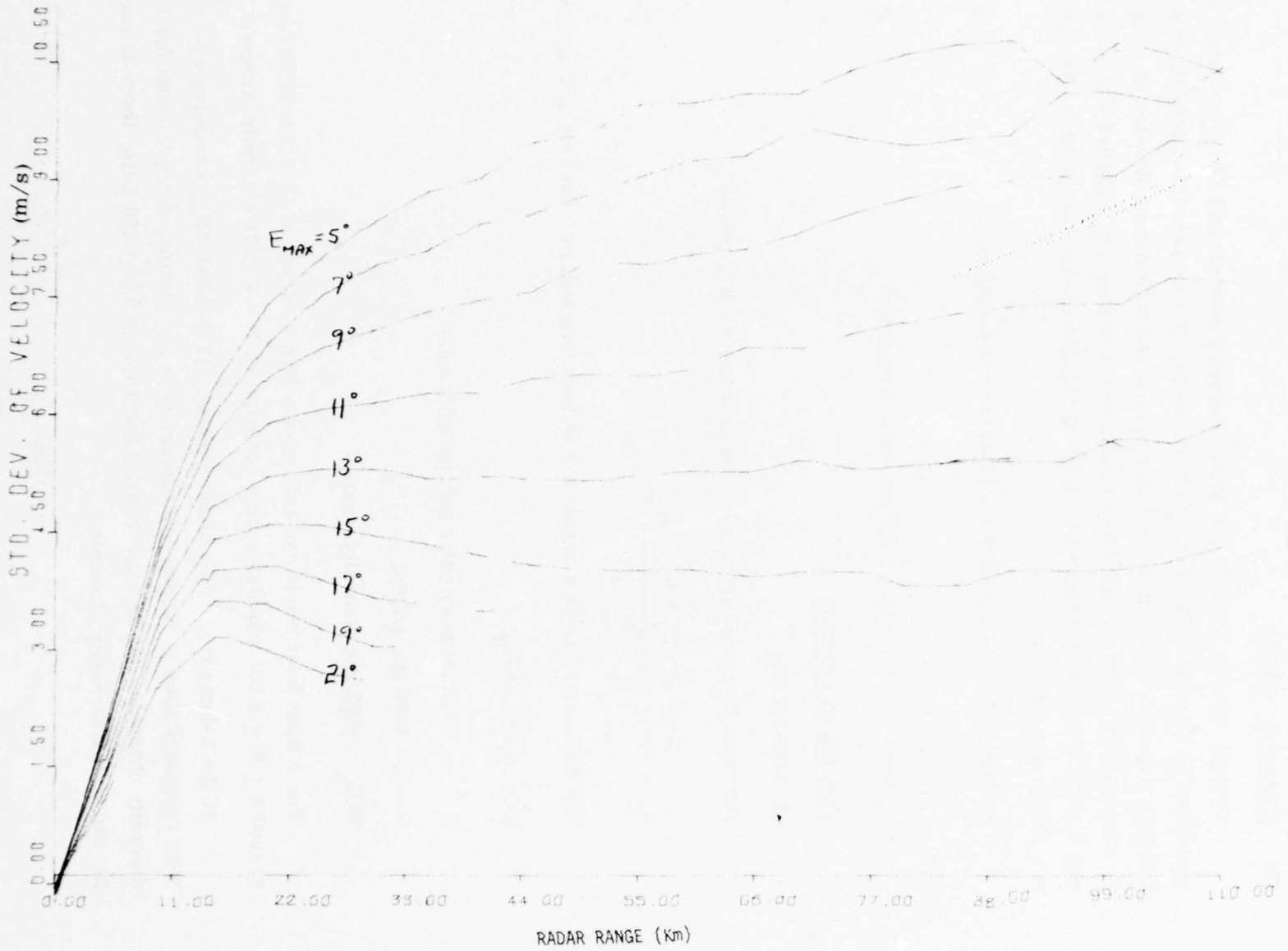


Figure 3-28. Clutter Velocity Spread (4500 Ft Radar Height)

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(5) Clutter Spectrum

Typical velocity profiles for weather clutter have already been discussed and presented in Figures 3-24, 3-25, 3-27 and 3-28. It was seen that the weather clutter had both a mean component as well as a spread and both were a function of range. Ground and sea clutter on the other hand tend not to have any significant mean velocity and a much lower velocity spread. Typical velocity spread are given for ground and sea clutter returns as:

$$\sigma_v \text{ (ground)} = 0.3 \text{ m/s; for a 40-knot wind condition} \tag{3-14}$$

and

$$\sigma_v \text{ (sea)} = 0.6 \text{ m/s; for sea state 4 condition} \tag{3-15}$$

2. SYSTEM SYNTHESIS

a. SENSOR SIZING

The peak RF power required of the transmitter is given by

$$P_p = \frac{(4\pi)^3 f^2 k T_s L R^4 SNR}{\sigma \tau G_T G_R} \tag{3-16}$$

The SNR per pulse is a factor of N/K less than that per diversity group, i.e.,

$$SNR = \frac{K}{N} SNR_K \tag{3-17}$$

K = no. diversity pulse groups (channels)

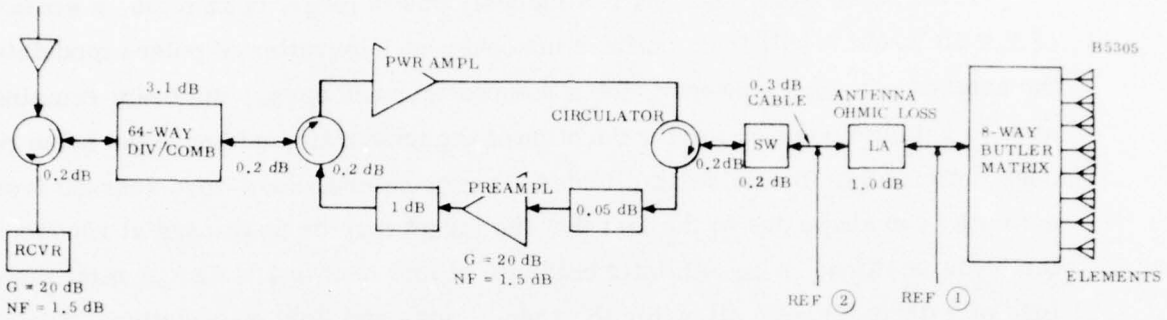
N = total no. pulses

SNR_K = SNR per diversity group

For a fixed total number of pulses, the SNR in Equation (3-17) is minimum around $4 \leq K \leq 8$ but remains nearly constant for K = 4 to 16 diversity channels.

At the L-band radar allocation frequency 1215-1400 MHz, assuming 20- to 50-MHz frequency span is required for diversity decorrelation, there is room for 4 to 9 diversity channels. At the UHF radar allocation band 420-450 MHz, there is room for one or two diversity channels.

Using the matrix-switched transmitter/receiver candidate configuration to be discussed in a subsequent section, and illustrated conceptually below (Figure 3-29) with estimated losses, the system noise temperature is calculated as follows:



Receive Loss: $L_R = 1.75$ dB

$$T_{S_1} = T_a + (L_R - 1)\, T_R + T_e\, L_R$$

T_a = ambient sky noise
= $0.876\, T'_a + 36°$ where T'_a is given in Figure 11 of L. V. Blake NRL Report 6930 "Guide to Pulse Radar Maximum Range Calculation".

L-Band (1300 MHz)	UHF (435 MHz)
$T'_a = 90°$	$T'_a = 130°$
0° Elevation	0° Elevation
$T_a = 114.84°$	$T_a = 149.88°$

T_R = ambient temperature of receiver losses
= 290°

Receiver Temperature Calculation: (T_e)

Device	Gain (dB)	Cumulative Gain (dB)	Unit Temp (Deg)	Contribution (Deg)	Cumulative Temp (Deg)
Preamp	20	20	119.64	119.64	119.64
Loss	-4.7	15.3	565.85	5.66	125.3
Receiver	20	35.3	119.64	3.53	128.83=T_e

L-Band $T_{S_1} = 114.84° + 143.91° + 193.25° = 452°$ $\left(T_{S_2} = \dfrac{T_{S_1}}{L_A} = 358.76°\right)$

UHF $T_{S_1} = 149.88 + 143.91 + 193.25 = 487°$ $\left(T_{S_2} = \dfrac{T_{S_1}}{L_A} = 387°\right)$

Figure 3-29. Matrix-Switched Transmitter/Receiver Candidate Concept

Transmit losses estimated for the matrix switched candidate transmitter are 1.7 dB. Signal processing losses, encountered in Doppler processing 4 diversity groups of 8 pulses each, total 4.32 dB for the "aligned Doppler" in which interpulse period is staggered to just compensate the frequency diversity stagger.

If the beam were scanning continuously past a target in azimuth, a scanning loss of 1.6 dB would result from uniform noncoherent integration of pulses modulated by the antenna pattern. However, for a stepped-scanned array, the beam remains fixed at each azimuth position for the duration of the pulse train and hence the beam pattern does not modulate the pulse amplitudes. Nevertheless, some loss accrues from the azimuth beamshape due to the fact that the target may be positioned at random within the beam position. A pessimistic estimate of this loss is 1.6 dB. A miscellaneous loss of 1 dB is taken to allow for the radome loss and field degradation. The atmospheric loss at 0° elevation angle and 30 nmi at L-band is 0.65 dB. At 60 nmi, it is 1.25 dB. For UHF it is 0.3 dB and 0.6 dB, respectively.

Table 3-3 is a Blake Radar Calculation Work Sheet summarizing designs for a 3° L-band radar taking into account the foregoing factors. The peak RF power required to get 60 nmi on a 16 m^2 RCS target is slightly higher than that required for 30 nmi on a 1 m^2 RCS target because of the 0.6-dB more atmospheric loss at the long range. The long range power required is 912 W. Note that this calculation is based on a one-out-of-four detection criterion. Because the antenna gains vary inversely with azimuth beamwidths and the number of pulses varies directly with beamwidth, the net variation of peak power required with beamwidth and frequency is approximately:

$$P_p = 912 \cdot \left(\frac{f_{MHz}}{1300}\right)^2 \frac{(\theta^\circ AZ)}{3.0} \cdot \frac{K\ SNR_k}{4\ SNR_4} \cdot \frac{T_S}{359^\circ} \cdot \frac{L_{atm}}{1.33} \qquad (3\text{-}18)$$

At an operating frequency of 1300 MHz, the peak power is

$$P_p = 912\ \frac{\theta AZ}{3.0} \qquad \text{L-Band} \qquad (3\text{-}19)$$

To make up 10-nmi difference in multipath performance requires an additional 7 dB for the UHF system. Taking this and the frequency difference into account, the required peak RF power at UHF is still less than at L-band for the same beamwidth.

$$P_p = 650\ \frac{\theta AZ}{3.0} \qquad \text{UHF} \qquad (3\text{-}20/3\text{-}21)$$

However, the size and cost of the UHF antenna to produce a 3° azimuth beam or narrower, coupled with less diversity availability and the need for separate IFF makes UHF a less attractive operating frequency choice than L-band.

TABLE 3-3

PULSE-RADAR RANGE-CALCULATION WORK SHEET *

Based on Eq. (13)

1. Compute the system input noise temperature T_s, following the outline in section A below.
2. Enter range factors known in other than decibel form in section B below, for reference.
3. Enter logarithmic and decibel values in section C below, positive values in the plus column and negative values in the minus column. For example, if $V_{0\,(dB)}$ as given by Figs. 4 through 9 is negative, then $-V_{0\,(dB)}$ is positive and goes in the plus column. For C_B, see Figs. 1 through 3. For definitions of the range factors, see Eq. (13).

Radar antenna height: h = ft. Target elevation angle: θ = °. (See Fig. 13.)

A. Computation of T_s:

$T_s = T_a + T_r + L_r T_e$

(a) Compute T_a.
For $T_{t_\theta} = T_{t_\phi} = 290$ and $T_g = 36$ use Eq. (37a).
Read T'_a from Fig. 11.
$L_{a\,(dB)}$: 1.0 L_a: 1.26
$T_a = (0.876\,T'_a - 254)/L_a + 290$
T'_a = 90° T_a = 150.98 °K

(b) Compute T_r using Eq. (40).
For T_{t_r} = 290 use Table 1.
$L_{r\,(dB)}$: .75 T_r = 54.67 °K

(c) Compute T_e using Eq. (41) or using Table 1.
$F_{n\,(dB)}$: 1.6 T_e: 128.83 °K
L_r: 1.19 $L_r T_e$ = 153.31 °K

Add. T_s = 358.76 °K

B. Range Factors		C. Decibel Values	Plus (+)	Minus (-)
$P_{t\,(kW)}$	0.912 kW	10 log $P_{t\,(kW)}$	-0 . 40	.
$\tau_{\mu sec}$	128 μs	10 log $\tau_{\mu sec}$	21 . 07	.
G_t	25.55	$G_{t\,(dB)}$	25 . 55	.
G_r	24.55	$G_{r\,(dB)}$	24 . 55	.
$\sigma_{(sq\,m)}$	16 m^2	10 log σ	12 . 04	.
f_{MHz}	1300	-20 log f_{MHz}	.	62 . 28
T_s (°K)	358.76°	-10 log T_s	.	25 . 55
V_0		$-V_{0\,(dB)}$	.	-1 . 6
C_B		$-C_{B\,(dB)}$		4 . 32
L_t		$-L_{t\,(dB)}$		1 . 7
L_p		$-L_{p\,(dB)}$		1 . 6
L_x		$-L_{x\,(dB)}$		1 . 0
Range-equation constant (40 log 1.292)			4.45	
4. Obtain the column totals →			87 . 26	94 . 85
5. Enter the smaller total below the larger →			.	87 . 26
6. Subtract to obtain the net decibels (dB) →			+ .	- 7.59

7. In Table 2 find the range ratio corresponding to this net decibel (dB) value, taking its sign (±) into account. Multiply this ratio by 100. This is R_0 → 64.6 nmi
8. Multiply R_0 by the pattern-propagation factor F = (see Eqs. (42) through (65) and Figs. 12 through 19):
$R_0 \times F = R'$ → 64.6 nmi
9. On the appropriate curve of Figs. 21 and 22 determine the atmospheric-absorption loss factor, $L_{a\,(dB)}$, corresponding to R'. This is $L_{a\,(dB)(1)}$. → 1.25 dB
10. Find the range factor δ_1 corresponding to $-L_{a\,(dB)(1)}$ from the formula δ = antilog $(-L_{a\,(dB)}/40)$ or by using Table 2. → 0.93
11. Multiply R' by δ_1. This is a first approximation of the range R_1. → 60.08 nmi
12. If R_1 differs appreciably from R', on the appropriate curve of Figs. 21 and 22, find the new value of $L_{a\,(dB)}$ corresponding to R_1. This is $L_{a\,(dB)(2)}$. →
13. Find the range-increase factor (Table 2) corresponding to the difference between $L_{a\,(dB)(1)}$ and $L_{a\,(dB)(2)}$. This is δ_2. →
14. Multiply R_1 by δ_2. This is the radar range in nautical miles, R. →

Note: If the difference between $L_{a\,(dB)(1)}$ and $L_{a\,(dB)(2)}$ is less than 0.1 dB, R_1 may be taken as the final range value, and steps 12 through 14 may be omitted. If $L_{a\,(dB)(1)}$ is less than 0.1 dB, R' may be taken as the final range value, and steps 9 through 14 may be omitted. (For radar frequencies up to 10,000 megahertz, correction of the atmospheric attenuation beyond the $L_{a\,(dB)(2)}$ value would amount to less than 0.1 dB.)

* 3° SYST
32 PULSES
(8 COHERENT, 4 DIVERSITY)

$P_d = 0.54$ $P_f = 0.25 \times 10^{-6}$
4-s FRAME FOR 360°

Figure 3-30, 3-31, and 3-32 show the approximate variation in peak, average, and prime powers required of the type A radar with beamwidth and frequency at a fixed 4-s frame time.

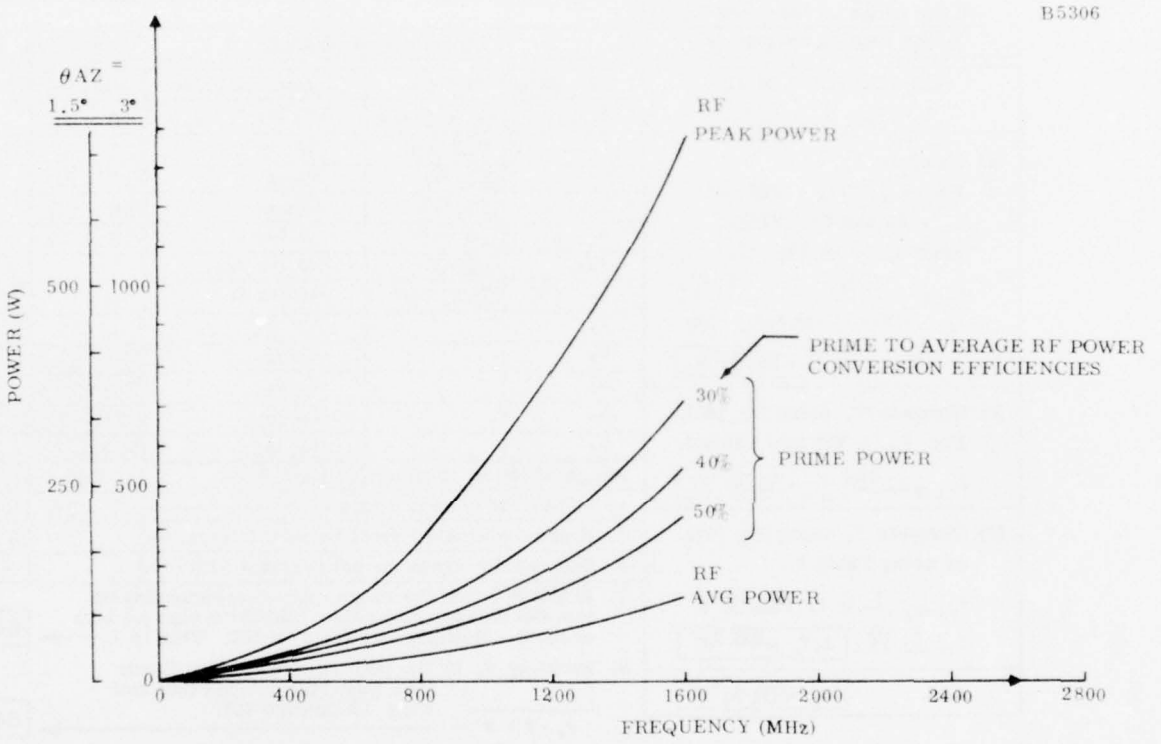


Figure 3-30. RF Power Variation With Frequency

These represent the prime power required of the final RF power amplifier, and must be combined with the prime power required of the other antenna and RF components to get the total shown in the first row of Table 3-4.

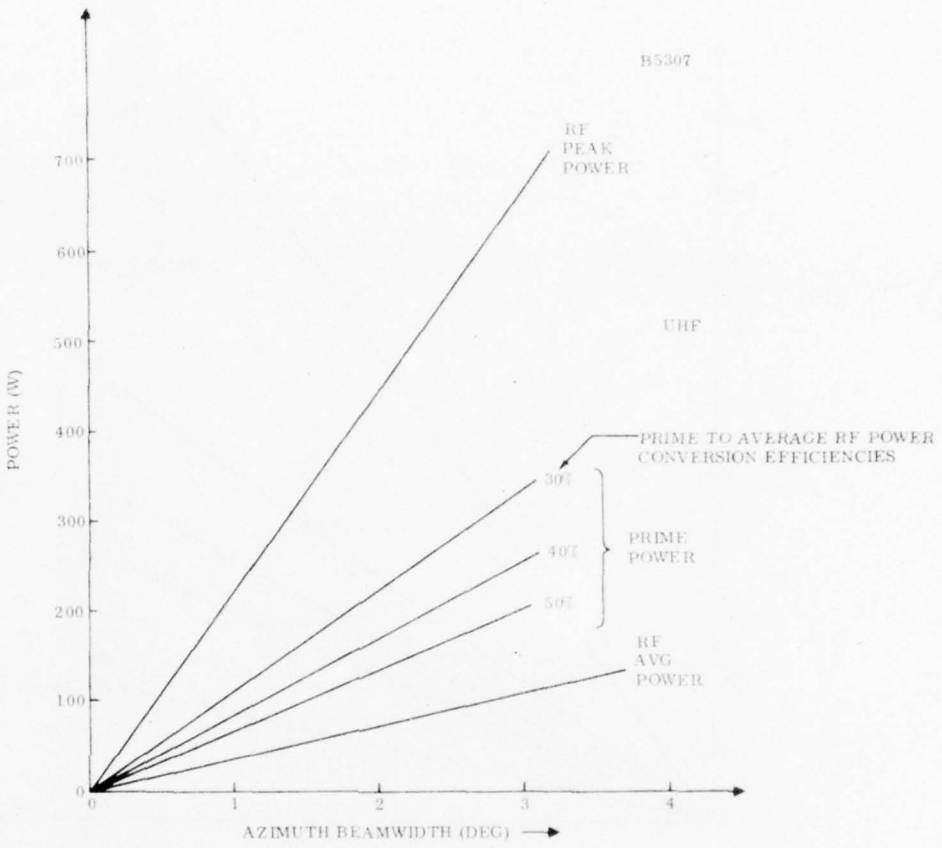


Figure 3-31. UHF RF Power Variation With Beamwidth

The range of total system prime power spans roughly 400 W to 1000 W over all viable design candidates. The primary design approaches include the matrix-steered array combined with an in-hand digital signal processor. The alternates which are attractive from a low prime power standpoint include replacing the Butler matrix column feed with a simple horn radiator . (This sacrifices the growth to 3-D operation); considering a low-inertia organ-pipe scanner rather than the electronically-steered matrix approach; and using a Charge-Coupled Device (CCD) Signal Processor rather than the Complementary Metal Oxide Semiconductor (CMOS) Digital Processor. The total prime power is summarized in Table 3-4. These estimates result from analysis of the conversion efficiencies of each transmitter design option.

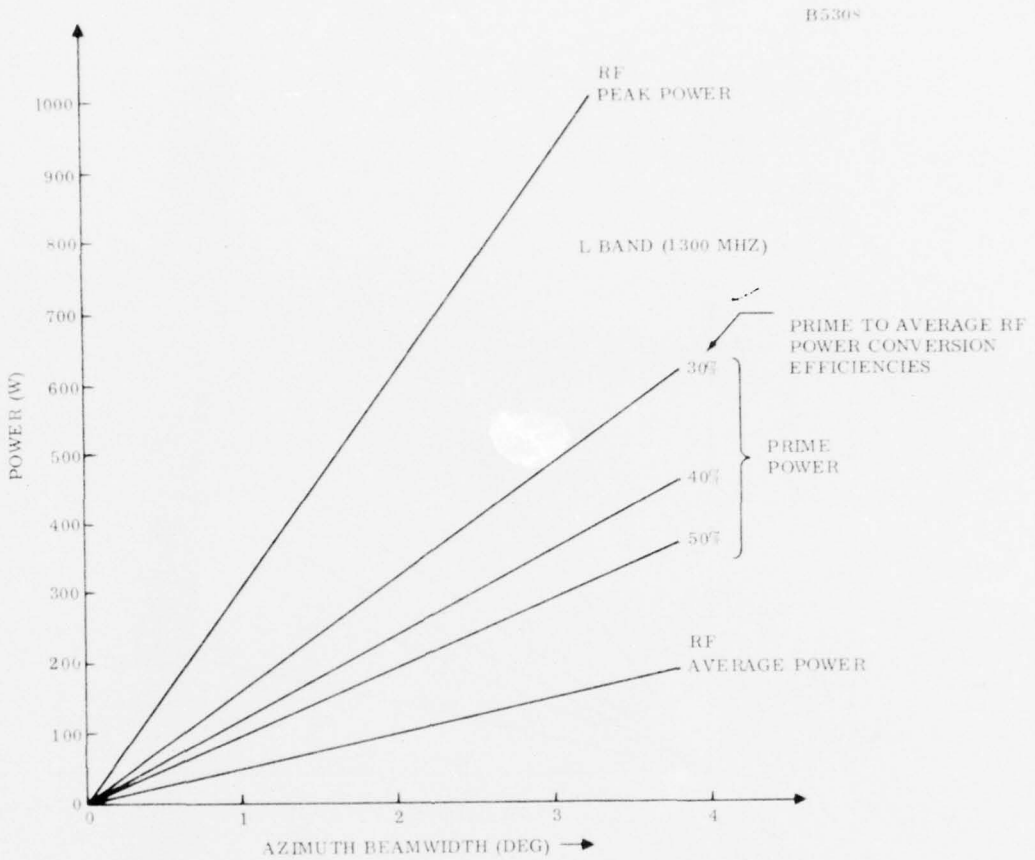


Figure 3-32. L-Band RF Power Variation With Beamwidth

TABLE 3-4. PRIME POWER REQUIREMENTS SUMMARY

	Lowest (1.5°)	Highest (3.0°)	Preferred* (3.0°)
Antenna and RF	180	1100	740
Receiver and Exciter/Waveform Generator	30	30	30
Signal Processor	25	130	25
Data Processor	180	180	180
	415 W	1440 W	975 W

*Simple Radiator and CCD Signal Processor

b. WAVEFORM AND SIGNAL PROCESSING SIZING

(1) Waveform Design

The primary requirements of the radar are that it shall detect a 16 m^2 target at 60 nmi, or correspondingly a 1 m^2 target at 30 nmi with a probability of 0.95 within 4 scans. A design configuration has been developed to achieve this goal with minimum radar power while operating in an environment of ground, sea and weather clutter.

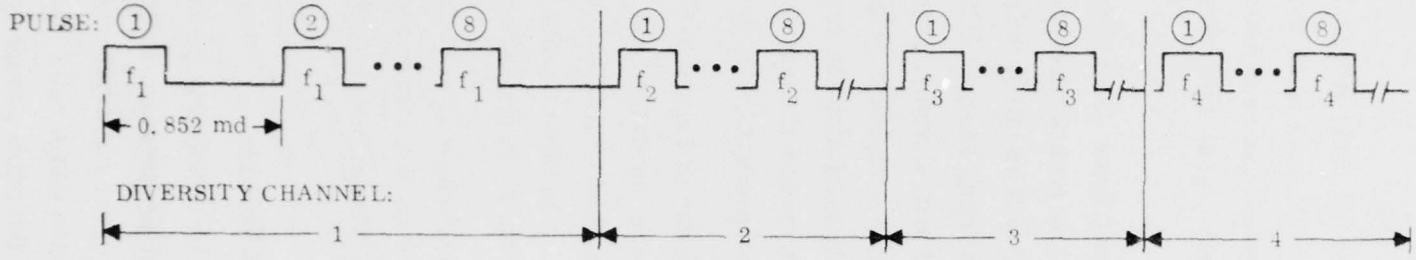
The radar will be step-scanned from one-azimuth beam position to the next. In each azimuth dwell, 32 pulses will be transmitted and processed in four groups of 8 coherent pulses each. Each group will be offset in frequency by 50 MHz to provide independent observations of the Swerling I target RCS. This frequency diversity changes the target to a Swerling II and, thereby, improves the probability of detection by a considerable amount over a completely coherent combination of the 32 pulses. The four diversity channels roughly minimize the required signal-to-interference ratio (SIR); more channels would increase the noncoherent integration loss so that it exceeds the gain achieved from independent looks at the target.

The selected waveform is shown in Figure 3-33. Each pulse is LFM (Linear Frequency Modulated) with a 250-kHz bandwidth and a 128-μs duration. Four μs (0.32 nmi) range resolution is achieved with this bandwidth waveform which exceeds the 0.5-nmi resolution specified. A minimum pulse separation of 0.868 ms provides an unambiguous range of 60 nmi with a 128-μs transmit pulse time.

Fifty-MHz frequency separation between the diversity channels shown in Figure 3-33 provides independent samples from a target composed of reflecting highlights spaced 3 m or more apart. Tactical aircraft typically have such spacing between highlights.

(2) Aligned Doppler Processing System

Each group of 8 pulses will be coherently processed by an 8-pulse parallel Fast Fourier Transform (FFT) Doppler processor. Eight Doppler filter outputs are obtained from this processor for every eight input samples, obtained from each of the eight transmissions at a common range cell. Doppler processed outputs are saved and noncoherently combined over the pulse groups for each separate range and Doppler cell.



PULSE: 128 μs DURATION
LFM CODED
250 kHz BANDWIDTH - 4 μs OR 0.32 nmi RESOLUTION
TIME - BANDWIDTH PRODUCT OF 32

PULSE SPACING: 0.852 ms NOMINAL

FREQUENCY SEPARATION: 50 MHz - 1-1/2 TO 3 m MIN. TARGET HIGHLIGHT SPACING

Figure 3-33. Candidate Waveform

Changing carrier frequency after each eight pulse transmission would normally cause a shift in target and clutter Doppler frequency. This shift makes it difficult to efficiently combine different diversity channel outputs. The Doppler shift can be effectively removed by adjusting the Pulse Repetition Period (PRP), in each group to just compensate for the carrier change. By keeping

$$f_i T_i = \text{CONSTANT} \tag{3-22}$$

where

f_i = Carrier frequency of i^{th} diversity channel transmission

T_i = Time between pulse transmissions of i^{th} diversity channel transmission

over the four diversity channel transmissions, targets and clutter will remain in the same Doppler channel. Choosing frequency and pulse period according to Equation (3-22) provides what will be referred to herein as the aligned Doppler system.

Noncoherent integration can be carried out between frequency diversity transmissions in the aligned Doppler system because targets remain in the same Doppler channel or filter. A typical set of frequency and pulse periods is given in Table 3-5.

TABLE 3-5. TYPICAL FREQUENCY AND PULSE PERIOD FOR 4-DIVERSITY CHANNEL, ALIGNED DOPPLER SYSTEM

Diversity Channel	Frequency (GHz)	Pulse Period (ms)
1	1.25	0.972
2	1.30	0.935
3	1.35	0.900
4	1.40	0.868

(3) Doppler Response/Doppler Weighting

Doppler processing of envelope-recurrent burst waveforms produce ambiguous responses in Doppler. Figure 3-34 shows the mainlobe responses of the eight Doppler filters for a pulse period of 0.868 ms which corresponds to the fourth diversity channel in Table 3-5. Filter No. 1, for example, responds to Doppler signals centered at 145 Hz as well as those frequencies offset from 145 Hz by integer multiples of 1.15 kHz, which is the reciprocal of the pulse period. While the other

diversity channels have slightly different Doppler scales for their respective Doppler filters, they all share the common velocity scale shown in Figure 3-34, when Equation (3-22) is satisfied. Also shown in Figure 3-34 is the 25 m/s range over which the average velocity of the weather clutter will vary and the 10.5 m/s velocity spread of this clutter. Clutter characteristics were used corresponding to worst case conditions, which is seen from Figure 3-26 as being an E_{max} (elevation angle at which radar gain maximum) of 5° with a radar height of 4500 ft. Comparing the clutter velocity characteristics to the filter responses in Figure 3-34 shows that the clutter center position (in velocity) can vary over three filter widths and because of its spread will be contained in two filters.

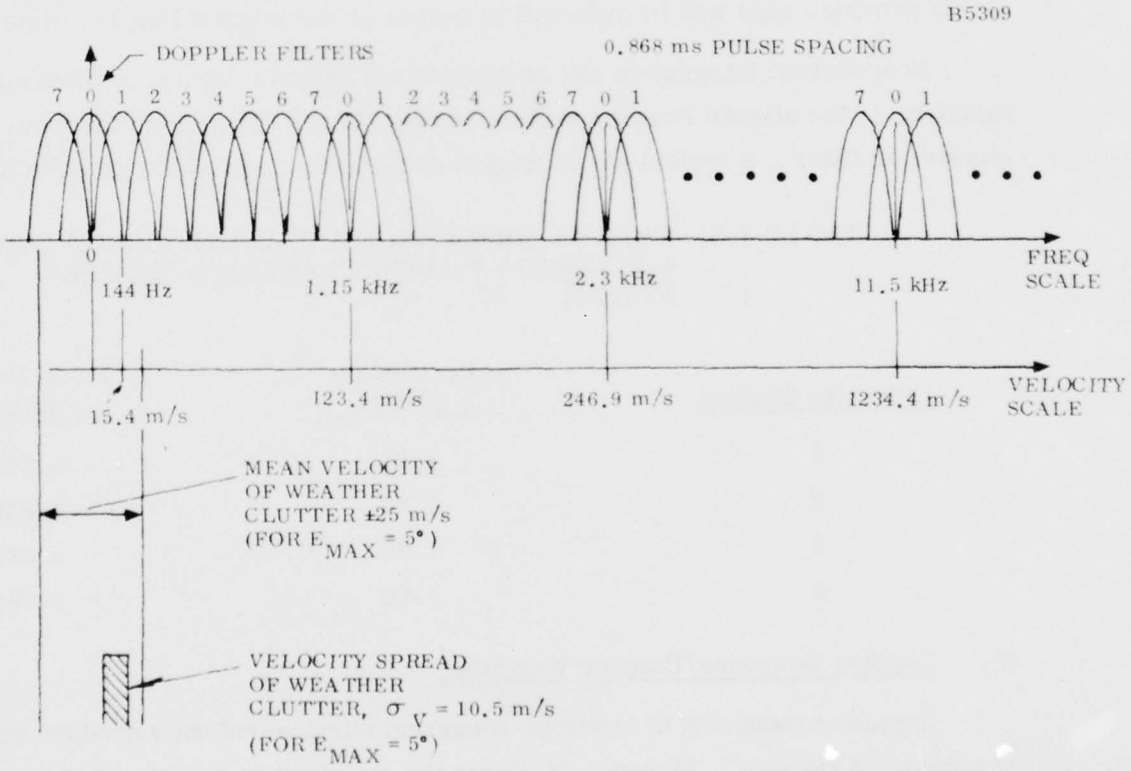


Figure 3-34. 8-Pulse Doppler Processor Response

Figure 3-35 shows a sketch of an expansion of the response of one of the Doppler filters. This filter would have a first sidelobe level of -13 dB if no weighting were employed. Sidelobes in Doppler can be very substantially reduced by a simple weighting of adjacent filters. Using the algorithm:

$$V_i' = -\frac{1}{2} V_{i-1} + V_i - \frac{1}{2} V_{i+1} \qquad (3\text{-}23)$$

where

V_i' = Weighted output of i^{th} Doppler filter

V_i = Unweighted output of i^{th} Doppler filter

V_{i-1} = Unweighted output of $(i-1)^{th}$ Doppler filter (where "i - 1" is evaluated modulo 8)

V_{i+1} = Unweighted output of $(i+1)^{th}$ Doppler filter (where "i + 1" is evaluated modulo 8)

produces a response as sketched in Figure 3-35. The negative signs in Equation (3-23) correct for the fact that there is approximately a 180° phase change in the response from adjacent filters to a sinusoidal input (more precisely the phase change is 157.5°).*

A further expansion of the Doppler responses is given in Figure 3-36. Here the weighted and unweighted filter response in the vicinity of a null are presented. As a point of reference, a single loop MTI canceller has a response which is virtually identical to that of the unweighted filter. It is seen from Figures 3-35 and 3-36 that weighting the filter reduced its sidelobes by some 15 dB or more and furthermore improved the rejection in the null region by some 10 dB. It will be shown that this latter effect greatly improves the radar rejection of ground clutter and reduces its sensitivity to Stabilized Local Oscillator (STALO) and Coherence Oscillator (COHO) oscillator instabilities.

*The zero-velocity filter output of a parallel FFT doppler processor is $e^{j\pi fT(N-1)} \cdot \frac{\sin \pi fTN}{\sin \pi fT}$ where f is frequency, T is pulse period and N is the order of the FFT. The frequency shift between adjacent filter is $\frac{1}{NT}$, which gives a phase difference in this equation between adjacent filters of $\frac{\pi(N-1)}{N}$ rad or 157.5° for N = 8.

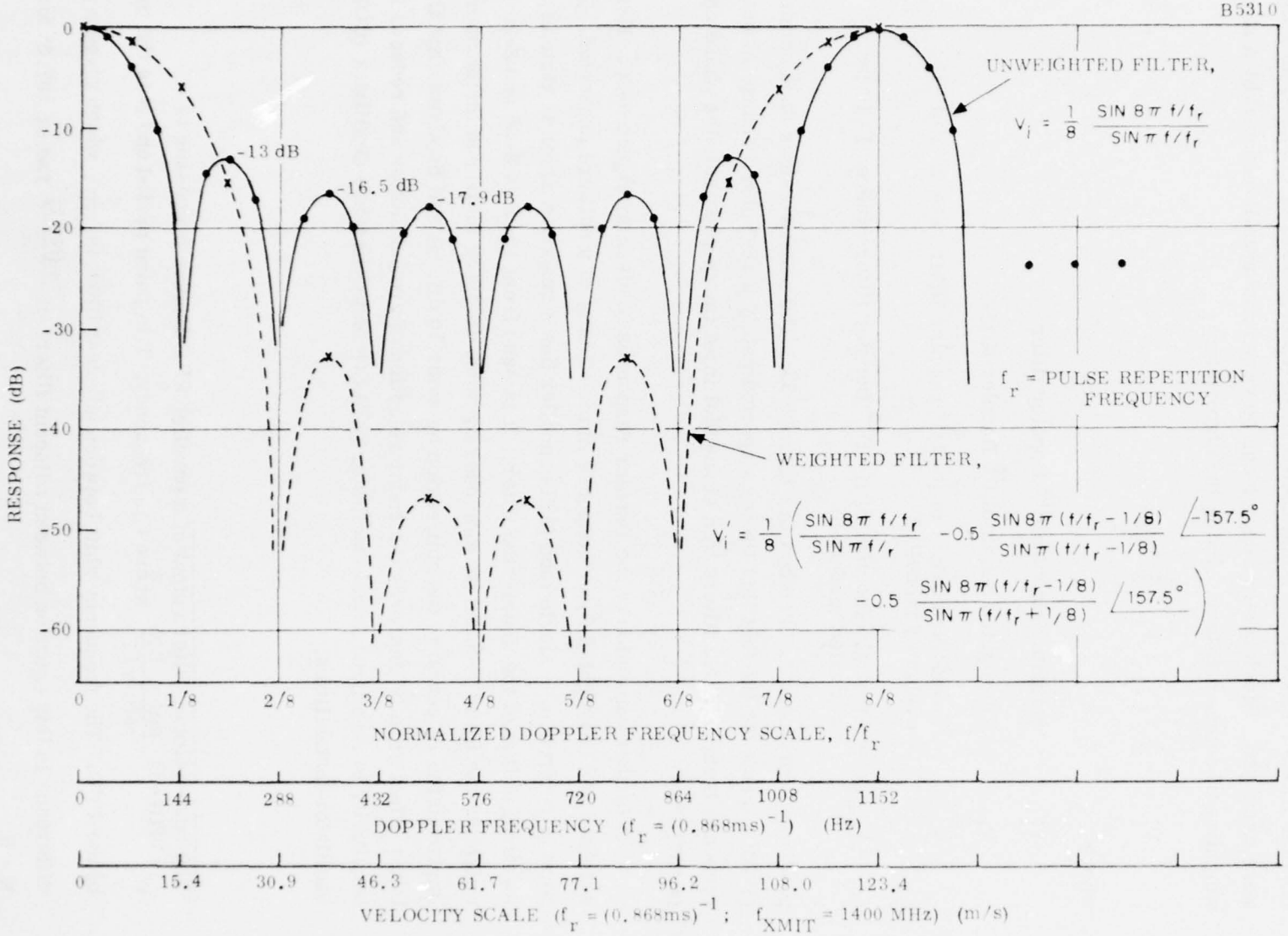


Figure 3-35. Weighting Effect on Doppler Filter Response

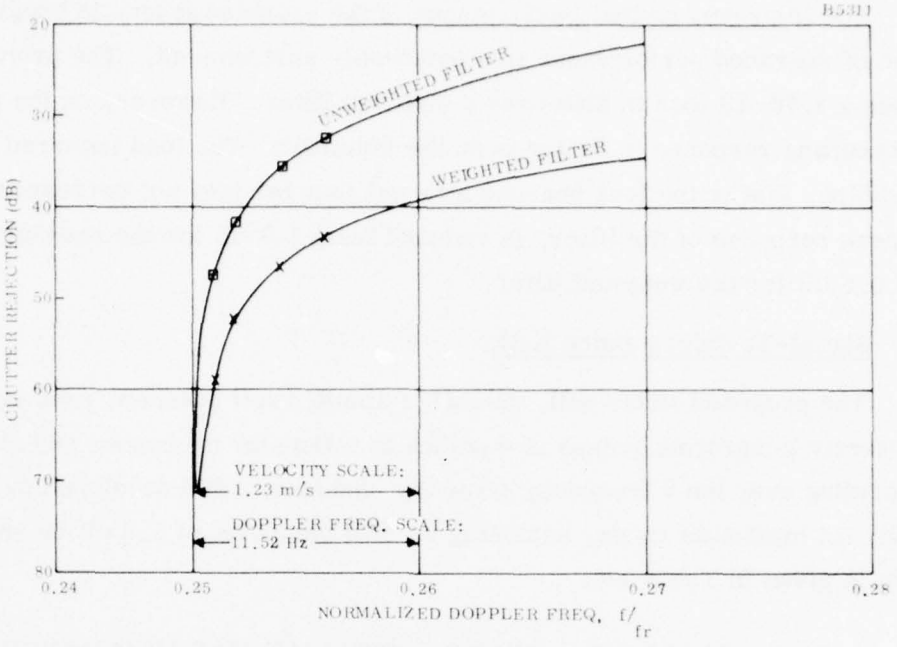


Figure 3-36. Doppler Filter Response in Null Region (of Second Null)

Locating the ground clutter, which is the most significant source of interference, relative to the Doppler filter response is necessary in determining which filters would benefit from weighting. Figure 3-34 shows each Doppler filter mainlobe response. If the entire response were drawn it would be seen that every filter except filter no. 0 has a null at zero frequency, which is the location at which ground clutter exists. The effect of weighting any filter, as shown in Figure 3-35, is to greatly widen the extent of the null region as well as widen the mainlobe so that the first null is eliminated. However, all remaining nulls of the weighted response correspond precisely in location with the nulls of the unweighted pattern. In the proposed design, filters 2 through 6 will be weighted. Each of these filters will, therefore, have a much higher rejection of clutter at zero frequency; i.e., ground and sea clutter. Also, these filters will have low sidelobes which improves their rejection of weather clutter. It would be counter-productive to weight filters 1 and 7 since they already have a null at zero frequency which, while not too wide, would be removed entirely by weighting. Furthermore, weather clutter because it is at low Doppler frequencies, will appear in the mainlobe of filters 1 or 7, so that reducing the sidelobes of these filters will have little effect on weather clutter rejection. Weighting filter zero provides no improvement to either ground or weather clutter.

The improved clutter performance of the weighted filters is bought at the expense of degraded performance in a noise-only environment. The proposed weighting causes a 1.76-dB loss in SNR over a matched filter. However, on the positive side, the resulting response is flatter over the mainlobe. The loss incurred by Doppler straddling, that is the loss because a target Doppler may not correspond exactly to the peak response of the filter, is reduced from 1.1 dB for the unweighted filter to only 0.5 dB for the weighted filter.

(4) Signal-To-Interference Ratio

The proposed radar will, on each azimuth dwell position, process 32 pulses by coherently integrating groups of 8 pulses in a Doppler processor and noncoherently integrating over the 4 frequency diversity channels. SNR developed over this single dwell, (at maximum range, assuming an SNR per pulse of 1.5 dB as shown in Figure 3-20) is given in Table 3-6.

TABLE 3-6. SNR PER DWELL AT MAXIMUM RANGE

SNR per pulse at maximum range (see Figure 3-20)	1.5 dB
Coherent integration gain (8 pulses)	9.0 dB
Noncoherent integration gain (4 samples summed, loss relative to coherent summation is 1 dB)	5.0 dB
Diversity gain (improvement in Swerling Case 2 target detection by obtaining 4 independent samples of the target RCS through frequency diversity)	4.5 dB
SNR Total Per 32-Pulse Dwell (at maximum range)	20.0 dB

(Corresponding Probability of Detection Per Scan For Swerling Case 1 Target for a P_{FA} of 2.5×10^{-7} (see pages 3-54B and 3-55)= 0.86)

Ground clutter causes the most severe form of interference to the proposed radar. Figure 3-20 shows the 84th percentile ground clutter reaches its highest level of 35.4 dB above a 1 m^2 target at the maximum range of 30 nmi. This -35.4 dB SCR Clutter ratio (SCR), will be greatly improved by the coherent Doppler filtering process. A ground clutter velocity spread (one standard deviation) of:

$$\sigma_v = 0.3 \text{ m/s}^* \qquad (3\text{-}24)$$

*Radar Equations for Jamming and Clutter, D.K. Barton, IEEE Transaction on Aerospace and Electronic Systems, Vol. AES-3, No. 5, November 1967.

and a radar oscillator stability of 2 parts in 10^9 over the 8-pulse transmission will be assumed. This gives a resulting velocity spread of:

$$\sigma_{v(total)} = \sqrt{\sigma_v^2 + (\Delta f \times \lambda/2)^2} = 0.42 \text{ m/s} \quad (3\text{-}25)$$

where

Δf = Frequency variation due to oscillator instability

$\Delta f = f \times 2 \times 10^{-9}$

f = Radar carrier frequency

λ = Wavelength $= \frac{c}{f}$

c = Speed of light $= 3 \times 10^8$ m/s

$\Delta f \times \lambda/2$ = Apparent velocity variation of a target due to oscillator instability

$\Delta f \times \lambda/2 = f \times 2 \times 10^{-9} \times \frac{1}{2} \times \frac{c}{f} = 0.3$ m/s

Figure 3-36 shows that the weighted doppler filter provides a rejection, to clutter having a spread of 0.42 m/s about the null of the filter, of 47.5 dB. The unweighted filter provides 37-dB rejection.*

Table 3-7 gives the signal-to-ground clutter, S/C_g, per dwell for the outputs of any of the weighted Doppler filters using 84th percentile clutter. Evaluation is made at maximum range where the S/C_g ratio is poorest. The resulting S/C_g of 21.6 dB can also be taken as the signal-to-median-ground-clutter ratio out of the unweighted filters (nos. 1 and 7). This occurs because the 10-dB poorer rejection is offset by the 10-dB lower level of the median clutter to 84th percentile clutter.

*It is not obvious that Figure 3-36 can be used to obtain clutter rejection of a filter by entering the curve with clutter velocity spread. A verification can be simply made since the unweighted response corresponds almost precisely to an unweighted single canceller MTI. The single MTI canceller has a rejection of 37 dB (Radar Design Principles, F. E. Nathanson, 1969, McGraw-Hill, Figure 9-10) for the following conditions corresponding to the proposed radar:

$\sigma_v = 0.42$ m/s, $= 0.21$ m and $f_r = (0.862 \times 10^{-3})^{-1}$

This 37-dB rejection agrees exactly with that obtained from Figure 3-36 as stated above.

TABLE 3-7. SIGNAL-TO-84TH-PERCENTILE-GROUND-CLUTTER PER DWELL AT MAXIMUM RANGE

S/C_g per pulse at maximum range (see Figure 3-20)	-35.4 dB
Weighted Doppler filter clutter rejection relative to signal (for $\sigma_{v(ground)}$, = 0.3 m/s and 2 parts in 10^9 radar oscillator stability)	+47.5 dB
Noncoherent integration gain* (4 samples summed, loss relative to coherent summation is 1 dB)	+5.0 dB
Diversity gain* (improvement in Swerling case 2 target detection by obtaining 4 independent samples of the target RCS through frequency diversity	+4.5 dB
S/C_g Total Per 32-Pulse Dwell (at maximum range) =	+21.6 dB

Sea clutter levels, C_s, are 16 dB below median ground clutter (see Figure 3-20). The velocity spread of the sea clutter is 0.6 m/s for sea-state 4 making the rejection of sea clutter somewhat more difficult than the ground return. Combining this velocity spread with the effect of radar instabilities (equivalent to 0.3 m/s) gives an effective spread of 0.67 m/s. The rejection of this clutter is obtained from Figure 3-36 as 44 dB for the weighted filter and 33 dB for the unweighted. Computing S/C_s in the same manner as S/C_g was calculated in Table 3-7 gives at maximum range:

$$S/C_s = \begin{matrix} 44.1 \text{ dB out of weighted filters 2 through 6} \\ 33.1 \text{ dB out of unweighted filters 1 and 7} \end{matrix}$$

Weather clutter differs from ground and sea clutter in that it has a significant mean velocity. Weather clutter varies over the velocity range shown in Figure 3-34. Intensity of weather clutter can be some 10 dB above the target levels (see Figure 3-20). If this level of clutter appears in the mainlobe (in frequency) of any of the Doppler filters it will mask the $1\,m^2$ target. For those filters in which the clutter is in a sidelobe considerable rejection is achieved. The weighted Doppler filters have peak sidelobes 32 dB down from their peak. For these filters, Table 3-8 shows the resulting signal to weather clutter, S/C_w, to be 31.5 dB.

*Frequency changes on the order of the LFM signal bandwidth (250 kHz) are sufficient to decorrelate the four clutter diversity samples. The signal plus clutter would then integrate in the same way as signal plus noise providing a noncoherent integration gain. Larger frequency separations result in independent signal samples which, for a fluctuating target in noise, produce a diversity gain. The two effects in combination account for the net 4 sample gain of 9.5 dB in detectability of a Swerling 2 target in uncorrelated clutter over that of a Swerling 1 target in correlated clutter.

TABLE 3-8. SIGNAL-TO-WEATHER-CLUTTER IN DOPPLER SIDELOBES AT MAXIMUM RANGE

S/C_W per pulse at maximum range	-10.0 dB
Weighted Doppler filter rejection in sidelobes	+32.0 dB
Noncoherent integration gain* (4 samples summed, loss relative to coherent summation is 1 dB)	+5.0 dB
Diversity gain* (improvement in Swerling case 2 target detection by obtaining 4 independent samples of the target RCS through frequency diversity)	+4.5 dB
S/C_W Total Per 32-Pulse Dwell for clutter entering through weighted Doppler filter sidelobes	31.5 dB

(5) Single-Scan Performance

A computer program was written to derive the probability of detection performance for the expected clutter conditions and radar operation; i.e., 8-pulse Doppler processor and 4-diversity channels noncoherently integrated. All of the worst case clutter conditions previously described were input to the program. The program, in turn, analyzes performance for a system which was approximately equivalent to the recommended radar. The results, presented in Figure 3-36A, shows the probability of detection of a 1 m^2 target at maximum range of 30 nmi as a function of target velocity. It is seen that certain velocity zones are in effect blanked out because of excessive levels of either weather or ground clutter. Filters not blanked by clutter are limited only by thermal noise and achieve a probability of detection of about 0.85 which is as predicted in Table 3-7.

The aligned Doppler approach has the advantage of permitting efficient noncoherent integration and Constant False Alarm Rate (CFAR) normalization between diversity channels. This comes at the expense of a velocity response which is completely periodic giving rise to the blind speeds; i.e., regions of very low probability of detection. A nonaligned Doppler approach obtained by using frequency diversity in 4 channels and not adjusting the PRF to compensate for Doppler shifts, is shown for comparison in Figure 3-37. It is seen that this approach is somewhat of a compromise in that the very good and very poor regions of the aligned approach have been spread out into what might be referred to as a mediocre performance level.

*Frequency changes on the order of the LFM signal bandwidth (250 kHz) are sufficient to decorrelate the four clutter diversity samples. The signal plus clutter would then integrate in the same way as signal plus noise providing a noncoherent integration gain. Larger frequency separations result in independent signal samples which, for a fluctuating target in noise, produce a diversity gain. The two effects in combination account for the net 4 sample gain of 9.5 dB in detectability of Swerling 2 target in uncorrelated clutter over that of a Swerling 1 target in correlated clutter.

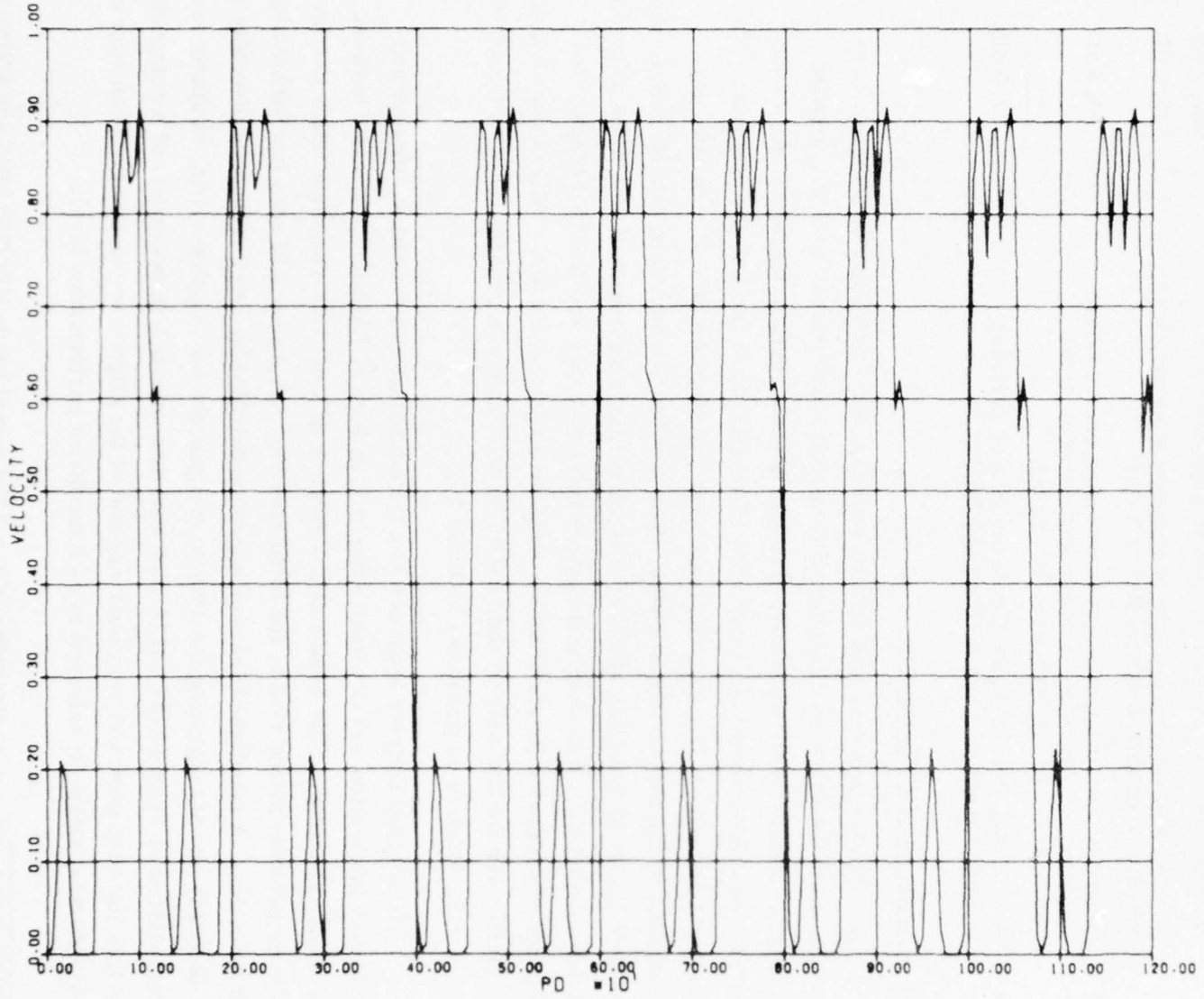


Figure 3-36A. Single-Scan Probability of Detection as Function of Target Velocity, Aligned Doppler Channels, Both Ground and Weather Clutter Present

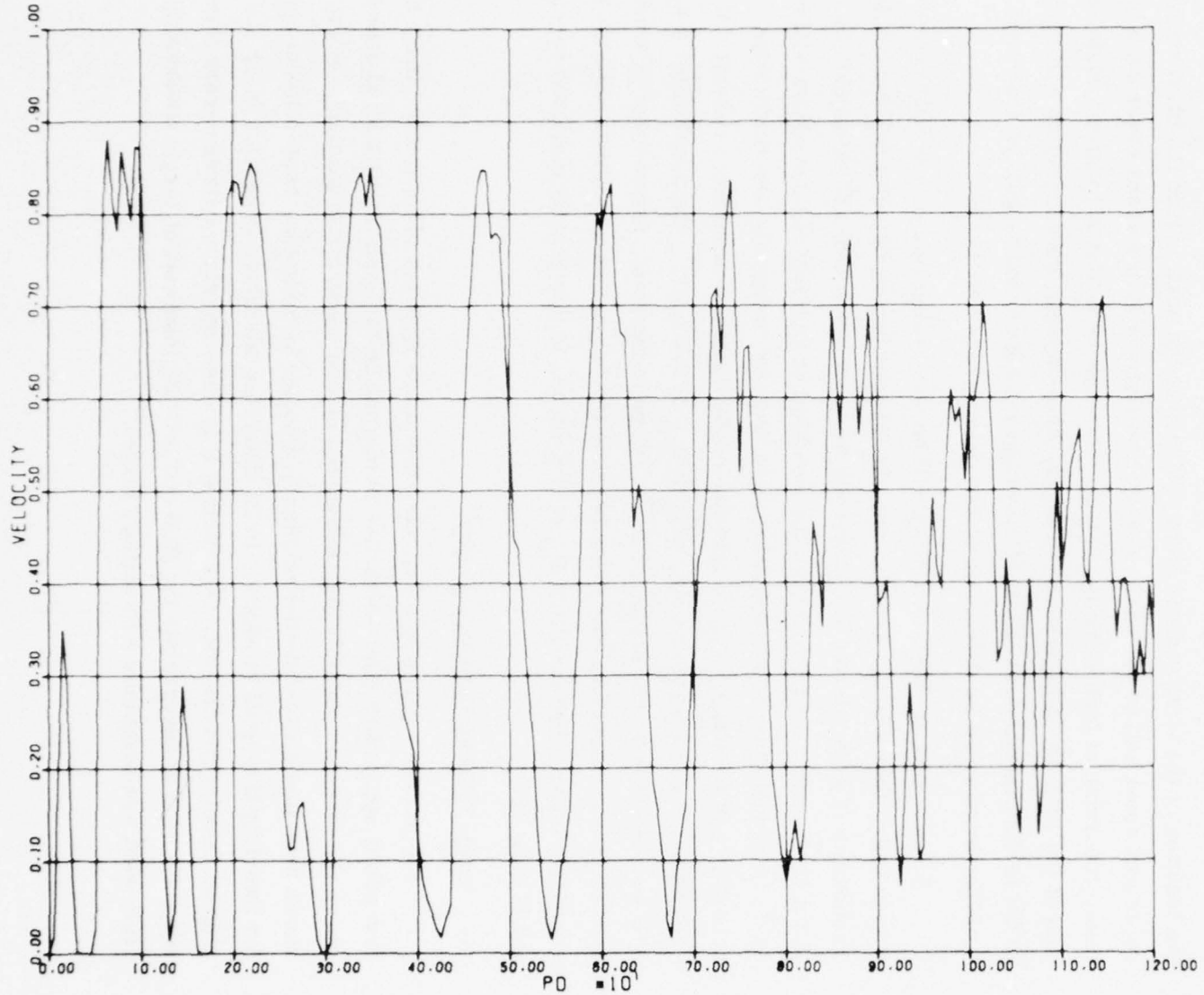


Figure 3-37. Single-Scan Probability of Detection as Function of Target Velocity, Unaligned Doppler Channels, Both Ground and Weather Clutter Present

Radar coverage is provided in the blind speeds of Figure 3-36A by changing the pulse repetition rate between each scan of the radar. This has the effect of changing the location of the blind regions from one scan to the next. Since the blind regions represent about half of the total velocity, the radar will in 4 scans cover each blind zone, occurring at high velocity, twice. This will be achieved by appropriate selection of the PRF set in each scan. That is, scan-to-scan PRF selection will be made to fill in the blanked out regions of coverage for high speed targets so that high velocity targets will be detectable in two out of every four scans.

A scan-to-scan detection policy will be used which requires simply one detection in every four scans. That is, one-out-of-four binary detector will be employed. Probability of false alarm, P_{FA}, in each range-azimuth cell will be adjusted to 2.5×10^{-7} so that over four scans the resultant probability of false alarm will be 10^{-6}. The one-out-of-four detection logic requires relatively low single scan probability of detection, P_D, to achieve a 0.95 detection probability overall. If each scan provides a P_D of 0.53, with a P_{FA} of 2.5×10^{-7}, the result after 4 scans will be a P_D of 0.95 and a P_{FA} of 10^{-6}. More to the point, assume that in 4 scans the target was detectable only twice because the target was at a blind speed for the other two scans. The resulting P_D over 4 scans, in this heavily cluttered case, would be 0.78.

(6) Scan-To-Scan Detection Policy

The previous paragraph indicated that a one scan out of four scan binary detection policy appears to offer attractive performance for systems with blind speeds, where the target is possibly only detectable on two scans out of the four. It will be shown here that a one-out-of-four binary detector is a simple, near-otimum approach for Swerling II targets in addition to its detection advantage in heavy clutter and aligned Doppler processing. A Swerling II is assumed since between scans there is adequate time to decorrelate the RCS and provide independent target observations from what was originally a Swerling I target.

The relationship between single-scan probability of detection, P_{D_1}, and four scan probability of detection, P_{D_4}, is given by the following equations for the various second thresholds, M:

- For four-out-of-four binary detector, (M = 4)

$$P_{D_4} = \left(P_{D_1}\right)^4 \tag{3-26}$$

- For three-out-of-four binary detector, (M = 3)

$$P_{D_4} = \left(P_{D_1}\right)^4 + C_3^4 \; P_{D_1}{}^3 \left(1 - P_{D_1}\right) \tag{3-27}$$

- For two-out-of-four binary detector, (M = 2)

$$P_{D_4} = \left(P_{D_1}\right)^4 + C_3^4 \left(P_{D_1}\right)^3 \; 1 - \left(P_{D_1}\right) + C_2^4 \left(P_{D_1}\right)^2 \; 1 - \left(P_{D_1}\right)^2 \tag{3-28}$$

- For one-out-of-four binary detector, (M = 1)

$$P_{D_4} = 1 - \left(1 - P_{D_1}\right)^4 \tag{3-29}$$

where C_j^i = combination of i things taken j at a time = $\frac{i!}{j!\,(i-j)!}$

The probability of false alarm, P_{FA}, on a single look is related to the resulting probability of false alarm by the same set of equations as above. For an overall P_{FA} of 10^{-6}, the P_{FA_1} per look is:

$$P_{FA_1} = \begin{cases} 3.2 \times 10^{-2}, & \text{for M = 4} \\ 6.3 \times 10^{-3}, & \text{for M = 3} \\ 4.1 \times 10^{-4}, & \text{for M = 2} \\ 2.5 \times 10^{-7}, & \text{for M = 1} \end{cases} \tag{3-30}$$

A plot of single-scan probability of detection as a function of SNR is given in Figure 3-37A for each of the above values of P_{FA_1} assuming a Swerling I target. That is, the target cross section is taken as an exponential probability density function. Single-scan detection is based on the recommended process of 8-pulse coherent integration followed by a 4 (statistically independent) sample noncoherent integration.

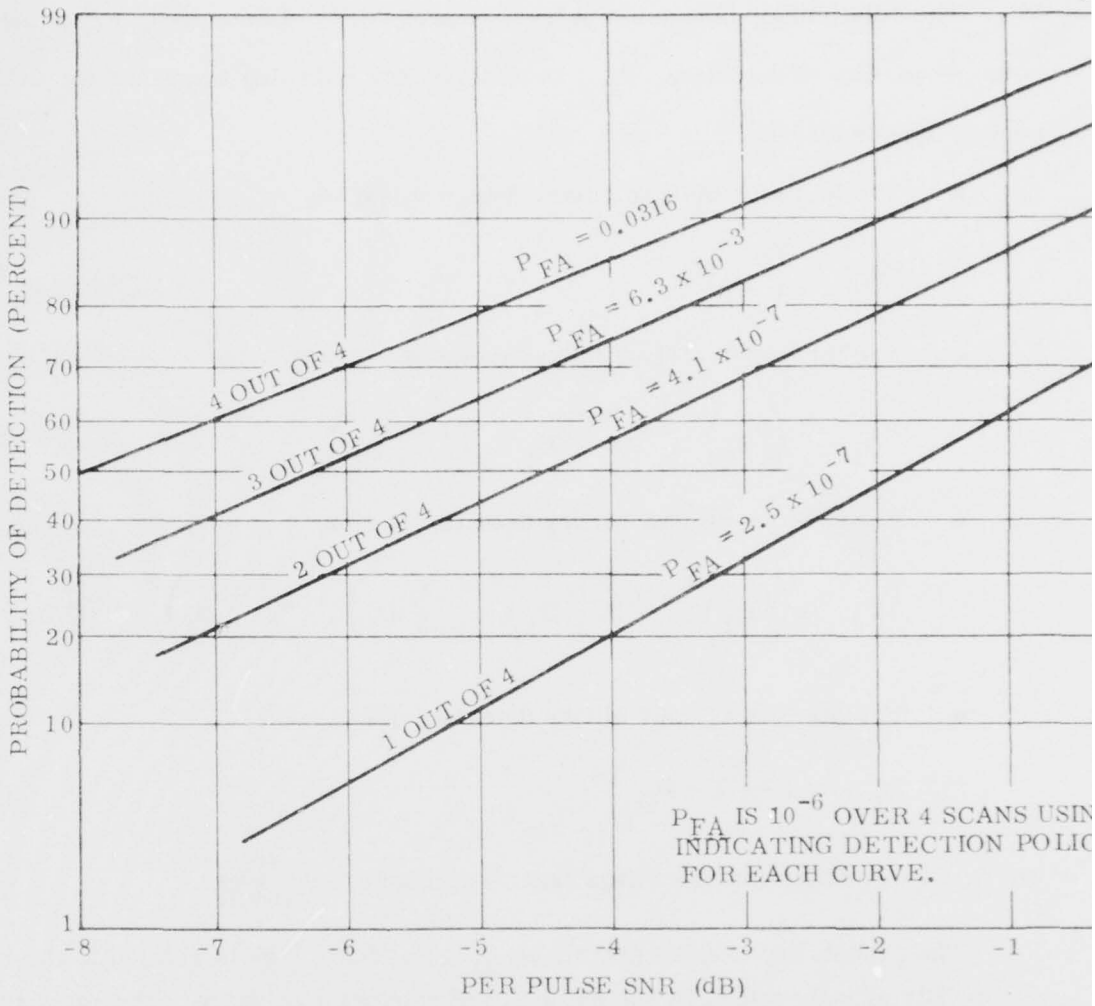


Figure 3-37A. Single-Scan Detection Probability

The probability of detection over four scans, P_{D_4}, is computed as a function SNR for each detection policy by substituting the single-scan probability of detectio results into the appropriate Equation (3-26) through (3-29). These results, for fou scan probability of detection are presented in Figure 3-38.

The results of this analysis show that a one-out-of-four binary detection polic require an SNR to achieve a given P_{D_4} that is within 0.5 dB of the three-out-of-fou scheme. The resulting false alarm reports on each scan, however, are far fewer the one-out-of-four policy as shown by Equation (3-30), thus reducing the data processing load.

Figure 3-38 indicates a 0.95 probability of detection can be achieved with an SNR of -1.6 dB per pulse using the one-out-of-four rule and an overall P_{FA} of 10^{-6}. This value corresponds to the probability of false track initiation due to noise of 10^{-6} for the one-out-of-four policy shown in Figure 3-38.

c. ECM RESPONSE

The unattended radar design goals included that of ECM warning. The principal means by which this is provided is via an azimuth strobe indication. This is generated by superthresholding of the range normalizer (i.e., mean level threshold circuits). Thus, when a jammer in the mainlobe causes a substantial increase in the background estimate derived by the normalizer, this condition is tested against a jamming threshold (note that multiple level thresholding can be employed if necessary) and reported if it exceeds this threshold. To prevent false jamming strobes from occurring due to strong returns from jammers in a sidelobe (from either large jammers, high sidelobes, or both), a mainlobe indicator technique is employed. That is, an auxiliary antenna whose gain is somewhat higher than that of the sidelobes is used to derive an estimate of the jammer power which is compared with that of the main channel normalizer to inhibit "strobe" indicators from sidelobe jammers. This fulfills the goal for jammer reporting. Other active ECCM techniques have been included in similar designs and are strongly recommended by General Electric in certain tactical environments. However, they were excluded by customer direction from this study.

Although sophisticated ECCM were not an integral part of this design, selected ECM responses are an inherent part of the baseline design approach. These include:

- High Duty Jamming Detection and Azimuth Reporting
- Redundant Channel Available as Sidelobe Blanker
- Low Duty Asynchronous Jammers Not Integrated
- Clutter Map Data Processing Logic Removes Fixed Delay Repeaters
- Intra-scan Diversity/Inter-scan Agility Forces Jammer to Spread or Increase Energy
- Solid-state Low Peak Power Presents More Difficult Acquisition Problem to ARM than Tube Radar

3. SENSOR SUBSYSTEM

a. INTRODUCTION

In the selection of candidate RF configurations for the 2-D radar, the most urgent requirements are for minimum power consumption and reliability. The allowed prime power rules out the traditional rotating 2-D antenna. Rotating parts, if used at all, must require very low drive power, and must have highly reliable drive mechanisms. The antenna must also have very low RF losses to minimize transmitter power. Redundancy is required to achieve the reliability levels required. In some cases, redundancy occurs naturally as in the multiplexity afforded in a phased array; in other cases, redundancy has to be provided.

These factors were considered in making a preliminary survey of antenna techniques applicable to this program. Three basic approaches are described below which are considered to have these desirable features; two are electrically scanned arrays, and one is a mechanically scanned array using a low inertia scan technique.

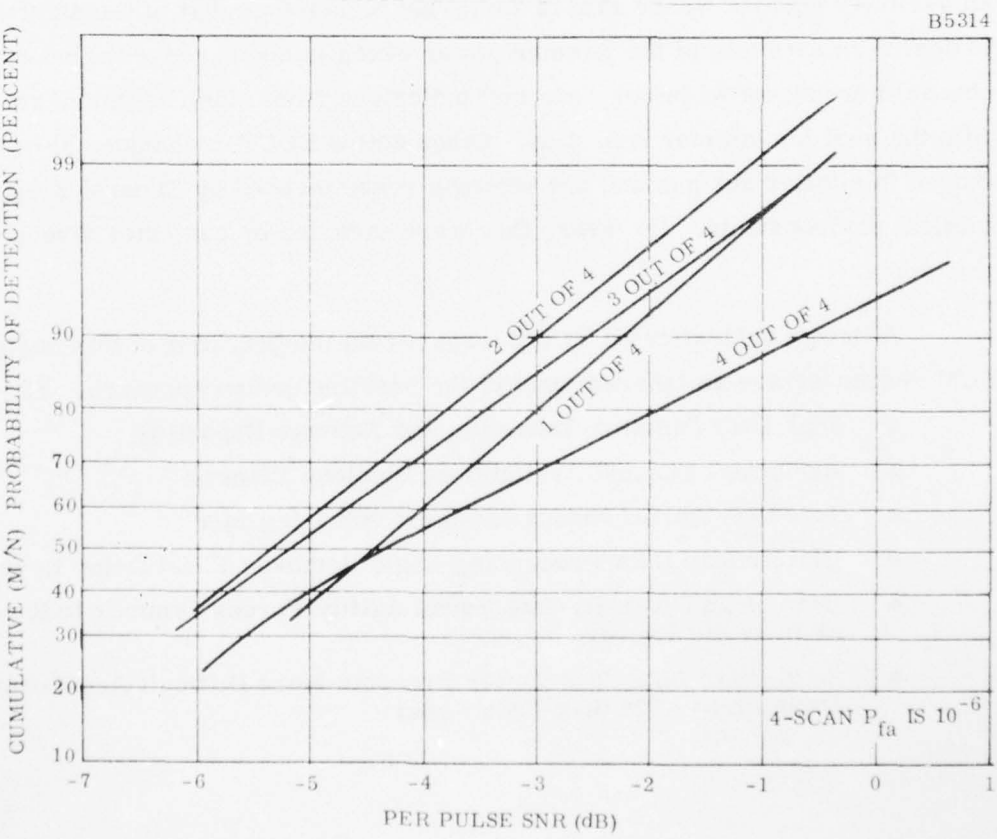


Figure 3-38. Binary Detection Over Four Scans

Four physical configurations for three basically different RF designs for a 2-D unattended radar are presented in Figure 3-39. Reliable unattended performance and low power consumption are prime considerations for a 2-D system. The configurations shown are representative of many possible equipment implementations which were evaluated in detail. These system illustrations do not include intersite communication antennas or power generation equipment but are presented to indicate general characteristics of candidates considered.

Figure 3-39(a) is a completely inertialess system with UHF cylindrical array and separate circular IFF antenna. The openness of the large UHF array lends itself to direct environmental exposure. However, radome protection may be required for the IFF antenna as shown depending on site location. A small arctic shelter beneath the antenna structure houses the remaining electronic equipment. This offers the advantage of low cost for RF power but requires a separate IFF antenna and high construction costs. It was eliminated from consideration for these reasons and the performance considerations (e.g. multipath performance, lack of diversity, etc.) cited above.

Figure 3-39(b) shows a possible configuration of an L-band cylindrical array with integral IFF. This higher frequency antenna is more prone to ice buildup and is more sensitive to wind and ice loading than UHF systems, and therefore radome protection has been provided. The antenna/radome assembly is tower-mounted to compensate for local terrain features and ground effects. An arctic shelter is shown adjacent to the air-lock hatchway for radar electronics. Several variants of this basic approach were designed in detail as discussed below.

A third representative 2-D configuration is shown in Figure 3-39(c). This system uses a fixed L-band antenna in a six-face Y-configuration. Bilateral feed networks connect to radiating dipoles on each face. Antenna protection is provided by three tubular air-supported radomes. The radomes are attached to the central air-lock structure and are guyed for increased stability. A center support tower and equipment shelter complete the radar system. This approach was given serious consideration, and is an attractive approach for this application. However, it was judged to require higher prime power than the L-band cylindrical array.

The fourth representative physical configuration for the 2-D radar is illustrated in Figure 3-39(d). This system utilizes a 360° parabolic torus antenna. This unique concept incorporates a dual rotating horn assembly to illuminate a $\csc^2$ shaped radome wall with imbedded polarizing wires. The concept is basically applicable

to both UHF and L-band. Considerable development remains to be done on this concept. However, it effectively combines mechanical rotation with fixed reflector and integral radome protection. The torus is tower-mounted, and an equipment shelter is shown underneath. This configuration was carried through the detailed design phase due to its potentially low prime power usage and low cost. This configuration is not recommended since other less risky low power cylindrical array configurations are available.

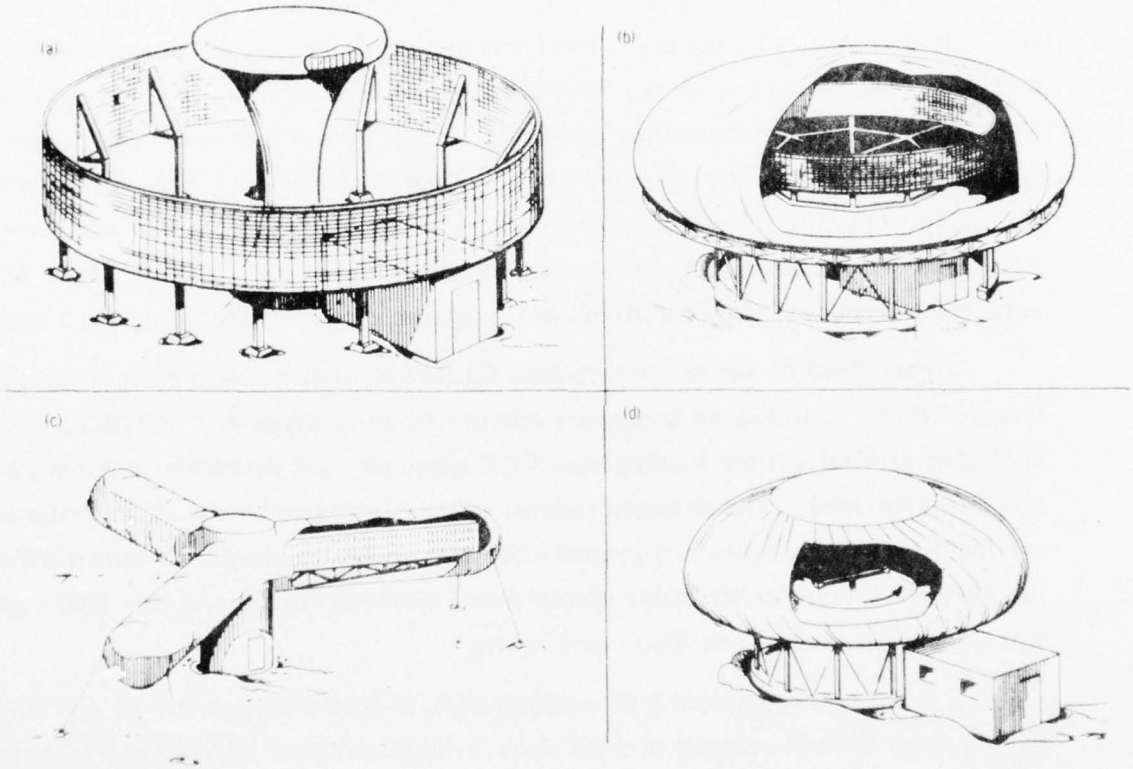


Figure 3-39. Type A Candidate Approaches

The above options were analyzed in the early phase of the design and emphasis was directed toward the several variants of the ring (or cylindrical) array with integral IFF. This was due to its attractive low-power high-reliability features combined with the flexibility to efficiently managed radar resources in terms of search frame time, azimuth coverage, and variable data rate tracking. In addition, a concept was derived for responsive Selective Identification Feature (SIF)/IFF operation wherein these transmissions are only generated and radiated in response to a verified skin return detection. In this manner, the radar and SIF/IFF functions are efficiently time-shared resulting in substantial prime power savings by allowing integral

IFF without sacrificing a large fraction of the time line to the SIF/IFF function. In addition, the ring geometry is ideally suited for generation of the transmit amplitude modulation required for Sidelobe Suppression (SLS) operation. The general characteristics of the ring array are discussed below.

b. PHYSICAL DESCRIPTION

Figure 3-40 shows an artist concept of the baseline cylindrical L-band system. The antenna enclosure and array structure are cut away to illustrate the basic configuration.

A ring of vertical steel trusses support a central roof structure and, along with connecting structural members, provide support for the 128 stripline RF feed boards. A half-torus shaped rigid radome cover provides weather protection for the array. The radome is constructed of thin fiberglass reinforced Teflon panels which result in negligible RF perturbation. This newly developed radome panel material has a 20-year maintenance free life and provides a high degree of natural anti-icing.

Wall panels on the inside of the ring trusses form a maintenance area and equipment room for remaining radar components. One rack accommodates the solid-state transmitter modules and two cabinets house signal processor and communication equipment. A work bench, storage cabinet and test equipment are included in the room. A total energy approach utilizing waste power generation heat, provides required environmental control within the radar equipment room.

The array and radar equipment enclosure is mounted on a 25-ft high tower. At required sites, the tower may be increased in height by adding modular 25-ft sections. Three 8- x 20-ft shelters are shown under and along side the radar tower. The power generation shelter is shown underneath where it provides a convenient interface with the radar for power and environmental air or water. A living quarters shelter provides accommodations for periodic visits by maintenance personnel. The third shelter houses power and radar spares. Emplacement of the shelters, tower and radar enclosure may be accomplished by crane or medium helicopters as shown in Figure 3-41. When required, the radar enclosure can be assembled at a local depot and sling-lifted to a remote site.

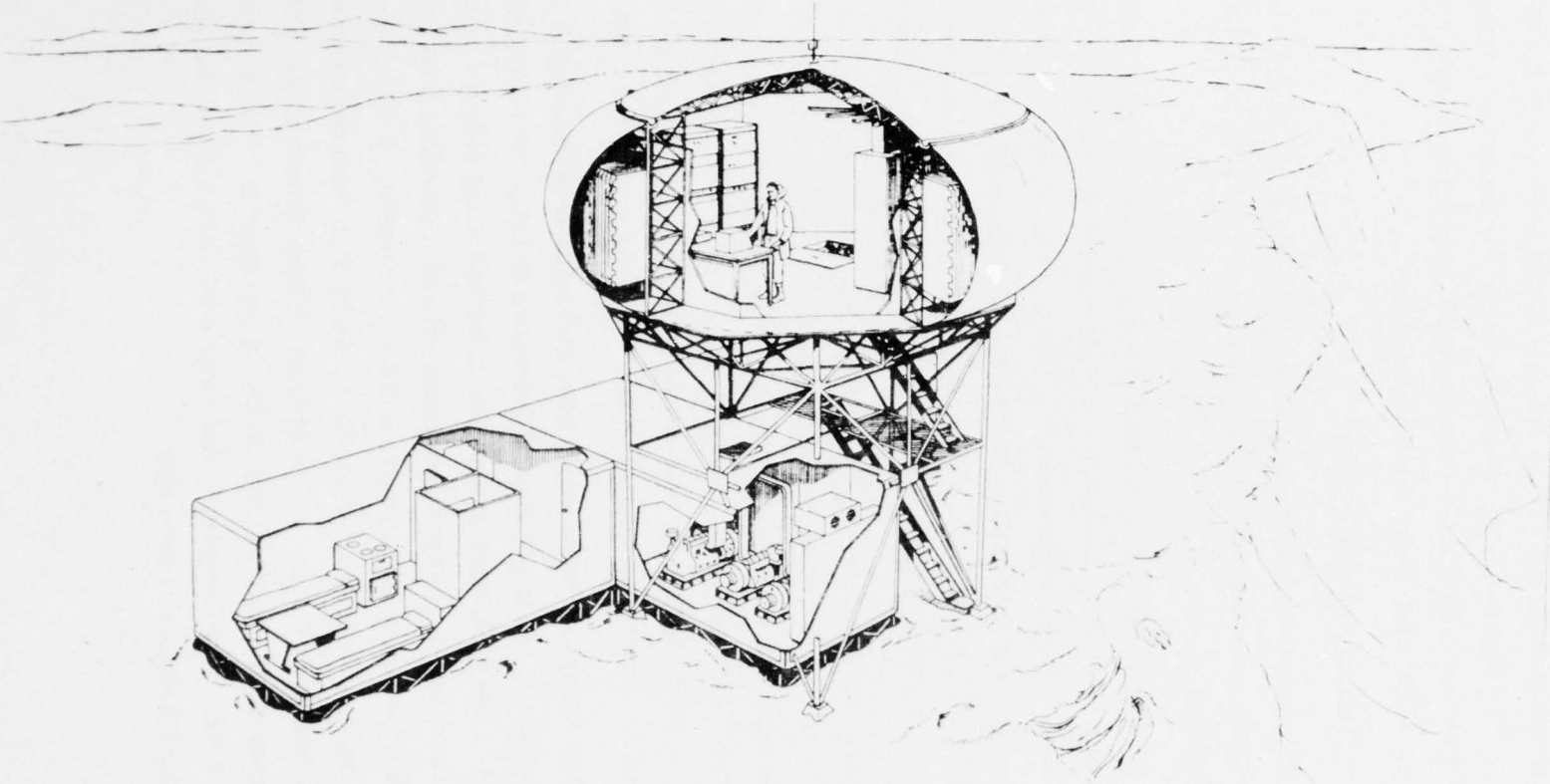


Figure 3-40. Baseline Unattended Radar Design

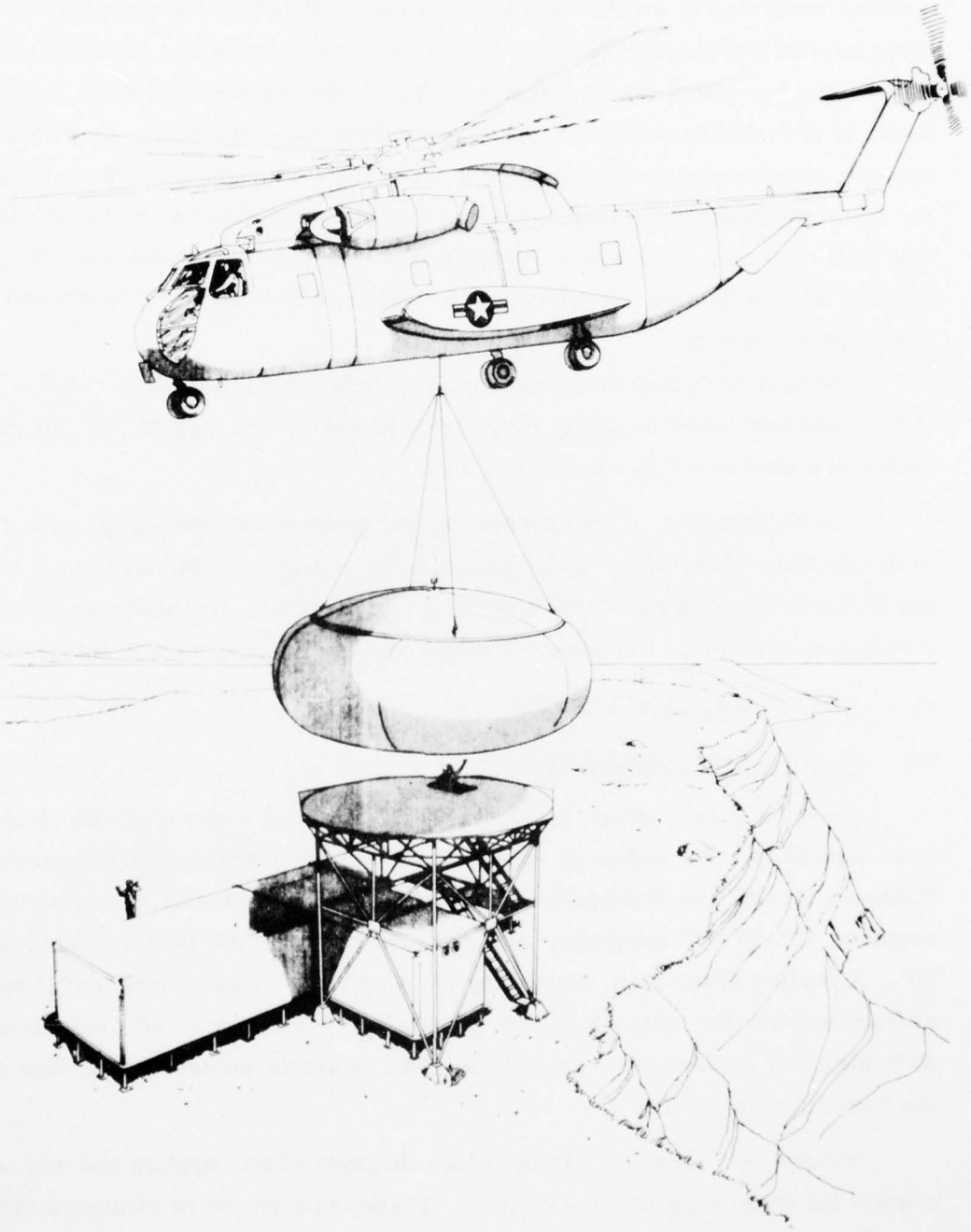


Figure 3-41. Unattended Radar Replacement

Figure 3-42 shows an alternate organ-pipe scanner array with radar tower and three support shelters. The array is composed of a central 256 port organ-pipe scanner connected to waveguide and expanded feedhorns. The rotating scanner is covered with a protective cover and openings between adjacent waveguides to provide water drainage within the dished assembly. A fiberglass-reinforced Teflon radome cover is provided to completely enclose the horn aperture ring. As with the baseline system, this radome cover provides natural anti-icing and environmental protection for the array aperture. This horn-feed approach can also be combined with the baseline radar concept as shown in Figure 3-42A and should be considered from the standpoint of simplicity and, therefore, lower costs as well as significantly reduced prime power requirements.

The scanner array is mounted on a modular steel tower with tubular connection to an equipment/spares shelter directly underneath. Waveguide, power and signal cables are enclosed in the protective tube.

The transmitter, signal processor and communications equipments are housed in the shelter, along with a maintenance bench. Adjoining the equipment shelter is the prime power generation shelter and a maintenance-personnel support shelter. Emplacement is made by truck and crane or by helicopter as with the baseline system.

c. RING ARRAY DESCRIPTION

(1) Performance Considerations

The ring array, shown in Figure 3-39, provides a 360° azimuth electronic step-scan capability. It consists of 156 columns of 8 elements each arranged on a 28.2-λ diameter circle. Excitation of 8 elements in a column is such as to provide the required -10° to +50° coverage, with $\csc^2$ pattern from 15° (100 k ft at 60 nmi) to 50°. A portion of the ring, consisting of 44 columns and covering a 101° sector, is utilized to form the azimuthal beam collimation. Scanning is accomplished by switching this active sector around the ring, in single-column steps, thus scanning the beam in steps of 2.3°.

Figure 3-43 shows a "string" block diagram of this system and was used as a basis for developing several options. These, in turn, were evaluated in terms of prime power reliability, and cost. Each column of eight elements is fed by an eight-way Butler Matrix. Proper amplitude excitation of the input ports of the Butler Matrix provides the desired elevation pattern. The principal variants which evolved in the design process are shown in summary form in Figures 3-44 through 3-46.

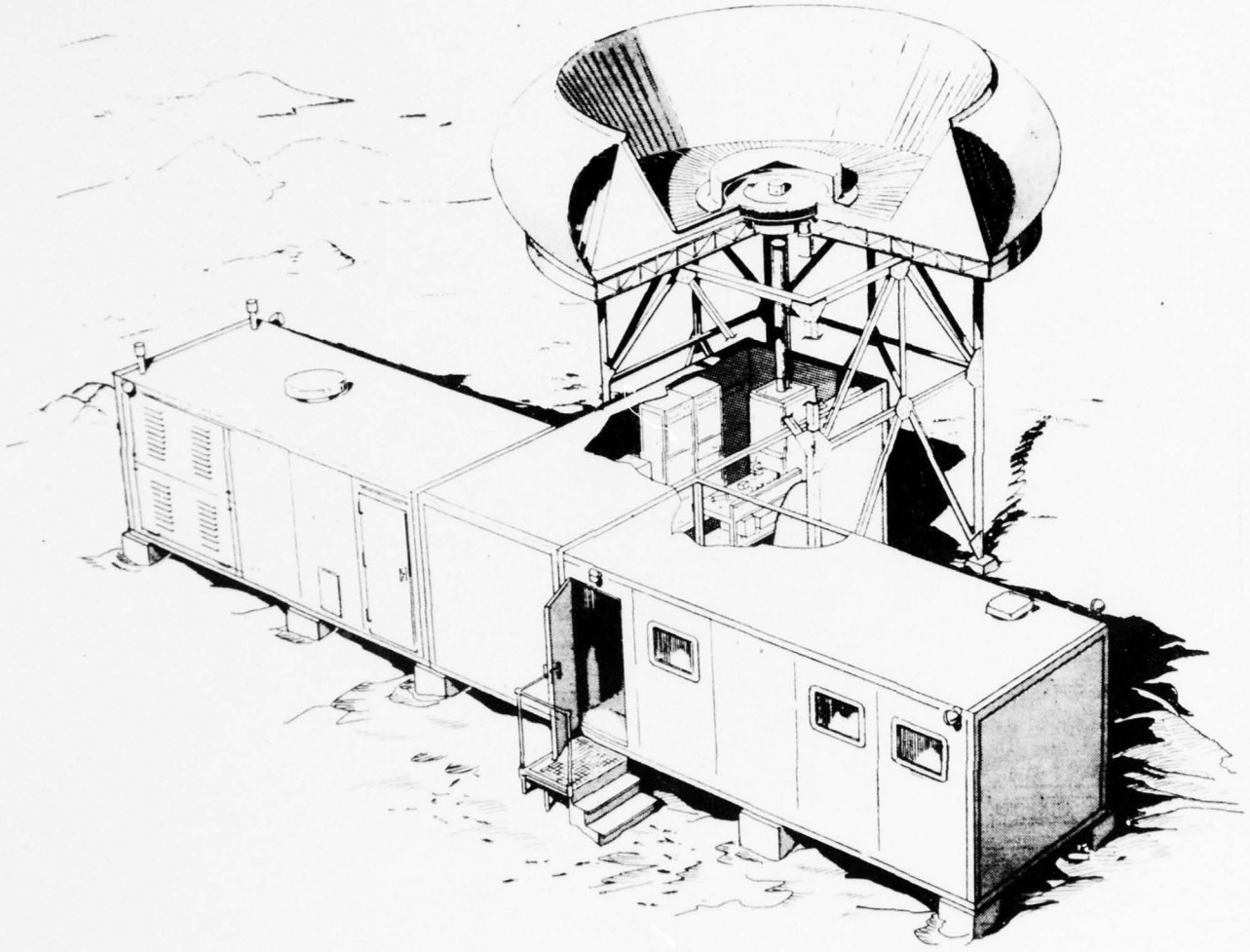


Figure 3-42. Alternate Unattended Radar Design

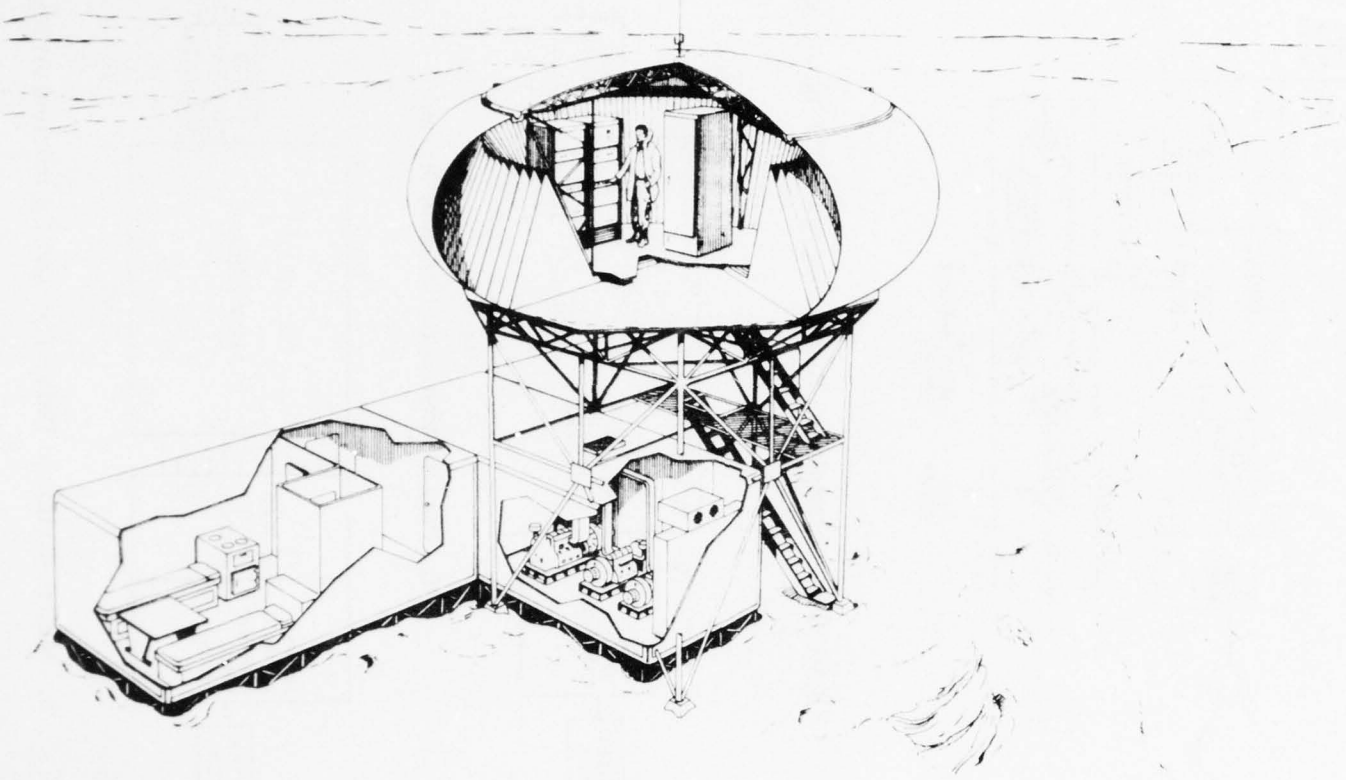


Figure 3-42A. Horn Array Inertialess Unattended Radar Design

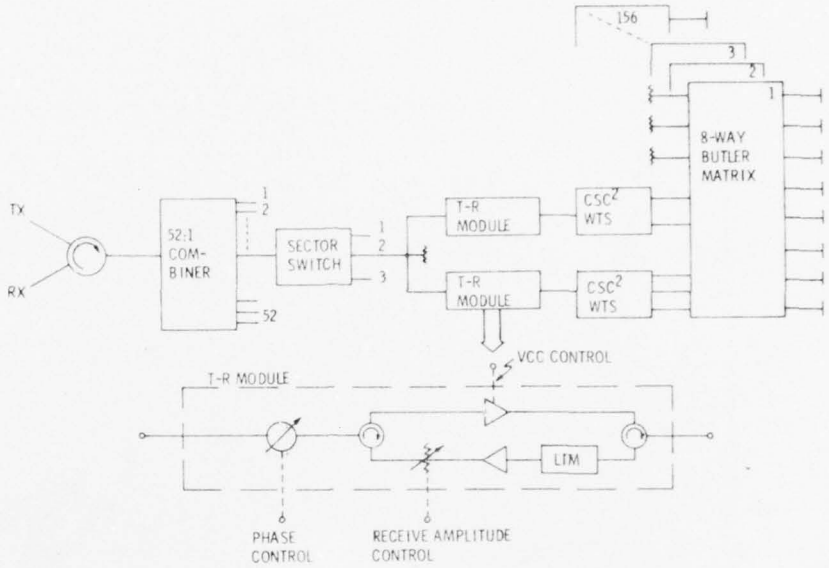
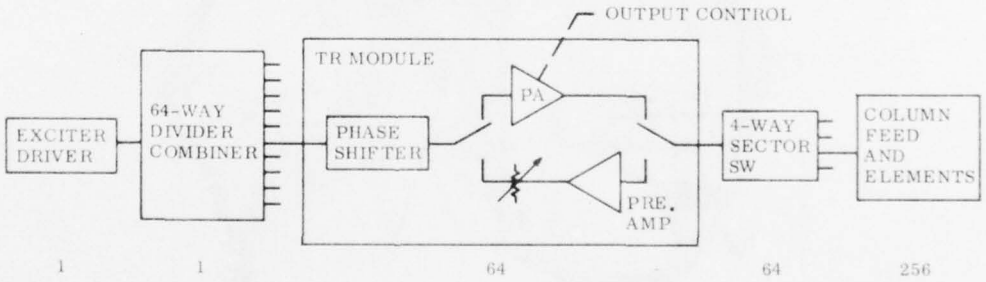
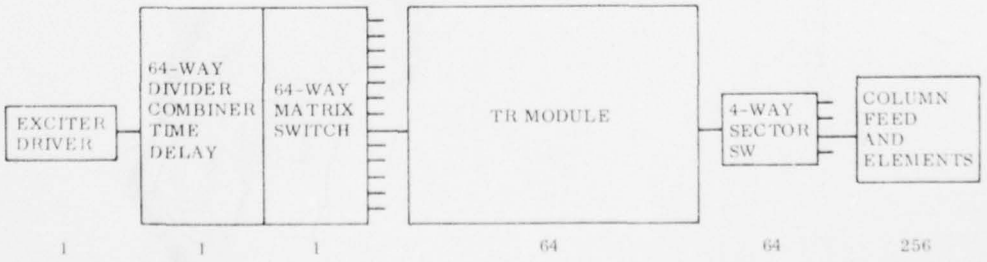


Figure 3-43. Simplified Block Diagram for Ring Array



a. Phase-Steered Cylindrical Array



b. Matrix-Switched Delay Focused Cylindrical Array

Figure 3-44. Cylindrical Arrays

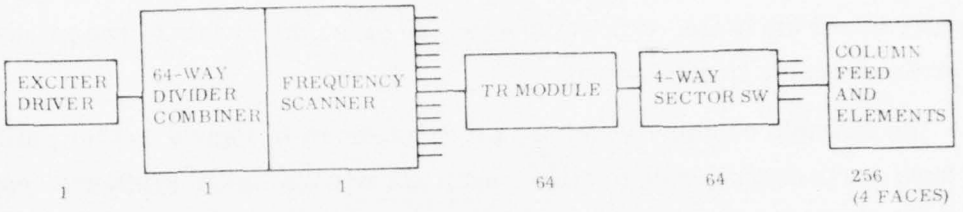


Figure 3-45. Frequency-Scanned Planar Array

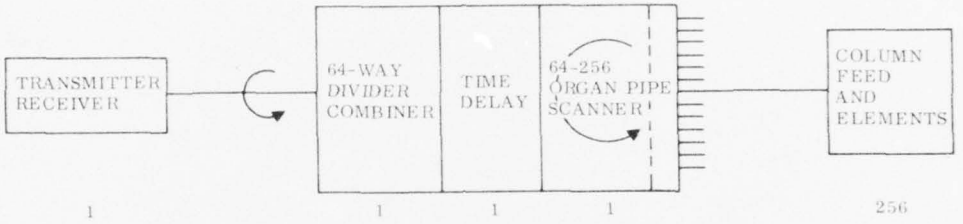


Figure 3-46. Organ-Pipe Scanned Cylindrical Array

In a ring array, the element phase excitation required to collimate the radiation, referenced to the ring center, is given by:

$$\Psi_p = -\frac{2\pi R}{\lambda} \sin\theta \cos\phi_p \qquad (3\text{-}31)$$

where

R = radius of the ring

θ = the polar angle

ϕ_p = the angular position of a radiating element, p, measured from the center of the active sector

Note that the phase is dependent on θ as well as on ϕ_p. If a ring array is collimated at a given elevation angle, it is improperly phased at angles somewhat removed in elevation. This is no problem for a pencil beam, but creates difficulty for a fan beam. The input ports of the Butler Matrix form narrow elevation beams at various elevation angles. Each of these elevation beams can be collimated in azimuth by applying a phase which is proper for that beam's elevation angle. Each Butler Matrix input port will then form a pencil beam commensurate with the aperture height and width at its particular elevation angle. By exciting several of these pencil beams stacked in elevation, an elevation fan beam is formed which maintains its beamwidth and sidelobe characteristics at all elevation angles. In some previous studies it has

been found unnecessary to independently phase each elevation beam. If the elevation coverage is not too large, it is satisfactory to phase the beams in two groups, with two or three beams in each group.

The example column elevation pattern as shown in Figure 3-47(b), utilizing five input ports corresponds to a five-beam sin x/x Woodward synthesis approximation to the desired pattern. In the case shown, the gain is allowed to decrease at negative angles, but coverage to -10° is provided.

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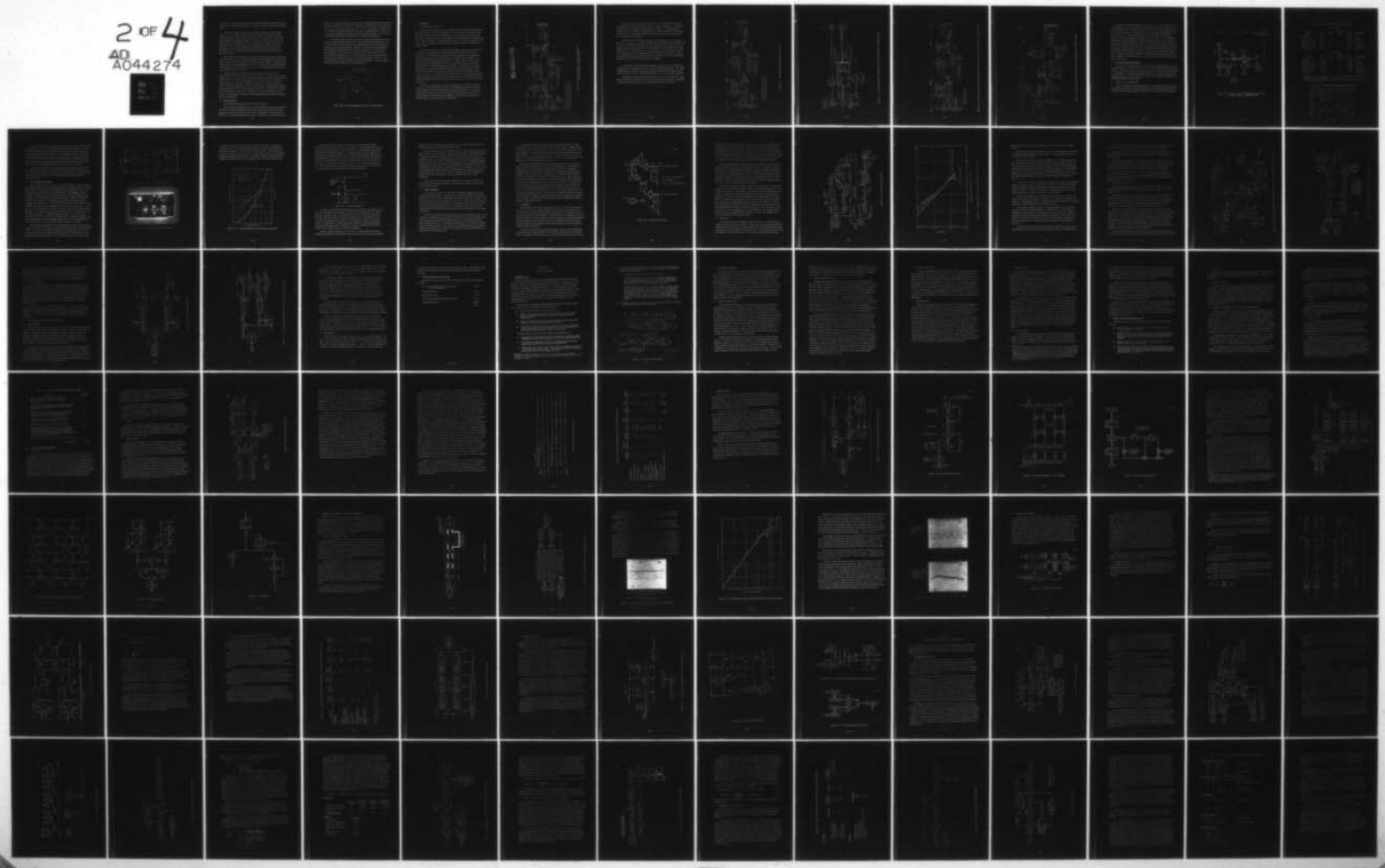


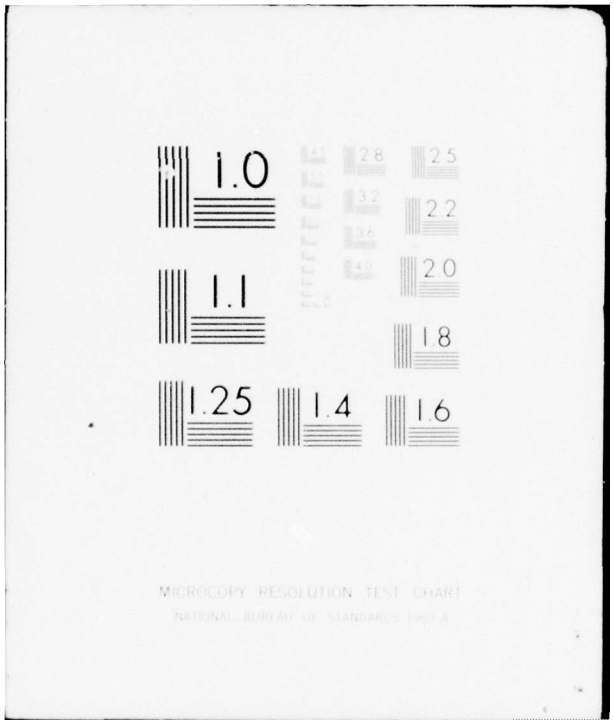
Figure 3-47. Cylindrical Array Patterns

Figure 3-43 shows the Butler Matrix being fed at five ports, but having independent phasing as two groups, one group being the lower three beams and the other group being the upper two beams. The azimuthal phasing is provided by phase shifters in the Transmit/Receive (T/R) modules which feed these two groups. The upper and lower groups are combined into a single channel on the input side of the

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UNATTENDED/MINIMALLY ATTENDED RADAR STUDY. VOLUME II. 2-D (UNAT--ETC(U)
AUG 77 T B SHIELDS, S E BELL, M I FOX F30602-76-C-0380
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

T/R modules. Subsequent analysis determined that acceptable tracks could lished with only single-level phasing to 50° elevation as shown in Figures 3- 3-46.

The sector switches consist of a set of 52 SP3T switches, which selec elements in a 120° sector which includes the active sector of 44 elements. switch is connected to three columns, separated by 120° in the array. One three will always be in the active sector. Thus, the 52 sector switches sel adjacent columns constituting a 120° sector of the array. These columns ar nected to the 52:1 divider/combiner which combines the channels and forms antenna input port. Of the 52 columns selected by the sector switches, 44 a activated at a time. The other eight are turned off by control of the amplifi their T/R modules.

This method allows flexibility in choosing the angular sector of the ac to be any value up to 120°. Small angular sectors require larger diameter larger sectors may exceed the element pattern beamwidth capability. Optir widths appear to be in the neighborhood of 100°, since this gives a reasonab to the radiation beamwidth of most array elements. The detailed designs of 3-44 through 3-46 use a 90° sector.

In order to achieve the specified sidelobes, an amplitude taper must b applied to the active sector in each mode. As the sector is switched, a give changes relative position in the sector; hence, its amplitude and phase must with azimuth scan. In the receive channel, this is done by means of a PIN modulator after the preamplifier, which is controlled by a central beam sca troller. Similarly, the transmit power level is controlled by controlling the voltage of the power module. This method provides a wide dynamic range The variable collector voltage can be supplied by a programmable power su which a variable reference voltage is used to control the output voltage in a with the scan schedule.

(2) Growth Potential

The specified growth path is from 2-D to 3-D operation.

System growth, particularly in terms of basic capability such as powe increases, are generally difficult to implement because of the compromises must be made in the basic design to allow for the modification. For this ca growth to 3-D requires relatively little, if any, compromise. The reason i

basic csc^2 coverage in elevation is provided for all configurations except the parabolic torus by a passive array column feed. The stated requirements are for coverage from -10° to +50°. As discussed in the ring array description, this may be implemented by a simple passive Butler matrix for each column of eight elements. The beam outputs are then combined and weighted to form the csc^2 beam pattern. For growth, any or all of the eight elevation beam outputs are available for processing.

A reasonable growth compromise may be one in which a subset of these eight beams are used to provide elevation data. This selection can be deferred by simply providing suitably terminated ports on the Butler Matrix for the initial design and adequate space for the subsequent processing. This approach has been derived on prior programs, and several variations may be considered. The most obvious implementation is the formation of up to eight beams on receive and the use of a stacked-beam processing approach. This necessarily increases the beamformer and processing complexity as with any stacked beam approach. However, if tri-coordinate data in search is required, this option is available. The beam configuration for a three-beam version is shown in Figure 3-48.

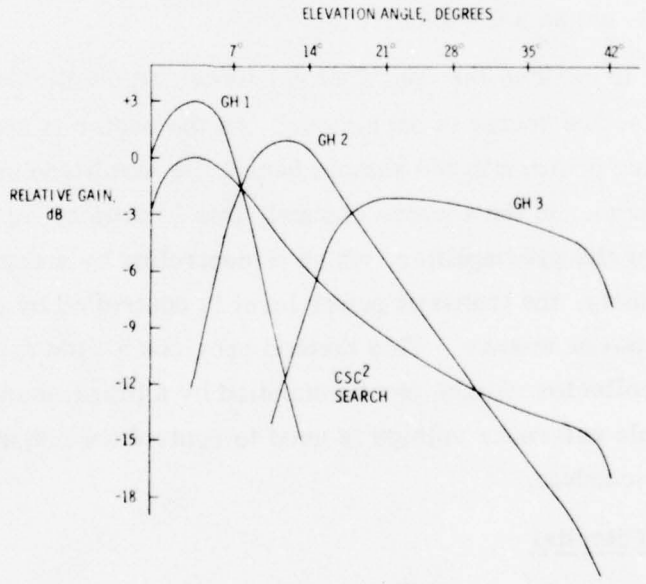


Figure 3-48. Sample Beamshapes for a Type A Growth Option

4. RF DESIGN

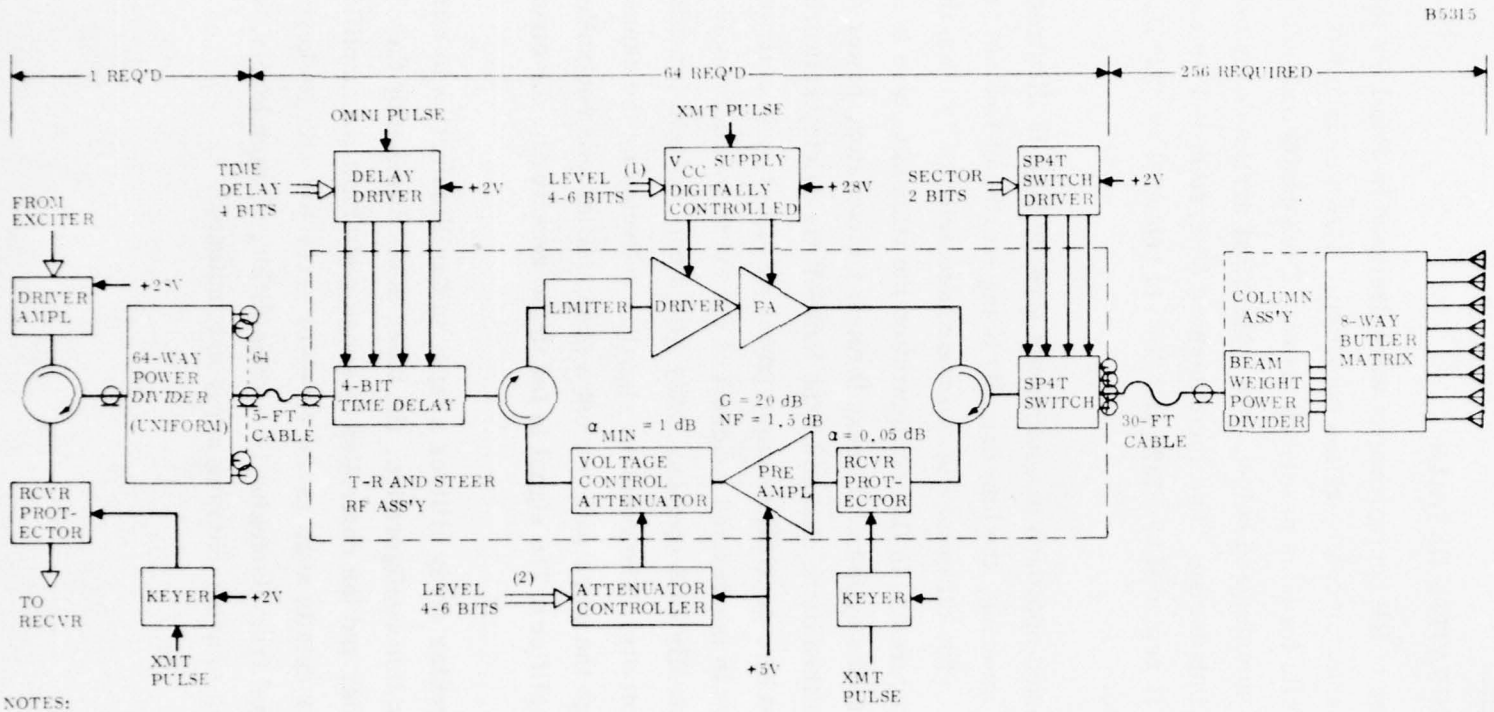
a. CONFIGURATION DETAILS

A number of RF configurations were designed in detail for the Unattended Radar to provide a basis for configuration selection. These include five cylindrical arrays and one parabolic torus as described above. Each configuration's principal merits and costs are summarized below. The cylindrical arrays described are appropriate to a 1.5° beamwidth design. The recommended 3° system is identical except that, in all cases, "256" is replaced by "128" and "64" is replaced by "32" due to the smaller array required.

The closest approach to equipments already built is illustrated in Figure 3-49. It utilizes bit steering, the bits actually being lengths of line but referred to as "phase" bits. (The difference is of importance principally when the steering commands are prepared.) In this configuration the transmit pulse is amplified in a driver, sent to the cylindrical array through a circulator, power divided 64 ways, with the pulse then being phased by the four-bit time delay network. The pulse is then amplified by a controlled-output power amplifier, and delivered to the appropriate element in the desired quadrant of the array by a four-pole switch. Each element is actually an 8-element array with a $\csc^2$ pattern providing the desired vertical directivity. The received signal is collected by the same elements and processed through the same path (except a preamplifier and controlled attenuator replace the power amplifier). The signal is fed to the receiver by the circulator at the input to the array.

The circular array utilizes a taper in the illumination to attain low azimuth sidelobes. In this configuration, the taper is established by the controlled output power amplifier and the controlled attenuator after the preamplifier. Figure 3-49 includes other details such as the receiver protector with its keyer to prevent the transmit signal from damaging the preamplifier. Power levels, and number of identical units in a 256-element array are indicated.

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NOTES:

1. 6-BIT BEAM POSITION NUMBER OR 5-BIT LEVEL SELECT NUMBER OR START-STOP TIMED PULSE PAIR

2. 6-BIT BEAM POSITION NUMBER OR 5-BIT LEVEL SELECT NUMBER OR ANALOG GAIN CONTROL LEVEL

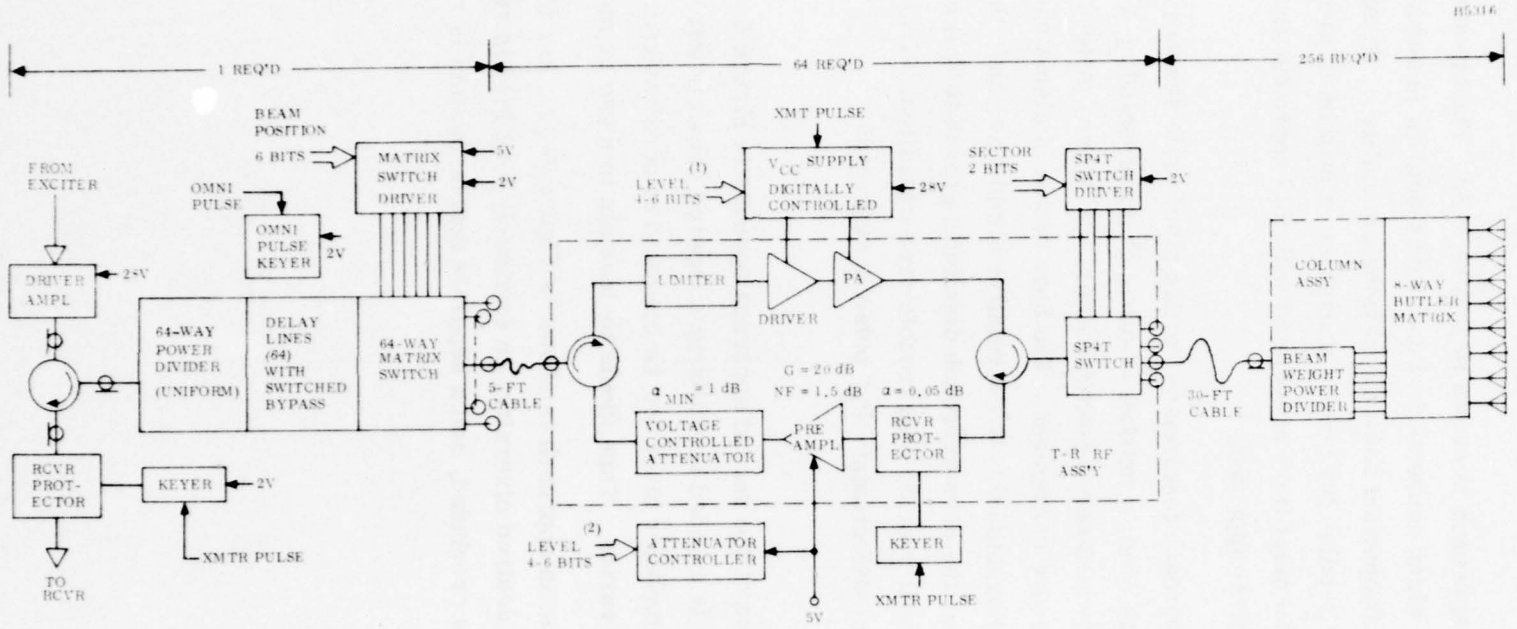
Figure 3-49. Delay-Bit Steered Cylindrical 1-64-256 Array, RF Block Diagram, Unattended Radar

An alternate approach is shown in Figure 3-50. The bit-steering is replaced by a switch matrix which connects 64 inputs to 64 outputs in sequence. A time-delay assembly provides broadband accurate phasing capability. To accommodate the omnidirectional "P_2" pulse for beacon operation, a method is provided for bypassing the delay lines. The amplifiers associated with this approach are essentially identical to that of the first approach.

The third approach features an "organ pipe" style scanner. This is shown in Figure 3-51. In this case, a number of other changes including a single transmitter and receiver, an amplitude-tapered power divider, and a horn instead of a Butler Matrix element assembly prove convenient. The horn option is also a candidate for all other cylindrical array alternates due to its relative simplicity, and, therefore, lost cost. In its simplest form, the horn approach disallows growth to 3-D operation. Proper mechanical design will provide long trouble-free operation. Note that an independent antenna for the omni-directional "P_2" pulse is suggested.

A modification of the second approach appears in Figure 3-52. The attenuator in the receive path is avoided by utilizing a tapered output power divider. The voltage controlled power amplifier must now be operated at constant gain and high efficiency as its drive power varies. This should be feasible in a two or more stage amplifier.

A frequency scan approach is shown in Figure 3-53. For four-frequency operation to provide the desired diversity, an extremely long feed is required. Independent frequency agility is precluded, and a separate beacon system is required.



NOTES:

1. 6-BIT BEAM POSITION NUMBER OR 5-BIT LEVEL SELECT NUMBER OR START-STOP TIMED PULSE PAIR

2. 6-BIT BEAM POSITION NUMBER OR 5-BIT LEVEL SELECT NUMBER OR ANALOG GAIN CONTROL LEVEL

Figure 3-50. Matrix Switched Cylindrical 1-64-256 Array

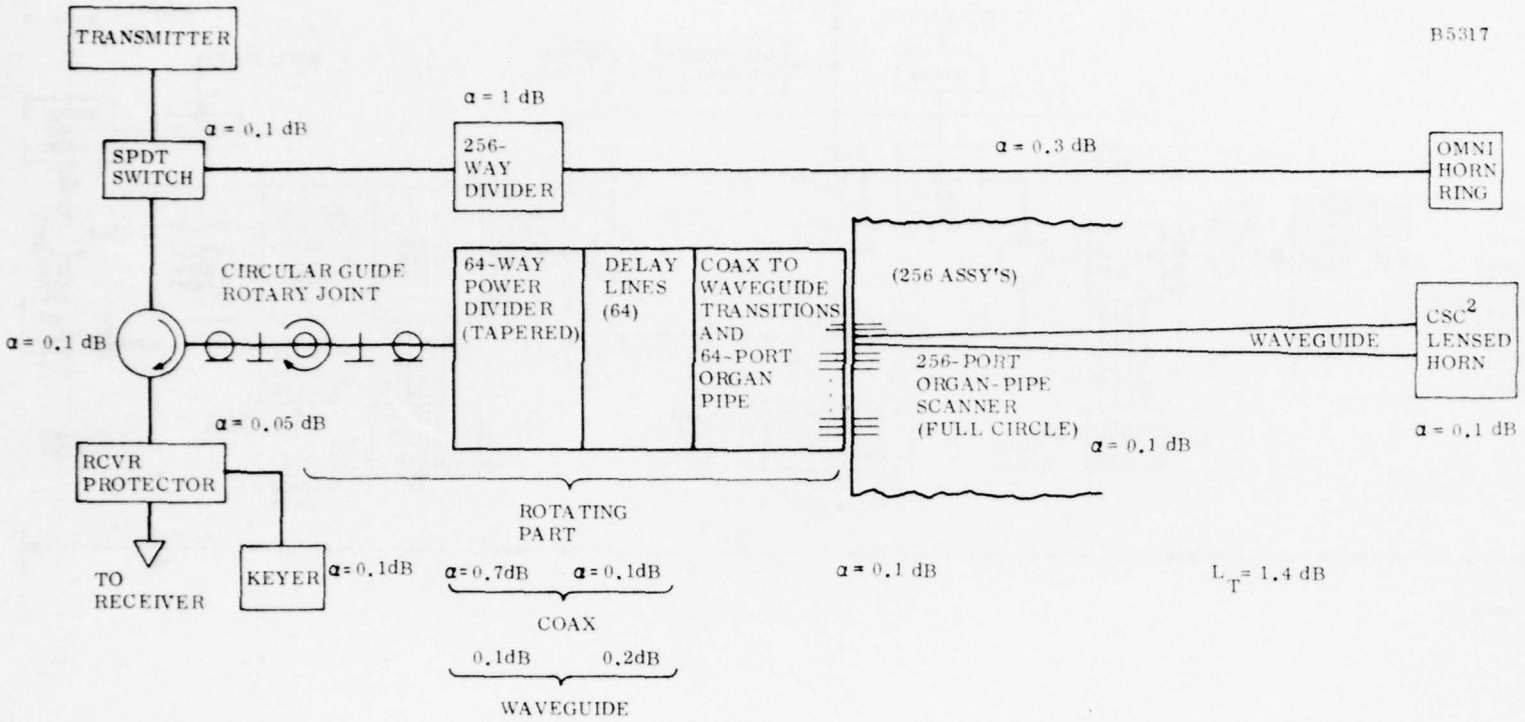
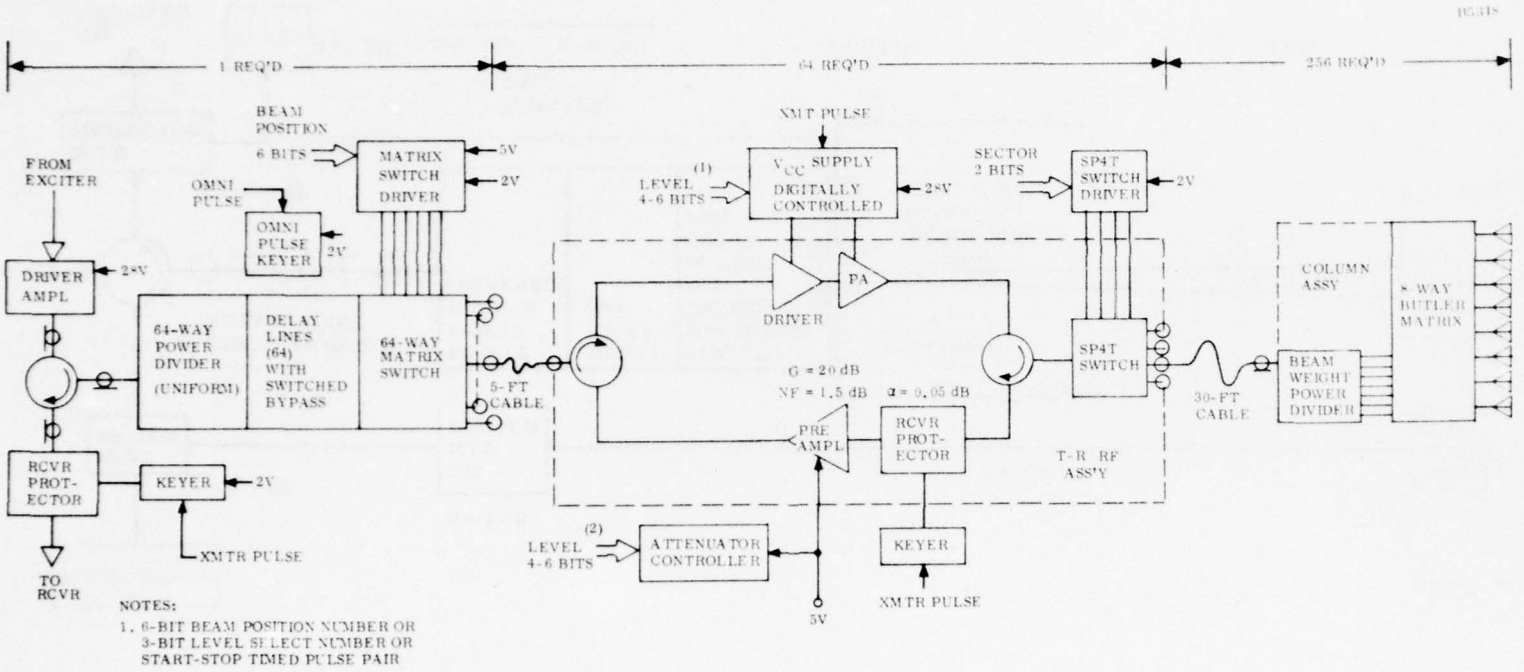


Figure 3-51. Organ-Pipe Scanner Cylindrical Array, RF Block Diagram, Unattended Radar



NOTES:
1. 6-BIT BEAM POSITION NUMBER OR 3-BIT LEVEL SELECT NUMBER OR START-STOP TIMED PULSE PAIR

Figure 3-52. Tapered Drive Matrix-Switched Cylindrical 1-64-256 Array, RF Block Diagram, Unattended Radar

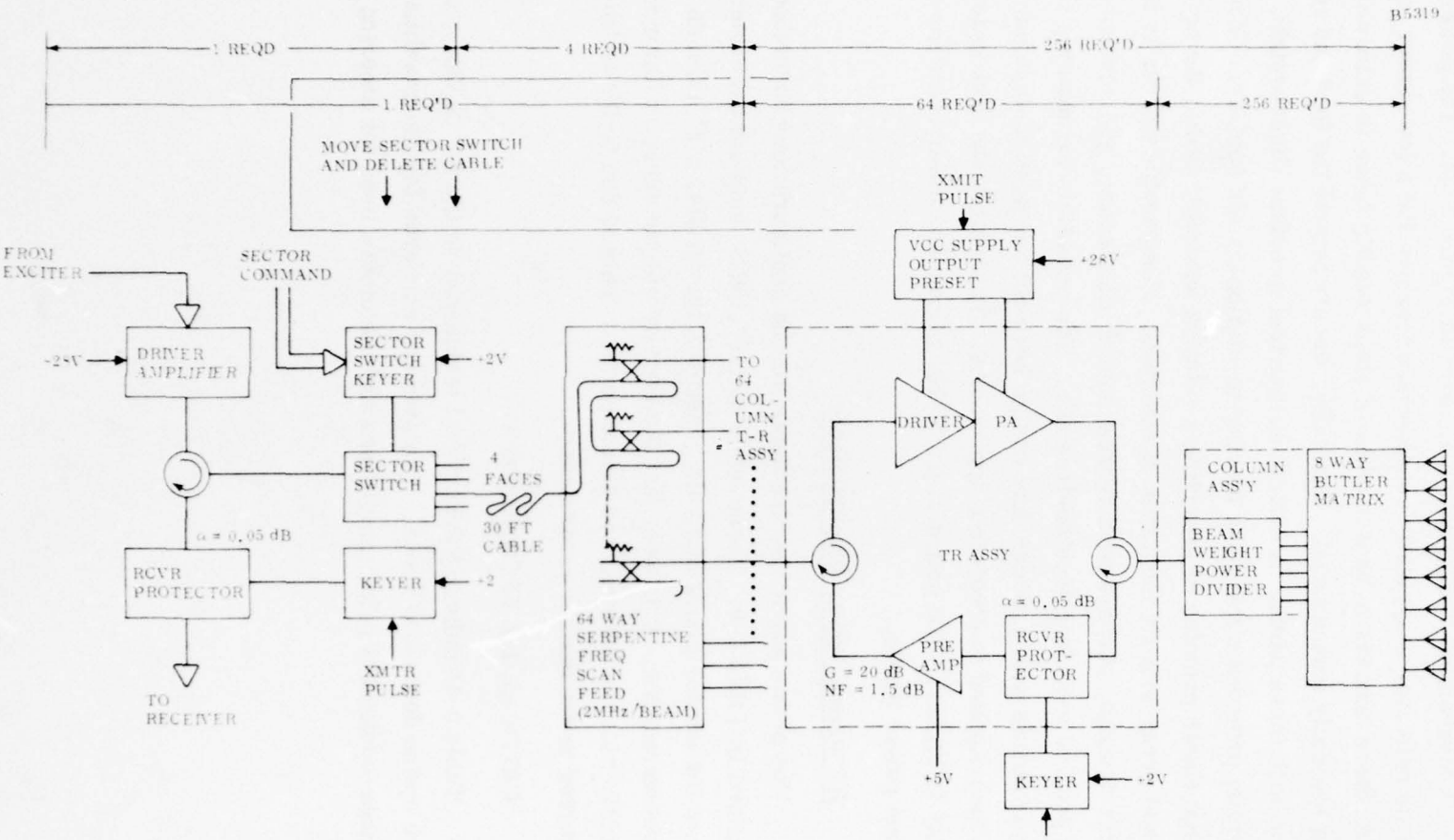


Figure 3-53. Frequency Scanner Planar Array, RF Block Diagram, Unattended Radar

A mechanical configuration appears in Figure 3-54. The power for rotation of a large reflector is typically considered excessive for a low-power installation. However, there appears to be a number of steps readily taken to eliminate the large wind drag normally encountered. Basically, the air around the feed and reflector must move with these parts. A smooth cylindrical interface (light-weight, low-loss radome) provides a low-drag moving-to-stationary air surface. Care in mechanical design shows promise of providing a rotating assembly within the power budget for a phased array with its multitude of switches. Comparable efforts in the bearing and motor designs, perhaps with routine annual maintenance and scheduled replacement, can provide very long trouble-free life. The potentials for meeting the power and life requirements with a mechanical design have not received the extensive study which has been applied to electronic approaches. Therefore, the risk in terms of uncertainty is higher. The potential payoff is, of course, lower costs for the very stringent prime power limits.

(1) RF Prime Power Requirements

The prime power requirements for the configurations described above are summarized in Table 3-9. These apply to 1.5° and 3° azimuth beamwidth L-band systems. From the sensor sizing analysis presented previously, a 3° azimuth beamwidth design is recommended. It is seen that the horn or simple array radiator approach significantly reduces the required prime power. This is due to the additional two-way loss incurred in the matrix array design.

b. CRITICAL RF TECHNOLOGY

Table 3-10 indicates the critical technology in the RF design area as a function of each option described above. The primary concerns for the baseline design are the voltage-controlled power amplifiers and the diodes used for steering and switching.

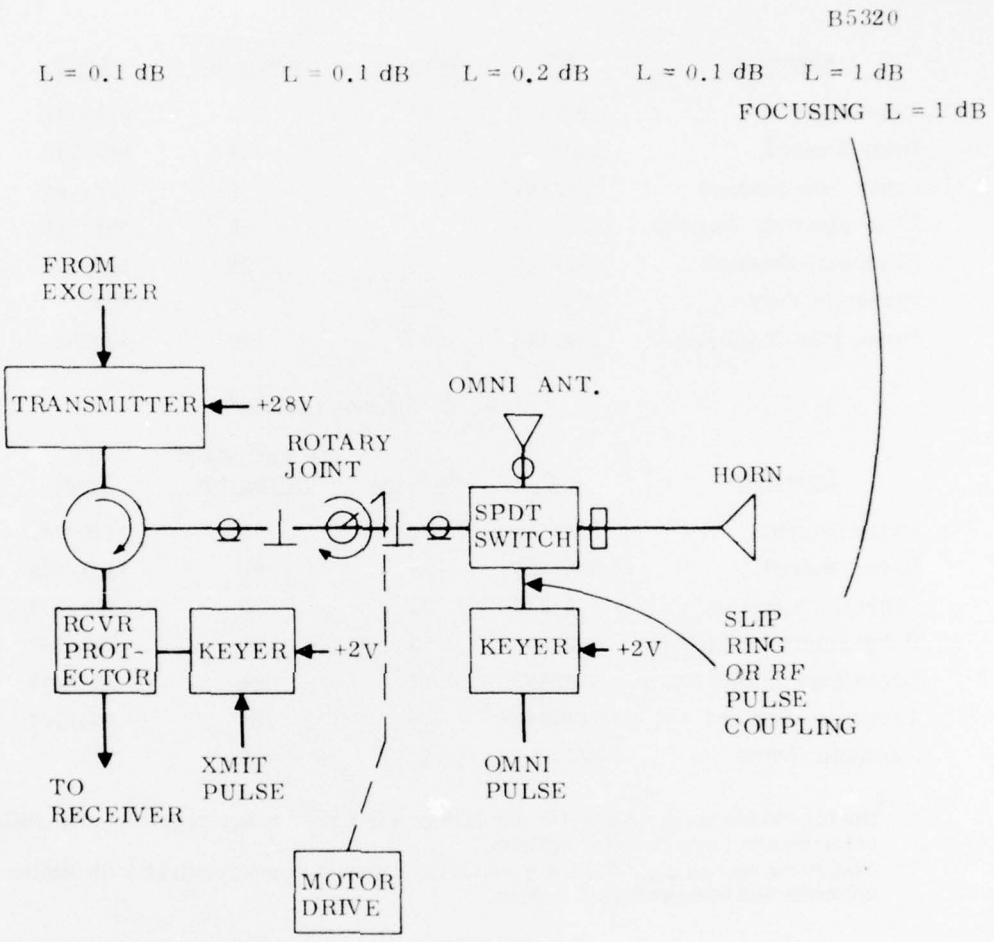


Figure 3-54. Parabolic Torus Mechanically-Scanned Antenna, RF Block Diagram, Unattended Radar

TABLE 3-9. DC POWER REQUIREMENTS L-BAND

a. 1.5° Antenna Options*

Approach	RF	Steering	Preampl and Attenuator	Total	IFF Capability
Phase Steered	293/185	51	179	523/315	Agile
Delay Steered	293/185	51	179	523/315	Agile
Organ Pipe Scanned	208/131	50	0	258/181	Uniform Scan
Delay Steered, Tapered	258/163	51	128	438/342	Agile
Frequency Scanned	225/142	0	128	353/270	Non-integral
Parabolic Torus	213	100	0	313	Uniform Scan
Organ Pipe, Tapered	252/159	50	128	430/337	Uniform Scan

b. 3° Antenna Options**

Approach	RF	Steering	Preampl and Attenuator	Total	IFF Capability
Phase Steered	990/625	25	90	1105/740	Agile
Delay Steered	990/625	25	90	1105/740	Agile
Organ Pipe Scanned	703/445	25	0	728/470	Uniform Scan
Delay Steered, Tapered	803/508	25	64	892/597	Agile
Organ Pipe, Tapered	784/496	25	64	873/585	Uniform Scan
Frequency Scanned	700/443	0	64	764/507	Non-integral
Parabolic Torus	663	50	0	713	Uniform Scan

* Double values (e.g., 523/315) indicate prime power range required with Butler matrix array columns and horn radiator options.

** Double values (e.g., 1105/740) indicate dc power range required with Butler matrix array columns and horn radiator options.

TABLE 3-10. RF TECHNOLOGY DEVELOPMENT STATUS

DEVELOPMENT EFFORT / APPROACH	VOLTAGE CONTROLLED POWER AMPLIFIER	LOW-LOSS LOW-POWER SWITCHES	ORGAN-PIPE SCANNER	FREQUENCY SCAN LABYRINTH	REFLECTION-TRANSMISSION GRID
PHASE STEERED	✓	✓			
DELAY SWITCHED	✓	✓			
ORGAN PIPE SCANNED			✓		
FREQUENCY SCANNED	✓	✓		✓	
PARABOLIC TORUS					✓

The power amplifier concerns center on the need for voltage control to effect a taper on transmit. Alternates to this include relief from the requirement for transmit sidelobe suppression and including resistive tapering and/or phase tapering on the antenna side of the transmit module. The first alternate should be reasonable considering the remote application but was not available as an option in this design effort. If available, it would result in elimination of the power amplifier concern. The second alternative, weighting on the element side of the power module, was not included due to the increased loss and the resulting prime power penalty.

The diode switch concern again is focused by the prime power concern both in terms of low loss and low power. These concerns would also vanish if the prime power constraint was relieved. With emphasis on prime power, it becomes imperative to utilize the lowest-loss lowest-cost switches available that satisfy the reliability concerns.

(1) Power Amplifiers Technology

Power amplifiers for the L-band radar and integral SIF/IFF require operation at 1030 MHz and across the 1215- to 1400-MHz band. Amplifiers in the 50- to 100-W power range are being produced or designed now for the radar band. The extension to 1030 MHz in the same circuit is not normally done. One amplifier, a driver replacing a traveling wave tube in General Electric's long-range HIPAR 2-D radar equipment has been built and its performance measured. Figure 3-55 shows the results. This 50-dB gain, 4.5-W nominal output amplifier meets the frequency-bandwidth requirement, but is a Class A device with low efficiency. Another L-band amplifier, made for the Naval Air Defense Center, appears in Figure 3-56. It provides 6- to 8-W output with 50 mW drive, at a 10-percent duty cycle, with a short or long pulse. Its nominal frequency range is 1200-1400 MHz, and provides some gain and output at 1030 MHz. A broadband solid-state amplifier is currently being developed for Lincoln Laboratories by General Electric. From this experience base GE is confident that an efficient amplifier can be made for the required frequencies and the required 10- to 15-W peak power output per column T/R modules.

The output of each amplifier must be adjustable downward from the maximum value for a range of about 20 dB to provide the desired illumination taper for sidelobe control. This can be accomplished by changing the supply voltages. Figure 3-57 presents the results on an existing one-stage amplifier with constant drive. Feedthrough limits the minimum output, with a minimum effective gain of about -4 dB.

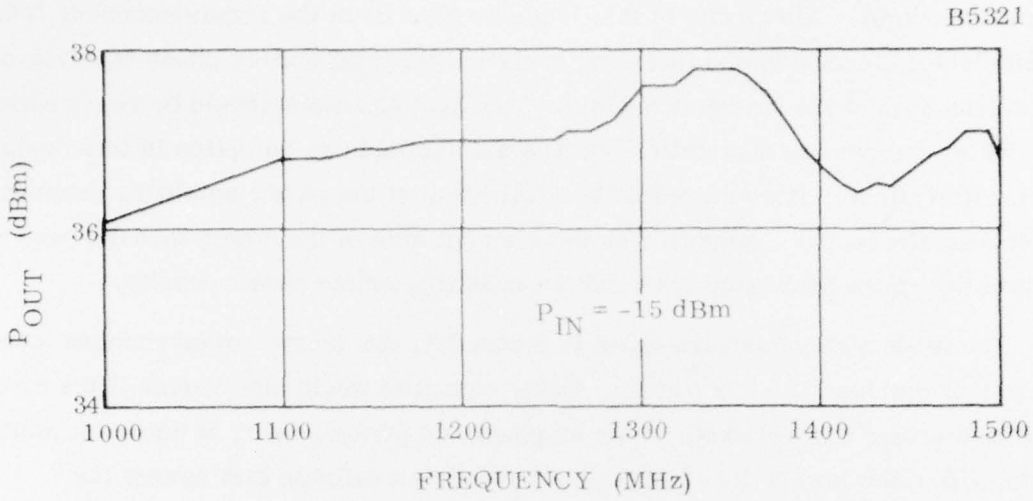


Figure 3-55. Solid-State 4.5 W Amplifier Chain

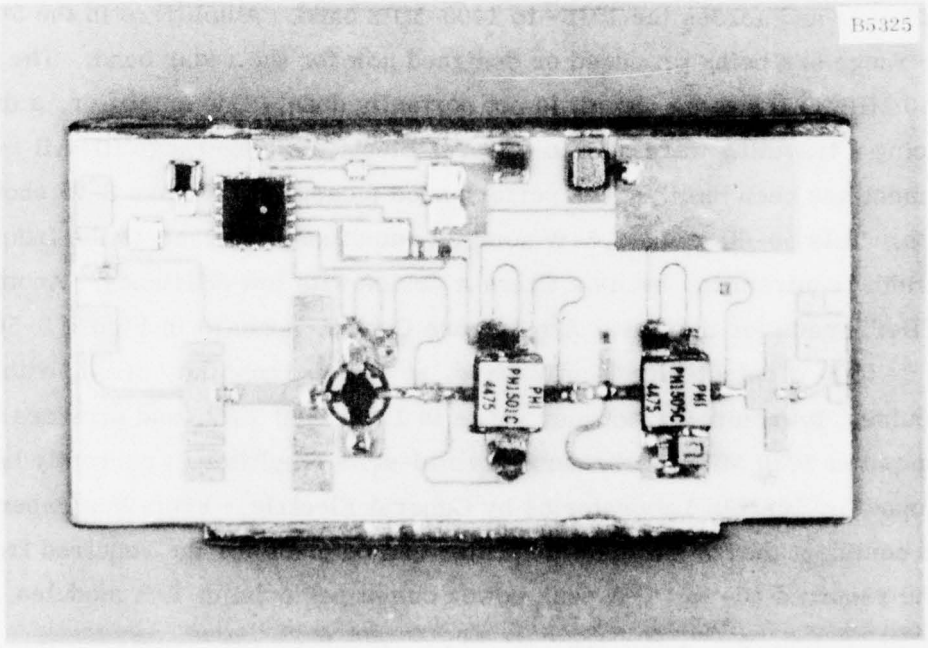


Figure 3-56. 8-W L-Band Amplifier Made for NADC

Two stages cascaded would provide the full 20 dB required range of outputs with a constant input, or with somewhat different voltages, it would provide the desired output with an effective "constant gain" from a tapered drive. The amplifiers for this service will require extra care in the design of the circuitry to avoid detuning as the applied collector voltage changes. The collector-voltage-controlled amplifier permits reasonable efficiency to be maintained over a wide range of output power.

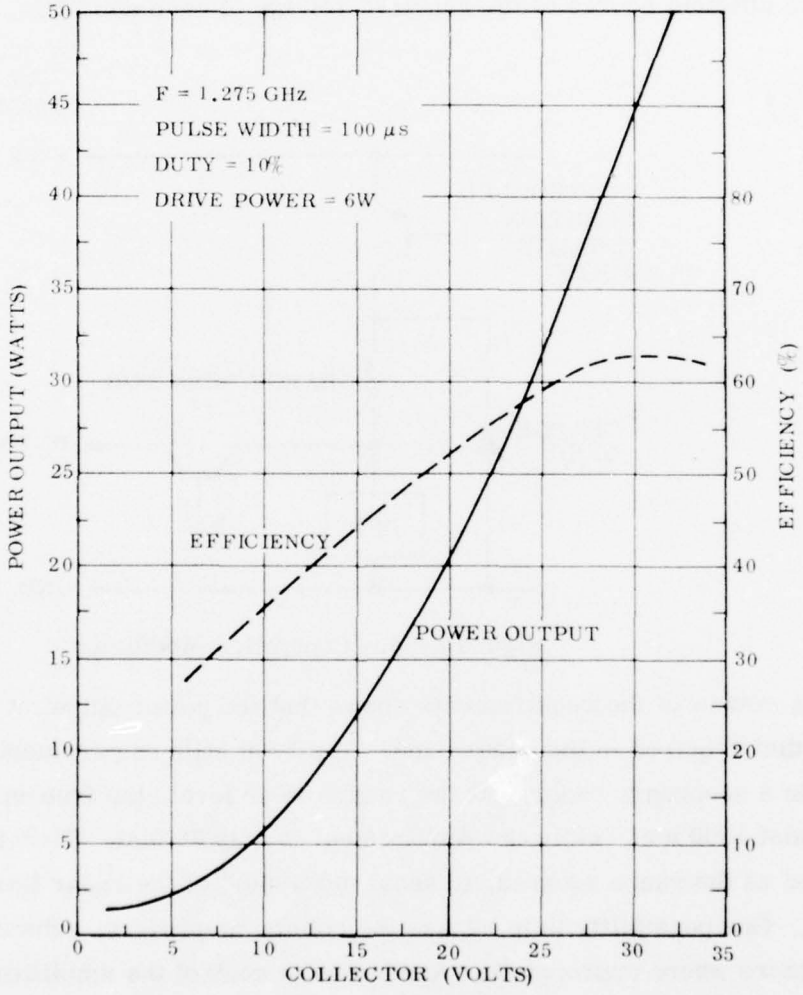


Figure 3-57. Voltage Controlled Power Amplifier Performance

Attaining a controlled collector voltage efficiently is necessary if overall efficiency and low total power drain is to be attained. Switch regulated power supplies provide one possible approach, but switch controlled resonant-charged line modulator should be the most efficient approach. A simplified circuit appears in Figure 3-58. Conceptually, the switch permits a start of a resonant charge until the required energy has been supplied to the inductor and the capacitance of the pulse line. The switch is then turned off, and that part of the energy in the inductor is transferred to the line. The energy is held until the transmitter is operated. The energy, and therefore the line voltage, is controlled by the time the charging switch is turned on. This should form an efficient source of the required voltage of each amplifier.

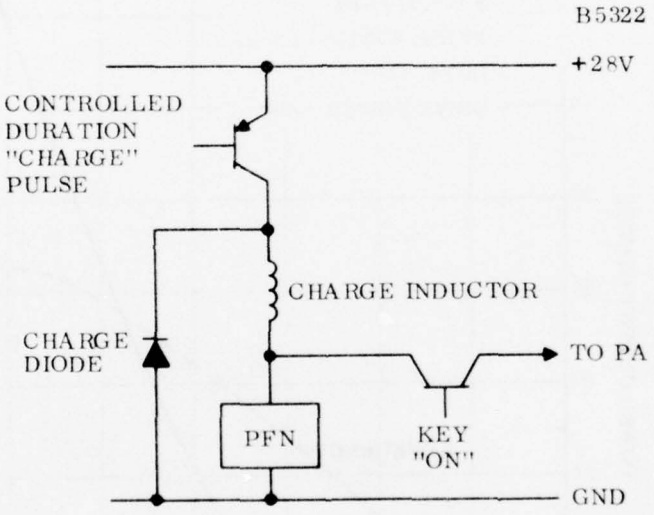


Figure 3-58. Controlled Modulator

A review of the requirements shows that the power output at 1030 MHz can be far below that required in the radar band. The 1030 MHz requirement is for an interrogator in a secondary radar. At the radar power level, the free-space range would be almost 1500 nmi, while the requirement is only 60 nmi. Thus the power can be reduced as the range squared, to about $(60/1500)^2$ of the radar level, or 28 dB less power. One possibility is to bypass the column amplifiers, substituting controlled attenuators where appropriate. Another is to control the amplifier amplitude and phase, but at a much lower gain, at the beacon frequency.

Another possible configuration would include a switched tuning element in the amplifier to establish proper impedances at the active devices on the beacon frequency

(when the equipment is operated as a beacon), while normal operation would provide uniform coverage of the 1215-1400 MHz radar band.

Each of these alternatives is considered feasible. The selection of the optimum approach will require some further system design maturation. The broadband amplifier imposes the fewest restrictions on the system design, but requires the most development effort. The switched tuning element will require less development, but requires an additional control. The switch bypassing the power amplifier introduces additional losses before and after the power amplifier, requiring more power in the nominal radar mode of operation, but requires the least development. It also is more easily implemented with a tapered-drive system than with a uniform drive system, and establishes the minimum drive level to be supplied to the power amplifiers as that required for beacon operation. (This is considered not to be a serious limitation).

There appears to be at least three alternatives in providing both beacon and radar operation in the same equipment. All are deemed feasible, and all require some development effort.

(2) Switch Technology

A major power consumer in each of the electronically scanned arrays in the myriad of switches required. The typical "on" current for each diode of a switch is more than 25 mA, to perhaps as high as 100 mA for lower diode loss. Existing driver circuits typically have not been designed for lower power drain. The power required is not an important design consideration since the total required has been small compared to the typical total system power. The unattended radar power limitations requires that great weight be given to both diode loss and control power in the design optimization.

There are basic semiconductor limitations which will probably preclude a major reduction in switching power into a diode at a desired RF power and impedance level. Some improvements should be possible by tuning out the shunt capacitance which limits available isolation, and by including switching time of the diode in the specification and selection process. The switch for the unattended radar requires careful selection of switching time, allowed loss and isolation to permit minimization of the diode losses and operating current.

The isolation provided by a single diode is typically about 20 dB at L-band, limited to this value by the inherent shunt capacitance of the diode. Higher isolation is unusually attained by cascading diodes. This increases the RF loss and the control power required. The isolation can be increased by tuning out the capacitance with a shunting inductor. This increases isolation over a limited bandwidth from 20 dB to 40 dB over a 10-percent band, and from 20 dB to 30 dB over a 30-percent band. The difference can be significant in this application.

The drive circuits typically utilized include a provision for removing stored charge keyed by the diode drive transistor, as in Figure 3-59. The self-driving circuit avoids extra control circuitry. It increases the voltage drop in the diode switching circuit. Current-control resistors are also included, making the circuit suitable for operation from a +5 V available source. The self-driving turn off circuit also shunts the diode, requiring a small additional current. These features can be changed to a different "turn off" circuit, with reduced voltage drops and slightly less current from the supply for the same diode "on" current. A +2 V supply at the same current will reduce the required power by 60 percent. Where possible, the turn off circuit should be eliminated and the diode be allowed to recover by recombination. For submicrosecond switching, as for the "P_2" pulse in the IFF/SIF mode, this circuit is probably required. In normal radar operation it should not be needed. The turn off circuit might be externally controlled, so that it draws power only when "P_2" is required. The steps noted should permit the power required for each diode switch to be kept below 100 mW.

5. IF DESIGN

The IF portion of the radar design consists of the exciter, waveform generator, and receiver. The exciter, along with the waveform generator, develops the waveform modulations to be transmitted and timing signals required throughout the radar. The receiver processes the RF signal by mixing it down to IF, amplifies the result and finally converts it to a video in-phase and quadrature signal by synchronous detection. IFF signal generation and processing will be accomplished in the same exciter and receiver as used for radar signals, sharing common hardware wherever possible to minimize power requirements.

The exciter will generate in the transmit mode a Linear Frequency Modulation (LFM) pulse at one of eight selectable L-band agile frequencies for radar transmission, or a Continuous Wave (CW) signal at 1030 MHz along with three gates of 0.8-μs

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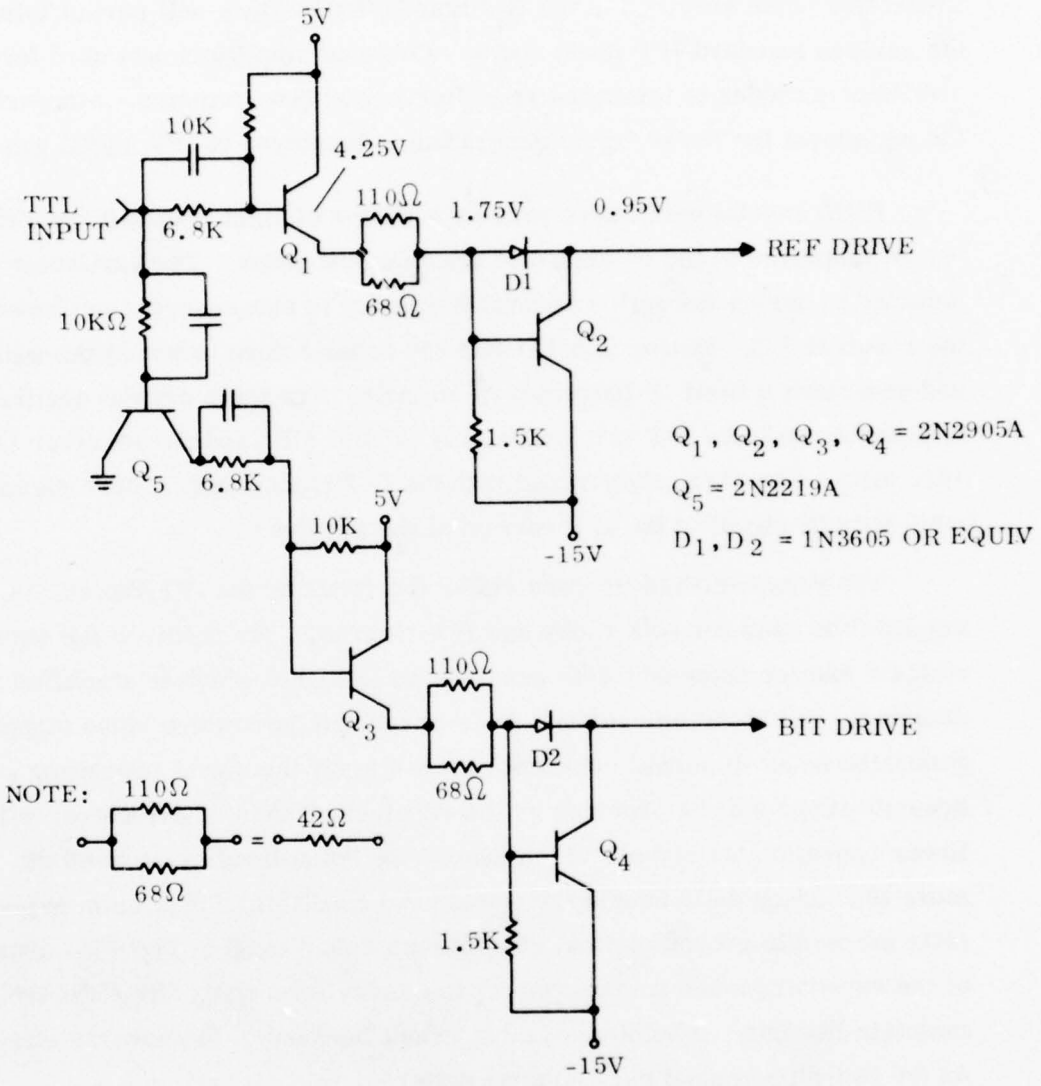


Figure 3-59. Typical Driver Circuit

duration for IFF interrogation transmission. In the receive mode, the exciter will generate an appropriate radar Local Oscillator (LO) frequency used to remove the agile frequency from the return signal, and provide an IFF LO for IFF/SIF replies. Controlled pulse spacings in the IFF transmission mode will permit interrogation of the various standard IFF mode codes. Common amplifiers are used for both transmit and receive modes to minimize amplifier power requirements. Similarly, much of the equipment for radar signal generation is employed in IFF signal generation.

Eight crystal oscillators provide a choice of eight transmit frequencies which can be employed at the command of the data processor. The particular oscillator selected to derive the agile transmit frequency is subsequently employed to make up the receiver LO. Mixing this LO with the radar return removes the agile frequency and generates a fixed IF frequency of 80 MHz. The ninth crystal oscillator is used to generate both the IFF transmit signal of 1030 MHz and the receiver LO, also of 1030 MHz. This LO, when mixed with the IFF transponder return signal, generates a 60-MHz IF signal in the IFF portion of the receiver.

The receiver shall process either the radar or the IFF return. A common RF amplifier is used for both radar and IFF returns. The received RF signal is mixed with the exciter supplied LO to generate an IF signal which is amplified and envelope detected. For the radar return, an in-phase and quadrature video signal shall be generated so as to permit coherent processing by the signal processor. A 60-dB dynamic range will be provided by the receiver; that is, the receiver will maintain linear operation for signals which exceed the noise level by up to 60 dB. This is more than adequate to handle the worst case condition of maximum expected clutter (84th percentile ground clutter) at minimum radar range. The wide dynamic range of the receiver makes it unnecessary to employ Sensitivity Time Control (STC) to maintain linearity, a highly desirable result because of the adverse effect of STC on the two-dimensional $\csc^2$ antenna patterns.

a. EXCITER

The exciter functional schematic is shown in Figure 3-60. The stable local oscillator (STALO) frequency is 80 MHz. The STALO is a state-of-the-art oscillator design which has been used in several high-performance, high-reliability applications including the Systems Technology Radar (STR) radar. A graph of the measured short-term stability is shown in Figure 3-61. The short-term stability after frequency

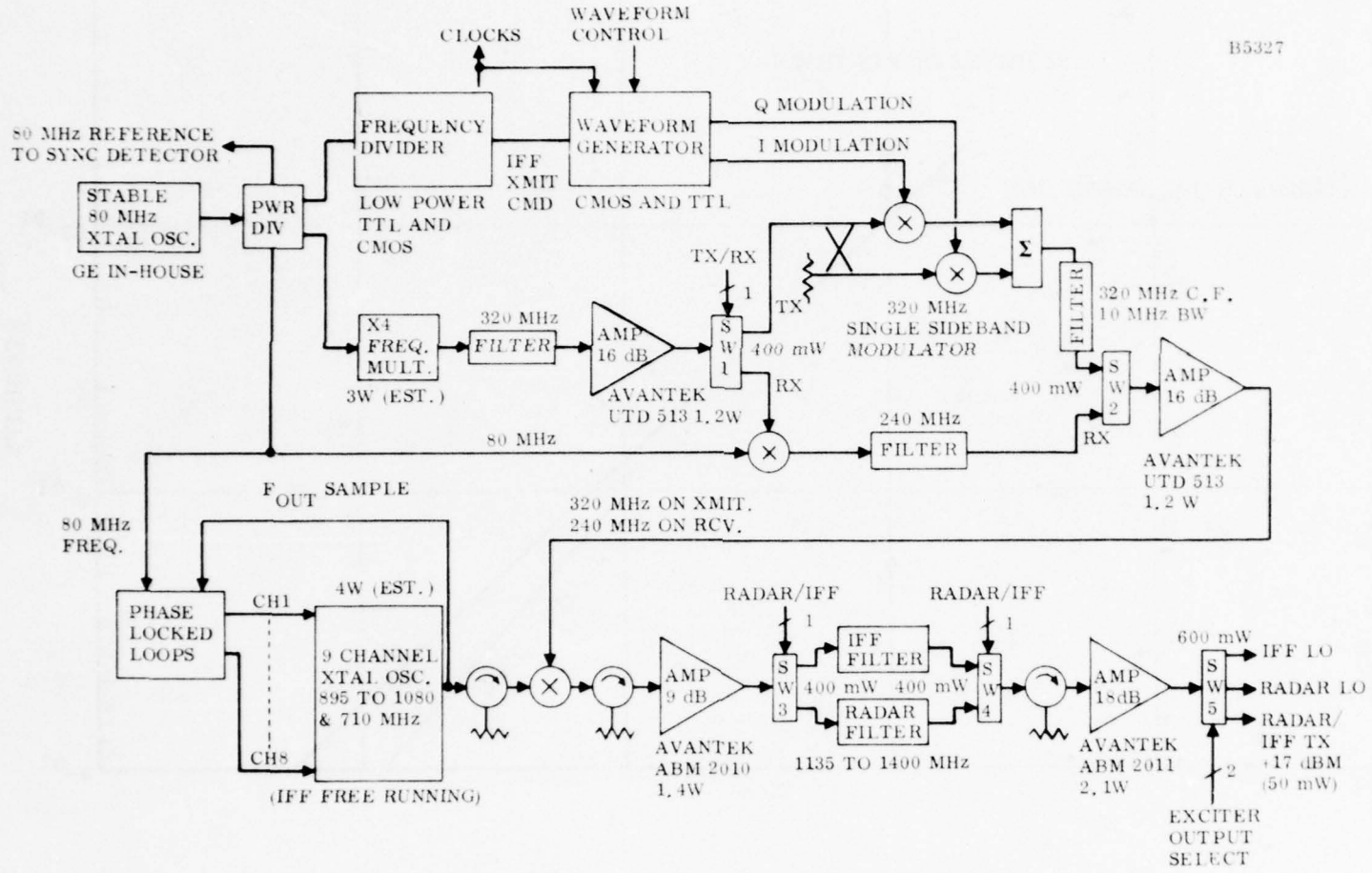


Figure 3-60. Exciter Waveform Generator

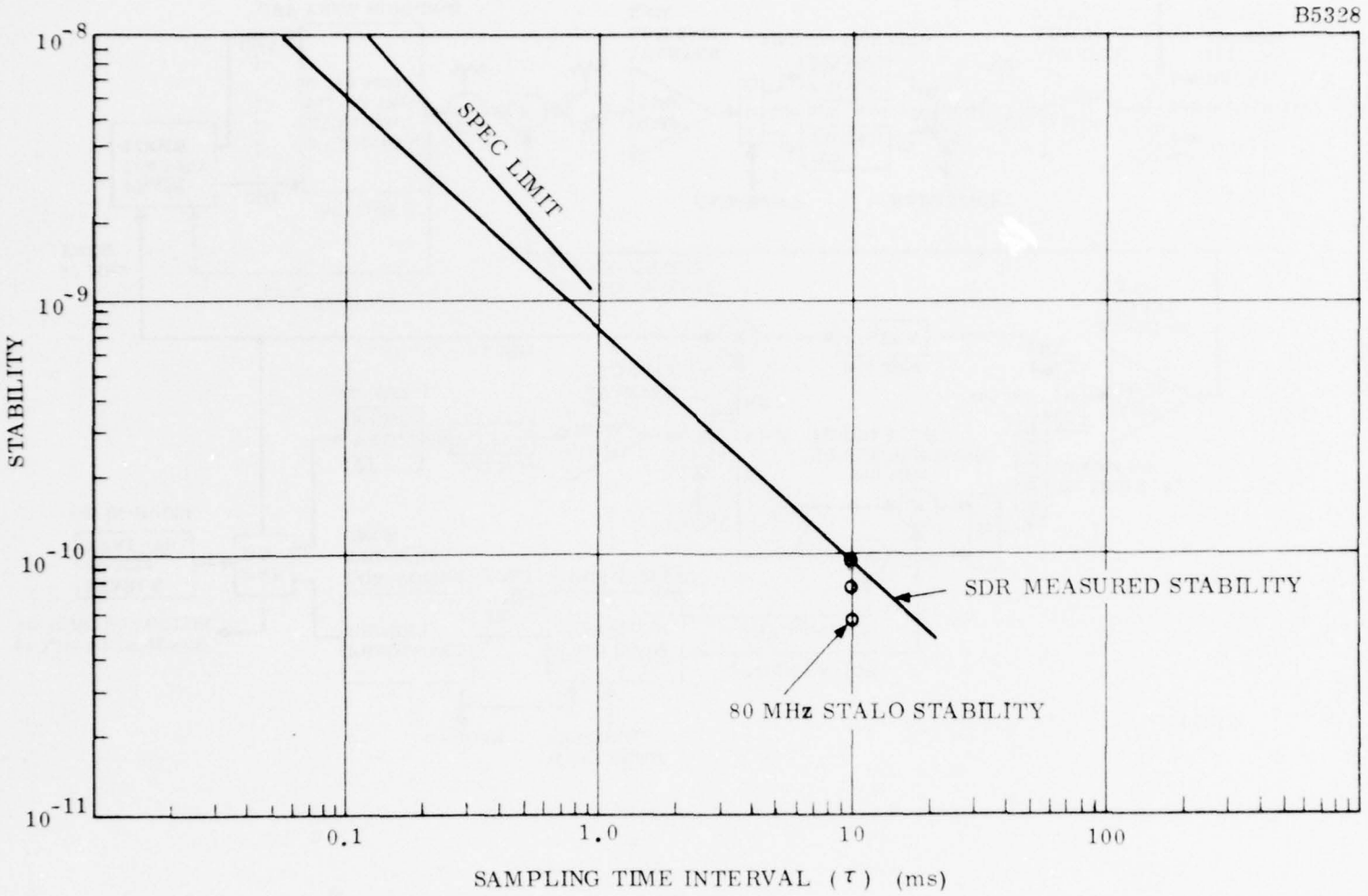


Figure 3-61. Measured Short-Term Frequency Stability of 80-MHz STALO

multiplication to 320 MHz will be better than 4 parts in 10^9 in a 1.0-ms sampling interval.

The times four frequency multiplier is a cascade of two frequency doublers with an interstage bandpass filter and power amplifier. A bandpass filter at the output is coupled to a power amplifier.

The exciter in Figure 3-60 performs as follows. The 320-MHz output from the frequency multiplier and power amplifier is applied to an RF switch. In radar and IFF transmit as well as the IFF receive mode, the 320-MHz LO signal is applied to a single-sideband modulator composed of a quadrature coupler, two double balanced mixers and an in-phase power combiner. A 320-MHz bandpass filter with a 3-dB bandwidth of 10 MHz (to accommodate the IFF pulse requirements) is used to couple the single-sideband modulator output to the complementary port of another RF switch.

In radar receive mode the RF switches mentioned above switch to their fail-safe position (in which no power is dissipated by the switch). This applies the 320-MHz frequency multiplier output to a double balanced mixer which also has the 80-MHz STALO as an input. The difference frequency is selectively filtered by a 240-MHz bandpass filter which rejects the 320 MHz by more than 60 dB.

The 240-MHz radar receive LO signal and the 320-MHz radar transmit, IFF transmit (and receive) LO signals are amplified in a common power amplifier and applied to a double-balanced mixer. An isolator couples frequencies from a 9-channel oscillator to the other input of the double-balanced mixer.

The 9-channel oscillator consists of 8 voltage-controlled crystal oscillators locked to the 80-MHz STALO frequency in a phase-locked loop. The 8 voltage-controlled crystal oscillators are arranged in two groups of four with a frequency difference of 50 MHz between adjacent channels in each group. The oscillator frequencies are between 895 MHz and 1080 MHz. Only one oscillator is selected at a time to conserve power. A common heater assures frequency tracking with no warm up.

The ninth oscillator is a free-running crystal oscillator at a frequency of 710 MHz which is used to generate the final IFF transmit and receive LO frequencies.

The output of the double-balanced mixer is isolator-coupled to a power amplifier which is used in both transmit and receive LO generation to conserve power.

A pair of RF switches and two bandpass filters are used to filter the radar and IFF transmit and receive LO signals. Two bandpass filters are required to avoid image frequencies.

An isolator and power amplifier are used at the common output of the RF switch to provide the required output levels. The power amplifier is common to the transmit and receive frequency generation function to conserve power. An RF switch following the power amplifier selects the proper path for the generated RF frequencies.

The frequency divider, which is a module of the exciter shown in Figure 3-60, generates all required system clocks as well as transmitted gates for generating the various IFF transmit interrogation codes. A functional schematic of the frequency divider is shown in Figure 3-62.

b. WAVEFORM GENERATOR

The waveform generator is also a module of the exciter shown in Figure 3-60. A functional schematic of the waveform generator is shown in Figure 3-63 and performs as follows.

The address counter, an 8-bit CMOS binary counter provides the address locations for the 64-bit by 8-bit CMOS Read-Only Memories (ROM's). Each ROM contains stored values of the in-phase (I) and quadrature phase (Q) samples of the Bandwidth Time (BT) 32 LFM waveform. The counter cycles through one complete sequence of address locations each time the LFM waveform is required.

The output of the CMOS ROM's is applied to DATEL DAC F18B 8-bit Digital-to-Analog (D/A) converters which are clocked at 500 kHz. The D/A converter current source outputs are converted to voltage outputs by high speed IC operational amplifiers (DATEL AM-103) which are referenced to the internal reference voltage of the D/A converters for precise temperature tracking. A gain control is provided for amplitude matching of the I&Q modulating signals. The output of the operational amplifiers is sufficient to drive the double-balanced mixers in the exciter while overcoming losses due to impedance buffering and filtering.

The low pass filters following the operational amplifiers provide rejection of the aliasing terms appearing in band due to discrete time sampling at twice the Nyquist

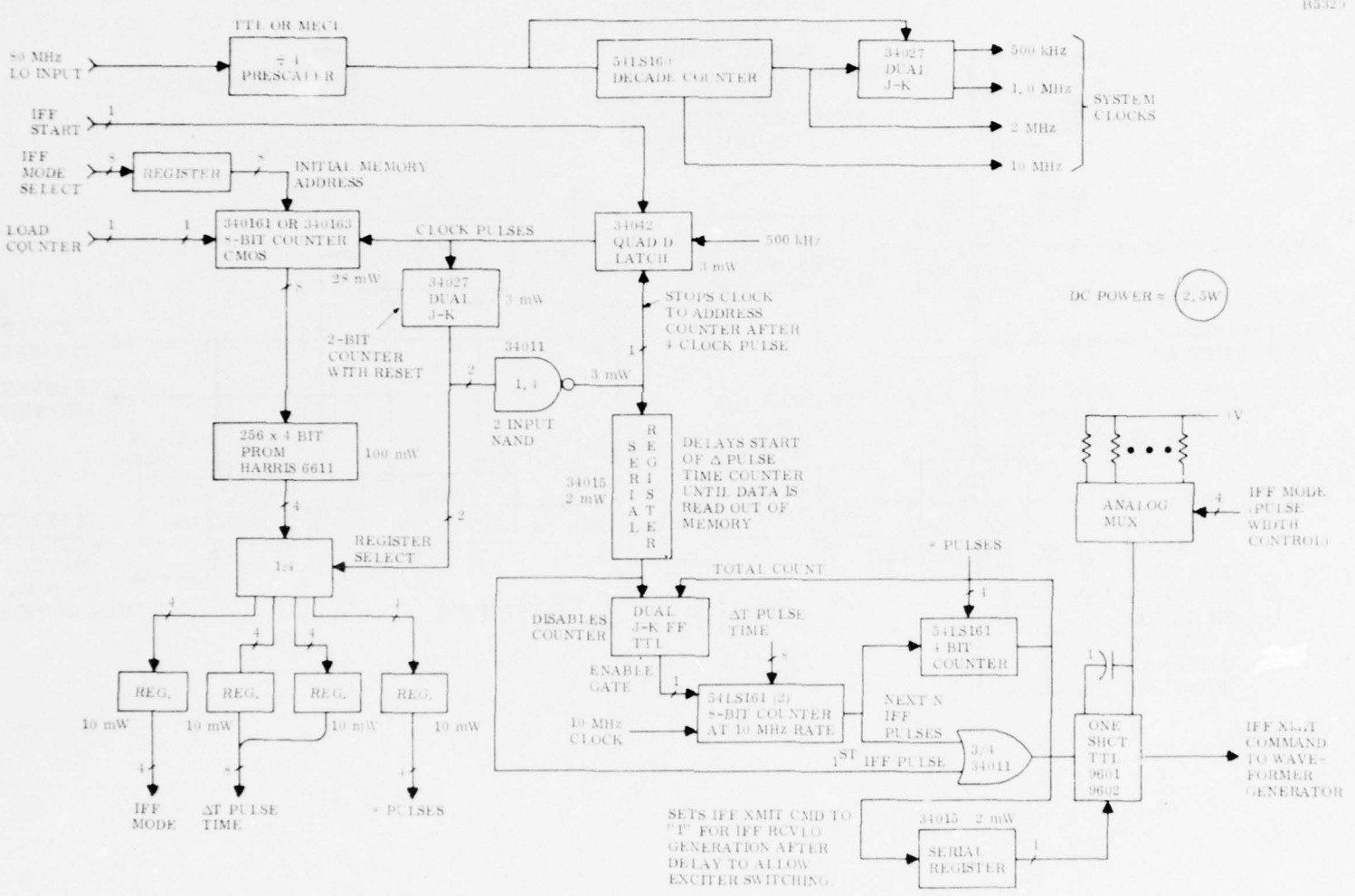


Figure 3-62. Frequency Divider/IFF Transmit Pulse Generator (Part of Exciter/Waveform Generator)

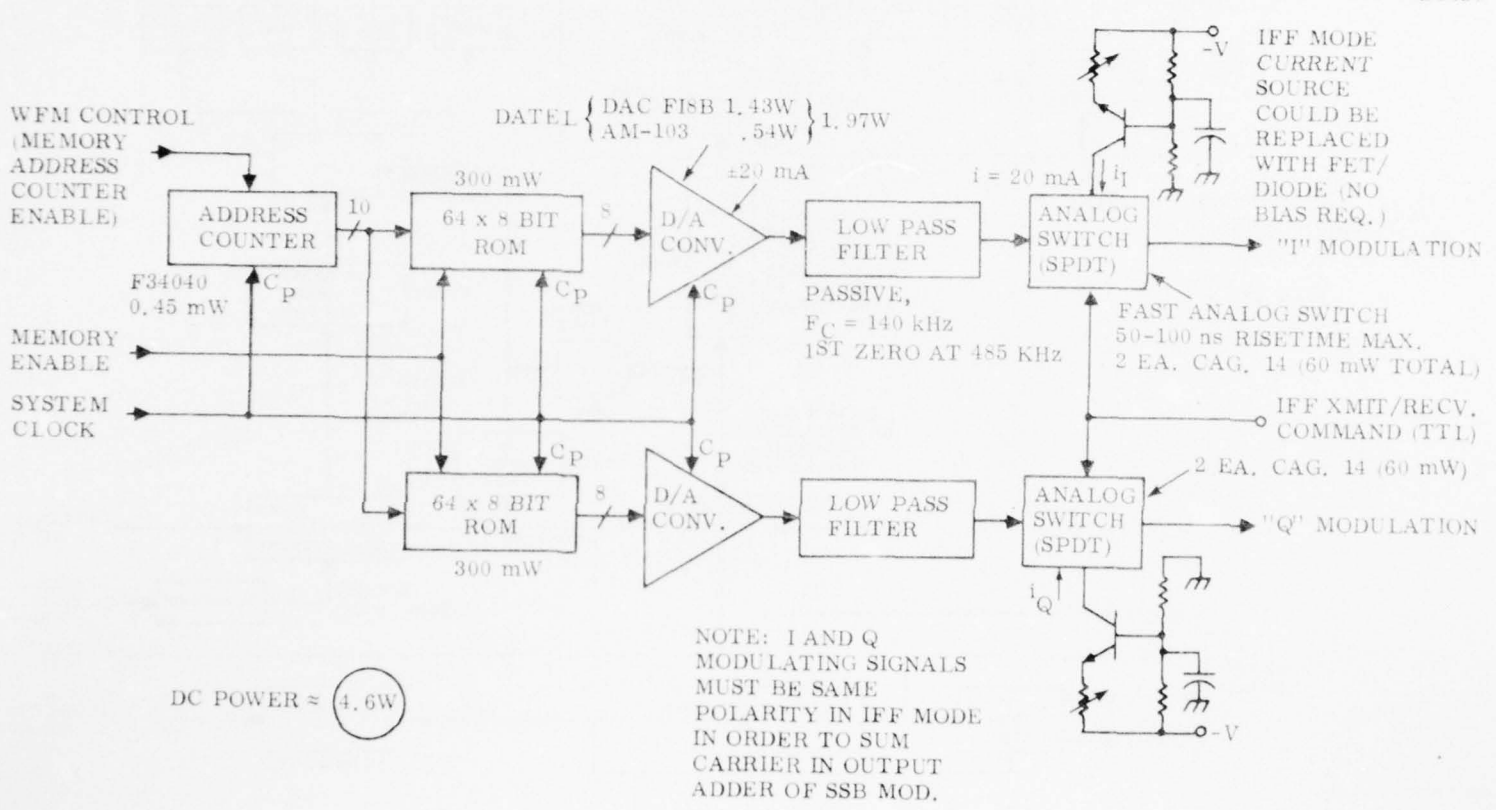


Figure 3-63. Unattended/Minimally Attended Radar Waveform Generator

rate. The filters are passive with an inverted Tchebyscheff response. This filter type allows superior flat amplitude and group delay characteristics in-band while also providing arbitrary zeroes of transmission in the stop band. The ultimate rejection will be approximately 52 dB with transmission zeroes placed near 425 kHz and 575 kHz (a natural "zero" occurs at 500 kHz due to the first order hold effect of the D/A converter sampling).

The low pass filter outputs are applied through high speed Field-Effect Transistor (FET) analog switches (Crystalonics CAG14) to the double-balanced mixers in the exciter. The high speed analog switch provides, in one position, the phase modulation for generating the LFM pulse. In the other position of the switch, a constant I&Q bias is output to the exciter to generate the CW signal used in the IFF mode for pulsed transmission and for the IFF receive LO. Balanced current sources in the switched arm provide the necessary dc bias to the modulating input of the double-balanced mixers.

The analog switches are controlled by commands from the IFF waveform generation circuitry which contains less than 25 CMOS IC's under the control of the data processor. Mode control inputs determine pulse widths and time between pulses. Less than five TTL IC devices are used in the frequency divider and IFF waveform generator.

c. RECEIVER AND SYNCHRONOUS DETECTOR

(1) Primary Radar

The primary radar receiver and synchronous detector functional schematics are shown in Figures 3-64 and 3-65, respectively. Inputs from the receiver protector are applied to a Performance Monitor/Fault Location (PM/FL) coupler. A low noise solid-state amplifier provides 20-dB gain for both IFF and radar IF sections and essentially establishes the system's noise temperature. An isolator-coupled frequency diplexer provides selectivity for the IFF and radar and allows a common low noise amplifier to be used for both radar and IFF receivers.

The radar output frequencies from the frequency diplexer are isolator-coupled to a high level double-balanced mixer which has an LO input drive level of 17 dBm. The LO frequency on receive is 80 MHz below the transmitted frequency. A PM FD/L coupler is placed ahead of the radar IF bandpass filter (an LC narrowband filter with about 4 dB insertion loss). The noise level output of the narrowband filter is approximately -92 dBm (noise power in a 280-kHz bandwidth).

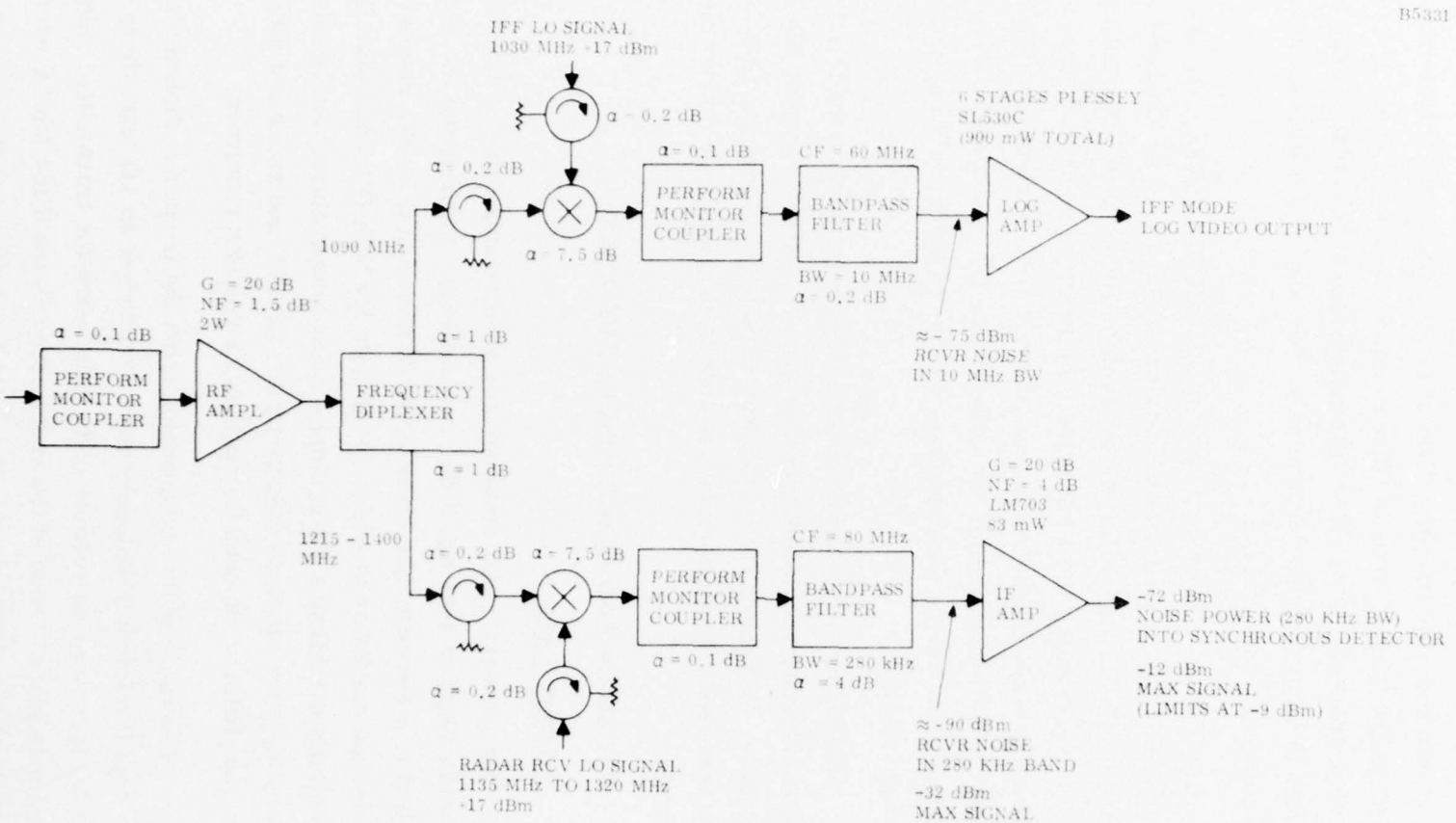


Figure 3-64. Unattended Radar Receiver

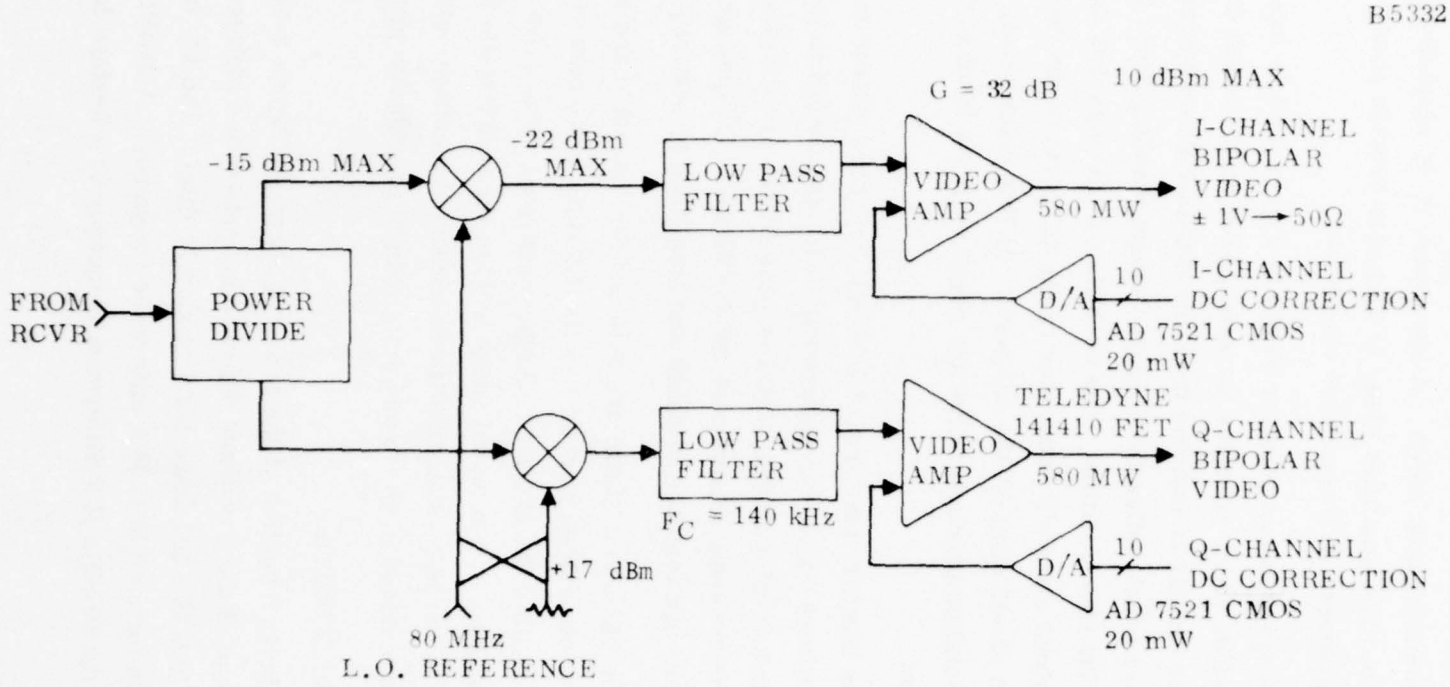


Figure 3-65. Unattended/Minimally Attended Radar Receiver Synchronous Detector

The IF amplifier section of the radar receiver will provide a minimum of 60-dB instantaneous dynamic range. A low-power IC IF amplifier (LM703) gives 20-dB of linear gain. The amplifier stage is biased to provide phase stable amplitude limiting to prevent severe A/D converter overdrive.

The synchronous detector shown in Figure 3-65 is input through an in-phase power divider which provides an equal power split to each double-balanced mixer. The power divider is isolated from the double-balanced mixers through 3-dB attenuators which buffer the IF port Voltage Standing Wave Ratio (VSWR) and improve the I&Q isolation. The 80-MHz STALO signal is applied through a quadrature hybrid and 3-dB attenuator to the LO ports of the double-balanced mixers at a level of +17 dBm (at the LO port). At this drive level, these mixers assure intermodulation products below the receiver noise level at the input to the video amplifiers.

The bipolar video from the double-balanced mixers is filtered by low pass passive filters which are buffered by 3-dB attenuators to provide a good match to the IF port of the mixers. The low pass filters are a Butterworth type which provide greater than 60-dB rejection of the 80-MHz STALO leakage terms from the mixers. The filters are matched in phase and amplitude to assure proper I&Q channel tracking.

The video amplifiers are selected for low noise and will provide at least ±1.024 V into a 50-Ω load across the 125-kHz video bandwidth. A dc offset correction loop within the signal processor assures a zero-mean noise level by averaging noise samples in a selected range window on a PRF basis and correcting the dc components in the I&Q video amplifiers through a feedback network. The video amplifiers are also matched in phase and amplitude to provide for proper I&Q channel balance.

(2) IFF Receiver

The IFF portion of the receiver shown in Figure 3-64 operates as follows. The IFF output of the frequency diplexer is applied to a high level mixer through an oscillator. The IFF LO drive level is also 17 dBm. The LO frequency is 1030 MHz which provides for a 60 MHz IFF difference frequency. A PMFL coupler and bandpass filter couple the 60 MHz IFF difference frequency to a 6-stage low-power IC log video

amplifier which provides an 80-dB instantaneous dynamic range. The log video output provides the envelope of the IFF transponder pulsed code to the Data Processing subsystem.

(3) Power Requirements for IF Design

The total dc power required for the IF portion of the radar is 28 W distributed as follows:

Exciter (not including frequency divider and waveform generator)	16.5 W
Frequency Divider	2.5 W
Waveform Generator	4.6 W
Receiver (not including Synchronous Detector)	3.0 W
Synchronous Detector	1.4 W
	28.0 W

SECTION IV

SIGNAL PROCESSOR

1. INTRODUCTION

The recommended waveform for the Unattended/Minimally Attended Radar consists of a 32-pulse transmission in each azimuth dwell position. Each pulse is 128 μs in duration with Linear Frequency Modulation (LFM) coding to provide a bandwidth of 250 kHz, corresponding to a compressed pulse of 4 μs and providing a range resolution of 0.32 nmi.* Eight pulses will be transmitted at a fixed carrier frequency, with a nominal separation in time of 0.9 ms providing an unambiguous range of 73 nmi. Three more 8 pulse groups with similar timing will be transmitted, with carrier frequency separation of nominally 50 MHz. A sketch of this waveform is shown in previous Figure 3-33.

A block diagram of the signal processor for this waveform is shown in Figure 4-1. The processor will perform the following functions:

- Pulse compression of the 128 μs LFM pulse to 4 μs.
- Doppler processing of the eight-pulse waveform train to provide eight Doppler channel outputs and achieve coherent summation over each eight-pulse train.
- Weighting of selected Doppler processor channels to reduce Doppler sidelobes and widen null regions of the Doppler response.
- Background estimation, based on an average from 32-range cell samples of signal around each range cell of interest, to determine the clutter level in each Doppler channel except the zero Doppler channel.

The Data Processor will complete the signal processing function by:

- Performing the four sample noncoherent integration by summing the signal magnitudes from each of the four-pulse trains for each range-Doppler cell.
- Completing the background estimation by combining the estimates from each of the four-pulse trains for each range-Doppler cell.
- Maintaining a zero-Doppler-clutter map by recursive update over each scan of the zero Doppler channel signals. The clutter map provides an average ground clutter level for each range-azimuth cell.

*Combining background estimates across the four frequency diversity channels provides an effective sampling time of 1 μs for mean level thresholding, as described in Section 1.c below.

- Performing target detection by first selecting peak signals in range and declaring a target present if the peak signal magnitude exceeds any of three threshold levels which are:
  - A fixed level based on expected thermal noise level
  - A level computed from the estimated background by multiplying the estimate in each range-Doppler cell by a specified constant which will provide a desired probability of false alarm. The background for Doppler channel zero is obtained from the clutter map.
  - A special level is computed for the Doppler channels on either side of the zero velocity channel. This level is the product of a constant and the ground clutter estimate from the clutter map. Large stationary point objects will thereby be prevented from causing false detections in the Doppler channels adjacent to the zero velocity channel. Rejection of low-velocity signals is adequate in the remaining Doppler channels so as to not require special processing for large stationary objects.
- Performing target azimuth estimation by interpolation of the signal magnitude over three successive azimuth dwell positions.

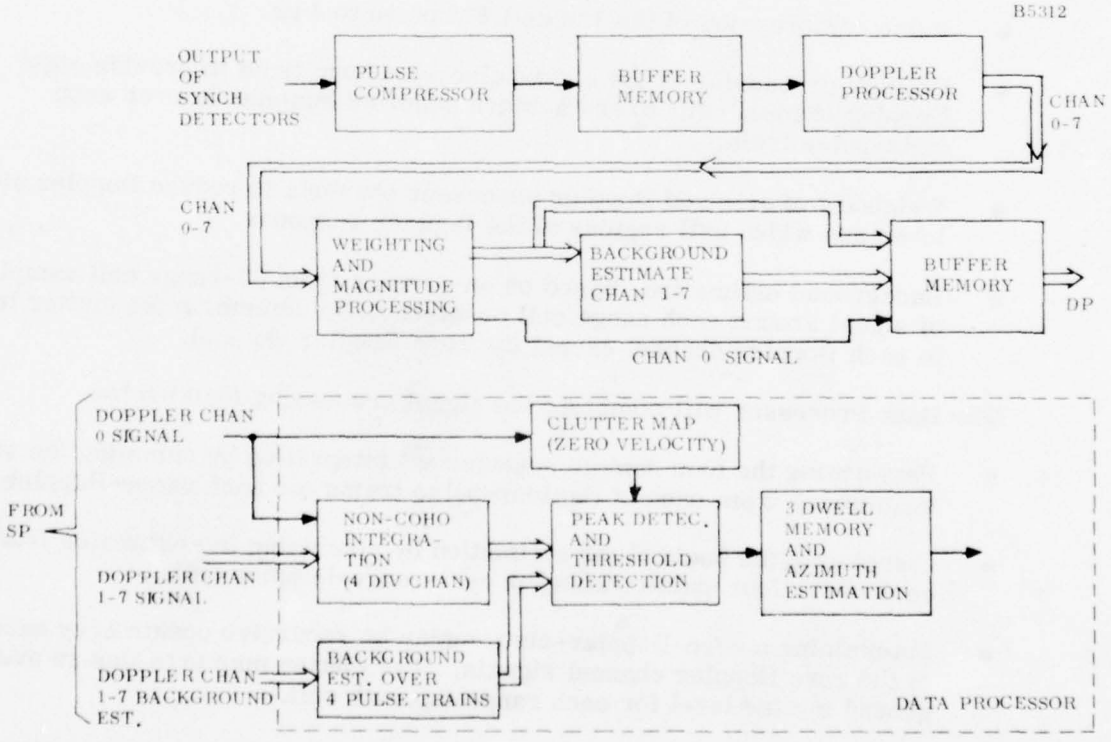


Figure 4-1. Processor Block Diagram

a. DOPPLER PROCESSING

The recommended Doppler sensitive waveform and associated Doppler processor has distinctive features which make it the best choice for the Unattended Radar. Like Moving Target Indicator (MTI) processing, Doppler processors will reject low-radial velocity interference in all filters except the one tuned to zero Doppler. Doppler filter response nulls, for all but the zero velocity filter, can be made to occur at zero Doppler frequency as shown in Figure 3-34, and thereby provide essentially the same rejection to low Doppler clutter as a single delay line MTI processor. In addition, however, the Doppler processor can handle two important situations which cannot be handled by the MTI. First, it provides coherent integration of zero-radial velocity targets, which in conjunction with the recommended ground clutter map will permit detection of low speed targets.

b. DOPPLER WEIGHTING

The second feature of Doppler processing is that it can accommodate interference which is not near zero Doppler, as well as interference whose Doppler (spectral) location changes appreciably with range. Interference which shifts its spectrum with range, as has been shown to be true of weather interference, cannot be cancelled by a single, fixed rejection zone filter. The Doppler processor attempts to isolate the interference in Doppler so that some Doppler channels can operate in a relatively interference-free environment. Weighting of the Doppler channel outputs greatly improves this isolation by decreasing the Doppler sidelobe response. Proposed design weights of -1/2, 1, -1/2 provide a response for the center filter, i.e., the one weighted by unity, whose Doppler sidelobes are down below 32 dB. Such weights are obviously extremely simple to implement in a digital processor since multiplication by 1/2 is equivalent to a single shift.

Besides reducing Doppler sidelobes, weighting provides a second important effect. Null regions of the Doppler response are very significantly broadened by weighting. Therefore, the rejection from any one of the weighted filters to ground clutter, which by design of the filters, will always be centered on a response null, is increased by 10 dB above what a single delay line MTI would provide. This same null region widening also decreases the Doppler filter sensitivity to radar frequency

instabilities by the same 10 dB over that of the MTI filter. Weighting will not be performed for the Doppler filters on either side of the zero velocity filter, or for the zero velocity filter itself, since the broadening of the mainlobe response due to weighting is detrimental to ground and weather clutter response of these filters.

c. BACKGROUND ESTIMATION

Weather clutter interference has been shown to vary its Doppler position as a function of range. A technique is therefore required which adaptively turns "off" the cluttered Doppler channels as they occur in range and turns them back "on" again when they are no longer cluttered. The background estimator aids in accomplishing this function by approximating the clutter level, for each separate Doppler channel except the zero channel, at every range cell using signals from 16 range cells on either side of the center cell of interest. The center cell signal and the two cells adjacent to the center range cell on either side are not used in the two 16 sample sets so the signal of interest (in the center cell) will not influence the background estimate. Once the background is derived, it is used to control the detection threshold. As clutter varies from one range cell to the next, the threshold is correspondingly raised or lowered to prevent the clutter from causing excessive false detection reports.

The recommended processor sampling rate of twice the signal bandwidth of 250 kHz provides the background estimator with 32 samples (two 16 sample windows) which span a range of 6 nmi (considering the 5 sample center gap). That is, the clutter extending 3 nmi on either side of every range cell is used to estimate a local background. A larger estimation window would be inappropriate because of the variation of weather clutter with range. The 32 samples used to estimate the clutter level are highly correlated because the samples are taken at twice the signal bandwidth. Effectively, only 16 independent samples are available from the 32 sample total. This is too few to obtain a reliable background estimate and the corresponding detection processor loss will be excessive. Therefore, the background estimates are combined separately for each range cell and Doppler channel from each of the four pulse trains comprising a single azimuth dwell. In this way, the number of independent samples is increased by a factor of 4 so that 64 samples are employed in making each estimate and the detection loss is reduced to a relatively low level. By providing 64 independent samples of clutter within a 6-nmi range window, the recommended design achieves an effective bandwidth of 1 MHz.

d. DOPPLER ALIGNMENT

Combining corresponding Doppler channel outputs from one eight-pulse train to next is normally not possible. Since each train employs a different frequency, the Doppler location, of any signal or clutter having a given (nonzero) radial velocity, will change. That is, signal or clutter could appear in different Doppler channels on successive pulse trains, making combinations from train to train impossible. Doppler alignment can however be maintained over all four-pulse trains by adjusting the PRF in each train to just compensate for the Doppler shift due to carrier frequency change. A Doppler aligned system is recommended for the Unattended Radar because it not only permits combining background estimates between pulse trains, to greatly reduce detection losses from clutter level uncertainty, but also permits more effective signal integration.

e. DIVERSITY GAIN

Each of the four 8 pulse trains is transmitted on a different carrier frequency. As a result, four independent samples of any target's fluctuating signal return are received. This can yield a dramatic improvement in detection performance. Assuming a Swerling II target cross section model, the four independent noncoherently-combined samples require, for a given probability of detection, a Signal-to-Interference Ratio (SIR) per sample which is 3- to 4-dB less than would be required if the samples were completely correlated and were coherently integrated. The noncoherent integration between independent samples required to achieve this diversity gain can only be accomplished if the Doppler channels remain aligned between pulse trains so that integration can be performed separately on each Doppler channel. Approximations to noncoherent integration required in a nonaligned Doppler configurations, such as summing the largest clutter normalized signal from among all the Doppler channels on each pulse train, would incur a very large detection loss because of the clutter level uncertainty. Such approximations and their associated detection losses are not required in the recommended Doppler aligned system.

f. BLIND SPEEDS *

One consequence of the aligned system is the presence of blind speeds. These occur because the recommended pulse train has a PRF of about 1.15 kHz leading to Doppler response foldover every 1.15 kHz. As a consequence, targets at Doppler frequencies which are integer multiples of 1.15 kHz (corresponding to a velocity of 123 m/s or 240 kts)will appear in the same Doppler channel as the zero-velocity ground clutter. High levels of ground clutter therefore not only mask targets at zero velocity, which is unavoidable, but also targets having velocity which correspond to Doppler frequencies of 1.15 kHz, 2.3 kHz, 3.45 kHz, etc. which are referred to as blind speeds. Detection performance loss at blind speeds caused by ground and weather clutter is quite apparent by the periodic nulls in previous Figure 3-36.

The aligned Doppler system will, on a given scan, generally be unable to detect targets whose radial velocities occur at blind speeds and whose range corresponds to the clutter range. A variation in PRF between successive radar scans will change the location of the blind speeds. A recommended PRF increase of five percent on each scan for four successive scans will adequately fill in the blind speeds. High speed targets will be detectable, that is out of the blind speeds, on at least two out of every four scans. Of course, the blind speed problem only exists in the presence of clutter so that in clear regions, a target would be detectable on all scans. In contrast, an MTI system places a response null at zero Doppler which generates blind speeds at integer multiples of the PRF whether clutter exists or not, although the effect of MTI blind speeds can also be significantly reduced by using "staggered" PRF's.

g. CLUTTER MAP

The characteristics of ground clutter are sufficiently different than weather clutter as to require special processing. The former is stationary and highly non-uniform, capable of exhibiting extremely large cross section in one range cell and virtually nothing in a neighboring cell. Background estimation techniques employed

*The term "blind speed" is used here to refer to a target radial velocity at which clutter masks the target return. This masking can only be caused by clutter near the range of the target and in the same Doppler filter. The mean level threshold is then adaptively raised, reducing the detectability of the target. This is a somewhat unconventional application of the term "blind speed", since it usually refers to a fixed (unwanted) null in the passband response of the devices used to remove clutter. By this conventional definition, the adaptive processing described in this report has no "blind speeds".

for weather clutter require a reasonably uniform density over the range interval used for averaging purposes. Such an estimator is inappropriate for ground returns because of the lack of uniformity. However, because these returns are stationary in range, an estimation process can be used which determines the clutter in each range cell by averaging the returns from that cell over many scans.

A clutter map will be maintained by the Data Processor which contains an estimate of the average return from each range cell for every azimuth beam position. Recursive update of the estimates for each range-azimuth cell are made each scan by using the output of the zero velocity Doppler filter. The updated estimate is obtained by taking the sum of 7/8 of the previous estimate and 1/8 of the new measurement. In this way slowly varying changes in ground clutter due to temperature, wind, and moisture variations will be taken into account.

The ground clutter map permits detection of very low radial speed targets such as those crossing tangentially to the radar beam. These target return signals which will appear in the zero Doppler filter are compared to the ground estimate. As the low speed target moves into range cells which are not heavily cluttered, the threshold detector will note that the signal is substantially above the background and will declare a target present.

2. SIGNAL PROCESSOR REQUIREMENTS

The signal processor for the Unattended Radar shall consist of the following functions:

- Pulse Compressor - to compress a 128-μs, LFM coded waveform of 250-kHz bandwidth to 4-μs width.
- Doppler Processor - to coherently integrate 8 samples uniformly spaced a nominal 0.9 ms apart, for all radar ranges over 8 interpulse periods. Eight Doppler filters will be provided with output weighting of selected channels.
- Magnitude Processor - to compute the output magnitude from each Doppler channel for all radar ranges.
- Background Estimator - to compute the average background at any range by summing signal samples at 32 points (16 samples on either side of the range of interest). The background shall be determined for each Doppler channel except the zero channel.

a. SAMPLING

If the signal processor is synthesized using discrete signal samples, the sampling rate shall be at least 500 kHz which is twice the signal bandwidth, to maintain a low sampling loss.

b. DYNAMIC RANGE

A dynamic signal range of 51 dB shall be accommodated at the input to the pulse compressor. That is, the signal processor shall maintain linearity for ground clutter, at the 84th percentile, which exceeds the thermal noise level by 51 dB. This same 51 dB shall be accommodated at the output of the pulse compressor since the ratio of ground clutter (or any range continuous clutter) to noise is not altered by pulse compression. Because ground clutter is narrowband around zero Doppler, the CNR will increase through the Doppler processor, demanding a 60-dB capability at the zero-velocity channel output.

c. DIGITAL PROCESSOR A/D CONVERTER REQUIREMENTS

A digital implementation offers one means of synthesizing the signal processor for the Unattended Radar. In this implementation, the output of the radar receiver is taken through a synchronous detector which develops an in-phase (I) and quadrature (Q) video signal. These I and Q video signals are then sampled by two analog-to-digital converters (A/D), one for I and one for Q. Each A/D would have to sample at least the signal bandwidth of 250 kHz to maintain the information content of the signal. This complex sampling rate equal to the signal bandwidth is referred to as the Nyquist rate. However, to maintain low sampling loss as stated in the above sampling requirements paragraph, the A/D will be operated at twice the Nyquist rate or 500 kHz.

An operational implementation using a single A/D operating at 1 MHz and time sharing between the I and Q signals is functionally equivalent and can be considered. In this configuration, one of the signals, either I or Q, will be time delayed by a sampling time period to maintain time alignment of the I and Q samples.

The A/D shall provide at least 10 bits of output, one bit for sign and 9 bits for amplitude. Setting the thermal noise level at 1.5 quanta provides a linear response, with these 10 bits, to signals 57 dB above the noise level on the I and Q channels.

Quantization noise is a measure of the uncertainty of the signal level due to quantizing amplitude to discrete levels. This noise increases the effective thermal noise by only 0.2 dB when the thermal noise is at the recommended level of 1.5 quanta. As a point for comparison, if the thermal noise level were set to one quanta, the quantization loss would be 0.35 dB.

Bit growth will be permitted through the signal processor to account for increased dynamic range requirements. At least 12 bits of I and Q shall be used at the output of the Doppler processor. At this point, the noise level will be established at 2 quanta. Signal amplitudes can consequently be represented in I and Q which exceed the noise level by 66 dB, which is greater than the required dynamic range at the Doppler processor output.

d. LOSSES

Minimizing signal processor detection losses is extremely important in the Unattended Radar. Each 1-dB loss necessitates approximately a 25 percent increase in transmitted radar energy and a corresponding increase in prime power. Signal processor losses have been held to a total of 4 dB in the recommended designs as shown by the breakdown in Table 4-1.

e. PRIME POWER

Two alternate signal processor implementations have been found to satisfy the requirement for the Unattended Radar. One design is a digital synthesis using existing high density integrated circuits (IC's) to accomplish the entire signal processing function for 127 W of dc power. The alternate design uses Charge Coupled Devices (CCD's) in a sampled analog design which accomplishes the signal processing function for only 22 W.

While the CCD based design offers the advantage of much lower power and fewer components (902 IC's versus 2330 IC's) it has a higher technological risk. Many of the CCD components which are ideally suited to the Unattended Radar application, such as the pulse compressor chip and the CCD Doppler processor configuration, are presently being developed and tested. It is recommended that a single-string CCD signal processor be breadboarded and verified before this design approach is selected for the Unattended Radar. Both design approaches, the digital and the analog CCD, are described in the remainder of this section.

TABLE 4-1. SIGNAL PROCESSOR DETECTION LOSSES

Cause	Loss (dB)
Doppler mismatch in the Pulse Compressor (for a mismatch corresponding to a 2400 knot target velocity)	0.3
A/D Converter Quantization Loss (applicable for digital signal processor implementation; for thermal noise level set to 1.5 quanta)	0.2
Range Straddling Loss (applicable to discrete sampled signal processor implementation; for a complex sampling rate of twice the signal bandwidth)	0.3
Doppler Straddling Loss (for Hamming weighting of adjacent filters using weights of 1/2, 1, 1/2)	0.5
Doppler Weighting Loss (for Hamming weighting)	1.8
Background Estimation (CFAR) Loss (due to incorrect setting of detection threshold because of uncertainty of precise background level; based on 32 correlated background samples for each of four 8-pulse transmission for a total of 128 correlated samples)	0.3
Implementation Losses (due to rounding truncation, etc.)	0.6
Total Losses	4.0 dB

3. DIGITAL SIGNAL PROCESSOR

a. SUMMARY

A block diagram of the digital signal processor design is shown in Figure 4-2. It was designed to be highly reliable while using little power. The reliability is achieved using redundant logic. Testing is done from the data processor and is organized into two areas: fault detection and fault location. Fault detection is achieved by inserting the same tests into the redundant functions and comparing their outputs. If a fault is detected by failure to compare exactly, then it is located by running the test again and examining the test results in the data processor. Low power is achieved by using CMOS logic, CCD digital memories and, in some instances, low power Schottky logic where higher processing speed was required. There is little difficulty interfacing CMOS and low power

Quantization noise is a measure of the uncertainty of the signal level due to quantizing amplitude to discrete levels. This noise increases the effective thermal noise by only 0.2 dB when the thermal noise is at the recommended level of 1.5 quanta. As a point for comparison, if the thermal noise level were set to one quanta, the quantization loss would be 0.35 dB.

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While the CCD based design offers the advantage of much lower power and fewer components (902 IC's versus 2330 IC's) it has a higher technological risk. Many of the CCD components which are ideally suited to the Unattended Radar application, such as the pulse compressor chip and the CCD Doppler processor configuration, are presently being developed and tested. It is recommended that a single-string CCD signal processor be breadboarded and verified before this design approach is selected for the Unattended Radar. Both design approaches, the digital and the analog CCD, are described in the remainder of this section.

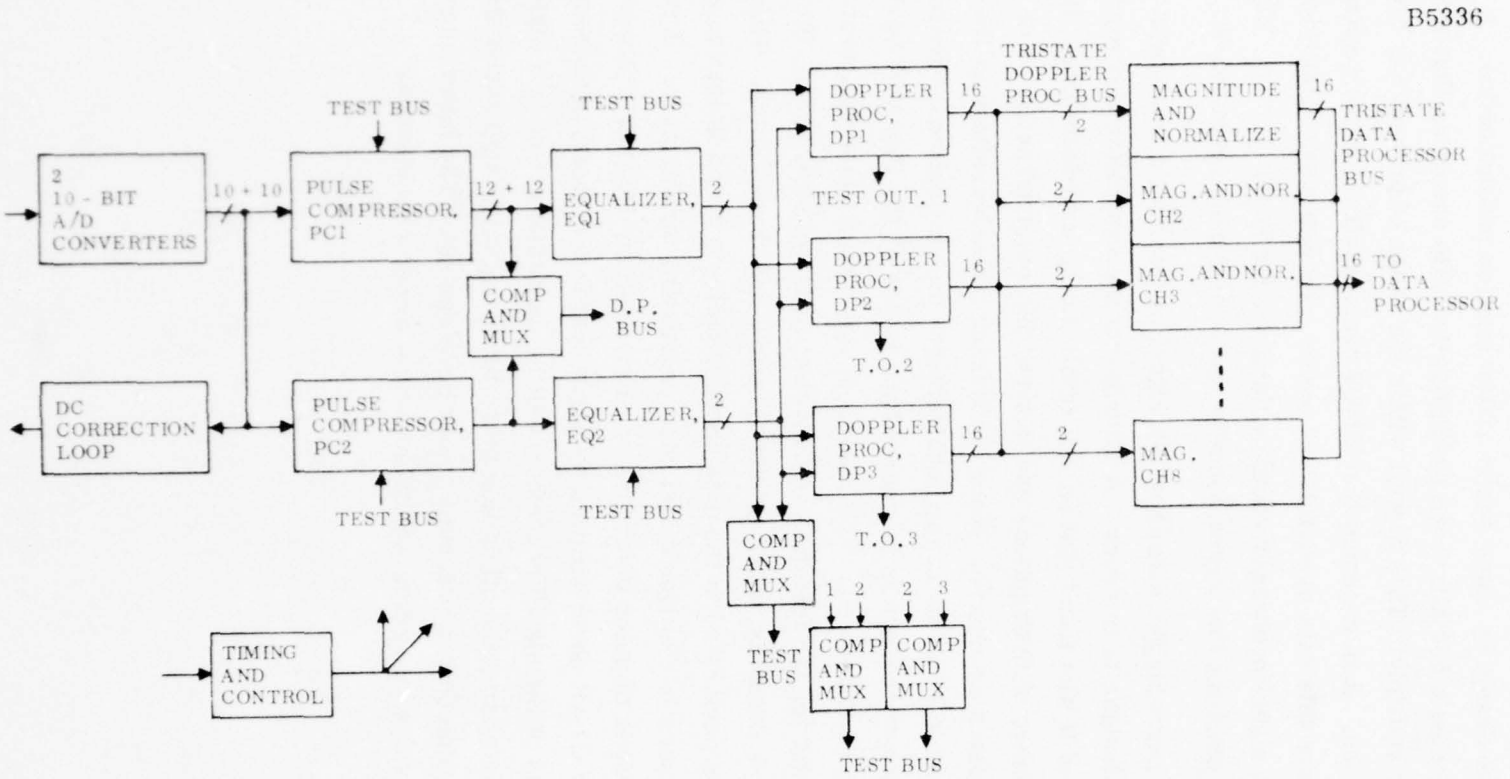


Figure 4-2. Signal Processor Block Diagram

Schottky if they are both run with a 5-V power supply. Further power savings were achieved in the design by using serial arithmetic for multiplication. A serial bit rate of 8 MHz provides a 500 kHz word multiplication rate assuming that it takes 16 clocks to do a 12-bit multiply. This is well within the range of present day low power Schottky devices. It is expected that CMOS serial multipliers will soon be available that can achieve this rate at even lower power. By using only CMOS logic and serial arithmetic, a signal processor could be designed for under 100 W. The present design which employs low power Schottky and CMOS uses about 125 W.

Before pursuing the details of the signal processor, a few words about one of the rejected designs is in order. A microprocessor approach was examined for signal processing and it was found that unless some simple waveform like a Barker code is used, the number of instructions and in turn, the required power to do pulse compression becomes excessive. Since the Barker coded waveform is Doppler sensitive, it is unacceptable in terms of the requirements for an Unattended Radar. Until the speed of microprocessors is increased by a factor of 10, they will be difficult to use in LFM pulse compression. The results of this design show that microprocessors are most useful for the functions of noncoherent integration across the four frequency channels, peak detection in range and azimuth, and thresholding. These functions are now being performed in the data processing logic which is implemented with microprocessors in a unique distributed processing architecture. It is recommended that the functions of pulse compression, equalization, Doppler processing, envelope detection and CFAR normalization be hardwired in the signal processor. Two implementations of the signal processor will be described. One is a digital design using existing components, the other is a more technologically aggressive design using analog CCD components presently under development. The latter approach provides signal processing at a remarkably low prime power requirement.

A block diagram of the recommended digital signal processor is shown in Figure 4-2. The corresponding time line is shown in Figure 4-3. The output of the synchronous detector is sampled by the two A/D converters each operating at a 500-kHz rate, so two 10-bit words are sent to the pulse compressor every 2 μs. The dc correction loop is included to eliminate any dc bias in the video amplifiers and A/D converters. The pulse compressor is a phase matrix (Butler matrix) pulse compressor using an 8 input Fast Fourier Transform (FFT-8) basic design. Actually, an FFT-4 front end is used with an output network that results in the correct impulse response. An equalizer, a small finite impulse response (FIR) filter, is included to reduce the sidelobes created by the pulse compressor. Here a conversion is made to serial arithmetic to save logic and power in the multipliers. The data is left in serial format and passed on to one of the Doppler processors, which also use serial arithmetic. The Doppler processors contain CCD digital memories and Combination-Exponentation (CE) chips. The CE chip is a General Electric invention that can be used to execute FFT's and related inner product functions with serial arithmetic. Eight of these chips are combined to make an FFT-8, which will be used to produce eight Doppler channels. The data is transferred to the magnitude and normalizer functions. While the transfer is serial, the data is reformatted into a parallel format in these functions. The magnitude, M, is calculated by adding the absolute value of the largest of I and Q to one-half of the absolute value of the smallest. The normalizer takes these magnitude values, squares them, and calculates an average background estimate (B^2) in a window of 16 range cells on each side of each cell with a total guard band of five cells around the center cell which is excluded from the averaging process. Background estimates are made for each Doppler channel output except the zero Doppler channel. The corresponding values of M^2 and B^2 are sent to the data processor, which noncoherently integrates them over the four frequency channels.

Table 4-2 is a summary of the number of boards, IC's, and power required by each function. The recommended board size is about 85 to 90 $in.^2$. It is capable of holding 60 to 70 IC's with a 110 to 120 pin connector. The total power adds up to 127 W, but if the equalizer can be converted to CMOS with the development of a CMOS serial multiplier capable of going at 8 to 10 MHz, then the total power could be cut to approximately 100 W.

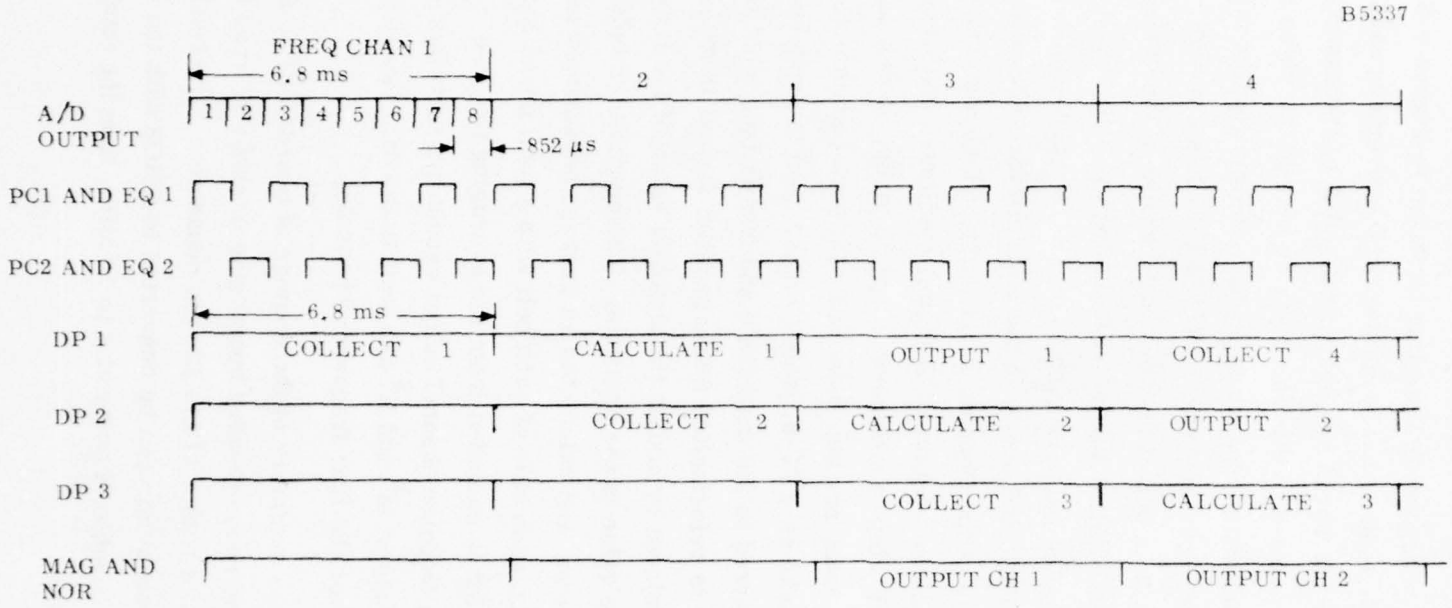


Figure 4-3. Signal Processor Time Line

TABLE 4-2. SIGNAL PROCESSOR POWER AND LOGIC ESTIMATES

	No. of Functions	Boards Per Function	IC's Per Function	Type of IC	Power Per Function	Total Boards	Total IC's	Total Power (W)
A/D Converter	2	1	-	-	3.1	1	-	6.2
D/C Correction Loop	2	1	41	CMOS	2.4	2	82	4.8
Pulse Compressor	2	7	350	CMOS	17.5	14	700	35.0
Equalizer	2	1	20	L.S.	15.0	2	40	30.0
Doppler Processor	3	1	40	CMOS	4.0	3	120	12.0
Magnitude Function	8	1	47	CMOS	1.7	8	376	13.6
Normalizer (7 required plus one standby)	8	2	110	CMOS	2.4	16	880	19.4
Compare and Multiplex (For Testing)	4	1	20	CMOS	1.0	4	80	4.0
Timing and Control	1	1	52	CMOS	2.0	1	52	2.0
OVERALL SIGNAL PROCESSOR TOTAL						51 BDS	2330 IC's	127.0 W

b. DESIGN DETAILS

The A/D converters and dc correction loops are shown in Figures 4-4 and 4-5. The main function of the dc correction loop is to eliminate the dc bias and drift found in A/D converters. A 32 sample input is made each PRF during some time when only receiver noise is present. This value is delayed one dwell time and added into an accumulator. The output is sent back to the synchronous detector where it is used to adjust the video amplifier for the next dwell.

The pulse compressor is shown in Figure 4-6. It is a dual-channel function that compresses LFM pulses with a BT of 32. The reason for the dual-channel feature is that sampling is at twice the Nyquist rate so there are essentially two channels of information to process for each pulse. The pulse compressor has the same impulse response as an FFT-8 even though the front end is just an FFT-4. The FFT-4 outputs are used twice with the appropriate delays to create this effect. The data is reclocked at the output of each adder and the complex multipliers (W^1 and W^3) contain a two adder network hardwired to look like a multiply by $1/\sqrt{2}$.

The equalizer is shown in Figure 4-7. The data is converted from a parallel to a serial format for the serial multipliers. The multipliers and adders are low power Schottky. For more detail the construction of these multipliers is provided in the subsequent signal processing element design description.

While a single pulse compressor and equalizer can handle the required data rate, a second has been added, as shown in Figure 4-2, for redundancy to increase the reliability of this portion of the signal processor. This area was assessed as critical to the system reliability because they are serial functions and do not have the functional redundancy found in the Doppler processor, and magnitude and normalizer functions.

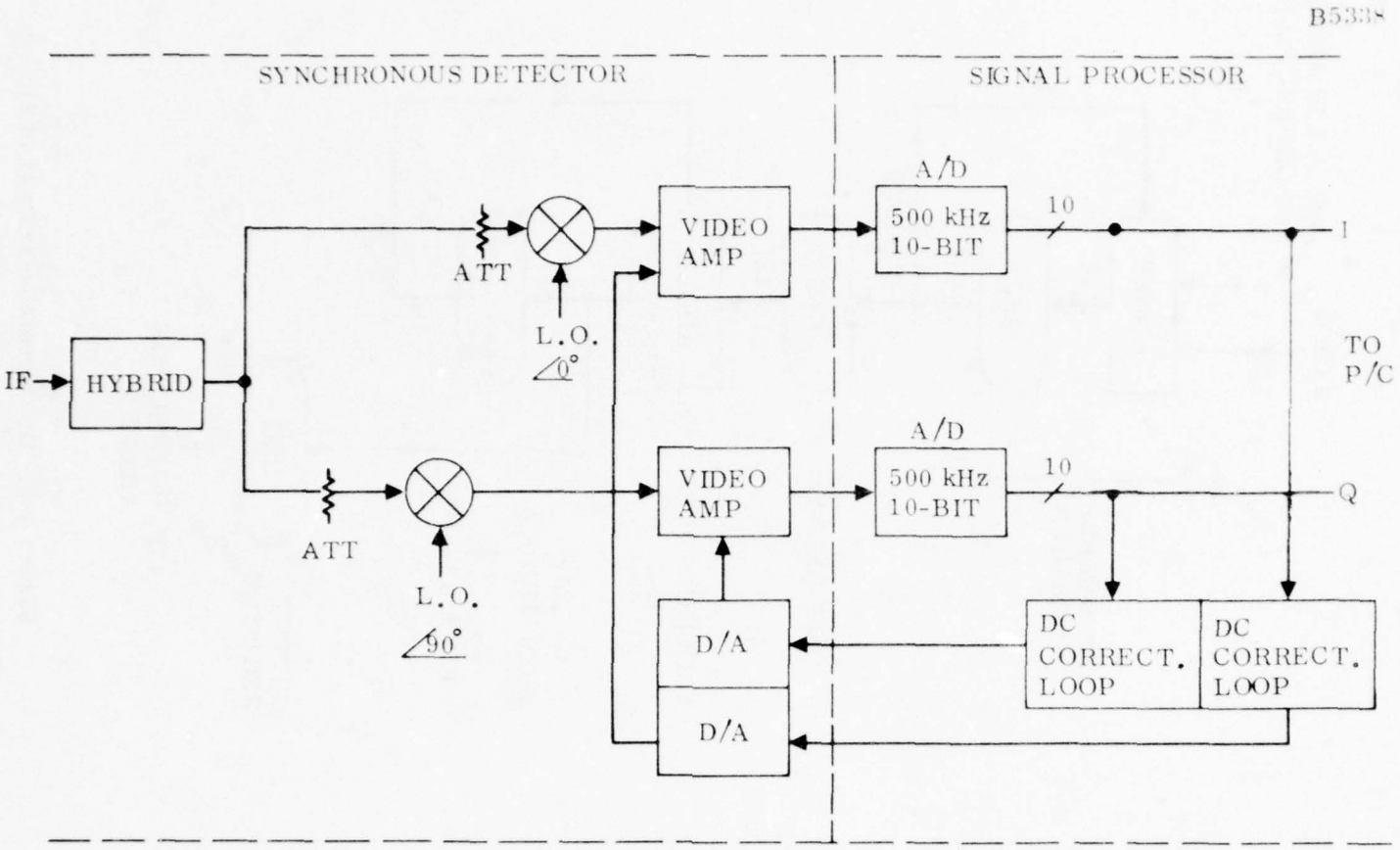


Figure 4-4. A/D Converter and Dc Correction Loop Block Diagram

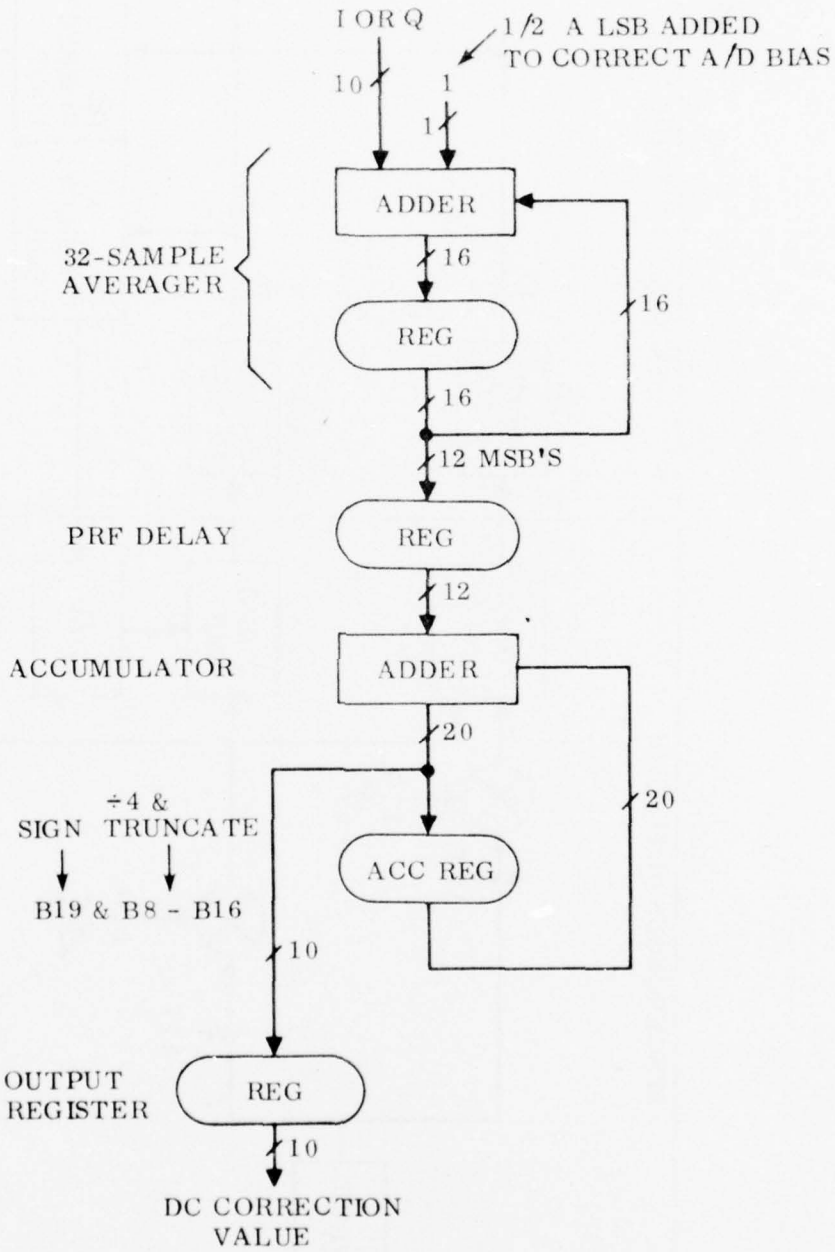


Figure 4-5. Dc Correction Loop (1 of 2)

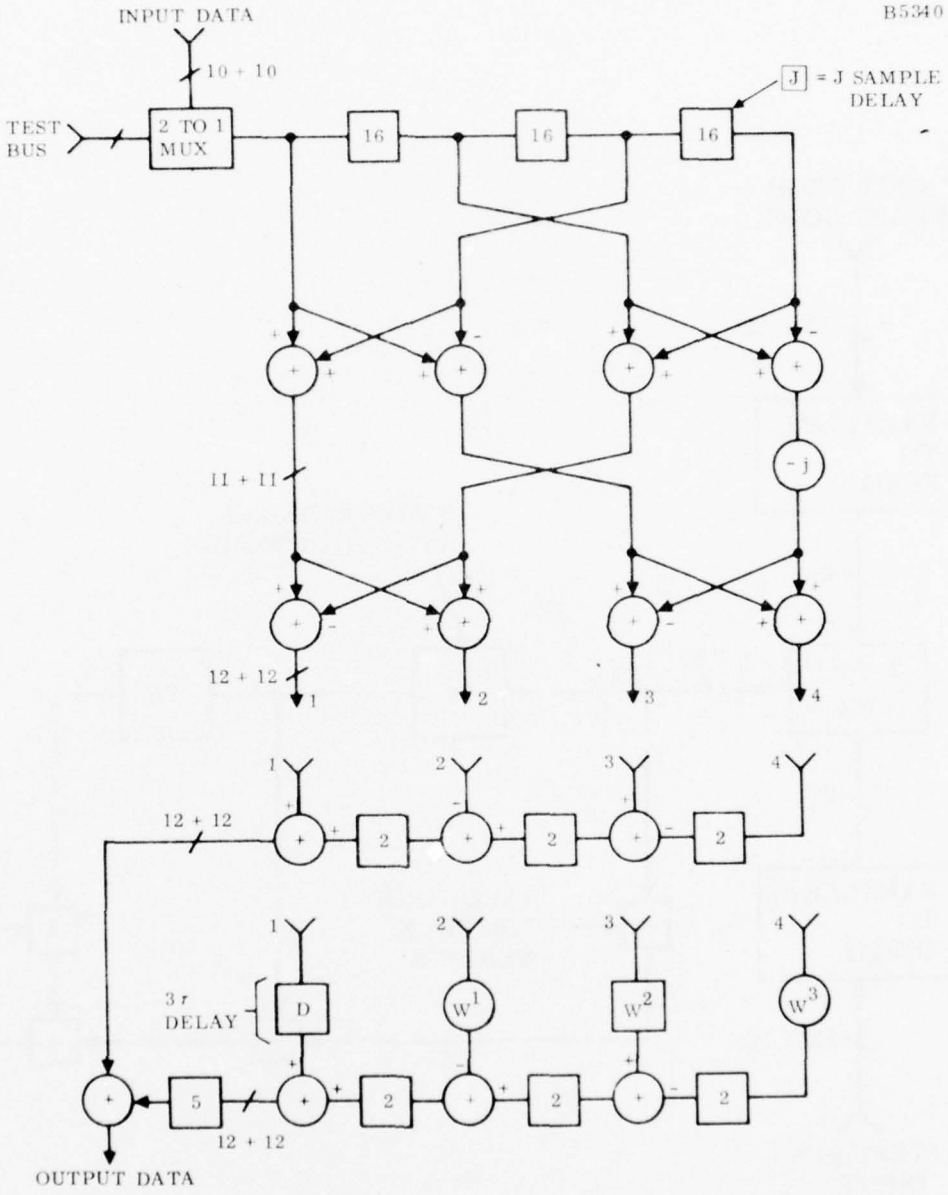


Figure 4-6. Pulse Compressor BT = 32, 2 Channels

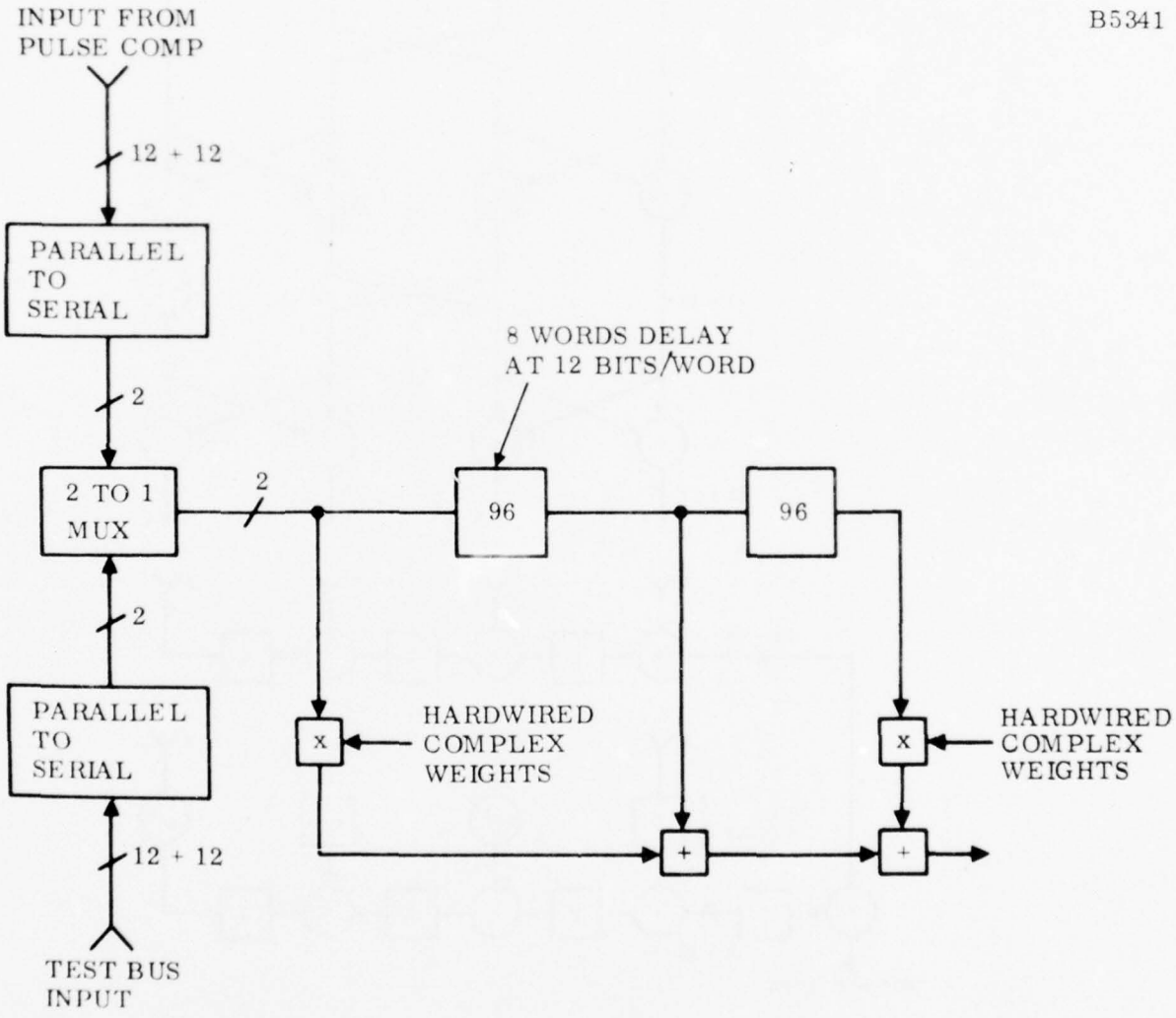


Figure 4-7. Serial Arithmetic Equalizer

The Doppler processor is shown in Figure 4-8. It uses eight CE chips to do an FFT-8. Each pair of CE chips work together to make an FFT-2. Three recursive passes have to be made through the CE chips to do an FFT-8. Each pass is equivalent to going through one stage of Figure 4-9.* The sorting multiplexer (mux) is used to perform the interconnects shown between the FFT-2 blocks in Figure 4-9. The CCD memories are organized to provide a long shift register function. Sixteen shift registers are required, each with a capacity of 362 words by 12 bits for a total of 4344 bits. The 16 registers provide storage for the I and Q samples from the 8 interpulse periods being processed. The two CCD memories can be organized to build shift registers in multiples of 128 bits up to 8192 bits long, so there is ample provision to expand (up to 680 words if necessary).

The magnitude calculator is shown in Figure 4-10. The input data is converted to a parallel format in the parallel-to-serial registers. The sign bit is examined to determine if the number is positive or negative. The positive value or the two's complement of the negative value is selected to get an absolute value for I and Q. The two values are compared and the magnitude (M) is calculated as the largest plus half of the smallest.

The magnitude is squared in the normalizer (Figure 4-11) by using a Programmable Read Only Memory (PROM) lookup table. The PROM's use less power than a multiplier because only four are selected at any one time. The unselected PROM's only consume 0.1 mW of power each. Another feature of the normalizer is the Random Access Memory (RAM) that is being used to synthesize the shift registers that would normally be used to provide the 32 cell background window. Background values are calculated in the accumulator register which requires only four memory accesses to calculate each B^2. The memory is a 64 word by 16 bit memory, which is addressed by a cyclic 37 address counter to implement a shift register 37 stages long. The four taps are found by addressing the proper locations relative to the address in the address counter with a modulo 37 addition. Actually, four modulo 37 address counters are being used to keep track of the tap addresses. Finally, the values of M^2 and B^2 are passed onto the data processor where they are integrated over the four frequency channels.

*The 4 CE chip pairs in Figure 4-8 correspond to the four FFT-2 butterflies shown in a single pass of Figure 4-9. In operation, all of the data stored in the CCD memories is processed by the 4 CE chip pairs and returned to memory. This is defined as a single pass. Repeating this operation 2 more times accomplishes the complete FFT-8 operation shown canonically in Figure 4-9.

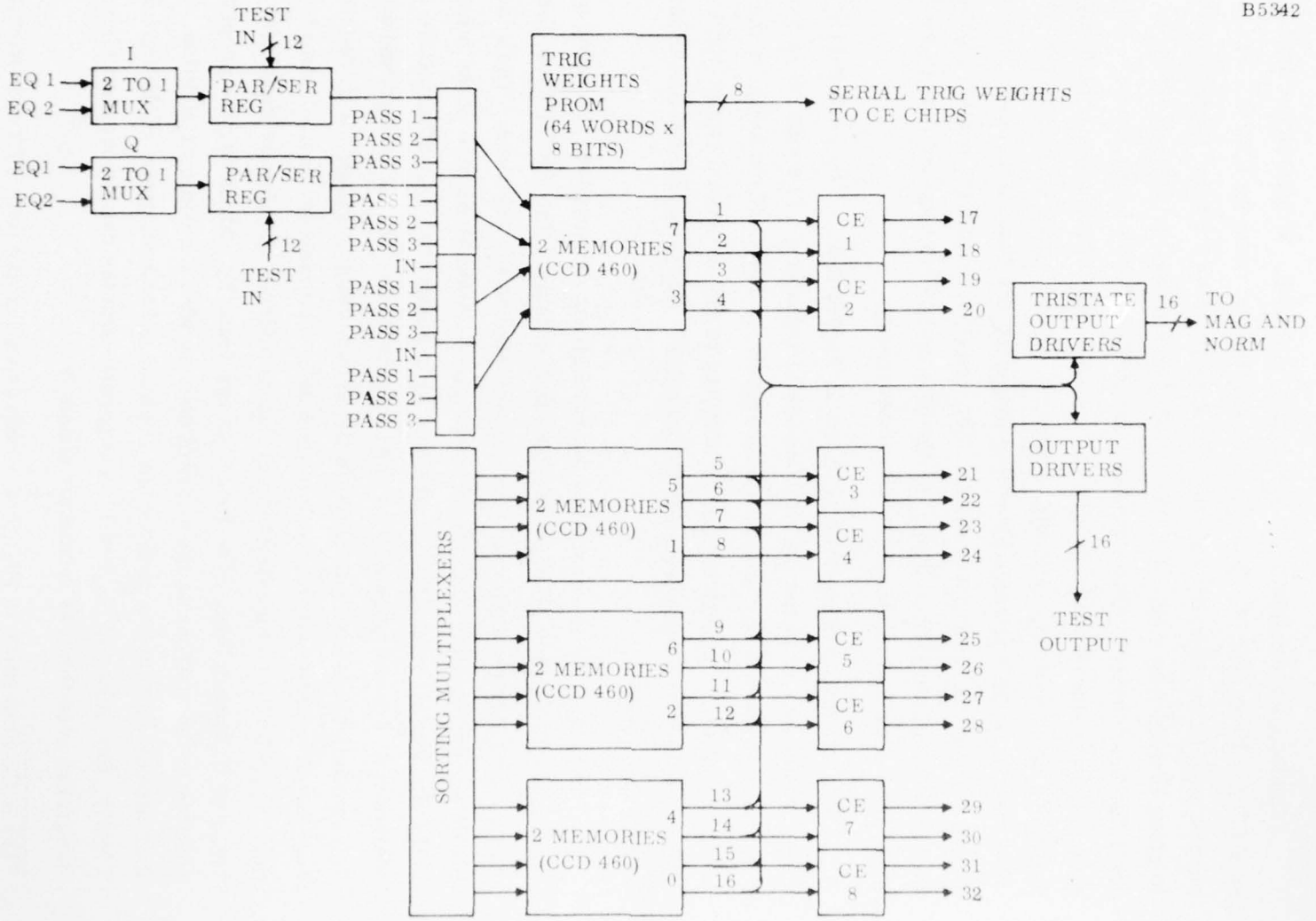


Figure 4-8. Doppler Processor Block Diagram

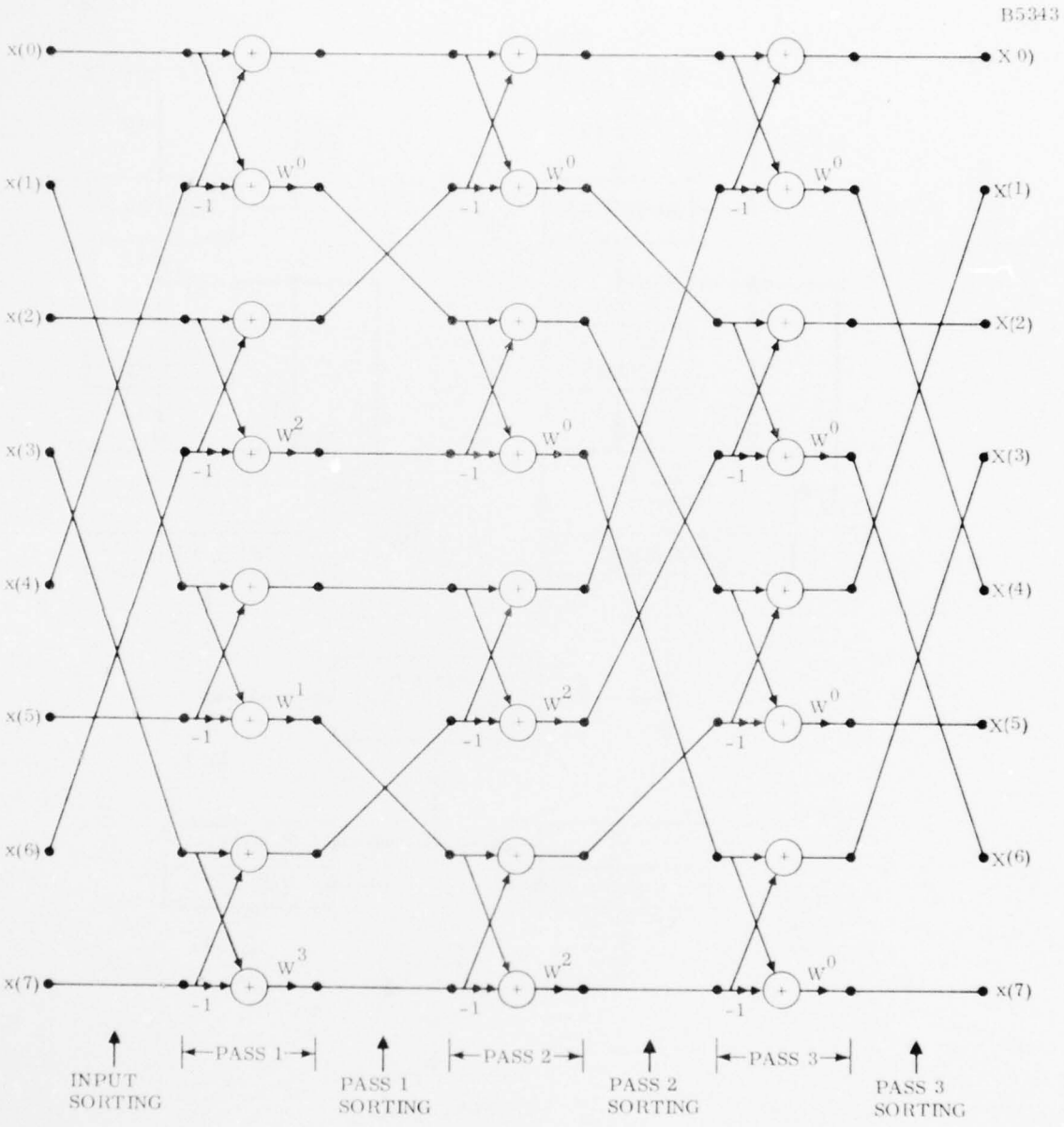


Figure 4-9. Decimation-in-Frequency FFT 8 Using FFT 2's

B5344

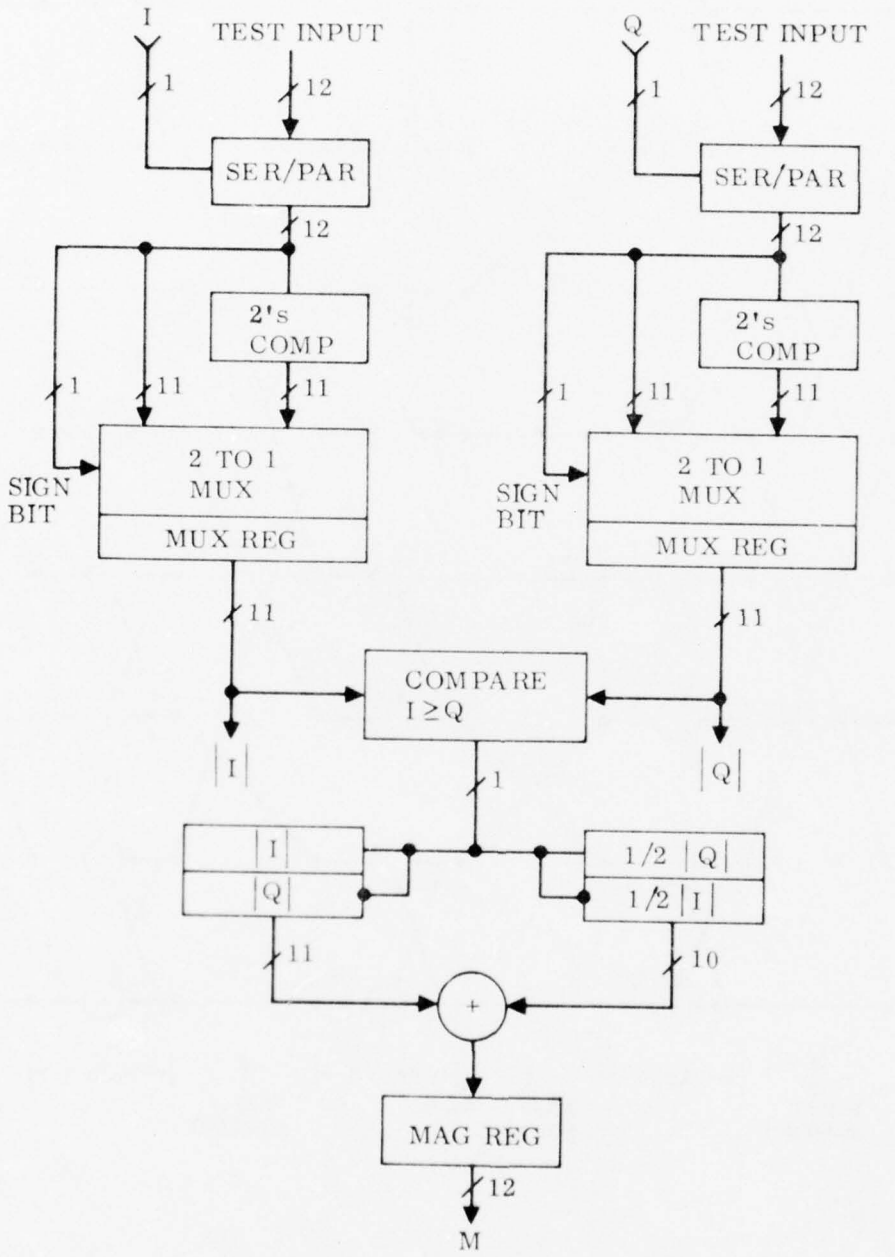


Figure 4-10. Magnitude Calculator

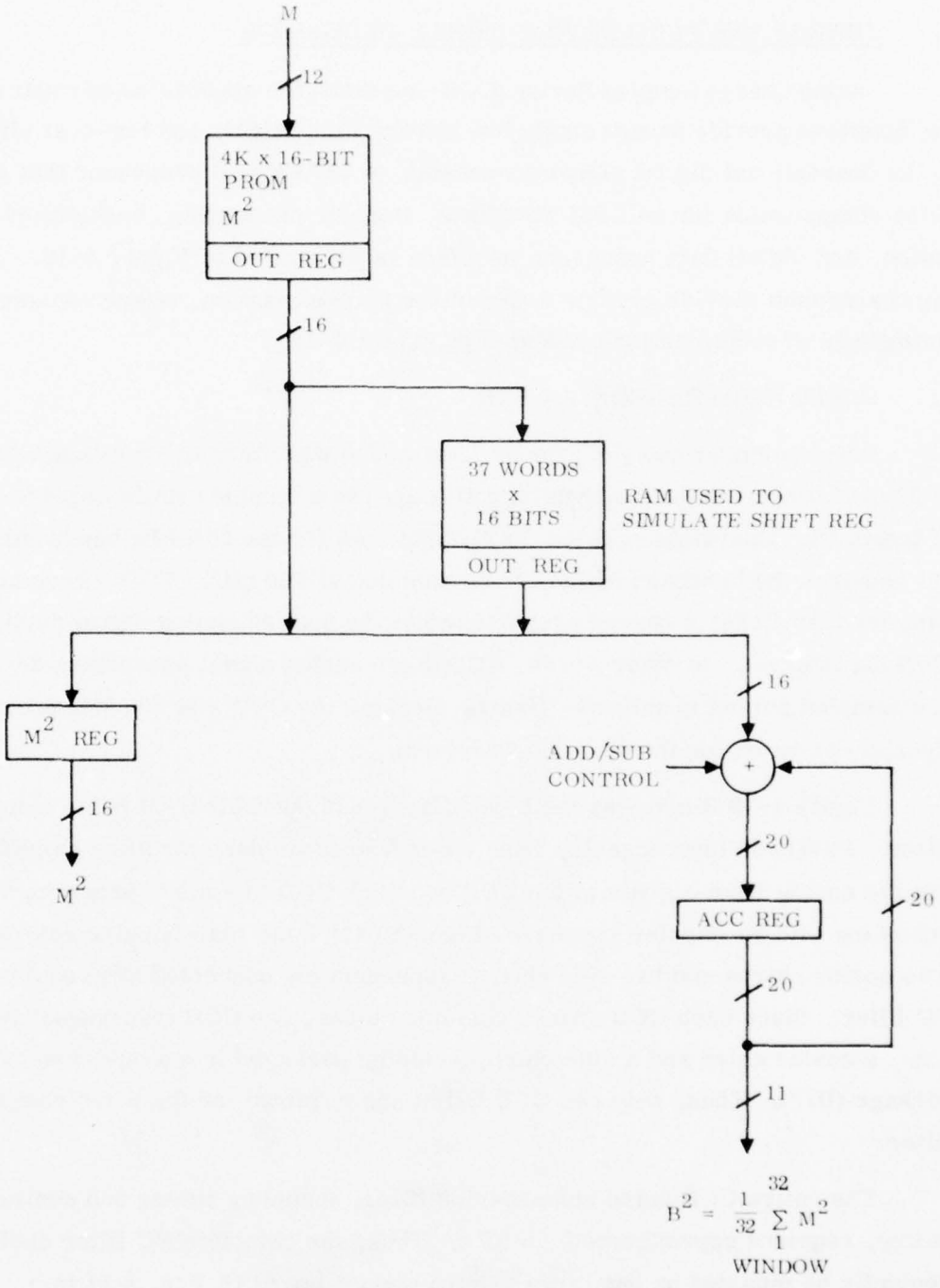


Figure 4-11. Normalizer

4. CHARGE COUPLED DEVICE SIGNAL PROCESSOR

Analog Charge Coupled Device (CCD) implementations of selected radar signal processing functions provide an extremely low power, lightweight, and low-cost alternative to the conventional digital signal processor. A CCD signal processor that performs pulse compression for an LFM waveform, Doppler processing, background normalization, and digital data processor interface is illustrated in Figure 4-12. The following paragraphs provide greater detail of the implementation, power requirements, and limitations of each function presented in Figure 4-12.

a. PULSE COMPRESSION FILTER

Pulse compression (PC) for an LFM coded waveform of time-bandwidth product of 32 operating at twice the Nyquist rate requires a complex finite impulse response of length 64. Operating at twice the Nyquist rate for the 250-kHz bandwidth LFM signal requires the baseband signals to be sampled at 500 kHz. CCD's have an internal sampler that stores a charge proportional to the applied analog signal during the clocking interval. In other words, CCD's are analog signal processing devices that are sampled but not quantized. Hence, clocking the CCD's at 500 kHz provides twice Nyquist operation for the baseline waveform.

Figure 4-13 illustrates the block diagram of the CCD LFM pulse compression filter. Baseband input signals, from the synchronous detector after amplification, are the analog input signals of the CCD's. Each CCD is a mask programmable serial structure with an impulse response of length 64. Four real-impulse response CCD's (two cosine chirps and two sine chirps) appropriately connected are required for the PC filter. Since each CCD shares common clocks, two CCD transversal filters, i.e., a cosine chirp and a sine chirp, would be packaged in a single dual in-line package (DIP). Thus, only two CCD DIP's are required for the pulse compression filter.

The entire CCD pulse compression filter, including timing and control circuitry, requires approximately 55 IC's. Thus, the complete PC filter could conveniently be mounted on one large printed circuit board (7.7 in. x 11 in.).

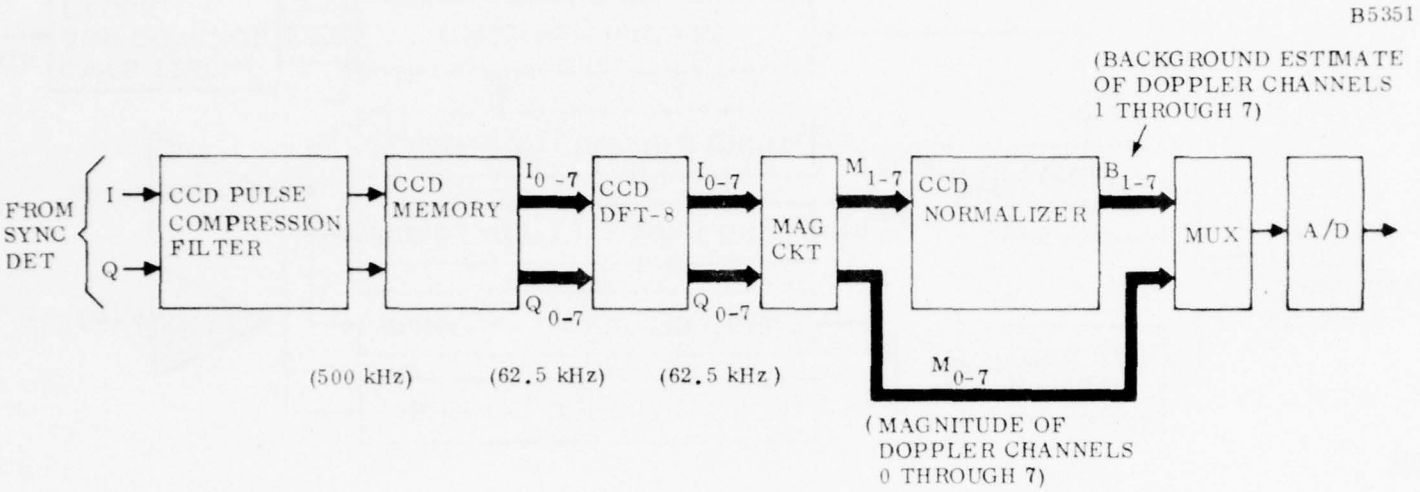


Figure 4-12. CCD Signal Processor

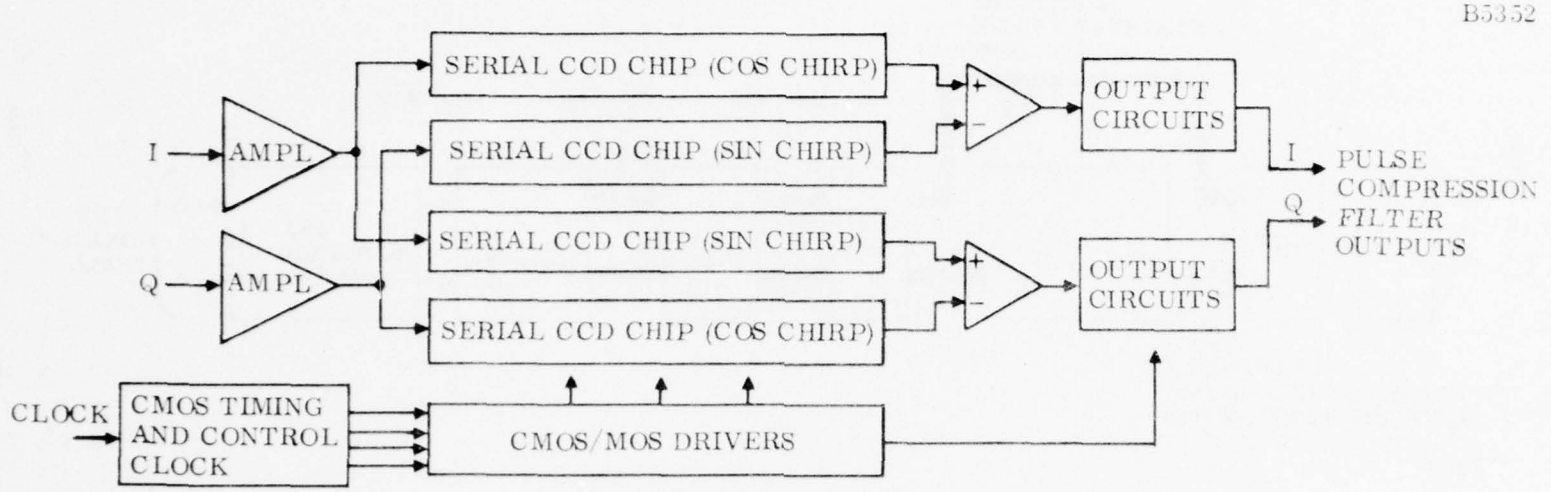
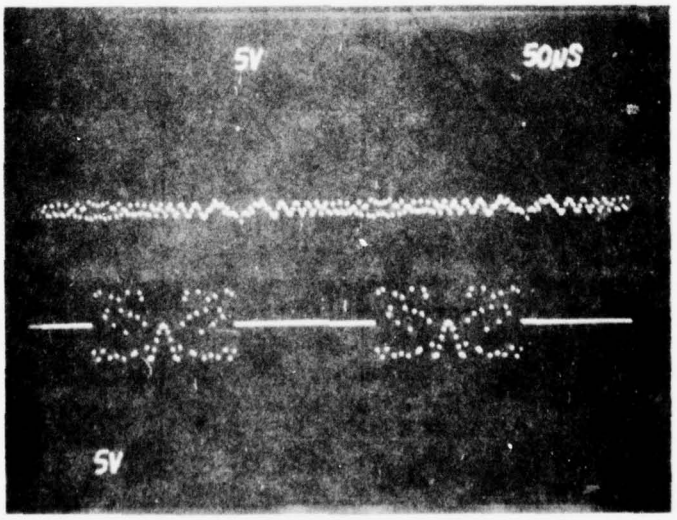


Figure 4-13. Serial CCD Pulse Compression Filter (One Board)

Power consumption is minimized by using low-power operational amplifiers (HA2700) and CMOS timing and control logic. Power consumption for the PC filter operating at 500 kHz is approximately 0.5 W.

General Electric has been building and evaluating mask programmable CCD transversal filters for several years. Impulse responses of these devices range from sin x/x, (low-pass filters), to LFM chirps (chirp z transforms and LFM pulse compression filters).

Figure 4-14 illustrates the matched filter response after Sample/Hold (S/H), and the impulse response of a sine chirp transversal filter. This CCD is being clocked at 500 kHz and has a quadratic phase function corresponding to a time bandwidth product of 64. Detailed measurements on this CCD chirp filter were made to determine its linear dynamic range. Figure 4-15 illustrates the transfer function of the CCD. The input level corresponding to the 1-dB compression point of the output occurs at an input of 8.5 V p-p. However, from a system standpoint, operating at this level introduces an additional SNR loss of nearly 1 dB. Thus, the 0.1 dB compression point, (6.5 V p-p at the input) will be used for the maximum input signal for *linear operation.*



Time 50 μs/Div

Upper Trace - Sine chirp matched filter response
Vertical scale = 5V/Div

Lower Trace - Sine chirp impulse response
Vertical scale = 5V/Div

Figure 4-14. CCD Matched Filter Response and Impulse Response At 500 kHz Clock Rate After S/H

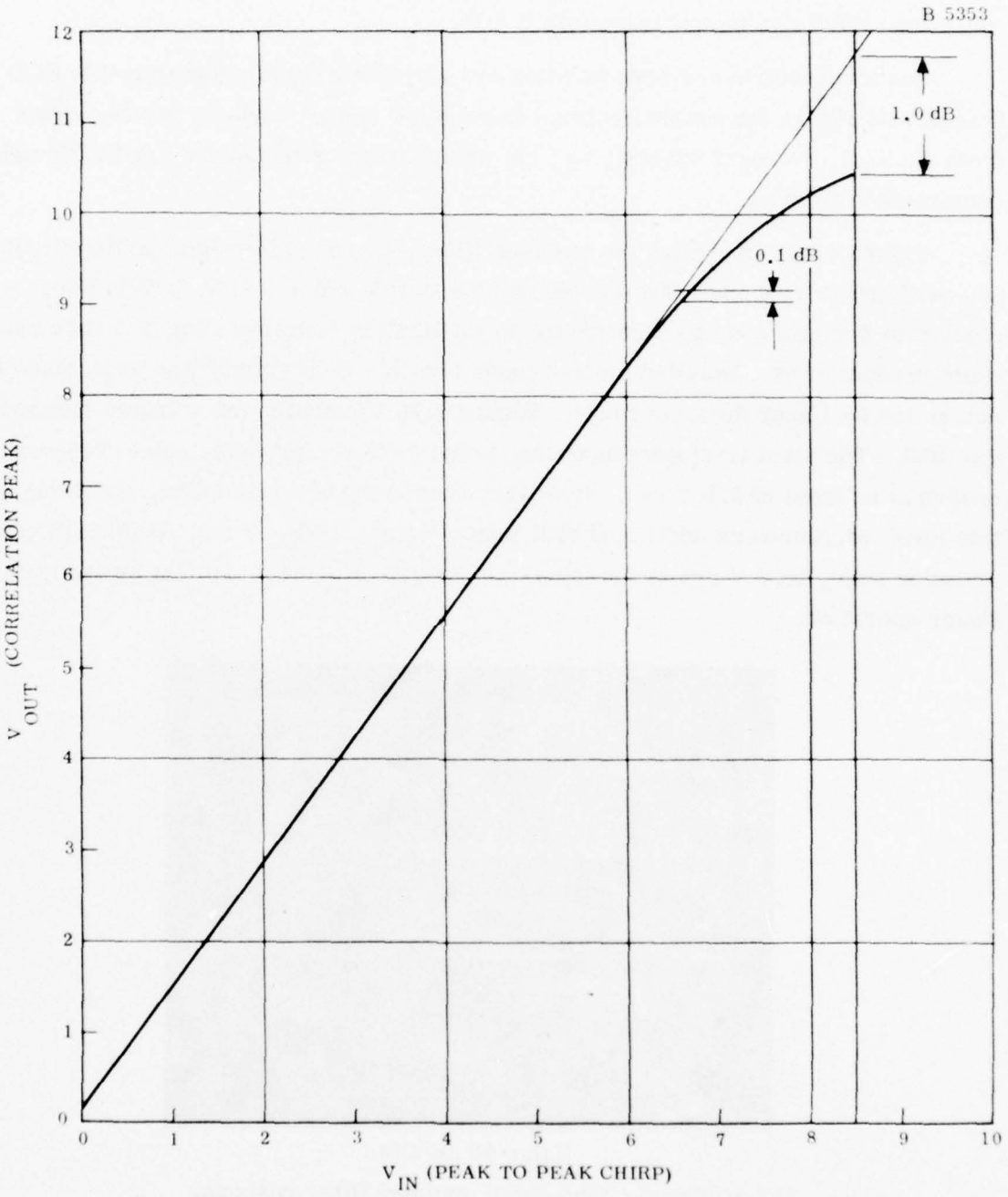


Figure 4-15. Experimental Transfer Function of CCD Sine Chirp Matched Filter

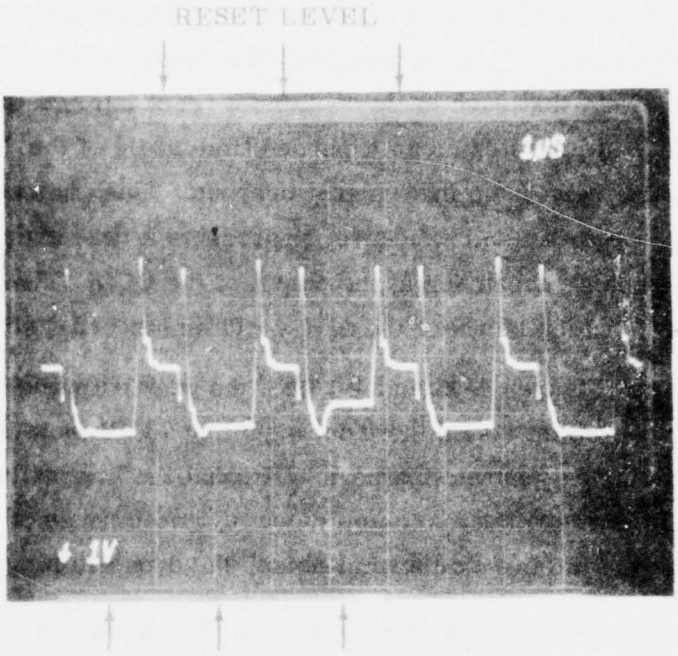
SNR of the CCD chirp matched filter is described via the following experimental data. Figure 4-16(a) illustrates the CCD output prior to S/H with an input signal present. Note that each cycle contains a reset interval prior to the valid signal level. Figure 4-16(b) illustrates an expanded time scale of the CCD signal output for the case where there is no input signal present. This photograph, taken from a 20 MHz oscilloscope with a 4-s exposure, represents a time averaged sample of the internally generated noise appearing at the output of the CCD. The noise level near the knee of the curve, which is where the S/H would be strobed, is approximately 2 mV.

From Figures 4-15 and 4-16(b), the peak output SNR of the device is determined to be 73 dB. Decreasing the input signal by 73 dB from the 0.1 dB compression point, the output correlation peak will equal the internally generated noise. Thus, this CCD device has a maximum output dynamic range of 73 dB. However, in an operational system with thermal noise, the dynamic range will be degraded slightly.

Improved device dynamic range performance will be obtained by reducing the internal generated noise through use of the proper S/H scheme. Additional improvement, if required from a system viewpoint, can be obtained by including special low-pass filters at the P/C output.

CCD pulse compression filter limitations, other than SNR effects, include tap weight accuracy and charge transfer inefficiency. Both of these effects are interrelated and depend on the physical geometry and clocking rates of the CCD device. Tap weight accuracy, as in the digital implementation, results when ideal multiplier coefficients are rounded to predetermined number of bits. Due to limitations of the equipment that generates the tap weights, typical tap weight quantization is 1 part in 600. Charge transfer inefficiency, which has a bandlimiting effect, increases as a function of the clock rate. A digital computer simulation of the CCD PC filter (BT 32, clocked at 500 kHz) with currently achieved values of tap weight quantization and charge transfer inefficiency indicated extremely small amounts of mainlobe broadening and negligible sidelobe degradation compared to an ideal reference case.

(a) Expanded CCD Matched Filter Output Prior to S/H



(b) Expanded Unfiltered Waveform (Signal Region) Illustrating Internally Generated Noise

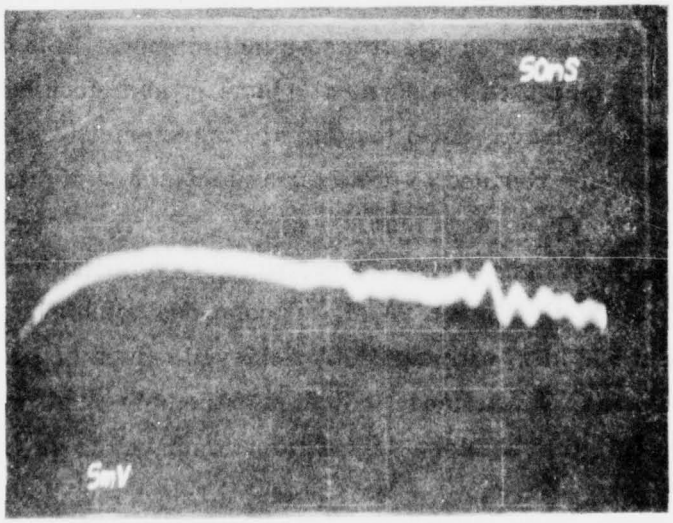


Figure 4-16. CCD Sine Chirp-Matched Filter Output Waveform

b. DOPPLER PROCESSOR

Charge coupled devices represent an efficient, low-power, low-cost technique to perform Doppler processing of a burst waveform. Doppler processing of an eight-pulse burst requires that return data be formatted on a range cell-by-range cell basis from each of the eight pulses, before processing by an FFT-8 or DFT-8. Thus, a memory is required to store data from the desired number of range cells, for each pulse. This memory must be organized to simultaneously output data for a given range cell for each of the eight pulses. Reduced DFT-8 computation rates are achieved by using a rotating buffer memory; while data is being written into one memory, data from the previous diversity frequency channel burst is read into the DFT-8 processor. Figure 4-17 shows a block diagram of an analog CCD Doppler Processor for an eight-pulse burst.

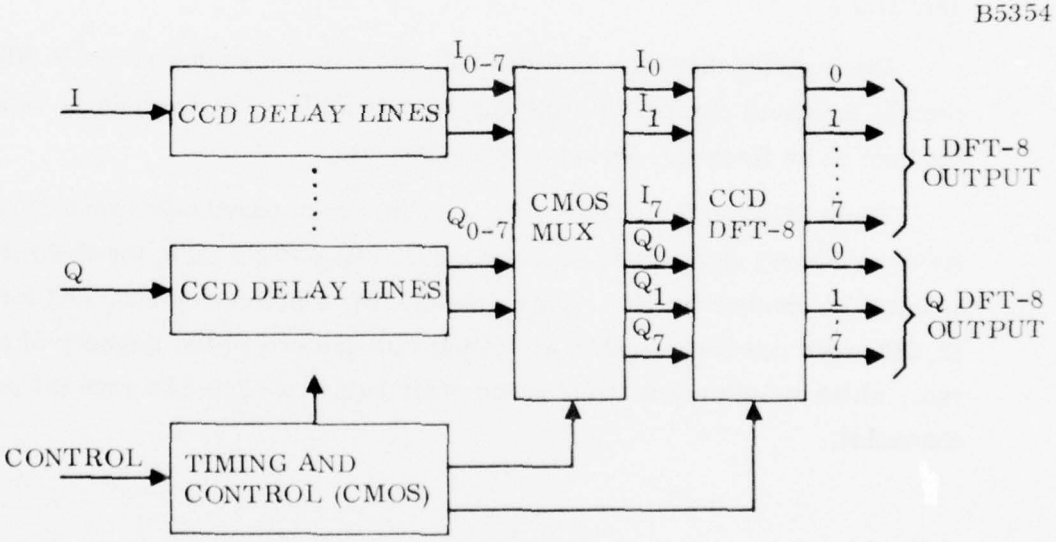


Figure 4-17. CCD Doppler Processor

Several CCD techniques are available to implement the rotating buffer memory. Although the minimum number of range cells required is 362, the CCD rotating memories will be designed for 384 range cells because they come in 128-cell segments. Total storage requirements for the rotating memory is 12,288 real analog words, and maximum storage time is approximately 7 ms. This provides dual storage so that input is made to one memory while the other is output to the DFT-8 for I and Q signals over eight interpulse periods. General Electric is currently developing a high-density CCD memory that will be compatible with the CCD DFT-8. A CCD memory, using commercially available CCD's (Reticon 128LR) is sized for the rotating matrix memory. A total of 48 CCD's are required to store the 8 Pulse Repetition Intervals (PRI's), 384 range cells of complex (I, Q) data. A dual-memory of twice this size (i.e., 96 Reticon 128LR CCD's) will be provided so that data is read from one memory while simultaneously writing into the other memory. Typical device parameters include 500-kHz bandwidth, 70-dB SNR, and typical retention time of 5 s.

Input analog data at a 500-kHz rate from the pulse compression filter is multiplexed, via gated clocks, into the appropriate CCD. The memory is configured to read out on 16 lines (8I, 8Q) at a 62.5-kHz rate.

Eight identical boards (7.7 in. x 11 in.) each board containing 12 CCD's and their peripheral equipment, are required. The control logic for this memory is mounted on another board. Approximately 6W of power are required for the rotating 12,288-word memory capable of writing into one half of the memory at a 500-kHz rate, while simultaneous reading the other half at a 62.5-kHz rate (16 parallel channels).

c. MAGNITUDE ESTIMATION, CCD NORMALIZER, AND DIGITAL INTERFACE CIRCUITS

Background estimation, used in a normalization function to obtain CFAR, is performed on Doppler channels one through seven. Figure 4-18 illustrates the block diagram of the magnitude estimation circuitry, CCD normalization, and digital data interface.

Figure 4-19 illustrates a magnitude detection circuit. The first section computes the absolute value of the bipolar I and Q channel samples. The latter portion estimates the magnitude via the algorithm.

$$MAG = |L| + \frac{1}{2} |S|$$

where

L = largest (I, Q) sample

S = smallest (I, Q) sample

Again, low-powered operational amplifiers and comparators are used exclusively in this magnitude estimation circuitry. Approximately 0.4 W are required for the magnitude detectors.

General-purpose analog squaring circuits were also considered for the magnitude estimation circuitry. However, they were rejected on the basis of their limited dynamic range (approximately 24 dB) due to internally generated noise, as well as their marginal temperature performance.

A finite impulse response of length 37 is used for background estimation. The specific impulse response implemented is:

$$\bar{B}_j = \frac{1}{32} \sum_{i=-18}^{i=+18} a_i M_{ij} \qquad (4-1)$$

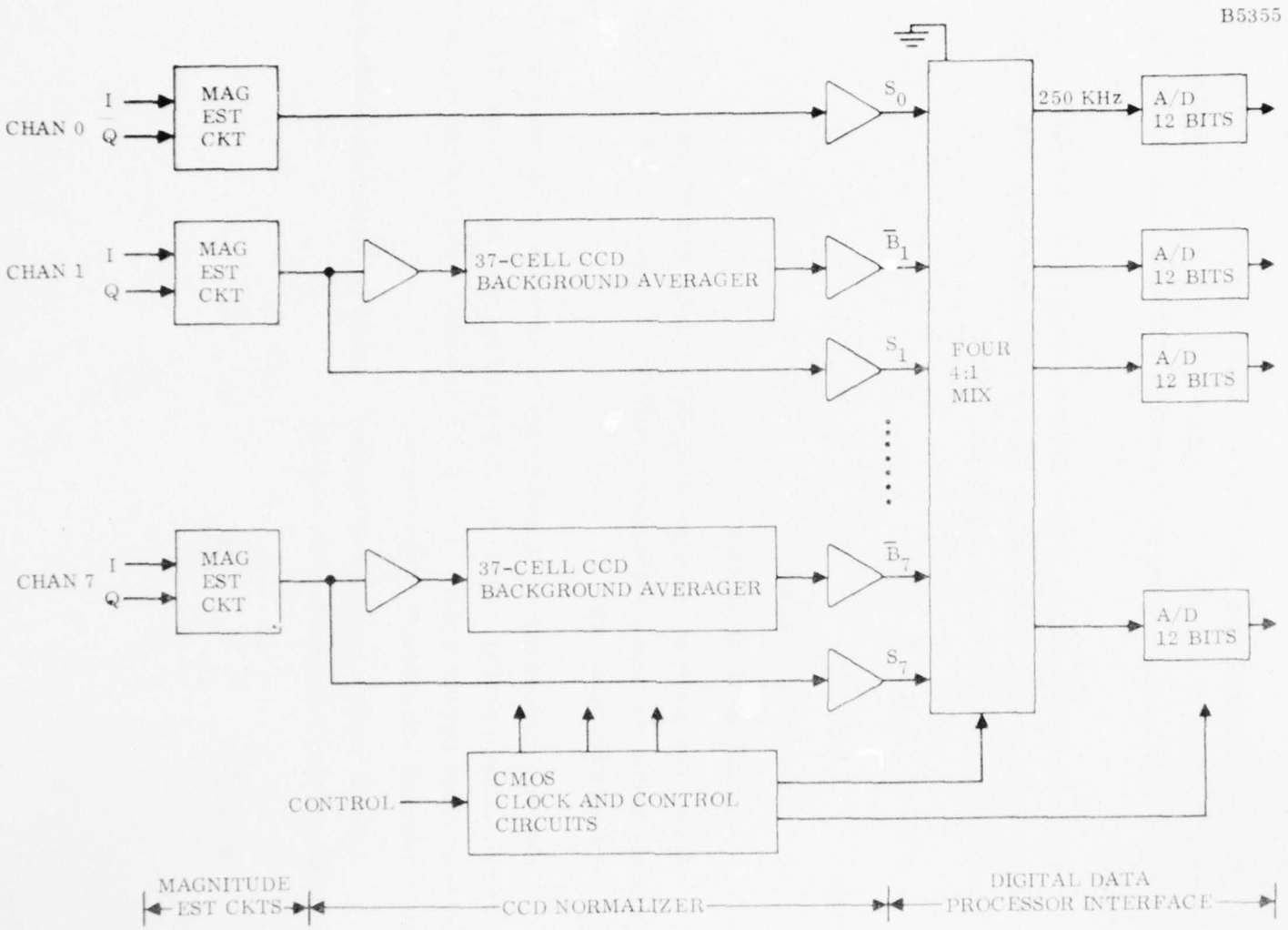


Figure 4-18. Magnitude Estimation Circuit, CCD Normalizer and Digital Data Interface

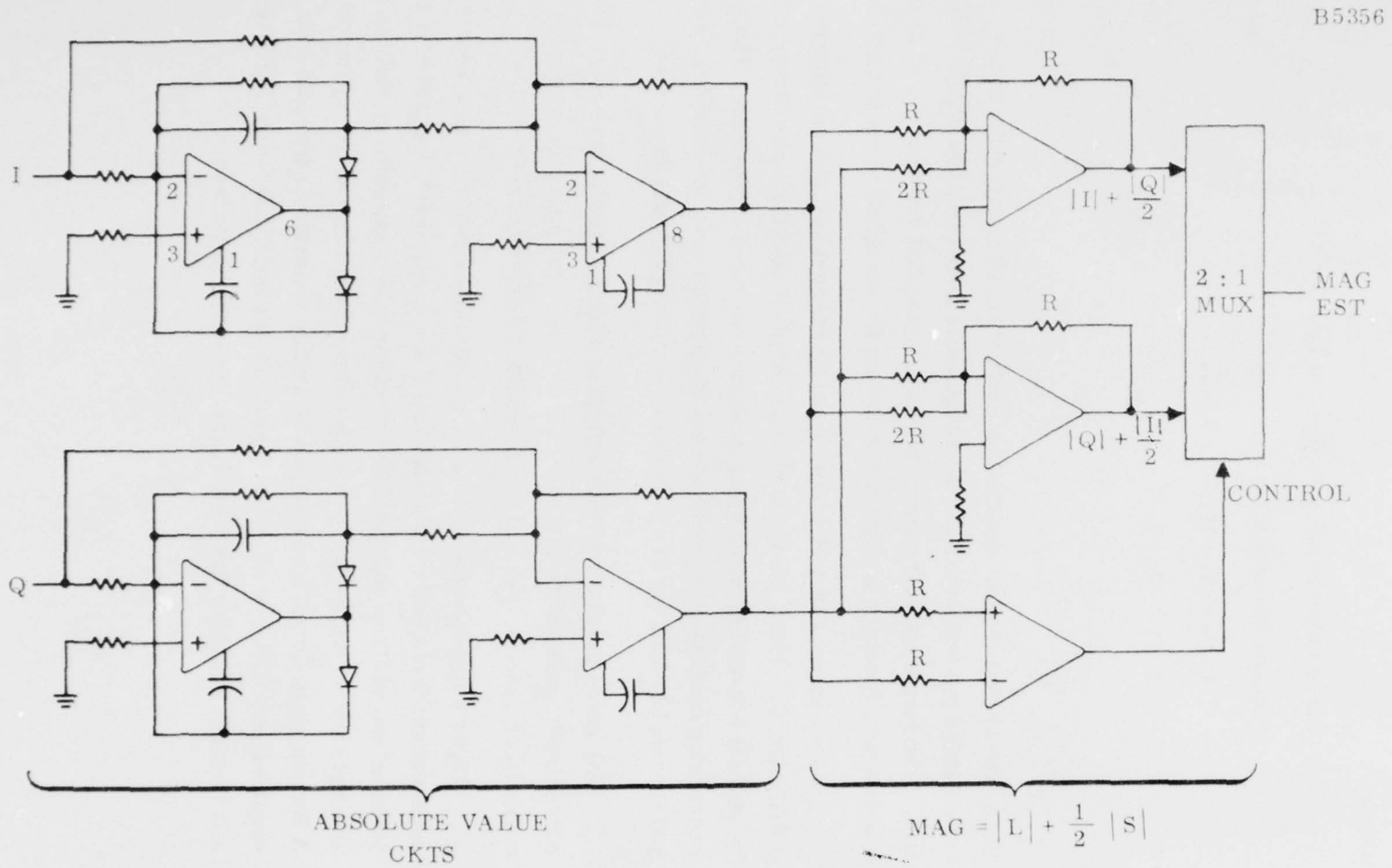


Figure 4-19. Magnitude Detection Circuit

where

i = range index relative to the test cell (i = 0)

j = Doppler bin index

$$a_i = \begin{cases} 1; & i = -18, -17, \ldots -3, +3, \ldots +18 \\ 0.; & i = -2, -1, 0, 1, 2 \end{cases}$$

$$M_i = \sqrt{I_i^2 + Q_i^2}$$

Thus, the background is obtained by estimating 16 range cells before, and 16 range cells behind the test cell with two range cells guard band on either side of the test cell. The required CCD normalizer is a simplified version of a CCD normalizer that General Electric is currently building for an infrared sensor application.

Normalizer output circuits, for both the test cell and background channels, have a S/H circuit. Thus, all channels are sampled (strobed) simultaneously and quantized by an A/D converter, after being multiplexed into a single line. The remaining processing operations of noncoherent integration over the four 8-pulse burst outputs and threshold detection are performed in the digital data processor.

All seven normalizer channels plus required timing and control circuitry are conveniently mounted on a single board. The total power consumption for the seven normalizer system, clocked at 62.5-kHz, is approximately 0.5 W.

Digital data processor interface with the CCD normalizer requires a 16:1 analog multiplexer, 8 channels for signal and 8 for background, toggled at a 1-MHz rate. Since all normalizer channel S/H output circuits (test cells as well as background average) are strobed simultaneously; channel-to-channel time jitter is minimized. A Harris multiplexer converts the 16 analog channels to four 250-kHz channels and requires only 120 mW of power. Four 12-bit Datel ADC-N A/D converters, requiring 3.3 W each, provides the digital data processor interface.

d. LOW-POWER HIGH-RELIABILITY DESIGN SUMMARY

Low-powered CCD signal processors are extremely reliable. This reliability, as well as performance monitoring and fault location, can be further improved by designing redundant systems. Figure 4-20 illustrates a block diagram of the redundant CCD signal processor for the Unattended Radar.

Under normal conditions, two identical CCD PC filters process alternate frequency diversity channels. The input multiplexing is accomplished by gating-on the clocks to the appropriate CCD's. Each CCD PC filter outputs are stored in a 6144 analog word CCD memory. After proper formatting, the eight parallel complex data lines from the matrix memory are the inputs for the CCD DFT-8. Magnitude estimation, normalization, and A/D conversion follows the CCD Doppler processor.

In the event that either a CCD PC filter and/or a CCD DFT-8 fails, the control circuitry will route the data without any performance degradation. Failure of a complete 6144 CCD matrix memory in this configuration will degrade the performance by loss of half of the diversity channels. However, loss of any row of the CCD matrix memory (384 range cells from a particular PRI) will provide a graceful performance degradation.

Table 4-3 summarizes the implementation and power consumption for the CCD signal processor for the Unattended Radar. The table is organized on a functional basis and presents IC counts, board counts, and power consumption. The top lines for each function represent minimal requirements for the signal processor. Where appropriate, representative numbers for the redundant CCD signal processor of Figure 4-20 are tabulated and shown within parenthesis.

TABLE 4-3. CCD SIGNAL PROCESSOR IMPLEMENTATION/POWER CONSUMPTION SUMMARY

Function	No. of Functions	IC's Per Function	CCD's Per Function	Total No. Large Boards	Total No. IC's	Total No. CCD's	Total Power
CCD Pulse Compressor	1 (2)	55	2	1 (2)	55 (120)	2 (4)	0.5 (0.6)
CCD - Doppler Processor Memory (1,536 words) and 8 Pulse Coherent Processor	8 (8)	66	12	8.9 (9.1)	526 (526)	97 (98)	6.5 (6.6)
Video Magnitude Detector	8 (16)	8	-	1.0 (2.0)	64 (128)	- -	0.4 (0.8)
CCD Normalizer (37 Cell Background Averager)	7 (14)	7	1	1.0 (2.0)	49 (98)	7 (14)	0.5 (0.6)
Digital Data Processor Interface (including 4 A/D)	1 (1)	20	-	1.0 (1.0)	20 (20)	- -	13.6 (13.6)
		TOTAL		12.9 (16.1)	714 (902)		21.5 (22.2)

Large board = 7.7 in. x 11 in.

( ) = for redundant system of Figure 4-20

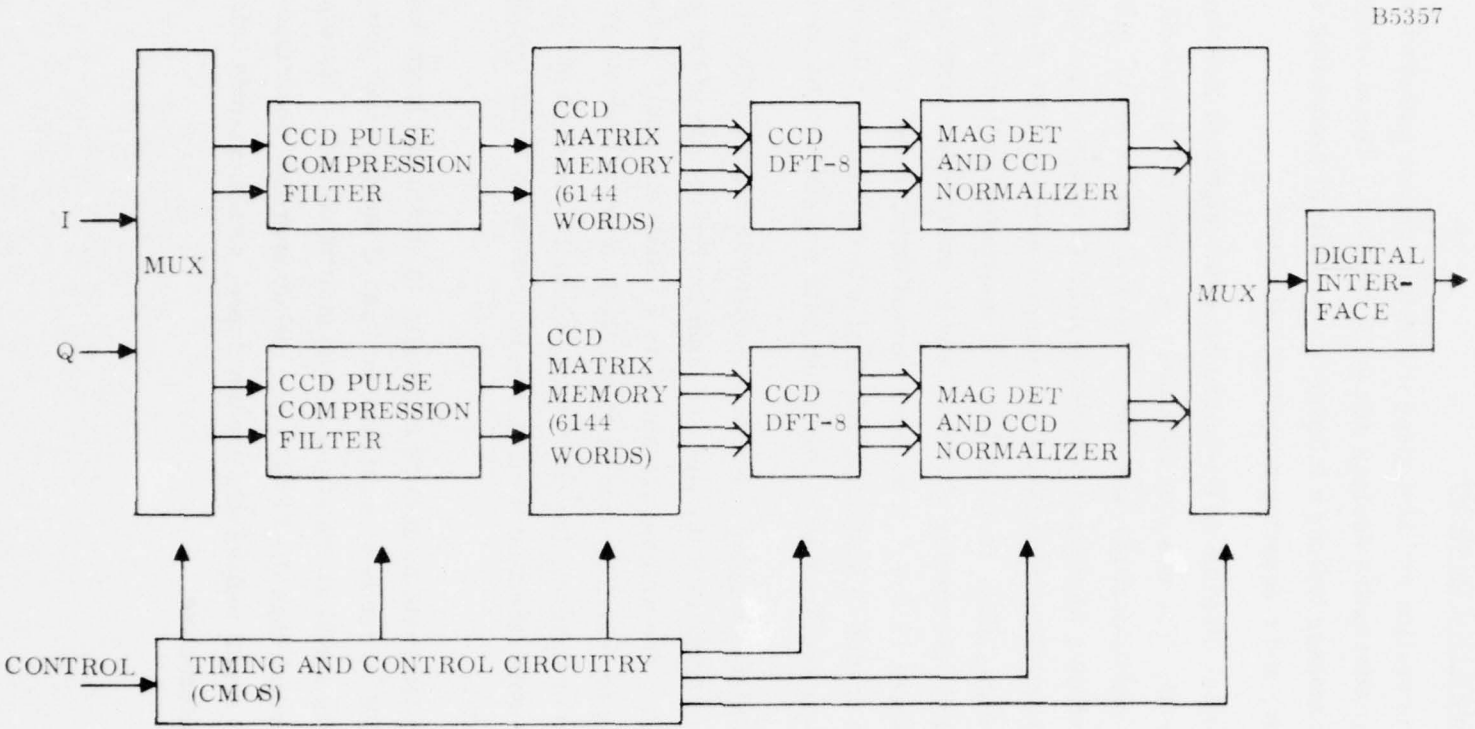


Figure 4-20. Redundant CCD Signal Processor

5. REJECTED DESIGNS

This section includes some of the information gathered in the process of evaluating the alternative designs that were rejected. The alternative designs for the signal processor include a microprocessor signal processing element, a DFT Doppler processor, and a squaring magnitude calculator.

A block diagram of the microprocessor signal processing element is shown in Figure 4-21. The complex multiplier is shown in Figure 4-22. It was added because complex multiplications are such an integral part of signal processing that it is logical to include a hardwired complex multiplier to speed up program execution times. This multiplier could multiply two complex numbers with 16-bit real and imaginary parts in 2 μs, which is equivalent to 5 instruction cycles of the microprocessor. The whole signal processing element would be put on two boards using 80 IC's and requiring about 17.5 W. It was determined that at least 16 of these processing elements would be needed to handle the required data rate for just the pulse compression. The total power required using these elements was found to be unacceptably high.

The DFT Doppler processor is shown in Figure 4-23. It represents a direct attempt to implement the DFT by summing the results of the complex weighting of the input data. The weights are stored in a PROM and could include any additional weighting for sidelobe suppression. Each of these processors could only process one Doppler channel, thus 8 of them would be required and the resulting power requirements (about 50 W) is excessive compared to the Doppler processor described previously.

An alternate magnitude calculator is shown in Figure 4-24. It calculates the value of M^2 directly by squaring the I and Q inputs. Low power Schottky is used along with serial arithmetic to do the multiplications. More power is consumed by this approach than the PROM table lookup approach described previously. However, if CMOS serial multipliers are developed, this magnitude calculator would be the better alternative.

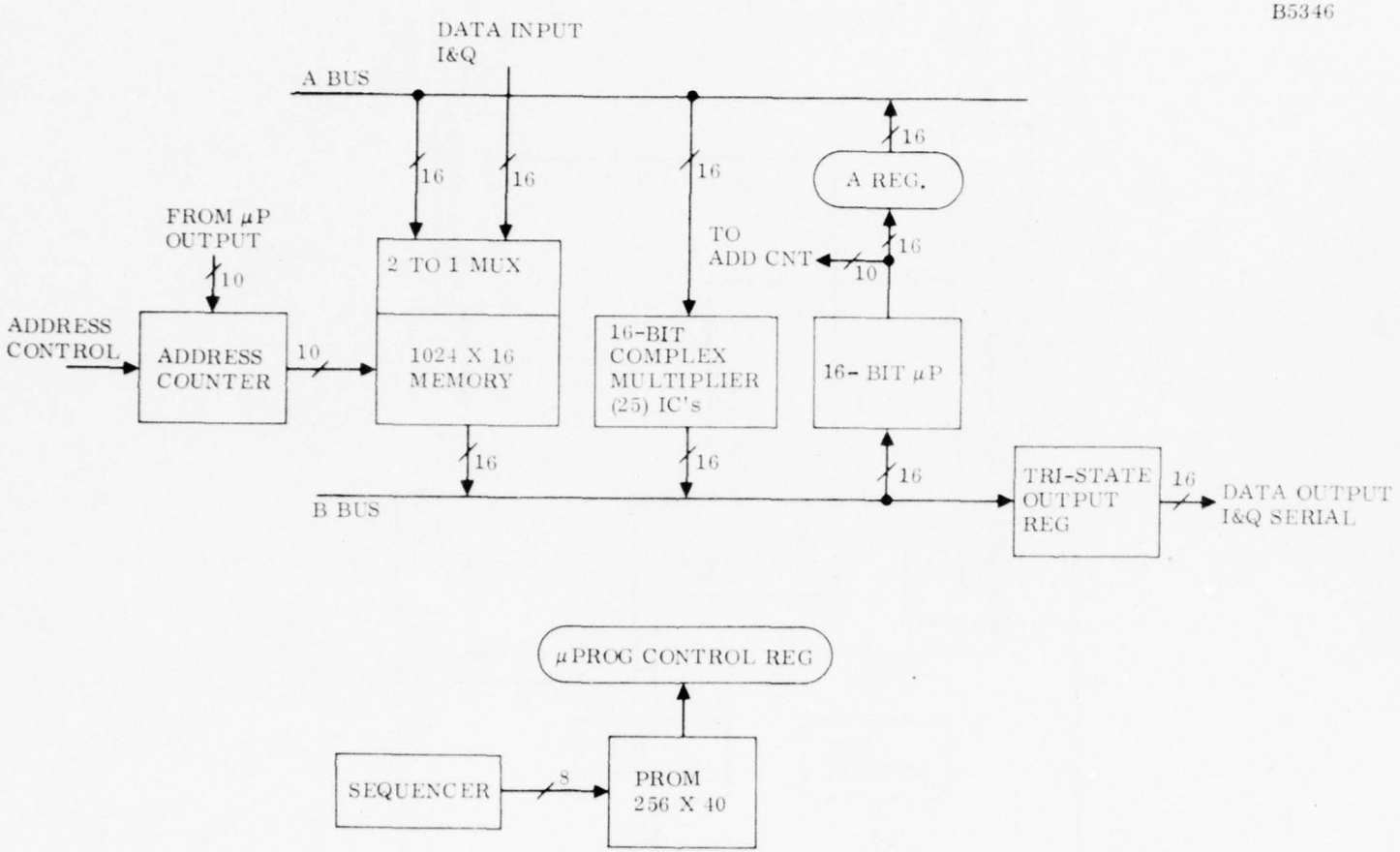


Figure 4-21. 16-Bit Signal Processing Element (2 MHz, 400-ns Cycle Time)

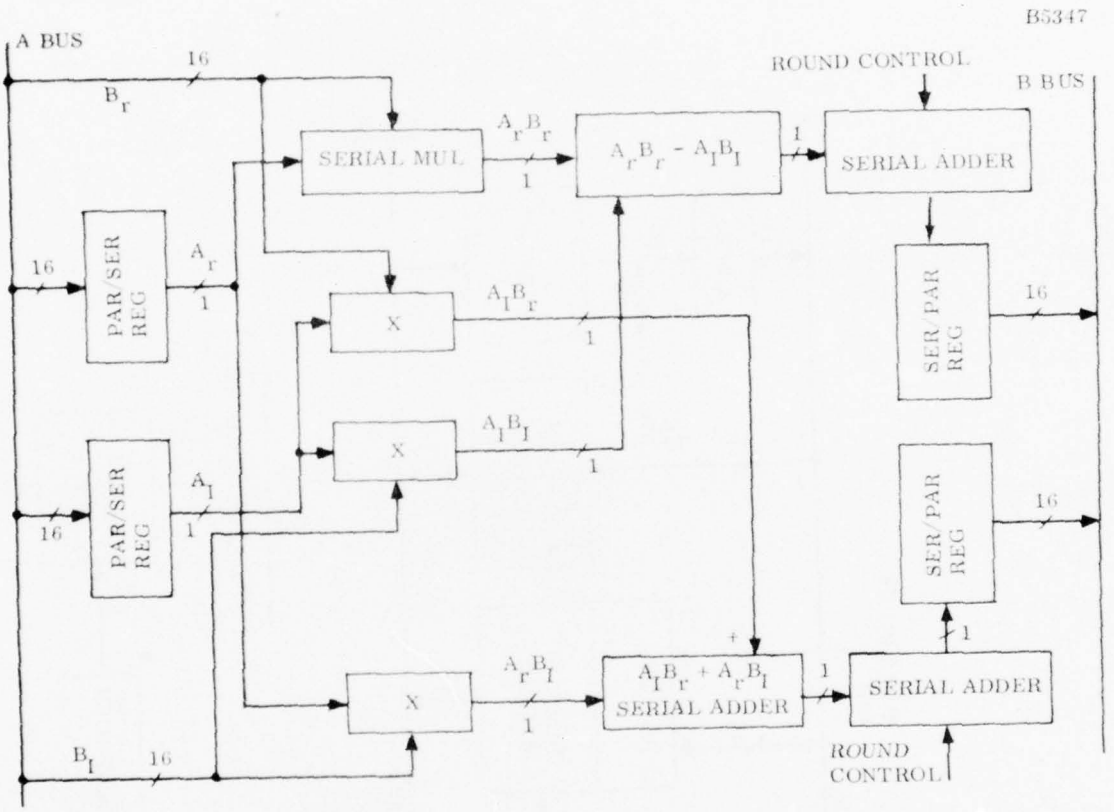


Figure 4-22. Serial Complex Multiplier

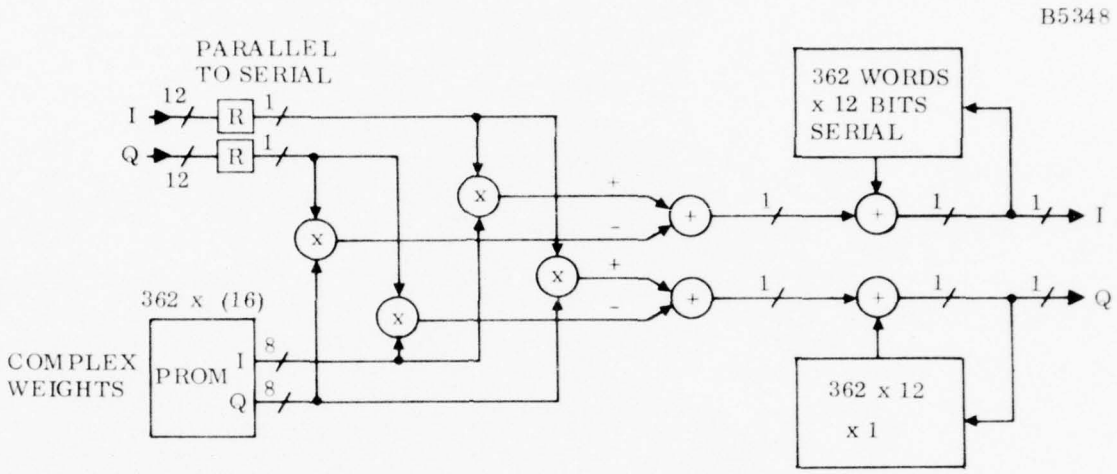


Figure 4-23. One of Eight Serial Arithmetic DFT Doppler Processors

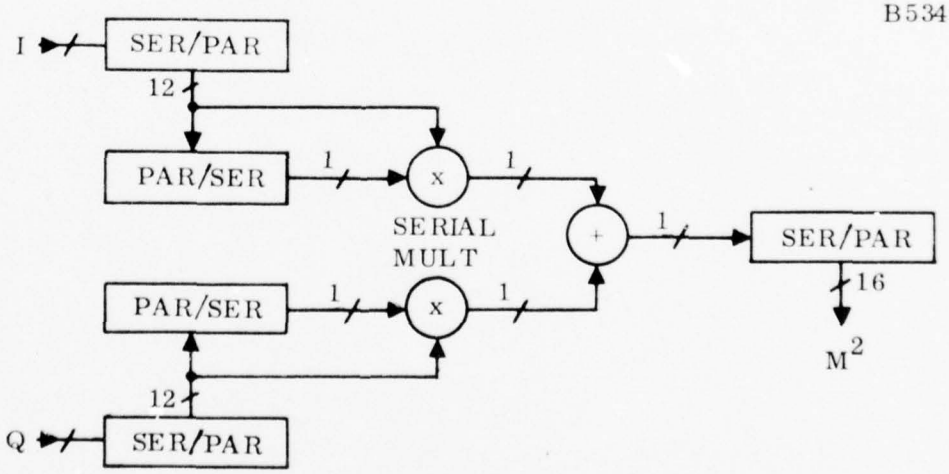


Figure 4-24. A Squaring Magnitude Calculator

SECTION V

DATA PROCESSING SUBSYSTEM REQUIREMENTS

The following sections describe the Data Processing Subsystem components and requirements for the Unattended Radar. A summary of the overall data processing function is first presented, followed by a detailed discussion of each of the primary functional components.

1. SUMMARY DESCRIPTION

The Data Processing Subsystem for the Unattended Radar is responsible for all system control, function scheduling, postdetection processing, target information processing, and Performance Monitoring/Fault Detection Location (PM and FD/L) reporting. The major Data Processing Subsystem components, and their relationship to the total radar system, is shown in Figure 5-1. The primary control and data flow paths are also indicated on this figure.

Each period of system operation is scheduled and configured by the Data Processor and Control Subsystem. For each period of operation, the Data Processor and Control Subsystem specifies the detailed control information, including the transmit frequency, detection threshold, array steering and weighting, and the radar mode (i.e., radar scan mode or IFF interrogation mode). This control information is passed to the radar synchronizer in the form of coded instructions, which when executed, cause the required timing signals and control information to be output to the array control subsystem, the signal processor subsystem and the IFF data processor. The radar synchronizer decouples the time-critical system control signals from the asynchronous processing and reporting of radar target and performance information.

Outputs from the final receiver are routed to either the signal processor or the IFF data controller depending on the radar mode. The Unattended Radar incorporates an integral IFF capability for the purpose of identifying targets which have been detected via their skin returns. Individual targets are interrogated by interrupting the normal radar scan. The IFF data controller accepts the final receiver video outputs produced by the IFF transponder returns, and performs the pulse detection and bracket decoding functions. The IFF data controller then outputs the reply code corresponding to the decoded brackets for defruiting and correlation with the interrogated target tracks in the Data Processor.

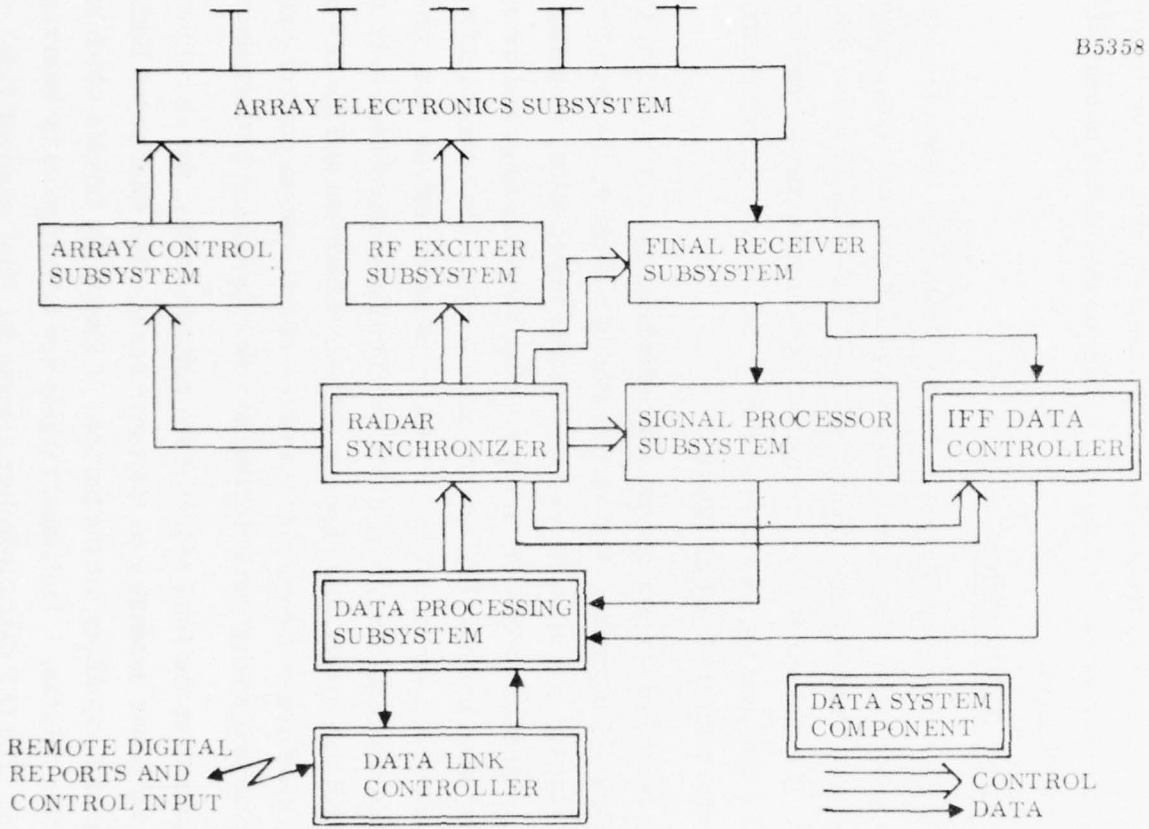


Figure 5-1. Unattended Radar Configuration

In the normal radar scan mode, the outputs from the final receiver are routed to the signal processor. The signal processor performs pulse compression and Doppler processing, and outputs the magnitude of the Doppler processor outputs to the data processor. The data processor then performs the postprocessing functions required to detect target returns, initiates and maintains tracks associated with the target returns, and outputs the target track reports to a remote manned site via the data link controller.

The Unattended Radar also accepts control inputs and operator requests from the manned remote site via the data link controller.

The major functional modules of the Data Processing Subsystem required to perform the above defined tasks are shown in Figure 5-2. The detailed requirements for each of these functions is discussed in the following paragraphs.

The timing and storage estimates included in the subsequent paragraphs were based on lower-level design flow charts which reflected assembly language coding of the envisioned processes. Multiplication (16:1) and division (32:1) were appropriately weighted relative to the load/store and add/subtract instruction classes in the derivation of instruction cycles. Additional efficiencies can be gained in terms of memory requirements and processing time in the actual hardware implementation via the memory access architecture as described in the subsequent implementation paragraphs. The timing and storage budgets establish a baseline to enable definition of an appropriate data processor architecture and identification of those real-time software functions which must be optimized for speed by microcoding critical sequences.

2. RADAR DATA INPUT PROCESSOR

The Radar Data Input Processor accepts the magnitude outputs produced by the signal processor following Doppler processing. Background estimates produced by the moving range window normalizer in the signal processor are also input to the radar data input processor for use in the detection thresholding process.

Two candidate processing lineups have been considered for the Radar Data Input Processor. The first processing lineup is based on an aligned diversity channel approach. The diversity frequencies (four frequencies/radar dwell) and the PRP are chosen such that all Doppler channels align in velocity, permitting noncoherent integration of the diversity channels without producing a collapsing loss. Blind speed unmasking is then performed utilizing a different set of diversity frequencies and PRP's on alternate radar scans.

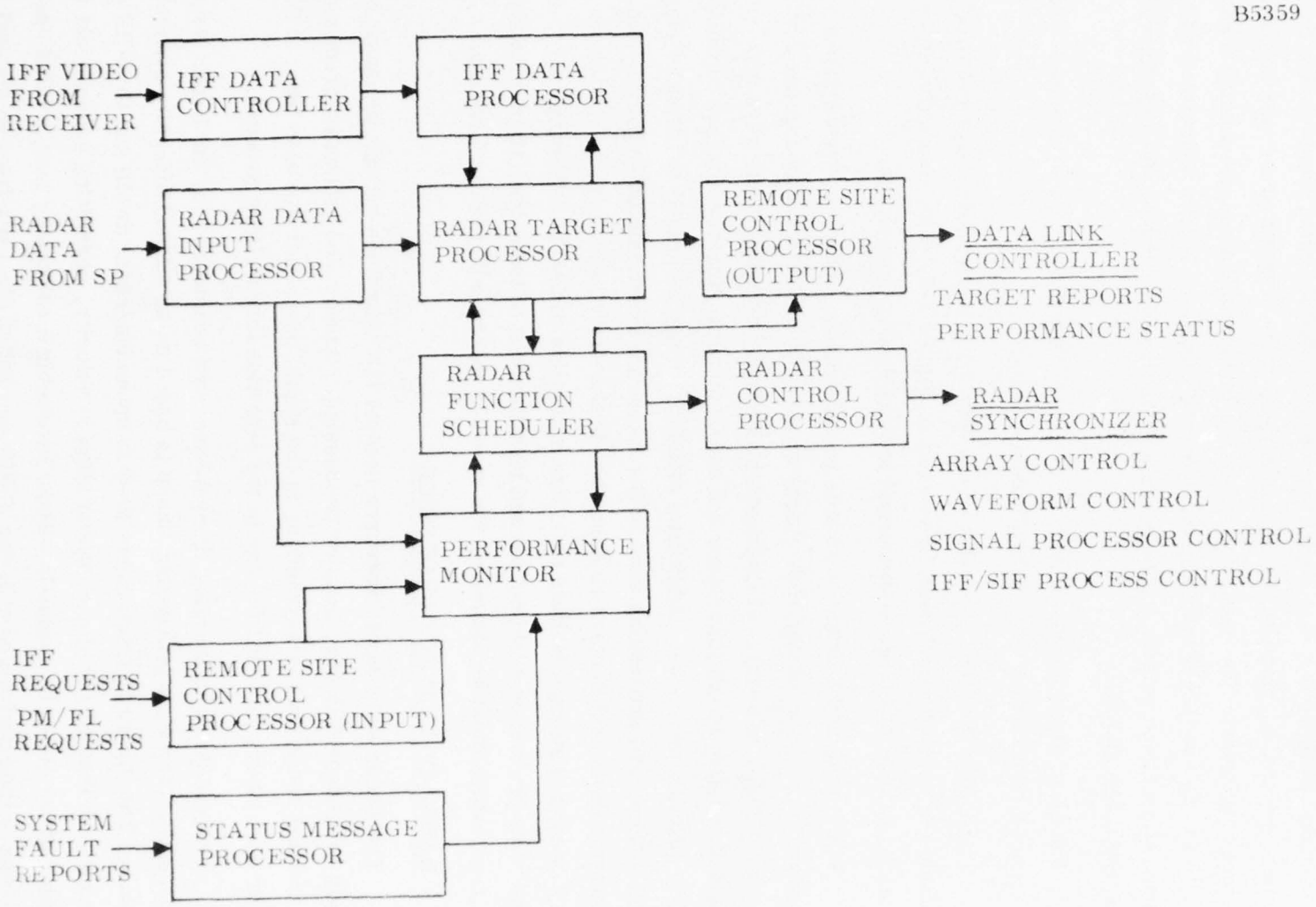


Figure 5-2. Data Processor and Control

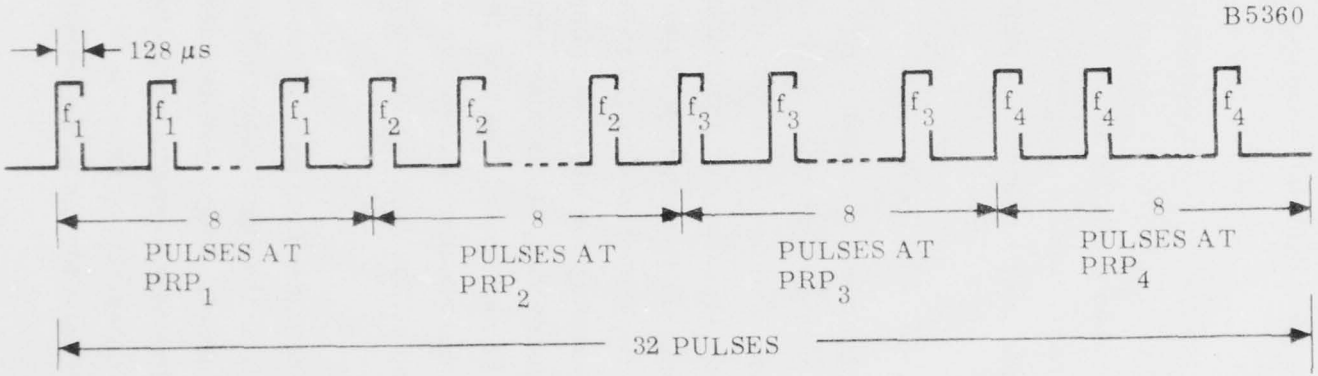
The second processing lineup is based on an unaligned diversity channel approach, in which the PRP is maintained constant, while four-frequency diversity is utilized on each radar dwell. The change in transmit frequency accomplishes blind speed unmasking, but a collapsing loss is now suffered when noncoherent integration of the four-diversity channels is performed due to nonalignment of the Doppler channels in velocity.

The above two configurations were considered to gain insight into the loading imposed on the data processor by the postprocessing functions in order to establish an appropriate interface between the signal processor and the data processor. An interface further back into the signal processor was deemed inappropriate due to the high data rate and processing load demands on data processor configuration, compared to alternate techniques available.

a. RADAR DATA INPUT PROCESSOR - ALIGNED SYSTEM

The aligned system processing requirements are dictated by a four-frequency diversity transmission with the PRP for each pulse group at one frequency varied such that the Doppler filter channels are aligned in velocity. The transmit waveform consists of a total of 32-LFM pulses of 128-us duration, with 8 pulses transmitted at each of four frequencies on each radar dwell in a single azimuth position (see Figure 5-3). Using the nominal PRP of 0.852 ms, the Doppler processor (FFT-8) generates an output every 8 pulses, or every 6.8 ms. Assuming a complex sampling rate of 500 kHz (2:1 oversampling of the 250-kHz signal bandwidth), the Doppler processor output consists of 8-Doppler samples for each of 362 range bins. The input to the Radar Data Input Processor thus consists of 2896-magnitude samples together with the corresponding moving window normalizer background estimates for each magnitude sample in each 6.82 ms period.

The processing requirements for the Radar Data Input Processor are shown in Figure 5-4. The magnitude samples from the signal processor are input following Doppler processing for each diversity channel. Each range-Doppler cell is then noncoherently integrated over the four-diversity transmissions, with a running summation computed following each doppler processing cycle. The zero-Doppler channel is utilized to update a clutter map estimate for use in the detection threshold



DIVERSITY CHANNEL	NOMINAL FREQUENCY (GHz)	NOMINAL PRP (ms)
1	1.215	0.916
2	1.245	0.894
3	1.275	0.872
4	1.305	0.852

3.534 ms x 8 = 28.27 ms/DWELL

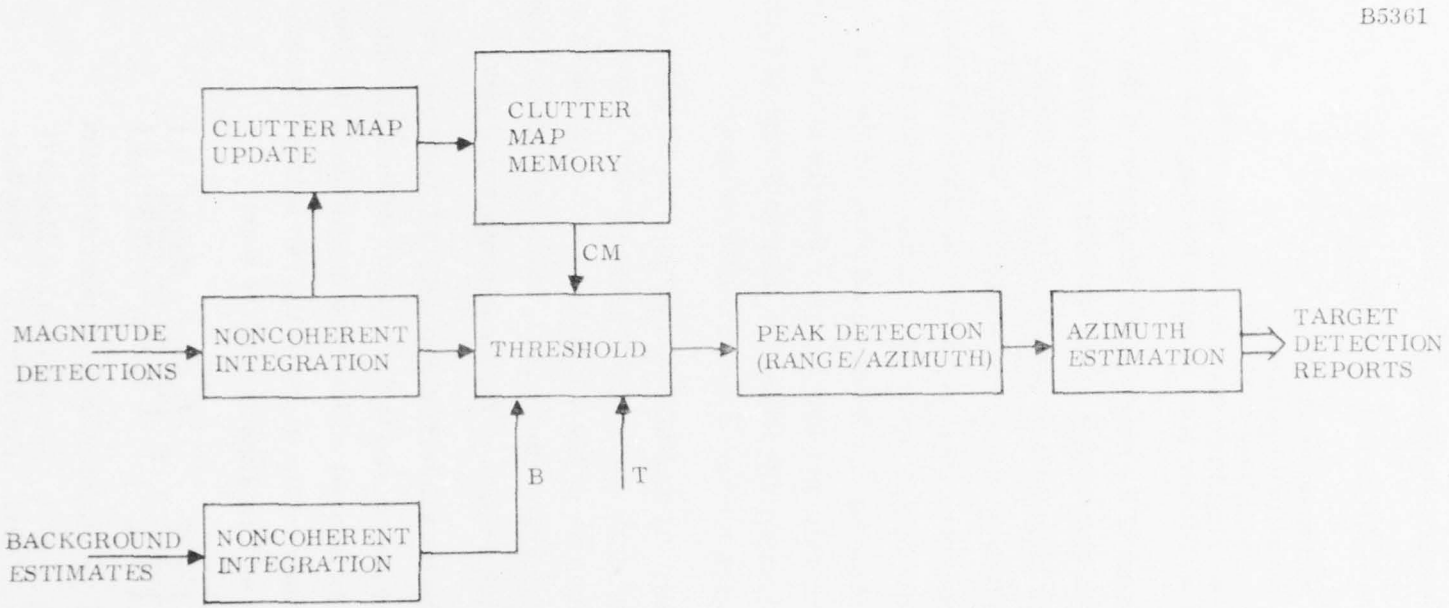


Figure 5-4. Radar Data Input Processor Aligned System

logic. A recursive filter is utilized to update the clutter map estimate for each range bin by the new zero-Doppler magnitude estimate;

$$CM_{NEW}(i, j) = \alpha\, M(i, j) + (1 - \alpha)\, CM_{OLD}(i, j)$$

where
- i = range bin index
- j = azimuth position
- α = weighting constant
- M = Magnitude estimate for current dwell
- CM = Clutter Map estimate for range bin i and azimuth beam j

(5-1)

Upon completion of the noncoherent integration of the four-diversity channels and the update of the clutter map, a thresholding operation is performed to ascertain signals of sufficient magnitude to qualify as target returns. For the zero-Doppler channel, the magnitude samples must exceed the largest of the thresholds from the clutter map, or the stored constant threshold. Process throughput is enhanced by utilizing the stored constant threshold to reduce the number of signal returns which must be tested against the remaining thresholds, as the clutter map threshold requires more slower-rate memory accesses than the stored constant threshold. Each data point which successfully passes the threshold logic is flagged in moving the data to a three-beam store for subsequent azimuth estimation.

Before performing azimuth estimation, peak detection in range and azimuth is performed. The local maxima of the signals which have been flagged as having passed the detection thresholds are isolated by testing each detection, first against the pair of adjacent range returns at the same azimuth and Doppler and then against the adjacent azimuth returns at the same range and Doppler.

Following the peak detection process, all those data points which remain tagged as valid detections are passed to the azimuth estimation algorithm. A fine-grained azimuth estimate is derived utilizing the magnitude of the peak detection together with the largest magnitude return in one of the two adjacent beams. The azimuth estimation is performed with an algorithm of the form:

$$P_{AZ}(i) = k \left\{ \frac{1}{2} \left[1 - K \left(\frac{Mag(i) - Mag(b)}{Mag(i) - Mag(b)} \right) \right] \right\} \qquad (5\text{-}2)$$

where
- i = Beam position of peak detection
- $b = \begin{cases} i-1 & \text{For } Mag(i-1) \geq Mag(i+1) \\ i+1 & \text{For } Mag(i+1) > Mag(i-1) \end{cases}$
- $k = \begin{cases} -1 & \text{For } b = i-1 \\ +1 & \text{For } b = i+1 \end{cases}$
- K = Beam shape constant

An indication of processing throughput requirements may be derived by considering the buffer management shown in Figure 5-5. Storage is allocated for the magnitude samples from the signal processor which are input at a rate of 2896 samples every 6.82 ms. The magnitude samples must then be noncoherently summed into the noncoherent summation buffers following completion of the Doppler processing for each diversity channel. Noncoherent integration is not performed following Doppler processing of the first diversity channel, but instead the role of the magnitude storage buffers and the noncoherent summation buffer are simply reversed. Noncoherent integration must be performed within 6.82 ms to avoid loss of data. Similarly, thresholding must be completed within 13.64 ms, to avoid loss of data upon completion of Doppler processing of the second diversity channel from the next beam position. The peak detection and azimuth estimation processing can be smoothed over the entire beam dwell period (nominal 27.28 ms). Storage requirements and processing rates are summarized in Table 5-1.

TABLE 5-1. RADAR DATA INPUT PROCESSOR LOADING AND STORAGE

CPU LOAD

	Instructions	Processing Cycle	Process Time (ms)	Require Cycle Time (μs)
Noncoherent Integration	20	28,966	6.82	0.235
Clutter Map Update and Threshold	46	35,838	13.64	0.381
Peak Detection and Azimuth Estimation	39	14,635	27.28	1.86

STORAGE

	16 Bit Words
Magnitude Store	2,896
Noncoherent Summation	2,896
Background Estimates	2,896
Background Noncoherent Sum	2,896
Three Beam Store	8,688
Clutter Map	52,852

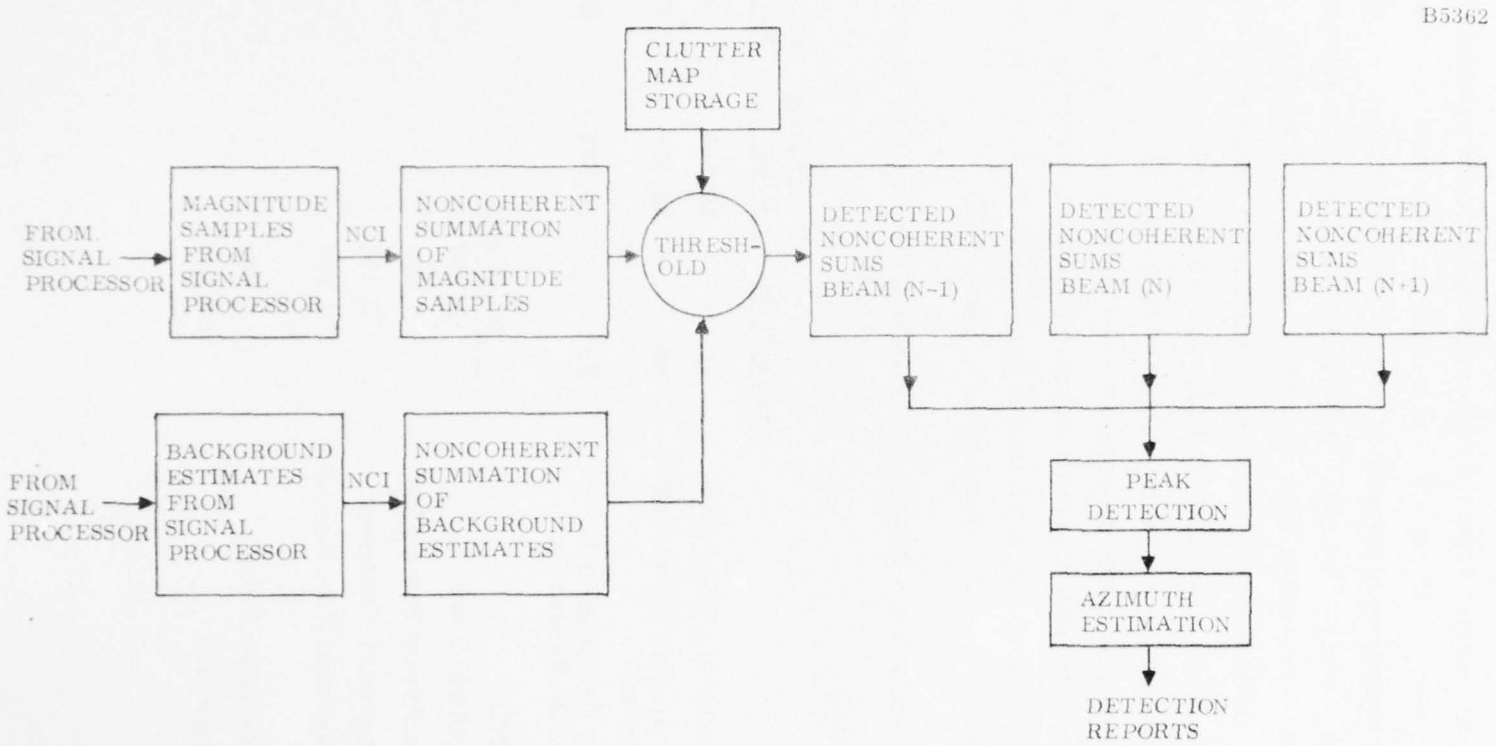


Figure 5-5. Radar Data Input Processor Buffer Management Aligned System

The major throughput rate requirement for the assumed buffer management approach is the noncoherent integration processing, which must be performed at a rate of 0.235 μs per instruction to avoid loss of data. While these cycle times establish a minimum processing rate to avoid loss of data, the total process load, including the other data processing requirements must be considered to determine total throughput requirements. Since the noncoherent integration process must be performed three times during a radar dwell, the total instructions per dwell for the Radar Data Input Processor can be computed as:

$$\text{Instructions/Dwell} = 3(28,966) + 6878 + 28,960 + 14,635 = 1.37(10)^5 \qquad (5\text{-}3)$$

or

$$\text{Process Rate} = \frac{27.28(10^{-3})}{1.37(10)^5} = 0.2\ \mu\text{s/instruction} \qquad (5\text{-}4)$$

The clutter map represents the single largest block of storage, with the requirement based on storage of a clutter estimate for each range cell (362) at each azimuth position (e.g., 146 azimuth positions for 3° beams and 0.82 packing factor).

b. RADAR DATA INPUT PROCESSOR - UNALIGNED SYSTEM

The unaligned system processing requirements are altered from those of the aligned system due to the fact that the Doppler filters are no longer aligned in velocity. The pulse repetition period remains constant for each diversity channel, so that a target will appear in different Doppler bin positions as the transmit frequency is varied. In order to perform noncoherent integration of the four diversity channels, Doppler compression via a greatest of operation must be performed in each range bin. In addition, before the Doppler compression can be performed, the magnitude samples must be normalized by the moving range-window normalizer background estimate. Finally, the clutter map must be updated before normalization and noncoherent integration, and thus be performed four times per radar dwell period.

The revised processing lineup is shown in Figure 5-6. The peak detection and azimuth estimation functions remain identical to those of the previous aligned system configuration. The clutter map update is performed on the input magnitude samples following Doppler processing of each diversity channel. The noncoherent integration function is performed following Doppler compression, and therefore operates on 8:1 fewer cells than previously.

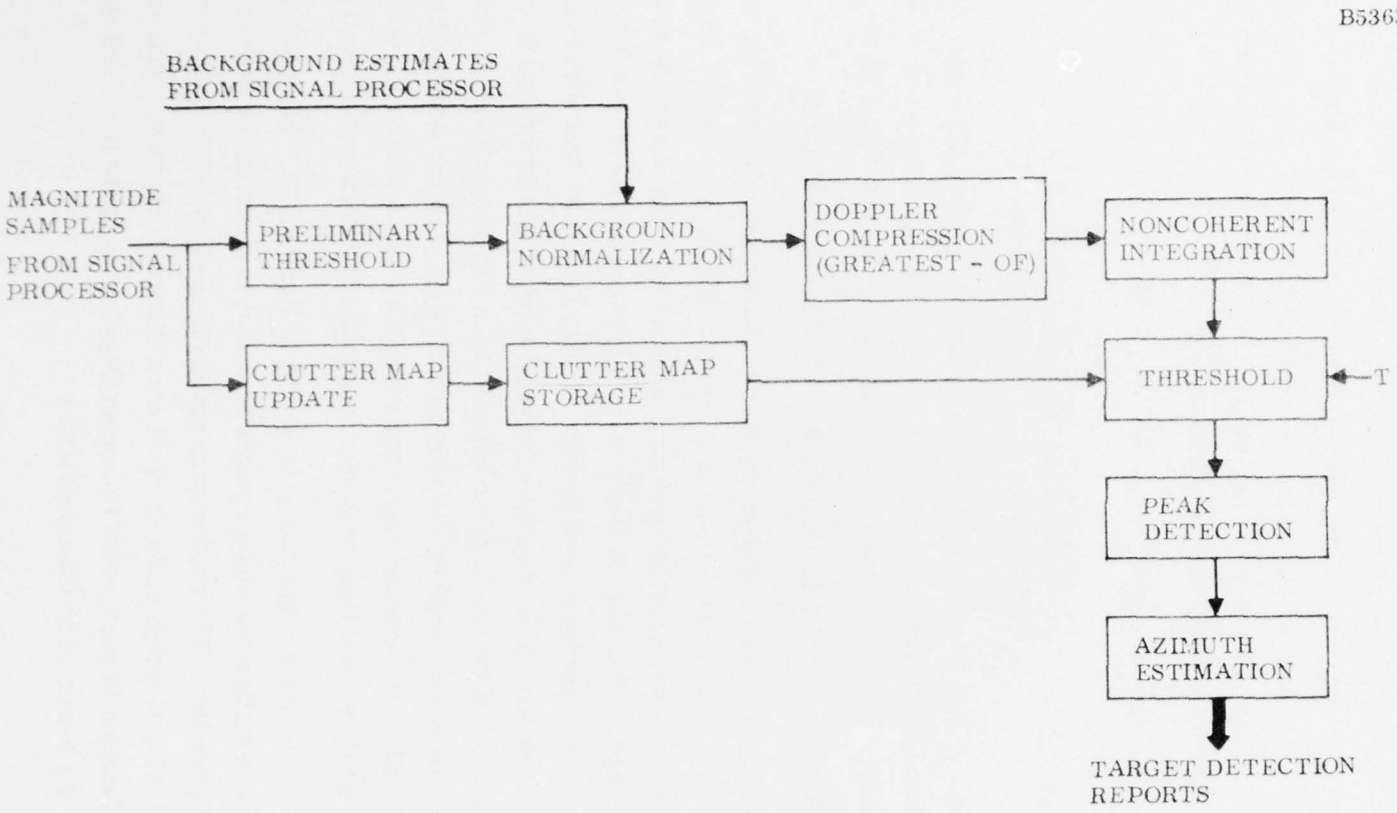


Figure 5-6. Radar Data Input Processor Unaligned System

The revised processing load and storage requirements are shown in Table 5-2. Processing required to perform the Doppler compression, noncoherent integration and clutter map update are grouped together for efficiency in performing the processing. Two loading estimates are given, which are dependent on the degree of preliminary thresholding performed on the incoming magnitude samples to reduce the number of points which must be normalized (via division) by the background estimates from the moving range-window normalizer. The buffer allocation and management required to support the defined processing is shown in Figure 5-7. The storage requirements are considerably reduced as a result of the Doppler compression which produces a single output for each range bin from the eight Doppler filter outputs.

An estimate of the total number of instructions per dwell which must be processed for the unaligned system may be obtained as:

$$\text{Instructions/Dwell} = 4(55,965) + 1833 + 1965 = 2.28\ (10^5) \qquad (5\text{-}5)$$

or

$$\text{Process Rate} = \frac{27.28(10^{-3})}{2.28(10)^5} = 0.119\ \mu\text{s/instruction} \qquad (5\text{-}6)$$

Note that the unaligned system requires 66% more instructions per dwell than the aligned system.

3. RADAR TARGET PROCESSOR

The Radar Target Processor accepts the detection reports output by the radar data input processor, and utilizes the reports to perform track initiation and maintenance. The functional flow of the Radar Target Processor is summarized in Figure 5-8.

Detection reports received at the input to the Radar Target Processor are first tested for association with existing tracks in the track table. Data association with existing tracks is performed by first selecting candidate tracks which are within ±20 beamwidths of the beam position corresponding to the detection report. This presort operation allows for selection of tracks which are flying a path tangential to the radar at the maximum speed (i.e., Mach 4), and which have not associated with a detection report for an elapsed time interval of 3 radar scans. This coarse azimuth gate size is consistent with a one-out-of-three track maintenance criteria, in which tracks are maintained in the track table if data association is achieved at least once every three radar scans.

TABLE 5-2. RADAR DATA INPUT PROCESSOR LOADING UNALIGNED SYSTEM

CPU LOAD

	Instructions	Processing Cycles	Time (ms)	Required Cycle Time (μs)
Doppler Compression Noncoherent Integration Clutter Map Update	38	55,965	6.82	0.122 (20% Threshold)
		36,707	6.82	0.186 (1% Threshold)
Threshold	18	1,833	13.64	7.44
Peak Detection and Azimuth Estimation	39	1,965	27.28	1.86

STORAGE

	16 Bit Words
Magnitude Samples	2,896
Background Estimate	2,896
Noncoherent Summation	362
Three-Beam Detected Noncoherent Sums	1,086
Clutter Map	52,852

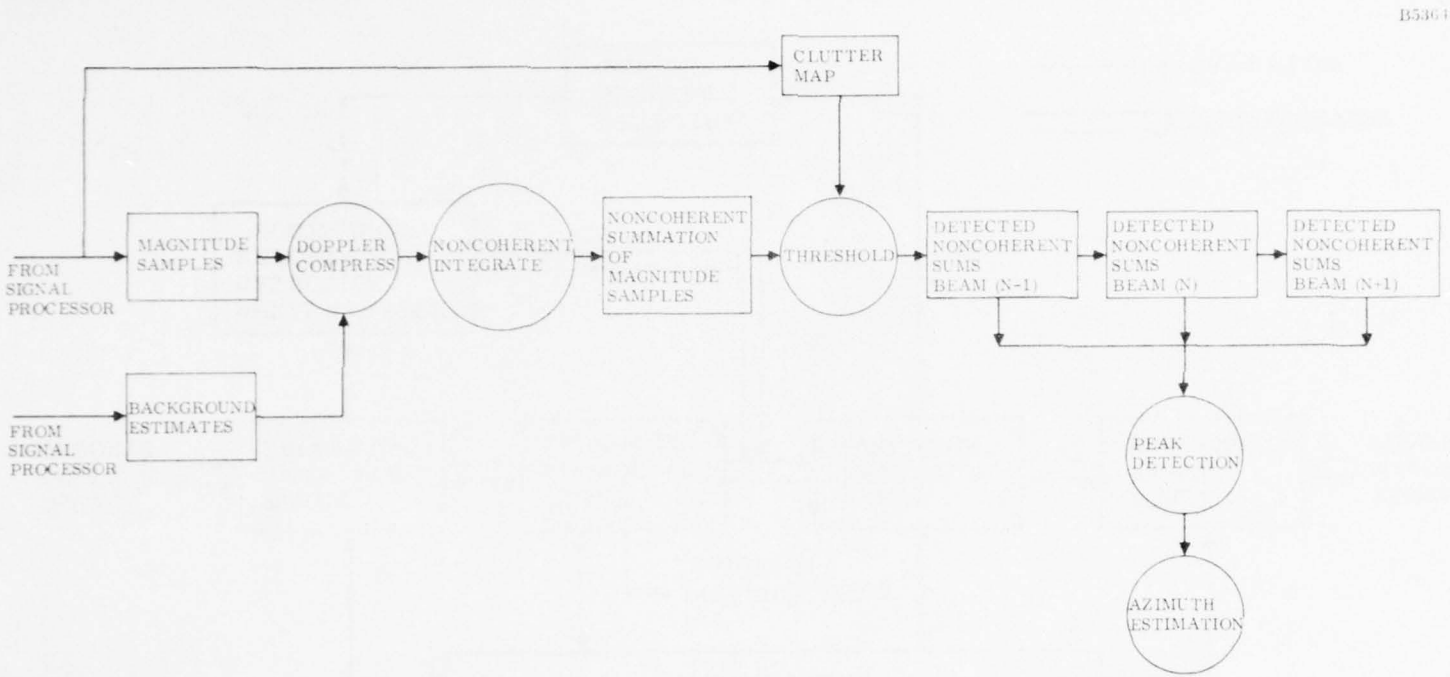


Figure 5-7. Radar Data Input Processor Buffer Management

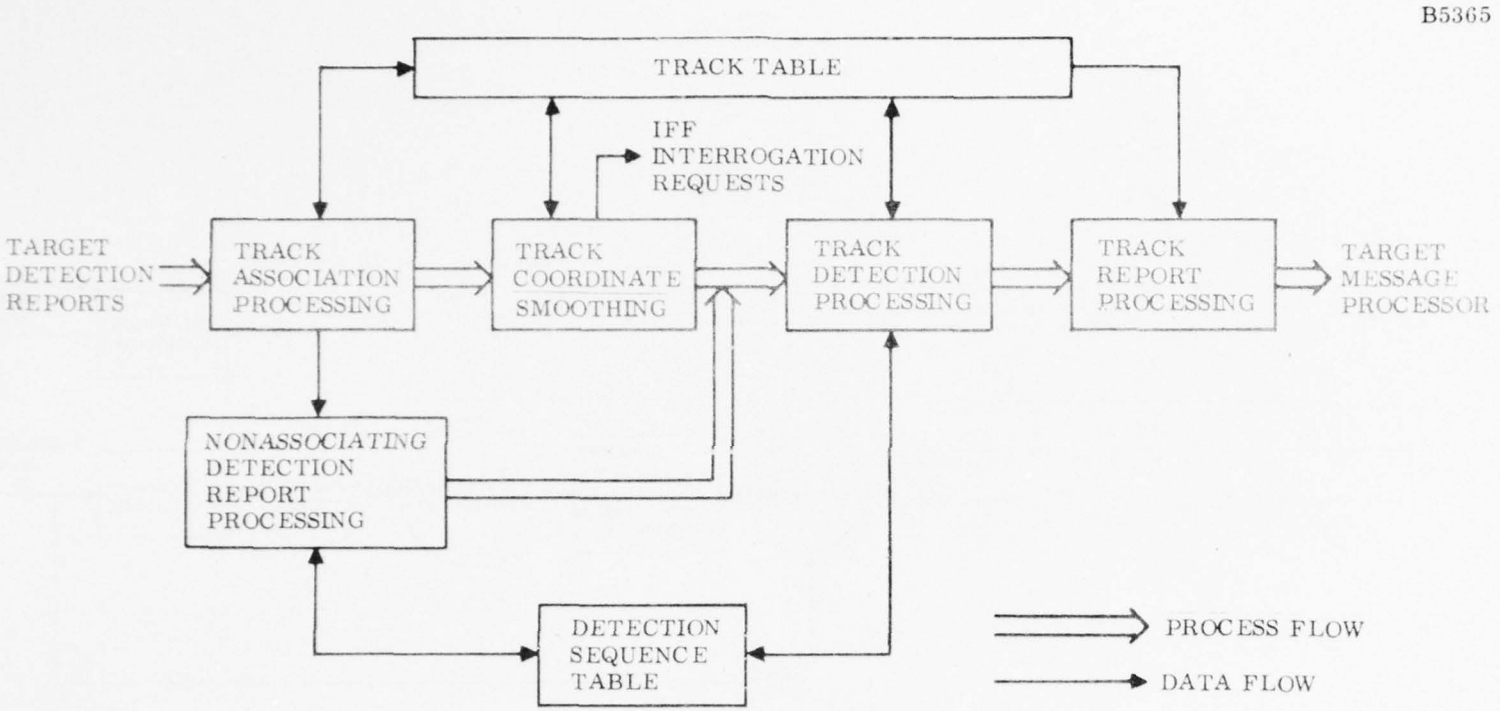


Figure 5-8. Radar Target Processor

Those tracks which successfully pass the coarse azimuth gate then have their coordinates (radar slant range and azimuth) predicted to the current time position. Track range is then tested against the range of the detection report utilizing a fine range gate consistent with track accuracy. One of three range gates is selected based on the number of successive association misses that have been experienced by the track. For a track which successfully associates in range, a fine azimuth association is next performed. The azimuth, predicted to the time position of the detection report, is compared to the azimuth position of the detection report utilizing one of three azimuth gates, selected based on the number of successive missed associations, and scaled by the target range. A track which successfully associates with a detection report has its coordinates smoothed with the coordinates of the detection report, and the track status (i.e., hit count) is updated to reflect a successful association (hit count = 3).

Track coordinate smoothing is performed utilizing a digital recursive weighted least-squares filter based on the Kalman filter. Range and azimuth are independently smoothed. The prediction and smoothing equations for the range coordinate are summarized in Table 5-3. An adaptive term is applied to update the range-rate variance based on the weighted range error residual to improve filter responsiveness to target maneuvers. The azimuth prediction and smoothing equations are identical in form.

Following the track association and smoothing process, those detection reports which do not successfully associate with a track are utilized to update detection sequences which have not qualified as tracks, or used to initiate a new detection sequence.

A one-out-of-four criteria (three-out-of-four was also considered) is employed to qualify a detection sequence as a track. For the three-out-of-four process, a detection sequence is dropped from the detection sequence table if two successive missed associations occur after initial detection. Detection reports which do not associate with tracks are next tested for association against report sequences in the detection sequence table. Prediction is not performed for the detection sequences, so that one of two range association gates is first selected, based on the number of missed associations for the detection sequence. For a detection report-detection sequence which associate in range, one of two azimuth gates is selected and scaled by the range of the detection report to enable azimuth association to be performed.

TABLE 5-3. TRACK PREDICTION AND SMOOTHING ALGORITHM

Prediction and Range Smoothing

$$TLD = TNOW - TLUD \qquad \text{Time Update}$$

$$TLS = TNOW - TLST$$

$$TLUD = TNOW$$

$$R_p = R_p + \dot{R}_s \cdot TLD \qquad \text{Range Prediction}$$

Covariance Update (Upon Association with Data Point)

$$b_{11} = b_{11} + 2\,b_{12}\ TLS + b_{22}\ TLS^2 \qquad \text{Range Variance}$$

$$b_{12} = b_{12} + b_{22} \cdot TLS \qquad \text{Range - Range Rate Covariance}$$

$$b_{22} = b_{22} + \frac{W_R}{TLS^2}\left(R_m - R_p\right)^2 \qquad \text{Range Rate Variance}$$

Compute Gains

$$K_{11} = \frac{b_{11}}{b_{11} + \sigma^2_{R_m}} \qquad \text{Filter Gains}$$

$$K_{21} = \frac{b_{12}}{b_{11} + \sigma^2_{R_m}}$$

Smooth Coordinates

$$R_p = R_p + K_{11}\left(R_m - R_p\right) \qquad \text{Range Smoothing}$$

$$\dot{R}_s = \dot{R}_s + K_{21}\left(R_m - R_p\right) \qquad \text{Range Rate Smoothing}$$

Update Covariances

$$b_{11} = (1 - K_{11})\,b_{11}$$

$$TEMP = b_{12}$$

$$b_{12} = b_{12}\ (1 - K_{11})$$

$$b_{22} = b_{22} - K_{21} \cdot TEMP$$

Those detection sequences which achieve one hit within four scans are declared to be a target track. The available hits and subsequent data are utilized to derive an estimate of track range rate and initialize the variances of the Kalman filter, as summarized in Table 5-4 for the range coordinates, with a corresponding procedure in azimuth.

Those detection reports which do not associate with either a track or a detection sequence are entered in the detection sequence table to enable subsequent association with detection reports on following scans.

Following association processing and coordinate smoothing, the status of all tracks and detection sequences is updated and tested. Track detection processing is performed once for each complete radar scan. The hit count of all tracks is decremented by one, such that all tracks which have not associated with a detection report in three scans achieve a hit count of zero and are dropped from the process. Tracks which are dropped are identified to the track report processor for output to the remote control site.

All detection sequences are also tested such that all sequences with an age of 4 scans, or a miss count (computed as the difference between the age and hit count) of 2 (for 3 out of 4 criterion) are dropped from the detection sequence table.

Finally, the target report processor is activated to periodically (nominally every three scans) output all track in the track table.

One final function performed by the Radar Target Processor is to output requests to the radar schedule to generate IFF interrogation requests. All new tracks are interrogated upon becoming an established track consistent with the responsive IFF mode of operation. Subsequently, if the initial interrogation is unsuccessful, an additional interrogation request is scheduled following the next successful association of the track with a detection report. If neither of the two interrogations is successful, the track is output as an unknown, via the target report processor, to alert the remote site control operator(s) to the inability to successfully identify the track. The IFF approach is further discussed in the following section.

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UNATTENDED/MINIMALLY ATTENDED RADAR STUDY. VOLUME II. 2-D (UNAT--ETC(U)
AUG 77 T B SHIELDS, S E BELL, M I FOX F30602-76-C-0380
UNCLASSIFIED RADC-TR-77-263-VOL-2 NL

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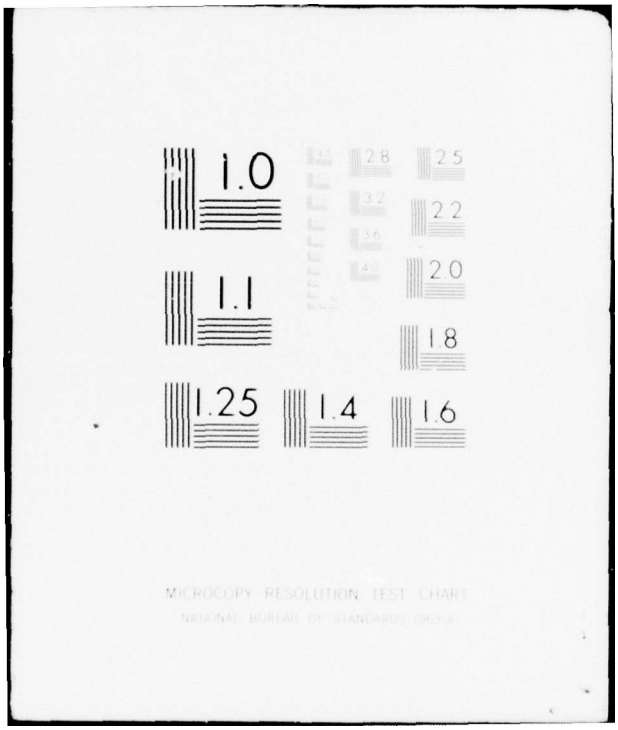

1.0
1.1
1.25
1.4
1.6
2.8
2.5
3.2
2.2
3.6
2.0
4.0
1.8
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

TABLE 5-4. TRACK FILTER INITIALIZATION

$$R_s = R_3$$

$$\dot{R}_s = \frac{R_3 - R_1}{t_3 - t_1} \qquad \text{Track Range Rate}$$

$$b_{11} = \sigma^2_{R_m} \qquad \text{Range Variance}$$

$$b_{12} = \sigma^2_{R_m} / (t_3 - t_1) \qquad \text{Range - Range Rate Convariance}$$

$$b_{22} = 2\,\sigma^2_{R_m} / (t_3 - t_1)^2 \qquad \text{Range Rate Variance}$$

where

$\sigma^2_{R_m}$ = Range Measurement Accuracy

t_3, t_1 = Last, First Time Position of Detection Reports

The data tables required to support the tracking process are shown in Tab
The sizing requirements are based on an assumption of a maximum of five dete
reports per beam. The track table provides for a maximum of 10-noise tracks
20-valid targets, with the detection sequence table allotted space for 16 sequen
These allocations are conservative in light of the false alarm probabilities (i.e
10^{-4} to 10^{-6} per resolution cell) and track load requirement (i.e., 20 tracks in
coverage at any one time).

The total processing load and storage requirements for the Radar Target
cessor is summarized in Table 5-6. The processing load is expressed in term
the total number of instruction cycles for a 4-s scan, assuming 20 targets trac
detections along with 5-noise detections over the 4-s scan. It is also expresse
the number of instruction cycles which must be executed to process a single de
report in a beam assuming a total of 20 tracks in the coverage. Assuming a cy
time of 0.5 μs for the processor, the track processing would require only 0.79
out of the 27.28 ms/dwell.

TABLE 5-5. TRACK DATA BASE

Track Table

	Word Size (Bits)
• Radar Coordinates	
Smoothed Slant Range	16
Smoothed Range Rate	16
Time of Last Smoothing	16
Smoothed Azimuth	16
Smoothed Azimuth Rate	16
• Track Status	
Hit Count	2
IFF Verification Status	3
IFF Verification Time	16
FAA Identification	12
Target Elevation	12
Verification Range	16
Verification Azimuth	16
• Smoothing Filter Coefficients	
Variance of Azimuth	16
Variance of Azimuth Rate	16
Variance of Range	16
Variance of Range Rate	16
Convariance of Range - Range Rate	16
Covariance of Azimuth - Azimuth Rate	16

• Storage Required - 30 Tracks
16 Words/Track
480 Words

Detection Reports

Measured Range	16
Measured Azimuth	16
Detection Report Time	16

Storage Required - 5 Detection Reports/Beam
3 Words/Hit
15 Words

TABLE 5-5. TRACK DATA BASE (Cont)

Detection Sequence Table

	Word Size
Detection Hit Count	2
Detection Sequence Age	2
Initial Detection Range	10
Initial Detection Azimuth	12
Initial Detection Time	16
Last Measured Range	10
Last Measured Azimuth	12
Last Detection Time	16

Storage Required - 16 Detection Sequences
6 Words/Detection Sequence
96 Words

TABLE 5-6. PROCESS LOAD AND STORAGE REQUIREMENTS FOR RADAR TARGET PROCESSOR

Instruction Storage	16 Bit Words
Data Association	66
Smoothing/Prediction	212
Detection Sequence Processing	150
Detection Processing/Reporting	53
Total Instructions	481

Data Storage	16 Bit Words
Track Table	480
Detection Reports	15
Detection Sequence Table	96
Total Data Storage	591

Processing Load	
Instructions/Scan (20 Tracks and 5 Noise Detections over 4-s scan)	28,240
Instructions/Dwell (20 Tracks with 1 Detection Report in 27.28-ms dwell)	1,596

4. IFF DATA CONTROLLER AND DATA PROCESSOR

The IFF subsystem for the Unattended Radar is utilized to identify friendly targets via transponder interrogation to obtain Federal Aviation Administration (FAA) assigned identification numbers and/or aircraft height information. A summary of the IFF requirements is shown in Table 5-7. Interrogation (i.e., initiation of a transponder return) of an aircraft consists of transmitting two interrogation pulses. The time relationship between leading edges of the interrogator pulses determines the mode in which the aircarft will reply.

The FAA has rigidly defined modes 1, 2, 3/A, B, C, D and 4 with respect to the interrogator pulse width, interrogator pulse spacing, and the type of data in the aircraft reply. Every interrogation, with the exception of Mode 4, produces the general transponder reply code format shown in Figure 5-9 regardless of interrogation mode. However, depending on the interrogation mode and response, not all bit positions are filled. Mode 4 is a classified transmission and reply which requires transmission and reception of an encrypted modulation. Sampling of the bit positions between the framing pulses, F_1 and F_2, permits extraction of certain information, such as target elevation and FAA identification number. Range information is derived by a timing measurement of the F_2 pulse with respect to the interrogation pulse transmission plus a built-in transponder delay.

Development of the IFF approach has been supported by General Electric's internal development efforts on the GE 592 Air Defense Radar System program, which addressed the desire to reduce cost and power consumption ($\approx$ 200 W) associated with OV "hang-on" equipment.

The total IFF process is functionally represented in Figure 5-10. A programmed interrogation sequence of four interrogations will be initiated by the radar track processor upon initiating a new radar track. If the initial interrogation sequence is unsuccessful, one additional attempt to automatically interrogate the target will be performed upon sensing a subsequent detection report association with the target track in the radar track processor. If neither attempt is successful, the target will be reported to the remote control site as an unknown requiring operator attention.

TABLE 5-7. INTEGRATED IFF MARK X SYSTEM PERFORMANCE

• **Interrogation Capability**	
Frequency	1030 ± 0.2 MHz
Polarization	Vertical
Modes Designation	Modes 1, 2, 3/A, C
Expansion Capability	Mode 4
Interrogation Modes	
Pulse-pair (P_1, P_3) spacing	
Mode 1 (Military)	3 ± 0.1 μs
Mode 2 (Military)	5 ± 0.2 μs
Mode 3/A (Common identify)	8 ± 0.2 μs
Mode B (Civil)	17 ± 0.2 μs
Mode C (Common altitude)	21 ± 0.2 μs
Mode D (Civil) spare mode	25 ± 0.2 μs
Pulse width	0.8 ± 0.1 μs
ISLS pulse (P_2)	2 ± 0.15 μs following P1 on each mode
Typical PRF	300-400
Target Interrogations Per Beam Position	4
Principle Interrogation Mode/Duty Factor	3/A, C-2:2
• Military Mode 1 Interrogation	3/A, 1-2:2
• Military Mode 2 Interrogation	3/A, 2-2:2
• **Response Capability**	
Frequency	1090 ± 0.2 MHz
Emergency Response	Mode 1, 2, 3/A
• Military Emergency	Mode 1, 2, 3/A
• Civil Emergency Code 7700 and Radio Failure Code 7600	Mode 3/A
• Expected 4 in a row Emergencies/ Interrogation	≤ 1
Target Density Per Beam (max.)	8
Target Density Per Sweep	20
Target Max. Range	60 nmi

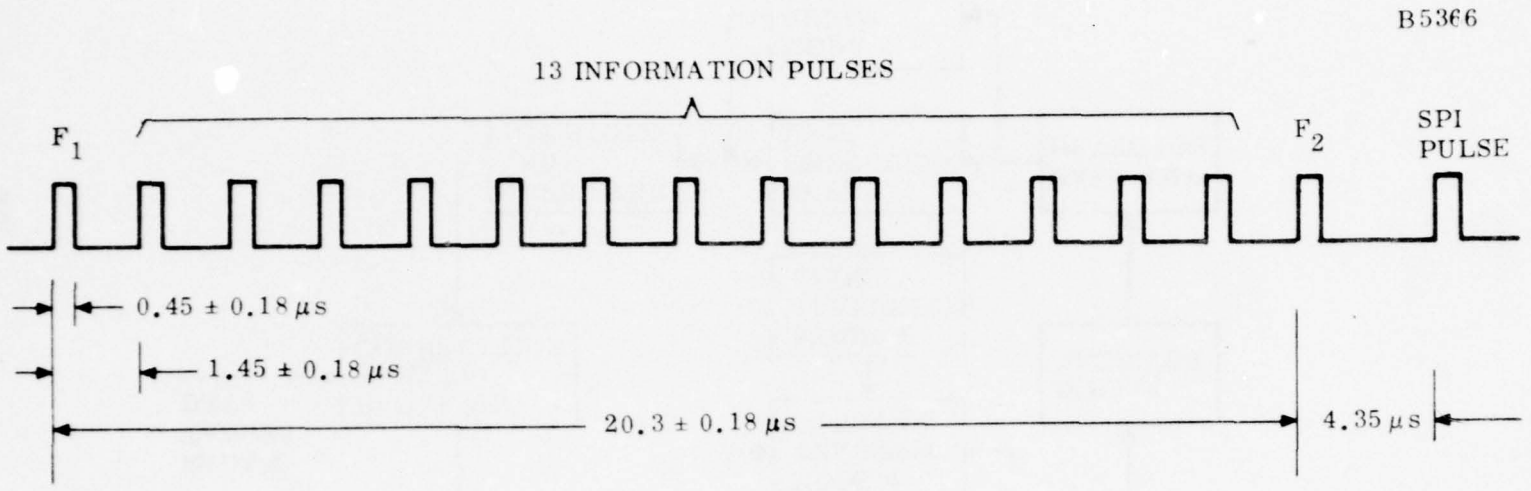


Figure 5-9. IFF Transponder Return

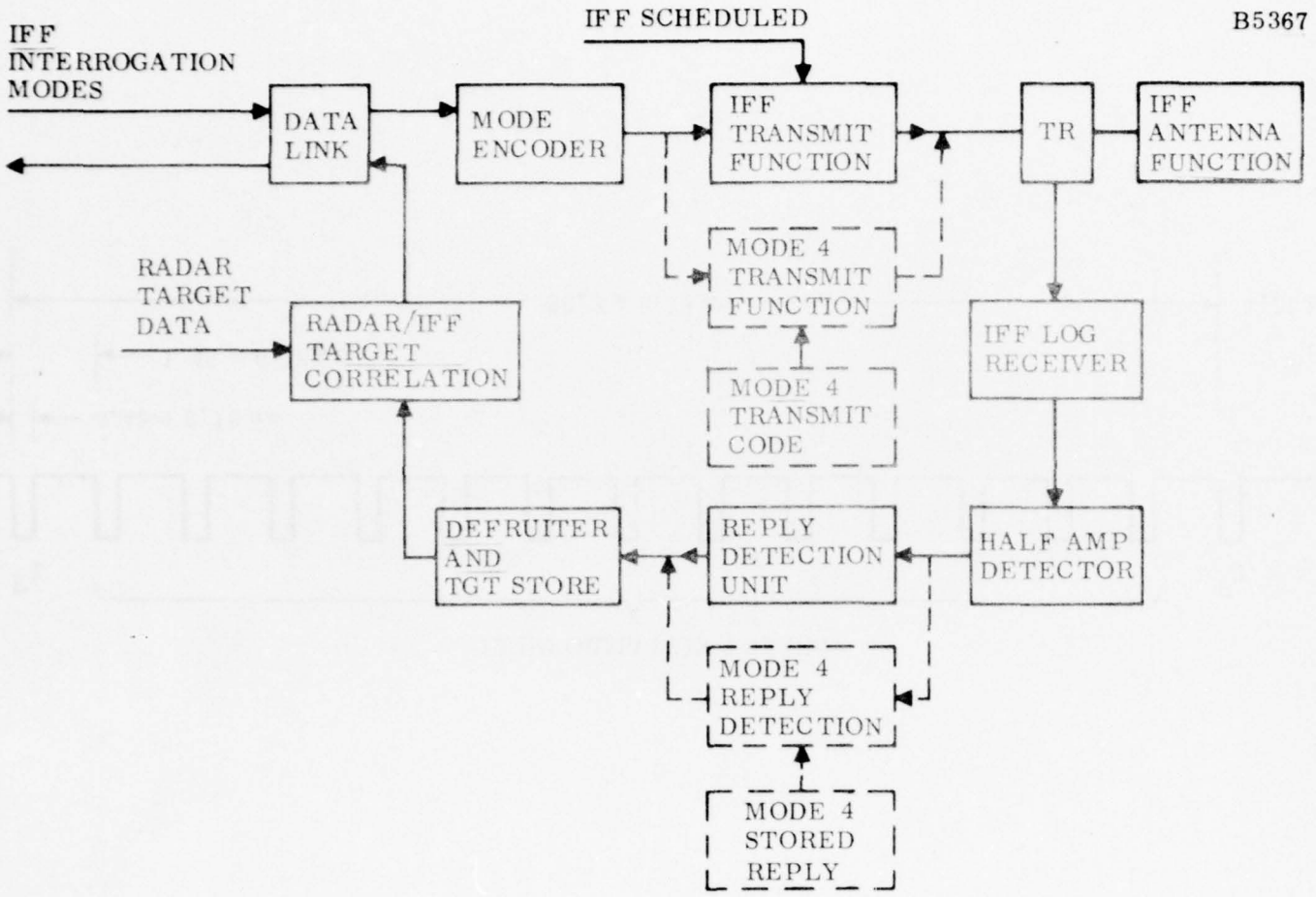


Figure 5-10. IFF Functional Block Diagram of IFF Processing

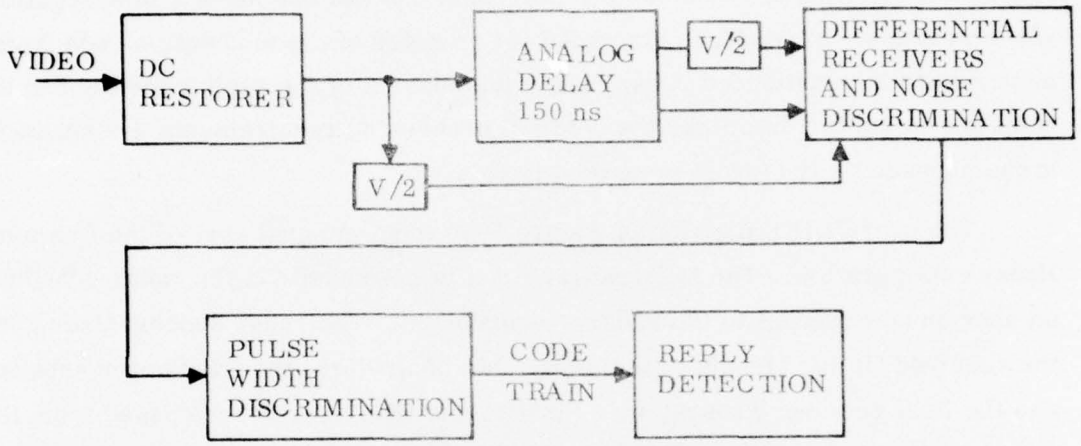
The programmed interrogation sequence consists of two interrogations in Mode 3A (FAA identification) and two interrogations in Mode 3C (elevation request) with the returns from each mode compared to confirm response validity. The remote site operator may alternately request a Military Mode 1 interrogation, consisting of two Mode 3A interrogations and two Mode 1 interrogations or a Military Mode 2 sequence consisting of two Mode 3A interrogations and two Mode 2 interrogations. While provision for Mode 4 is included via transfer of the modulation code from the remote site to the unattended radar, and transmission of the reply code back to the remote site via the data link, the detailed processing requirements are not included in the subsequent IFF processing description.

The overall IFF function of Figure 5-10 is an integral part of the Unattended Radar configuration. The IFF transmission is scheduled via the radar schedular with an appropriate request to the radar synchronizer. The radar synchronizer generates the required timing signals to the array data controller, the RF exciter subsystem and the final receiver subsystem. Finally, the IFF returns are passed from the final receiver subsystem to the IFF data controller and IFF data processor.

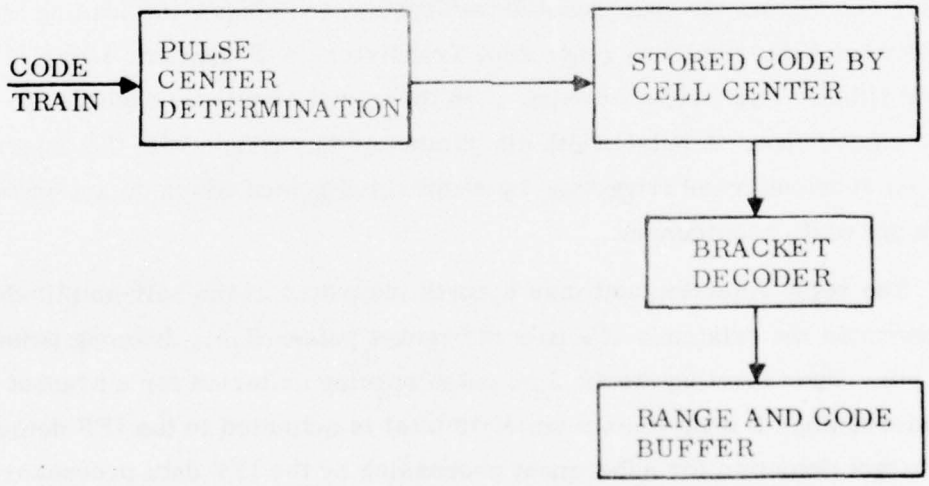
The IFF data controller consists of a half-amplitude detector and the reply detection unit as shown in Figure 5-11. The Half-Amplitude Detector accepts the IFF log video from the final receiver subsystem and shapes the leading and trailing edges of the video signal to generate a Transistor-to-Transistor Logic (T^2L) compatible pulse. This output appears when the signal amplitude exceeds the 50% points of the video pulse. A pulse width discriminator in cascade with the detector further reduces spurious noise triggering by eliminating pulses which do not exceed the minimum width requirement.

The reply detection unit then accepts the output of the half-amplitude detector to determine the existence of a pair of bracket pulses (i.e., framing pulses spaced 20.3 μs). Upon meeting the 20.3 μs pulse spacing criterion for a bracket decode, the intervening bit code (maximum of 13 bits) is outputted to the IFF detection buffer as a target detection for subsequent processing by the IFF data processor. Range is determined from a range counter at the time of the bracket decode. All bracket decodes, including phantom (ambiguous)brackets created due to closely spaced targets (less than 5 nmi), are output to the IFF detection buffer. The IFF data controller function is implemented in special-purpose digital hardware, as described in a subsequent paragraph.

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a. 1/2 AMPLITUDE DETECTOR



b. REPLY DETECTION UNIT

Figure 5-11. IFF Data Controller

For the assumed target density (i.e., maximum of 8 targets which reply to an interrogation), an IFF Detection Buffer of 32 words by 16 bits is allocated. Note that two-closely spaced targets (i.e., less than 5-nmi spacing) can generate in excess if 24-false bracket decodes as the framing pulses are indistinguishable from the information bits.

The remaining IFF processing is performed in the IFF data processor as part of the data processor and control subsystem, and time-shares the basic processor elements normally employed in processing radar skin returns and target detections. Note, however, that while the IFF data processor creates program storage requirements for the data processor design, no computational burden is imposed by the IFF data processor as the normal radar scan mode is interrupted during IFF interrogation, such that processing of radar skin returns is not simultaneously required.

The IFF Data Processor is shown in Figure 5-12. The IFF data processor performs the functions identified as defruiting and radar/IF target correlation as shown in the functional block diagram of Figure 5-10. The IFF data processor first performs bracket decode validation by ensuring that successive bracket decodes do not overlap in time (i.e., the range of successive bracket decodes is greater than 20.3 μs). Before passing nonoverlapping bracket decodes as a valid IFF detection a test must be performed for a four-in-a-row emergency return. A four-in-a-row emergency is declared when a target existing at a range R generates repetitive transponder outputs which produce bracket decodes at R, $R + R_1$, $R + 2R_1$ and $R + R_2$, where R_1 and R_2 are fixed time delays or radar ranges. Thus, whenever a bracket decode exists at a given range and three fixed subsequent ranges, a four-in-a-row emergency flag is set in the IFF Detection Buffer for the IFF detection at range R. The emergency bit is subsequently reported via the data link to the remote control site along with the target data.

In addition to the four-in-a-row emergency, an emergency can also be reported via the normal IFF information code returns for any interrogation mode as well. In this case, the emergency codes (i.e., 7600 or 7700 in the information bits) within the brackets do not set the emergency flag, but are reported as valid response codes in place of the normal elevation or FAA idenfication.

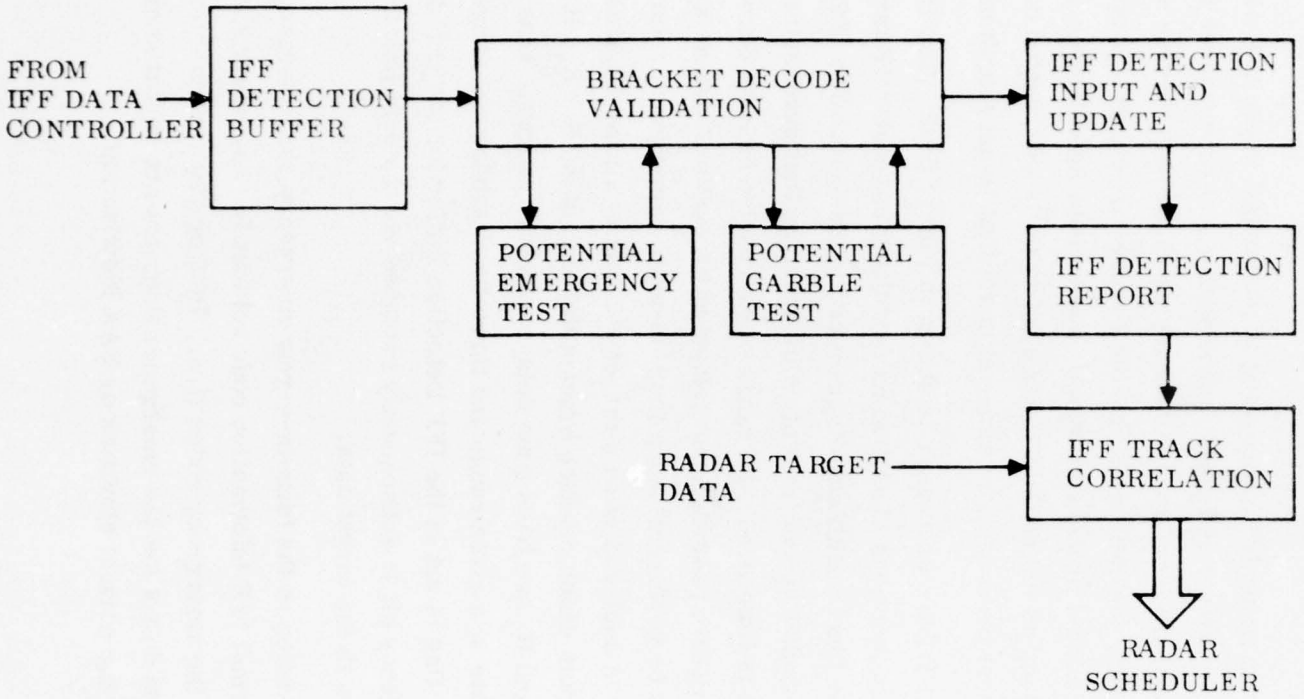


Figure 5-12. IFF Data Processor

The IFF Data Processor next determines if a garbled signal condition exists. If two bracket decodes occur within a 20.3 μs period, garble is suspected. To resolve a probable garble condition, the IFF Data Processor determine if:

- The brackets occur on the same pulse centers
- The second bracket decode is part of a closely spaced target
- The bracket decode is part of an overlapping target, or
- The bracket decode is part of three overlapping targets.

Garbled targets are flagged to inhibit subsequent track data association with the garbled returns.

Finally, those bracket decodes which are validated are output as IFF detection reports. Data association of the coordinates of the target(s) interrogated for the current IFF request is then performed by testing the range of the IFF detection reports against the range of the interrogated targets.

The process load and storage requirements for the IFF data processor function is summarized in Table 5-8. Since the maximum interrogation rate is 400 pulses/s, for the programmed sequence of four interrogations approximately 10-12 ms of radar scan time would be required to perform the IFF interrogation function for each target, as compared to the nominal radar dwell time of 27.28 ms. Since the total instructions which must be executed over the 10 ms (i.e., 4595 instructions per programmed IFF request sequence) exclusive of the synchronizer, represent only 2.3 ms of processor time for a 0.5 μs processor cycle time, PM/FL functions could be overlapped with the IFF processing function.

5. RADAR CONTROL PROCESSOR/SYNCHRONIZER

The Radar Control Processor accepts requests from the radar scheduler to generate the control data and timing signals for operation of the radar. The Radar Control Processor generates the beam steering and transmit module amplitude control commands for the array control subsystem. Control signals are generated for the RF exciter subsystem to define the transmit frequency for each transmission and the pulse repetition schedule and range gate control for both the normal radar scan mode and the IFF interrogation mode. The Radar Control Processor also generates the range start and range end controls to the signal processor subsystem together with the detection threshold constant. Finally, test mode control signals are output to the rf exciter to enable injection of test signals to the final receiver in support of PM/FL functions.

TABLE 5-8. PROCESS LOAD AND STORAGE REQUIREMENTS FOR IFF DATA PROCESSOR

Instruction Storage	16 Bit Words
Bracket Decode Determination	28
Potential Emergency Test	46
Potential Garble Test	28
IFF Detection Input and Update	38
IFF Detection Output and Correlation	49
Total Instructions	189 Instructions

Data Storage	16 Bit Words
IFF Reply Store	32
IFF Detection Store	32
Total Storage	64 Words

Processing Load	Instruction Cycles/ IFF Request
Bracket Decode Determination	480
Potential Emergency Test	185
Potential Garble Test	2400
IFF Detection Input and Update	640
IFF Detection Output and Correlation	890
Total Instruction Cycles/Request	4595

Actual transmission of the real-time radar control and timing signals is decoupled from the Data Processing Subsystem via the radar synchronizer. The Radar Control Processor generates the control instructions by accessing preprogrammed instruction templates for computation of element steering commands based on beam position. Subfields of the instructions define the key events which must take place on the parameter values to be utilized for each PRP. The times at which these instructions are to be executed are controlled by a time tag subfield. Following generation of the appropriate control template by the Radar Control Processor in response to the radar schedular request, the control instruction blocks are placed in an output queue for processing by the synchronizer, where they are accessed in a First-In-First-Out (FIFO) manner. The radar synchronizer compares the time tag to the radar time count. On compare, the timing strobes required to transfer the control data to the designated subsystem controllers are generated. The execution of PRP type instructions resets the radar time count, thus referencing all modifying and supplemental instructions to the beginning of the PRP in which they occur.

The above concept of operation is important because it enables a programmable radar system operation. Any realizable set of operations can be created within a waveform period and any mixture of periods can be scheduled. The data processing subsystem is effectively divorced from high-speed, real-time operational constraints, and the intricacy of radar timing and control is removed as an influence on software development and maintenance.

The primary Radar Control Processor/Synchronizer requirements are summarized in Table 5-9. The primary processing load on the Radar Control Processor is the computation and output of the array steering and phase/amplitude controls. Two forms of array control were considered in order to estimate the processing load associated with the Radar Control Processor. These alternate approaches are considered in the next two sections. The following discussion is developed in the context of a 1.5° azimuth beamwidth system. For the 3° design, the array size is halved and array-related components reduced correspondingly (e.g., 128 columns rather than 256).

a. MATRIX SWITCHED CYLINDRICAL ARRAY

The Matrix Switched Cylindrical Array considered consists of 256 columns, of which 64 are active for each radar dwell. Sector select switches (64 switches) connected to 4-columns each, select 1-of-the-4 columns corresponding to the illuminated beam position. The appropriate time delays for each of the 64 columns are selected via a 64-way matrix switch. The functional blocks are summarized in Figure 5-13.

For the matrix switch array, the phasing of the elements is accomplished by selection of 64 delay lines by the matrix switch, so that the matrix switch commands are independent of frequency. The matrix switch consists of 6 levels of switching with 32 diode switches at each level. Due to symmetry and switching characteristics, 64 bits are required to define the switch settings. The Radar Control Processor must compute the matrix switch commands only once for each radar dwell (28.27 ms), due to the frequency independence of the switch settings and then has a complete radar dwell time in which to compute the switch settings for the next dwell. The matrix switch settings, as well as the sector select switch commands, are computed based on beam number to allow for arbitrary positioning of the beam in support of an IFF interrogation request followed by a subsequent re-positioning of the beam to continue the normal radar scan. Note that provision for a separate omni-directional transmission is included to enable transmission of the Sidelobe Suppression (SLS) pulse for the IFF mode.

TABLE 5-9. RADAR CONTROL PROCESSOR/SYNCHRONIZER FUNCTIONS NORMAL RADAR SCAN

Timing	Control Command	Destination
Each PRP (0.852 ms to 0.916 ms)	Main Bang/Transmit Pulse	Exciter/Waveform Gen Array T/R Module
	Range Counter Start, End, PRP	Signal Processor
Every 8 PRP's (6.816 ms to 7.328 ms)	Frequency Select (Diversity Step)	Exciter/Waveform Gen
	Array Phase Control (Array - Bit Steered)	Array T/R Module Array Sector Select
Every 32 PRP's (28.27 ms)	Array Steering Command (Matrix Steered)	Array Switch Matrix Array Sector Select
	Array Amplitude Control (Transmit/Receive)	Array T/R Modules
	Detection Threshold	Signal Processor
	Radar/IFF Mode Control	Exciter/Waveform Gen Receiver

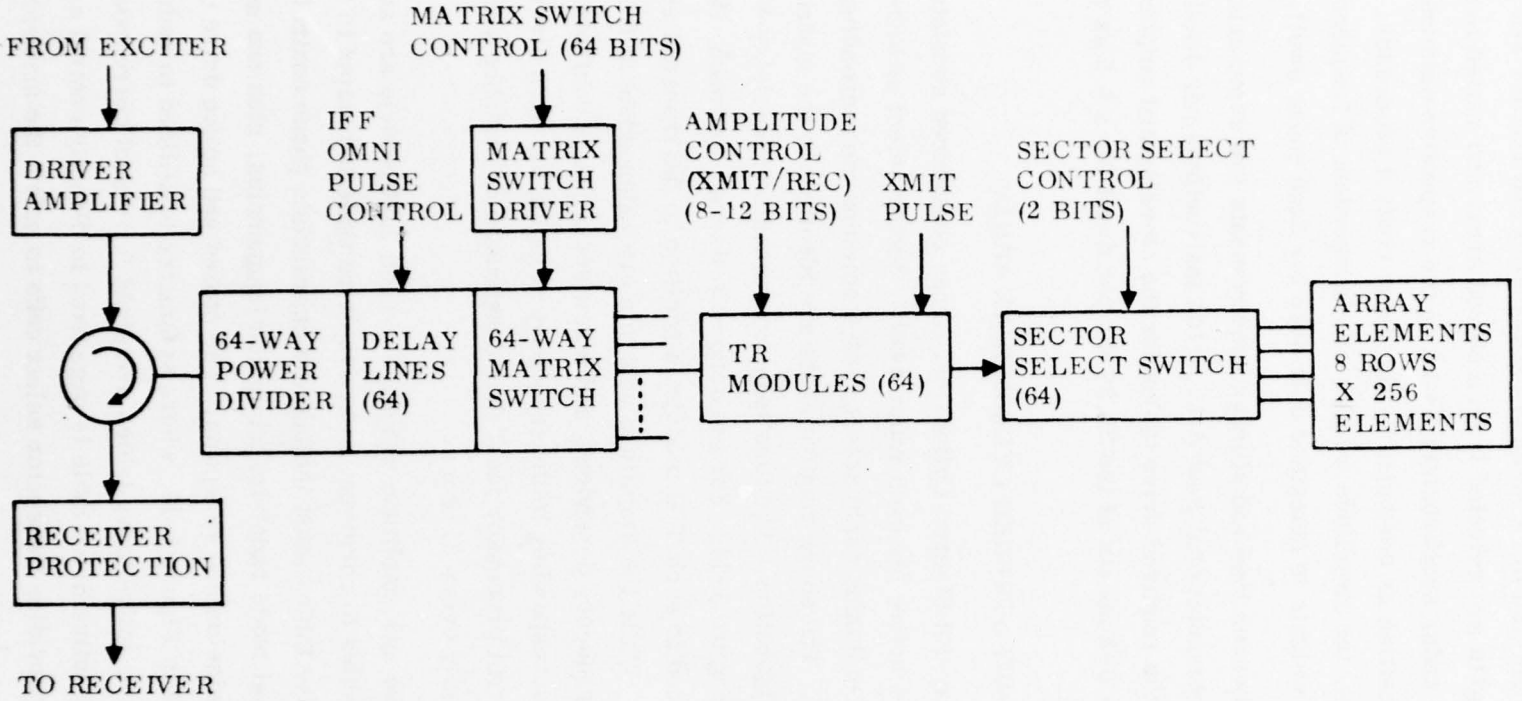


Figure 5-13. Matrix-Switched Cylindrical Array

Independent amplitude weights for transmit and receive are also assumed. The amplitude weights are selected from a stored array and routed to the appropriate T/R module by the radar synchronizer based on the respective element position relative to the beam position as computed by the radar control processor. As with the matrix switch settings, the amplitude weights are independent of frequency such that the routing of the weights is computed only once for each radar dwell.

The processor load and storage requirements are summarized in Table 5-10. Note that the computational load (i.e., 1164 instructions per dwell) associated with generation of the required drive tables for the steering and amplitude weights would require only 0.582 ms out of the 28.27 ms per dwell for a 0.5 μs processor cycle time.

b. DELAY-BIT STEERED CYLINDRICAL ARRAY

The Delay-Bit Steered Cylindrical Array considered consists of 256 columns, of which 64 are active for each radar dwell. Sector select switches (64 switches connected to 4-columns each) select 1-of-4 columns corresponding to the illuminated beam position. The above requirements are identical to the matrix-steered cylindrical array configuration. The functional components of the delay-bit steered approach are shown in Figure 5-14. For the delay-bit steered approach, the phase control must be provided to each T/R module in addition to the transmit and receive amplitude controls. While the amplitude controls are independent of frequency, the phase controls are frequency dependent, and a new set of phase controls is required every eight PRP's corresponding to the frequency stepping for each diversity transmission. The radar control processor must thus construct a drive table with a new set of phase weights nominally every 6.82 ms.

The phase and amplitude weights for each T/R module are accessed from stored drive tables to construct an active drive table for output to the synchronizer. The stored drive tables must include the appropriate phase controls for up to eight different normal mode radar transmission frequencies, plus one additional set for the IFF transmission and reception. The stored and active drive table organization is summarized in Figure 5-15, where symmetry is utilized to reduce the stored drive tables, while the active drive tables are sized for direct correspondence to the T/R modules. The active drive table is organized to directly control each of 64 elements, together with providing the sector select code to select the appropriate element for the active quadrant.

TABLE 5-10. PROCESS LOAD AND STORAGE REQUIREMENT FOR MATRIX STEERED CYLINDRICAL ARRAY

Instruction Storage	16-Bit Words
Steering Matrix Switch Setting	110
Amplitude Weight Access	10
Element Sector Select	16
Total Instructions	136

Data Storage	
Stored Amplitude Weights	32
Active Drive Tables (and Weights)	64
Steering Matrix Drive Table	4
Total Data Storage	100

Processing Load	Instruction/Dwell
Steering Matrix Switch Settings	80
Element Sector Select	700
Amplitude Weight Access	384
Total Instructions/Dwell	1164

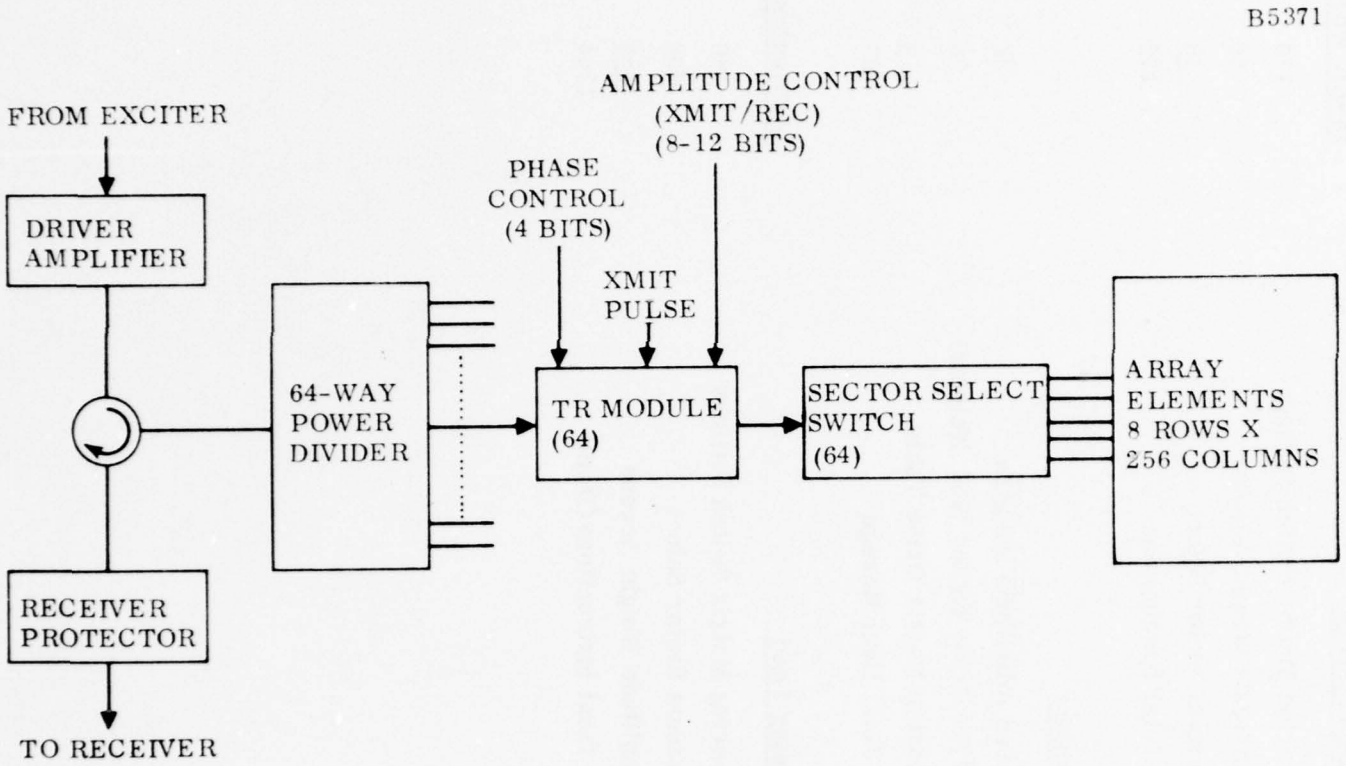


Figure 5-14. Delay-Bit Steered Cylindrical Array

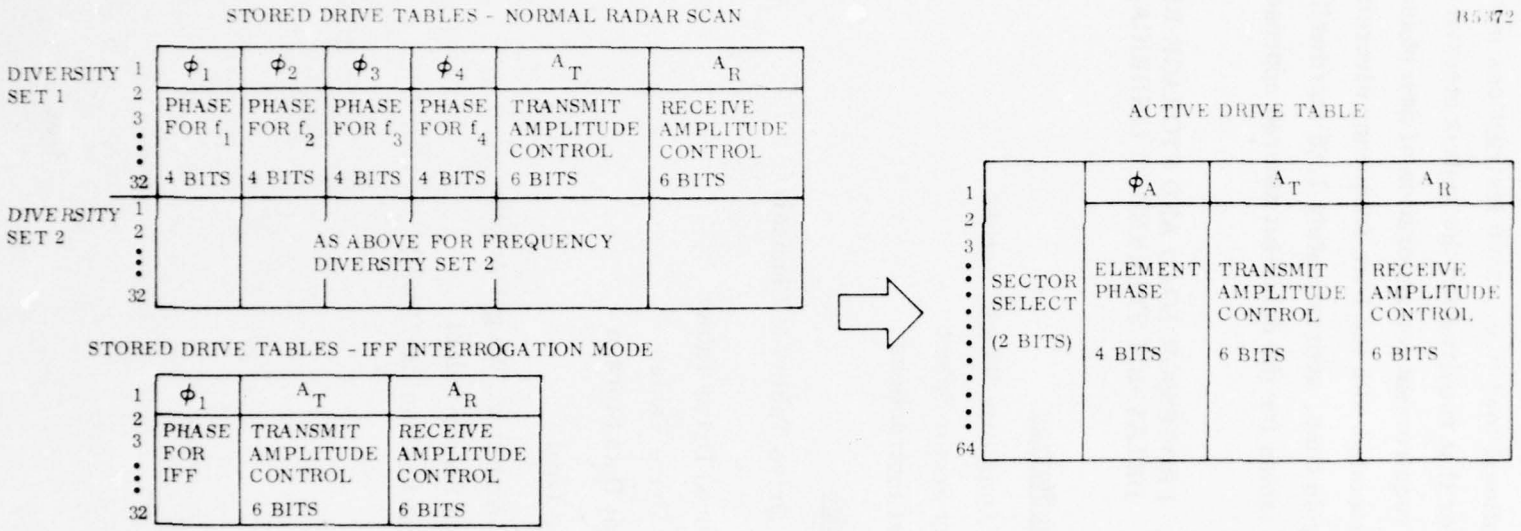


Figure 5-15. Delay Bit Steered Drive Table Definition

The processor load and storage requirements are summarized in Table 5-11. Note that the computational load (i.e., 3300 instructions per dwell) has increased approximately 3:1 over that required for the matrix steered configuration. This is primarily due to the requirement for generation of new phase control words for each frequency change associated with the four-frequency diversity waveforms. Again, assuming a 0.5 μs cycle time, approximately 1.65 ms/dwell (27.28 ms) is required to compute the drive tables for the delay-bit steered approach.

TABLE 5-11. PROCESSOR LOAD AND STORAGE REQUIREMENTS FOR DELAY-BIT STEERED CYLINDRICAL ARRAY

Instruction Storage	16 Bit Words
Phase/Amplitude Weight Access	20
Element Sector Select	16
Total Instructions	36
Data Storage	**16 Bit Words**
Stored Drive Tables (4 Channels/ 2 sets)	128
IFF Stored Drive Tables	32
Active Drive Tables	64
Total Data Storage	224
Processor Load	**Instruction Dwell**
Phase/Amplitude Weight Access	2600
Element Sector Select	700
Total Instructions/Dwell	3300

c. RADAR CONTROL PROCESSOR/SYNCHRONIZER SUMMARY

While the Delay-Bit Steered Cylindrical Array approach results in a somewhat higher (3:1) processing load for the Radar Control Processor, the matrix-stored and delay-bit steered approaches are essentially comparable in terms of overall storage requirements ($\approx$ 250 words). The remaining command words, summarized in Table 5-12 represents a small additional load on the synchronizer in comparison to performing the array steering function.

TABLE 5-12. SYNCHRONIZER DRIVE COMMANDS

Exciter/Waveform Generator Commands

	Data Bits
Main Bang or Transmit Pulse	1
Transmit/Receive	1
Radar/IFF Mode Control	1
IFF Mode Select	8
Frequency Select	3

Signal Processor Commands

	Data Bits
Range Counter Start	1
End PRP	1
Detection Threshold	16

6. REMOTE SITE CONTROL PROCESSOR

The Remote Site Control Processor provides the interface for the data link controller to respond to remote site control commands/request and to output track report data and performance status information to the remote control site.

The input and output data associated with the Remote Site Control Processor is summarized in Table 5-13. The primary output data consists of track reports which summarize the track coordinate information and track status information, including the reply information associated with the IFF interrogations. For 20 tracks in the system, transfer of the track reports represents approximately 3520 bits of information which must be output over the 2400 baud line every 12 s (assuming output of all track reports every 3 scans). Operator requests are envisioned to be relatively infrequent and require minimal information transfer.

The only additional burden which may be placed on the Data Link Control is transfer of PM and FD/L information. The level of PM and FD/L support required must be considered as a portion of an overall logistics support trade involving PM and FD/L complexity, spares location etc. and would be handled in a background manner similar to a prioritized time-sharing computer service network. The lead and timing requirements of the PM and FD/L data transmission represents no difficulty with the proposed voice-grade communication link.

7. PERFORMANCE MONITOR/FAULT DETECTION AND LOCATION

A principal design consideration for the PM and FD/L support of the radar system is the ability to operate unattended with cyclic preventive maintenance visits. In order to operate unattended, the PM and FD/L approach must provide for natural redundancy and automatically switched self-healing implementation. In order to accomplish switched self-healing, the hardware design must provide for the ability to detect the occurrence of a fault in order to activate appropriate software/firmware responses to accomplish automatic switching, and provide for reporting to the remote control site of degraded conditions.

The hardware features required to support the PM and FD/L approach are summarized in Table 5-14. The integrity of data and instruction transfers to/from memory is monitored by hardware computation of byte parity to identify faulty memory modules to the performance monitor function. Provision for alternate communication paths between redundant processor modules enables switched self healing, as

TABLE 5-13. DATA LINK CONTROLLER REQUIREMENTS

Output Data

- Track Reports

  Target Slant Range
  Target Slant Range-Rate
  Target Azimuth
  Target Azimuth Rate
  Time of Last Detection
  Hit Count
  IFF Status (Reply Verified, Emergency)
  IFF Verification Time
  FAA Identification Code
  Target Elevation
  Verification Range
  Verification Azimuth

- Performance Status

  Array Control Subsystem Status
  RF Exciter Subsystem Status
  Final Receiver Subsystem Status
  Signal Processor Subsystem Status
  IFF Data Controller Status
  Data Processing Subsystem Status

Input Data

- IFF Requests
- PM and FD/L Requests
- Reconfiguration Commands

TABLE 5-14. HARDWARE PM AND FD/L DESIGN REQUIREMENTS

- Byte Parity - Modulo 2 Count of Ones for All Memory Transfers
- Alternate Communication Paths - Redundant Bus Structure
- Redundant Processing Modules - Switched Self-Healing
- Data Transfer Timeout - Timed Data Transfers to Prevent System Lockup
- Test Signal Injection - System Sensitivity Measurement
- Power Fail Interrupts - Subsystem Failure

well as an ability to compare the outputs of several processors operating on identical data for fault location. Data transfer timeout is provided on all Input/Output (I/O) to facilitate a re-try of an unsuccessful I/O request upon timer runout followed by activation of error recovery procedures (i.e., memory switching for redundant memory modules). The capability to activate test signals injected into the final receiver is required to enable system performance measures to be performed on the receiver-signal processor chain. Test vectors injected to the data processor are required to isolate faulty memory and processor modules. Finally, power fail interrupts are included in the subsystem components to enable recognition of the loss of radar subsystems due to power loss.

Three levels of PM and FD/L are supported directly by software/firmware resident in the processor modules. The first level of support is the on-line error sensing associated with memory parity, power failure and data transfer timeout as summarized in Table 5-15. If any of these errors are sensed in the data processor by the firmware error processing function, an attempt is first made to locate the source of the error by performing memory read/write cycles, register to register transfers and test calculations based on test vector injection. If the error is located, an attempt to reconfigure the system is performed via reallocation of memory modules, or by disabling (i.e., set busy) faulty processors. When possible, self-tests are activated in faulty processors to isolate a fault to the board level. The degraded status is reported to the remote site controller and recorded to support subsequent system test levels.

A second level of system test is activated on a periodic basis to assess overall system health. The second level of testing consists of test vectors injected to the data processing subsystem, as described above, together with injection of test signals by the exciter/waveform generator to the final receiver. The test signals from the exciter/waveform generator enable measures of system sensitivity to be performed to validate the receiver-signal processor chain. Status is again reported to the remote site control process via the data link controller.

A third level is system PM and FD/L involves human interaction. This level of test involves both status assessment and interactive control. Selective execution of subsystem and system level tests is performed in response to operator requests over the data link based on operator assessment of the performance status information returned over the link. The status assessment includes a detailed reporting of

TABLE 5-15. PM AND FD/L APPROACH SOFTWARE/FIRMWAVE DESIGN

Level	Activation Mechanism	Processing
1	Error Detected Parity Power Fail Timeout	• Error Location via Status Word Identify Nature of Fault Reconfigure Activate Module Self-Test Report Degraded Status
2	Periodically	• Subsystem Test Test Vector Injection Status Report • System Performance Evaluation Test Signal Injection for Sensitivity Measurement
3	Remote Control	• Selective Execution of Subsystem/System Test • Directed Reconfiguration • System Reinitialization

system parameters, such as interference measures and detection thresholds. Based on performance assessment, the operator then performs a commanded system reconfiguration to remove defective modules from the active processing lineup if required.

Capability for a fourth level of PM and FD/L must be recognized. The data processor architecture must also provide for support of on-site maintenance. It is anticipated that the resident PM and FD/L software/firmwave will be sufficient to isolate faults to the board level. On-site interactive control and response can be provided via an interface to the data link controller with an interactive display terminal (either on-site or transported to the unattended site by maintenance personnel). Operation of FD/L can be accomplished to an arbitrary low level by also providing for diagnostic program entry via the display terminal or via an on-site magnetic peripheral provided for system program initialization. The final decision on the level of PM and FD/L is a portion of a total system network logistics support trade. The data processor hardware architecture to be described in the subsequent sections is supportive of the basic PM and FD/L approach described above.

8. DATA PROCESSOR ARCHITECTURE

The architecture chosen for the Data Processor implementation was influenced by the functional requirements it must meet but also by the important factors of cost, reliability, ease of fault location, and maintainability concepts of modularity. The details of each of these features of the architecture are to be described in this section.

The functional requirements indicate both a large volume of signal processor and IFF outputs and a corresponding complexity of the Data Processing and Reduction Task to reduce the outputs of the signal and IFF processor to target detection and target tracks. Analysis of these requirements suggests a network of multiple processors as a favorable method of implementation. Modularity and reliability considerations indicate each processor should be identical to the others and fault tolerance should be a design constraint. The generalized architecture of Figure 5-16 is implied, but not practical.

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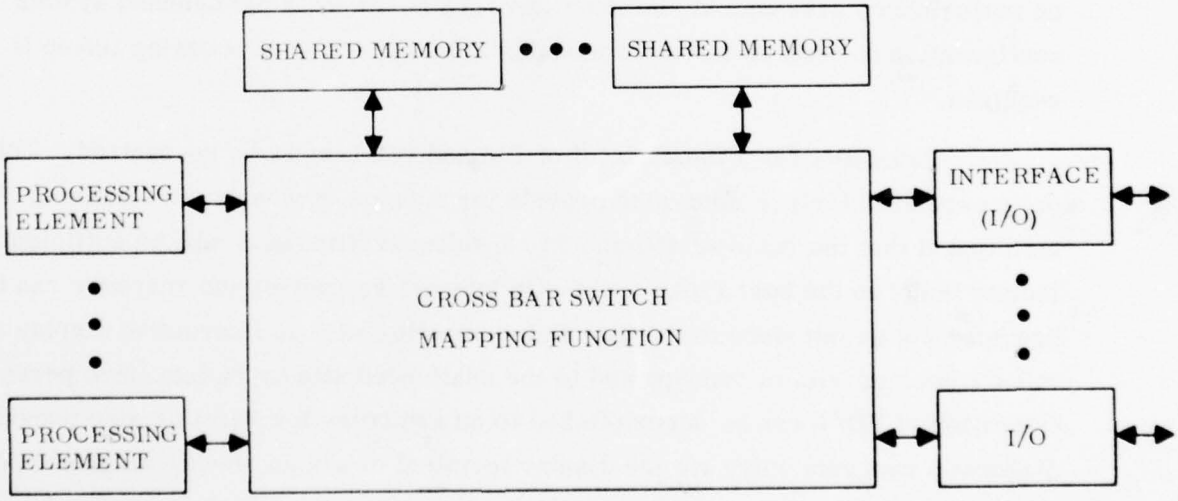


Figure 5-16. Processor Network

The multiplicity of paths evident and their cost is not only undesirable but unnecessary. The interfaces are limited to signal and IFF processor returns, and the command interfaces to the synchronizer and data link functions. By using a FIFO organized memory, each of these may be buffered from radar time and introduced as sections of the shared memory. This shared memory may be partitioned into a target returns section and a command sequencing function. Task directives, synchronizer commands, track files, data link files, and clutter map functions are broadly referred to as command sequencing activities.

Control sequencing for the network of processors is accomplished by placing task directives in one of the FIFO queues (prioritized according to level) organized for that purpose. Each processor as it completes a previous job, scans the task directive file for the next task. This task directive directs the processor to begin a given operation, receive data from a particular source, place results in a given shared memory, and schedule further processing. This mechanism allows each processor to function independently of every other. Changing the number of processors affects reliability and the overall processing rate but does not change the control philosophy or implementation.

Processor loading studies indicate the functional requirements of the aligned system could be met in four processors, with six processors required for the unaligned signal processor approach. Fail safe concepts increase this by one processor for either system. This now completes the overall structure of the hardware implementation. Figure 5-17 details the composite structure and Table 5-16 summarizes the total devices and power consumption. Each of the component blocks is next detailed.

TABLE 5-16. POWER AND DEVICE SUMMARY

		Devices	Power (W)
I	1 IFF Processor	70	6.8
II	Data Processor		
	5 Processing Elements 50/16.1	250	80.5
	5 Data Memories 60/11.3	300	56.5
	5 Program Memories 51/4.0	255	20.0
	1 Clutter Map	63	12.5
	1 Synchronizer/Data Link	49	3.5
	Totals	987	178.8

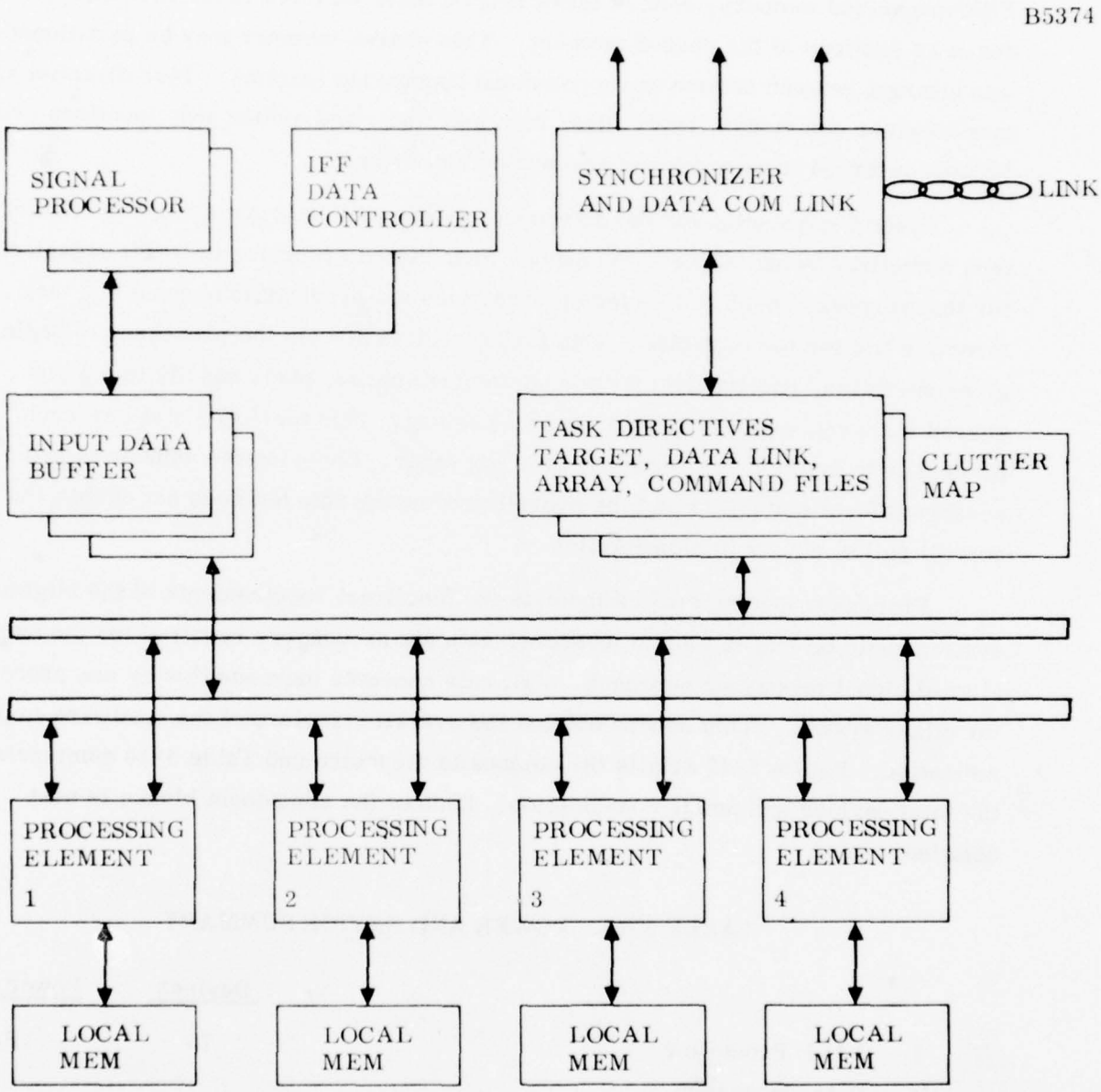


Figure 5-17. Overall Data Processor Configuration

a. PROCESSING ELEMENT

The first system building block to be considered is the Processing Element (PE). This module performs most of the mathematical and sequencing functions of a microprogrammable general-purpose computer. The mathematical functions are implemented in a bit-sliced microprocessor chip set. A 16-bit Arithmetic Logic Unit (ALU) is adequate to serve most of the functional requirements and is augmented by a small amount of shift logic to facilitate multiple shifts, multiplication and division.

The control sequencing functions are implemented in a microprogram sequencer. Multiple levels of looping and microsubrouting and a single microcycle-conditional branch capability allow efficient implementation of bit test and controller functions. Simultaneous generation of address and ALU mathematical functions are provided for by parallel data and address paths and separate hardware elements. This allows the flexible use of memories as general-purpose registers. Error checking hardware is included to simplify performance monitoring (PM). Real and pseudoparity of the data bus is used to functionally check proper program execution on a cycle-by-cycle basis.

In view of the importance of optimizing the power-speed characteristics of this module, two implementations were studied. The first is a complementary metal oxide semiconductor (CMOS) design employing the recently announced Fairchild chip set (CMOS macrologic -4700 series). The second design features low-power Schottky logic (LS-TTL) in a system employing both AMD parts (AM2901 microprocessors) and Fairchild Parts (LS-TTL Macro logic-9400 series). Each of these processors have their strengths and only through close examination is a proper evaluation possible.

The CMOS processor is diagrammed in Figure 5-18. This chip set is compatible with the generalized four-bus architecture (data in, out, control, and address) and is optimized to make maximum use of the narrow microcode PROM width. Overall there are 27 Registers (REG), (8 in the 4705 ALU, 16 in the 4710 File and 3 in the 4707 data address reg), distributed within the processor but not all of these may be classes of general-purpose single-cycle registers. Note the inclusion of offset branch and multi-instruction loop capability with the mircoprogram sequencer. The

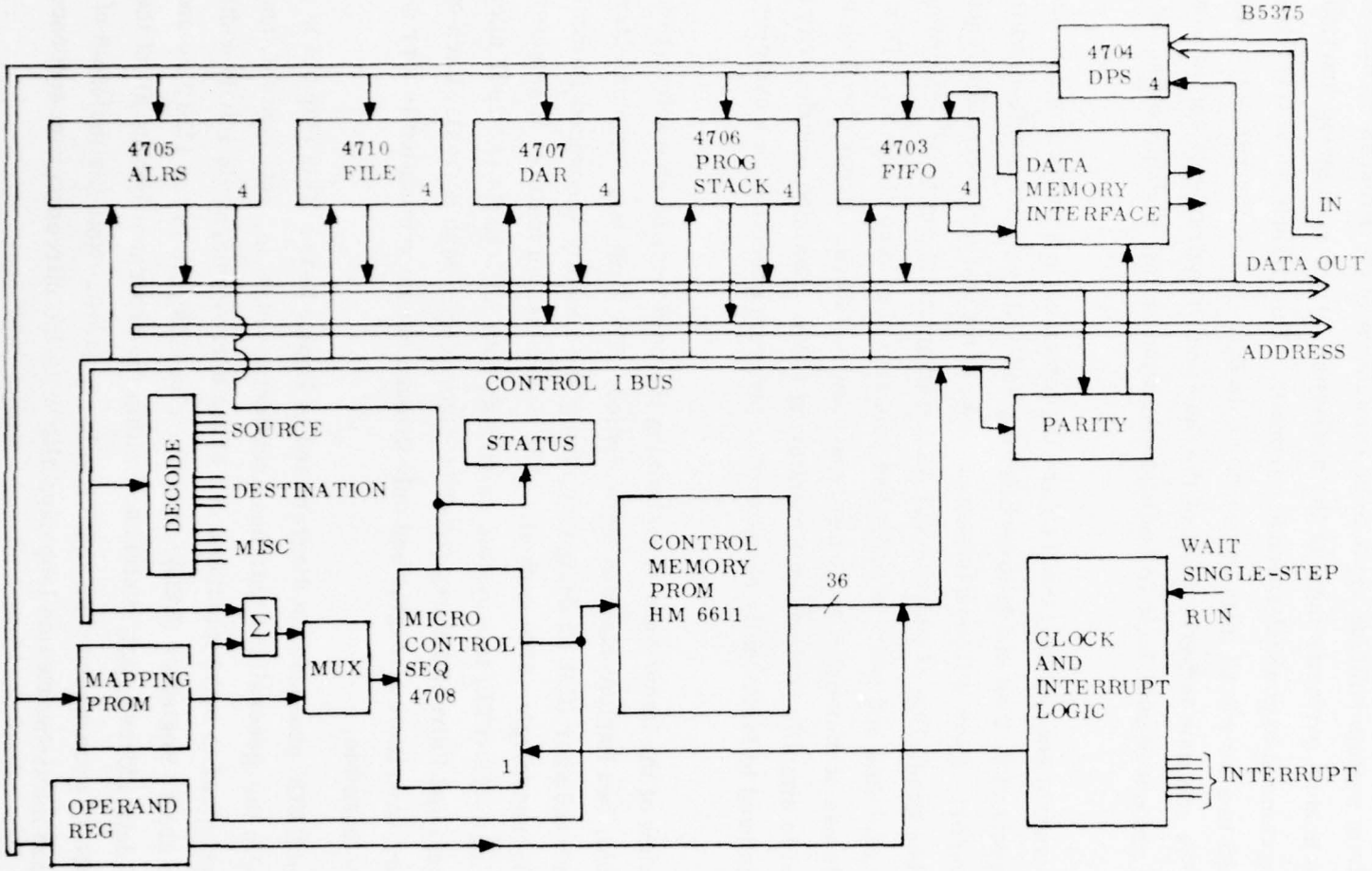


Figure 5-18. CMOS PE Architecture

parts list and layout area summary (Table 5-17) detail the low expected power of the CMOS implementation. Device specifications indicate a typical microcycle time of 2.5 μs for nonpipelined processor (i.e., incorporating branch and jump class instructions) operating from 5 V power supplies. Improvement by a factor of two is possible by raising the supply to 10 V but system interconnections compatibility suffers.

Figure 5-19 details the LS-TTL processor. Math and logic operations are performed in the ALU section of the AM2901. The data path organization of this device emphasizes flexibility in use of the 16-general purpose and Q-registers. Memory address operations may occur independently as they are performed in a separate adder (part of the Data Address Reg 9407). The control ROM efficiency is not as high with this processor — a 40 bit word width is required. The control sequencer is functionally the same as the CMOS version with higher speed. The power and parts list is summarized in Table 5-18. A microcycle of 400 ns is feasible for the nonpipelined processor.

Comparison of the two technologies is now possible. The speed power product for each of the implementations is nearly identical (0.4 μs x 15 W = 2.5 μs x 2.5 W = 6 μW/s). A calculation-limited application of these processors will require more CMOS processors. Hence, construction costs will be higher. Fault-tolerant design practices will however favor the CMOS processor, the extra redundant processor consumes less power. Overall, a good argument could be made for either implementation. LSTTL is recognized to be a more mature, high reliability technology. The parts chosen are "second-sourced", well qualified, proven devices. On this basis, the LSTTL processor is recommended as lowest risk. However, the implementation time frame may well change this decision in light of specific product lines available within a year (i.e., prior to the Engineering Development Model Contract Phases.

The quoted cycle times were on the basis of a nonpipelined processor architecture (i.e., including provision for branch and jump class instructions). This choice was made from the observation of the frequency of conditional branch decisions to the data processing algorithms. Selection of speed compatible memory and I/O components also allow most operations to be performed in a single microcycle. These factors weigh heavily in the chosen architecture.

TABLE 5-17. PARTS LIST FOR CMOS PE

Q	Type	Function	Width Pins/ Power (mW)
8	F4703	FIFO Buffer Register	0.4-24/50
4	F4704	Data Path Switch	0.4-24/50
4	F4705	Arithmatic Register Logic Stack	0.4-24/50
4	F4706	Program Counter Stack	0.4-24/50
4	F4707	Data Address Register	0.4-24/50
1	F4708	Microprogram Counter	0.6-40/50
4	F4710	Register File	0.3-18/20
1	F4582	Look Ahead Carry	0.3-16/10
1	F4008	4-Bit Adder	0.3-16/10
6	F40097	Tri-State Buffer	0.3-16/10
20	Hm6611	256 x 4 PROM's	0.3-16/50
2	F4531	Parity Element	0.3-16/10
1	F4532	Priority Encoder	0.3-16/10
7	F4076	Registers	0.3-16/10
5	CMOS & LS-TTL	Misc SSI	0.3-16/40
72			65 $in.^2$/2.7 W

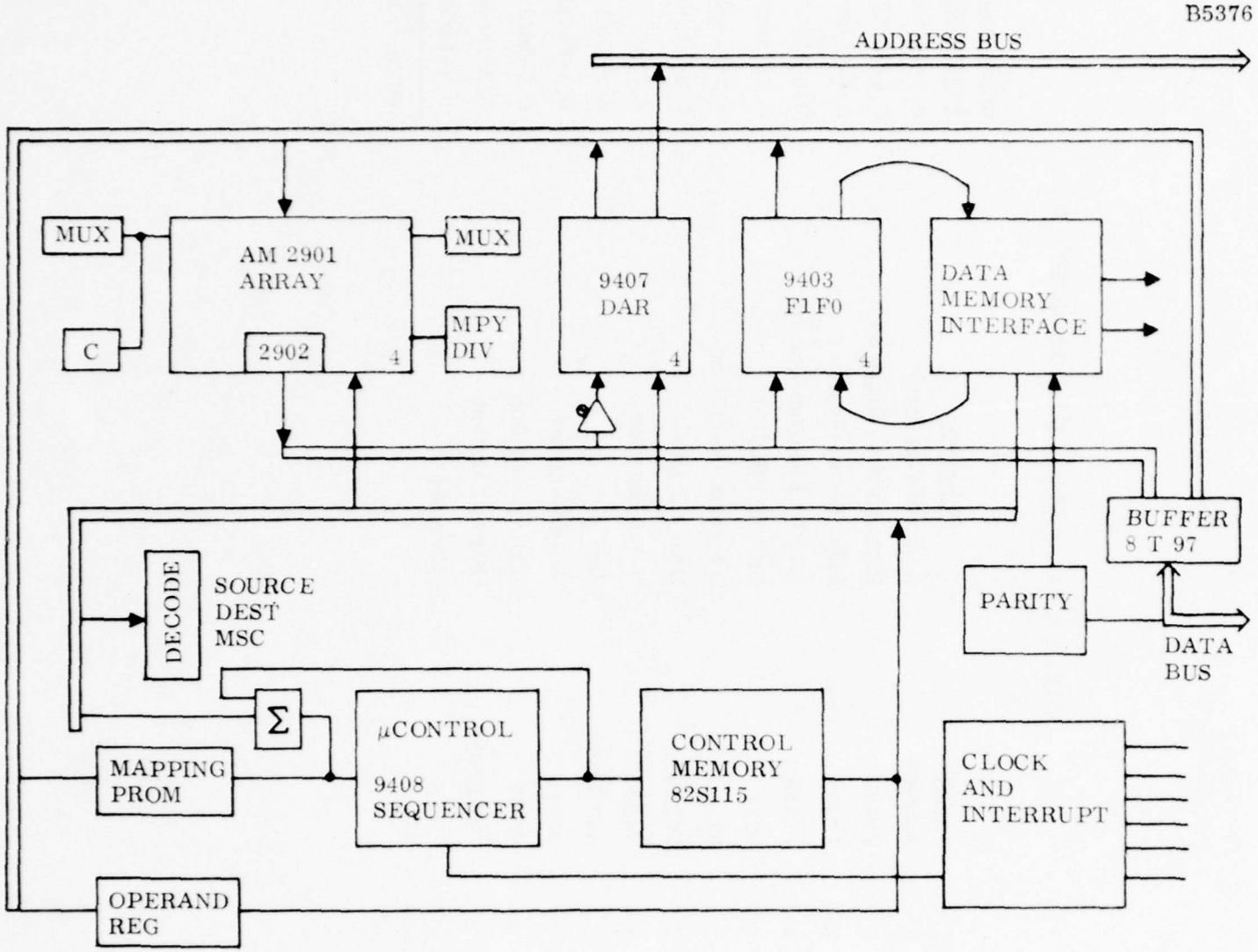


Figure 5-19. LS-TTL PE Architecture

TABLE 5-18. PARTS LIST FOR LS-TTL PE

Q	Type	Function	Width Pins/ Power (mW)
4	AM2901	ALU and Reg Stack	0.6-40/800
4	F9407	Data Address Register	0.4-24/600
4	F9403	FIFO Buffer Register	0.4-24/600
1	F9408	MICRO Program Counter	0.6-40/600
6	82S115	512 x 8 PROM's	0.6-24/800
1	3214	Interrupt Controller	0.6-24/550
2	74LS253	Dual 4:1 Mux	0.3-16/50
6	74LS374	8-Bit Register	0.3-20/70
5	74LS138	Decoder	0.3-16/50
2	AM2918	4 Bit Register	0.3-20/150
3	8T97	Tristate Buffer	0.3-16/200
2	74L3280	Parity Element	0.3-16/70
10	74LS	Misc SSI	0.3-16/50
50			60 in.^{2}/16.1 W

The microcode memory was sized (512 words) to allow the inclusion of both a "standard" instruction set and the run-time critical special functions in all processors. A simplified standard instruction set, composed of 30-40 instructions and 3-4 addressing modes, allows optimum efficiency in programming for the calibration, track, data communication, and PM routines. The short real-time software functions may be optimized for speed by microcoding the critical sequences.

b. DATA MEMORY

For each of the systems under consideration, there is a requirement for a large data memory module. Buffering of signal and IFF processor outputs, track store, command files, synchronizer data-link drive files and the interprocess data base all contribute to the total memory load. Each of these must be able to be accessed independently by each of the PE's but the number of data organizations of each file may be limited. FIFO organization is considered ideal for the signal processor outputs and command and drive files. However, multiple word associations are required for some of the track and interprocess files. An intelligent Memory Controller (MC) is proposed to solve these problems and provide the extra capability needed for a fault-tolerant network organization. This MC will also eliminate much of the load-store overhead associated with the use of general-purpose processors. The transfer bus between the PE's and their data memories has both a data field and a job tag field. The job tag tells the memory controller a group of words is desired (read mode) or are waiting (write mode) for transfer. The MC associates the type of group and their number with real-physical memory locations. Short FIFO buffers allow the memories and processing elements to work asynchronously.

CCD memory technology promises several speed, power and density benefits that are important to this application. The Line-Addressed Random Access Memory (LARAM) architecture (Fairchild-CCD460) is suitable for implementing all the desired data organizations. Each IC contains 16384 bits of memory organized as 32 groups of 128 four bit words. A 4096 word block is formed by using 4 together. Figure 5-20 details the functional organization of the data memory. Four 4096 word blocks form the page boundaries and are controlled by a single MC. PE reference

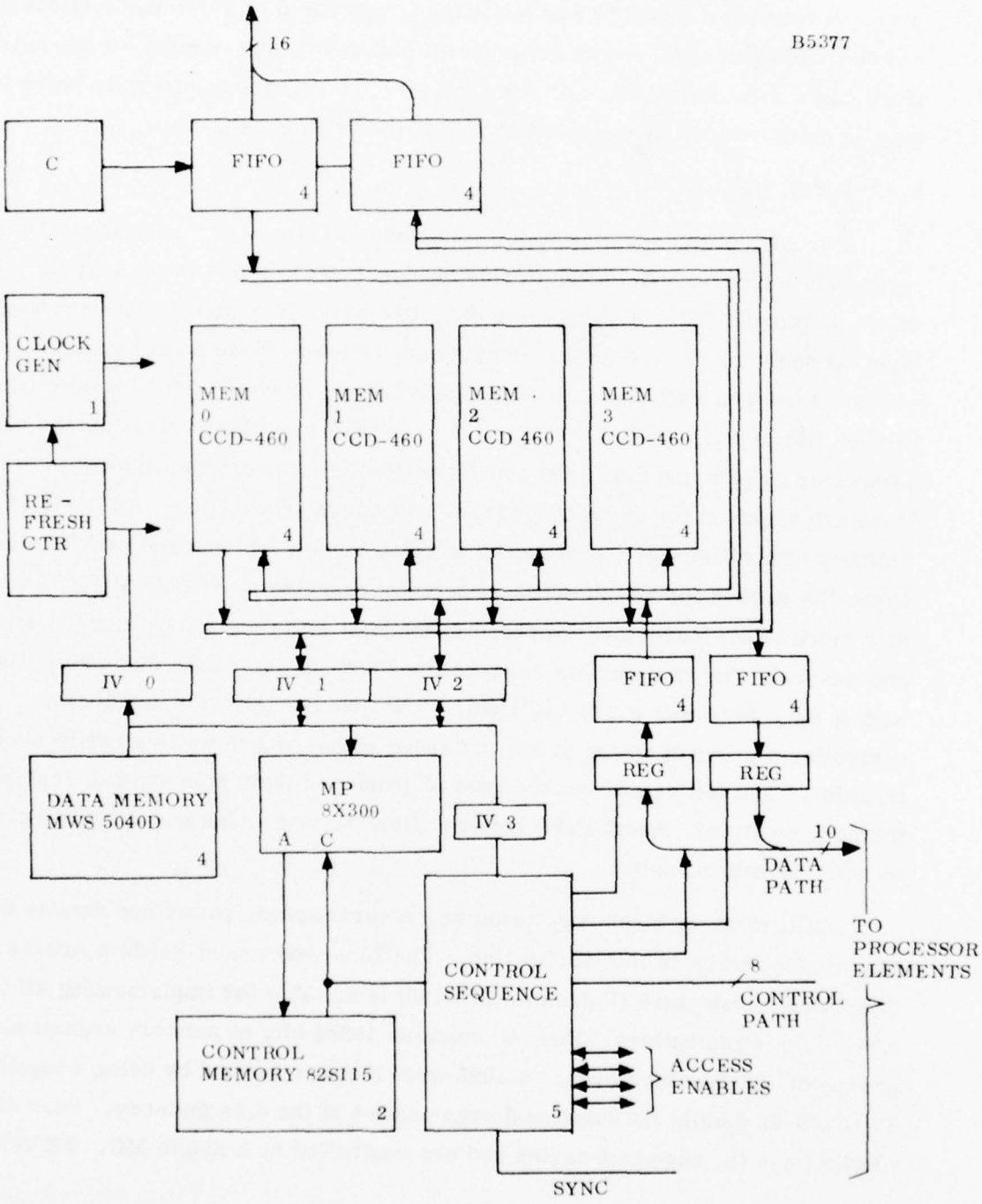


Figure 5-20. FIFO Block Diagram

to a given piece of data is made via a page register and a functional mode of data transfer. This information is contained in the 8-bit job tag field partioned in the following manner:

7	6 5	4 3	2 1 0
R/W	Page No.	Spare	Mode

Block transfers of data at the end of the radar time cycle is prevented as both the page and block access to the data is by programmable indirect memory reference. The CDC memory requires periodic refreshing to retain data. This is performed via special counters - the end user of the data, the PE, is blind to the refresh process. The MC keeps tabs on the refresh process and the position of the data in each of the 128 register groups it controls.

The memory controller is a Signetics 8 x 300. This monolithic IC is a high-speed (300-ns cycle time) microprocessor optimized for controller applications. Featuring a separate control and data path and compatible support IC's (data interface -8T32 and control PROM 82S 115), this processor greatly reduces the random logic required to construct the control functions. The multiple-data transfer modes are all implemented in firmware increasing the versatility. In order to implement the indirect data reference modes, coordination between MC's must be arranged. Each of the memories decode by function, not by real address. The MC's scan the control registers for a data transfer request. The selected memory page will stack up data to be transferred in the buffer FIFO conditional on space in the FIFO and refresh state of the particular memory register. Synchronizing signals allow alternate data transfers from different pages and other sophisticated data structures.

The other interface interacts with the outside world through a FIFO buffer. This part is programmable as well and allows both input and output at various asynchronous rates. Interaction with the signal and IFF processor (input) and the synchronizer and data link (input and output) is expected but others are possible.

Table 5-19 details the expected parts and power lists. Only one version of this board was studied -- speed compatible with the LSTTL processor. The operating firmware was roughed out to check conceptual validity. It is expected the proposed configuration would support the 1 MHz data rate of the signal processor paths.

TABLE 5-19. PARTS FOR FIFO BUFFER

Q	Type	Function	Width Pins/ Power (mW)
16	F4703	16 x 4 VMOS FIFO	0.4-24/50
16	CCD460	16384 CCD Memory	0.4-22/200
1	8 x 300	Control Interpreter μP	0.9-50/1800
2	82S115	512 x 8 PROM	0.6-24/600
4	8T33	Interface Vectors	0.6-24/600
2	MWS 5040 D	CMOS Data Memory (256 x 4)	0.4-22/5
8	74C174	4-Bit Register	0.3-16/10
2	74C169	Counter	0.3-16/10
1		Clock Generator	0.3-16/100
6	74LS	Misc Control	0.3-16/70
2	74C85	Comparators	0.3-16/10
62			62 in.^{2} /11.3 W

Control Word 8 Bits



Mode

0	PM - Test and Status
1 ↓ 6	Data Organization Format
7	Idle Mode

Special mention should be made of the fact that data from the CCD memories does not actually pass through the 8 x 300 processor. Access strobes and enables gate the data directly to the buffer.

PM and FD/L has been considered in configuring the data memory. Additional data paths (serial transfers in the FIFO buffers) allow quite extensive self-test functions. The page and block register circuitry is to be reinitialized to reflect hardware faults. Continued operation is possible as spare memory pages are to be included in system sizing. The design of the control register scanner is somewhat critical in this respect. Fail-safe design practices are required since each page contains a scanner. Provision is made for disabling the rest under normal operation, as only one is needed. Disabling from an external source (PE) may be required for certain hardware faults.

c. PROGRAM MEMORY

Associated with each of the processing elements is a program memory board. In addition to its program storage role, this board contains two data memory interfaces. *Nonvolitile storage* (PROM) is provided for 512 words of programs associated with System Initialization (SIN), data communication and PM/status processing. These functions have to be able to be performed immediately after any power interruption. All other programs are resident in the RAM memory. Initialization of this memory is performed by use of a nonvolitile magnetic peripheral or by data-comm link. Battery power backup is a third alternative as the standby power requirement is quite low.

Figure 5-21 and Table 5-20 detail the chosen implementation. CMOS memories are chosen for their medium-speed low power characteristics. Compensation for access times is accomplished by a wait signal returned to the clock timing circuit of the PE. Access times for the CMOS on silicon-on-sapphire (SOS) RAM and the data memory interfaces are short enough to allow 400-500 ns cycle times. PROM access times would add about 100-220 ns to this. Parity protection is included on RAM transactions. Expansion to 8K of RAM or additional PROM is possible considering the low density of board components.

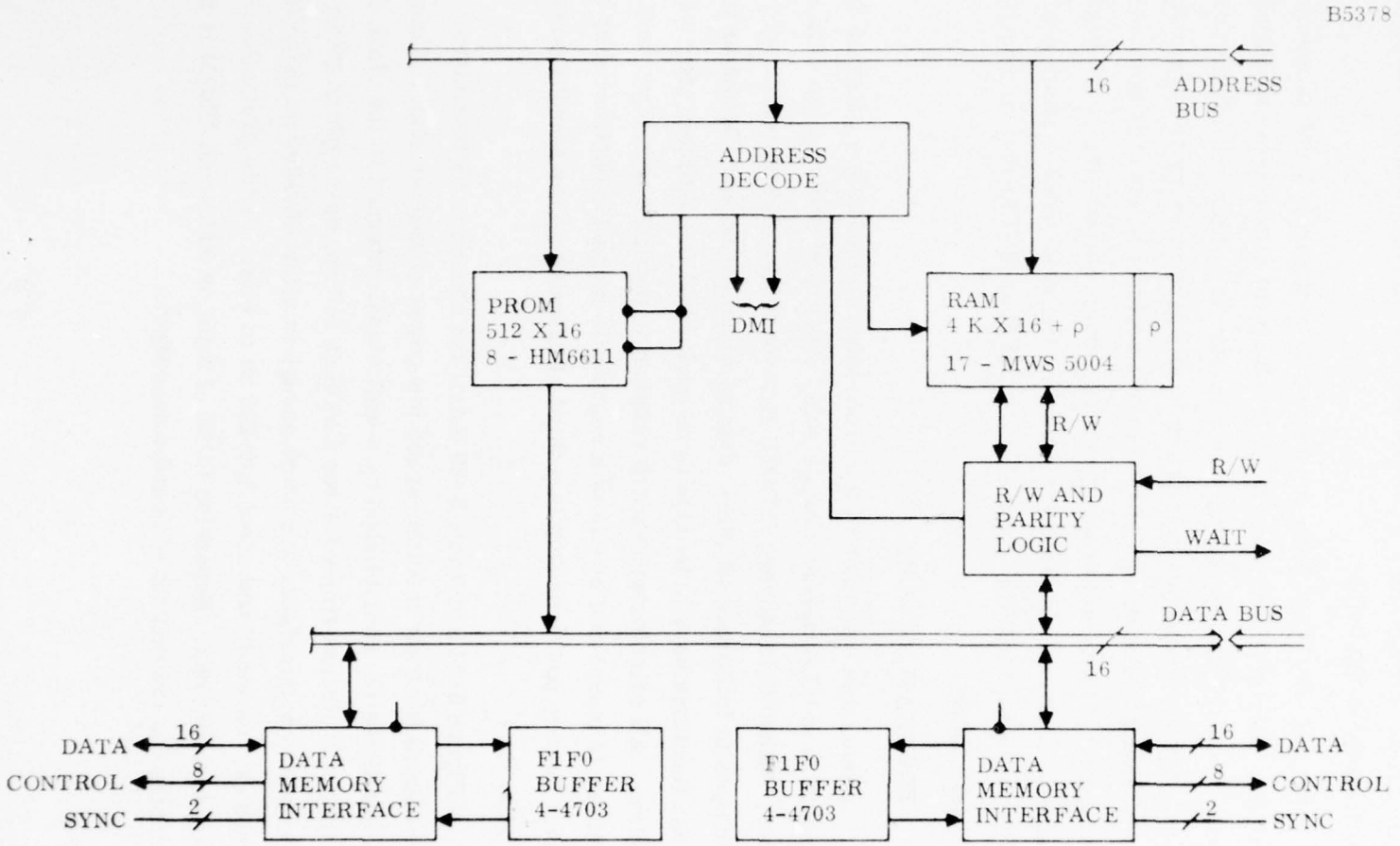


Figure 5-21. Program Memory Block Diagram

TABLE 5-20. PARTS LIST FOR PROGRAM MEMORY

Q	Type	Function	Width Pins/ Power (mW)
17	MWS 5004	4KX1 CMOS PAM	0.3-16/50
8	HMbb11	256X4 CMOS PROM	0.3-16/50
8	F4703	FIFO Buffer Register	0.4-24/50
2	74LS280	Parity Element	0.3-16/70
2	74LS138	Decoder	0.3-16/70
10	74LS374	Register	0.3-16/70
10	74LS	Misc SSI	0.3-16/70
57			50 $in.^2$/4.0W

d. CLUTTER MAP

The clutter map (see Figure 5-22) requires a large store (52852 words) to remember the zero Doppler channel ground clutter returns. The data is range and azimuth ordered so random access is not required in the step scan mode. The interface to this memory should be compatible with the previously defined system concept. Overall reliability is a requirement as well, since as a unit, duplication is not desirable. Further, this module should be compatible with the self-diagnosis features of the PM and FD/L architecture.

One possible implementation of the clutter map is to use four of the data memory modules. This approach satisfies all of the above requirements but does so at a high cost and power demand. Another CCD memory is scheduled for release in the first quarter of 1977 - the Fairchild CCD-465. This is a serial-parallel-serial organized 65536 x 1 memory. Using this IC, it is possible to realize the clutter map on a single board. A single-bit Hamming error correction mechanism is included to provide the needed reliability. Five additional check bits are stored with each word, hence the memory size is 20 bits (15 bits of positive magnitude + 5 check bits). A reliability improvement of 5-to-1 is expected for 5000 h operation time. The clutter map memory is interfaced to the system buses exactly as are data memories. An 8 x 300 microprocessor is used as the interface manager. Self-test and PM capabilities thus may be included.

The functional block diagram is presented in Figure 5-22. The parts and power requirements are summarized in Table 5-21.

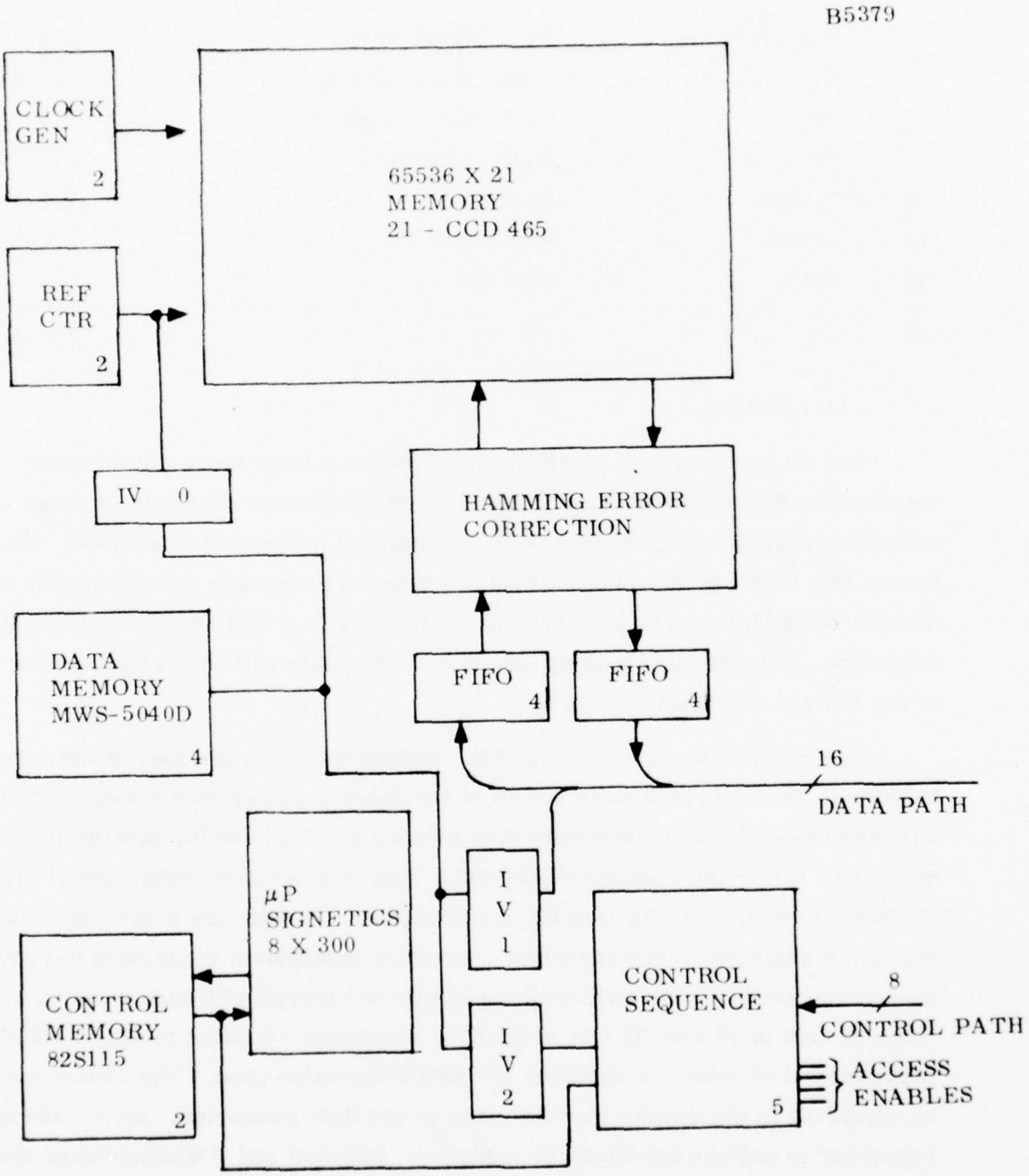


Figure 5-22. Clutter Map Memory

TABLE 5-21. PARTS LIST FOR CLUTTER MAP

Q	Type	Function	Width Pins/ Power (mW)
21	CCD465	65536 CCD Memory	0.3-16/300
8	F4703	16 x 4 FIFO Memory	0.4-24/50
1	8 x 300	Control Interpreter (μP)	0.9-50/1800
2	825115	PROM 512 x 8	0.6-24/600
3	8T33	Interface Vector	0.6-24/600
2	MWS 5040D	256 x 4 CMDS Memory	0.4-22/5
2	74C169	Binary Counter	0.3-16/20
2	-	Clock Generator	0.3-16/200
5	-	Parity Generator	0.3-16/10
4	74C86	Xdr	0.3-16/10
2	74C138	Decoder	0.3-16/10
6	74C174	Register	0.3-16/10
5	74Ls	Misc Control	0.3-16/70
63			56 in.^{2}/12.5 W

9. DATA COMMUNICATION LINK

Sharing part of the board allotted to the synchronizer output logic is the Data Communication Link logic. This function makes maximum use of available Large Scale Integration (LSI) components for the baud rate generator (Fairchild F4702) the universal asynchronous receiver/transmitter (UART-Harris Hd - 6402) and universal modem (Motorola MC 6860). Use of standard frequencies and data rates simplifies the communication interface. On-site maintenance may be simplified by the use of a "suitcase" system monitor made up of existing commercial peripherials. The data-comm link interface would serve this second function as well.

The implementation is pictured in Figure 5-23 and summarized in Table 5-22. The left interface is designed to work with the parallel output of a data memory. Link information would be stored in a FIFO organized data file available to any of the PE's. The communication linkup on the right side is to be made via either a direct wire connection or radio link. Further study is required for this specification.

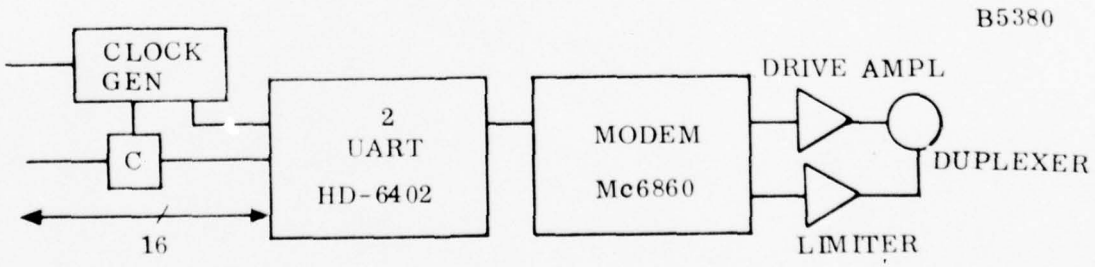


Figure 5-23. Data Communication Link Block

Table 5-22. PARTS LIST FOR DATA COMMUNICATIONS

Q	Type	Function	Width Pins/ Power (mW)
2	HD-6402	CMOS UART	0.6-40/50
1	MC 6860	Modem	0.6-24/300
1		Drive Amplifier	0.3-16/500
1		Limiter Amplifier	0.3-16/300
1	F4702	Clock Generator	0.3-16/50
3	CMOS	Misc SSI	0.3-16/20
	Misc	Discrete Parts	10 2
9			21 in.^{2}/1.30 W

10. RADAR SYNCHRONIZER

The purpose of the Radar Synchronizer is to accept instructions from a control source (computer) and translate them into control, data, and timing signals for operation of the radar. It also provides for acquisition, preprocessing, formatting, and transmission of resulting target data, performance measurements and status information to a data link. A functional diagram appears in Figure 5-24.

Each unique period of radar operation is represented by a preprogrammed block of instructions stored in a microcomputer. Subfields of these instructions control key events which must take place or parameter values which are to be used during that operation. Times at which these instructions are to be executed are accurately controlled by a time tag subfield. When system functions are scheduled by the CPU, the corresponding control instruction blocks are placed in an output queue for transmission to the Synchronizer, where they are entered into a FIFO command que to await execution.

In the Unattended Radar, a given synchronizer input command instruction is defined for each type of PRP to be executed. Additional instructions may define modifiers for PRP instructions such as an "end of range" or "generate a test target and take a PM test sample", etc., during execution of a PRP. Each instruction contains a time field (to indicate execution time) as well as mode and data fields required to perform the desired action. The execution of PRP type instructions resets the radar time count, thus referencing all PRP and/or modifying and supplemental instructions to the beginning of the PRP in which they occur.

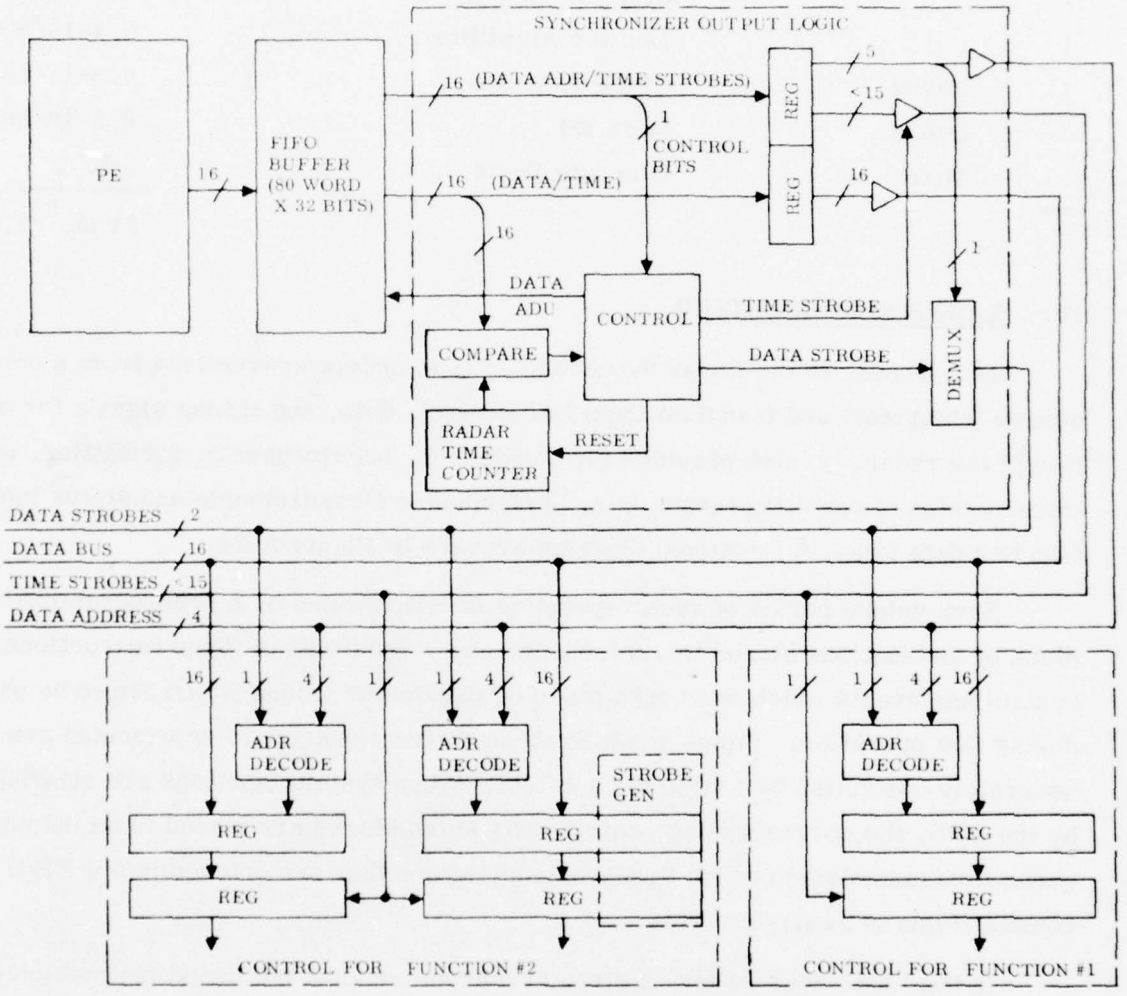
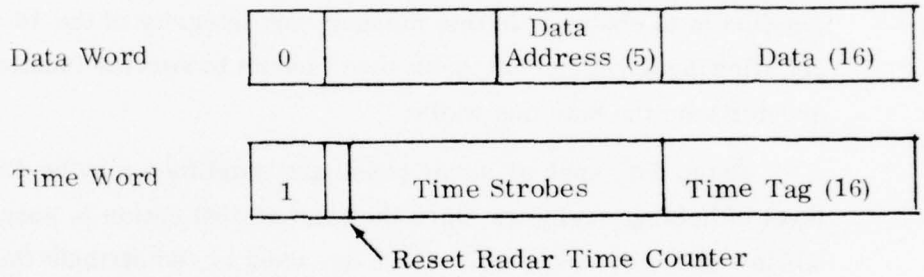


Figure 5-24. Synchronizer

The above concept of operation is important because it means that the radar system operation is programmable. Any realizable set of operations can be created within a waveform period and any mixture of periods can be scheduled. The CPU is effectively divorced from high-speed real-time operational constraints and the intricacy of radar timing and control is removed as an influence on software development and maintenance.

The function of the synchronizer now becomes that of translating the synchronizer input commands into an ordered set of data and time words which can operate on the controlled function storage registers. The required format of the data and time words is shown below:



A data word is defined for each 16-bit byte defined for the controlled functions. The data field is broken down into unique subfields for a given 16-bit byte and a specific address is assigned.

The time word contains a time tag field which is compared with a radar time counter. On compare, time strobes are generated as indicated by the contents of the time strobe field. The reset radar time counter bit allows selective reset of the radar time counter at the beginning of each PRP.

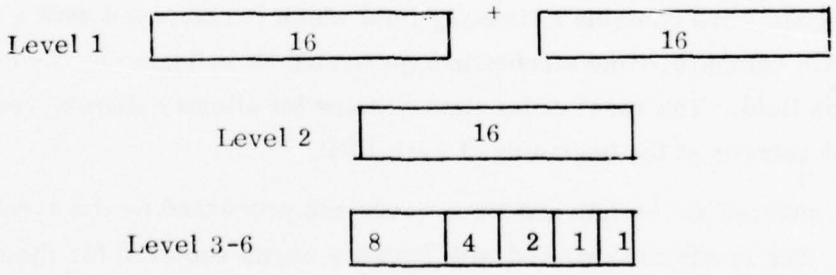
The ordered set of data and time words are processed by the synchronizer output logic. The words are ordered with the data words required for the next control change followed by a time word with the corresponding time strobe bits set. Data words are transferred by the output logic as soon as they are received. Time words are held until a compare occurs between the time tag field and the radar time count. When a time compare occurs, the designated time strobes are produced and the output logic advances to the next word.

Data transfers from the synchronizer to the controlled radar subsystem is via a 16-bit data bus, a 4 bit address bus and a data strobe. This method of transfer minimizes the number of interconnecting wires but does require local address decoding for each 16-bit byte of storage register. Time strobes for loading the second register are individually distributed to each controlled function.

For the functional parts of the radar, it is necessary to effect a simultaneous parallel setup condition, since local timing is not provided for an alternate sequential setup. The widths of the output storage registers are of sufficient size to hold the setup data, gates, and strobes required by the function. The output registers are double buffered to allow functional loading from a common data bus when addressed, and the transfer is made to the second register at the time the data to the controlled function is to change. In this manner, the integrity of the 16-bit data bus is preserved yet allowing n-number of 16-bit byte fanouts to service functional requirements greater than the data bus width.

Setup data such as array phase and amplitude may be distributed to a single level of holding registers since the time of application is noncritical within the time window allotted. Data multipliers are used to redistribute the phase and amplitude as required to program the array.

Command data for the matrix steered array may be distributed to the different sections of the array by using four 16-bit words arranged as follows:



Array symmetry reduces the drive requirements by a factor 2^{n-1} at the N^{th} level. Single holding registers are adequate to store the drive control.

The translation from synchronizer input commands to the ordered set of data and time words is implemented using the modular 16-bit microprocessor as designed

for other Unattended Radar data controller applications. The important characteristics and steps of the translation process are as follows:

- The translation process operates on one PRP at a time.
- The PRP instruction is translated into data and time words by a subroutine for the specific type PRP using information from the instruction and a stored data base. The generated data and time words are temporarily stored in a PRP data queue in the μP memory.
- Modifying and supplemental instructions associated with the PRP are processed in a similar way and stored in additional data queues.
- All data queues for the PRP are merged into a time ordered string of data and time words and output to a FIFO buffer. Time and data conflicts are resolved during the merging process. If a time overlap exists with the next PRP, an additional overlap data queue is generated to be processed during the merging of the next PRP.

This synchronizer concept, Figures 5-24 and 5-25 and Table 5-23, has a number of advantages over more conventional implementations:

1. High usage of LSI (in μP), reducing IC board count.
2. Uses standard modular μP configuration, reducing number of different kinds of boards in the system.
3. Unique logic of the synchronizer is not dependent upon the specific functions implemented, allows easy adaptation to different or changing requirements.
4. Output bus concept minimizes output signal fanout.
5. The instruction set for the microprocessor controlled synchronizer and all the data controllers is the same, e.g., each microcode memory is the same.

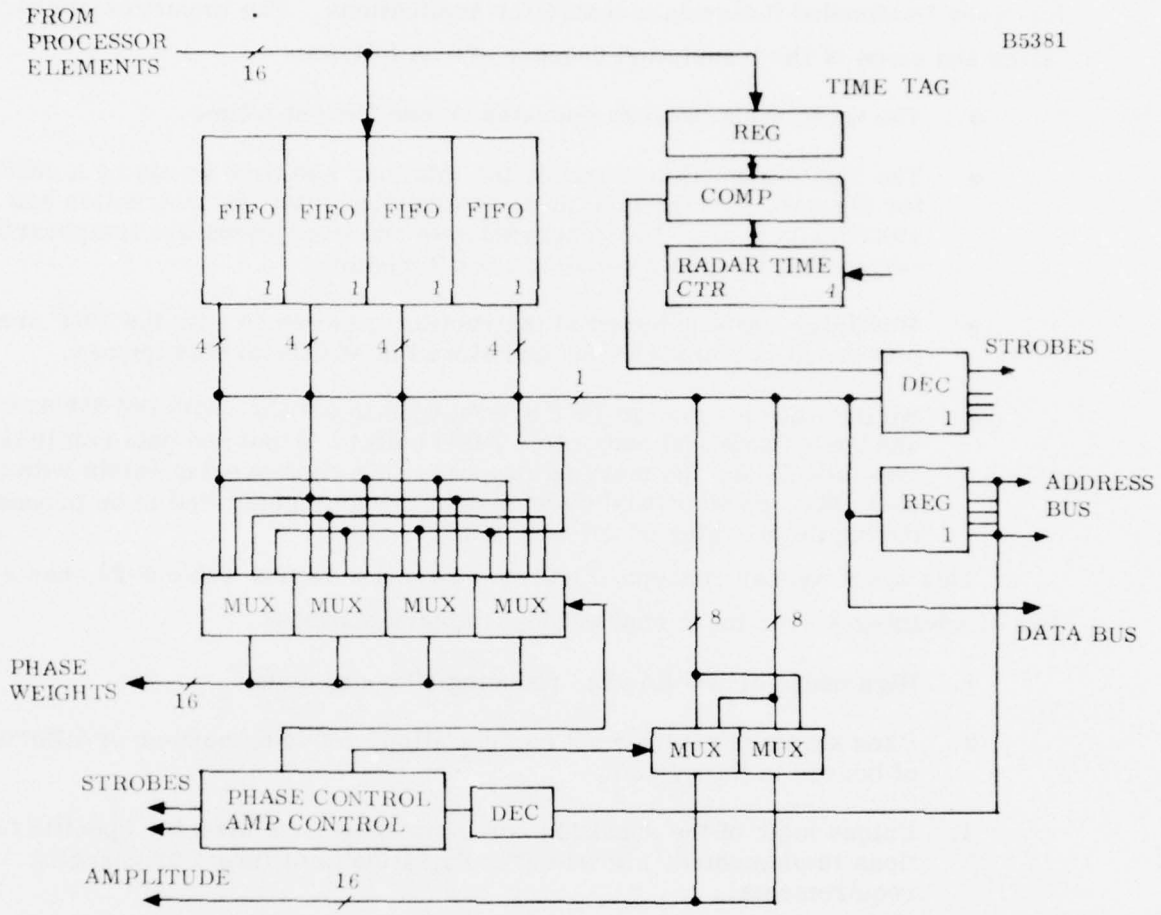


Figure 5-25. Synchronizer Output Logic

TABLE 5-23. PARTS LIST FOR RADAR SYNCHRONIZER

IC's	Type	Function	Width Pins/ Power (mW)
4	4703	FIFO Buffers	0.4-24/50
8	34539	Dual - 4:1 Mux	0.3-16/10
4	F4019	Quad 2:1 Mux	0.3-16/10
5	F4042	Register	0.3-16/10
4	340085	Comparator	0.3-16/10
5	340163	Counter	0.3-16/20
10	Misc	CMOS and LSTTL Control	0.3-16/50
40		Totals	32 in.^{2}/1 W

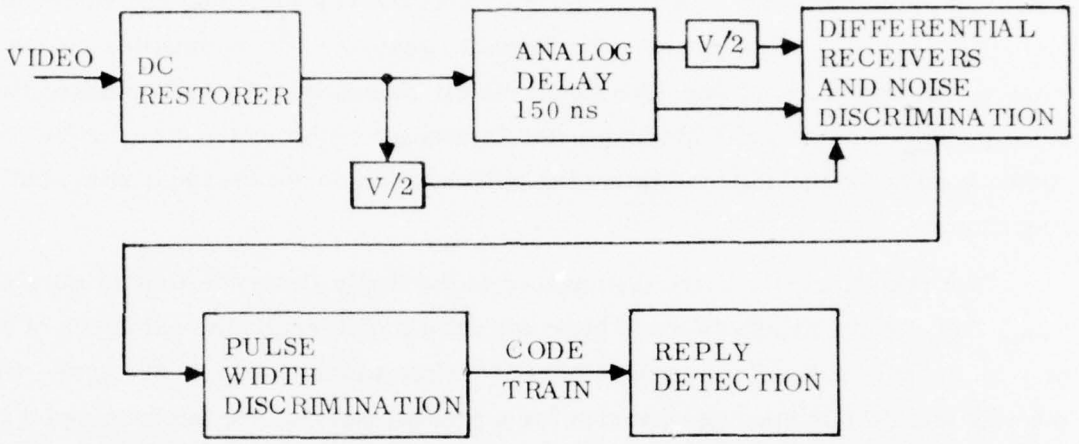
11. IFF DATA CONTROLLER IMPLEMENTATION

The IFF Data Controller hardware provides for conversion of the analog information output from the final receiver into the digital format amenable to the Processing Elements. The final receiver outputs a video pulse to the IFF data controller. A half-amplitude detector (Figure 5-26a) accepts the IFF log video and shapes the leading and trailing edges of the video signal to generate T^2L compatible pulses. This pulse output is generated when the signal amplitude exceeds the 50% points of the input video pulse. A pulse width discriminator in cascade with the detector further reduces spurious noise triggering by eliminating pulses which do not exceed a minimum width requirement.

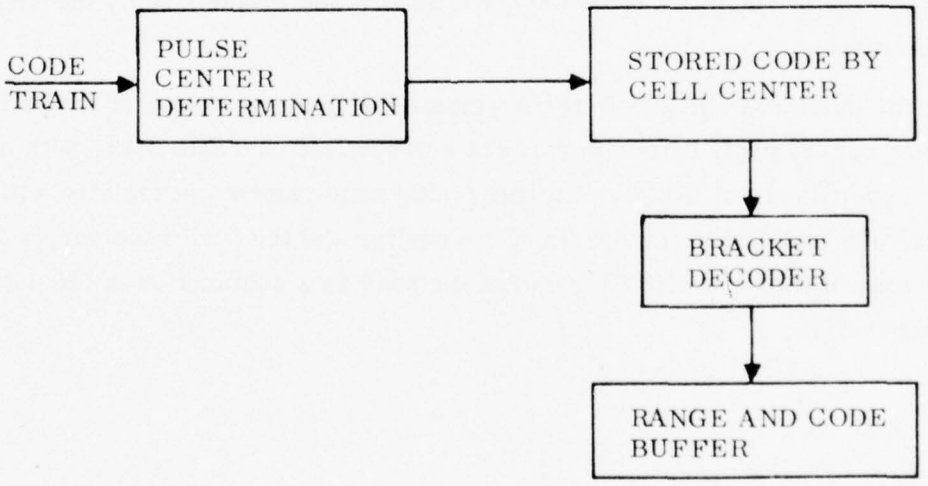
The resulting pulses are then passed to the Reply Detection Unit (Figure 5-26b) which includes the bracket decode logic required to determine the existence of bracket or framing pulses (i.e., two pulses of appropriate width spaced by 20.3 μs). Upon meeting the 20.3 μs spacing criterion for a bracket decode, the intervening bit code (maximum of 13 bits) is outputted to a buffer as a target detection. Range is determined from a range counter output at the time that the bracket decode occurs. All bracket decodes, together with the intervening bit codes and the range count, are output to a buffer memory for subsequent access and processing by the data processor elements.

The parts list and power requirements for implementation of the half-amplitude detector and the reply detection unit are summarized in Table 5-24, with a total power requirement of 6.8 W. The remaining requirements associated with the IFF process are included in the design of the exciter and the final receiver, with the data processing of the digitized IFF returns included as a subfunction of the data processing subsystem.

B5368



a. 1/2 AMPLITUDE DETECTOR



b. REPLY DETECTION UNIT

Figure 5-26. IFF Data Controller

TABLE 5-24. IFF DATA CONTROLLER COMPONENT SUMMARY

Parts List for Reply Detection Unit

			Width-Pins/ Power (mW)
20	74LS164	Shift Register	0.3-16/108
16	74LS163	4 Bit Counters	0.3-16/128
4	74LS73	Flip Flops	0.3-16/20
10	74LS	Misc Control	0.3-16/70
		Total Board Space/Power	35.5 $in.^2$/5.0 W

Parts List for One-Half Amplifier Detector

			Width-Pins/ Power (mW)
2		Differential Receivers	0.3-16/100
3	74LS164	Shift Register	0.3-16/108
3		Analog Delay Line	0.3-16/100
12		Misc Control	0.3-16/100
		Total Board Space/Power	15 $in.^2$/1.8 W

SECTION VI

RELIABILITY AND MAINTAINABILITY

1. OBJECTIVES

The prime objectives for the Reliability/Maintainability (R/M) Program during this study were as follows:

- Evaluate proposed designs for compliance to R/M requirements
- Propose system reconfiguration (when required) to meet R/M requirements
- Optimize designs based on various R/M approaches to minimize cost, power consumption and equipment complexity
- Provide R/M base data for Life Cycle Cost (LCC) models
- Evaluate each proposed system design for potential graceful degradation

Various subsystem configurations analyzed during this study period for the 2-D Unattended Radar are shown in Table 6-1.

The emphasis in this report will deal mostly with discussion pertinent to the aligned (i.e., aligned Doppler filters) processing system approach since this approach was selected. However, note that a negligible difference exists in R/M performance for the unaligned vs aligned signal processor or data processor. For example, an addition of only two multiwire boards are required for the data processor using an unaligned processing approach.

It also became evident in the early study phases that using microprocessors for the signal processor design was not advisable. Component complexity required for the base signal processor was quite excessive compared to the other two approaches. Considering the extensive power consumption required, as well as the inherent unreliability of this design approach, no further investigation was conducted at that time. Any design for the 2-D system can be configured using any of the suggested approaches shown in Table 6-1.

TABLE 6-1. ANALYZED SYSTEM CONFIGURATIONS FOR 2-D RADAR

Subsystem	Design Equipment Configuration	Equipment Configurations for Higher Reliability
Array	Delay Bit Steered	Higher Reliability Components
	Matrix Switched	Higher Reliability Components
	Tapered Delay Steered	Higher Reliability Components
IF/IFF Receiver	One Only	Duplex-Redundancy High Reliability Components
Waveform/Generator Exciter	One Only	Duplex-Redundancy High Reliability Components
Signal Processor	Charge Coupled Devices Analog Processor (Unaligned/Aligned)	Duplex-Redundancy High Reliability Components
	CMOS Digital Processor (Unaligned/Aligned)	Duplex-Redundancy High Reliability Components
Data Processor	Microprocessor (Unaligned/Aligned)	Duplex-Redundancy High Reliability Components
Power Supply	One Only	Duplex Redundancy

The array configurations are similar in reliability design. Therefore, very little difference exists in their reliability impact on the system. The majority of the design is influenced by their inherent redundancy (allowable graceful degradation) due to multiple parallel paths. The impact on subsystem reliability due to the component quality levels selected for the design was considered for all subsystems.

The requirements set forth by the statement of work are shown in Table 6-2. The analyses made during this study have shown that these requirements are realizable for the FY 1980 time frame.

TABLE 6-2. R/M SUMMARY REQUIREMENTS

	2-D	3-D
Reliability	Note 1	Note 2
MTTR (h)	0.5	0.5
M_{max} (ct) at 90th Percentile (h)	1.5	1.5
Availability, Operational	Note 1	As Determined by Reliability, MTTR, and PM (Growth Potential) (Note 2)
Availability, Inherent	As Determined by Reliability, MTTR, and PM	
Preventive Maintenance (PM)	3 h at 90 Day Visit Intervals	3 h/60 Day Visit Intervals

Note 1: The Type A radar design and associated investment cost curves will be made for operating the radar without intervening maintenance for periods of 3-, 6-, and 12-month intervals with allowable graceful degradation which maintains the detection and tracking performance specified in par. 4.4 (of the work statement) with a 0.9 confidence.

Note 2: The Type B radar design and associated cost curves will be made for operating the radar without intervening maintenance for periods of 0.5-, 1-, and 3-month intervals with allowable graceful degradation which maintains the detection and tracking performance specified in par. 4.4 (of the work statement) with a 0.9 confidence.

The 2-D Unattended Radars are capable of meeting these requirements due to their unique design features which include:

- Design for modularity
- Inherent as well as added redundancy design
- Design for graceful degradation assuming 2-dB allowable sensitivity performance margin
- No technology limitation for the FY 1980 time frame
- Self-testing with automatic switchover of redundant elements/equipments
- Local as well as remote performance monitoring

Figure 6-1 shows an overall reliability block diagram for a 2-D Unattended Radar using a CMOS digital signal processor, delay-bit steered cylindrical array and full redundancy. The components selected are representative of high reliability devices such as would be expected to be procured to Mil-M-38510 Class A (Integrated Circuits), JAN TXV (Transistors, Diodes) quality. The corresponding curve of probability of successful operation as a function of time is shown in Figure 6-2 with a three-month preventive maintenance cycle assumed. Also shown is the same system using JAN TX transistors and diodes and Class B2 integrated circuits to illustrate the reliability advantage provided by the higher reliability components.

Each subsystem represented by a block (e.g., array, receiver, etc.) illustrates the reliability for that subsystem after a three-month period without any intervening maintenance. However, at the end of the three-month period, a maintenance team would be sent to the site to replace any failed equipment. Each block also indicates the subsystem mean-time-to-repair (MTTR), and the maximum repair time anticipated for 90% of all failures. The low $MTTR/M_{max}$ (ct) values are representative of fault location to one board, 90% of the time, and the modularity concept of the equipment.

Further discussions regarding

- System reliability block diagrams
- System reliability model
- Component failure rates
- Maintenance concept
- Maintenance design

are provided below.

2. RELIABILITY ANALYSIS

a. GENERAL

The reliability of any system has a direct impact on the cost of spares to the system over its useful life. This paragraph treats the reliability impact of quality level of components. Improving the reliability of a systems building block (i.e., using better military components vs commercial parts, etc.) must be balanced with the resultant acquisition and spares cost impact. For an unattended maintenance concept, a radar's reliability has a major cost impact as shown in the life cycle cost trade studies, on maintaining a system.

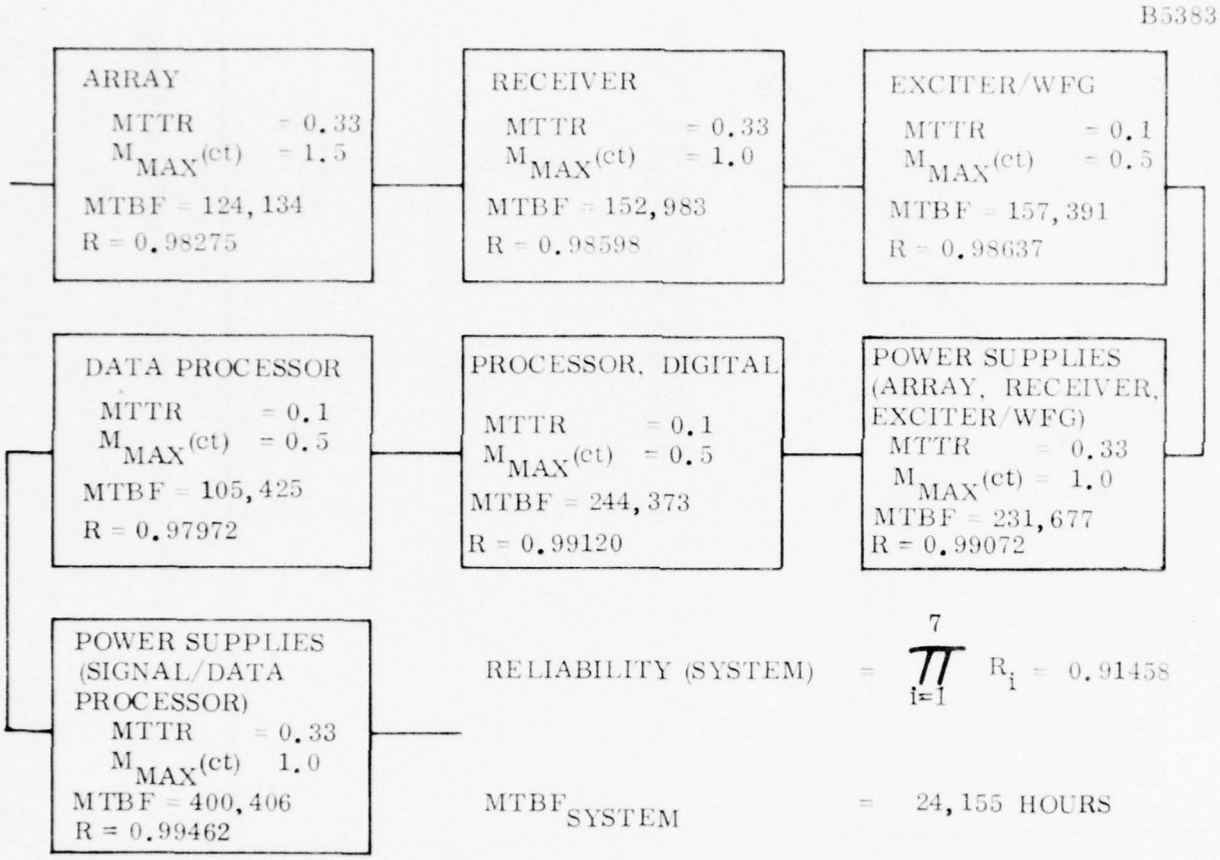


Figure 6-1. Overall 2-D Radar Reliability Block Diagram

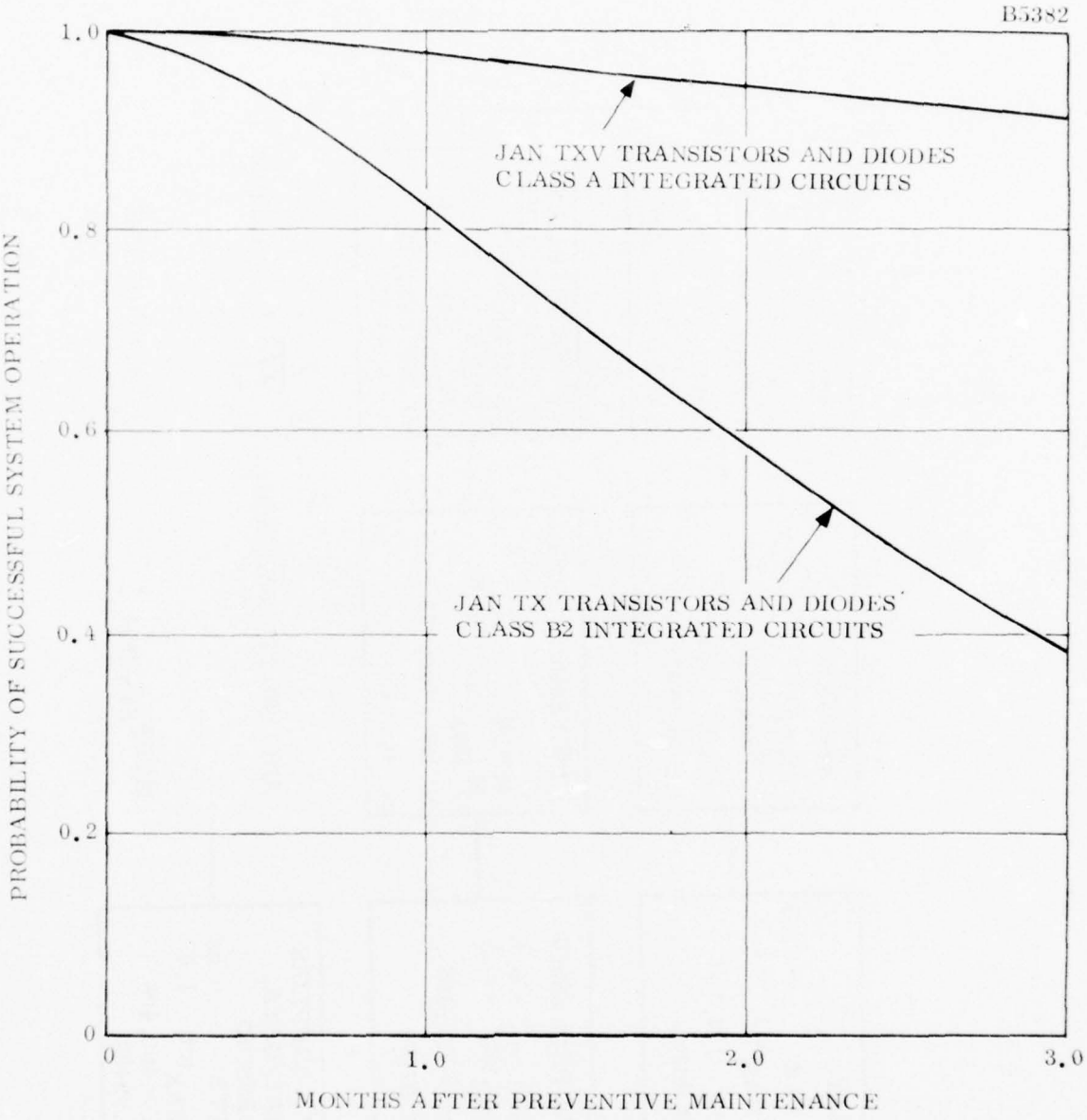


Figure 6-2. Probability of Successful System Operation

The radar type encountered in this study report is an all solid-state radar. There are no rotating and/or moving parts treated in the designs analyzed herein. Unlike a mechanically rotating or tube-type radar, the all solid-state design is not prone to a wearout phenomena within the designed life of the radar. Although the basic elements of a solid-state transmitter are reliable and many can fail without degrading the system to a predetermined and acceptable level, the failed elements must be replaced at some time to minimize the probability of a system failure. Unlike a conventional radar, a solid-state transmitter does not fail in a catastrophic sense. Rather, based on specified system performance parameters, one determines when a system fails to perform to design limits. The designs described in this report allow 2-dB degradation to system sensitivity.

Table 6-3 shows the following:

- Subsystem Reliability (i.e., probability of successful system operation at the end of the specified period) for maintenance intervals of one, two, and three months
- Subsystem reliability for differing quality level devices
- System reliability for CMOS (Digital) and CCD (Analog) processor vs the two steps above

The conclusion to be drawn is that either the CMOS digital or CCD signal processor will provide a probability of successful system operation in excess of 0.9 if high reliability devices are incorporated in a functionally fail-safe system architecture. This level of reliability can be achieved for up to three months between preventive maintenance intervals as shown in Table 6-3.

b. RELIABILITY BLOCK DIAGRAMS

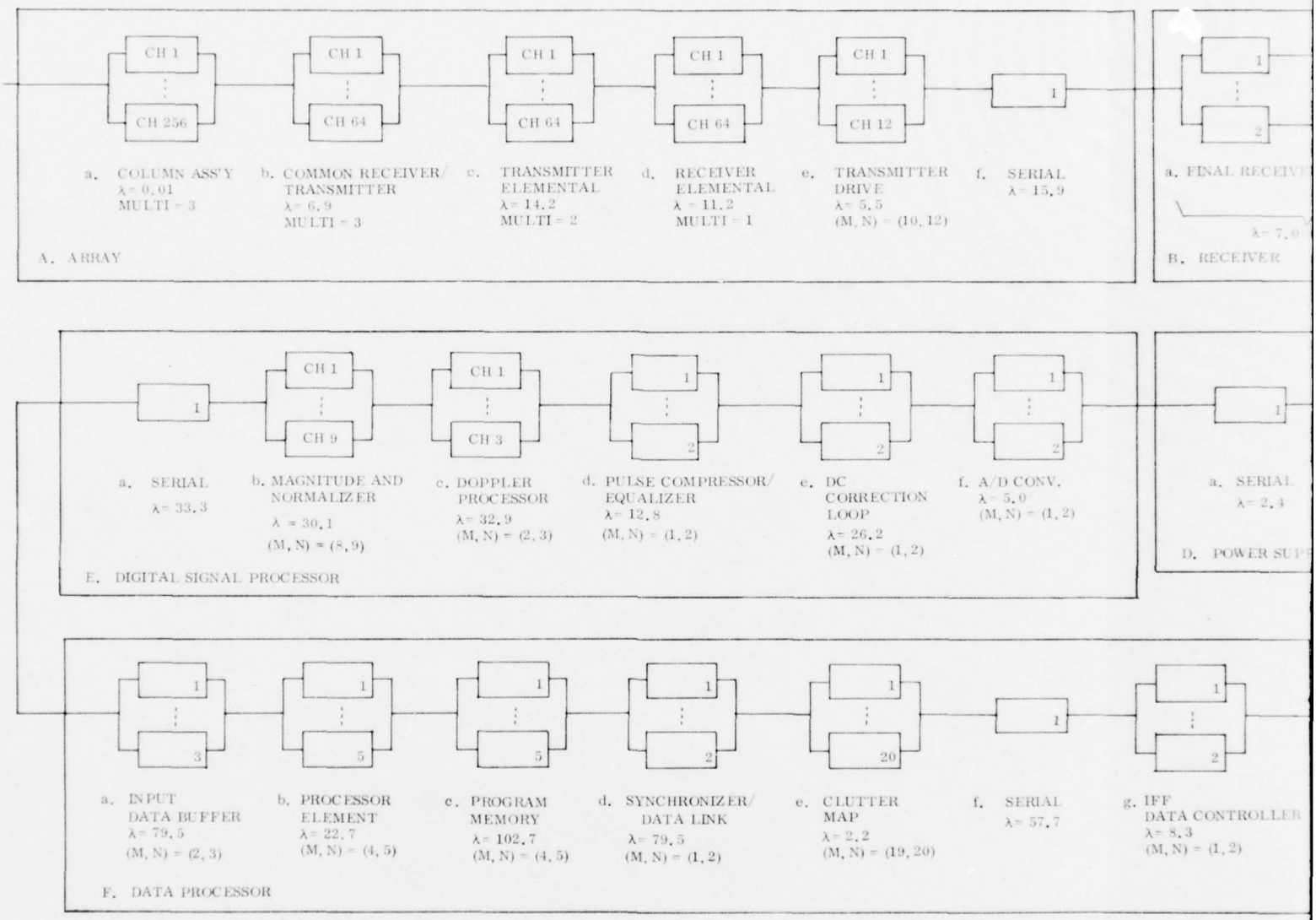
The reliability block diagrams shown in Figures 6-3 and 6-4 represent a baseline configuration analyzed for this study. Figure 6-3 represents the complete system using a digital processor (CMOS devices) and a delay bit steered cylindrical configuration. Figure 6-4 is a reliability block diagram of the CCD analog processor. This block diagram replaces block E of Figure 6-3 when applicable.

TABLE 6-3. SUBSYSTEM RELIABILITY FOR ALIGNED MODELS VS PM FREQUENCY

Configurations		Subsystems Reliability								System Reliability	
Note	Months Between PM	A Array	B Receiver	C Exciter/ WFG	D Power Supplies	E CMOS Signal Processor	F CCD Signal Processor	G Data Processor	H SP/DP PS	CMOS Digital Processor	CCD Analog Processor
1	1	0.98860	0.99072	0.99221	0.99778	0.95971	0.92530	0.88813	0.99825	0.82502	0.79540
	2	0.97717	0.98146	0.97966	0.99468	0.89536	0.79160	0.70827	0.99645	0.59055	0.52211
	3	0.96493	0.97222	0.96318	0.99072	0.81737	0.64310	0.52760	0.99462	0.38397	0.30210
2	1	0.98860	0.99072	0.99221	0.99780	0.99742	0.99699	0.99491	0.99825	0.96055	0.96014
	2	0.97717	0.98146	0.97966	0.99468	0.99448	0.99278	0.98810	0.99646	0.91508	0.91351
	3	0.96493	0.97222	0.96318	0.99072	0.99120	0.98746	0.97972	0.99462	0.86465	0.86139
3	1	0.99425	0.99530	0.99672	0.99780	0.99742	0.99699	0.99491	0.99825	0.97529	0.97455
	2	0.98854	0.99054	0.99214	0.99468	0.99448	0.99278	0.98810	0.99646	0.94617	0.94456
	3	0.98150	0.98576	0.98637	0.99072	0.99120	0.98746	0.97972	0.99462	0.91320	0.90977
4	1	0.99425	0.99532	0.99672	0.99780	0.99742	0.99697	0.99491	0.99825	0.97531	0.97457
	2	0.98853	0.99065	0.99214	0.99468	0.99448	0.99278	0.98810	0.99646	0.94627	0.94668
	3	0.98276	0.98598	0.98637	0.99072	0.99120	0.98746	0.97972	0.99462	0.91458	0.91113

Note: Four system reliability levels are evaluated for differing component reliability levels.

1. JAN TX Trans stors, diodes; MIL-M-38510 Class B-2 IC
2. MIL-M-38510 Class A IC's for Subsystems E, F, and G
3. JAN TX V Transistors, diodes for only Subsystem serial equipments
4. JAN TX V Transistors, diodes for redundant as well as serial equipments in the array and analog portions of the system


CH 1
CH 256
CH 64
CH 12
1
2
a. COLUMN ASS'Y
λ = 0.01
MULTI = 3
b. COMMON RECEIVER/ TRANSMITTER
λ = 6.9
MULTI = 3
c. TRANSMITTER ELEMENTAL
λ = 14.2
MULTI = 2
d. RECEIVER ELEMENTAL
λ = 11.2
MULTI = 1
e. TRANSMITTER DRIVE
λ = 5.5
(M, N) = (10, 12)
f. SERIAL
λ = 15.9
A. ARRAY
a. FINAL RECEIVE
λ = 7.0
B. RECEIVER

1
CH 1
CH 9
CH 3
2
a. SERIAL
λ = 33.3
b. MAGNITUDE AND NORMALIZER
λ = 30.1
(M, N) = (8, 9)
c. DOPPLER PROCESSOR
λ = 32.9
(M, N) = (2, 3)
d. PULSE COMPRESSOR/ EQUALIZER
λ = 12.8
(M, N) = (1, 2)
e. DC CORRECTION LOOP
λ = 26.2
(M, N) = (1, 2)
f. A/D CONV.
λ = 5.0
(M, N) = (1, 2)
E. DIGITAL SIGNAL PROCESSOR
a. SERIAL
λ = 2.4
D. POWER SUP

1
3
5
20
2
a. INPUT DATA BUFFER
λ = 79.5
(M, N) = (2, 3)
b. PROCESSOR ELEMENT
λ = 22.7
(M, N) = (4, 5)
c. PROGRAM MEMORY
λ = 102.7
(M, N) = (4, 5)
d. SYNCHRONIZER/ DATA LINK
λ = 79.5
(M, N) = (1, 2)
e. CLUTTER MAP
λ = 2.2
(M, N) = (19, 20)
f. SERIAL
λ = 57.7
g. IFF DATA CONTROLLER
λ = 8.3
(M, N) = (1, 2)
F. DATA PROCESSOR

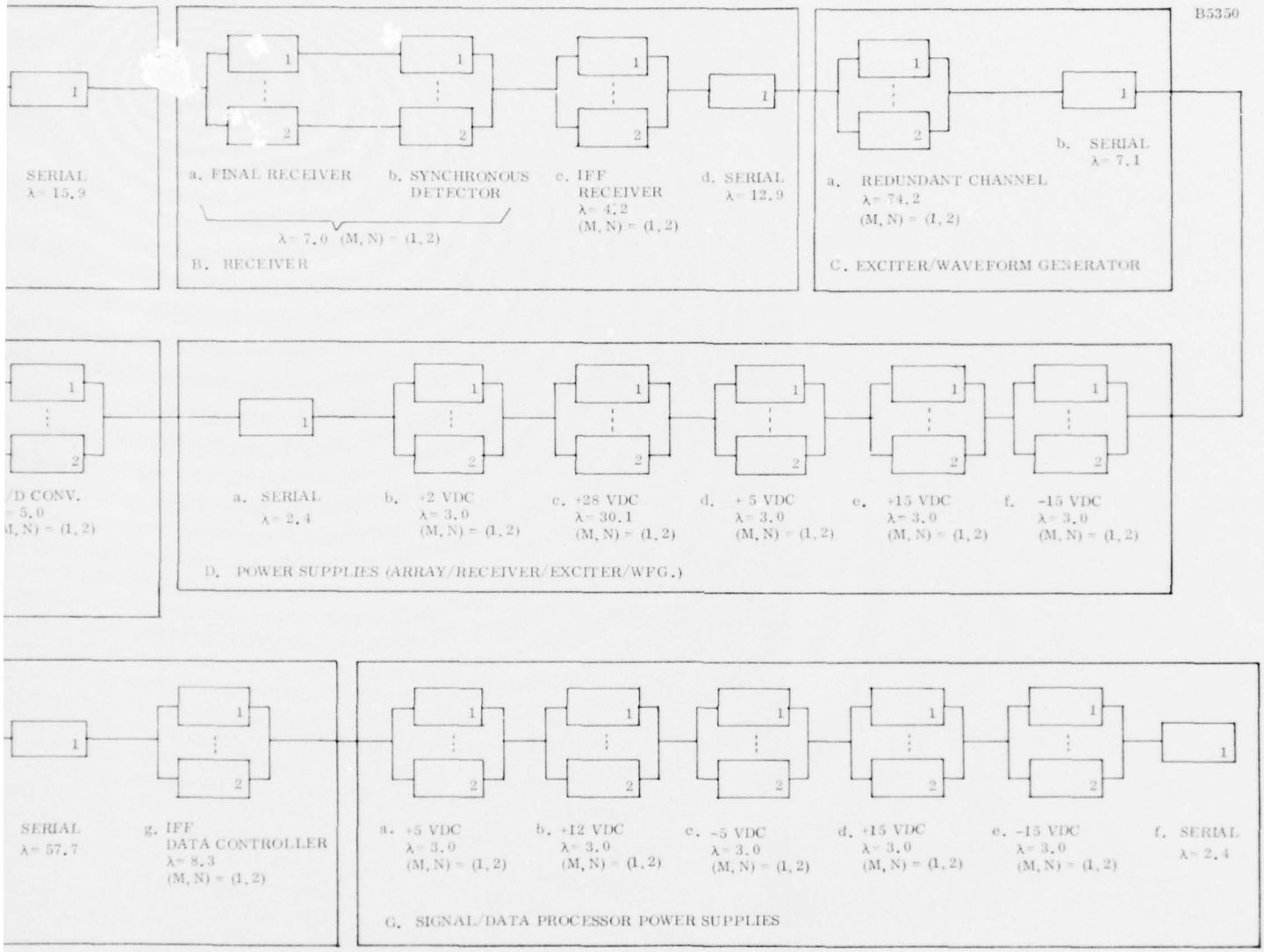
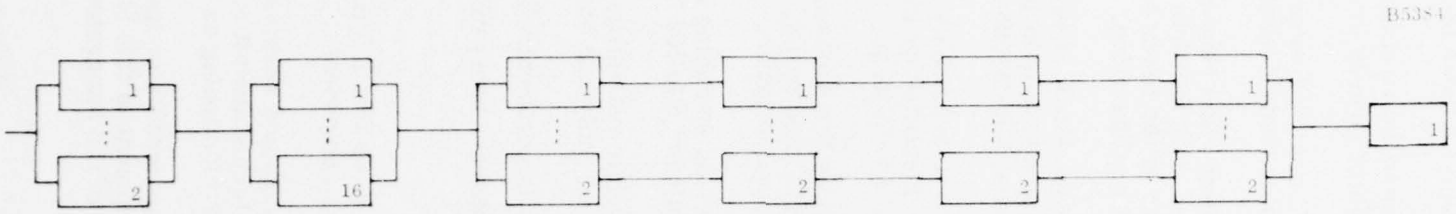


Figure 6-3. Unattended Radar Reliability Block Diagram



a. CCD PULSE COMPRESSOR FILTER
$\lambda = 38.3$
$(M, N) = (1, 2)$

b. DOPPLER PROCESSOR MEMORY
$\lambda = 30.2$
$(M, N) = (15, 16)$

c. CCD DFT-8
$\lambda = 13.2$
$(M, N) = (1, 2)$

d. VIDEO MAGNITUDE DETECTOR
$\lambda = 50.0$
$(M, N) = (1, 2)$

e. NORMALIZER
$\lambda = 42.3$
$(M, N) = (1, 2)$

f. DIGITAL DATA PROCESSOR INTERFACE
$\lambda = 12.6$
$(M, N) = (1, 2)$

g. SERIAL
$\lambda = 32.9$

Figure 6-4. CCD Signal Processor Reliability Block Diagram

General comments that apply to these block diagrams are as follows:

1. Serial equipment, depicted as a single in-line block, represents equipment where a hardware failure results in a system failure.

2. Redundant equipment, depicted as parallel blocks, represents equipment where a hardware failure only degrades performance.

3. The number in the lower right hand corner of each block represents that item's quantity usage. For multiple redundant units, the number in the lower right corner of the lower two blocks, represents the total quantity used for that configuration.

4. The failure rate for each block identified is listed right below the block (e.g., $\lambda = 1.0$). Failure rate is in failures per million hours. The failure rates depicted represent Mil-M-38510 Class B-2 and JAN TX components.

5. Redundancy applicable to sensitivity degradation (2 dB) for a particular equipment function is identified by its weighting factor directly below the blocks indicated failure rate (e.g., multi = 3).

6. Redundancy which allows for successful operation based on M out of N operational units is indicated by (M, N) = (1, 2) below the failure rate indicated for that equipment group.

7. Performance monitor and switching circuits necessary to implement switching of a good unit for a failed unit is included in the serial equipment.

8. Since there is a negligible reliability difference for each of the three array configurations analyzed, only one block diagram is used.

The following information is pertinent when describing individual subsystems shown in the reliability block diagram subsystems.

1. Block A - Array

   Sub-block a. The 5 ft x 2 ft x 1.5 in. column feed assemblies are basically passive components.

   Sub-block b. When common receiver/transmitter equipments fail, they affect both transmit and receive function. A common circulator functioning as a T/R switch falls into this category.

   Sub-block c. A power module or its associated driver is representative of equipment in this block. The power module/driver form a part of the integrated transceiver module.

Sub-block d. Low-noise receiver amplifier is representative of the equipment in this block. The receiver is also packaged within the integrated receiver.

Sub-block e. Drive power for the 64 elemental transmitter comes from a power pack. The power pack is made up of a predriver driving 12 power modules whose power is combined for an approximate 74 W of power output. Sufficient power to drive the 64 power modules is supplied by only 10 power pack modules.

2. Block B - Receiver

No attempt was made to optimize the receiver for redundancy other than duplexing the entire function after the first stages of amplification. Further improvement could be achieved with the added redundancy to this front end whose serial failure rate contribution is included with the receiver serial equipment. Note, that the failure rate for a single channel is only 11.2 failures/10^6 hours for the redundant portion. For the 3-month maintenance intervals, making this equipment serial would only reduce the system reliability from 0.91458 to 0.90355, for Configuration 3 system approach.

3. Block C - Exciter/Waveform Generator

Due to its relatively high failure rate the exciter/waveform generator equipment has been completely duplexed, where possible.

4. Block D - Power Supplies

The power supplies are designed to be bussed into a common bus, thus eliminating any switchover in case of failure. This technique to bus power supplies has been successfully demonstrated on General Electric's System Technology Radar (formerly designated as Site Defense Radar) presently at Kwajalein Island.

5. Block E - Digital Signal Processor

Sub-block b. The magnitude and normalizer function has had a ninth channel added for redundancy. This approach minimizes power consumption, acquisition, and spares cost. The performance monitor capability monitors the output of each eight channels, and initiates switchover to the ninth in case of failure.

Sub-block c. Rather than implement a totally duplexed Doppler processor, one Doppler channel with switching and monitoring capability is used.

Remaining elements of the digital signal processor have been duplexed to meet reliability requirements.

Figure 6-4 is the reliability block diagram representation for the CCD signal processor. The Doppler processor memory Block b representing 16 channels is configured into 2 groups of 8 channels. Due to logic speed constraints alternate frequencies are processed. For instance, frequencies F_1 and F_3 are processed in the first group. The resultant effect of a channel loss will be negligible to overall system performance. It was necessary to duplex the remaining equipment to achieve the specified reliability requirements.

6. Block F - Data processor

Sub-block a. Redundancy is implemented with the addition of one multiwire board containing four input data buffer channels.

Sub-blocks b./c. Associated with each program memory is a processor element. An additional program memory/processor element has been added to implement four/fifth redundancy.

Sub-block d. The clutter map is basically a CCD memory storage channel. Only 19 of these channels are required for complete performance. The remaining equipments, as shown, are duplexed.

7. Block G - Signal/Data Processor Power Supplies

These power supplies, as described above for Block d. are bussed together for redundancy. Clearly, reduced power supplies quantities will be required if all power supplies are packaged such that associated subsystems requiring common voltages can be furnished from one supply.

c. RELIABILITY MODEL

A computer program developed by General Electric was used to compute the system Mean Time Between Failure (MTBF) from the data in the reliability block diagram in the previous section. The program calculates system MTBF taking into account redundancy and allowable degraded operation.

The reliability analysis assumes that failure rate follows the exponential distribution

$$R(t) = e^{-\lambda t} \tag{6-1}$$

where

$R(t)$ = Probability of success (i.e., the probability that 0 failures occur in time t)

λ = Constant failure rate

The MTBF of a given unit with the probability of success or reliability of $R(t)$ is given by integrating over all time

$$\text{MTBF} = \int_0^\infty R(t)\, dt \tag{6-2}$$

The model depicting the interrelationships shown by the reliability block diagram is illustrated by

$$\text{MTBF}_{\text{System}} = \int_0^T R(t)_1\, dt + \int_0^\infty R(t)_2\, dt \tag{6-3}$$

where

$R(t)_1$ = The probability that 0 failures will occur in the redundant portion of the system.

T = The Preventive Maintenance Schedule

$R(t)_2$ = The probability that 0 failures occur within the serial components of the system

$\text{MTBF}_{\text{Steady-State}}$ = The equivalent MTBF of redundant equipment which can be repaired on-line.

The second term of Equation (6-3) is handled by the addition of all those designated serial failure rate units in the system. The mathematics for redundant elements of the model are handled somewhat differently. A discussion of the redundant related electronics follows.

The electronics equipments for the 2-D Radar are of two types:

1. Those subsystems which have system degradation associated with them (degradable subsystems).

2. Those subsystems which have a specified minimum number of elements which must be operable for that subsystem to be operable (M-out of N-subsystems).

The following characteristics of the degradable subsystem are needed as program inputs:

1. The number, N_i, of parallel elements making up subsystem i (all elements assumed identical).

2. The failure rate of an element (assumed to be equal for all parallel elements) in subsystem i (λ_i, given in failures per 10^6 h).

3. The dB multiplier for that subsystem ($MULT_i$), an integer used to account for the fact that elements of various subsystems affect the degradation of the SNR of the system differently.

SNR can be expressed as:

$$SNR = K P_T G_T G_R \qquad (6\text{-}4)$$

where

K is a constant including all other variables in the radar equation

P_T is the average transmitted power

G_T and G_R are the transmit and receive gains, respectively.

The degradation in SNR is expressed as the dB loss per element of the subsystem ($10 \log \frac{N-1}{N}$) scaled by a multiplier of 1, 2, or 3 to indicate which combination of P_T, G_T, and G_R are affected.

The following characteristics of an M out of N type subsystem are needed:

1. N, the total number of elements
2. λ assumed to be equal for each of the parallel elements in the subsystem
3. The minimum number of elements, M, which must be operating out of the total number of elements, N, for the subsystem to be considered operative.

The reliability of this M out of N subsystem can be found exactly by examining the binomial expansion of the function.

$$f(t) = [p(t) + q(t)]^N \tag{6-5}$$

where

p(t) is the probability that one element has not failed in the time interval (0, t) and is given by

$$p(t) = e^{-\lambda t} \tag{6-6}$$

q(t) is the probability that one element has failed in the interval (0, t) and is given by:

$$q(t) = 1 - p(t) = 1 - e^{-\lambda t} \tag{6-7}$$

Expending Equation (6-5) (and dropping the independent variable t, for convenience) yields:

$$f(t) = p^N + Np^{N-1}q + \frac{N(N-1)}{2} p^{N-2} q^2 + \cdots + Npq^{N-1} + q^N \tag{6-8}$$

where the (r + 1) term is given by

$$\frac{N!}{r!\,(N-r)!} p^{N-r} q^r$$

The terms in the above expressions can be interpreted as follows:

1. The first term represents the probability that all elements are operative (no failures have occurred).

2. The second term represents the probability that all elements but one are still operative.

3. The (r + 1) term represents the probability that (N-r) elements are operative while r elements have failed.

The computer program assesses the reliability and MTBF of the system as a function of how often replacement to the failed distributed electronics takes place. This replacement takes place during scheduled preventive maintenance.

When preventive maintenance allows for replacement of failed redundant equipment on the array before the allowable 2-dB degradation in performance occurs, then the probability of a system outage at time, t, is minimized. This reduction of the probability for a system failure is dependent on how often the system is scheduled for preventive maintenance. The MTBF for the radar increases as the frequency of preventive maintenance increases.

d. COMPONENT FAILURE RATES

For the most part, predictions were performed using techniques and data primarily from Mil-Std-756A and Mil-HDBK-217B (Reliability Prediction of Electronic Equipment) Notice 1 dated 1 September 1976. Failure rates from Mil-Hdbk-217B were derived by using techniques cited by par. 3.0, "Parts Count Reliability Prediction". Table 6-4 is a summary of the environmental/quality factors used for predicting failure rates.

During this study an investigation was made as to the reliability (failure rates) for representative semiconductor used during the AN/TPS-59 (Marine Corp radar presently being field tested) development and acceptance test phases.

Table 6-5 is a summary of general classes of semiconductor data derived from these tests and representative failure rates used for this study report.

TABLE 6-4. REPRESENTATIVE COMPONENT ENVIRONMENTAL/ QUALITY FACTORS

Representative Component	Environment	Quality Level (π_Q)	Stress Level (S)	Ambient Temp
Semiconductors				
JAN TX	GF	0.6		
JAN TX V	GF	0.3		
IC's			50%	50°C
Class B-2	GB	5		
Class A	GB	0.5		
Established Reliability				
Components*				
Base	GF	1.0		
High Reliability	GF	0.5		

*For capacitors and resistors

TABLE 6-5. AN/TPS-59 RELIABILITY* FAILURE RATE DATA

Component Type IC's	Failure Rates (Failure/10^6 h) AN/TPS-59*	Study Report**
Analog		
Operational Amplifier	0.53	
Linear	1.23	
Digital		
LSI (Bipolar)	0.55	1.6
MSI (Bipolar)	0.44	0.4
SSI (Bipolar)		0.1
MOS (LSI)	0.72	1.8
CCD		2.2

*Representative failure rates based on point estimates. Data for AN/TPS-59 over 1.5 yrs of testing during which all extremes of environmental conditions existed.

**MIL-STD-217B.

3. MAINTAINABILITY ANALYSIS

a. MAINTENANCE CONCEPT

The 2-D Unattended Radar site will be operated continuously, at a utilization of 8,760 h/yr, except for downtime to perform preventive maintenance or downtime to make repairs due to system outage. One depot (central control site) is assigned to support 15 surveillance radars as directed. Sensitivity to this guideline is examined in the operation and maintenance cost discussions below.* This depot will contain all the software/computer capability to sustain operation of its assigned radars. Digital outputs from each radar will be transmitted to its respective depot where the data will be handled on a time-share basis. This data, in addition to target information data, will contain radar performance data. The radar is, therefore, designed with provisions for on-line and continuous performance monitoring.

In the event of a system failure or system degradation, further data reduction of transmitted data obtained from the performance monitoring tests will provide the capability to isolate failures to a major element or subfunction of the radar.

The operating and maintenance center at the depot will be continuously manned by an operations director who will monitor the operation of the unmanned radars by a maintenance control panel and/or hardcopy printout from a central computer. In the event of a fault indication at a radar site, he will identify the fault location to a specific function of the radar, such as the transmitter, etc. He will then dispatch a maintenance crew to the affected radar site.

The depot will contain a 100% complement of spares for the unmanned sites under its control. The maintenance crew will select the complement of spares required to repair the faulted function. In addition, all tools and test equipment required to make the repair will be carried by the maintenance crew. Repair at each site shall consist of the removal and replacement of a failed unit. The failed printed circuit boards (PCB's) and/or modules will be returned to the depot for repair or disposition. The depots shall have the capability to test and repair all failed PCB's or modules from the unmanned sites.

*Previous effort (e.g., Unattended Radar Study Contract performed by GE for the USAF Electronics Systems Division in 1974) have addressed the relative economy of various depot-to-radar ratio.

b. MAINTENANCE FEATURES

The 2-D Radar is easily maintained by two technicians. A Skill Level 5 (USAF definition) is capable of the remove/replace philosophy advocated for this radar.

The technicians perform the following tasks:

- Observation of the built-in performance monitoring status display panel
- Corrective maintenance
- Routine scheduled maintenance
- Depot repair of faulty subassemblies to the component level

The two aspects of the 2-D Radar design most responsible for the minimal maintenance requirements are gradual degradation through inherent and added redancy permitting maintenance to be deferred and automatic data-processor-controlled performance assessment and fault detection/location procedures.

Some of the built-in features of the radar hardware design which contributed to short repair times, safe maintenance actions, reduced manpower requirements, minimal requirements for special test instruments, and low operational costs over the life of the system are:

- A maintenance console which presents comprehensive status information.
- Circuit cards in the processing equipment replaceable without disturbing system operation.
- Modular, lightweight replaceable subassemblies, easily handled by one man. The largest/heaviest being the column feed assemblies (5 ft x 2 ft x 1.5 in.) weighing 30 lbs.
- Replaceable subassemblies of the same type, mechanically and electrically interchangeable.
- All replaceable subassemblies mounted with captive hardware.
- Replaceable cards keyed to prevent the accidental introduction of a wrong card.
- Replaceable cards/subassemblies having accessible test points and adjustment controls where required.
- Special tools and test equipments minimized through incorporation of standard hardware.

- Special board tester at the site used to verify faulty boards.
- Swingout racks and pull-out drawers to provide accessibility to replaceable subassemblies.
- Need for scheduled depot repairs eliminated.

Reconfiguration by the on-line performance monitor provides a significant increment to system performance. Reconfiguration is performed in order to compensate for a particular fault. For example, if one of the two waveform generators fails, the good waveform generator is switched to the on-line position.

By injecting test signals into the element receivers and sampling the elemental transmitter outputs, the data processor can continuously monitor the array for performance degradation.

c. FAULT LOCATION

A review has been made of techniques applicable to PM/FL testing. Fault location for the 2-D Radar is expected to be an off-line process which will test hardware in a sequential manner, locating faults to a replaceable equipment level. The 2-D Radar fault location procedure will be capable of isolating a fault directly to the equipment level that is spared and replaced by the technician. Examples are:

Digital signal processor	1 board
Data processor	2 boards
Waveform generator/exciter	1 board
Receiver	2 boards
Array	
Transceiver	1 module
Power pack	1 module

d. EQUIPMENT REPAIR

The easily replaceable, lightweight modules in the 2-D Radar allow maintenance technicians to perform the typical equipment repair in less than the specified 30 minutes. The types and quantities of replaceable modules in the radar are listed by subsystems in Table 6-6. Included are subassemblies, plug-in wiring boards, and other miscellaneous components.

TABLE 6-6. REPLACEABLE UNITS

Subsystem	Nomenclature	Qty	Types(s)
Array/Electronics	Column Feed Assemblies	256	1
	Type 1 Digital Boards	6	6
	Integrated Transceivers	64	1
	Equipment Plates	1	1
Receiver/WFG Exciter	Analog Boards	12	6
	Digital Boards	2	2
	Equipment Plates	2	1
CCD Signal Processor	Large Digital Boards	15	5
CMOS Signal Processor	Large Digital Boards	51	9
Data Processor	Large Digital Boards	18	5
Power Supplies*		20	7

*Total quantity of power supplies could be reduced to fourteen (7 seven for redundancy) depending on final packaging.

The majority of the replaceable items can be handled by one man. The only item that, because of bulk and size, may require two men is the Column Feed assembly (5 ft x 2 ft x 1.5 in. and 30 lbs). All other units weigh from a few ounces to a few pounds. The mechanical replacement of all modules requires little specialized technical skill.

The predominant type of repair on the array involves replacing subassemblies (integrated transceivers). All equipment repairs are made with fully interchangeable subassemblies. All other subassemblies are housed in three cabinets located in the array dome structure.

The equipment area is a 14-ft diameter room. A workbench is supplied within the room, and ample space is provided to test boards. The two processor cabinets house the signal processor, data processor, receiver, associated power supplies, IFF equipment, and microwave communication equipment. The transceiver cabinet houses the array hardware and waveform generator/exciter.

SECTION VII

BUDGETARY 2-D RADAR PROCUREMENT SCHEDULE AND COSTS

1. DEVELOPMENT AND ACQUISITION

Cost estimates were prepared for the development, validation testing and production of eighty 2-D Unattended Radars. A nominal schedule is shown in Figure 7-1. The Engineering Development Contract phase provides for the development, fabrication, and testing of three pre-production units which are used to provide the design confidence prior to production go-ahead. Two of these units are reserved for extensive reliability testing because of the very high reliability demanded by these radars. Testing of two full systems plus selected subsystems and analytical extrapolation of the results, will provide the required level of confidence before committing to a full production run.

The production phase includes the fabrication and testing of a first production article, followed by full production at a rate of four units per month. This represents a reasonable production rate, which could be increased, if desired, because of the relative simplicity of the radar.

In arriving at the budgetary costs associated with this schedule, it was assumed that the following items are to be Government-furnished.

- Transportation
- Helicopter Services
- Tower and Personnel/Storage Shelters
- Site Preparation
- Prime Power

Costs were likewise not included for technical orders, training and instruction books, and spares.

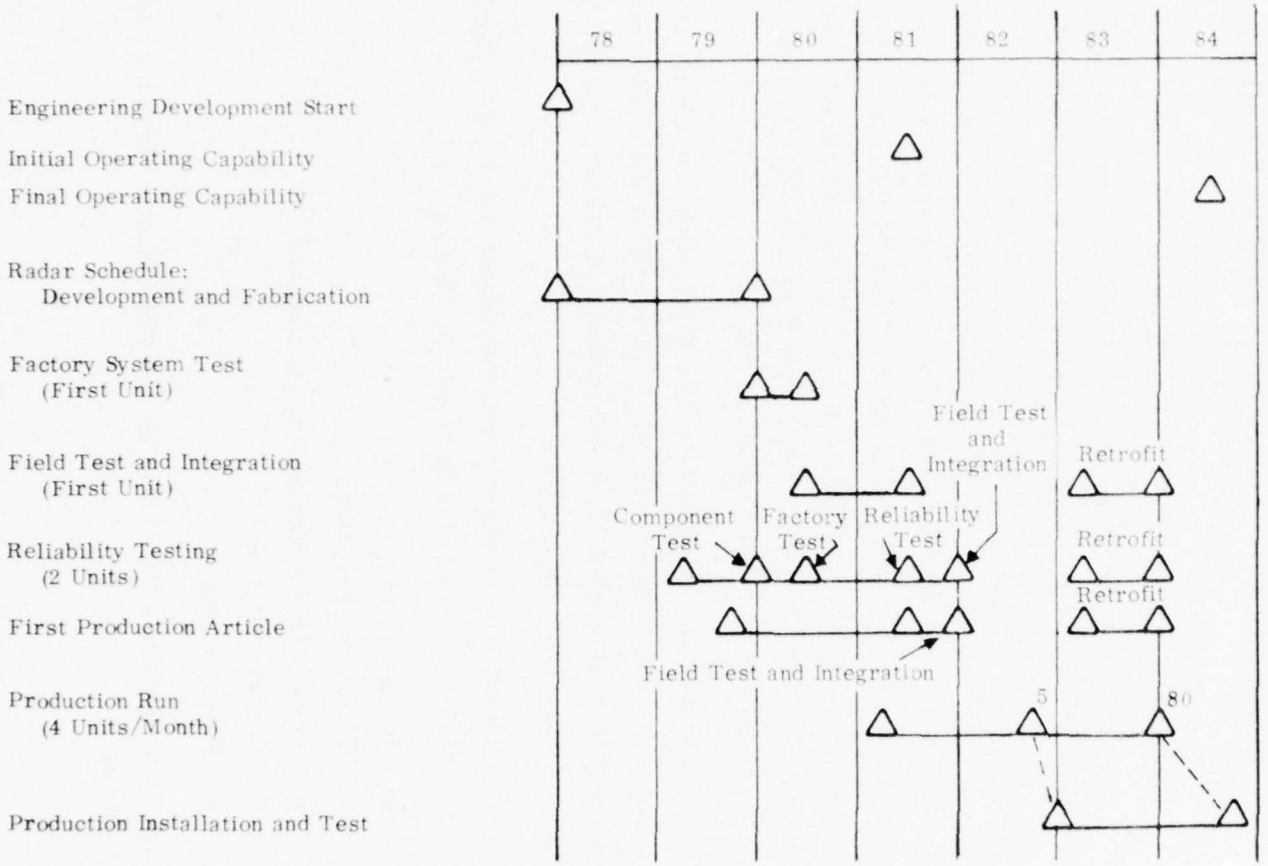


Figure 7-1. 2-D — Development and Acquisition Schedule

2. OPERATIONS AND MAINTENANCE COSTS

a. INTRODUCTION

The life cycle cost of operation and maintenance is a principal factor in the choice between alternative designs for the 2-D Unattended Radar. The candidate configurations discussed herein include two RF and two signal processor designs.

This report includes the following items as Operational and Maintenance (O&M) costs:

- Initial and Replacement Spares
- Material Cost of Repair
- Labor Cost of Repair
- Supply Item Management
- Prime Power Costs
- Test Equipment Cost
- Transportation Costs

The key assumptions made in the course of the analysis are:

- No on-site component repair
- All costs based on 1976 dollars
- All spares are produced during initial system construction or no retooling is required to construct new spares during the system life
- Radar life is 20 yrs with no salvage value

b. COST METHODOLOGY

The 2-D Radar can be broken into 17 main categories to be costed. Thirteen of these categories are common to all designs. The remaining four comprise the differences between the systems.

The component categories are listed in Table 7-1. Associated with each category are the following:

- Failure Rate (failures per 10^6 h) FR_i
- Percentage condemned upon failure $COND_i$

TABLE 7-1. SYSTEM COMPONENT PARAMETERS (2-D)

Category	Quantity Qty_i	No. of Types $NTYP_i$	Failure Rate (Failures Per 10^6 h) FR_i	% Condemn On Fail $COND_i$	On-Site Labor Man-Hours BMH_i	Depot Labor Man-Hours DMH_i	Repair Parts Cost $ RPC_i
Large Digital Boards[1]	71	24	3.81	1	0.1	0.33	60
Large Digital Boards[2]	35	12	6.0	1	0.1	0.33	60
Analog Boards	12	6	1.58	1	0.33	0.33	20
Equipment Plate	2	1	23.49	1	0.33	0.2	120
Low Current Power Supply	18	6	3.0	1	0.33	1.0	20
High Current Power Supply	2	1	30	1	0.33	2.0	400
Receiver Protect/Keyer	1	1	2.29	100	0.33	0	0
Matrix Switch[3]	1	1	4.2	1	0.33	0.5	50
Transceiver Module	32	1	12	100	0.33	0	0
SP4T Switch	32	1	1.7	100	0.33	0	0
Circulator	1	1	0.5	100	0.33	0	0
64 Way Power Divide	1	1	0.1	100	0.33	0	0
Omni Pulse Keyer[3]	1	1	0.7	100	0.33	0	0
Column Assembly	128	1	0.01	100	0.33	0	0
Driver Amplifier[3]	1	1	26	1	0.33	0.2	350
Driver Amplifier[4]	1	1	37	1	0.33	0.2	350
Attenuator Controller[4]	32	1	1.56	100	0.33	0	0
Delay Driver[4]	32	1	4.2	100	0.33	0	0
HIC Circuit	2	1	14.16	1	0.33	0.33	20
VCC Supply Control	32	1	2.29	100	0.33	0	0

Notes: 1. CMOS Signal Processor
2. CCD Signal Processor
3. Tapered-Drive Matrix Switched Array
4. Delay Bit Steered Array

All Parameters for Reliability Level 3

- On-site labor (average mh to identify, remove and replace faulty components) BMH_i
- Depot labor (average mh to repair faulty component) DMH_i
- Average repair parts cost RPC_i
- Number of types of components in this category, and the quantity of each type

With respect to the last item listed above, three of the categories contain different types of components. For example, the "Large Boards" category contains up to 20 different large boards and the "Low Current Power Supply" category contains 6 different power supplies. Costs and parameters for these categories are determined as weighted averages across all types.

Table 7-1 lists the parameters for the four systems.

c. MAINTENANCE CONCEPT EFFECTS

The following assumptions are made concerning the maintenance concept:

- There is no on-site repair of failed components.
- The netting policy has not been determined, hence, costs are to be determined on a per site basis.
- Two maintenance men per trip.
- Preventive maintenance trips will be made when the probability of successful operation has dropped to 0.9.
- Remote fault detection and location is accurate enough to predict the failed component to within:

  2 analog boards 90% of the time

  2 digital boards 90% of the time

  1 row transmitter, receiver, power supply, etc.
- One helicopter team per depot (affects only test equipment cost)
- The term "depot" refers to the logistic nodes.

d. TEST EQUIPMENT COSTS

Two sets of test equipment are required; the equipment transported to the site (or possibly, kept at each site) and the depot test station. Table 7-2 is a list of the test equipment required at the depot. (Costs are approximate, and in 1976 dollars). A yearly maintenance cost of five percent is assumed. This cost represents repair and calibration.

Costs for the transportable equipment are assumed to be $20,000, plus $1000/y calibration, and maintenance cost. The total life cycle cost for each depot is then

$$93600 + 93600 + (20,000 + (20)(1000))N = TEC \qquad (7-1)$$

where N is the number of repair crews for each depot. Assuming 1 repair crew per depot and 6 depots, the total test equipment cost is $1,363,000.

e. RELIABILITY CONSIDERATIONS

The baseline approach to component reliability was to design the system using MIL-M-38510 class B-2 integrated circuits, JAN TX discrete components and established reliability resistors and capacitors, evaluate the probability of successful operation as a function of time, and upgrade components as required.

The following ground rules were derived:

- Increasing reliability from class B-2 to class A produced a ten to one increase in component mean-time-between failures (MTBF) with a two-to-one cost increase.
- Increasing reliability from JAN TX to JAN TXV produced a two-to-one increase in component MTBF with a two-to-one cost increase.
- Class A (or equivalent) quality versions were available for all integrated circuits used. JAN TXV quality versions were available for all discrete components.

Four levels of reliability were evaluated:

1. The baseline approach (using JAN TX and class B-2 components)
2. Conversion of all class B-2 to class A components, thus reducing the failure rate of all large digital boards by a factor of 10. This approach affects only the signal and data processor.

TABLE 7-2. TEST EQUIPMENT COSTS

Required Equipment	Cost
Analog Board Tester	$8,200
Digital Board Tester	46,500
Tools	4,400
Power Supplies	4,000
Oscilloscope	5,700
Sweep Generator	5,000
Signal Generator	6,400
VTVM	2,700
VOM	200
Power Meter	3,000
RF Couplers	600
Misc Cables/Adapters	1,000
VSWR Meter	1,200
Spectrum Analyzer	3,500
Attenuator	1,400
	93,600
Maintenance (5%/yr) 20 yrs	93,600
Total	$187,200

3. Conversion of all JAN TX components in serial portions of the analog and array sections to JAN TXV components. (Class A components again used in the signal and data processors.) The serial portions of the system have a dominant effect on the failure rate.

4. Conversion of all remaining JAN TX components in the analog and array sections to JAN TXV components.

The criteria used to evaluate the reliability is the time at which the probability of successful operation drops below 0.9.

Figure 7-2 is a plot of probability of successful operation for these four approaches as a function of time. It is seen that there is virtually no difference between 3 and 4.

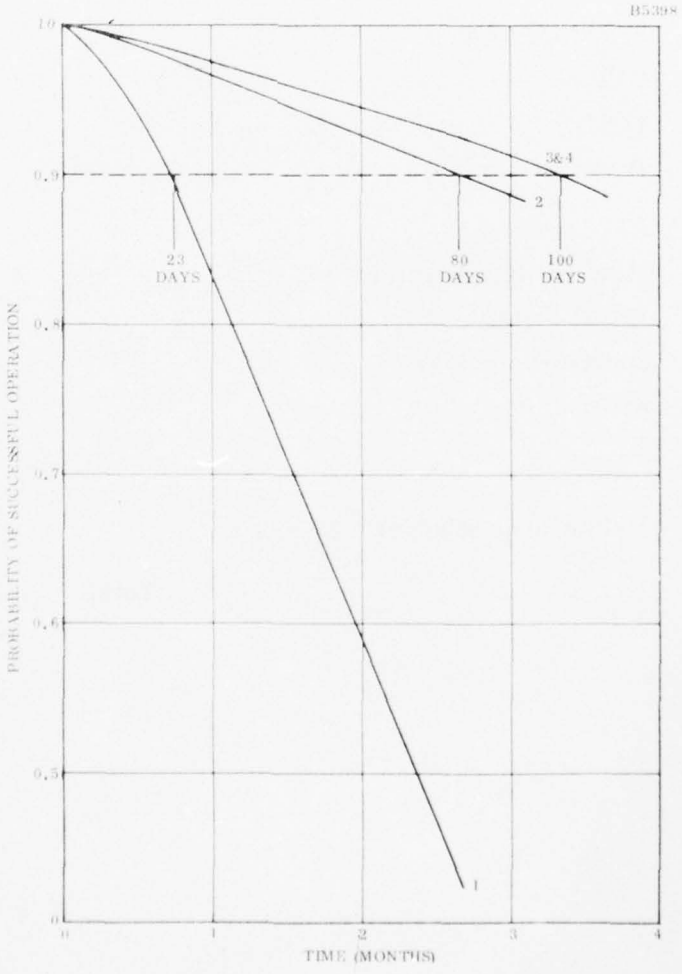


Figure 7-2. Probability of Operation for Four Reliability Options

Assuming the preventive maintenance, PM, actions occur when the probability of successful operation drops below 0.9, then Figure 7-2 can be used to determine the required time between PM trips, ΔPM

Option	ΔPM
1	23 days
2	80 days
3	100 days
4	100 days

With this information the most cost-effective reliability level can be determined, based on the cost of a trip to the site.

The cost of transportation includes:

- Cost of helicopter usage
- Cost of helicopter fuel
- Cost of pilot and crew while in flight and waiting at the site
- Cost of maintenance crew in flight and while performing PM

The following guidelines are derived:

- Seven hours total time from departure to return
- Four hours flight time
- Two helicopter costs used

  900 lb payload $1500/trip
  3000 lb payload $3000/trip

- Two-man maintenance crew at $20/mh

Based on the above assumptions, total cost per trip (CPT) for the two helicopters are:

900 lb payload helicopter CPT = $1780
3000 lb payload helicopter CPT = $3280

The number of trips required per year per site (NT) is given by

$$NT = 365/\Delta PM \tag{7-2}$$

f. LIFE CYCLE COST EQUATIONS

The system and component parameters needed in these equations are listed in Tables 7-3, 7-4, and 7-5.

The O&M cost equations to be used are described as follows:

1. No. of failed components of this type. $NFAIL_i$

$$NFAIL_i = \sum_{j=1}^{NTYP_i} \left(\frac{NSYS \cdot NYR \cdot YOH \cdot FR_i \cdot NPTYP_{ij}}{10^6} \right) \quad (7\text{-}3)$$

Note: The quantity within the summation should be raised to the next highest integer.

2. No. of pipeline spares required, $NPIPE_i$

NPIPE represents the spares required to keep the system in service while the failed components are being repaired

$$NPIPE_i = \sum_{j=1}^{NTYP_i} \left(\frac{NSYS \cdot NYR \cdot YOH \cdot FR_i \cdot NPTYP_{ij} \cdot DRCT \cdot (1 - COND_i)}{10^6} \right) \quad (7\text{-}4)$$

Note: If the quantity within the summation is less than the number of depots, then the quantity is set equal to NDEPOT. In any case, it must be integerized.

3. No. of spares purchased, NPUR

$$NPUR_i = \sum_{j=1}^{NTYP_i} \left(\frac{NSYS \cdot NYR \cdot YOH \cdot FR_i \cdot NPTYP_{ij} \cdot COND_i}{10^6} \right) \quad (7\text{-}5)$$

Once again, the quantity within the summation, if it is nonzero, must be integerized and greater than the number of depots.

TABLE 7-3. COST VARIABLES AND PARAMETERS

Symbol	Description	Units	Value
	System Parameters		
NSYS	No. of systems		80
NYR	No. of years in the radar life	yrs	20
YOH	Yearly operating hours	h	8760
$CPIM_R$	Cost to maintain an item in the government inventory	$/item	105
$CPIM_I$	Cost to enter an item in the government inventory	$/item	500
DRCT	Depot repair cycle time (Fraction of total radar life)		0.00833
BLR	Base labor rate	$/mh	20
DLR	Depot Labor rate	$/mh	25
NI	No. of new items		200
PT	Total power used	W	975/1080
CKW	Cost per kilowatt hour	$/kWh	0.12
CPT	Cost per trip	$	1780/3280
NDEPOT	No. of depots		6
NT	No. of trips per year per system		
NCAT	No. of component cost categories		17

TABLE 7-4. COMPONENT PARAMETERS

Symbol	Description
$COST_i$	Cost of component category
QTY_i	Total number in this component category
$NTYP_i$	No. of different types within category (e.g., no. of different kinds of large boards)
$NPTYP_{ij}$	No. of j^{th} type of component within the i^{th} category
$COND_i$	Fraction of components condemned on failure
BMH_i	On-site mh to identify, remove and replace failed component
DMH_i	Depot level mh to repair failed component
RPC_i	Average repair parts cost for component

TABLE 7-5. COST VARIABLES AND PARAMETERS - OVERALL COSTS

Symbol	Description
CMCR	Material cost of repair. Total cost of repair parts
CLE_1	Cost of initial and replacement spares
CLE_2	On-equipment (on-site) labor costs
CLE_3	Off-equipment (at-depot) labor costs
CPP	Cost of prime power (yearly)
CT	Cost of preventive maintenance trips (yearly)
$CSIM_R$	Yearly cost of maintaining an item in the government inventory
$CSIM_I$	Initial cost of maintaining an item in the government inventory

4. Cost of initial and replacement spares, CLE_1

The cost of spares over the life of the system, assuming no safety spares, and no change in cost of spare production, is given by

$$CLE_1 = \sum_{i=1}^{NCAT} NPUR_i \cdot COST_i \tag{7-6}$$

5. Material cost of repair, CMCR

The cost of repair parts over the life of the system is given by:

$$CMCR = \sum_{i=1}^{NCAT} NFAIL_i \cdot (1 - COND_i) \cdot RPC_i \tag{7-7}$$

6. On-equipment labor costs, CLE_2

The cost of labor for repair at the site is given by:

$$CLE_2 = \sum_{i=1}^{NCAT} NFAIL_i \cdot BMH_i \cdot BLR \tag{7-8}$$

7. Off-equipment labor costs, CLE_3

The cost of labor repair at the depot level is given by:

$$CLE_3 = \sum_{i=1}^{NCAT} NFAIL_i \cdot DMH_i \cdot DLR\ (1 - COND_i) \tag{7-9}$$

8. Cost of prime power, CPP

The yearly cost of prime power, per system is given by

$$CPP = YOH \cdot PT \cdot CKW \tag{7-10}$$

9. Cost of supply item management

a) Initial

$$CSIM_I = CPIM_I \cdot NI \tag{7-11}$$

b) Yearly

$$CSIM_R = CPIM_R \cdot NI \tag{7-12}$$

10. Cost of transportation, CT (per system per year)

$$CT = NT \cdot CPT \tag{7-13}$$

h. LIFE CYCLE COSTS

The equations displayed in the previous section were used to develop costs for four different systems and four different levels of component reliability. The systems and reliability levels are described below. The total 80 system, 20 year costs are displayed in Table 7-6 and the per year, per system costs are displayed in Table 7-7.

(1) System Descriptions

The following systems were costed on the basis of 128 boards in the array.

- CCD Signal Processor and Matrix Switched Array
- CCD Signal Processor and Delay Bit Steered Array
- CMOS Signal Processor and Matrix Switched Array
- CMOS Signal Processor and Delay Bit Steered Array

(2) Reliability Options

The following reliability options apply:

1. Baseline approach using JAN TX and B-2 type components.
2. Increased reliability obtained by using type A components on all digital boards.
3. Further reliability increased by using JAN TXV components in serial portions of array and analog receive.
4. Final reliability increase obtained by using all JAN TXV components in the array and receiver.

Cost coefficients were assumed for base and depot labor rates and prime power cost. An analysis of the sensitivity to these coefficients is performed in the following section.

TABLE 7-6. OVERALL OPERATIONS AND MAINTENANCE COSTS

50 System 20 Yr Costs
(Values in Millions of Dollars)

System	Material Cost of Repair CMCR	Spares Cost CLE_1	Base Labor Cost CLE_2	Depot Labor Cost CLE_3	Inventory Management CSIM	Power Cost CPP	Test[1] Equipment TEC	Transportation CT^2	Transportation CT^3	Total Cost[2] (O&M)	Total Cost[3] (O&M)	Change in Initial Cost
A-1	1.57	6.75	0.313	0.315	0.52	1.64	1.12	45.20	83.28	57.43	95.51	-
A-2	0.872	6.56	0.139	0.098				12.99	23.94	23.94	34.89	1.26
A-3	0.75	6.55	0.136	0.096				10.40	19.16	21.21	29.97	1.47
A-4	0.71	6.57	0.098	0.093				10.40	19.16	21.15	29.91	9.06
B-1	1.74	7.49	0.348	0.344				45.20	83.28	58.40	196.48	-
B-2	1.05	7.07	0.175	0.129				12.99	23.94	24.69	35.64	1.26
B-3	0.87	7.05	0.171	0.127				10.40	19.16	21.90	30.66	1.44
B-4	0.879	7.06	0.133	0.124				10.40	19.16	21.83	30.57	9.03
C-1	1.82	7.17	0.370	0.383		1.82		45.20	83.28	58.40	96.48	-
C-2	0.92	6.64	0.144	0.104				12.99	23.94	24.26	35.21	2.55
C-3	0.92	6.63	0.142	0.103				10.40	19.16	21.66	30.42	2.77
C-4	0.88	6.65	0.104	0.100				10.40	19.16	21.59	30.35	10.35
D-1	2.00	7.64	0.405	0.414				45.20	83.28	59.12	97.20	-
D-2	1.10	7.11	0.180	0.136				12.99	23.94	24.98	35.93	2.55
D-3	0.92	7.09	0.176	0.133				10.40	19.16	22.18	30.94	2.74
D-4	0.88	7.11	0.138	0.131				10.40	19.16	22.11	30.88	10.32

Notes: 1. Assumes 6 depots at 187,200 /depot
2. Assumes use of a 900-lb payload helicopter
3. Assumes use of a 3000-lb payload helicopter

TABLE 7-7. OPERATIONS AND MAINTENANCE COSTS

System	Material Cost of Repair CMCR	Spares Cost CLE_1	Base Labor Cost CLE_2	Depot Labor Cost CLE_3	Power Cost CPP	Transportation Cost CT^1	Transportation Cost CT^2	Total Cost[1]	Total Cost[2]
	Per Yr Per System Costs (Thousands of Dollars)								
A-1	0.98	4.22	0.2	0.2	1.02	28.25	52.05	34.87	58.67
A-2	0.55	4.10	0.09	0.06		8.12	14.97	13.94	20.79
A-3	0.47	4.10	0.09	0.06		6.5	11.97	12.24	17.71
A-4	0.44	4.11	0.06	0.06		6.5	11.97	12.19	17.66
B-1	1.09	4.68	0.22	0.21		28.25	52.05	35.47	59.27
B-2	0.66	4.42	0.11	0.08		8.12	14.97	14.41	21.26
B-3	0.54	4.41	0.11	0.08		6.5	11.97	12.66	18.13
B-4	0.52	4.42	0.08	0.08		6.5	11.97	12.62	18.09
C-1	1.14	4.49	0.23	0.24	1.14	28.25	52.05	35.49	59.29
C-2	0.58	4.15	0.09	0.07		8.12	14.97	14.15	21.0
C-3	0.58	4.15	0.09	0.06		6.5	11.97	12.52	17.99
C-4	0.55	4.16	0.06	0.06		6.5	11.97	12.47	17.94
D-1	1.25	4.78	0.25	0.26		28.25	52.05	35.93	59.73
D-2	0.69	4.45	0.11	0.09		8.12	14.97	14.60	21.45
D-3	0.92	4.43	0.11	0.08		6.5	11.97	13.18	18.65
D-4	0.55	4.44	0.09	0.08		6.5	11.97	12.80	18.27

Notes:
1. Assumes use of a 900-lb payload helicopter.
2. Assumes use of a 3000-lb payload helicopter.

i. PARAMETER VARIATIONS

Since the maintenance concept has not been specified, only a general concept was assumed and therefore, some of the cost parameters are not well defined. It was decided to choose typical values for these parameters, and then analyze the sensitivity of the costs to these values. The parameters to be varied are:

CKW	Cost per kilowatt of prime power
DLR	Depot labor rate
BLR	Base labor rate
NDEPOT	No. of depots

(1) Prime Power Cost

Since power cost coefficients are not known, the power cost for each of the systems will be analyzed parametrically.

Figure 7-3 shows the yearly power costs for various cost coefficients.

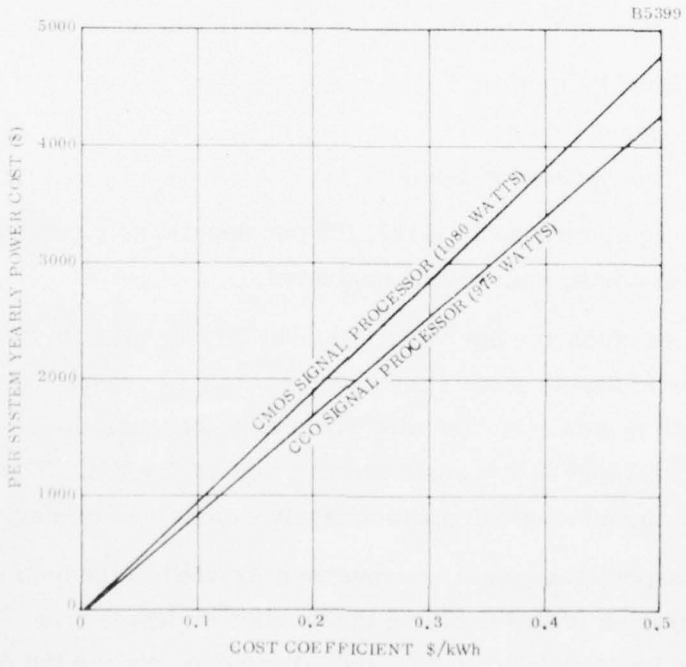


Figure 7-3. Power Cost as a Function of Rate

Exclusive of power, the average yearly operating cost for each system is on the order of $20,000. Assuming cost coefficients in the area of 0.05$/kWh to 0.15$/kWh, then power ranges from 2% to 10% of the total yearly cost of operating. Over the life of the system, the difference between the maximum and minimum power systems is about $2000 per system or about $200,000 for all 80 systems. This difference is less than 0.5% of the total life cycle cost of the 80 systems. Therefore, overall system costs are insensitive to power cost coefficients over reasonable ranges.

(2) Base and Depot Labor Rates

Labor costs appear in the transportation costs, as well as in the depot and base repair costs. Depending on the system, labor costs average between 8 to 15 percent of the yearly O&M costs. Thus, variations in labor rates over wide ranges will not drastically affect overall costs.

(3) Number of Depots

The effect of the number of depots is felt in three ways:

1. Test Equipment Costs
2. Spares Costs
3. Transportation Costs

Test equipment costs ($187,200 per depot) are a relatively small fraction of total system costs, and may be neglected.

Spares costs are not negligible, but the variation in these costs when increasing the number of depots from 1 to 12 is less than 1 percent. In fact, to completely spare all 80 systems at each site would only increase the cost of spares (for system D-1 the CMOS signal processor) from $13M to $14.8M. Therefore, the effect of increasing the number of depots on spares costs will be neglected.

Transportation costs are inversely related to the number of depots. A reasonable assumption is that doubling the number of depots from 6 to 12 will essentially reduce the transportation time, and, therefore, reduce the costs by a factor of two. Table 7-8 shows this would be a significant cost savings.

Thus, from the standpoint of O&M costs for the unattended radar, the net effect of increasing the depots is to reduce the overall costs.

j. SMALL BOARD/LARGE BOARD COMPARISON

The choice between small, throw-away printed circuit boards and large repairable multiwire boards is not clear cut. A true comparison should not only include the initial construction and checkout costs, but also the maintenance and spares cost over the life of the system. Actually, these costs can all be expressed in relatively simple equations, but the simplicity is deceptive since most of the parameters in the equations are not precisely known.

The following definitions, ground rules and assumptions will be used throughout the analysis:

- Costs are based on 80 systems operating for 20 years.
- Large and small board construction costs are based on broad averages. The cost of each large board is assumed to be the same, as is the cost of each small board.
- The number of different types of boards does not have a significant effect so all boards will be treated as if they were identical.
- All small boards are condemned on failure ("throw-away"), all large boards are depot repairable.
- Small boards have a 10 board fault area, large boards have a 1 board fault area.

(1) Large-to-Small IC Growth

It is unlikely that exactly the same number of IC's will be required for both the large and small board concepts. Fault detection and location will probably force more components to be needed for the small boards. A five to ten percent growth in the number of IC's is assumed.

Board Descriptions:

Small - (Type I) 3 in. x 3.4 in.

4 IC's 1-56 pin connector

Large 7.7 in. x 11 in.

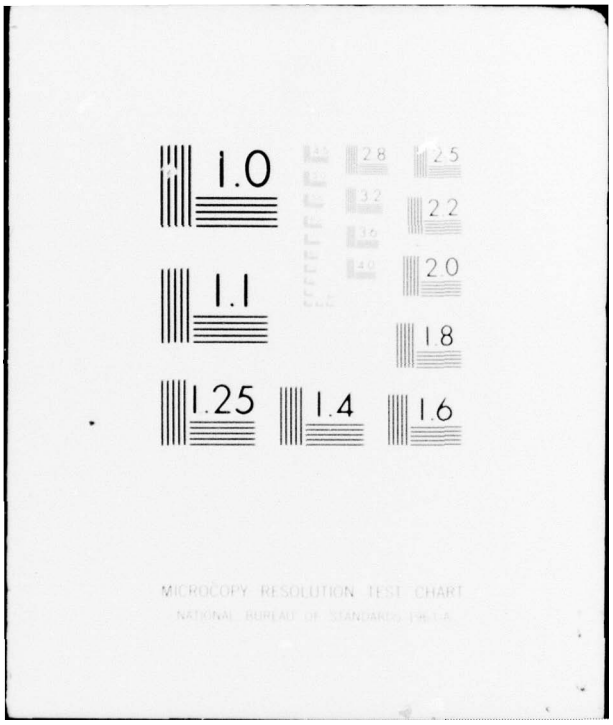
slots for 90 IC's but usually limited by connectors, wires, etc. to ≈ 45 IC's/board 155 pin connector

AD-A044 274 GENERAL ELECTRIC CO SYRACUSE N Y ELECTRONIC SYSTEMS DIV F/G 17/9
UNATTENDED/MINIMALLY ATTENDED RADAR STUDY. VOLUME II. 2-D (UNAT--ETC(U)
AUG 77 T B SHIELDS, S E BELL, M I FOX F30602-76-C-0380
UNCLASSIFIED RADC-TR-77-263-VOL-2 NL

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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

Basic material and labor costs:

Large Board Material:	=	$155
Labor:	=	$69
IC's:		$900
Total Cost		≈$1120

Small (Type I) Board:

Material	=	$31
Labor	=	$8
IC's	=	$80
		≈$120

Total-Life Cycle Cost of Electronics:

The following listings affect the electronics total life cycle costs:

Variables

NL	=	No. of large boards	= 60
NS	=	No. of small boards	= 720
$MTBF_L$	=	Mean time between failures (large boards)	= 3.3×10^4 h
$MTBF_S$	=	Mean time between failures (small boards)	= 4×10^5 h
NSYS	=	No. of systems purchased	= 80
NYR	=	No. of years of operation	= 20 yrs
YOH	=	Yearly operating hours	= 8760
DRCT	=	Depot repair cycle time (fraction of total radar life)	
BMH_L	=	Man-hours to identify, remove, replace boards on site (large)	= 0.1
BMH_S	=	Same as BMH_L except for small boards	= 0.2
DMH_L	=	Same as BMH_L except at the depot	= 0.33
BLR	=	Base labor rate	$20/h
DLR	=	Depot labor rate	$25/h
$COST_L$	=	Large board cost	1120
$COST_S$	=	Small board cost	120
RPC_L	=	Average repair parts cost	60

1. Total Investment Costs (CI)

$$CI_L = N_L \cdot NSYS \cdot COST_L = \$5.376 \times 10^6$$

$$CI_S = N_S \cdot NSYS \cdot COST_S = \$6.912 \times 10^6$$

2. Cost of Initial and Replacement Spares

$$CLE_{1L} = NSYS \cdot NYR \cdot YOH \cdot NL \cdot DRCT \cdot COST/MTBF_L = \$2.37 \times 10^5$$

(Cost to keep pipeline full)

$$CLE_{1S} = NSYS \cdot NYR \cdot YOH \cdot N_S \cdot COST/MTBF_S = \$3.03 \times 10^6$$

3. Material Cost of Repair

(Since no small boards are repaired, this cost is zero for small boards.)

$$CMCR_L = NSYS \cdot YOH \cdot NYR \cdot NL \cdot RPC_L/MTBF_F = \$1.53 \times 10^6$$

4. Labor Cost of Repair

(On equipment)

$$CLE_{2L} = YOH \cdot NSYS \cdot BMH_L \cdot NYR \cdot BLR \cdot N_L/MTBF_L = \$5.09 \times 10^4$$

$$CLE_{2S} = YOH \cdot NSYS \cdot BMH_S \cdot NYR \cdot BLR \cdot N_S/MTBF_S = \$1.01 \times 10^5$$

(Off equipment)

(This cost is zero for small boards.)

$$CLE_{3L} = YOH \cdot NYR \cdot NSYS \cdot NL \cdot DMH_L \cdot DLR/MTBF_L = \$2.08 \times 10^5$$

Total Cost

Large Board $\$7.4 \times 10^6$

Small Board $\$10.04 \times 10^6$

Thus, under the stated ground rules, the large board costs are approximately 74% of the corresponding small board design and, therefore, the recommended approach is to use large boards.

k. TOTAL SYSTEM MANHOURS

The total number of manhours spent in maintenance is not a cost figure, but is included for consideration. Table 7-8 identifies the per year per system manhours spent in replacing and repairing radar components for each of the systems costed.

TABLE 7-8. TOTAL PER YEAR PER SYSTEM MANHOURS

System	On-Site Manhours	Depot Manhours
A-1	10.0	10.0
A-2	4.5	3.0
A-3	4.5	3.0
A-4	3.0	3.0
B-1	11.0	10.5
B-2	5.5	4.0
B-3	5.5	4.0
B-4	4.0	4.0
C-1	11.5	12.0
C-2	4.5	3.5
C-3	4.5	3.0
C-4	3.0	3.0
D-1	12.5	13.0
D-2	5.5	4.5
D-3	5.5	4.0
D-4	4.5	4.0

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