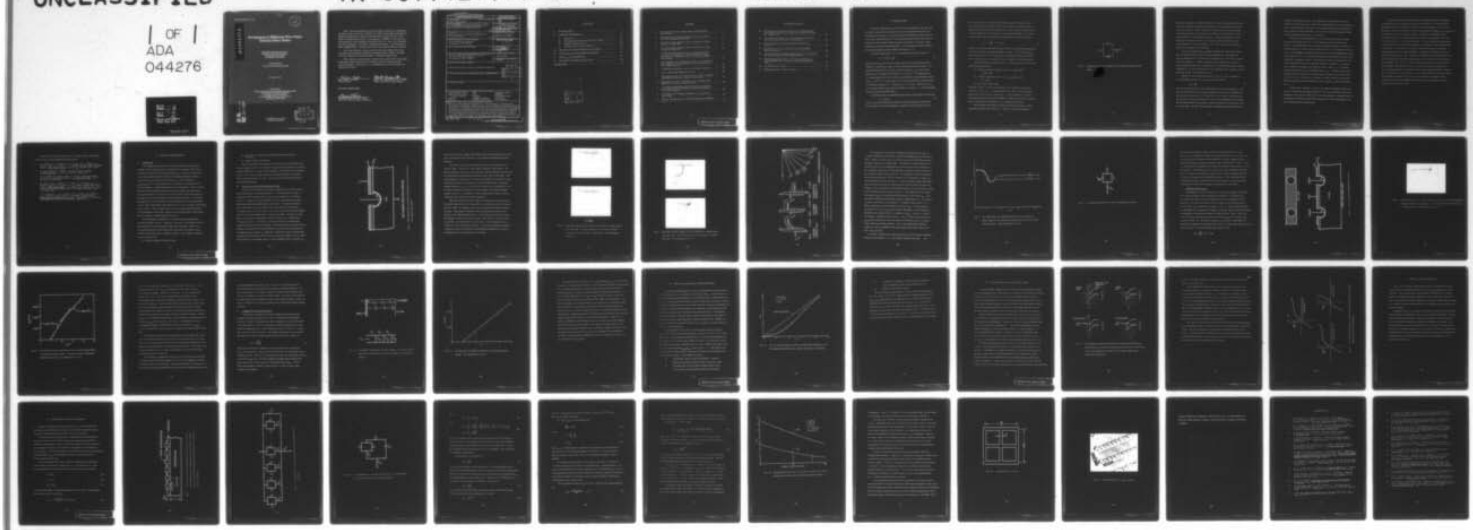
AD-A044 276 AEROSPACE CORP EL SEGUNDO CALIF IVAN A GETTING LABS F/G 9/5
DEVELOPMENT OF MILLIMETER-WAVE SUPER SCHOTTKY MIXER DIODES.(U)
AUG 77 M MCCOLL, M F MILLEA, A H SILVER F04701-76-C-0077
UNCLASSIFIED TR-0077(2777)-1 SAMSO-TR-77-194 NL

1 OF 1
ADA
044276



END
DATE
FILMED
10-77
DDC

REPORT SAMSO-TR-77-194



# Development of Millimeter-Wave Super Schottky Mixer Diodes

Electronics Research Laboratory
The Ivan A. Getting Laboratories
The Aerospace Corporation
El Segundo, Calif. 90245

Progress Report

(1 July 1975—30 September 1976)

19 August 1977

Prepared for

SPACE AND MISSILE SYSTEMS ORGANIZATION
AIR FORCE SYSTEMS COMMAND
Los Angeles Air Force Station
P.O. Box 92960, Worldway Postal Center
Los Angeles, Calif. 90009

This report was submitted by The Aerospace Corporation, El Segundo, CA 90245, under Contract No. F04701-76-C-0077 with the Space and Missile Systems Organization, Deputy for Advanced Space Programs, P.O. Box 92960, Worldway Postal Center, Los Angeles, CA 90009. It was reviewed and approved for The Aerospace Corporation by G. W. King, Vice President and General Manager, The Ivan A. Getting Laboratories. Lieutenant Dara Batki, SAMSO/YAPT, was the project officer for Advanced Space Programs.

This report has been reviewed by the Information Office (OI) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

Dara Batki
Dara Batki, Lt, USAF
Project Officer

Robert W. Lindemuth
Robert W. Lindemuth, Lt Col, USAF
Chief, Technology Plans Division

FOR THE COMMANDER

Floyd R. Stuart
Floyd R. Stuart, Colonel, USAF
Deputy for Advanced Space Programs

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

| (19) REPORT DOCUMENTATION PAGE | | READ INSTRUCTIONS BEFORE COMPLETING FORM |
|---|---|---|
| 1. REPORT NUMBER<br>SAMSO-TR-77-194 | 2. GOVT ACCESSION NO. | 3. RECIPIENT'S CATALOG NUMBER |
| 4. TITLE (and Subtitle)<br>DEVELOPMENT OF MILLIMETER-WAVE SUPER SCHOTTKY MIXER DIODES. | | 5. TYPE OF REPORT & PERIOD COVERED<br>Progress<br>1 July 1975 - 30 Sept 1976 |
| | | 6. PERFORMING ORG. REPORT NUMBER<br>TR-0077(2777)-1 |
| 7. AUTHOR(s)<br>Malcolm McColl, Michael F. Millea and Arnold H. Silver | | 8. CONTRACT OR GRANT NUMBER(s)<br>F04701-76-C-0077 |
| 9. PERFORMING ORGANIZATION NAME AND ADDRESS<br>The Aerospace Corporation<br>El Segundo, Calif. 90245 | | 10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS<br>(12) 55 p. |
| 11. CONTROLLING OFFICE NAME AND ADDRESS | | 12. REPORT DATE<br>19 August 1977 |
| | | 13. NUMBER OF PAGES<br>52 |
| 14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)<br>Space and Missile Systems Organization<br>Air Force Systems Command<br>Los Angeles, Calif. 90009 | | 15. SECURITY CLASS. (of this report)<br>Unclassified |
| | | 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE |

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited



17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

| | | |
|---|---|---|
| Super Schottky Diode | InSb | Multiple Contacts |
| Superconductor-Semi-conductor Diode | InAs | MOSFET |
| | (InGa)Sb | Self-Aligned Gate |
| Mixers | Leakage Currents | Inversion |
| Detectors | Contact Array Diode | Accumulation |

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The Electronics Research Laboratory of The Aerospace Corporation is developing a heterodyne millimeter wave Superconducting Low Noise Receiver. This report, covering FY 76 and FY76T, discusses the progress in developing techniques to extend the performance of the super-Schottky mixer diode into the millimeter wavelength region. The report is divided into four subjects: (1) the identification of leakage mechanisms and their control; (2) a superconducting Schottky contact to n-type InSb; (3) a superconducting contact to an (InGa) Sb surface on n-InSb, and. (4) the contact array diode.

DD FORM (FACSIMILE) 1473

409 944

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

CONTENTS



## FIGURES

FIGURES (Continued)

# I. INTRODUCTION

The major emphasis from July 1975 through September 1976 has been to extend the frequency performance of the super-Schottky diode into the millimeter wave region. In this introduction we identify the state of the art of the super-Schottky diode as it is presently being fabricated, discuss the parameters which limit its high frequency performance, and then outline methods to overcome these limitations. Our progress with these methods are then discussed in greater detail in Sections II - VI.

The noise temperature, $T_r$, of a heterodyne receiver is given by

$$T_r = L_c(T_d + T_{IF}) \tag{1}$$

where $T_d$ and $T_{IF}$ are the noise temperatures of the mixer diode and IF amplifier, respectively, and $L_c$ is the conversion loss of the mixer. The proportionality between $T_r$ and $L_c$ illustrates that $L_c$ is a very critical ingredient in the design of the mixer for a receiver. The importance of $L_c$ is particularly true for a receiver incorporating a super-Schottky mixer. Using $3 \times 10^{19}$ $cm^{-3}$ p-type GaAs as the substrate material, measurements at X-band have yielded $L_c \approx 7$ dB and $T_d = 1.2$ K [1,2]. This value of $T_d$ is well below values of $T_{IF}$ that are available, and hence, $L_c$ is the dominant mixer parameter with this device.

Conversion loss is conveniently expressed as the product of two terms

$$L_c = L_0 L_1 \tag{2}$$

where $L_0$ is the intrinsic loss associated with the frequency conversion process that occurs in the nonlinear resistance of the junction and $L_1$ is

the loss arising from the parasitic elements $R_s$ and C, shown in Fig. 1. $R_s$ is the spreading resistance and is the resistance within the semiconductor that arises from the crowding of the current near the metal contact. C is the capacitance of the junction. It is easily shown that $L_1$, the ratio of power absorbed by R and $R_s$ to that absorbed by R alone is given by

$$L_1 = 1 + \frac{R_s}{R} + \omega^2 C^2 R R_s \qquad (3)$$

where $\omega$ is the signal angular frequency and R is the signal input impedance of the local oscillator pumped nonlinear resistance. The $\omega^2$ dependence of the third term in Eq. 3 is the origin of the difficulty with the Schottky barrier type of mixer, including the super-Schottky, at high frequencies.

Several methods for minimizing $L_1$ by reducing $R_s$ have been investigated during this period:

(1) A superconducting Schottky contact to n-type InSb or p-type InAs;

(2) A superconducting contact to an $In_{1-x}Ga_xSb$ surface on n-InSb;

(3) The contact array diode.

Methods (1) and (2) involve the reduction of the resistivity of the semiconductor. Since $(L_1 - 1)$ is proportional to $R_s$ which in turn is proportional to the semiconductor resistivity, $L_1$ can be reduced by choosing semiconductors that have large mobilities. Method (3) involves a reduction of $R_s$ by utilizing the dependence of $L_1$ on geometrical factors.

High mobility semiconductors with low effective masses are ideal substrates because they have low $R_s$. However, some low band gap

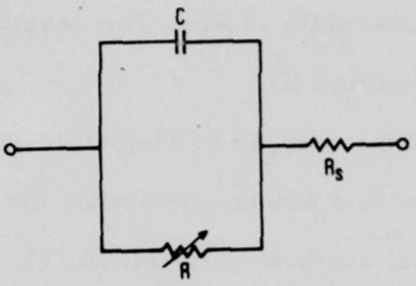



Fig. 1 Equivalent circuit of a single-contact super-Schottky barrier diode.

materials, notable n-InSb [3] and n-InAs [4], [5] are characterized by near zero barrier heights with most metal contacts. An exception to this rule is the Au contact to n-InSb. Method (1) combines this fact with the superconducting proximity effect wherein a thin film of Au in contact to a bulk superconductor becomes superconducting. Initial experiments with this approach have involved the use of a thin film contact of plated Au onto n-InSb followed by a thick overplate of Pb. The results of these experiments are summarized in Section III.

The ternary material $In_{1-x}Ga_xSb$ of Method (2) combines the advantage of a high mobility [6] with a strong possibility for controlling the barrier height by the crystal surface composition [7]. Thus these crystals would be capable of providing a suitable barrier height for a variety of superconducting metals and, simultaneously, permit achieving lower series resistances. We are in the process of investigating these crystals, and our progress to date is outlined in Section V.

Method (3) involves the dependences of $R_s$, R, and C on diameter. The spreading resistance of a single contact is given by

$$R_s = \frac{\rho}{2d} \tag{4}$$

where $\rho$ is the resistivity of the semiconductor and d is the diameter. The behaviors of R and C on d are more conventional, as they are dependent on the area of the junction: $R \propto d^{-2}$ and $C \propto d^2$. As a result, both of the loss terms in Eq. 3 are proportional to d. Hence it would appear by this reasoning that the parasitic loss problem could be minimized by reducing the size of the junction. However, this approach if simply followed will produce an

impedance mismatch problem. The impedance of the microwave circuit dictates the total active area of the super-Schottky diode on a given substrate, and for areas well below that size the resulting mismatch loss (contained in the $L_0$ term) becomes intolerable. The contact array diode approach alleviates this dilemma between $L_0$, $L_1$, and size.

The contact array approach is one of connecting in parallel a large number of small diodes [8, 9]. In its simplest terms the concept is as follows. It is easily shown for an array of independent diodes connected in parallel that the $L_1$ of the array is identical to the $L_1$ of a single diode of that array. The impedance matching condition can be met by maintaining the total conducting area, i.e., the sum of the areas of the small diodes, at the value needed for an impedance match. By holding this total area fixed as the size of the small diodes is reduced and their number increased, $L_1$ is reduced, and $L_0$ remains unchanged at its optimum value. Since $(L_1 - 1)$ is proportional to the diameter d of an individual diode, $(L_1 - 1)$ becomes inversely proportional to the square root of the number of diodes in the contact array structure. Hence, a structure consisting of a large number of very small diodes achieves the minimum values for both $L_0$ and $L_1$, and consequently, for $L_c$.

Of these three methods, (1) and (2) are material dependent approaches which can extend the desirable properties of the super-Schottky well into the millimeter wave region. Method (3) is strictly geometric in approach and can be applied to both the present p-GaAs diodes and to diodes developed by the other methods under consideration.

Leakage currents with Schottky barriers on InSb have been investigated in some detail and our progress is discussed in Section II. We feel that this phenomenon should be well understood because its elimination is basic to the operation of the super-Schottky on whatever semiconductor (InSb, $In_{1-x}, Ga_xSb$, etc.) is ultimately proven the most successful. Leakage is controllable using a field plate structure and is minimized when the field plate voltage drives the oxide-InSb interface to a flat band condition. We have measured the properties of this inversion on p-type InSb and indeed a well defined n-type channel exists at the surface. The low barrier height of gold contacts to the n-type InSb channel apparently offers little impedance and permits straight-forward conductance measurements. The conductance properties of this channel agree well with the field-plate-dependent leakage data. The channel has an enormously large mobility, $10^4$ $cm^2/V\text{-}s$. This is disadvantageous but is a direct result of our originally choosing InSb in order to reduce the bulk series resistance. As an interesting fallout, this high mobility channel could possibly be utilized in the construction of a high frequency, low-noise field effect transistor (FET). The frequency capability of an FET is proportional to the mobility of the channel and such a device might function well as an IF amplifier in a millimeter wave low-noise receiver.

In the past period our progress with the super-Schottky and related work has led to several publications listed below.


1. M. McColl, R. J. Pedersen, M. F. Bottjer, M. F. Millea, A. H. Silver, and F. L. Vernon, Jr., "The super-Schottky diode microwave mixer", Appl. Phys. Letters, vol. 28, pp. 159-162, 1 Feb. 1976.

2. M. McColl and M. F. Millea, "Schottky Barriers on InSb", J. Electronic Mat., vol. 5, pp. 191-207, April, 1976.

3. M. F. Millea, M. McColl, and A. H. Silver, "Electrical Characterization of Metal/InAs Contacts", J. of Electronic Mat., vol. 5, pp. 321-340, June 1976.

4. M. McColl, M. F. Millea, A. H. Silver, M. F. Bottjer, R. J. Pedersen, and F. L. Vernon, Jr., "The super-Schottky Microwave Mixer", IEEE Trans. Mag., vol. MAG-13, pp. 221-227, Jan. 1977; presented as an invited paper at the 1976 Appl. Supercond. Conf., 19-20 Aug. 1976.

5. F. L. Vernon, Jr., M. F. Millea, M. F. Bottjer, A. H. Silver, R. J. Pedersen, and M. McColl, "The super-Schottky Diode", IEEE Trans. Microwave Theory Tech., special issue on Low-Noise Technology; vol. MTT-25, pp. 286-294, April 1977.

## II. LEAKAGE EXPERIMENTS

### A. Background

The ultimate performance of a super-Schottky barrier depends on forming a nearly ideal structure in which the free carriers in the semiconductor tunnel directly to the superconductor. Leakage currents, that is any charge flow other than this direct tunneling component, detract from the device performance by increasing $L_0$ via the reduction in $g_{max}/g_{min}$ [1,2]. During this past FY an intensive investigation of the surface leakage on InSb Schottky barriers was undertaken. Surface leakage has always been a problem with semiconductor devices, but with narrow band gap materials it is even more serious because of the relatively weak pinning of the surface potential at the oxide-InSb interfaces. An intensive investigation of surface leakage on InSb Schottky barriers was undertaken to gain a more fundamental understanding of the carrier transport mechanism on the surface. These results, and even more so the experimental techniques developed in this study, should be directly applicable to minimizing surface leakage on (InGa)Sb Schottky barriers.

Our investigation employed a somewhat unique self-aligned gate-controlled Schottky barrier. This device structure, which operates on the same principle as an isolated gate field-effect transistor, allows us to control the electronic energy band in the region where the metal, semiconductor and surface have a common boundary. Three types of measurements are performed:

(a) Surface leakage versus gate bias;

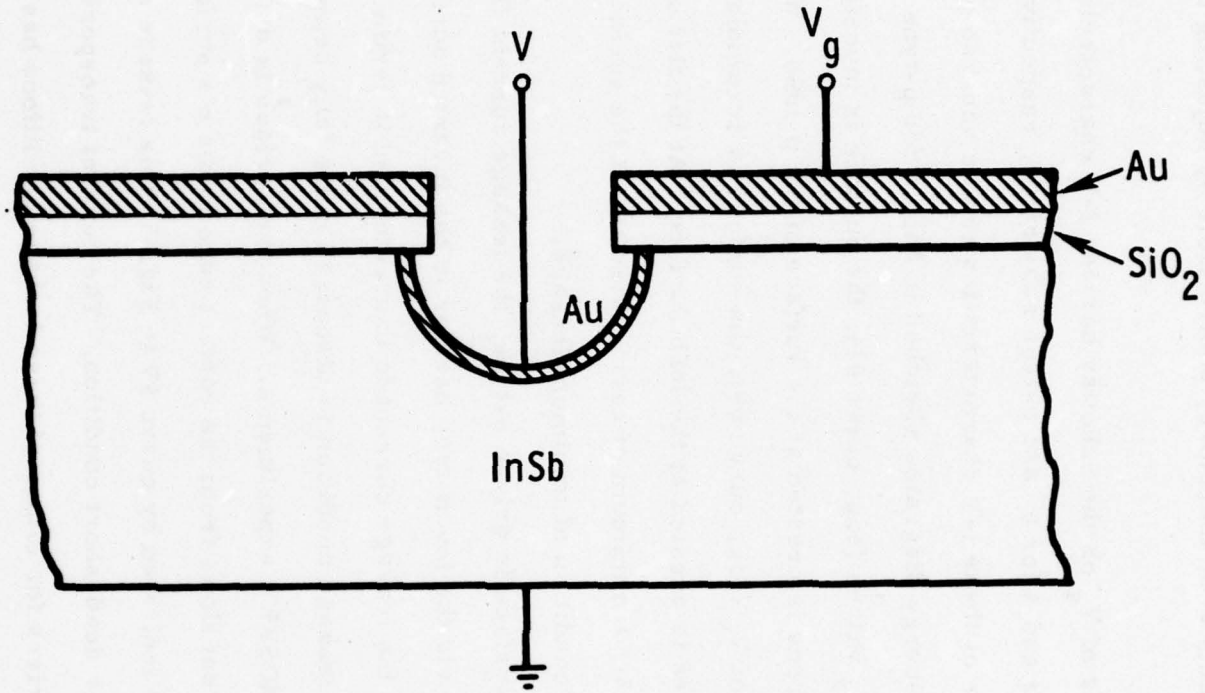
(b) Capacitance versus bias of the gate-oxide-semiconductor structure;

(c) Surface channel conductance.

These experiments have allowed us to construct a firm model for the surface leakage current. A relatively strong p+ surface exists on our oxide-coated p-InSb wafer. A large surface leakage results from this accumulated surface, but it can be greatly reduced by driving the surface to flat band with a positive gate bias. In effect, the surface channel shorts the metal contact to the substrate.

B. The gate-controlled Schottky barrier diode

The structure devised for the leakage experiments is shown in Fig. 2 and is fabricated in the following manner. A cleaved surface of InSb is coated with 1600 Å of $SiO_2$ using the pyrolysis of silane for ≈ 20 minutes at 215° C. Windows 5 mils in diameter are then etched through the $SiO_2$ film using standard photolithographic techniques. A methonal-bromine etch is then used to produce both a cavity in the InSb and an $SiO_2$ lip, or overhand, around the entire cavity. The cavity is then heavily electroplated with Au to form a Schottky barrier contact to the InSb. The gate, or field plate, is created by evaporating Au on the $SiO_2$ surface, completely encircling the contact. The function of the lip overhang is to electrically isolate the contact from the field plate. In the parlance of the semiconductor industry, the field plate is self-aligned because the electric field produced by applying a gate voltage $V_g$ completely overlaps the contact ensuring that the entire surface adjacent to the contact is under the influence of $V_g$. Hence strong effects in the leakage behavior of the Schottky barrier contact by $V_g$




SELF-ALIGNED FIELD PLATE STRUCTURE

Fig. 2 Self-aligned gate controlled Schottky barrier structure used in the leakage experiments.

would verify that the leakage is dominated by the surface potential near the edge of the contacts and, therefore, controllable by adjusting the surface potential.

The effects of $V_g$ on the Schottky barrier I-V characteristics are shown in Figs. 3 and 4 for n- and p-type substrates, respectively. The general behavior of these I-V characteristics can be understood in reference to the potential energy diagrams sketched in Fig. 5 for p-type InSb. With large positive $V_g$ values (e.g. curve #1), the surface is inverted (n), and a channel of electrons is created at the surface of the p-InSb. With large negative biases of $V_g$ (e.g. curve #9), the surface is accumulated (p), and an excess of holes is created at the InSb surface. At the flat band gate voltage (curve #3), a minimum of carriers exists at the surface, and the contact is in its condition of minimum leakage.

When the surface is driven n-type, the leakage current flows from the contact edge via the low n-type barrier to the inverted surface channel, and as a result, the leakage current is characterized in terms of surface currents. This leakage condition is discussed more fully below in the section on our MOSFET experiments. When the surface is driven p-type, the leakage current flows from the contact edge to the p + surface to the p-type InSb. As indicated by curve #9 in Fig. 5, this leakage can be increased to a near dead-short condition. The current transport across the "weakened" barriers for either of these leakage conditions has not been investigated but is most likely due to tunneling.

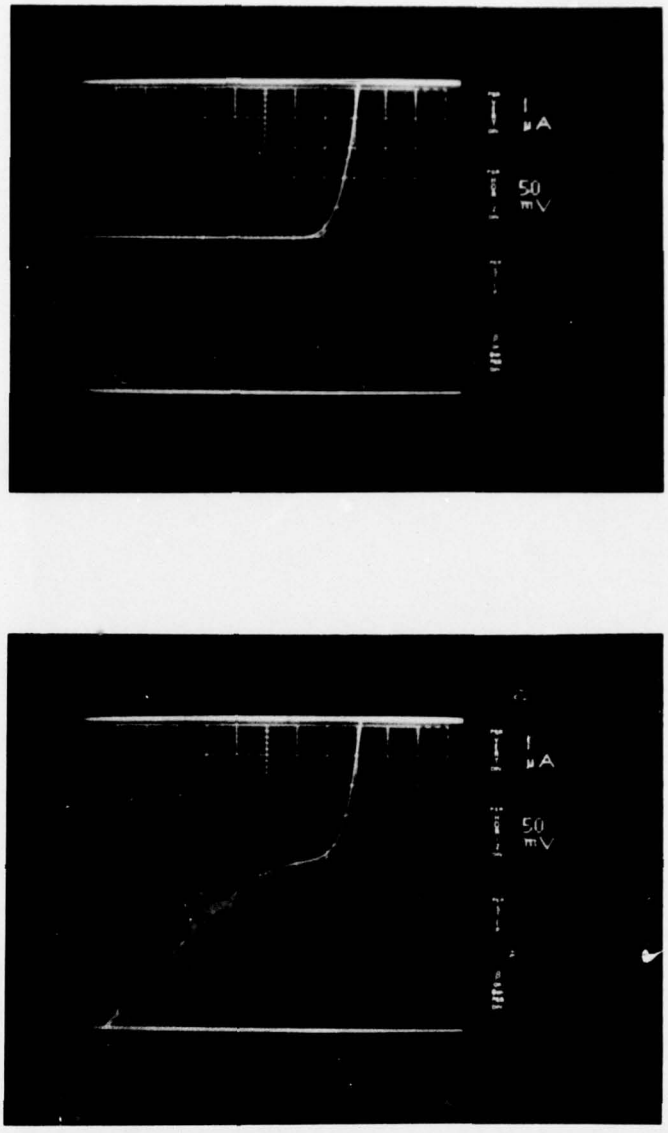



Fig. 3 The effect of gate voltage on the I-V behavior of a gold contact to n-type InSb. The gate voltages for the upper and lower curves are 0 and -16 volts, respectively. The temperature is 77 K.

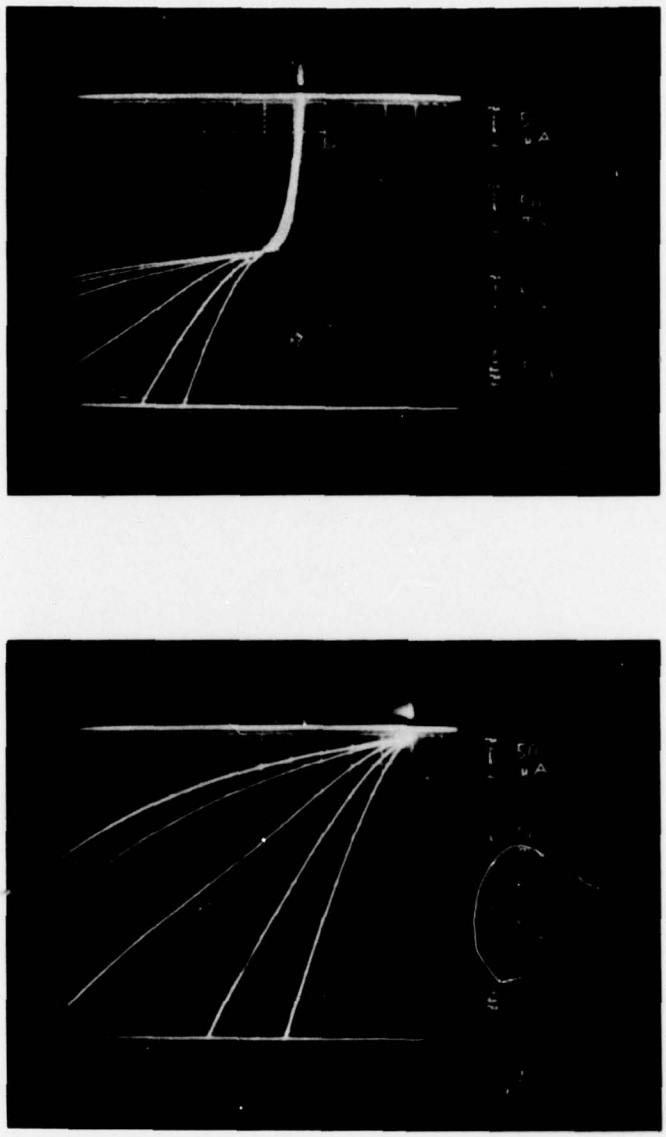


Fig. 4 The effect of gate voltage on the I-V behavior of a gold contact to p-type InSb. The increments in gate voltages are -2 volts per step. The temperature is 77 K.

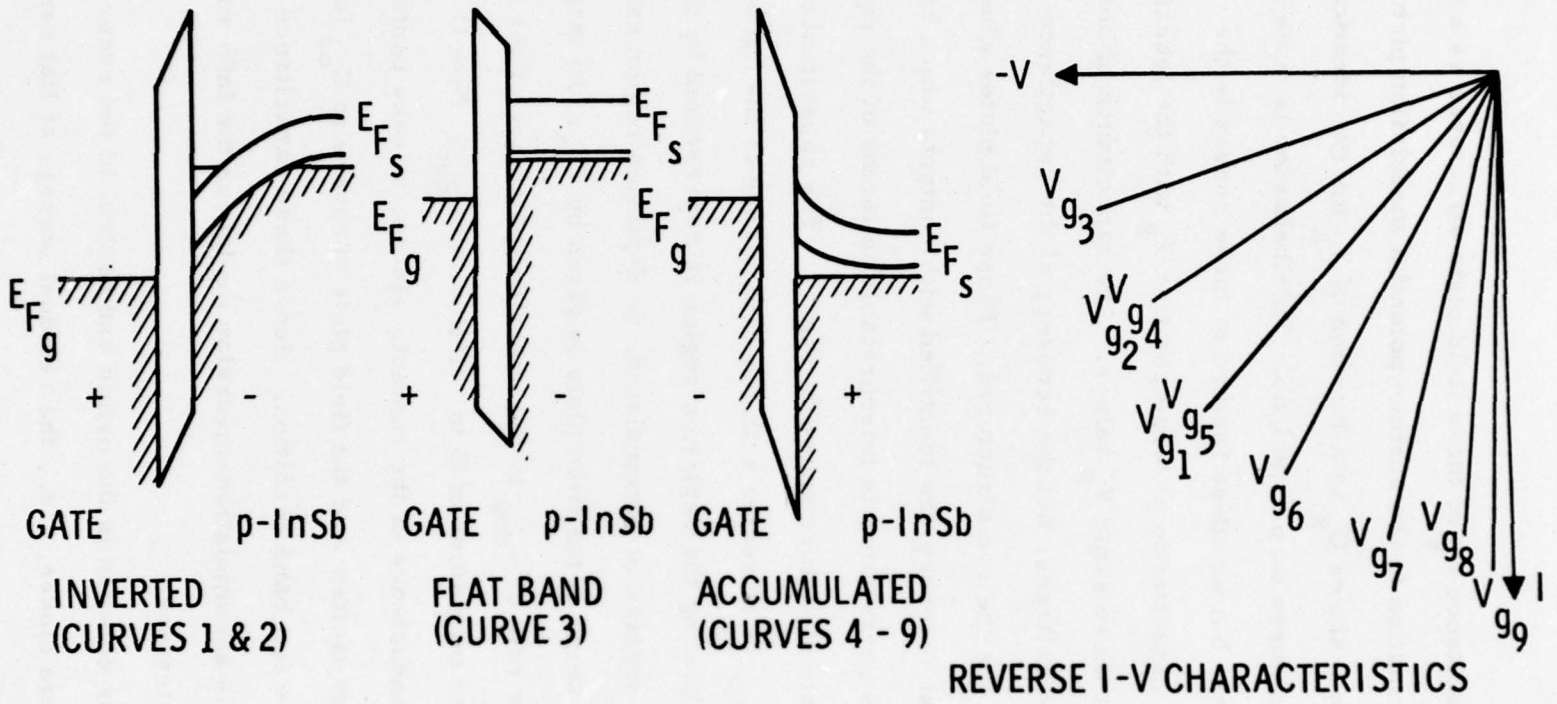



Fig. 5 A schematic illustration of the correlation between the reverse I-V characteristics and the potential energy diagram at the neighboring surface for different applied gate voltages.

The capacitance $C_g$ of these field plate structures as a function of $V_g$ adds confirmation to the surface potential modulation picture discussed above. Figure 6 shows $C_g$ as a function of $V_g$ for two identically prepared field plate structures on p-type InSb. This behavior is quite standard for MOS structures, but an added feature of these curves is the correlation of the field plate capacitance at large positive $V_g$ with the leakage behavior of the contacts at these same $V_g$ values. The capacitance of both field plates dip at flat band voltages, but the recovery of the capacitance at higher $V_g$ values differs for the two structures. Those field plates whose capacitance shows the most recovery are identified with contacts which have the most leakage. This correlation is interpretable in terms of the equivalent circuit of the field plate structure shown in Fig. 7. The capacitance of the depletion region $C_{dep}$ is in series with the capacitance of the oxide $C_{ox}$. The conductance shunting the depletion region is represented by G. At negative $V_g$ values the surface is accumulated, no depletion region exists, $G \rightarrow \infty$, and the capacitance of the field plate is given by $C_{ox}$. At large positive $V_g$ values, the role of $C_{dep}$ in the overall capacitance of the field plate is modified by the magnitude of G in relation to $\omega C_{dep}$. Now G is, in effect, the leakage conductance of the contact. Hence, a leaky contact shorts out $C_{dep}$ and the capacitance of the field plate recovers to $C_{ox}$ for $V_g$ values larger than the flat band condition. Hence these capacitance data add credance to the accumulation-inversion model for the InSb surface at the InSb - $SiO_2$ interface.

Of major concern is the origin and control of the excessive minimum leakage of these diodes, i.e., the residual leakage at flat band. This

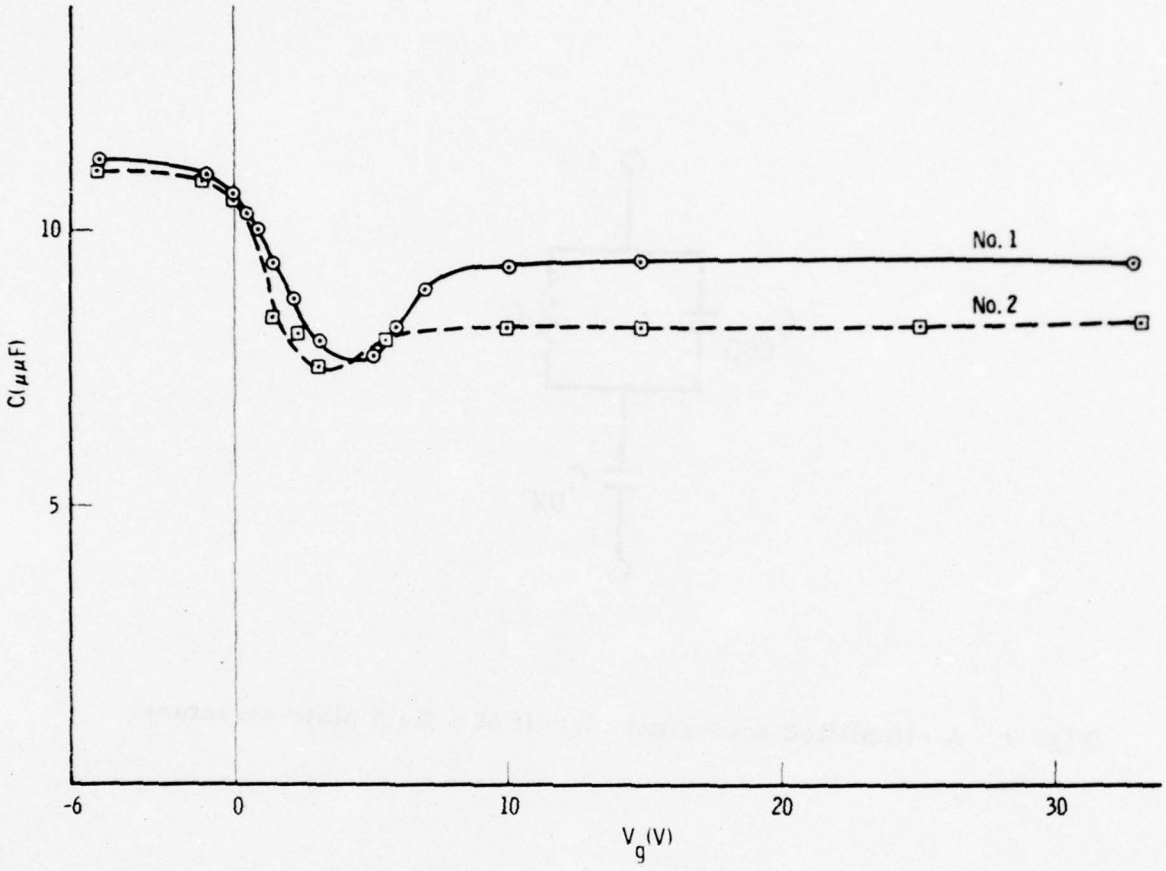



Fig. 6 The capacitance of a field plate structure as a function of plate voltage for two identically prepared structures on p-type InSb substrates. The temperature is 77 K.

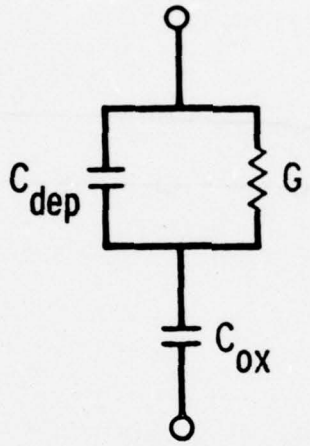



Fig. 7 A simplified equivalent circuit of a field plate structure.

leakage could be either a bulk or surface related phenomenon, or both; however, one would have to suspect it is surface related. The surfaces are nonuniform as is in evidence by the differing flat band voltages between identically prepared contacts across the same, and different, wafers. That is, patch effects could make it very difficult to bias the entire surface to a cut-off condition. Experiments are now centering on the chemistry of the InSb surface in order to both produce a more unique, uniform condition and also to reduce the leakage with chemical processing. These experiments are producing promising results, but the work is in such an early stage that it is difficult to assess their potential or significance at this time.

C. MOSFET Measurements

The MOSFET structure shown in Fig. 8 was investigaged with p-InSb to (1) add a quantitative understanding of the leakage, (2) characterize the surface currents, and (3) assess the FET device implications of the material. The family of drain-to-source voltage versus drain-to-source current with $V_g$ as a parameter is shown in Fig. 9. (These characteristics are dependent on the magnitude of applied $V_g$ and the length of time the voltage is applied due to instabilities within the oxide and at the oxide - InSb interface.) The zero bias drain-to-source conductance $G_{ds}$ as a function of $V_g$ is shown in Fig. 10. This type of operation is called the triode mode of operation as opposed to the pentode mode which is a saturated, constant current type of device. In the triode mode $G_{ds}$ is given by [10]

$$G_{ds} = \frac{\mu\epsilon}{t_{ox}} (V_g - V_{FB}) \qquad (5)$$

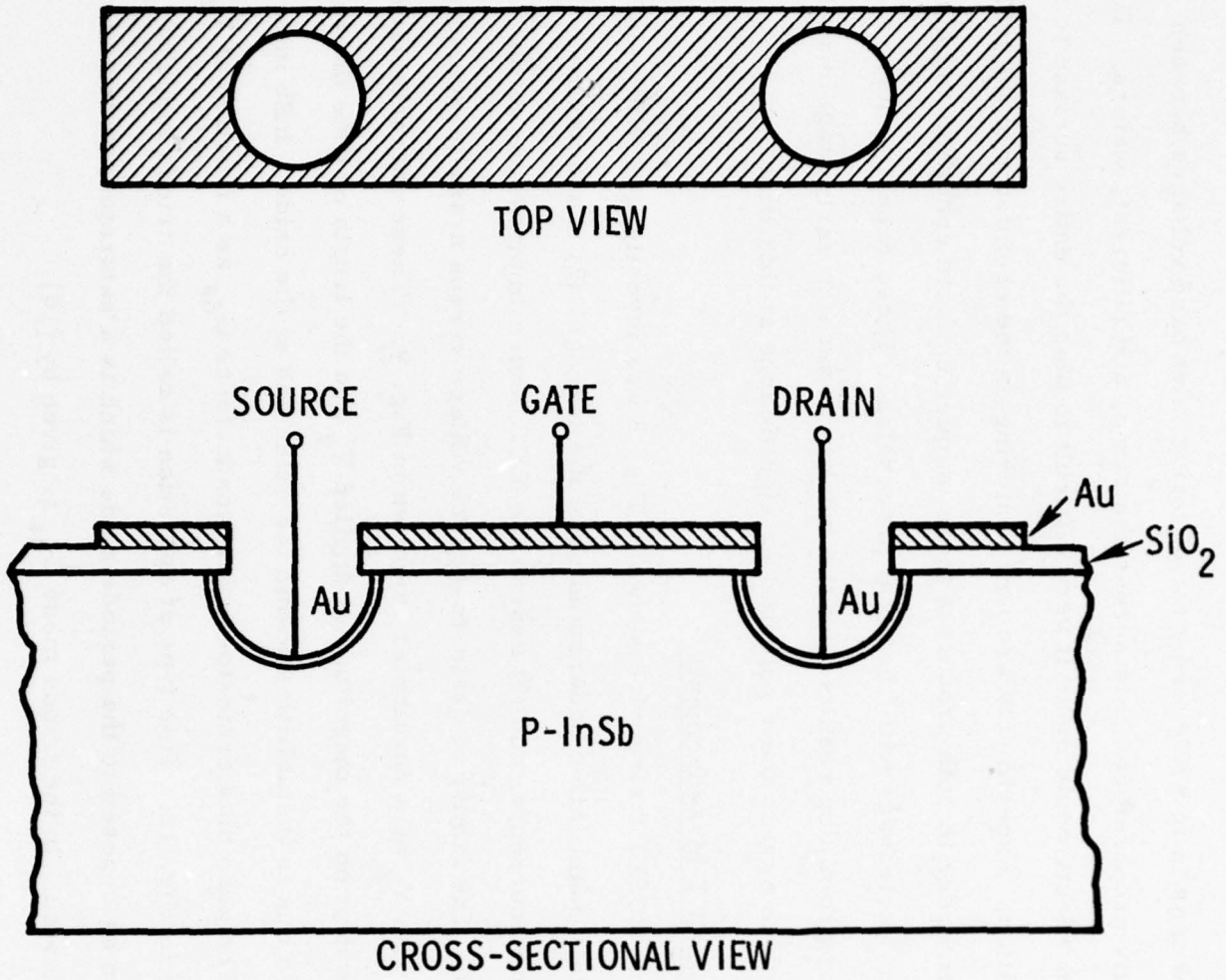



Fig. 8 The n-channel InSb MOSFET structure.

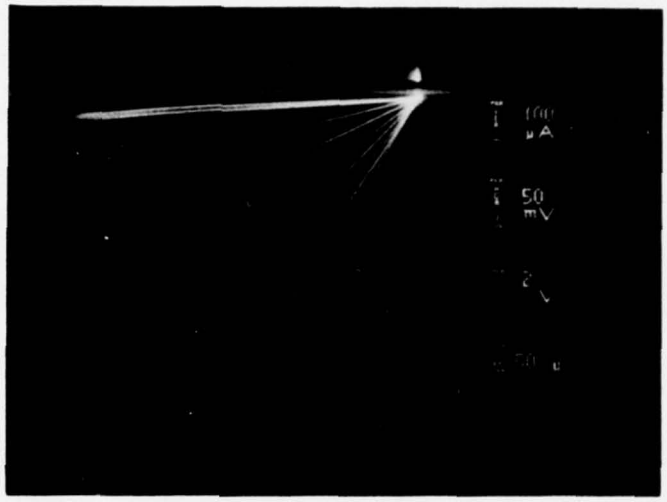



Fig. 9 The drain-to-source I-V characteristics of the n-channel InSb MOSFET with gate voltage as a parameter. The increments in gate voltage are + 2 volts per step. The temperature is 77 K.

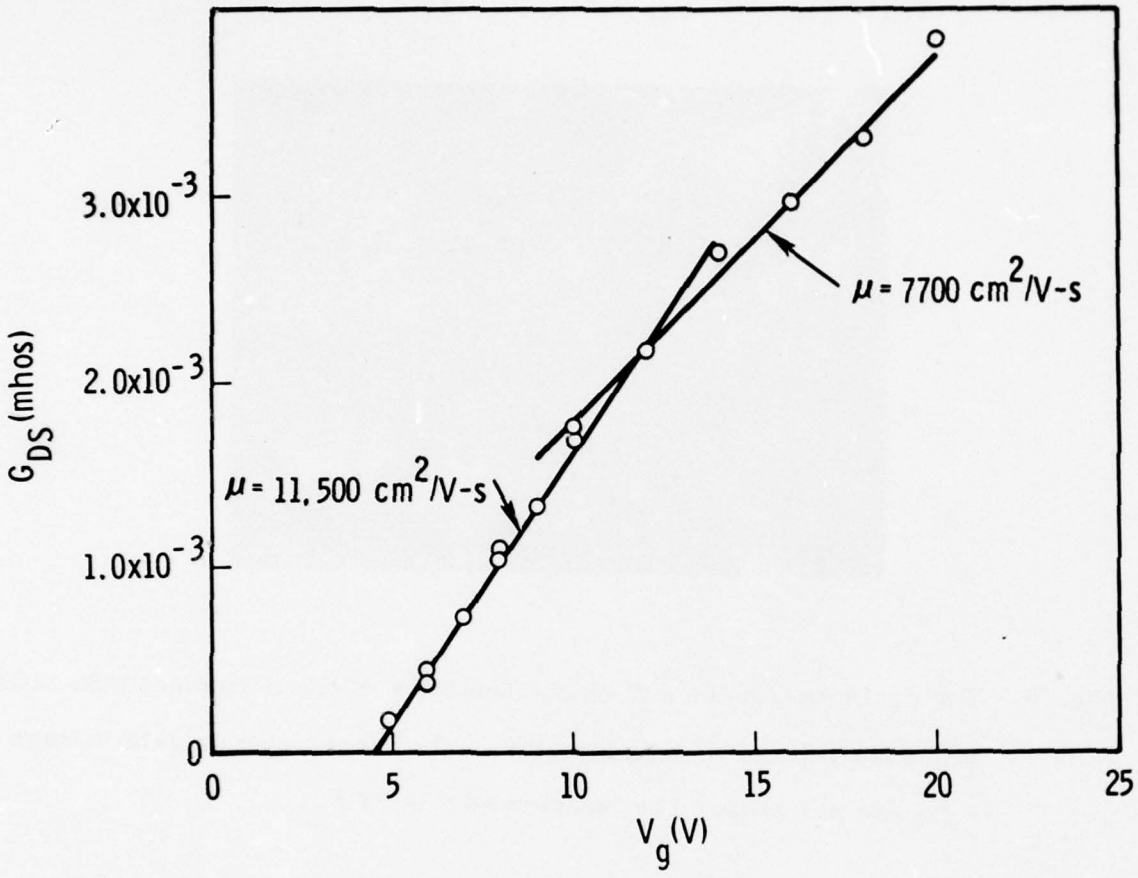



Fig. 10 The drain-to-source conductance of the n-chanel InSb MOSFET as a function of gate voltage. The slopes yield the field effect mobilities indicated. The temperature is 77 K.

where $\mu$ is the field effect mobility of the field induced carriers, $\epsilon$ is the permittivity of the oxide, $t_{ox}$ is the thickness of the oxide, and $V_{FB}$ is the flat band voltage. From Eq. (5) and Fig. 10, one calculates $\mu \approx$ 10,000 $cm^2$/V-sec. This is an exceptionally high mobility, and it would imply that the material is capable of providing a high frequency, low noise FET transistor. That is, high mobility material ensures less resistive losses associated with high frequency capacitive induced currents. A high mobility also suggests a higher cut-off frequency due to transit-time limitations for the device since high mobility carriers are faster. Another gauge as to the transit-time limitation of the material is the maximum drift velocity $v_{d,max}$ of the carriers. Here again, n-InSb appears to be an outstanding candidate. Published data for bulk n-InSb show $v_{d,max} \approx 8 \times 10^7$ cm/sec[11] which is a factor of 4 higher than that for bulk n-GaAs [12].

Clearly there are FET device possibilities with this material, Moreover, the device falls within the framework of a high frequency, low noise receiver. The main technical obstacle associated with this material would appear to be the formation of a stable oxide-InSb system. This obstacle may be solved in time by our, or other, laboratories as we pursue the super-Schottky using InSb or (InGa) Sb.

The literature is suggestive that there are several ongoing programs with InSb for FET and CCD operation [13-15], but the emphasis is entirely on p-type surfaces on n-type InSb. A possible explanation for this choice of material is that reports published in the open literature suggest that there are

fabricational difficulties with p-InSb. Foyt, et al, [16] report that it is extremely difficult to fabricate n-type regions in p-InSb by diffusion. We find n-type surfaces on p-InSb are easily field induced and coupling to this surface is a natural occurrence for most metals. The latter observation is in conflict with several published reports in the Western world on metal contacts to n-InSb [17-19], but in agreement with a less visible Russian publication [20].

D. Leakage via an inversion channel

This section correlates the surface mobility measurements with leakage measurements made on the "source" electrode of the MOSFET structure. Figure 11 illustrates the flow of leakage current from the edge of the metal contact to the inverted surface and its subsequent flow to the bulk of the semiconductor. Also illustrated in Fig. 11 is the D. C. equivalent circuit for this current flow. The leakage conductance $G_L$ (in units of mhos per cm of contact width) as measured at the contact, is given by

$$G_L = \sqrt{\frac{G_{np}}{R_\square}} \tag{6}$$

where $R_\square$ is the surface resistance of the inversion layer in ohms and $G_{np}$ is the conductance of the current flow from the n- to the p-type regions in mhos per $cm^2$. Since $R_\square^{-1}$ is proportional to the zero bias drain-to-source conductance $G_{DS}$, Eqs. (5) and (6) imply that leakage data should yield a linear plot of $G_L^2$ versus $V_g$ with a voltage intercept of $V_{FB}$. Such a linear relationship is found, as shown in Fig. 12, and, as such, adds credance to the model.

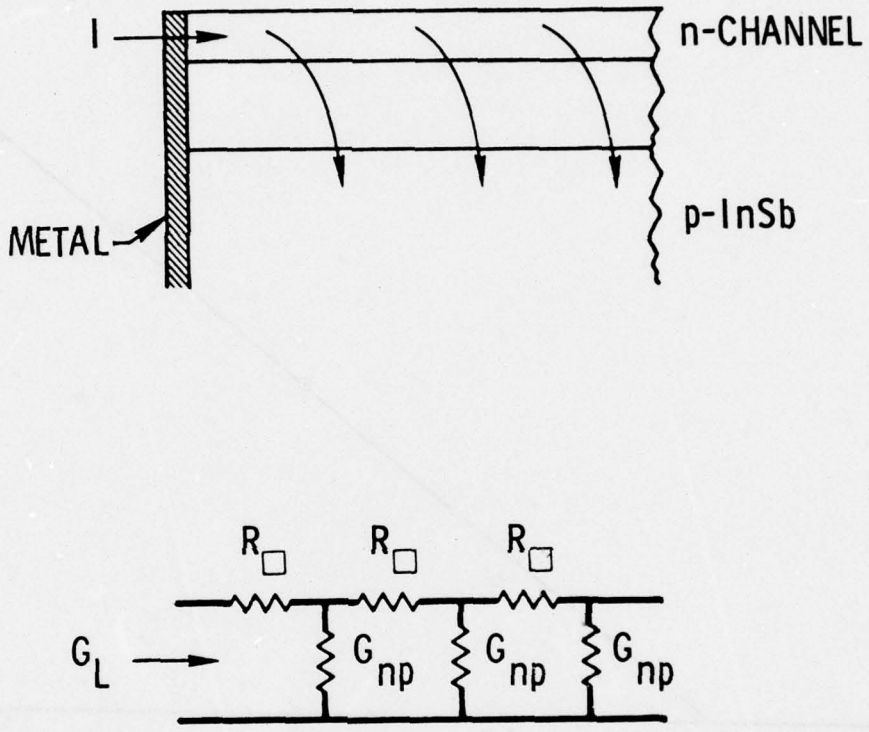



Fig. 11 A schematic illustration of the DC leakage current flow and an appropriate equivalent circuit for the leakage to an inversion channel.

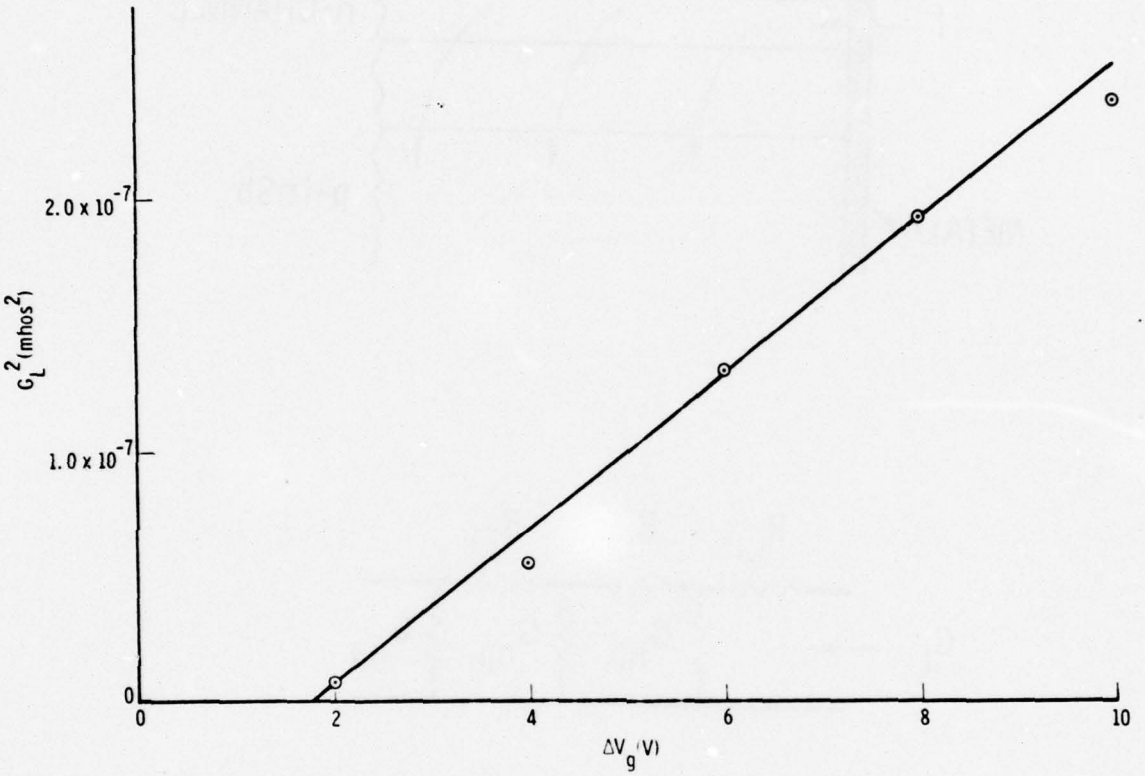



Fig. 12 The square of the leakage conductance as a function of gate voltage. The temperature is 77 K.

With the aid of Fig. 12 and Eq. (6), one calculates $G_{np} = 0.4$ mhos/cm$^2$. This value is in sharp contrast to the $4 \times 10^{-5}$ mhos/cm$^2$ measured by Kim [21] for a thermally generated n- to p-type conductance and indicates that our measured $G_{np}$ is the result of a more dominant conductance mechanism. A very probably explanation for our large $G_{np}$ is that the surface current is being drained off to the p-type substrate at the edges of the field plate. (In FET terminology, the "channel stops" in our structure are less than perfect. Channel stops are usually wide p-n junctions which block and confine the drain-to-source current to a definite channel.) Other observations have indicated that the coupling between the inversion layer and the bulk semiconductor would be strong at the edge of our field induced inversion. That is, our studies in MOSFETs with field plate structures which are not self-aligned show that (1) with no gold overplate on the $SiO_2$ an inversion layer is non-existent and (2) leakage from the source and drain contacts are large. One concludes that some surface current is being dumped to the substrate at the edges of the field plate metallization and these edges are the source of the unusually large $G_{np}$ value.

## III. THE Pb/Au/n-InSb super-SCHOTTKY DIODE

The Pb/Au/n-InSb approach is a barrier modification scheme involving the manipulation of the constituents of the metal contact. It has been determined from previous experiments at our laboratory that an insufficiently low barrier is formed with Pb (a superconductor) contacts to n-type InSb, whereas the barriers formed with Au (a non-superconductor) contacts are adequate [3]. It is also well known that thin films of Au deposited on bulk superconductors become superconducting by means of the proximity effect. Consequently, we have attempted to combine these features by introducing a thin plate of Au directly on the n-InSb followed by a thick overplate of Pb. Ideally the barrier would have the characteristic of an Au contact to n-InSb, and the Au should be superconducting.

This prediction is born out to a certain degree by the I-V plot in Fig. 13 for a Pb/Au (thin) 25 $\mu$m diameter contact on 3 x $10^{17}$ $cm^{-3}$ n-type InSb at 1 K. The nonlinearity extends out to $\approx$ 2 mV which is indicative of Pb contacts ($\Delta \approx 1.3$ mV) versus $AuPb_2$ contacts ($\Delta \approx 0.8$ mV) [22]. Hence Pb, rather than $AuPb_2$, dominates the I-V curve. What is disturbing is the lack of nonlinearity; the $g_{max}/g_{min}$ ratio is only 5 : 1. This ratio is well below what is needed for good conversion efficiencies and is possibly the result of one, or more, of the following causes:

(1) Nonuniform, and/or, porous Au plating. It may be difficult to prevent Pb from directly contacting n-InSb.

(2) Nonuniformity of the Au plate yielding regions which are too thick for the proximity effect to be effective.

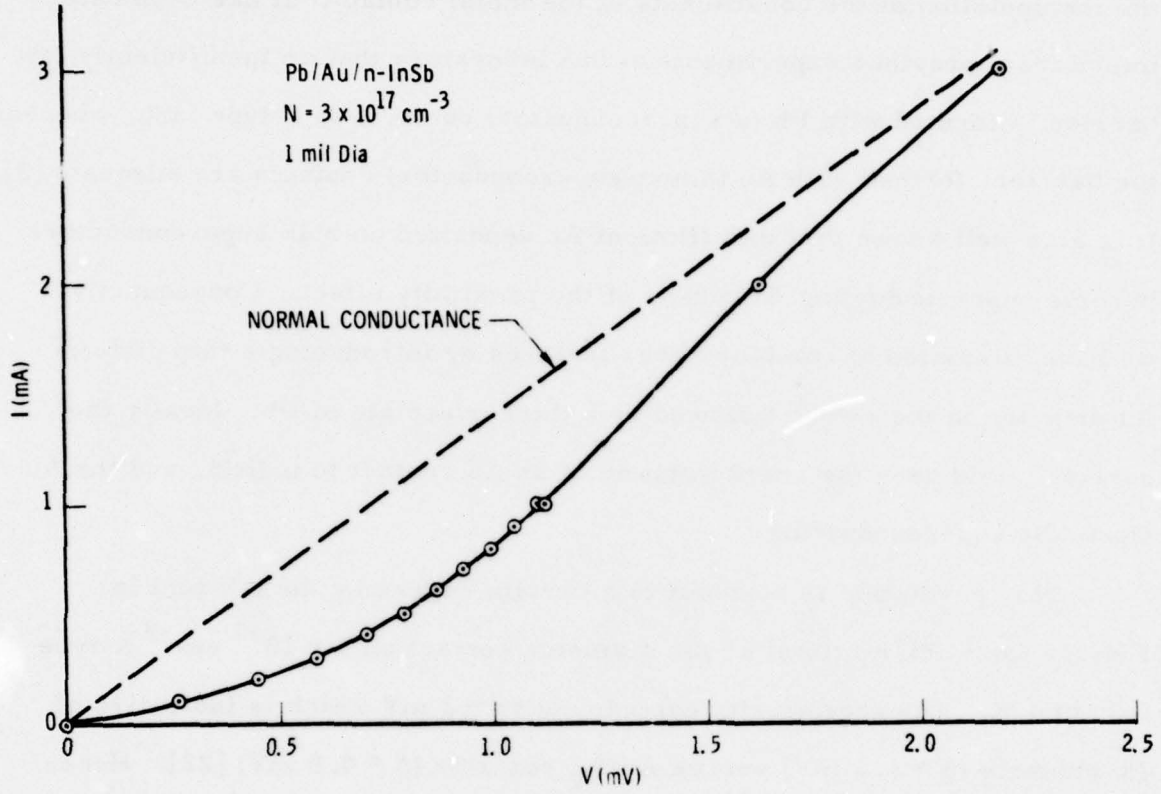



Fig. 13 The I-V characteristic of a Pb/Au/n-InSb super-Schottky at 1 K. The dashed line indicates the normal conductance of the diode.

(3) Creating of crystallites of $AuPb_2$ whose contribution to the nonlinearity would be less than that of Pb.

(4) Dominance of surface leakage.

The conductance characteristics of these junctions would suggest, however, that $3 \times 10^{18}$ $cm^{-3}$ n-InSb would be a suitable substrate if the $g_{max}/g_{min}$ difficulties can be mastered. Such a material would have mobility of 20,000 $cm^2$/V-sec and would yield an $L_1$ of 0.3 dB at 100 GHz and an $L_1$ of 2 dB at 300 GHz with a single contact structure. Incorporating a contact array structure would extend an $L_1 < 1$ dB performance well into the sub-millimeter wave region. A less porous Au film, a less leaky surface, plus other metals and barrier modifications will be sought.

## IV. THE Pb/p-InAs super-SCHOTTKY DIODE

A super-Schottky behavior has been observed for lead plated contacts on heavily doped p-InAs. These devices are unqiue in that the super-Schottky behavior is not believed to occur by direct tunneling from the superconductor to the semiconductor, as in a normal super-Schottky barrier such as Pb/p-GaAs, but from induced superconductivity in the InAs surface channel. This induced superconductivity results from the semiconductor's surface electrons being in intimate contact with the superconducting lead contact.

Metal contacts to InAs are especially interesting because the surface Fermi level is not stabilized within the forbidden band but is located above the conduction band minimum. Evaporated contacts to heavily doped p-InAs have been previously investigated [5]. These devices displayed a strong *negative resistance* in the forward direction (i.e., metal negative). It was suggested that this negative resistance is due to an atomically thin interfacial layer separating the metal from the semiconductor's surface electrons, as illustrated in the energy band diagram presented in Fig. 14a.

With these evaporated contacts, little super-Schottky behavior is observed. An evaporated lead contact at 1.4 K has less than a factor of two change in conductance for voltage comparable to the lead superconducting band gap. This effect can also be explained by the existance of a fully inverted surface and an interfacial barrier model proposed to explain the negative resistance. In this case, one does not observe the super-Schottky behavior because the surface electrons are prevented from going superconducting

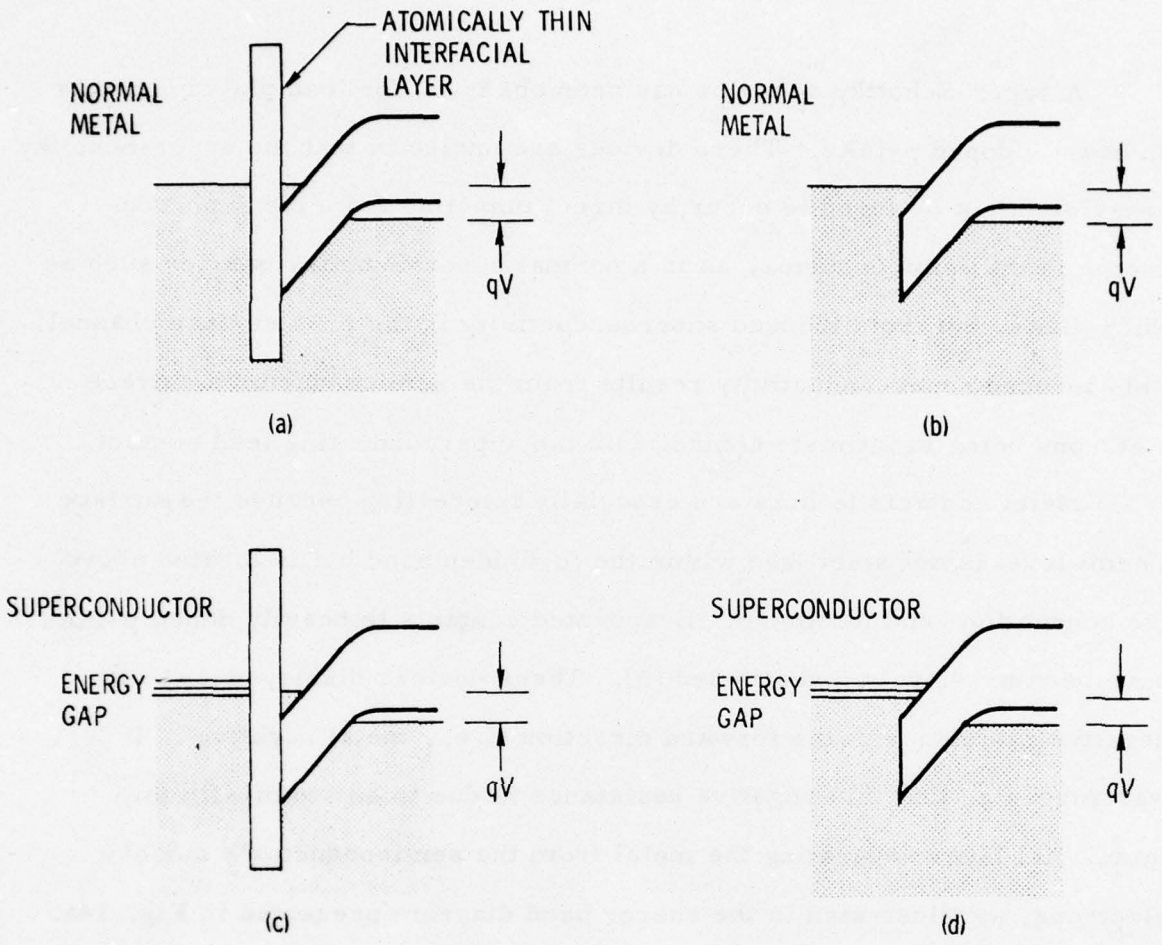



Fig. 14 The proposed energy band diagrams for evaporated and electroplated contacts on p/InAs are presented in (a) and (b), respectively. In the lower diagrams, the effect of the contact going superconducting is indicated.

because of the interfacial layer separating them from the superconducting contact. (See Fig. 14c).

Electroplated lead contacts differ from evaporated contacts in two interesting respects. A negative resistance behavior is not observed but a strong super-Schottky behavior is. Typical data are reproduced in Fig. 15. Consider the high voltage behavior first. In general the liquid nitrogen and 1.4 K curve are approximately equal, which clearly indicates tunnel emission. The decrease in the differential conductance with low forward bias indicates that these electroplated contacts produce a Full-Inversion barrier as indicated in the energy level diagram of Fig. 14b, which is identical to the energy band diagram for an evaporated contact except for the absence of an interfacial layer between the metal and semiconductor.

The absence of this interfacial layer allows the superconducting energy gap to penetrate into the inversion channel on the semiconductor as indicated in Fig. 14d, which results in the strong super-Schottky behavior at low voltage. This observation is interesting in that it not only demonstrates that super-Schottky behavior can be observed with InAs but also that semiconductor surface electrons can be made superconducting.

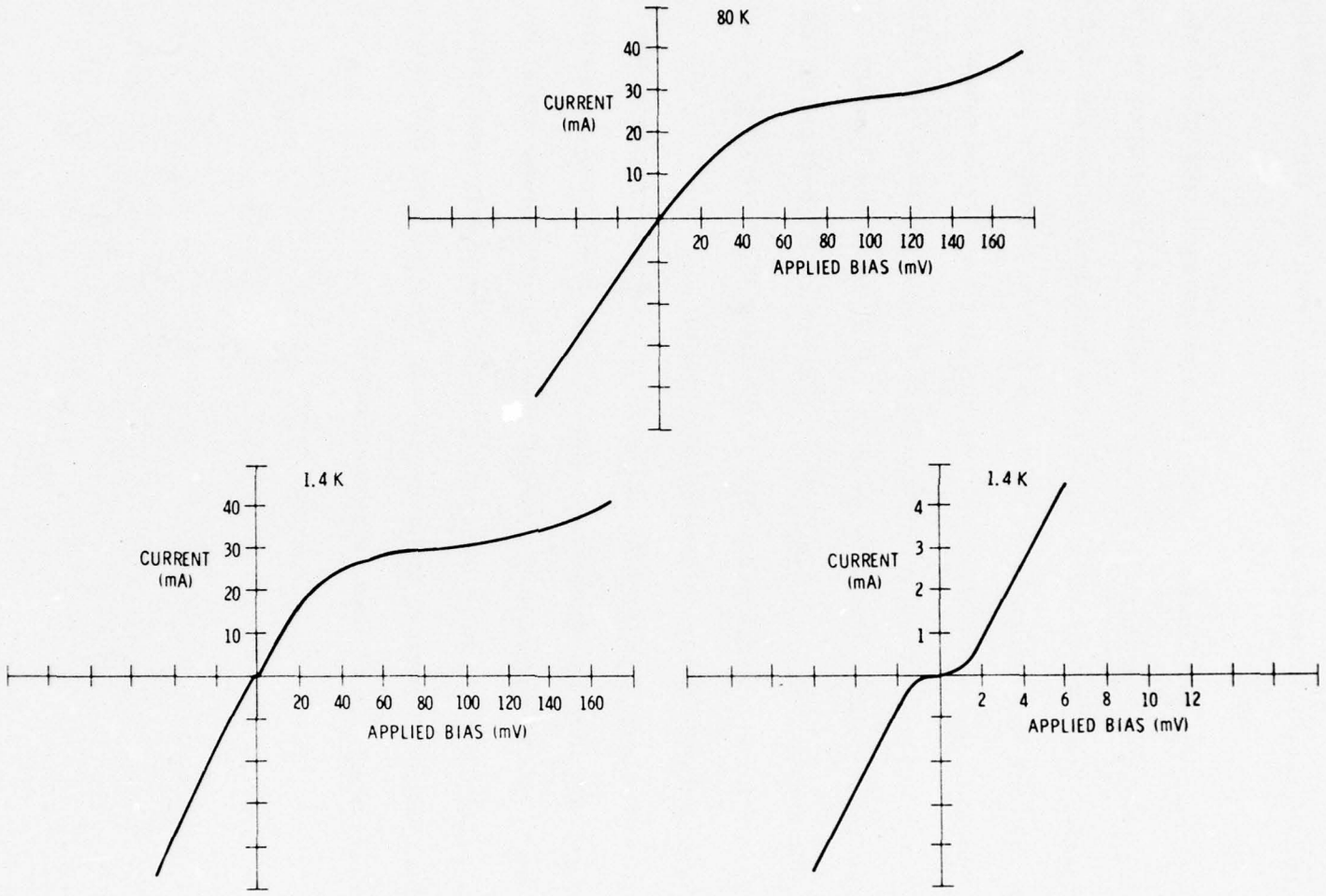



Fig. 15 The electrical behavior of an electroplated lead contact on heavily doped p/InAs (125 μm diameter)

## V. THE $In_{1-x}Ga_xSb$ SUBSTRATE

The use of the ternary material (InGa) Sb is a method to tailor the surface barrier of InSb by forming a layer of n-$In_{1-x}Ga_xSb$ on an n-InSb substrate. This material has a high mobility [6] and its barrier height should be controllable by the composition of the crystal at the surface [7]. Hence, this material should be capable of providing a suitable barrier height for a variety of superconducting metals and, simultaneously, produce a low series resistance.

Epitaxial layers of $In_{1-x}Ga_xSb$ on InSb have been grown by the sliding boat technique as developed for the growth of epitaxial GaAs [23]. We have constructed the apparatus and conducted preliminary crystal growth runs which show that the material is readily precipitated in our system. The growth solution used was an InSb saturated Ga-In melt. The first crystal growth runs yielded low quality, Ga rich crystals. While the crystals were unsatisfactory for device purposes the results show that no unsurmountable problems exist for production of materials of the composition $x = 0.12$ required for the device.

## VI. THE CONTACT ARRAY STRUCTURE

Figure 16 illustrates the proposed structure. It is constructed by fabricating the small diodes in a linear cluster and then plating the superconductor to the extent that each diode contacts its neighbors.

The contact array concept is more complex than that outlined above because the structure as a whole has parasitic elements which must be included in the analysis. Figure 17 shows the equivalent circuit with these extra parasitics included. The impedance components of each diode are $R_i$, $C_i$ and $R_{si}$. The total capacitance between the overplate and the substrate is represented by $C_{ox}$; the spreading resistance of the structure as a whole is represented by $R_{ss}$.

The circuit elements of Fig. 17 may be combined in the equivalent circuit of Fig. 18 which now replaces Fig. 1. The elements R, C, and $R_s$ represent the sum of their individual counterparts and are given by

$$R = \frac{1}{n} R_i \tag{7a}$$

$$C = n\, C_i \tag{7b}$$

$$R_s = \frac{1}{n} R_{si} \tag{7c}$$

where n is the number of individual diodes in the structure. The parasitic loss of this structure is given by

$$L_1 = 1 + \frac{R_s + R_{ss}}{R} + \omega^2 C^2 R R_s' \tag{8}$$

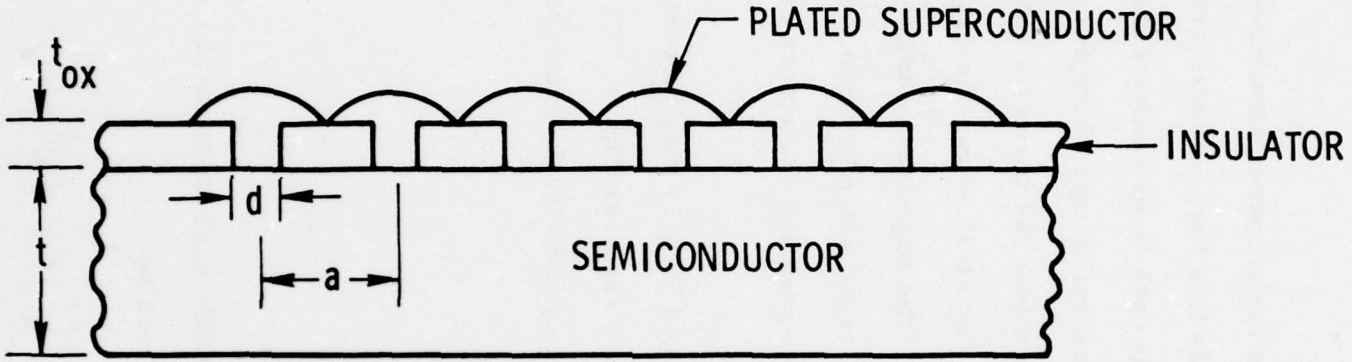



Fig. 16 Cross sectional view of the proposed contact array structure. The small diodes are fabricated in a long row (linear cluster) with the superconductor plated to the extent that each diode contacts its neighbors.

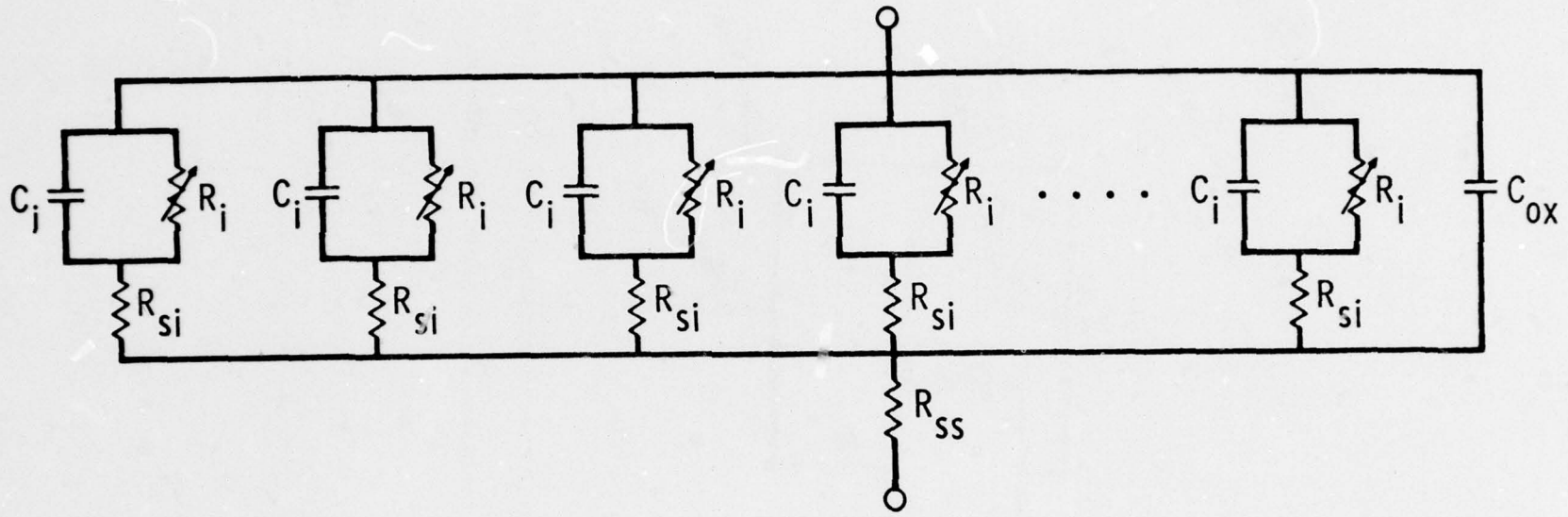



Fig. 17 Equivalent circuit of a contact array super-Schottky barrier structure.

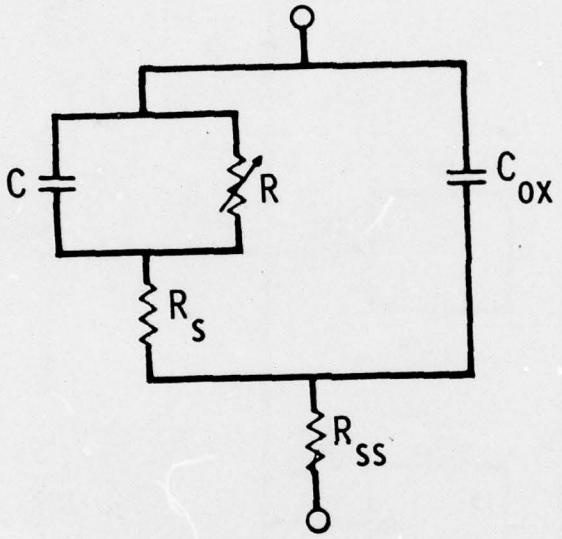



Fig. 18 The equivalent circuit obtained from Fig. 17 by combining the circuit elements of the individual diodes.

where

$$R_s' = R_s + M R_{ss} \tag{9}$$

and

$$M = \left(1 + \frac{C_{oc}}{C}\right)^2 + \frac{C_{ox}^2}{C^2} \frac{R_s}{R} \left(2 + \frac{R_s}{R} + \omega^2 C^2 R R_s\right)$$
$$M \approx \left(1 + \frac{C_{ox}}{C}\right)^2 \tag{10}$$

$R_s'$ can be regarded as the equivalent high frequency series resistance of the structure. In the design of this structure for the super-Schottky mixer, $R_s'$ is the only variable circuit element of importance. R and C are constant and the second term in Eq. 8 is negligible. Hence $R_s'$ must be evaluated and minimized.

To first order, $R_{si}$ is given by

$$R_{si} = \frac{\rho}{2d} \tag{11}$$

where d is the diameter of the small diodes. This approximation does not include the interdependence of the currents of one diode by its neighbors; however, because of the relatively large spacings that are dictated by $R_{ss}$, this approximation is not a serious one. Moreover, it can always be re-examined in the final design. From Eqs. (7c) and (11)

$$R_s = \frac{\rho}{2\ nd} \tag{12}$$

If $D_e$ is defined as the diameter of a single contact which has the same conducting area, then by equating areas, one has

$$D_e = n^{1/2}\ d \tag{13}$$

Since the conducting area remains constant, both $D_e$ and $n^{1/2}d$ remain fixed in the following analysis.

The ratio $C_{ox}/C$ can be expressed as

$$\frac{C_{ox}}{C} = K\, b^2 \tag{14}$$

where

$$K \equiv \frac{\varepsilon_{ox}}{\varepsilon_s}\ \frac{W}{t_{ox}} \tag{15}$$

$$b \equiv \frac{a}{d} \tag{16}$$

and $\varepsilon_{ox}$, $\varepsilon_s$ are the dielectric constants of the insulator and semiconductor, respectively, W is the depletion width of the barrier, a is the separation between contacts, and b is the ratio of the spacing of the diodes to their diameter.

A comment on the geometry of the cluster is in order. The choice of cluster geometry must be based on minimizing $R_s'$. Examining Eqs. 9, 10 and 14 reveals that the only cluster dependent circuit element is $R_{ss}$. ($C_{ox}/C$ is independent of cluster geometry using the overplating method of fabrication.) From purely intuitive reasoning the cluster geometry with the minimal $R_{ss}$ would appear to be a linear array.

The spreading resistance $R_{ss}$ of a linear cluster is given approximately by

$$R_{ss} = \frac{\rho \ln (4\sqrt{2}\, n)}{\pi n a}\ ;\quad n >> 1 \tag{17}$$

where na is the length of the cluster and a is both the width of the cluster and the spacing of the diodes. Equation 17 is valid for a long, thin cluster.

From Eqs. 9 - 17 one obtains

$$R_s' = \frac{\rho}{2n^{1/2} D_e} \left[1 + \frac{2(1 + Kb^2)^2}{\pi b} \ln(4\sqrt{2}\, n)\right]. \tag{18}$$

Notice $R_s' \to 0$ as $n \to \infty$. That is, with this structure both $R_s$ and $R_{ss}$ approach zero with increasing n. $R_s'$ may be optimized with respect to b to yield an optimum space-to-diameter ratio of

$$b_{opt} = \left(\frac{1}{3K}\right)^{1/2}. \tag{19}$$

This value of b results in a $C_{ox}/C$ of 1/3 or a 33% increase in the capacitance of the total diode due to the overplated metal structure. With the insulator thicknesses envisioned for this structure $b_{opt} \approx 10$.

For $b_{opt} = 10$, R = 100 ohms, $D_e = 5.7\ \mu m$, $\rho = 3.4 \times 10^{-3}$ ohm cm, and $N = 3 \times 10^{19}\ cm^{-3}$, $L_1$ is plotted in Fig. 19 as a function of n for both 35 GHz and 90 GHz. At 35 GHz with n = 400 (d = 0.3 $\mu$m), $L_1 = 1.9$ dB, and as a result, $L_c = 7.9$ dB. Increasing n to 1000 ($d \approx 0.2\ \mu m$) yields an $L_1 = 1.4$ dB, and $L_c = 7.4$ dB. This would be applicable to the p-GaAs material which has been used in our previous diodes at X-band.

A method to reduce the number of diodes, and hence increase the percentage yield of these structures, is to resort to a larger impedance. For a given size of diode, the number of diodes is inversely proportional

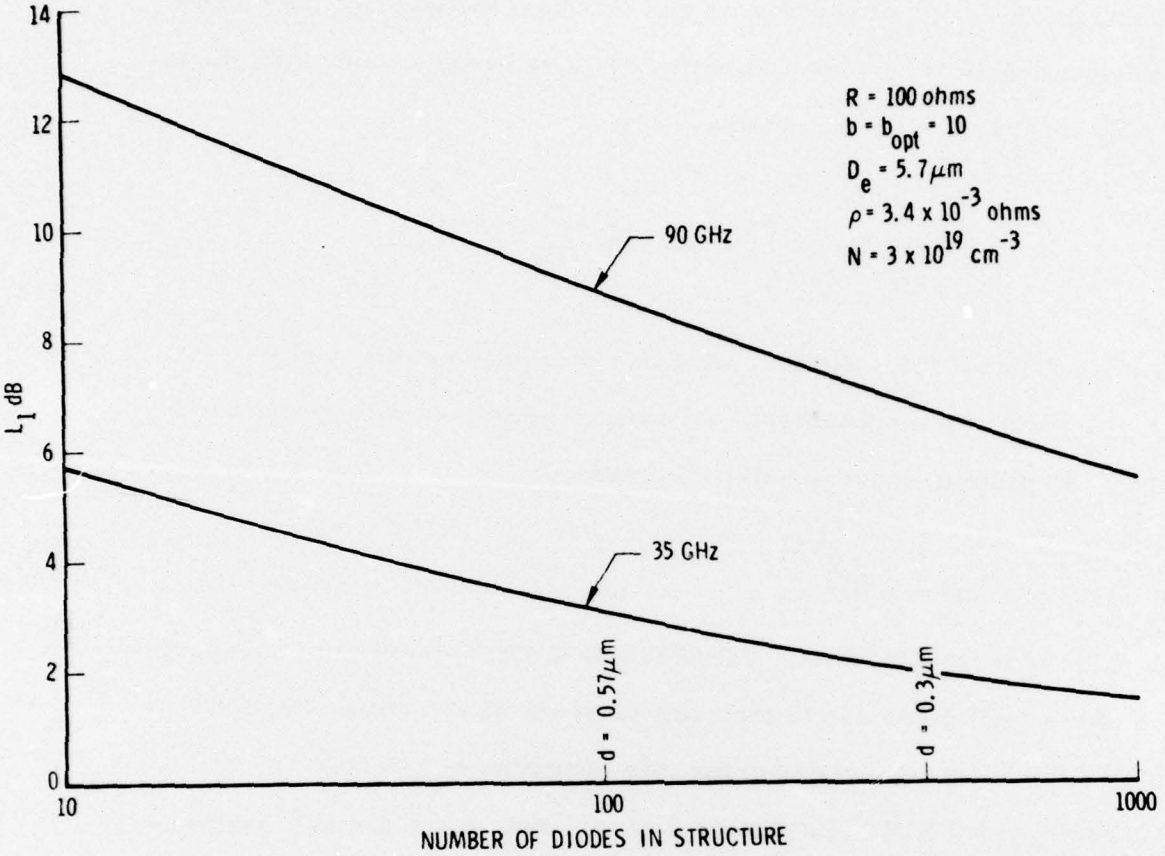



Fig. 19 Calculated parasitic loss $L_1$ of a linear contact array super-Schottky barrier structure using the parameters shown.

to impedance. An $L_c$ of 7.4 dB at 35 GHz is achievable with only 500 diodes if the impedance of the microwave circuit is increased to 200 ohms.

One extra effect must be considered in the geometric design of the cluster. With large values of n, the length of the linear cluster can become comparable to the microwave wavelength. For instance, with n = 400, one has a cluster length na of 1.2 mm which is an appreciable fraction of a quarter-wavelength at 35 GHz, and therefore, is unacceptable. However, the linear cluster can be modified slightly without significantly increasing $L_1$. Figure 20 is a sketch of a modified linear cluster which is nearly equivalent to the linear structure if the spacing between the parallel lines is larger than the thickness of the wafer.

There are also fabrication and reliability advantages with this modified linear cluster. Based on our preliminary experience in fabricating contact array structures, the percentage yield of the modified version should be higher. That is, a certain percent of the diodes will be missing in the chain. The extra paths provided by the modified version adds a needed redundancy to the structure. The structure would also have extra reliability from failures in chain integrity introduced by maltreatment, e.g., scratches introduced by the whisker.

The Aerospace Corporation is well equipped for this task because it possesses both the e-beam technology to fabricate the proposed contact array structure and the microwave instrumentation needed to assess its performance. Figure 21 shows scanning electron microscope (SEM) photographs of some preliminary linear clusters fabricated in this laboratory. The SEM, which

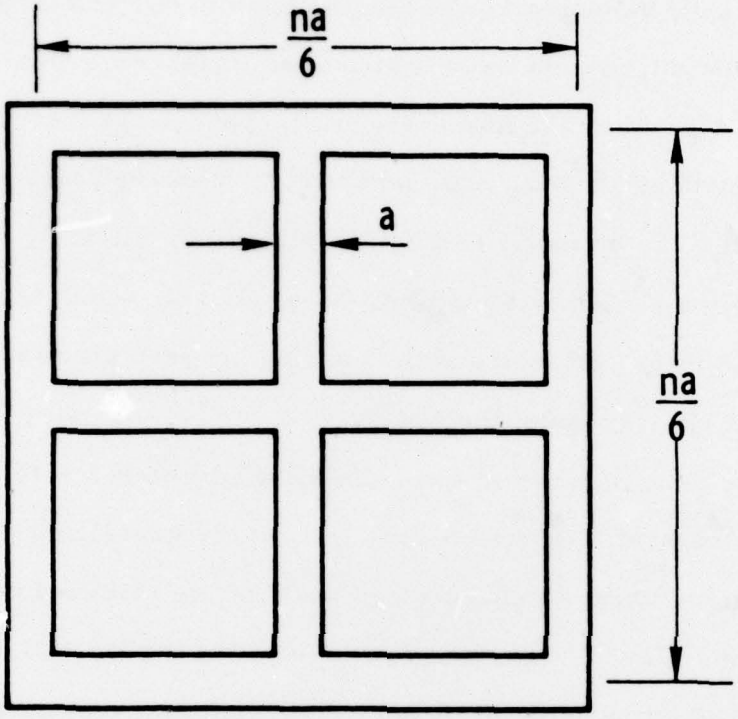



Fig. 20 A modified linear cluster.

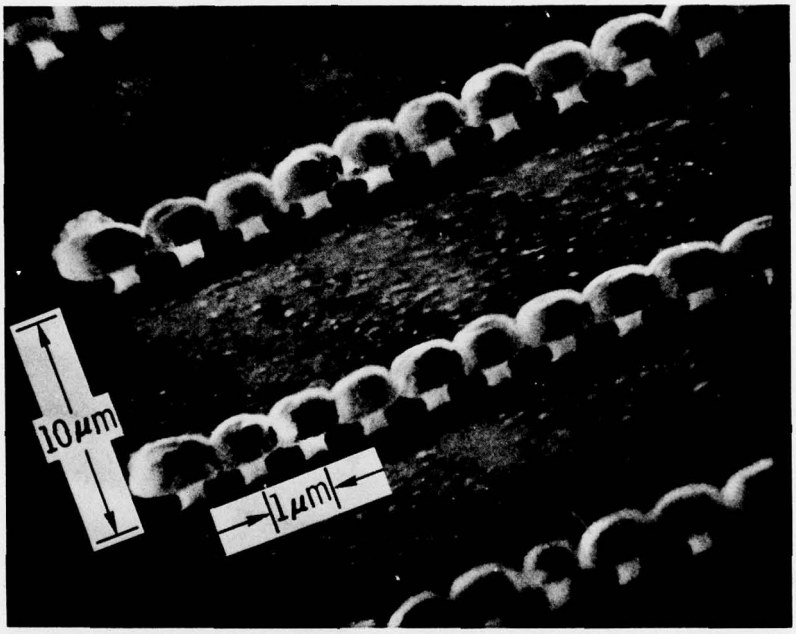



Fig. 21 SEM photographs of linear clusters.

is also involved in the exposure of the electron resist, is programmable to allow for rapid changes in design of cluster geometry, spacing, and number of diodes.

## REFERENCES


1. M. McColl, M. F. Millea, A. H. Silver, M. F. Bottjer, R. J. Pedersen, and F. L. Vernon, Jr., "The super-Schottky Microwave Mixer", 1976 Appl. Supercond. Conf. 17-20 Aug. 1976

2. F. L. Vernon, Jr., M. F. Millea, M. F. Bottjer, A. H. Silver, R. J. Pedersen, and M. McColl, "The super-Schottky Diode", to be published in IEEE Trans. Microwave Theory Tech.

3. M. McColl and M. F. Millea, "Schottky barriers on InSb", J. Electronic Mat., vol. 5, pp. 191-207, April, 1976.

4. C. A. Mead and W. G. Spitzer, "Fermi level position at semiconductor surfaces", Phys. Rev. Lett., vol. 10, pp. 471-472, 1 June 1963.

5. M. F. Millea, M. McColl, and A. H. Silver, "Electrical characterization of metal/InAs contacts", J. of Electronic Mat., vol. 5, pp. 321-340, June 1976.

6. H. Miki, K. Segawa, M. Otsubo, K. Shirahata, and K. Fujibayashi, "Growth of $In_{1-x}Ga_x$ Sb by liquid phase epitaxy," Proc. 5th Int. Symp. Gallium Arsenide and Related Compounds, 1974, London and Bristol: Institute of Physics, 1975, pp. 16-21.

7. K. Kajiyama, Y. Miyushima, and S. Sakata, "Schottky barrier height of n-$In_xGa_{1-x}$ As diodes," Appl. Phys. Lett., vol. 23, pp. 458-459, 15 Oct. 1973.

8. H. C. Torrey and C. A. Whitmer, Crystal Rectifiers (M.I.T. Radiation Lab. Ser., vol. 15), New York: McGraw-Hill, 1948, p. 248.

9. H. M. Day, A. C. MacPherson, and E. E. Bradshaw, "Multiple contact Schottky barrier microwave diode", Proc. IEEE, vol. 54, pp. 1955-1956, Dec. 1966.

10. R. S. G. Cobbold, The Theory and Application of Field-Effect Transistors, New York: Wiley, 1970.

11. M. Glicksman and W. A. Hicinbothem, Jr., "Hot electrons in indium antimonide", Phys. Rev., vol. 129, pp. 1572-1577, Feb. 15, 1963.

12. S. M. Sze, Physics of Semiconductor Devices, New York: Wiley, 1969, p. 747.

13. J. Shapper, S. Margalet, and I. Kidron, "p-channel MOS transistor in indium antimonide", IEEE Trans. Electron Devices, vol. ED-22, pp. 960-961, Oct. 1975.

14. J. C. Kim, "InSb MIS technology and CID devices", Proceedings of 1975 International Conf. on the Application of Charge-coupled Devices, pp. 1 - 17, Oct. 1975.

15. R. D. Thom, R. E. Eck, J. D. Phillips and J. B. Scorso, "InSb CCDs and other MIS devices for infrared applications," Proceedings of 1975 International Conf. on the Application of Charge-Coupled Devices, pp. 31-42, Oct. 1975.

16. A. G. Foyt, W. T. Lindley, and J. P. Donnelly, "n-p junction photodetectors in InSb fabricated by proton bombardment", Appl. Phys. Lett. vol. 16, pp. 335-337, May 1970.

17. C. A. Mead and W. G. Spitzer, "Fermi level position at metal-semiconductor interfaces," Phys. Rev., vol. 134, pp. A713-A716, May 1964.

18. B. C. Cavenett, "Electron-phonon interacting in InSb junctions", Phys. Rev. B, vol. 5, pp. 3049-3057, April 1972.

19. A. S. Volkov, Yu A. Goldberg, D. N. Nasledov, N. G. Neronova, and B. A. Saimkulov, "Surface-barrier diodes based on InSb," Sov. Phys. - Semicond., vol. 5, pp. 1987-1990, June 1973.

20. M. L. Korwin-Pawlowski and E. H. Hessell, "Metal-InSb surface barriers", Metal Semiconductor Contacts, M. Pepper, Ed., The Institute of Physics, London (1974), pp. 255-262; Solid St. Electron., vol. 18, p. 849 (1975).

21. J. C. Kim, "Infrared detector mosaic development", Technical Report AFAL-TR-73-352, Air Force Avionics Laboratory, Sept. 1973.

22. M. F. Gendron and R. E. Jones "Superconductivity in the $CuAl_2$ (C16) crystal class", J. Phys. Chem. Solids, vol. 23, pp. 405-406, 1962.

23. A. Joullie, R. Aulcombard, and C. Bougnet, "Growth of $Ga_xIn_{1-x}Sb$ phase capitaxial layers from a knowledge of the ternary phase diagram", Journ. of Crystal Growth, vols. 24/25, pp. 276-281, 1974.

## THE IVAN A. GETTING LABORATORIES

The Laboratory Operations of The Aerospace Corporation is conducting experimental and theoretical investigations necessary for the evaluation and application of scientific advances to new military concepts and systems. Versatility and flexibility have been developed to a high degree by the laboratory personnel in dealing with the many problems encountered in the nation's rapidly developing space and missile systems. Expertise in the latest scientific developments is vital to the accomplishment of tasks related to these problems. The laboratories that contribute to this research are:

Aerophysics Laboratory: Launch and reentry aerodynamics, heat transfer, reentry physics, chemical kinetics, structural mechanics, flight dynamics, atmospheric pollution, and high-power gas lasers.

Chemistry and Physics Laboratory: Atmospheric reactions and atmospheric optics, chemical reactions in polluted atmospheres, chemical reactions of excited species in rocket plumes, chemical thermodynamics, plasma and laser-induced reactions, laser chemistry, propulsion chemistry, space vacuum and radiation effects on materials, lubrication and surface phenomena, photosensitive materials and sensors, high precision laser ranging, and the application of physics and chemistry to problems of law enforcement and biomedicine.

Electronics Research Laboratory: Electromagnetic theory, devices, and propagation phenomena, including plasma electromagnetics; quantum electronics, lasers, and electro-optics; communication sciences, applied electronics, semiconducting, superconducting, and crystal device physics, optical and acoustical imaging; atmospheric pollution; millimeter wave and far-infrared technology.

Materials Sciences Laboratory: Development of new materials; metal matrix composites and new forms of carbon; test and evaluation of graphite and ceramics in reentry; spacecraft materials and electronic components in nuclear weapons environment; application of fracture mechanics to stress corrosion and fatigue-induced fractures in structural metals.

Space Sciences Laboratory: Atmospheric and ionospheric physics, radiation from the atmosphere, density and composition of the atmosphere, aurorae and airglow; magnetospheric physics, cosmic rays, generation and propagation of plasma waves in the magnetosphere; solar physics, studies of solar magnetic fields; space astronomy, x-ray astronomy; the effects of nuclear explosions, magnetic storms, and solar activity on the earth's atmosphere, ionosphere, and magnetosphere; the effects of optical, electromagnetic, and particulate radiations in space on space systems.

THE AEROSPACE CORPORATION
El Segundo, California

• • •