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PORTABLE UNIVERSAL PULSER (PUP) OPERATING MANUAL.(U)
AUG 77 D C KOLLER, R A HAYS
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PORTABLE UNIVERSAL PULSER (PUP) OPERATING MANUAL

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August 1977

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Final Report

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AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
Kirtland Air Force Base, NM 87117

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Richard A. Hays

RICHARD A. HAYS
Project Officer

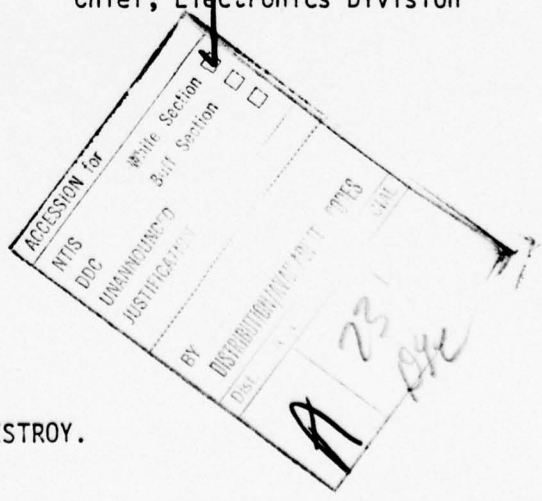
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This report represents the results of the complete development of a portable direct drive pulser system. Though fabricated for a specific application (EMP Direct Drive Test of the 1200 kVA Power System for the E-4), the pulser system in a modular configuration allows great flexibility through simple hardware changes. Presently configured for 12 Damped Sine Wave frequencies at a fixed Q of 24, the two output amplifiers can be driven series push-pull for high voltage (>1500 volts) or in parallel for high current

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20. ABSTRACT

(>20 amperes) output. Burst cw and cw at the 12 preselected frequencies are available without additional modification. Presently available are 10 kHz, 20 kHz, 50 kHz, 100 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz, 10 MHz, 30 MHz, 50 MHz, and 100 MHz. Other waveforms can be amplified for direct drive given an external low level source.

PREFACE

This document is the final report on the development of a versatile direct drive pulser system. With continuing requirements for a portable system which could be brought to the site of large or complicated test items, the Portable Universal Pulser (PUP) was conceived and brought to a conclusion in an attempt to meet existing needs with flexibility for future modification.

The authors wish to thank Mr. Lorin Black and Sgt Mike Harris of the Air Force Weapons Laboratory (AFWL) for their assistance in the construction and verification phase. This effort was supported through funds provided by the Airborne Command Post Project Office specifically for the electromagnetic pulse direct drive testing of the 1200 kVA power system.

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SECTION I

PULSER CHARACTERISTICS

The Portable Universal Pulser (PUP) is a portable pulsing system designed around the concept of generating the desired pulse shape at low power levels and amplifying with wide band linear amplifiers to the desired power level. This concept allows an almost infinite range of output pulse shapes and power levels within the ratings of the amplifiers.

PUP (figure 1) consists of two mating rack cabinets together with an external

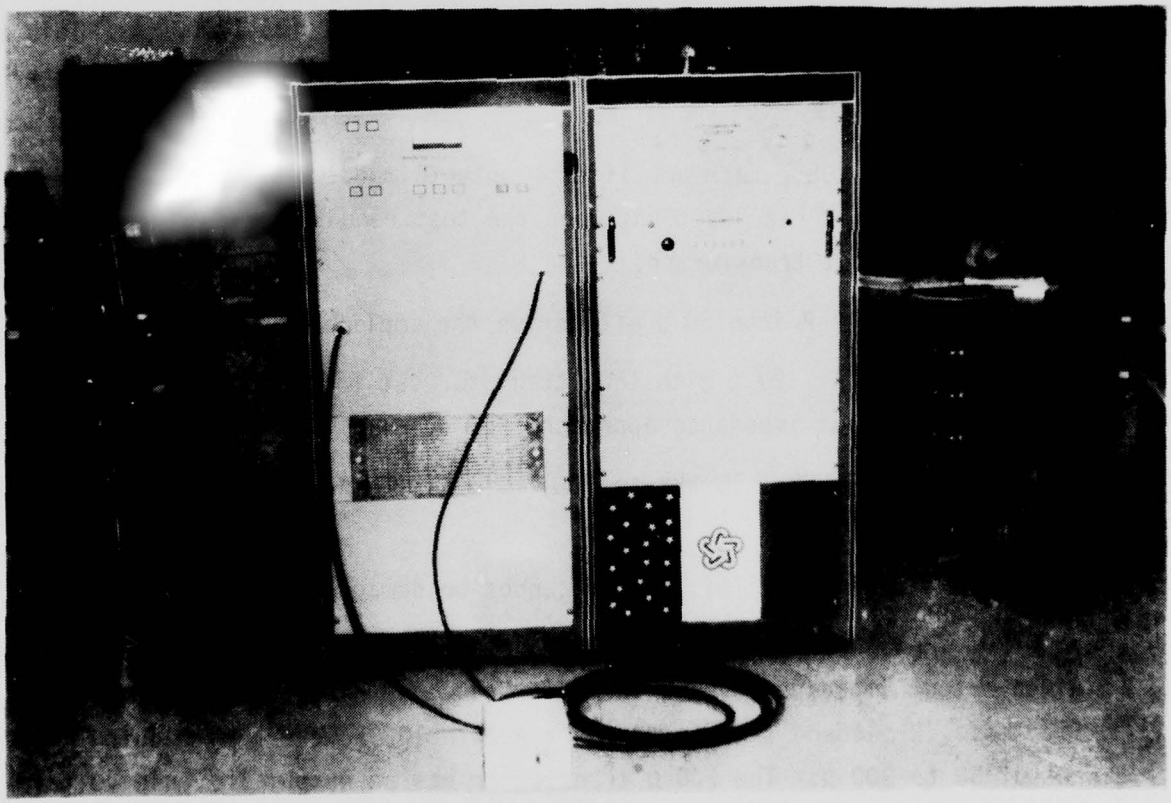


Figure 1. Portable Universal Pulser (PUP)

output transformer assembly. Within the rack cabinets are the amplifying system, power supplies, and a signal source which presently generates damped-sine pulses.

The amplifying system (figure 2) consists of a preamplifier which feeds a driver amplifier. This driver feeds a transformer which drives two power amplifiers in push-pull. Each of the power amplifiers feeds an output jack on PUP's front panel. Each of these outputs is coupled by cable to an output transformer which is usually located close to the test point being pulsed. This output transformer recombines the signals from the two power amplifiers and is designed to provide the desired Thevenin output impedance for the test.

An attenuator built into the preamplifier is used to adjust the output signal amplitude.

AMPLIFIER SPECIFICATIONS:

OUTPUT POWER: (1) 2000W Pulsed. This is measured with each of the power amplifiers working into its own individual 50 Ω load. (2) 1000W cw. This is measured with one of the power amplifiers operating into 50 Ω and the other amplifier biased off.

OUTPUT IMPEDANCE: Each amplifier's output impedance is 100 Ω. The output impedance of PUP is dependent upon the test requirements and is determined by the output transformer.

GAIN: 750 mV P-P into 50 Ω will drive the amplifiers to full power out.

INPUT IMPEDANCE: 90 Ω with the attenuator set to 0 dB. As attenuation is increased, the input impedance approaches 50 Ω.

FREQUENCY RESPONSE: 10 kHz to 200 MHz ± 2 dB. This does not include the output transformer.

MISMATCH TOLERANCE: This system cannot be damaged operating into any load.

OUTPUT TRANSFORMERS: The output transformer is normally designed to provide a given output impedance over a specific frequency range as required for a specific test. Broadband transformers are available, however, with output impedances of 50 to 200 Ω. The 200 Ω transformer has an output Thevenin voltage capability in excess of 1740 V peak.

DAMPED SINE GENERATOR CHARACTERISTICS:

FREQUENCIES: 10 kHz, 20 kHz, 50 kHz, 100 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz, 10 MHz, 30 MHz, 50 MHz, and 100 Mhz.

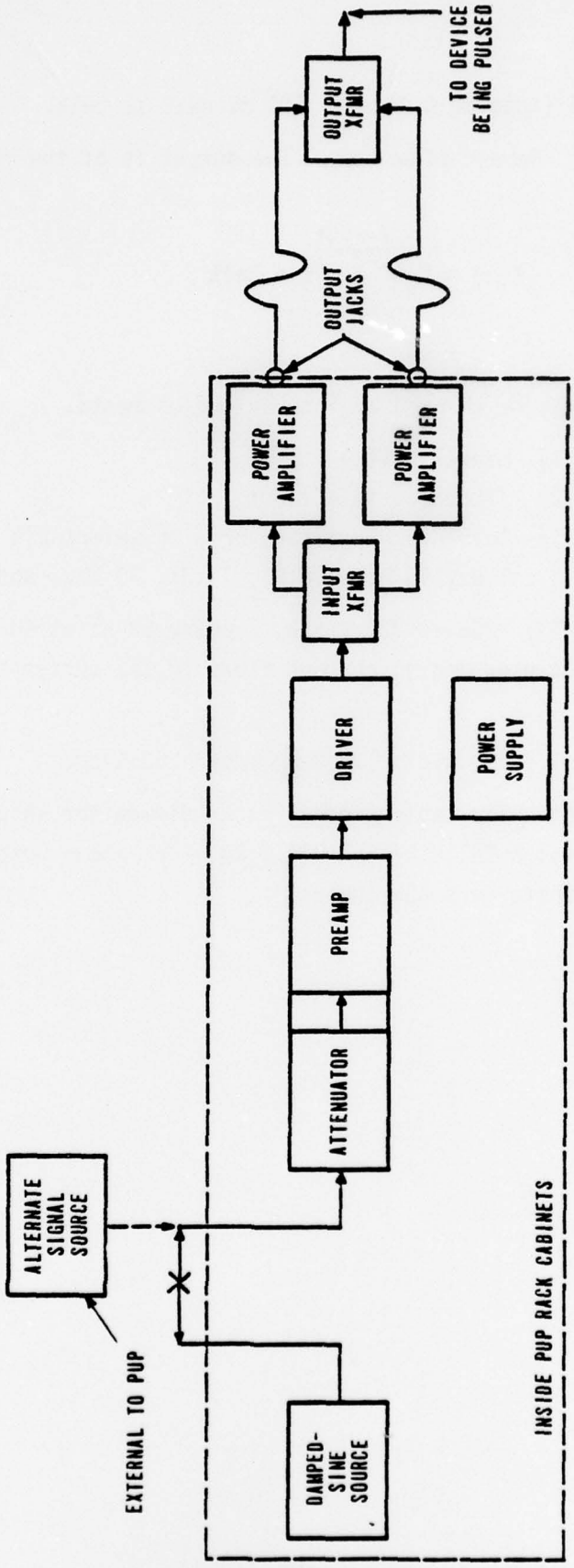


Figure 2. System Block Diagram

OUTPUT AMPLITUDE (into 50 Ω load): 750 mV peak to peak.

OUTPUT WAVEFORM: Damped sine wave. The output is of the form

$$\ell(t) = E_0 \ell^{\left(\frac{-\pi ft}{Q}\right)} \sin 2\pi ft$$

with $Q = 24$

The value of Q may be changed by internal adjustments.

FIRING MODES: (1) Manual switch
(2) TTL compatible input
(3) Internal PRF generator with selectable rates of 1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz, and 100 kHz.

POWER REQUIREMENTS: 208 to 230 V a.c. 3 phase 60 Hz at 40 amps. The power system neutral is not used and no current flows in the system's "equipment ground."

SIZE: Height 151.4 cm, width 137.2 cm, depth 63.5 cm.

WEIGHT: 459.5 kg. The two equipment racks divide for shipping purposes. The separate racks weigh 241.8 kg and 217.7 kg. The above weights do not include the output transformers and cables.

SECTION II

AMPLIFIER CONTROLS

The Portable Universal Pulser (PUP) amplifier controls are indicated below with their respective function.

OFF, ON (pushbutton with lamps).

The "OFF" pushbutton illuminated indicates:

1. The power cord is connected to line power.
2. All power within the system is off with the exception of a small control transformer.

Pushing "ON" supplies power to the cooling blower. Closure of the airflow switch supplies power to the control circuits, tube heaters, and IFI 5000 preamplifier.

Pushing "OFF" from the on state will remove power from the entire unit with the exception of the blower which will remain operating for approximately 30 seconds and shut down automatically (see Blower Overrun).

C - A - U - T - I - O - N

The shutdown of the unit must be accomplished by the "OFF" pushbutton to prevent tube hot spots. Any other means of shutdown will circumvent the blower overrun feature.

BLOWER OVERRUN: (lamp only)

This lamp indicates the approximately 30 second blower operation after the "OFF" button has been pushed disconnecting power to the amplifiers.

FILAMENTS ON: (lamp only)

Indicates airflow switch closure and power is applied to tube heaters.

WAIT: (lamp only)

"WAIT" lights when power is applied to control circuits. It indicates that tube cathode warmup is in progress.

STANDBY: (pushbutton and lamp)

"STANDBY" lighting indicates that the tube heater delay has timed out and the control logic is in the standby state. Plate voltage is off but ready to be turned on if all interlocks and overloads are satisfied. If unit is in the operate state pushing "STANDBY" will return the unit to the standby state turning off plate voltage.

OPERATE: (pushbutton and lamp)

Pushing "OPERATE" places the control logic in the operate state and applies plate voltage to the power amplifiers. The lamp indicates this status.

LAMP TEST: (pushbutton and lamp)

Pushing "LAMP TEST" lights all panel lamps, including itself, on the amplifier control panel.

INTERLOCK OPEN: (lamp only)

"INTERLOCK OPEN" indicates one or more safety interlocks are open. This condition inhibits the OPERATE command.

OVERLOAD PRESS TO RESET: (pushbutton and lamp)

"OVERLOAD" indicates one of the following has occurred:

1. Excess plate or screen current in any power amplifier.
2. Excess current in the primary of the plate transformer.
3. Incorrect bias supply voltage.
4. Insufficient tube bias.

Any of the above overloads will return the system to the standby state. The system will remain in this state until the overload is corrected and reset by pushing the "OVERLOAD" button.

AMP A
BIAS ON: (lamp)

AMP B
BIAS ON: (lamp)

The lighting of either or both lamps indicates that the bias on their respective power amplifier (PA) will allow plate current to flow. The system is

now ready to accept an input with resultant delivery of energy to the output. When these lamps are off, the power amplifiers are biased to cutoff.

MODE SWITCH: (3 position rotary)

Position 1: Normal
Position 2: Test-CW AMP A
Position 3: Test-CW AMP B

NORMAL

When the system is in the operate state, plate voltage is applied to all amplifiers and plate current flows in the driver and both intermediate power amplifiers (PA). The bias on the power amplifiers is obtained from a pulsed source which normally maintains the tubes in cutoff. In the "NORMAL" position both amplifiers are controlled in parallel. When a bias-on command is received, both amplifiers are biased on momentarily together.

TEST-CW AMP A

When the system is in the operate state, this position continuously biases power amplifier A on and biases power amplifier B off. It is useful for monitoring operating conditions such as plate current of amplifier A or cw applications involving 1/2 power (1 kW) output.

TEST-CW AMP B

This is the same as position 2 above except that amplifier B is biased on and amplifier A is biased off.

METERING SWITCH: (12 position rotary)

This switch is used to monitor plate and screen voltages and currents in the 5 power amplifiers (Driver, IPA-A, IPA-B, PA-A, and PA-B). Observation is made with the system in the operate state, and the mode switch in either "TEST-CW AMP A" or "TEST-CW AMP B" depending on which amplifier it is desired to monitor.

TYPICAL (NOMINAL) VALUES ARE AS FOLLOWS:

E_{BB}	Plate Voltage PA	780 V	
E_{BB}	Plate Voltage Driver & IPA	450 V	
E_{SG}	Screen Voltage All Amplifiers	350 V	
I_B	Plate Current Dirver & IPA	2.5 AMP	
I_B	Plate Current PA	7.2 AMP	
I_{SG}	Screen Current Driver & IPA	less than 200 mA	(Screen current may be positive or negative; meter will read upscale in either case.)
I_{SG}	Screen Current PA	less than 450 mA	

SECTION III

DAMPED SINE GENERATOR CONTROLS AND PORTS

The damped sine generator is designed to produce a damped (Q = 24 presently) sine at any of 12 frequencies in proper time relation to an internally generated pulse which biases the power amplifier on. The damped sine generator also provides suitable inputs and outputs such that other waveforms externally generated may be properly synchronized to the amplifier bias on pulse.

DAMPED SINE FREQUENCY (HMz): (12 position rotary switch)

This switch is used to select the desired damped sine frequency. Both carrier frequency and proper damping are selected. The carrier itself (cw) may be monitored or used for external generation of other waveforms. This carrier frequency is available at the carrier output monitor jack.

The 12 internally generated frequencies are:

10 kHz	800 kHz	10 MHz
20 kHz	1 MHz	30 MHz
50 kHz	2 MHz	50 MHz
100 kHz	4 MHz	100 MHz

The damped sine is available at the damped sine output jack. This jack is normally connected to the input of the PUP preamplifier (IFI 5000 Preamp.).

OUTPUT POLARITY: (2 position rocker switch)

This switch selects the polarity of the damped sine output. Plus or minus refers to whether the first half cycle will be positive or negative. If outputs other than from PA are utilized, the polarity may vary depending on the output selected.

REPETITION RATE GENERATOR (kHz): (six-position switch in connection with 2-position rocker switch with lamp)

The repetition rate generator is used for repetitively firing the damped sine generator, generally for setup and calibration. The rocker switch controls the rate generator on/off. The lamp is lighted when the rate generator is on.

MANUAL FIRE: (spring return rocker switch with lamp)

Pushing this switch will bring up the amplifier bias, generate one damped sine pulse, and return the bias to cut off. Lamp lighting indicates that the modulator has generated a damped sine pulse.

MODULATOR TRIGGER: (two-position rocker switch with lamp)

With this switch in the "EXT" position, the modulator can be triggered by an external signal rather than directly following the bias-on pulse. This allows the damped sine to be more closely synchronized to an external event. It should be noted that the trigger must come within the time duration of the amplifier ready pulse if the damped sine is to be amplified, since the amplifier bias is returned to cut off at the end of the amplifier ready pulse. Lighting of lamp indicates it is in the "EXT" position.

DAMPED SINE OUTPUT: (750 mV P-P into 50 ohms)

This output is normally connected to PUP preamplifier input directly or through external attenuators as necessary.

DAMPED SINE MONITOR: (100 mV P-P into 50 ohms)

This output allows observation of the damped sine as it leaves the modulator.

CARRIER MONITOR: (IV P-P into 50 ohms)

This output allows observation of or external use of the basic unmodulated carrier.

TRIGGER OUTPUT: (250 mV Peak into 50 ohms)

This output provides an output coincident with a zero-crossing of the carrier following a trigger signal and one carrier cycle in advance of the damped sine output.

AMPLIFIER READY: (TTL compatible output)

A positive pulse is available on this output during the time when the amplifier is biased on and is able to amplify a signal. The amplifier ready pulse will last for 96 ms.

EXT. MODULATOR TRIGGER: (TTL compatible input)

A positive going pulse on this input will trigger the modulator if the "MODULATOR TRIGGER" switch is in the "EXT" position.

EXT. FIRE SIGNAL: (TTL compatible input)

A negative going pulse or switch closure on this input will fire the system in the same manner as the manual fire switch.

PREAMPLIFIER: (IFI 5000)

The preamp contains the gain control and attenuator controlling the output of PUP. The switches control attenuators of the labeled value. With the switch in the up position, the attenuator is in the system. Thus, with all switches up and the control set to maximum CCW, the output will be a minimum.

SECTION IV

ASSEMBLY AND SET UP INSTRUCTIONS

PUP is shipped as two separate equipment racks for ease of handling. To assemble PUP, proceed as follows:

A. Remove each rack from its wrapping and skid.

B. See figure 3, remove the back and both side panels from the rack containing the damped-sine generator and the PUP preamplifier. The side panels are removed by removing the screws at the top of the panel and sliding the panel up.

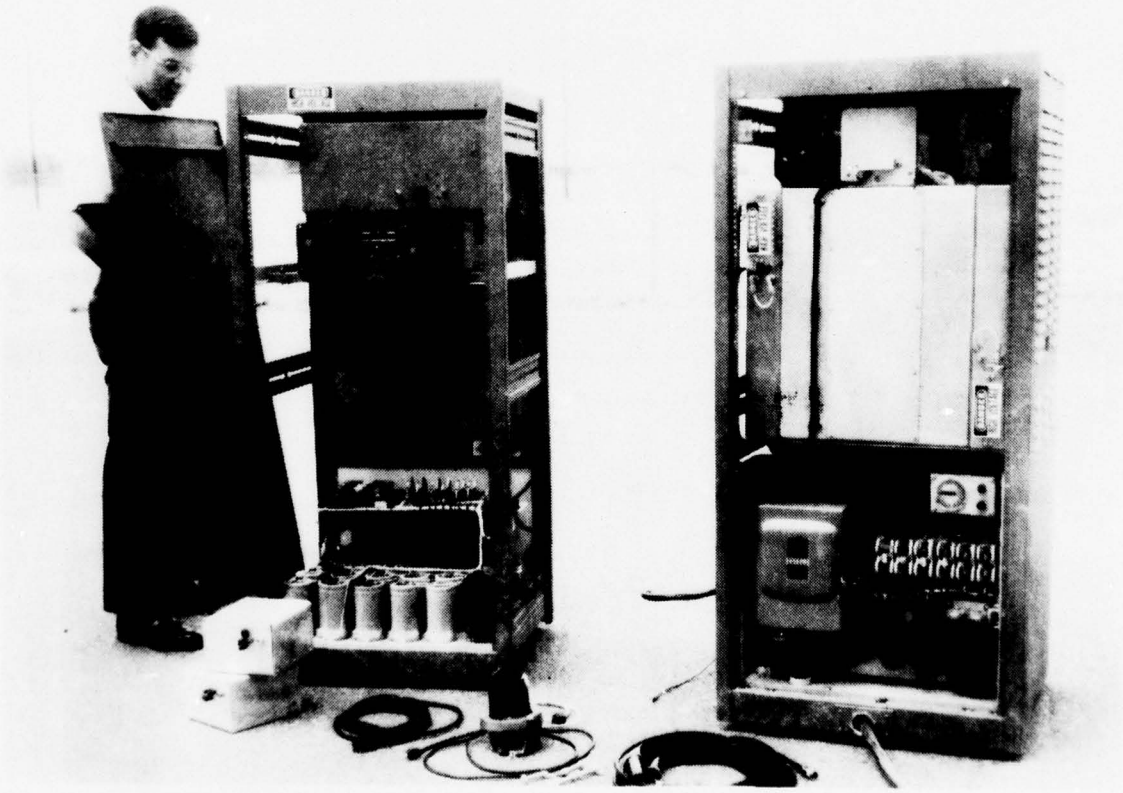


Figure 3. PUP Equipment Racks, Rear View

C. See figure 3, remove the back and right side (facing front of rack) of the rack containing the power amplifiers.

D. See figure 4, roll the racks together. The amplifier rack is on the left

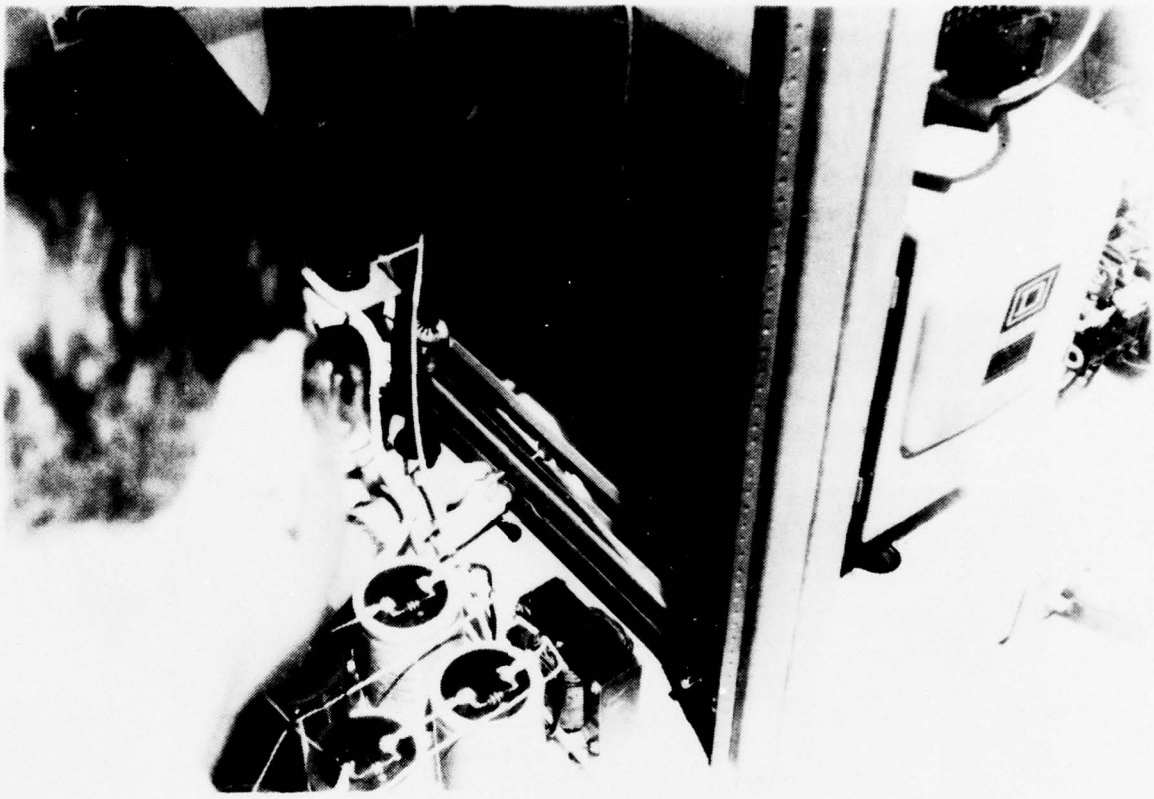


Figure 4. Rack Mating Connections

and the rack containing the PUP preamp and damped sine generator is on the right. Allow the guides on the amplifier rack to engage the holes on the right hand rack, and fasten the racks together with the 4 carriage bolts. The wing nuts do not come off of the bolts. The bolts are slid through the holes in the supporting members of the rack and then slid in the slots to the front and rear of the rack. Two bolts go on the top supporting member, and two bolts go on the bottom.

E. Connect the following cables:

1. Plate transformer a.c. primary power connections (a screwdriver is needed) (figure 5).

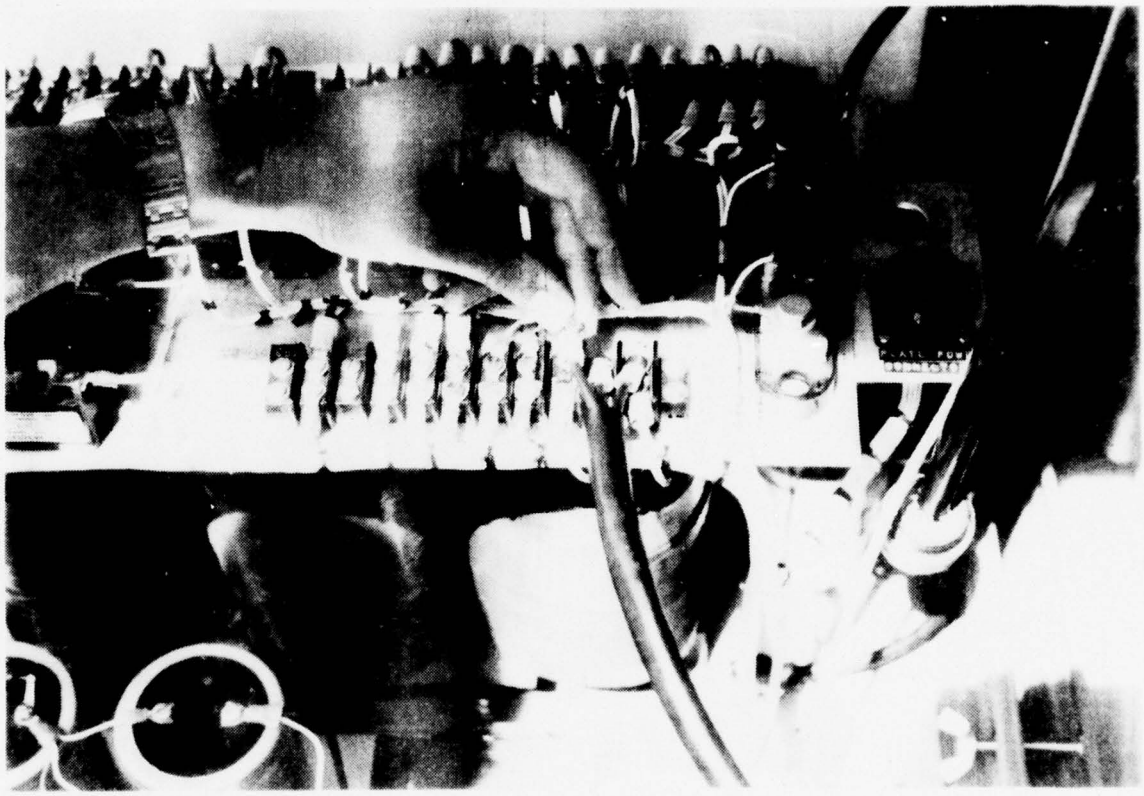


Figure 5. Plate Transformer a.c. Primary Power Connections

2. Plate circuit connector (figure 6).
3. a.c. power for the front panel convenience outlets (figure 7).
4. Connect the a.c. power cord to the PUP preamplifier. It is connected to receptacle "A" in figure 7 and receptacle "A" in figure 8.
5. Connect the damped-sine generator power cable. The connections are labeled "B" in figure 8.
6. Connect the "Bias-On" cable. It is shown being connected in figure 8.

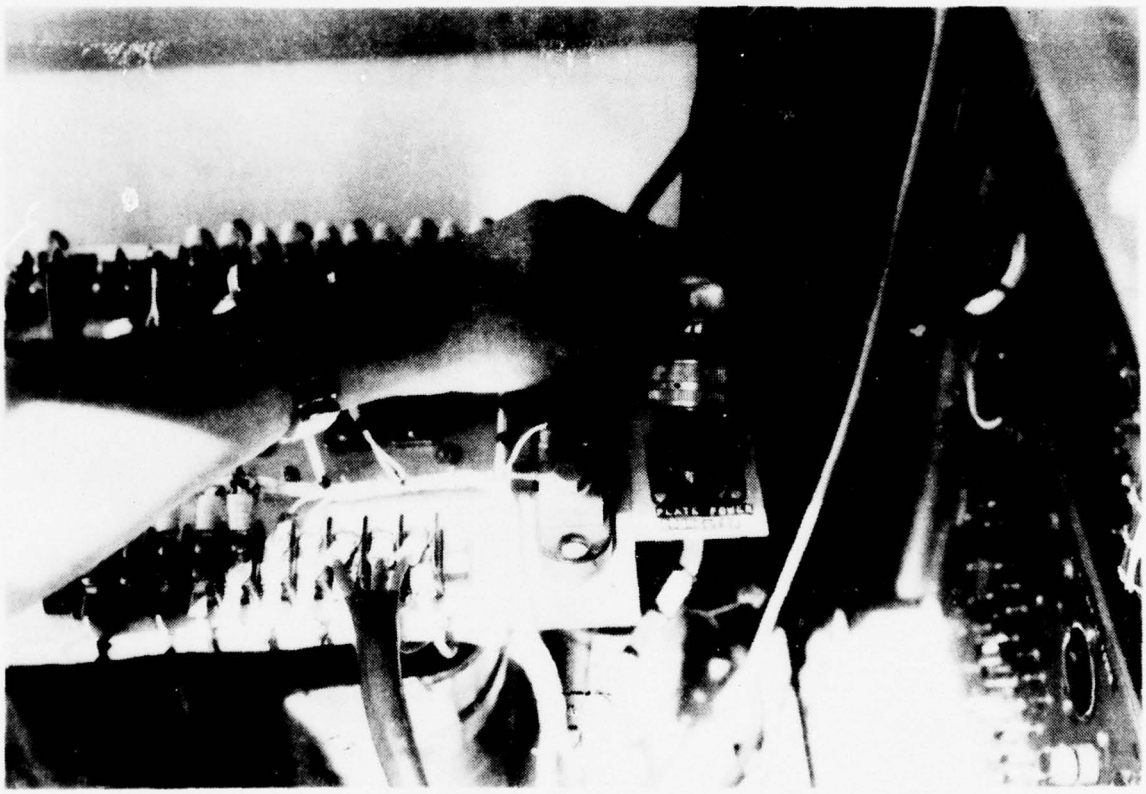


Figure 6. Plate Circuit Connector and Cable

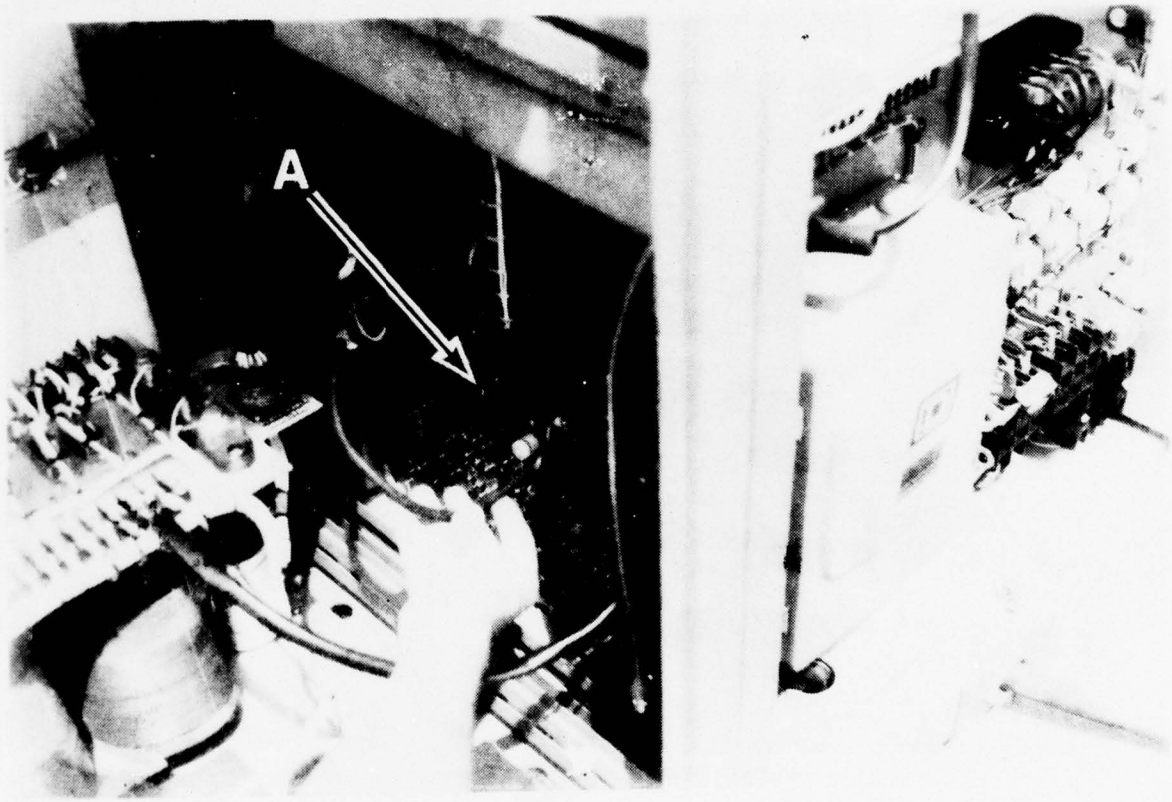


Figure 7. a.c. Power for Front Panel Convenience Outlets

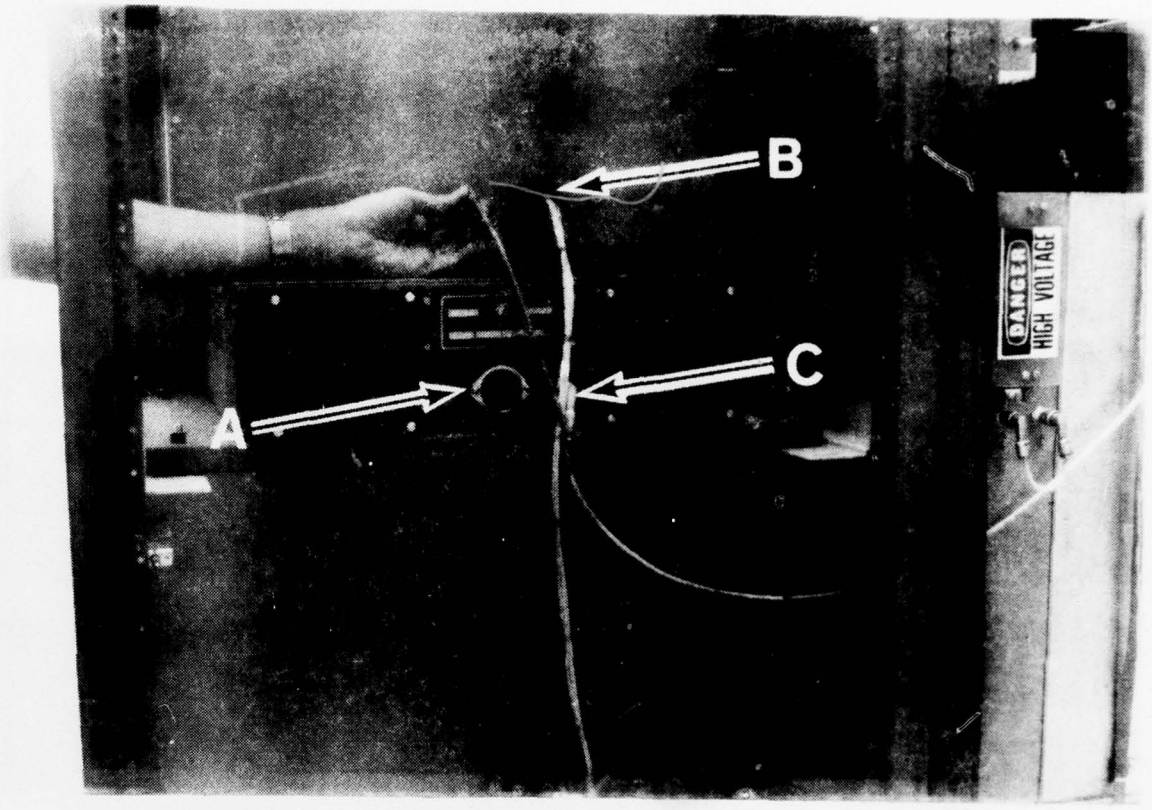


Figure 8. Damped Sine Generator, PUP Preamplifier and Driver Amplifier Connections

7. Connect the cable between the PUP preamplifier output and the driver amplifier input. This is labeled "C" in figures 8 and 9.

8. Connect the safety light. Be sure to thread the wire as shown in figure 9 or the side panel will not go back on.

F. Replace the side panel as shown in figure 10. The safety-light cord fits through a slot in the top of the panel.

G. Replace the back cover on the rack containing the damped-sine generator and PUP preamplifier. Remove the left side cover of the rack containing the amplifiers. This is shown as "E" in figure 10.

H. Make sure the fused-disconnect switch shown as "D" in figure 10 is off (handle down).

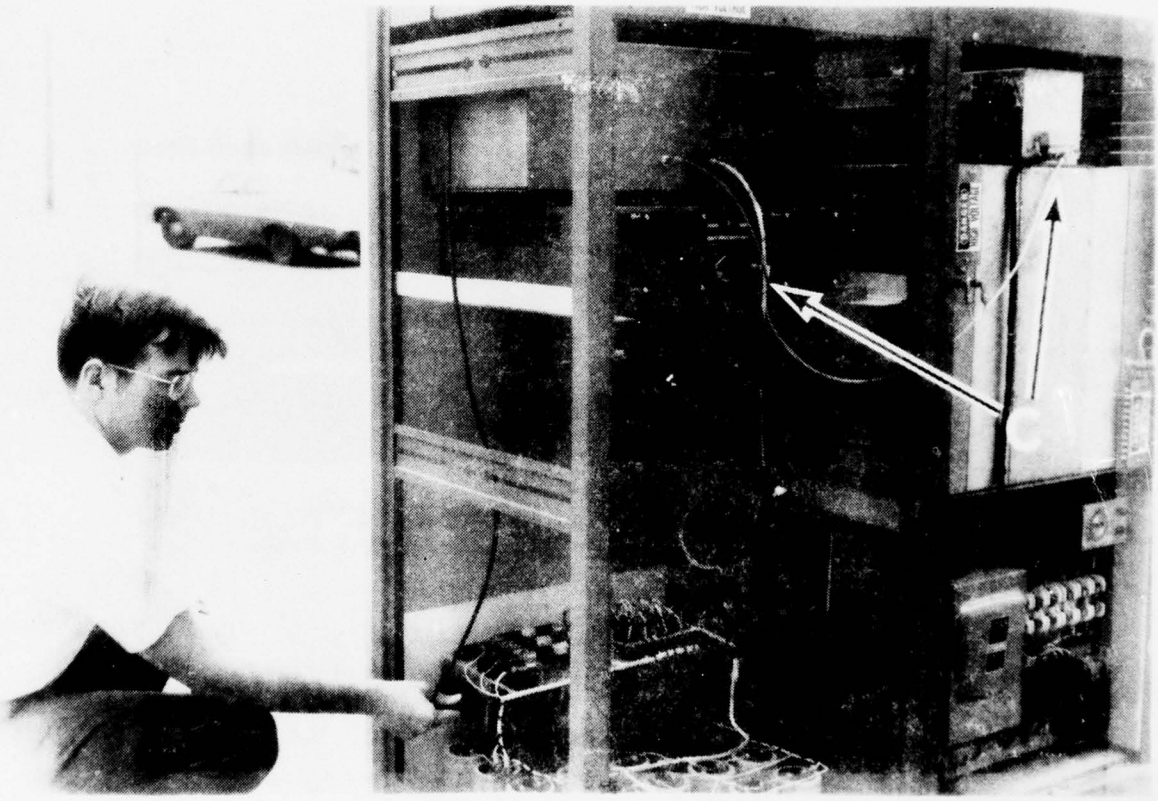


Figure 9. Safety Light Connection

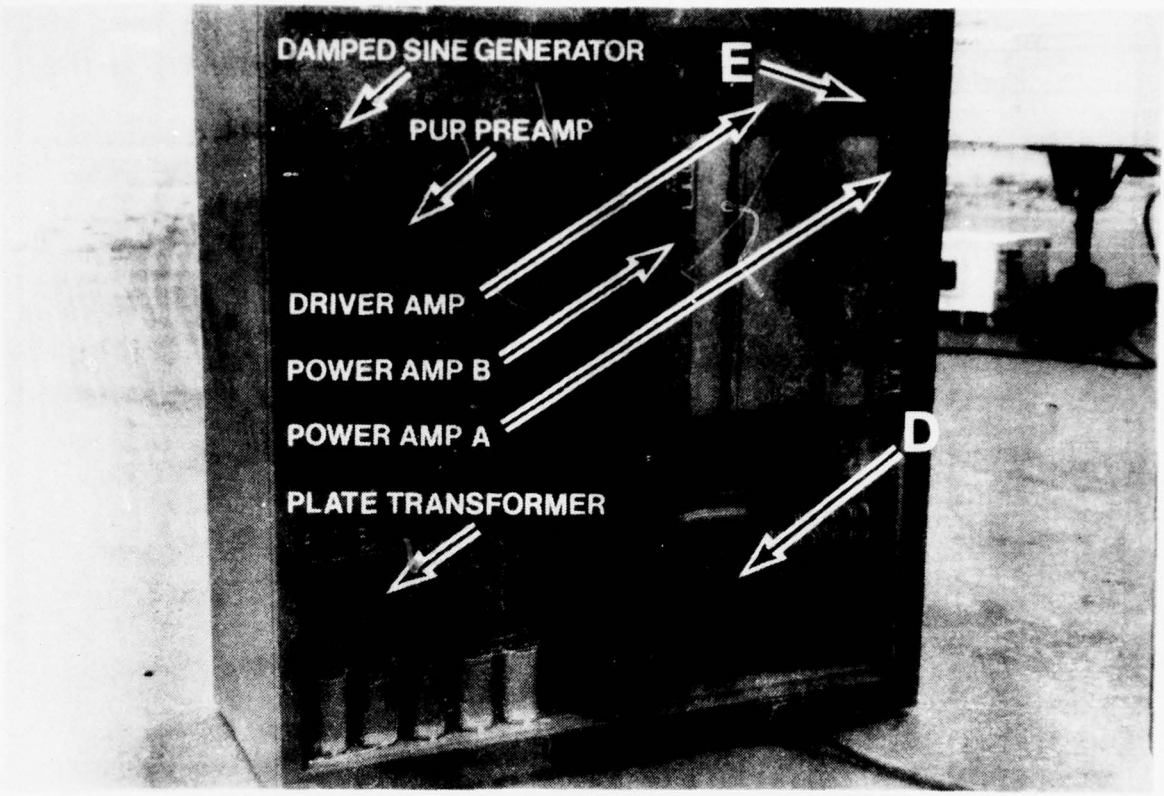


Figure 10. Completed Assembly With Rear Panels Removed

I. Connect the power cable to a source of 208V 3 phase 60 Hz (208V line to line, nominal) power. Extreme care must be taken to assure that the green conductor in the cable is connected to a good equipment ground. The other three wires are connected to the 208V 3 phase supply in any order. Phase sequence is not important. The neutral wire of the electrical system is not used in PUP and NO current flows in its equipment ground wire.

J. Open the fused-disconnect switch ("D" in figure 10) and check for the correct voltages at the top lugs. (208 nominal volts between lugs.) Accurately measure the line to line voltage. The taps on the primary of the filament transformer must now be adjusted so that the line to line voltage as measured will result in 6.0 volts on the filaments of the tubes in the power amplifiers.

Make sure that the disconnect switch is still off.

Refer to drawing 7513613 (Appendix D). Locate the measured line to line voltage in the left hand column in the table located in the lower left of drawing 7513613. The primary terminal board (F in figure 11) is then

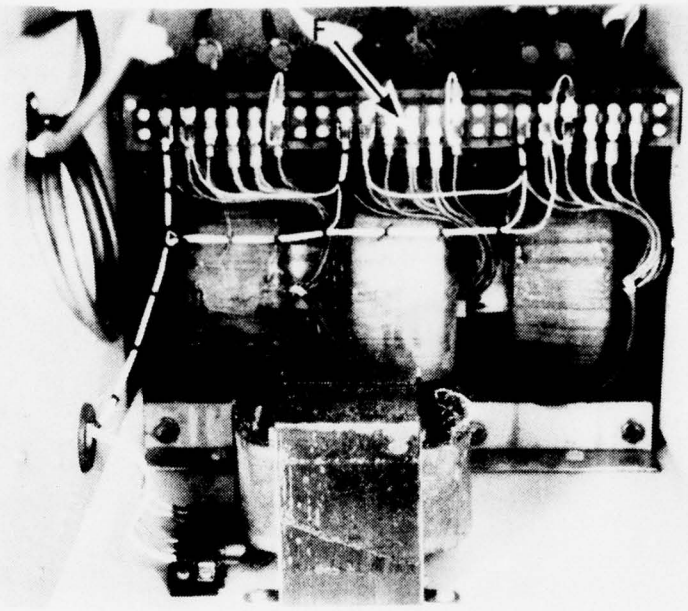


Figure 11. Filament and Control Transformers

strapped according to the row in the table corresponding to the measured voltage.

EXAMPLE: If the line to line voltage is measured at 209.6 volts, the 210 volt row is used in the table of drawing 7513613. Thus "A" would be jumpered to "Q", "S" would be jumpered to "P", etc. Power is always fed to the transformer on "A", "B", and "C". The connections for 210 volts are shown in figure 12.

K. Turn the fused-disconnect switch on and replace the side and rear covers. The "off" push button on the front panel should now be illuminated.

L. Proceed with initial startup.

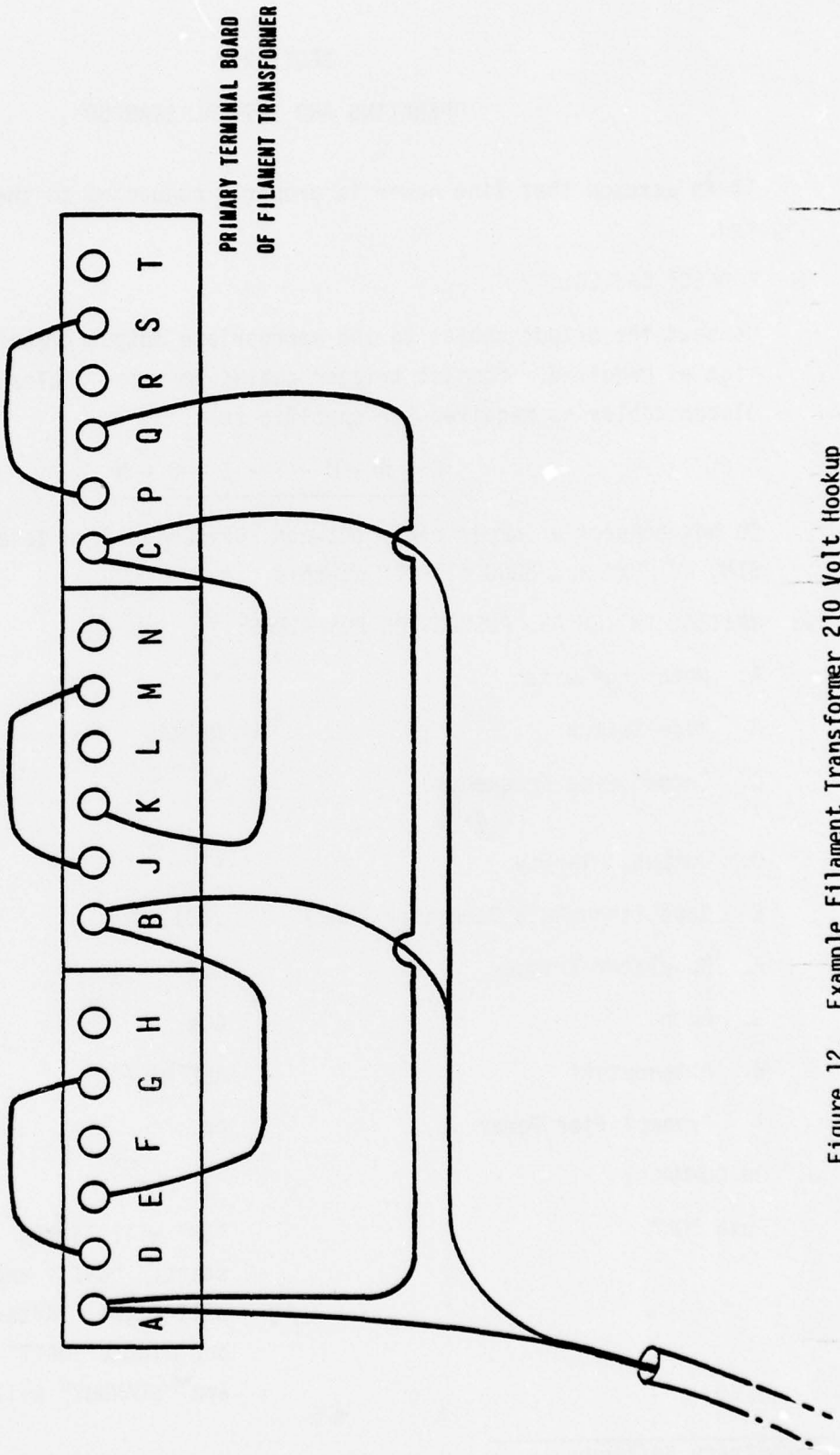


Figure 12. Example Filament Transformer 210 Volt Hookup

SECTION V

OPERATING AND INITIAL STARTUP

It is assumed that line power is properly connected to the PUP with "OFF" lighted.

1. CONNECT CABLES:

   Connect the output cables to the appropriate output transformer or termination as required. Connect trigger cables, monitor cables, and external modulator cables as required for specific test.

   C - A - U - T - I - O - N

   Do not connect a jumper cable between PUP Damped Sine Generator "DAMPED SINE OUTPUT" and 5000 "INPUT" at this time.

2. INITIAL SWITCH AND PUSHBUTTON POSITIONS:

A.	Metering Switch	*
B.	Mode Switch	NORMAL
C.	Damped Sine Frequency	*
D.	Output Polarity	*
E	Repetition Rate Generator (KHz)	.001, Off
F.	Modulator Trigger	INT
G.	Gain	CCW
H.	Attenuators	ALL UP (IN)
I	Preamplifier Power	ON

3. ON COMMAND:

Push "ON"	"ON" will light. The blower will start. "WAIT" and "FILAMENTS ON" will light. After approximately one minute "WAIT" will extinguish and "STANDBY" will light.

*Arbitrary setting.

4. OPERATE COMMAND:

Push "OPERATE"	"STANDBY" will extinguish; "OPERATE' will light; and the red safety lamp will light.

5. METERING OBSERVATIONS:

Rotate Mode Switch to "TEST-CW AMP A"	"AMP A BIAS ON" will light

NOTE: If an overload occurs when the Mode Switch is switched to "TEST-CW AMP A", locate the holes below the "TEST-CW AMP A" light on front panel. Behind each hole is a potentiometer which controls the bias to a power amplifier. With a screwdriver rotate both potentiometers fully CCW. Push "RESET" then return to Step 4.

Use the Metering Switch to read plate currents	Driver I_B 2.5 amperes IPA I_B 2.5 amperes PA I_B 7.2 amperes

NOTE: Locate the two holes below the "TEST-CW AMP A" light. With a screwdriver in the lower hole, adjust the potentiometer for PA I_B of 7.2 amperes.

Rotate the Mode Switch to "TEST-CW AMP B"	"AMP B BIAS ON" will light
Use the Metering Switch to read plate currents	IPA I_B 2.5 amperes PA I_B 7.2 amperes

NOTE: Repeat the previous note with the screwdriver in the upper potentiometer.

Return the Mode Switch to "NORMAL"

6. BIAS ON CHECK:

Push the Repetition Rate Generator Switch to "ON"	Both "AMP A BIAS ON" and "AMP B BIAS ON" will flash at a 1 pps rate.
Push "STANDBY"	"STANDBY" will light.

7. DAMPED SINE CHECK, IF DESIRED:

Insure the system is in Standby state	"STANDBY" lighted
Rotate the "DAMPED SINE FREQUENCY" Switch to desired frequency	

Switch "ON" the Repetition Rate Generator, Select a rate for best observation

Observe the damped sine output at "DAMPED SINE OUTPUT" or "DAMPED SINE MONITOR" with an oscilloscope.

C - A - U - T - I - O - N

The system must be in the "STANDBY" state and the Repetition Rate Generator switched "OFF" before proceeding further.

8. FINAL SETUP

Connect "DAMPED SINE OUTPUT" to IFI 5000 INPUT. Select the desired damped sine frequency, trigger mode repetition frequency, and peak amplitude as desired.

Push "OPERATE"

SECTION VI

DISASSEMBLY AND SHIPPING PREPARATION

1. Disconnect the line power cord from the source and remove the amplifier output cables from the system.
2. Remove both back panels and right (as viewed from front) side panel.
3. Disconnect the plate circuit cable. The connector is located to the right on a large aluminum plate on top of the plate transformer (left rack as viewed from rear).
4. Disconnect the plate circuit primary power leads. These three leads are in a black cable connected to a barrier strip on the aluminum plate on top of the plate transformer. Remove three screws to free the cable. Replace screws securely in the barrier strip.
5. Disconnect the BIAS ON cable. This cable is the only BNC cable connected to the back of the DAMPED SINE GENERATOR.
6. Disconnect, for separate packing, the following:
   a. IFI 5000 Power Cord
   b. IFI 5000 Output Cable
   c. DAMPED SINE GENERATOR Power Cord
   d. Safety Light
   e. Four Carriage Bolts with Wing Nuts (these four bolts secure the racks together. Loosen nuts and slide bolts toward center for removal through enlarged holes).
7. Separate the racks.
8. Secure all loose cables. With tape or cable ties, secure the Plate Circuit Cable, Plate Circuit Primary Power Leads, and BIAS ON Cable.
9. Replace all Back Panels (eight screws/panel).
10. Replace the Right Side Panel (removed in Step 2) and two side panels used for shipping only. Match the punch marks (1, 2, 3 or 4) on the top edge of the side panel and rack (two screws/panel).

11. Crate both racks. Secure the Line Power Cord prior to crating.
12. Assemble the following items for shipment:
    a. IFI 5000 power cord
    b. IFI 5000 output cable
    c. DAMPED SINE GENERATOR power cord
    d. Safety light
    e. Four carriage bolts with wing nut
    f. Two amplifier output cables (20 ft RG-7 cable, Type N to brass adapter Type N)
    g. Output transformer assemblies
    h. Amplifier system (AFWL/PUP) S/N 0001 (2 racks).

SECTION VII

FUNCTIONAL OPERATION OF DAMPED SINE GENERATOR

The damped sine generator is located at the top of the right hand rack of PUP. This generator produces the damped sine pulses which are subsequently amplified by the PUP amplifiers.

A functional block diagram of the damped sine generator is shown in figure 13. There is, within the damped sine generator, an oscillator (carrier generator) which generates a continuous sine wave carrier. The frequency of this carrier is selected by the front panel damped sine frequency switch and any one of 12 frequencies can be selected: 10 kHz, 20 kHz, 50 kHz, 100 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz, 10 MHz, 30 MHz, 50 MHz, and 100 Mhz. When a damped sine pulse is generated, its frequency will be the frequency selected above. A sample of this carrier can be monitored or counted using the carrier-monitor output Jack (J4) on the front panel. This Jack will put out 1 volt peak to peak into a 50 Ω load.

There is, within the damped sine generator, a combination of circuits consisting of: (1) a zero-crossing detector, (2) an envelope generator, and (3) a modulator. These three circuits operate on the carrier and generate from it a damped sine wave. (For more detail of this, see figure 13 and the damped sine generator circuit description.) This damped sine is available at the "DAMPED SINE OUTPUT" Jack J1 and the "DAMPED SINE MONITOR" Jack J2 on the front panel. Jack J1 will deliver 750 mV peak to peak into 50 Ω and usually drives the PUP preamplifier through a BNC cable. Jack J2 will deliver 100 mV peak to peak into 50 Ω and is used to monitor the damped sine waveform.

Just prior to the generation of the damped sine, a scope trigger signal is generated within the damped sine generating circuits. This scope trigger is available as a 250 mV peak positive pulse on the trigger output Jack J3. It is used to trigger the scope when observing the damped sine wave.

There is, within the damped sine generator, a wire between terminal 8-17 and the zero crossing detector in the damped sine generating circuits block. This line carries the trigger signal which initiates production of a damped sine. Terminal 8-17 is normally at a TTL logic high. When a damped sine is desired, 8-17 goes low, producing the sequence of events shown in figure 14.

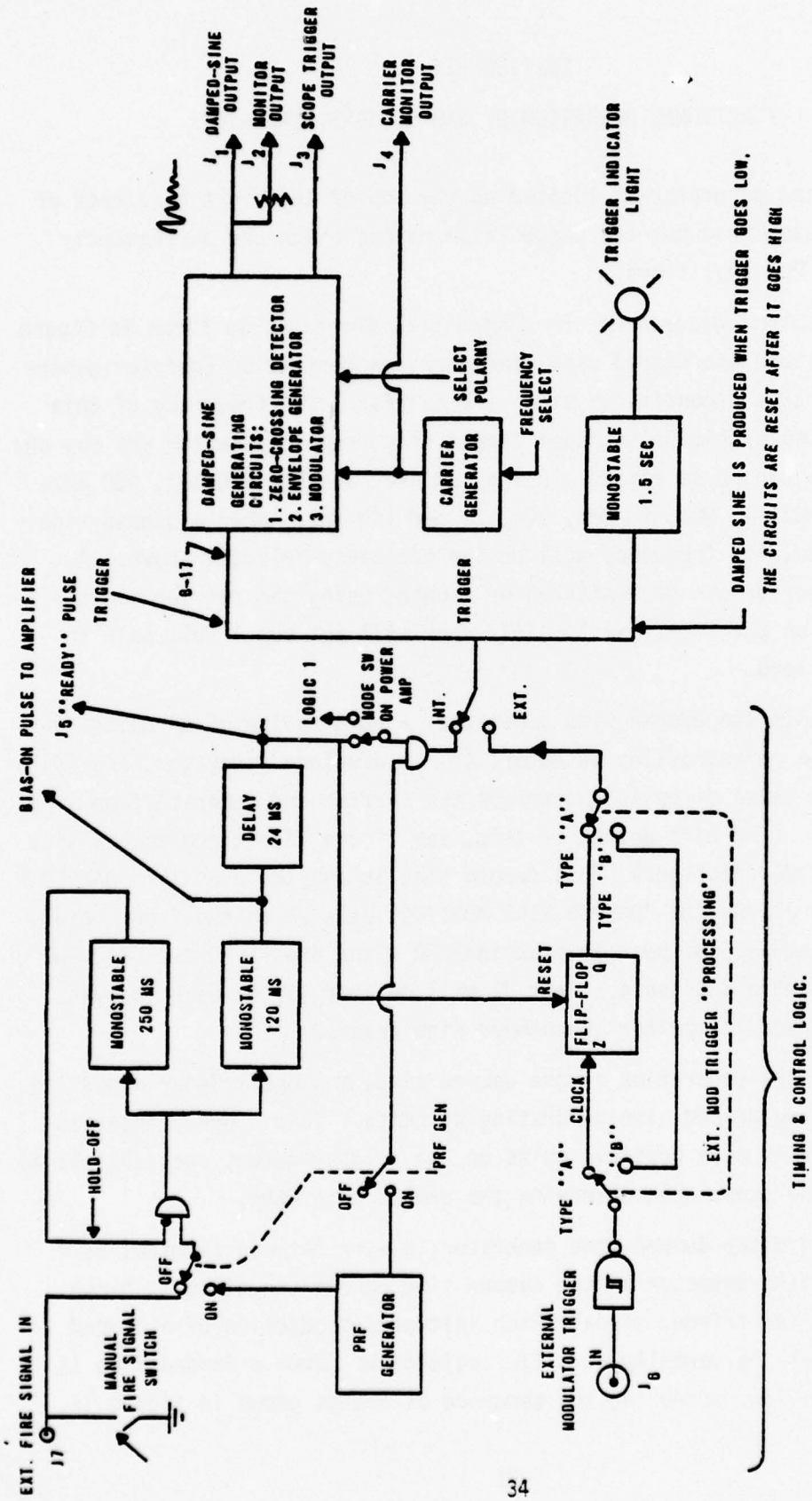


Figure 13. Damped Sine Generator Functional Diagram

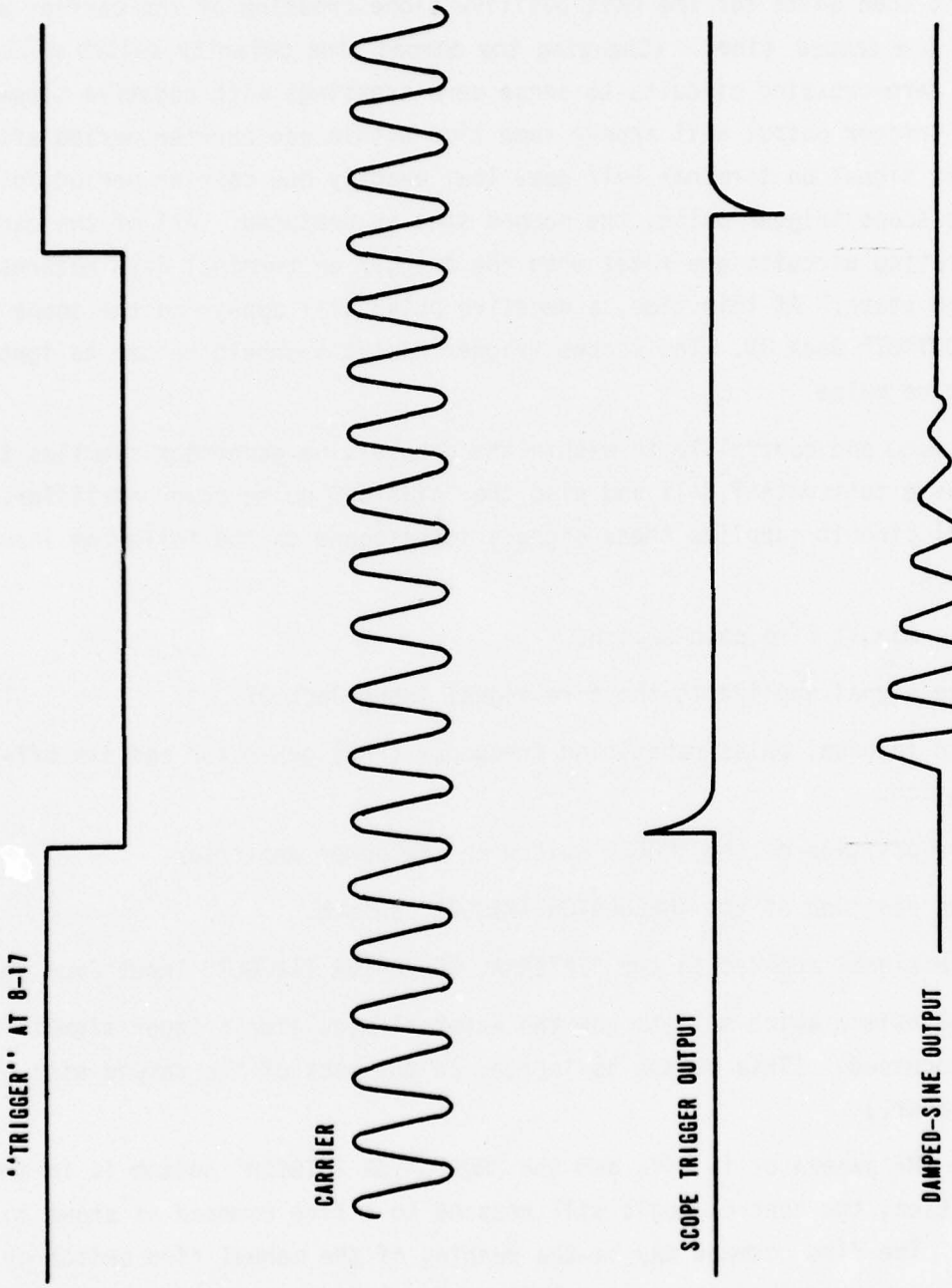


Figure 14. Damped Sine Generator Timing Diagrams

After terminal 8-17 goes low, the circuit waits for the carrier to cross zero with positive slope. When it does, the circuit produces a scope trigger pulse. The circuit then waits for the next positive slope crossing of the carrier and initiates the damped sine. (Changing the damped sine polarity switch will cause the zero-crossing circuits to sense zero-crossings with negative slope.) The scope trigger output will appear some time within one carrier period after the trigger signal on terminal 8-17 goes low; exactly one carrier period following the scope trigger pulse, the damped sine is produced. All of the carrier generating circuits are reset when the trigger on terminal 8-17 returns to its high state. At this time, a negative pulse will appear on the scope "TRIGGER OUTPUT" Jack J3. The scopes trigger controls should be set to ignore this negative pulse.

The timing and control logic within the damped sine generator supplies the trigger pulse to terminal 8-17 and also the "bias-on" pulse power amplifier. The control circuit supplies these signals in response to the following inputs and switches:

1. The manual fire push-switch.
2. The signal applied to the fire signal input Jack J7.
3. The internal pulse repetition frequency (PRF) generator and its off-on switch.
4. The position of the "MODE" switch on the power amplifier.
5. The position of the "MODULATOR TRIGGER" switch.
6. The signal applied to the "EXTERNAL MODULATOR TRIGGER" Input Jack J6.
7. The switch which selects how the external modulator trigger signal is processed. (This switch is located on the back of the damped sine generator.)

If the PRF generator is off, and the "MODULATOR TRIGGER" switch is in the "INT" position, the control logic will respond to a fire command as shown in figure 15. The fire command may be the pushing of the manual fire switch or a TTL logic zero applied to the external fire signal in Jack J7. The fire signal triggers two monostable circuits (figures 13 and 15). The first produces the 250 ms hold-off pulse. This is used to inhibit any additional fire signals which might occur within 250 ms of the accepted fire signal. The second

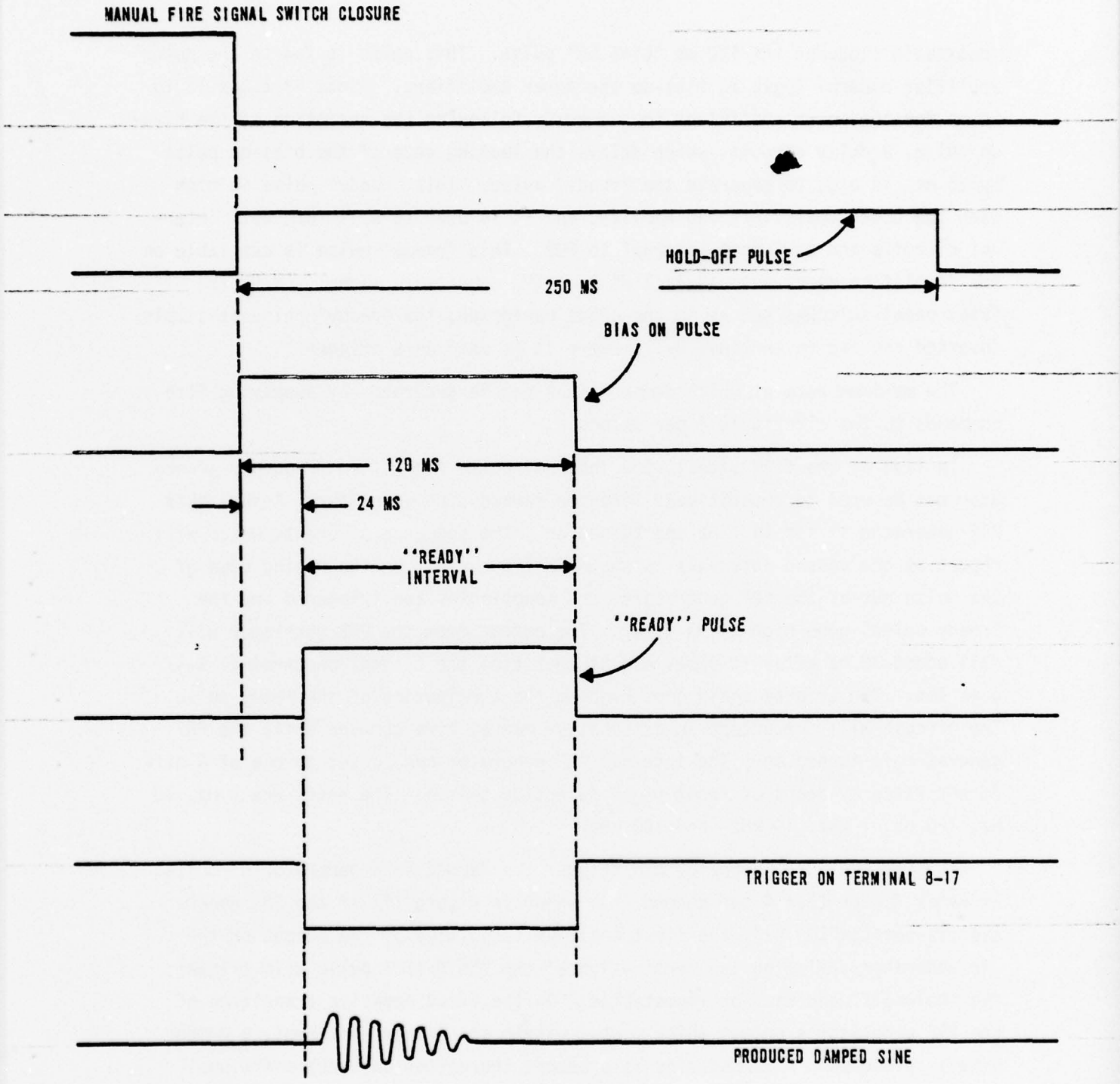


Figure 15. Damped Sine Generator Control Timing Signals, Manual Fire Mode

monostable produces the 120 ms "bias-on" pulse. This pulse is fed to the power amplifier control logic to bias-up the power amplifiers. Since it takes 15 to 20 ms for the power amplifiers to get ready following the reception of the bias-on pulse, a delay circuit, which delays the leading edge of the bias-on pulse by 25 ms, is used to generate the "ready" pulse. This "ready" pulse is high when the power amplifiers can amplify, and it is used to so inform both internal circuits and equipment external to PUP. This "ready" pulse is available on the "amplifier ready output" Jack J5 as a TTL compatible signal. With the front panel switches set as in the above paragraph, the "ready" pulse is simply inverted and fed to terminal 8-17, where it is used as a trigger.

The maximum rate at which damped sines can be generated by supplying fire commands to the circuit is 4 per second.

In lieu of the fire signal, the internal pulse repetition frequency generator can be used to repetitively fire the damped sine generator. Assume this PRF generator is set to 1 Hz and turned on. The sequence of events which will repeat at one second intervals is shown in figure 16. On the rising edge of the pulse out of the PRF generators, the monostables are triggered and the "ready pulse" goes high 24 ms later. The output from the PRF generator will fall about 30 ms after it rises and at this time the trigger on terminal 8-17 goes low. The trigger again goes high at the termination of the ready pulse. The circuit will not accept an external or manual fire command while the PRF generator is turned on. The internal PRF generator can be set to one of 6 different rates by means of front panel selection switch. The rates are 1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz, and 100 kHz.

The internal PRF generator can trigger the damped sine generator circuits at rates faster than 4 per second. As shown in figure 17, if the PRF generator is set to "100 Hz", the first positive transition of the output of the PRF generator following the termination of the "hold-off" pulse will trigger the "hold-off" and bias-on monostables. On the first negative transition of the PRF generator's output which occurs within the "ready" interval, a damped sine is produced. A damped sine is produced thereafter on every additional negative transition and the damped sine generating circuits are reset on the following positive transition of the PRF generator's output, so long as these transitions fall within the "ready" interval. A permanent reset is applied to the damped sine generating circuits (terminal 8-17) when the "ready" pulse

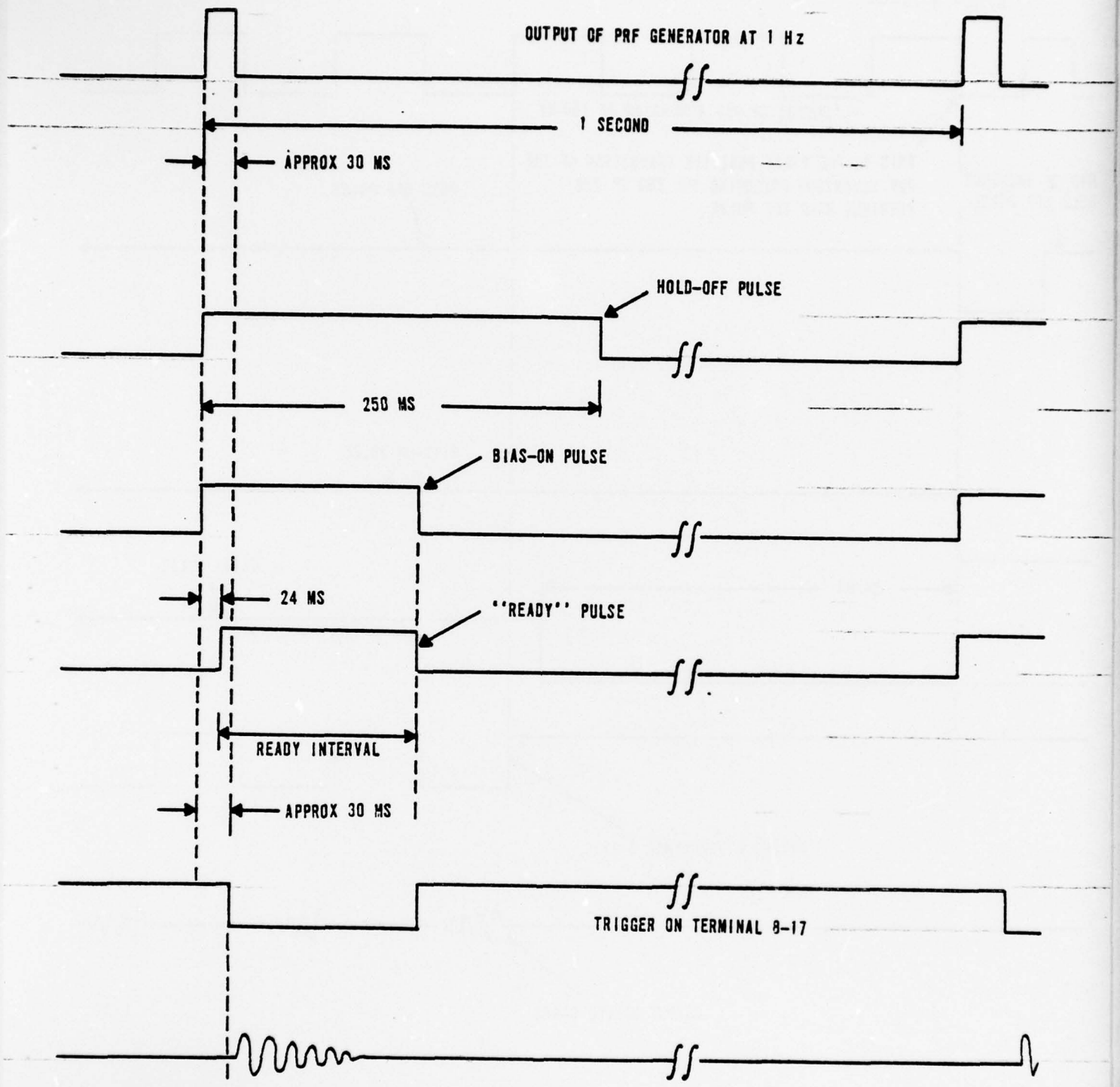


Figure 16. Damped Sine Generator Control Timing Signals, Repetitive Mode, 1 Hz

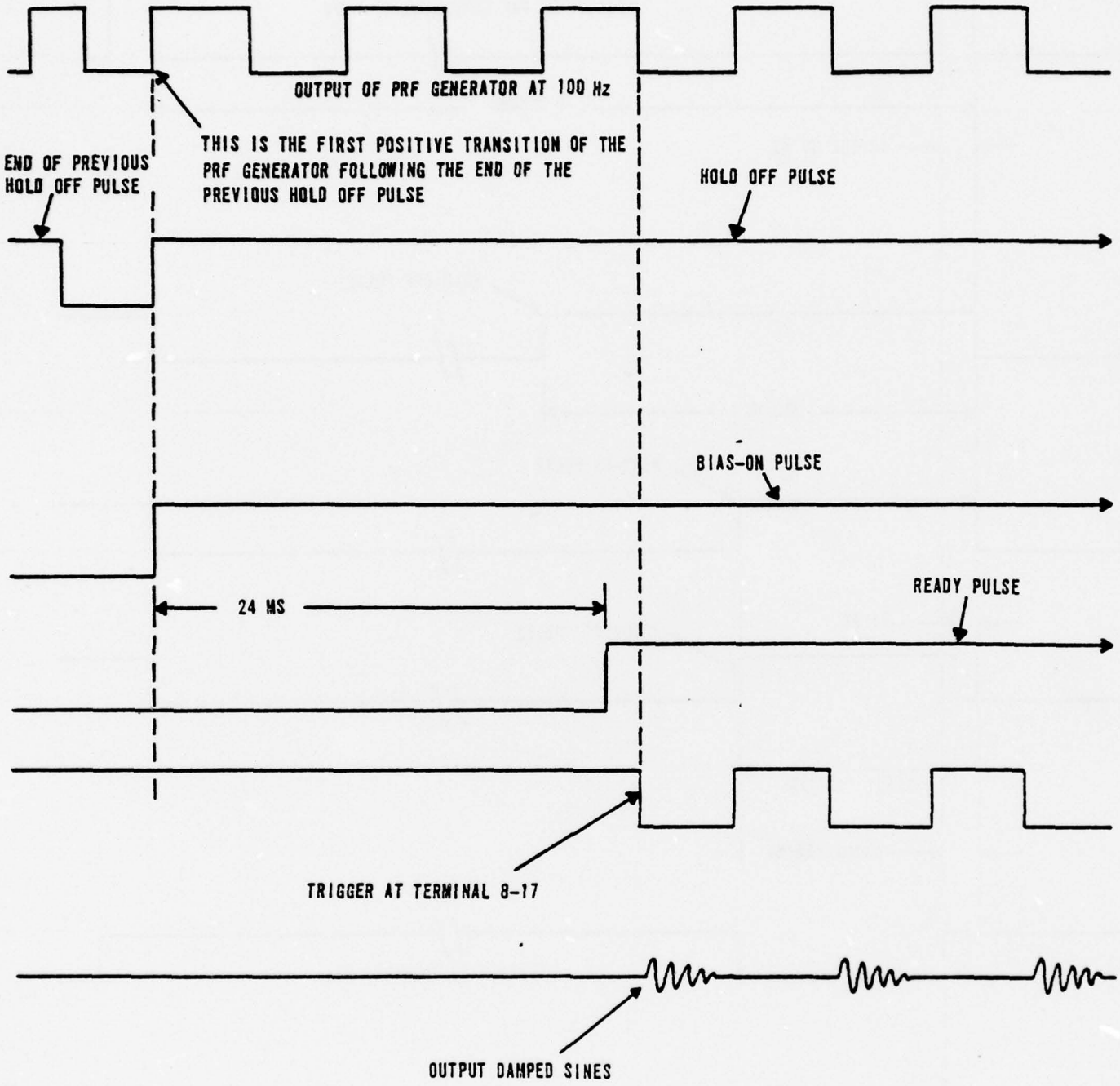


Figure 17. Damped Sine Generator Control Timing Signals, Repetitive Mode, 100 Hz

terminates. A series of damped sine pulses is therefore produced during the "ready" interval. The number of pulses produced during the "ready" interval is a function of the rate of the PRF generator. The rate of the PRF generator should, however, be kept low enough for a particular damped sine frequency to allow a complete damped sine pulse to be produced. If the damped sine generator circuits are reset too soon after a trigger, the tail of the damped sine will be noticeably chopped off.

If the power amplifiers in PUP are operated in either the "TEST-CW AMP A" or "TEST-CW AMP B" modes, the bias-on pulse does nothing, and therefore it is not necessary to synchronize the damped-sines to the "ready" interval. In these two operating modes, therefore, the synchronization is disabled, and the PRF generator's output is fed directly to the damped sine generating circuits to provide a continuous succession of damped sine pulses.

When it is desired to synchronize the damped sine pulse to some external event with more accuracy than can be obtained by the use of the "fire" command, the external trigger input can be used. This input (J6) is called the EXTERNAL MODULATOR TRIGGER on the front panel of the damped sine generator. To use this input, the "modulator trigger" switch is placed in the external position, and the damped sine generating circuits will be triggered coincident with a TTL logic 0 to logic 1 transition on J6. The damped sine will be produced between one and two carrier periods later. PUP must, of course, still have a fire command to bias up the power amplifiers, and the external trigger must occur within the "ready" interval for normal mode operation.

The external trigger signal can be processed in two ways, Type A, and Type B. The type of processing is selected by a switch on the rear panel of the damped sine generator.

In Type A processing, a continuous succession of pulses may be applied to the ext. trigger input. Following a fire command, only the first ext. trigger pulse which occurs within the "ready" interval will trigger the damped sine generating circuits. Only one damped sine pulse will be generated for each fire command since the damped sine generating circuits will not be reset until termination of the "ready" pulse.

In Type B processing, the EXT modulator trigger input is coupled directly into the damped sine generating circuits, and a damped sine is produced by the damped sine generator for every positive transition on the trigger input, independent of the fire pulse or "ready" interval. Here again, the fire command is still necessary to bring "up" the PUP power amplifier, and the trigger must occur within the "ready" interval for normal mode amplifier operation. When the amplifiers are operated in the "TEST-CW AMP B" or "TEST-CW AMP A" mode, the fire command is not necessary since the amplifier is continuously ready.

In Type B processing, the trigger must remain high (TTL logic 1) longer than the duration of the damped sine pulse since the damped sine generating circuits will be reset when the external trigger input returns to a logic low.

A 1.5 sec timer tied to the trigger line (8-17) of the damped sine generating circuits is triggered each time a damped sine is produced. This timer lights a lamp (trigger indicator light) located in the handle of the FIRE switch. Illumination of the handle indicates a damped sine has been generated.

SECTION VIII

CIRCUIT DESCRIPTION

PUP is a pulsing system mounted in two rack panels. It consists of a damped since pulse generator, an amplifier system to bring the pulses up to a 2 kW level or less as desired, and a set of output transformers to provide the desired coupling from the amplifiers to the device under test. The system has the capability of amplifying pulses other than the internally generated damped sines if they are supplied to it from an external source.

AMPLIFIERS:

The signal flow in the amplifier is shown on Drawing 7613268 (Appendix D). The damped sine generator located in the top of the right hand rack feeds a signal via a front panel jumper to the input of the preamp. The signal level into the preamp is 750 mV P-P into 50 Ω. The preamp is an IFI Model 5000L; it has a frequency response from 10 kHz to 220 MHz, and a gain of 30 dB max. Attenuators on this preamp allow its gain to be reduced by any amount up to 50 dB. These attenuators are used to adjust and set PUP's output amplitude. Additional information on the 5000L can be obtained from the IFI instruction manual (Appendix A) and IFI Drawings 8-0510-00-202-1, 8-0500-00-202-1, and 466-2047 (Appendix D).

The output of the 5000L is fed to the input of the driver amplifier. The driver amp is an IFI type 402 six-tube distributed amplifier with an output capability of 100W (IFI Drawing 8-0404-01-102). The signal is amplified approximately 9 dB in this stage. The output from the driver is fed to the input transformer assembly where it is split into two signals to drive the intermediate power amplifiers (IPA).

The IPAs have an input impedance of 50 Ω. The input transformer in effect places the two 50 Ω inputs in series across the 90 output of the driver amp. A switch in the input transformer assembly is provided to change the phase of the signal fed to the IPA by 180°.

PUP's output stage consists of two IFI type 406 unit amplifiers. Each unit consists of an IPA of 6 tubes and a power amplifier of 24 tubes. Each unit feeds an output on the front of PUP, and each unit is capable of supplying 1 kW to a 50 Ω load. The two units normally work in push-pull with respect to each

other in that the input signals to them are 180° out of phase. The power output from both units is then combined in the output transformer external to the PUP racks.

The units can also be operated in parallel by connecting their outputs in parallel and changing the switch in the input transformer assembly to the "PARALLEL" position producing "in phase" inputs to both units.

The six-tube IPAs are distributed amplifiers, essentially electrically identical to the six-tube driver amplifier. They each have six type 4CX250B tetrode tubes operating at 2.5A (total for six tubes) plate current, 450V plate potential, and 350V screen potential. The output (plate) transmission line's impedance is 90 Ω and the input (grid) transmission line's impedance is 50 Ω. Each six-tube IPA drives a power amplifier through a BNC jumper on the back of the units. Each power amplifier is a distributed amplifier using 24 type 4CX250B tubes operating at 7.4A plate current (total for 24 tubes), 800V plate potential, and 350V screen potential. The power amplifiers have an output (plate) transmission line impedance of 100 Ω and an input (grid) line impedance of 50 Ω.

Distributed amplifiers are used to extend the frequency range of an amplifier beyond what is possible with multistage cascaded amplifiers. The low frequency gain of a single stage in a cascaded amplifier is a function of the load resistor and the Gm of the tube. If two tubes are operated in parallel, the Gm of the parallel combination will be twice that of one tube. Thus, if tubes are operated in parallel, the total gain will be the sum of the individual gains.

At high frequencies, the input and output capacitances of the tubes shunt the load resistors and cause the amplifiers' high frequency response to roll off. To increase the high frequency response, the load resistor can be lowered, but at the expense of gain. Thus, as the load resistor is lowered, more cascaded stages would be required to supply the desired gain. A high frequency limit is reached as stage gain approaches one. If several tubes are paralleled, their gains add. Their capacitances parallel each other, however, and this requires that R_L be lowered to maintain bandwidth. The resulting gain will be as before. The only improvement is in power output capability.

Consider now two lumped transmission lines, each having the same delay per section. Consider also that the plate capacitance of the tube is used as the shunt capacitance for one section of one line (plate line) and the tubes input capacitance is used as the shunt element for one section of the other line (grid line). The frequency response of this amplifier is now determined by the line cutoff frequencies. The gain of this configuration may be less than one; however, as many tubes as desired can be "paralleled", in effect, to obtain useable gains without lowering the bandpass by adding one section to each line for each tube added (see IFI Drawing 8-0404-01-102 (Appendix D).

The individual plate currents add because the velocity of propagation in both transmission lines are the same. The only trade-off is in increased delay time through the amplifier. The six tubes in the IFI type 404 amplifier provide 9 dB of circuit gain out to 220 MHz. The PUP output stages use 24 tubes each. This number is too large to be efficient as a distributed amp from a gain-bandwidth point of view, but the large number are used to provide the output power capability.

The tubes in the driver, IPA, and power amplifiers are forced-air cooled by means of the filament blower which feeds air to a plenum located between the amplifiers.

POWER SUPPLY:

A power source of 208V, 3 Phase, 60 Hz with a capability of 40 amp is supplied to the fused-disconnect switch in the rear of the PUP (rack #2) (see Drawing #7513614, Appendix D). Power from this switch is supplied to two sets of fuses. One set of fuses (FU7, 8, and 9) (30A) feeds the plate transformer through plate contactor R5 and the plate primary overload detector. The other fuse set (FU4, 5, and 6) feeds the control transformer directly, and the filament transformer through filament contactor R4.

When power is supplied to PUP, and the fused-disc switch is closed, power is immediately supplied to the control transformer. This transformer supplies 15V a.c., 60 Hz to the "off-on" and "lamp test" circuits through FU10. This transformer also supplies 115V a.c., 60 Hz to operate the blower, R2, R3, and R4 through FU11.

When power is supplied to PUP, 15V from the control transformer is supplied to the "OFF" push button. Current flows through the "OFF" button, through a normally closed contact on R1, and through a diode to the "OFF" lamp. This lamp is then lighted, showing that primary power is supplied to PUP. If "LAMP TEST" is pushed, 15V a.c. is supplied to all lamps on the PUP amplifier control panel through diode decoupling circuits which prevent this voltage from back feeding into any other circuits.

If the "ON" button is pushed, current flows from the control transformer through the "OFF" button, the "ON" button, and the 18 Ω resistor to the coil of R1. A normally open holding contact on R1 across the "ON" button latches R1. Current is also supplied to the "ON" lamp through a diode. The "OFF" lamp is extinguished by the closing of R1.

Latching in R1 causes current to flow from the 115V winding on the control transformer through FU11, a normally open contact on R1, and a normally closed contact on R3 (time delay relay) to coil of R2 (blower relay). R2 is pulled in causing 115V to be supplied to the filament blower. As air flow increases, the air flow switch is closed supplying power to R4 (filament relay) through a normally open contact on R1. When R4 pulls in, 208V 3 Phase power is supplied to the primary of the filament transformer.

If the "OFF" button is pushed, power is interrupted to the coil of R1 and it unlatches. The "ON" lamp is extinguished and the "OFF" lamp lights. The normally open contact in series with R4 opens and R4 drops out removing power from the filament transformer. The normally open contact on R1 feeding R2 also opens but a normally open contact on R2 in parallel with the normally open contact on R1 maintains R2 latched in. When R1 drops out, current flowing through the normally open R2 contact is directed through a normally closed R1 contact to the anode of a 1N5059 diode on PC board B15. This rectified current slowly charges 500 μf of capacitance. When the capacitors charge to the breakover potential of the GE-X13 diode, the energy in the capacitors is dumped into the coil of R3. R3 then momentarily pulls in, interrupting current flow to R2 and unlatching it. At this point, power is removed from the blower and PC board P15. The interval between pushing "OFF", and blower shutdown is called "blower over run". During this interval, power is fed from the "OFF" lamp via a normally open contact on R4 to the "blower overrun" lamp. This lamp indicates that

the blower will remain running for a small length of time after the "OFF" command to prevent tube hot spots.

All of the lamps on the PUP amplifier control panel are type 330, 14V, 80 mA lamps. Some of the lamps receive power from a 15V winding on the control transformer. A diode in series with these lamps reduces the rms voltage fed to the lamps by 3/10 to about 10.5V rms. This provides long lamp life. Other lamps on the amplifier panel receive their power from a 12V d.c. supply. The voltage is again reduced to about 10.5V rms this time using series resistance.

The filament transformer assembly (see Drawing #7513613, Appendix D) supplies most of the power used in PUP for control, bias, and filaments. It provides, along with rectifiers mounted on it, the following:

1. 6.0V a.c. at 180 amp total for the filaments of the 4CX250B tubes (two windings).
2. 115V a.c. at 6 amp max for the M5000 preamp.
3. 115V a.c. at 3.5A max for AUX power (front panel) recepticals).
4. 14V a.c. for a floating d.c. supply on the plate overload PC board B2.
5. 115V a.c. at 0.5 amp to operate the plate relay coil (R5), dump relay coil (R6), and running time meter.
6. -200V d.c. for tube bias.
7. +12V d.c. 6 amp max for control circuit power.
8. +15V, AUX power to damped sine generator or other equipment as may be added at a later date (open circuit voltages shown).
9. -15V, same as 8.
10. +22V, same as 8.
11. -22V, same as 8.

The d.c. potentials are produced using 3 Phase full wave rectifiers. The inputs to these rectifiers have resistors in series with them to act as fuses should a rectifier fail.

PLATE POWER CIRCUITS:

The plate transformer supplies the necessary power for the amplifier plate circuit. The primary of this transformer is supplied with 208V 3 Phase at about 30A (see drawing 7513614, Appendix D). Power is fed to it through the plate primary overload detector, three 30 amp fuses, and normally open contacts on plate relay R5. The plate transformer has 4 sets of secondaries (see drawing 7513757, Appendix D). Three of these sets feed full wave 3 Phase bridge rectifiers; two have an output of 350V and the third produces 100V. The fourth winding supplies 100V a.c. 60 Hz to operate a safety light.

The outputs of each rectifier bridge are filtered with large capacitors and the outputs are "stacked", that is, the rectifier outputs are wired in series with one 350V output rectifier on the bottom, the 110V rectifier in the middle, and the last 350V rectifier on top.

This series string of rectifiers produces the following outputs: +350V (output of bottom rectifier, +450V (output of 100V rectifier), and 800V at the top. The 350V output is used to supply all 4CX250B screen grids. The 450V output is used for driver and IPA plates and 800V is used for the power amplifier plates. By series stacking the supplies, the power supply is able to accommodate screen current of either polarity. (Screen grid currents in tetrodes can be negative due to secondary emission from the screen grid.)

Primary power to the plate transformer is controlled by relays R5 and R6 and PC board B3 (drawing #7513614, Appendix D). When a current from the control logic is applied to the gate of the TRIAC on PC board B3, a.c. current flows from a 115V winding on the filament transformer through the coil of R6, through the TRIAC, to GND. R6 then pulls in. A 100 ohm resistor connected from the 800V plate supply through two normally closed contacts on R6 to ground is open circuited (drawing #7513757, Appendix D). Current also flows through a normally open contact on R6 to the coil of R5. R5 then pulls in supplying 208V a.c. to the primary of the plate transformer.

When d.c. current is removed from the gate of the TRIAC on PC Board B3, both relays R5 and R6 drop out. Power is removed from the plate transformer's primary and the 100 ohm resistor is again shunted from the 800V supply to ground, discharging the power supply capacitors.

Power for the coils of R5 and R6 is supplied by a winding on the filament transformer to ensure that power cannot be supplied to the plate circuit in case of control circuit fault if the filament transformer is not on.

The 800V from the top rectifier is fed through FU16 to PC board B2 (see drawing #7513757, Appendix D). Here the current splits into two paths. Each path goes to one of the 24 tube power amplifiers through a 0.3 Ω resistor (made up of three 1 Ω resistors in parallel). The 0.3 Ω resistors are part of a current splitting network which directs a small percentage of the plate current to flow through the LEDs (light emitting diodes) in the MCT2E opto-isolators. The two paths in the current splitting network are: (1) the 0.3 Ω resistance, and (2) the series path of 10 Ω, MCT2E, 220 Ω, and an NPN transistor (saturated). Thus, the photo current in the phototransistor in the MCT2E is ideally a replica of the plate current. The avalanche diode and transistor circuit are used to protect the MCT2E from excess currents and transients. The opto-isolators are used to interface the overload sensing circuits which operate within a few volts of ground to the plate circuit which is 800V above ground.

The rectifier stack supplies 450V to the plates of the driver and both IPA amplifiers through FU16, one ohm resistors on opto-isolator board B2, and the current sensing resistors: CSR2, CSR3, and CSR4. CSR2, CSR3, and CSR4 are used along with the front panel meter to monitor plate currents in their respective amplifiers.

The driver and both IPA amplifiers each have their own individual plate current sensing 1 ohm resistors on Board B2. The potential drop across each of these resistors is fed to a simple one transistor op-amp type circuit which has a 470 Ω resistor in its input and the LED of an opto-isolator in its feedback path. The LED current is then directly proportional to the plate current. The opto-isolators interface this replica of each plate current from the 450V level of the plate supply to the bias regulators which operate near ground potential. A diode "or" type circuit connected to the three 1 ohm resistors provides an input to a fourth one transistor op-amp circuit which uses 330 Ω in its input and the LED of a fourth opto-isolator in its feedback path. The current in this LED is therefore proportional to the largest of the three plate currents. This replica of the largest plate current is interfaced to the place overload circuits by the fourth opto-isolator. Power for PC Board B2 comes from a filtered full wave rectifier supplied from a 14V winding on the filament transformer.

Power for the screen grids of all tubes in the 5 amplifiers is supplied from the 350V point on the rectifier stack, through FU17, through individual overload current sensing resistors on PC Board B1, through individual ammeter shunt circuits on B1 and then to each amplifier.

Each amplifier's screen current is monitored by switching the front panel ammeter across a current sensing resistor located on the d.c. side of a bridge rectifier. Screen current flows into and out of the a.c. side of the rectifier. Thus, screen current always flows through the current sensing resistor in the same direction resulting in an upscale ammeter reading regardless of screen current direction.

Five screen overload current sensing resistors, one for each amplifier, are sized such that the potential drop across them is the same at overload for each amplifier. (Screen overload for the power amplifiers is 450 mA and the current sensing resistor value is 5 Ω; overload for the driver and IPAs is 200 mA and the resistor value is approximately 11.25 Ω. Voltage drop is about 2.25V at overload.) A five-diode "or" circuit feeds a simple one transistor op-amp circuit which has 220 Ω in its input and an LED from an opto-isolator in its feedback path. The LED current is then proportional to the largest screen current normalized to its overload value of current. The opto-isolator interfaces this current replica from the 350V level to the overload detection circuits.

CONTROL CIRCUITS:

The control circuits, located in a box behind the front panel of rack number two, controls the following functions:

1. Control of plate voltage.
2. Control and regulation of tube bias.
3. Sensing overloads, incorrect voltages, and interlocks.

When PUP is turned on, a "WAIT" state occurs. The "WAIT" state lasts for about one minute, and it gives the tubes a chance to warm up. The unit then goes to "STAND BY". Plate power is off and all tubes have a high negative bias. The unit now awaits the "OPERATE" command. If the unit is not or was not in overload, if all interlocks are satisfied, and if all monitored voltages are correct, the unit will accept an "OPERATE" command. Pushing "OPERATE" turns on the plate supply voltage, and supplies the correct bias to the control grids of

the tubes. Should any condition of overload, incorrect voltage, or open interlock occur, the system is returned to "STANDBY".

The plate supply is not large enough to handle all five amplifiers operating continuously. Therefore, under normal operation in the "OPERATE" state, the driver AMP and both IPA amplifiers are biased on. Plate current of 2.5 AMPS flows in each. The control grids of the 24 tube power amplifiers, however, are held highly negative to prevent tube conduction. Upon command from the external signal source, the power amplifiers are biased into conduction (7.2A Ip for each AMP) long enough to amplify the required signal and then the bias is returned to a level below tube cutoff.

PUP can also amplify cw type signals, but at 1/2 of its normal output power (1kW instead of 2kW). A front panel switch selects either one of the 24 tube power amplifiers to operate by itself. Under this condition, the driver, one IPA, and the corresponding PA are biased on in the "OPERATE" mode. This cw mode is also used for metering plate and screen currents in the individual amplifiers.

The control circuits are shown in drawing 7513755 (Appendix D). No attempt will be made here to describe each circuit detail, the basic circuit operation only will be discussed. Integrated circuits will be referred to by their package number, and where more than one gate exists in a package, the output pin number will follow the package number. Example: the plate primary overload detector feeds gate 14-3 through filter F10.

WAIT FUNCTION:

After "ON" is pushed and power is applied to the filament transformer, 12 volts is available to operate the control circuits. This unregulated 12 volts comes in through filter F9 and is applied to IC20 (309K) among other things. The 5V output of IC20 supplies power to most of the logic in the control circuits. When the 5V is supplied to IC16 (555 timer) its output (pin 3) immediately goes high. IC16 is the "WAIT" timer, and its output will stay high for one minute and remain low thereafter. The time interval is determined by the two 39 μf capacitors and the 750K resistor. The high output from pin 3 of IC16 lights the wait lamp, holds the standby-operate flip-flop (gates 15-6 and 14-3) in the "STANDBY" state (output of gate 15-6 high) and holds both overload flip-flops (gates 14-8 with 14-11 and 13-3 with 13-6) in their nonoverload states.

Thus the "WAIT" timer, in addition to ensuring sufficient tube warm-up time, also resets any incorrect states that may have occurred in the control circuit during power-up.

Standby-Operate Functions: The state of a flip-flop composed of gates 15-6 and 14-3 determines whether PUP is in the "STANDBY" or "OPERATE" state. If the "WAIT" period has timed out, and all overload conditions are satisfied, the logic signal on pin 5 of gate 15-6 will be high. The flip-flop can now be set to either of its states by pushing either the "STANDBY" pushbutton or the "OPERATE" pushbutton. The output of the flip-flop is taken from pin 6 of gate 15-6, and pin 6 is high in the "STANDBY" state. Pin 6 is coupled through a 4.3V Zener Diode to the emitter of a transistor whose base is biased from the 12V and 5V supplies. If pin 6 is low ("OPERATE" state), the transistor will not turn on if the 5V supply is below 4.3 volts or if the 12V supply is below 10 volts. The collector of this transistor is coupled to the base of a second transistor whose emitter drives the operate lamp and whose collector supplies current through filter F5 to the gate of the triac on PC Board B3. (This triac controls primary power to the plate transformer.) Thus, if the 5V and 12V supplies are not deficient, switching the flip-flop (gates 15-6 and 14-3) to the "OPERATE" state (pin 6 on gate 15-6 goes low) causes illumination of the operate lamp and power to be supplied to the primary of the plate transformer, supplying plate power to the tubes. A circuit from the operate lamp driver through a 36K resistor extinguishes the standby lamp when the operate lamp is illuminated.

The "STANDBY HOLD" circuit (PC Board B16) operates in parallel with the "STANDBY" pushbutton. When the "STANDBY" pushbutton is pushed, power is removed from the plate transformer and relay R6 (see drawing #7613268, Appendix D) shunts a 100 Ω resistor from the plate supply to ground. At the same time, IC22 (555) is triggered. Its output saturates a transistor whose collector circuit is in parallel with the "STANDBY" pushbutton, and in effect, holds it "IN". The "OPERATE" pushbutton is then inoperative until IC22 times out (about 3 seconds). This prevents an operate command current from causing R6's contacts to open while a heavy discharge current is flowing through them.

Bias Control: Grid bias for all amplifiers is obtained from a 200V source supplied by the filament transformer through filter F17. It is then supplied to five bias regulators, one for each amplifier. The regulators for the driver, IPA A, and IPA B are essentially identical feedback regulators which actually

sense plate current in their respective amplifiers, and regulate this current to a desired value (2.5A). The regulators for both power amplifiers are constant voltage feedback regulators which operate the power amplifiers at fixed bias.

Consider the regulator for IPA B: IPA B's plate current is to be regulated at 2.5A. As previously discussed under plate power circuits, IPA B's plate current is sampled on PC Board B2, and fed to an opto-isolator. The opto-isolator's output phototransistor has a collector current proportional to the plate current of IPA B. The collector of the phototransistor is connected to the summing junction of a 741 OP-AMP (IC5) through B2-17, RG1740 cable, Jack J3, and a 680 Ω resistor. The emitter of the phototransistor is grounded. An adjustable reference current, opposite in direction to that of the collector current of the phototransistor, is also fed to the summing junction of the 741. The reference current is obtained from a 12 volt regulated supply (IC21) through a bias-switch transistor, a 270 Ω resistor, and a 1.2K Ω resistor. The 714's positive input is biased at 6 volts.

Actual bias is supplied to the grids from the -200V supply through a series impedence consisting of two 68K resistors in parallel, and a shunt control transistor, type 2N4347. The output of the 741 OP-AMP is interfaced to the 2N4347 shunt transistor by a 2N5344 transistor and a 2N3583 darlingtoned to the 2N4347. Output from the shunt control transistor is taken from its emitter, through B6-32, through a 5.6 Ω resistor, through filter F16, to terminal 6 on IFI power AMP unit B where it feeds the grids of the six 4CX250B tubes in IPA B. The sampling of the Plate current of these tubes on Board B2 then closes the loop. Voltage gain from the output of the 741 OP AMP (IC5) to the tube grids is about 13. IC5 is connected as an integrator with a 39 μf capacitor in its feedback circuit. The output of the IC5 is ideally the integral of the difference between the reference current and the opto-isolator's collector current. The gain of this integrator is set low so that the control loop responds slowly to changes in collector current. This makes the amplifier appear to operate with fixed bias during amplification of short pulses. When a large amplitude pulse or cw signal is applied to a single end class A amplifier of the type used in PUP, the amplifier will to some extent distort the signal or pulse. The percent a.c. plate current shift is essentially the same as the percent second harmonic distortion. When this change in plate current is applied to a

regulator which responds slowly compared to the width of the pulse being amplified, the tube bias remains essentially constant during the pulse.

The aforementioned bias switch (whose collector ties to B5-7) controls the 12 volt reference applied to the IPA AMP B Bias Adj. Pot. When this bias switch transistor is turned off, the reference current fed to the 741 IC5 goes to zero. The control regulator will then regulate the plate current in IPA B to zero, cutting off this amplifier. The bias regulators for the driver and IPA A work in the same manner.

Consider the regulator for PA-A. This bias regulator acts as a constant voltage source to operate the amplifier with fixed bias. This regulator can also be switched to provide a high negative output to cut off plate current in the power amplifiers.

Minus 200V is supplied through a series element consisting of two 68K resistors in parallel, through 470 Ω, to terminal B6-5, through 5.6 Ω, through filter F12 to terminal 7 on IFI unit power amplifier A where it feeds the grids of the 24 type 4CX250B tubes in PA A. The voltage at B6-5 is shunt controlled by a 2N4347 transistor. Two type 2N3583 transistors are darlingtoned to the 2N4347 transistor and a differential pair consisting of two MM 4001 transistors feeds the darlington. One transistor's base is fed with two currents. One current is a feedback current obtained from the voltage at B6-5 (grid bias voltage) dropping across a 43K resistor. The other current is a reference current, opposite in direction to the feedback current, supplied through a 4.3K resistor, and the 5K "PA AMP B Bias Adjust" potentiometer from the 12V reference supply (IC21). The regulator, like a simple OP-AMP with 43K in its feedback path and 4.3K in its input, tends to balance the currents at the input of the differential pair to zero. Thus, 4 volts at the wiper of the 5K bias adjust pot, would give -40V at the tube grids.

The emitters of the differential pair (MM 4001's) are fed through a 2.7K resistor, B6-8, B5-3, and bias switch transistor to the 12V reference source (IC21). Normally the regulator's output (term. B6-5) is at a level determined by the bias adjust potentiometer. When the bias-switch transistor (collector connected to B5-3) is turned off, collector current in the differential pair goes to zero, and the voltage at terminal B6-5 goes highly negative, cutting off the power amplifier. The bias regulator for PA-B works in the same manner.

The bias circuits within the IFI unit amplifiers contain large capacitors (50 μf or more) in shunt with the bias supply. When a bias switch transistor is turned on after being off, the bias rises from its high negative value to its normal operating value. The rate of rise of this bias voltage must be limited to prevent excessive current from flowing in the shunt control transistors due to capacitor discharge. In the regulators for the IPA and driver amplifiers, the slow integrator response limits the voltage rate of the rise of the bias. In the power amplifier bias regulators, slew rate limiting is accomplished by a 0.1 μf capacitor placed between the collector and base of one of the MM 4001's constituting the differential pair. The PA bias regulators take about 20 ms to come up to operation.

The load capacitance of the bias circuits is isolated by 5.6 Ω resistors, from the points in the bias regulators where feedback is taken. This, together with the slew-rate limiting elements gives these regulators good stability.

When "OPERATE" is pushed, pin 6 of IC15-6 goes low. This, in addition to turning on the plate power supply, turns off the NPN transistor coupled to pins 2 and 6 of IC17. IC17 is the bias delay timer and about 1/4 of a second after the "OPERATE" command, its output (pin 3) goes low. This saturates an NPN level-shifting transistor which in turn, saturates the bias switch transistor for the driver AMP. B5-7 is pulled up to 12 volts, causing plate current to flow in the Driver Amp. When pin 3 of IC17 goes low, the output of gate 11-11 goes high. This "HIGH" is coupled into at least one input on gates 10-6, 9-8, 9-6, and 9-12. The outputs of any of these gates can now go low depending upon the logical combination of signals obtained from the mode switch through filters F1 and F2 and the "BIAS-ON" signal obtained from pin 6 of IC8-6. Gates 9-12 and 9-6 will each control the bias to power amplifier PA-A and PA-B respectively, along with their respective "BIAS-ON" lamps (through terminals B5-1 and B5-2). Gates 10-6 and 9-8 will control the bias to amplifiers IPA-A and IPA-B respectively.

The logical inputs to the above four gates will control the bias to the amplifiers in accordance with table 1. When PUP is returned to standby, the output on pin 3 of IC17 goes high, the output of gate 11-11 goes low, forcing the outputs of gates 10-6, 9-8, 9-6, and 9-12 high. All bias switch transistors are then cut off, and all the amplifies are biased to cutoff.

Table 1

AMPLIFIER BIAS CONDITIONS

State	Position of Mode Switch On Front Panel	Driver Bias	IPA A Bias	IPA B Bias	PA A Bias	PA B Bias
Wait - Standby	---	OFF	OFF	OFF	OFF	OFF
OPERATE	"NORMAL"	ON	ON	ON	OFF*	OFF*
	"AMP A BIAS ON"	ON	ON	OFF	ON	OFF
	"AMP B BIAS ON"	ON	OFF	ON	OFF	ON

"ON" indicates plate current is flowing.

"OFF" indicates that the grids are biased highly negative and no plate current is flowing.

"OFF*" is the same as "OFF" above, but a command from the signal source can bring up the bias to its normal operating level for up to 150 ms so plate current can flow and pulse can be amplified.

The "AMP A BIAS ON" and "AMP B BIAS ON" lamps will be illuminated when the tubes in their respective amplifiers are biased "ON".

The bias-on signal on pin 6 of gate 8-6 has been processed through two safety timers. Normally a bias-on pulse (positive going) is obtained from the signal source and is applied to J8. This bias-on pulse should be between 25 and 150 ms long depending on the length of time needed to amplify the desired signal. The bias-on pulse should remain low for at least 100 ms. Should the bias-on pulse match these conditions, it will be processed unaltered (except for an inversion) through B5-21, gate 116, gate 8-8, gate 15-8, gate 8-11, and gate 8-6 to the bias-on gates 10-6, 9-8, 9-6, and 9-12.

When the bias-on pulse at J8 goes positive, IC18 (555) will start timing. If the applied bias-on pulse exceeds 150 ms in length, timer 1C18 will time out, its output on pin 3 will go low, causing pin 8 on gate 15-8 to go high. This will force pin 6 of gate 8-6 high, biasing off the power amplifiers. At the end of the bias-on pulse, pin 11 of gate 8-11 will go low. This will trigger IC19 (555 timer) and its output (pin 3) will go high and remain high for 100 ms. The resulting low logic level applied to pin 4 of gate 8-6 will prevent its output (pin 6) from going low for 100 ms. The power amplifiers are therefore assured of at least 100 ms "OFF" time and a maximum "ON" time of 150 ms.

The bias-on pulse circuits are only operational in the normal mode of operation (see table 1).

Overload Detection: The outputs of the opto-isolators used to interface the overload circuits on PC Boards B1 and B2 (as described under plate power circuits) to the control circuits are connected to them with RG 174U cable through Jacks J4, J5, J6, and J7. The output stage of these opto-isolators is a phototransistor, and the circuits on Boards B1 and B2 are adjusted such that a collector current of 3 to 4 mA flows in these phototransistors when the currents which they interface reach their respective overload levels. The collectors are biased from a 12 volt source (IC21) through calibration resistors of about 1.5K to 2K which are trimmed to provide exactly 6 volts drop across them when overload is reached. IC's 1, 2, 3, 4 (311 comparators) compare the voltage dropped across the calibration resistors to a fixed 6V potential derived from the 12 volts source. When the potential drop across any one of the calibration resistors exceeds 6V (overload condition) the open collector output of the comparator is pulled low. All four comparators have their outputs tied in parallel and connected to a flip-flop consisting of gate 14-8 and gate 14-11. A low output from any of the comparators sets this flip-flop to its "OVERLOAD" state. This lights the "OVERLOAD" lamp and returns PUP to "STANDBY".

A solid state overload detector is inductively coupled to the primary leads of the plate transformer. If a primary overload should occur, a normally closed contact inside the overload detector and connected from filter F10 to ground will open. Should this occur, a second overload flip-flop consisting of gates 13-3 and 13-6 will be set to its "OVERLOAD" state (pin 6 of IC13-6 goes high). PUP will then be returned to standby, and the "OVERLOAD" lamp will be illuminated.

Low Voltage Interlocks: As previously discussed, a low 5V supply or a low 12V unregulated supply will prevent primary power from being applied to the plate transformer. In addition, PUP has several other voltage monitors. These are designed to look more for supply failure than for an "OUT OF TOLERANCE" supply.

The 12 volt reference supply interlock: An NPN transistor sinking current from pin 9 of IC16-8 is held in saturation with current flowing from the 12 volt regulated supply through an 8.2V avalance diode and a 1.8K resistor. This transistor will come out of saturation when the 12 volt supply drops below about 10 volts causing PUP to switch to standby and lighting the overload lamp. The

12 volt reference voltage is necessary for proper operation of the overload and bias regulator circuits.

The -200 volt interlock: AN NPN transistor (whose emitter ties to B5-23) has its base biased 10 volts negative by a 10V avalanche diode. The transistor is held in saturation by emitter current obtained from a voltage divider (22K and 200K) from the -200 volt supply. The transistors collector drives a second transistor whose collector circuit is in parallel with the outputs of the 311 comparators used for overload sensing. Should the magnitude of the -200V source drop below about -110 volts, the transistor would come out of saturation, causing saturation of the second transistor, causing an overload condition and returning PUP to standby. The -200V supply is necessary for tube bias.

Bias check interlock: The grid bias fed to the amplifiers is usually between -20V and -50V. Any failure in the system which causes the bias to be excessively negative will do no harm to the amplifiers. If the magnitude of the bias is too low, excessive plate currents can flow. A wire called "BIAS CHECK" has diodes coupling it to all five bias lines such that the wire will always have a potential equal to the highest (cloest to zero) bias voltage feeding any amplifier. This wire is connected to B5-23, and if this wire rises above -10 volts, it turns off the first transistor mentioned in the paragraph above. This cuases an overload indication, and returns PUP to standby, if it was in operate. This interlock will also prevent the "OPERATE" command if any bias line is higher than -10 volts. This will happen if any tube develops a grid to cathode short. (A grid to cathode short will not damage the shunt type bias regulations, but the 1/10 A fuses in the bias regulators for the power amplifiers may blow.)

Door Interlock: A loop is connected from filter F11, through TB4-8 (drawing 7513757, Appendix D) through as many interlock switches as desired, and then to ground. The opening of any switch in the Loop will put a logic high on B5-19. This will return PUP to "STANDBY" and prevent an "OPERATE" command. It will also light the "INTERLOCK OPEN" lamp on the front panel. The loop normally contains two door interlock switches (closed when the rear doors are in place) but as many other switches as desired for safety may be added to the loop at TB4-8.

DAMPED SINE GENERATOR:

The damped sine generator located in the top of rack #1 (right hand rack) is PUP's internal signal source. When it receives a fire command, it will produce a damped sine pulse at any one of 12 frequencies. It will also provide a correctly timed bias-on pulse to turn on the power amplifiers. The block diagram in figure 18 shows how the damped sine is produced. A cw carrier is generated at the frequency of the desired damped sine. This carrier is then modulated to produce the damped sine. The envelope generator produces a pulse with the same shape as the envelope of the desired damped sine, and the zero-crossing detector is gated by the trigger signal applied to it from the timing logic. When the trigger line to the zero-crossing detector goes low, the zero-crossing detector looks for two zero crossings (with the same slope) of the carrier. On the first crossing, it generates a positive scope trigger pulse, and on the second crossing, the envelope generator is gated into operation, producing a damped sine. All of the circuits are reset when the trigger line returns to a high level. When the timing logic receives a fire command from the outside world, it immediately sends a "Bias-on" command to the PUP amplifier control circuits. It then waits 24 ms and applies a low level to the trigger of the zero-crossing detector. Within two periods of the carrier, a damped sine is generated and sent to the amplifier. One hundred twenty ms after the fire command is received, the bias-on pulse is terminated, and the trigger to the zero-crossing circuits is returned to a logic high. Drawing 7613267 (Appendix D) shows the schematic of the damped sine generator. Box A shown on this drawing contains the carrier oscillator, envelope generator, and modulator. The schematic for this box is shown on drawing 7613266 (Appendix D). The zero-crossing detector and control logic are contained in Box B, and its schematic is on drawing 7613114. Box A (drawing 7613266) is a sectioned aluminum box which houses the carrier oscillator in one section, the carrier buffer and leveler in the second section, the envelope generator and modulator in a third section, and the power supply regulators for the above three circuits in a fourth section. The oscillator, housed in section 1 of Box A, uses an MC1648 emitter coupled oscillator IC and LC resonators to determine the frequency. Twelve LC resonators are switch selected. The output from the oscillator is taken from pin one (the collector of a transistor) and fed through RG174U cable to section 2. The signal on this cable is essentially a square wave. The buffer stage in section 2

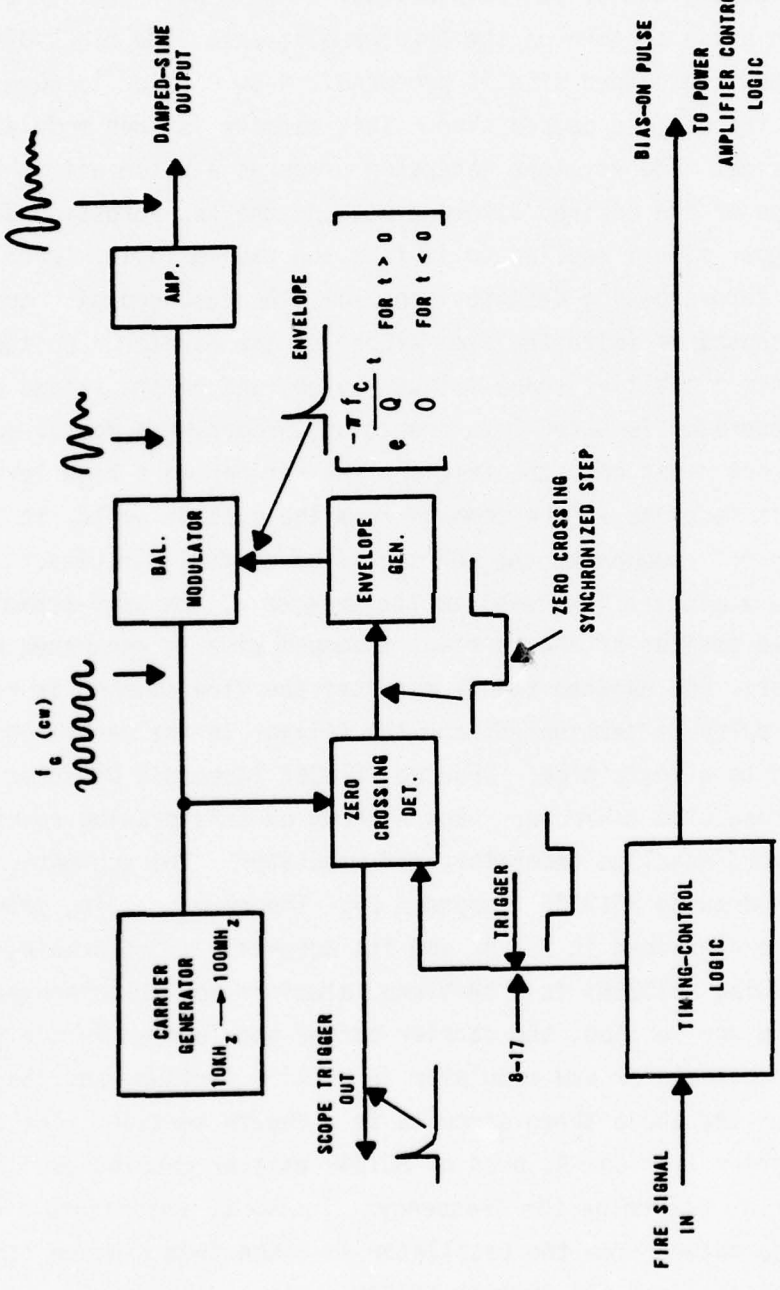


Figure 18. Damped Sine Generator Block Diagram

converts this square wave to a sine wave and regulates its amplitude. In section 2 of Box A the signal from the oscillator feeds a transistor differential pair (Q1 and Q2) whose gain can be controlled by controlling emitter current to the pair. The output of Q2 drives an LC resonator (buffer tank) which is tuned to the same frequency as the oscillator. A sine wave a.c. voltage is developed across the tank circuit at the carrier frequency. This a.c. voltage, whose amplitude is a function of the emitter current in the 2N5771 differential pair, is buffered to a low impedance level by the LH0063C. The output of the LH0063C is a low impedance source of carrier signal whose level is maintained at approximately 2 volts P-P for all carrier frequencies by a leveling control loop. It operates as follows:

Carrier output from the LH0063C is fed through a 0.2 μf capacitor to the cathode of a HPD5082-2800 diode. This diode, together with the 0.2 μf capacitor, acts to clamp the sine wave's negative peak to GND. The resulting d.c. potential at the cathode of the diode is compared to a referenced d.c. potential available from one of the carrier amplitude adjust pots. The difference is amplified by the 308A OP-AMP (K2), and its output controls the emitter current of the differential pair (Q1 and Q2) through transistors Q3 and Q4 and therefore controls the amplitude of the carrier at the output of the LH0063C. Thus the loop is closed, and the carrier output is regulated to 2V P-P.

Carrier from the output of the LH0063C is fed to Jacks J2, J3, and J4 located on Box A through resistor networks to obtain a specific Thevenin output voltage and impedance for each Jack. Since the output of the LH0063 is regulated to a constant amplitude, the Thevenin impedances at the Jacks are primarily determined by the networks between the LH0063 and the Jacks. Jacks J3 and J4 have approximately 50 Ω Thevenin impedances. J4 feeds the front panel carrier monitor which will deliver IV P-P into 50 ohms, J3 feeds the zero-crossing detector, and J2 feeds carrier to the modulator.

The carrier from Jack J3 on Box A is fed to Jack J1 on Box B. Here it feeds the zero-crossing detector circuits (drawing 7613114, Appendix D). The carrier signal is decoupled, d.c. referenced to V_{BB} (about -1.3 volts), and then applied to a comparator, implemented from two gates in an MC1692L QUAD Line receiver. The gates in the MC1692L act as differential amplifiers. The first gate (gate 1-15) is wired as a schmitt trigger. Thus, the output of this comparator (pin 15 on gate 1-15) switches when the carrier signal crosses zero. A relay (RL1)

in the input circuits of gate 1-2 is used to interchange the inputs so that the positive transition at the comparator's output can be selected to occur on either the positive slope zero crossing or the negative slope zero crossing of the carrier. Since the envelope generator is triggered into operation by a signal from this comparator, the polarity of the damped sine produced by the system is dependent upon which slope is selected. Two potentiometers (one for each polarity as selected by RL1) in the comparator's input circuit are used to adjust a small bias voltage which is applied to the comparator to compensate for offset error. The output of the comparator is fed to the clock inputs of two "D" type flip-flops (MC1670, IC3, and IC4), IC3's set input is normally held high. When the trigger at terminal 8-17 (PC board 8) goes low, indicating a damped sine pulse is desired, the set input of IC3 goes low. On the next carrier zero crossing the positive transition from the comparator (1-15) clocks IC3, and the logic zero on its "D" input is transferred to the Q output. The positive transition on IC3's Q output is fed to Jack J6 and then to the front panel of the damped sine generator to be used as a scope trigger. The negative transition at IC3's "Q" output is fed to the set input of IC4, and the next carrier zero crossing will cause IC4 to transfer the logic zero on its "D" input to its "Q" output. Thus, the negative transition of IC4's "Q" output occurs one carrier cycle after the scope trigger on J6. The negative transition on IC4's "Q" output is buffered to 4 Jacks (J5, J4, J3, and J2) by an MC1692 QUAD line receiver. The negative transitions at these Jacks are used to trigger the envelope generator. (Jacks J3, J4, and J5 are unused at this time.) The levels at Jacks J2, J3, J4, and J5 remain low until the trigger at terminal 8-17 is returned to a high state. At this time, the circuit is reset to await another trigger. Return now to drawing 7613266.

The modulator and envelope generator are located in Box A, section 3. The envelope waveform is the product of an exponential function and a step function. The exponential function is generated by an RC time constant, specifically, the switch selected "R" and "C" tied to point E in the circuit. The exponent generator circuits are d.c. referenced to -8 volts. Normally current in Q6 holds

point E about 4 to 5 volts above the -8 volts reference. A negative transition from the zero-crossing detector (J2) is applied to J7 on Box A, section 3, and then to Q5. This negative transition causes Q5 to turn on and Q6 to turn off. Point "E" in the circuit then decays exponentially to -8V, starting in concidence with a carrier zero crossing. The decaying exponential voltage at point "E" is buffered and converted to an exponentially decaying current in the collector of Q10 by Q10, IC4 and a 330 ohm resistor. The collector current in Q10 is normally flowing through Q8 to ground. The negative transition applied to J7 from the zero-crossing detector is processed out of J6 into J5 and applied to the base of Q8. This negative transition at the base of Q8 will turn it off and turn on Q9. Since the Q8-Q9 pair is switched at the same time as Q6 is turned off, the collector current of Q10 is switched to Q9 just as the current starts to decay. The collector current of Q9 therefore has the desired envelope shape, i.e., it has a fast rise followed by an exponential decay.

The damped sine is generated in balanced modulator IC6. Here the carrier (obtained from J2 through J8 to pin on IC6) is multiplied by the envelope (obtained from the collector current of Q9 dropping across 62 ohms and applied to pin 4 of IC6). The damped sine output from IC6 (pin 12) is fed to J9 on Box A.

Detections of a carrier zero crossing, switching of Q6 and Q8, and conversion of an exponential voltage to the current do not occur instantaneously. There is a time delay between the carrier zero crossing and the negative transition on J7. It takes time for Q5 and Q6 to switch, and it takes time for the decaying exponential to propagate through IC4 and Q10. A delay line between J6 and J5 allows Q8 to switch at the same time as the decaying exponential current arrives at its emitter, and a delay line between J2 and J8 delays the exact carrier zero crossing which was detected by the zero-crossing detector to appear at the input to the modulator IC6 coincident to the start of the envelope waveform. Thus, the output of IC6 is an accurate damped sine at all frequencies.

The voltage at "E" before a negative transition on J7, determines the amplitude of the envelope waveform, and hence, the amplitude of the damped sine. Since the value of "R" is changed to obtain different damping time constants, and Q6 is not operated as a saturated switch, the collector current of Q6 must be varied to obtain a constant voltage at "E" for all values of "R". This is accomplished by means of a servo loop consisting of IC5 and Q7 along with Q6, IC4, and Q10 to complete the loop. Before a negative transition on J7, while

Q6 is on, the voltage at the emitter of Q10 (which is the same as the voltage at "E") is compared to a reference voltage obtained from potentiometer z. The difference is amplified by IC5 and fed VIA Q7 to the emitter of Q6 where it controls the collector current of Q6. This servos the voltage at "E" to a fixed value independent of the value of "R". When a negative transition appears on J7, this servo loop is disabled by the switching off of Q6, and the generation of the envelope occurs. When the negative logic level is removed from J7, Q6 is again turned on, and the servo loop resets the voltage at "E" to its initial value.

The carrier generator, buffer, and envelope generator modulator are located in different sections of aluminum Box A. The "damped sine Frequency" selector switch is a wafer switch with a long shaft which extends through sections 1, 2, and 3 in Box A, and operates wafer decks in each section. In section 1, the switch selects the proper oscillator tank circuit for the desired damped sine frequency. In section 2, it selects the proper buffer tank circuit. In section 3, it selects the proper "R" and "C" so as to provide proper damping of the damped sine at the selected frequency.

The damped sine output from J9 on Box A is fed to J1 on Box C. Box C (see drawing 7613267) contains the output booster amplifier which feeds two jacks (J1 and J2) on the front panel of the damped sine generator. This amplifier consists of a two transistor, feedback amplifier stage having a gain of about 8 and a bandwidth of about 200 MHz. This is followed by an LH0063C buffer AMP (IC3) whose gain is about 1. Some phase lead is added to the input of the transistor amplifier (the 8 to 38 pf trimmer capacitor) in an effort to compensate for high-end deficiencies in the LH0063C. The magnitude of the damped sine at the output of IC3 is about 1.5V P-P, and this drives Jack J2 on the booster AMP through 47 ohms. Jack J2 on the booster AMP, feeds the damped sine output Jack, J1, on the front panel of the damped sine generator. This output has a Thevenin source impedance of 50 Ω (approx) and will supply 750 mV P-P into 50 Ω. The damped sine monitor output Jack, J2 on the damped sine generator front panel, is supplied from Jack J3 on the booster amplifier which in turn is supplied with signal from the output of the two transistor feedback amplifier stage through a divider network. The amplitude of the signal at the damped sine monitor output (J2) is 100 mV P-P into 50 Ω, and J2's source impedance is about 50 Ω.

The timing and control logic is located in box B (drawing 7613114, Appendix D). When the fire switch is pushed, it puts a logic low on J9 which in turn causes the output of IC5-3 to go high. This turns on Q1 and its collector goes low, coupling a low into IC5-11. The output of IC5-11 (pin 11) will go high and stay high until the 0.47 μf capacitor connected to pin 13 of IC5-11 charges enough to provide a logic high at pin 13; at which time pin 11 of IC5-11 goes low. This logic-high pulse at pin 11 of IC5-11 is coupled through IC6-3 to the hold-off monostable IC9 and to the bias-on monostable IC7. Both of these monostables are triggered by the pulse. The output of hold-off monostable (pin 3 of IC9), will go high and remain there for 250 ms. During this time, it will turn on Q2 and also hold on Q1. This will prevent any further fire pulses which occur within the 250 ms from triggering the circuits. At the termination of the 250 ms hold-off period, a time constant in the collector of Q2 gives IC9 time to fully recover before another fire pulse triggers it.

The bias-on monostable, IC7, which is also triggered by the fire signal, puts out a pulse 120 ms wide. The output from this monostable is fed through IC6-11, and IC6-6 to J8 and then by cable to bias gate input J8 on the amplifier control circuits (drawing 7513755, Appendix D) where the pulse biases on the power amplifier for 120 ms. The leading edge of the 120 ms pulse also initiates the delay monostable IC8 into operation. The output on pin 3 from IC8 goes low 24 ms after the start of the 120 ms bias-on pulse, and remains low for the duration of the 120 ms pulse. Output from pin 3 of IC8 is coupled through IC6-8 to Jack J7 and then to the "Amplifier-Ready" Jack J5 on the front panel of the damped sine generator. A high logic level (TTL), at this Jack indicates that the amplifier is ready and can amplify a signal. Output from pin 3 of IC8 is also coupled through terminal 8-10 to IC12-11, to the R&S inputs of IC15-11, through IC12-8, IC13-6, and IC14-8 to terminal 9-6. The waveform at terminal 9-6 is the same as it is at pin 3 of IC8 except for an inversion. Terminal 9-6 is connected to terminal 8-17. The signal at 8-17 is the trigger signal to the zero-crossing detector. The zero-crossing detector, therefore, generates its signals 24 ms after the fire pulse and is reset at the end of the 120 ms bias-on pulse.

An internal pulse repetition frequency generator (PRF gen.) can be used to supply the fire command instead of the manual switch. When the PRF Gen. is turned on, a logic high appears on terminal 8-16. This enables the PRF oscillator IC10. IC10 is a 555 timer wired as an oscillator whose frequency can be switch selected from 1 Hz to 100 kHz in 6 steps.

The logic high at terminal 8-16 is also supplied to gates 5-6, 5-8, and 12-3. The output of gate 12-3 will be unchanged, its output will remain high. The output of gate 5-6 will go low, disabling the operation of Q1. This will prevent a manual fire signal from firing the circuits. The low at the output of gate 5-6 also forces the output of gate 12-6 high, disabling the ability of the ready pulse to "set" flip-flop 15-11. Therefore, termination of the "ready" pulse will still reset flip-flop 15-11, but the "Q" output of 150011 will no longer rise at the same time as the "ready" pulse. The logic high at terminal 8-16 also enables gate 5-8 and allows the output of the PRF oscillator (IC10, pin 3) to be coupled into gate 5-11. Therefore, a positive transition at pin 3 of IC10 will trigger the hold-off and bias-on monostables into operation. When the "ready" pulse (J7) goes high, the "R" input to 15-11 will also go high. Since flip-flop 15-11 has its "J" input high, its "K" input low, and its clock "C" tied to the PRF oscillator output (pin 3); the flip-flop will toggle to the "Q" = High State on the next negative transition of the PRF oscillator's output. The high output on "Q" of 15-11 is processed to a low output at terminal 8-17 which triggers the zero-crossing detector. Terminal 8-17 will return to a logic high resetting the zero-crossing detector when flip-flop 15-11 is reset upon termination of the "ready" pulse. At low PRF frequencies (1 Hz and 10 Hz) the output of the PRF oscillator is not symmetric; the negative transition will occur about 26 to 30 ms after the positive transition. Therefore, at low PRF frequencies, one trigger will always occur within the "ready" time, and it is synchronized to the PRF oscillator, not the "ready" pulse. The output of the PRF oscillator is essentially symmetric at 100 Hz, 1 kHz, 10 kHz. The output from the PRF oscillator is fed through gate 5-8 and is then fed to gate 12-8. When the PRF oscillator is operating at higher frequencies where more than one cycle will occur within the "ready" time, the output cycles from the oscillator following clocking of flip-flop IC15 are fed directly (through gate 12-8) to the trigger input on the zero-crossing detector. Each cycle from the PRF generator becomes a trigger and reset to the zero-crossing detector, causing a

succession of damped sines to occur within the "ready" time. These higher PRF rates are useful to provide brighter scope traces during testing and calibration of the damped sines. The use of IC15 to synchronize the first trigger to the PRF generator and not the ready pulse prevents jitter when using these higher PRF rates.

The PRF rate must be low enough consistent with the selected damped sine frequency such that truncation of the damped sine wave does not occur. The 100 kHz rate would be good only for damped sines with frequencies at 4 MHz or above, etc.

When the power amplifier is operated in the "TEST-CW AMP A" or "TEST-CW AMP B" mode, it is not necessary to correlate the trigger to the "ready" pulse because the power amplifier is always ready. When the mode switch on the amplifier is placed in one of the above modes, a logic high appears on FL5, and hence on terminal 9-10. This high is applied to gate 12-3 where it inhibits the resetting of IC15 at the end of the ready pulse. The system will then produce a continuous succession of damped sines with any selected repetition rate.

To facilitate the synchronizing of the damped sine wave to some external event (such as placing the damped sine on the crest of a 400 Hz waveform, or on top of a particular data word), an external trigger input is provided. This is Jack J6 on the front panel of the damped sine generator and J6 is coupled to J1 on Box B. When the "modulator trigger" select switch is placed in the "Ext." position, it allows for the externally applied signal to trigger the zero-crossing detector. This externally applied input may be processed in two ways before it is applied to the zero-crossing detector:

TYPE A: The trigger to the zero-crossing detector will go low coincident with the first positive transition of the externally applied trigger signal following the positive transition of the "ready" pulse. The zero-crossing detector's trigger will remain low until the "ready" pulse terminates.

TYPE B: The externally applied trigger waveform is inverted and applied directly to the zero-crossing detector.

When the "modulator" trigger select switch is placed in the "Ext" position, it places a logic high on FL4 and hence terminal 9-11. This removes the permanent "set" on flip-flop 15-15, disables gate 13-6 by placing a logic low on its pin 4, and enables gate 14-12 by placing a logic high on its pin 13. The type of processing (A or B above) is selected by a switch on the rear panel of the damped sine generator. When type A processing is selected, a logic high appears on FL 3 and hence on terminal 9-12. This removes the "reset" from flip-flop 15-15 during the "ready" interval. Since J is high and K is low on 15-15, the first positive transition on the external trigger input which occurs during the "ready" interval will clock 15-15 and the low to high transition on its output is coupled through gate 14-8 to trigger the zero-crossing detector. The circuit is then insensitive to any more positive transitions on the external trigger input and the trigger to the zero-crossing detector will terminate at the end of the "ready" interval. When type B processing is selected, a logic low appears on terminal 9-12. This places a low on the reset of flip-flop 15-15 causing its "Q" output to be low, independent of the "ready" pulse. The low on terminal 9-12 also places a high on pin 1 of gate 14-12 allwoing the externally applied trigger appearing on terminal 9-13 to pass directly through gates 13-8, 14-12, and 14-8 to the zero-crossing detector.

A trigger signal of any kind feeding the zero-crossing detector must pass through terminal 8-9 to terminal 8-17. The signal is also passed through a 1K resistor to IC11. IC11 is a 555 timer wired as a monostable with an output pulse width of about 1.5 seconds. It is triggered by the negative going trigger feeding the zero-crossing detector. IC15's output feeds Q4 whose collector drives a lamp located behind the manual fire switch. This lamp indicates that a trigger signal has been received by the zero-crossing detector.

APPENDIX A

INSTRUCTION MANUAL

MODELS M5000/M5000L

WIDEBAND POWER AMPLIFIER

1.0 GENERAL INFORMATION

1.1 Scope of this Manual. This manual pertains to the Instruments for Industry M5000 series of medium power broadband amplifiers. It includes detailed equipment description, principles of operation, operating instructions, adjustment procedures and appropriate schematics for maintenance and servicing.

1.2 Purpose and Features of Equipment. The M5000 Series of amplifiers is intended for applications requiring approximately 30 dB of power gain over a wide range of frequencies with power output capability of 5 to 10 watts continuous or 20 watts on an intermittent basis.

The series consists of two general versions: (1) the M5000 with frequency response from 200 kHz to 220 MHz, and (2) the "L" version with extended frequency response from 10 kHz to 220 MHz. These two versions differ primarily in basic components and in factory alignment procedure.

Broadband power amplifiers derive their usefulness by providing linear amplification of low-level signals over an extremely wide range of frequencies with little or no frequency discrimination. Any low-level signal within the specified passband will be amplified, complete with modulation (frequency or amplitude) and passed on to the load at a power level determined by the gain of the amplifier and the input level.

Gain of the M5000 Series, 30 dB minimum ±2 dB over the frequency range was selected to permit use of standard laboratory signal generators to serve as signal sources.

The M5000 Series is quite tolerant of load mismatch, being capable of operating into a 4:1 mismatch without damage. However, it is possible to damage the unit by prolonged use with loads that produce higher vswr. This subject is treated in detail in the OPERATION section of this manual.

1.3 Equipment Specifications. The specifications of the M5000 amplifiers are as follows:

	M5000 Version	"L" Version
Max. Frequency	220 MHz	220 MHz
Min. Frequency	200 kHz	10 kHz
Bandpass Ripple	±1.5 dB max.	±1 dB typical
Power Gain	30 dB	
Gain Control		
Input Attenuator	41 dB in 1 dB steps	
First Stage Gain Control	10 dB continuous	
Input		
Impedance	50 ohms (nominal unbalanced)	
Power	5 watts continuous, linear*	
	10 watts continuous	
	20 watts intermittent	
Duty Factor	Continuous up to 10 watts at 2.5 watt output, all harmonics down min. 20 dB	
Rise Time	Less than 7 nanoseconds	
VSWR Tolerance	Unit will not be damaged at rated drive with load vswr up to 4:1	
Power Requirements	115 V a.c., single phase, 50/60 Hz	
Cooling	Self contained blowers	
Size	5-1/4" H, 19" W, 20" D	
Cabinet Options		
BF	Bench cabinet, output conn. on front	
BR	Bench cabinet, output conn. rear	
RF	Rack mount, output conn. on front	
RR	Rack mount, output conn. at rear	
Connectors	BNC (others on special order)	
Weight	33 pounds	

*Distortion

NOTE: The above specifications pertain to minimum performance with at least 115 V a.c. line voltage. Variations may be expected for other line voltages.

2.0 PRINCIPLES OF OPERATION

2.1 Distributed Amplifier Theory. The M5000 system is comprised of a series of distributed amplifier (DA) modules or sub-units, and a common d.c. power supply. Three of the sub-units are identical and form two of the "stages" (two in parallel constitute the output state and the third, its driver stage). The fourth module contains the first two stages of the system.

In all stages, type 6AN5 vacuum tubes are arranged so their input capacitances form the shunt capacitance of an artificial, lumped-constant transmission line.

A signal propagating along the input line will feed each successive grid with a signal which is increasingly delayed in time. Similarly, the signals appearing at the plate as a result of the grid excitation will be similary delayed.

It should be noted that for a signal propagating in the forward direction in the plate line, there will be signal addition if the phase shift in the plate line is the same as the phase shift in the grid line per section. The signal appearing at the output terminal is the sum of the forward propagating signals generated by each of the tubes along the line.

It should also be noted that part of each tube's output signal will travel the "wrong way" on the plate line. Therefore, each line is terminated at the reverse end by a resistive load equal to the characteristic impedance of line (which is fundamentally determined by the tube and circuit capacitance of the bandpass desired). In this way there is no reflection from the far end of the transmission line. The reverse propagating signal in the plate line does not build up in amplitude but arrives in random phase dependent on the frequency and is absorbed in the reverse termination.

In essence, then, the distributed amplifier, by distributing the tubes along these two transmission lines, operates the tubes in parallel so far as their ability to generate current into a load is concerned, but splits up the capacitances so that they do not similarly add and thereby hold the gain bandwidth factor constant. It is thus possible to build an amplifier having a gain-bandwidth in excess of the gain bandwidth product of the individual tubes used.

2.2 Input/Output Impedance. Input and output impedances are shown under EQUIPMENT SPECIFICATIONS to be 50 ohms "nominal" unbalanced. This value was chosen for convenience in matching standard test equipment and typical loads.

The M5000 is tested and aligned with 50 ohm source and load and will meet all specifications under such conditions. However, slightly different impedances may actually exist at input and output. In fact, these impedances vary with frequency and cannot be specified with any degree of accuracy over the unit's entire frequency range.

For applications where internal impedances of the unit must be known or estimated for their effect on external circuitry, it may be said that the nominal intrinsic values are approximately 91 and 75 ohms for input and output, respectively.

2.3 Distortion. A conventional tuned or bandpass amplifier can be designed to discriminate against harmonics of the signal to be amplified and therefore exhibit better distortion characteristics than a broadband distributed amplifier like the M5000. The DA derives its usefulness from its ability to amplify all frequencies, including harmonics.

In a DA, linearity is determined solely by the linearity of the tubes used. Tube characteristics usually exhibit good linearity over a limited portion of their operating range but progressively poorer linearity (greater distortion) as limiting begins to occur. The M5000 exhibits good linearity characteristics (essentially Class A operation) up to 2.5 watts; as the power level is increased (greater input for a given load) the combined effects of grid current flow and current limitations cause harmonic distortion to occur.

At normal 115 volt line voltage conditions, all harmonics should be at least 20 dB below carrier for harmonic-free input. At lower and higher levels, harmonic output will be proportional.

The following curves show how distortion and overall gain may be expected to vary with line voltage.

3.0 OPERATING INSTRUCTIONS

3.1 Installation Notes. A visual check of the M5000 interior should be made prior to placing the unit in service. Access may be gained by removing

the top cover plate and inspecting for loose tubes or other components. Any internal or external damage should be reported immediately.

Rack mounted cabinets require support from the rear or sides of the rack enclosure. Simple angle brackets will serve this purpose. No attempt should be made to support the unit by the rack panel alone.

3.2 Cooling. The top cover must be in place for proper operation of the M5000 cooling system. Care should be taken to see that the rear and sides of the amplifier are clear of all objects that might restrict flow of cooling air which flows in the rear and out both sides.

3.3 Heat Dissipation. The M5000 is designed for continuous operation into a nominal load of 50 ohms with sufficient drive to produce 10 watts on a continuous basis. It is capable of being driven to higher output power levels, but prolonged operation under these conditions may cause overheating and permanent damage to the equipment.

In addition, prolonged operation into a severely mismatched load may cause excessive reflection and dissipation in the reverse termination resistors (see Distributed Amplifier Theory).

3.4 Safety Precautions. With top cover plate removed, and line power applied, potentially dangerous potentials are exposed. Only qualified technical personnel should be allowed access to the equipment under these conditions.

3.5 Connection to Power Source. The M5000 is designed to operate with 115 volt, 50/60 cps, single phase power. System performance will be degraded if significantly different voltage is used.

3.6 Front Panel Controls and Indicator. The M5000 requires no adjustments. The front panel attenuator (which adjusts the signal applied to the first stage) and gain control (which adjusts the gain of the first two stages by varying the control grid voltage) are provided as an operating convenience to permit setting output power level for a given input signal level.

The attenuator is ideal for coarse (1-dB steps) calibrated gain adjustments and the gain control is best suited for precision or vernier gain adjustments. Together, they afford a gain control range of over 50 dB.

Other front panel controls and indicators are obvious as to their purpose and function.

3.7 Placing Equipment in Service. With a nominal 50 ohm resistive load and an input signal appropriate to produce a power output within the limitations specified above, the unit may be placed in operation without complication. To interrupt output, simply interrupt the input signal or increase the input attenuator setting to produce commensurate output level reduction. The amplifier may be run indefinitely at rated output (with appropriate input).

Output is usually measured by inserting a tee at the load and monitoring the load voltage to compute output power. Or, through-line wattmeter may be used with an appropriate load attached.

In setting up a system using the M5000 as a power source, care should be taken to avoid the condition of no output load with a signal applied to the input. Injecting 20 or 30 dB of attenuation (using the two most significant elements of the input attenuator) will prevent damage to the M5000 with normal input signal applied--thus preventing necessity for removing input or turning off M5000 power. This technique will become automatic after operators become acquainted with the unit.

4.0 SERVICING

4.1 Tube Replacement. There are no adjustments required and an occasional replacement of a tube is all that is expected in normal service. Complete failure of a tube makes only a small difference in the performance of the amplifier. Therefore, if a deterioration in gain or power output is suspected, check the tubes. It is suggested that Raytheon type 6AN5 tubes be used for replacement. Differences in grid lead inductances have been observed between tubes of different manufacture.

4.2 Fuse Replacement. If the main fuze blows and a replacement blows, try to isolate the faulty stage by disconnecting the power plug at the chassis of each stage in turn, one at a time. Having found the faulty stage, the circuit problem can usually be quickly found by standard trouble shooting procedures. If a tube in a stage develops a grid to cathode short, the bias for the entire stage is shorted out, thus causing all tubes to draw excessive plate and screen currents, quickly blowing the primary fuse. Usually the fuse blows before the other tubes are damaged.

4.3 Checking Gain and Alignment. The bandpass and gain may be checked by standard sweep and attenuator techniques. The gain may also be checked by adjusting the input attenuator (the variable gain control is set for maximum gain) until the overall gain from input to output terminals is unity. The step attenuator then indicates the approximate amplifier gain.

CAUTION: WHEN COVERS ON PANELS OF THIS UNIT ARE REMOVED, TERMINALS WITH POTENTIALLY LETHAL VOLTAGES ARE EXPOSED. OPERATION OF THE UNIT WITH COVER REMOVED OR SERVICING THE UNIT, SHOULD ONLY BE ATTEMPTED BY A QUALIFIED PERSON, THOROUGHLY TRAINED IN HANDLING POTENTIALLY DANGEROUS ELECTRICAL CIRCUITS.

The input stage is the IFI Model 510 Wideband Amplifier. The second stage is a single IFI Model 500 Amplifier and the third and final stage uses two IFI Model 500 amplifiers in parallel.

4.4 Tube Compliment. The M5000 uses a total of 40 type 6AN5 tetrodes. All other components are solid state.

APPENDIX B

IFI MODEL 402 POWER AMP SPECIFICATIONS

(PUP DRIVER AMPLIFIERS)

FREQUENCY RANGE	10 kHz to 220 MHz
GAIN	90 dB
POWER OUTPUT	50W (into 50Ω)
INPUT IMPEDANCE	50Ω
OUTPUT IMPEDANCE	90Ω
RISE TIME	<5 ns
DISTORTION	HARMONICS ARE DOWN MORE THAN 20 dB BELOW 25W OUTPUT
POWER REQUIRED	+450V at 2.5A +350V at ± 200 mA MAX 6.0V a.c. at 16 AMP BIAS -10 to -30 VOLTS AS REQUIRED
COOLING	FORCED AIR

APPENDIX C

IFI MODEL 406 POWER AMP SPECIFICATIONS

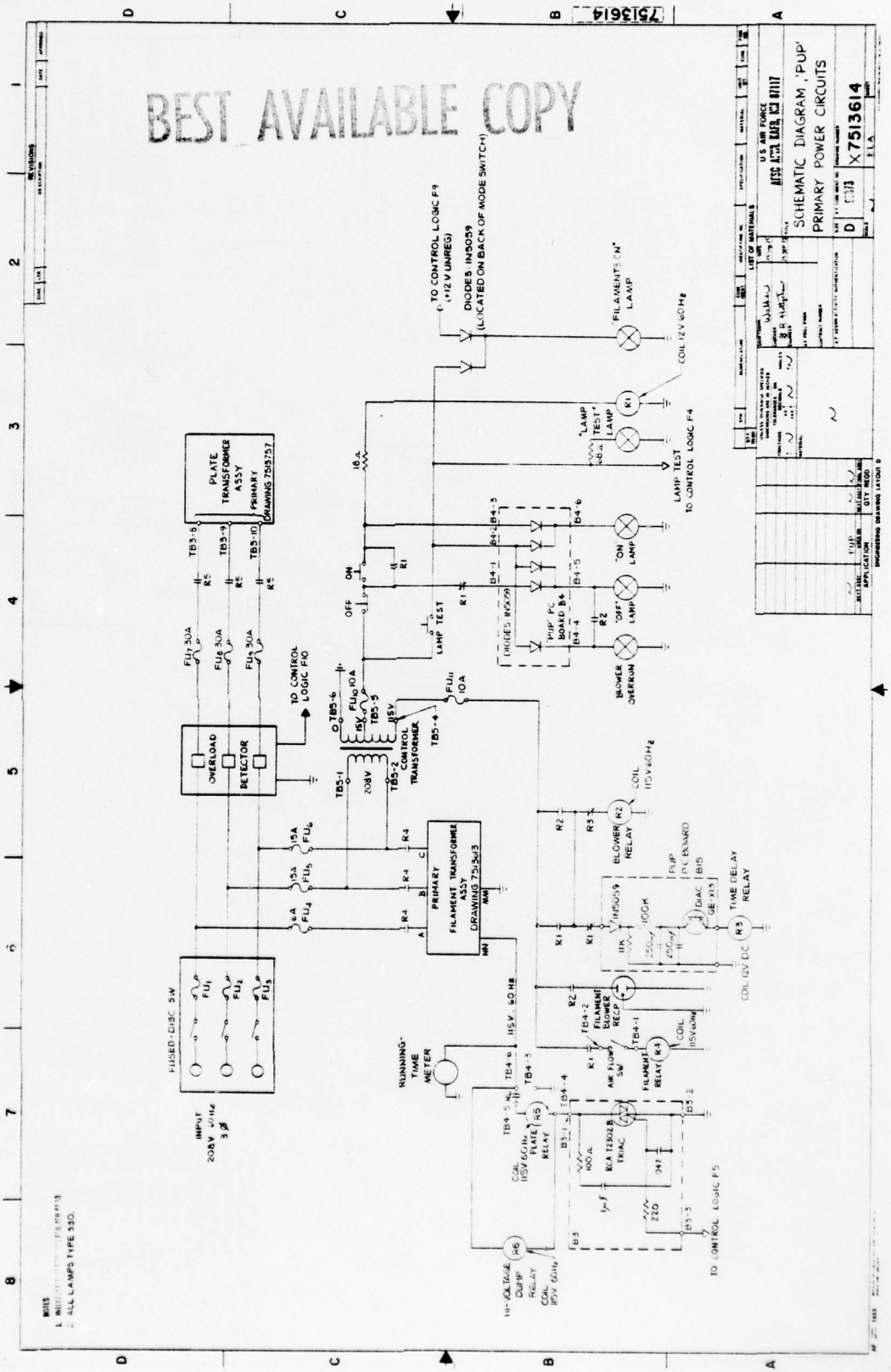
(PUP OUTPUT AMPLIFIERS)

FREQUENCY RANGE	10 kHz to 220 MHz
POWER OUTPUT	1000 W (into 50Ω)
GAIN	21 dB
INPUT IMPEDANCE	50Ω
OUTPUT IMPEDANCE	100Ω
POWER REQUIRED	+800V at 7.2A +350V at ± 450 mA MAX BIAS, -10 to -40 VOLTS AS REQUIRED
COOLING	FORCED AIR

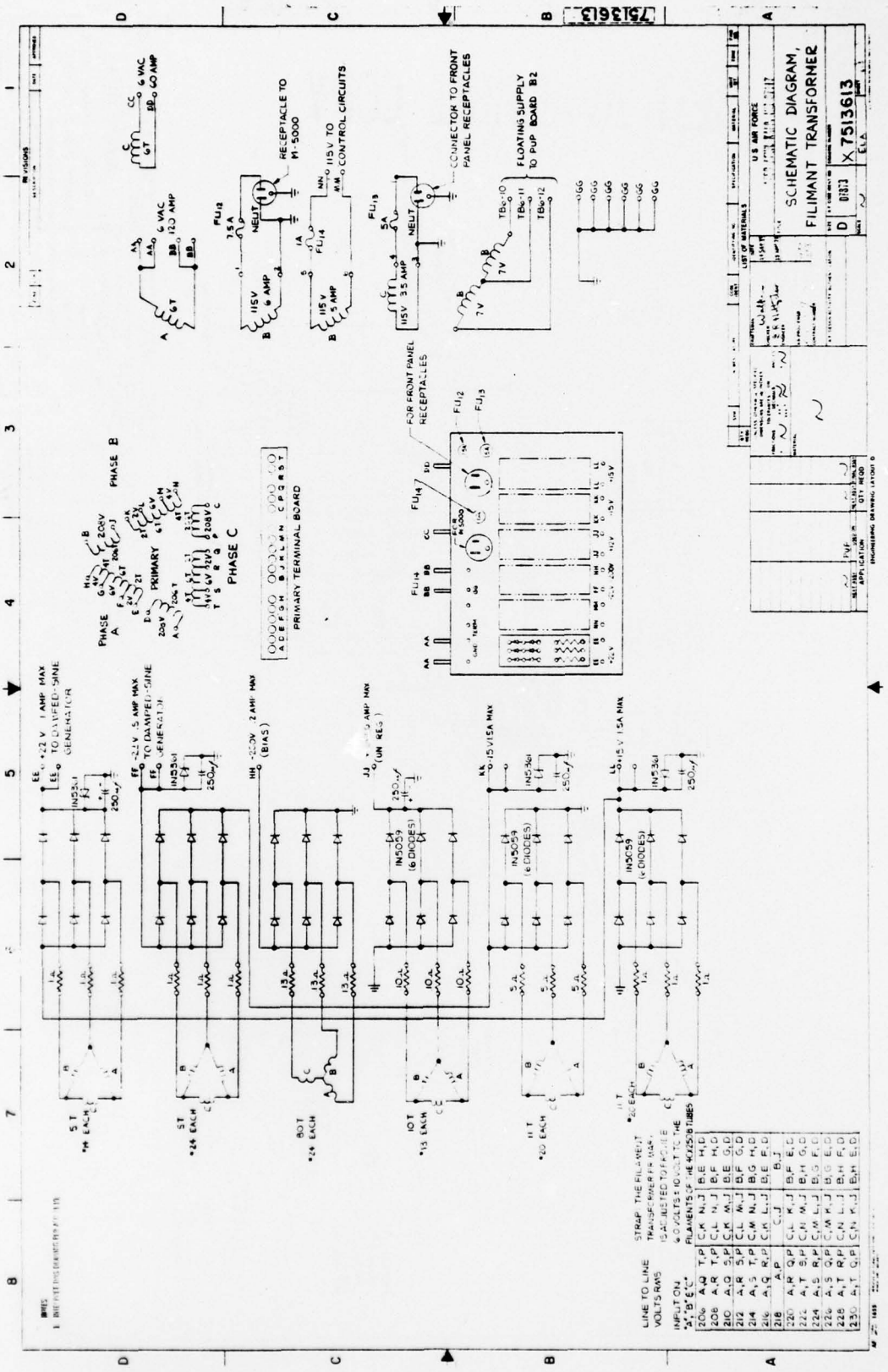
APPENDIX D

PUP DRAWINGS

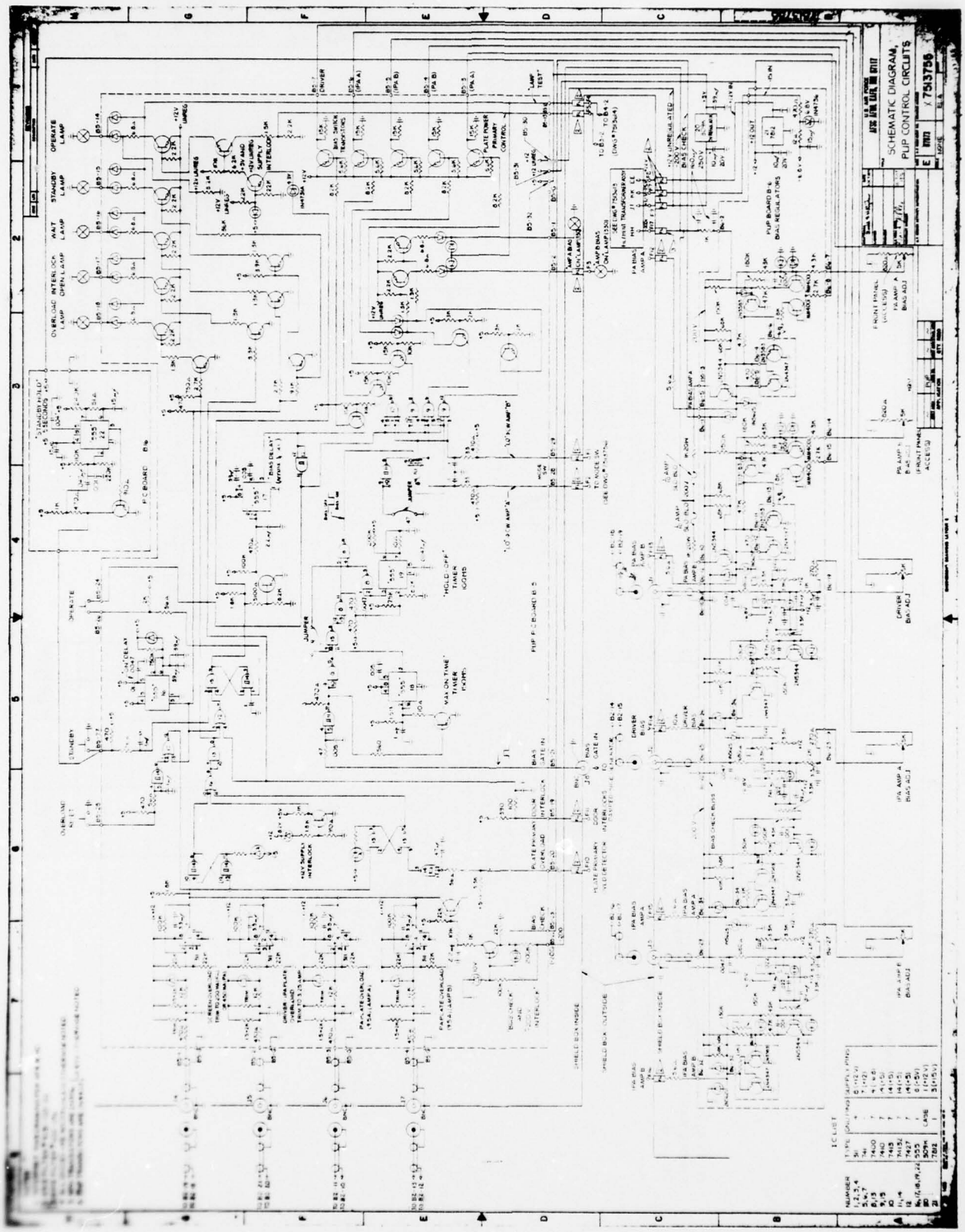
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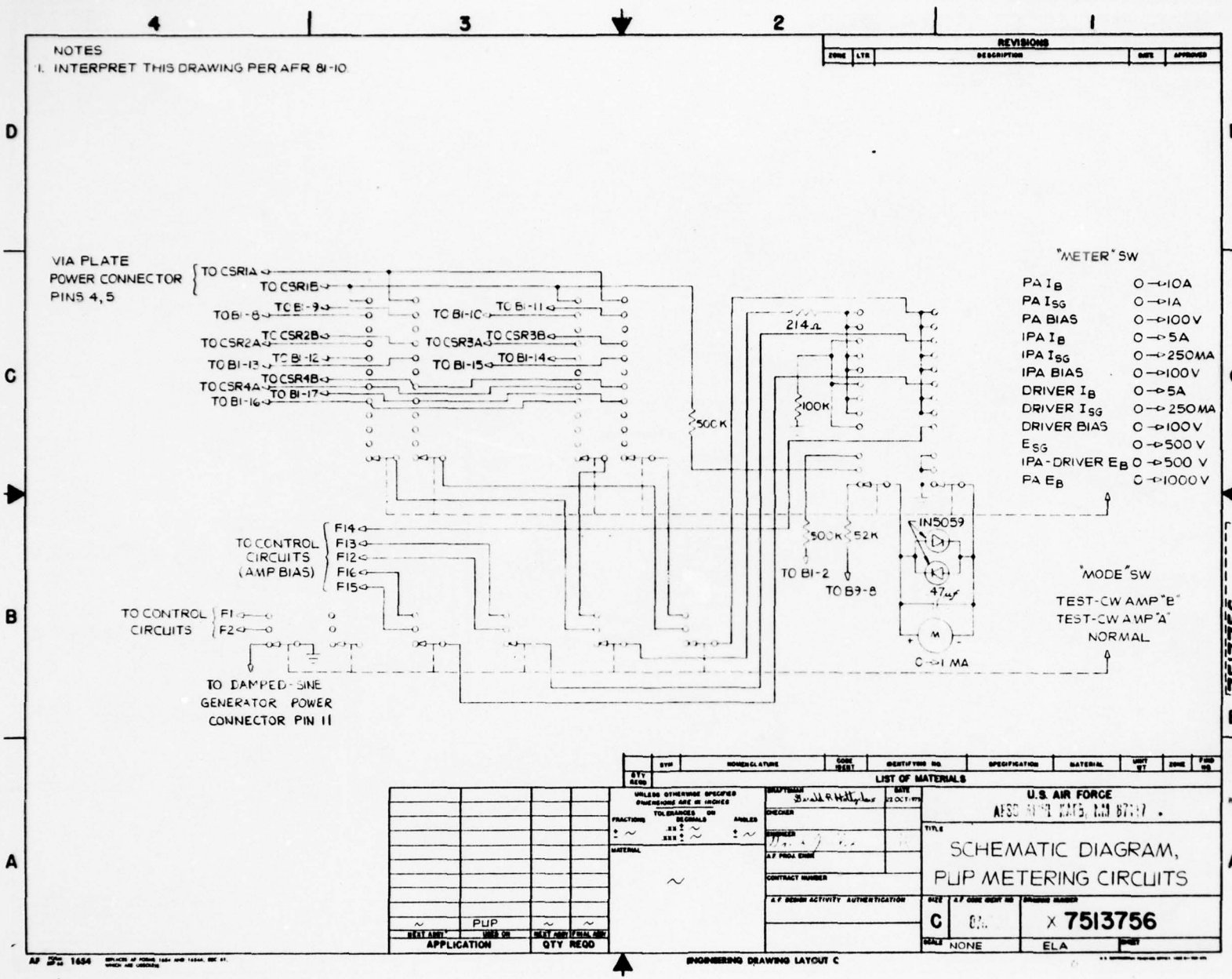


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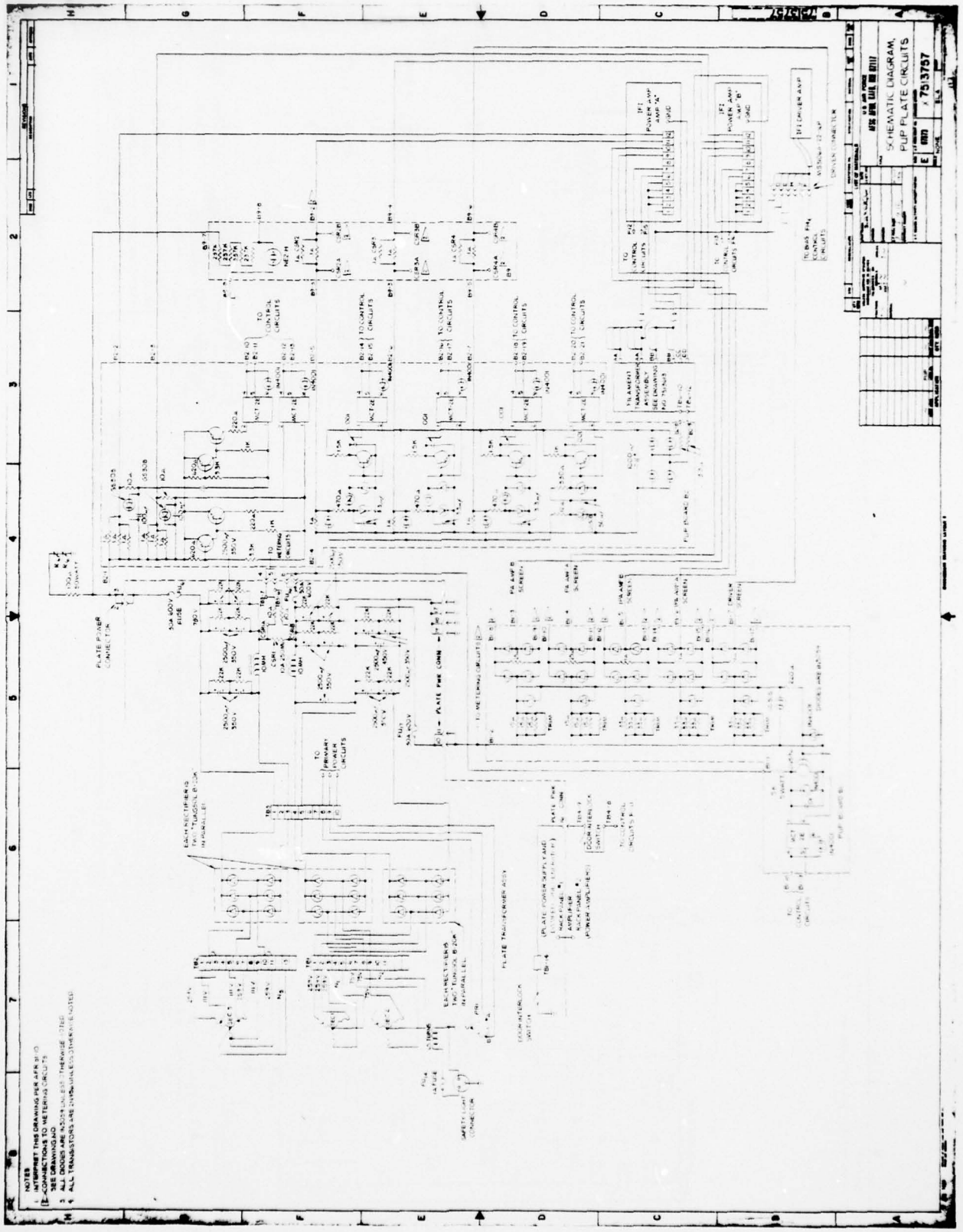
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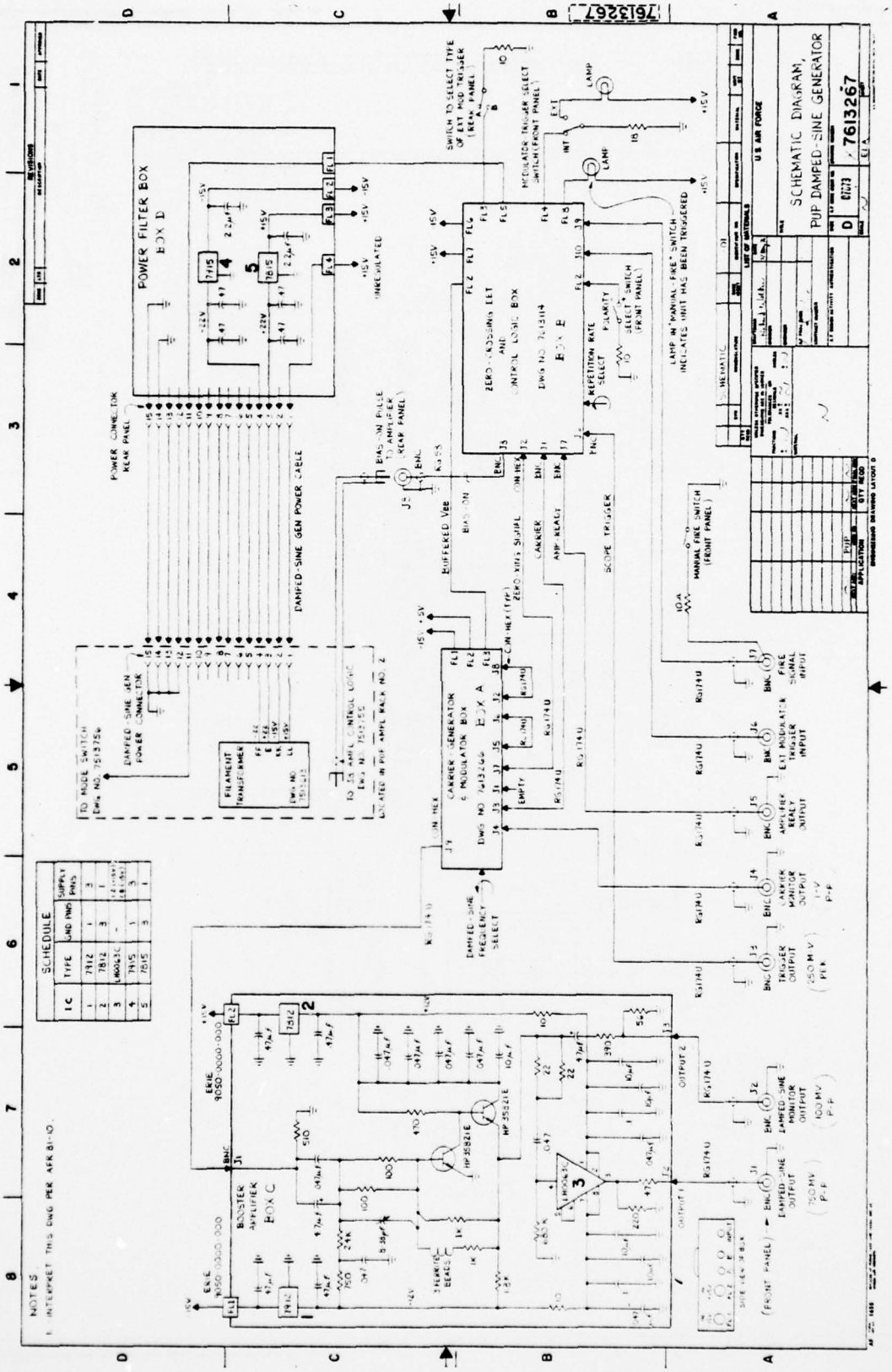


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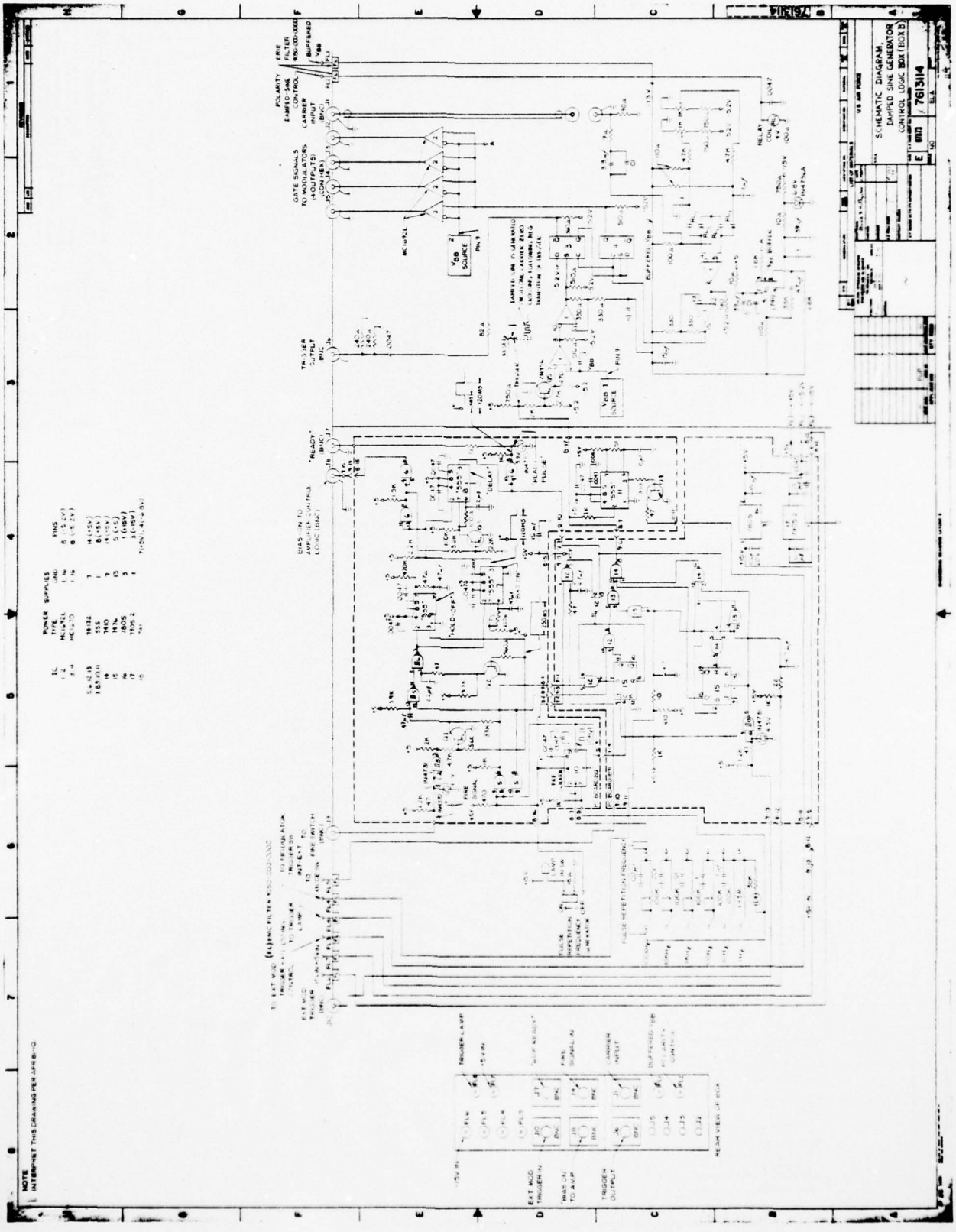
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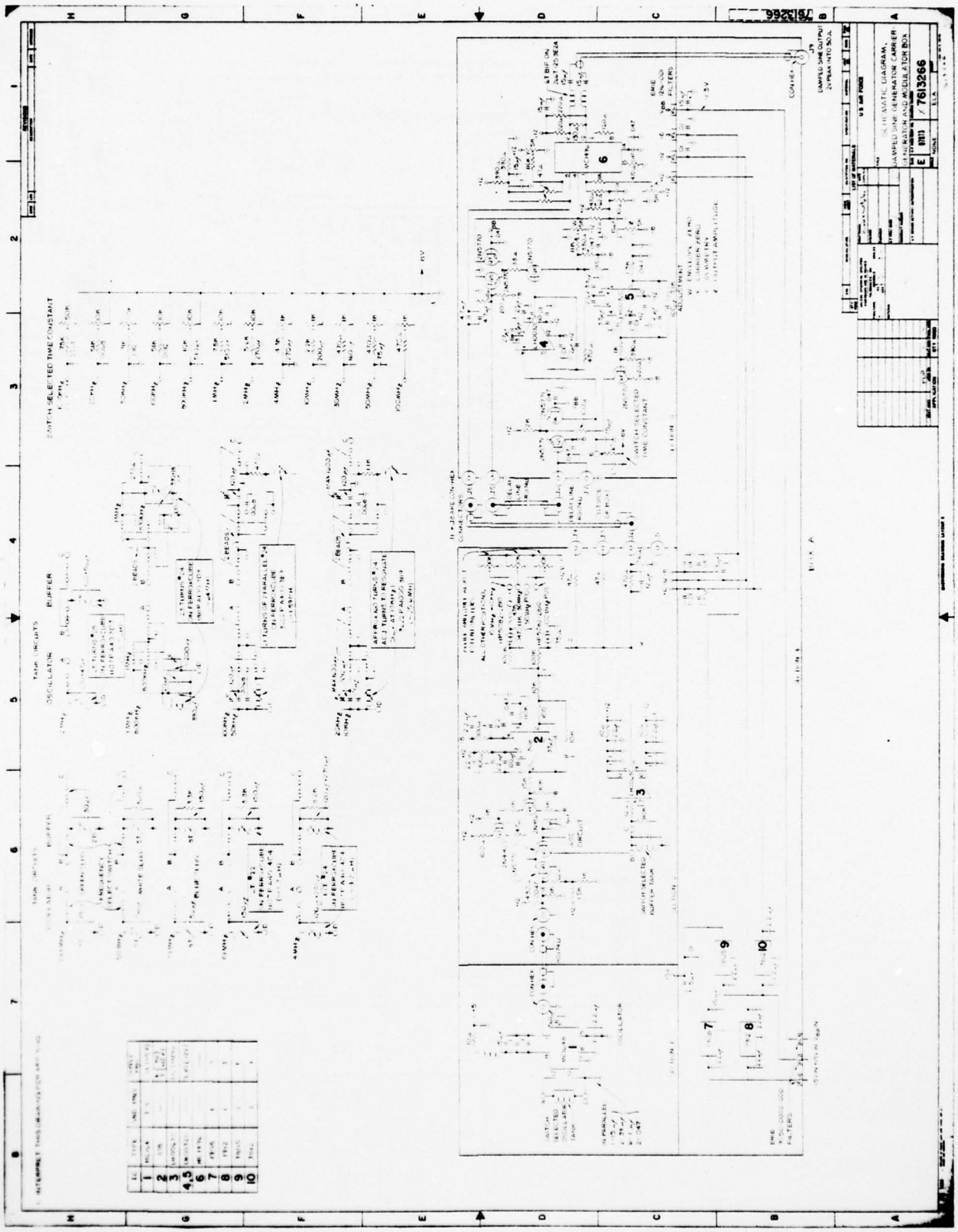
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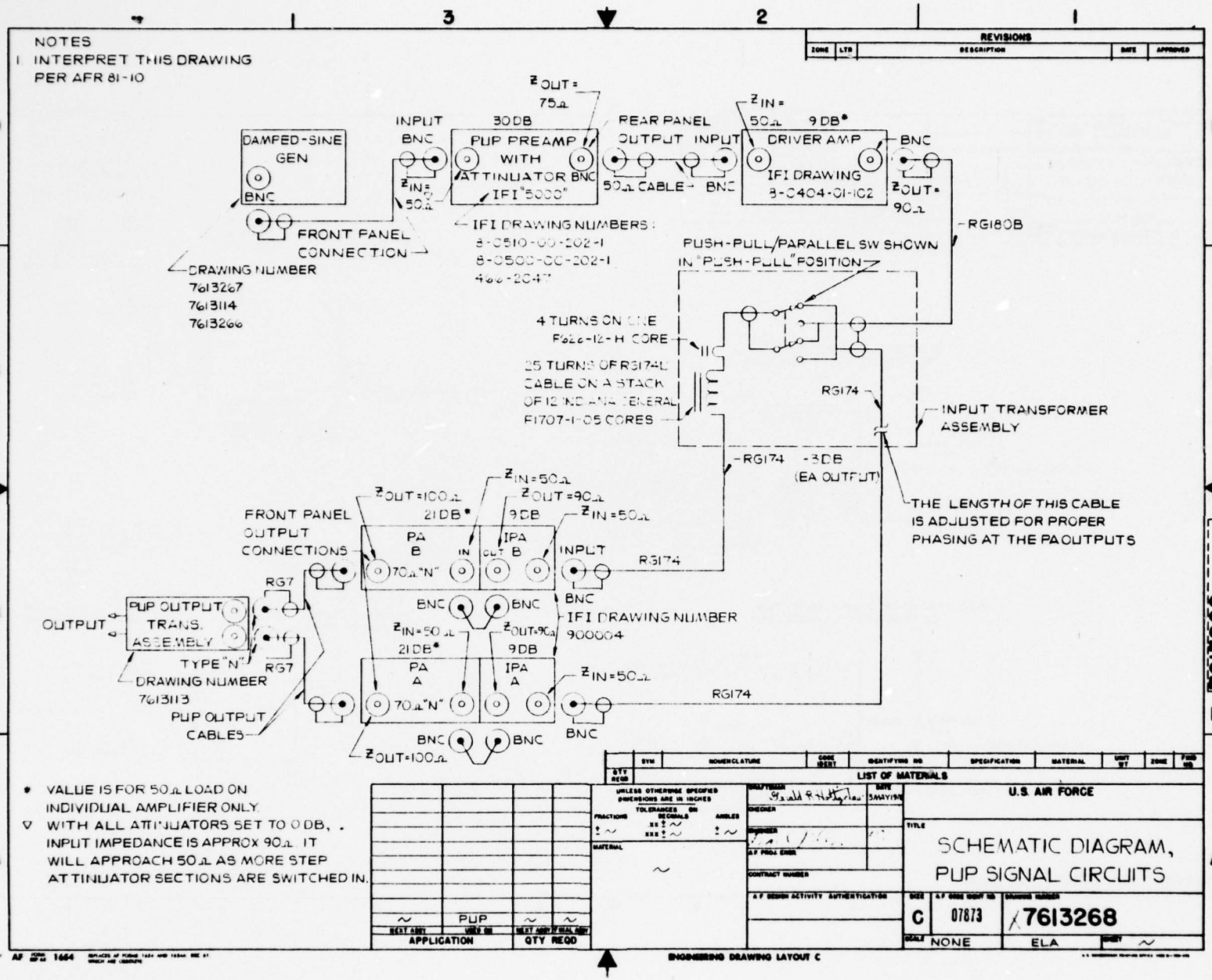
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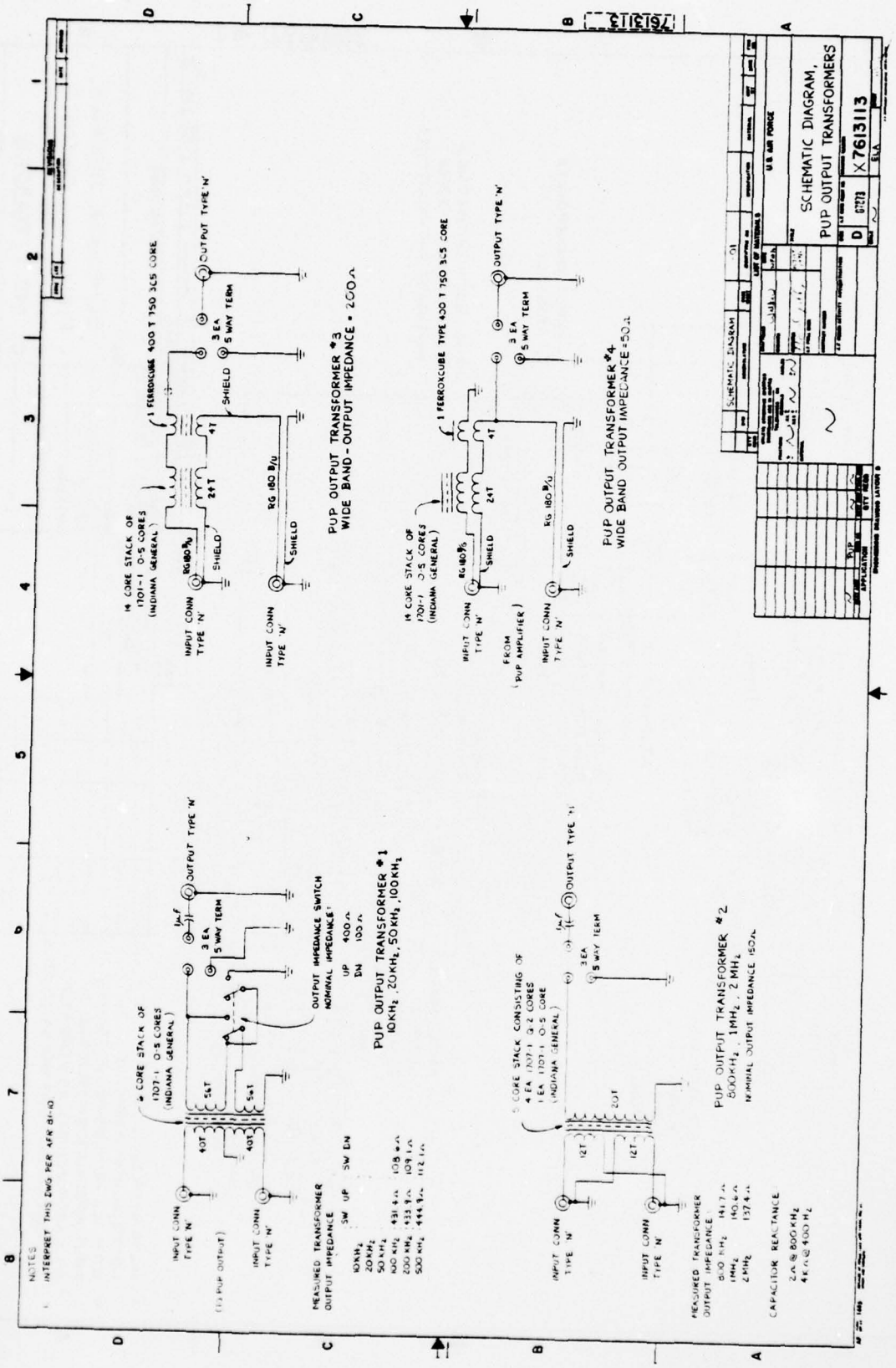
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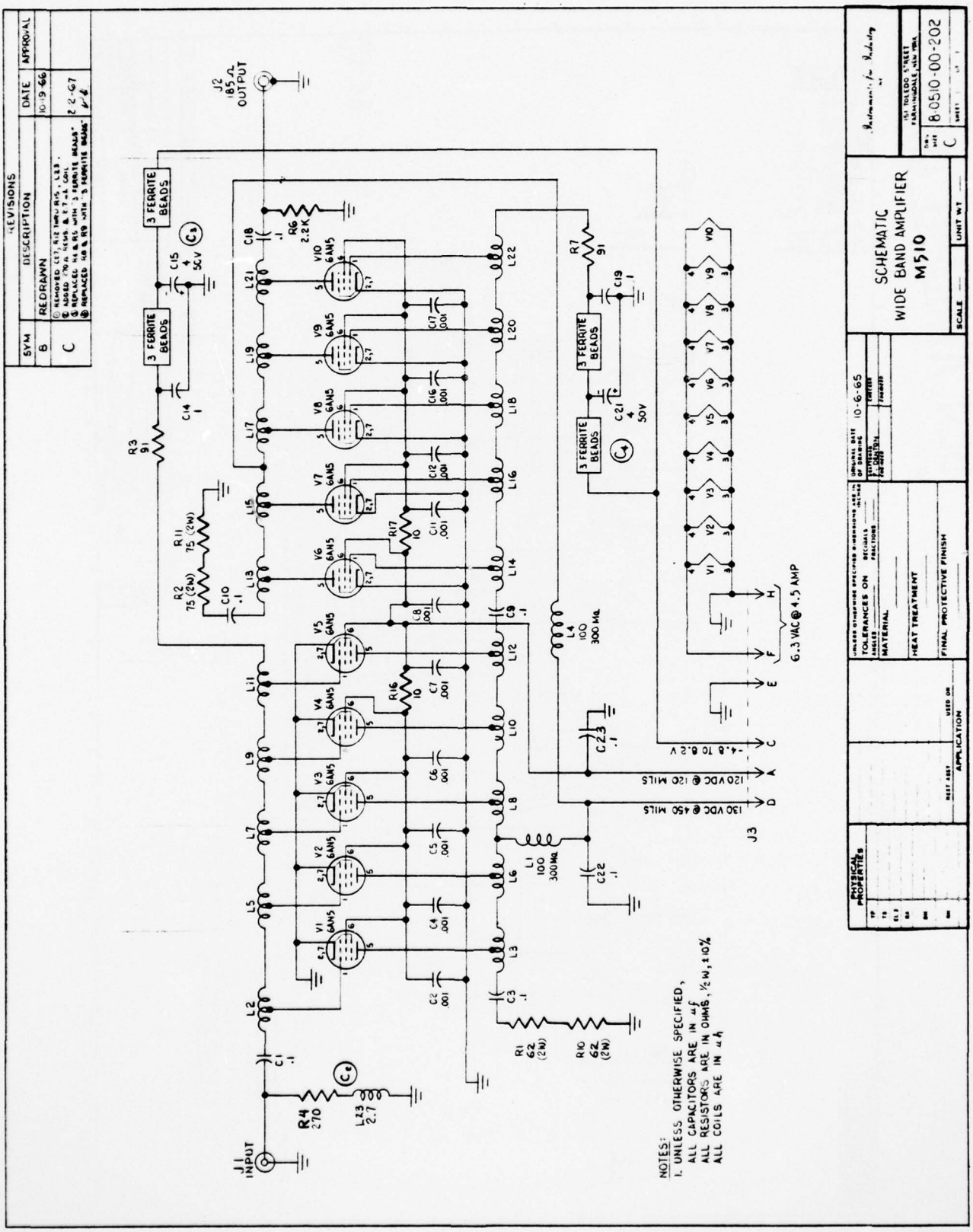


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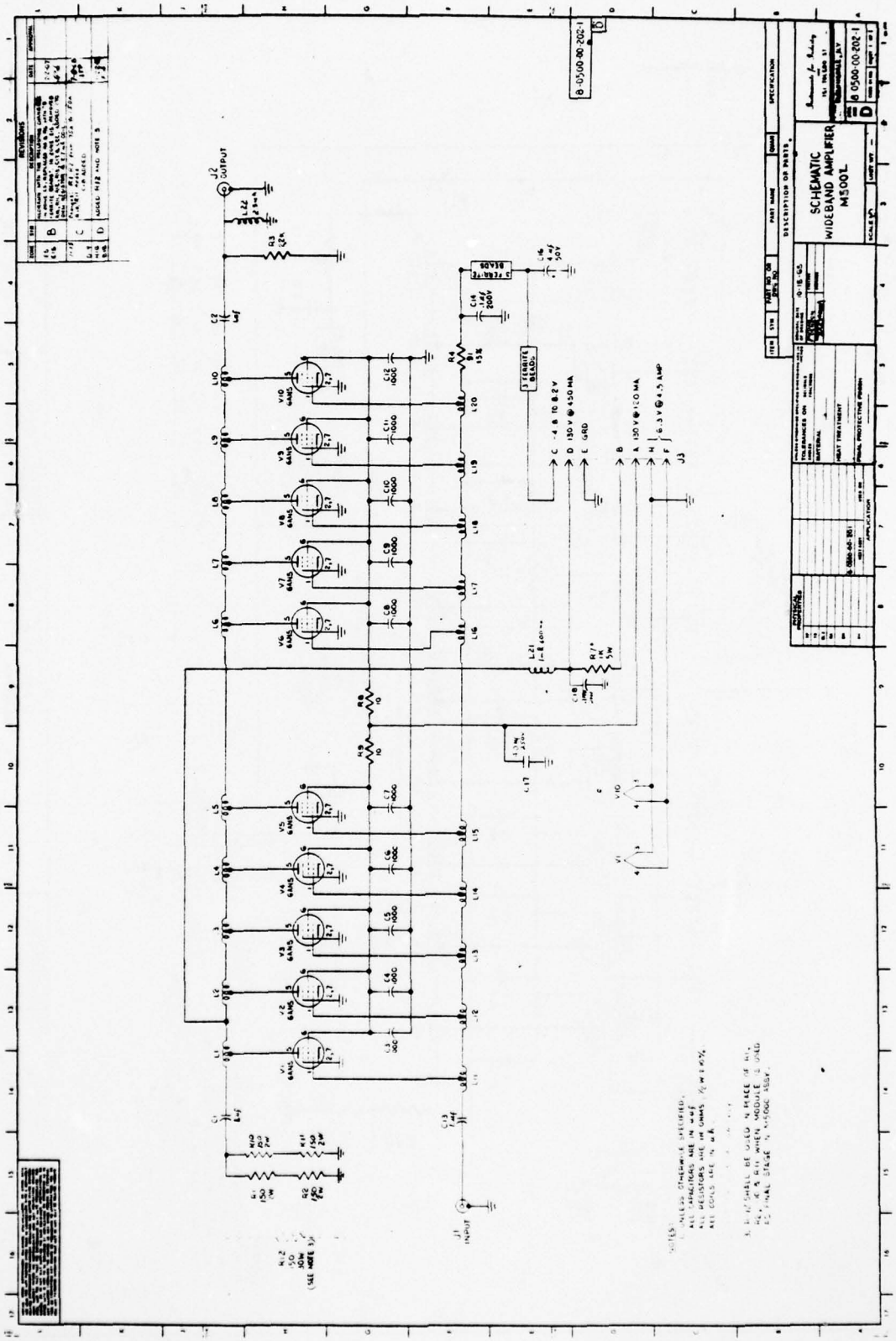


AD-A032 976

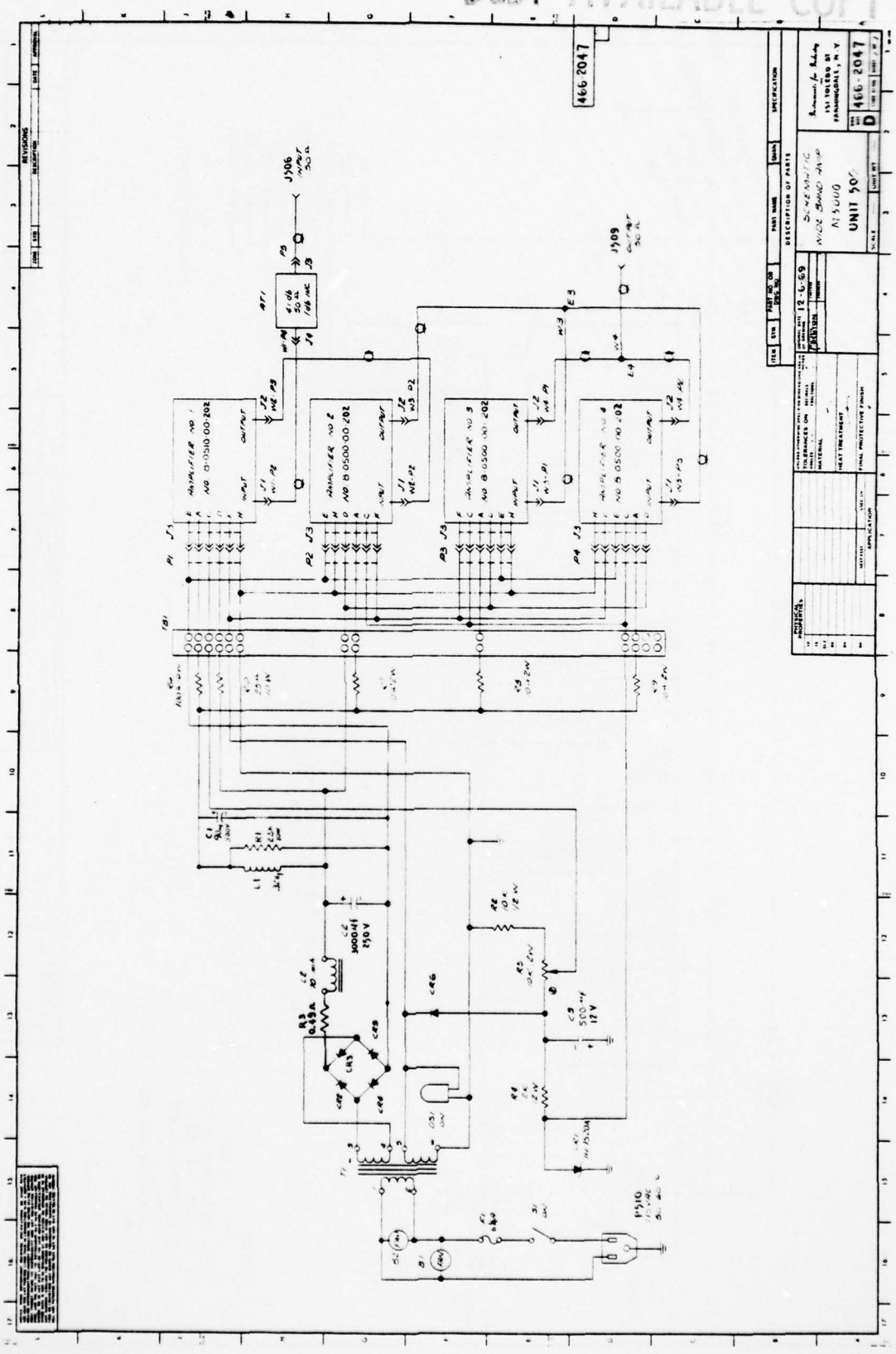

NOTES
1. INTERPRET THIS DWG PER AFR 81-10
PUP OUTPUT TRANSFORMER #3
WIDE BAND - OUTPUT IMPEDANCE = 200Ω
PUP OUTPUT TRANSFORMER #4
WIDE BAND OUTPUT IMPEDANCE=50Ω
PUP OUTPUT TRANSFORMER #1
10KH₂, 20KH₂, 50KH₂, 100KH₂
PUP OUTPUT TRANSFORMER #2
500KH₂, 1MH₂, 2 MH₂
NOMINAL OUTPUT IMPEDANCE 150Ω
SCHEMATIC DIAGRAM,
PUP OUTPUT TRANSFORMERS
D
X7613113

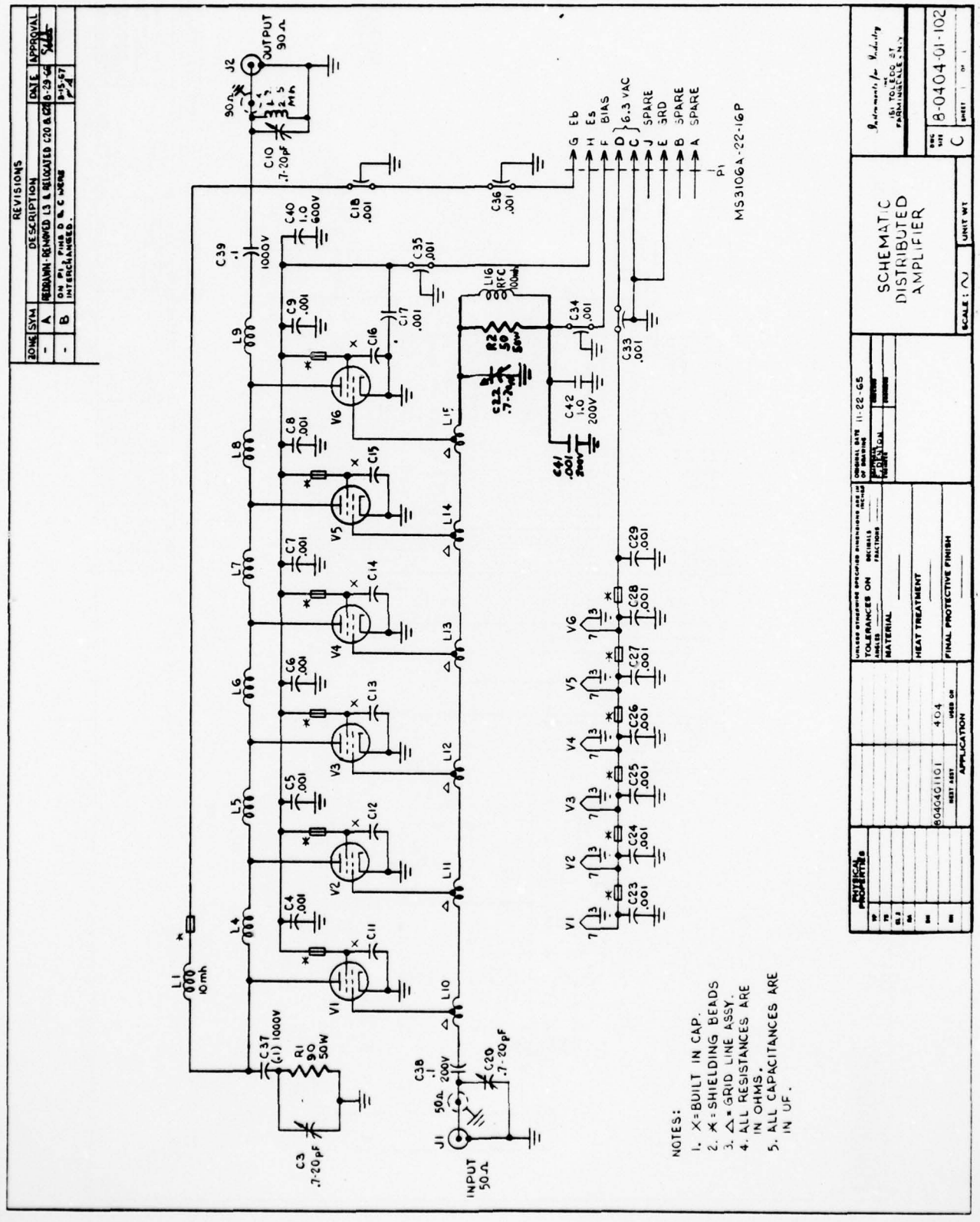

REVISIONS
SYM
DESCRIPTION
DATE
APPROVAL
B
REDRAWN
10-19-66
C
2-2-67
SCHEMATIC
WIDE BAND AMPLIFIER
M510
8 0510-00-202
J1 INPUT
J2 185Ω OUTPUT
J3
3 FERRITE BEADS
6AN5
6.3 VAC @ 4.5 AMP
120 VDC @ 120 MILS
130 VDC @ 450 MILS
-4.8 TO -8.2 V
NOTES:
1. UNLESS OTHERWISE SPECIFIED,
ALL CAPACITORS ARE IN μf
ALL RESISTORS ARE IN OHMS, ½ W, ±10%
ALL COILS ARE IN μh

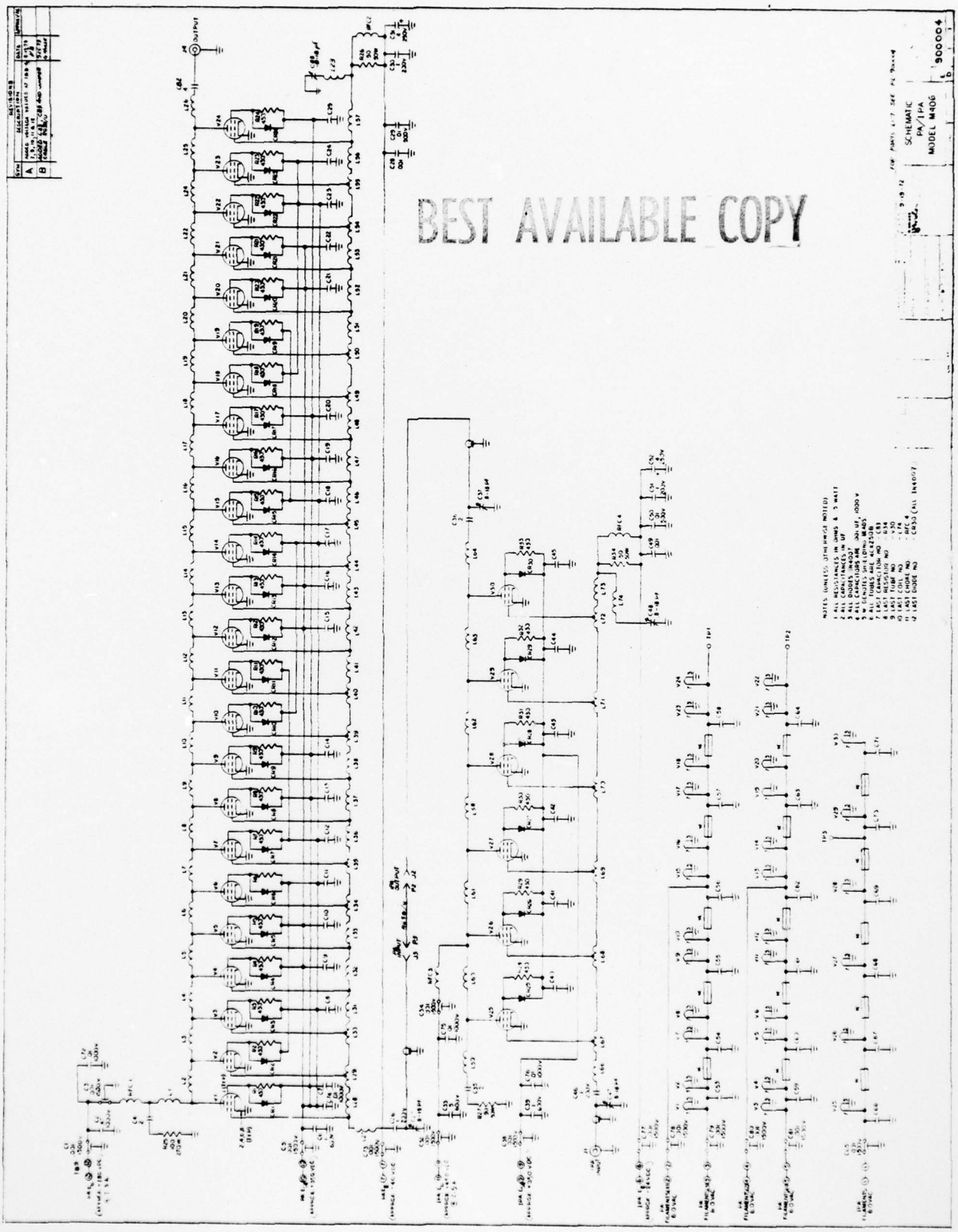
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REVISIONS
ZONE SYM DESCRIPTION DATE APPROVAL
- A REDRAWN: REMOVED L3 & RELOCATED C20 & C21 8-23-66
- B ON P1, PINS D & C WERE INTERCHANGED. 8-15-67
SCHEMATIC
DISTRIBUTED
AMPLIFIER
8-0404-01-102
SCALE: NONE
UNIT WT
SHEET 1 OF 1
MS3106A-22-16P
P1
J1 INPUT 50Ω
J2 OUTPUT 50Ω
C3 .7-20pF
C10 .7-20pF
C20 .7-20pF
C22 .7-20pF
R1 90 50W
R2 50 50W
L1 10mh
C37 (.1) 1000V
C38 .1 200V
C39 .1 1000V
C40 1.0 600V
C41 .001 2000V
C42 1.0 200V
C18 .001
C36 .001
C35 .001
C17 .001
C33 .001
C34 .001
L16 RFC 100mh
G Eb
H Es
F BIAS
D 6.3 VAC
C SPARE
J 3RD
E SPARE
B SPARE
A SPARE
V1 V2 V3 V4 V5 V6
L1 L2 L3 L4 L5 L6 L7 L8 L9 L10 L11 L12 L13 L14 L15
C4 C5 C6 C7 C8 C9 C11 C12 C13 C14 C15 C16 C23 C24 C25 C26 C27 C28 C29
NOTES:
1. X=BUILT IN CAP.
2. *=SHIELDING BEADS
3. △=GRID LINE ASSY.
4. ALL RESISTANCES ARE IN OHMS.
5. ALL CAPACITANCES ARE IN UF.



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