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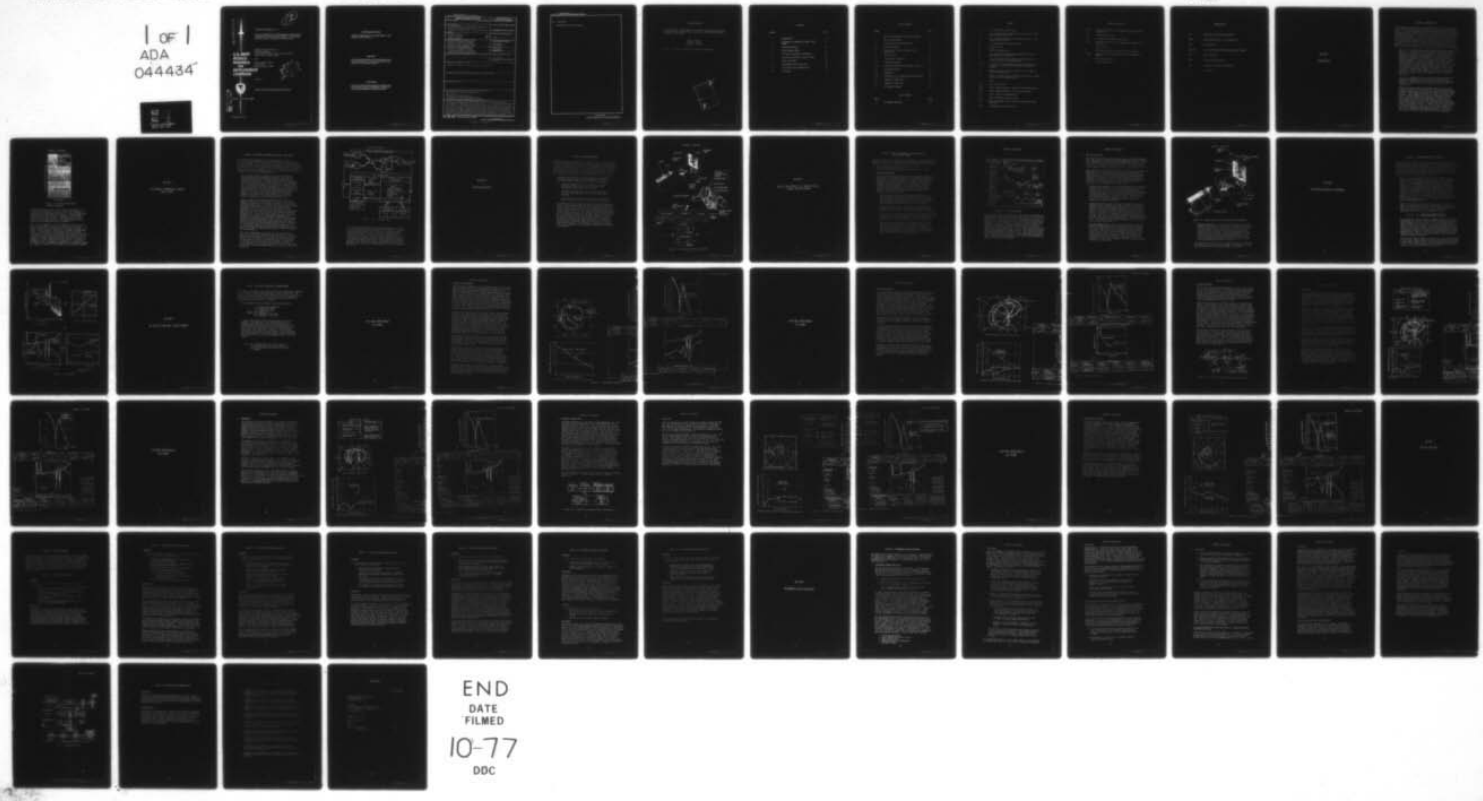

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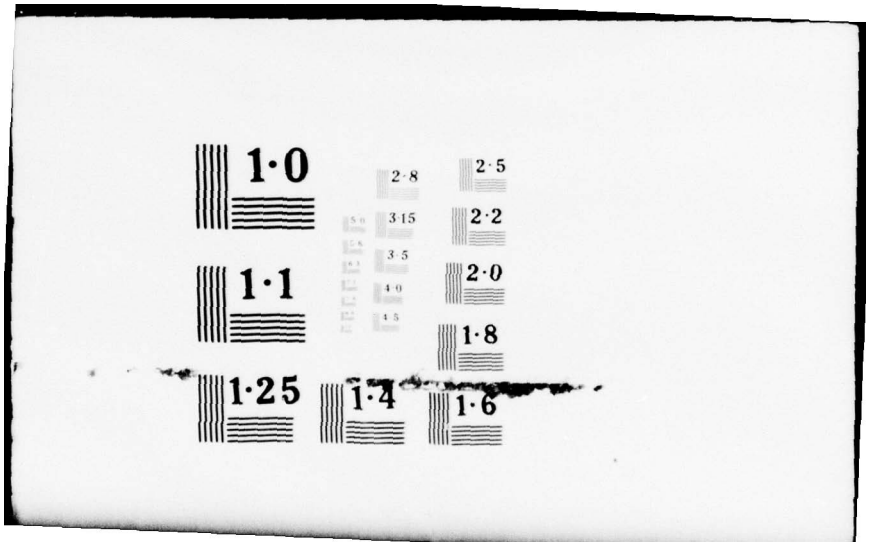
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U.S. ARMY MISSILE RESEARCH AND DEVELOPMENT COMMAND

Redstone Arsenal, Alabama 35809

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TECHNICAL REPORT TG-77-21

THE DEVELOPMENT OF A DISTURBANCE ACCOMMODATING CONTROLLER TO REDUCE "SPOT JITTER" IN A PRECISION POINTING SYSTEM - A PRACTICAL DESIGN GUIDE

Guidance and Control Directorate
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and

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1 July 1977

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Results of applying Disturbance Accommodating Control (DAC) theory to a precision pointing system are presented. Reductions in stabilized mirror "spot jitter" of up to 10:1 were achieved in side-by-side testing with the same system utilizing conventional servo design. From the lessons learned during hardware development and test, practical design guidelines are developed for achieving even better performance in future application of DAC design techniques. It is concluded that the technology has now been developed and demonstrated to where it is a viable candidate for design of operational precision pointing/tracking (Cont)

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stabilization control systems.

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James A. Daniel
William H. Lawler
Stephen J. Massaro

and Dr. C. D. Johnson, University of Alabama in Huntsville.

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SYMBOLS

A	n x n plant state dynamic matrix
b	n x 1 column matrix relating the control u(t) to the plant state velocity vector $\dot{x}$ (t)
c	1 x n row matrix relating the measured output y(t) to the plant state vector x(t)
D	r x r disturbance state dynamic matrix
f	Frequency in Hz
f_c	Critical frequency in Hz
h	1 x r row matrix relating the disturbance w(t) to the disturbance state vector z(t)
K	1 x n row matrix of gain constants chosen to place the closed loop plant poles where desired
K_x, K_z	n x 1 and r x 1 column matrices of gain constants chosen to place the composite state constructor poles where desired
n	Number of elements in the plant state vector = number of poles in the plant model
r	Number of elements in the disturbance state vector = number of poles in the disturbance model
t	Time
u(t)	Total control signal
$u_c(t)$	Control signal required to regulate an undisturbed system
$u_d(t)$	Control signal generated to cancel the disturbance
V_θ	Output voltage of integrating gyro
w(t)	Total disturbance acting on system
$\hat{w}(t)$	Real time estimate of w(t) obtained from composite state constructor
x(t)	n-dimensional plant state vector

SYMBOLS (Continued)

$\hat{x}(t)$	Real-time estimate of x(t) obtained from composite state constructor
$y(t)$	Measured plant output
$z(t)$	r-dimensional disturbance state vector
$\hat{z}(t)$	Real time estimate of z(t) obtained from composite state constructor
τ	Torque in oz-in
θ_I	Inertial Position of Stabilized Platform in radians
$\ddot{\theta}_{INPUT}$	Rotational acceleration induced by electro-mechanical shaker
γ	Real valued constant
$(\cdot)$	Time derivative of ( )

ABBREVIATIONS

DAC	Disturbance Accommodating Controller
DDT&E	Design, Development, Test and Evaluation
LHP	Left Half Plane
MIRADCOM	U.S. Army Missile Research and Development Command
RHP	Right Half Plane
TASM	Two-Axis Stabilized Mirror
UAH	University of Alabama in Huntsville
μR	Microradians

SECTION 1

INTRODUCTION

SECTION 1, INTRODUCTION

A high performance compensator for stabilizing the Line of Sight (removing "spot jitter") in a helicopter-borne laser designator was developed and tested. The program evaluated a modern control design method - Disturbance Accommodating Control (DAC) Theory - that offered theoretical improvements in pointing stability of one to two orders of magnitude over compensators of conventional design. It was found that such improvements are possible, but they demand a much more rigorous analysis and test program than do conventional design techniques, plus a relatively clean, low noise system. The lessons learned from this program are presented as practical design guidelines for the benefit of future precision pointing and tracking programs. While evaluation of DAC theory was the objective of the study, many of the guidelines also apply to other modern control design procedures.

The concept of Disturbance Accommodating Control Theory was developed by Dr. C. D. Johnson, University of Alabama in Huntsville (UAH), (References 1 through 5). An experimental study was conducted to determine how well DAC Theory performed for various disturbance and plant model combinations (Reference 6). The promise of this technique prompted the U.S. Army Missile Research and Development Command (MIRADCOM) to initiate the design of disturbance compensation hardware for a precision pointing system. The system selected was the Two-Axis Stabilized Mirror (TASM), a unit developed to investigate an inertial balance stabilization concept. This unit included disturbance compensation designed by conventional techniques. Under Contract DAAH01-74-C-0176 to UAH, DAC theory was applied to design a new compensator for TASM. In this report, results of the above contract are referred to as the "Original UAH Design."

As a part of MIRADCOM's missile technology program for Automatic Tracking and Integrated Fire Control, an investigation was conducted in implementing the DAC theory into actual compensation hardware for TASM. This report presents the results of the investigation.

Airborne precision pointing and tracking systems must provide sufficient stabilization and tracking in the aircraft environment to allow a laser spot to be kept on the targets for homing missile guidance. These designator systems are either contained in a pod attached to the armament wing store or integrated into the helicopter. The DAC compensator was designed to suppress position error caused by the 11 Hz helicopter rotor frequency and its first harmonic at 22 Hz, along with transients from wind gusts, gunfire and coulomb friction in the stabilized mirror positioning system (see References 1 and 2). Figure 1 shows that improvements in pointing stability of from 3:1 up to 10:1 were obtained over the 11-22 Hz frequency range, based on side-by-side testing of the DAC and conventionally designed compensators. This compares with the 12:1 (22 Hz) to more than 100:1 (11 Hz) improvement

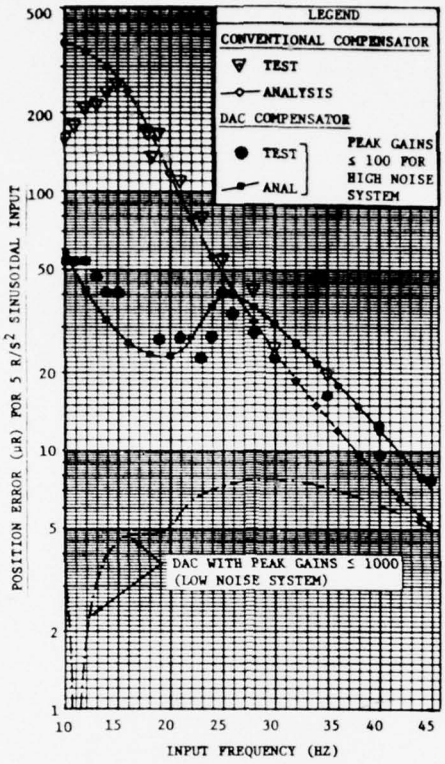


Figure 1. DAC versus conventionally designed compensator.

predicted analytically prior to the start of the program. What caused the big difference? The main culprit was the large (1 volt rms) broadband noise produced by the system's obsolescent integrating gyro and demodulation network. It was necessary to reduce the peak gains of the DAC compensator from the design value of 1000 to less than 100 to keep amplified noise from saturating the torquer amplifier. The damaging effect of this reduction on performance is shown in Figure 1.

While low noise hardware is now available that permits the use of gains exceeding 1000, system noise is still one of the major factors that limit how far modern control design techniques can be pushed. System stability, sensitivity to changes in system parameters, plus realizability of the design in actual hardware - these are other practical considerations that dictate how the theory is applied. In the sections that follow, key elements of the DAC Design, Development, Test and Evaluation (DDT&E) program will be examined. From this examination, we will develop: (1) tests the designer can apply to find out if his system is a candidate for DAC design, and (2) recommended procedures for carrying the initial DAC computer solutions on into workable, high performance hardware.

SECTION 2

DISTURBANCE ACCOMMODATING CONTROL (DAC) THEORY

SECTION 2, DISTURBANCE ACCOMMODATING CONTROL (DAC) THEORY

The Disturbance Accommodating Control Theory was developed by Dr. C. D. Johnson, University of Alabama in Huntsville (References 3-5). The unique feature of this technique is the "Composite State Constructor" - a simplified Kalman filter that provides simultaneous real-time estimates of both the plant state and disturbance state vectors, $\hat{x}$ and $\hat{z}$, respectively. The z estimate is used to generate a signal $-\hat{w}(t)$ that cancels (within estimation errors) the disturbance $w(t)$. The $\hat{x}$ estimate can then be used to control an essentially undisturbed plant.

The key to DAC theory is the way it represents disturbances. Since disturbances are generated by physical events and are transmitted through physical media, they typically possess a characteristic waveform. An example would be gunfire transients transmitted through the helicopter structure to a laser-designator unit. The gunfire disturbance seen by the laser designator will have a characteristic waveform determined by: (1) the gun recoil pulse shape, and (2) the filtering effects of the helicopter. The amplitude and time of occurrence of such disturbances are unpredictable. They have no well-defined statistical properties. However, their characteristic wave shapes can be predicted. Knowledge of this wave shape permits the design of a linear filter to estimate the actual disturbance in real time.

Figure 2 shows the block diagram and design equations for a regulator system with a DAC-designed controller. This design approach is based on "pole placement techniques." Starting with the design requirements, the designer first decides where he wants the poles of the closed loop plant and the composite state constructor to lie. Using matrix manipulation of the state equations, he then solves for a set or controller gain constants K that will place the closed-loop plant poles where he wants them (Reference 7). Finally, the state constructor poles are placed so they cancel quasi-steady disturbances (helicopter rotor harmonics) and rapidly detect and "absorb" transient disturbances (gun bursts, wind gusts)(References 1, 2 and 8). In theory, the farther into the left-half plane (LHP) these poles are placed, the more rapidly the disturbance-induced errors can be "absorbed." But placing poles deep into the LHP requires large gains. In any real system, there is a practical limit to where these poles can be placed without amplifying system noise to where it destroys system performance.

Notice that math models of the plant and the disturbance are required to design the composite state constructor. If the math model used in the design is not accurate, the poles may not wind up where they are "placed." The designer must perform stability and performance studies to make sure his design is insensitive to reasonable variations in both the math model and physical system parameters. These studies must also assure that the effects of any higher frequency dynamics neglected in the model are truly negligible.

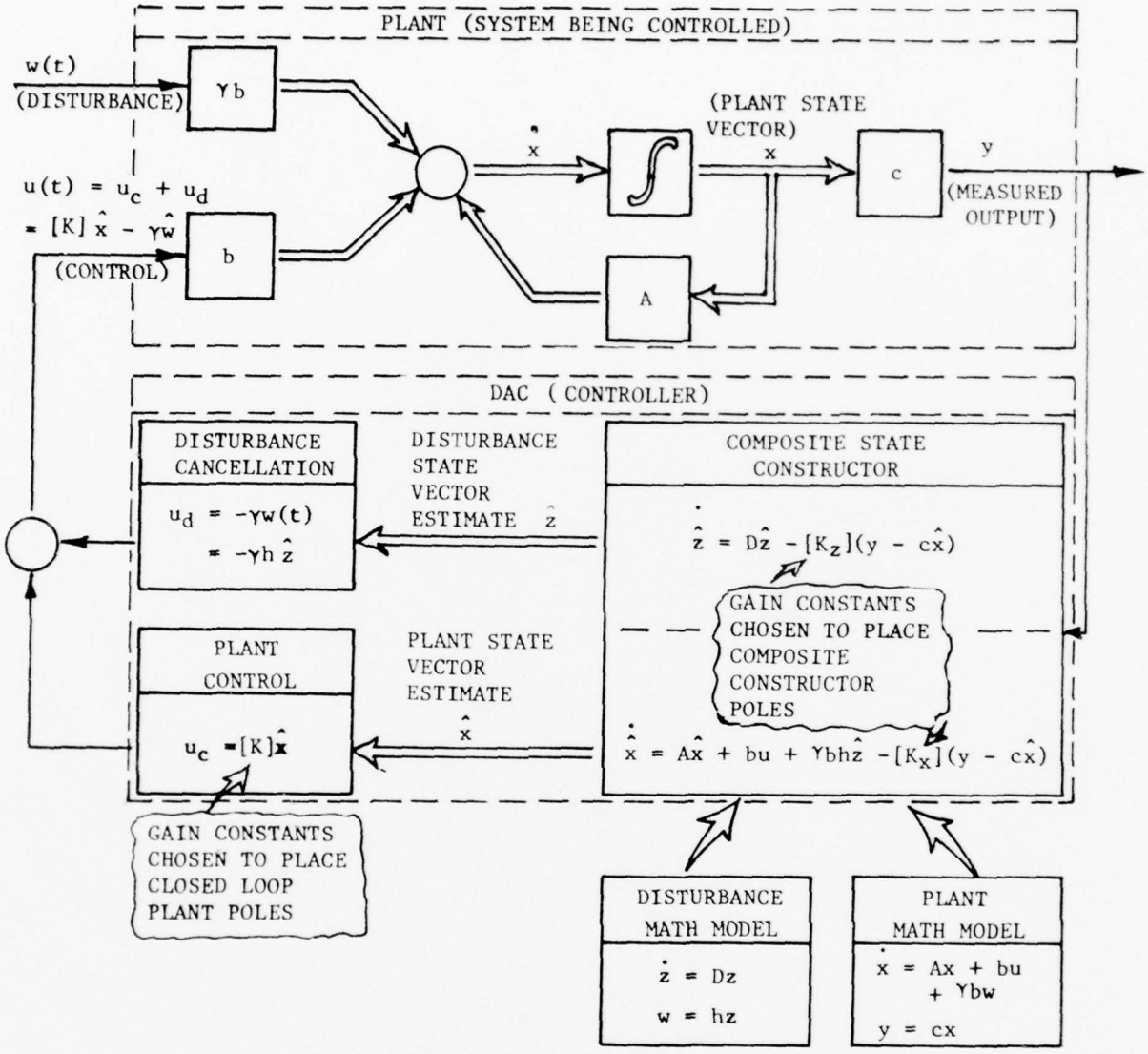


Figure 2. The DAC design model.

The "pole placement" design process typically produces a controller with a high gain over a broad bandwidth - the ideal noise amplifier. In some cases, the design can be carried out via Optimal Control techniques (Reference 9), which also lead to high gain designs. In either case, the art of the design comes from finding where to place the poles (or how to choose the optimizing penalty functions) to obtain good disturbance absorption while maintaining stability and controlling noise amplification. Before presenting the design guidelines, key steps in the hardware development process will be sketched. This background will add meaning to the design guidelines that follow.

SECTION 3

SYSTEM DESCRIPTION

SECTION 3, SYSTEM DESCRIPTION

MIRADCOM's Two-Axis Stabilized Mirror (TASM) was the test bed for the DAC. A small electro-mechanical shaker was used to introduce elevation axis rotational vibrations to the TASM. The resulting mirror deviations from a steady line of sight were measured to 10 microradian precision with an optical laser-detector system. Each test was first run using the TASM's compensator, which was designed via conventional techniques. The DAC was then switched into the loop and the same test repeated to obtain direct side-by-side comparisons of the performance of the two devices.

The TASM is an excellent test bed for precision pointing and tracking technology since it has an abundance of features that stress modern control design techniques (see Figure 3):

- Extremely broadband open loop "plant" with a lightly damped wire drive resonance at 170 Hz, and other significant dynamics from 3 Hz to 600 Hz.

- Broadband noise with particularly strong components at multiples (and submultiples) of the 900 Hz gyro spin frequency.

- Low control torque limited by the torque motor amplifier, which saturates at 7.3 oz-in of torque (8 volts input).

The TASM is inertially balanced so that rotational disturbances (such as those induced during the vibration tests) are mechanically offset, except for frictional effects. Integrating gyros on an inertial platform sense the elevation and azimuth position errors produced by the friction forces. Vibration testing was performed in the elevation axis only. The elevation position signal was used by the compensator to generate corrective commands to the torque motor, which positions the mirror through a wire drive system. The wheels in the wire drive mechanism are sized to drive the mirror through one half the angle of vibration. This maintains a fixed spot on a downrange target when the stable platform is inertially motionless. The compensator is designed to maintain a zero rate of departure from a fixed pointing position determined by the operator.

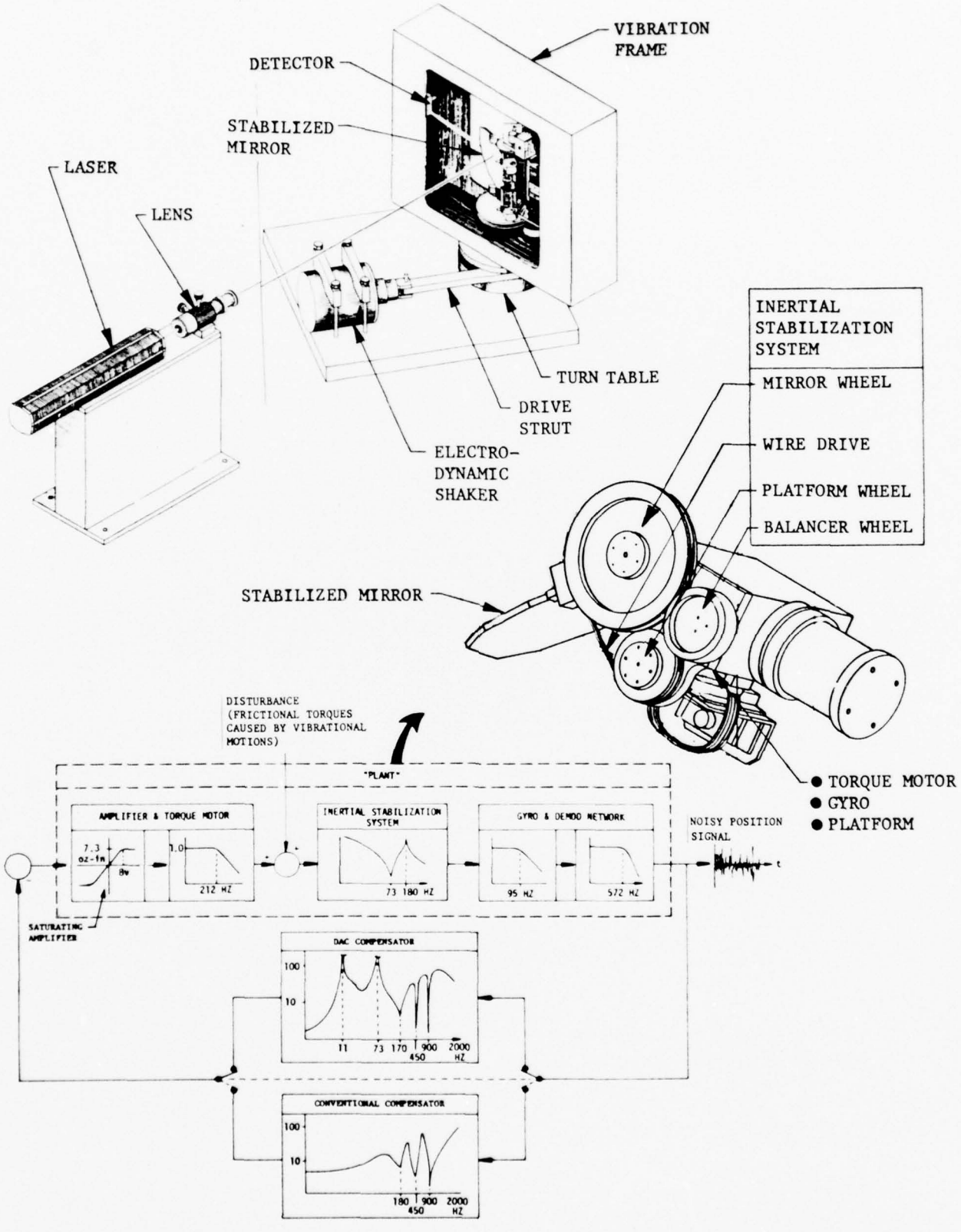


Figure 3. Test setup and system description.

SECTION 4

DESIGN, DEVELOPMENT, TEST AND EVALUATION (DDT&E) PROGRAM SUMMARY

SECTION 4, DESIGN, DEVELOPMENT, TEST AND EVALUATION (DDT&E) PROGRAM SUMMARY

Evaluation of DAC design techniques was accomplished via a 12-month research program which emphasized highly interactive Design/Development and Test/Evaluation Phases. This interplay (Figure 4.0) was deliberately designed to:

- *Drive out potential problems in applying DAC theory*
- *Develop workable design solutions*
- *Evolve design guidelines for future application of the theory.*

I. DESIGN AND DEVELOPMENT

The program started with the fabrication of a design developed by the University of Alabama in Huntsville (UAH) under a prior contract (Reference 2). In parallel with this, a rigorous math model test verification program was conducted to be ready for subsequent re-designs, which were a planned part of the program. The exact components in the math model - the gyro and demodulation network, the torque motor and amplifier, and the inertial stabilization system - were individually tested and results compared with the analysis. Four major differences were identified which had a significant effect on the design:

1. The torque motor amplifier gain and motor saturation torque were each one-half of the predicted value (examination of the actual hardware showed 1/4 of the torque motor field windings were being used, rather than 1/2 as stated in the documentation). This severely limited the ability of the system to execute a control command and doubled sensitivity to system noise.

2. The gyro roll-off frequency occurred at 95 Hz instead of the documented 160 Hz. This produced phase lag that significantly impacted system stability. Additional compensation was required.

3. The 60 Hz zero in the inertial stabilization system model occurred at 73 Hz. This required shifting one of the DAC compensator poles, which had been deliberately placed at the zero frequency, and sacrificing some design performance to obtain stable operation.

4. The noise riding on the demodulation network output was much more severe than anticipated. Eliminating the known primary components at 450 and 900 Hz with notch filters revealed significant broadband noise over the 10-100 Hz range, where the high gain compensator poles had been placed. Compensator gain had to be severely limited over this range to keep amplified noise from saturating the torquer amplifier.

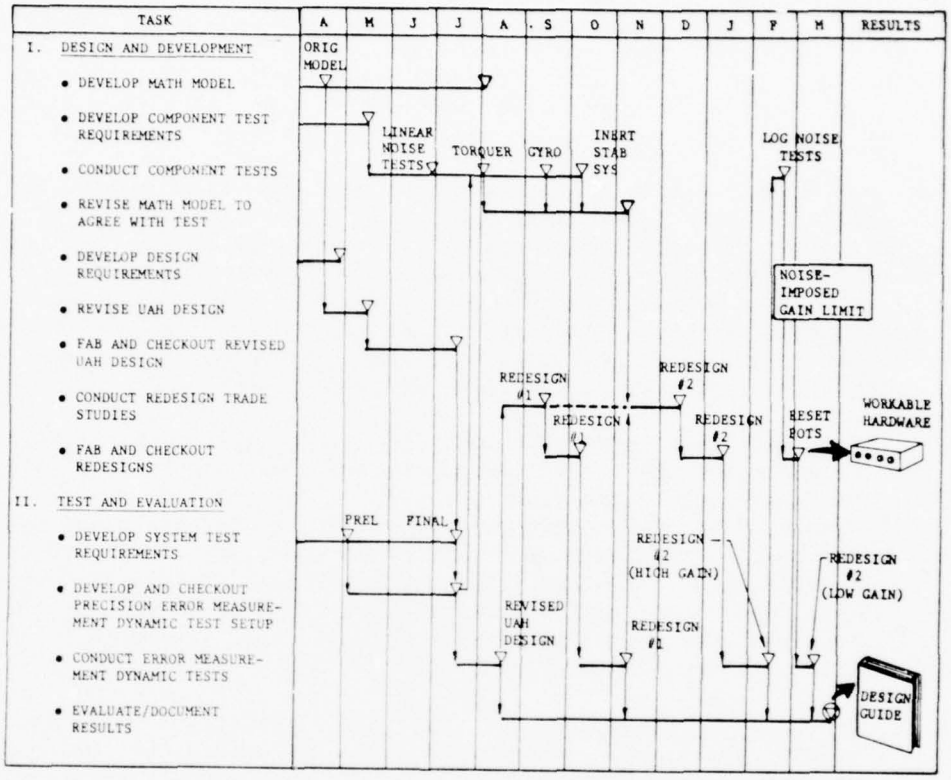


Figure 4.0. DAC DDT&E program.

The high performance DAC designs were highly sensitive to changes in the math model, which was the primary design tool. The initial design, plus the first redesign were made while the math model was still in the process of being verified by test. The hardware was deliberately designed to be easily modified. All pole and zero coefficients were adjustable through potentiometer settings. All fixed resistors and capacitors were placed on headers that were readily removed and replaced. Room was reserved on the circuit cards for increasing the order of the compensation network. All of these provisions for change were used repeatedly as the design evolved. The original UAH design was modified extensively to account for the known math model changes prior to putting the unit into test. Three additional redesigns were made to improve system performance and to evaluate design techniques that could benefit future programs.

II. TEST AND EVALUATION

The target end-to-end accuracy of the test setup was ±10 microradians (μR). The laser and detector alone were calibrated to ±1 μR. A 10 μR arc is equivalent to 2 arc seconds, or 1/1800th of a degree. *A system with ±10 μR pointing stability could project a laser beam across a football field, focus it on the period at the end of this sentence and keep it from ever drifting outside the perimeter of this little dot.*

After consulting with precision measurement experts from both Boeing and MIRADCOM, a list of potential error sources were compiled for the planned test setup. The rotational vibration system was developed under previous laboratory studies which required a lesser degree of precision. A systematic test program was conducted to isolate each candidate error source in this test setup, measure its contribution and reduce it to acceptable levels. The most significant error sources are listed below (refer to Figure 4.1):

1. Turntable Bearing Wobble: The truck axle bearing in the turntable produced 3000 μR errors around twin roll/azimuth coupled 15 Hz resonant peaks. The error was reduced and shifted upward in frequency by placing teflon shims under the turntable and torquing the bearing retainer nut to where the input wave form started to show measurable Coulomb friction distortion. Future designs of this type should employ a turntable on the top as well as the bottom of the vibration frame braced by ample framework to eliminate any chance of side play.

2. Vibration Frame Distortion: The "rigid" vibration frame showed significant elastic deformation (1000 μR) within the 10-50 Hz frequency range in which the DAC would be tested. The frame was designed by beam theory without considering the local load paths required to distribute the TASM inertial loads into the frame. Failure to recognize local structural deformation mechanisms is the most common cause of undesirable vibration modes appearing in a design. The checkout tests were designed to detect these modes and either eliminate them, or map their effect on measured position error. The frame was structurally reinforced to move the onset of these errors above 50 Hz.

3. Laser Beam Distortion: Errors of 200 μR were detected from two sources: thermal gradient (air current) distortion of the laser beam, and 120 Hz oscillations in the intensity of the He-Neon laser beam. These effects were controlled by moving the laser within two feet of the mirror and adding a 120 Hz notch filter to the detector output. Where these simple solutions are not adequate, optical systems (spatial filter, beam expander, re-collimator) and electronic networks (averaging circuits) are available to control thermal gradient effects, and beam intensity fluctuations, respectively.

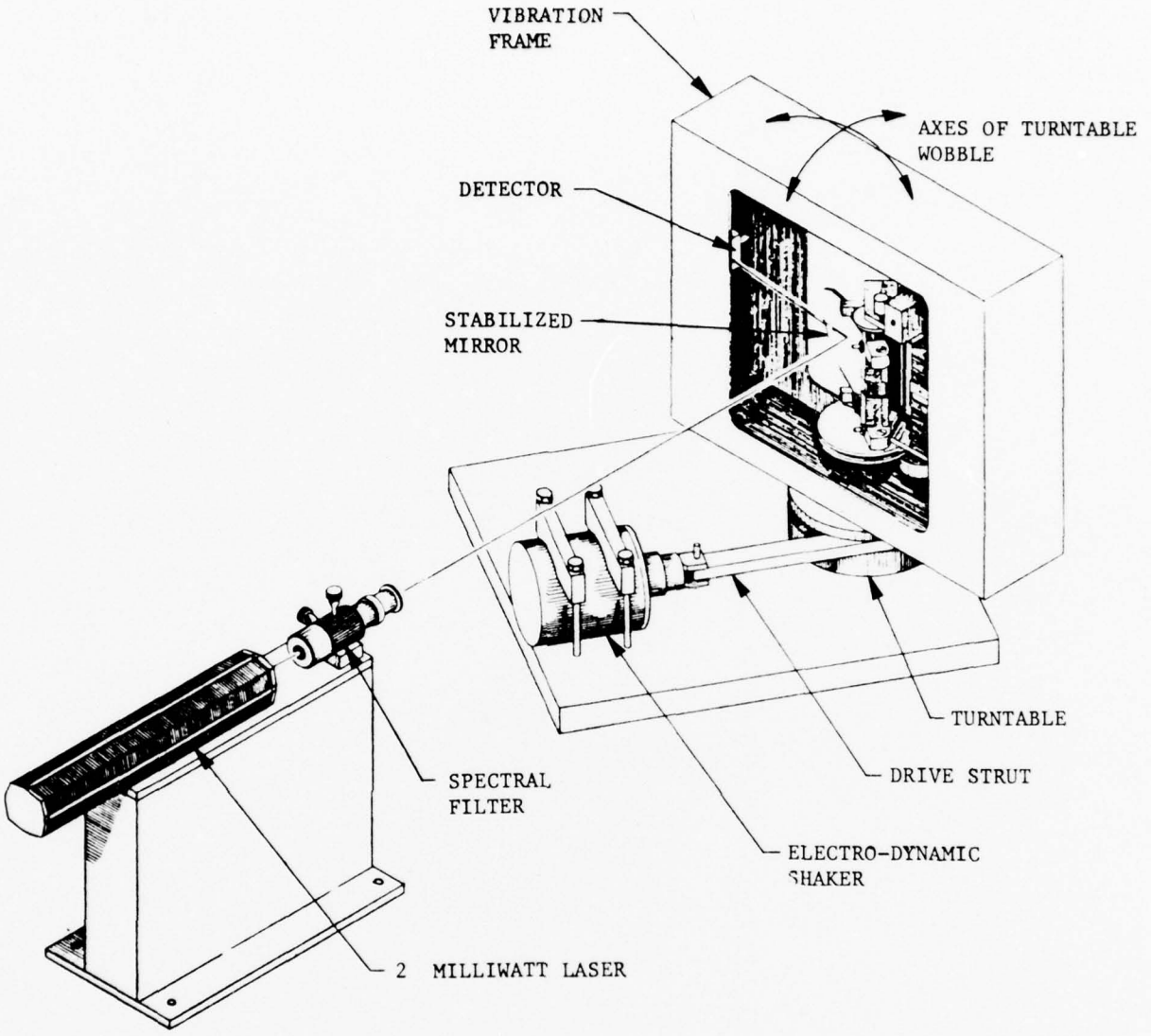


Figure 4.1. Dynamic test setup for precision error measurement.

4. Background Vibration: The test was initially set up on an air bearing "isolated" pad. Closing a door or walking in the facility produced transient errors of up to 200 μR. The test was moved into an isolated facility which had a 6-inch concrete floor poured directly on the earth. The tile floor covering proved to be an effective isolator of background disturbances. Surface waves created by the vibration system were disrupted by the joints in the tile before they could reach the laser. Normal activity (walking, electrodynamic shaker operation) during the test produced disturbances of ±4 μR or less.

The calibrated test setup was used to measure compensator performance and evaluate the results of design changes. The designs that evolved from this process are discussed in the next two sections.

SECTION 5

THE DESIGN CHALLENGE IN RETROSPECT

SECTION 5, THE DESIGN CHALLENGE IN RETROSPECT

Two features of the TASM - the high broadband noise threshold, coupled with a readily saturated torque motor amplifier - combined to impose hard limits on compensator gain, and consequently on system performance (Figure 5). No features of DAC control theory and no amount of careful pole placement were capable of increasing performance above this noise-imposed limit. The test program demonstrated that pushing performance any further would require attacking the problem at its source - replacing the noisy TASM integrating gyro network with cleaner components.

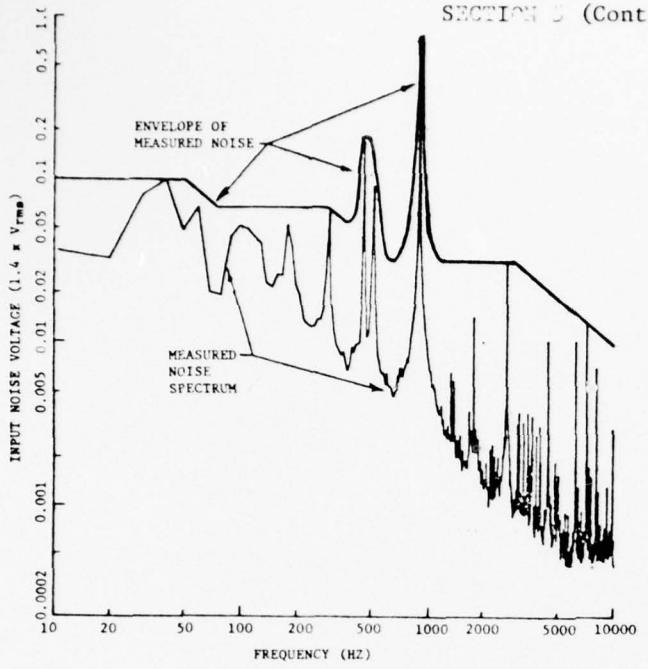
At the start of this program, the existence of the large noise spikes at 450 and 900 Hz were known. What was not recognized was the broadband noise threshold that was masked by these large spikes. In our component test program, we made the mistake of analyzing the noise using a linear, rather than a logarithmic amplitude scale. This made it look like we could notch out the 450 and 900 Hz peaks and eliminate the noise problem. Once the presence of the broadband noise was recognized, the only design recourse was reduction of compensator gain. The other options, adding more noise filters and shifting pole placements, were ruled out by two practical considerations: (1) the noise was too broadband to attack with notch filters, and (2) system stability did not permit shifting the poles or introducing more phase lag with low pass/bandpass filters.

Figure 5a shows the noise spectrum measured at the compensator input. The envelope of this noise was combined with the torquer saturation characteristics (Figure 5b) to obtain the compensator gain limit shown in Figure 5c. For example, the 10-50 Hz compensator gain limit of 80 was computed as follows:

$$\text{Gain Limit (80)} = \frac{\text{Saturation Voltage (8.0 Volts)}}{\text{Noise Envelope (0.1 Volts)}}$$

In this 10-50 Hz frequency range, a compensator gain of 80 or more would amplify the noise to where the torquer was fully saturated; no control commands could be executed. In the calculation above, the closed loop system had little effect on the noise amplification. This is not the case in general. Systems with lightly damped closed loop poles will amplify the open loop noise spectrum at the closed loop resonant frequencies (frequencies at which the Nyquist diagram approaches the -1 point). Such closed loop "coloring" of the noise envelope must be included to develop meaningful noise-imposed gain limits for compensator design.

The gain limit shown in Figure 5c proved to be a very real constraint on the design. Figure 5d shows the drastic loss of performance that resulted from having to reduce the peak compensator gains from 1000 to 100. This order-of-magnitude reduction increased position error over the critical 10-25 Hz range by a factor of 10.



a. A High Noise Level

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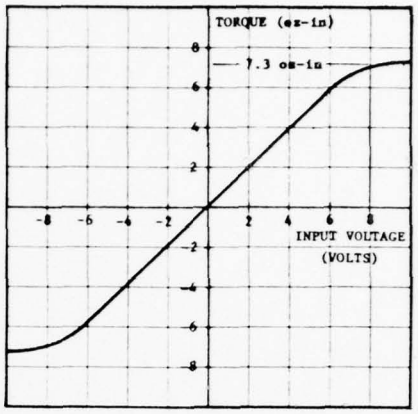

b. An easily Saturated Torquer

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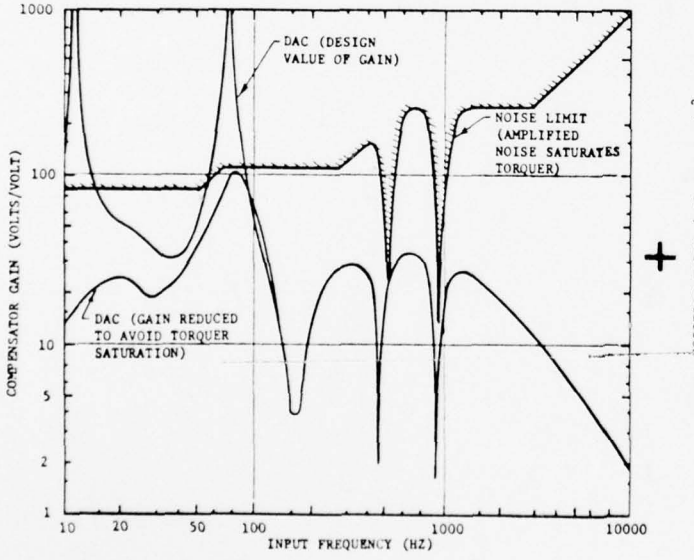

c. Severe Limits on Compensator Gain

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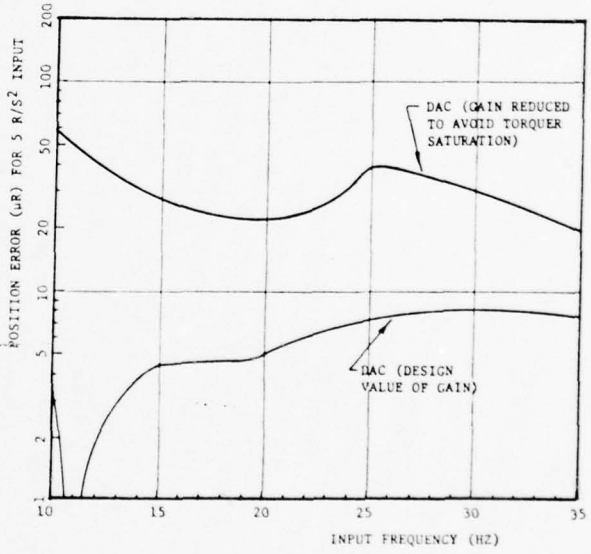

d. Drastically Reduced Performance

Figure 5. The real world.

SECTION 6

THE DESIGN ITERATIONS; LESSONS LEARNED

SECTION 6, THE DESIGN ITERATIONS; LESSONS LEARNED

Five different DAC designs were built and tested to optimize DAC performance in the TASM, and evaluate design options for future applications. The features of the original conventional compensator and each of the five DAC designs will now be developed. What was learned from this sequence of design steps will be underscored to support the Design Guidelines and Procedures presented in the next two sections.

The compensators will be discussed in the following order:

- Conventional Compensator
- 5 DAC DESIGNS:
  - Original UAH Design
  - Revised UAH Design
  - Redesign #1
  - Redesign #2 (High Gain)
  - Redesign #2 (Low Gain)

A foldout page appears opposite the discussion of each compensator. The right half of the foldout shows the block diagram of the closed loop system, including Bode plots of the compensator and plant model used in the compensator design. On the left, the Nyquist diagram and the predicted position error plots appear, along with a summary of changes (where applicable). The latter lists the elements of the compensator that were changed from the previous design. Elements that have been changed are also encircled with dashed lines on the block diagram.

NOTE: The following narrative has been printed on even numbered pages only so that the text can be read as the corresponding foldout page is examined.

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1. Conventional Compensator

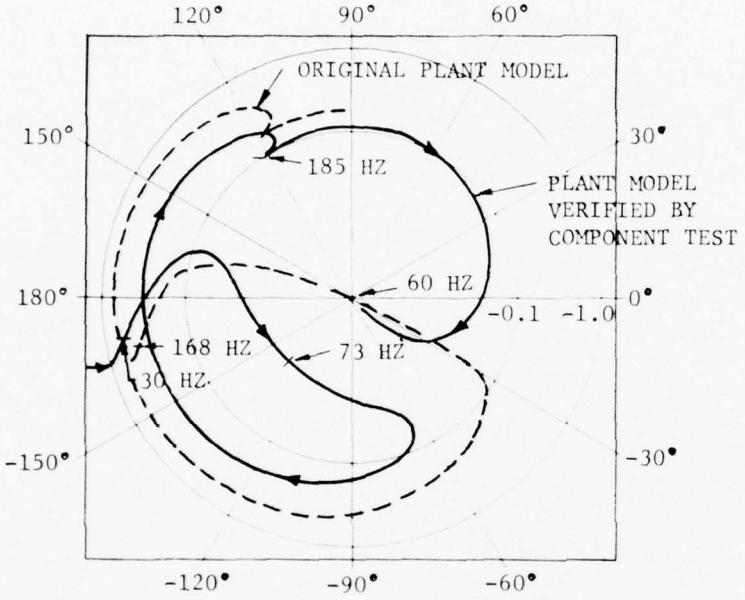
The Conventional Compensator will be discussed first, since it is the basis of comparison of all the subsequent DAC designs. The original TASM compensator was designed by conventional techniques. The numerator and denominator of the design equations were each of eighth order. A fourth order slice of this was used to create rather broad notch filters for the 450 Hz and 900 Hz gyro noise components. The design equations appear at the bottom right of Figure 6.1 (foldout page). Immediately above is the plot of the compensator gain versus frequency. Notice that the compensator gain is below the noise limit at all frequencies, being at least a decade below at most frequencies. Of course, the designers did not possess any such noise limit curve at the time they created the design. The Nyquist diagram (upper left of foldout) shows that the gains were limited by the need to maintain adequate stability margins, rather than by noise.

The plant model that was used in the design appears in block diagram form across the right center of the foldout. Notice in the block diagram how the "disturbance" affects the plant. The friction in the pulley wheels and wire drive mechanism (Inertial Stabilization System - see Figure 3) converts the disturbing angular motions into frictional torques that produce undesirable changes in position. The plant Bode plot is immediately above the block diagram. This plot also shows how the plant model changed as a result of input-output testing of the plant components (amplifier, torquer, inertial stabilization system, integrating gyro, and demodulation network) during the DAC program. The solid line shows the model as the conventional compensator designers believed it to be, while the dashed line shows its true characteristics, as verified by test.

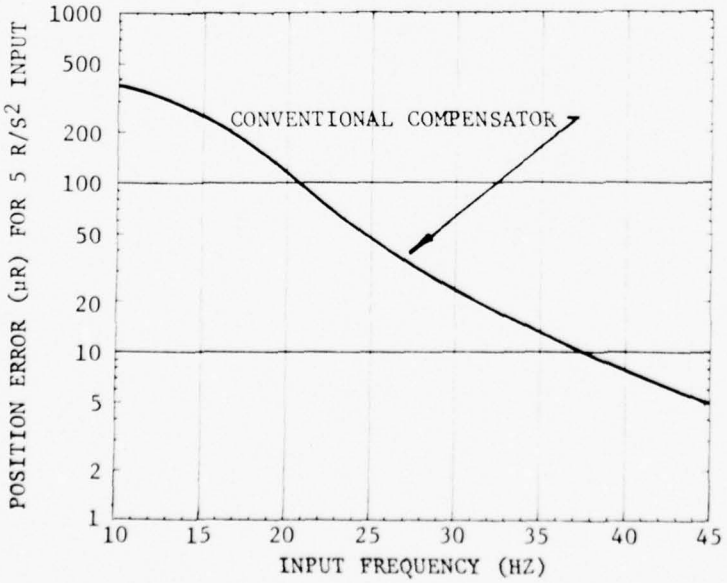
The solid line Nyquist plot shows the true system stability, while the dashed line shows the stability picture predicted at the time of the design. The system is actually more stable than predicted. The compensator gains could have been increased to squeeze out a little better error performance without driving the system unstable, or exceeding the noise limit.

The lower left figure plots position error versus frequency for the system. This is the elevation axis error in stabilized mirror position when the TASM is disturbed by a sinusoidal rotational acceleration of 5 rad/sec^2 peak value ($\ddot{\theta}_{INPUT} = 5 \sin 2\pi ft$; f = input frequency in Hz). Since the peak input acceleration is held constant, the peak input position is falling off in proportion to f^2. This decrease in position input is the reason that mirror position error falls off with frequency; the roll off in this frequency range is not due to any feature of the plant or compensator.

The conventional design is not acceptable for helicopter-borne operations, since it has its greatest errors over the 11-22 Hz region driven by the rotor inputs. The need to improve performance in this frequency range, coupled with the potential offered by DAC theory, led to MIRADCOM to contract with Dr. Johnson, UAH, for the original DAC design discussed next.



Nyquist Diagram For Conventional Compensator



Position Error For Conventional Compensator

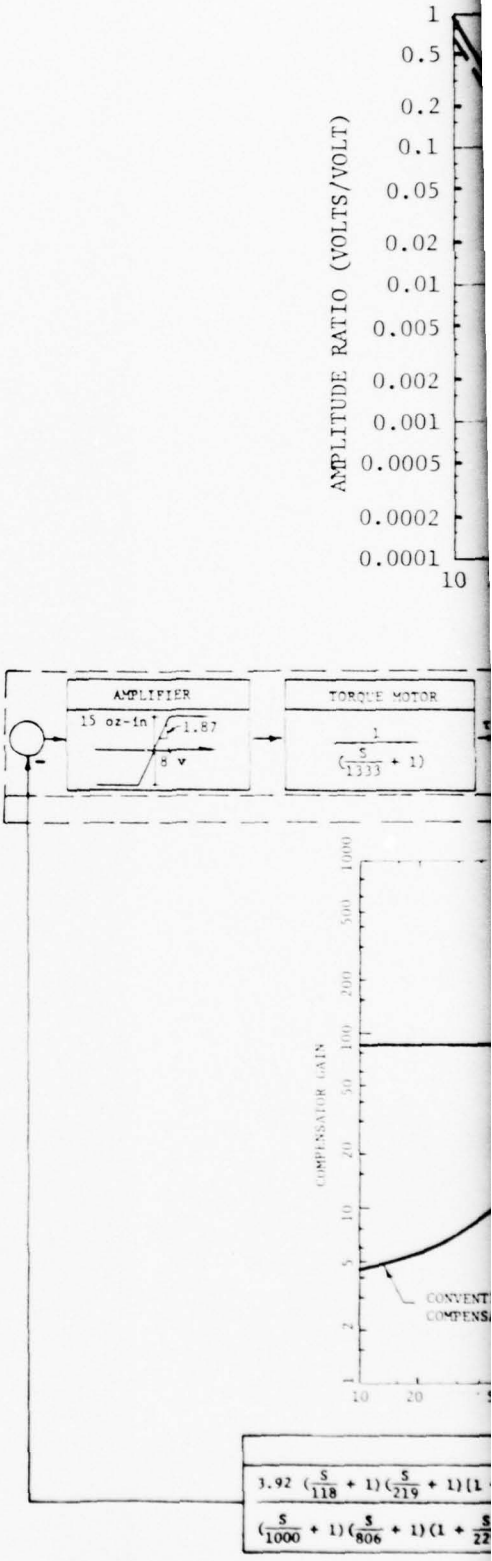
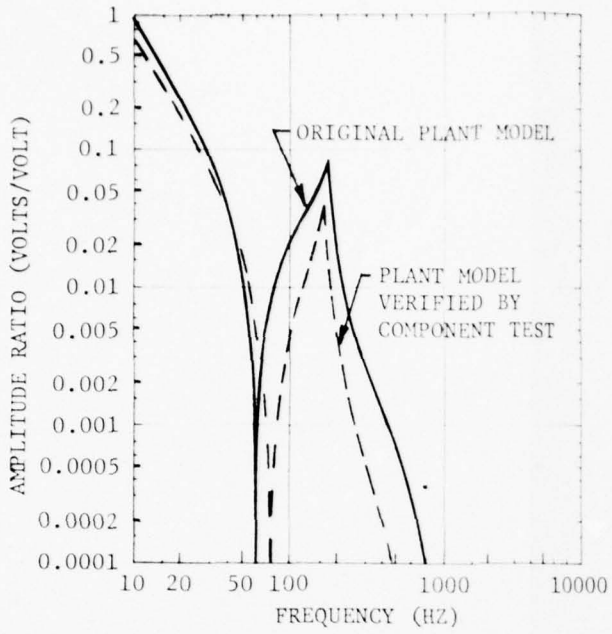
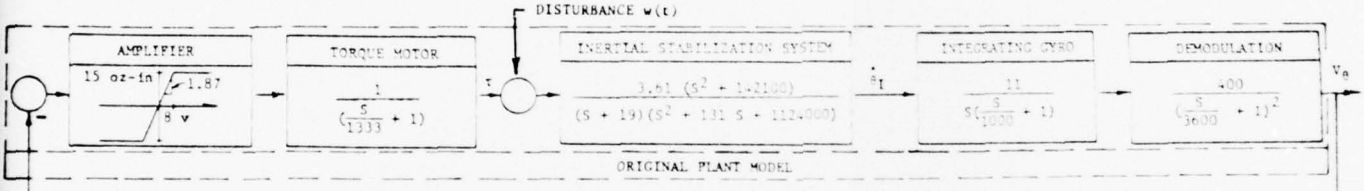
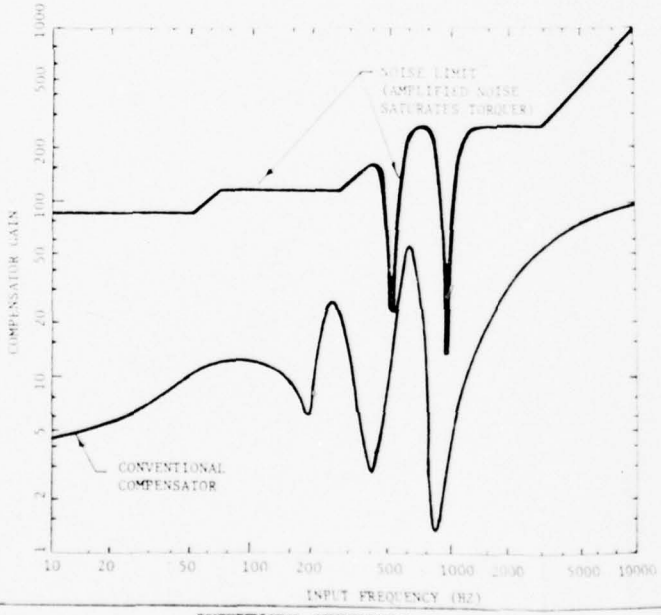


Figure 6.1. Conventional compensator.







CONVENTIONAL COMPENSATOR AND NOTCH FILTERS

$$\frac{3.92\left(\frac{S}{118}+1\right)\left(\frac{S}{219}+1\right)\left[1+0.228\left(\frac{S}{1230}\right)+\left(\frac{S}{1230}\right)^2\right]\left[1+0.104\left(\frac{S}{2690}\right)+\left(\frac{S}{2690}\right)^2\right]\left[1+0.049\left(\frac{S}{5680}\right)+\left(\frac{S}{5680}\right)^2\right]}{\left(\frac{S}{1000}+1\right)\left(\frac{S}{806}+1\right)\left(1+\frac{S}{229}\right)\left[1+0.244\left(\frac{S}{1563}\right)+\left(\frac{S}{1563}\right)^2\right]\left[1+0.129\left(\frac{S}{4060}\right)+\left(\frac{S}{4060}\right)^2\right]\left(1+\frac{S}{38400}\right)}$$

ntional compensator.

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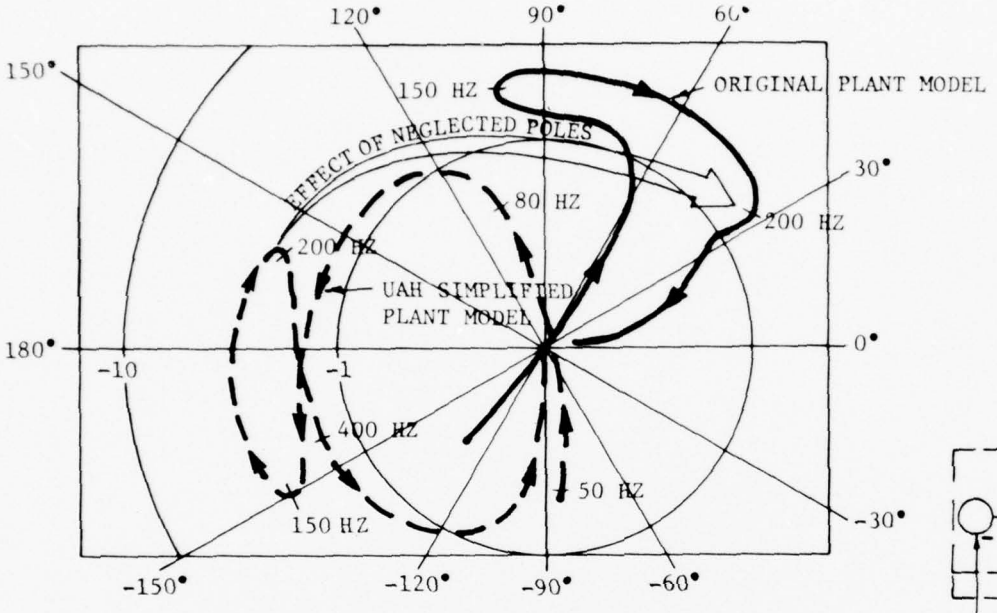
2. Original UAH Design

The original UAH DAC design was developed assuming that a noise-free rate output could be obtained from the TASM. It was also assumed that all plant poles with break frequencies of 1000 rad/sec or greater could be neglected in the DAC design. This reduced the plant model to third order, as shown opposite. The key design requirements were to maintain a zero rate of departure from a fixed gyro position in the face of four disturbances: (1) wind gusts and Coulomb friction, (2) 11 Hz, (3) 22 Hz, and (4) gunburst transients. The disturbance suppression required four second order modules, as shown in Figure 6.2. A fifth second order module was added to eliminate the lightly damped 168 Hz wire drive resonance in the plant. The DAC solution provided a pair of nearly critically damped right half plane poles for this purpose (see Block V opposite). This block produced over 100° of phase lead, at near unity gain at 168 Hz.

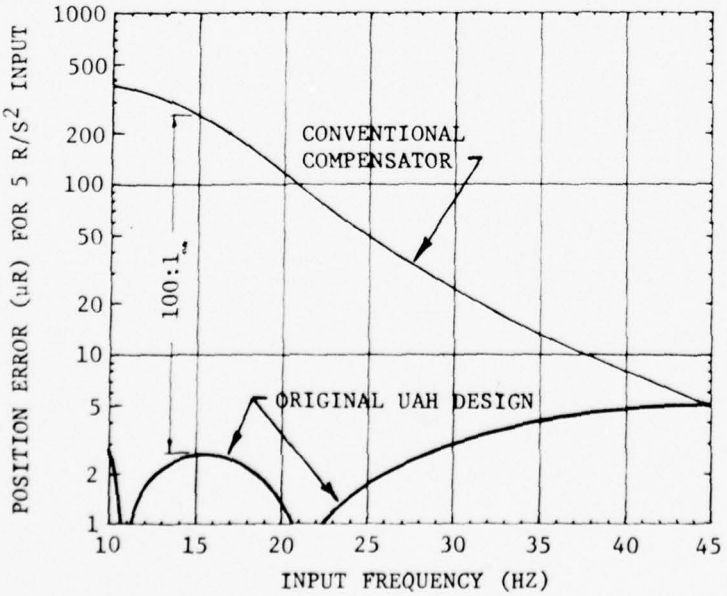
After several pole placement iterations to reduce DAC gains to realizable values, the design converged to the equations shown in the Figure 6.2 block diagram. Reference 1 presents the details of the design.

Using the simplified plant model, Nyquist and analog simulations of the design were performed by UAH. Because of the RHP poles in the compensator, the Nyquist plot had to encircle the -1 point for stability. The dashed line Nyquist plot shows the UAH design to be very stable, with stability margins increased by increasing compensator gain. The solid line (original plant model) reconstruction, which was made following analysis and some hardware testing on the DAC program, shows how the higher frequency poles in the plant produced enough lag in the critical 80-200 Hz range to completely eliminate the Nyquist encirclement of the -1 point.

The plot at the lower left shows the results of the UAH analog simulation of position error. The analog simulation was nonlinear, representing the saturating amplifier by the model shown near the center of the foldout page. Up to two orders of magnitude improvement were predicted for DAC, with even greater performance at 11 and 22 Hz. This was the design that started the DAC DDT&E program.



Nyquist Diagram For Original UAH Design



Predicted Position Error For Original UAH Design

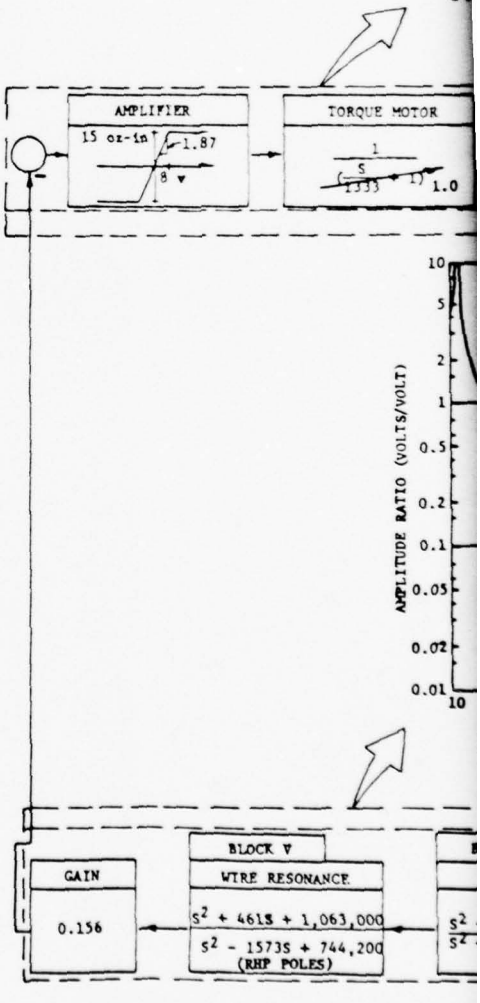


Figure 6.2. Original UAH desi

MODEL

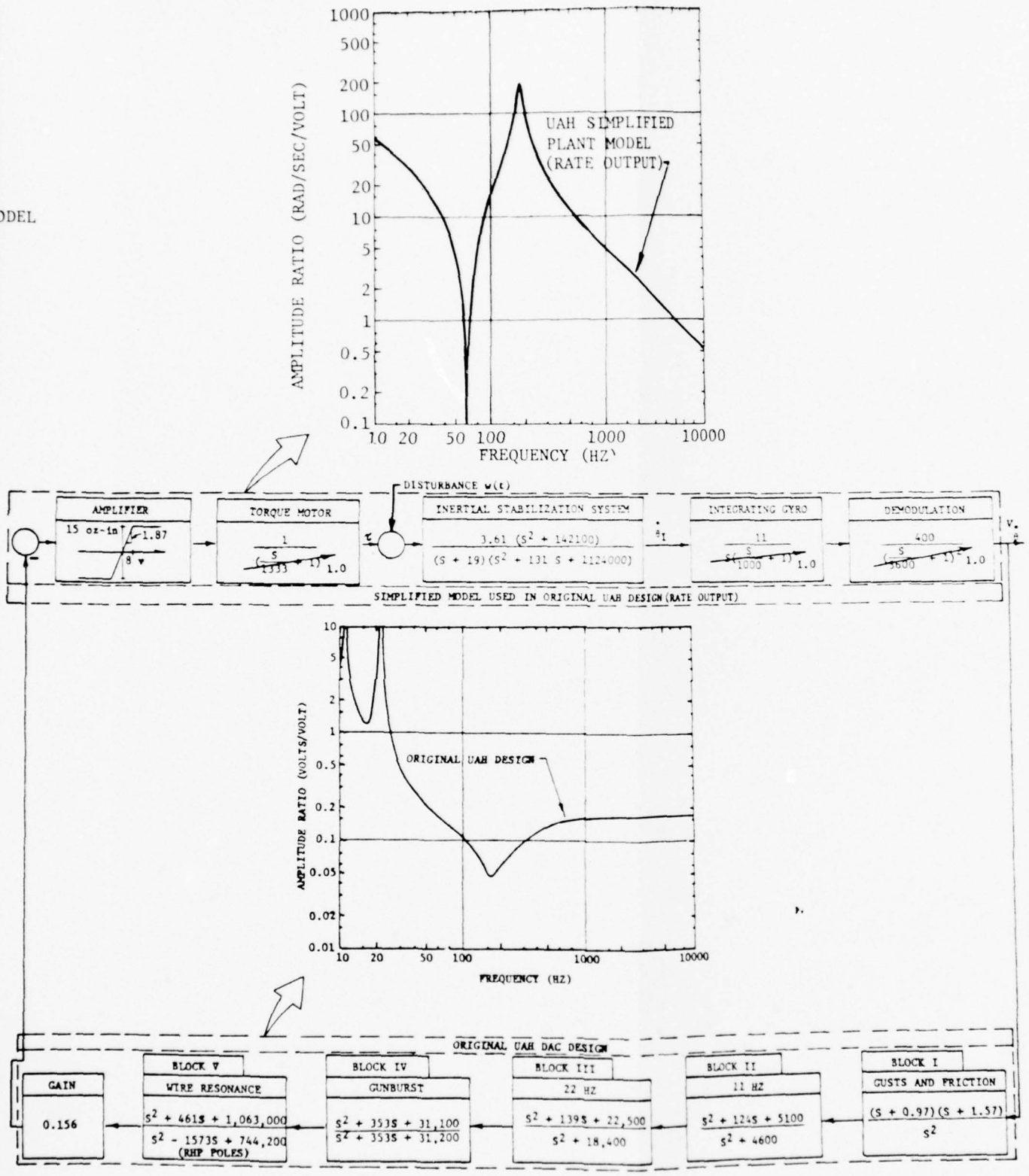


Figure 6.2. Original UAH design.

3. Revised UAH Design

The first step in the DAC DDT&E program was to find a way to obtain a rate output from the TASM. Since torquer current is proportional to rate, the original idea was to use this as the DAC input signal. However, investigation of the actual hardware showed this to be impractical. First, the torquer current signal was even more corrupted with noise than was the gyro output. Second, the torquer circuit contained limiting diodes that switched it from a rate to a rate integrating mode for low level inputs.

Since the TASM could not be modified to output an acceptable rate signal, it was decided to add a "differentiator" to the DAC design. This module was designed to act like a differentiator out to 1000 rad/sec (160 Hz). Since differentiators are by nature noise amplifying devices, the module was placed at the end of the DAC to minimize the chance of saturating operational amplifiers. The "differentiator" proved to be a poor design decision for two reasons: (1) the TASM had a much higher noise floor in the 0-200 Hz range than anticipated, and (2) the "differentiator" added more phase lag to an already phase destabilized system. Since our noise measurements on TASM showed large spikes at 450 and 900 Hz, two notch filters were also added to the UAH design. This brought the total DAC compensator design equations to 15th order. Changes to the UAH design were predicted to have a negligible effect on position error. As shown on the lower left of the foldout, improvements of 100:1 were still anticipated.

Actual hardware was developed using components that were screened to ±1% accuracy. The design equations were realized using the Rectangular Method of Programming. This method uses feed-forward paths to shape the numerator polynomial and feedback paths to form the denominator polynomial. Figure 6.3a illustrates this design approach for Block II of the DAC. The Block II design was developed into a network of linear amplifiers using first order design models. These design models idealize each operational amplifier as having infinite gain and input impedance.

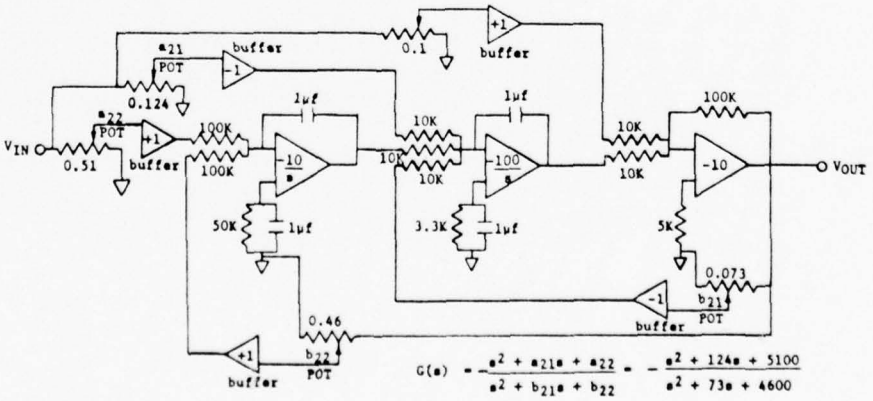


Figure 6.3a. Rectangular design method applied to block II.

3. (Continued)

Each coefficient in the five main DAC blocks was made variable by inserting potentiometers in the feed-forward and feedback paths. In addition, all fixed resistors and capacitors were placed on headers that could be unplugged from the circuit cards for quick replacement or repair. We anticipated that testing the plant and the closed loop system would lead to changes in the compensator design. Our hardware was designed to simplify these changes rather than minimize the number of components used.

The actual DAC hardware was tested block-by-block and end-to-end and shown to reproduce the design equations faithfully out to 2000 Hz. A compensator was placed around Block V to stabilize its RHP poles. The compensator was designed to switch itself out of the loop whenever the DAC was switched into closed loop operation in the TASM. Above 2000 Hz, the hardware started to depart from the equations, due to second order effects neglected in the design. A 7000 Hz low pass filter was added to suppress a high frequency resonance in the DAC produced by these secondary effects.

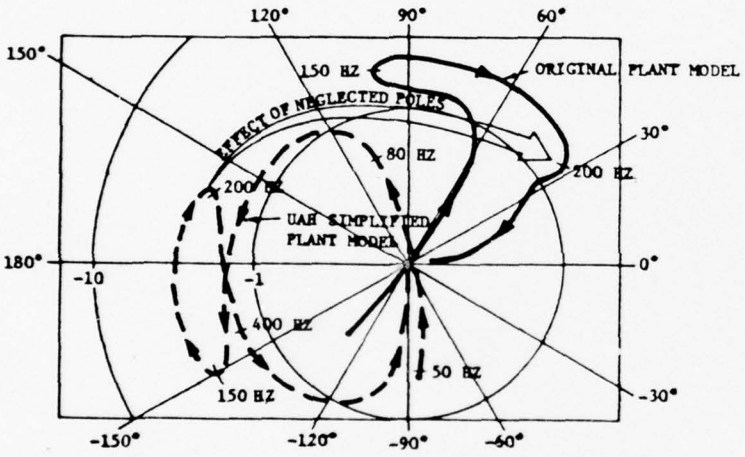
By the time the Revised UAH Design hardware was being readied for testing in the TASM, our math model had been implemented on the digital computer. Initial Nyquist and error analysis results were being evaluated to pinpoint any errors in the digital simulation. The Nyquist analysis showed the system to be unstable, but this was attributed to an error in the computer input.

When the DAC hardware itself was switched into the TASM loop, its operational amplifiers saturated instantly, giving no clue to the source of the problem. Two days of careful module-by-module testing failed to uncover any hardware problems. The math model results started to look more and more credible.

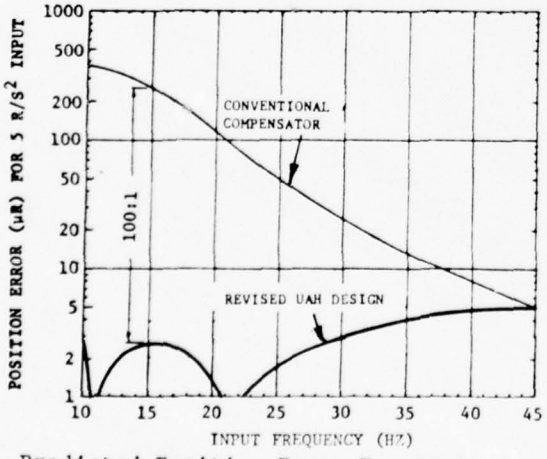
Several days were required to completely debug the computer solution and verify that there were no errors in it. While we were doing this, Dr. Johnson performed a graphical solution that showed the system was indeed unstable due to the cumulative effects of the phase lag terms neglected in the plant model. The solid line Nyquist plot on the right shows how this phase lag distorted the Nyquist diagram away from the necessary encirclement of the -1 point, making the system highly unstable. The redesign we made to restore stability is discussed next.

SUMMARY OF CHANGES: REVISED UAH DESIGN

CHANGE	REASON FOR CHANGE
• ADD "DIFFERENTIATOR"	• UAH DESIGN ASSUMED RATE SIGNAL COULD BE OBTAINED; MODIFYING TASM HARDWARE TO OUTPUT RATE (RATHER THAN POSITION) PROVED UNFEASIBLE
• ADD 450 HZ NOTCH FILTER • ADD 900 HZ NOTCH FILTER	• REMOVE LARGE NOISE SPIKES GENERATED BY 900 HZ GYRO SPIN FREQUENCY
• INCREASE GAIN BLOCK GAIN FROM 0.156 TO 156	• OFFSET 1/1000 GAIN IN "DIFFERENTIATOR"



Nyquist Diagram For Revised UAH Design



Predicted Position Error For Revised UAH Design

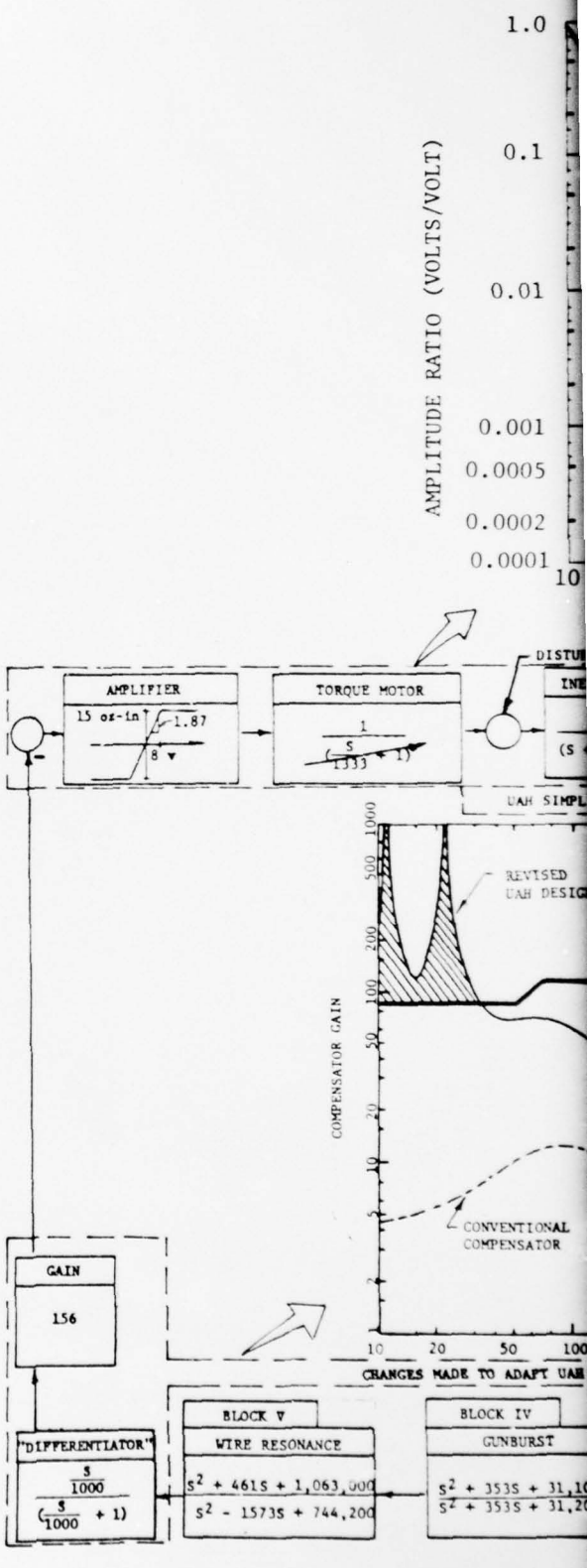


Figure 6.3. Revised UAH design.

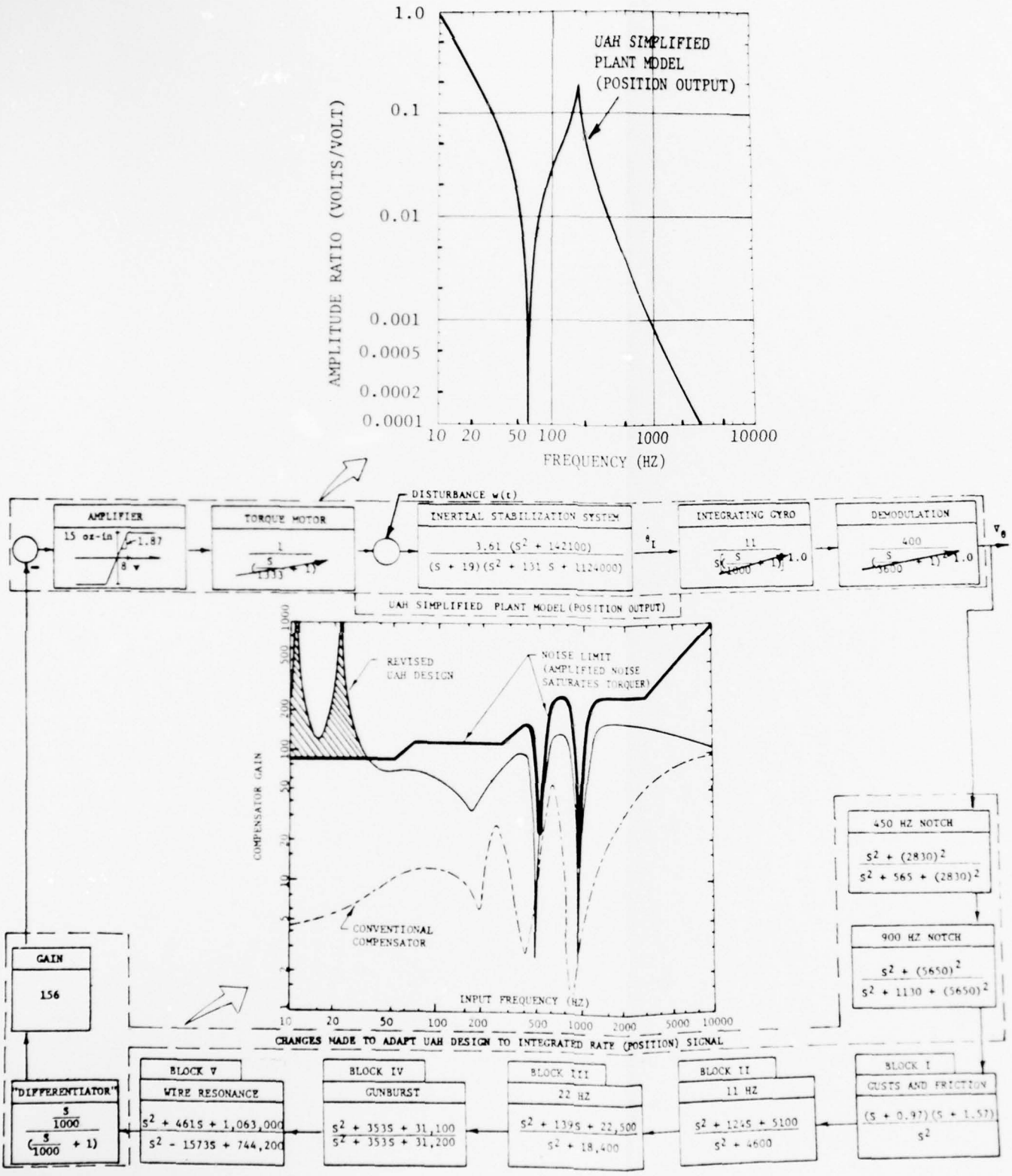


Figure 6.3. Revised UAH design.

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4. Redesign #1

The simplest way to recover stability was to add lead compensation over the critical 150-1000 Hz range. We recognized that the lead networks might increase the DAC gain to where noise amplification became unacceptable. During checkout of the module-by-module testing of the DAC hardware, we measured the output of the notch filters. The signal appeared relatively clean, with well dispersed frequency components. Since this was a research program, we elected to take the risk of being able to make a high gain design work. We covered ourselves by initiating a redesign trade study to be prepared with a totally new design in case this one failed.

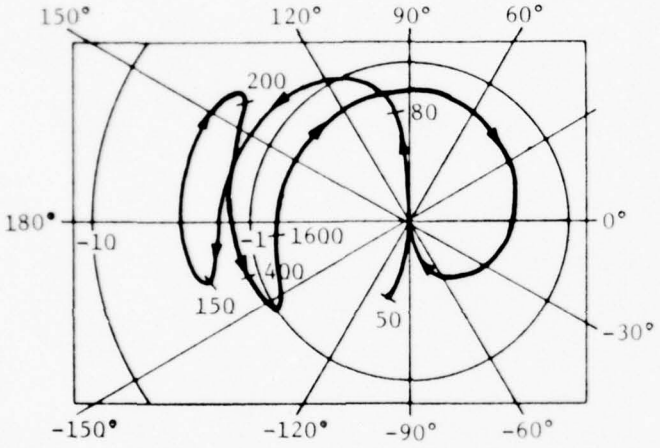
The changes that were made to the hardware are summarized at the upper left of the foldout page (Figure 6.4). These changes are also outlined in the compensator block diagram on the lower right. Of the original five DAC blocks, only one - Block IV - was changed. This block was converted from suppressing high frequency gunburst transients to a second order lead/lag network. A second identical lead/lag network was added (Block IV'), bringing the compensator to 17th order. The "differentiator" pole was moved from 1000 to 20000 rad/sec to reduce phase lag.

The Nyquist diagram on the right shows the net effect of these changes. A banana-shaped encirclement of the -1 point was achieved. The DAC gain block setting was reduced from 156 to 105 to center the "banana" about the -1 point. Reducing the gain increased the predicted position error slightly (see plot at lower left). However, it still appeared that improvements of 75:1 could be achieved.

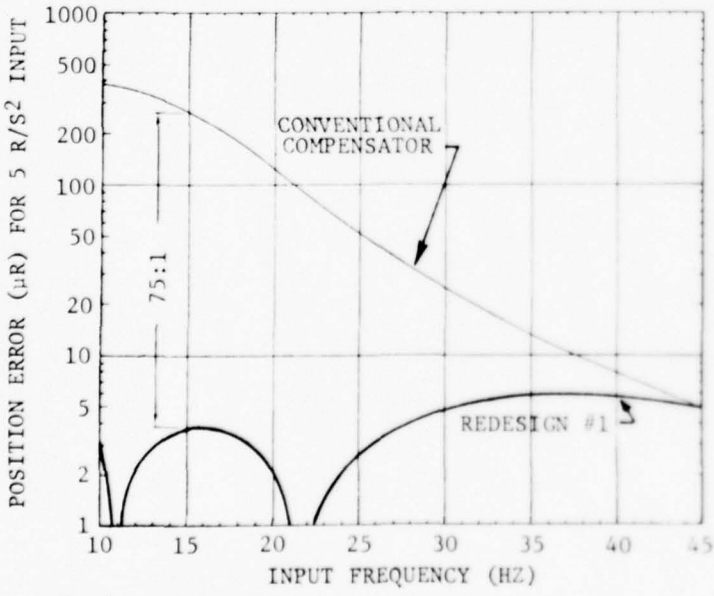
The design was built and tested. The redesign did not behave any better than its predecessor. The TASM noise drove the operational amplifiers in the downstream DAC stages into immediate saturation. We were soon convinced that the lead/lag networks and the "differentiator" would have to be eliminated. We finally recognized that the noise spectrum output by the plant demodulation network would have to be analyzed on a logarithmic amplitude scale, and the results used to limit the gains designed into DAC.

SUMMARY OF CHANGES: REDESIGN #1

CHANGE	REASON FOR CHANGE
• MOVE "DIFFERENTIATOR" POLE FROM 1000 R/S TO 20000 R/S • CONVERT BLOCK IV TO LEAD/LAG NETWORK #1 • ADD LEAD/LAG NETWORK #2 (BLOCK IV') • REDUCE GAIN BLOCK GAIN FROM 156 TO 105	• OFFSET DESTABILIZING PHASE LAG CAUSED BY HIGH FREQUENCY PLANT POLES ($\omega \geq 1000$ R/S) NEGLECTED IN UAH DESIGN • MAXIMIZE STABILITY MARGIN (CENTER NYQUIST ENCIRCLEMENT OF -1 POINT)



Nyquist Diagram - Redesign #1



Predicted Position Error For Redesign #1

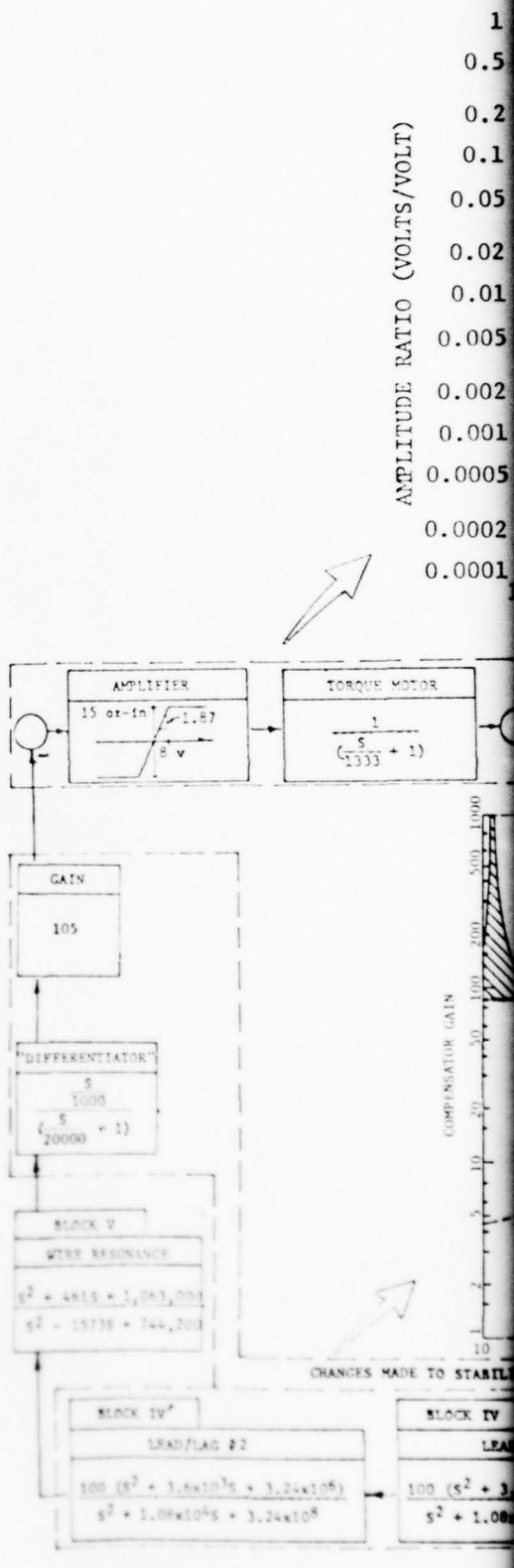


Figure 6.4. Redesign #1.

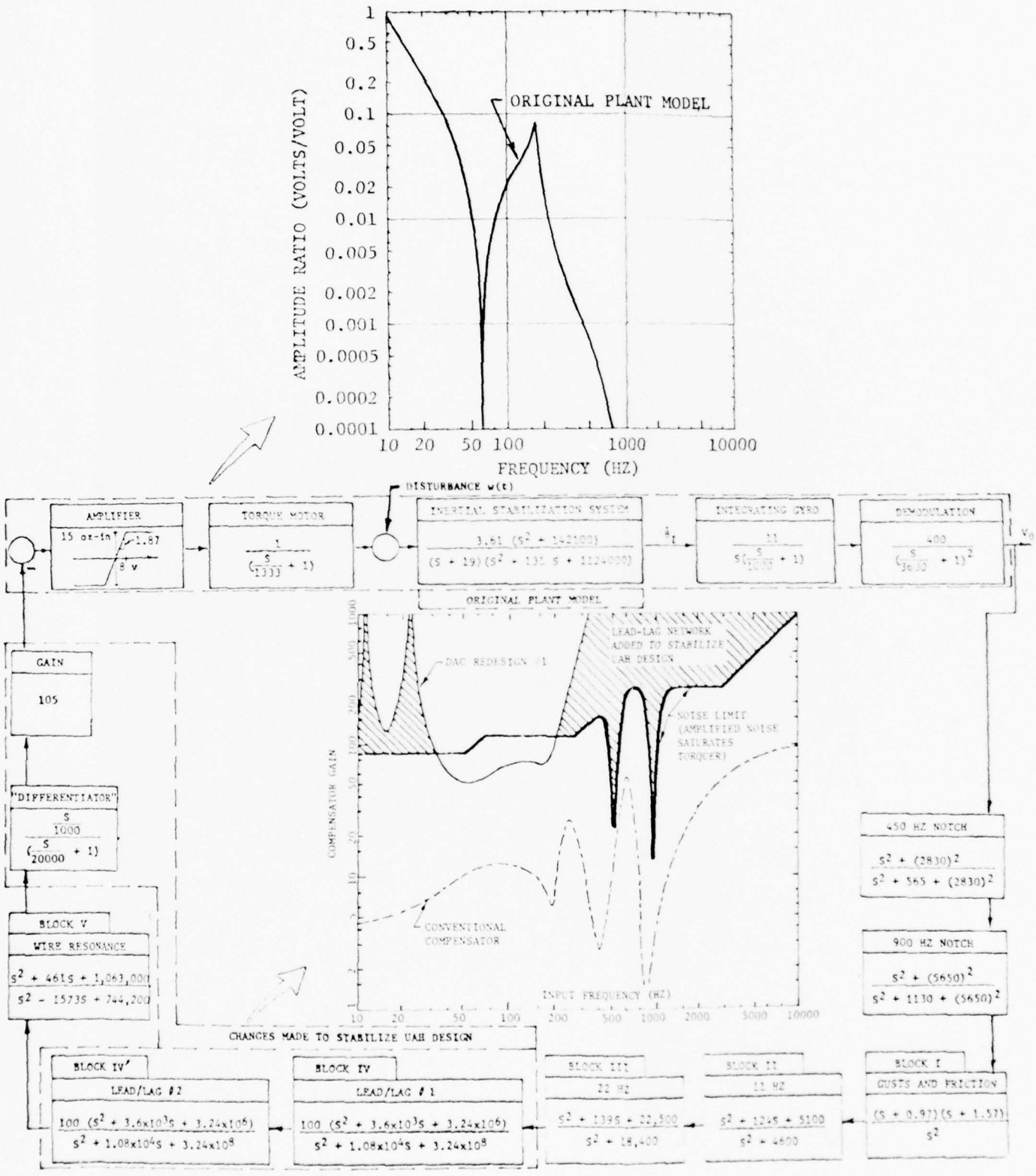


Figure 6.4. Redesign #1.

5. Redesign #2 (High Gain)

The design tradeoffs that were going on while Redesign #1 was being built and tested showed that the key to reducing DAC gain was to eliminate the Block V RHP poles. Since we now had a test verified model of the plant, we could proceed with confidence in analyzing candidate design concepts (refer to foldout page for the math model changes made because of component testing). The function of Block V was to suppress the lightly damped plant resonance at 168 Hz. It was found that making the Block V pole into an undamped oscillator tuned to the plant 73 Hz zero would perform this same function. This change eliminated the requirement for the Nyquist diagram to encircle the -1 point and shifted the critical frequencies from 100-2000 Hz downward to 20-50 Hz. The system no longer required high gain lead/lag elements to achieve stability. The design changes are listed at the upper left of the foldout.

When Block V was revised to a 73 Hz oscillator, a potentiometer controlled feedback loop was included to allow damping to be added. Damping in the Block II and III poles also could be added by changing potentiometer settings. Stability requirements made it necessary to add damping to Block III. Blocks II and V were left undamped (within design limits). The compensator design equations and a plot of compensator gain are shown at the lower right of the foldout. Our noise analysis produced the compensator gain limit shown in this same plot. The 11 and 73 Hz poles were allowed to violate this gain limit, since we still had reservations about its accuracy. Our approach was to start with undamped poles and dial in whatever damping was required to prevent torquer saturation during test.

The "differentiator" was eliminated by pole/zero tradeoffs involving several DAC modules. The block diagram algebra is shown in Figure 6.5a.

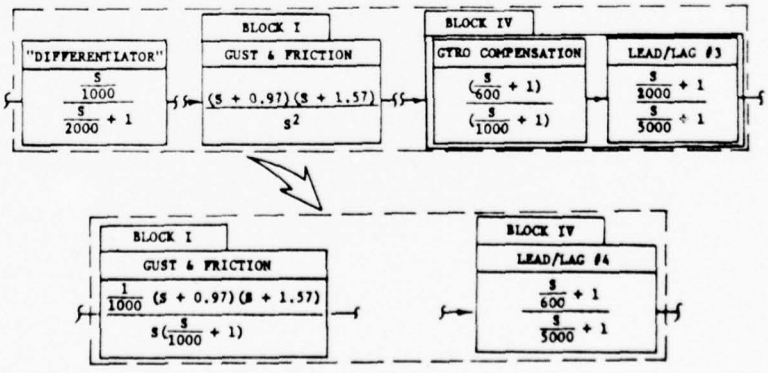


Figure 6.5a. Elimination of the approximate differentiator.

5. (Continued)

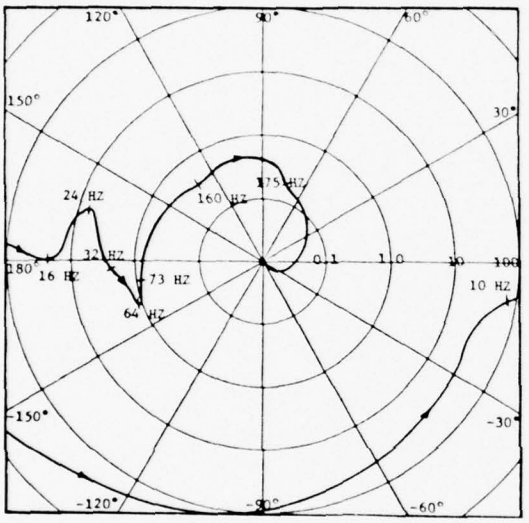
Since the system was no longer sensitive to phase lag above 1000 rad/sec, the "differentiator" pole was moved from 20000 to 2000 rad/sec. This cancelled a zero that appeared in the new Block IV redesign. The s term in the numerator of the "differentiator" cancelled the free s in the Block I denominator. The block was balanced by picking up the 1000 rad/sec pole from Block IV.

The resulting system showed small stability margins near 32 Hz. This did not create concern, however, since we had confidence in the accuracy of our model by now. We could also improve stability if we had to by adding damping to the 11 and 22 Hz poles. The system still retained good error performance. Improvements of 60:1 were still possible if we could avoid any more reductions in gain.

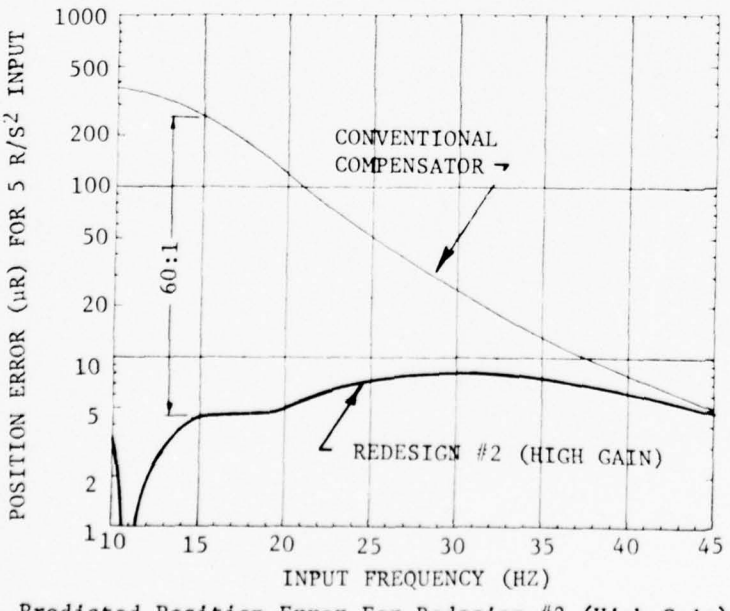
Redesign #2 produced the first encouraging test results. The output of the DAC was predominantly the sum of two narrow band random signals centered about 11 and 73 Hz. These quasi-periodic signals would drive the torquer in and out of saturation up to 73 times each second. During each part cycle the torquer was unsaturated, it could carry out some of the control commands to maintain mirror position. The system would operate from 5-20 seconds before amplified noise would totally saturate the torquer and cause loss of control. Optimizing the performance now reduced to varying the gain block setting and changing the damping in the 11 and 73 Hz poles (minimum damping of 20% in Block III was dictated by stability requirements).

SUMMARY OF CHANGES: REDESIGN #2 (HIGH GAIN)

CHANGE	REASON FOR CHANGE
• ELIMINATE DIFFERENTIATOR VIA POLE/ZERO TRADEOFFS WITH BLOCKS I AND IV	• ELIMINATE A MAJOR SOURCE OF NOISE AMPLIFICATION
• REPLACE BLOCK V RHP POLES WITH 73 HZ UNDAMPED OSCILLATOR	• ELIMINATE REQUIREMENT FOR HIGH GAIN LEAD/LAG NETWORKS (ELIMINATE NEED FOR NYQUIST DIAGRAM TO ENCIRCLE -1 POINT)
• REPLACE BLOCK IV' WITH LOW GAIN DAMPED SECOND ORDER POLE/ZERO	
• ADD DAMPING TO BLOCK III 22 HZ POLE	• OBTAIN STABLE SYSTEM WITH MINIMUM LOSS OF PERFORMANCE
• REPLACE BLOCK IV WITH PAIR OF FIRST ORDER LEAD/LAG NETWORKS	• COMPENSATE FOR TEST RESULTS SHOWING GYRO ROLL-OFF STARTING AT 600 R/S RATHER THAN 1000 R/S
• ADD LOW PASS FILTER	• SUPPRESS HIGH FREQUENCE NOISE
• CHANGE GAIN BLOCK GAIN TO 33.6	• COMPENSATE FOR GAIN CHANGES MADE TO OTHER BLOCKS TO MAINTAIN CONSTANT LOOP GAIN



Nyquist Diagram For Redesign #2 (High Gain)



Predicted Position Error For Redesign #2 (High Gain)

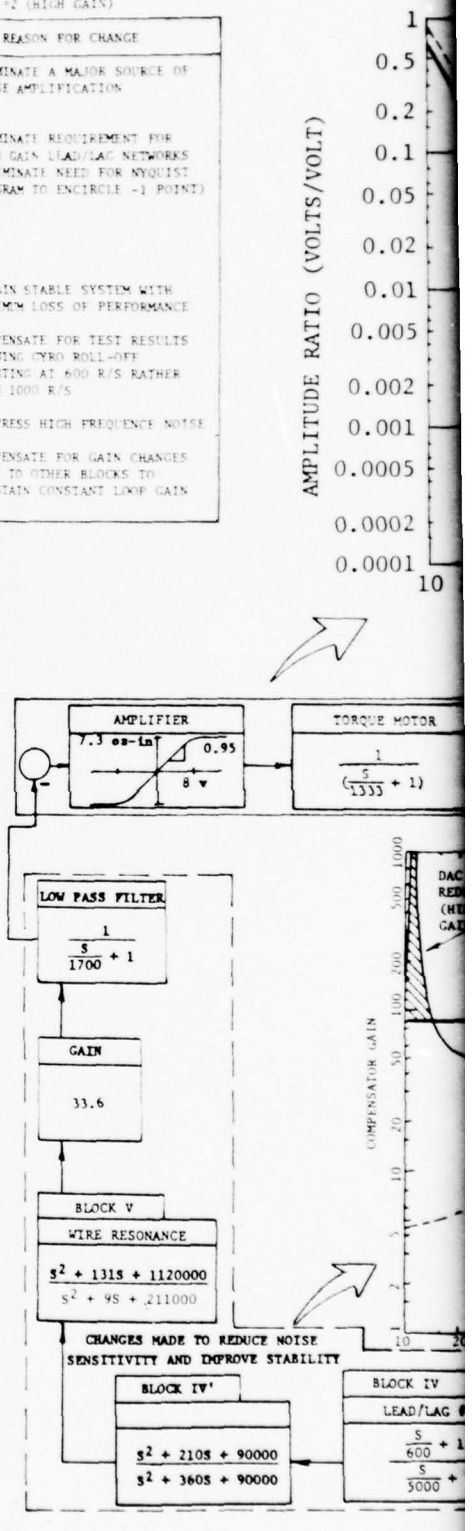
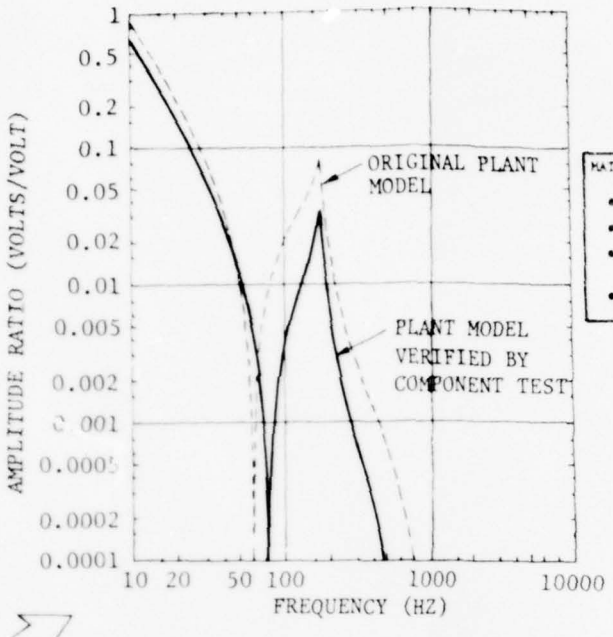


Figure 6.5. Redesign #2 (High Gain).

NGES: REDESIGN #2 (HIGH GAIN)

	REASON FOR CHANGE
ATOR FFS	• ELIMINATE A MAJOR SOURCE OF NOISE AMPLIFICATION
POLES	• ELIMINATE REQUIREMENT FOR HIGH GAIN LEAD/LAG NETWORKS (ELIMINATE NEED FOR NYQUIST DIAGRAM TO ENCIRCLE -1 POINT)
TH ND III	• OBTAIN STABLE SYSTEM WITH MINIMUM LOSS OF PERFORMANCE
TH LEAD/	• COMPENSATE FOR TEST RESULTS SHOWING GYRO ROLL-OFF STARTING AT 600 R/S RATHER THAN 1000 R/S
	• SUPPRESS HIGH FREQUENCE NOISE
AIN	• COMPENSATE FOR GAIN CHANGES MADE TO OTHER BLOCKS TO MAINTAIN CONSTANT LOOP GAIN



MATH MODEL CHANGES RESULTING FROM COMPONENT TESTING

- 60 HZ PLANT ZERO ACTUALLY 73 HZ
- TORQUER AMPLIFIER GAIN OF 1.87 ACTUALLY 0.95
- TORQUER SATURATION OF 15 OZ-IN ACTUALLY 7.3 OZ-IN
- GYRO ROLL-OFF FREQUENCY OF 1000 RAD/SEC ACTUALLY 600 RAD/SEC

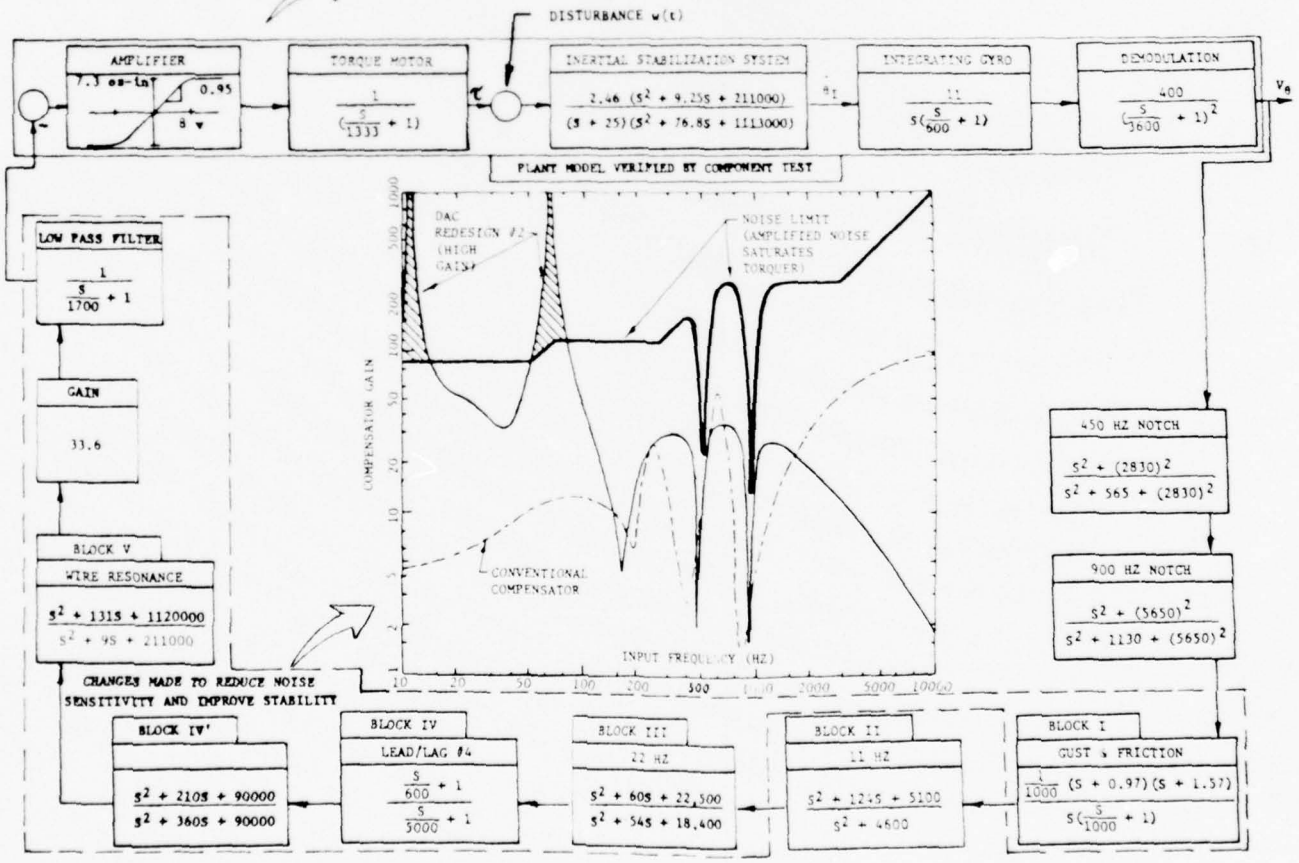


Figure 6.5. Redesign #2 (High Gain).

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6. Redesign #2 (Low Gain)

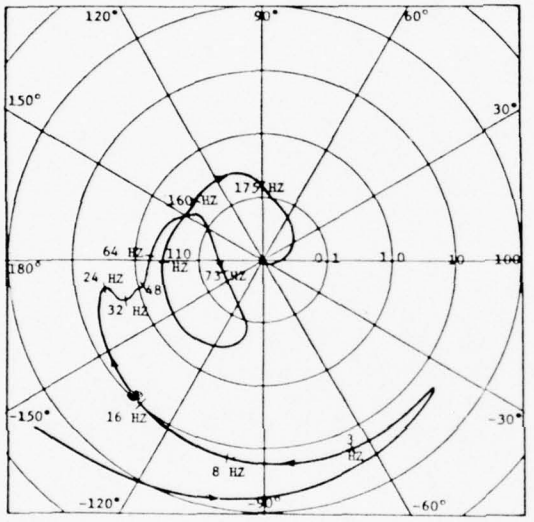
The three variables, gain block setting, 11 Hz pole damping, and 73 Hz pole damping, could not be manipulated independently to optimize performance. For example, reducing loop gain made the system unstable at 28 Hz. However, stability could be recovered by adding damping to the 11 Hz pole (the reason for this can be seen in the Nyquist plot of Figure 6.5, the previous foldout page). The best overall performance was obtained with the gain block reduced from 33.6 to 20, and with 54% and 15% critical damping in the 11 and 73 Hz poles, respectively. The compensator gain plot at the lower right shows how the "optimized" gain stacks up against the noise limit. The 73 Hz pole had to be reduced to the gain limit to eliminate torquer saturation. The 11 Hz pole was set well below this limit. However, this reduction was dictated by stability, not noise amplification. Overall, we gained a healthy respect for noise limit plots, and strongly recommend their use as design tools on applications of DAC theory to other systems.

The reduction in gain dictated by the noise and stability constraints caused a significant loss in performance. As shown on the lower left of the foldout, the position error reduction actually achieved was 10:1 or less over the critical 10-25 Hz frequency range. The desired notch at 11 Hz was eliminated in order to maintain stability.

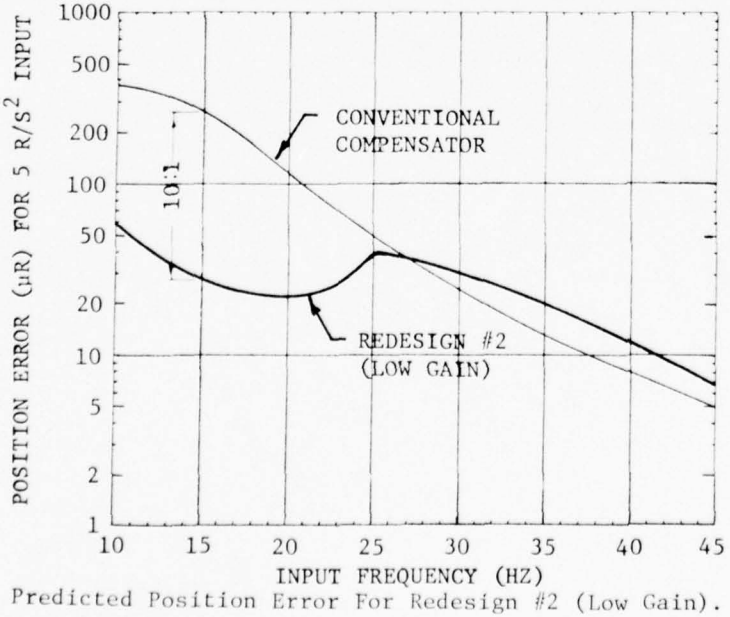
The design trade studies and the test results both showed that performance improvements exceeding 50:1 could be achieved in a low noise system. This level of performance was attainable using a lightly damped Redesign #2 (High Gain) if the TASM noise spectrum from 10-100 Hz could have been reduced from 0.1 volt peaks to 0.01 volt peaks. Keeping the noise threshold below this level is no longer difficult using current solid state elements. Noise in our DAC hardware was maintained well below this value.

SUMMARY OF CHANGES: REDESIGN #2 (LOW GAIN)

CHANGE	REASON FOR CHANGE
• REDUCE GAIN BLOCK GAIN FROM 33.6 TO 20 • ADD DAMPING TO BLOCK I 11 HZ POLE* • ADD DAMPING TO BLOCK V 73 HZ POLE	REDUCE LOW FREQUENCY GAIN BELOW NOISE-IMPOSED GAIN LIMIT
*ADDITIONAL DAMPING WAS REQUIRED TO PHASE STABILIZE SYSTEM	



Nyquist Diagram For Redesign #2 (Low Gain).



Predicted Position Error For Redesign #2 (Low Gain).

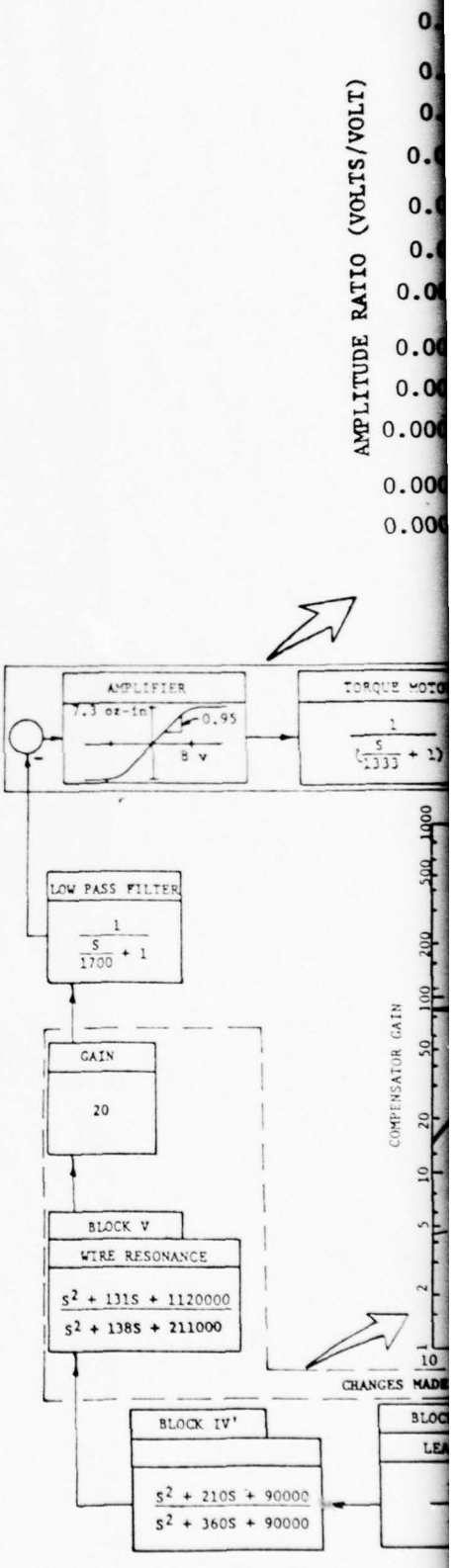
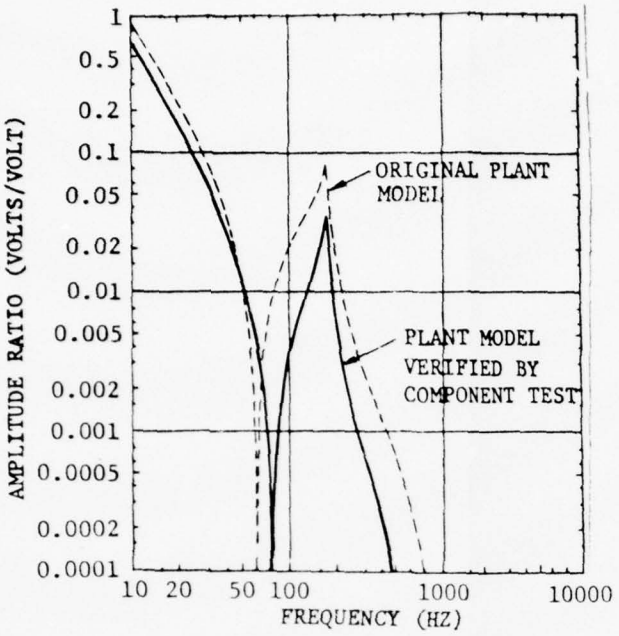
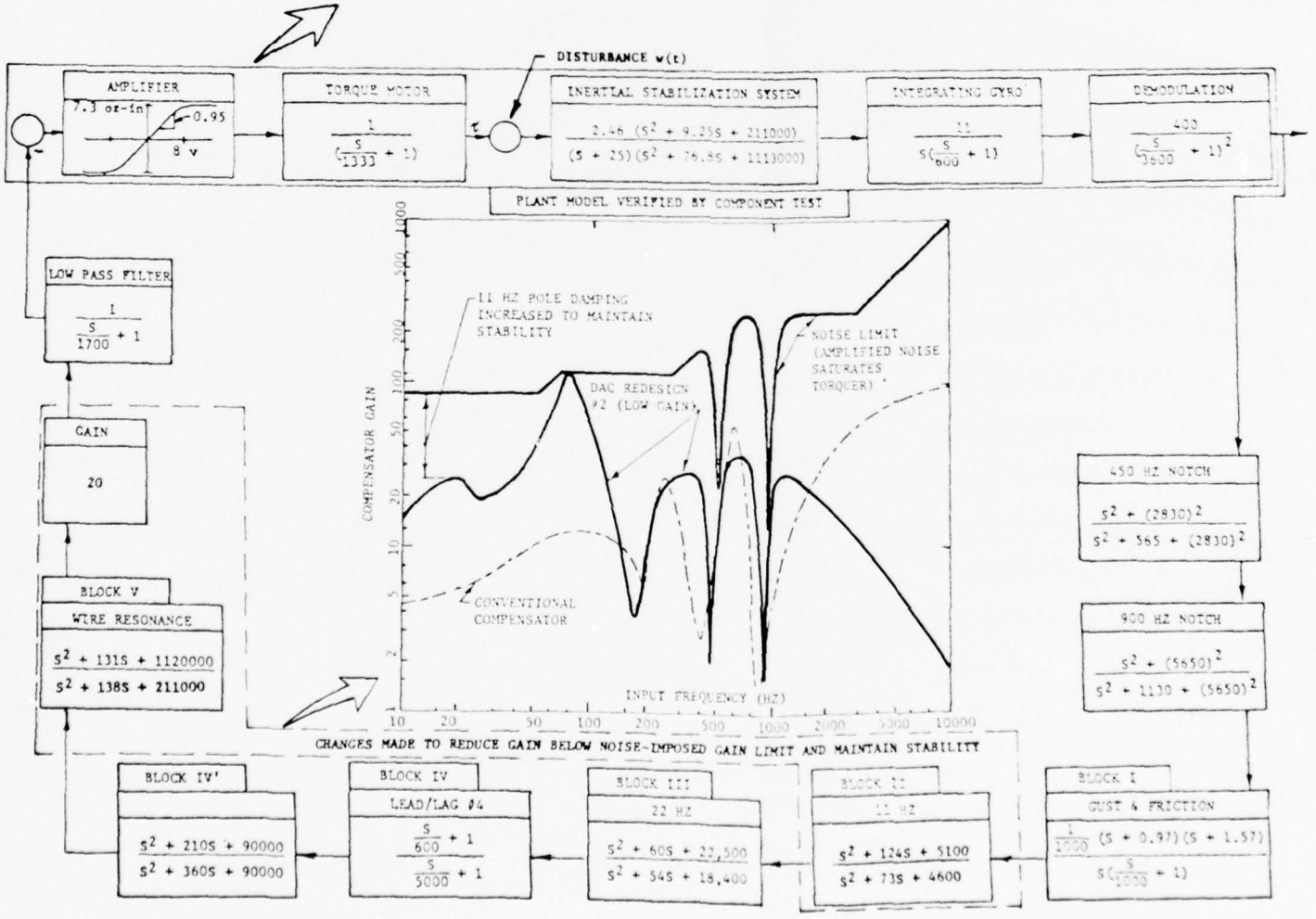


Figure 6.6. Redesign #2 (Low Gain).





lesign #2 (Low Gain).

SECTION 7

DESIGN GUIDELINES

SECTION 7, DESIGN GUIDELINES

The development and test of DAC-designed hardware has provided a valuable learning process for future application of the theory. It has demonstrated that the DAC design process can produce high performance designs that may never be uncovered by conventional techniques. It has also shown that once the DAC design is established, it requires more, rather than less, evaluation and refinement via conventional Nyquist, root locus, and Bode techniques. Table 7-I presents practical guidelines to anticipate and avoid the design pitfalls through application of conventional analyses and test techniques.

TABLE 7-I. DAC DESIGN GUIDELINES

GUIDELINE

1. *Know your system before selecting the compensator design approach:*
   - o Plant closed loop frequency response from a decade below through a decade above controller pole locations
   - o System noise spectrum over range of significant plant and compensator frequency response
   - o Limiting characteristics of all non-linear or "weak link" elements
   - o Conservative tolerances (uncertainty bounds) on the system and math model parameters.

DISCUSSION

DAC design techniques are not applicable to every system. DAC performance is heavily dependent on (1) good math models of system, (2) amplitude and frequency characteristics of system noise, and (3) limiting "weak link" characteristics such as saturating amplifiers. Before committing to this approach, the designer must understand how the plant dynamics, noise and non-linearities of his system limit his pole placement options and place bounds on the performance he can realize from the design. Techniques for making this evaluation are developed in the next section (Section 8.0).

TABLE 7-I. DAC DESIGN GUIDELINES (Continued)

GUIDELINE

2. *Develop an accurate math model, verify it with test data, and use it to guide the design process:*

   - o Start with a good analysis of the plant and the candidate compensator designs
   - o Test each plant and compensator component as soon as the hardware becomes available
   - o Revise the math model to agree with test results
   - o Use the test-verified math model to:
     - a) Perform design/performance tradeoffs
     - b) Assess the impact of variations in system or math model parameters
   - o Verify the entire system with end-to-end tests

DISCUSSION

Like all modern pole placement techniques, the DAC design can be no better than the math models used to construct the linear filters (the composite state constructor). Application of DAC design techniques requires a good math model, proven by a thorough test verification program as actual hardware becomes available. This is the price that must be paid if the high performance payoffs offered by the technique are to be achieved with confidence.

In developing the plant model, the designer should be careful about neglecting "high frequency" poles and/or zeros. For example, a pair of first order poles at five times a critical system frequency f_c will produce over 20 degrees of phase lag at f_c. This much phase shift, neglected in the math model, can significantly alter the stability and performance of the real hardware. Liberal use of Nyquist diagrams and other conventional analysis techniques are required to pinpoint the critical frequency regions where math model fidelity must be carefully preserved.

To facilitate test verification, the physical components represented in the math model should be easily tested blocks of hardware. The verification test program should measure the input-output characteristics of these same, exact components. A direct apples-to-apples comparison then can be made between analysis and test results. This greatly simplifies "troubleshooting" when the two do not agree.

Whenever analysis and test results disagree, it is dangerous to assume that the math model is at fault and arbitrarily revise it to match test data. Several times in our program, the disagreement was traced to a subtle problem in the test setup or data system that had not been uncovered by the checkout tests. Enough detective work to pinpoint the actual cause(s) of the disagreement provides a powerful check and balance on both the analysis and the test.

TABLE 7-I. DAC DESIGN GUIDELINES (Continued)

GUIDELINE

3. *Develop a design noise spectrum early in the design process, refine it with test data, and use it to establish realistic bounds on the design*

   - o Develop the initial noise estimates for each anticipated major noise source using experience and test data from similar hardware
   - o Use the closed loop model to compute the noise spectrum at the compensator input.
   - o Refine the noise spectrum with test data as actual hardware components become available
   - o Obtain the final "Design Verification" noise spectrum by enveloping numerous measurements on several "identical" components.
   - o Always use a logarithmic rather than a linear amplitude scale to improve the estimate of the true noise floor.

DISCUSSION

Since noise is a major constraint on a DAC design, a system noise spectrum should be estimated early in the design process (ways of doing this are developed in Section 8.0). This spectrum should be improved as better test and analysis data become available. In its earliest, most primitive form, it can be used to establish reasonable upper bounds on compensator gain. As it becomes more refined, it can dictate adjustments in where compensator poles are placed, and establish filter requirements.

The earliest noise estimates will have to be based on test results and experience with hardware components similar to those that will appear in the new system being designed. In time, as actual components are selected or developed, their noise characteristics can be measured. The noise characteristics should be measured several times on each component, and on several different "identical" components. We tested six different gyros of the same make, model, and manufacturer's lot and found differences in the noise spectrum of several hundred percent. This was not unexpected, but the differences were large enough to make substantial changes in overall system performance.

The noise analysis should always be plotted on a logarithmic rather than a linear amplitude scale so that the noise "floor" and smaller spikes are not hidden by the dominant noise peaks. The repeated noise measurements should be superimposed and conservatively enveloped to obtain the design noise spectrum.

TABLE 7-I. DAC DESIGN GUIDELINES (Continued)

GUIDELINE

4. *Use conventional design/analysis techniques to support DAC/modern control design methods:*

   - o Don't rely on pole placement to assure adequate stability and performance
   - o Use Nyquist and/or root locus analyses to determine sensitivity to parameter changes and to optimize the DAC design
   - o Use Bode diagrams to aid in pole placement, evaluation of hardware realizability and identification of what noise frequencies are most critical to the design
   - o Use simulation to assure good performance in the face of parameter variations, noise and nonlinear effects

DISCUSSION

Modern control design techniques work best when supported with proven conventional analysis techniques. Advanced techniques like DAC can identify high performance designs. Conventional techniques then provide powerful tools for refining and verifying the design.

It is particularly important not to rely on pole placement techniques to assure stability. Anyone who has performed root locus analyses can appreciate how sensitive some roots are to changes in system parameters. Roots "deep" in the LHP may migrate rapidly into the RHP with only small changes in a critical parameter. Simplifying assumptions inherent in any math model may result in the real hardware having poles well away from where they were placed - including some in the right half plane. Conventional techniques should be used liberally to assure that the system is stable and meets performance requirements under all reasonable parameter variations. Once DAC theory has produced a good baseline design, conventional techniques also can be used to optimize the design more readily than continued pole placement iterations.

TABLE 7-I. DAC DESIGN GUIDELINES (Continued)

GUIDELINE

5. *Use ingenuity rather than brute force in pole placement:*

- o Don't try to push all composite constructor poles beyond the plant poles (unless the plant poles span less than two decades in frequency).
- o When placing composite constructor poles within the plant bandwidth, locate near plant zeros and at least 10-20% away from the nearest plant pole.
- o Try to cluster controller poles and zeros in groups of similar frequency with at least a 4:1 frequency gap between each group.

DISCUSSION

The closed loop plant poles are assigned to satisfy the design criteria (rise time, peak overshoot, settling time,...). Ideally, the composite constructor poles should be placed at 5-10 times the frequency of the disturbance and plant events they are trying to reconstruct. This will assure that the estimation errors tend to zero rapidly.

Unfortunately, it takes large gains to move poles to a much higher frequency. As a crude yardstick, the maximum gain required is roughly proportional to $(\omega_2/\omega_1)^n$, where ω_1 is the original pole frequency, ω_2 is the desired pole placement, and n is the order of the controller. For example, if the designer has a 12th order system, and wants to move his poles a frequency decade deeper into the left half plane, he should expect the DAC design process to give him a 10^{12} gain requirement. He can get around this impass by resorting to his ingenuity. Rather than pushing all constructor poles beyond the plant pole frequencies, he can tuck them in around plant zeros and away from plant poles (constructor poles placed too near closed loop plant poles can force the latter away from their intended position). By settling for a smaller shift in pole frequencies, the designer may be able to reduce his gain requirement to a realizable value and still achieve acceptable performance.

Clustering the constructor poles and zeros in groups with a frequency separation between each group can also be used to reduce gain requirements. This has the effect of decoupling a higher order system into a series of lower order blocks that are much easier to realize in actual hardware. If the same 12th order system can be "clustered" into three semi-uncoupled blocks of 4th order, gains of less than 10^3 may still be enough to achieve a 5:1 shift in pole frequency.

TABLE 7-I. DAC DESIGN GUIDELINE (Continued)

GUIDELINE

6. *Don't design for the last ounce of performance:*

- o Limit gains to reasonable levels so the design can be realized in hardware without heroic measures
- o Design a stable system that is tolerant of changes in system parameters

DISCUSSION

Obtaining the last few percent improvement in performance may disproportionately increase program cost and development time, and produce a design that cannot accommodate future modifications. When we "tuned" our system to peak performance, we found it to be very intolerant of changes. Even replacement of the gyro with an "identical" unit would sometimes cause unacceptable loss of performance due to changes in the noise spectrum and small shifts in critical frequencies. When the design is pushed to the ultimate, rigorous configuration control and maintenance procedures will have to be applied to the hardware. It is well worth the investment to conduct tradeoffs between performance, P, design sensitivity, S, and cost, C. Limit the design to the range where $\partial P/\partial S$ and $\partial P/\partial C$ still show good positive slopes. The end product may look a little more "conventional," but it can be realized in hardware with confidence, and within realistic cost and schedule constraints.

GUIDELINE

7. *Design hardware that is easy to modify by:*

- o Making each pole/zero module an isolated hardware block
- o Placing resistors and capacitors on easily changed headers
- o Leaving room on the circuit cards for growth.

DISCUSSION

Plant design changes that occur during hardware development will have more effect on a high performance controller than on one of conventional design. As actual system hardware is built and tested, the math model used to design the compensator will also undoubtedly have to be changed to match test results. This can have a real impact on the design. Often being able to shift a compensator pole frequency by 10-20%, or adjust its damping can recover the performance that would otherwise be given up. The ability to accommodate these types of changes should be engineered into the compensator design at the expense of using a few extra "op amps." This goes against normal design training which teaches us that our skill as designers is measured by how few components we need.

TABLE 7-I. DAC DESIGN GUIDELINES (Concluded)

GUIDELINE

8. *Use first order linear operational amplifier models for initial design, evaluate with higher order analysis, and verify with end-to-end test:*

   - o Designs based on normal first order approximation operational amplifier design models (infinite gain, infinite input impedance) break down above 2000 Hz
   - o Neglected second order effects can introduce high frequency (>2000 Hz) resonances that severely impact performance
   - o Adding low pass (~2000 Hz) filters to each block can eliminate these undesirable high frequency effects

DISCUSSION

Using components (resistors and capacitors) screened to ±1% accuracy, first order approximation design models were good enough to predict the actual performance of our hardware to 2000 Hz. These models idealize the operational amplifiers as having infinite gain and infinite input impedance. Above 2000 Hz, the neglected second order effects started to alter performance. Second and even third order design models were required to predict desired frequency response characteristics above 2000 Hz. These models were particularly necessary to predict impedance loading between supposedly isolated stages. Separate blocks or stages may reproduce the design equations beautifully when tested by themselves. When coupled together, however, these supposedly isolated blocks may develop high frequency (>2000 Hz) resonances strong enough to saturate the downstream operational amplifiers. If the system characteristics permit it, the ideal solution is to add low pass filters that attenuate the response of any blocks that do not roll off by 2000 Hz.

In the next section, explicit design procedures are developed for applying the above guidelines.

SECTION 8

RECOMMENDED DESIGN PROCEDURES

SECTION 8, RECOMMENDED DESIGN PROCEDURES

What systems are suitable candidates for DAC design? A crude yardstick for making this evaluation will now be developed along with procedures for applying the guidelines from the previous section. The numbered paragraphs that follow explain the corresponding blocks in the flow chart of Figure 8.

1. Preliminary Design Evaluation

Not all systems can benefit from DAC design. Ideal candidates are plants that have a narrow closed loop bandwidth, low background noise, and ample control authority. Before committing to the DAC approach, the designer should perform tradeoffs to answer the following questions about his system:

a. Will the closed loop plant poles span more than two decades of frequency?

b. Will compensator amplification of background noise exceed 10% of available control authority?

c. Will compensator amplification of background noise produce unacceptable performance errors?

To answer these questions, the designer must have at least preliminary estimates of his closed loop plant pole placements, the "weak links" in his control system and plant, the noise spectrum of the compensator input signal and/or compensator gain characteristics. How to obtain these data will be discussed shortly. First, let's examine the three questions individually, starting with a. Increasing the plant bandwidth drives both compensator bandwidth and gain levels up. This means that lower noise levels must be maintained over this increased frequency range in order to avoid the problems b. and c. above. System stability and performance become much more sensitive to small changes in physical parameters. In short, the design tends to lose its flexibility, and becomes more intolerant of change.

The last two questions sound the same, but they are not. On our TASM system, we had to reduce compensator gain by more than an order of magnitude to keep amplified noise from saturating the torquer, which was the "weak link" in the TASM. Given a torquer with at least 10 times more muscle, we could have operated at full compensator gain. The mirror position errors produced by the amplified noise still would have been less than 10 μR - well within our performance requirements. Consequently, it is very critical to define the "weak links" downstream of the compensator when using high gain designs. Typical "weak links" include:

- Saturating amplifiers
- Diode overload protection circuits
- Peak torquer output
- Maximum actuator rate and stroke
- Structural limits

1. (Continued)

After the designer has converted system requirements into preliminary designs of the plant, established control force requirements, and made a few cuts at a compensator design, he should have an estimate of the closed loop plant dynamics and the "weak links" in his control system. This still leaves the noise spectrum and the compensator gain characteristics to be determined before Questions a., b., and c. can be answered. There are two ways of proceeding: (1) Front-to-Back, and (2) Back-to-Front. The Front-to-Back approach is applicable to new systems in which the plant itself is under design. It proceeds as follows:

1) Estimate the noise spectrum using experience and test data from similar hardware. This estimate may be as crude as a flat "white noise" value. Discrete "spikes" can be superimposed for known physical sources such as gyro spin frequencies, 60 Hz hum, and lightly damped closed loop system resonances.

2) Compute the compensator output versus frequency required to use 100% of the available control authority in responding to noise alone. This requires an estimate of the "weak links" in the subsystem that will implement the control command (torquer and electronics, actuator and power supply, support structure).

3) Compute a "design limit" compensator gain versus frequency. This is the gain required to amplify the noise from Step (1) to 10% of the output levels from Step (2).

4) Evaluate whether the DAC compensator can meet design requirements without exceeding this target "design limit" gain. The designer can use the following guidelines to help establish gain requirements:

   - o Poles of the composite state constructor should lie 3-10 times deeper into the LHP than the poles of the plant and disturbance states being reconstructed (see Guideline #5, Section 7).
   - o The plant state constructor poles should be real, or nearly critically damped (Reference 6).
   - o Assume a Q = 50 notch filter to compensate for each discrete "sinusoid" included in the disturbance model.

   The 10% rule of Step #3 has been chosen somewhat arbitrarily. It may be violated successfully in some designs provided proper precautions are exercised. These precautions are developed at the end of the Back-to-Front approach which follows.

The Back-to-Front approach is the logical choice if plant hardware has already been built. It starts with a preliminary compensator

1. (Continued)

design based on a knowledge of both the plant and disturbance characteristics. Using an estimate of the "weak links" in the system, plus the closed loop system response characteristics, compute the compensator input versus frequency required to use all of the available control authority, or produce unacceptable performance (whichever occurs first). Then take 10% of this spectrum as the target maximum noise level. If this noise level falls well within state-of-the-art hardware performance, the designer can proceed with confidence. If not, he can still proceed under the precautions outlined next.

After making the calculations required to answer Questions a through c, what if one or more answers are yes? The designer may still elect to use a DAC design if the added precision is worth the extra effort he must expend to:

- o Develop an accurate math model proven via a rigorous test verification program.
- o Perform extensive design tradeoffs to evaluate the sensitivity of system stability and performance to parameter changes.
- o Impose tight specifications on the hardware noise and performance characteristics.
- o Require careful maintenance and configuration control of the operational system to prevent an accumulation of small changes from eroding performance.

2. Develop Accurate Math Model and Verify via Test

The DAC Theory has matured to where it can be applied to operational precision systems. Since models of the plant and disturbance are the principal DAC design tools, such applications must be supported by a sound program of math model development and test verification. These programs must be implemented in any precision control application - regardless of the design approach - to assure that the actual system will perform as predicted.

A successful analytical design program depends on alert technical management as much as on good engineering. It is the manager who must layout and control the step-by-step program plan which will assure that his engineering team arrives at the right answers. A successful plan should include the following elements:

1) Continuing systems analyses to pinpoint features of the plant, disturbance, and compensation that drive performance; use of this information to guide the entire program

2) Development of a noise model to establish realistic limits on compensator gain

2. (Continued)

   3) Use of analysis and test as a check and balance to drive out errors that occur in either technique if used alone.

   4) Regular technical reviews between the plant and compensator design/analysis teams to assure that configuration changes do not slip by unnoticed.

   5) Use of sensitivity analyses to determine how much stability and performance are affected by the "tolerances" on the math model parameters. These "tolerances" are conservative estimates of how much each math model parameter value could be in error because of modeling uncertainties. This approach minimizes the chance of unpleasant surprises when hardware is finally available to test and verify the math model.

   6) Final verification of the math model and the system design by testing each plant and compensator component as soon as hardware is available (repeated measurements of the noise spectrum of each component should be a part of this test verification program).

Whenever analysis and test results disagree significantly, the manager should have the analysis and test teams each make a list of possible error sources that could cause the disagreement. He then assigns actions to each team (specific analyses and tests) to systematically evaluate each candidate error source until the physical causes of the disagreement are identified. These can then be eliminated by rational changes in the math model and/or test setup. This test verification process is greatly simplified if the math model elements represent blocks of hardware whose input/output characteristics can be readily tested.

At each step of the program, the compensator designers and systems analysts should be operating with the best plant, disturbance, noise, and tolerance models available. The manager must make sure that these models are based on the latest configuration and test data. Whenever a model is simplified to facilitate the design computations, it is up to the manager to see that system level analyses are performed to verify that the neglected terms do not affect overall stability and performance.

3. a. Design and Evaluate Closed Loop Plant/b. Design and Evaluate Composite Constructor

In theory, the closed loop plant design can be carried out independent of the design of the composite constructor. To do this, designer assumes that the composite constructor can provide him with an accurate estimate of the true (undisturbed) state vector $\hat{x}(t)$. Using

3. (Continued)

a linear control law proportional to the state vector, he then selects feedback gain constants which place the closed loop poles in the desired locations (assuming the system is completely controllable). In practice, there should be cross talk between the two designs, since the poles of the composite constructor should not be placed close to the poles of the closed loop plant. Otherwise, when the loop is closed on the total system, any poles that are close together can interact and move away from their intended location (see Reference 6). This can destroy system stability and performance.

As a result of the Preliminary Design Evaluation, the designer should know where some of his composite state constructor poles will have to be placed. For example, each sinusoid in his disturbance model will require a high Q filter. He has no flexibility to select the center frequency of this filter - it must be equal to the corresponding disturbance frequency. However, he does have flexibility in where he places at least some of the closed loop plant poles. On the other hand, there may be some closed loop plant pole (or zero) locations that are dictated by closed loop stability or performance requirements, or by the hardware itself. These in turn impose a constraint on where the composite constructor poles can be located. These "fixed" locations should be defined first and plotted on a good pole-zero map, which will prove a very useful tool for making the remaining pole placements.

The design proceeds through the use of experience to locate the remaining closed loop poles or via optimal control methods. Either technique readily generates solutions with such high gains that they cannot be realized in actual hardware. Consequently, the design is an iterative process. Each design trial will produce a set of gain constants that allow the closed loop plant and composite constructor equations to be written in state variable form. The designer has to convert this information into actual hardware designs. He must then use his practical experience to answer the questions, "Can the design be realized in hardware?" and "Are the gains within the noise imposed limits?" The iterations proceed until realizable designs start to emerge. At this point we found it was easier to switch to conventional techniques to evaluate and refine the designs, rather than continue with the pole placement iterations.

4. Assess System Stability and Performance

Once viable design candidates start to emerge, conventional analysis techniques must be used to evaluate system stability and performance. The first step is to make sure that the design satisfies stability and performance requirements when the math model with "nominal" parameter values is used in the analysis. Designs that pass this gate are then screened to see how well they

4. (Continued)

hold up as the critical parameters are varied. Both stability and performance should be evaluated as the key physical parameters are varied through their full "tolerance" limits. At this point, these "tolerance" limits should include the uncertainty bounds on the math model, plus estimates of how much the plant configuration itself could change as the design matures. These tolerances should be conservative to start with, and tightened as the program goes along, and hardware is built and tested.

Root locus analysis is very effective for evaluating sensitivity of a design to changes in system parameters. It is particularly attractive for multi-loop systems where quantitative physical interpretation of the Nyquist results becomes difficult. While root locus is often thought of as a simple loop gain variation technique, modern computer solutions permit rapid evaluation of the effects of changing individual parameters at either the state variable, or transfer function level. These changes can involve either gain, or phase or both. These solutions readily display the eigenvector as well as the root locus information. The eigenvector data provide powerful insight to the physical variables that are (and are not) sensitive to changes in parameters.

The objective of these system analyses is to drive the compensator design to where it achieves good performance and stability without being hypersensitive to changes in the physical parameters. Chances are good that this objective can be met if it is adopted at the program outset, and some potential performance is sacrificed to obtain a design more tolerant of change.

What if system requirements demand a design tuned for peak performance? Chances are such a design will be very sensitive to changes in the system itself or its operational environment. System analyses can be used to define acceptable operational limits on the plant and compensator parameters. A comprehensive maintenance and configurational control program may well have to be implemented to keep the hardware within these limits.

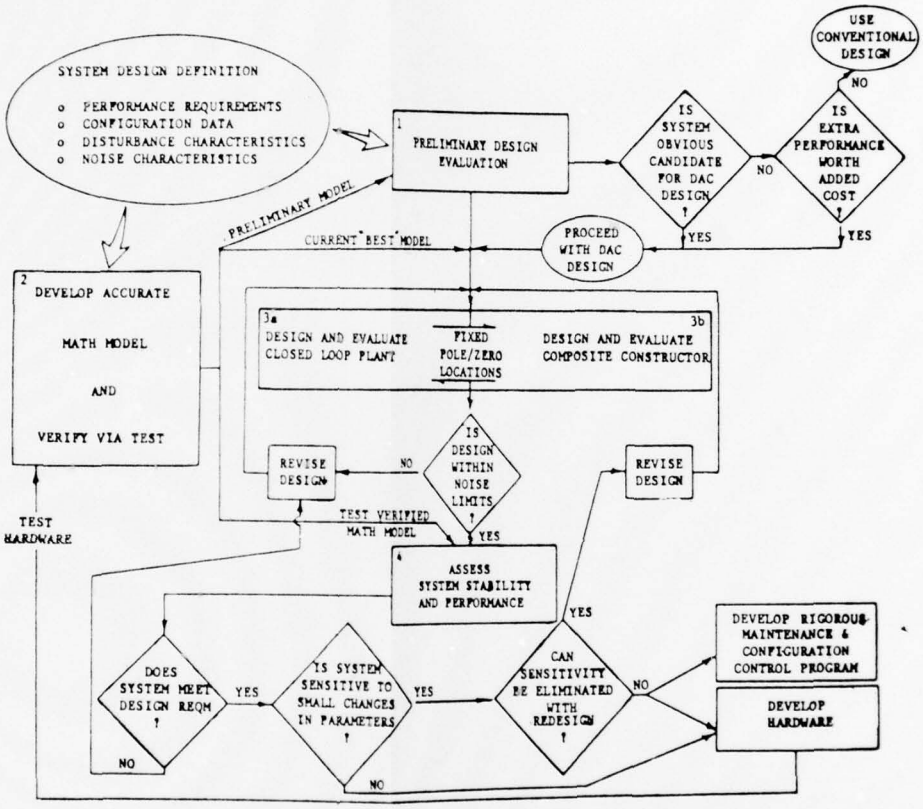


Figure 8. DAC Design Procedure.

SECTION 9, CONCLUSIONS AND RECOMMENDATIONS

CONCLUSIONS

DAC Theory has been developed and demonstrated as a viable design technique for precision pointing/tracking control systems. Significant performance payoffs can be realized through the analytical DAC design approach backed by the proven conventional design analyses and testing suggested in this report.

RECOMMENDATIONS

DAC Theory is recommended as a candidate design method for precision pointing/tracking applications. Initial use of the technique should be limited to plants meeting the criteria of Section 8.1. Subsequent applications can be made to systems that violate these criteria as actual DAC-designed hardware experience is accumulated. It is recommended that the design guidelines and procedures contained herein be revised periodically to include knowledge gained from future applications of the technique.

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