AD-A045 543 ITT GILFILLAN VAN NUYS CA F/G 17/9
UNATTENDED/MINIMALLY ATTENDED RADAR STUDY. VOLUME II. RADAR DES--ETC(U)
AUG 77 F30602-76-C-0383
UNCLASSIFIED ITTG-TP-0002/L-7018-VOL-2 RADC-TR-77-270-VOL-2 NL

1 OF 4
ADA045 543

Vol I, AD45 702

RADC-TR-77-270, Volume II (of three)
Final Technical Report
August 1977

UNATTENDED/MINIMALLY ATTENDED RADAR STUDY
Radar Designs

ITT Gilfillan

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

This report contains a large percentage of pages which are not of the highest printing quality but because of economical consideration, it was determined in the best interest of the government that they be used in this publication.

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This report has been reviewed and is approved for publication.

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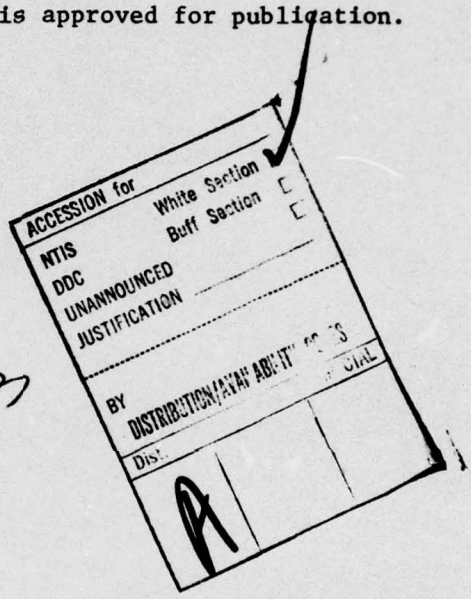

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: RADC-TR-77-270, Vol II (of three)	2. GOVT ACCESSION NO. Volume II.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle): UNATTENDED/MINIMALLY ATTENDED RADAR STUDY. Radar Designs.		5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report, 6 Aug 76 - 6 Jan 77.
		6. PERFORMING ORG. REPORT NUMBER: TP-0002/L-7018-Vol-2
7. AUTHOR(s): Land Based Air Defense Systems Group		8. CONTRACT OR GRANT NUMBER(s): F30602-76-C-0383
9. PERFORMING ORGANIZATION NAME AND ADDRESS: ITT Gilfillan, 7821 Orion Avenue, Van Nuys CA 91409		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 63101F, E2330102
11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (OCDE), Griffiss AFB NY 13441		12. REPORT DATE: August 1977
		13. NUMBER OF PAGES: 308
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same		15. SECURITY CLASS. (of this report): UNCLASSIFIED
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

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The effort reported here was sponsored by the Electronic Systems Division/XR, Hanscom Air Force Base MA 01731.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

UAR - Unattended Radar
MAR - Minimally Attended Radar
DEWLine
Life Cycle Cost
Surveillance
Reliability

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report presents results of a study of alternative radar design approaches that could be developed to optimally satisfy requirements for unattended and minimally attended radar operations. The requirements, detailed in the study statement of work, consist of two sets of nominal radar performance parameter goals; one set for the unattended radar (UAR) and a second for the minimally attended radar (MAR). Based on these requirements, alternative radar design approaches were synthesized for both UAR and MAR, and evaluated for reliability, life cycle cost (LCC) and performance. (cont'd)

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The radar designs recommended for UAR and MAR displayed the greatest potential for optimally satisfying all stated requirements. These designs are detailed in Volume II of the report. The UAR, a 60 nmi 2D radar, automatically outputs target track data that can be remoted to manned logistics nodes and/or ROCCs via narrowband communications links. It provides all altitude surveillance coverage of aircraft targets between 100 and 100,000 feet, and is configurable to be sufficiently reliable to guarantee, to a >90 percent confidence level, failure-free system operation for periods of time from three months to one year. The MAR, a 200 nmi 3D radar, also automatically outputs target track data to logistics nodes and/or ROCCs. It provides all altitude 3D coverage of aircraft targets between 100 and 100,000 feet, and is configurable to be sufficiently reliable to guarantee, to a >90 percent confidence level, failure-free system operation for periods of time from five days to 0.5 month.

Volume I provides an Executive Summary of the Unattended/Minimally Attended Radar Study. Volume II presents alternative approaches investigated and details the radar designs recommended. Volume III presents data estimating radar acquisition and Life Cycle Costs.

PREFACE

This Final Report covers a five-month study of Unattended/Minimally Attended Radars (UAR/MAR), conducted by ITT Gilfillan (ITTG) for RADC under contract No. F30602-76-C-0383. The study was performed between 6 August 1976 and 6 January 1977.

The study was directed to evaluate alternative radar designs that can potentially achieve unattended/minimally attended radar operations at low cost. Consequently, a major study objective was to identify R&D activities which should be undertaken to support development of UARs/MARs that could, in the 1980s, provide the Air Force with increased, long-term, cost effective systems.

Two types of radars are addressed: a short range 2D radar designed for long term, completely unattended operations in remote areas; and a medium range 3D radar designed for minimally attended operations. Recommendations are provided for R&D activities that potentially offer high pay-offs in reducing systems costs.

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EVALUATION

The effort reported is one of three parallel study contracts performed under Project E233 by direction of ESD/XR. These reports identify alternative concepts and activity necessary to support the development of a short-range, unattended radar and a long-range minimally attended radar. The short-range radar is being viewed for application in DEW Line to replace the AN/FPS-19 and the long-range radar is being viewed for application by the Alaskan Air Command to replace the AN/FPS-93. These studies provide the assurance that current technology can support the development of unattended/minimally attended rad[illegible]hat offer improved performance and can significantly reduce operating [illegible]ntenance costs.

These efforts were performed in accordance with 1978-1982 TPO III, Thrust C Advanced Sensor Technology. The results will be used by ESD to develop system acquisition strategy for SEEK FROST (Project 2448), PE 12412F. It also provides supplemental data supporting SEEK IGLOO (Project 968H), PE 12325F.

Adrian S. Briggs

ADRIAN S. BRIGGS
Project Engineer

SECTION 1

STUDY APPROACH/CONCLUSIONS

1.0 STUDY APPROACH/CONCLUSIONS

1.1 Technical Problem

The unattended/minimally attended radar (UAR/MAR) concept is being examined by the USAF as a means of reducing high Operations and Maintenance (O&M) costs associated with present Distant Early Warning (DEW) Line system operations, and additionally as a method to improve the DEWLINE's air surveillance, e.g., low altitude coverage.

Air Force studies have indicated that a fence of contiguous, short range, unattended 2D radars (UARs) has the potential of being a cost effective, low risk, near term, system solution (i.e., lowest life cycle cost (LCC) system providing the necessary air surveillance). This new DEWLine consisting of approximately 80 UARs, geographically spaced, to improve low-altitude surveillance coverage, and seven manned logistical support nodes is postulated to provide early warning of all threat penetrations at a low LCC through significant reductions in O&M costs. Augmentation of this UAR fence with new, long range, 3D minimally attended radars (MARs), possibly located at the logistical nodes, is suggested as an approach that would provide an additional capacity for aircraft control (GCI) and weapons fire control needed to support air sovereignty/air defense missions.

Radar Design Requirements

The driving requirement for both the UAR and MAR is high operational reliability at low LCC. To satisfy this requirement, the system designs shall be constrained as follows:

1. Employ minimal operations and maintenance personnel

   a) Short range radar sites -- 60 mile range

      unattended operation
      periodic scheduled maintenance (e.g., 3, 6 or 12 months)
      unscheduled corrective maintenance

   b) Long range radar sites -- 150 to 200 mile range

      minimally attended operation
      common maintenance personnel

2. Have sufficient MTBF/MTTR to allow a single maintenance team stationed at a centralized maintenance node to support up to fifteen (15) assigned radar sites; and

3. Require minimal amounts of prime power so as to minimize system LCC.

Within this overall framework the radar(s) shall operate in the Arctic, provide all weather/altitude air surveillance coverage, correlate IFF and skin

reports, have a low false alarm rate, output track, ECM strobe, and radar/site status data via narrowband (e.g., 2400 bps) communication channels, and have a high system operational availability.

Recognizing both the cost to spare different components/assemblies and the likelihood for system requirement changes over a 20 year period, design guidelines need to be defined which permit change at nominal cost. Potential changes envisioned include UAR growth to a 3D capability, MAR growth to unattended operation and UAR/MAR support of air sovereignty/air defense missions. Therefore, the following design guidelines have been employed during this study:

1. Multiple function modules -- use of programmable modules suitable for performing a variety of different functions is to be considered wherever practicable;

2. Compatible system architectures -- UAR/MAR systems shall consider compatible architectures to accommodate 3D/unattended operation growth requirements respectively;

3. Common modules -- UAR/MAR designs shall consider the use of common (identical) modules where common functions are performed;

4. Standard interfaces -- where UAR and MAR systems perform similar functions but require different processing schemes standard input/output interfaces shall be considered;

5. Duplex communications -- two-way communication shall be considered to reconfigure UAR sites for equipment outages and to adapt to potential growth requirements; and

6. Logistic node/MAR colocation -- reduction in logistics support costs afforded by MAR and logistic node colocation shall be considered in selecting MAR emplacement sites.

Radar Performance Goals

The UAR/MAR design concepts evaluated were in response to the nominal performance goals supplied with the study SOW and summarized in Tables 1.1-1 and 1.1-2. Although these goals may be altered to reflect cost sensitivities revealed by contractor trade-off studies, they serve as a useful basis for determining individual concept sensitivities and totem poling alternative concepts. These baseline performance goals also provide the basis for identifying technological improvement areas which could result in significant improvements in reliability and/or performance, or significantly reduce implementation risks.

TABLE 1.1-1. NOMINAL UAR PERFORMANCE GOALS

Instrumented Range	60 nmi
Height Coverage	Radar horizon to 100K feet
Azimuth Coverage	360^{o} every 4 seconds
Elevation Coverage	-10^{o} to $+50^{o}$
Range Resolution	$\leq$0.5 nmi
Azimuth Resolution	$\leq 3.0^{o}$
Range Error	$\leq$0.25 nmi
Azimuth Error	$\leq 0.5^{o}$
Sidelobes, Transmit and Receive	-30 dB or lower each way
RF Bandwidth	10%
Primary Radar Power	500 watts maximum
Target Radial Speeds	-2400 to +2400 knots
Probability of Target Detection	0.95 probability of obtaining 3 detections in 4 trials on a $1m^2$ SWI target at 30 nmi range
Probability of False Alarm	10^{-6} per radar resolution cell
Probability of Track Initiation/Maintenance	0.95 probability of track initiation within 16 seconds of target entering the coverage volume; 0.95 probability of track maintenance
Probability of False Track Initiation	1 per hour
Probability of Terminating Track	0.999 probability of dropping track within 12 seconds of target leaving the coverage volume
Target Tracking Error	Heading $\pm 5^{o}$ Speed $\pm$10 percent
Simultaneous Track Capacity	$\geq$20
Reliability	0.9 probability of operating unattended for periods of 3, 6 and 12 months
MTTR	Minimal

TABLE 1.1-2. NOMINAL MAR PERFORMANCE GOALS

Instrumented Range	150/200 nmi
Height Coverage	Radar horizon to 100K feet
Azimuth Coverage	360^{o} every 12 seconds
Elevation Coverage	-10^{o} to $+25^{o}$
Range Resolution	$\leq$ 0.5 nmi
Azimuth Resolution	$\leq 3.0^{o}$

TABLE 1.1-2. NOMINAL MAR PERFORMANCE GOALS (Cont'd)

Range Error	≤ 0.25 nmi
Azimuth Error	≤ 0.5°
Height Error	±2000 ft at 100 nmi
Sidelobes, Transmit and Receive	-30 dB or lower each way
RF Bandwidth	10%
Primary Radar Power	Minimal
Target Radial Speeds	-2400 to +2400 knots
Probability of Target Detection	0.95 probability of obtaining 3 detections in 4 trials on a $1m^2$ SWI target at 150/200 nmi range
Probability of False Alarm	10^{-6} per radar resolution cell
Probability of Track Initiation/Maintenance	0.95 probability of track initiation within 50 seconds of target entering the coverage volume; 0.95 probability of track maintenance
Probability of False Track Initiation	1 per 15 minutes
Probability of Terminating Track	0.999 probability of dropping track within 36 seconds of target leaving the coverage volume
Target Tracking Error	Heading ± 5° Speed ±10 percent
Simultaneous Track Capacity	≥ 100
Reliability	0.9 probability of operating without intervening maintenance for periods of 0.5,,1 and 3 months
MTTR	0.5 hour

1.2 Study Methodology

The standard systems engineering approach tailored to reflect input data and desired outputs was employed for the UAR/MAR study (see Figure 1.2-1). The requirements analysis portion of the study was drastically reduced as a desired set of performance goals was furnished in the study statement of work (SOW). The stringent reliability requirement was used to limit alternative design approaches to be synthesized/evaluated. Trade-offs conducted were oriented towards providing acquisition and support costs versus reliability so as to establish optimized reliability goals, and thus, the lowest LCC system. Particularly cost sensitive and/or technically restrictive areas identified by the analyses formed the basis for recommended research and development.

Review of performance goals supplied in the SOW identified the UAR 90 percent reliability of operation for mission times of three months to one year and 500-watt UAR primary radar power allocation as the two most stringent

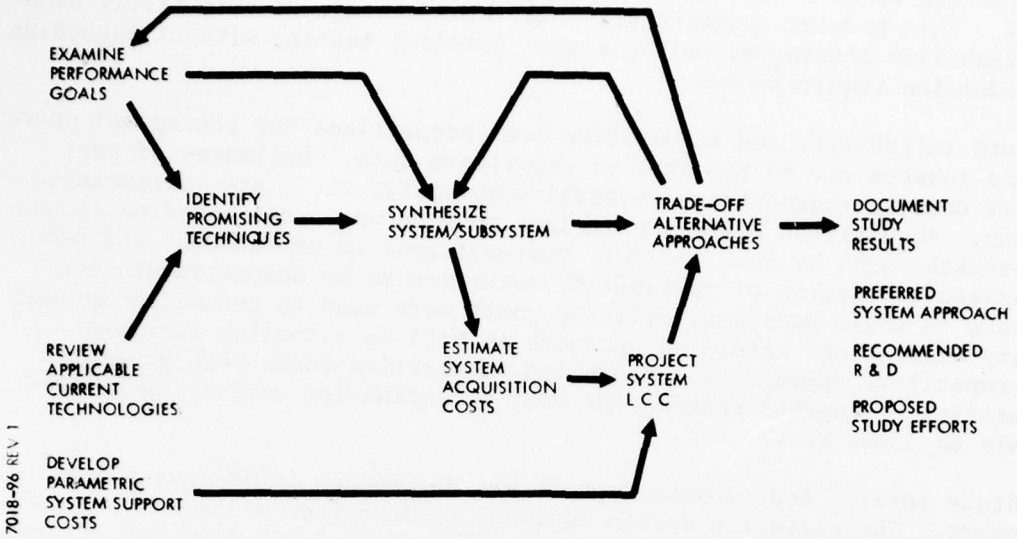

Figure 1.2-1. UAR/MAR Study Methodology

goals. Based on examination of current technology and ITT Gilfillan experience, rotating antenna approaches were eliminated from consideration (for UAR) and a requirement to implement with high reliability (screened) components assumed. The most promising techniques for satisfying UAR/MAR goals identified during the technology search were inputted to the synthesis process for evaluation.

Maintenance team composition and support requirements were also analyzed to determine support costs versus reliability. Although these costs are required for LCCs, initial usage for these data was to establish optimized reliability goals which would result in the lowest LCC. Costs were developed for single maintenance teams at each maintenance node and incremental costs associated with adding additional teams as required to maintain the desired system availability estimated.

Reference system and subsystem approaches were synthesized from promising techniques identified by the technology review and evaluated to determine their degree of compliance with reliability goals. The selection of an

M/N architecture allowed any requirement for reliability to be implemented via redundancy. This modular approach also has the advantage of effectively expediting reliability testing by multiple unit parallel testing without exceeding normal production requirements.

Both reliability and acquisition cost predictions for conceptual phase systems are tenuous due to the lack of experience data. Estimates of part types, part counts, redundancies, overall complexity, etc., are extrapolated projections. Acquisition costs are subject to wide variances based on technological breakthroughs or lack thereof, perturbations in procurement and production schedules, degree of reliability assurance to be demonstrated, etc. In deference to these problems, relative costs were used to establish optimal reliability allocations within an approach as well as establish rankings between competitive approaches. Projected acquisition costs were generated for competitive approaches showing the most potential for satisfying performance goals at lower LCCs.

Study results and recommendations are documented in following sections of the report. The preferred system approach is described along with the supporting trade-off analyses. Recommendations for study identified R&D efforts, and analytical study refinements are summarized. ITT Gilfillan internally funded, ongoing programs that are directly related to UAR/MAR program objectives are also included.

1.3 Study Conclusions

Reliability

The radar designs selected by ITT Gilfillan as most promising for the unattended radar (UAR) and for the minimally attended radar (MAR) are detailed in Sections 2 and 3 of this report. To achieve the very high functional reliability required for unattended/minimally attended operations, it was concluded that use of high reliability parts/components was necessary and that full advantage had to be taken of system/subsystem architectures which inherently provide redundancy and allow for graceful system performance degradation. Examples of the architectures utilized in the radar designs are detailed in Sections 2.3 (the M/N solid-state transmitter) and Section 2.6 (the M/N digital signal processor). These architectures employ M + N identical redundant channels of hardware to effect specific functions. Only M channels are needed for full function performance with N additional channels provided as standbys, that can be switched on line in case of M channel failures. This approach, in the extreme, can provide an infinitesimal probability of function failure. The actual number of N channels employed however, has been specified to yield a more cost effective approach, i.e., providing the reliability required for the minimum cost.

Performance

To guarantee the low altitude coverage required for the new DEWLine of short range overlapping UARs, while minimizing total system life cycle cost (LCC), it was concluded that the radar's operating frequency should be

specified to be high L-band, i.e., 1215 to 1400 MHz. This conclusion is substantiated in Section 2.1.1 of this report where it is shown for the situation with UAR antennas mounted on 100-foot towers, low altitude (100 ft) aircraft in a severe multipath environment can be detected to a maximum range of 13.7 nmi if the radar is operated at UHF, to 19.2 nmi if operated at L-band and to 21.3 nmi if operated at S-band.

Continuing Research and Development

To complete a study of the scope desired, in a time period limited to five months required us to proceed with due haste and to base some decisions on certain assumptions. This was unavoidable since the dialogue permitted between USAF and study contractors was, of necessity, also limited. To correct any misinterpretation of requirements and/or invalid assumptions made, it is recommended that the dialogue established between the USAF and ITT Gilfillan be continued in order to permit further optimization of the UAR and MAR designs. The next two sections of the report are devoted to a discussion of those R&D efforts recommended to optimize designs and minimize technical risk, and to a description of those programs ongoing at ITT Gilfillan that directly support the UAR/MAR program objectives.

1.4 Recommended Research and Development

Cost sensitivities revealed during the five month UAR/MAR study identified radar performance parameter goals which require firming and radar subsystem designs requiring research and development. Table 1.4-1 lists study areas and technology Research and Development (R&D) activities recommended.

The first three study areas are to refine radar design and harden costs by utilizing revised input requirements to optimize LCC effectiveness, and to solidify the program schedules by establishing reliability demonstration requirements. The final three analysis studies are to assure information requirements are met and potential means of improving operation and maintenance examined.

TABLE 1.4-1. RECOMMENDED RESEARCH & DEVELOPMENT

STUDY AREAS
1) Optimize site reliability goals
2) Refine system/subsystem designs
3) Develop UAR/MAR reliability demonstration program requirements
4) Delineate inter-site communication routing/interface standards
5) Assess advantages/disadvantages of remote fault isolation and correction aids
6) Investigate capability of an adaptive tracker to reduce effects of multipath and ECM
TECHNOLOGY R&D
1) M/N transmitter
2) M/N processor
3) Periodically loaded waveguide feed

The technology R&D efforts identified address those areas where innovative subsystem design approaches can be employed to improve operational reliability and/or significantly reduce production cost. The M/N transmitter development program recommended (see Appendix A) requires development in two critical areas. The development of distributed signal and data processing to optimally provide fault tolerance (see Sections 2.6.7 and 2.7.3) is also recommended. Development of the periodically-loaded waveguide feed (an ITT Gilfillan initiated development) will reduce the cost of producing frequency scan antennas (see Appendix B).

To accommodate the above activities and provide operable radar systems in a reasonable period of time, the UAR and MAR program schedules, shown in Figures 1.4-1 and 1.4-2 are offered.

The expeditious UAR program schedule assumes: 1) critical part orders for the engineering development model are placed 90 days after Contract Award Date (CAD), 2) a reliability growth program is instituted immediately following engineering model fabrication to improve reliability confidence level, 3) critical part orders for production prototype are placed 30 days after production contract award, 4) production builds to one/week, 5) UARs are air shipped by the local C-130 Air National Guard Unit, 6) western half of the system is installed and checked out the first year, 7) eastern half of the system is installed and checked out the second, and 8) reliability improvements required to achieve designated confidence level are retrofitted in the field. The production rate of one/week is considered high and a more relaxed schedule could result in reducing acquisition costs.

The MAR expeditious program schedule assumes: 1) prototype system critical parts are ordered 90 days after CAD, 2) systems are air shipped to Alaska by C-130s, and only one radar can be taken out of the air defense net at a time. Only the M/N processor development activity is shown as it is the only recommended R&D activity pertinent to the MAR development.

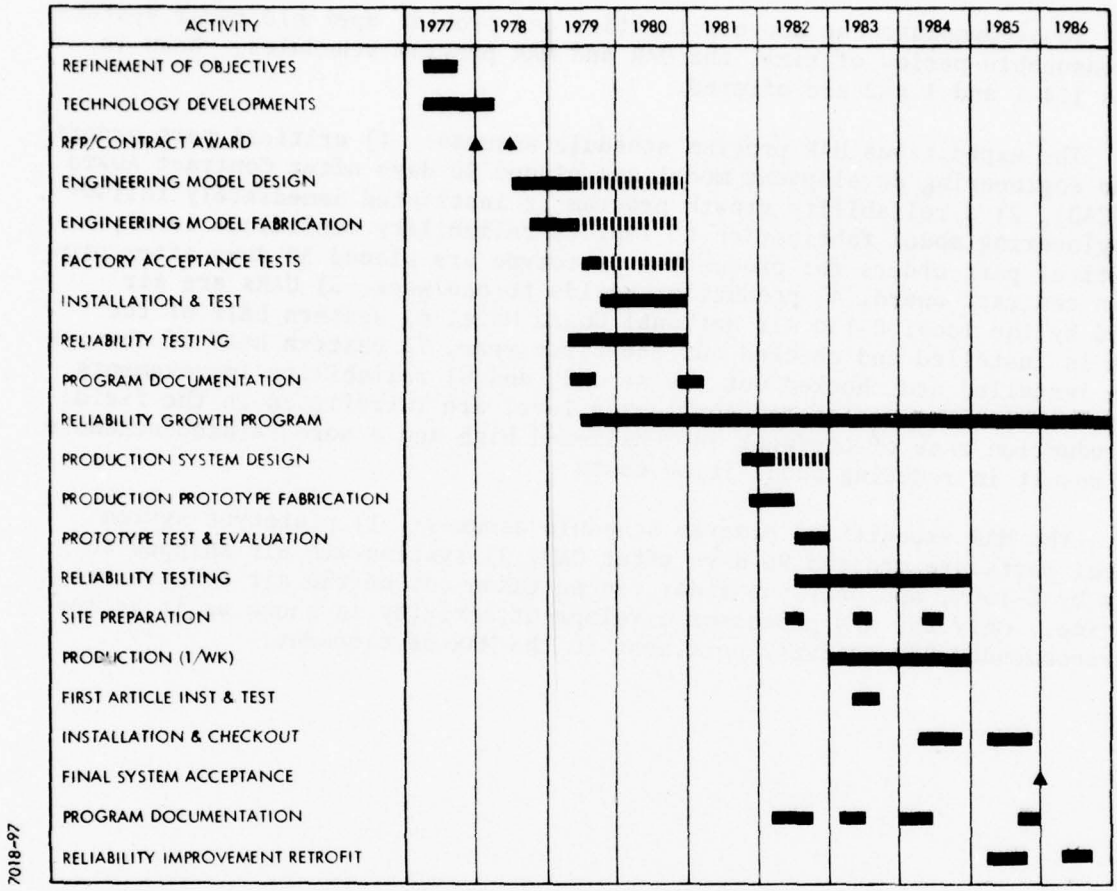

Figure 1.4-1. UAR Program Schedule

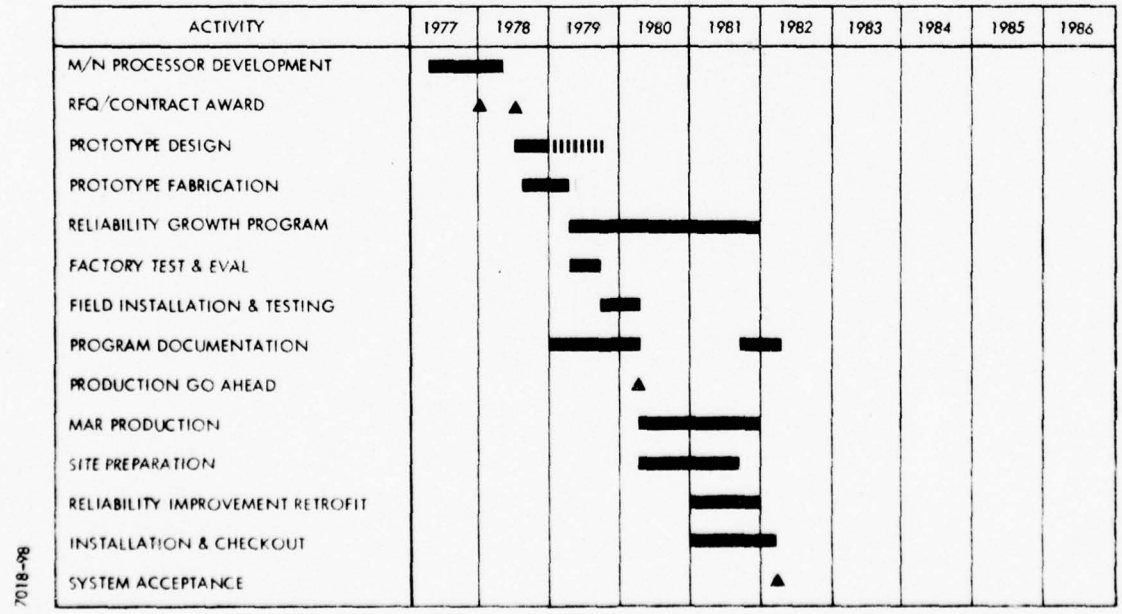

Figure 1.4-2. MAR Program Schedule

1.5 Special Comments

ITT Gilfillan's past and current internally-funded programs are structured to develop minimum LCC system/subsystem designs that have direct applicability to both the minimally attended and unattended radars' requirements.

Signal and Data Processing IR&D

Unattended/minimally attended radar operations dictate automatic target detection/tracking with surveillance data remoting via narrowband communications links. Of necessity, false alarms from clutter and/or interference must be kept to a minimum. Therefore, UAR/MAR parameter and signal/data processing selections must be specifically attuned to satisfying these requirements, e.g., good SCV and ECM identification capabilities must be provided.

In 1975, ITTG developed technology in the area of wideband Doppler signal processing. Preliminary designs were completed for two processors, a high resolution, real time, 128-point FFT with 200 nanosecond range resolution, and a target recognition processor which operates on the FFT output to effect the classification of aircraft targets.

In 1976, signal processing technology was developed in areas of radar waveform design — required for Doppler processing and for maximization of radar performance in heavy clutter and ECM environments, and correlation processes — employing adaptive algorithms to extract target signals imbedded in clutter and ECM backgrounds. In the data processing area, an adaptive tracking filter algorithm was developed which operates in various clutter environments and is constrained to provide high probability of target track with fixed low rates of false track initiation.

For 1977, development of signal processor architecture and technology is emphasized. The capabilities of previously developed programmable digital signal processors are being extended and new forms of analog (CCD, SAW) signal processing are being explored. One task is the development of a low cost array processing model for operating on digitized radar signal data. Two applications are: processing of a set of signals received by the elements of an antenna array to effect beamforming as in Array Signal Processing; or Doppler filtering by DFT processing. An array signal processing radar has the potential to attenuate unwanted interfering signals while detecting and locating desired target signals, if there is an angular difference between the two signals. Thus, substantial improvement in the performance of a radar operating in a clutter, multipath, or ECM environment could be obtained by use of array signal processing.

CCD technology provides a basis for development of a high performance MTI signal processor. Many of the performance characteristics of a digital processor can be obtained on an analog processor of small size and relatively low cost. The possibility of extending CCD technology to provide sophisticated filter or spectrum analyzer functions is being investigated. Additionally low LCC digital logic is being investigated via expanding the use of LSI with improved BITE capability.

Antenna Technology IR&D

There is an established need for cost-effective 3D antennas/radars having frequency agility and wideband multibeam capabilities. Frequencies generally acceptable for 3D system operation start at L-band and go higher. At L-band, compared to higher frequencies, it is less costly to effect physically large antenna apertures. Large apertures permit transmitter power (and prime power) requirements to be reduced and thereby provide inherently higher reliability and lower LCC systems. Another advantage attributable to an L-band radar is that its performance in clutter is superior to that of higher frequency systems.

In 1976, ITTG developed a wide (15 percent) operating bandwidth, low sidelobe (-35 dB peak), dual-slot, waveguide array design and a high-power, 4-bit diode phase shifter. This is the antenna that is described in Section 3.2 for use as the MAR antenna.

For 1977, a refinement of the antenna design above will be completed along with the fabrication of a subarray, beamforming network, vertical feed and prototype phase shifters. Also in 1977, the feasibility and limitation of an integrated multifrequency band array antenna will be demonstrated. For certain DEWLine sites, where it is not feasible or desirable to have UAR antenna systems mounted on very high towers to assure detection of low level penetrators in the multipath environment, it may be more desirable to use a radar capable of operating in multifrequency bands. A technique for integrating three radar frequency bands (centered at 900, 1300 and 3400 MHz) within a common antenna aperture has been conceived and will be investigated.

It is recognized that the UAR/MAR requirements could/can be satisfied employing phased array antennas The high cost and comparatively low reliability of the phase shifters, however, has limited our recommendation to use of the phased array approach only for the MAR (one mechanically rotated array that is phase scanned in elevation). A "variphase exciter" concept that uses diode-controlled coupling of multiple waveguide slots to form variable-phase elements from an integral series network feed has recently been developed at ITTG. This approach may have direct applicability for eliminating the separately identifiable phase shifters used in the MAR antenna and thereby increase its reliability and reduce its LCC.

RF Technology IR&D

The ITTG IR&D efforts in the RF technology area having applicability to the UAR/MAR requirements encompass the following:

1. Development of an L-band transmitter to keep pace with current and projected demands of automated minimally attended radar systems, e.g., RF frequency agility on a pulse-to-pulse or group-to-group basis, with intrapulse waveform coding agility, and having sufficient stability to permit required signal to clutter enhancement (≥50 dB in ground clutter): preliminary studies

indicated that the optimum approach was a low-cost, single stage, shadow-gridded TWT amplifier transmitter. This approach adopted for the MAR application (described in Section 3.3 as the MAR transmitter) permits the use of an all solid-state, low power, grid pulse modulator and has improved stability (≥55 dB).

2. Development of solid-state driver and exciters for the TWT transmitter described above, with improved performance in intermodulation products, power handling capability, and phase settling and all with higher reliability.

3. Development of frequency agile, wideband, stable Phase-Locked Loop Synthesizers: some of the benefits of the Phase Locked Synthesizer are — less in-band spurs, lower complexity, and fewer parts with reduced failure rates.

Systems Study Efforts

In addition to the technology developments discussed above, ITTG has internally funded systems study case efforts that are aimed at optimization of radar system approaches to provide required performance and reliability at minimum LCC.

One case having direct applicability to the MAR requirements is structured to conduct design trade-offs to optimize 3D architectures that achieve performance goals very similar to those stated for the MAR while minimizing system acquisition costs. This case additionally addresses definition of an adaptive track initiation process to ensure rejection of clutter false alarms, to accommodate the functions of ECM strobe reporting/elimination, and to provide track continuity on targets that fly courses traversing antenna pattern nulls due to multipath.

Another case having direct applicability to the UAR requirements optimizes 2D systems architectures to provide very high reliability at acceptable LCC.

SECTION 2

UNATTENDED RADAR (UAR) DESIGN

2.0 UNATTENDED RADAR (UAR) DESIGN

2.1 System Design

2.1.1 Operating Frequency Selection

The recommended operating frequency for the Unattended Radar (UAR) is L-band (1215-1400 MHz). Three frequency bands were evaluated for use in the UAR; these were UHF, L-, and S-bands. In addition to the 1215-1400 MHz band, the region from 890-942 MHz was also considered. These frequencies were all evaluated in terms of total system performance, ease of implementation, and cost impact. While each frequency offers certain advantages, the recommended frequency band is 1215-1400 MHz.

Clutter Backscatter

The frequency dependency of clutter backscatter coefficients is one important consideration. Figure 2.1-1 depicts typical coefficients for ground, sea, and rain clutter as a function of frequency. (Note: ground and sea

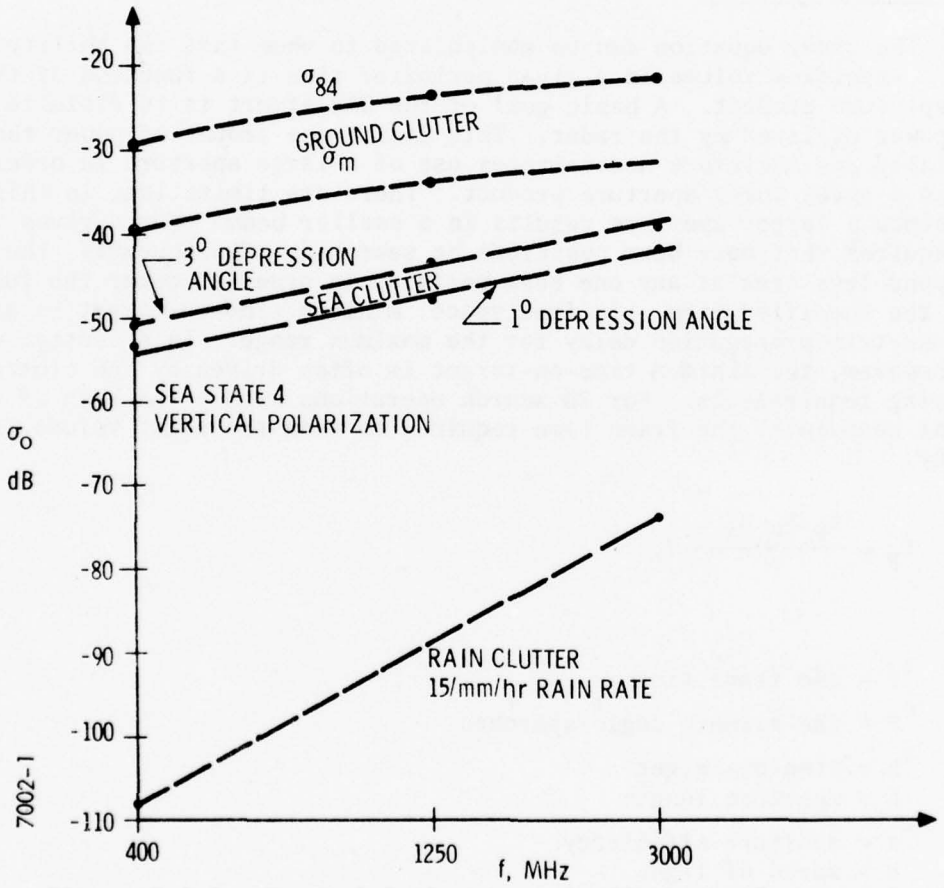

Figure 2.1-1. Typical Backscatter Coefficients for Ground Sea, and Rain Clutter

clutter coefficients are dB values of the clutter cross sections in $m^2/1m^2$, while rain is expressed in dB's as the ratio of $m^2/1m^3$.) Figure 2.1-1 clearly shows the advantage of lower frequency radars in terms of clutter backscatter coefficients — especially that of rain. However, this advantage is usually somewhat offset by the smaller cell sizes that typically result from higher frequency radars.

Solid-State Device Cost and Efficiency

Due to the extreme reliability requirements of the radar, solid-state power amplifiers are strongly preferred over tube-type amplifiers. State-of-the-art technology L-band or lower frequency transistors can be efficiently used in this application. For higher frequencies, however, the high power transistor development efforts are not as mature. Consequently, the devices produce much lower output power at lower efficiencies and higher costs. While advances will continue in higher frequency, solid-state development, it is expected that the lower frequency devices will maintain their lead in output power, efficiency, and lower costs.

Large Aperture Effects

The radar equation can be manipulated to show that the ability to search a specified volume in a given period of time is a function of the power-aperture product. A basic goal of the UAR effort is to minimize the prime power utilized by the radar. This limits the amount of power that can be radiated and therefore necessitates use of a large aperture in order to maintain a given power aperture product. There are limitations in this, however, since a larger aperture results in a smaller beam. For a given volume this requires that more beam positions be searched. Consequently, the radar must spend less time at any one beam position in order to cover the full volume in the specified time. In free space, minimum time-on-target is at least the round-trip propagation delay for the maximum range. In a clutter environment, however, the minimum time-on-target is often driven by the clutter processing requirements. For 2D search operations with a fan beam of constant vertical beamwidth, the frame time required to scan the radar volume is given by:

$$t_F \approx \frac{\theta_F \, t_b \, \eta_a \, L}{c} f,$$

where

t_F = the frame time
θ_F = the azimuth angle searched
t_b = time-on-target
L = aperture length
η_a = aperture efficiency
c = speed of light
f = transmit frequency.

Assuming a fixed aperture length and a constant minimum time-on-target as dictated by the clutter environment, the frame time is then directly proportional to the transmit frequency. A typical example is illustrated in Figure 2.1-2. Again lower frequencies offer an advantage over the use of higher frequencies.

Aurora - The presence of auroral echoes is a potential problem in the arctic. These result in rapidly changing clutter returns that are doppler shifted and produce a broadened clutter spectrum. However, the echo intensities are primarily a factor at lower frequencies of VHF and UHF, and frequency dependence of the intensity may vary from f^{-5} to f^{-10}. Auroral echoes are apparently insignificant at L-band or higher.

Frequency Allocation and RFI - Due to the large number of closely spaced radars, the possibility of interference from adjacent radars is a serious consideration. For this reason, as well as for possible ECCM advantages, a large operational band is desirable. The allocated radio location bands from 420-450 MHz and 890-942 MHz are very limited in the spectrum available. Both high L- and S-bands are more compatible with a wide bandwidth requirement.

Multipath - The presence of multipath and the requirement for detection of low flying targets are important factors in selecting the radar frequency. Figures 2.1-3 to 2.1-8 illustrate the signal strength in a multipath environment for UHF, L-, and S-band frequencies. The 0 dB signal level

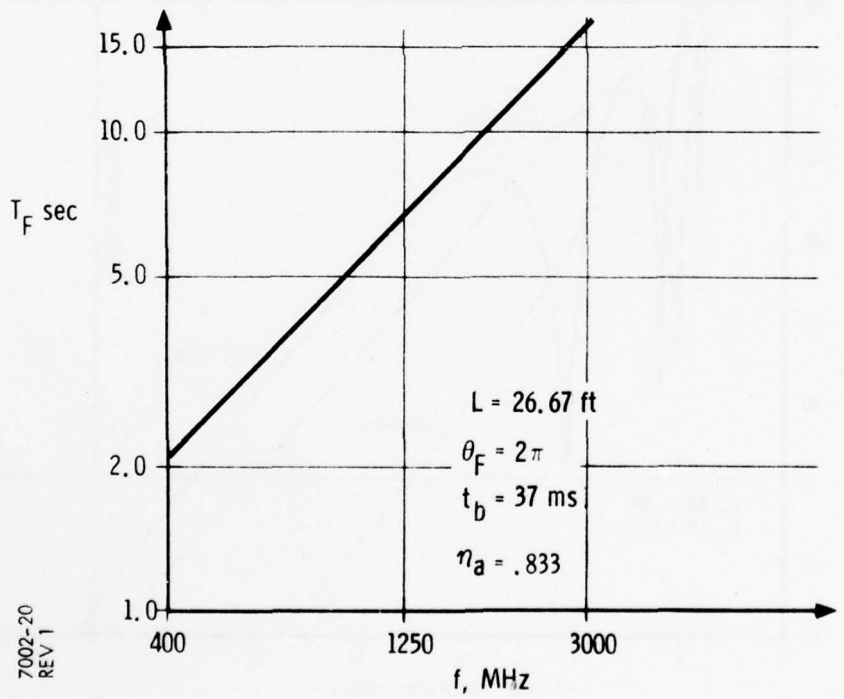

Figure 2.1-2. Frame Time vs Frequency For Typical Fixed Length Antenna

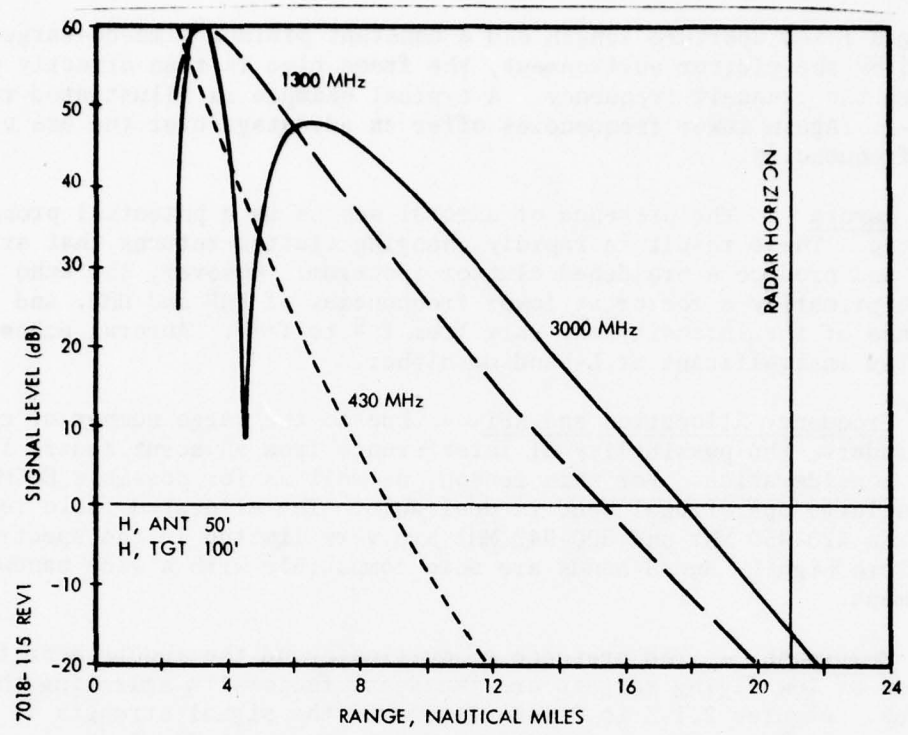

Figure 2.1-3. Signal Strength vs Range for Constant Height Targets

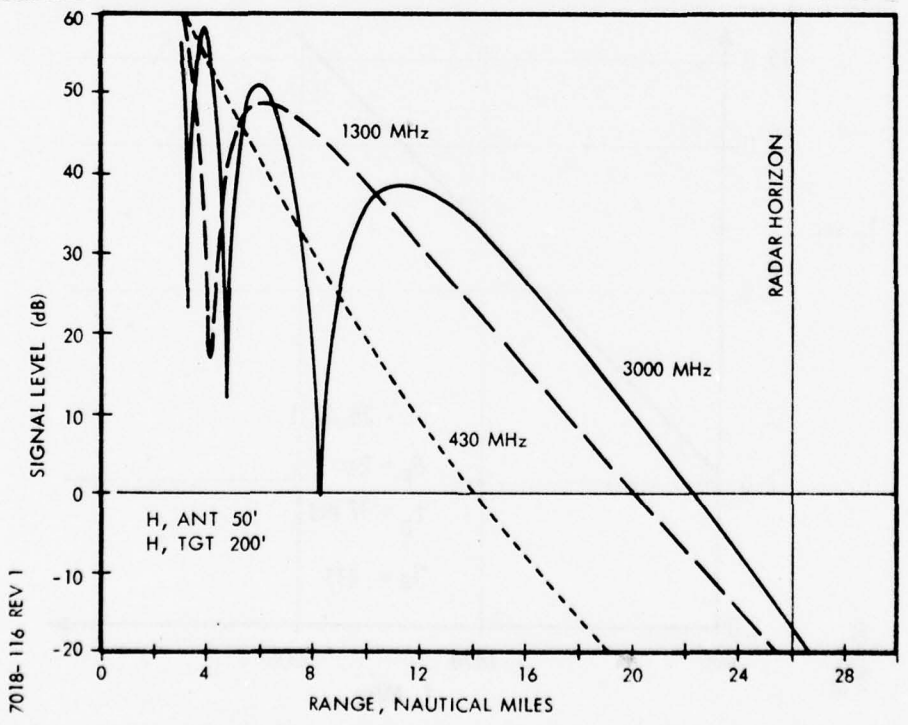

Figure 2.1-4. Signal Strength vs Range for Constant Height Targets

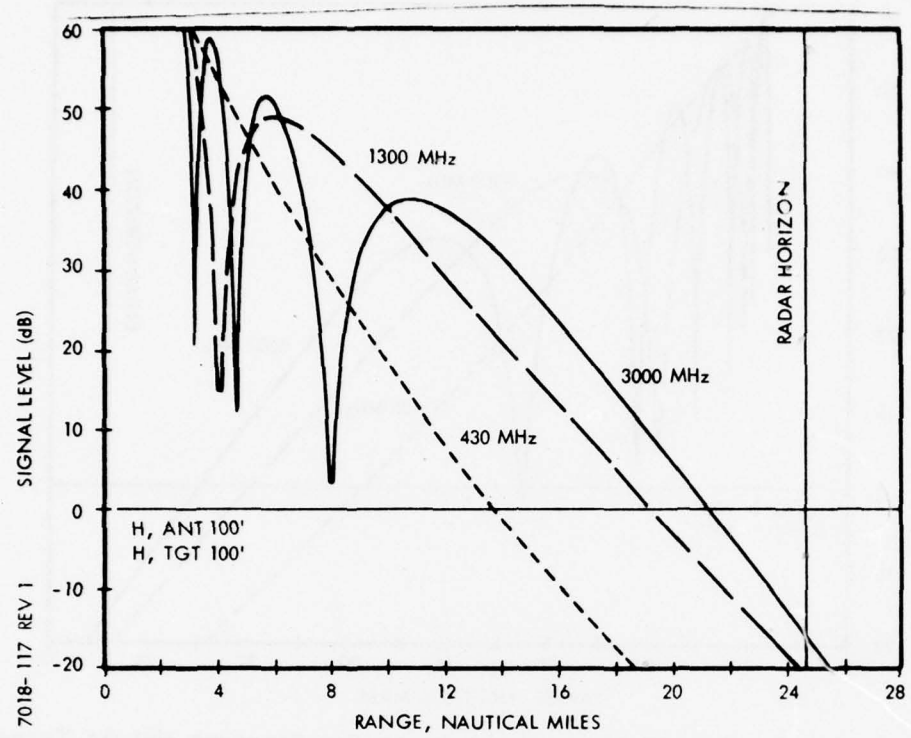

Figure 2.1-5. Signal Strength vs Range for Constant Height Targets

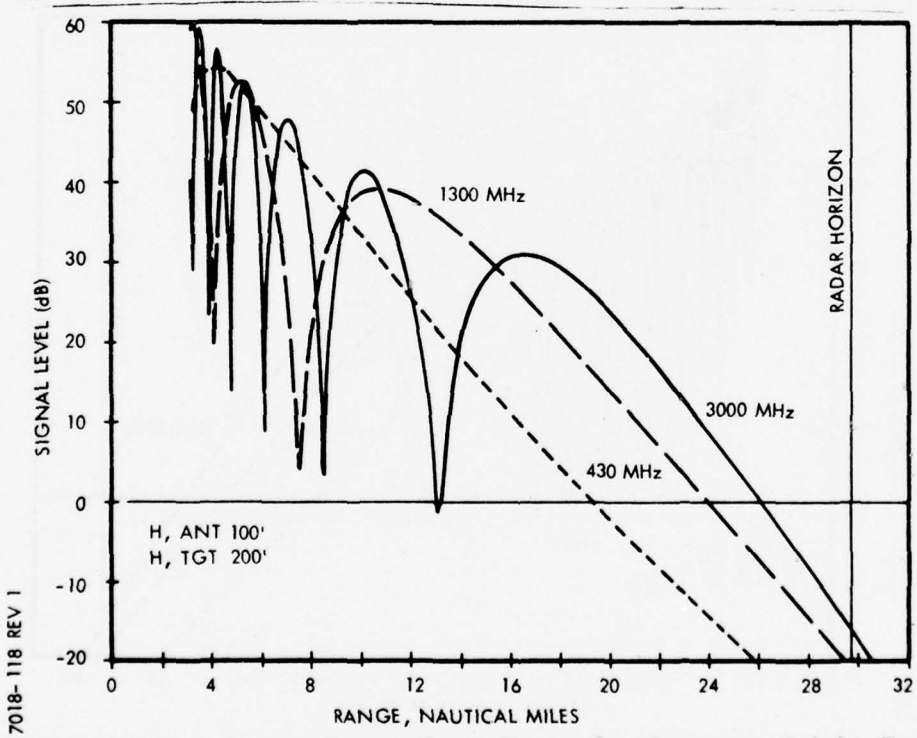

Figure 2.1-6. Signal Strength vs Range for Constant Height Targets

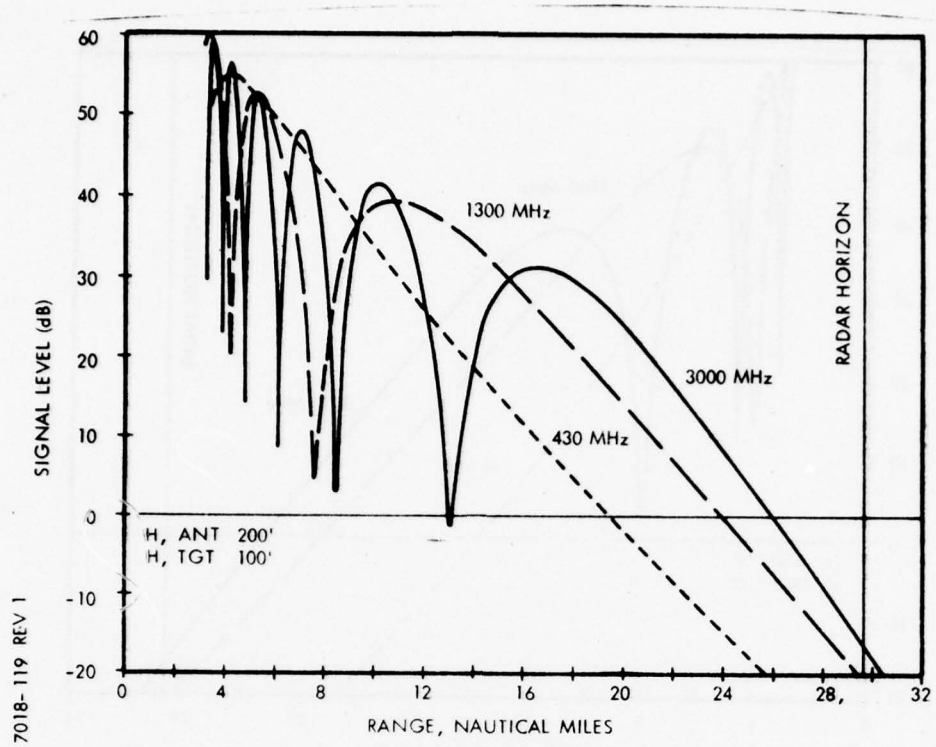

Figure 2.1-7. Signal Strength vs Range for Constant Height Targets

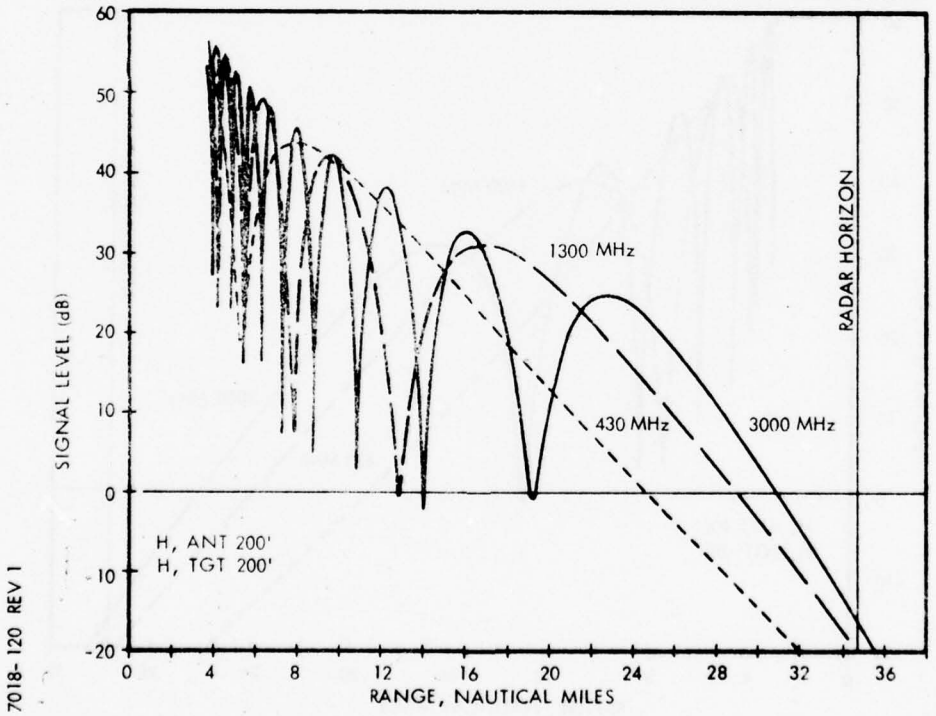

Figure 2.1-8. Signal Strength vs Range for Constant Height Targets

represents the radar's minimum detectable signal (MDS) required for the stated probability of detection. The worst-case reflection coefficient of $\rho = -1$ was used, and the assumed free-space range is 60 nmi. The figures are produced for three different antenna heights - 50, 100, and 200 feet. For each antenna height, two target heights are assumed - 100 and 200 feet. The superior performance offered by the higher frequencies is obvious. It is interesting to note, for example, that in Figure 2.1-5 the L-band MDS range is about 19 nmi. This assumes a 100 foot antenna and a 100-foot high target. In Figure 2.1-7 the MDS range for the UHF signal is also about 19 nmi. Again the target height is 100 feet, however, the antenna height for this case is 200 feet. In other words, for this multipath condition, the UHF tower height must be twice that of the L-band antenna in order to obtain the same low altitude target detection performance.

Frequency Selection Comparisons - Figure 2.1-9 provides a qualitative comparison of the various factors discussed previously. The lower frequencies offer advantages in ground, sea, and rain clutter and provide superior solid-state device power, efficiency, and cost characteristics. The lower frequencies are also more compatible with utilization of a large aperture while maintaining an acceptable frame time. On the other hand, the higher frequencies provide some improvement in the presence of auroral backscatter and in simplifying the mutual interference problem. The principal advantage of the higher frequencies, however, is improved performance in detecting low-flying targets in multipath. This is considered to be a very significant factor and tends to offset the advantages of UHF. Without specific weights to

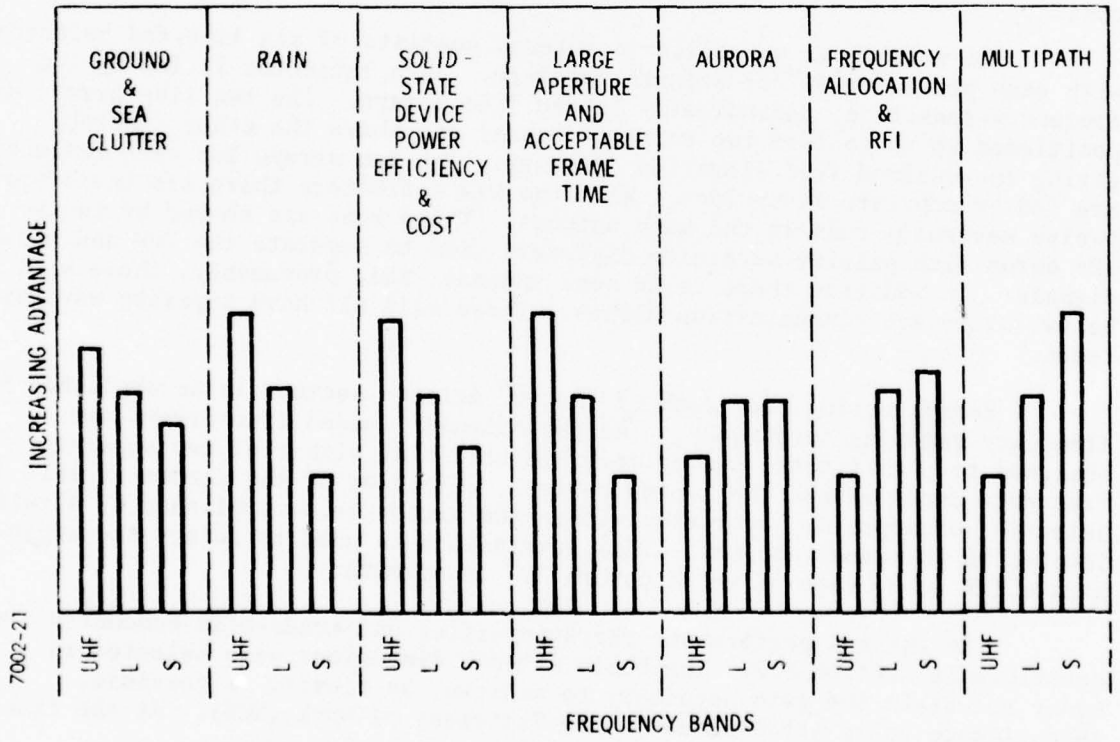

Figure 2.1-9. Frequency Selection Considerations

indicate the relative importance of the various factors from the operational requirements viewpoint, the selection of L-band (1215-1400 MHz), in our estimate, provides a near optimum solution.

2.1.2 System Configuration

The unattended radar system has been configured to provide maximum performance compatible with reliability, life cycle cost, and prime power constraints. The fundamental system requirements include performing the following operations: 360° 2D target surveillance and tracking, IFF, jam strobe reporting, and narrowband data remoting. The system has been designed to perform these operations in a reliable and cost-effective manner. The desired performance goals described in Section 1.1 were used as recommended means for achieving the fundamental performance requirements listed above. For situations in which specific goals conflicted with the constraints of reliability, cost, and prime power, the recommended approach was selected based on the criterion of reasonableness.

Numerous trade-offs were made throughout the study at virtually all levels of system design. Particular emphasis was placed on the critical problem of implementing a highly reliable, efficient, and low-cost antenna. Both cylindrical and linear arrays were examined, along with a variety of beam scanning implementations. The recommended approach employs frequency scanning arrays with only passive radar elements mounted on the tower. This approach provides good radar performance and is superior to the other approaches in terms of reliability, maintainability, power consumption, and cost.

The main radar surveillance antenna consists of six line-fed relectors with each providing 60° of azimuth coverage. Each reflector is fed by two frequency-sensitive, periodically loaded line arrays. The two line arrays are positioned so as to form two vertical beams, one above the other, thereby giving the desired full elevation coverage. The two arrays for each reflector are fed by separate waveguides. With the six reflectors there are therefore twelve waveguide runs to the main antenna. These runs are shared by twelve IFF horns with passive waveguide diplexers used to separate the IFF and radar signals. In addition there is an omni antenna, and, presumably, there will be two microwave communication dishes. These will all have separate waveguide feeds.

Beam steering over each of the 60° azimuth sectors is accomplished by frequency scanning techniques. The periodically loaded line arrays are designed to permit total sector coverage utilizing either of two separate frequency bands within the L-band region. Selection of the sector as well as selection of upper or lower beam within the sector is accomplished by a switch located in the radar shelter. This same switch is used to select the appropriate IFF horn, each of which covers 30° in azimuth.

The antenna performance characteristics and trade-offs conducted are described in Section 2.2. The basic antenna dimensions were selected in order to obtain the gain necessary to achieve, as closely as possible, surveillance goals established in the Statement of Work (SOW). At the final

study review with Air Force personnel, it was suggested that modification of the 3/4-detection scheme discussed in the SOW may permit reducing the size of the antenna aperture. This has subsequently been addressed and is described in greater detail in Section 2.1.5. As a consequence of this change, lengths of the line arrays were reduced from 40 feet to 26.67 feet and the reflectors from 44 feet to 30 feet. In discussion of the antenna trade-offs in Section 2.2, comparison data of the various approaches has not been recomputed for the decreased antenna size. It was apparent that this change would not affect the basic conclusion that frequency scanning was the preferred implementation.

The basic antenna structure is illustrated in Figure 2.1-10. This shows the arrays and reflectors placed in a hexagonal arrangement on the antenna tower. Also shown at the center of the platform are the 12 IFF horns, the omni antenna, and the microwave communication dishes. Depending on environmental conditions, a radome may or may not be required. If necessary, a 67-foot diameter radome will suffice.

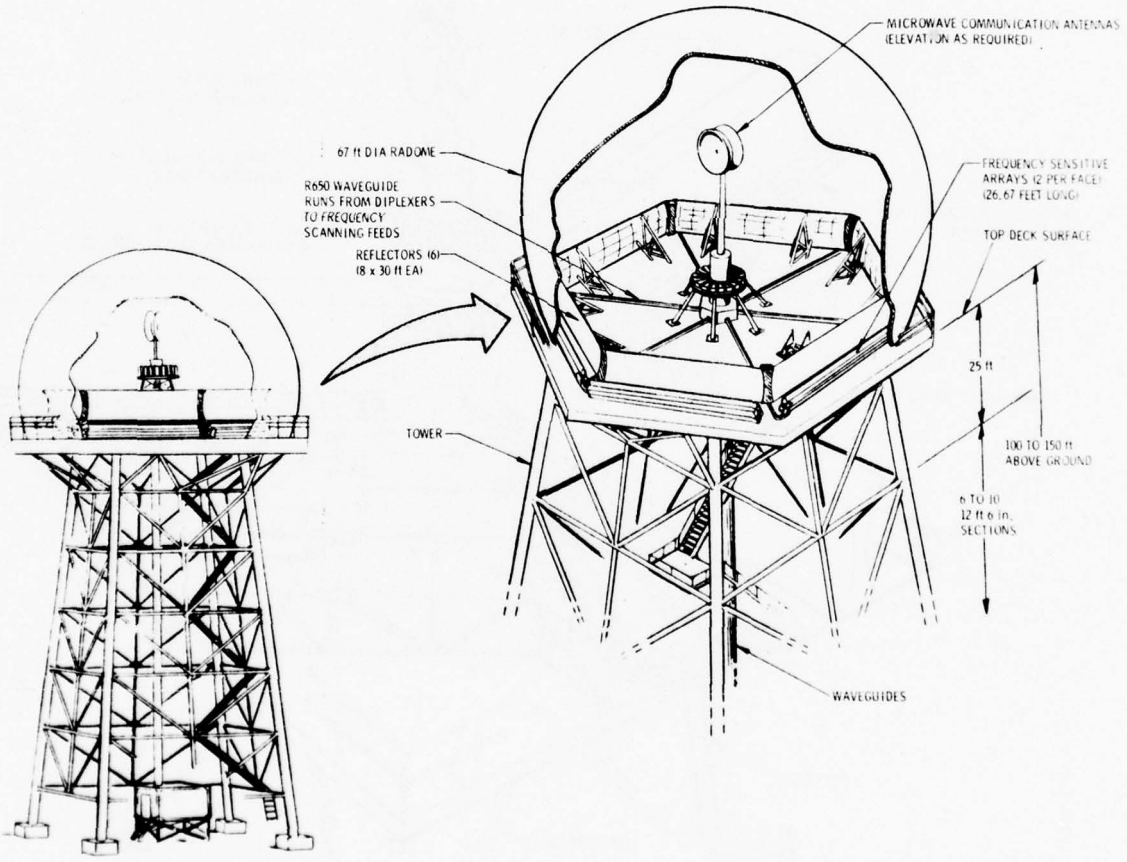

Figure 2.1-10. UAR Conceptual Sketch (Hexagonal Arrangement)

In a further attempt to reduce the size of the antenna structure, an alternate configuration was developed. This is called the tri-form arrangement, and it is shown in Figure 2.1-11. Array and reflector dimensions are the same as for the hexagonal arrangement, and the electrical characteristics are essentially identical. There are obvious structural advantages to the tri-form arrangement, however; and these are discussed in Section 2.1.6.2. Due to these advantages, the tri-form arrangement is the recommended configuration.

2.1.2.1 System Parameters - The system parameters were selected to satisfy the basic operational requirements of the radar. The major parameters incorporated in the system concept are listed in Table 2.1-1. These are closely related to various system and subsystem implementations and are themselves the results of numerous trade-offs.

Selection of L-band as the basic operating frequency was discussed previously in Section 2.1.1. Scan angle vs frequency sensitivity of the antenna is designed so that each of the six faces scans a 60° sector with two

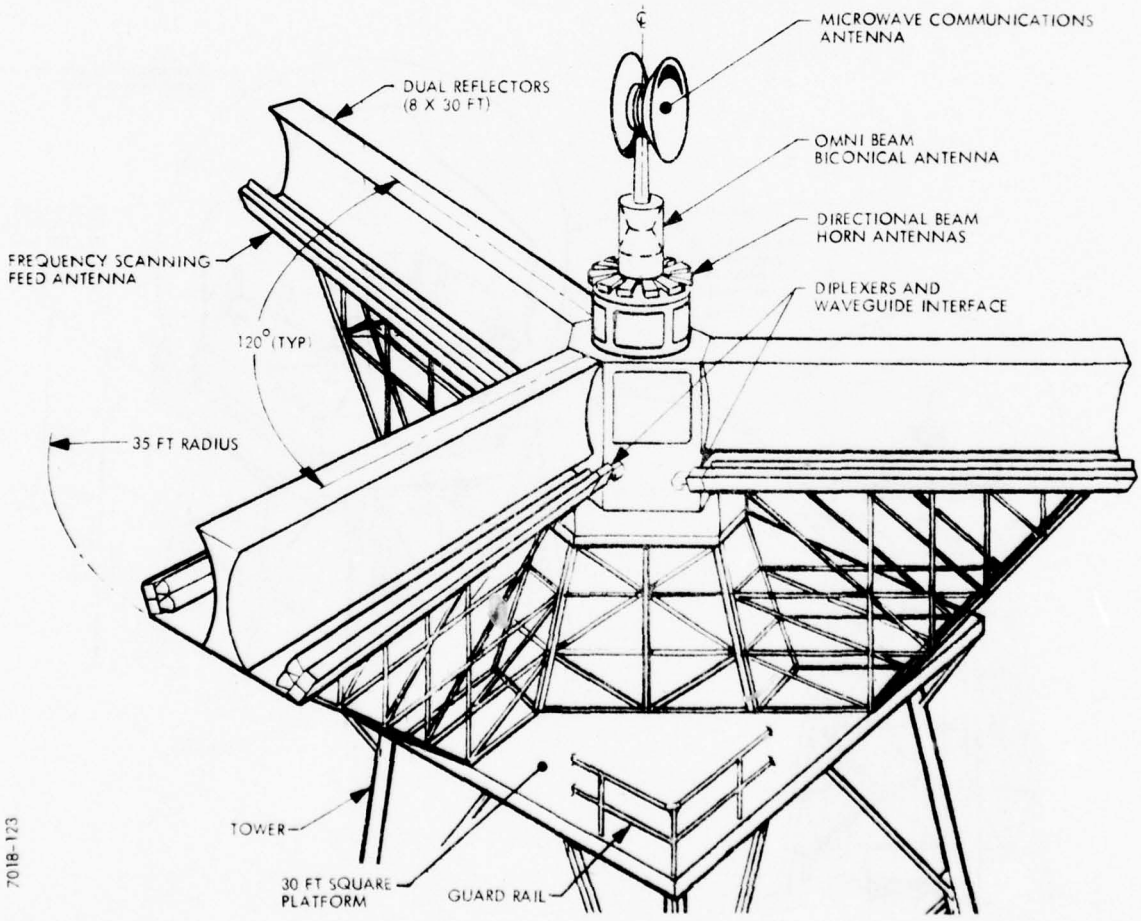

Figure 2.1-11. UAR Conceptual Sketch (Tri-Form Arrangement)

TABLE 2.1-1. UAR SYSTEM PARAMETERS

- FREQUENCY - 1215 - 1400 MHz (2 OPERATING FREQUENCIES FOR EACH BEAM POSITION)
- TRANSMIT POWER - 2 kW PEAK, 100W AVG
- WAVEFORM - NON-LINEAR FM, 40.0 μSEC EXPANDED, 1.333 μSEC COMPRESSED, 750 kHz BW
- EIGHT PULSES PER GROUP AT CONSTANT PRF AND CARRIER FREQUENCY
- SUCCESSIVE PULSE GROUPS AT DIFFERENT PRF AND CARRIER FREQUENCY
- FRAME TIME ~6 SEC
- IFF OPERATION WITH INTERROGATION SIDELOBE SUPPRESSION (ISLS)
- JAM STROBE REPORTING (NARROW-BAND) WITH SIDELOBE BLANKING
- PRIME POWER - 500W

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different frequency bands within the total operating range. This is useful in partially decorrelating the slowly fluctuating Swerling I targets and in providing somewhat greater jamming immunity.

The transmitter peak power of 2 kW is considered to be achievable through the use of current technology L-band bipolar transistors. An efficient and fault tolerant power combiner using 20 transistors is proposed. This combiner, described in Section 2.2.3 has build-in fault monitoring and switching circuitry for automatically energizing up to four cold standby transistor modules. The 100 watts average power assumes a five percent duty cycle.

Nonlinear frequency modulation is the recommended pulsecoding for this application. This waveform provides excellent range sidelobes for low velocity clutter and target returns while producing virtually no loss in SNR. The penalty paid for this performance is a degradation of range sidelobes for higher velocity targets. The trade-offs that were conducted in selecting this waveform are described in Section 2.6.2. The expansion and compression filters will be implemented with Surface Acoustic Wave (SAW) lines.

The average PRF of the radar is 1250 Hz; this is compatible with a 40 μsec transmitted pulse and a maximum range of 60 nmi. Sufficient stagger is incorporated to assure that the first blind speed will exceed 2400 knots. Coherent processing in a bank of eight discrete doppler filter channels is performed on groups of eight pulses at a constant PRF and carrier frequency. Between groups, both the PRF and carrier are changed. The beam is stepped 1/3 beamwidth in azimuth so that returns from three 8-pulse groups occur within the 3-dB beamwidth. The total frame time required for full 360° surveillance is about six seconds.

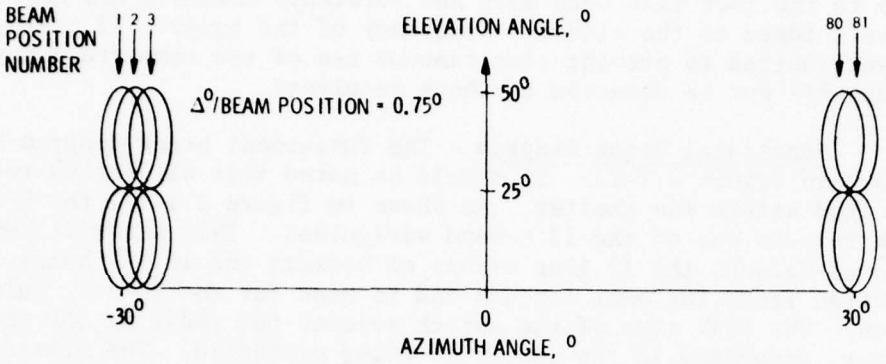
The IFF operates in a nonconventional manner. Coverage is provided by 12 IFF horns, each with a 30^{o} azimuth beamwidth. Interrogation and reception are not performed continuously. Rather, the IFF is activated only after a radar target track has been established and the appropriate 30^{o} sector determined. Once a satisfactory IFF reply has been received, interrogation of that target is halted. This sequential approach to IFF was adopted in order to minimize power consumption of the radar, to maintain a low fruit environment even with the overlapping coverage of nearby radars, and to further simplify defruiting requirements of the individual radars by range-gating the beacon response. The low fruit environment is also sustained through use of Interrogate Sidelobe Suppression. The P_2 pulse of the interrogation sequence is transmitted through the omni antenna.[2] This signal is used by the aircraft transponder to suppress responses that would normally be triggered by the sidelobe energy of the interrogating radar.

Mode 4 operation imposes special problems on the UAR IFF approach. It is assumed that classified encrypting equipment will not be installed at the unmanned site. As a consequence, the UAR will act essentially as a relay link between an operator at a manned installation, e.g., the ROCC, and the aircraft being interrogated. The encoded interrogation signal will be digitized and transmitted via the data link from the ROCC to the UAR. This will be stored in a buffer memory and, upon command, will be fed to the IFF exciter/transmitter for transmission. The encoded return will likewise be digitized, stored, and relayed back to the ROCC. There does not appear to be a security problem with this approach since the information transmitted over the data link is nothing more than the digitized form of the signals that are being radiated.

The radar also performs a jam strobe reporting function. This is accomplished by the log video detection of two signals, one from the main antenna array and one from the omni antenna. The omni antenna signal is used as a reference to inhibit reporting of strobes due to jamming energy entering the radar through the sidelobes of the main antenna.

2.1.2.2 Radar Scanning - As previously mentioned, the 360^{o} azimuth coverage is divided into six sectors of 60^{o} each. Furthermore, there are two separate vertical beams required to give the desired vertical coverage. This results in a total of 12 frequency sensitive line arrays used for the main antenna. Each of these arrays has a separate waveguide feed, and switching between the arrays is accomplished with a PIN diode switch located within the radar shelter.

The arrays themselves are designed to scan $\pm 30^{o}$ over two bands within the 1215-1400 MHz spectrum. In other words, any beam position within the 60^{o} scan limits of the array can be obtained with two different transmit frequencies. A typical scan program for a single sector is depicted in Figure 2.1-12. It is assumed that carrier frequencies f_L (for lower band frequency) and f_U (for upper band frequency) both result in a scan angle of -30^{o}. Also, a frequency shift of Δf produces a change in beam position of 0.75^{o}. In beam position 1, f_L is transmitted for eight pulses through the lower beam array. The next set of eight pulses is then transmitted through the upper beam array. For beam position 2, the lower beam array is again switched in,



BEAM POSITION NUMBER	CARRIER FREQUENCY
1	f_L
2	$f_u + \Delta f$
3	$f_L + 2\Delta f$
4	$f_u + 3\Delta f$

f_L = LOWER BAND FREQUENCY FOR -30^0 SCAN

f_u = UPPER BAND FREQUENCY FOR -30^0 SCAN

Δf = FREQUENCY SHIFT FOR 0.75^0 BEAM SHIFT

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Figure 2.1-12. Representative Scan Program

and carrier frequency is changed to the upper band with the appropriate frequency shift to move the beam 0.75^0, i.e., $f_u + \Delta f$. Following the 8-pulse group at the low beam, the upper beam is then transmitted at the same frequency. This process is repeated, alternating between upper and lower beams and between upper and lower frequency bands until the full 60^0 sector has been scanned. With an azimuth beamwidth of 2.25^0, this scan program produces three "hits" (groups of eight pulses) per target. Moreover, the frequency shifts between the upper and lower bands tend to decorrelate the target returns, thereby changing the target statistics from Swerling I to Swerling II.

Due to the close proximity of UARs required to give good low altitude coverage, the problem of interference between adjacent or nearby radars can be significant. In one sense, use of frequency scanning aggravates this problem, since a substantial portion of the frequency band is used to scan the beam. On the other hand, proper orientation of antenna arrays will completely eliminate the possibility of mainbeam-to-mainbeam interference. Unfortunately, antenna orientation alone will not eliminate sidelobe interference. Obviously low antenna sidelobes will offer some improvement; however, it is possible that synchronization of adjacent sites may be required to totally eliminate the problem. The synchronization problem is complicated somewhat by the requirement for IFF interrogation and by the verification beams used in track initiation. This can be overcome, however, by either "stealing" some time from other sectors, or by allocating a period of time for each sector in which these operations are performed. The latter method will slightly increase the frame time of the radar.

Frequency synchronization will also eliminate possible mutual interference problems associated with jam strobe reporting capability. This is due to the fact that both main and reference channels use narrowband receivers tuned to the transmit frequency of the radar. If nearby radars are synchronized to prevent simultaneous use of the same frequency, interference will not be detected in these receivers.

2.1.2.3 Functional Block Diagram - The functional block diagram of the UAR is shown in Figure 2.1-13. It should be noted that all active radar equipment is located within the shelter. As shown in figure 2.1-13, the SP13T RF switch selects one of the 13 L-band waveguides. This accomplishes the beam switching between the 12 line arrays or between the 12 IFF horns. The 13th connection feeds the omni antenna and is used for the ISLS P_2 pulse transmission. The SP4T side of the switch selects the radar or IFF transmitter or receiver, according to the operation being performed. The remaining major elements of the radar are described in the appropriate design sections of this report.

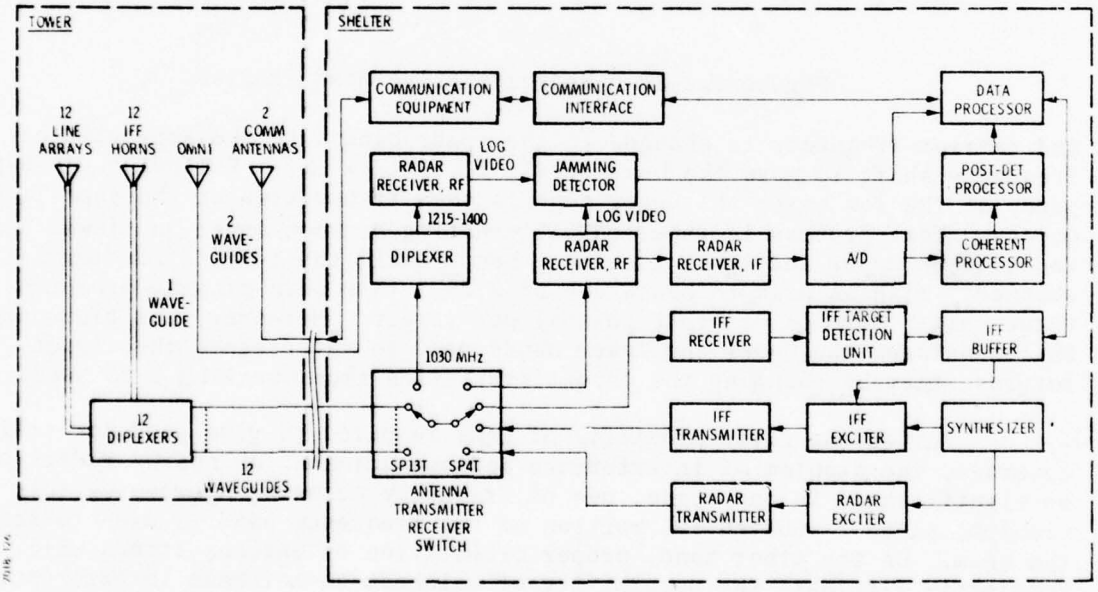


Figure 2.1-13. UAR Functional Block Diagram

2.1.3 Performance

Basic performance characteristics of the radar are listed in Table 2.1-3. Generally these characteristics satisfy design goals established in the SOW. Maximum range (for 0.9 P_D) is slightly less than the desired 60 nmi. Also, frame time has been extended from four to six seconds. However, with additional prime power allocations these characteristics could be improved.

Free Space Performance

Range performance was computed using the range calculation worksheet of Figure 2.1-14. The terms are generally self-explanatory except for possibly the various losses and visibility factor, V_Q. The losses are discussed in the sections covering the subsystems in which the losses occur. The visibility factor, V_Q = 3.4 dB, results from subtracting 9 dB (for eight pulses of coherent processing) from the required batch visibility of 12.4 dB. Justification of the 12.4 dB value is given in Section 2.1.4.

TABLE 2.1-3. UAR PERFORMANCE

Target Detectability Range (16 m^2)	
Free Space	58.2 nmi
84th Percentile Ground Clutter	57.2 nmi (50 dB Improvement Factor)
15 mm/Hour Rain	57.9 nmi (30 dB Improvement Factor)
Frame Time	6 sec
Range Accuracy	0.1 nmi
Azimuth Coverage	360°
Azimuth Accuracy	0.35°
Altitude Coverage	Radar Horizon (with reduced range in multipath) to 100K feet
Probability Track Initiation	0.95 in 24 sec
Probability False Track Initiate	1/hour
Number of Tracks	> 30
Prime Power Requirement	518.5 watts
IFF Capability - Including Mode 4	
Strobe Reporting with Sidelobe Blanking	

*RANGE CALCULATION WORKSHEET FOR RADAR

ENTER MISCELLANEOUS INFORMATION.			TARGET AT BROADSIDE	
1	θ - DEG	TARGET ELEVATION ANGLE	5^{o}	
2	σ - m^2	MEAN TARGET AREA	16	
3.	P_t - kW	PEAK TRANSMITTER POWER	2	
4	τ - USEC	PULSEWIDTH	40	
5	f - MHz	TRANSMITTER FREQUENCY	1300	
6	F_n - dB	RECEIVER NOISE FIGURE	2	
7	L_r - dB	RECEIVER TRANSMISSION LOSSES	0.5	
8	L_t - dB	TRANSMITTER TRANSMISSION LOSSES	0.5	
9	L'_a - dB	ANTENNA OHMIC LOSSES +0.58 dB	3.7	
10	N	NUMBER HITS PER SCAN	3 BATCHES	
11	F	ANTENNA PROPOGATION FACTOR	1	
COMPUTE $T_s = (T'_a + T_{a(l)})/L'_a + T_r + L_rT_e$				
12	L_r - (rat)	OPPOSITE L_r - dB IN TABLE 1	1.12	
13	T_e - °K	OPPOSITE F_n - dB IN TABLE 1	169	
14	L'_a - (rat)	OPPOSITE L'_a - dB IN TABLE 1	2.34	
15	$T_{a(l)}$ - °K	OPPOSITE L'_a - dB IN TABLE 1	387	
16	T'_a - °K	FROM FIGURE 11.	30	
17	–	ADD LINES 15 AND 16	417	
18	T_a - °K	DIVIDE LINE 17 BY L'_a (LINE 14)	178	
19	T_r - °K	OPPOSITE L_r - dB IN TABLE 1	35	
20	L_rT_e - °K	MULTIPLY LINE 12 BY LINE 13	189	
21	T_s - °K	ADD LINES 18, 19, AND 20	402	
COMPUTE NET RANGE IN DECIBELS:			+	–
22	P_t	10 LOG (P_t - kW)	3.0	.
23	τ	10 LOG (τ - USEC)	16.0	.
24	G_t	G_t (dB)	26.2	.
25	G_r	G_r (dB)	26.2	.
26	σ	10 LOG (σ - m^2)	12.0	.
27	f2	-20 LOG (f - MHz)	.	62.3
28	T_s	-10 LOG (T_s °K)	.	26.0
29	V_o	$-V_o$ (dB)	.	3.4
30	C_B	$-C_B$ (dB), FROM FIGURE 1	.	0.0
31	L_t	$-L_t$ (dB)	.	0.5
32	L_p	$-L_p$ (dB)	.	1.6
33	L_x	$-L_x$ (dB)	.	2.9
34	RANGE EQUATION CONSTANT (40 LOG 1.29)		4.45	–
35	OBTAIN COLUMN TOTALS		87.9	96.7
36	ENTER SMALLER TOTAL BELOW LARGER		.	87.9
37	SUBTRACT FOR NET RANGE DECIBELS		.	8.8
38	R_o	IN TABLE 2 FIND RANGE RATIO CORRESPONDING TO NET RANGE DECIBELS. MULTIPLY BY 100 FOR R_o	60.3	
39	R'	MULTIPLY R_o BY PATTERN PROPAGATION FACTOR F	60.3	
40	L_α - dB	FROM CURVES OF FIGURES 21 AND 22 FIND L_α CORRESPONDING TO R'	0.6	
41	δ_1	FROM TABLE 2 FIND RANGE-DECREASE FACTOR FOR L_α dB	0.966	
42	R_1	MULTIPLY R' BY δ_1. THIS IS RADAR RANGE IN NAUTICAL MILES	58.2	

*FOR USE WITH NRL REPORT 6930

V_o = 12.4 dB - 9 = 3.4 dB

Figure 2.1-14. Range Calculation Worksheet

Coverage provided by the two vertical beam antennas is illustrated in the Range-Height diagram of Figure 2.1-15. As shown in the figure, high altitude coverage of 100K feet specified in the SOW is obtained with the radar. Low-altitude performance depends greatly on the height of the antenna and upon radar reflectivity coefficient of the surrounding terrain. As was discussed in Section 2.1.1, antenna heights in excess of 100 feet may be required at some locations in order to ensure detection of low-flying targets.

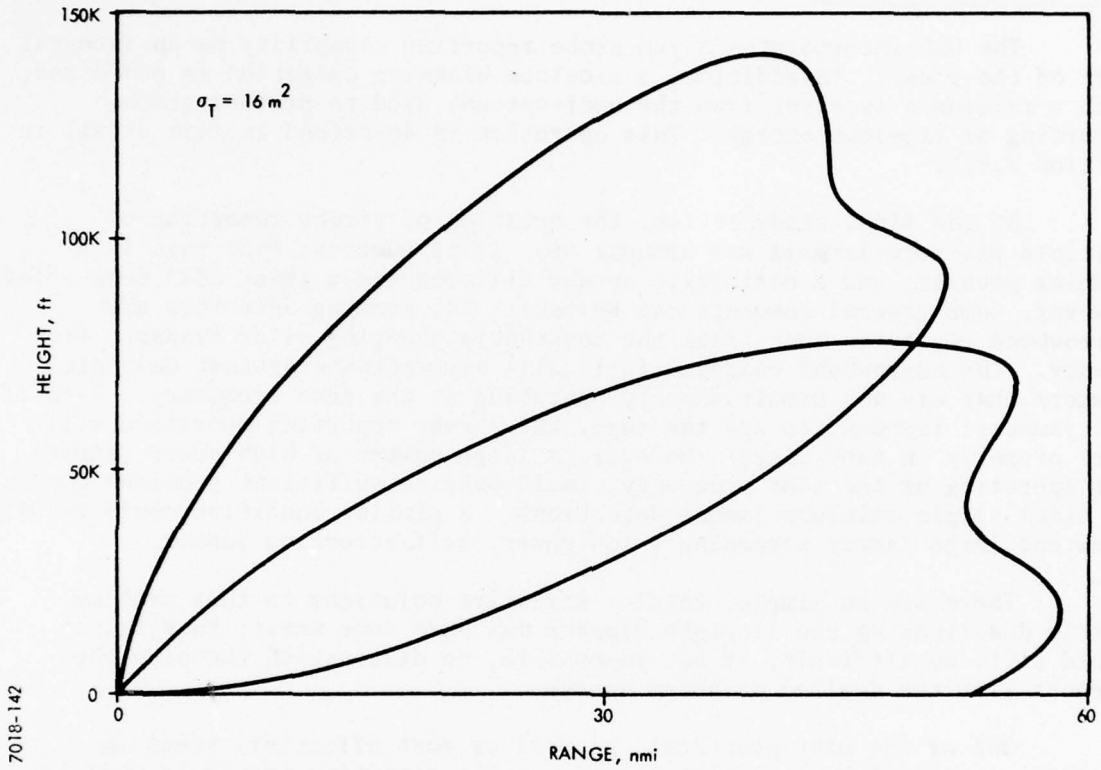


Figure 2.1-15. Range Height Diagram

Performance in Clutter

UAR performance in the presence of ground, sea, and weather clutter is discussed in detail in Section 2.6. The fact that the UAR coherently processes eight pulses at each beam position permits implementation of narrowband doppler filtering of the radar returns. This, in turn, permits rejection of clutter energy without seriously reducing the doppler spectrum available for target detection. Also, output of each narrowband doppler filter is processed by a CFAR filter to reduce the effects of extended clutter returns. Finally, adaptive clutter maps are used to censor radar cells which still exhibit clutter residue detections.

The radar beam is stepped one-third of a beamwidth between pulse groups. PRF stagger is incorporated between the three hits that occur within

the 3 dB beamwidth. This is done to eliminate target blind speed problems that would occur at doppler frequencies that are integer multiples of the PRF. In addition, at some locations exhibiting a lot of second-time around clutter, it may be desirable to transmit an extra pulse at the start of the 8-pulse string. This "fill" pulse is not processed directly in the receiver, but rather it is used to insure that the 8-pulse filters receive eight (and not seven) returns from the second-time-around clutter. This provision is easily implemented; however, it does increase the frame time of the radar.

Performance in Jamming

The UAR incorporates a jam stobe reporting capability as an integral part of the radar. In addition, a sidelobe blanking operation is performed, with a reference receiver from the omni-antenna used to prevent strobe reporting of sidelobe energy. This operation is described in more detail in Section 2.6.5.

At the final study review, the question of strobe reporting of multiple platform jammers was brought up. It is apparent that this is a complex problem, and a definitive answer will require a great deal more effort. However, some general comments can be made. The jamming detectors are narrowband receivers that track the constantly changing radar transmit frequency. The narrowband characteristic will discriminate against multiple jammers that are not simultaneously operating at the same frequency. Even if the jammers' frequencies are the same, the strobe reporting operation will work properly in many cases. However, a large number of high power jammers, all operating at the same frequency, could provide sufficient sidelobe energy to blank single mainlobe jammer detections. A similar condition could result from one large jammer screening a low-power, self-screening jammer.

There are no simple, totally effective solutions to this problem. Merely deactivating the sidelobe blanker may have some merit; however, it would still be difficult, if not impossible, to distinguish the sidelobe strobes from the desired mainbeam energy.

One of the most practical, as well as most effective, steps in handling the problem of multiple jammer strobe reporting is use of very low sidelobe antennas. The sidelobe-to-mainlobe jammer energy ratio must be very high to offset the difference between the antenna mainlobe and sidelobe gains. In addition, low antenna sidelobes provide improved radar detection performance in the presence of stand-off jamming. The degree of improvement is obviously dependent on the specific radar and jamming characteristics. Figure 2.1-16 illustrates UAR performance for a typical broadband stand-off jammer for several antenna sidelobe levels.

IFF Operation

The IFF transmitting, receiving, and processing operations are described in the sections for the respective subsystems. The basic IFF approach of interrogating only targets under track was discussed in Section 2.1.2. Table 2.1-4 shows the IFF interrogator transmitter power and IFF receiver sensitivity needed to perform the IFF function. These values are readily attainable with current solid-state devices and should cause no major development problems.

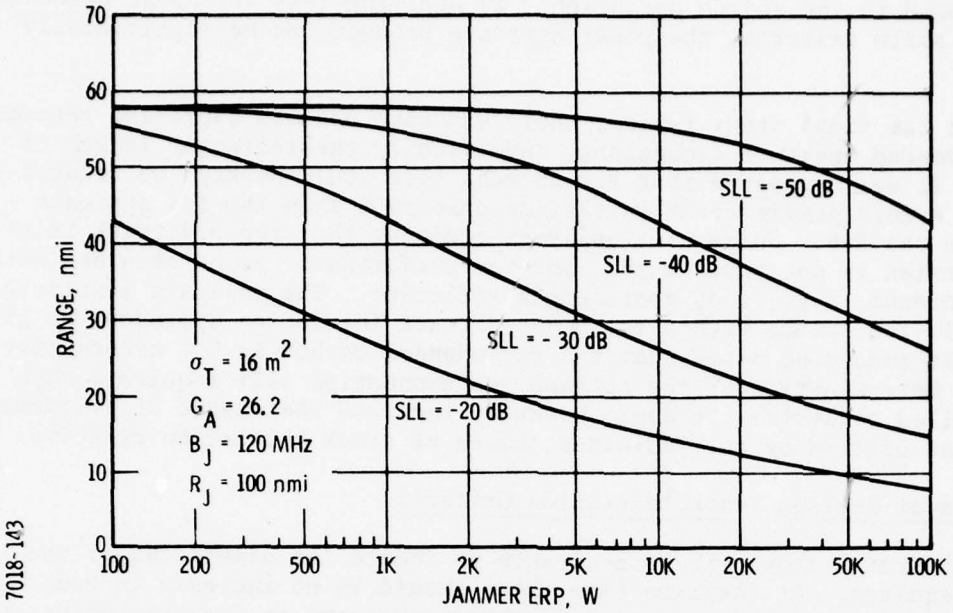


Figure 2.1-16. UAR Range Performance in Jamming Environment

TABLE 2.1-4. IFF POWER AND SENSITIVITY REQUIREMENTS

Interrogation Mode:	
Free Space Path Loss (60 nmi)	133 dBw
+ Airborne RCVR Sensitivity = -69 dBm	-99 dBw
∴ Required Interrogation ERP	34 dBw
- Interrogator Antenna Gain	-15 dBw
∴ Required Interrogator Transmit Power	19 dBw = 80 Watts
Reception:	
Transponder Power (27 ± 3 dBw) ≥	24 dBw
+ IFF Antenna Gain	15 dBw
- Free Space Path Loss (60 nmi)	-133 dBw
∴ Required Radar Sensitivity	-94 dBw = -64 dBm

2.1.4 Energy Management

A major concern of the UAR effort is minimization of the prime power required for the radar. As discussed previously, the power-aperture product is a fundamental radar characteristic indicating the ability of the radar to search a given volume in a specified time. Obviously, the required power-aperture product is dependent on the probabilities of detection and false

alarm assumed in the search operation. By applying less stringent detection and false alarm criteria, the power-aperture product can be significantly reduced.

At the final study review, there was some concern expressed regarding the recommended aperture dimensions, specifically the reflector length of 44 feet. It was suggested that the antenna size could perhaps be reduced by employing a less severe track initiation criterion than the 3/4 approach implied in the SOW. Subsequent analyses indicate that the 3/4 track initiation criterion is not optimum and improved performance can be obtained with a smaller antenna, e.g., a 30-foot length reflector. The analysis justifying this conclusion, along with a recommended track initiation approach, is given herein. It should be noted that the recommended method is not necessarily optimum. Determination of the optimum implementation will require a much more detailed analysis. It does, however, indicate the degree of performance improvement offered by the judicious choice of track initiation criteria.

Objectives of Revised Track Initiation Criteria

As stated above, it is desirable to reduce the dimensions of the antenna required. At the same time there should be no increase in radar prime power consumption. In order to obtain the same or improved detection performance, the following means are used to compensate for reduced antenna gain:

a) If the same frame time is maintained, more hits per beamwidth are available for processing by binary integration, viz., three hits vs. two hits.

b) Derivation of the probability of false alarm per resolution cell from the required false track initiation rate results in a higher permissible probability of false alarm than 10^{-6} per resolution cell called for in the SOW. This factor reduces the SNR required for a given probability of detection.

c) Introduction of a track verification procedure that is a form of sequential detection reduces the SNR required for detection. This is obtained at the cost of a small amount of additional time in the track initiation process.

The last item is beneficial not only in reduction of the SNR requirement, but (perhaps of more importance) it also results in reduction of the rate of false track initiations induced by clutter detections.

Conditions for Calculations

The primary performance requirements are assumed to be:

a) 0.95 probability of track initiation in four scan frames. (A frame time of six seconds is assumed.)

b) A false track initiation rate of one per hour including those resulting from noise and clutter detections.

Additional assumptions to be used in system design and in performance calculations are:

a) An additional 10 percent time budget is deemed acceptable for verification of tentative tracks.

b) An average track initiation gate of 740 resolution cells is required for track initiation on a 2400 knot target (see Appendix D).

c) An average of four clutter reports per scan are assumed to pass the clutter maps. It is assumed that the probability of clutter repeating in the same resolution cell on a subsequent scan(s) is 0.06. The clutter map is designed to censor higher probability clutter; see Section 2.6.4.

d) A Swerling II target is assumed to result as a consequence of frequency shift and elapsed time between batch transmissions. In order to assure this condition, the azimuth scan program may be designed to jump back and forth between beam positions rather than scan in a monotonic fashion.

Consideration of Simple Bernoulli Trial Criterion for Track Initiation

We consider, first, use of the following track initiation criterion: if m detections of a target (or noise) occur within n consecutive scans, a target track is initiated. The maximum value of m permissible is assumed to be four, since specification for the probability of track initiation is based upon the time required for four trials. For an initial comparison of the merits of various criteria, the case of false tracks initiated only on noise (no effects of clutter) will be examined. In Figure 2.1-17 the acceptable probability of false alarm per resolution cell P_{FA}/cell is plotted as a function of the rate of false tracks per hour initiated on noise. (See Appendix D.) One of the curves in this figure is identified with the notation 2/3/4 which denotes a m/n = 2/3 sliding window that encompasses four trials for target detection; as far as false track initiation is concerned, this is identical to a 2/3 criterion.

If we budget 0.5 false track initiation per hour due to noise, we note that the permissible P_{FA}/cell is approximately 3.6×10^{-5} for the 3/4 criterion, a factor 36 times the P_{FA}/cell initially used in detection performance calculations. From these data, we may derive the signal-to-noise ratios (SNR) required to give a 0.95 probability of track initiation in four trials as presented in Table 2.1-5.

In arriving at the required SNR, the probability of false alarm for each batch output (series of eight pulses) per range cell is obtained by considering the collapse of false alarms from: the dual antenna beams, eight filter outputs, and the three batches per beamwidth (a total collapse of $2 \times 8 \times 3 = 48$). The collapse factor of three per beamwidth arises from a 1/3-criterion for target detection in each scan, since it may be shown that this is the most efficient form of binary integration for this application.

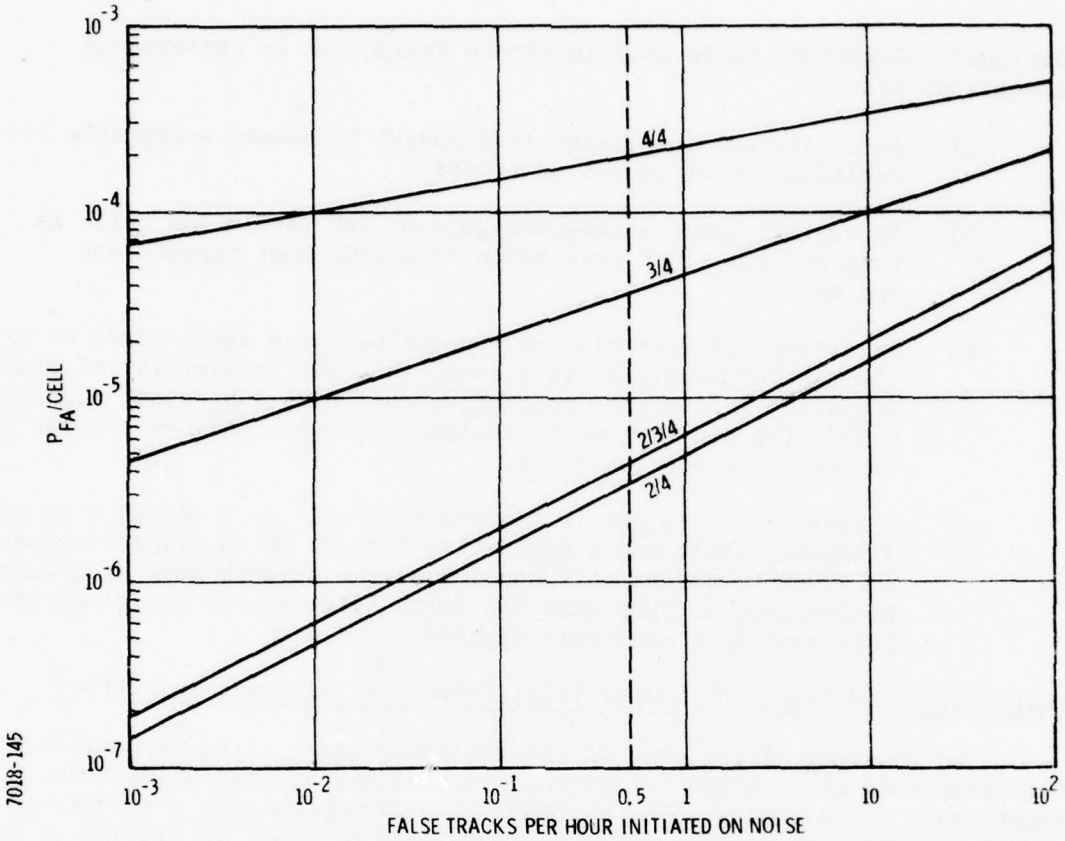


Figure 2.1-17. False Tracks Per Hour Initiated on Noise

TABLE 2.1-5. CALCULATION OF SNR FOR 0.95 P_{TI}/4

(Using data from Figure 2.1-17 with 0.5 false track initiations per hour)

	2/4	2/3/4	3/4	4/4
P_{FA}/cell (Figure 2.1-17)	3.5×10^{-6}	4.3×10^{-6}	3.6×10^{-5}	2×10^{-4}
P_{FA}/Batch (with 48 collapse)	7.3×10^{-8}	9.0×10^{-8}	7.5×10^{-7}	4.2×10^{-6}
P_D per Scan	0.752	0.805	0.902	0.987
P_D per Batch	0.370	0.420	0.539	0.765
SNR Required	11.9 dB	12.4 dB	13.5 dB	16.6 dB

Likewise, transformation of P_D per scan to P_D per batch is based upon the 1/3 criterion. This tabulation shows a performance degradation from 2/4 to 2/3/4 to 3/4 and finally 4/4. That is, the SNR required to maintain a probability of track initiation of 0.95 at the end of four trials increases progressively from 11.9 dB for the 2/4 criterion to 16.6 dB for the 4/4 criterion. However, the calculations were based upon use of a constant track initiation gate size. This is optimistic for the case of 2/4, since the gate must expand in some situations to allow two consecutive misses; it is pessimistic for the case of 4/4 since no misses are permitted and, therefore, a smaller track initiation gate could be used.

Now, however, when the clutter model previously stated is considered, the 3/4 criterion yields about 26 false track initiations per hour resulting from clutter detection. Hardening the criterion to 4/4 would be beneficial in the reduction of false track initiations on clutter, but at the expense of requiring a higher SNR. Since the clutter residue map contains the present clutter status and, thus, the probability of clutter, it can be used to adaptively harden the criteria only in those areas where excessive residue exists. This is a subject that ITTG proposes for further study.

Performance Improvement by Use of Track Verification Program

The design feature of inertialess scan affords an opportunity to improve efficiency of track initiation by using a form of sequential detection. After a tentative track is established by applying an m/n criterion to successive scans, the tentative track is verified or rejected by directing a series of pulses at the bearing of the suspected target.

There are probably many ways in which the combination of tentative track tests and verification can be applied. No claim is made that the scheme described below is optimum. It does, however, offer these features:

a) It reduces SNR required for track initiation.

b) It reduces the false track initiation rate on clutter.

c) These advantages are obtained with less than 10 percent additional time budgeted for the verification procedure.

The proposed scheme consists of a 2/3/4 criteria for the determination of a tentative track followed by a 3/5 verification routine, with the beam directed at the predicted bearing of the target. In each case, "binary integration" of m/n = 1/3 precedes the secondary Bernoulli trial process. Thus, the 3/5 verification routine actually involves transmission of as many as 5 x 3 = 15 batches of eight pulses. In order to assure a Swerling II target model, the batches transmitted at this same frequency must be separated by several tenths of a second.

In order to obtain a 0.95 probability of track initiation, an arbitrary assignment of equal probabilities was budgeted for tentative track and verification functions. Thus the probability of detection in each function must be 0.975. Another simplifying assumption, although possibly not an

optimum design, is that the threshold setting is constant for the detection and verification processes. In calculation of the probability of false alarm in the verification process, a gate of the same size as that used for tentative track initiation (740 resolution cells) was used, although a reduction of the gate size can be realized through the estimation of the target position.

It is a coincidence that approximately the same probability of detection (~0.855) for individual trials in both the 2/3/4 tentative track process and the 3/5 verification process yield the same probability of success (0.975) at the outputs of the two processes.

Under the above assumptions, the false alarm rate per batch was adjusted to yield an output false alarm initiation rate for thermal noise of about 0.4 per hour. Allowing for the same collapse factors as described in the last section, the threshold at the output of each filter must be set for a probability of false alarm of 1.35×10^{-6}. The 0.855 probability of detection at the output of the 1/3-binary integrator maps into a probability of detection of 0.475 on each pulse. From these values, a required SNR of 12.4 dB may be derived from standard curves for the single hit detection of a Swerling I or Swerling II target. In comparing this performance with Table 2.1-5 we note that the same SNR is required as for the simple 2/3/4 procedure (with a higher threshold setting). However, this process operating on the same clutter residue model reduces the false track initiation rate resulting from clutter detections to 0.6 per hour, thus reducing the total false track initiation rate to the acceptable value of one per hour.

It may be argued that this verification scheme delays track initiation beyond the four scan frames stated as the requirement. While an additional fraction of a scan is required to achieve a 0.95 probability of track initiation with the verification procedure, the average time for track initiation should be less than that of the simple 3/4 trial scheme. This results from the fact that the 2/3/4 criterion can produce a tentative track and initiate the verification action on only two trials; the 3/4 scheme always requires at least three trials.

An average number of verifications required because of tentative tracks established on noise or clutter was calculated to be less than one per scan. Thus the time required for transmission dedicated to verification is much less than 10 percent of the total time budget.

Conclusions

From the above exercise it appears that:

a) The 3/4 Bernoulli trial scheme for track initiation is probably not the optimum design for operation in a noise environment, and unless a very low level of clutter residue is maintained it may result in excessive track initiations due to clutter detections.

b) A track verification procedure will provide superior reduction of the effects of clutter while maintaining about the same performance in noise.

c) The 2/3/4 tentative track initiation scheme followed by a 3/5 verification procedure requires an SNR of 12.4 dB at the output of the doppler filter. This is approximately 2 dB less than that required with a 3/4 scheme and with a 10^{-6} probability of false alarm per cell. When this improvement is coupled with the increased number of hits per scan as a result of the greater azimuth beamwidth, the range performance originally calculated, using a greater antenna aperture can be achieved.

2.1.5 System Reliability

Reliability Design Approach

The inherent reliability of any equipment is basically a function of the type, reliability, and application of its component parts and the equipment complexity. Early in the UAR/MAR study, reliability predictions and mathematical models of a series configuration (no redundancy) UAR were made using various quality levels of component parts. These predictions and models were modified to incorporate the redundancy needed to provide a one-year radar with an inherent reliability of at least 0.9. It was determined that high quality or high reliability component parts were required throughout the radar to minimize redundancy and that no part type should be used that has a limited life of less than 200,000 hours.

During the study, various combinations of series/parallel redundant configurations were explored to determine the optimum configuration. The criterion for optimum was simple and practical monitoring and switching requirements, least required redundant paths, and lowest equipment costs.

Reliability Prediction

The predicted inherent reliability of 0.909 for a one-year mission for the UAR was determined in accordance with MIL-STD-756 procedures. Radar parts count data were estimated for the subassemblies of the UAR design, consisting of parts type and quantity per subassembly. Nominal failure rates of the detail parts were used for calculating the subassembly failure rates. Table 2.1.5-1 is a tabulation of the nominal failure rates used. The failure rates are based upon a part temperature of 25°C and a fixed ground environment. The tabulation also contains nominal application stress ratio for the failure rates.

For the reliability predictions it was assumed that only high reliability and high quality parts are used. Passive components (resistors and capacitors) are Military specified "ER" level S parts. Semiconductors (transistors and diodes) are JAN TXV quality components. Microcircuits are screened to MIL-STD-883, Level A, requirements. And magnetics (transformers and inductors) are Military qualified components.

Table 2.1.5-2 lists the predicted inherent failure rates and MTBF's for the assemblies of the one-year UAR. Data contained in this table is based upon having the necessary redundancy in the equipment design. Redundancy characteristics are provided in subsequent paragraphs. If all redundant

circuit paths were eliminated from the UAR, the predicted inherent MTBF of the series radar would be 4651 hours. Assembly failure rates for the nonredundant radar are contained in Table 2.1.5-3. In Appendix E of this report are detail parts estimates and failure rates for subassemblies of the UAR design.

From the series configured UAR, redundancy similar to the one-year UAR, but less extensive, is added to produce a reliability of at least 0.9 for a six-month or a three-month mission time. This is expanded upon in the mathematical models section of this report.

TABLE 2.1.5-1. PARTS FAILURE RATES

Part Type	Stress Ratio	Failure Rate Source	Failure Rate ($f/10^9$ Hrs.)
Resistor, Comp.	0.3	MIL-HDBK-217B	0.013
Resistor, Film	0.2	MIL-HDBK-217B	0.214
Resistor, Film Pwr	0.4	MIL-HDBK-217B	332.000
Resistor, W.W.	0.3	MIL-HDBK-217B	0.548
Potentiometer, Film	0.2	MIL-HDBK-217B	49.234
Potentiometer, W.W.	0.2	MIL-HDBK-217B	1.525
Capacitor, Tant.	0.4	MIL-HDBK-217B	0.086
Capacitor, Elect.	0.5	MIL-HDBK-217B	41.000
Capacitor, Other	0.1	MIL-HDBK-217B	0.092
Transistor, Sil	0.25	MIL-HDBK-217B	6.197
Transistor, Sil, RF	0.3	MIL-HDBK-217B	27.000
Transistor, Sil, SCR	0.3	MIL-HDBK-217B	5.500
Transistor, L-Band	0.3	MIL-HDBK-217B	270.000
Diode, Comp.	0.1	MIL-HDBK-217B	1.260
Diode, Rect.	0.3	MIL-HDBK-217B	5.100
Diode, Zener	0.3	MIL-HDBK-217B	10.725
Diode, PIN	0.3	Hewlett Packard	20.000
IC, SSI/MSI, Dig	NA	MIL-HDBK-217B	17.262
IC, SSI/MSI, Lin	NA	MIL-HDBK-217B	24.205
IC, 256B RAM	NA	MIL-HDBK-217B	27.980
IC, 1024B RAM	NA	MIL-HDBK-217B	87.350
IC, 256B ROM	NA	MIL-HDBK-217B	16.560
IC, 1024B ROM	NA	MIL-HDBK-217B	39.830
Microwave Diode, Mixer	0.3	MIL-HDBK-217B	600.000
Microwave Diode, Det	0.1	MIL-HDBK-217B	390.000
Xfmr, Pwr & Fil		MIL-HDBK-217B	6.601
Xfmr, Pulse		MIL-HDBK-217B	1.781
Xfmr, RF		MIL-HDBK-217B	8.904
Inductor, Filter		MIL-HDBK-217B	6.601
Inductor, RF		MIL-HDBK-217B	8.904

TABLE 2.1.5-2. UAR - ONE YEAR - RELIABILITY PREDICTION

Assembly	Failure Rate ($f/10^9$Hrs.)	MTBF (K Hrs.)
Antenna	1642.295	608
Radar Transmitter	450.323	2,220
IFF Transmitter	178.649	2,965
Receiver	1867.304	535
Signal Processor Front End	337.300	6,337
Signal Processor (Less Front End)	2274.732	439
Data Processor	3239.214	308
Power Supplies	2.244	
Transmit-Receive Switch	483.368	2,068
Cabling & Control	552.640	1,809

Total FR = 11,028.069 $f/10^9$ Hours

MTBF = 90,678 Hours

R(8760 Hours) = .908

NOTE: Failure rates based upon redundant circuits.

TABLE 2.1.5-3. UAR WITH NO REDUNDANCY RELIABILITY PREDICTION

Assembly	Failure Rate ($f/10^9$Hrs.)	MTBF (K Hrs.)
Antenna	1,902.022	525
Radar Transmitter	15,659.936	63
IFF Transmitter	1,535.304	651
Receiver	21,910.830	45
Signal Processor Front End	35,161.996	28
Signal Processor (Less Front End)	24,330.200	41
Data Processor	111,893.992	9
Power Supplies	1,832.728	545
Transmit-Receive Switch	241.684	4,137
Cabling & Control	552.640	1,809

Total FR = 215,021.332 $f/10^9$ Hours

MTBF = 4651 Hours

Reliability Models

Reliability block diagrams and mathematical models, based on the UAR conceptual designs are presented and discussed in this section. The one-year UAR model is contained in Figure 2.1.5-1. As shown, standby redundancy is used for the Receiver and Signal Processor (less front end) with other assemblies of the radar in series. The math model used for the redundant failure rate of the Receiver is:

$$R'_R = e^{-\lambda_R t}(1 + \lambda_R t) = 0.984$$

$$\lambda'_R = \text{Ln } R'_R/t = 1867.3 \text{ f/}10^9 \text{ Hours.}$$

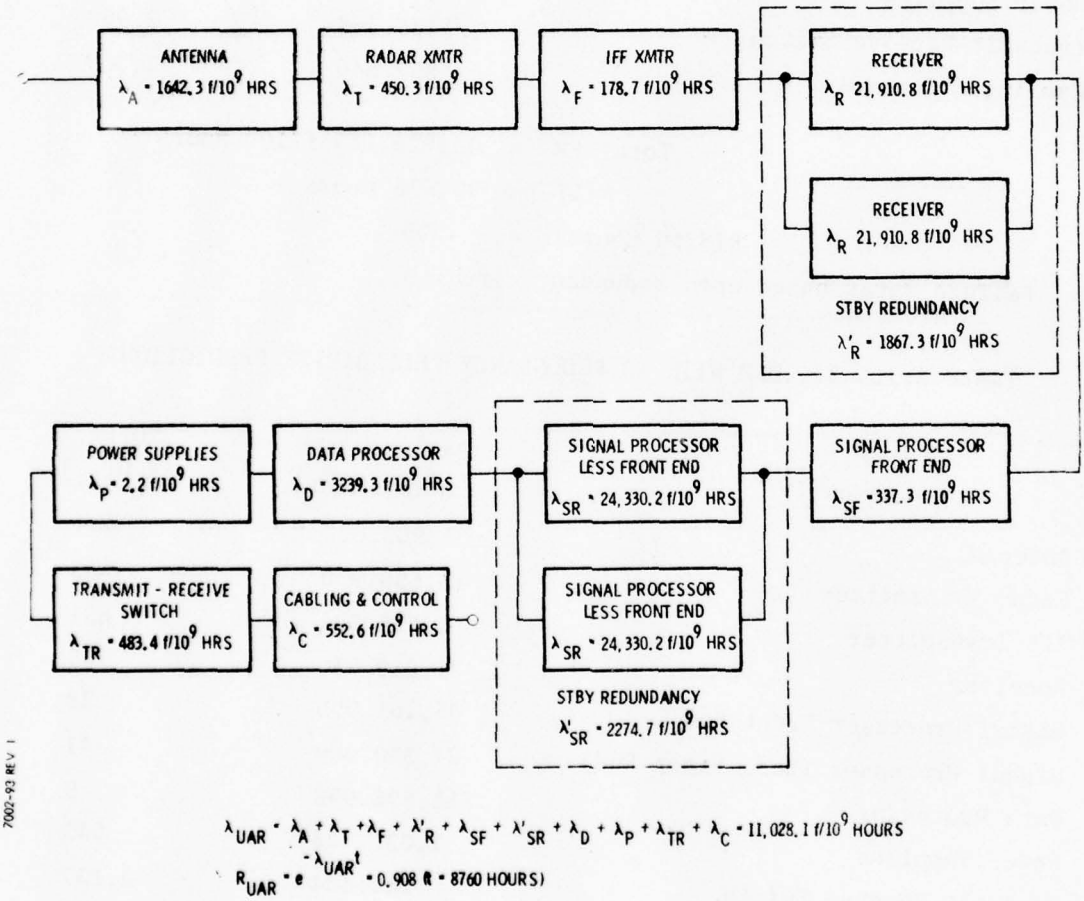


Figure 2.1.5-1. UAR - One Year - Reliability Math Model

This redundant failure rate is based upon the probability of one or less receiver channels failing in an 8760-hour (one year) time period. The same general model is used for the redundant failure rate of the Signal Processor (λ_{SR}). Reliability block diagrams and math models for the UAR's assemblies are contained in Figures 2.1.5-2 through 2.1.5-9.

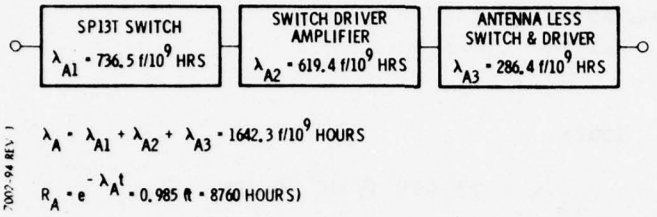


Figure 2.1.5-2. UAR Antenna - One Year Reliability Math Model

Antenna

The three subassemblies of the Antenna (Figure 2.1.5-2) are in series. The only redundancy in this assembly exists in the single pole thirteen throw (SP13T) PIN diode switch. An additional PIN diode is provided at each switch position to provide active redundancy for the PIN diodes. In terms of failure rate, this redundancy could be omitted. However it is recommended, as this is considered a potential failure mode and the failure rate data on PIN diodes is limited. The switch driver amplifier subassembly consists of thirteen identical driver amplifier modules which are all considered in series (no redundancy).

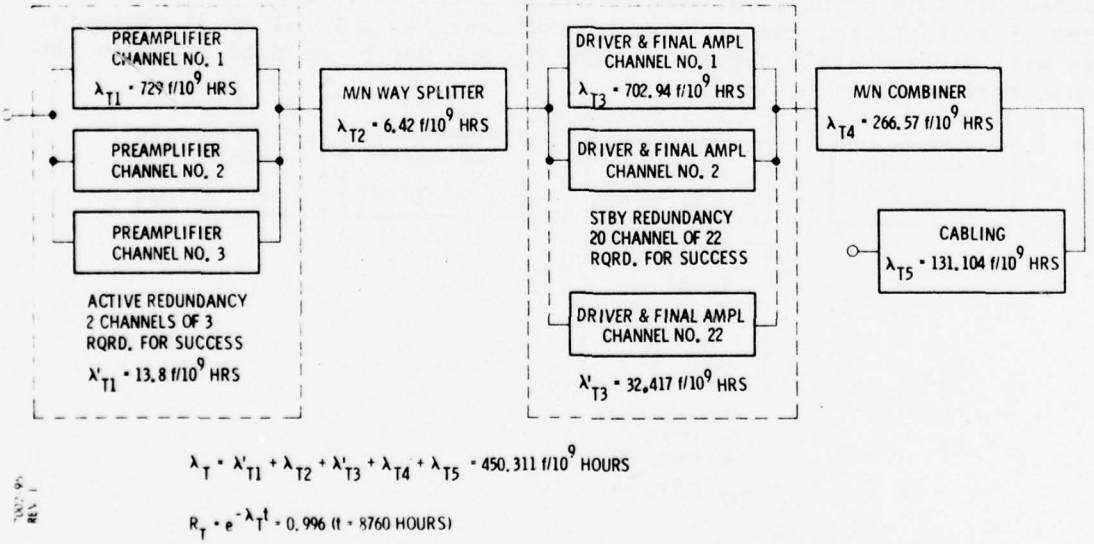


Figure 2.1.5-3. UAR Transmitter (Radar) - Reliability Math Model

Radar Transmitter

The Radar Transmitter (Figure 2.1.5-3) contains active redundancy in the preamplifier section and standby redundancy in the driver and final amplifier stages. Other items of the transmitter are in series. The preamplifier consists of three energized amplifier channels of which the combined output power level from two channels is required for full operating capability. Soft degradation due to a one channel failure is therefore operationally acceptable. The model for the preamplifier is:

$$R'_{T1} = 3e^{-2\lambda_\eta t} - 2e^{-3\lambda_\eta t}$$

For t = 8760 Hours

$$\lambda'_{T1} = -\text{Ln } R'_{T1}/t = 13.819 \text{ f/}10^9 \text{ Hours.}$$

The driver and final amplifier stages contain 20 identical channels, which are normally energized, plus two deenergized standby redundant channels. This provides standby redundant configuration in which 20 of 22 channels are required for full performance operation. The model is;

$$R'_{T3} = e^{-20\lambda_{T3}t}\left[1+20\lambda_{T3}t + \frac{(20\lambda_{T3}t)^2}{2}\right]$$

For t = 8760 Hours

$$\lambda'_{T3} = -\text{Ln } R'_{T3}/t = 32.417 \text{ f/}10^9 \text{ Hours}$$

Switching driver and final amplifier channels is accomplished with PIN diode switches. As in the Antenna, redundant PIN diodes are recommended and are assumed for this prediction. Note: While 20 of 22 channels is sufficient in terms of reliability, the recommended combiner has a total of 24 channels. This will provide still higher reliability and may be used to increase the transmitter power if desired.

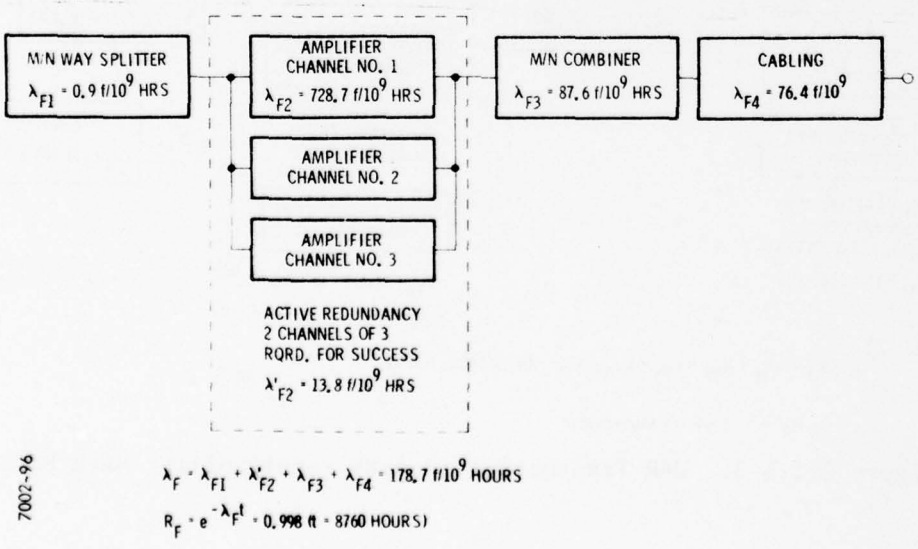


Figure 2.1.5-4. UAR Transmitter (IFF) - One year Reliability Math Model

IFF Transmitter

The IFF Transmitter (Figure 2.1.5-4) contains active redundancy in the RF amplifier and is the same as that which is provided for the preamplifier in the Radar Transmitter. The same general math model that applies for the Radar Transmitter Preamplifier is applicable to the IFF Transmitter RF Amplifier. Other subassemblies of the IFF Transmitter are in series and contain no internal redundancy.

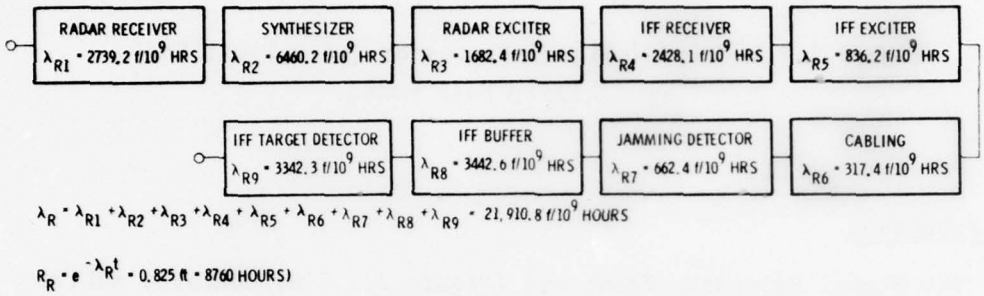


Figure 2.1.5-5. UAR Receiver - Reliability Math Model

Receiver

The UAR Receiver (Figure 2.1.5-5) contains no redundancy. All parts of the receiver subassemblies are in series.

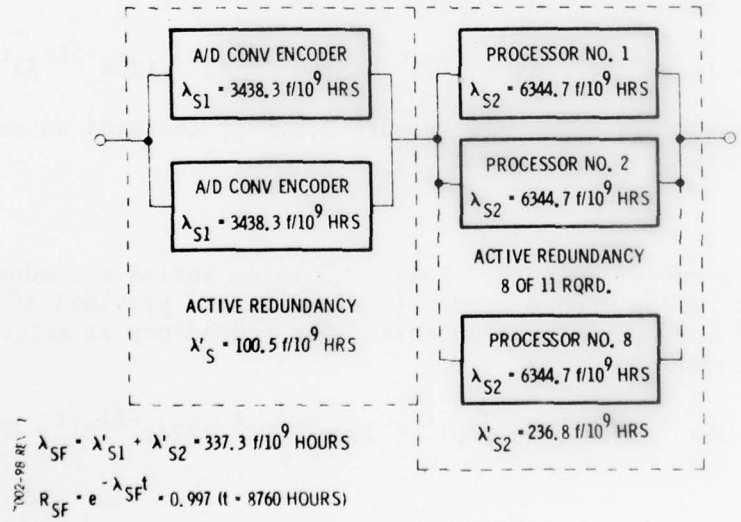


Figure 2.1.5-6. UAR Signal Processor Front End - One year Reliability Math Model

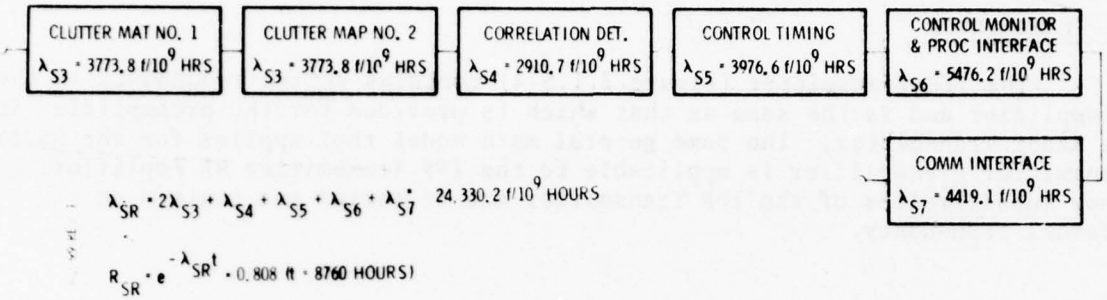


Figure 2.1.5-7. UAR Signal Processor (Less Front End)
Reliability Math model

Signal Processor

The Signal Processor front end (Figure 2.1.5-6) contains active redundancy for the A/D converter encoder and the processor subassemblies. Two A/D converters are provided but only one required for mission success. The math model for the A/D converter is;

$$R_{S1}' = 2e^{-\lambda_{S1} t} - e^{-2\lambda_{S1} t}$$

There are eight processor subassemblies required for full performance operation and eleven are provided. The math model for active redundant processors with eight out of eleven required for success is;

$$R_{S2}' = 165e^{-8\lambda_{S2} t} - 440e^{-9\lambda_{S2} t} + 396e^{-10\lambda_{S2} t} - 120e^{-11\lambda_{S2} t}$$

The signal processor, less front end (Figure 2.1.5-7) contains no redundancy. All parts of this assembly are in series.

Data Processor

The Data Processor (Figure 2.1.5-8) contains series redundant subassemblies. Eight random access memory (RAM) units are provided of which four units are required for operational success. The redundancy is active and the reliability math model is;

$$R_{D1} = 35e^{-8\lambda_{D1} t} - 160e^{-7\lambda_{D1} t} + 280e^{-6\lambda_{D1} t} - 224e^{-5\lambda_{D1} t} + 70e^{-4\lambda_{D1} t}$$

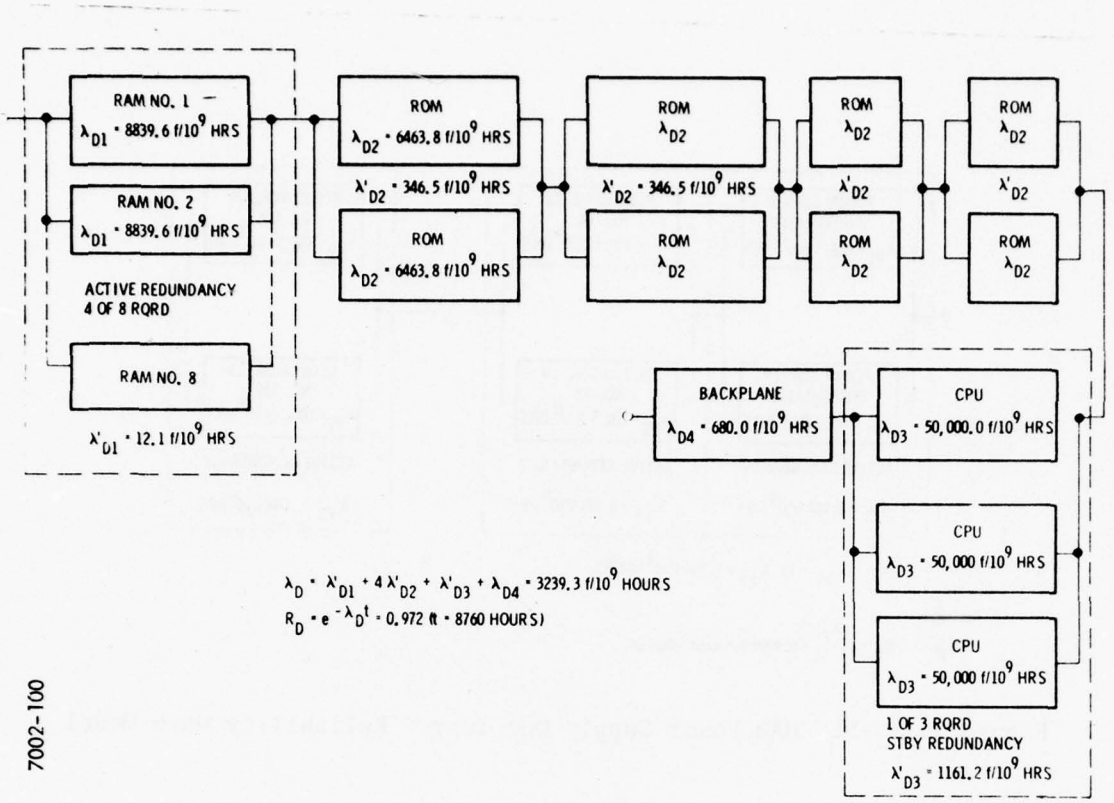


Figure 2.1.5-8. UAR Data Processor One Year - Reliability Math Model

The read only memory (ROM) units are configured in four series dual path active redundant units. The math model for the ROM's is;

$$R'_{D2} = (2e^{-\lambda_{D2}t} - e^{-2\lambda_{D2}t})^4$$

The central processing unit (CPU) is a UYK-30 general purpose computer. Tnis is the only item in UAR that does not use very high quality and reliability component parts throughout its design. Thus the relatively high failure rate of 50,000 f/10^9 hours. In the DP there are three CPU's with one unit required. The two spare redundant units are in standby (deenergized) and the math model is;

$$R'_{D3} = e^{-\lambda_{D3}t}\left[1 + \lambda_{D3}t + \frac{(\lambda_{D3}t)^2}{2}\right]$$

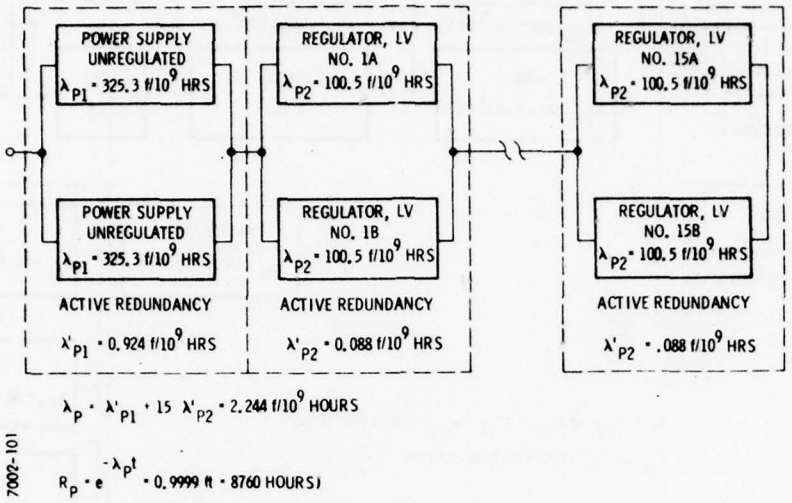


Figure 2.1.5-9. UAR Power Supply One Year - Reliability Math Model

Power Supplies

Active parallel redundancy is provided for the unregulated power supply (low voltage) and for each of fifteen low voltage regulators (see figure 2.1.5-9). The general math model for the 16 redundant elements is;

$$R' = 2e^{-\lambda t} - e^{-2\lambda t}$$

Regardless of the failure rate of the power supply and regulators it is considered necessary to include redundancy throughout the power supply system, since failure or loss of a low voltage (with no redundancy) would be a critical failure mode in the UAR. A critical failure is considered a failure that causes the radar performance to degrade below an acceptable operational level.

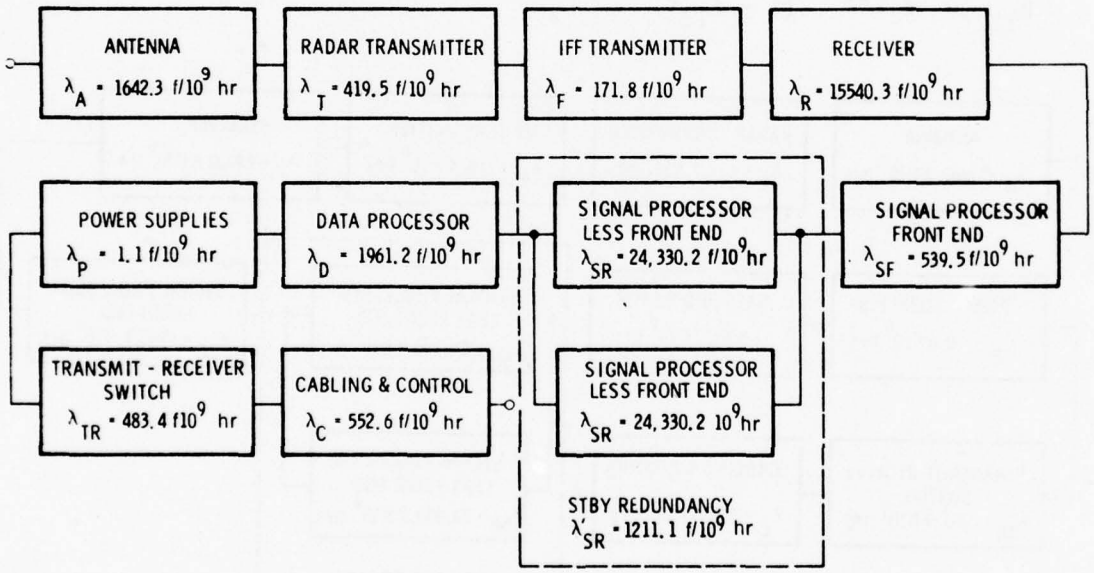
Six Month System

Figure 2.1.5-10 contains the reliability block diagram and math model for a six-month mission of the UAR. As in the UAR one-year model, two signal processors (less front end) are used to provide standby redundancy, and the signal processor math model is;

$$R'_{SR} = e^{-\lambda_{SR}t} (1 + \lambda_{SR}t).$$

Unlike the UAR one-year model, a standby redundant receiver channel is not required. However, a standby redundant synthesizer unit is provided as an additional subassembly of the receiver. The same general math model, as used for the signal processor, applies for the receiver's redundant synthesizers. The UAR signal processor front end one-year model is modified to eliminate one processor subassembly to provide an active redundancy of eight required out of ten available and the processor math model for a six-month mission is;

$$R'_{S2} = 36e^{-10\lambda_{S2}t} - 80e^{-9\lambda_{S2}t} + 45e^{-8\lambda_{S2}t}.$$



$\lambda_{UAR} = \lambda_A + \lambda_T + \lambda_F + \lambda_R + \lambda_{SF} + \lambda'_{SR} + \lambda_D + \lambda_P + \lambda_{TR} + \lambda_C = 22,522.8 f/10^9$ HOURS

$R_{UAR} = e^{-\lambda_{UAR}t} = 0.906$ (t = 4380 HOURS)

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Figure 2.1.5-10. UAR - Six Month - Reliability Math Model

The UAR data processor one-year model is also modified to eliminate two RAM subassemblies to provide an active redundancy of four required from six available, and the RAM math model for a six-month mission is;

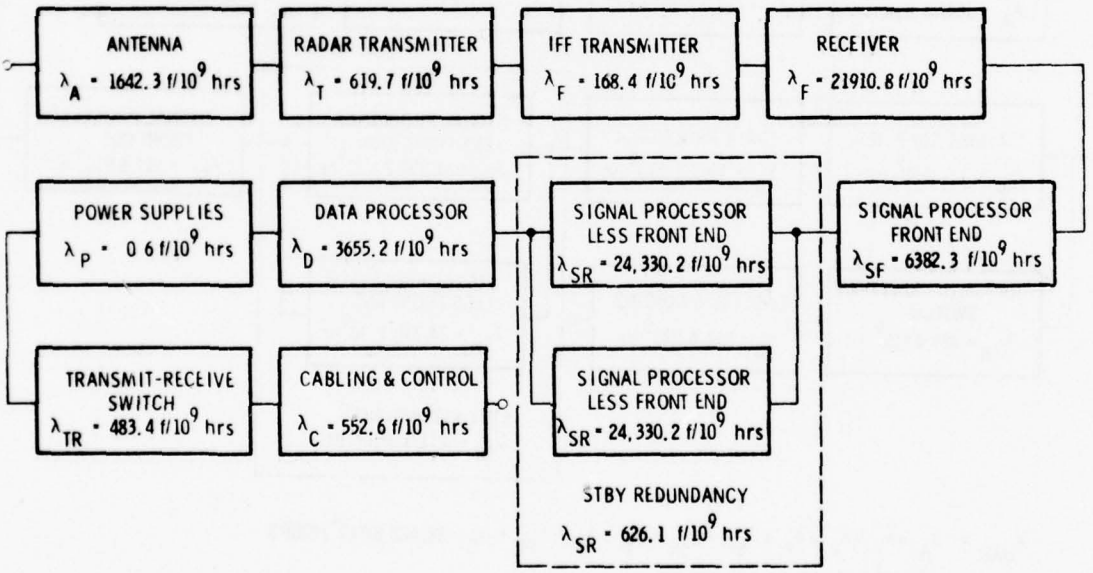
$$R'_{D1} = 10e^{-6\lambda_{D1}t} - 24e^{-5\lambda_{D1}t} + 15e^{-4\lambda_{D1}t} .$$

All other assemblies and all subassemblies of the six-month UAR are the same as the one-year radar and their one-year math models are applicable to the six-month UAR. As indicated in Figure 2.1.5-10, the predicted inherent reliability of the six-month UAR is 0.906.

Three Month System

The predicted inherent reliability for a three-month UAR is 0.924, as shown in the reliability block diagram and math model of Figure 2.1.5-11. The subassemblies used in the three-month UAR are the same as used in the one-year and the six-month radars. However, the quantity of redundant subassemblies is less. In the radar transmitter assembly there is one less driver and final amplifier channel which leaves a standby redundancy of 20 required from 21 available. The math model is;

$$R'_{T3} = e^{-\lambda_{T3}t} (1 + \lambda_{T3}t) .$$



$\lambda_{UAR} = \lambda_A + \lambda_T + \lambda_F + \lambda_R + \lambda_{SF} + \lambda_{SR} + \lambda_D + \lambda_P + \lambda_{TR} + \lambda_C = 36,041.4 \text{ f/}10^9 \text{ HOURS}$

$R_{UAR} = e^{-\lambda_{UAR}t} = 0.924$ (t = 2190 HOURS)

Figure 2.1.5-11. UAR - Three-Month Reliability Math Model

The redundant synthesizer subassembly used in the six-month receiver is not required in the three-month equipment. All items of this receiver are in series. The redundant A/D converter encoder unit is not used in the three-month signal processor front end and only one redundant processor subassembly is used. Having an active redundancy of eight required out of nine available processors in series with an A/D converter encoder, the three-month signal processor front end math model is;

$$R_{SF} = e^{-\lambda_{S1}t} \left(9e^{-8\lambda_{S2}t} - 8e^{-9\lambda_{S2}t}\right) .$$

The three-month DP assembly has one less CPU which provides a standby redundancy of one required from two available and the math model is;

$$R'_{D3} = e^{-\lambda_{D3}t} \left(1 + \lambda_{D3}t\right) .$$

Based upon the predicted reliability of the three-month UAR, it appears that a further reduction of redundant subassemblies can be made.

2.1.6 UAR/Unattended Radar Station Interface

The unique requirements of the UAR and the severe arctic environment impose numerous constraints on the radar station design. While the station design itself was not specifically addressed in the radar study, attention was continuously given to the impact of various approaches on both radar and site requirements. For example, the decision to use frequency scanning as the primary beam steering mechanism is especially attractive in that this conveniently permits locating all active radar elements within a shelter. Only passive radar equipment is exposed directly to the harsh arctic environment.

This section describes various interfaces between the UAR and the station itself. The mechanical configuration is defined for the shelterized active radar elements. Also, the electrically passive components mounted on the antenna tower are identified. The major environmental assumptions are discussed, and radar prime power requirements are listed. Finally, the communication needs are described and some general siting considerations are given.

2.1.6.1 Mechanical Considerations - Shelterized Equipment - All electrically active components are locatable within one site shelter. The principal mechanical characteristics for active elements of the UAR are summarized in Table 2.1-6. The baseline configuration describes minimum equipment needed to perform the radar operation. This configuration contains no redundancy other than that inherent in the design of the transmitter and digital processor. As a result, its predicted MTBF is 4651 hours, which is inadequate for even the three-month maintenance interval design goal. The 12-month configuration lists estimated quantities, sizes, and weights for various items needed to achieve the reliability for one-year unattended operation. The three and six-month configurations use different combinations of various modules and boards. The volume and weight characteristics of these implementations fall within the range defined by the baseline and 12-month configurations. Theoretically, the entire 12-month configuration could be mounted in a single 19" x 26" x 60" equipment rack, although this is not the recommended approach.

As noted in Table 2.1-6, the receivers, exciters and synthesizer are made up of similar size modules. These are all Line Replaceable Units (LRUs) and require no on-site maintenance. Repair of failed modules will be performed either at the maintenance node or at a central depot depending on the type of failure. The radar and IFF transmitters utilize replaceable transistor modules. These modules are automatically monitored and electronically switched in event of a failure. Similarly, the signal and data processor boards, consisting primarily of digital logic, contain their own fault monitoring and automatic switching circuitry. Failed boards are replaced by the maintenance team, again with no repairs performed at the site. The antenna/transmit/receive switch is functionally two switches connected back-to-back. This is depicted in the radar block diagram of Figure 2.1-13. A SP13T switch provides the switching between the 12 line arrays, or IFF horns, and

TABLE 2.1-6. WEIGHT AND VOLUME BREAKDOWN FOR UAR ACTIVE ELEMENTS

Item	Description	Dimensions, inch	Baseline Configuration			12-Month Configuration		
			No.	Vol, ft^3	Wt, lb	No.	Vol, ft^3	Wt, lb
Radar Receiver, RF	Modules	2 x 4 x 8	2	0.08	4.8	4	0.16	9.6
Radar Receiver, IF	Modules	2 x 4 x 8	1	0.04	2.0	2	0.08	4.0
IFF Receiver	Modules	2 x 4 x 8	1	0.04	2.3	2	0.08	4.6
Radar Exciter	Modules	2 x 4 x 8	1	0.04	2.5	2	0.08	5.0
IFF Exciter	Modules	2 x 4 x 8	1	0.04	2.2	2	0.08	4.4
Synthesizer	Modules	2 x 4 x 8	3	0.12	6.0	6	0.24	12.0
Radar Transmitter	Assembly	18 x 18 x 10	1	1.88	40.0	1	1.88	40.0
IFF Transmitter	Assembly	3 x 5 x 6	1	0.05	5.0	1	0.05	5.0
Signal Processor	Boards	14 x 15 x 2.5	18	5.47	94.0	30	9.12	156.7
Data Processor	Boards	5 x 8 x 1	11	0.30	25.0	24	0.65	55.5
Antenna/Transmit/Receive Switch	Stripline Board	24 x 24 x 6	1	2.00	15.0	1	2.00	15.0
Power Supplies	Modules	8 x 12 x 12	1	0.67	20.0	2	1.34	40.0
		Totals		10.73	218.8		15.76	351.8

the omni antenna. The SP4T switch performs the switching between the radar and IFF transmitter and receivers. (For the 12-month configuration this will be a SP6T switch; however, this will not result in a substantial change in the size and weight of the switch.) Maintenance of the switch will consist of PIN diode module replacement. Dual power supplies will be employed and again maintenance will involve module replacement only. In addition to the items listed in Table 2.1-6 a BITE/Fault Monitor/control panel may also be desirable. This would only be used during visits by maintenance personnel to facilitate system checkout and module replacement. While various features can be incorporated into this panel, the size and weight impact on the station design will probably be insignificant.

In addition to the active elements described above, the shelter must also accommodate inputs from the waveguide runs to the antenna. These consist of 13 L-band guides which will connect directly to the Ant/Xmt/Rcv switch. For simplicity in making this connection, reduced size waveguide may be preferable. Waveguide or coax cables will also connect the switch to appropriate receiver and transmitter assemblies. Furthermore, an L-band/IFF diplexer will be required for the omni antenna feedline.

2.1.6.2 Mechanical Considerations - Tower Mounted Equipment - All tower mounted equipment, which is exposed to the arctic environment, is passive and highly reliable. Excluding the required communication equipment, there are

13 L-band waveguide runs from the shelter to the top of the tower. One of these guides feeds directly into the omni antenna. Each of the other 12 waveguides feeds a passive, L-band/IFF diplexer. The diplexer directs radar L-band energy to one of the 12 line-feed arrays of the main radar antenna. The IFF energy, on the other hand, is directed to one of the 12 IFF horns.

The hexagonal antenna structure is illustrated in Figure 2.1-10. The six solid reflectors are each eight feet high by 30 feet long, and the line-feed arrays are 26.7 feet long. The 12 IFF horn antennas are mounted on a platform about 14 feet above the top deck of the tower. Directly above the IFF horns is the omni antenna. Communication antennas are depicted on a mast above the omni. Depending on the actual tower height and masking conditions, it may be possible to mount the communication antennas on the tower itself, below the main radar reflectors. In many, and perhaps all of the site locations, a radome may not be required. However, if it is determined to be necessary, a 67 foot diameter radome will accommodate this configuration.

An alternate antenna configuration is shown in Figure 2.1-11. The main antenna reflectors are placed back-to-back in a tri-form arrangement. The reflector and array dimensions are the same as before. This configuration has a number of structural advantages. The reflector support structure can be stronger and lighter. The arrays can be fed from the center, eliminating waveguide runs to the antenna periphery required in the hexagonal arrangement. Also, the weight has been shifted from the edges of the tower platform toward the center of the tower. While a square tower and platform are illustrated in the figures, there is no requirement for this type of structure. If an existing tower can conveniently be used, this may be the most cost-effective approach. However, if a new tower is to be designed, a triangular tower would be preferable.

The IFF, omni, and communication antennas are installed in the same manner as described for the hexagonal arrangement. A radome structure, if required, could be much smaller, in that cylindrically shaped radomes could be used for each of the three reflector structures. Depending on the location of the communication antennas, a small spherical radome could be placed over the IFF and omni antennas.

Weight estimates for these two antenna configurations and for the waveguide runs up the tower are summarized below:

Hexagonal Arangement	5692 lbs
Tri-Form Arrangement	5087 lbs
Vertical Waveguide (100' Tower)	2570 lbs
Vertical Waveguide (150' Tower)	3855 lbs.

These estimates are for the antenna and waveguide components only and do not include the weight of radomes or tower/platform. It should be noted that the hexagonal arrangement will require a substantially heavier platform than that of the tri-form arrangement.

2.1.6.3 Environmental Considerations - The principal environmental consideration is controlling the temperature of the shelterized equipment. Housing all active electronic radar equipment within a shelter is recommended both to facilitate system maintenance and also to provide a more stable ambient temperature to prevent reliability degradation. Classically the major temperature problem affecting reliability has been associated with high temperatures. In fact, MIL-HDBK-217B makes the unequivocal statement, "Of course, lower temperatures produce better reliability..." while adding that additional cooling may impact the system environmental loading capacity. Another, less well-defined consideration is associated with the effects of temperature cycling on system reliability. There are indications that such cycling, even within the designed temperature range, may significantly degrade component reliability. However, it also appears that not only the extent of the temperature variation but also frequency of the cycling must be considered in determining the possible reliability degradation. Apparently, rapid temperature fluctuations are far more deleterious than slower variations over the same temperature range. As a consequence, it is recommended that shelter temperature be kept constant within approximately $\pm 15^{o}C$. Greater long-term variations, such as summer-winter cycling, may be acceptable; however, this needs to be verified.

Assuming that temperature can be maintained within about $30^{o}C$, an acceptable region in terms of reliability considerations is from $-5^{o}C$ to $+25^{o}C$. Clearly, a detailed thermal analysis of the shelter and energy available for environmental control is needed to determine the feasibility of maintaining these temperatures. For example, there will be approximately 400 watts of power dissipated by the radar within the shelter. For a heavily insulated shelter, this could make a significant contribution to temperature control.

Another possible consideration involves the use of heat pipes similar to those used along the Alaskan pipeline. These heat pipes, which also serve as supports for the oil pipeline, draw heat from the permafrost during cold weather. This causes the ground to freeze solidly, anchoring the supports in place. This process is repeated each winter so that the ground remains permanently frozen during the summer. For application to the UAR, the heat pipe radiators could be installed within, or built into, the radar shelter. During very cold weather the heat pipes would draw heat from the ground up into the shelter. Since the permafrost temperature usually remains constant at about $0^{o}C$, this could assist substantially in moderating the extremely low temperatures that often occur in the Arctic.

Avoiding high temperatures should not be a major problem. If, however, it is feasible to sufficiently insulate the shelter so that the dissipated heat of the radar provides adequate heat during the winter, then some means must be adopted to prevent possible overheating during warm weather. The shelter could have automatic or operator controlled air vents, for example. Furthermore, it is obvious that for minimum power consumption the equipment in the shelter should be located so that fans or blowers will not be required.

Another environmental consideration, which may vary significantly depending on the site, is that of humidity control. The major problem that can be expected here is water condensation in the waveguides. It may be necessary at some site locations to use desiccant bottles to prevent this from occurring. Similarly, the use of drying agents within the shelter may be called for at some installations.

2.1.6.4 Power Requirements - In accordance with the goals of the UAR design study, the prime power available for the radar is assumed to be about 500 watts of dc power. The estimated power consumption for the ITTG UAR design is 518.5 watts. In the design study statement of work there was no specification for the voltage level of the input power or its degree of regulation. Consequently, dc to dc converters and regulators were considered necessary to provide the five voltages used by the radar, viz., +28, ±15, ±5V. Efficiency of the power supplies was estimated at 80 percent with the result that slightly over 100 of the available 500 watts are dissipated in the supplies. This could be reduced by nearly 50 watts if the input power is say, 28V regulated dc. This is the operating voltage required for the UAR transmitter, which consumes nearly half of the UAR power. Of course, depending on the prime power source design, this could simply shift efficiency loss from the radar to the prime power supply itself with no significant net gain for the system.

Dual power supplies are recommended for UAR because of the high reliability requirements of the radar. It may be necessary to use two separate prime power supply/buses to ensure that reliability of the prime power is compatible with that of the radar. For this arrangement, one of the radar power supplies could be dedicated to each bus, or, if more reliability is needed, separate supplies could be switched to either of the two buses.

The radar has been designed for minimum on-site maintenance; however, it is possible that certain failures could require the use of test equipment such as signal generators and oscilloscopes. As a consequence, it is desirable that ac power be available as well. This power would not be needed by the radar during normal operation and could be activated by the maintenance team.

2.1.6.5 Communication Requirements - The UAR was designed to operate with a narrowband data link, and, as a consequence, its communication requirements are very modest. The UAR design study did not specifically address the site communication problem. The main consideration was to ensure compatibility with a narrowband (2400 bits per second) data link. Such a link is more than adequate for reporting UAR track data. For example, track reports of 20 targets updated every frame time of six seconds would permit use of over 700 bits for each track - nearly an order of magnitude more than required. Obviously there are other considerations. A spare data channel would probably be required for the sake of reliability. In addition, use of a separate channel to perform radar and site fault monitoring and reconfiguration control may be more satisfactory than sharing the radar data channel. A voice channel may also be desirable to facilitate communication between the site and maintenance node during visits by maintenance personnel. Presumably, fault monitoring and voice channels could be shared by all the sites in a particular string, since the data rate requirements are low.

It is assumed that line-of-sight microwave links will provide the principal means of communication between adjacent sites and with the maintenance nodes. This will require elevated microwave antennas to ensure line-of-sight propagation between sites. As shown for example, in Figures 2.1-10 and 2.1-11, the main radar antenna tower can also support these communication dishes. Whether these antennas need to be mounted above the radar reflectors as shown, or whether they can be mounted directly to the tower below the radar antenna reflectors, depends upon specific site spacing and masking conditions. The use of other means of communication, such as troposcatter or direct satellite transmissions, will impose no special constraints on the radar design or its communication interface.

2.1.6.6 General Siting Information - Perhaps the most important siting consideration involves optimum use of available terrain for detecting low flying targets. Low flyer detection is greatly impacted by the presence of multipath since signal levels are drastically reduced from targets near the radar horizon. Increasing the height of the radar antenna extends the radar horizon and improves the received signal levels; compare Figures 2.1-3 and 2.1-5, for example. It is therefore advantageous to utilize existing high ground in order to reduce height requirements of the antenna tower. On the other hand, the site must be readily accessible to helicopter-borne maintenance teams. This may require the construction of a helicopter pad reasonably near the site and may possibly eliminate the use of sites which would otherwise be ideal.

In certain locations, terrain features may be such that adequate coverage can be obtained without an antenna tower. Nevertheless a certain minimum tower height must be assumed. Ignoring local terrain features, which may produce some masking, the principal requirement is that the antenna be sufficiently high to avoid blockage by the radar shelter. Moreover, the shelter itself will probably be elevated both to avoid snow buildup problems and to facilitate site security control. As a consequence, minimum tower height should be between approximately 15 and 25 feet. The actual value is not critical and should be established so as to minimize impact on tower design and construction.

2.2 UAR ANTENNA DESIGN*

2.2.1 Subsystem Requirements

The antenna for the UAR application must emphasize high reliability, low life cycle cost, low prime power dissipation, and must be capable of meeting the performance goals.

Table 2.2-1 shows requirements for the two-dimensional UAR antenna, based on overall system performance goals. The high antenna gain dictates the need for a narrow 1.5-degree azimuth beamwidth, and for dual elevation beams to cover the -10-degree to 50-degree elevation sector.

Remaining performance parameters meet the needs of the overall system. A signal bandwidth of 750 kHz is based on the chirped pulse waveform, and requires an antenna that is capable of achieving a somewhat broader bandwidth. Fortunately, the pulse spectrum is expected to fall off very rapidly beyond the 750 kHz band, eliminating need for the usual 2 or 3:1 ratio in antenna-to-pulse-spectrum bandwidth.

TABLE 2.2-1. UAR ANTENNA REQUIREMENTS

Gain	27 dB
Frequency	1215-1400 MHz
Coverage (az/el)	360^{o}/-10^{o} to 50^{o}
Azimuth Beamwidth	1.5^{o}
Azimuth Accuracy	0.5^{o}
Number of El Beams	2
Sidelobe Level	-30 dB
Signal Bandwidth	750 kHz
Prime Power	30 Watts
RF Power (Peak)	2 kW
Reliability (MTBF)	160,000 hours (minimum)
Maintainability (MTTR)	0.5 hour

*The antenna discussion and trade-offs in Sections 2.2.1 and 2.2.2 are based on the use of a 40' long antenna aperture. See Sections 2.1.2 and 2.1.5 for a discussion of the selection of a smaller aperture.

Key requirements on the antenna as well as the overall system are high reliability, low maintainability, and low prime power dissipation. The budgeted antenna reliability is about 160,000 hours mean-time-between-failures (MTBF). This high reliability is desirable without a major amount of redundancy or other unusually expensive techniques in deference to the low life-cycle cost goal. Furthermore, maintenance costs must be kept to a minimum by minimizing the number of spare parts required, and simplifying repair of the more expensive units.

Also required by the system is low prime power dissipation of 30 watts budgeted to the antenna. Thus, the number of RF switches/phase shifters must be either minimized, or they must be designed to operate with a lower dissipation than the typical L-band devices. Additional requirements on the antenna are low maintenance time and environmental performance. The 0.5 hour mean time to repair (MTTR) dictates a need for easily accessible parts and very few operations during their replacement. Environmental conditions are those typically occurring in the arctic regions. These conditions are particularly important for this antenna design since operation without a radome is desirable, particularly when the antenna sizes dictate radomes that may approach over 80 feet in diameter, and radar siting factors may require antenna towers up to 150 feet in height.

2.2.2 Antenna Tradeoff Studies

2.2.2.1 Basic Configurations Studied - Elementary forms of a multiple-faced cylindrical reflector fed by linear arrays, and a circular reflector fed by a ring array will be compared. Two classes of antennas were evaluated in detail during the study program. The first consisted of several faces of a cylindrical reflector fed by scanning line arrays. Two line arrays were chosen to provide the multiple beams in elevation; additional beams were not necessary to meet the gain requirements and could conceivably cause aperture blocking due to the additional line array. The second class consists of circular ring arrays feeding a circular reflector which forms the two beams in much the same manner. Although a frequency scanning approach is obviously less expensive, scanning with phase shifters will be considered first because of their frequency diversity, ECCM and signal bandwidth advantages.

Scanning 360 degrees with the line arrays is accomplished by a combination of phase scanning over a sector with the individual arrays and switching to the other arrays for the remaining portion of the 360 degrees. With the circular arrays, scanning is accomplished mainly by sequencing the excited portion of the ring around the entire ring, in one element increments.

Both of these techniques have a reasonably small number of active components as required by the cost, reliability, maintainability, and power dissipation budgets. Other antenna techniques, such as planar arrays, the "Dome" array, or scanning lens arrays are expected to fall short of these goals and have not been evaluated.

Figures 2.2-1 and 2.2-2 show possible switching arrangements for these approaches. Both arrangements dictate a centralized feed network with transmission lines running to the radiating elements located in front of their respective reflectors to form the elevation beams. Only one of the elevation beams is shown to be formed by these feeds for simplicity. The formation of the second beam will be discussed later.

The linear array (Figure 2.2-1) consists of a simple series feed network which couples into phase shifters. The power is then switched in total to one of the faces. Six faces are shown since it minimizes the number of components, as discussed later. With this approach, eight PIN diodes are required for each phase shifter, and two PIN diodes for each leg of the SP6T switch (one for each element). This achieves adequate redundancy and graceful degradation.

The circular array is also fed by phase shifters and switches. In operation, only one sector of the circle, (a quadrant in this case), is excited which forms a beam normal to the center of the sector. Scanning is accomplished by sequencing the illumination around the circle, one element at a time. The SP4T switches provide this sequencing function, however the phase shifters and amplitude sequencer are required to preserve order of the illumination function. The operation of the amplitude sequencer is discussed in more detail below. Eight PIN diodes are required for both the phase shifters and the SP4T switches. The amplitude sequencer requires two PIN diodes for each output port.

2.2.2.2 Comparing Basic Configurations - Basic configurations discussed in the previous subsection are compared in size, number of components, and accuracy. The following tables compare the basic scanning line feed and circular array antennas as discussed in the previous subsection. Line feed arrays having 3, 4, 5, and 6 faces are compared with cylindrical arrays made up of both 3 and 4 sectors (a 120-degree or a 90-degree sector).

Table 2.2-2 gives pertinent performance features, such as required element spacing, and beamwidth and gain variation with scan angle. Tables 2.2-3, 2.2-4, 2.2-5 and 2.2-6 compare the antennas based on three different design criteria: equal performance optimized at beam normal, equal beamwidth at maximum scan angle, and equal gain at maximum scan angle. Equal performance at beam normal case is included for reference but is not considered a viable approach. Either of the other two criteria may be acceptable, depending on the design margin. Six different antenna types and three design criteria result in eighteen different antennas that are compared. The first design comparison table (Table 2.2-3) shows the required size of the individual arrays. This is the overall extent of the excited portion of the radiating array feed and is used to obtain the remaining parameters. Table 2.2-3 also includes a comparison of the overall diameter of the complete antenna system. Table 2.2-4 compares the total number of radiating elements required, and the number of PIN diodes required. This comparison is for linear and circular arrays as discussed up to this point.

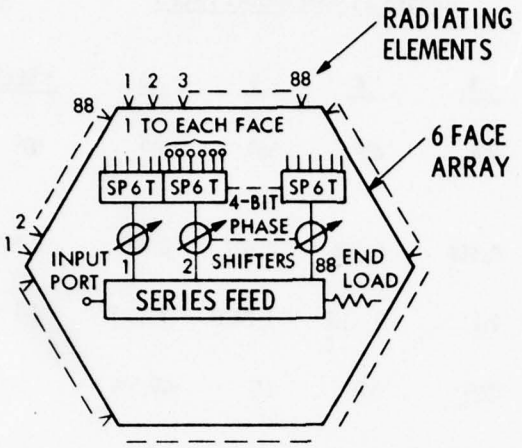


Figure 2.2-1. Basic Linear Array Approach

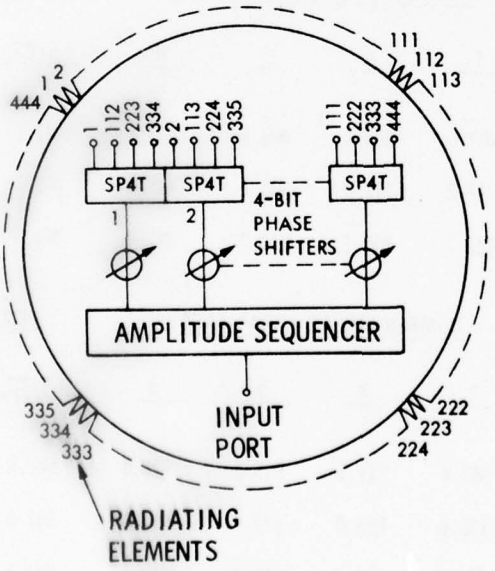


Figure 2.2-2. Basic Circular Array Approach

TABLE 2.2-2. PERFORMANCE FEATURES OF VARIOUS ANTENNA CONFIGURATIONS

PERFORMANCE FEATURES	NUMBER LINEAR ARRAY FACES 3	4	5	6	CYL ARRAY 3 SECT.	4 SECT.
MAX SCAN	60^0	45^0	36^0	30^0	60^0	45^0
MAX EL SPACING (WAVELENGTH)	0.519	0.566	0.607	0.641	0.519	0.566
ΔAZ BW MAX	2:1	1.41:1	1.24:1	1.15:1	1:1	1:1
MAX. REFL. PWR	11%	3%	1%	≤0.5%	---	---
ΔGAIN MAX dB	-3.5	-1.6	-1.0	-0.6	---	---

7002-49

TABLE 2.2-3. SIZE COMPARISON OF VARIOUS ANTENNA CONFIGURATIONS

INDIVIDUAL ARRAY SIZE (INCHES)	NUMBER LINEAR ARRAY FACES 3	4	5	6	CYL ARRAY 3 SECT.	4 SECT.
1.5^0 AND 27 dB @0^0 SCAN	408.6	408.6	408.6	408.6	491.7	476.5
1.5^0 @ MAX. ∢	817.2	577.8	505.1	471.8	491.7	476.5
27 dB @ MAX. ∢	918.2	595.7	510.2	471.9	491.7	476.5

TOTAL OVERALL CIRCLE DIM. (INCHES)	NUMBER LINEAR ARRAY FACE 3	4	5	6	CYL ARRAY 3 SECT.	4 SECT.
1.5 AND 27 dB @0^0 SCAN	663.8	713.6	813.8	928.1	567.8	673.8
1.5@ MAX. ∢	1135.6	953.0	977.9	1054.5	567.8	673.8
27 dBI @ MAX. ∢	1252.2	978.2	986.6	1054.5	567.8	673.8

7002-50

TABLE 2.2-4. COMPARISON OF NUMBER OF COMPONENTS OF VARIOUS ANTENNA CONFIGURATIONS

NO. ELEMENTS TOTAL	NUMBER LINEAR ARRAY FACES 3	4	5	6	CYL ARRAY 3 SECT.	4 SECT.
1.5° & 27 dBI @ 0° SCAN	282	344	400	456	408	444
1.5 @ MAX ∢	561	484	495	528	408	444
27 dBI @ MAX ∢	630	500	500	528	408	444

NUMBER OF DIODES	NUMBER LINEAR ARRAY FACES 3	4	5	6	CYL ARRAY 3 SECT.	4 SECT.
1.5° BW & 27 dBI @ 0° SCAN	1316	1376	1440	1520	2176	1998
1.5° BW @ MAX ∢	2618	1936	1782	1760	2176	1998
27 dBI @ MAX ∢	2940	2000	1800	1760	2176	1998

ASSUMES 1 ARRAY WITH SPNT SWITCHES FOR EACH FACE

$$NTOT \left[2 + \frac{8}{NF} \right]$$

AMPLITUDE SEQUENCER TECHNIQUE

$$NTOT \left[\frac{8+2}{NSEQ} + 2 \right]$$

7002-51

Table 2.2-5 compares the number of PIN diodes for linear arrays made up of a new integrated variphase/coupler device. These two approaches are shown in Figures 2.2-3 and 2.2-4. The variphase/coupler technique is essentially a series feed device with coupling phase controlled by diodes. Only four PIN diodes are required for each output, thereby saving half the number usually required for normal phase shifters. However, performance is limited due to its phase accuracy and inherent amplitude error. It is included here because these drawbacks may be overcome with future research.

Table 2.2-6 compares azimuth error caused by scanning with a line feed reflector for both single beam case and dual beam case. This error occurs from the inherent scanning characteristics of a linear array. The beam shape is actually conical rather than the desirable planar shape

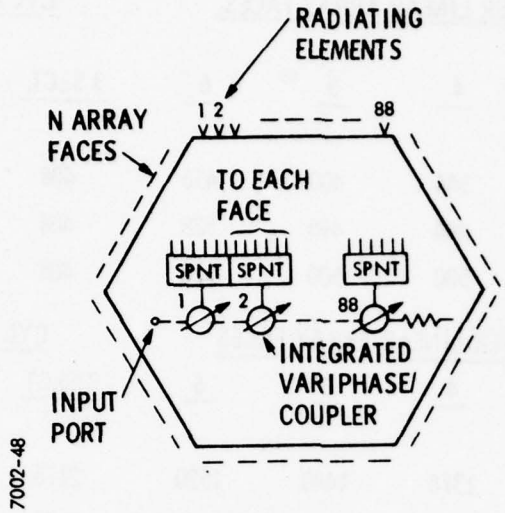


Figure 2.2-3. One Variphase/Coupler Element with SPNT Switches for Each Face

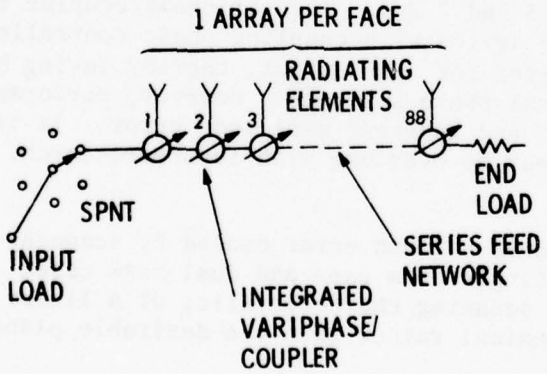


Figure 2.2-4. One Variphase/Coupler Array Per Face

TABLE 2.2-5. COMPARISON OF NUMBER OF PIN DIODES WITH VARIOUS VARIPHASE/COUPLER CONFIGURATIONS

NUMBER DIODES	NUMBER OF LINEAR ARRAY FACES				
	3	4	5	6	
1.5^0 BW & 27 dB GAIN @ 0^0 SCAN	1128	1376	1600	1824	4 NTOT
1.5^0 BW @ MAX $\sphericalangle$	2244	1936	1980	2112	
27 dBI @ MAX $\sphericalangle$	2520	2000	2000	2112	

ASSUMES 1 VARIPHASE COUPLER ARRAY ON EACH FACE

NUMBER DIODES	NUMBER OF LINEAR ARRAY FACES				
	3	4	5	6	
1.5^0 BW & 24 dB GAIN @ 0^0 SCAN	740	1032	1120	1216	$NTOT\left[2+\frac{4}{NF}\right]$
1.5^0 BW @ MAX $\sphericalangle$	1870	1452	1386	1408	
24 dBI @ MAX $\sphericalangle$	2100	1500	1400	1408	

ASSUMES 1 VARIPHASE COUPLER ARRAY AND SPNT SWITCHES FOR EACH FACE

7002-52

occurring in the cylindrical array. Thus, as the azimuth angle increases off the array normal, azimuth error for the larger elevation angle also increases. The following relationship is tabulated for azimuth angle error:

$$\Delta az = \sin^{-1}\left[\sin az_0 \cos el_0/\cos el\right] - az_0$$

where:

az_0 is desired azimuth angle,

el_0 is elevation angle where the error is made zero, and

el is actual elevation angle.

Table 2.2-6 assumes the error is made zero at the horizon, and at 25 degrees for the upper beam in the 2-beam case. Although these errors are major drawbacks of a linear array antenna system, they can be reduced to under two degrees up to about 40 degrees elevation for the six-face array case with

TABLE 2.2-6. COMPARISON OF AZIMUTH ERROR WITH VARIOUS LINEAR ARRAY CONFIGURATIONS

SINGLE BEAM AZ ERROR (MAX DEG)	NUMBER LINEAR ARRAY FACES 3	4	5	6
10^0 EL ANGLE	1.6^0	0.9	0.6	0.5
20^0	7.2	3.8	2.7	2.1
30^0	30.0	9.7	6.7	5.3
40^0	NO BEAM	22.4	14.1	10.7
55^0	NO BEAM	NO BEAM	NO BEAM	30.7

2-BEAM AZ ERROR (MAX DEG) (UPPER BEAM ERROR)	NUMBER LINEAR ARRAY FACES 3	4	5	6
25^0 EL ANGLE	0	0	0	0
30	5.0	2.7	2.0	1.6
40	NO BEAM	11.8	8.1	6.3
55	NO BEAM	NO BEAM	32.2	22.2

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two beams by proper optimization of el_0. They can be further reduced by taking advantage of overlapping coverage from an adjacent face.

Figure 2.2-5 shows how the beam shapes overlap. Dual-beam arrays and six array faces are assumed. If a target's true angle were 30 degrees, an average of the two antenna readings would reduce the error to zero. For other true target angles, a more complex algorithm must be used. However, a major reduction in errors in the table can be effected. Since these errors may still be significant, a six-face configuration is selected as the optimum linear array configuration.

The six-face array is nearly optimum in most respects. It has the minimum number of PIN diodes, is only 10 percent larger in diameter than the smallest linear array, and is nearly constant in gain with scan angle. A circular array with a four-sector feed, although smaller in overall diameter,

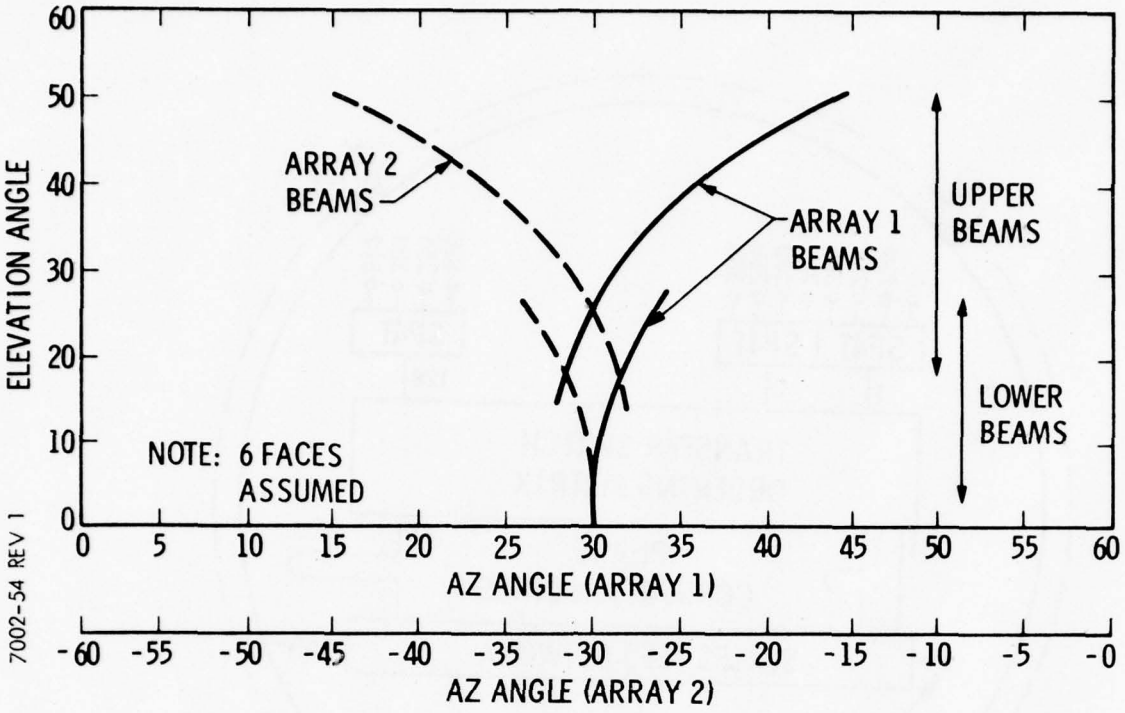

Figure 2.2-5. Overlapping Beams From Adjacent Dual Beam Arrays

has more PIN diodes and accompanying drivers and associated dissipation. Therefore, both the six-face linear array configuration and four-sector circular array are optimized in more detail in following subsections. The four-sector circular array has been selected over the three-sector since it is expected to have better pattern performance with the circular reflector.

2.2.2.3 Optimized Circular Array Without Phase Shifters - An optimized reflector-fed circular array which uses a transfer matrix instead of an amplitude sequencer and phase shifters is shown to be unsuitable for UAR. Before discussing optimized circular array with amplitude sequencer, a more common network feed will be discussed for reference. This network, shown in Figure 2.2-6 uses a transfer matrix to sequence the amplitude and phase, thus avoiding the need for phase shifters. In operation, with a single beam, element numbers 1 through 128 will first be excited by the SP4T switches. The illumination amplitude will be tapered for low sidelobes and the phase will correct for the circular shape. The first SP4T switch will then sequence to element number 129; since the illumination amplitude and phase have lost their order, the transfer switch ordering matrix must be used to correct it. In theory, this arrangement appears simple enough, and avoids the need for phase shifters. However, the transfer matrix is actually quite a complicated device for this application. Figure 2.2-7 shows a transfer switch matrix designed for a 64-output port and 8-input port application. Figure 2.2-8 shows the individual switch schematic. With this device, any input port can go to any output port. For our application, 128 outputs and

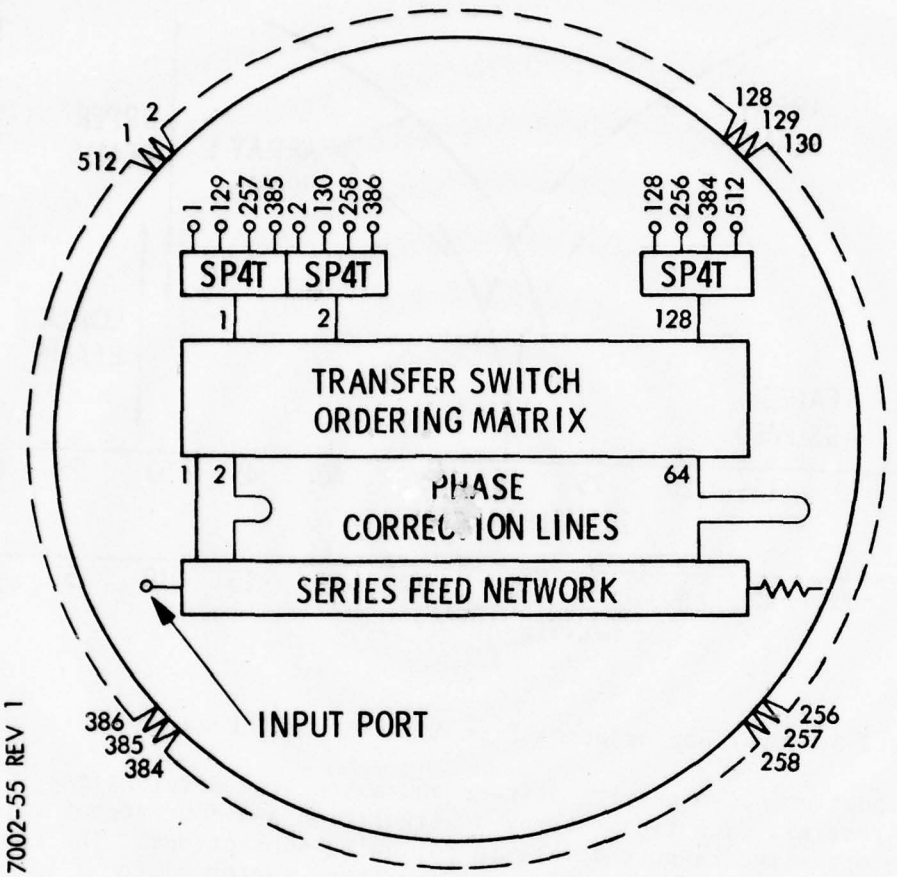

Figure 2.2-6. Circular Array Without Phase Shifters

64 inputs are required. The number of array elements must be increased to 512 due to the binary nature of the device. The resulting number of transfer switches is 384 with six switches in any one series path. This requires 768 PIN diodes in the transfer switch matrix, for a total number of 1792. For the 2-beam case, SP8T switches and two series feeds are used for a total of 2944 PIN diodes. Although the number of diodes is competitive, the number of total components is not, since numerous coax runs between switch modules will assuredly be required. Furthermore, reliability will be poor, and total RF loss will be about 6.4 dB.

2.2.2.4 Optimized Circular Array With Amplitude Sequencer - The reflector-fed circular array which uses an amplitude sequencer is optimized, and its performance features are summarized. Figure 2.2-9 shows a more optimized version of the single beam circular array feed network which was used for Tables 2.2-2 through 2.2-6. It consists of 112 4-bit phase shifters and an amplitude sequencer with 28 outputs which are divided into 112 ports

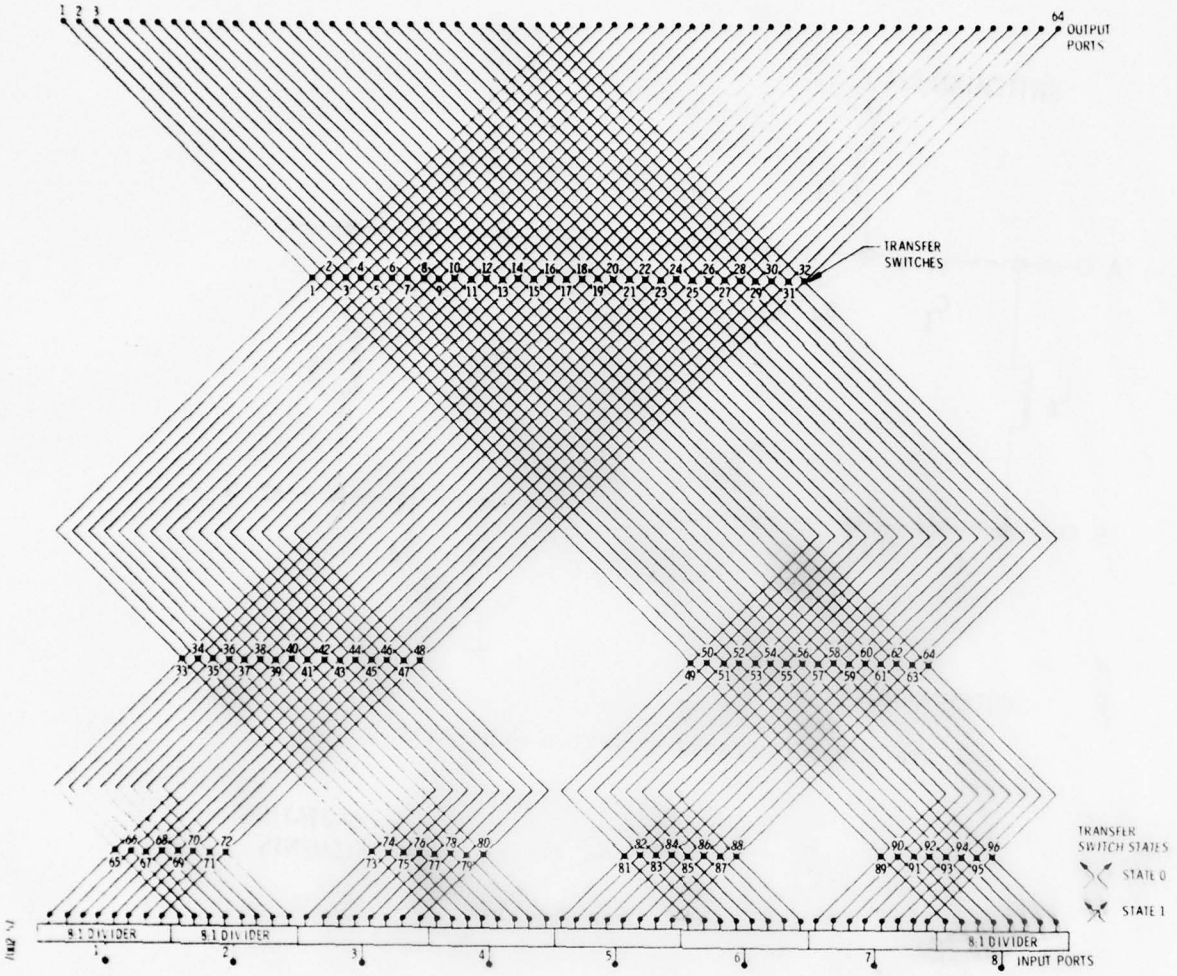

Figure 2.2-7. Transfer Switch Ordering Matrix

with 4:1 dividers. Operation is similar to that of the above circular array without phase shifters (see Section 2.2.2.3). However, since the amplitude sequencer can only provide the sequencing function for amplitude, separate phase shifters are required. They must be variable phase shifters since their position can occur anywhere in the excited portion of the circle, such as on the edge, or in the center. Separate control of phase for every element is required, whereas control of amplitude can be quantized into groups of four equal sub-arrays by the 4:1 dividers. The amplitude sequencer is a low-loss, multimode section of coaxial waveguide that has been produced for many TACAN circular arrays. Figure 2.2-10 shows a block diagram of the device;

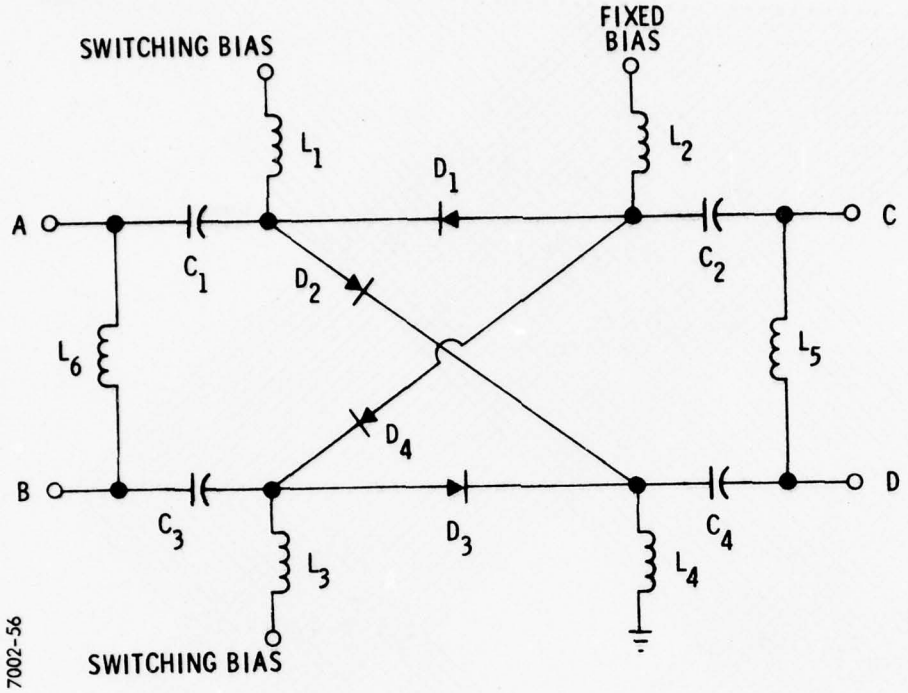

Figure 2.2-8. Transfer Switch Schematic

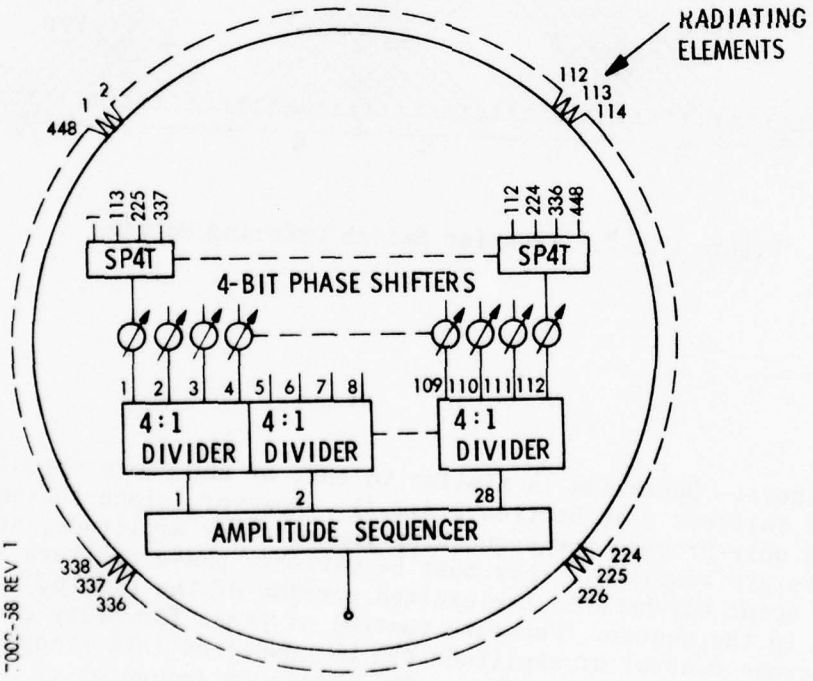

Figure 2.2-9. Circular Array With Phase Shifters

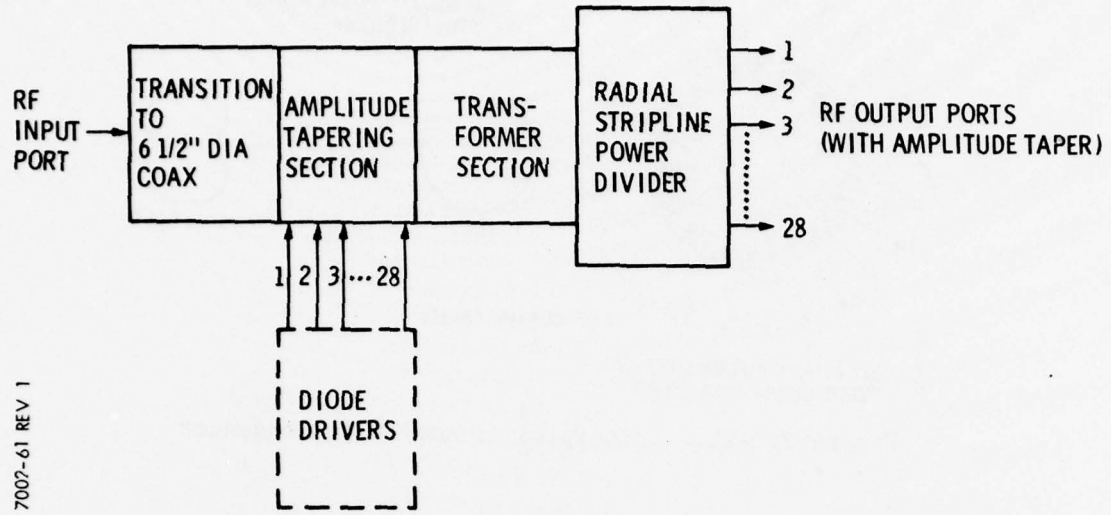

Figure 2.2-10. Amplitude Sequencer Block Diagram

Figure 2.2-11 shows the principle of operation; and Figure 2.2-12 is a drawing of the device used for the TACAN application. A slight modification will be required for this application.

The number of PIN diodes required in the amplitude sequencer is 56, resulting in an overall total of 1848. For the dual-beam case, two rings of elements must be used; this is accomplished by using SP8T switches in place of the SP4T switches. The phase shifters must be adjusted differently for the upper and lower beams. Thus the PIN diode total for dual beams is 2744. Figure 2.2-13 shows the phase shifter/SP8T module.

An overall view of the circular array on a tower is shown in Figure 2.2-14. The reflector shape is similar to that of a shaped reflector revolved about an axis, 24 feet from the center. The upper and lower ring feeds provide the lower and upper beams respectively, similar to that of a dual horn reflector. The following lists show expected RF losses and prime power dissipation.

Circular Array Insertion Loss

Component	Loss
Amplitude Sequencer	0.3 dB
Short Transmission Lines (Air Coax)	0.25 dB
Long Transmission Lines (Air Coax)	0.75 dB
4:1 Power Dividers	0.3 dB
4-Bit Diode Phase Shifters	1.2 dB
SP8T Switches	1.5 dB
Total Loss	4.3 dB

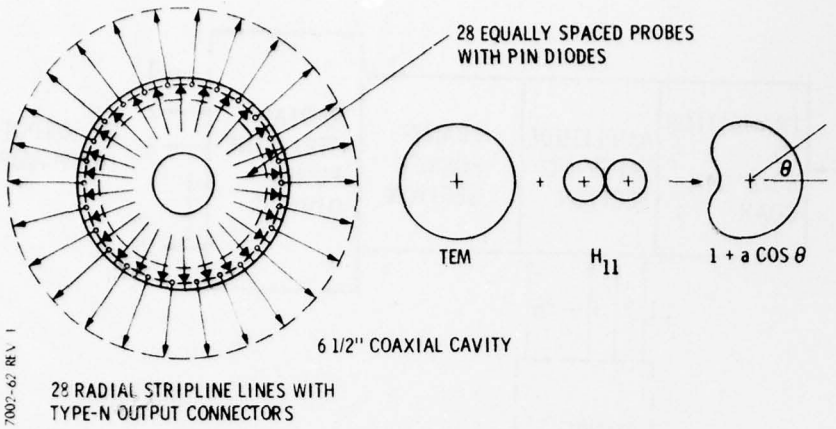

Figure 2.2-11. Principles of Amplitude Sequencer

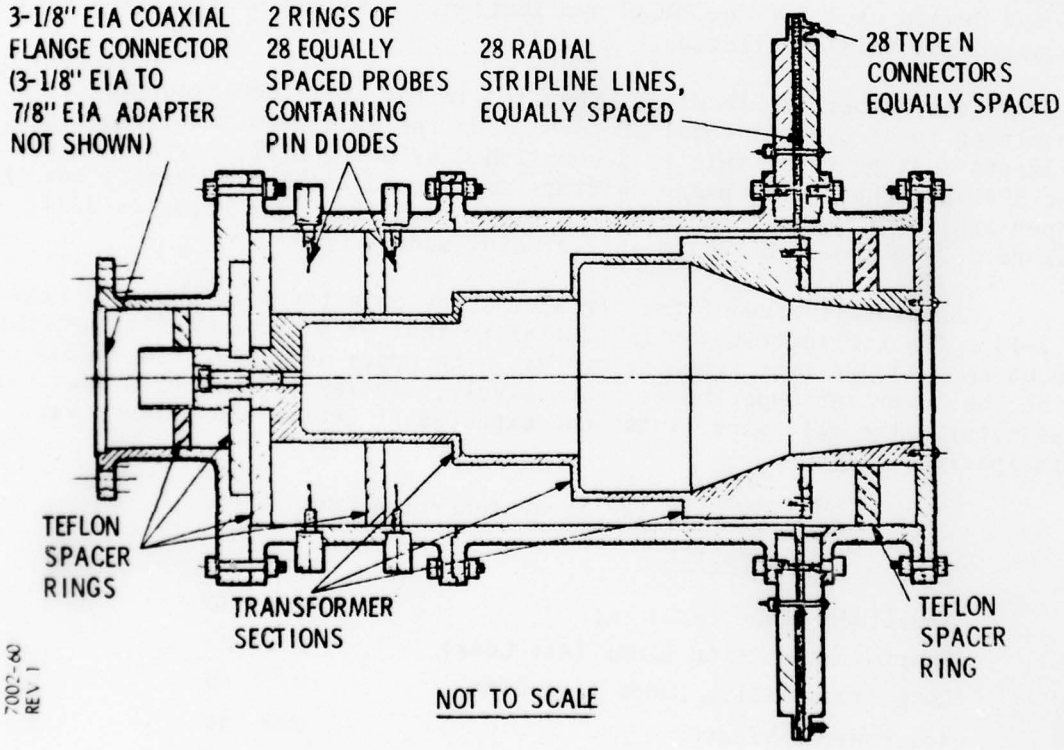

Figure 2.2-12. Amplitude Sequencer Cross-Section

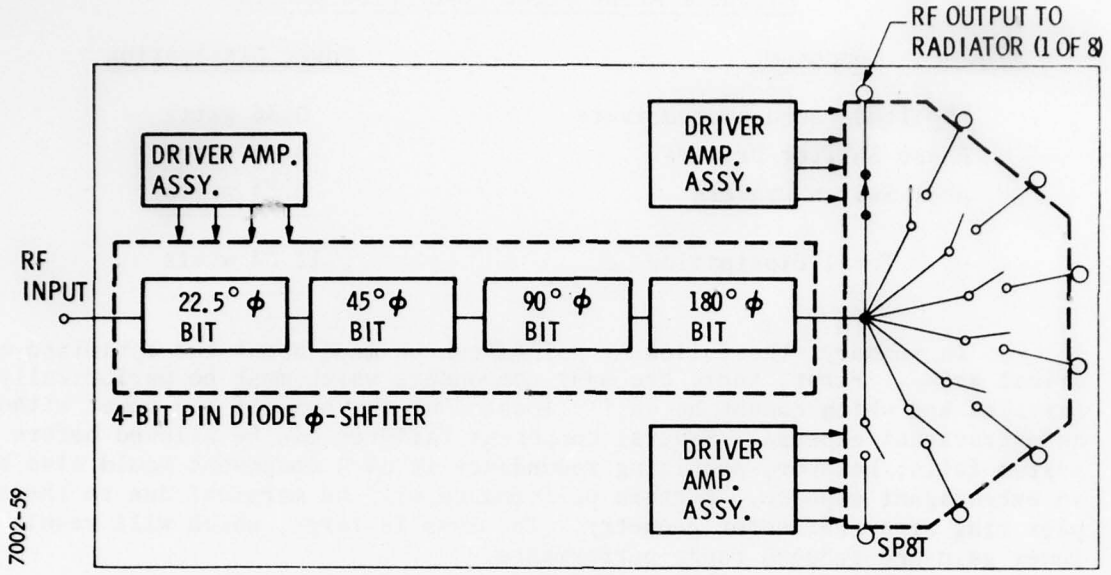

Figure 2.2-13. Phase Shifter/SP8T Switch Assembly

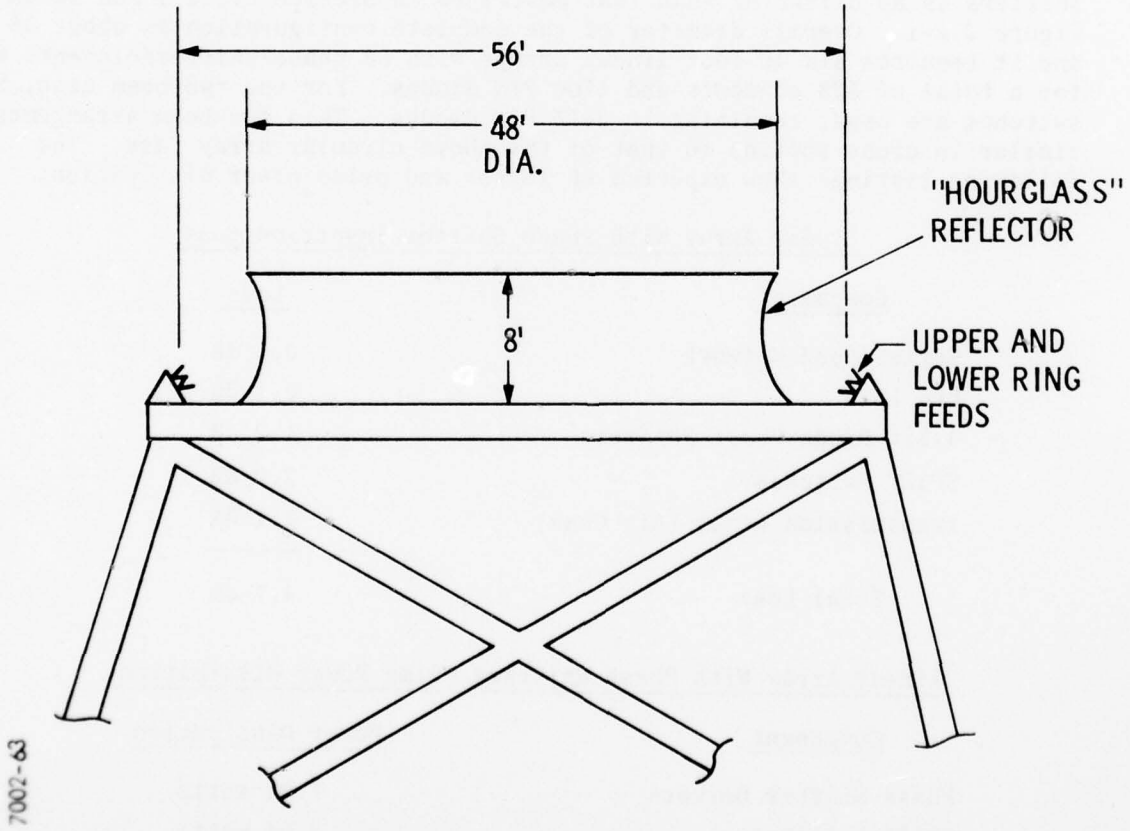

Figure 2.2-14. Circular Array on Tower

Circular Array Prime Power Dissipation

Component	Power Dissipation
Amplitude Sequencer Drivers	0.34 watts
Phase Shifter Drivers	8.96 watts
SP8T Switch Drivers	2.24 watts
Total Dissipation	11.54 watts

In summary, the following points can be made about the optimized cylindrical array. First, there are many components which must be periodically serviced and which cannot be easily located at the base of the tower without an extravagant expense. Several component failures can be allowed before the system fails; however, providing redundancy in each component would also be an extravagant expense. Pattern performance will be marginal due to the complex ring array/reflector geometry. The loss is large, which will result in lower gain and reduced range performance.

2.2.2.5 Optimized Six-Face Linear Array With Phase Shifters - Performance features of the optimized six-face reflector fed by linear arrays with phase shifters are discussed. The optimized six-face linear array with phase shifters is no different than that described in Section 2.2.2.1 and shown in Figure 2.2-1. Overall diameter of the complete configuration is about 88 feet and it requires six 40-foot linear arrays with 88 phase-shifter/elements each, for a total of 528 elements and 1760 PIN diodes. For the two-beam case, SP12T switches are used, resulting in 2816 PIN diodes. This two-beam arrangement is similar in cross-section to that of the above circular array case. The following listings show expected RF losses and prime power dissipation.

Linear Array With Phase Shifter Insertion Loss

Component	Loss
Series Feed Network	0.3 dB
End Load	0.1 dB
4-Bit Diode Phase Shifters	1.2 dB
SP12T Switches	2.0 dB
Transmission Lines (Air Coax)	1.1 dB
Total Loss	4.7 dB

Linear Array With Phase Shifters Prime Power Dissipation

Component	Power Dissipation
Phase Shifter Drivers	7.04 watts
SP12T Switches	2.64 watts
Total Dissipation	9.68 watts

In summary, an optimized linear-array with the phase shifters is very similar in most respects to the cylindrical array. The only substantial difference is in pattern performance. The linear array pattern is much easier to form and is more likely to achieve the specified shape in elevation and low sidelobe level in azimuth. The only other point of comparision is the overall size, with linear array size being about 57 percent greater. However, structural costs are probably small in comparison to the overall life-cycle costs since they will not require much maintenance.

2.2.2.6 Optimized Six-Face Linear Array With Frequency Scanning - Highlights of the optimized six-face reflector fed by frequency scanning linear arrays are discussed herein. The basic element of the frequency-scanning linear array is shown in Figure 2.2-15 for the single-beam case. A SP6T switch is located in the equipment shelter, and six low-loss waveguide runs feed six frequency-scanning array feeds. A SP12T switch and 12 waveguide runs are required for the dual-beam case. Waveguide is used for its reliable low-loss characteristics, without a major cost disadvantage due to the limited amount. Waveguide is also used for the dispersive "serpentine" feed which provides $\pm 30^{o}$ scan by varying frequency within the operating band. No active components nor any other components with a limited life are used other than the central switch, which can be made highly reliable through use of redundant components, if required. The following listings show the expected RF losses and prime power dissipation:

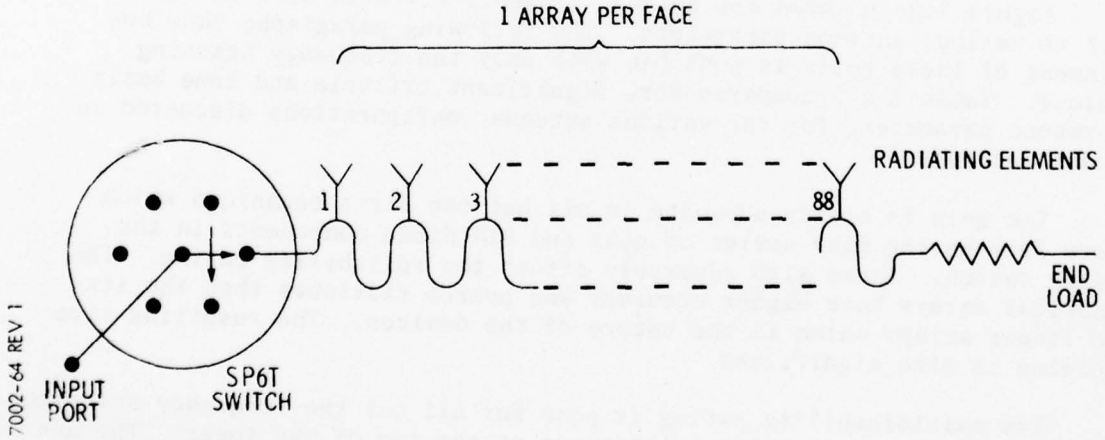

Figure 2.2-15. Frequency Scanning Array Element

Linear Array With Frequency Scan Insertion Loss

Component	Loss
SP12T Switch	1.6 dB
Waveguide Run	0.1 dB
Frequency Scanner	0.9 dB
End Load	0.1 dB
Total Loss	2.7 dB

Linear Array With Frequency Scan Prime Power Dissipation

Component	Power Dissipation
SP12T Switch	3.30 watts

In summary, the frequency scanning approach appears to be the optimum antenna configuration for the proposed UAR application because of its obvious advantages in high reliability, low maintenance, low prime power dissipation, and low cost. The following section describes this comparison in detail.

2.2.2.7 Tradeoff Analysis Summary - The six-faced cylindrical reflector with frequency-scanning line feeds is selected over other candidate antenna techniques to provide adequate performance along with major cost, reliability, and maintenance advantages.

Figure 2.2-16 shows the antenna tradeoff criteria used and their effect on various antenna parameters. The following paragraphs show how attainment of these goals is possible with only the frequency scanning technique. Table 2.2-7 compares more significant criteria and some basic performance parameters for the various antenna configurations discussed in previous sections.

The gain is nearly adequate in all but the first technique which suffers from having many series of coax and PIN diode components in the transfer switch. These also adversely effect the reliability rating. The cylindrical arrays have higher accuracy and poorer sidelobes than the six-faced linear arrays which is the nature of the devices. The resulting size difference is also significant.

The maintainability rating is poor for all but the frequency scanning technique because they require maintenance at the top of the tower. The use of four or five-hundred waveguide runs needed to provide an acceptable loss limit is considered not economically practical. Furthermore, phase matching of these runs is extremely difficult.

TABLE 2.2-7. COMPARISON OF TECHNIQUES

Technique	Performance Factors: Gain	SLL EST	Angle Error	Cost Factors: Overall Size	Number PIN Diodes	Reliability* Rating	Maintenance* Rating
Circular Array Without Phase Shifters	24.0 dBI	-24 dB	0.1^{o}	56'	3072	2	2
Circular Array With Amplitude Sequencer	26.1 dBI	-23 dB	0.1^{o}	56'	2744	5	2
Six-Face Linear Array With Phase Shifters	25.1 dBI	-28 dB	0.7^{o}	88'	2816	7	2
Six-Face Linear Array With Integrated Variphase-Coupler	25.6 dBI	-22 dB	0.7^{o}	88'	2464	7	2
Six-Face Frequency Scanning Array	27.1 dBI	-30 dB	0.7^{o}	88'	24	9	10

NOTES: *Ratings use scale of from 1 (lowest rating) to 10 (highest rating) with 5 being acceptable.
Gain referenced to base of tower (at max scan for linear arrays) 2-beam cases assumed.
Angle error assumes adjacent beam comparison used.
All techniques except frequency scan have feed networks on tower.

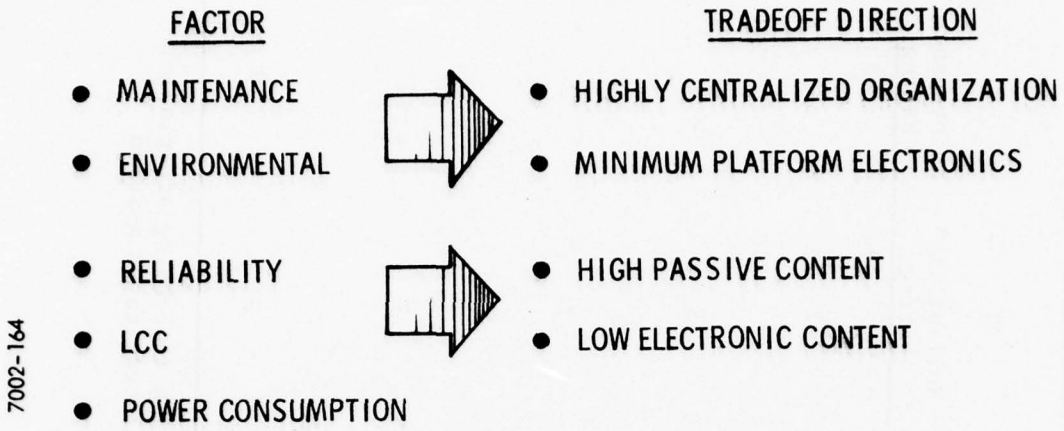

Figure 2.2-16. Antenna Tradeoff Criteria

Reliability ratings are estimated based on the number of series components that are prone to failure. As indicated, the first technique has many failure-prone components in series that can each cause an antenna failure. Redundant use of components is considered impractical because of the large number required.

The circular array with phase shifters has three components in series. If five elements are allowed to fail before the antenna is considered to fail, then five failures in either the SP8T switches, phase shifters, amplitude sequencer, or some combination of these can be allowed to fail. Thus, it is expected that enough redundancy is available for meeting minimum MTBF requirements.

The linear array with phase shifters has only two series failure-prone components, and is expected therefore to provide more reliability. However, the frequency scanning approach has only one failure-prone component for each face and is thereby given the highest rating. Furthermore, these components can be made more reliable by using slightly more expensive diodes, by having a more suitable environment, or by using additional redundancy.

The integrated variphase/coupler technique for dual beam configuration is also included in Table 2.2-7 for reference. It is not expected to be a viable candidate due to its poor sidelobe performance, but is worthy of mention for other respects. It is included here because it may overcome the high sidelobe deficiency with future research.

In summary, frequency scanning technique is expected to have major performance, cost, reliability, and maintenance advantages. Prime power dissipations are not considered significantly large in any of the techniques.

2.2.3 UAR Baseline Antenna Description*

Six cylindrical-shaped reflectors are each fed by dual periodically-loaded slot arrays to form the frequency-scanning dual elevation beam antennas for UAR. Figure 2.2-17 shows the overall configuration of the frequency scanning approach. Two frequency scanning linear arrays feed the cylindrical shaped reflector to form the upper and lower-shaped beams. Scanning over 360 degrees is accomplished with six separate faces, each one scanned in frequency plus and minus 30 degrees. Twelve waveguide runs couple power from the equipment shelter at the bottom of the tower to the individual antennas. An SP12T switch located in the equipment shelter, determines which beam and sector coverage will be used.

The reflector used for each sector is approximately 8 feet high by 30 feet wide. It is shaped in the vertical plane to broaden the beamwidth while still maintaining a sharp fall-off and low sidelobes. Figure 2.2-18 shows typical patterns for this application. Beamwidths of about 33 degrees are shown with the lower beam -3 dB point at the horizon. Sidelobes for this ideal case are below 30 dB; however, in practice, errors in the illumination will increase these levels somewhat. The optimum beam crossover level will

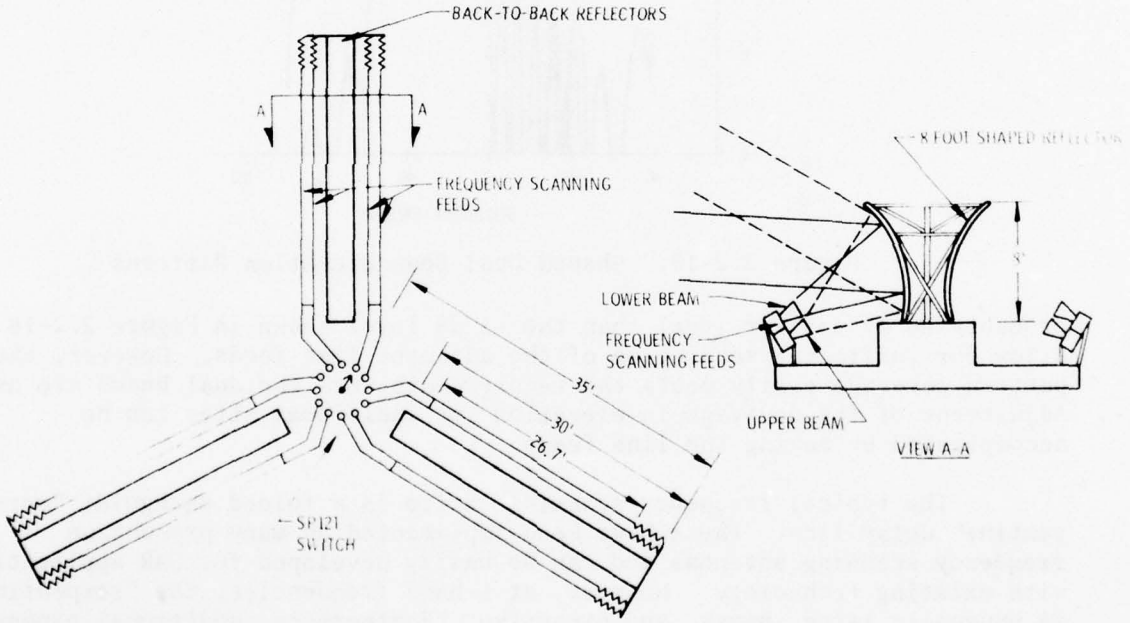

Figure 2.2-17. Overall Configuration of Frequency-Scanning Antenna

*Discussions in Sections 2.2.3 and 2.2.4 refer to the 26.7 ft. aperture antenna (see footnote on p. 2-44).

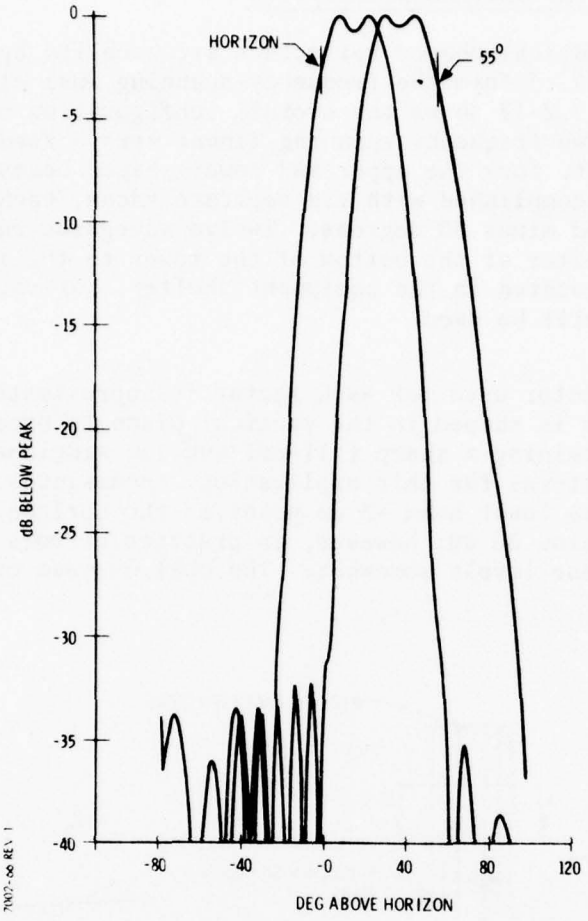

Figure 2.2-18. Shaped Dual-Beam Elevation Patterns

probably be at a lower level than the -1 dB level shown in Figure 2.2-18 to allow for sufficient separation of the adjacent line feeds. However, the pattern coverage easily meets the requirements when the dual beams are used. Adjustment of the coverage in elevation for individual sites can be accomplished by moving the line feeds.

The typical frequency scanning device is a folded waveguide "serpentine" delay line. These have been implemented on many production frequency scanning antennas and can be easily developed for UAR application with existing technology. However, at L-band frequencies, the "serpentine" is unusually large, heavy, and expensive. Furthermore, additional expense is incurred by the interconnection from the "serpentine" line to the radiating elements. The approach shown in Figure 2.2-17 assumes a frequency scanning feed with a low profile. To satisfy this format, a periodically loaded waveguide slot array (PLSA) will be used.

Figure 2.2-19 shows the proposed PLSA line feed configuration. A waveguide, which would normally be below cutoff, is capactively loaded with posts to produce the required dispersive characteristics usually obtained with the serpentine. Recent R&D at ITT Gilfillan has demonstrated the feasibility of this approach. Scan angle ranges beyond 60 degrees with frequency are easily obtained through selection of the proper waveguide sizes and post capacitances.

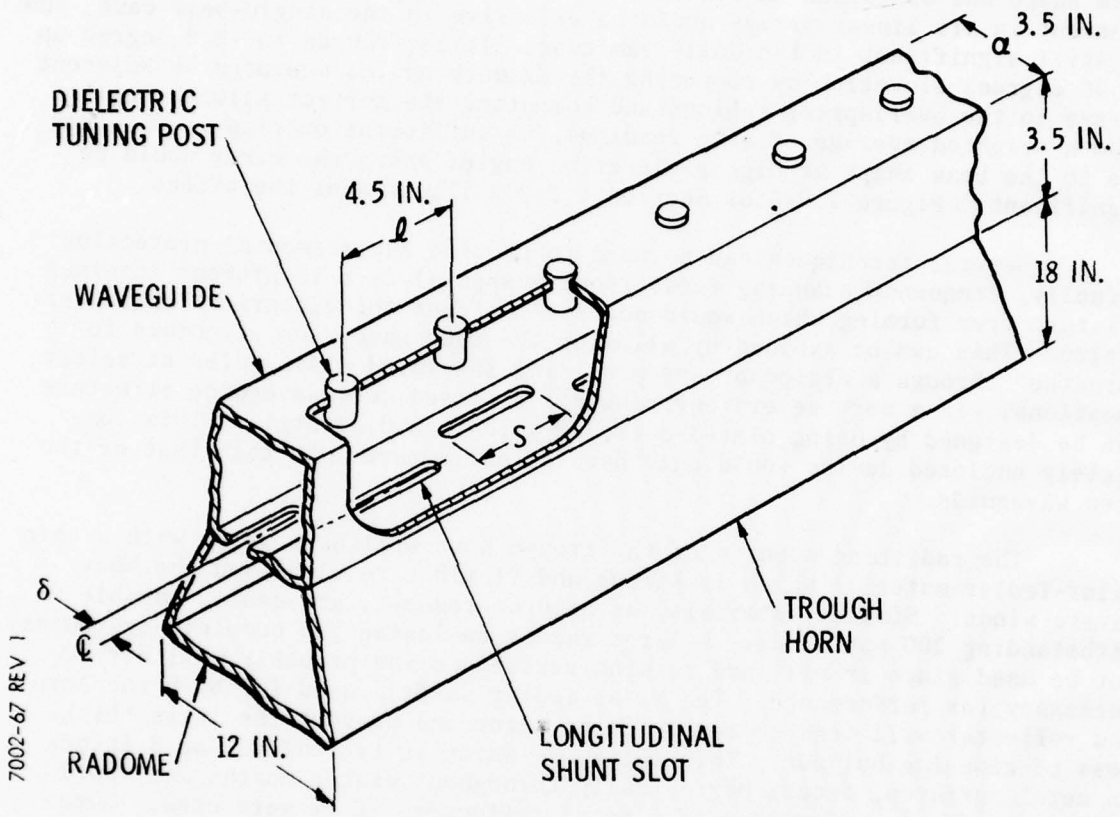

Figure 2.2-19. Periodically-Loaded Waveguide Slot Array (PLSA)

The proposed configuration will be designed to scan 30 degrees over two separate, small segments of the overall frequency band. The lower band segment will be from about 1215 to 1275 MHz, and the upper from about 1330 to 1400 MHz. In the center segment, the beam passes out of real space as a grating lobe is formed which then becomes the main beam. This segment will not normally be used. The list below shows frequency scan characteristics of the proposed approach.

Frequency (MHz)	Azimuth Scan Angle (Deg.)
1216	-30.2
1242.7	0.0
1272	30.9
1332	-30.5
1364.3	0.0
1399	30.5

Loss of the device is similar to loss in the serpentine, and the transient response is identical for the same scanning characteristics. However, tuning during production is much easier because simple adjustments in the tuning posts can be made externally before they are permanently sealed. Thus, 30 dB sidelobes are easily obtainable, and 40 dB sidelobes are also possible.

The technique for correcting azimuth error introduced by the conical beam shape was discussed in Section 2.2.2.2. To review briefly, this error inherent in all linear arrays would be excessive in the single-beam case, and is still significant in the dual-beam case. It is reduced to -0.8 degree up to 40 degrees elevation by comparing the azimuth angles measured by adjacent arrays in the overlapping regions and computing the correct azimuth angle from a weighted average of both readings. A sufficient overlap is obtained due to the beam shape at higher elevation angles where the error would be significant. Figure 2.2-5 of Section 2.2.2.2 illustrates the effect.

Several techniques can be used to provide environmental protection. Normally, frequency scanning feeds require special care to prevent internal moisture from forming which would adversely affect the electrical characteristics. This can be avoided by allowing the open waveguide structure to "breathe" through a desiccant and providing insulated drain holes at select locations. In a more severe environment, a closed-cell waveguide structure can be designed by using plated-over, ceramic-foam dielectric. This completely enclosed device would only have slightly more loss than that of the open waveguide.

The radiating opening of the trough horn will be covered with a thin Mylar-Tedlar material which is strong and flexible to withstand the most severe winds. Similar materials, as used on radomes, are easily capable of withstanding 200 mph winds. A large radome enclosing the complete system may not be used since it will add to wind resistance and probably will not be necessary for performance. The Mylar-Tedlar surface used for both the horn and reflector will tend to repel ice or water and prevent the large thickness of rime-ice buildup. This thickness which is typically 2 or 3 inches on metal surfaces, occurs periodically throughout winter months and would adversely affect performance of a metal reflector, if it were used. Some sites, particularly in Baffin Island, have severe rime-ice buildup, and may require special antenna techniques, such as cylindrical radomes covering the outer radiating portion of each of the antennas. In these special cases, the 6- or 7-inch rime-ice buildup could cause as much as 3 dB loss if it covered the radiating surface of the trough horn. The effects of ice buildup on the reflector is not nearly as significant as the horn radome, which is somewhat shielded from direct exposure to wind and ice. A summary of environmental tradeoffs and radome recommendations are shown in Table 2.2-8.

The waveguide runs from the PLSA down the tower to the equipment shelter will not require any special techniques for environmental protection. Standard WR-650 waveguide can easily provide this function, although a reliable, lightweight, low-loss transmission line would be more desirable. Hollow waveguide made from plated dielectric material is a possible alternative if its reliability proves attractive.

TABLE 2.2-8. RADOME TRADEOFF ANALYSIS

	ACCUMULATION	EFFECT IN PERFORMANCE	OVERTURN MOMENT	RELATIVE COST	RECOMMENDATIONS: SEMIARID REGION	RECOMMENDATIONS: REGION BAFFIN ISLAND
SPHERICAL RADOME	MINIMUM DUE TO SHAPE AND AIR FLOW	MODERATE	VERY HIGH	HIGH ADDED COST	NOT REQUIRED	PARTIAL SECTION DESIRABLE
REFLECTOR	MAXIMUM	LOW DUE TO LOW FIELD	MODERATE	--	ACCEPTABLE	AERODYNAMIC BUBBLE INTEGRAL WITH REFLECTOR
FEED	MINIMUM ON APERTURE	HIGH	--	--	ACCEPTABLE WITH PROPOSED RADOME COVER	AERODYNAMIC BUBBLE INTEGRAL WITH REFLECTOR

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The SP13T switch assembly* in the equipment shelter (see Figure 2.2-20) receives RF energy from the transmitter, then switches this energy between both the upper and lower beams of a given array, and from one array to another. The switch assembly will be implemented in stripline, and packaged PIN diodes will be used to handle the 2 kW peak power. To provide adequate isolation, two diodes will be used in each output leg of the switch assembly and insertion loss for a given leg is expected to be approximately 1.4 dB.

The diodes will be shunt-mounted on 3/4 stubs to comfortably handle peak RF power and to provide added reliability. The most common mode of diode failure is an open, and the circuit is designed so that should a diode fail to open, that leg will continue to operate with slightly degraded performance. If it is proved necessary, 26 additional diodes will be used for redundancy. Because only one leg of the switch is on at a time, the prime power required is approximately 3.3 watts.

The coupling capacitors shown will be printed circuit, interdigital types, thus reducing the number of discrete components required. A driver amplifier will be required to bias each PIN diode pair. The driver amplifier module will include BITE circuitry which provides fault warning for semiconductor failures either in the driver amplifiers or in the switch assembly module. The switch assembly size will be approximately 9" x 14" x 1.5". Should failures occur in the assembly that prevent reliable radar performance, the entire switch module assembly will be replaced. Repair of the module is expected to be performed at the depot level.

The overall antenna parameters are shown in Table 2.2-9 and a detailed estimate of gain and loss is shown in Table 2.2-10. These tables summarize performance expected for the UAR main antenna.

*The 13th connection is used for transmitting the IFF P_2 pulse.

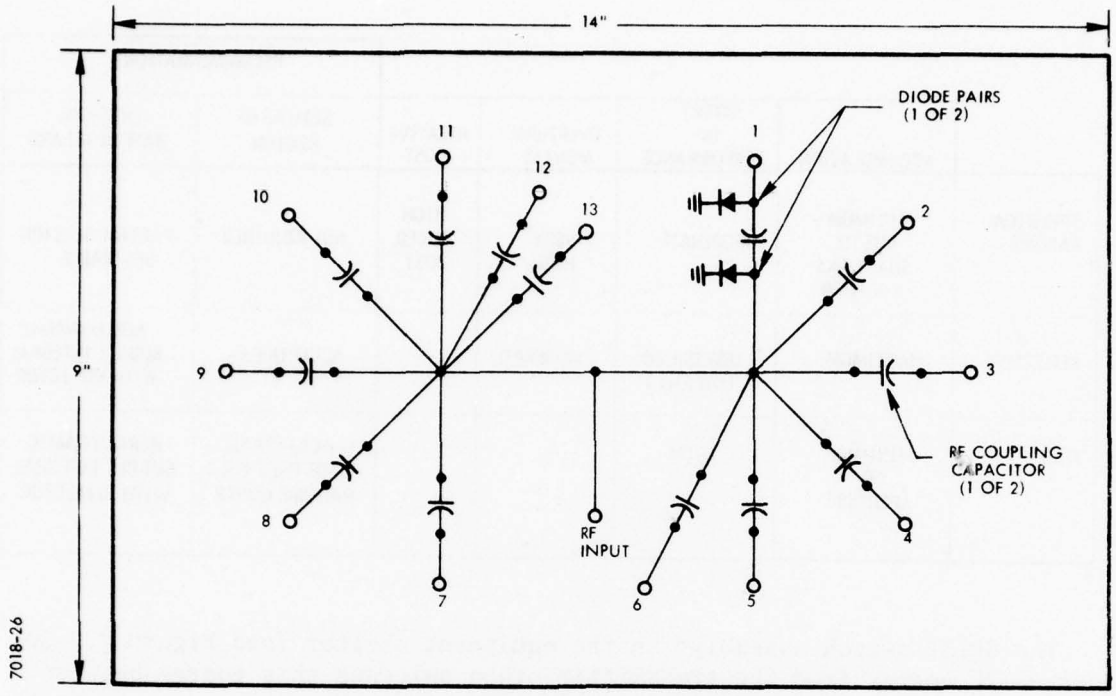

Figure 2.2-20. SP13T Switch Assembly

2.2.4 IFF/Omni Antennas

A separate antenna system consisting of 12 horns spaced at their 30 degree beamwidth increments in azimuth will be used for IFF. Figure 2.2-21 shows the IFF antenna system. The directional beam is formed by 12 horn antennas separated 30 degrees in azimuth. One horn is excited at a time, to form the directional P1 pulse. A separate omni-antenna is used for the P2 ISLS pulse. Each directional beam covers the required 0 to 50-degree elevation angle range, and an azimuth angle range approximately equal to the 3 dB beamwidth of 30 degrees. Finer resolution of adjacent, separate targets will be based on range. The entire IFF system is centrally located within the main antenna configuration and is at a slightly higher level to avoid interference.

Figure 2.2-22 shows recommended techniques for incorporating the IFF feed into the feed network for the main radar antenna. Twelve waveguide diplexers are located at the top of the tower to combine each IFF and radar signal into a single waveguide, thus minimizing the number of waveguide runs up the tower. A single SP13T switch is also used for IFF and radar instead of two separate devices. With proper design, the bandwidth of both the IFF and radar frequencies can be accommodated by the switch. Use of a separate diplexer in the omni-antenna line allows this antenna to be used for the IFF

TABLE 2.2-9. UAR MAIN ANTENNA PARAMETERS

TYPE	REFLECTOR FED FREQUENCY SCANNER
OVERALL SIZE	70 FT MAXIMUM DIAMETER
SIZE OF 1 FACE	30 FT X 8 FT REFLECTOR WITH 27 FT SCANNING LINE FEEDS
NUMBER OF FACES	SIX
NUMBER OF EL BEAMS	TWO
FREQUENCY SCANNING DEVICE	PERIODICALLY LOADED SLOT ARRAY
GAIN AT TOWER BASE	26.2 dBI
DISSIPATIVE LOSS	3.12 dB
COVERAGE AZ/EL	$360^{0}/0^{0}$ to 50^{0}
COVERAGE PER FACE	OVER 60^{0} AZ
AZIMUTH BEAMWIDTH	2.25^{0}
AZIMUTH ACCURACY	0.7^{0}
SIDELOBE LEVEL	-30 dB
OPERATING FREQUENCIES	1215 TO 1272 AND 1332 TO 1400 MHz
INSTANTANEOUS BANDWIDTH	1 MHz
NUMBER OF PIN DIODES	26
PRIME POWER DISSIPATION	3.3 WATTS

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TABLE 2.2-10. GAIN/LOSS ESTIMATE

AREA GAIN	37.24 dBI
TAPER LOSSES	
AZ	1.0
EL	6.3
TOTAL	7.3
DIRECTIVITY	29.94 dBI
DIRECTIVITY @ 30^{0} SCAN	29.32 dBI
LOSSES	
SPILLOVER	0.6 dB
SCANNING WG	0.6 dB
END LOAD	0.12
TOTAL	1.32 dB
GAIN AT INPUT TO 1 FACE	28.0 dBI
LOSS OF DIPLEXER	0.3 dB
LOSS OF SP13T SWITCH	1.3 dB
LOSS OF 100' TOWER WG	0.2 dB
TOTAL	1.8 dB
GAIN AT BASE OF TOWER	26.2 dBI

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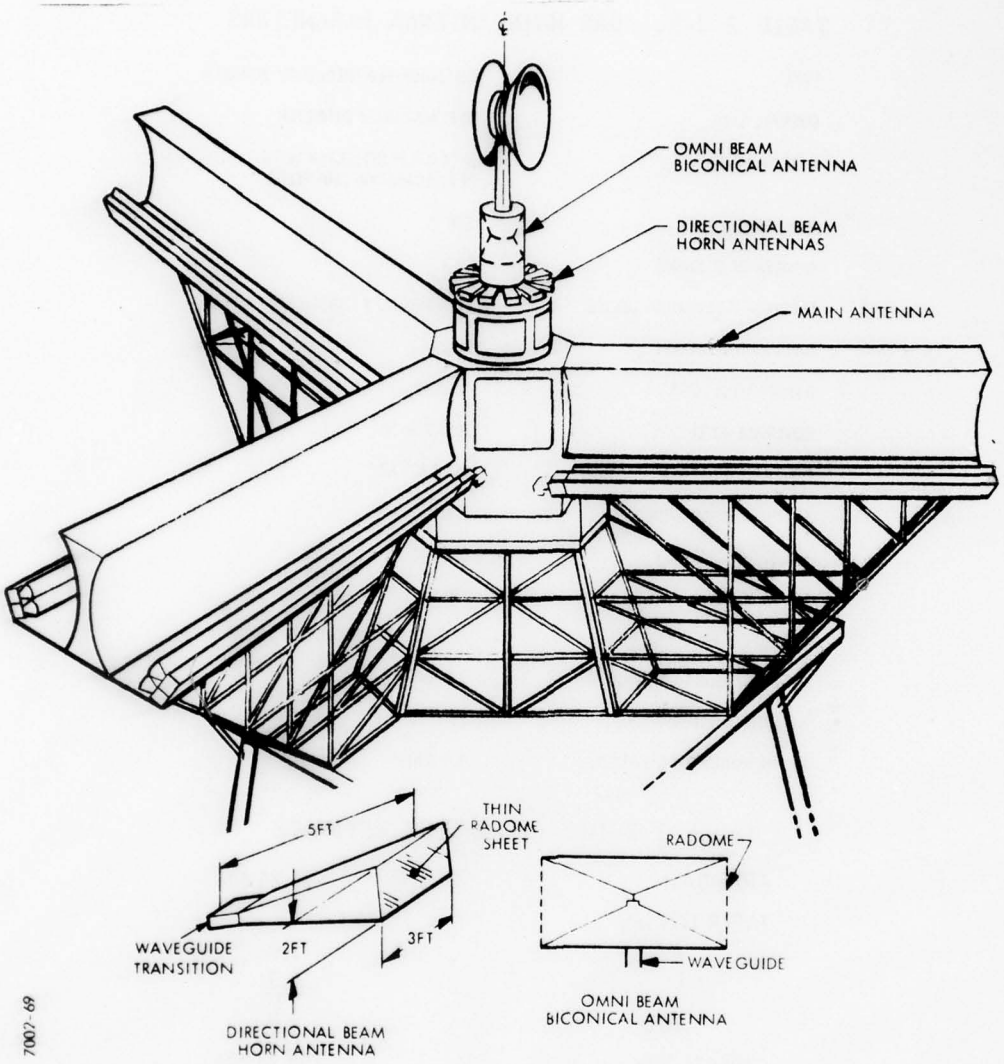

Figure 2.2-21. IFF Antenna System

P2 pulse and for a radar reference beam or sidelobe suppression mode. The omni antenna can also be used to provide IFF Receiver Sidelobe Suppression (RSLS) if desired. This would require an additional IFF receiver and modification of the omni antenna switching circuitry.

The gain of each directional horn is about 15 dBI, with the omni-gain being about 4 dBI. Additional diplexer loss to the main antenna is about 0.3 dB each, resulting in a gain of 26.2 dBI for the main antenna. No additional reliability problems or maintenance procedures are required by this system.

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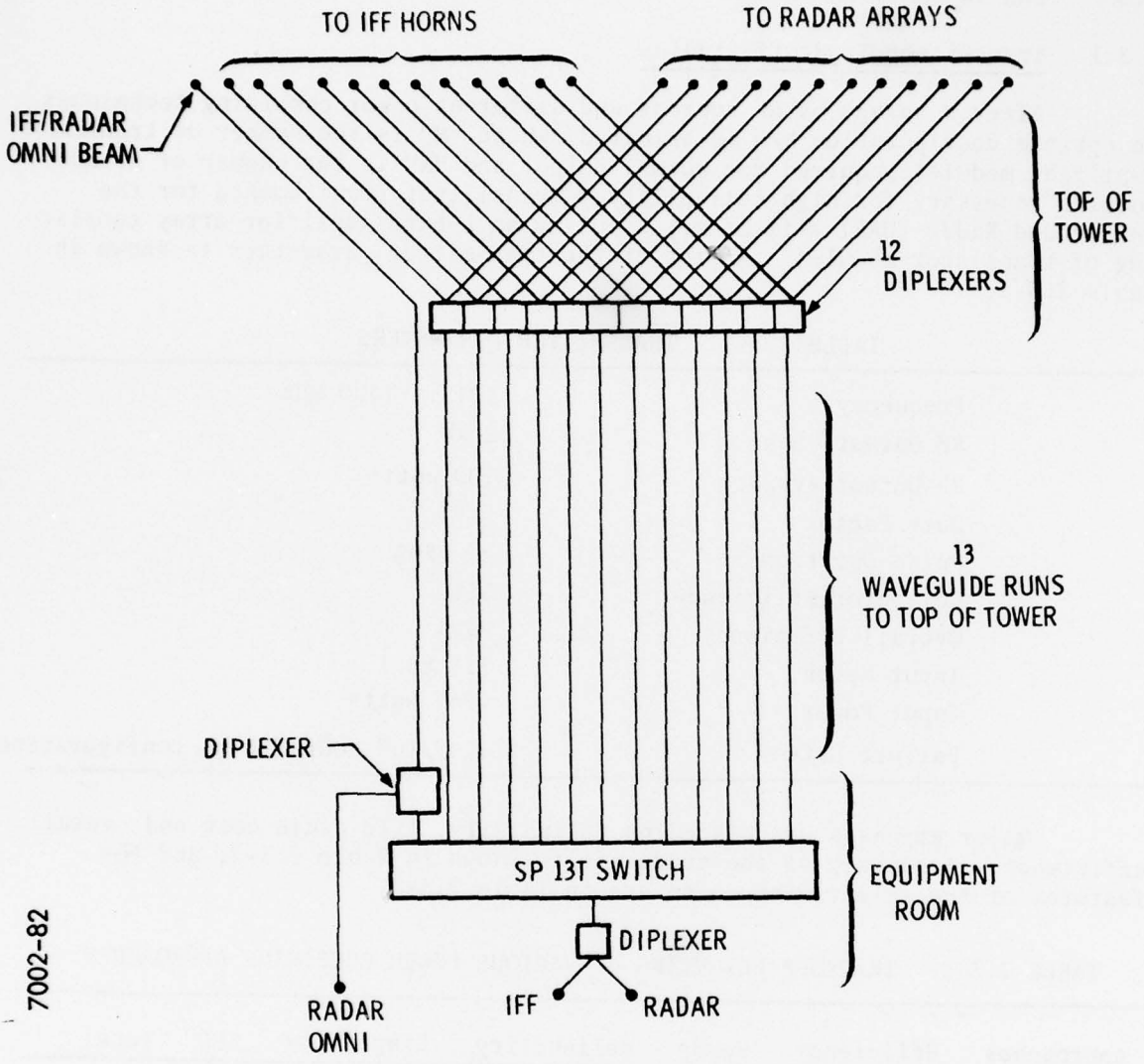

Figure 2.2-22. IFF, Omni Beam and Radar Transmission Lines

2.3 UAR TRANSMITTER DESIGN

2.3.1 Transmitter Tradeoff Studies

After a survey of RF sources and different power combining techniques, an optimum configuration M/N is selected, where "M" is the number of transistor amplifier modules required for normal output and "N" is the number of standby modules necessary for high reliability. Transmitter requirements for the Unattended Radar (UAR) will be met by using an L-band amplifier array consisting of transistor modules. A list of the transmitter parameters is shown in Table 2.3-1.

TABLE 2.3-1. TRANSMITTER PARAMETERS

Frequency	1215 - 1400 MHz
RF Output Peak	2 kW
RF Output Average	100 watts
Duty Factor	0.05
Pulse Duration	50 μsec
Collector Efficiency	55%
Overall Efficiency	>40%
Input Match	1.5 to 1
Input Power	∿240 watts
Failure Rate	$450f/10^9$ hours (12 mo. configuration)

Major emphasis was placed on reliability, life cycle cost and overall efficiency. A summary of the tradeoffs is shown in Table 2.3-2, and the features of the selected approach are in Table 2.3-3.

TABLE 2.3-2. TRADEOFF WEIGHTING OF VARIOUS POWER COMBINING APPROACHES

Approaches	Efficiency	Power	Reliability	Simplicity	LCC	Total
M/N	10	5	10	4	10	39
Gysel	10	5	6	4	6	31
Wilkinson	10	3	6	3	6	28
Parallel	6	5	6	5	6	23
Series	2	4	6	4	6	22

TABLE 2.3-3. ADVANTAGES AND DISADVANTAGES OF M/N POWER COMBINING

Highly Reliable Due to Built-in Stand-By Module

Very Efficient Because Of:
- Low circuit loss
- Low mismatch
- No degradation in power caused by module failure

Low LCC:
- No maintenance of module is necessary before $M_f > N$
- Requires fewer modules

Power Handling is Excellent Because Of:
- Small amount of power dissipated in the combiner
- Unused channel has negligible wasted power

Disadvantages:
- Additional switching circuit is required
- Greater initial development effort necessary

The requirement of high power and efficiency suggested that an array of modules is required and each individual module must have high collector efficiency plus an efficient way of combining the modules. In the process of module selection, a survey of different classes of RF sources was conducted. Because of the emphasis on high efficiency requirements, many RF devices such as Trapatt amplifiers, Impatt amplifiers, miniature traveling wave tubes, and electron bombarded semiconductors were eliminated candidates.

Recently, bipolar technology has progressed rapidly so that high peak power can be achieved along with high collector efficiency. The most significant improvements were achieved in the area of internal matching micro networks, reliable gold metallization, and individually isolated elements with ballast resistors. Therefore, the bipolar transistor is considered the most suitable candidate to be used in each module.

Once a module was identified, an extensive study was conducted to come up with a good architecture of combining the modules. The different classes of combiners which were considered are: a parallel combiner using in-phase power dividers or 90^{o} coupler, series couplers with progressive coupling values, a multioutput Wilkinson divider/combiner, an improved version of the Wilkinson combiner by Gysel. All of these approaches have some drawbacks, either in efficiency or lack of reliability. (See Table 2.3-2.) The selected approach has overall advantages which greatly exceed the above classes of combiners. The following is a brief description and comparison of the different classes of combiners. A schematic of the parallel approach is shown in Figure 2.3-1. The input signal is amplified in the first stage, divided into four branches, and amplified again in each stage. The amplified signals are subdivided into sixteen branches to feed the final amplifiers. This approach has the advantage of simplicity, but has high insertion loss. The cost to incorporate redundancy is prohibitive, and a large percentage of power is lost for each failed module.

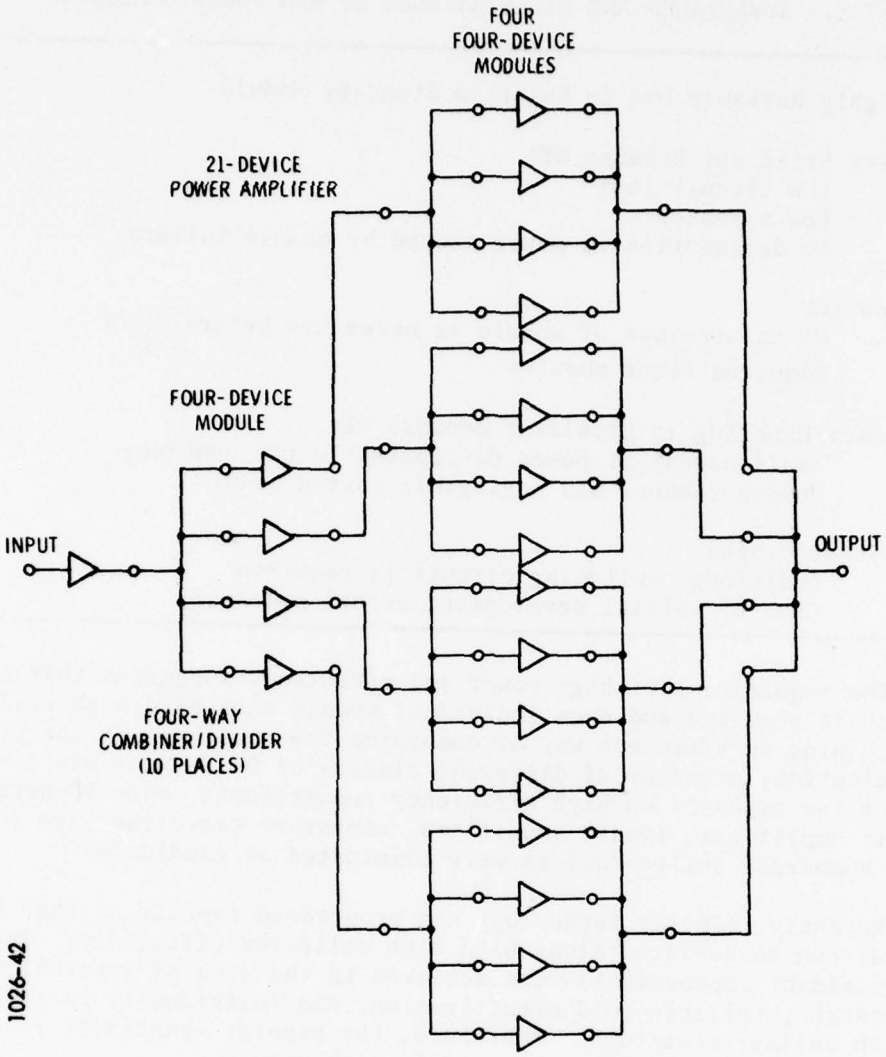

Figure 2.3-1. Power Amplifier Combiner

A schematic of the series combiner is shown in Figure 2.3-2. The signal to each coupler is divided proportionally. After each signal is amplified, they are combined again in reverse order. When the number of required modules increases, the insertion loss increases rapidly. Also, there is no simple way to introduce redundant amplifiers.

A Wilkinson divider or combiner has been used commonly for networks with a small number of ports. It has the advantage of low insertion loss, high isolation between output ports, and a good match in all ports. However, it has the disadvantage of difficulty in realizing the required star network and removing heat from the network. When this network is used as a power combiner, the total power output is decreased by 2/N with one module failure, where N is the total number of modules.

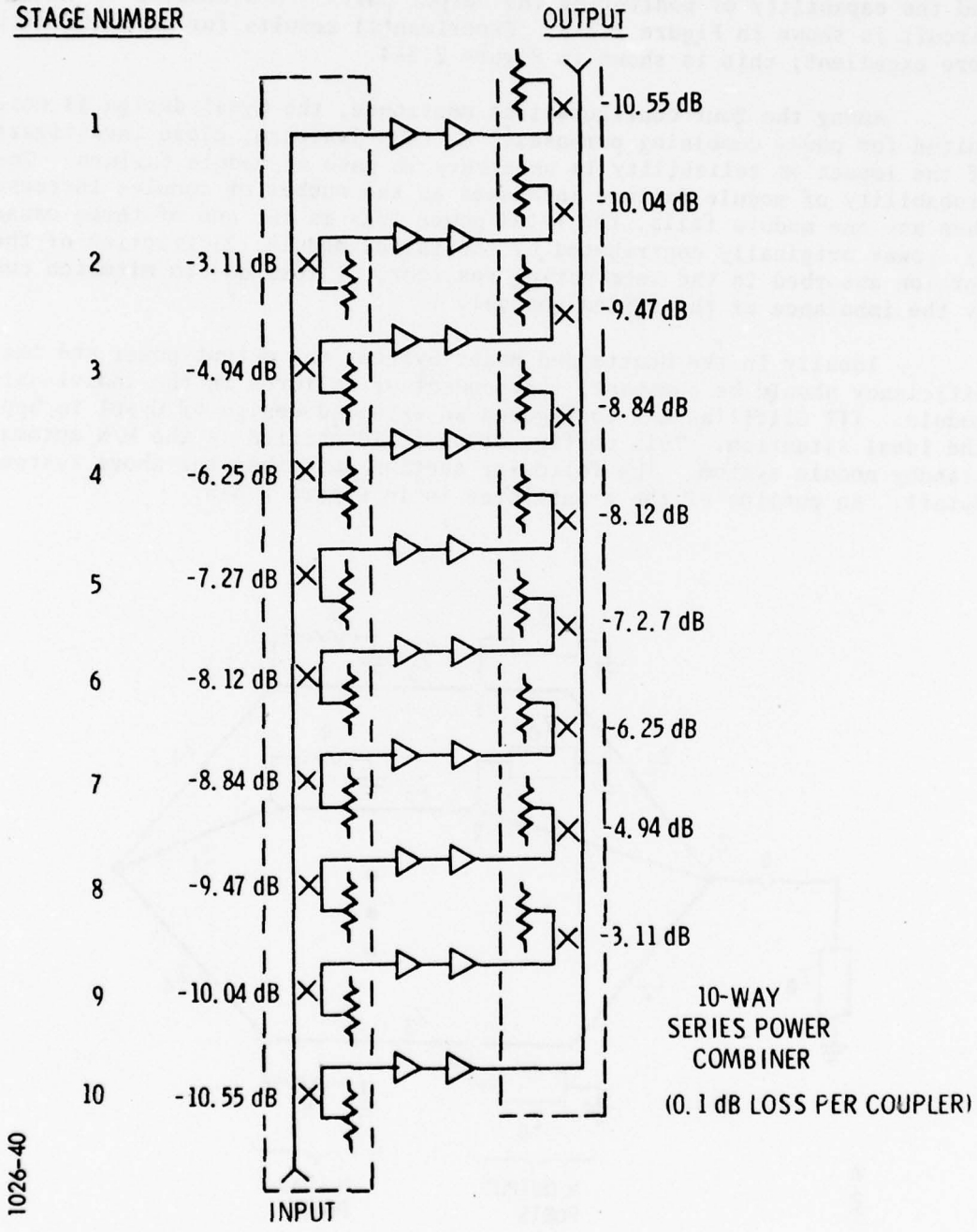

Figure 2.3-2. Series Combiner

Recently, U. Gysel of Stanford Research Institute has developed an extended configuration of the network by Wilkinson. The new design has the advantage of external loads, realizable circuits for large numbers of ports and the capability of monitoring the output ports. A schematic of the general circuit is shown in Figure 2.3-3. Experimental results for an 8-way divider were excellent; this is shown in Figure 2.3-4.

Among the four configurations mentioned, the Gysel design is most suited for power combining purposes. At this juncture, close investigation of the impact on reliability is necessary in case of module failure. The probability of module failure increases as the number of modules increase. When any one module fails, the total power loss is the sum of three causes: 1) power originally contributed by the failed module, 2) fraction of the portion absorbed in the terminating resistor, 3) loss due to mismatch caused by the imbalance of the failed channel.

Ideally in the Unattended Radar System, the output power and the efficiency should be constant, independent of failures in the individual module. ITT Gilfillan has configured an extended design of Gysel to approach the ideal situation. This configuration is identified as the M/N automatic standby module system. The following section describes the above system in detail. An outline of the transmitter is in Figure 2.3-5.

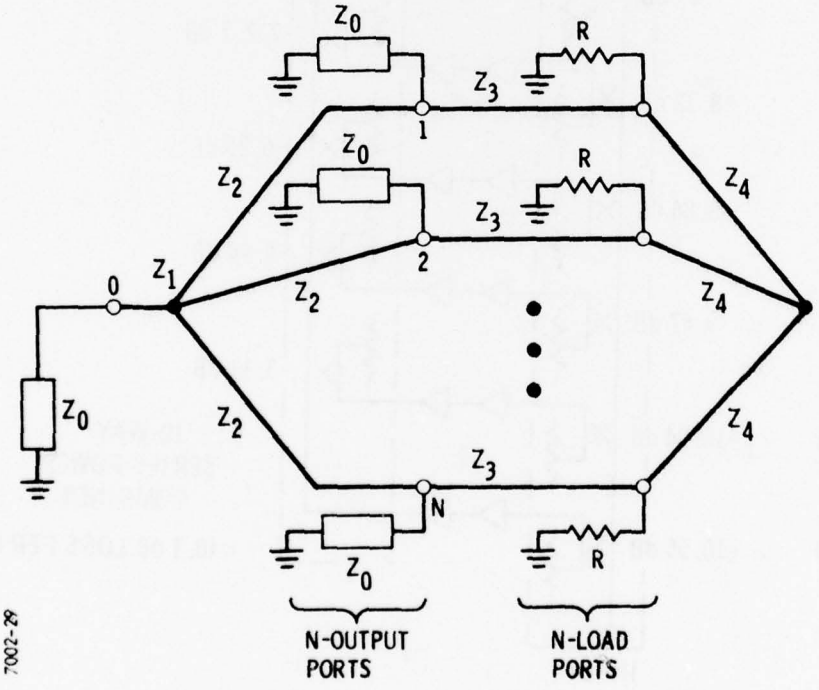

Figure 2.3-3. Gysel N-way Divider/Combiner

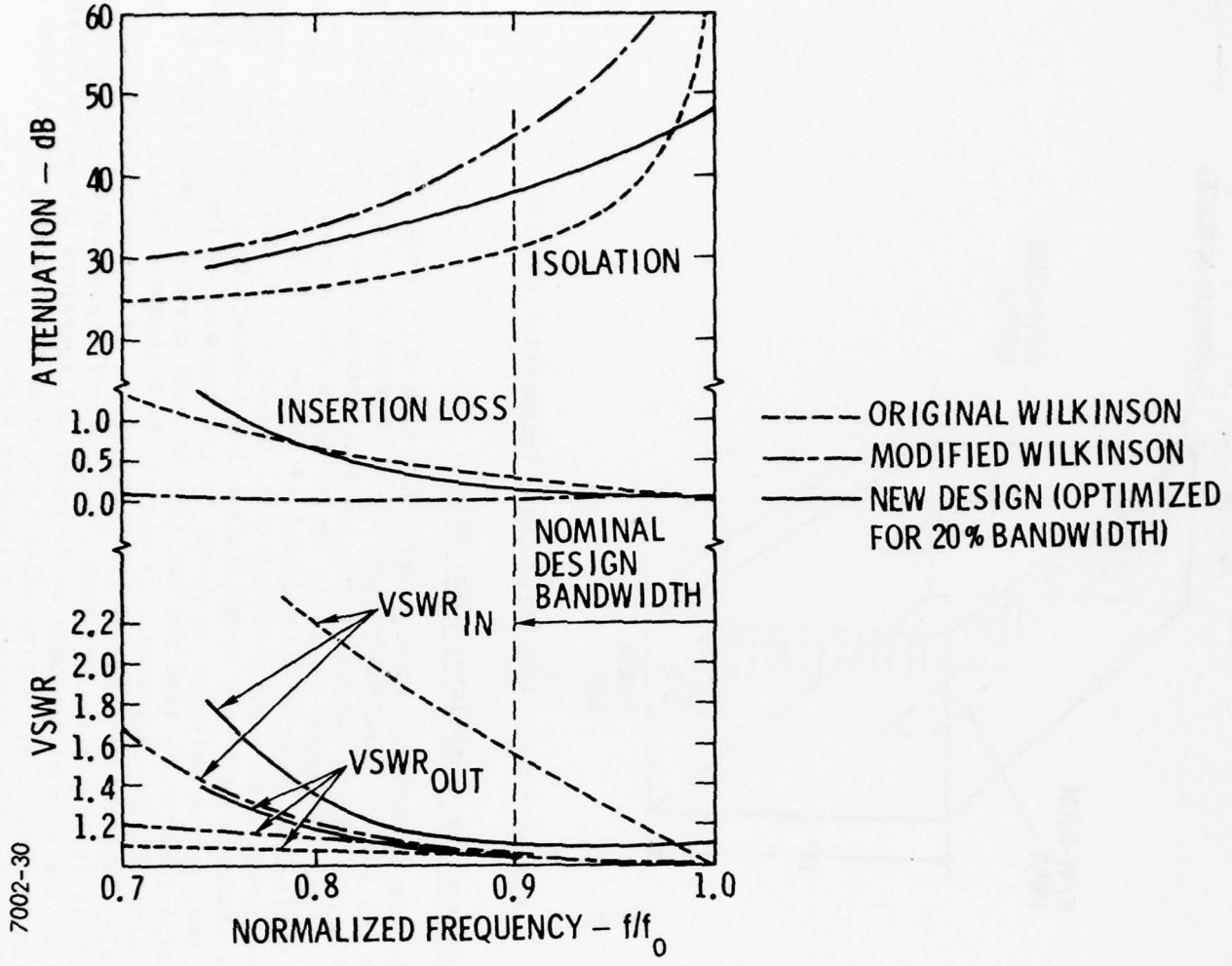

Figure 2.3-4. Theoretical Performance Of These Different Power Dividers (after Gysel)

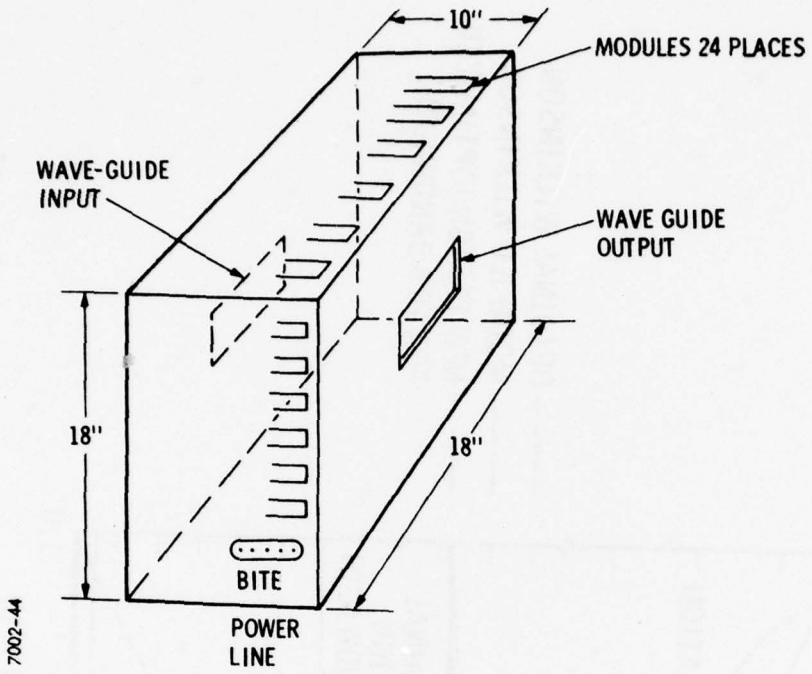

Figure 2.3-5. M/N Solid-State Transmitter Outline

2.3.2 UAR Baseline Transmitter Description

The M/N transmitter configuration has high efficiency, low life cycle cost, high reliability, and no degradation of performance with "N" number of module failures. The principle of the M/N Solid-State Transmitter is shown in Figure 2.3-6. The input signal is amplified in the preamplifier and the output is sufficient to drive M + N number of channels. M is the number of channels required to give the combined total output power, and N is the number of standby channels necessary to maintain a low probability of failure. Each M or N channel can be switched in or out by the commands of the steering logic which obtains information from the monitors at each channel. Initially, M number of channels are operating. As one of the M channels fails, it is automatically replaced with one of the N channels. If consequently one of the N channels fails, it is also replaced by one of the operable N channels. Each inoperative channel consumes no B+ power and therefore the overall power consumption is minimized. A simplified version of the steering logic which is necessary for the above operation is shown in Figure 2.3-7.

The basic functional blocks for the M/N transmitter are: a preamp module, a 24-way Gysel power divider, 20 M amplifier modules, four "N" amplifier modules, an extended Gysel combiner, which includes switching networks and monitors, a steering logic, and a switch driver assembly.

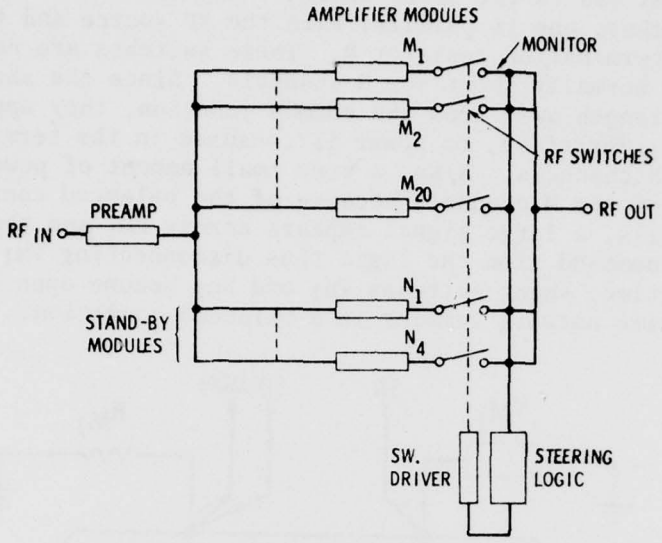

Figure 2.3-6. M/N Solid State Transmitter Schematic

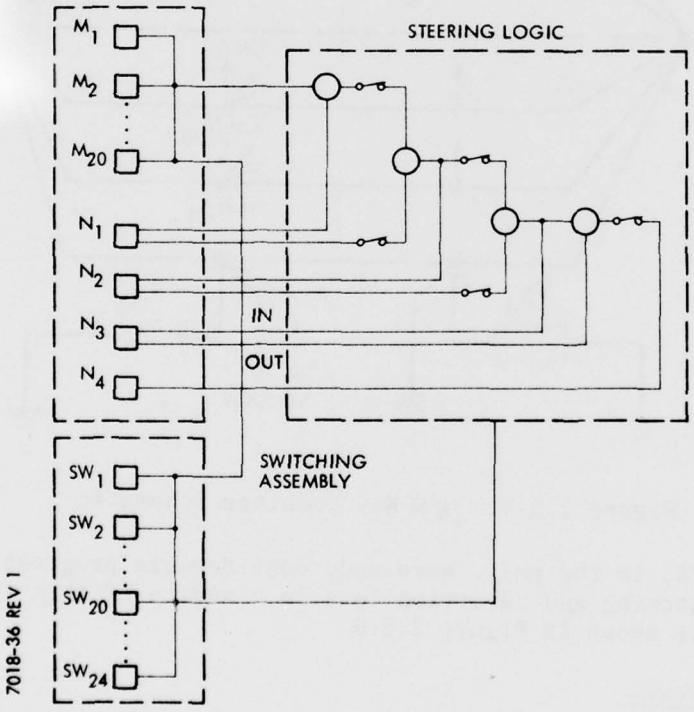

Figure 2.3-7. Normal And Stand-by Modules Steering Logic

An M/N way combiner schematic is shown in Figure 2.3-8. It contains all the circuit that was in the Gysel design. The extension is achieved by adding two RF switches, one in parallel with the RF source and the other in parallel with the termination resistor R. These switches are normally open for M channels and normally short for N channels. Since the shorted junctions are a quarter-wavelength away from the common junction, they appear as an open to both ends. Therefore, no power is consumed in the termination resistor R of the N channels. Also, a very small amount of power is consumed in the resistor R of the M channel, because of the balanced configuration. When Vm_1 module fails, a large signal appears across Rm_1 and the shunt switch will be shorted by command from the logic thus disconnecting Vm_1 and isolating Rm_1. At the same time, shunt switches Vn_1 and Rn_1 become open circuits. Therefore, the entire network remains in a balanced condition. Engineering

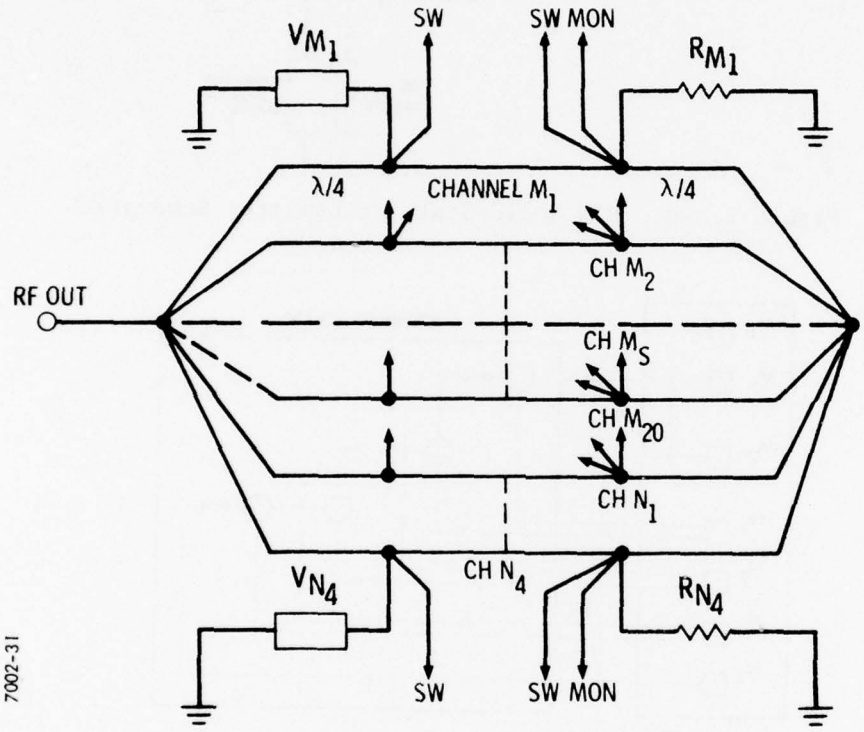

Figure 2.3-8. M/N Way Combiner Schematic

groups within ITTG, in the past, have made considerable progress in perfecting both the input matching and insertion loss in a device of this type and the general outline is shown in Figure 2.3-9.

Fault Monitor Circuit

A schematic of the fault monitor circuit is shown in Figure 2.3-10. The RF signal is detected by two diodes, D1 and D2, and they are isolated by the series resistor, Rs. The detected video output is fed to the scanner such that common channels of amplification can be used for all signals.

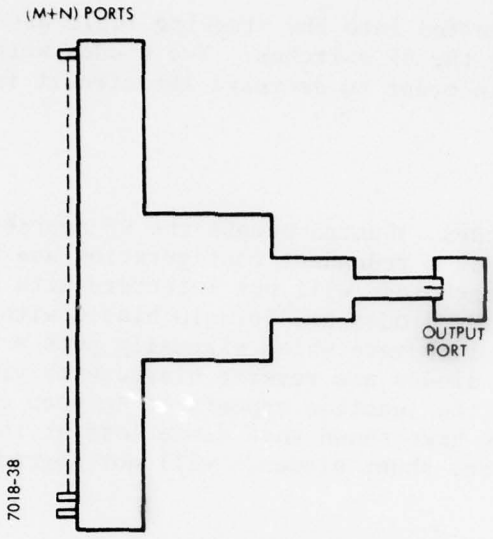

Figure 2.3-9. M/N Power Combiner Outline

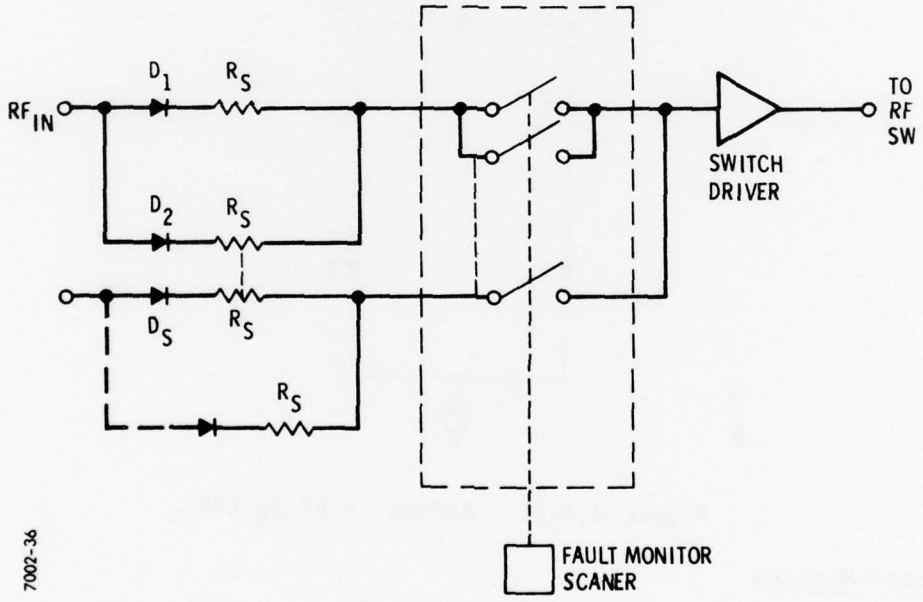

Figure 2.3-10. Fault Monitor System

Amplified signals are fed into the steering logic assembly where commands are generated to control the RF switches. Two diodes were used for each channel of video detection in order to decrease the circuit failure rate due to diode failure.

RF Redundant Switch

The RF switches, shunted across the RF sources and termination, use PIN diodes arranged in a redundant configuration and as shown in Figure 2.3-11. The failure of any one diode will not interfere with the intended function of the circuit. When the diodes are forward biased with a small current, the RF path has a very low impedance which virtually puts a short at the connecting junction. When the diodes are reverse biased with greater than six volts, the RF impedance across the junction appears as an open circuit. At L-band, experimental results have shown that diode loss at the open circuit is close to 0.1 dB. Therefore, shunt elements will not degrade the total network performance.

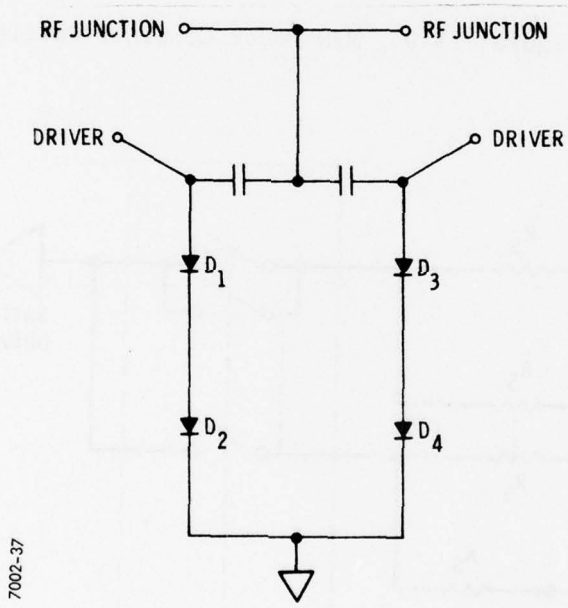

Figure 2.3-11. Redundant RF Switch

Transistor Modules

The transistor module is the major dominating factor in the overall efficiency of the transmitter. It also sets the limit of the maximum power available. Therefore, the description of this is placed under the Performance Characteristics Section where detail function and performance can be treated.

2.3.3 Performance Characteristics

The transistor amplifier has high peak power, high efficiency, and wide bandwidth primarily due to advanced technology in internal matching, uniform current density distribution, and thick, smooth, gold metallization.

High power output is difficult to obtain in microwave transistors because of the small geometry. In order to achieve usable power, research and development efforts were concentrated in improving the following parameters: 1) number of fingers per cell was increased by using ballasting technique; 2) number of cells per transistor was increased by internal matching; 3) average current density was increased with new processing technique; and 4) the thermal resistance has decreased substantially. In addition to the improvement of the above parameters, the transistor geometry has been optimized for high efficiency and gain.

Output Power Characteristics

First consideration of performance of the bipolar transistor for the Unattended Radar (UAR) was frequency range and bandwidth. Engineering personnel in the transistor industry were consulted on performance of state-of-the-art devices. Transmitter power output projection is based on these devices and is shown in Figure 2.3-12. Performance of the 12-cell transistors is based on 1976-1977 technology while performance of the 24-cell device is projected from performance of the 12-cell device in 1977 and the 56 cells that were achieved at 1.1 GHz. Twenty transistors are required to deliver 2 kW.

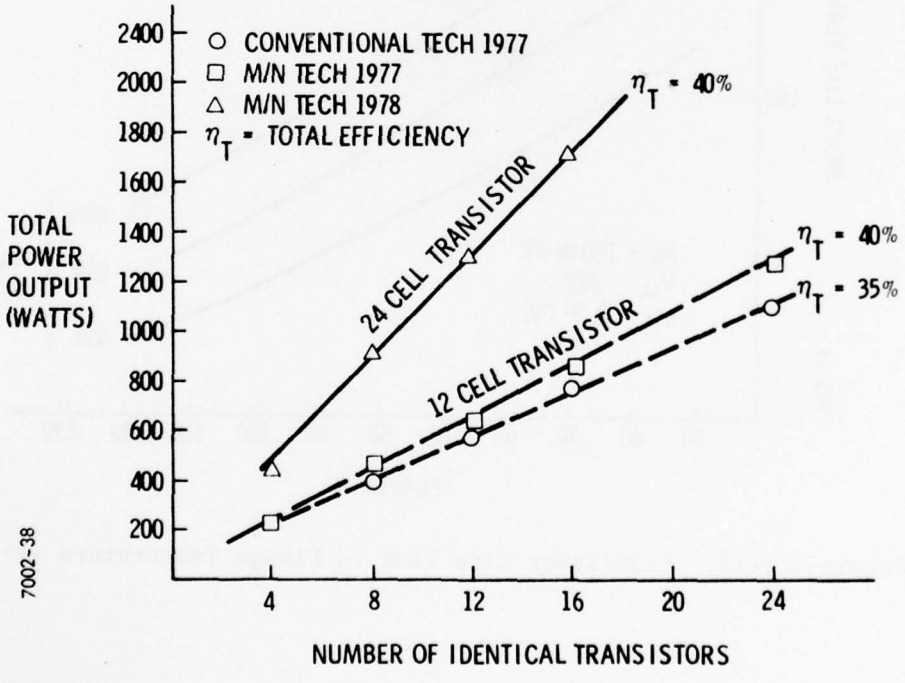

Figure 2.3-12. L-Band Transistor Amplifier-Array

Transistor Device Characteristics

Bipolar transistors have been constructed using both gold and aluminum metallization. In recent years, gold metallization techniques have advanced rapidly where failure due to electromigration is exceedingly small. Once a good metal system is formed, cautions are taken to design the transistor to have low current density and low junction temperature at the required power level in order to preserve the high MTBF. The metal fatigue function of junction temperature is shown in Figure 2.3-13 and of output power is shown in Figure 2.3-14.

The TRW SB-2000 has proven to be a good design based on the above characteristics. Therefore, it is recommended for use in the module for the UAR System. Additional detailed information describing the transistor is included in Appendix C. Also, other information regarding gold metallization techniques can be found in final report, No. NADC-76108-20.

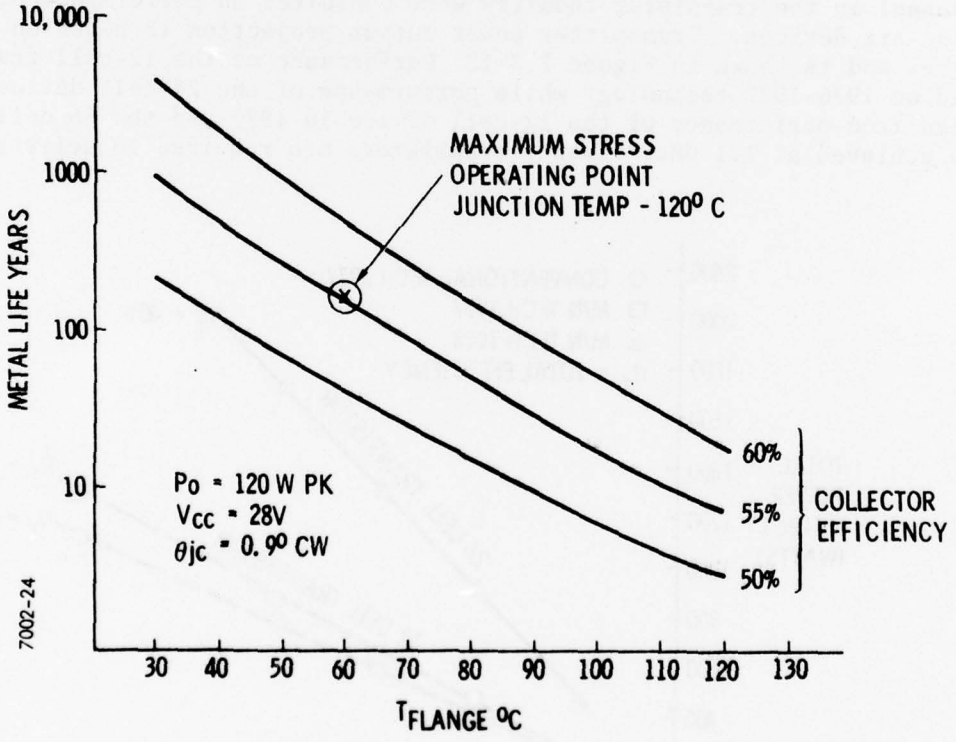

Figure 2.3-13. Transistor Life Time vs Flange Temperature (Projected)

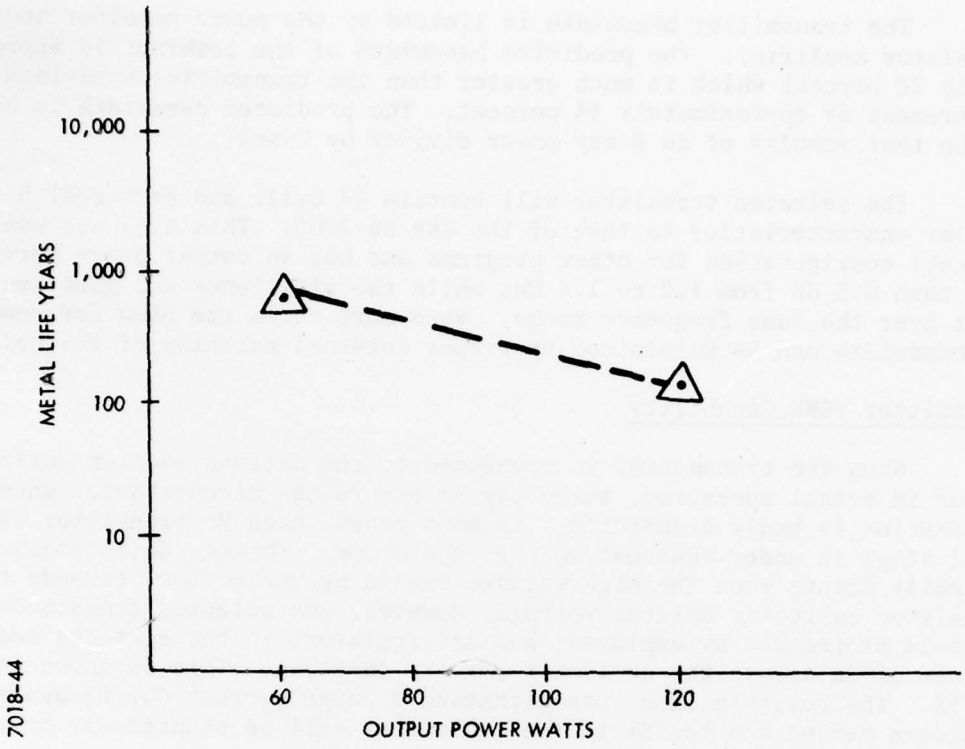

Figure 2.3-14. Transistor Life Time vs Output Power (Projected)

Transmitter Efficiency

Transmitter efficiency is related directly to collector efficiency and gain of each stage, and inversely to the combiner loss of each stage. Assuming that collector efficiency is the same for each stage, efficiency of the transmitter can be calculated as follows:

$$N_T \simeq \frac{N_c \, \alpha}{1 + \frac{1}{G_1} + \frac{1}{G_1 \, G_2}}$$

where

N_T = total efficiency

N_C = collector efficiency

α = combining efficiency factor

G_1 = gain of last stage

G_2 = gain of driver stage.

The total efficiency is 40 percent when $N_C = 0.55$, $\alpha = 0.91$, $G_1 = 5$ and $G_2 = 5$.

Transmitter Bandwidth

The transmitter bandwidth is limited by the power combiner and the transistor amplifier. The predicted bandwidth of the combiner is approximately 20 percent which is much greater than the transmitter bandwidth requirement of approximately 14 percent. The predicted bandwidth is based on the test results of an 8-way power divider by Gysel.

The selected transistor will contain 24 cells and each cell has similar characteristics to that of the TRW SB-2000. This cell was used in a six-cell configuration for other programs and has an output power spread of less than 0.3 dB from 1.2 to 1.4 GHz while the efficiency and gain are constant over the same frequency range. When more cells are used for combining, the bandwidth can be maintained by proper internal matching of the cells.

Transmitter VSWR Capability

When the transmitter is connected to the antenna section during testing or in actual operation, there may be unforeseen circumstances where the termination is badly mismatched. In most cases, each RF transistor in the final stage is under abnormal voltage and thermal stress. Catastrophic failure generally occurs when the high voltage caused by reflection, exceeds the rated transistor collector emitter voltage. However, the selected transistor has built-in protection by employing ballast resistors in the elements and placing a shunt diode across the collector emitter junction. This is shown in Figure 2.3-15. The built-in diode can withstand a large current during avalanche breakdown period and the B+ to the transistor will be shunted-off by a command from the logic box.

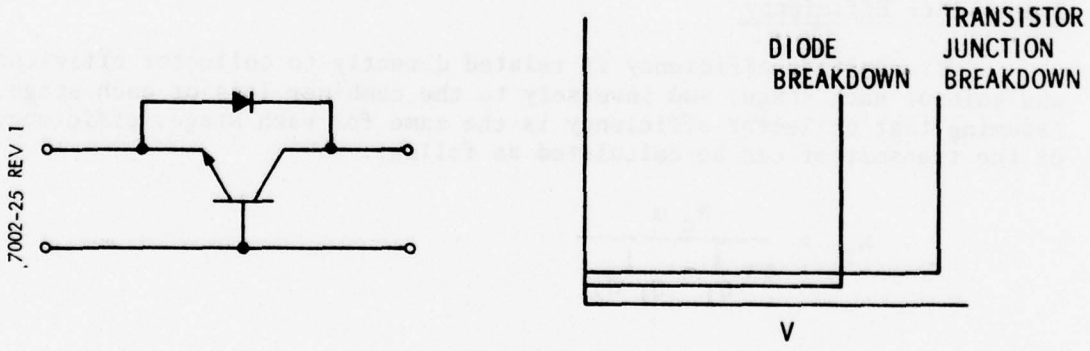

Figure 2.3-15 (a). Transistor Protection With Diode at High VSWR
(b). Breakdown Characteristics of VSWR Protected Device

Thermal Stress Characteristics

The transmitter failure rate is directly related to the thermal stress in the transistors. Maximum MTBF is obtained when the transistor junction is operated in a safe, low temperature region. The thermal stress will be small because of the low thermal resistance from the junction to the flange when

operated under pulse conditions. A 12 cell SB-2000 has a thermal resistance of 1.13 degrees centigrade/watt under CW condition and 0.79 degrees/watt under pulse conditions. Based on this, the 24 cell device is expected to have a peak power thermal resistance of less than 0.5 degree centigrade/watt. The delta rise of junction temperature at full operating power will be less than 30° centigrade. A predicted thermal resistance of a 24-cell unit is shown in Figure 2.3-16.

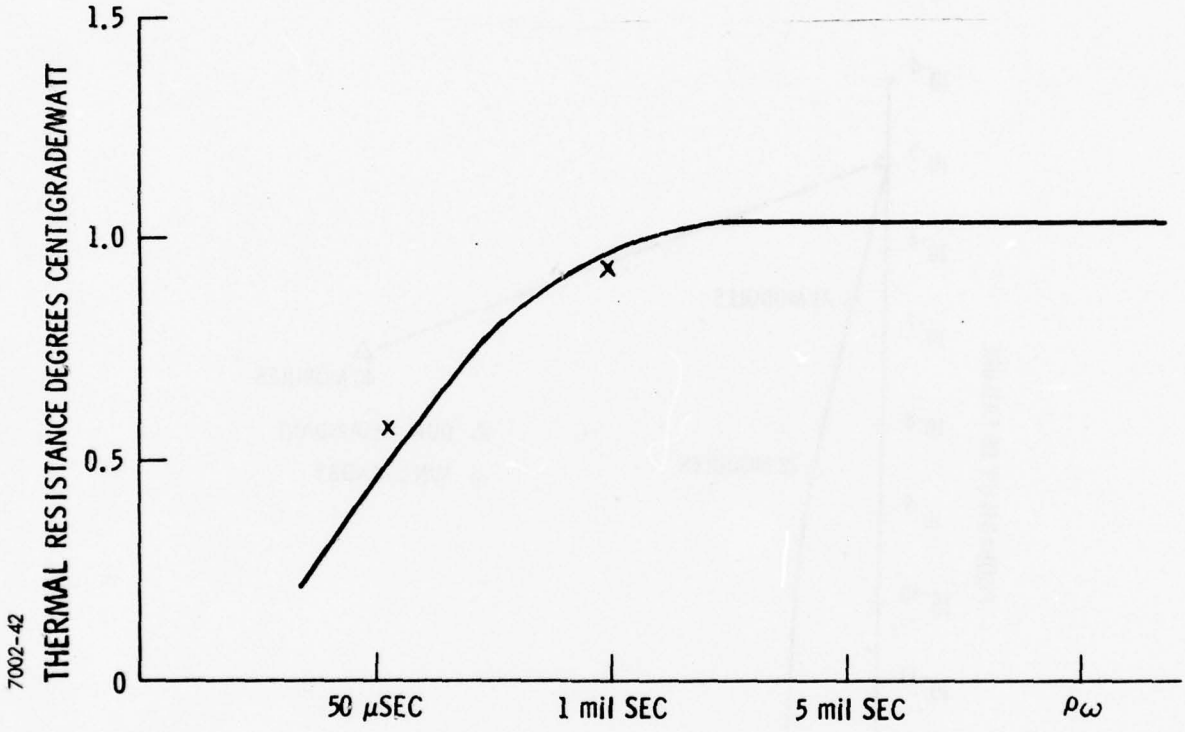

Figure 2.3-16. Thermal Resistance vs Pulse Width

2.3.4 Reliability/Maintainability

The M/N automatic standby configuration has a very low module failure rate, only 3.9×10^{-9} with two standby modules. This has a large impact on life cycle cost and allows a large margin for individual module failure rate. The concept of using active redundant modules to extend reliability has been widely accepted. The common technique is to have a redundant module for each device. This is very impractical because of the high cost in using twice the number of modules plus the additional cost of size, weight and inefficiency.

Let us assume that using one active redundant module per module is permissible. A comparison of reliability can be made between the dual redundant and the M/N automatic standby configuration by using the same basic module in both cases and setting M = 20, N = 2 in the M/N configuration. The dual redundant configuration, which contains 40 modules, has a failure rate of at least one order of magnitude higher than the M/N configuration. A comparison chart is shown in Figure 2.3-17. As mentioned previously, the M/N configuration provides constant RF output when the number of failure modules is less than N. Moreover, when the failure rate count is greater than N, the RF output decreases softly. The approximate output versus the number of failure modules is shown in Figure 2.3-18.

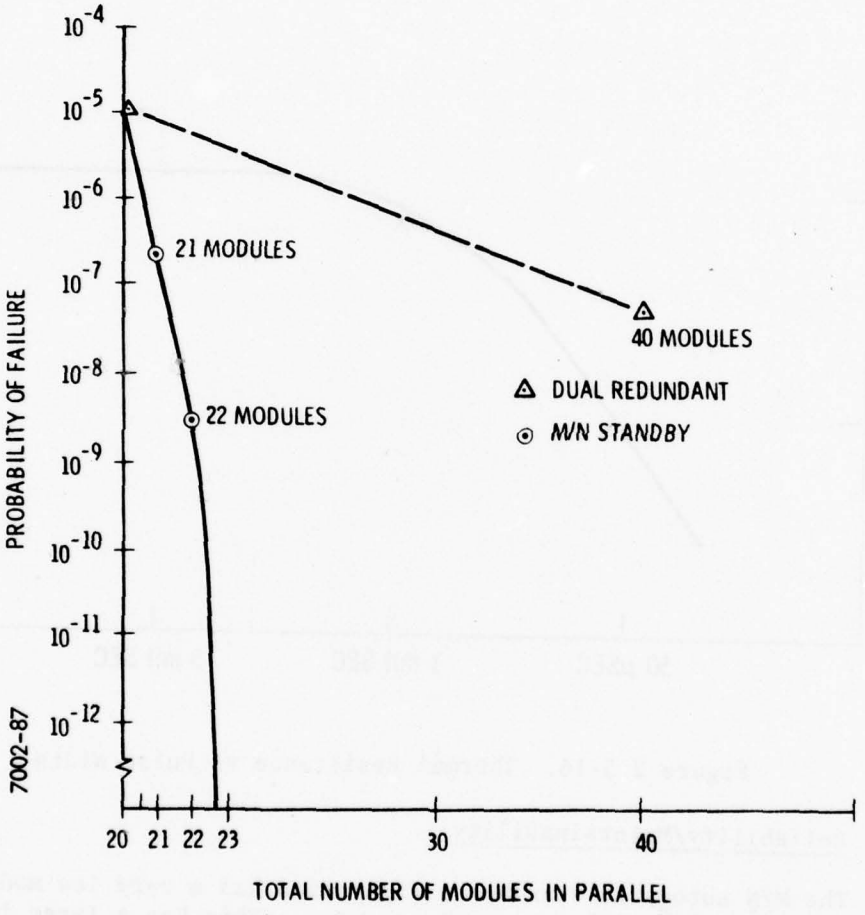

Figure 2.3-17. Comparison of Module Reliability...Dual vs M/N Configuration

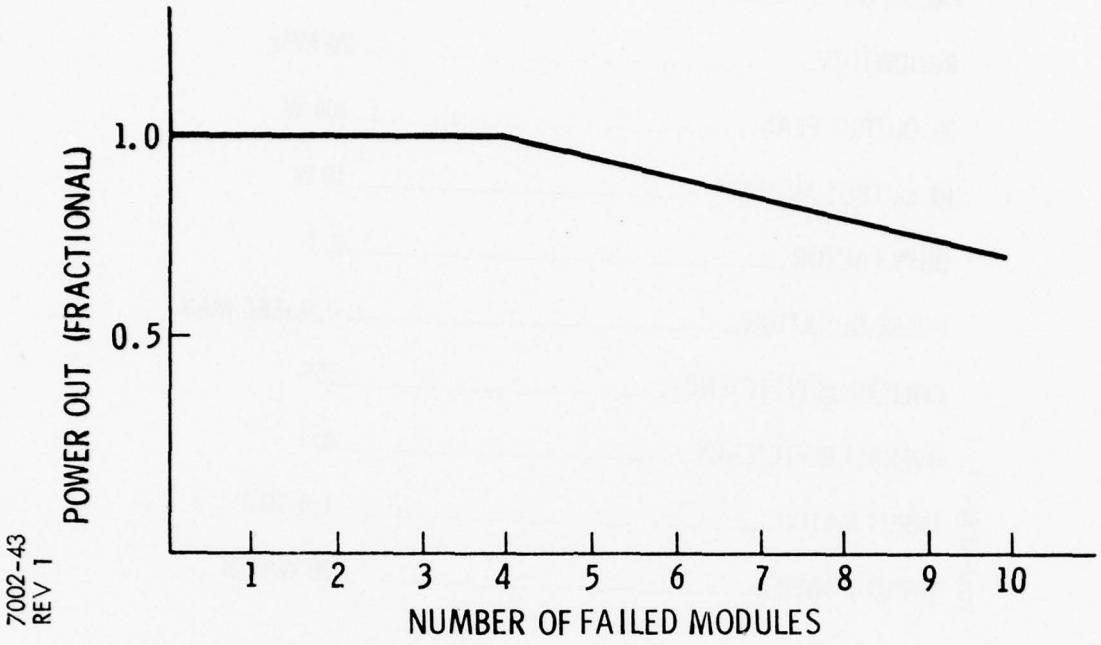

Figure 2.3-18. Fractional Power Out vs Module Failure

The transmitter should be designed such that active components or modules can be readily replaceable. The amplifier module will have two RF connectors, one receptacle and four mounting holes. Replacement of a module involves identifying the failed unit by observing the digital readout and then removing the inoperative unit. A new unit can be installed and followed with a digital checkout. Smaller RF components can be replaced in the same manner as changing a plug-in crystal.

2.3.5 IFF Transmitter

The transistor module for the IFF transmitter uses the same transistors that were designed for modules of the main transmitter, and the input and output matching circuit of the module is tailored for the IFF frequency. Requirements for the IFF transmitter for the UAR System can be met by using bipolar transistor amplifiers. A list of requirements is shown in Table 2.3-3. The transmitter will have one normal operating channel and one standby channel. The monitoring and switching mechanism is similar to that of the radar transmitter. The module construction is different only in input and output matching because of different frequency range requirement. Although a transistor with different geometry and no internal matching may be adequate, it is an advantage to use the same device to avoid additional quality control of a separate item.

TABLE 2.3-3. IFF TRANSMITTER PARAMETERS

FREQUENCY	1030 MHz
BANDWIDTH	20 MHz
RF OUTPUT PEAK	100 W
RF OUTPUT AVERAGE	10 W
DUTY FACTOR	0.1
PULSE DURATION	0.9μSEC MAX
COLLECTOR EFFICIENCY	55%
OVERALL EFFICIENCY	45%
INPUT MATCH	1.5 TO 1
INPUT POWER	20 WATTS

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Peak power output of a 24 cell transistor is 120 watts. Thermal resistance of the device is less than one degree centigrade/watt for any pulse duration of less than 100 microseconds. Therefore, the junction temperature will always be well below the safe operating region. There are two stages of amplification which will have a total gain of approximately 14 dB. Therefore, the amplifier module will have a total efficiency of greater than 40 percent, assuming the collector efficiency is at 55 percent.

2.4 UAR FREQUENCY SYNTHESIZER DESIGN

2.4.1 Tradeoff Studies

Frequency agile radars require programming of local oscillator frequencies over wide bandwidths typically 200 MHz. In addition, the radar hopping scheme is such that comparatively fast settling times at each frequency are required, typically to within 0.03 degree of the final phase in 50 μsec. The additional requirements for very low phase noise and spurious output on each local oscillator make the synthesizer design an exacting task.

Synthesizer Configurations

There are two basic synthesizer configurations which are applicable to radar local oscillator design: direct and indirect. Most present designs use standard direct synthesizers which depend on selecting a frequency from a multitude of pre-existing oscillator frequencies and mixing via sum and difference modes to produce the desired output frequency.

This direct frequency technique (crystal matrix oscillators) meets most radar requirements very well, but with increasing costs in design and test this matrix approach is reaching a limit of its capability. Since the crystal oscillators are always in the on position, frequency switching speed can be quite rapid (approximately 10 μsec).

The existence of many simultaneous frequencies, however, presents a problem in maintaining a spurious-free output. The spectral purity of the output depends, to a large degree, not only on the reference, but on: select and sum scheme, selector switch isolation, mixer intermodulation, and filter rejection characteristics. As the radar bandwidth requirements increase, the direct synthesizer becomes less able to maintain an acceptable spurious-free output.

The direct synthesizer is relatively bulky and costly due to the large number of mixers, amplifiers, switches, oscillators, and filters used. The indirect approach uses a voltage-controlled oscillator to set the different frequencies required. It is inherently simpler and less expensive than the direct matrix approach. In addition, it can produce an output signal of high spectral purity since the output is taken directly from a fundamental tunable oscillator, which is locked to a stable reference.

Tradeoffs

A comparison of the two types of synthesizers is shown in Table 2.4-1. The indirect synthesizer is clearly superior in most operational characteristics and was selected for the UAR synthesizer design approach.

Several types of phase locked loop configurations were studied, including the analog loop, digital loop, and multiple/hybrid loop types. Table 2.4-2 summarizes the characteristics of each type.

Operational requirements for the UAR impose the following requirements on the synthesizer.

Frequency Bandwidth	185 MHz
Minimum Step Size	0.75 MHz
Frequency Settling Time	50 μsec to within 0.03^{o} of the final phase
Phase noise for 60 dB improvement factor	0.09^{o} *rms*

The multiple phase locked loop was selected since it satisfies the above-mentioned critical parameters.

TABLE 2.4-1. FREQUENCY SYNTHESIZER TRADE-OFF CHART

	DIRECT SYNTHESIZER	PHASE LOCK LOOP SYNTHESIZER
COMPLEXITY	MOST COMPLEX, UTILIZES LARGE NUMBERS OF OSCILLATORS, MIXERS AND AMPLIFIERS	RELATIVELY SIMPLE, UTILIZES VCO TO COVER FREQUENCY RANGE
COST	HIGH	LOW
REPAIRABILITY	MORE COMPLEX BITE	SIMPLER QUICK MODULE REPLACEMENT
RELIABILITY	HIGH PARTS COUNT SOME INHERENT REDUNDANCY	LOW PARTS COUNT, NO INHERENT REDUNDANCY
PERFORMANCE	FAST SWITCH TIME, HI SPURS	SLOWER SWITCHING TIME LOW SPURS
RFI	DIFFICULT TO FILTER	SIMPLE FILTERING
POWER CONSUMPTION	HIGH	RELATIVELY LOW
COMMONALITY	REQUIRES CRYSTAL CHANGE FOR OTHER FREQUENCIES	DIGITAL TUNING, COMMON UNIT FOR ALL FREQUENCIES
FLEXIBILITY	HARDWARE CHANGE FOR FREQUENCY PROGRAM CHANGE	DIGITAL PROGRAMMING, EASY CHANGE OF FREQUENCY PROGRAM

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2.4.2 Baseline Synthesizer Description

The synthesizer supplies all local oscillator frequencies to the various receivers. The block diagram of Figure 2.4-1 shows the basic configuration for generating these frequencies from the master reference.

A crystal oscillator at 171.666 MHz followed by a SAW filter supplies the stable reference for coherent frequency processing by the multiplier and phase locked loops. All the fixed frequencies are generated by direct multiplication and filtering from the reference. The IFF receiver requires 1030 MHz or 6x the reference. The transmitter exciter and receiver COHO signals are derived from the reference by dividing by six and then multiplying x17 to obtain 486.3 MHz. Power splitters and circulators provide isolation between the various local oscillators, to keep spurs and interaction to a minimum.

TABLE 2.4.2. PHASE LOCKED LOOP COMPARISON CHART

	Simple Analog	Simple Digital	Multiple Loop	Multiple/ Hybrid
Step size	100 MHz	10 MHz	< 10 KHz	< 10 KHz
Settling time	10 µsec	50 µsec	50 µsec	30 µsec
Spurious purity	best	very good	good	good
Phase Noise	best	very good	good	good
Cost	lowest	low	high	high
Complexity	simplest	simple	complex	complex
Bandwidth	> 500 MHz	≤ 200 MHz	> 500 MHz	> 500 MHz

The main receiver tunable local oscillator frequencies are obtained from a dual phase locked loop configuration. The frequency range covered at the synthesizer output is 730 MHz to 915 MHz in 0.75 MHz steps. The coarse phase locked loop can increment in 7.5 MHz steps over the full 180 MHz frequency range, while the fine phase locked loop increments in 0.75 MHz steps over a 7.5 MHz range so that complete coverage is obtained by the addition of both loops.

The 9.53 MHz reference is obtained from a divide by six and a divide by three from the master reference. The relatively high reference frequency assures wide bandwidth, low spurious outputs, and low phase noise. The output frequencies of the phase locked loops are set by input lines to the programmable counters. The final output is obtained directly from a low noise, fast slew voltage controlled oscillator, so that there is no further multiplication or mixing to degrade spurious and noise output.

The complete synthesizer consists of three field replaceable modules for quick replacement. These consist of the multipliers, coarse phase locked loop, and the fine loop. Figure 2.4-2 is an artist's concept of the packaging to be used for both the synthesizer and receiver modules.

Synthesizer Bite

Built-in test will identify failure of any module, and module replacement requires no tuning or adjustment. BITE for the synthesizer will be accomplished by continuously monitoring outputs of the individual modules with a power detector and comparator. When the level drops below the minimum allowable value a fault signal will be transmitted.

The phase locked loops will also have indicators to identify loss of lock.

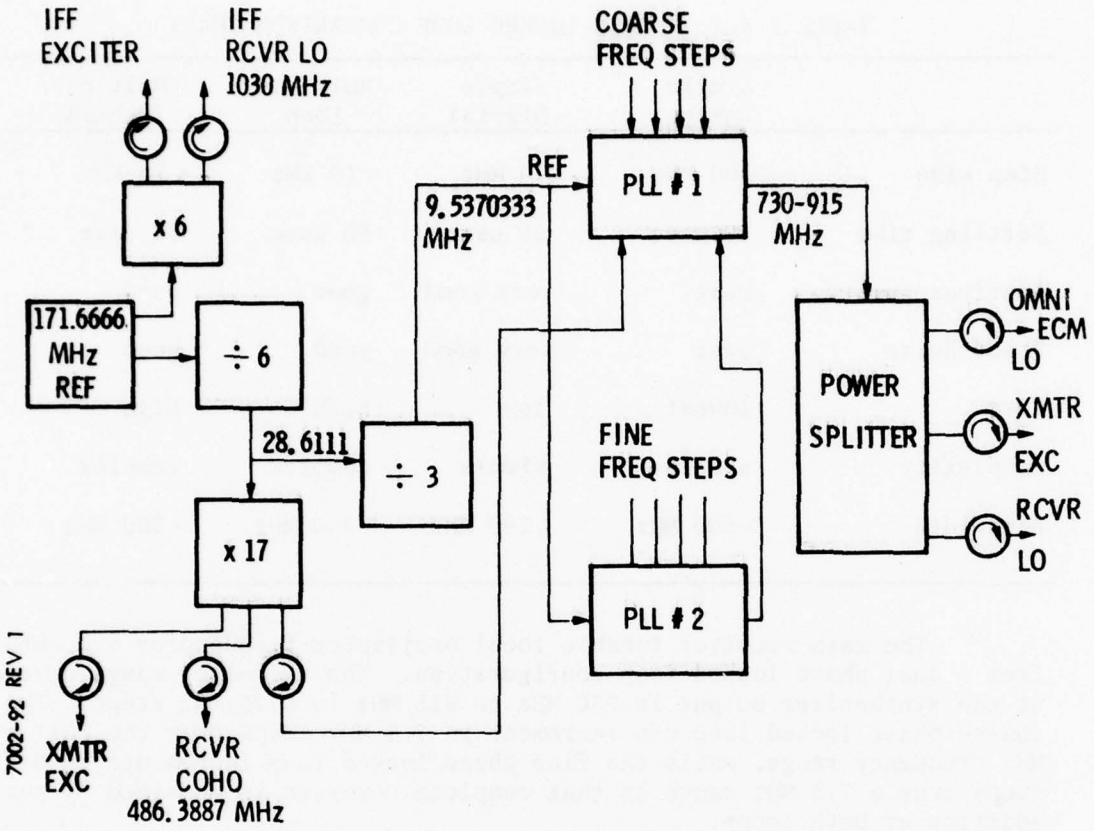

Figure 2.4-1. UAR Frequency Synthesizer

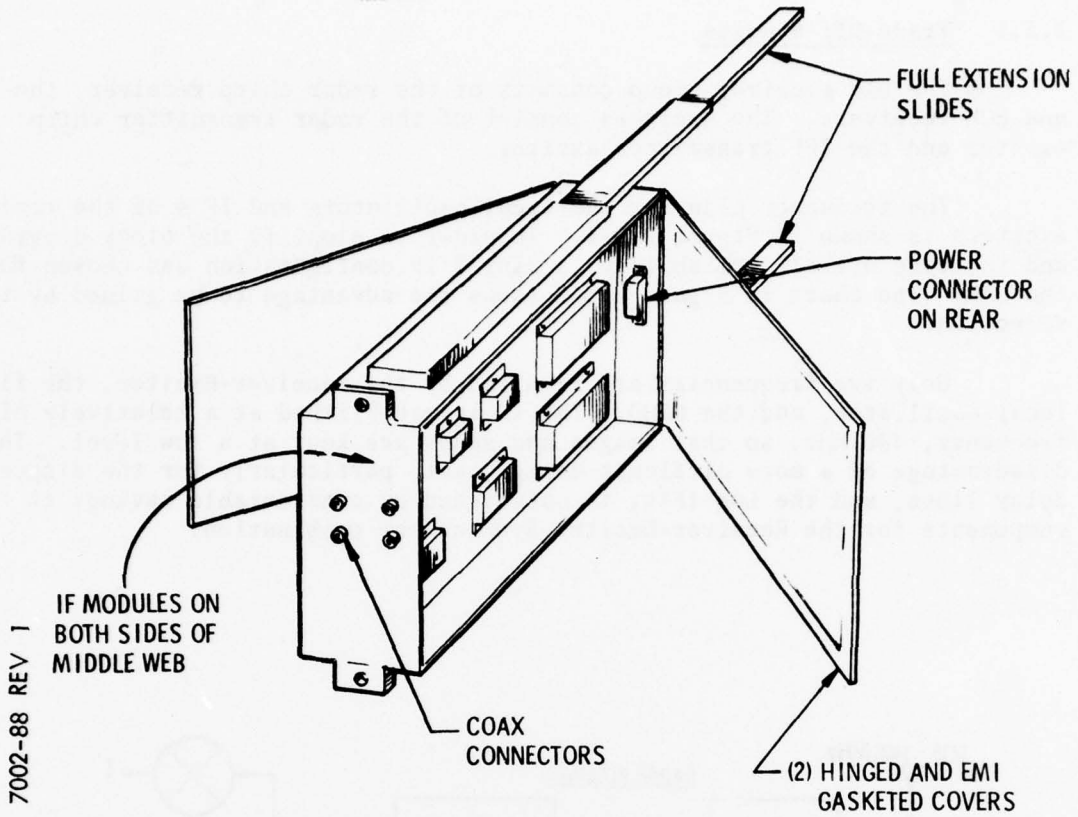

Figure 2.4-2. Synthesizer and Receiver Modules

2.5 UAR RECEIVER DESIGN

2.5.1 Trade-Off Studies

The UAR receiver group consists of the radar chirp receiver, the IFF, and ECM receivers. The exciters consist of the radar transmitter chirp exciter and the IFF transmitter exciter.

The frequency plan for the local oscillators and IF's of the receiver exciters is shown in Figure 2.5-1. In order to simplify the block diagram and increase overall reliability, a single IF configuration was chosen for the UAR. The chart in Figure 2.5.2 shows the advantage to be gained by this selection.

Only two frequencies are required by the Receiver-Exciter, the first local oscillator, and the COHO. The IF is established at a relatively high frequency, 486 MHz, so that images and spurs are kept at a low level. The disadvantage of a more difficult design task, particularly for the dispersive delay lines, and the Log IF's, is outweighed by considerable savings in components for the Receiver-Exciter-Synthesizer combination.

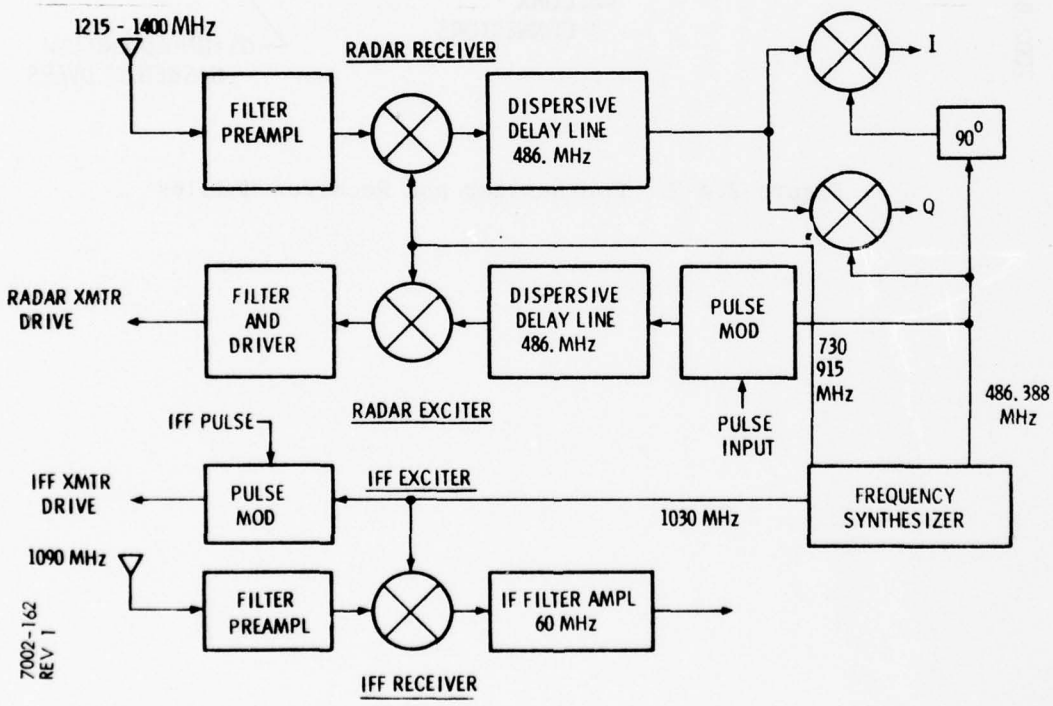

Figure 2.5-1. UAR Receiver-Synthesizer Local Oscillator Plan

	SINGLE IF	DUAL IF
CIRCUIT COMPLEXITY	SIMPLER	MORE COMPLEX
SPECIAL DESIGN REQUIREMENTS	SAW DISPERSIVE DELAY LINE AT 486 MHz	NONE
SPURS	GOOD	POOR DUE TO DUAL CONVERSION
SYNTHESIZER REQUIREMENTS	ONE LO, ONE COHO	MORE FREQUENCIES REQUIRED
RELIABILITY	BETTER, LOWER PARTS COUNT	10 PERCENT MORE PARTS LESS RELIABLE
TOTAL RCV - SYNTH SIZE, WEIGHT AND POWER	LOW	HIGH
RFI SUPPRESSION	SIMPLER	MORE DIFFICULT

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Figure 2.5-2. Receiver Trade-Off Chart

The IFF receiver-exciter requires a single frequency at 1030 MHz, for transmission, and converts the received signals at 1090 MHz to a 60 MHz IF.

2.5.2 UAR Receiver Description

Radar Receiver

The main radar receiver block diagram appears in Figure 2.5-3. The incoming received signals are applied to a diode limiter which also acts as a variable gain element for the STC function. A bandpass filter covering 1215 to 1400 MHz eliminates the image and minimizes spurious reception. The RF Amplifier provides the necessary gain for establishing the noise figure of the receiver.

The converted signal following the first mixer is at 486 MHz and is made available via a buffer amplifier to the main receiver processing and to the ECM IF Log Amp. The main IF channel feeds a SAW dispersive delay line which correlates the received RF waveform. IQ demodulation is accomplished by dual balanced phase detectors with quadrature COHO signals. The IQ is then fed to the digital processor.

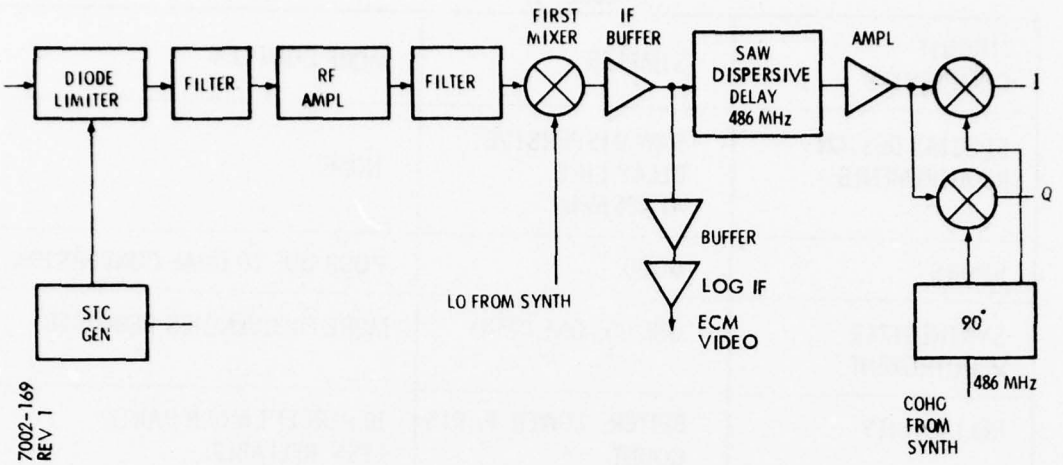

Figure 2.5-3. Radar Receiver Block Diagram

The radar ECM portion consists of a Log IF Channel having a 60 dB dynamic range. The radar receiver is packaged in two field replaceable modules similar to those used for the synthesizer. The input components through the first mixer IF buffer and ECM Log IF comprise one module, while the SAW delay line, and the COHO demodulator make up the second module. BITE will isolate any faults to the module level of the receiver. The input LO and COHO signals are monitored by a power detector and comparator. If these levels drop below the minimum, the fault is localized to the synthesizer or interconnecting cables.

An RF pulse sample from the exciter is applied to the input of the receiver just preceding the dead time. The IF output following the first mixer is monitored for proper pulse amplitude by a detector and a comparator. A fault signal is generated for low-level or no-pulse amplitude. Similarly the BITE pulse is monitored at the input and output of the second module for improper level. During the time of the generation of the BITE RF pulse, the radar transmitter driver amplifier is turned off to prevent front end limiting.

ECM Receiver

The ECM receiver gets its input from the omni Antenna and generates a log video for comparison with the ECM video received via the main antenna and radar receiver.

The ECM Receiver is identical to the radar receiver first module which houses all the components through the first mixer and Log IF.

2.5.3 Radar Exciter Description

The radar exciter supplies the chirp pulse at the transmit frequency to the transmitter. A block diagram of the radar exciter is shown in Figure 2.5.4

The input CW signal at 486 MHz from the synthesizer is pulse-modulated with the main radar transmitter video pulse. The pulse modulator consists of a cascaded pair of double balanced modulators acting as switches. The output of the modulator is an RF impulse centered at the center frequency of the dispersive delay line which follows. This SAW "chirp" line produces a non linear FM pulse which is subsequently limited and gated to establish the pulse-width of the RF pulse. The mixer upconverts the 486 MHz pulse to the proper transmit frequency in the 1215 to 1400 MHz range. The final filter and amplifier limit the spurious signal and provide proper level for the radar transmitter.

The BITE for this module consists of amplitude monitoring circuits for all input signals which include the first local oscillator, the 486 MHz, the radar transmitter video pulse, and the gated limiter video input. The output RF pulse is monitored at each pulse period. Any dropout is transmitted to the system fault monitoring module.

2.5.4 IFF Receiver Exciter Description

IFF Receiver

The IFF Receiver/Exciter block diagram is shown in Figure 2.5-5. The IFF received signal is applied through a diode limiter and 1090 MHz bandpass filter to the RF amplifier which sets the noise figure of the receiver. The converted signal following the first mixer is fed to a 60 MHz filter and log amplifiers. The IFF video pulses appearing at the output are routed to the IFF processor.

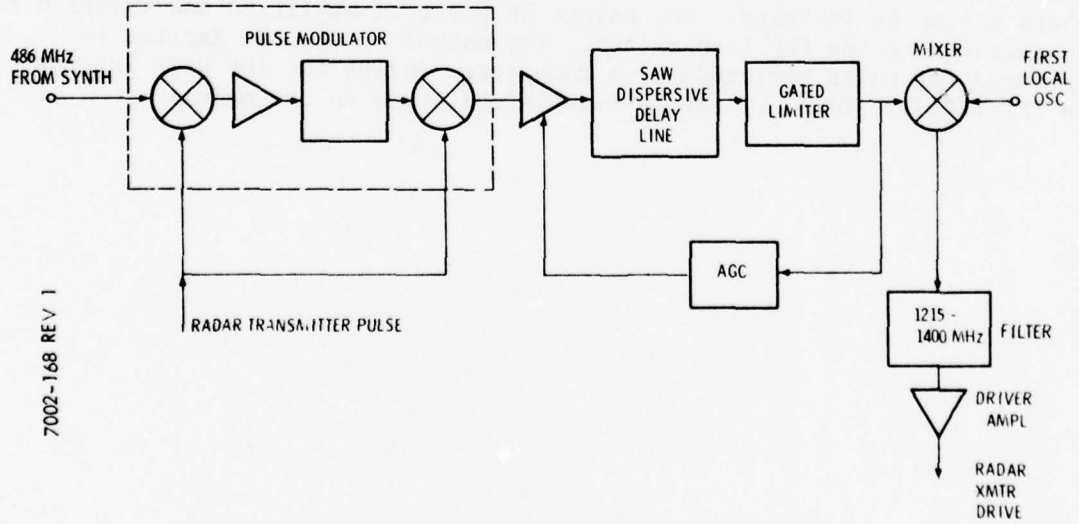

Figure 2.5-4. Radar Exciter Block Diagram

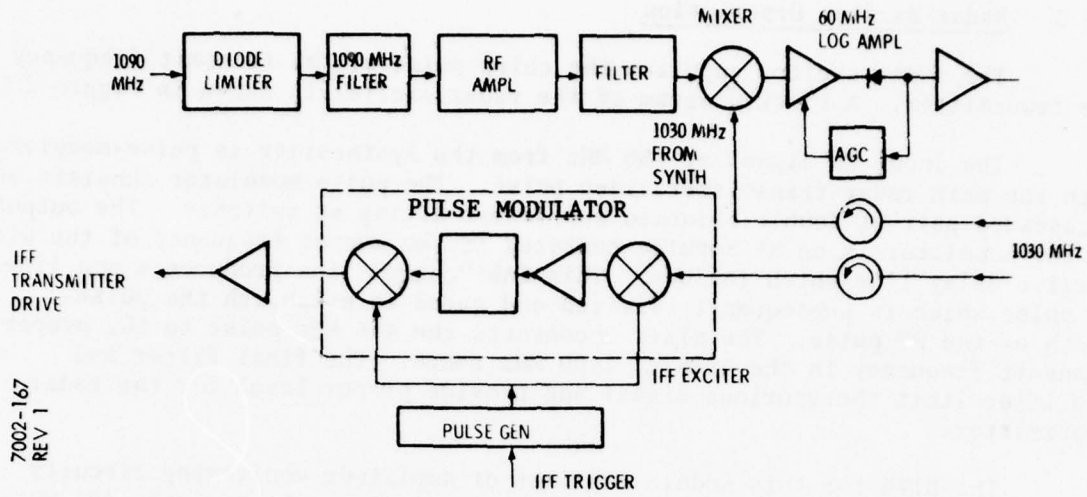

Figure 2.5-5. IFF Receiver/Exciter Block Diagram

BITE

A BITE pulse at 1090 MHz is fed into the input of the IFF receiver at periodic intervals. This test pulse is generated by mixing the 1030 MHz pulse from the IFF exciter with 60 MHz from a crystal oscillator. The IFF video output line is monitored during the IFF BITE period for amplitude with a comparator. A fault signal is generated if the video pulses drop below a specific amount. The 1030 MHz from the synthesizer is also monitored for incoming power level.

IFF Exciter

The 1030 MHz from the synthesizer is pulse modulated by the IFF pulse train. The modulator consists of a cascaded pair of double balanced modulators acting as switches. The output RF pulse is amplified and filtered for transmission to the IFF transmitter. The output of the IFF Exciter is monitored for pulse amplitude by a comparator during the IFF BITE interval. The IFF RECEIVER-EXCITER combination is contained in one module.

2.6 UAR SIGNAL PROCESSOR DESIGN

2.6.1 Requirements

Several system configurations (defined primarily by antenna design and methods of scan) were considered. Relative to design of the signal processor, the most important classification of system design is the division into sequential scanning techniques or intrapulse scanning techniques. The latter is used, in a broad sense, to include both continuous scanning schemes and discrete scanning schemes by use of multiple simultaneous beams.

A possible consideration in the interrelationship between designs of the processor and basic system is the method of extraction of azimuth data. In particular, the choice of monopulse vis-a-vis beam splitting techniques would affect most system elements. In considering accuracy requirements relative to beam size requirements arising from other considerations, it was concluded that monopulse is not required; tradeoffs regarding methods of azimuth data extraction are then confined to the signal processor.

Intrapulse scanning is advantageous from the standpoint of reducing frame time. However, in order to implement intrapulse scanning techniques without prohibitive losses in the process of target detection, a multiplicity of signal processing channels is implied. The added equipment is not considered acceptable from the standpoint of system reliability and excessive power consumption.

Step-scanning with several pulses at each beam position is necessary in order to accommodate rain and snow clutter filtering requirements imposed upon the signal processor. Moreover, given the requirement for moderate filtering of ground clutter via batch processing, a wideband MTI filter has higher loss than a multiple filter bank. Therefore, various options in signal processing were examined on the basis of generating a multiple filter bank. The determination of number of pulses per batch (i.e., per beam position) is subject to the following tradeoffs: (a) number of pulses must be sufficiently small to achieve the required search frame time, considering factors of beamwidth, multiple beams, range coverage requirements, and the necessity for avoidance of blind-speeds in doppler filtering; (b) a large number of pulses improves signal processing, with regard to processing losses and clutter filtering, but at the expense of complexity of the processor; (c) extra pulses within a batch can alleviate processor design complexity and improve rejection of second-time-around clutter at the expense of greater frame time and greater processor losses. Processing losses are roughly the ratio of extra pulses to the total number of pulses within a batch. "Extra pulses" may be either those not processed at all to allow for second-time-around fill time, or those processed in such a fashion that they contribute virtually nothing to the improvement in SNR.

In tradeoffs involving system design, processor design, and system performance, it was determined that approximately eight pulses per batch should be used. A trade-off discussion relating to the number of pulses and the processor design and performance appears in Section 2.6.2.

Pulse Waveform

Some form of pulse compression must be used in order to obtain an efficient transmitter design. In determining the particular pulse compression configuration, tradeoffs must deal with the choice of waveform and methods of implementation of pulse compression for a given waveform. Restricting our choice of waveforms to continuous frequency modulation (either linear or nonlinear), or binary phase coding, the choice of analog or digital implementation was addressed. If nonlinear signal processing of binary phase coded signals is acceptable prior to pulse compression, implementation of pulse compression by digital techniques offers an attractive hardware design. Hard limiting ahead of pulse compresssion also serves the function of CFAR. However, this nonlinear process is significantly more lossy than linear pulse compression with linear CFAR for the time bandwidth products and detection threshold levels studied for application in the UAR system. Assuming linear processing, analog expansion and compression of either waveform using surface acoustic wave (SAW) delay lines results in a more efficient hardware design. This tradeoff consideration among subsystems results in a decision to implement pulse compression in the receiver. Therefore, the trade-offs reported in the next section relative to pulse compression address only the choice of waveforms.

Processing Loss

When considering search radar performance in detecting targets in a noise environment, it is customary to think in terms of power-aperture product as a figure of merit. Tradeoffs are then directed to various costs (economic costs, power consumption, reliability, etc.) of transmitter power versus similar costs of antenna aperture. Losses are also an important factor in cost apportionments among subsystem elements, particularly with regard to processor versus transmitter costs for the UAR system. Where loss can be reduced by increasing the processor complexity, cost of that reduction must be weighed against the cost of an equal increase of transmitter power. We note, however, some processing loss tradeoffs are not related to loss versus processor costs, but loss versus other performance parameters. For example, with pulse compression assumed to be a necessity, some losses incurred in receiver/processor mismatch may be necessary in order to obtain desired time sidelobes. Design for superior clutter performance usually extracts some cost in losses in detection of targets in the clear: performance factors include both doppler filter considerations (reducing sidelobes through weighting), and choice of resolution cell size (small cells reduce clutter but increase opportunities for false alarm). Reduction of CFAR losses can result in a less robust CFAR operation.

Some losses, rather than being the result of performance parameter tradeoffs, result from limitations on processor complexity and, hence, processor cost factors: losses increase with quantization granularity of sampling in both time and amplitude dimensions. The number of filters within a filter bank along with methods of combining outputs of the filters and accomplishing subsequent noncoherent integration are factors in determining filter straddle losses, collapse loss and integration loss. A goal for these losses plus CFAR loss is 3.5 dB.

Review of Signal Processor Requirements

With reference to the above discussion and prior performance discussion, processor requirements as established by system/subsystem tradeoffs leading to baseline designs are listed in Table 2.6-1.

TABLE 2.6-1. PROCESSOR REQUIREMENTS

Input Characteristics	
Pulses per Batch	∿8
Pulse-Batches/Beam/Beamwidth	∿3
Compressed Pulsewidth	∿1.33 μsec
Average Interpulse Period	∿750 μsec
Dynamic Range (clutter to rms noise)	> 50 dB
Rain Clutter Spectrum	-350 to +350 Hz
Filter Performance Requirements	
Ground Clutter Improvement Factor	∿50 dB
Rain Clutter Improvement Factor	∿30 dB
Special Features Required	
CFAR Against Noise, Jamming, Rain Clutter (Rayleigh Distributions)	
Automatic Detection of Targets to ±2400 Knots Velocity and at Zero Radial Velocities if Clear of Clutter	
Clutter Mapping to Remove Residue from High Level Stationary Targets	
ECM Analysis via Jamming Strobe Extraction	
Automatic Switching of Redundant Filter Channels	
Processing of IFF Data and Correlation with Radar Targets	
Nominal A/D Conversion Parameters	
I&Q Sampling at 1 MHz Rate	
9 Amplitude Bits Plus Sign Bit	
Power Budget Goal	150 watts
Processing Loss Goal	<3.5 dB

2.6.2 Tradeoff Studies

The baseline waveform and processor configuration combine potentials for high reliability with high performance. The ideal waveform for this application would have range sidelobes and processing losses that are low over the full range of target velocities. Principal candidate waveforms were limited to those tending to have these properties, combined with relatively low technical risk. Partial trade study results are shown in Figure 2.6-1. One waveform considered is constant amplitude linear FM with an expanded pulse duration of 40 μsec, a BT of 30, and a compressed pulse-width of 1.33 μsec. The modified Hamming weighting includes compensation for the Fresnel ripple in the transmitted waveform giving range sidelobes with zero doppler shift of -35 dB. Although this waveform tends to be doppler tolerant, the compensation required for lower range sidelobes with zero doppler shift results in some degradation in range sidelobes (about 5 dB) with maximum doppler shift. Because the transmitted waveform and receiver response are somewhat mismatched, S/N ratio losses are not insignificant (1.3 to 1.4 dB). A nonlinear FM waveform was adopted for the baseline because operation under more nearly matched conditions is possible. Low range sidelobes for zero doppler shift can be obtained with a suitable combination of weighting and Fresnel ripple compensation. Also, S/N ratio

CANDIDATE WAVEFORMS	RANGE SIDELOBES (dB)		S/N RATIO LOSSES (dB)	
	STATIONARY CLUTTER	MAXIMUM VELOCITY TARGET	ZERO RADIAL VELOCITY TARGET	MAXIMUM VELOCITY TARGET
LINEAR FM (T = 40 μsec, BT = 30, HAMMING WEIGHTED WITH FRESNEL RIPPLE COMPENSATION)	-35.0	-30.0	1.3	1.4
NONLINEAR FM (T = 40 μsec, BT = 30, TAYLOR WEIGHTED GROUP TIME DELAY FUNCTION WITH FRESNEL RIPPLE COMPENSATION)	-35.0	-14.0	0	1.0
BINARY PHASE CODE (13 BIT BARKER, T = 35.75 μsec)	-22.3	-5.0	0	2.3

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Figure 2.6-1. Waveform Comparison Data

losses can be quite small over the entire range of doppler frequencies. However, the range sidelobes become degraded for maximum doppler shift (from -35.0 to -14.0 dB). The 13-bit Barker code was included because at zero doppler the range sidelobes are fairly good for waveforms of this type, and the S/N ratio losses can be very low. However, at maximum doppler, the losses become significant (2.3 dB) and the range sidelobes deteriorate drastically (from -22.3 to -5.0 dB).

The baseline UAR signal processor is shown in Figure 2.6-2. The I & Q detected video consists of groups of eight pulses each. They are first digitized, then integrated coherently by a bank of eight doppler filters. Each of these filters has a frequency response that is tailored according to its particular passband and clutter rejection requirements. CFAR action is obtained as follows. Each filter output is envelope detected, and then compared with a reference that is proportional to the average of the detected outputs in a group of nearby range cells. The seven non-zero doppler channels are OR'd such that a target occurring in any of the seven channels can be detected. The binary integration shown results from three different pulse groups illuminating every azimuth beam position. The clutter map monitors all detections that occur in fixed range-azimuth zones. If the number of detections in any particular zone exceeds the threshold, the data in that zone is censored. The zero doppler channel is processed in a similar manner. However, activity of the clutter map would tend to be considerably higher because of point ground clutter. The range-azimuth zones and response characteristics of the zero doppler clutter map are chosen such that aircraft

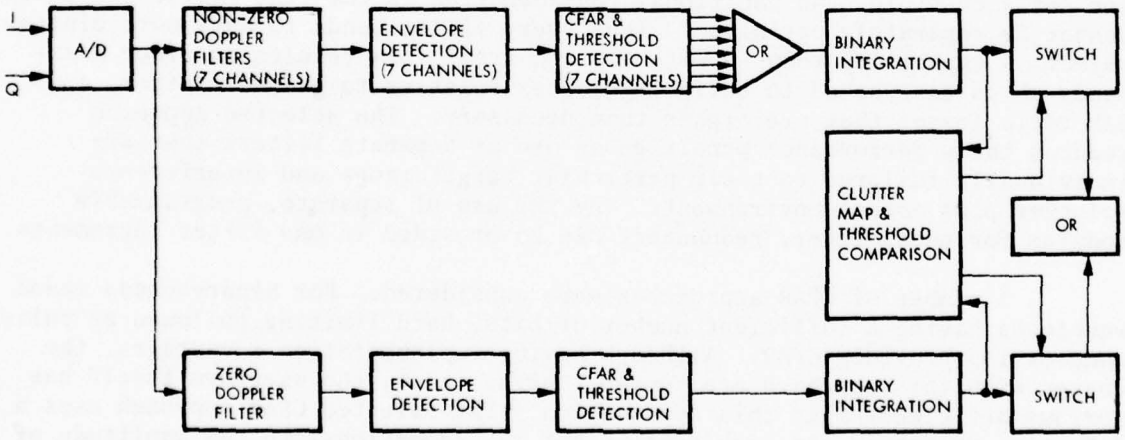

Figure 2.6-2. Baseline UAR Signal Processor

targets having zero doppler are not censored. Finally, uncensored detections occurring in the non-zero doppler channels and the zero doppler channel are OR'ed.

In a broad sense, the total waveform includes the scan program. Selection of both the scan program and signal processing configuration was strongly influenced by the need for highly efficient operation. Thus the scan program provides maximum opportunity for coherent integration consistent with multiple frequency operation and blind speed avoidance. The general approach to coherent integration was influenced by the spectral distribution of the clutter. Being a 2D radar, the elevation beams will provide little spatial filtering of weather clutter. Typically, the lower elevation beam could be illuminating the ocean plus a rain storm cell of maximum vertical extent. The total clutter spectrum would be very broad. Filters that reject narrow bands of clutter only, such as cancellers, are not well matched to the clutter environment. A much better match with respect to clutter rejection can be obtained with filters having narrow passbands (and thus broad clutter rejection bands) tuned to the radial velocities of all possible targets. Thus efficient coherent integration of each group of eight pulses is provided by a bank of narrow band filters. At least three pulse groups are received from each target. Because successive groups are at different frequencies and PRF's, the additional integration is noncoherent.

Two principal approaches were considered in designing the narrow band filter bank. The FFT approach provides eight narrow filters having frequency responses that are identical except for their equally spaced center frequencies. For adequate clutter attenuation, the peak sidelobes should be uniform and down about 50 dB. Overall implementation requirements for this approach are an advantage if the reliability is adequate without redundancy. If not, then redundant filter banks must be provided; the individual filters are not accessible. An additional consideration is that the filter responses cannot be separately optimized. Thus every filter tends to have more clutter rejection capability than is actually required. This results in wider passbands which correspond to eclipsing losses relative to ground clutter, and S/N ratio losses that are higher than necessary. The selected approach reduces these performance penalties by use of separate filters that are individually tailored to their particular target range and interference (clutter plus noise) environments. By the use of separate, programmable modules for each filter, redundancy can be provided in one filter increments.

A number of CFAR approaches were considered. For binary phase coded waveforms having a sufficient number of bits, hard limiting followed by pulse compression provides CFAR. Although having implementation advantages, the losses with this approach are somewhat high. Also, the waveform itself has serious deficiencies in this application. The selected CFAR approach uses a detection threshold for each filter that is proportional to the amplitude of filtered envelopes averaged over a group of adjacent range cells. This approach works well for Rayleigh distributed clutter which is normally expected. A distribution-free approach was also considered which is based on ranking the filtered envelope amplitudes in a similar group of range cells. However, this approach is not feasible with only three samples (pulse groups) per azimuth position.

2.6.3 Baseline Doppler Filtering Description

Doppler filter modules are physically identical for practical redundancy and graceful degradation, and have responses that are separately tailored to meet their individual requirements. When the system is operating with maximum capability, eight doppler filter modules will be in use. Although physically identical, the frequency response of each filter will be tailored to meet the requirements for its particular sub-band. A functional block diagram of the doppler filter building blocks is shown in Figure 2.6-3. During each range sweep, the digital data bus provides I & Q video to all eight filter modules in parallel. Immediately prior to each sweep, each module receives the weight to be used during the next sweep. In the module switch S_1 directs the weight into local storage. During the sweep, this weight is multiplied by the video at the processing rate of 1.5 MHz. If this sweep is the first of a batch of eight, then switch S_2 causes zero to be added to the multiplier output, and S_3 directs 1024 partial sums to be stored according to range. For the Nth range bin, the first partial sum can be called $W_1V_1^N$ where W_1 is the first weight, and V_1^N is the first video sample in the Nth range bin. During the next range sweep, $W_1V_1^N$ is retrieved through S_2 and added to $W_2V_2^N$. Thus, the second partial sum becomes

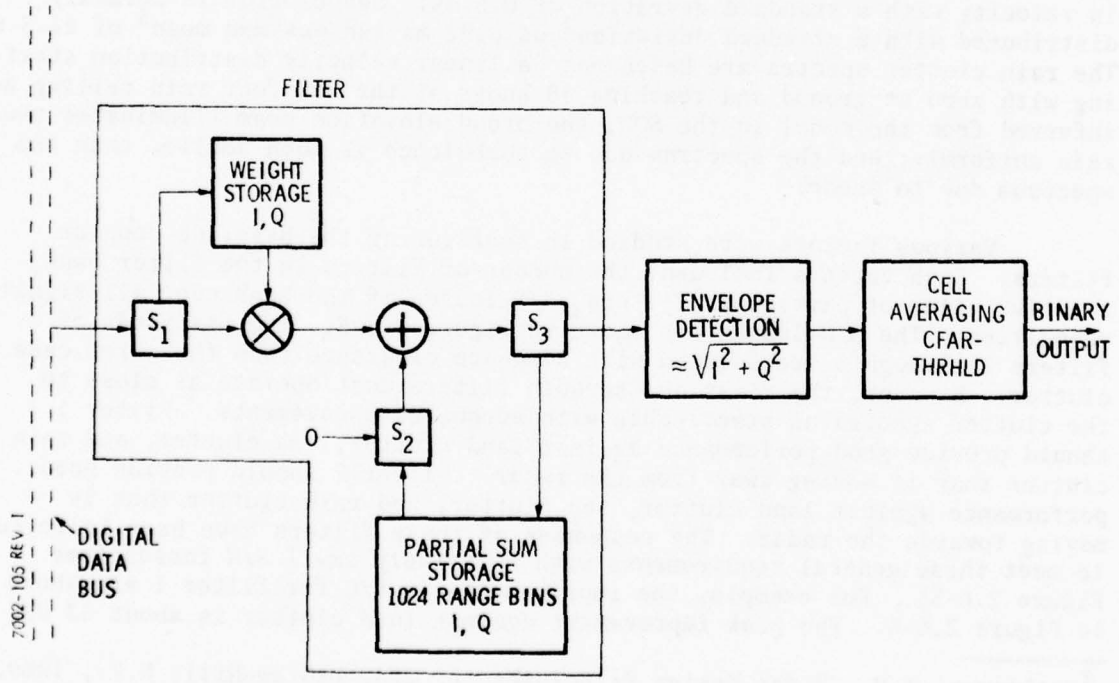

Figure 2.6-3. Basic Building Blocks (Filter, Detector, CFAR)

$W_1V_1^N + W_2V_2^N$. The final (coherent) sum $\sum_{i=1}^{8} W_iV_i^N$ is formed during the eighth range sweep and S_3 switches out this result for further processing. To this point, the processing has been coherent. Phase information has been preserved by the use of I & Q components. As further operations are to be noncoherent, the envelope of the filtered waveform is calculated by an algorithm that approximates $\sqrt{I^2 + Q^2}$. During the last sweep of a pulse group, the envelope data becomes available for all ranges. Every range bin is tested for target presence by a threshold detector in which the threshold has been set by a cell averaging CFAR. The output of the doppler filter modules is the binary result of this test.

The optimum doppler filter would maximize the improvement in signal to total interference (noise plus clutter) ratio. For interference that is distributed uniformly in frequency, a matched filter would be optimum. For the UAR, distribution of the clutter and C/N ratio varies over a wide range. True optimization of filter weights would involve measurement of clutter noise properties and adaptation of weights to optimize detection performance in specific clutter environments. Since the clutter environment can vary appreciably as a function of time and space, the optimization would require very complex hardware - expecially in coping with the variation of environment as a function of slant range.

Filter design was based upon selection of weights for near optimum performance for detection of targets in the combination of land, sea, and rain clutter as illustrated in Figure 2.6-4. Land clutter[1] is normally distributed in velocity with a standard deviation of 0.5 ms. Sea clutter is normally distributed with a standard deviation[2] of 0.92 ms and maximum mean[3] of ±1.5 ms. The rain clutter spectra are based on: a linear velocity distribution starting with zero at ground and reaching 48 knots at the 30K foot rain ceiling as inferred from the model in the SOW; the broad elevation beam illuminates the rain uniformly; and the spectrum due to turbulence is much smaller than the spectrum due to shear.

Various factors were studied in configuring the baseline doppler filters. Such factors included; the number of filters in the filter bank, relative value of particular filters, S/N losses of the bank over all signal velocities. The S/N losses are shown in Figure 2.6-5. The passbands of filters 2 through 6 are located with adequate clearance from the worst case clutter. However, the first and seventh filters must operate as close to the clutter spectra as practicable with adequate improvements. Filter 1 should provide good performance against land clutter, sea clutter, and rain clutter that is moving away from the radar. Filter 7 should provide good performance against land clutter, sea clutter, and rain clutter that is moving towards the radar. The responses of these filters have been tailored to meet these general requirements with relatively small S/N losses (see Figure 2.6-5). For example, the improvements in S/C for filter 1 are shown in Figure 2.6-6. The peak improvement against land clutter is about 53 dB.

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[1] Nathanson, F.E., Radar Design Principles, p. 274, McGraw-Hill, N.Y., 1969.
[2] op cit, p. 243.
[3] op cit, p. 248.

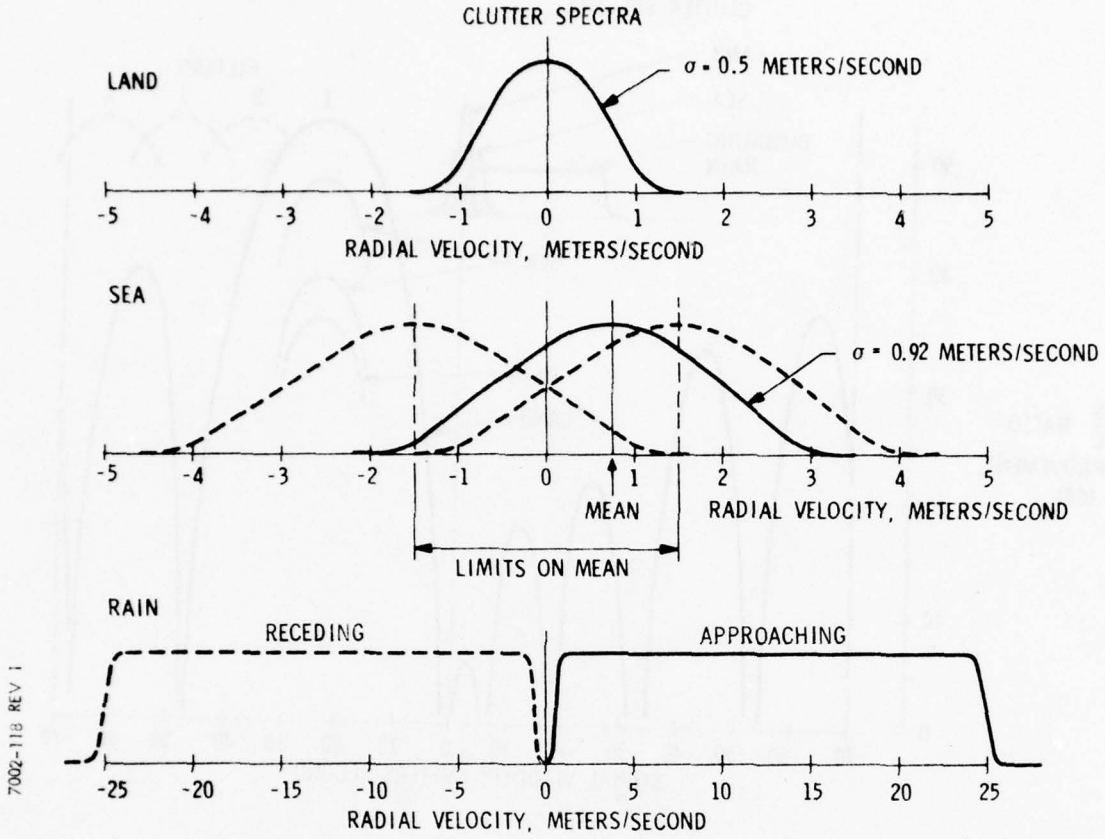
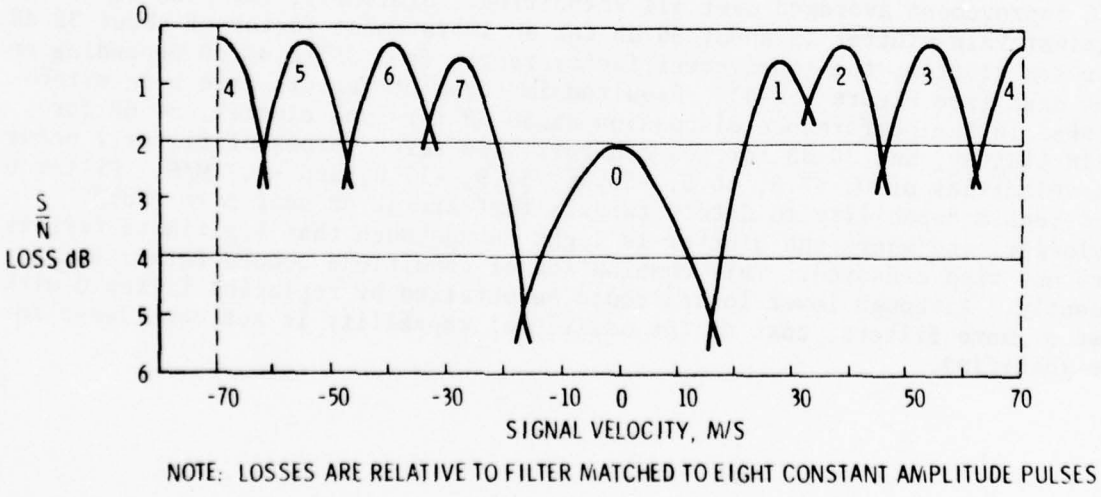


Figure 2.6-4. Clutter Spectra



NOTE: LOSSES ARE RELATIVE TO FILTER MATCHED TO EIGHT CONSTANT AMPLITUDE PULSES

Figure 2.6-5. Doppler Filter S/N Ratio Losses

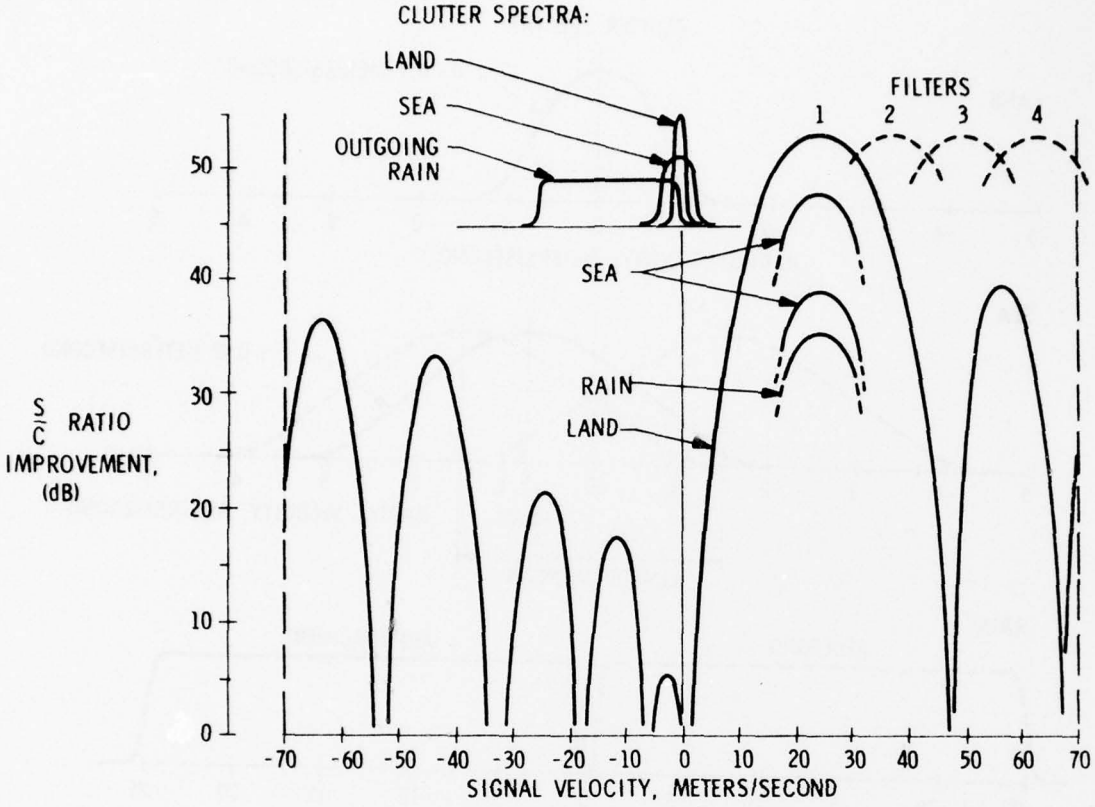


Figure 2.6-6. Filter No. 1 S/C Ratio Improvement

When similar improvements for filters 2 through 6 are included, the improvement factor is about 50 dB, where the "improvement factor" is defined as the S/C improvement averaged over all velocities. Similarly, the peak improvement against rain clutter is about 35 dB for an improvement factor of about 32 dB. For sea clutter, the improvement factor ranges from 36 to 45 dB depending on the mean (see Figure 2.6-4). Required improvement factors have been established in the performance discussion as 50 dB for land clutter, 30 dB for rain clutter, and 30 dB for sea clutter. The seven zeroes of filter 1 occur at velocities of 0, 47.8, 66.5, -53.3, -31.9, -17.9, and -4.7 M/S. Filter 0 provides a capability to detect targets that are at or near zero radial velocity, and where the clutter is light enough such that legitimate targets are not also censored. This combination of conditions occurs rather infrequently. Although lower losses could be obtained by replacing filter 0 with two or more filters, cost of the additional capability is not considered to be justified.

2.6.4 Baseline CFAR Detection

Adaptive clutter filtering and maintenance of a low false alarm rate are accomplished by use of a combination of cell averaging CFAR threshold adjustments and clutter maps.

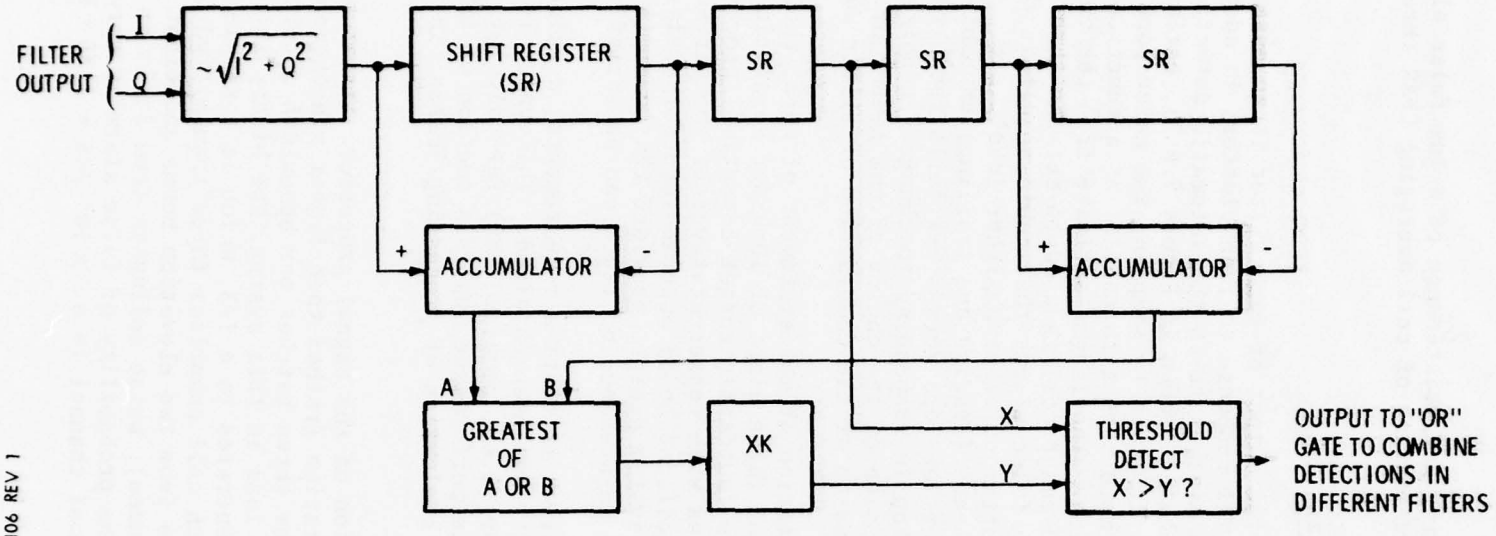
Detection of Targets in the Clear

Application of CFAR to the output of each filter is an essential element for obtaining an adaptive MTI response to rain clutter, in addition to maintenance of a constant false alarm rate in the automatic detection of targets. The CFAR configuration chosen (shown in Figure 2.6-7), estimates the mean of the probability density function by sampling the noise population in the range dimension. This estimate sets a threshold, as a function of the factor K, for threshold detection. The larger estimate from the ensembles that lead or trail the observed range cell is used to set the threshold, thereby avoiding an increase in false alarms that could result at the transition from receiver noise to clutter noise of a higher level, etc. Choice of the number of cells comprising each (leading and trailing) ensemble involves the trade-offs of many cells for low-loss versus few cells for hardware simplicity and better CFAR action in responding to changes in noise statistics as a function of range. Discussion of the choice of the number of cells is deferred until after the discussion of the combination of filter outputs.

From a strict interpretation of the statement of work, there is a requirement for a probability of false alarm of 10^{-6} per resolution cell (range and azimuth) for the ATD (automatic target detection) process operating with a noise input. Discussions with representatives of the Air Force have led us to believe that the specification of intermediate false alarm probability should not govern the system design, provided that overall requirements for track initiation and maintenance of track can be satisfied.

From the analysis of track initiation requirements, a value of P_{FA} per cell of approximately 6.5×10^{-5} has been obtained. This value is used for obtaining the visibility factor (i.e., required SNR) for calculation of maximum detection range, in the performance analysis section of this report. It is also used below for the evaluation of processing losses, including CFAR losses.

In the prior description of the signal processor, it has been established that binary integration (rather than linear noncoherent integration) is used in processing the three batches per beamwidth obtained during the search scan. For minimum loss in this system, the binary integrator (sliding "m/n" detection) degenerates to a 1/3, which is a simple threshold detection. Assuming an azimuth cell comprises three transmitted batches and considering noise collapse from two elevation beams and eight filters (with noise decorrelation assumed), noise collapses from $3 \times 2 \times 8 = 48$, independent sources. Since the probability of false alarm is very small, the required P_{FA} for each individual channel is $6.5 \times 10^{-5}/48 = 1.35 \times 10^{-6}$.



$$\sim\sqrt{I^2+Q^2} \approx \text{MAX}\ [|I|,\ |Q|] + 1/2\ \text{MIN}\ [|I|,\ |Q|]$$

Figure 2.6-7. UAR CFAR Circuit

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With a Swerling 2 target assumed, by virtue of use of frequency agility and elapsed time between batches, the combined losses due to collapse of beam and filter outputs and binary integration rather than linear integration may be found as follows:

A reference visibility factor obtained for a $P_D = 0.854$ (budgeted to yield a 0.95 probability of track initiation), a $P_{FA} = 6.5 \times 10^{-5}$, and three hits for a Swerling 2 model is 10 dB. The visibility factor is then found to be 12.4 dB for a 1/3 binary integrator ($P_D = 0.743$ on each hit) and a $P_{FA} = 1.35 \times 10^{-6}$ resulting from the collapse. The net loss is 12.4 - 10 = 2.4 dB. This loss is tabulated here for reference, but is not included explicitly in the range calculation, because it is implicit in the visibility factor. In order to reduce CFAR loss to 1 dB with the P_{FA} as stated above, it is necessary to obtain a total of 42 independent samples.* Assuming 1.33 μsec per independent sample, samples would extend about 2.3 miles in each direction.

In addition to the above losses, are sampling losses in conversion of analog signals to the digital domain and losses in the coherent integration process exclusive of the collapse loss previously considered. Sampling losses due to granularity of amplitude sampling can be maintained to about 0.3 dB by setting the amplitude quantum to approximately the rms noise level. Sampling losses due to granularity in the range dimension are approximately 1.2 dB for one sample per pulsewidth reducing to about 0.4 dB with a 2:1 oversampling, i.e., two samples per pulsewidth. If a 1.5 MHz clock is used in the digital processor and the pulse out of the pulse compressor is 1.33 sec, the 0.4 dB is obtained. The filter losses have been discussed previously and it is difficult to arrive at an accurate overall assessment of losses. It is estimated that an average of one dB is achieved for cases where all filters, including the zero doppler filters, are used; this loss is relative to coherent integration, rather than noncoherent integration. A summary of losses is given in Table 2.6-2.

TABLE 2.6-2. ESTIMATE OF SIGNAL PROCESSING LOSSES

	Reference	Losses Used in Range Calculations**
Filter collapse, beam collapse and binary integration	2.4 dB	—
$I^2 + Q^2$ approximation	0.2 dB	0.2 dB
Amplitude quantization	0.3 dB	0.3 dB
Range quantization	0.4 dB	0.4 dB
Filter losses	1.0 dB	1.0 dB
CFAR	1.0 dB	1.0 dB
	5.3 dB	2.9 dB

*Hansen, V.G., Constant False Alarm Rate Processing in Search Radars, International Conference on Radar - Present and Future, 23 — 25 October, 1973, London, p. 330, Figure 3.

**Other losses are implicit in value of V_0 used.

Detection Of Targets In Clutter

The detection process for targets in clutter is similar to that for detection of targets in the clear, with the exception that means must be provided for prevention of false alarms on clutter residue. Clutter residue can result from the few points of clutter of such great amplitude that the capability of the doppler filter system to suppress clutter is exceeded.

Detection of targets in the clear is enhanced if the outputs of all filters, including the zero doppler filter, are used. Therefore, a means of automatically switching the output of the zero doppler filter on or off is also desired. Blanking of clutter residue can be combined with automatic switching of the zero doppler filter by use of clutter maps operating in parallel as shown in conceptual form in Figure 2.6-8. The clutter maps, through sequential observation of detections in individual range-azimuth map cells, identify the detections of stationary or slowly moving targets and

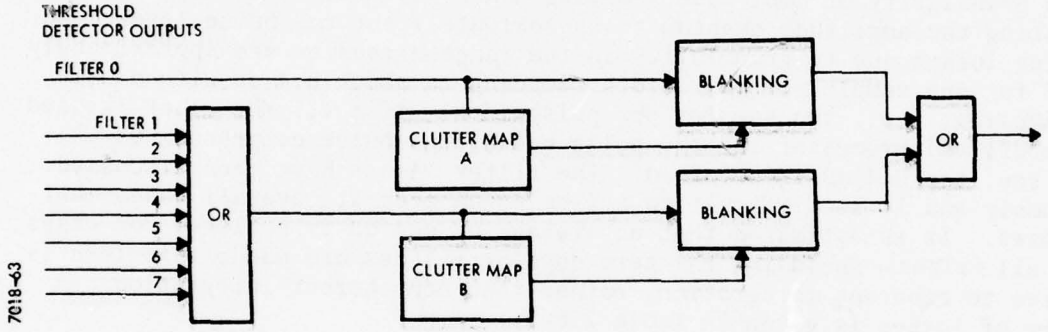

Figure 2.6-8. Automatic Switching Of The Low Velocity Filter And Blanking Of Clutter Residue Is Provided By Use Of Parallel Clutter Maps

blank these outputs to the target position computation and tracking processes. The mapping function operates as follows: in each map cell, target detections are observed every jth azimuth scan. Upon initial detection of a target, an azimuth word is assigned to that cell and a clutter count is started with an initial value of k. Upon each subsequent observation that a target is detected in the cell, the count is incremented by k, while on each subsequent observation that no target is detected within that cell, the count is decremented by one. When the clutter count exceeds a threshold level, T, the presence of a stationary target within the map cell is declared and all targets appearing in that map cell are blanked. This state continues to exist as long as the count remains above the threshold.

Important design parameters for the mapping function are: cell dimensions of the map, sampling count-down ratio (j), the increment factor (k), threshold level (T), and the clutter count frame size.

By making map cell dimensions larger than the resolution cell dimensions, memory space is saved and a more positive mapping action is achieved for clutter residue with a low probability in a resolution cell, but with a higher probability of appearing in at least one resolution cell among several within a map cell. The disadvantage of a larger cell is that the probability of blanking a target clear of residue increases. As a baseline, an azimuth cell dimension of three degrees and range dimension of one mile (approximately nine range resolution cells) is suggested for Map B. This yields 7200 cells, but since the likelihood of residue in filters 1 - 7 is small, a small percentage of these cells should be activated by clutter or target reports. Therefore a push-down memory with approximately 1000 words should suffice for this map.

The likelihood of clutter reports is much greater for the output of filter 0. Therefore, either a larger memory, or larger cell dimensions, or a combination of both is required. It is noted that increasing the cell dimensions for Map B imposes a much smaller penalty in target loss than would be suffered by a corresponding increase in Map A.

Choice of the value of the factor, k, should be based upon the predicted probability of reporting in each observation stationary targets (clutter) that results in a fluctuating residue. The value of k should be greater than the reciprocal of the expected probability of a clutter report. While values as low as five have been used in some systems, it is desirable in this system to maintain a very low probability of track initiation on clutter. A value of 20 is suggested. Given k, the values of T, j, and clutter count frame size must be selected to prevent blanking of slow moving targets. An 80-knot target on a tangential course at 60-mile ranges crosses a three degree azimuth cell in 135 seconds. Selection of $k = 20$, $j = 4$, and $T = 120$, and an azimuth frame time of six seconds prevents threshold crossing caused by a target moving at 80 knots and requires a clutter count frame size of seven bits.

A refinement of the clutter mapping technique would be to use separate mapping functions for upper beams and lower beams, to avoid needless blanking of targets in the upper beam, due to clutter in the lower beam. Since very little clutter is expected in the upper beam, a much smaller map could serve the upper beam.

2.6.5 Jam Strobe Extraction

ECM analysis consists of reporting the amplitudes and bearings of multiple jammers in the form of jam strobes. While effective CFAR performance is essential for automatic radar operation, the presence of jamming is obscured by CFAR action. As a minimum form of analysis, sampling of the ECM environment without application of CFAR is required in order to provide a warning of the existence of jamming. ECM analysis can be refined, without resorting to use of extensive hardware, to indicate the direction and intensity of jamming. More comprehensive analysis of jamming, e.g., identification of jamming waveforms and jamming spectra, is probably not justified unless it could be used locally to enable automatic control or switching of ECCM fixes. Extensive manipulation of an ECCM configuration is not consistent with requirements for high reliability and low power consumption. However, an option for coarse jamming spectral analysis and clear channel selection is discussed below.

In the baseline UAR system, a batch of pulses is transmitted at a given frequency (and, hence, a fixed azimuth), and the synthesizer frequencies are then shifted in preparation for transmission of the next batch of pulses. By sampling receiver output in the period of time following frequency retuning, and prior to the first transmitted pulse within the batch, a measure of jamming power may be obtained free of the corrupting influence of backscatter signals. Received noise jamming is envelope-detected and integrated during the sample period to obtain an estimate of the mean noise power received. If a 50 μsec sample gate is used and if the receiver bandwidth is about 0.75 MHz, approximately 35 independent noise samples are obtained, which is sufficient to maintain the standard deviation of the estimate of mean jamming level to less than 1 dB.

The jamming power estimate so obtained from the antenna (through the main radar receiver channel) may be converted to a digital quantity and delivered as jamming output as a function of azimuth angle.

Assuming existence of a single jammer with constant power output, the relative power as a function of azimuth would indicate the antenna pattern. Reporting of jamming power entering antenna sidelobes is not considered to be important in this system configuration; moreover, identification of multiple jamming sources may be obscured by reporting the jamming power entering via sidelobes. By the application of sidelobe blanking, the measurement of jamming entering sidelobes can be avoided. Sidelobe blanking operates by comparing jamming power received from the main antenna with that received from an omnidirectional antenna. When the latter is greater, the measurement function is disabled, thus blanking sidelobe responses.

Since the bearing of the jammer may be useful in passive location via triangulation, it is desirable that bearing of the jammers be measured accurately. This is accomplished by using the edge-point estimation algorithm used in extraction of radar target angle following a threshold detector The report on each jammer then, consists of the estimate of the bearing of the jammer and the jamming power received at the peak of the beam.

A baseline block diagram for extraction of the jamming strobe is shown in Figure 2.6-9. Use of logarithmic amplifiers allows for a larger input dynamic range of jamming and compresses the output dynamic range. As an alternative, the radar's linear receiver output may be used by the addition of an envelope detector. Whether the pulse compression filter (SAW delay line) is inserted makes little difference with regard to noise detection. Possible advantages of this configuration is the commonality of modules (with possible redundancies) and some reduction in the consumption of power.

Since the baseline system has use of two frequency bands to scan the same azimuth space, a coarse form of frequency agility is provided. If a jamming spectrum covers less than the two scanning frequency bands, jamming might be avoided in some cases by operation of the radar on only the clear band. Determination of the least jammed band could be accomplished by the ECM analysis function described above, which is, by comparison of the jamming levels at the two frequencies at each beam position. Also, the reporting of jamming levels to the command and control center could be expanded to include separate reports on the two bands, if that information is deemed useful.

In the method of sampling jamming described above, effect of ground clutter is avoided by the frequency shift between active listening period and the sampling of jamming. Mutual interference between adjacent radars should occur with a very low probability. If mutual interference proves to be of concern, a scheme similar to that shown in Figure 2.6-10 may be used to prevent generation of jam strobes due to this interference.

2.6.6 IFF Processing

IFF processing for identification of a specific target is initiated after a firm track is established for that target. Processing of IFF signals (Figure 2.6-11) serves to identify targets on which firm tracks have been established. The special purpose processing equipment will receive commands from the general purpose computer to test identity of a target at a specific range and azimuth angle. The radar timing and programming unit will then interrupt the radar scan and program IFF interrogations, selecting the IFF antenna that covers the thirty degree azimuth sector in which the target is reported. The pulse code modulation used for IFF interrogation will be supplied from the GPC, which also receives mode4 instructions via the remote data link. Control of the interrogation process includes necessary switching from the chosen sector antenna to the omniantenna to enable ISLS in the IFF transponder.

The IFF reply is processed through a receiver channel and processor integrated into the radar system design. After the normal decoding process, the range of the IFF response is tested for correlation with the range of the target obtained from the target track. For more positive identification of a target, several pulses may be programmed and a test made from m/n detections at the target range. This procedure also serves the defruiting function. If there is no reply from a target, additional interrogations with suitable mode control can be programmed in order to avoid false classification of friendly targets.

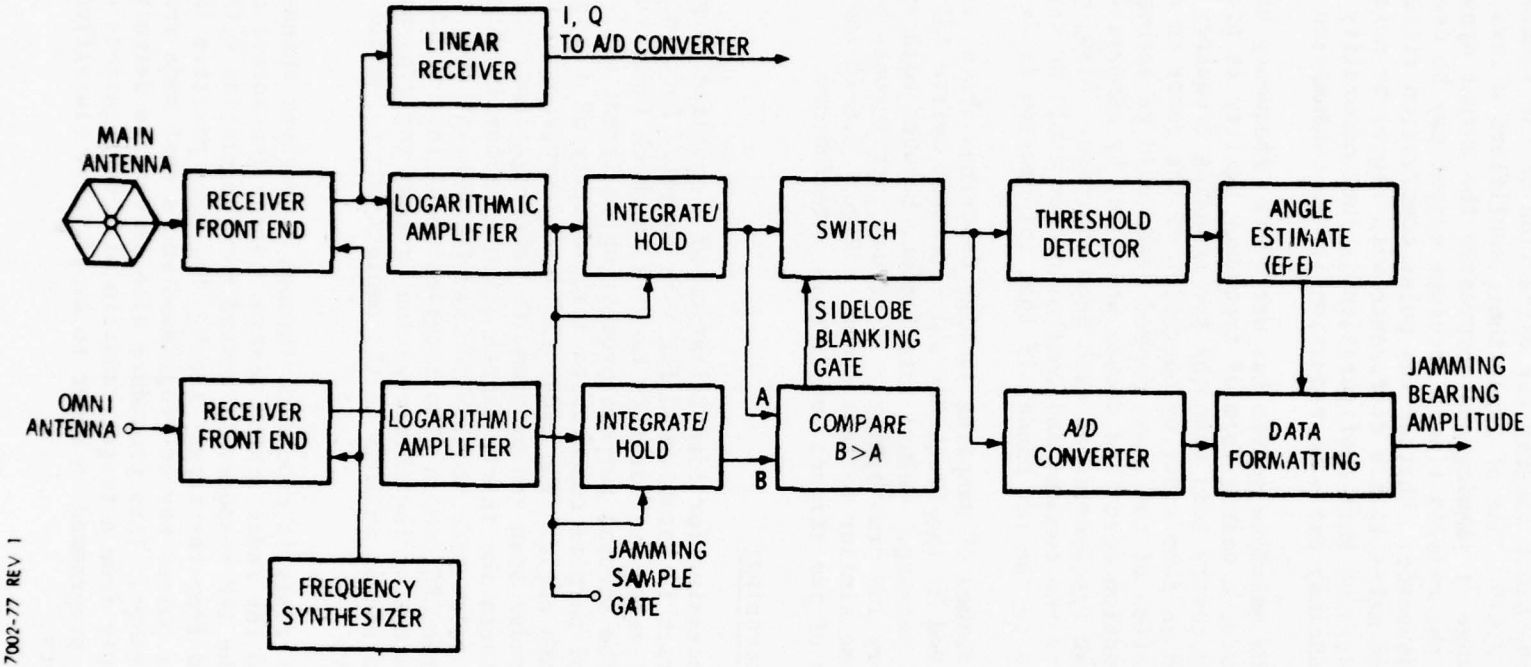

Figure 2.6-9. ECM Analysis Is Accomplished By Generation Of Jamming Strobes, Through The Application Of Sidelobe Banking. The Bearing And Peak Amplitude Of The Power Of Various Jammers Are Reported To The Command And Control Center

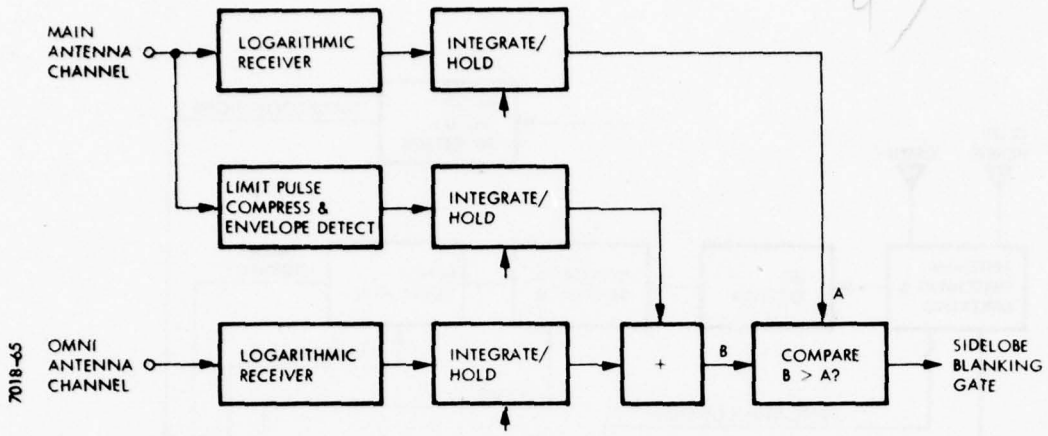

Figure 2.6-10. Generation Of Jamming Strobes Due To Interference From An Adjacent Radar Entering The Antenna Mainlobe May Be Avoided By Inhibiting The Strobe Generation When A Coded Signal Is Detected Within The Strobe Sample Gate.

2.6.7 Design For Reliability/Maintainability

High reliability and a capacity for graceful degradation are obtained by use of a highly parallel signal processing structure. As shown in Figure 2.6-12, an N-channel Filter/Detector is used. These are independent signal processors operating in parallel. Each channel processes the digitized I-Q video from all range bins and implements one filter of the doppler filter bank. CFAR detection and thresholding functions are included within each channel. The output is a binary first-level target detection signal.

The baseline system proposed requires a bank of eight filters. The number of processing channels is made somewhat larger, so as to provide spare channels for mechanization of a self-repair capability. With eight filters required, the value N = 10 providing two spares would be appropriate.

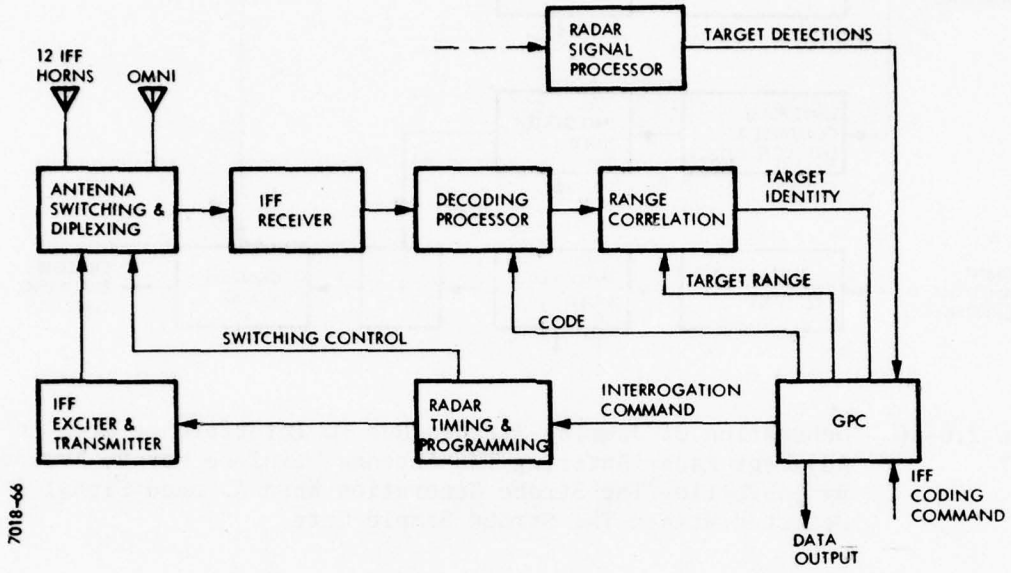

Figure 2.6-11. The Identity Of A Target Is Tested By Programming IFF Interrogation And Correlating IFF Target Responses With The Range Of The Tracked Target

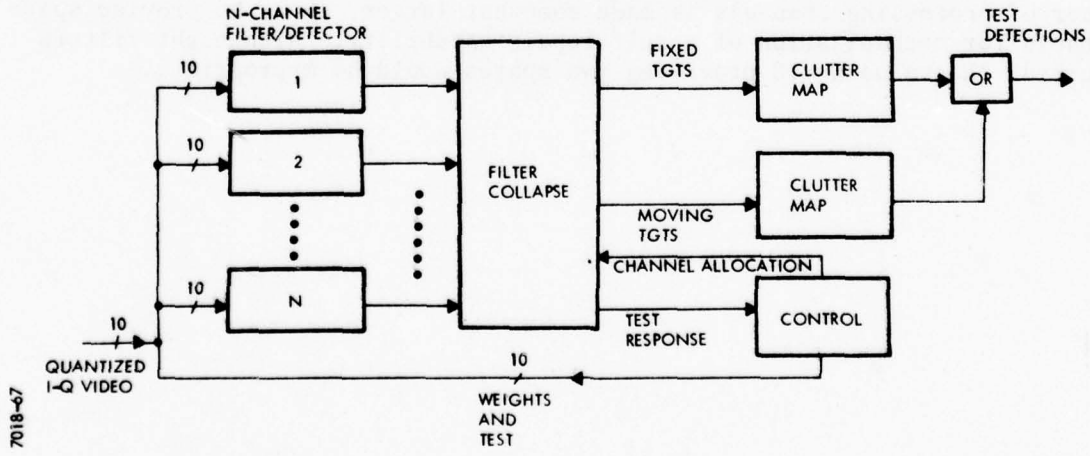

Figure 2.6-12. Signal Processor Implementation

In normal operation eight channels are active. A FIR (finite impulse response) filtering function is effected in each channel by performing a weighted summation of the I-Q video in each range resolution cell. Complex valued weight coefficients, each consisting of a pair of 10-bit words, are supplied to each channel during the radar dead time of each interpulse period. Using the same word rate as for transfer of the I-Q video, the time required to load the set of weights into the individual channel registers is small, only eight μsec being required in a processor with one μsec range resolution.

The controller monitors the status of each processor channel and controls channel allocation. A ROM is used to provide permanent storage of the filter weights, a 10 x 128-bit memory being required for a bank of eight 8-point filters.

A Filter Collapse function provides selective combining of the N-channel Filter/Detector outputs. These binary signals arrive in parallel during the eighth interpulse period of the dwell time. They are selected in accordance with the channel allocation designated by the control unit. The output of one channel, that provides zero doppler filtering, is delivered to the ground clutter mapping unit. Outputs from the other active channels are selected and combined in an OR operation to form the moving target signal.

Fault detection and isolation are accomplished by means of a self-test system. A digital signal simulating quantized I-Q video is generated in the control unit and transferred into the N-channel processor during dead time. The Test Response contains the channel outputs and closes the self-test loop.

The N-channel Filter/Detector with redundant channels is proposed, based on the high reliability attainable. This architecture also provides graceful degradation of performance. Loss of the two redundant channels, plus a third channel does not completely disable the radar. It only results in a loss of detectability for target velocities corresponding to the lost filter (channel).

The graceful degradation characteristic of this processor can be enhanced substantially by means of a slight elaboration of the control function, consisting primarily of an increase in the size of the table of stored filter weights. This is shown in Table 2.6-3.

It is seen that a modest increase in memory size substantially improves the graceful degradation characteristic of the processor.

In degraded mode operation the number of doppler filters is reduced below eight. If optimal performance consistent with the number of available channels is to be maintained as the size of the bank is reduced, the frequency response of each filter remaining in the bank must be revised. This is implemented by use of predetermined sets of distinct filter weights as indicated in the above tabulation.

TABLE 2.6-3. FILTER WEIGHT MEMORY SIZE

Mode	Number of Filters	Number of Words Per Mode	Number of Words Cumulative
Normal	8	128	128
Degraded	7	112	240
Degraded	6	96	336
Degraded	—	—	—

The requirements for high reliability and low power consumption will dominate the detail design of the processor. Maximum usage of power efficient LSI logic must be made if these requirements are to be satisfied.

At the present time several LSI technologies suitable for this application are available. The leading contenders are I^2L and CMOS. Usage of TTL and NMOS may also be appropriate in certain instances. Comparison data are provided in Table 2.6-4.

TABLE 2.6-4. LOGIC TYPE COMPARISON DATA

Type	I^2L	CMOS	TTL	NMOS	
Prop. Delay	30	30	5	100	nsec
Speed-Power	0.1	2	10	30	pJ
Gates/Chip	2000	300	300	2000	

As shown by these data, I^2L is the preferred technology. The speed power product is better by an order of magnitude resulting in outstanding power efficiency. Also with 2000 gates per chip a high level of integration is attainable. These are the device characteristics which are required in order to satisfy the high reliability and low power utilization performance requirements of the signal processor design. Maximum utilization of I^2L is therefore indicated.

In some cases localized utilization of a higher speed logic such as TTL may be needed in the implementation in order to satisfy data rate requirements. Obviously, because of the speed power product and gates per chip characteristics of this logic, its use should be minimized.

In other cases utilization of CMOS may be appropriate. An outstanding characteristic of this technology, not shown in Table 2.6-4, is extremely low power drain which obtains when operating in the static mode. In cases where intermittent logic operations occur, this technology can provide the most efficient power utilization. One drawback not shown in the table is the relatively high cost of the technology.

NMOS provides lower performance than the other technologies tabulated. It, however, does offer a high level of integration. It is a more mature technology and, depending on the timeframe of the design effort, use of this technology may be required in cases where a large number of gates per chip is needed and a suitable I^2L device is not available.

Mechanization of some specific signal processing functions is now considered. The proposed baseline processor has approximately one μsec per range cell. Word size is 10 bits. Dwell time for the doppler filtering is eight interpulse periods.

The principal operations required in each channel of the N-channel Filter/Detector processor are:

1) Complex weighting of radar video

2) Accumulation of weighted video over eight interpulse periods

3) Detection using a $\sqrt{I^2 + Q^2}$ functional approximation

4) CFAR thresholding based on a cell average estimation process.

In the first of these operations complex multiplications at a one MHz rate are required. Since $(a+jb)(c+jd) = ac-bd + j(ad + bc)$ each of these complex operations consists of four rela-valued multiplications and two additions. High speed logic, say TTL, will likely be required in the mechanization of this operation. However, feasability of the use of I^2L should be evaluated. The second operation listed above requires memory and an adder function operating at a 2 MHz word rate. Use of I^2L is indicated.

The third and fourth operations require adder and compare, functions with a small amount of memory for the cell average CFAR. An I^2L design would be satisfactory. However, use of CMOS likely would be advantageous in this case since as presently envisaged these operations occur with a 1/8 duty cycle, no computations being required during the first seven periods of the eight interpulse period dwell time. It is expected that the use of CMOS would minimize the power consumption for this operation.

2.7 UAR Data Processor Design

2.7.1 Major Functions

A Data Processor subsystem has been designed to couple the UAR with the ROCC, and to provide a target correlation and track processing capability that exceeds the UAR requirements. In addition, the combination of performance monitor software and fault tolerant subsystem organization meets the UAR goals for high reliability, operational availability, and low power consumption.

The UAR design includes a fault tolerant configuration of digital computer components, collectively referred to as the Data Processor (DP) subsystem. The DP subsystem is situated between the signal processor and the narrow band data link equipment, and serves three primary roles:

1. Radar Sensor/User Interface
2. Target/Track Processing
3. System Performance Monitoring.

Basically, the Data Processor provides an intelligent interface between the user, i.e., the ROCC, and the subsystems that comprise the UAR sensor. That is, although the actual communications path is through standard narrow band data link equipment, control of the data link resides in the DP. All message data transferred between the UAR site and the ROCC, in either direction, must be processed and routed by the DP.

When operating in this role, the DP must format/decode the data content of messages and generate/validate checksums and other message header and trailer information.

The UAR transfers track update reports and system operational status messages to the associated ROCC. The ROCC in turn, requests mode 4 interrogations, and supplies the interrogation pattern. Other messages may be created for system operational control purposes or for additional information transfer.

The Target/Track Processing function is a logical continuation of the operations begun in the signal processor (SP). The functional dividing line between the SP and DP occurs after the target detection point. Basically, the SP transforms the outputs of the Radar receiver to digital form, and applies a sequence of operations designed to detect targets and to eliminate most of the false alarms that could arise from random and residual clutter and thermal noise detections. The output of the SP, for each target detected, is a hit pattern consisting of range, antenna face, frequency of first beam containing a return from the target, and the number of consecutive hits on the target.

The DP executes those steps required to transform the hit pattern into a target position estimate, compare the estimate with target reports received previously, smooth the target position estimates, predict next target position, and update the track data base. The data processor initiates a new confirmed track automatically when predefined criteria have been satisfied. The

outputs of this target processing function are track reports, generated each time a detection is associated with a target that has passed the autotrack initiate criteria.

Two types of system performance monitoring functions are performed by the data processor subsystem. First, the data processor is responsible for maintaining its own state of health, to assure a high operational availability. This is accomplished by combining a fault tolerant subsystem organization with a performance monitor program and control monitor device that, together are able to detect component failures and reconfigure the data processor subsystem accordingly.

The DP also monitors overall UAR system performance. As with the DP subsystem, each of the UAR's other subsystems incorporates the logic needed to detect failures in their own subsystem, and to effect a reconfiguration to maintain operation. However, the monitoring and reporting of the UAR's subsystems status is the responsibility of the DP. The UAR system organization includes necessary data and control paths to enable the DP to poll each of the UAR's subsystems, and to receive a reply that indicates the state of operability of each of the subsystem's reconfigurable components. The DP polls the other subsystems periodically, and sends a system status message to the ROCC (and/or maintenance node) reporting any failures noted, and the current system performance level.

2.7.2 Target Processing

A Best Linear Unbiased Estimator (BLUE) track technique is combined with an adaptive autotrack initiation criterion to provide low false alarm rate, high track quality, and long track life.

The Target Processing function encompasses those operations performed by the data processor (DP) after a target has been detected by the signal processor. Basically, the operations include target position estimation, correlation with previous detections, auto initiation and maintenance of firm tracks, and generation of track reports. The operations are described briefly, after which a discussion of the recommended smoothing and prediction algorithm is presented.

Target Position Computation — The signal processor provides detections in the form of:

- Range cell number (1024 range cells for 60 nmi)
- Beam frequency number of first hit (80 frequency steps per 60^{o} azimuth sector)
- Face of antenna (six faces, one per 60^{o} sector)
- Number of hits (i.e., number of consecutive beams within the current scan which detected a target within the specified range cell).

This data is transformed, first into range and azimuth, then into cartesian coordinates, X and Y.

The target position is assumed to be at the center of the hit pattern in azimuth, and at the range corresponding to the specified range cell. If the target is on the boundary of two range cells, the signal processor identifies the nearest range cell. Once the range, azimuth position has been estimated, a polar-to-cartesian coordinate transformation is applied to derive the X, Y position.

Correlation/Association – Each new target detection must be associated with a previously predicted target position, or else a new tentative track is established. Correlation refers to the process of attempting to match a target position report with one of a set of predicted target positions. If the target report correlates with more than one prediction, the matching process must be refined to associate the detection with just one prediction. Later detections may, in fact, provide a closer correlation with a given prediction than some detection that has already been associated. Therefore the correlation process provides for tie breaking in the case of multiple correlations.

Autotrack Initiation – The final phase in target processing is autotrack initiation, which changes the designation of a target track from tentative to firm. The objective of autotrack initiation is to declare and begin reporting on real targets within the minimum number of scans possible, while holding the rate of false track initiations to an acceptable level. Thus, autotrack initiation provides a final stage of clutter filtering. For the UAR application, a 3/4 criterion has been suggested in the SOW. That is, a suspected target must be detected and correlated in at least three out of four consecutive azimuth scans before a firm track is declared. ITTG is presently investigating alternatives to the 3/4 criterion, that can provide adaptive response to variations in clutter residue and target signal strength. One such criterion is referred to as the 2/3/4 method (or 2 out of 3 out of 4). Basically, 2/3/4 uses a 2 out of 3 criterion, coupled with a verification procedure, to provide a 95 percent probability of detection within four scans. This method is discussed further in Section 2.1.3, UAR Performance.

A track initiation requires three additional operations to be performed:

- A new track report will be sent to the ROCC
- An IFF interrogation will be initiated
- The IFF/SIF correlation sequence will be performed.

Smoothing/Prediction – A BLUE tracker (Best Linear Unbiased Estimator) is applied recursively to the sequence of target detections to provide a minimum variance estimate of present target position and velocity, and to obtain a prediction of future target position. The BLUE tracker is applied to tentative, as well as firm tracks, to permit the quickest possible convergence to a firm track.

Track Maintenance – Periodically during each scan, several bookkeeping operations must be performed in order to keep the track update and reporting data current. Basically, this consists of processing the track file records for all targets that were predicted to lie in a sector that has just been scanned. All tentative correlation/associations for the sector are finalized, hit/miss counts are updated, and autotrack initiation/deletion occurs. The smoothing and prediction process is applied to all tentative and firm tracks, and the track file records updated accordingly. Track reports are generated on all firm tracks, for subsequent transmission to the ROCC.

The objective of the smoothing and prediction process is to give an estimate of the present and future target position. The class of estimators which yield the most accurate estimates are collectively referred to as minimum variance estimators, that is, an estimator which minimizes the risk for quadratic cost functions. In particular, since the process of target dynamics can be accurately described by a linear differential equation, of order n, the tracker selected for UAR is the best linear unbiased estimator or BLUE tracker. The order of the tracker is predicated on the highest order time derivative of the target dynamics per look. Thus for high data rate systems, a second order tracker is used, since nearly constant velocity exists between successive looks. Overestimating the order of the track results in a severe penalty in loss of variance reduction.

The BLUE tracker equations are applied separately and independently to the X and Y components of the target dynamics. The following discussion covers the smoothing and prediction process for the x-axis components; however, the y-axis equations, notation, and procedures are identical. Likewise, in the 3D MAR application, the z-axis components are treated in the same manner.

The second order BLUE tracker has the following smoothing and prediction algorithms,

$$\hat{x}(k/k) = \hat{x}(k/k-1) + K_1(k)\,[x(k) - \hat{x}(k/k-1)]$$

$$\hat{\dot{x}}(k/k) = \hat{\dot{x}}(k/k-1) + K_2(k)\,[x(k) - \hat{x}(k/k-1)]$$

$$\hat{x}(k+1/k) = \hat{x}(k/k) + \hat{\dot{x}}(k/k)\,T$$

$$\hat{\dot{x}}(k+1/k) = \hat{\dot{x}}(k/k)$$

where $x(k)$ is the value of x as measured at look k, the caret ($\wedge$) indicates an estimate, and $\hat{x}(i/j)$ indicates the estimate of x at time (i), based on all measurements up through time (j). Thus $\hat{x}(k/k)$ is the smoothed estimate of position at look k based on all data up to and including look k, whereas $\hat{x}(k+1/k)$ is the predicted estimate of x at look k+1, based on the same set of data. $K_1(k)$ and $K_2(k)$ are elements of the optimal tracking gain matrix, $K(k)$ which is determined from

$$K(k) = P(k/k-1)\left(\frac{\partial O}{\partial S}\right)^T\left[\left(\frac{\partial O}{\partial S}\right)P(k/k-1)\left(\frac{\partial O}{\partial S}\right)^T + R(k)\right]^{-1}$$

where P(k/k-1) is an n x n covariance matrix of the predicted estimates and $\frac{\partial O}{\partial S}$ is an n x p matrix whose rows are the partial derivatives of the components of the state vector. For the UAR/MAR, the above may be written as

$$K(k) = P(k/k-1)\ H(k)^T\ [H(k)P(k/k-1)H(k)^T + R(k)]^{-1}$$

where H(k) is the measurement matrix and R(k) is the measurement covariance matrix. Using tracking gains from this equation results in minimum variance estimates of position and velocity.

Mechanization of the BLUE tracker algorithm proceeds in the following steps, assuming scan k has just occurred, and scan k+1 will occur next:

(1) Compute the smoothed, (i.e., current) estimates for position and velocity, $\hat{x}(k/k)$ and $\hat{\dot{x}}(k/k)$, respectively.

(2) Compute the predicted position estimate, x(k+1/k), at look k+1. Note that predicted velocity is the same as current velocity; i.e., $\hat{\dot{x}}(k+1/k) = \hat{\dot{x}}(k/k)$.

(3) Compute the smoothed variances

$$P_{11}(k/k) = K_1(k)\sigma_m^2$$

$$P_{12}(k/k) = K_2(k)\sigma_m^2$$

$$P_{22}(k/k) = P_{22}(k/k-1) - \frac{P_{12}^2(k/k-1)}{P_{11}(k/k-1)+\sigma_m^2}$$

where σ_m is a system variance, representing the measurement error due to the chosen tracking coordinate system.

(4) Compute the predicted variances

$$P_{11}(k+1/k) = P_{11}(k/k) + 2TP_{12}(k/k) + T^2P_{22}(k/k) + \frac{T^4}{4}\sigma_a^2$$

$$P_{12}(k+1/k) = P_{12}(k/k) + TP_{22}(k/k) + \frac{T^3}{2}\sigma_a^2$$

$$P_{22}(k+1/k) = P_{22}(k/k) + T^2\sigma_a^2$$

where T = time interval between looks

σ_a = state noise

(5) Compute the predicted tracking gains for use in the smoothing and prediction equations at look k+1.

$$K_1(k+1) = \frac{P_{11}(k+1/k)}{P_{11}(k+1/k) + \sigma_m^2}$$

$$K_2(k+1) = \frac{P_{12}(k+1/k)}{P_{11}(k+1/k) + \sigma_m^2}$$

(6) Repeat steps (1) through (5) for the y-axis estimates (and again for the z-axis estimates in a 3D radar application such as the MAR, or upgraded UAR).

In conjunction with the smoothing and prediction process, correlation windows must be computed for the next scan. Basically, a correlation window is a geometric area drawn about the predicted position. Any detection that falls inside the area is said to correlate with the target corresponding to the correlation window. In the case of multiple correlations with one target, only the detection that statistically lies nearest the prediction (i.e., nearest neighbor criterion) is finally associated with the target.

The first correlation window is a circle with radius equal to the distance that a maximum velocity target may travel during one scan interval. After two detections have been received and correlated, a tentative track is initiated and the correlation window becomes rectangular. As shown in Figure 2.7-1, the rectangular correlation window is subdivided into a nonmaneuver bin and a maneuver bin. A correlation is first attempted by comparing a detection with the nonmaneuver bin limits. If the detection cannot be correlated with any existing track, correlation criterion is relaxed, and detection is compared with the maneuver bins. If no correlation is possible under the relaxed constraints, detection is assumed to be a new target.

The rectangular correlation windows are obtained from the following inequalities:

- Nonmaneuver Correlation

  Initial correlation (k=2)

$$x(k) - \hat{x}(k/k-1) \leq C\left[\sigma_m^2 + P_{11}(k/k-1)\right]^{1/2}$$

  Successive correlation (k=3)

$$x(k) - \hat{x}(k/k-1) \leq C\left[\sigma_m^2 + P_{11}(k-1/k-1)\right]^{1/2}$$

- Maneuver Correlation

$$x(k) - \hat{x}(k/k-1) \leq C\left[\sigma_m^2 + P_{11}(k/k-1)\right]^{1/2} + \tfrac{1}{2}\sigma_a T^2 + \hat{x}(k/k-1)\,T$$

  where C is a statistical constant.

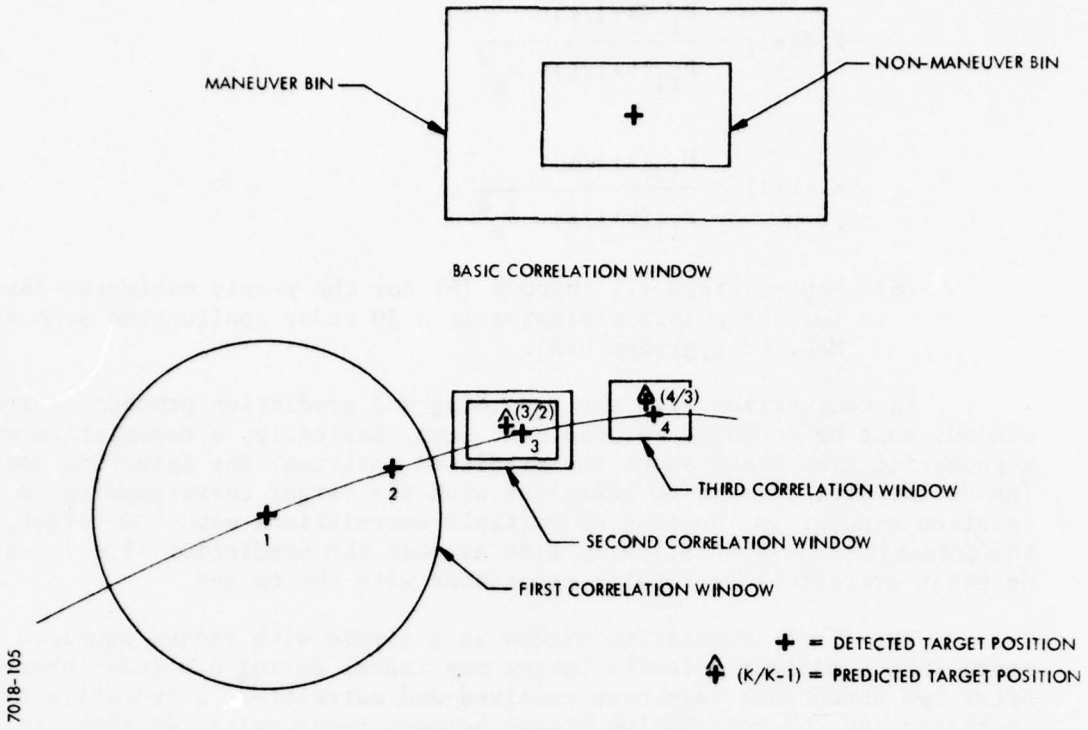

Figure 2.7-1. Typical Sequence of Correlation Windows

2.7.3 Fault Tolerant System Organization

A fault tolerant system organization philosophy is described, which permits the basic configuration to be expanded as necessary to meet any desired operational availability. The concept of fault tolerance described herein employs distributed control, with centralized monitoring. That is, each major subsystem is responsible for maintaining its own state of health, while the data processor subsystem is responsible for monitoring and reporting the status of all subsystems. To accomplish this, logic elements and functional redundancy are incorporated throughout the system to enable each subsystem to detect failed components, and to perform its own reconfiguration, automatically. In addition, each subsystem is capable of reporting the status of each of its major reconfigurable elements (usually LRU's) when interrogated by the DP.

Extending this concept, the DP subsystem is responsible both for assuring its own operability, and for monitoring and reporting its own status and that of the other subsystems. These requirements are met by a combination

of hardware, firmware (i.e., DP programs), and system organization techniques that may be adjusted to provide any degree of availability desired. The system organization and hardware complement will be described first, followed by a discussion of the operational concept.

The recommended DP subsystem organization is illustrated in Figure 2.7-2. The principal components of this organization are:

(1) Central Processing Unit — Two redundant units are shown, but three or more can be connected in parallel, depending upon the system availability requirements; these are designated CPU A, CPU B, . . .

(2) Bootstrap ROM — One 4K word module of read-only memory (ROM) will be installed with each CPU, and will contain the minimum set of programs required to enable the CPU to self-check, reconfigure, and bring the DP subsystem up to full operation.

(Note: the term "ROM" is used generically here and in the following discussion. Any programmable variants, such as PROM, EPROM, etc., may be used in practice.)

(3) BUS — One BUS set will be installed with each CPU, shown as BUS A, BUS B, . . ., corresponding to the associated CPU. Each BUS will contain separate parallel paths for data, address, and control signals, and will be routed to each device that must communicate with the CPU. Note that each such device will be provided with an electronic crossbar interface, to enable it to communicate over any of the busses.

(4) Program Memory — The UAR operational program will be stored in 4K word ROM modules, similar to the bootstrap ROM's. Each 4K word section of program will be replicated across two or more memory modules, as necessary, to meet the desired subsystem availability.

(5) Data Memory — Track files and other dynamic data will be stored in random access semiconductor memory (RAM), organized as 4K word modules. The operational program will treat the data memory as a pool of 4K word pages.

(6) Control Monitor — The key to DP subsystem availability lies in the control monitor. This unit will contain the minimum set of logic elements needed to determine when to reconfigure CPU's, and to effect the switchover. The control monitor will also reconfigure memory modules upon command from the on-line CPU.

The DP subsystem organization achieves the desired availability by means of a "cold standby" backup philosophy. In this scheme, only one CPU is powered up and on-line at any given time. The other CPU(s) will be powered up and placed into operation only if the on-line CPU fails. Likewise, power is supplied to just those memory modules that are needed to support a fully operational system. The primary advantage to this scheme is that sufficient

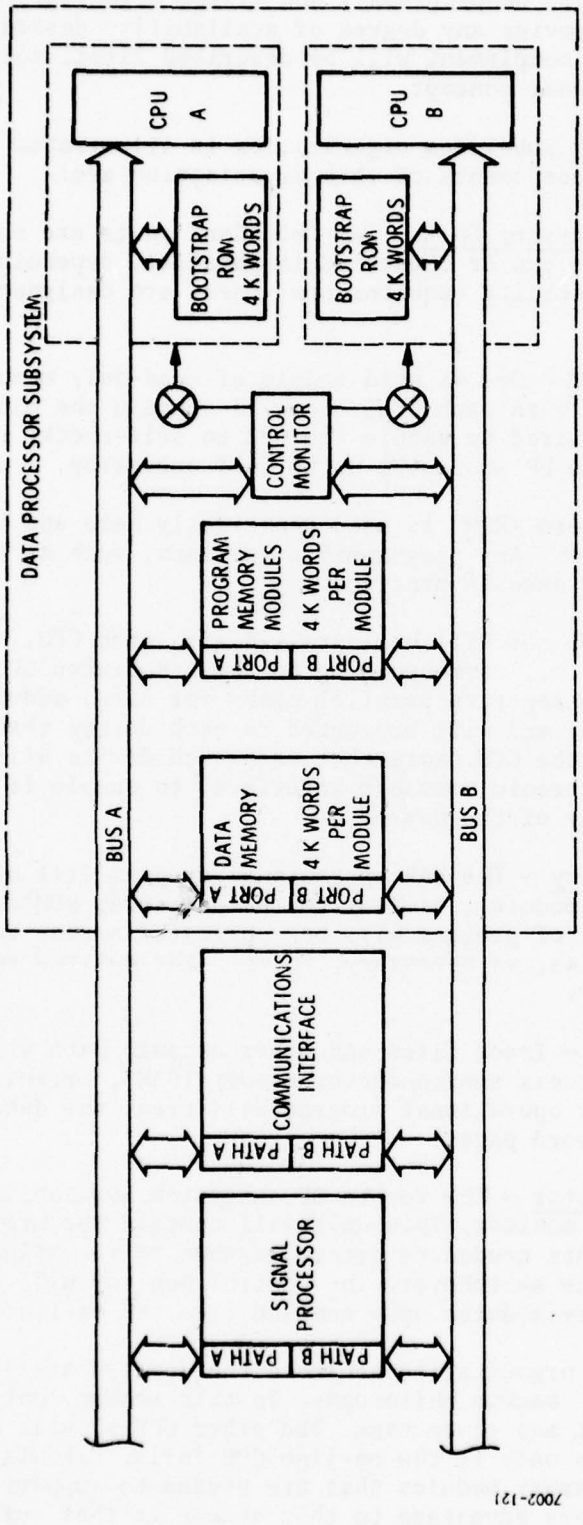

Figure 2.7-2. Fault Tolerant Data Processor Configuration

redundancy exists for the DP subsystem to meet its availability goals, but the power requirements are only slightly greater than for a single computer configuration. The single shortcoming of this approach is that it does not provide non-stop operation, but requires a temporary cessation in normal operation if an automatic reconfiguration occurs. However, the outage will be very short — less than one minute in most cases — which should be acceptable in the UAR environment of overlapping coverage from adjacent sites.

Operational control of DP subsystem configuration lies in the replicated Control Monitor hardware, and in the Performance Monitor program that executes in the on-line CPU. The interplay between these two is described in the following scenario:

(1) System Startup — Power is supplied to the control monitor which immediately switches on CPU A and its associated bootstrap ROM. The power-on logic causes the CPU to execute a startup routine that resides in the Bootstrap ROM. This program runs a self-check of the CPU and Bootstrap ROM, then outputs a 16-bit checkword to the control monitor. If the pattern does not match the prespecified value, or if the CPU output is not received within the prescribed time interval, the control monitor will power down CPU A (and its bootstrap ROM) and turn on the alternate CPU and bootstrap.

After a CPU has successfully passed the initial self-check, the startup routine proceeds to turn on program and data memory modules, via requests to the control monitor. Diagnostic tests are executed for each memory module until the required complement of program and data memory has been configured. Memory modules that fail the tests are powered down, and a record of the failure is logged for reference. After the startup test sequence has been completed, the executive routine takes control and proceeds to put the UAR into normal operation.

(2) Normal Operation — CPU Fails — During normal operation, the on-line CPU executes the performance monitor program periodically. A real-time clock interrupt is employed to signal when this and other periodic tasks are to occur. The performance monitor runs through a sequence of self-checks on the CPU and memory, then outputs a 16-bit pattern to the control monitor.

To avoid tying up the CPU for too long during this operation, the performance monitor executes a subset of the total self-checks available, with a different subset selected each time. The bit pattern to be output will identify the selected subset, and will include a value that is derived during execution of the subset. As in system startup, the control monitor must receive the prescribed pattern within the prescribed time interval. If the correct pattern is not received as specified, the control monitor will initiate a CPU switchover, as described previously.

(3) Normal Operation – Memory Fails – When a memory failure is detected, the CPU takes remedial action immediately. One of three alternatives is selected, depending upon which area of memory is affected:

a) Bootstrap ROM – A CPU switchover will occur, since it is not obvious whether the failure is in the ROM or in the CPU. That is, the performance monitor program will function improperly regardless of whether its instructions are fetched from a bad ROM, or executed in a faulty CPU. After the CPU switchover has occurred, subsequent diagnostic tests can be executed by the alternate CPU/ROM to further isolate the failure.

b) Program Memory – A failure in one of the program memory (ROM) modules will require switching to a specific alternate. The performance monitor program will command the switchover, via the control monitor. The startup program will execute a restart to cause a normal resumption of operations.

c) Data Memory – If a failure is detected in one of the data memory (RAM) modules, any one of the available spares may be switched in to replace the failed unit. After the performance monitor has effected the switch, and tested the selected spare, the Executive Program will execute a restart to reinitialize the data storage areas, then resume normal operations.

(4) Other Failures – Other failures may occur in the BUS interfaces. If the failure is such that a BUS is rendered useless, a CPU switchover will occur, thus providing an alternate BUS, and correspondingly, an alternate to the failed BUS interface.

2.7.4 Software Architecture

The UAR operational program performs the functions of target position estimation, automatic track initiation, and track maintenance and report generation. In addition, the Performance Monitor Subprogram operates in concert with the equipment configuration to achieve the required system operational availability. The UAR operational program is totally self-contained and self-sufficient within the data processor ROM modules. No program loading device is required at the UAR sites, nor is it necessary to transmit programs to a UAR site via data link. Neither of these approaches is precluded, however, if for example, it is desired to load more extensive diagnostic programs than are normally resident in the DP ROMs.

A hierarchy chart depicting the overall UAR DP program organization is presented in Figure 2.7-3. The UAR program is composed of six principal modules, each of which consists of several subroutines. The term task is used here to indicate same sequence of processing steps that are performed within the UAR program, without regard to the type or number of program elements involved.

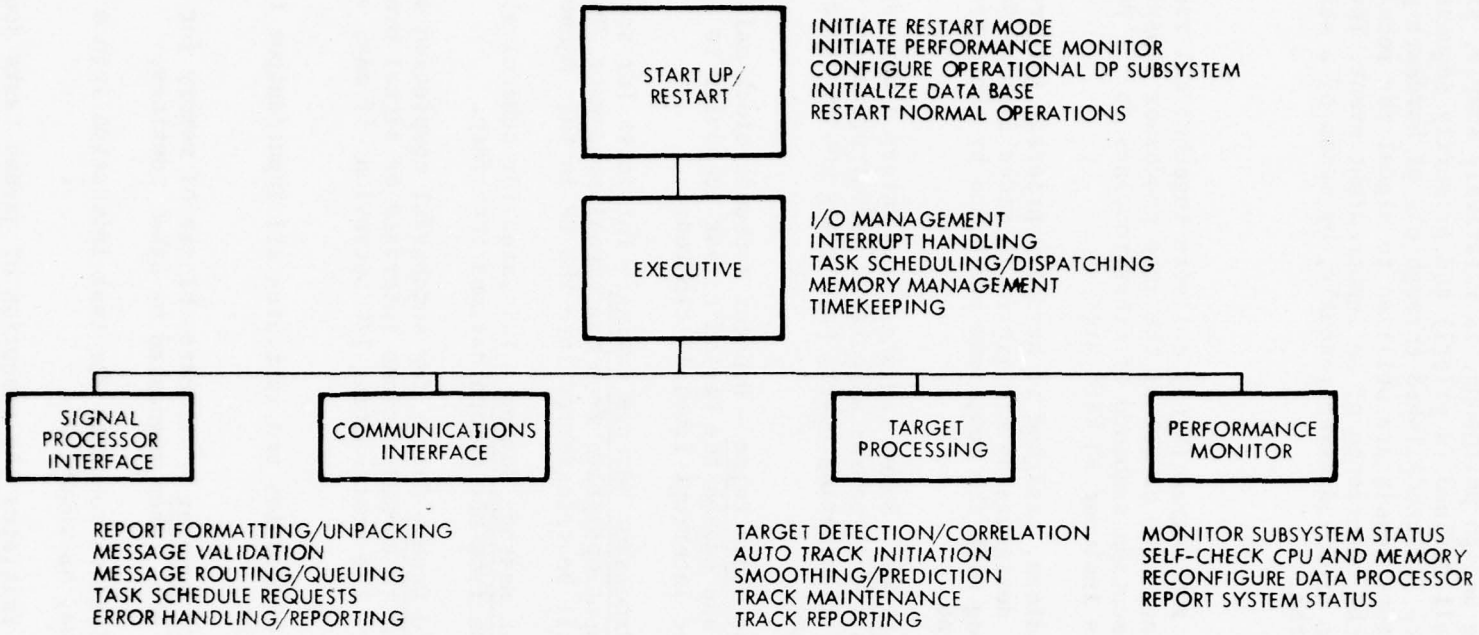

Figure 2.7-3. UAR/MAR DP Program Organization

The underlying design philosophy is relatively simple, since the tasks to be performed are well-defined (a priori) and primarily sequential. Initiation of a task sequence is accomplished through use of hardware priority interrupts. The interrupt levels are utilized to signal the receipt of a real-time clock pulse, or the occurrence of an input/output event. The major processing tasks are then executed asynchronously, by means of a software priority scheduling algorithm.

Executive

The Executive subprogram (EXEC) collects together all routines which control the flow of data into or out of the data processor subsystem or which control the normal execution sequence of other routines in the UAR program. The principal routines included in EXEC are:

Interrupt handlers, assigned to hardware priority interrupt levels. The interrupt designations are listed in order from highest to lowest priority, along with the functions performed by the corresponding handler routine.

- Power Failure – Saves registers and enters a wait state until power up signal causes a restart. Useful primarily under conditions of fluctuating power; may or may not be needed in UAR environment.

- Real Time Clock Pulse – Updates a pseudo-clock maintained in DP memory, and causes the Periodic Task Scheduler to be executed after the interrupt level is cleared.

- Signal Processor Message Coming – Initiates (or schedules) a block input operation from the signal processor. Target detections will be transferred into the DP in this manner.

- Data Link Message Coming – Initiates (or schedules) a block input operation from the communications interface.

- Block I/O Done – Checks for successful completion of block input or output to communications interface or signal processor, and initiates the next waiting I/O operation, if any, via the I/O manager.

I/O Manager – Schedules and initiates all input/output transfers over the common bus.

Dynamic Memory Manager – Allocates blocks of memory for I/O buffers, track files, etc., when requested by other routines.

Schedular – Inserts requests for task initiation into a high or low priority queue, as requested.

Dispatcher – Initiates the execution of queued tasks sequentially by priority and in order of request.

Periodic Task Schedular – Initiated as an immediate task each time a real-time clock pulse is received; examines a queue of operations that must be executed on a periodic basis, and prepares them either for immediate execution or for normal high or low priority scheduling.

Startup/Restart

Whenever a startup or reconfiguration of the DP subsystem occurs, this subprogram is executed as an initialization executive. There are two task entrances to this module.

Power Up – Whenever power is applied to a DP subsystem, it automatically strobes a power up device, which supplies the address of the power up task. Program execution begins automatically at the supplied address. A general reconfiguration operation will then be performed.

Restart – When the performance monitor detects a memory failure, the Restart Task is initiated. The Restart Task will cause memory (whether ROM or RAM) to be reconfigured, and will then take whatever reinitialization steps are required.

Both Startup/Restart tasks make extensive calls to the performance monitor subprogram to cause a thorough self-test of the DP subsystem. The final configuration is specified by the Startup/Restart task, and effected by the Performance Monitor.

Communications Interface

Communications between a UAR site and the ROCC/Maintenance node involves the following components:

- Narrowband data link
- Communications Interface Device
- DP Subsystem and Software Modules
  - I/O Manager Routine
  - Block I/O Done Interrupt
  - Data Link Message Coming Interrupt
  - Communications Subprogram.

The narrowband data link is assumed to be a bidirectional, full-duplex digital communications channel, capable of maintaining a 2400-bit per second transfer rate in each direction.

The recommended Communications Interface is an intelligent, buffered, fault-tolerant microprocessor array, attached to the DP subsystem busses. The primary benefit of the selected design concept lies in the optimization made possible in the DP I/O utilization. This is achieved by using the high-speed block I/O mode between the DP and Communications Interface, and transferring only complete messages. The communications interface buffers the messages, both incoming and outgoing, in its local memory. The DP subsystem is signalled only when an outgoing message has been transmitted (implying that another may now be sent), or that an incoming message has been received, and may now be input to the DP.

Control of the data flow between DP and communications interface resides in the EXEC I/O routines. All I/O operations are initiated by the I/O Manager to avoid conflicts in use of the one I/O bus controlled by the on-line CPU. The Data Link Message Coming interrupt is used to signal the DP that a complete message has been received via the data link and is ready to be transferred into the DP. In response, the associated interrupt handler queues the input request for subsequent action by the I/O Manager. The Block I/O Done Interrupt signals that either a block I/O operation has been completed successfully, or that a fault has been detected somewhere in the data transfer operation. The associated interrupt handler polls the communications interface, via the discrete I/O mode, to determine success or failure of the last I/O operation. Each time an I/O operation is completed, the interrupt handler dispatches the I/O Manager to cause initiation of the next scheduled I/O operation.

The Communications subprogram performs all higher level functions associated with data link messages. These functions include:

Preparation of messages for transmission from a UAR site:

Pack data into message format

Attach message type, site identification, message number

Generate and insert validation check code (e.g., parity, cyclic redundancy code, etc.)

Request transmission of the message via the I/O Manager

Processing of messages received at the UAR site:

Decode message type
Validate the message check code and other header data
Unpack data from message
Request scheduling of the routine that will process the data.

The Communications subprogram will also include logic required to initialize the data link, establish communications with the ROCC, perform alternative actions in event of faulty transmissions, and reestablish communications in case of a temporary outage.

Signal Processor Interface

Signal Processor I/O functions are handled in the DP in a manner similar to the data link communications just described. The signal processor interface device is attached to the DP busses exactly as the communications interface, except that it recognizes a different device address. The DP software modules involved are:

I/O Manager Routine
Block I/O Done Interrupt
Signal Processor Message Coming Interrupt
Signal Processor Interface Subprogram.

The I/O Manager and Block I/O Done Interrupt Handler operate with SP I/O the same as with Communications I/O. The signal processor Message Coming Interrupt indicates that the signal processor is ready to transfer a target report or IFF response into the DP. As with communications I/O, a SP input request must be queued to the I/O Manager, to avoid a conflict in bus usage.

The Signal Processor Interface Subprogram performs the higher level functions associated with signal processor I/O. These functions include:

Processing of target and IFF reports received from the signal processor

- Decode message type
- Validate message integrity
- Unpack data
- Request scheduling of appropriate processing routine

Preparation of Messages to the signal processor and IFF interrogator (which share the same SP interface)

- Pack data into message format
- Attach message type
- Generate and insert message validation code
- Request output via I/O manager.

Target Processing

The Target Processing Subprogram implements the functions and algorithms described previously in Section 2.7.3. As inferred, target processing in the DP is performed in two phases, in addition to the basic I/O operations related to target detection and track reporting.

Phase 1 is detection driven, and will be referred to as the Target Detection Association Task. It is scheduled for execution as a high priority task each time a target detection report has been processed by the Signal Processor Interface Subprogram. Figure 2.7-4 depicts the processing steps performed by this task. The following points should be noted:

The azimuth of the center beam(s) of the hit pattern is obtained from a table stored in ROM, that relates beam frequency step to true azimuth angle. The table is determined empirically for each antenna at the time of manufacture. Temperature compensation is also applied at this time.

The polar to cartesian coordinate transformations make use of sine/cosine tables, stored in ROM.

Link-list techniques are used to reduce the number of track file records that must be searched for possible correlations. The object of the correlation step is to produce a small list of tracks (ideally, just one) that might be associated with the detection.

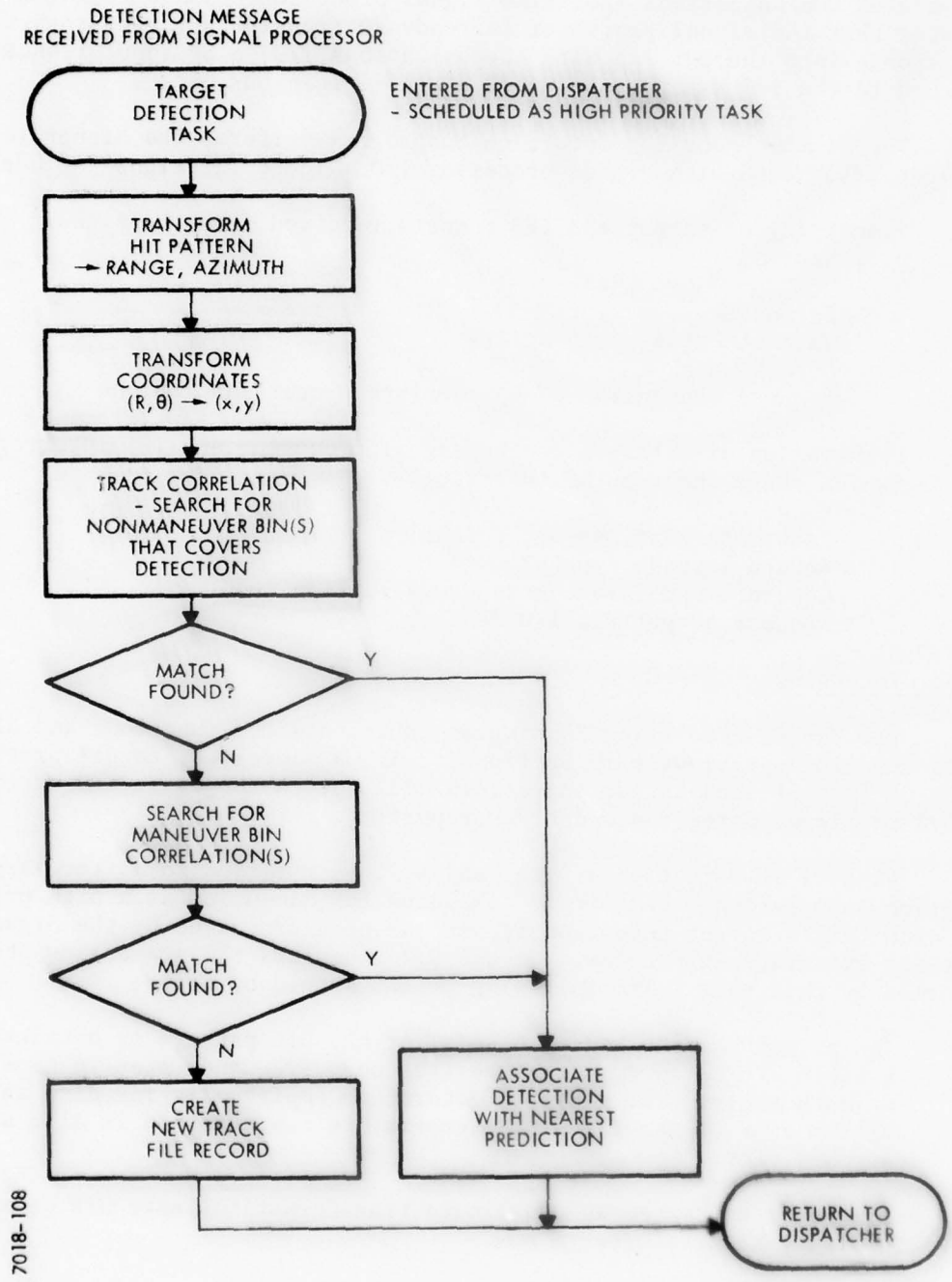

Figure 2.7-4. Target Detection/Association Task Processing

If a detection correlates with more than one track, the association step consists of selecting the track (i.e., predicted target position) nearest to the detection position; i.e., the track that minimizes the expression

$$\left\{\left[x(k) - \hat{x}(k/k-1)\right]^2 + \left[y(k) - \hat{y}(k/k-1)\right]^2\right\}^{\frac{1}{2}}$$

Tracks that have already been associated with a detection are still candidates for association with a new detection. In the case that a new detection is closer to a predicted target position than a previously associated detection, the new detection supplants the old. The old detection must then be reassociated, by reprocessing the list of correlations generated earlier for that detection. For this reason, the correlation list generated for each detection is retained until the Track Maintenance Task finalizes all associations in that sector.

The Track Maintenance Task performs Phase 2 of the Target Processing Subprogram.This task is scheduled for execution via the low priority queue, which assures that all detections will be processed before the start of a track maintenance cycle that may affect them. The scheduling frequency is approximately once per second, synchronized with the scan cycle. Each execution of this cleanup process takes care of the tracks associated with one face of the antenna, just after the scan cycle has completed its passage through that sector. The tracks to be processed during a track maintenance cycle are those with correlation windows that cover part of the sector being processed, but which do not extend into the sector currently being scanned. Nonassociated detections that lie in the sector are also processed by this task.

Figure 2.7-5 is a simplified flow diagram of the Track Maintenance Processing. As indicated, the processing steps are repeated for each track linked to the sector being processed. For each track, the following basic functions are performed:

(1) New Detection Processing – Detections that have not been associated with a specific track are assumed to be new targets. A new track file record is created, and a circular correlation window is set up, in preparation for the next scan. The radius of the window is equal to the distance that may be traversed by a maximum speed target during one scan period.

(2) Track Quality/Auto-Initiate Processing – The hit/miss counts are updated and decisions made whether to drop track or initiate a firm track.

(3) Smoothing/Prediction – The BLUE tracker equations are applied to the track, as discussed in Section 2.7.2. The correlation window coordinates are also calculated for use during the next scan.

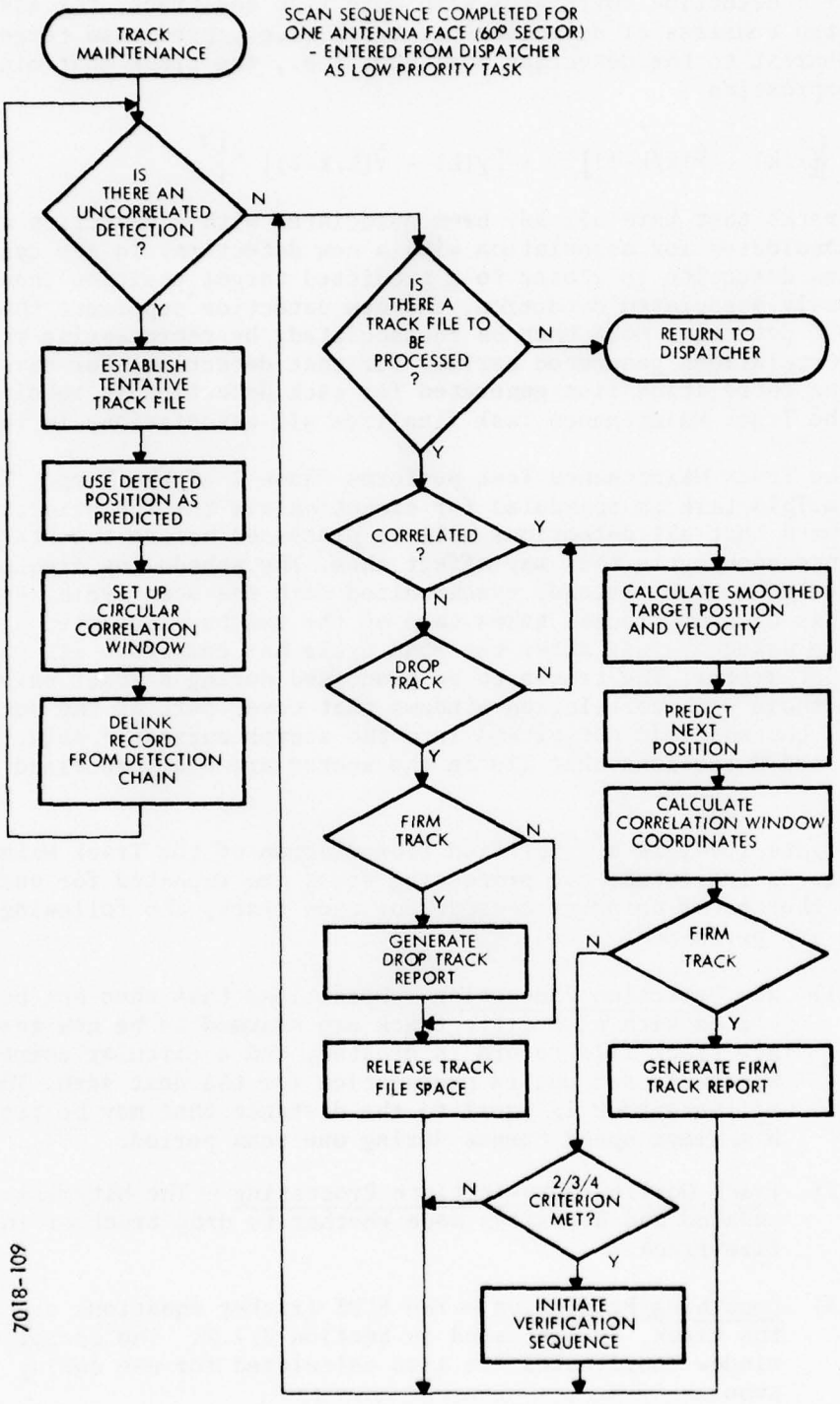

Figure 2.7-5. Track Maintenance Task Processing

(4) Track Reports - A firm track report or a drop track report is generated if either of these conditions apply. The communications interface subsystem is then requested to format and transmit the track report message.

Performance Monitor

Section 2.7.3 includes a comprehensive scenario of Performance Monitor functions. Therefore, this paragraph includes only that information required to further clarify the role of the Performance Monitor Subprogram.

Basically, the performance monitor is comprised of three main tasks:

System Performance Monitor
Self-check
Startup/Reconfiguration.

The first two tasks are initiated by the Periodic Task Schedular on a regular basis. System performance monitoring consists of polling each subsystem to obtain the status of its components. This information is then incorporated into a system status message and transmitted to the maintenance node. This message is also treated as a communications test message, which must be received at the maintenance node at regular predefined intervals, resulting in a test message reply back to the UAR site.

The self-check task performs a confidence test of the DP itself. At any one execution of this task, only a subset of the currently on-line components is tested, to avoid excessive delays in the normal target processing sequence. However, the composition and sequence of the subtests can be designed to detect component failures in the minimum possible time. The subtests that will be performed at each execution of the self-check task include the following:

CPU Test - A subroutine is executed to exercise a subset of the instruction repertoire, using all registers and addressing modes, and accessing each on-line 4K memory module (both ROM and RAM). The result of this subtest is a 12-bit pattern with an appended subtest identifier, that is output to the control monitor. If the bit pattern and test identifier do not match the predefined pattern stored in the control monitor ROM, or if the output is not received within a predefined time interval, the control monitor initiates a full reconfiguration.

ROM Test - One 256-word segment of program or bootstrap memory is tested by computing a checksum of the segment contents, and comparing with the predefined value stored in the 4K word module that contains the segment. Each time the self-check task is executed, a segment is selected from a different module than was previously tested, in order to detect module failures early.

RAM Test - One 256-word segment of data memory is tested by storing and retrieving alternating bit patterns in each word of the segment. The contents of each word are saved and restored as the test sweeps the memory. Interrupts are inhibited during this test to avoid apparent memory failures that could be caused by an interrupt handler gaining control and storing into a memory cell under test. However, interrupts are enabled at several specific points during the test, to permit time critical processing to continue.

Subsystem Interface/Bus Test - A test poll message is sent to each of the subsystem interfaces, resulting in an echo of the test bit pattern back to the CPU.

A detected failure during any of the above tests causes either a reconfiguration of the affected component, or a complete restart, depending on the nature of the failure. The total execution time consumed by the self-check task is estimated to be approximately seven milliseconds. A reasonable repetition rate is ten times per second, which consumes approximately seven percent of the CPU bandwidth, but assures that the complete CPU and every word of on-line memory is tested nearly ten times per minute.

The Startup/Reconfiguration Task is initiated whenever a major reconfiguration must take place. The startup subprogram acts in place of the EXEC, to cause the entire DP subsystem memory complement to be powered up and self-checked. The current on-line CPU is also thoroughly self-checked, as are the subsystem interfaces. At the conclusion of this comprehensive self-check operation, the startup subprogram selects an operational memory configuration, and commands the other components to be powered down, via the performance monitor. The final results of this set of operations are; (1) test pattern sent to the control monitor, (2) restart/status message sent to the ROCC, and (3) a reinitialized operational program.

Timing and Memory Estimates

A conservative estimate of UAR processing load has been derived, using instruction execution times quoted for the Hughes AN/UYK-30 microcomputer. (See Section 2.7.5.)

Table 2.7-1 presents CPU execution time estimates for principal time consuming tasks performed by the DP, under normal operating conditions. Table 2.7-1 is organized to aid in estimating the effect of additional tracks, or of a significant change in the clutter environment.

A relatively heavy DP load for a UAR site, during any one scan, might consist of:

- 20 firm tracks
- 15 false detections due to clutter and noise.

Table 2.7-1. CPU Timing Estimates

Target Processing	
Target Detection Task	
Per Detection	< 100 μsec
Per Detection/Correlation Test	< 40 μsec
Per Associated Test	< 35 μsec
Track Maintenance Task	
Per New Detection (Create Tentative Track)	< 100 μsec
Per Associated Detection (Smoothing, Prediction)	< 700 μsec
Per Firm Track Report	< 200 μsec
Communications/I/O	
SP Interrupt & Input Handling (Per Detection)	< 200 μsec
Data Link Communications/Interrupt Handling (per Firm Track)	< 200 μsec
Performance Monitor	
Self-Check & System Monitor (Per Execution)	< 7 ms

Assuming none of the false detections correlate with previous false detections, the following basic load factors are calculated:

Target Processing

(35 detections)·(100 μs) = 3500μs
(35 detections)·(10 correlation tries each)·(40 μs) = 14000μs
(20 correlation tracks)·(2 associations each)·(35 μs) = 1400μs

Track Maintenance Task

(15 new detections)·(100 μs) = 1500μs
(20 firm tracks)·(700 μs - smoothing, etc.) = 14000μs
(20 firm tracks)·(200 μs - track reports) = 4000μs

Communications & I/O

(35 detection reports)·(200 μs) = 7000μs
(20 firm track reports)·(200 μs) = 4000μs

Total Target/Track Processing per Scan = 48000μs

Average Target/Track Processing = $\frac{48 \text{ ms}}{6 \text{ sec}}$ = 8 ms/sec

Average Performance Monitor Time = 7ms x 10/sec = 70 ms/sec

Thus, the basic processing load associated with the postulated target processing and performance monitoring functions will consume less than eight percent of the CPU bandwidth. The overhead attributed to executive routine services

and general data manipulation will consume no more than five percent additional, for an average total of less than 15 percent of the available CPU bandwidth.

Not stated in Table 2.7-1 is the processing time associated with target verification. While the exact algorithm is still under study, it is certain that verification processing will require less than 2 ms/sec of CPU time during one scan cycle, for each target in the verification phase. For the detection/track load postulated previously, less than two targets are expected to be in the verification phase during any one scan. Thus, verification processing will add only 0.4 percent to the average processing load, which still totals less than 15 percent of the available CPU power. Therefore, sudden increases in target density will not overload the CPU.

Table 2.7-2 presents estimates of memory requirements for a nonredundant DP subsystem. The estimates given are generous, to provide for expansion in functions. The data base estimates are purposely large, relative to the stipulated track processing capability, for two reasons. First, extra space is provided for track files to enable a UAR site to handle a greater track capacity, e.g., up to 100 firm tracks. Second, the additional space permits more rapid searching for correlations, by providing for large index tables and linked lists through the data base.

The limiting performance factor for the UAR configuration presented here is communications capacity. Approximately 64 bits are required to encode a track report message — more if required by the communications protocol selected. If a 2400-bit-per-second data link speed is used, then 37.5-message-per-second rate is the maximum achievable. Overhead due to communications line discipline and other factors could reduce this rate, along with the demand for other types of message transmission. Therefore, the average track report message capacity is about 25 reports per second, or 150 reports per scan.

Table 2.7-2. MEMORY REQUIREMENTS
(Non-Redundant Configuration)

Function	Memory Area	Allocation (16-bit words)	Subtotals
Startup	Bootstrap ROM	500	
Executive	Bootstrap ROM	1000	
Performance Monitor	Bootstrap ROM	2000	3,500
Target Processing	Program Memory	4000	
Signal Processor Interface	Program Memory	2000	
Communications Interface	Program Memory	2000	
Static Data Base	Program Memory	3000	11,000
Dynamic Data Base	Data Memory	6000	6,000

2.7.5 Data Processor Hardware

The data processor configuration selected meets the UAR system objectives for operational availability, low power consumption, functional capability, and cost effectiveness. The recommended DP subsystem has been configured around a recently announced, militarized microcomputer, the Hughes AN/UYK-30. It is anticipated that even more capable, reliable, and cost-effective microcomputers will be available by the time UAR system implementation actually begins. However, by focusing on one device which is presently available and capable of supporting the UAR mission, it is possible to remove the conjecture associated with a purely theoretic approach, and to develop more concrete estimates of life cycle costs, power requirements, and functional capability.

Several alternatives were considered for providing data processing capability required in the UAR system, ranging from distributed microprocessors to duplexed general-purpose computers. In general, it was determined that the available discrete microprocessors suffer from a lack of support software, and most do not yet offer the execution speed required in the UAR application. Minicomputers consume too much power. The UYK-30 based configuration described herein represents an approach that lies midway between the two extremes, and offers most of the advantages of each. The UYK-30 offers the low-cost, low-power consumption and high reliability associated with current microprocessor technology, as well as the instruction repertoire, execution speed, central processing unit architecture and I/O interface of the more capable, general-purpose minicomputers. The principal features of the UYK-30 microcomputer are presented in following paragraphs, after which its role in the UAR DP subsystem is discussed.

AN/UYK-30 Military Microcomputer

The Hughes AN/UYK-30 is a militarized bipolar microcomputer developed for use in real-time applications such as avionics, radar data processing and communications. The basic UYK-30 consists of a microprogrammed arithmetic and control unit plus a powerful digital I/O interface, constructed from approximately 70 LSI and MSI packages. The UYK-30 is generally implemented on three circuit cards (5.6 x 6.5 x 0.5"). Memory is supplied by the user (in this case, the UAR system implementer) on separate circuit cards. The UYK-30 provides an asynchronous memory interface, which permits use of virtually any memory technology and speed, in any combination, up to a maximum of 65,536 16-bit words. Figure 2.7-6 shows a UYK-30 block diagram for a single CPU system, with all available I/O modes utilized.

Principal features of the AN/UYK-30 microcomputer are summarized in Table 2.7-3.

UAR Site Data Processor Subsystem Configuration

The general concepts of a fault tolerant system organization are discussed in Section 2.7.3. The 2-CPU configuration shown therein will meet requirements of the three-month unattended operation model, if we use the 20,000 hour MTBF quoted for the UYK-30 CPU. In order to satisfy the six-month and one-year unattended operation models, the DP subsystem must be expanded.

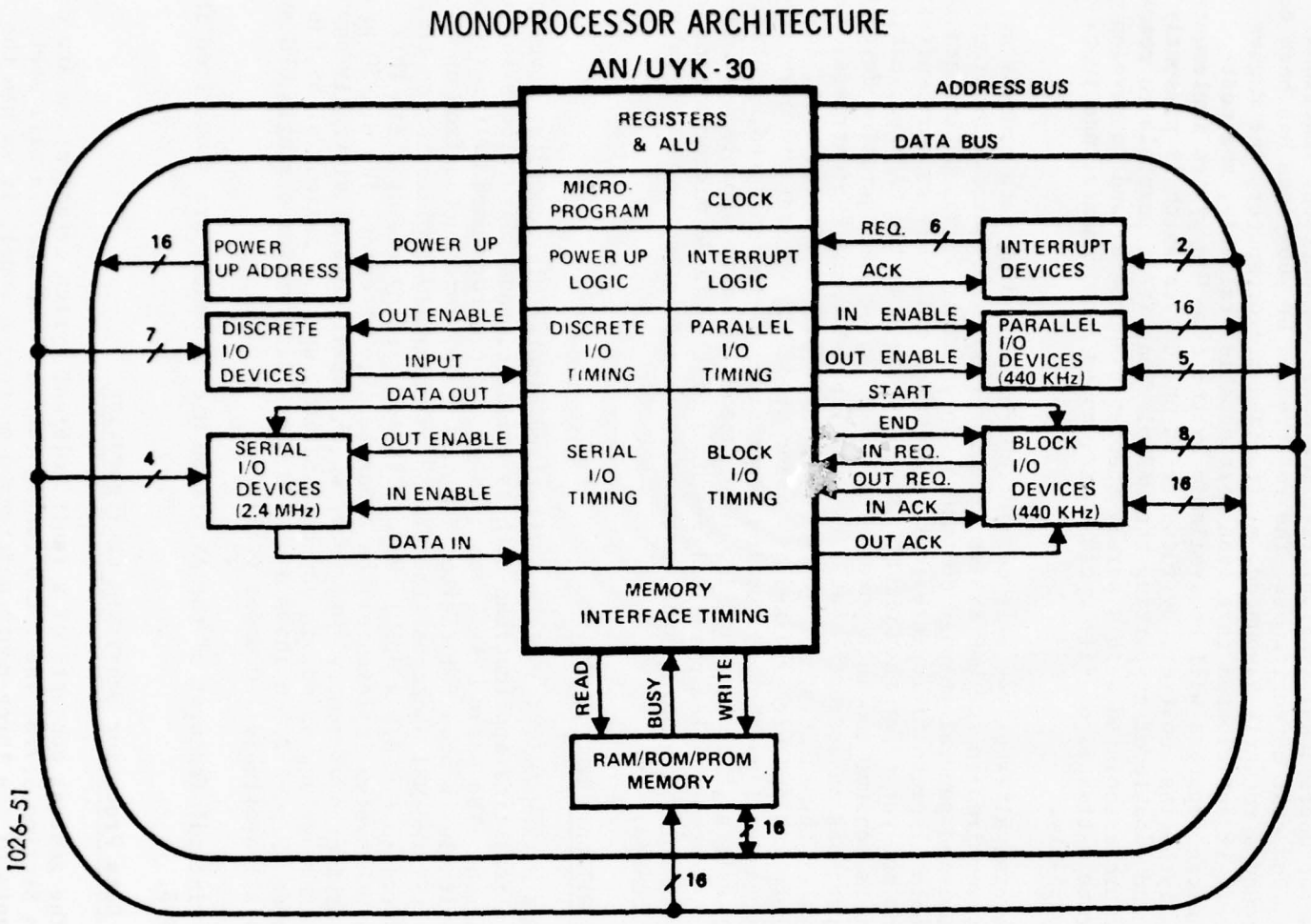

Figure 2.7-6. AN/UYK-30 Microcomputer, Showing Memory and Input/Output Interfaces

Table 2.7-3. AN/UYK-30 Features

Wordlength	- 16-bits
General Registers	- 4 Accumulators - 2 Index Registers - Stack Pointer - Program Counter
Arithmetic Mode	- 2's complement fractional
Number system	- Binary fixed point
Maximum Memory Size	- 65,536 words; any mix of ROM, PROM & RAM
Priority Interrupts	- Power Fail - 4 User-defined Interrupt Levels - Halt, used for external control of the CPU
Instruction Repertoire	- 50 Instruction Types, including high-speed multiply and divide - Both Memory-Register and Register-Register operations - Single and double precision arithmetic
Typical Execution Times*	- Add - 2.25 µsec - Multiply -10.75 µsec - Divide - 20.5 µsec - Shift - 2.5 µs + .5 µs per bit shifted - Compare - 2.5 µsec - Branch - 2.5 µsec
Memory Addressing Modes	- Direct - Indexed - Relative - Relative Indirect - Indirect - Immediate - Register
I/O Modes & Rates (words per second)	- Serial - 154K peak 93K avg - Parallel - 455K peak 154K avg - Block - 455K peak 455K avg - Discrete - used for I/O device control and external condition sensing (Above listed modes are built into UYK-30 CPU; an optional DMA is available but not required for UAR application)

*Assumes memory access time less than 660 nsec.

Table 2.7-3. AN/UYK-30 Features (Cont'd)

Operating temperature range	- Mil spec (-55^{o} to $+125^{o}$C)
Approximate throughput	- 300 - 600 KOPS
Technology	- Low Power Schottky LSI
System clock	- 4 MHz, 50 nsec pulsewidth
Power supply voltage	- +5 Vdc
Logic levels	- TTL voltages
Power consumption	- 16W (typ)/24W (max)
IC count	- 70

Figure 2.7-7 shows a UYK-30 based configuration that embodies the same concepts of fault tolerance discussed previously. Three CPUs are included to achieve the required operational availability. Three bootstrap ROMs are included also, one for each CPU, because of the intimate association of the bootstrap ROM with the CPU during startup and reconfiguration phases. Only two redundant sets of program memory are required, however, because of greater inherent reliability of these modules, compared with the CPU. The recommended configuration also includes spare data memory with sufficient redundancy to satisfy the one-year unattended operation model.

The control monitor is shown as a single unit with interfaces to each BUS. It provides the ability to switch power automatically to any one of the three CPUs and associated bootstrap ROMs. The control monitor provides power on/off control also for each of the program and data memory modules. The decision to power up a particular CPU is made within the control monitor as described in Section 2.7.3. The powered up CPU then makes all decisions as to which program and data memories to turn on, via commands to the control monitor.

The control monitor is envisioned as a relatively small array of redundant logic elements, control circuits, and read-only memory. Since only a few simple decision and switching operations are required of the control monitor, it will be inherently far more reliable than the CPUs. The control monitor will report status of its internal components to the on-line CPU, for maintenance monitoring purposes.

I/O interfaces to the DP subsystem are colocated with the signal processors. Control and data lines to the narrow band data link equipment, and to each UAR subsystem, will be connected to a centralized redundant bus interface, thus making the I/O paths simpler and more reliable. Data transfers to/from the UYK-30 will take place by means of the Block I/O mode for multiword messages; single word transfers will utilize the parallel I/O mode. The

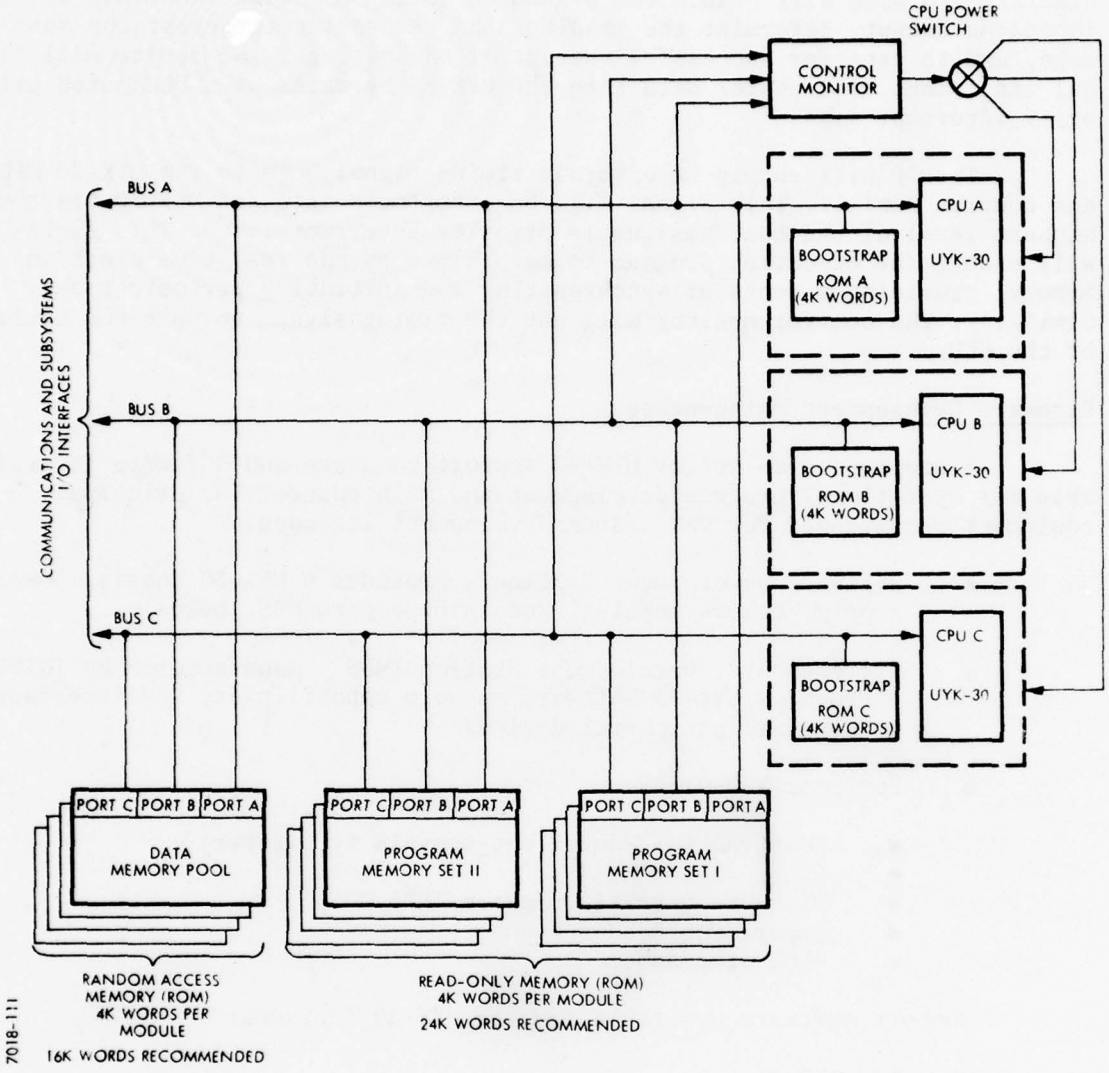

Figure 2.7-7. UAR Data Processor Subsystem Configuration

discrete I/O mode will enable the UYK-30 to notify a device interface of an impending output, determine the readiness of the device to accept the message, and to test for successful receipt of the message. The device will signal its intent to transfer data into the UYK-30 by means of a dedicated priority interrupt line.

The SP will supply an external timing signal both to the UYK-30 CPUs and control monitor. This signal will be interfaced into the UYK-30 via the highest level of the four assignable priority interrupt lines. This signal will enable the executive program to maintain a pseudo real-time clock in memory, providing a means of synchronizing and initiating periodic tasks. Similarly, the control monitor will use the timing signal to pace the actions of the CPU.

Firmware Development/Maintenance

A comprehensive set of UYK-30 support hardware and software is available for operational program development and maintenance. The principal equipment recommended for UAR system development includes:

- Software Development Station - Provides a UYK-30 chasis, power supply, memory modules, and interface to MDS, below.
- Microcomputer Development Station (MDS - manufactured by INTEL) - Provides UYK-30 software support capabilities, and interfaces to standard peripheral devices
- Peripheral Devices
  - Teletype (or equivalent console typewriter)
  - Line Printer
  - Diskette Operating System (MDS-DOS)
  - Paper Tape Reader/Punch
  - PROM programmer

Support software available for the UYK-30 includes:

- Assemblers
  - UYK-30 resident assembler runs on the MDS, and generates object code that may be executed immediately on the UYK-30 Software Development Station
  - Cross assembler runs on any host computer that has an ANSI FORTRAN compiler, and generates object code for subsequent loading and execution on a UYK-30
- Simulator - Executes UYK-30 object programs on any host computer with ANSI FORTRAN capability; used to simulate the logical operation of a UYK-30, and debug object programs before installing in the UYK-30 system

- DEBUG Package - runs in a UYK-30 Development Station, and enables a user to test, modify and execute programs under DEBUG control

- MDS Operating System Software

  - System Monitor - provides a basic monitor for software development

  - INTEL System Implementation Supervisor (ISIS) - provides file management capabilities for use with the Diskette Operating System

  - ISIS Text Editor - provides source language editing capability

The equipment and support software listed above will be used initially to develop and debug the UAR operational program. Maintenance of the UAR sites may also require one or more of these configurations, depending upon how firm the operational program becomes. A scenario of the software/system development follows, to clarify usage and need for these tools.

Development of the UAR operational program will take place in several stages. Initial code generation and checkout would utilize the cross assembler and simulator on a host computer such as an IBM 370. This procedure permits the individual code modules comprising the UAR operational program to be assembled and debugged in a batch mode, independent of one another. Integration of code modules would take place first on the host, then on the UYK-30.

During the early stages of checkout on the UYK-30, the Software Development Station would house the UYK-30 CPU and memory. RAM modules would be used for the program and bootstrap memories, instead of ROM, to facilitate debugging and program modification. The UYK-30 loader would be used for loading the operational program during this phase of development.

When the UAR subsystems are ready to be integrated, the UYK-30 assemblies would be installed in their destined rack space for system checkout. However, an interface would be retained to the MDS, for access to peripheral devices and support software that will be required during integrated system checkout. RAM will still be used for program storage throughout this phase.

After the operational program has undergone thorough on-site debugging. the PROM Programmer device would be used to produce the read-only form of program and bootstrap memory. Site-specific parameter tables would be generated in PROM also, and stocked separately for each site.

In the event that additional changes are required in the operational program, the PROMs can be reprogrammed using the PROM Programmer. For this reason, a software development station should remain at each site until correct operation of the site has been verified, and site-specific parameters validated. Thereafter, PROM programming capability should be retained at each maintenance node for generation of spares or preparation of upgrade versions of the operational program.

2.8 POWER SUPPLIES

The reliability and efficiency requirements of the UAR power supplies dictate the need for a thorough design analysis of the power distribution system. The goal of performing the entire radar operation with only 500W of prime power requires stringent power budgeting for the various radar subsystems. The UAR power budget is illustrated in Table 2.8-1 and, as noted, the prime power requirement is 518.5W. This includes dissipation of over 100W within the power supplies themselves, which are assumed to be 80 percent efficient.

Table 2.8-1. UAR POWER BUDGET

ITEM	POWER, WATTS
ANT/XMT/RCV SWITCH	5.3
RADAR XMTR	240.0*
IFF XMTR	0.0**
RADAR RCVR	5.0
REFERENCE RCVR	2.5
IFF RCVR	1.0
RADAR EXCITER	3.0
IFF EXCITER	1.0
SYNTHESIZER	10.0
SIGNAL PROCESSOR	90.0
DATA PROCESSOR	57.0
	414.8
POWER SUPPLIES (η = 80%)	103.7
TOTAL	518.5

*This assumes continuous radar operations and does not account for the average power reduction during IFF interrogation.
**Included in RADAR XMTR.

The assumption of 80 percent power supply efficiency is considered reasonable and, in fact, may be rather conservative, depending on the characteristics of the input prime power. Since the voltage level and degree of regulation of available dc power has not been specified, dc-dc converters and regulators are assumed necessary to provide the five voltages used by the radar, (ie, +28, ±15, ±5V). A substantial increase in overall efficiency results if the available power is regulated 28Vdc - the power used by the solid-state transmitter. Somewhat less of an efficiency increase will be obtained if an unregulated dc voltage in excess of 28V is provided. In this case, a voltage regulator will be needed, and the dc-dc converter eliminated for the 28V power. Since both positive and negative values of 15V and 5V are required, dc-dc converters will presumably still be needed to obtain these levels.

Because of high reliability requirements of the radar, dual power supplies are recommended for the UAR. Based on a simple numerical comparison of failure rates of the various modules, power supply redundancy does not offer the greatest reliability increase for each dollar of investment.

However, power supply operation is critical to mission success, whereas failures in other assemblies may simply result in degraded performance. As a consequence power supply redundancy is recommended.

The most effective power supply implementation has not been fully identified. There are advantages in efficiency in using standby redundancy in which a failed supply is switched out and replaced by its backup. On the other hand, using both supplies in a shared-load arrangement eliminates switching requirements at some cost in efficiency. An additional consideration is the trade-off between central and distributed power supplies. Both of these approaches have advantages, and the optimum configuration is probably a compromise between the two. Specifically, power buses with crude regulation could supply power to load points at the modules or groups of modules. Here, additional regulation is provided to satisfy requirements of the individual modules. A further benefit of this approach is that powering-up and -down of standby redundant modules can be effected very simply by appropriately biasing the switching or series pass transistor in the regulator circuit. A final determination of the optimum power supply approach requires careful study of power requirements of the individual modules and a detailed trade-off of system reliability and efficiency requirements.

SECTION 3

MINIMALLY ATTENDED RADAR (MAR) DESIGN

3.0 MINIMALLY ATTENDED RADAR (MAR) DESIGN

3.1 System Design

3.1.1 Operating Frequency Selection

Agile frequency operation over the 185 MHz band from 1215 to 1400 MHz is selected as optimum for the MAR application. Most of the arguments presented in Section 2.1.1 (UAR frequency selection), [with the exception of the one concerning solid-state device efficiency vs frequency (the MAR employs a tube transmitter)], can be validly used to determine the optimum operating frequency for the MAR. At first glance this may seem to be inconsistent since the MAR must provide a 3D capability as opposed to the UAR's 2D capability, and since the narrow beamwidths needed for 3D operations should be more cost effectively attained at higher operating frequencies. However, when data rate, time on target for adequate target to clutter enhancement, and prime power consumption are additionally considered, L-band is found to be superior to higher frequencies, i.e., better system performance can be provided at lower overall system cost.

Furthermore, the deleterious effects from multipath have been shown (Section 2.1.1) to be less at the higher operating frequencies (i.e., L and S-band), but L-band MAR detection performance in the worst case multipath environment should be adequate as shown in Figure 3.1-1. If the MAR application should require determinations of target heights at low elevation angles ($<1^{o}$) where effects from multipath are most severe, various solutions are possible: 1) employ a pencil beam on transmit ($\sim 2^{o}$ in el) vs fan beam ($\sim 10^{o}$) and use multiple pencil beams on receive (this is one mode of MAR operation already offered); 2) consider higher tower mounting for the MAR antenna; 3) investigate multi-frequency (S&L) band operations; 4) investigate array signal processing.

For the application postulated, as radar sensors in a new DEWLine, UARs and MARs that have the same operating frequency provide additional advantages: 1) frequency commanlity should result in reduced cost for RF test equipment, and 2) frequency commonality would provide a means of decoying ARMs locked on to a specific MAR or UAR. Disadvantages such as mutual interference between MARs would be precluded to a large extent due to the spacing between sites (i.e., $\sim$500 nmi between logistical nodes). Mutual inteference between a MAR and nearby UARs would be basically precluded due to the difference in operating modes. The MAR employs mechanical rotation in azimuth at 5 rpm with phase scanning in elevation. The UAR employs frequency scan in azimuth covering 360^{o} in nominally six seconds.

In conclusion, the operating frequency band for the MAR should be as wide as practical, be centered in L-band (1300 MHz), and be identical to the UAR band. The MAR should have an agile frequency capability. The need and/or desirability of frequency agility for the MAR is discussed in Section 3.1.2.

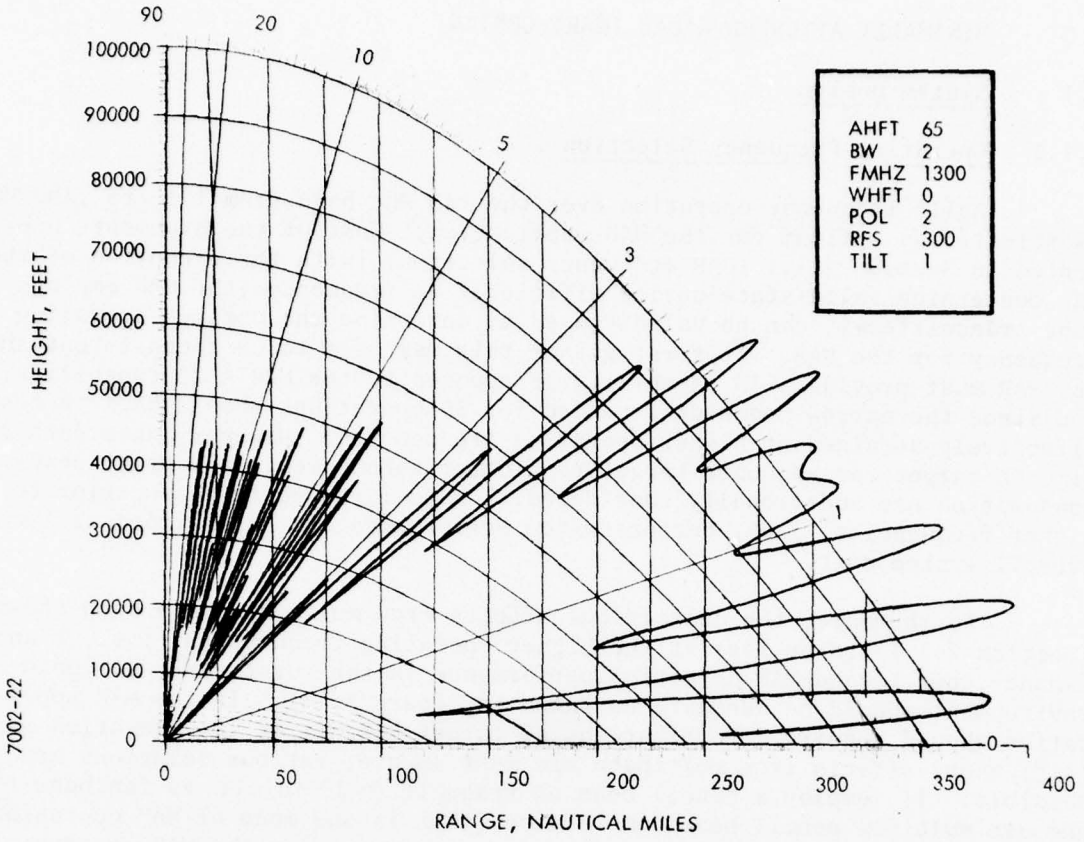

Figure 3.1-1. MAR Range Height Diagram For Lowest Receive Beam (1 of 6 Receive Beams) and 50' Tower

3.1.2 System Configuration

The baseline MAR system is configured to provide the inherent availability needed to support minimally attended operations.

System Design Approach

The mission postulated for the MAR is one that encompasses ATC/GCI (air sovereignty/air defense) and back-up surveillance coverage for the DEWLine UARs. In the latter role, MARs are assumed to be located at manned logistical nodes, therefore, the MAR's reliability requirement is significantly reduced compared to the UAR's. With a much lower MTBF required, the MAR's need to have a design which will assure a low MCT becomes vitally important in order to effect the needed availability.

From the above, it can be concluded that design approaches possible for implementing an optimal MAR are somewhat less restricted than those for the UAR. For the MAR, rotating antennas in radomes can be considered, tube type transmitters are not precluded, etc. Highlights of the design approach taken to define the MAR are shown in Table 3.1-1.

TABLE 3.1-1. MAR DESIGN APPROACH

WIDEBAND FREQUENCY AGILITY - ECCM, TARGET FLUCTUATION, MULTIPATH

NARROW AZIMUTH BEAM - ECCM, CLUTTER

SHAPED ELEVATION BEAM(S) ON TRANSMIT - CLUTTER, ECCM, MULTIPATH

MULTIPLE ELEVATION BEAMS ON RECEIVE - REDUNDANCY, GRACEFUL DEGRADATION, CLUTTER/TIME

PHASE SCAN - MULTIMODE (2D, 3D, BT), FREQUENCY PULSE CODING/COMPRESSION

PRETRACK FILTERING - CLUTTER, ECCM (STROBE), MULTIPATH

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The baseline design (see artist's concept (Figure 3.1-2) and system block diagram (Figure 3.1-3)) was configured to operate over a 185 MHz band (nominally centered at 1300 MHz) and to have an agile frequency capability (pulse-to-pulse or group-to-group). Wideband frequency agility operations reduce the effects of ECM and multipath and minimize the SNR required for detection of the Swerling I fluctuating target. This in turn minimizes the MAR's transmitter and prime power requirements. To further reduce the transmitter power needed for detection, the MAR antenna aperture is selected to be as large as possible, constrained only by the desired data rate, dwell time on target required for clutter processing,a nd radome size permitted to be used for arctic tower mounting. Phase scanning in elevation, coupled with mechanical rotation in azimuth was selected as the least costly approach that is compatible with full frequency agility, multimodal systems operations (2D, 3D, BT), and wide bandwidth intrapulse coding using phase and/or frequency modulation. Multiple simultaneous elevation receive beams were specified to assure sufficient dwell time on target for clutter suppression, to maintain desired data rate, and to provide inherent receiver/processor redundancy that permits graceful degradation.

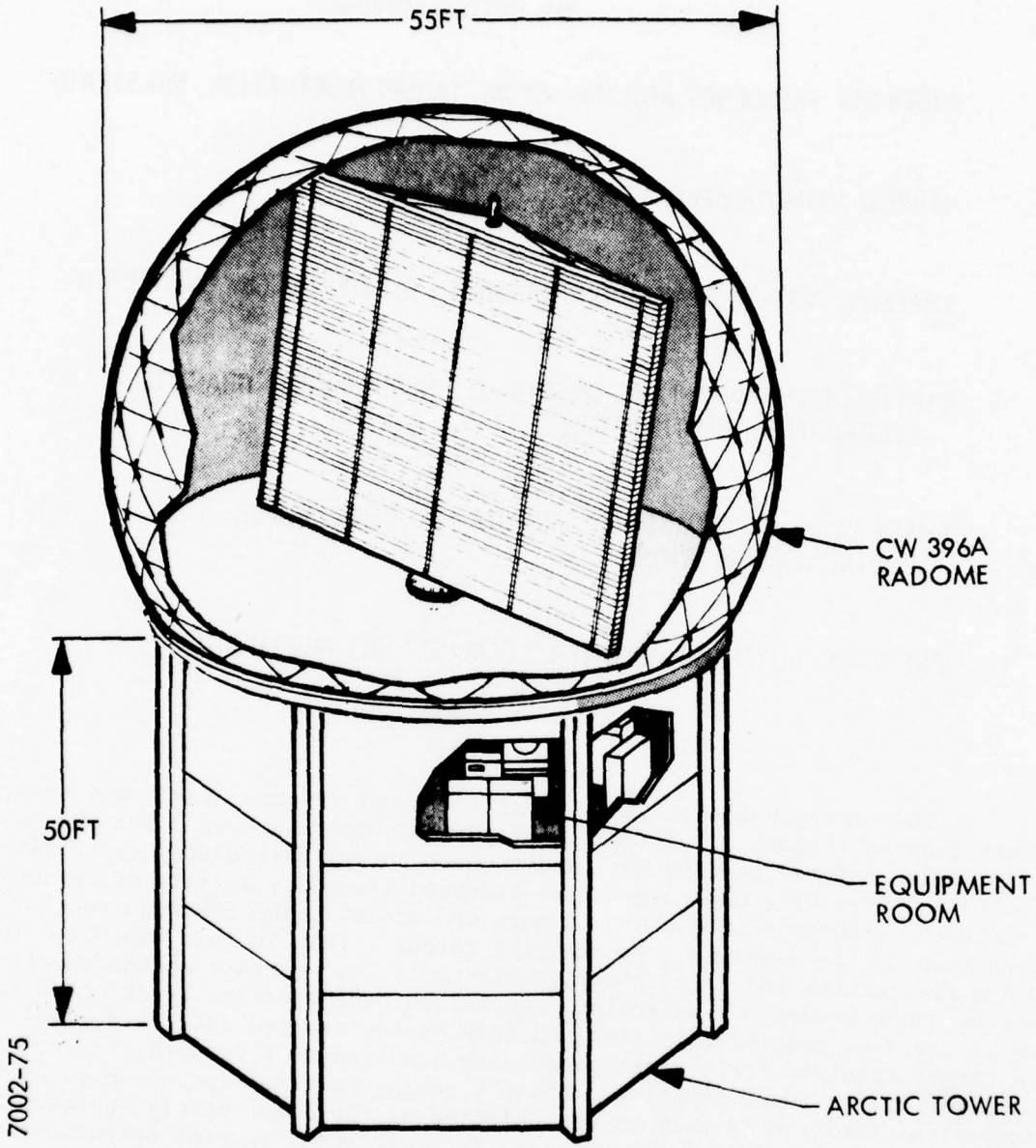

Figure 3.1-2. Artists Concept MAR

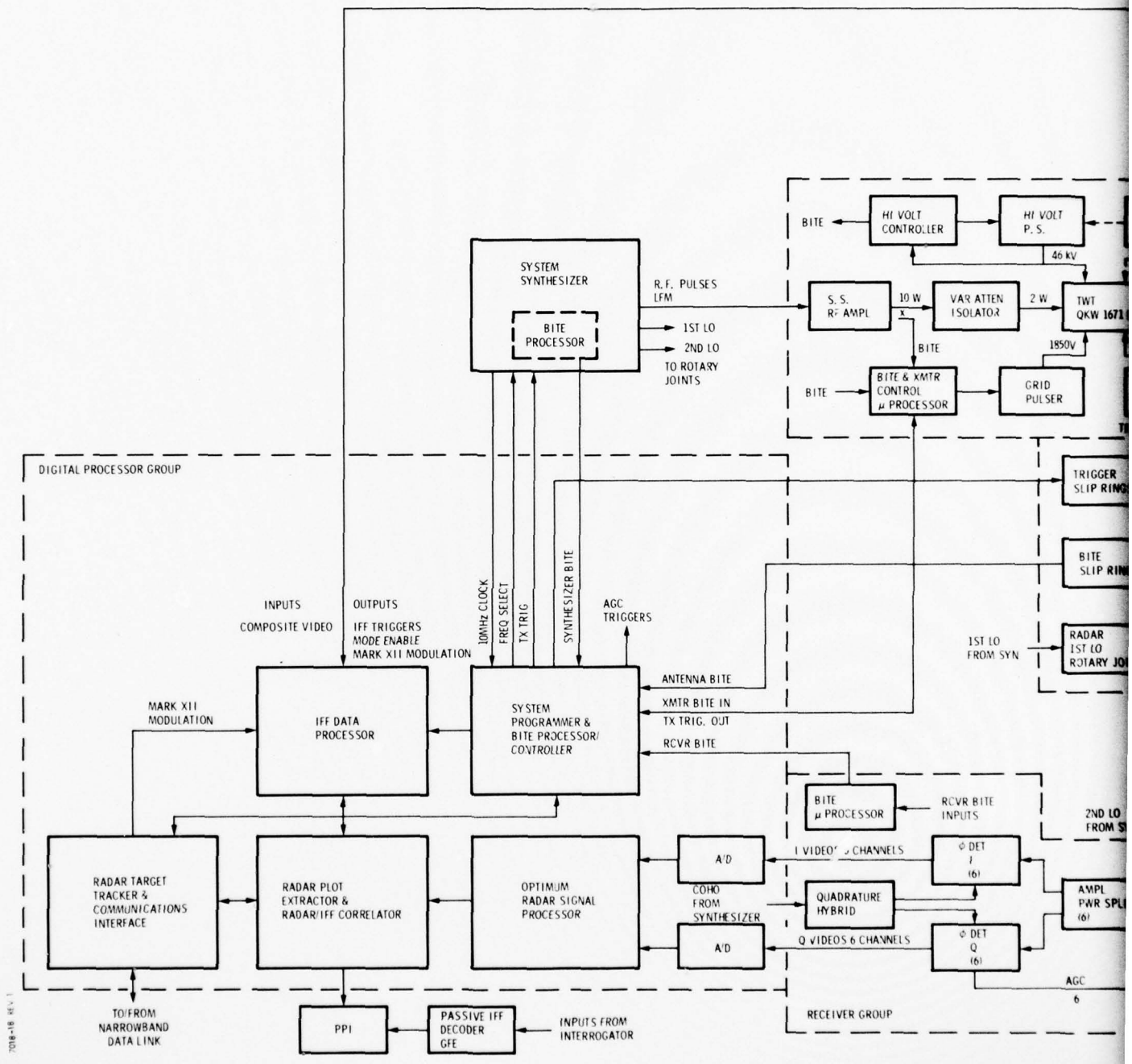
SYSTEM SYNTHESIZER
BITE PROCESSOR
R.F. PULSES LFM
1ST LO
2ND LO
TO ROTARY JOINTS
BITE
HI VOLT CONTROLLER
HI VOLT P.S.
46 kV
S.S. RF AMPL
10 W
VAR ATTEN ISOLATOR
2 W
TWT QKW 1671
1850V
BITE & XMTR CONTROL μ PROCESSOR
GRID PULSER
DIGITAL PROCESSOR GROUP
TRIGGER SLIP RING
BITE SLIP RING
RADAR 1ST LO ROTARY JOINT
1ST LO FROM SYN
INPUTS
COMPOSITE VIDEO
OUTPUTS
IFF TRIGGERS
MODE ENABLE
MARK XII MODULATION
10MHz CLOCK
FREQ SELECT
TX TRIG
SYNTHESIZER BITE
AGC TRIGGERS
MARK XII MODULATION
IFF DATA PROCESSOR
SYSTEM PROGRAMMER & BITE PROCESSOR/ CONTROLLER
ANTENNA BITE
XMTR BITE IN
TX TRIG. OUT
RCVR BITE
BITE μ PROCESSOR
RCVR BITE INPUTS
2ND LO FROM SYN
RADAR TARGET TRACKER & COMMUNICATIONS INTERFACE
RADAR PLOT EXTRACTOR & RADAR/IFF CORRELATOR
OPTIMUM RADAR SIGNAL PROCESSOR
A/D
I VIDEOS 6 CHANNELS
Φ DET I (6)
COHO FROM SYNTHESIZER
QUADRATURE HYBRID
AMPL PWR SPLIT (6)
A/D
Q VIDEOS 6 CHANNELS
Φ DET Q (6)
AGC
6
TO/FROM NARROWBAND DATA LINK
PPI
PASSIVE IFF DECODER GFE
INPUTS FROM INTERROGATOR
RECEIVER GROUP

Figure 3.1

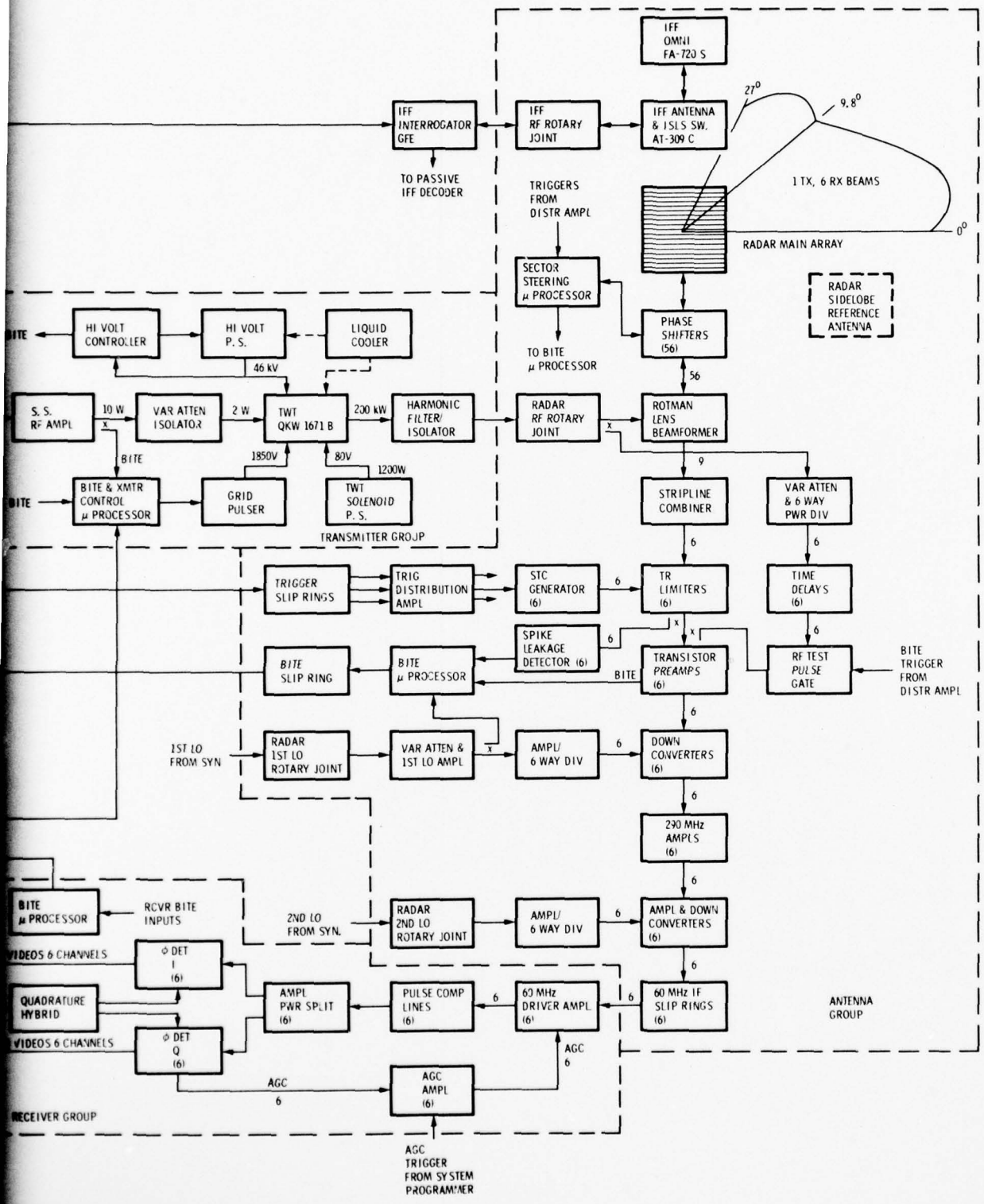

Figure 3.1-3. MAR Baseline Block Diagram

Operating Modes

In the normal (3D) mode of system operation, the MAR employs a broad shaped transmit beam to effect the desired spatial illumination. This rather broad transmit beam is phase scanned to sequentially illuminate two elevation sectors (a lower and an upper sector). The lower sector extends nominally from 0^{o} to $+10^{o}$ and the upper covers from $+10^{o}$ to $+27^{o}$. For receive six simultaneous beams are formed that cover the elevation extent of each sector, consequently the six receive beam group is also phase scanned in elevation. Data describing the six receive beams at mid frequency band are given below:

Beam #/ Sector	Instrumented Range Coverage	Beam Peak El Angle	Beam Width	Beam -3 dB Angles	Beam Peak Spacing/ Crossover Level
1/L	200 nmi	$+1.05^{o}$	2.06^{o}	$+0.02^{o}/+2.08^{o}$	
					$> 1.54^{o}/-1.6$ dB
2/L	200 nmi	$+2.59^{o}$	2.06^{o}	$+1.56^{o}/+3.62^{o}$	
					$> 1.54^{o}/-1.6$ dB
3/L	175 nmi	$+4.13^{o}$	2.06^{o}	$+3.10^{o}/+5.16^{o}$	
					$> 1.54^{o}/-1.6$ dB
4/L	145 nmi	$+5.67^{o}$	2.06^{o}	$+4.64^{o}/+6.70^{o}$	
					$> 1.54^{o}/-1.6$ dB
5/L	120 nmi	$+7.21^{o}$	2.06^{o}	$+6.18^{o}/+8.24^{o}$	
					$> 1.54^{o}/-1.6$ dB
6/L	100 nmi	$+8.75^{o}$	2.06^{o}	$+7.72^{o}/+9.78^{o}$	
					$> 2.06^{o}/-3.0$ dB
1/U	85 nmi	$+10.81^{o}$	2.06^{o}	$+9.78^{o}/+11.84^{o}$	
					$> 1.54^{o}/-1.6$ dB
2/U	75 nmi	$+12.35^{o}$	2.06^{o}	$+11.32^{o}/+13.38^{o}$	
					$> 1.54^{o}/-1.6$ dB
3/U	65 nmi	$+13.89^{o}$	2.06^{o}	$+12.86^{o}/+14.92^{o}$	
					$> 3.08^{o}/-3.0$ dB
4/U	55 nmi	$+16.97^{o}$	4.12^{o}	$+14.91^{o}/+19.03^{o}$	
					$> 4.12^{o}/-3.0$ dB
5/U	45 nmi	$+21.09^{o}$	4.12^{o}	$+19.03^{o}/+23.15^{o}$	
					$> 4.12^{o}/-3.0$ dB
6/U	40 nmi	$+25.21^{o}$	4.12^{o}	$+23.15^{o}/+27.27^{o}$	

The lower elevation sector transmit beam is a shaped beam that provides maximum gain over the region from 0^{o} to $+3.25^{o}$ in elevation and reduced gain ($\csc^2$ falloff) above $+3.25^{o}$ in elevation. The azimuth beamwidth (transmit/receive) is nominally 1.8^{o} at midband. Maximum gain at midband on transmit (lower elevation sector) is 31.5 dB and on receive (lower elevation sector) beam peak gain is 41.4 dB. Antenna losses attributable to cables, phase shifters and the Rotman Lens beamformer are 2.85 dB on transmit and 3.55 dB on receive.

In addition to the normal 3D mode, MAR can be operated in a 2D mode (fan beam on transmit and fan beam on receive) and in a Burnthrough (BT) mode (pencil beam(s) on transmit and pencil beam(s) on receive). The 2D mode is considered a degraded operational mode that requires only one of the six receive/processor channels. The BT mode could be employed to put more energy on specific targets of interest and/or as a possible aid in determining the height of targets at low elevation angles, i.e., embedded in the multipath environment. In the normal 3D operation mode the MAR employs amplitude comparison of data received in the azimuth beam and from adjacent elevation beams to measure target position in elevation and azimuth.

Antenna Group

The MAR antenna group consists of the radar array described above and in Section 3.2, plus an IFF antenna (GFE) mounted on back of the radar array. Thus, radar and IFF returns will be out of sync by 180^{o} in azimuth (approximately six seconds in time). The radar/IFF plot correlator in the digital processor is, however, implemented to compensate for this condition. Additionally, a radar sidelobe reference antenna is supplied for strobe reporting purposes which provide a receive pattern having sufficient gain to encompass all main array lower el sector receive beam sidelobes.

Waveform/Digital Processor

An unambiguous range waveform has been adopted for use in the MAR. The waveform used for system performance evaluations can be described as an 8-pulse coherent burst transmitted in the lower elevation sector followed by a single pulse transmitted in the upper elevation sector. This waveform constitutes one elevation scan. Nominally, three el scans (three 8-pulse bursts and three single pulses) are completed in the time it takes the antenna to rotate (at 5 rpm) through the 2^{o} azimuth beamwidth. See Figure 3.1-4. The waveform for each of these three el scans is transmitted at a different discrete radar frequency and each of the 8-pulse bursts is generated at a different, but constant, PRF to preclude blind speeds in the velocity region of interest extending to 3050 knots. The average interpulse period for the group-to-group PRF stagger is 2531 μsec. Interpulse period selections were made to minimize dim speeds in the velocity region extending from 80 knots to 585 knots.

The radar signal processor for the 8-pulse bursts is implemented as an "optimum processor" (MTD type) that provides an improvement (signal-to-clutter plus noise) factor of 50 dB minimum with ground clutter and 30 dB minimum with volumetric clutter. A filter centered at zero doppler is of interest and is synthesized to provide superclutter visibility of zero (and low) doppler frequency targets. To minimize the LRUs (board count) required to implement the "optimum radar signal processor," processing is provided only to the instrumented ranges shown for the six beams in the lower elevation sector.

To estimate (measure) target angular position in both elevation and azimuth, the radar plot extractor employs amplitude comparison of data from the azimuth beam and adjacent elevation beams.

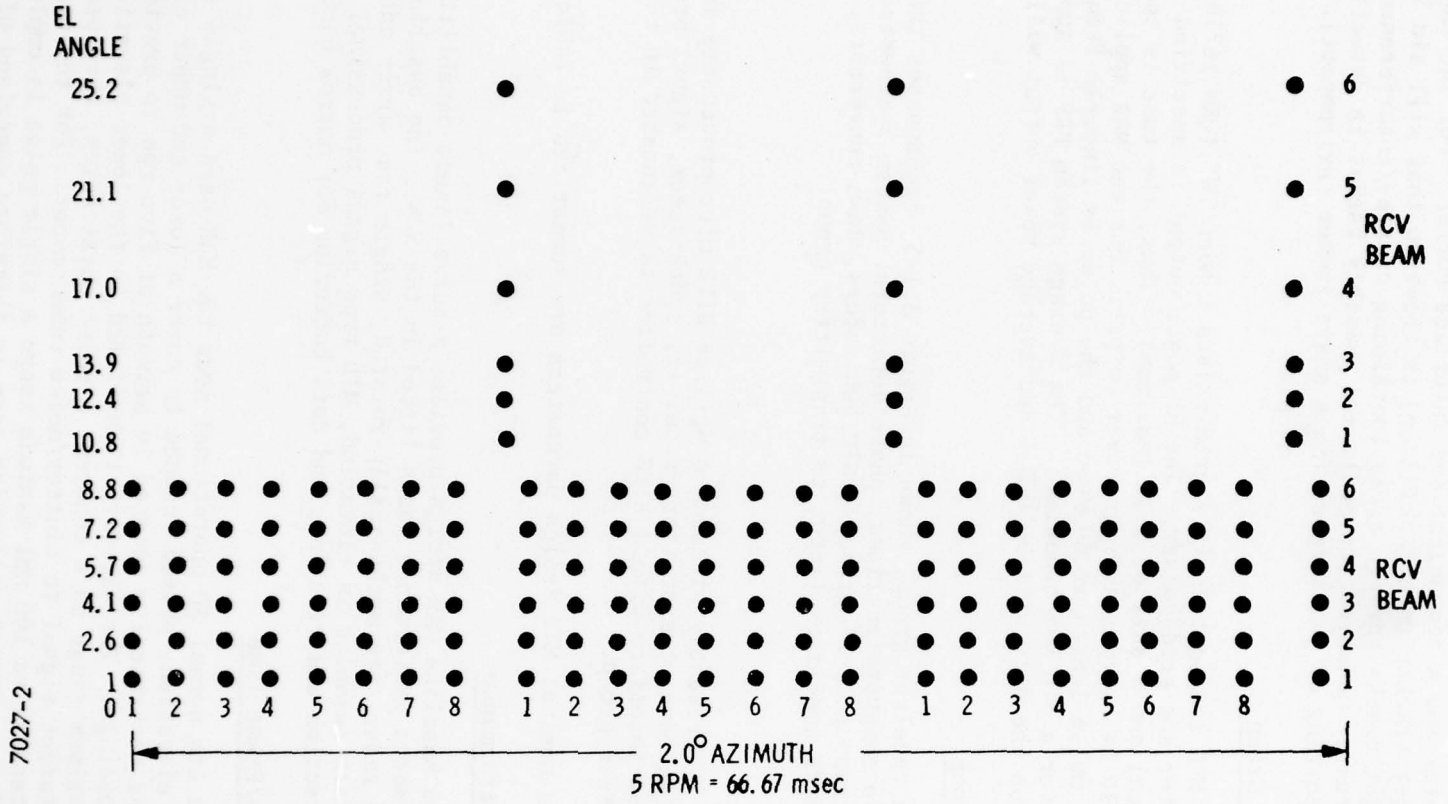

Figure 3.1-4. Typical Scan Program

The digital processor also provides an IFF data processor, a radar/IFF plot correlator and a communications interface buffer. For the MAR application, a target tracker (pretrack filter) is required that will aid in maintaining target tracks through areas containing clutter/interference residue that are normally censored (mapped), and possibly assist in detection/definition and reporting of jam strobes (in a smart jammer environment).

Transmitter Group

The MAR transmitter is a grid-pulsed L-band TWT (QKW 1671B) with solid-state inverter and grid pulser. The RF power output is specified at 200 kW peak (minimum) and a duty of 0.05 (maximum). Thus, the tube is capable of running at 10 kW maximum average power output. For the MAR application, the transmitted pulse length is 60 μsec and the pulse is linearly frequency modulated over a 3.0 MHz bandwidth. The average system PRF is approximately 417 Hz. Thus the duty will be 0.025 and average power output will be 5.0 kW.

Receiver Group

The receiver group, shown in Figure 3.1-3, encompasses the IF amplifiers, pulse compression lines, phase detectors, System synthesizer, TR limiters, transistor RF preamps, STC generators, down-converters, and the solid-state RF amplifier (input to transmitter group).

BITE

It is presently planned to utilize BITE microprocessors in each major subsystem (antenna, transmitter, receiver, synthesizer, signal processor) and to have them interface with a BITE controller to be located in the digital data processor group.

The nominal MAR design parameters are summarized in Table 3.1-2.

3.1.3 Performance

The baseline MAR design provides a surveillance capability that basically meets performance goals listed in the SOW. The baseline MAR is an L-band, 3D radar with mechanically-rotated, single face array antenna. It employs phase scanning in elevation, MTD type signal processing, automatic target detection and tracking, and data buffering for narrow band data remoting.

Dwell Time/Frame Time

In its normal 3D operational mode the MAR uses a single transmit beam shaped in elevation, phased scanned to cover a lower and upper elevation sector, and mechanically rotated in azimuth at five rpm to provide the desired spatial coverage. The waveform transmitted in the lower elevation sector to 200 nmi maximum range is a coherent 8-pulse burst which, when processed, provides target signal to clutter/noise enhancement. For the upper elevation sector extending to 100 nmi maximum range a single pulse is employed. The waveform for a complete elevation scan is therefore comprised of an 8-pulse burst plus a single pulse, with all pulses 60 μsec in length that are linear

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TABLE 3.1-2. MAR DESIGN PARAMETERS

SPATIAL COVERAGE	
ELEVATION	-2° TO +25°
ALTITUDE	HORIZON TO 100k ft
AZIMUTH	360° IN 12 SECONDS
P_D SINGLE SCAN	0.9 FOR $1m^2$ TGT @ 150 nmi
P_{FA}	10^{-6}
ACCURACY	
RANGE	≤200 ft
AZIMUTH	≤0.25°
HEIGHT	≤3000 ft @ 100 nmi
RESOLUTION	
RANGE	≤500 ft
AZIMUTH	≤2°
ELEVATION	≤2°

ANTENNA	
ELEVATION BEAM	13.5° T_x, 2° R_x
AZIMUTH BEAM	≤2°
GAIN (NO LOSSES INCLUDED)	31.5 dB T_x, 41.4 dB R_x
SIDELOBES	-30 dB MAX.
TRANSMITTER	
OPERATING FREQUENCY	1215 - 1400 MHz
PULSE WIDTH	60 μsec
PRF (MULTIPLE)	417 Hz AVERAGE
PEAK POWER	200 kW MIN.
AVERAGE POWER	5.0 kW
RECEIVER/PROCESSOR	
HITS/BEAMWIDTH	24 LOWER SECTOR, 3 UPPER SECTOR
NOISE FIGURE	2.0 dB (4.5 dB SYSTEM)
NUMBER CHANNELS	6
SIGNAL TO CLUTTER IMPROVEMENT	≥50 dB (GROUND), ≥30 dB (WEATHER/CHAFF)
PRIMARY POWER	≤75 kW

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frequency modulated having three MHz dispersion. Nominally, three elevation scans are completed in the time it takes the antenna at five rpm to rotate through 2^{o} (the azimuth beamwidth). The waveform for each of the three elevation scans is transmitted at a different radar frequency and at a different PRF (for the 8-pulse burst). For the three elevation scans: average time between the first and eighth pulse of the 8-pulse burst is 2531 μsec (200 nmi × 12.355 μsec/nmi + 60 μsec); average time from the start of the eighth pulse to the leading edge of the single pulse used in the upper elevation sector is 2551 μsec (the additional 20 μsec is the time required to switch the phase shifters); time from the start of the single pulse to the leading edge of the first pulse of the 8-pulse burst used in the lower elevation sector is 1315.5 μsec (100 nmi × 12.355 μsec/nmi + 60 μsec + 20 μsec). Thus, total average time required for a complete elevation scan is 21,583.5 μsec (7 × 2531 μsec + 1 × 2551 μsec + 1 × 1315.5 μsec), which is equivalent to an average system PRF ≅ 417 Hz. Three elevation scans require 64.75 m/sec and at five rpm the 2^{o} azimuth beamwidth scan time is 66.67 m/sec.

Waveform Processing

The MAR signal processor, an MTD type, provides 50 dB (ground clutter) and 30 dB (weather/chaff clutter) improvement factors. To provide sufficient data samples for the processor, the MAR illuminates every target in the lower elevation sector with three 8-pulse bursts (average PRF ≅ 395 Hz). Each of the three bursts is transmitted at a different radar frequency and different but constant PRF. The radar frequency changes between the 8-pulse bursts effectively alter target fluctuation statistics from Swerling I to those more closely represented by Swerling III. PRF changes between 8-pulse bursts eliminate blind speeds over the target velocity region of interest, and the constant PRF within a burst precludes possible difficulties with returns from second-time-around clutter (at ranges beyond 200 nmi). The MAR illuminates every target located in the upper elevation sector, i.e., above $\sim 10^{o}$ elevation, with three single pulses. Targets in this sector in rain (30,000-ft altitude ceiling) cannot be at ranges greater than about 30 nmi from the radar. At this short range, the S/C resulting from 3-pulse processing should be sufficient for detection without having to resort to clutter processing. This assumes a $\Sigma_{\sigma_i} \cong -87$ dB (16 mm/hr rain) and a 16 m^2 target (due to target aspect at this elevation angle). For targets in chaff at higher altitudes, a CHAFF mode of system operation could be employed illuminating the upper elevation sectors with the 8-pulse burst waveform/MTD type processing where specifically required.

The transmitted waveform employs pulses that are linearly frequency modulated with three MHz dispersion over their 60 μsec width which provides approximately 250 foot system range resolution after pulse compression.

System Losses

The baseline MAR system losses are embodied in two parameters L_R and L_S. L_R represents those losses incurred on receive that contribute to the effective system noise temperature, and L_S represents all other system losses not contained in L_R. The 3.55 dB value for L_R is the summation of the phase shifter element insertion loss = 1.25 dB, a cabling loss = 1.0 dB and the beamformer loss = 1.3 dB. The 14.65 dB value for L_S is the summation of the following losses:

Atmospheric loss (2 way to 150 nmi for 1^o elevation)	= 1.8 dB
Antenna loss on transmit	= 2.85 dB
(consisting of phase shifter = 1.25 dB, cables = 1.0 dB, beamformer = 0.6 dB)	
Harmonic filter, waveguide and rotary joint	= 0.5 dB
Beam shape	= 3.0 dB
Signal processing loss	= 6.5 dB
	14.65 dB

System Operating Noise Temperature/Factor

The system noise temperature referred to the antenna face is determinable from:

$$T_S \simeq T_a + T_0 (L_R F - 1)$$

where

T_a = antenna sky noise temperature $\cong 65^oK$ at 1^o elevation and 1300 MHz

T_0 = ambient temperature (assumed as 290^oK)

L_R = receive loss = 3.55 dB = factor of 2.26

F = RF preamplifier noise figure = 2 dB = factor of 1.58

$T_S \simeq 65^oK + 290^oK (2.26 \times 1.58 - 1) = 810^oK$

The system operating noise factor $(NF)_0 = T_S/T_0 = 810^oK/290^oK = 2.79 = 4.5$ dB.

RF Power

The RF power that must be transmitted to assure detection of a $1m^2$ target at 150 nmi slant range can be determined from:

$$E = \frac{S/N \; R^4 \; L_s \; (NF)_0}{\upsilon \; G_T \; G_R \; \sigma \; \lambda^2 \; \eta}$$

where

E = single pulse energy required for detection (joules)

S/N = single hit S/N required for 0.9 P_D and 10^{-6} P_{FA} for Swerling III target ($\cong$ 17.5 dB)

R = required detection range (nmi) = 150 ($R^4 = 150^4 = 87.0$ dB)

L_S = system losses (dB) = 14.7 dB

$(NF)_0$ = system operating noise factor = 2.79 = 4.5 dB

υ = conversion factor for mixed units employed = 0.3 dB

G_T = antenna gain on transmit (no losses) = 31.5 dB

G_R = antenna gain on receive (no losses) = 41.4 dB

σ = target cross section = $1m^2$ = 0 dB

λ = operating wavelength (cm); for 1300 MHz = 23.08 cm, λ^2 = 27.3 dB

η = integration gain for 24 hit processing = 12.4 dB.

From above it is determined that the single pulse energy required is 10.8 dB above 1 joule, or 12 joules/pulse which corresponds to the transmitter output pulse energy (200 kW peak pulses × 60 μsec length = 12 joules).

Performance in Land Clutter

For the worst case situation, i.e., 4500 foot MAR site above MSL, detection of a low flying $1m^2$ target at 60 nmi range in ground clutter could be required. For this situation the ground clutter RCS can be found from:

$$RCS_G = \frac{1.06\ \theta_1\ R_{RES}\ R}{\sqrt{2}}\ \sigma^o$$

where

1.06 = normalizing factor to account for clutter intake from ±10° of beam axis

$\theta_1/\sqrt{2}$ = 2 way -3 dB azimuth beamwidth = $1.8^o/\sqrt{2}$

R_{RES} = system range resolution = 50 meters

R = range to the target and clutter = 60 nmi

σ^o = clutter reflectivity = σ^o_{50} = -34 dB (median).

From the equation RCS_G = 17.2 dB. After processing by the MTD type signal processor, the median S/C will be (-17.2 dB + 50 dB) 32.8 dB. With the log-normal clutter statistics and a 10 dB standard deviation (from the SOW) target detection will be permitted at the 2.77 sigma which will accommodate >99th clutter percentile.

Performance in Rain

The clutter limiting detection performance due to a 30K feet rain ceiling occurs at 105 nmi range. This is the maximum range at which any of the MAR's receive beams can be filled with rain. For this situation the rain clutter RCS can be found from:

$$RCS_R = \frac{\pi}{4}\ \theta_1\ \phi_1\ R_{RES}\ R^2\ \Sigma_{\sigma_i}$$

where

θ_1 = 1 way azimuth beam = 1.8^o

ϕ_1 = 1 way elevation beam = 2.06^o

R_{RES} = system range resolution = 50 meters

R^2 = square of the range to the target = $(105\ nmi)^2$

Σ_{σ_i} = clutter reflectivity = -87 dB (for 16 mm/hr rain).

From the equation RCS_R = 5.25 dB. Since a 17.5 dB S/C is required for 0.9 P_D and the MAR signal processing loss is 6.5 dB, the required clutter improvement factor is 5.25 + 17.5 + 6.5 = 29.25 dB. A small safety margin for detection is therefore assured by the MTD type processor providing $\geq$ 30.0 dB improvement.

Data Accuracy

The height accuracy of the baseline MAR is primarily determined by the nominal 2^o elevation beamwidths and high S/N returns. The elevation angle of arrival of target returns will be determined in the MAR digital processor to the accuracy needed to provide height measurements within ±3000 feet (or better) for fluctuating targets at 100 nmi slant range. Azimuth accuracy should be determinable to $\leq 0.25^o$.

Prime Power Consumption

Prime power consumption of the MAR is predicted to be $\leq$60 kW. Budgeted allocations are as follows:

Antenna Group	6.0 kW	(includes 2.5 kW heater for lubricants)
Receiver Group	2.0 kW	
Transmitter Group	43.0 kW	
Signal Processor	3.0 kW	
Data Processor	3.0 kW	
IFF Interrogator (GFE)	2.0 kW	
Display	1.0 kW	
	60.0 kW	

Growth to Unattended Operations

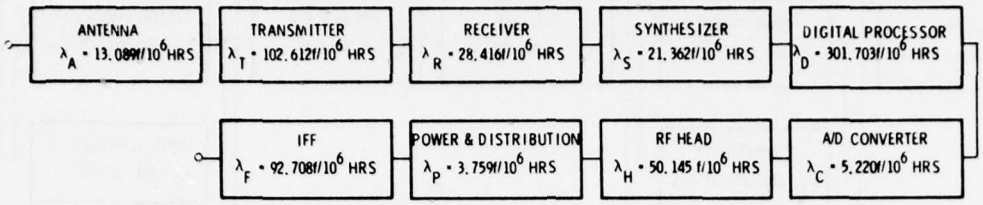
Reliability of the baseline MAR has been estimated at 1615 Hour MTBF including IFF. The major failure rate contributors are the IFF Interrogator (λ = 93 f/10^6 hrs), radar digital processor (λ = 301 f/10^6 hrs) and the radar transmitter (λ = 103 f/10^6 hrs). Through redundancy the MAR MTBF could be increased to on the order of 5000 hours which would supply a 90 percent probability of failure-free operations for a 22-day period. This may be sufficient in some applications to qualify for unattended operations status.

3.1.4 System Reliability

A reliability prediction for the MAR design was developed in accordance with the same procedures used for the UAR prediction (reference section 2.1.5). Detail parts data on subassemblies of the MAR were used and nominal failure rates for detail part types, as used in the UAR prediction, were applied to calculate the equipment reliability. As in the UAR prediction, high quality and reliability parts were considered to be used throughout the MAR. Contained in Appendix F are detail parts data and failure rates for the MAR assemblies.

Figure 3.1-5 contains the reliability block diagram and math model for conceptual design of a series configured MAR. With exception of the Antenna, there is no redundancy considered in this configuration. The conceptual design Antenna is a phased array antenna using 60 finite phase shifters for beam control. Inherent in this type antenna is an allowable soft degradation which provides inherent active redundancy. In each of four sections of the antenna, one phase shifter and driver circuit can fail without causing MAR performance degradation below the level of full operational requirements. Figure 3.1-6 contains the block diagram and math model of the Antenna which presents the phase shifter and driver circuits redundancy.

The MAR configuration contained in Figure 3.1-5 is predicted to have an inherent reliability of 0.901 for a seven day (168 hours) continuous operational period and -0.928 for a five day operational period . For operational time periods greater than seven days, redundant items can be added to the series configuration to provide a reliability of at least 0.9. Contained in Figure 3.1-7 is the math model for a one-half month MAR which uses an active redundant transmitter and a standby redundant DP assembly to provide a reliability of 0.918 for a one-half month (365-hour) mission. Reliability of at least 0.9 can be realized in a one-month and a three-month MAR through simplification of the present MAR conceptual design and through further trade-off analyses to incorporate optimum redundancy.



$\lambda_{MAR} = \lambda_A + \lambda_T + \lambda_R + \lambda_S + \lambda_D + \lambda_C + \lambda_H + \lambda_P + \lambda_F = 619.014\ f/10^6$ HOURS

$R_{MAR} = R_A R_T R_R R_S R_D R_C R_H R_P R_F$

$R = e^{-\lambda t}$

R_{MAR} (168 HOURS) = 0.901

R_{MAR} (120 HOURS) = 0.928

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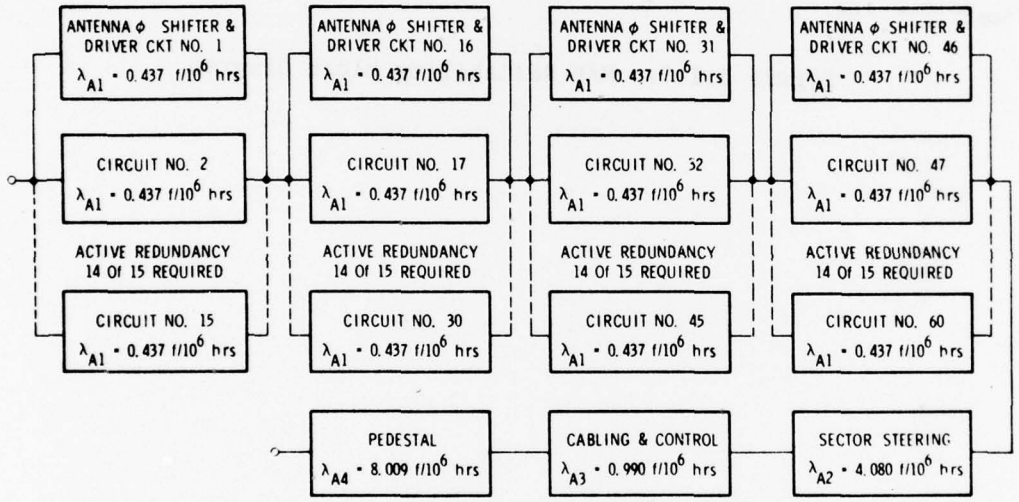
Figure 3.1-5. MAR Reliability Block Diagram



PHASE SHIFTER REDUNDANT FAILURE RATE: λ'_{A1} (5 DAYS) = 0.0024 f/10^6 HOURS FOR 1 OF 4 SECTIONS

λ''_{A1} (0.5 MO) = 0.0073 f/10^6 HOURS FOR 1 OF 4 SECTIONS

λ_A (5 DAYS) = $4\lambda'_{A1} + \lambda_{A2} + \lambda_{A3} + \lambda_{A4}$ = 13.0886 f/10^6 HOURS

λ_A (0.5 MO) = $4\lambda''_{A1} + \lambda_{A2} + \lambda_{A3} + \lambda_{A4}$ = 13.1082 f/10^6 HOURS

$R_A = \left(15R_{A1}^{14} - 14R_{A1}^{15}\right)^4 R_{A2} R_{A3} R_{A4}$

R_A (5 DAYS) = 0.998

R_A (0.50MO) = 0.995

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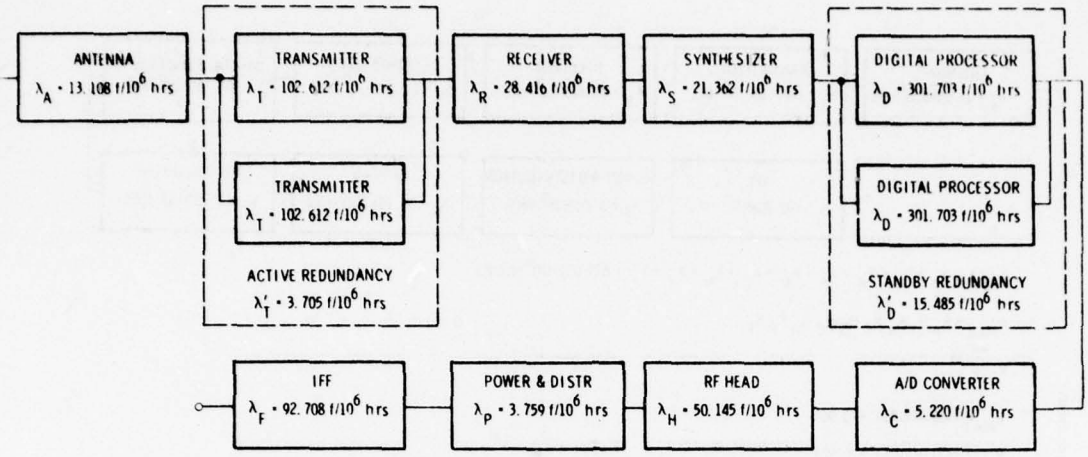
Figure 3.1-6. MAR Antenna Reliability Math Model



$$\lambda_{MAR} = \lambda_A (0.5\ mo) + \lambda'_T + \lambda_R + \lambda_S + \lambda'_D + \lambda_C + \lambda_H + \lambda_P + \lambda_F = 233.908\ f/10^6\ HOURS$$

$$R_{MAR}(365\ HOURS) = R_A\left(2R_T - R_T^2\right) R_R R_S \left[R_D\left(1 + 365\lambda_D\right)\right] R_C R_H R_P R_F$$

$$R_{MAR}(365\ HOURS) = 0.918$$

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Figure 3.1-7. MAR Reliability Block Diagram

3.2 MAR Antenna Design

During transmission the antenna radiates a fan beam, and during reception the incoming signals are received simultaneously by a cluster of pencil beams. All beams are horizontally polarized, phase scanned in elevation and mechanically scanned in azimuth. The horizontally polarized antenna (Figure 3.2-1) can form a fan beam, a pencil beam, or a cluster of pencil beams with very low azimuth sidelobes. The beam is mechanically scanned 360 degrees in azimuth at five rpm, and is phase scanned 27 degrees in elevation. The overall characteristics of this planar array are listed in Table 3.2-1.

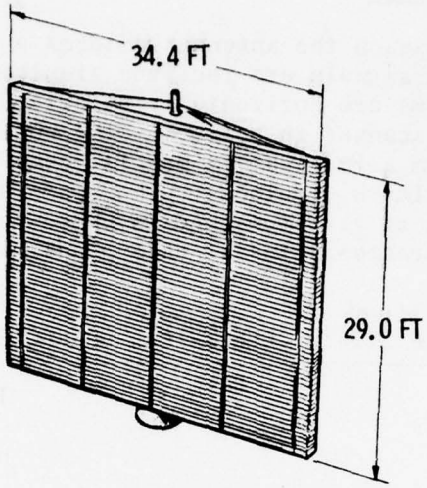
TABLE 3.2-1. ELECTRICAL CHARACTERISTICS

Operating Frequency	1215 - 1400 MHz
Polarization	Horizontal
Sidelobes:	
Cardinal Planes Azimuth	-30 dB Max ($<20^{o}$) -40 dB Max ($>20^{o}$)
Elevation (Sum Output)	-30 dB Max
Intercardinal Planes	-40 dB Median (5^{o} to 20^{o}) -50 dB Median (20^{o} to 90^{o})

The principal component of the elevation beam-forming network (see Figure 3.2-2) is a parallel-plate Rotman lens 8-feet long by 6-1/2 feet wide*. This lens has 56 antenna ports connected to waveguide slotted arrays via 4-bit phase-shifters, nine ports connected to the receive outputs of the beam-forming system, and a single port connected to the high-power input from the transmitter. The input power is propagated to the 56 antenna ports, lens geometry being such that the antenna ports receive signals with a symmetrical amplitude taper thus generating an elevation fan beam. This fan beam can be scanned to either of two sectors by selecting the appropriate phase-shifter commands or it can be a specially shaped beam (e.g., to reduce ground clutter) by other phase-shifter commands.

On reception, incoming signals at the 56 lens ports are focused at the nine output ports, and after passing through receiver protectors and amplifiers, these nine signals are processed in a stripline combining network to provide six simultaneous sum beam outputs corresponding to the six beams in either elevation sector. The combiner is designed to produce output beams each with 2.1^{o} half-power beamwidth and sidelobes better than 35 dB below the beam peak, spaced 1.54^{o} apart and crossing at 1.6 dB below the peak. Outputs from the combiner are mixed with the first local oscillator frequency to

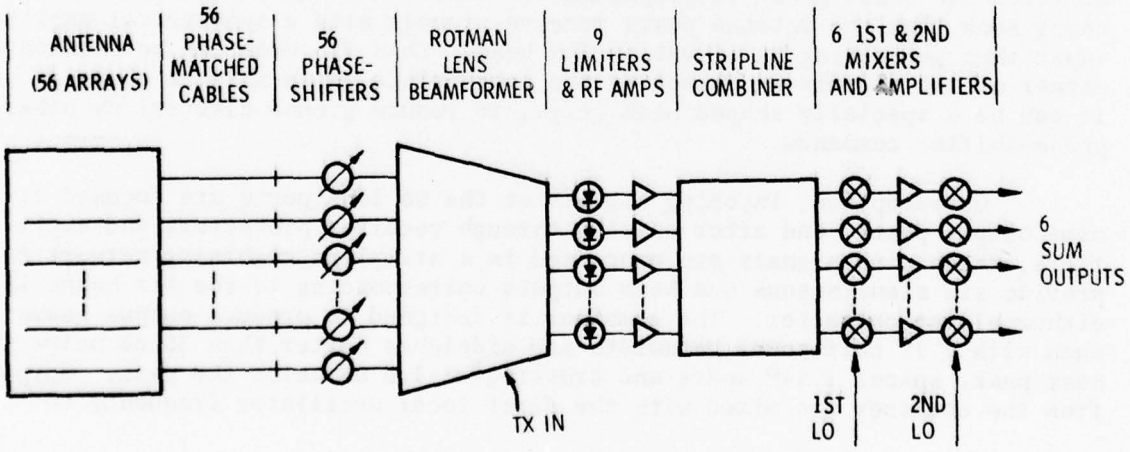
*"Wide-Angle Microwave Lens for Line Source Applications", W. Rotman and R.F. Turner, IEEE Trans., Vol. AP-11.



OVERALL WIDTH ..... 10.5 m (34.4 feet)	OVERALL HEIGHT ..... 8.8 m (29.0 feet)
EFFECTIVE (APERTURE) WIDTH ..... 10.1 m (33.0 feet)	ARRAY SPACING ..... 15.9 cm (6.25 inch)
ARRAY SLOT SPACING ..... 12.4 cm (4.9 inch)	NUMBER OF ARRAYS 56
NUMBER OF SLOT PAIRS 82	ANTENNA TILT-BACK ..... 8.5 DEGREES
ARRAY WAVEGUIDE ..... 16.5 X 8.3 cm	
CROSS SECTION ..... (IEC-R14)	

7002-145

Figure 3.2-1. Antenna Mechanical Characteristics



7002-144

Figure 3.2-2. Antenna Schematic

produce nominally 290 MHz signals, then amplified and mixed with the second local oscillator frequency to produce nominally 60 MHz signals, and finally amplified again before being transmitted through slip-rings to the receivers.

Each of the 56 horizontal linear arrays (see Figure 3.2-3 for photo of one array) has 82 dual radiating slots which couple RF energy from the waveguide as it propagates from the feed end toward the array end load. These dual slot radiators provide not less than twice the bandwidth of the "industry accepted" single slots used on production antennas. This characteristic ensures much more uniform coupling across the required frequency band resulting in significantly lower sidelobes at the band edges. The coupling of edge slot radiators is designed to provide the horizontal linear array elements with a -50 dB Chebyshev aperture illumination, while coupling out 94 percent of the input power; the remaining six percent is dissipated in the array matched end loads. This slightly less-efficient, lower-sidelobe design is required to assure less than -40 dB azimuth plane sidelobes beyond ±20 degrees from beam peak for production antennas. Table 3.2-2 lists the antenna gains and beamwidths at three operating frequencies.

Coupling of the dual edge slot radiators is proportional to the angle at which the slots are cut in the waveguide narrow wall. The larger the slot angle, the greater the power coupled by the slot from the waveguide.

The FA-7202 (ATC-309C) IFF Antenna is mounted at the rear of the array, with its associated FA-7205 omnidirectional SLS antenna at the top of the array.

BITE for the antenna monitors all important operating functions: waveguide pressurization, antenna drive motor current, and encoders.

3.3 MAR Transmitter Design

The MAR transmitter consists of a 10-watt, solid-state amplifier, a high power L-band travelling wave tube (TWT), a 46 kV high voltage power supply, a grid modulator, performance and fault monitoring meters and indicators, and appropriate safety devices. The transmitter contains liquid cooling supply and return lines for connection to an external heat exchanger system.

TABLE 3.2-2. GAIN AND BEAMWIDTHS FOR TRANSMISSION AND RECEPTION

Freq. (MHz)	Transmission Gain (Fan beam) (dB)	Reception Gain (dB)	Az Beamwidth at -3 dB Points (Degree)	El Beamwidth at -3 dB Points (Sum beam) (Degree)
1215	28.0	37.1	1.97	2.20
1305	28.6	37.8	1.77	2.06
1400	29.2	38.4	1.63	1.91

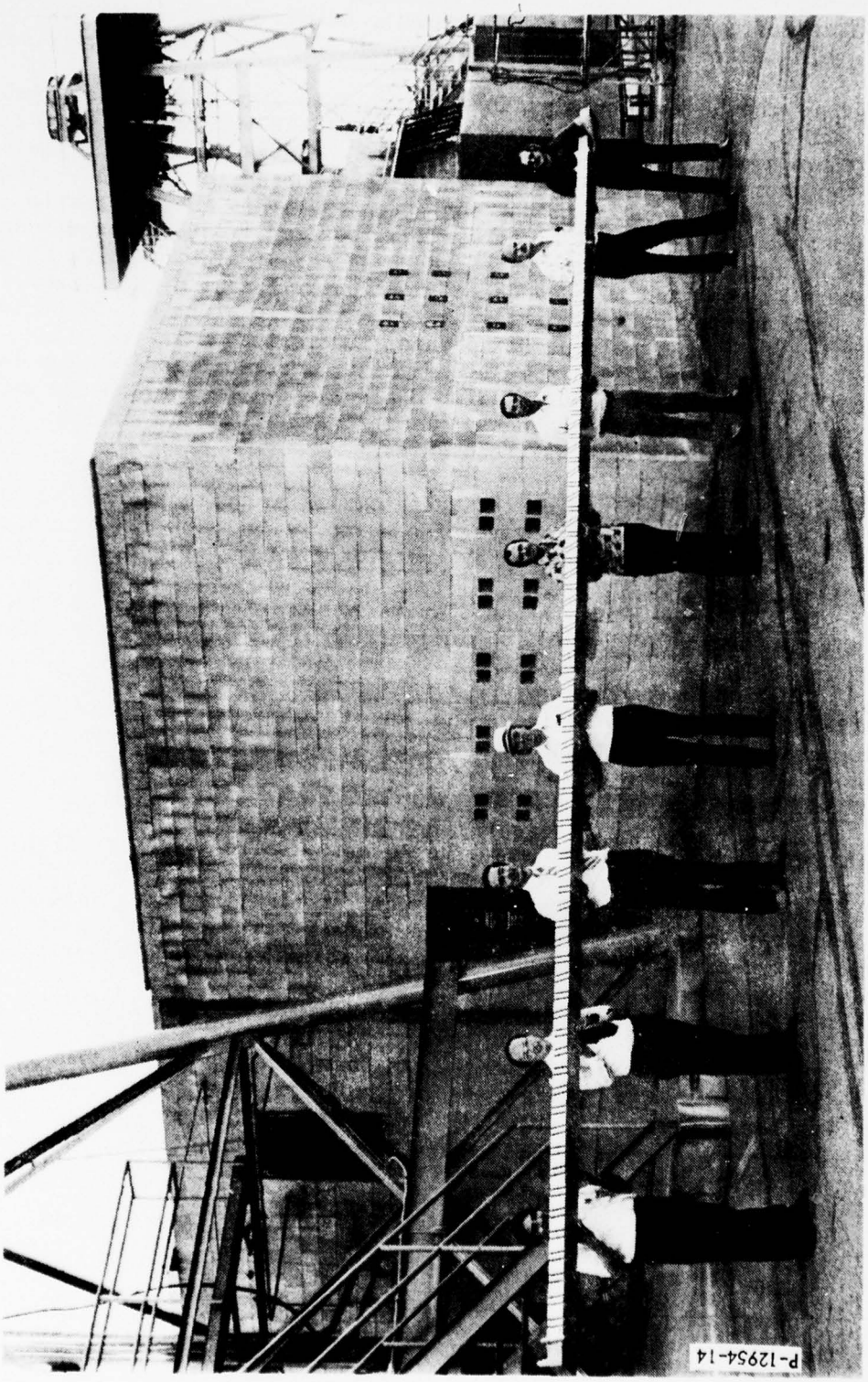


Figure 3.2-3. L-Band Array

A pulsed microwave power source from the radar exciter provides an input to the transmitter. This drive is amplified to 200 kW peak by the 10-watt amplifier and the TWT. The high-gain, gridded TWT is pulsed on by the grid pulser in synchronism with the RF drive to the transmitter.

Performance Characteristics

The transmitter characteristics are shown in Table 3.3-1. Table 3.3-2 shows the transmitter phase-stability budget required for MAR clutter processing. TWT cathode and grid voltages have the greater phase sensitivity. The voltages are well regulated to limit the total rms phase deviation to 0.090 degree (60.9 dB stability) thus providing a margin in satisfying the 55 dB minimum transmitter stability budget. The total phase deviation is a worst-case estimate based on specified, rather than typical, TWT phase sensitivities, which would not likely occur. The cathode voltage sensitivity of 100^{o}/kV of change requires that the peak-to-peak, pulse-to-pulse variation be held to within 1.73V. The cathode voltage variation is limited to this value by employing a bootstrap regulator in the high voltage power supply in conjunction with inverter preregulation. In addition, the TWT grid voltage is regulated and clamped to a constant level.

Transmitter Physical Characteristics

Figure 3.3-1 shows a pictorial layout of the transmitter. It is composed of standard aluminum structural shapes and panels built into a rigid framework compartmented to suite the electronics. Cabinets are similar to units currently in production. All compartments are fully accessible from the front by either hinged or removable panels. All panels are mounted with a combination of guide pins and quick-release fasteners and, when in place, function as shear plates for enhanced structural rigidity.

TABLE 3.3-1. TRANSMITTER CHARACTERISTICS

Transmitter Type	Crystal Controlled Master Oscillator Power Amplifier (MOPA)-TWT
Frequency Bandwidth	1200-1400 MHz, Instantaneous
RF Power Output-Peak	200 kW
RF Power Output-Average	5 kW (10 kW max)
RF Pulsewidth	60 μsec
Stability	55 dB, Min
RF Tube Type	Raytheon QKW 1671B, Gridded, Solenoid Focused TWT

TABLE 3.3-2. TRANSMITTER STABILITY

The phase stability budget allocated to the transmitter for a 60 dB MTI Improvement using the QKW 1671B TWT is as follows:

Parameter	QKW 1671B Spec. Reference *Deg/Volt or* Deg/dB	RMS[1] *Pulse-to-Pulse* Variation	Peak-to-Peak *Pulse-to-Pulse* Variation	RMS[2] *Phase* Variation Deg.
Cathode Voltage	0.1^{o}/V	0.500V	1.732V	0.0500
Collector Voltage	0.001^{o}/V	19.05V	66.0V	0.01905
Grid Voltage	0.75^{o}/V	0.00577V	0.020V	0.00433
Filament Voltage	0.01^{o}/V	0.1443V	0.50V	0.001443
Solenoid	$4^{o}/1^{o}\Delta$ is	0.005%	0.0173 %	0.02
RF Drive	12^{o}/dB	0.0058 dB	0.020 dB	0.00696

$$\sigma \Delta \phi^{(2)} = 0.09^{o}$$

Note (1): Peak-to-Peak = $\sqrt{12}$ RMS (for a uniform distribution)

Note (2): $[(0.05)^2 + (0.01905)^2 + (0.00433)^2 + (0.001443)^2 + (0.02)^2 + (0.0696)^2]^{1/2} = 0.09^{o} = 0.00157$ radians $= \sigma \Delta \phi$

IF (Improvement Factor) = $\dfrac{3}{\Delta \phi^2}$ (Note 3)

where

$$\frac{3}{\Delta \phi^2} = 1.216 \times 10^6$$

$\therefore$ IF = 10 Log 1.216×10^6 = 60.9 dB

Note (3): Nathanson, F.E. "Radar Design Principles," Equation 9-22, Page 342, McGraw-Hill Book Co.: New York, 1969.

High voltage components such as capacitors, grid pulser, the HV transformer, etc., are installed in separately-shielded compartments to effect maximum separation from low-voltage sections. Access panels to these areas are equipped with safety interlocks and self-acting shorting bars. Assemblies of smaller components, such as the inverters are slide-mounted. Shear pins are provided on the rear of each slide-out chassis for positive positioning. The mating surfaces of all access panels contain appropriate EMI gaskets for RF leakage suppression. The overall packaging concept has arranged subassemblies and components for logical circuit flow, minimum interconnection lengths, maximum accessibility, and personnel safety.

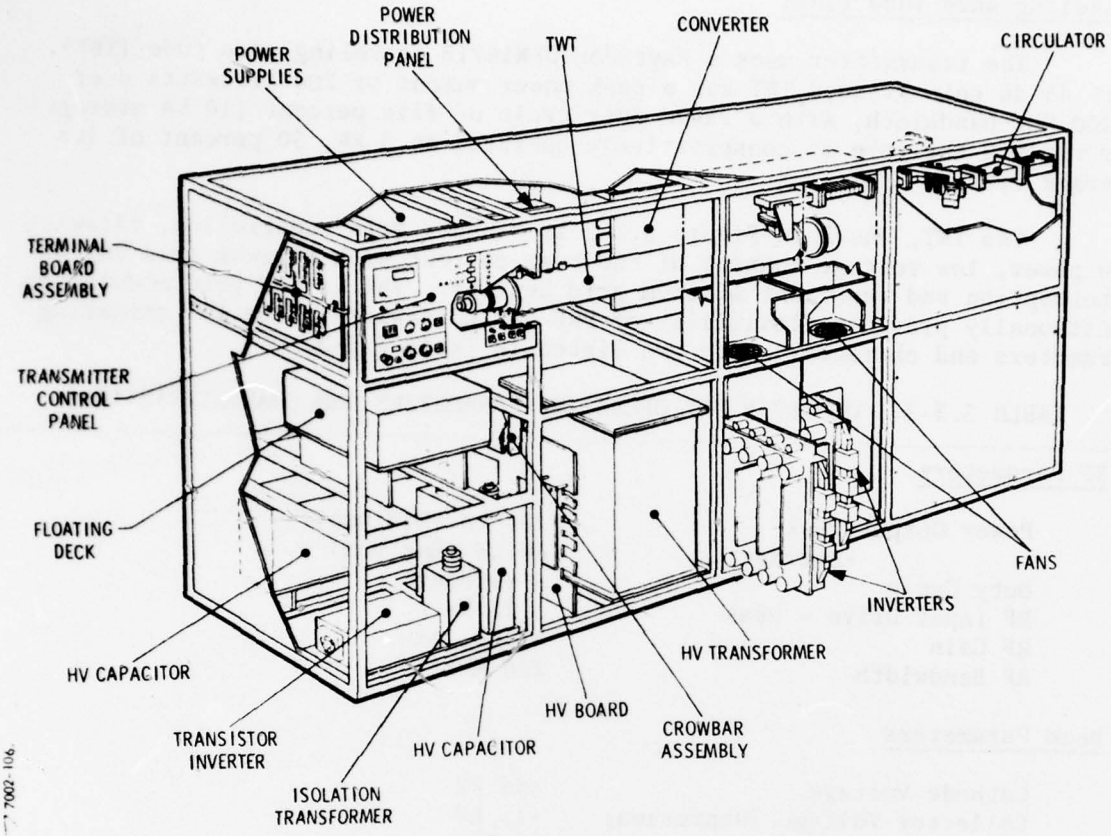


Figure 3.3-1. L-Band TWT Transmitter

Traveling Wave Tube (TWT)

The transmitter uses a Raytheon QKW1671B traveling wave tube (TWT). This 45 dB gain-gridded TWT has a peak power output of 200 kilowatts over a 200 MHz bandwidth, with a rated duty cycle of five percent (10 kW average). For the MAR the tube is conservatively operated at 5 kW, 50 percent of its average rating.

The TWT, shown in Figure 3.3-2 is "shadow grid" controlled, allowing low power, low voltage control of the beam current with minimum grid current interception and resultant minimum grid heating. The use of grid modulation additionally provides flexibility of PRF and pulsewidth. The TWT operating parameters and characteristics are listed in Table 3.3-3.

TABLE 3.3-3. QKW1671B TWT OPERATING PARAMETERS AND CHARACTERISTICS

RF Parameters	
Power Output-Peak	200 kW (Minimum)
-Average	10 kW (Maximum)
Duty Cycle	5 percent
RF Input Drive - Peak	1.25 Watt
RF Gain	45 dB, min.
RF Bandwidth	200 MHz
Beam Parameters	
Cathode Voltage	-46 kV
Collector Voltage (Depressed)	-15 kV
Beam Current - Peak	16.5A
Grid Parameters	
Grid Bias Voltage	-800V
Grid Pulse Voltage - Peak	+1800V
Grid Current - Peak	100 mA
Grid Type	"Shadow Grid"
Mechanical Characteristics	
RF Input - Connector	Type SC
RF Output - Waveguide	WR 650
Focusing	Solenoid
Cooling	Water or Water & Ethylene Glycol
Length	75 inches
Weight	75 kilograms

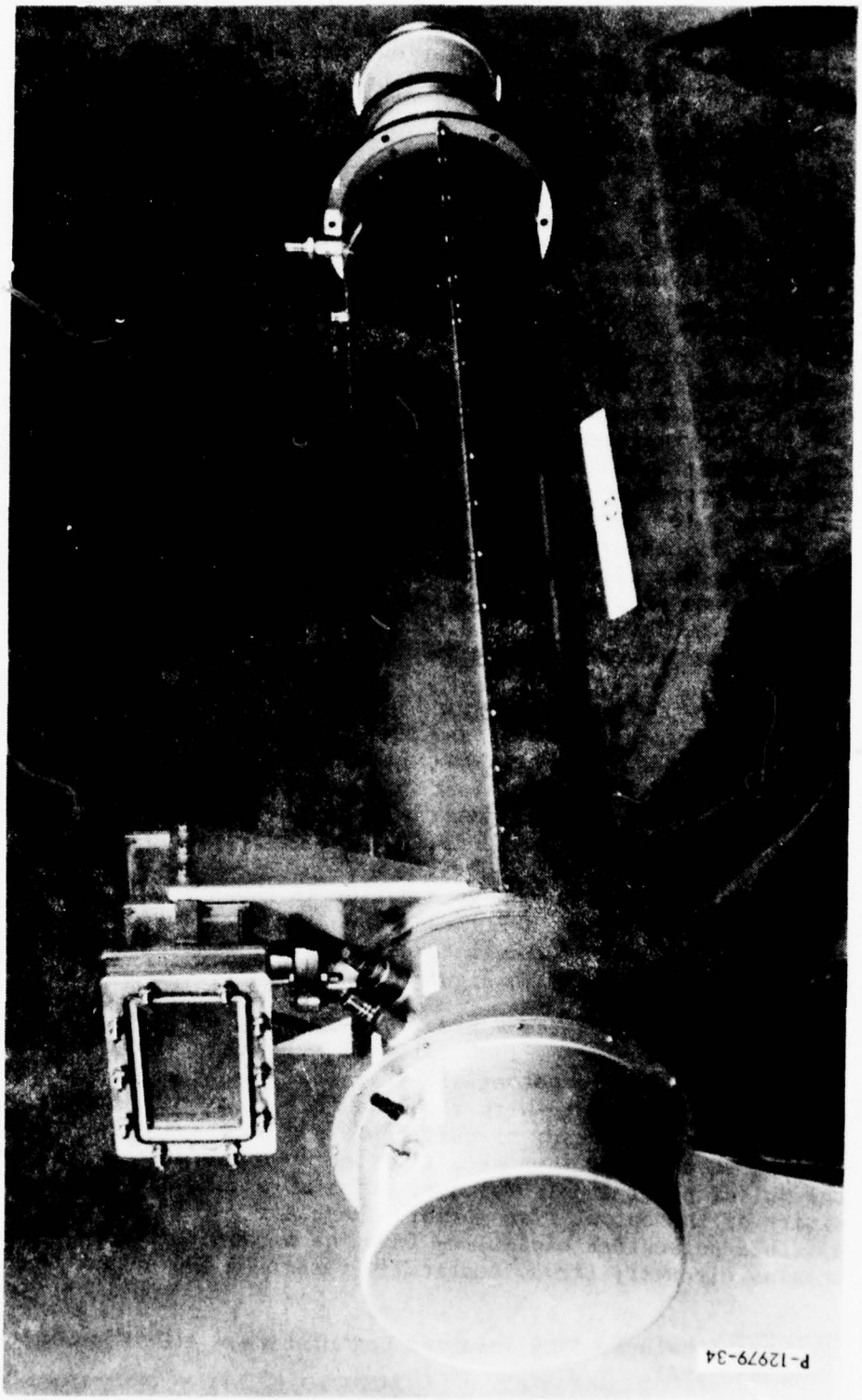


Figure 3.3-2. QKW1671B TWT

TWT HV Power Supply and Pulser

A solid-state, high voltage, power supply provides TWT cathode and collector voltages with efficient regulation, rapid response and margin in achieving 55 dB minimum transmitter stability.

The TWT high voltage power supply (HVPS), uses a single, high-voltage transformer with a solid-state bridge rectifier assembly to provide the TWT cathode and collector voltages. A capacitor filter, on the cathode and collector high voltage outputs, yields clean, low ripple voltages and provides adequate energy storage for minimum pulse droop. The HVPS is regulated by a primary inverter to achieve overall pulse-to-pulse phase stability. Figure 3.3-3 shows a block diagram of the TWT transmitter.

Regulation is provided by feeding back a sample of the cathode voltages from a resistive-capacitive (RC) divider to the primary inverter which operates to maintain constant cathode voltage. On the output of the HVPS, a crowbar protective circuit senses abnormal TWT current and triggers a spark gap, rapidly discharging the storage HV capacitors, and inhibiting inverter triggers. If the transmitter BITE indicates no faults, or a clearance of faults, the transmitter automatically recycles back to operate. The 3-phase prime input power is converted to dc power by a solid-state converter, which also includes a ramp-up circuit to reduce inrush current to the storage capacitors. The dc power is converted to 2 kHz ac power by a single solid-state inverter module. The inverter module is the McMurray SCR[1] type which provides high efficiency with reduced SCR stress.

A modular, low power, solid-state grid pulser, which floats at the TWT cathode voltage, provides grid bias and turn-on pulses. Turn-on and turn-off triggers supplied by the radar programmer are optically coupled to the grid pulser. The TWT RF driving signal is bracketed by the TWT voltage pulse and thus the RF rise and fall time is determined by the RF drive signal. The grid pulse provides complete programming flexibility of pulse duration and PRF.

A pictorial diagram of the grid pulser is shown in Figure 3.3-4 and a simplified schematic is shown in Figure 3.3-5. An oscilloscope picture of the output pulse showing a video swing in excess of 2800 volts and a pulsewidth in excess of 100 sec is shown in Figure 3.3-6.

The grid pulser provides a video output swing of 2800 volts to bring the grid from a bias level of - 1000 volts to 1800 volts where a diode and power supply clamps the grid potential. The grid pulser is capable of delivering a longer pulsewidth with rise and fall times of 0.5 μsec or better, at up to 0.08 duty. The pulser circuit employs a bootstrap transistor switch circuit coupled to the load through a 1:2 step-up transformer. The switch applies the pulser power supply voltage, adjustable from 350 to 700 volts, to the primary of the output transformer. Forced reset is employed to obtain maximum possible pulsewidth capability from the transformer core. The pulser contains circuitry for automatically resetting the output transformer

Note 1: McMurray/Shatuck, "SCR Inverter Commutation," AIEE Paper 61-718, November 1961.

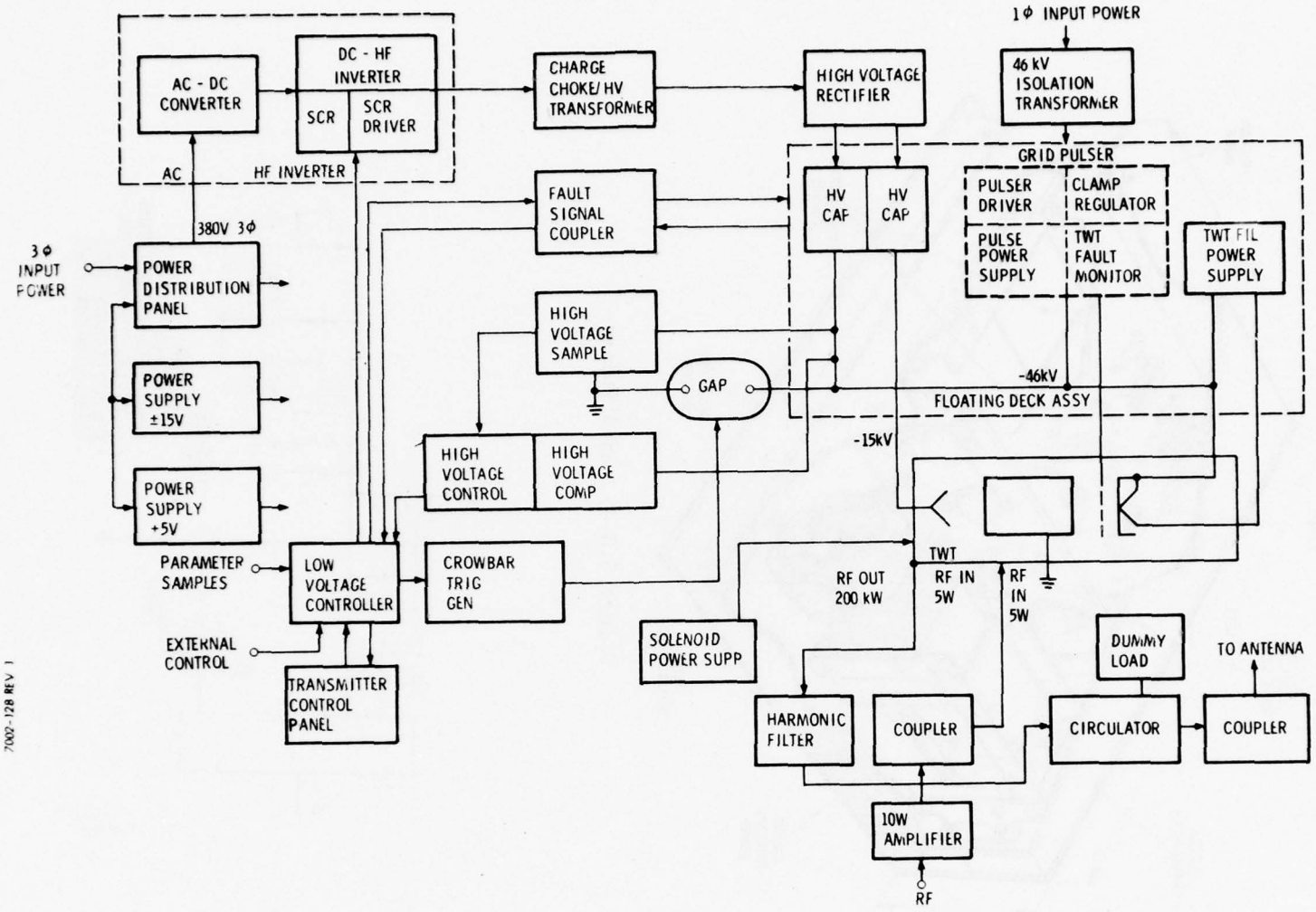


Figure 3.3-3. Block Diagram of TWT Transmitter with Solid-State High Voltage Power Supply

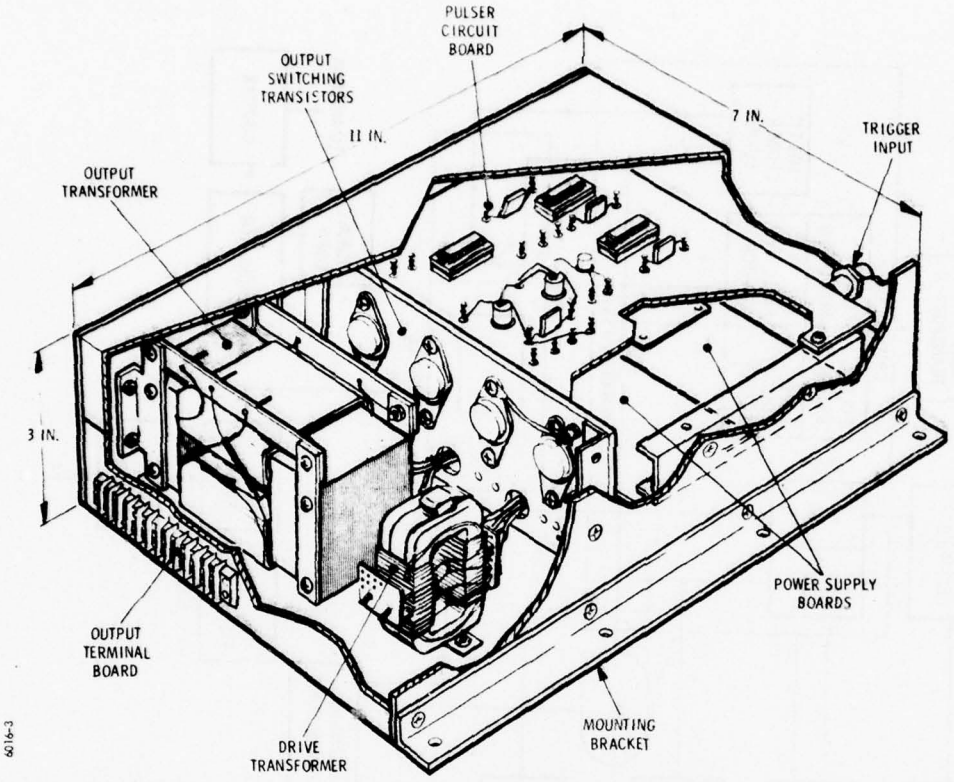


Figure 3.3-4. Grid Pulser

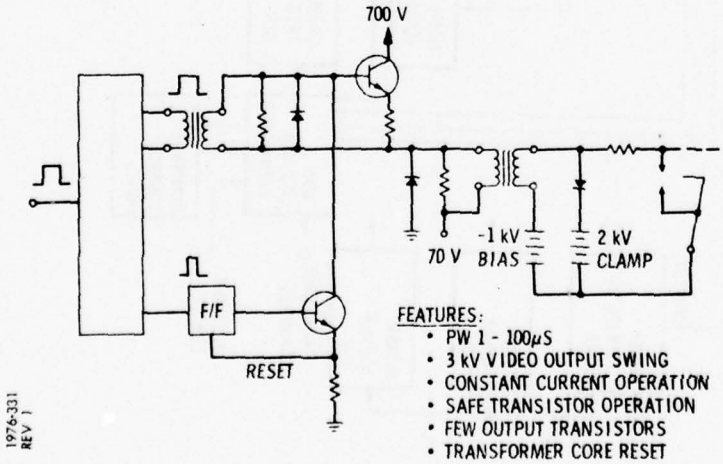


Figure 3.3-5. Grid Pulse Modulator

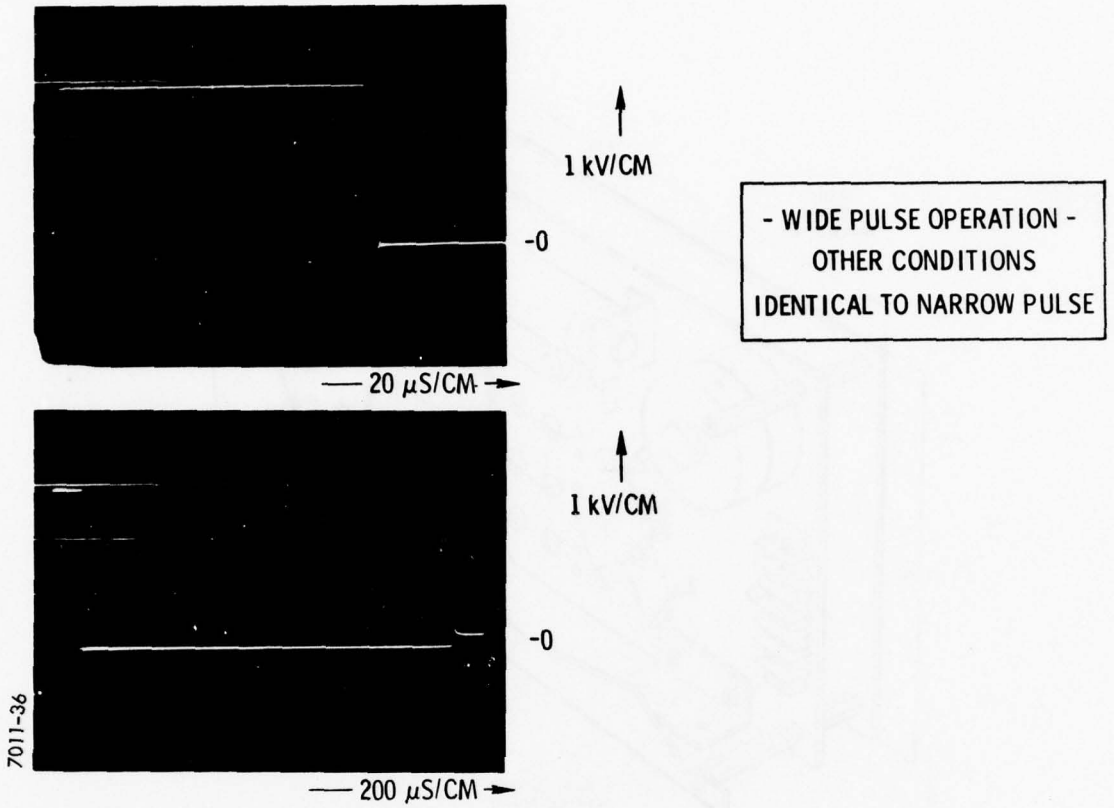


Figure 3.3-6. Grid Pulser Output Voltage

core under all operating conditions. The grid bias power supply (see figure 3.3-7) is fed to the grid through the secondary winding of the transformer. The pulser power supply and the filament power supplies are both flyback converter type units (see Figure 3.3-8 and 3.3-9). The control circuitry, pulsewidth modulator circuitry and input power circuitry are identical for both power supplies. The output transformer is different to provide 28 volts for the filament power supply and 350 to 700 volts for the grid pulser power supply. The long-term regulation of each power supply is ±1 percent.

Microwave System

The proper microwave environment is extremely important to insure a long operating life of the TWT. The TWT is followed by a high power circulator to provide the proper isolation and match requirements. In the event of arcing or a high VSWR in the waveguide system, the abnormally high reflected power is sampled by a directional coupler and coupled to transmitter control circuitry to prevent damage.

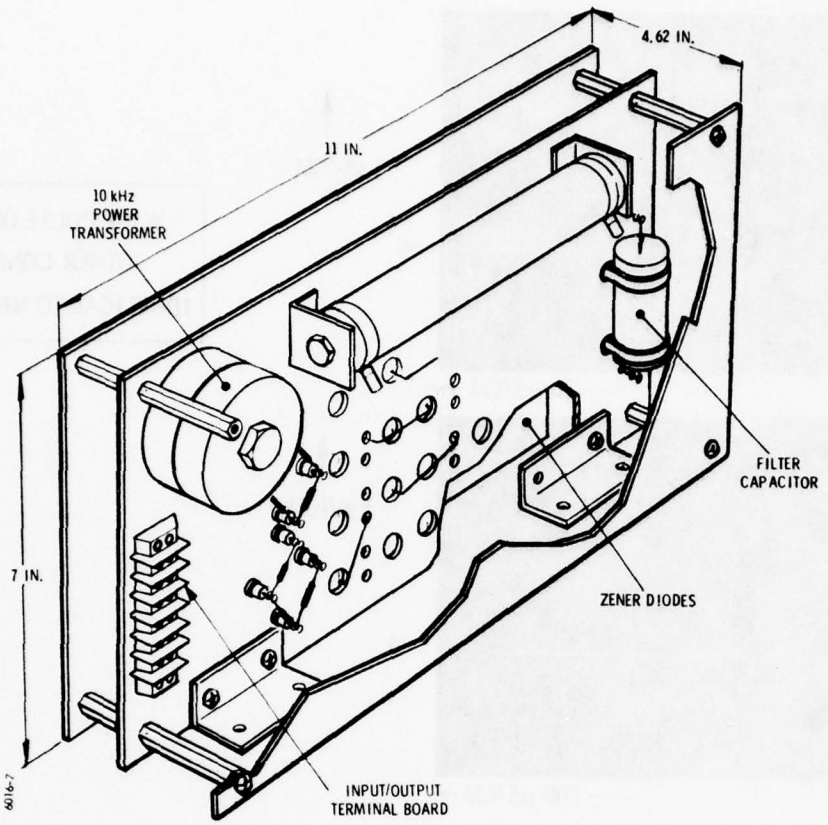


Figure 3.3-7. Grid Bias Power Supply

The input RF signal to the transmitter from the exciter is amplified by a 10-watt amplifier located in the transmitter. The signal is routed to the input of the TWT through a variable attenuator to set the proper drive of 5 watts maximum for saturated operation, and a coaxial isolator to provide the proper match for the TWT. The TWT produces a minimum output of 200 kW peak at an average operating power level of 5 kW. Loss through the harmonic filter, circulator and waveguide is less than 0.5 dB. The waveguide system is pressurized to 140 kPa or 20 psi with dry air to produce reliable high power operation.

Hardwave Status

The L-band TWT transmitter described herein is being designed and developed by ITT Gilfillan. During 1976, major subsystems of the transmitter were designed. Assembly of many of these subsystems is complete and testing has begun. Based on the design parameters discussed, an electrical design

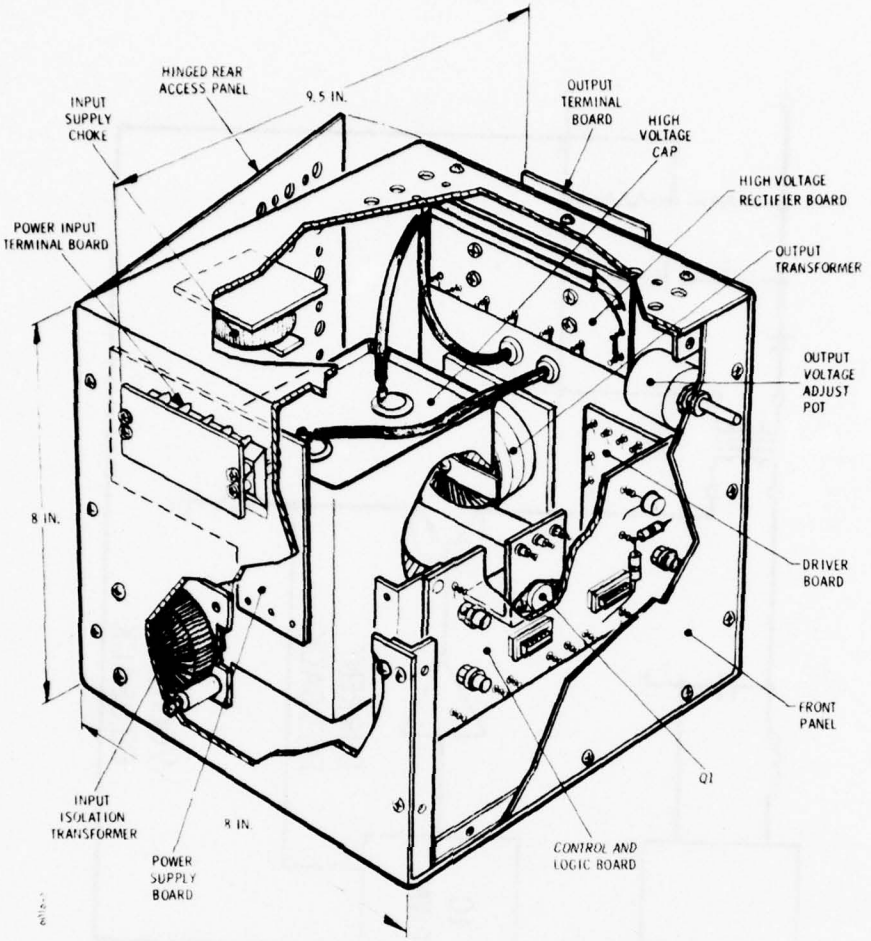


Figure 3.3-8. Pulser or Screen Power Supply

model was prepared including block diagrams, stage input/output requirements, and subassembly input/output requirements. As the design progressed, sizes were established for each of the subassemblies, and unit design history compiled via detailed design memos for future use.

A TWT has been purchased and is ready for transmitter integration. During 1977, assembly and test of the transmitter will be completed.

3.4 MAR FREQUENCY SYNTHESIZER DESIGN

3.4.1 Description

The Frequency Synthesizer supplies the local oscillator frequencies required for the MAR receivers and exciter. These include the first local oscillator which covers 925 to 1110 MHz, the second LO at 228.88 MHz, and the COHO at 57.222 MHz. The basic MAR Synthesizer is similar to the UAR Synthesizer except for addition of the second LO frequency. A crystal oscillator at 171.666 MHz supplies the basic reference from which all other frequencies are derived.

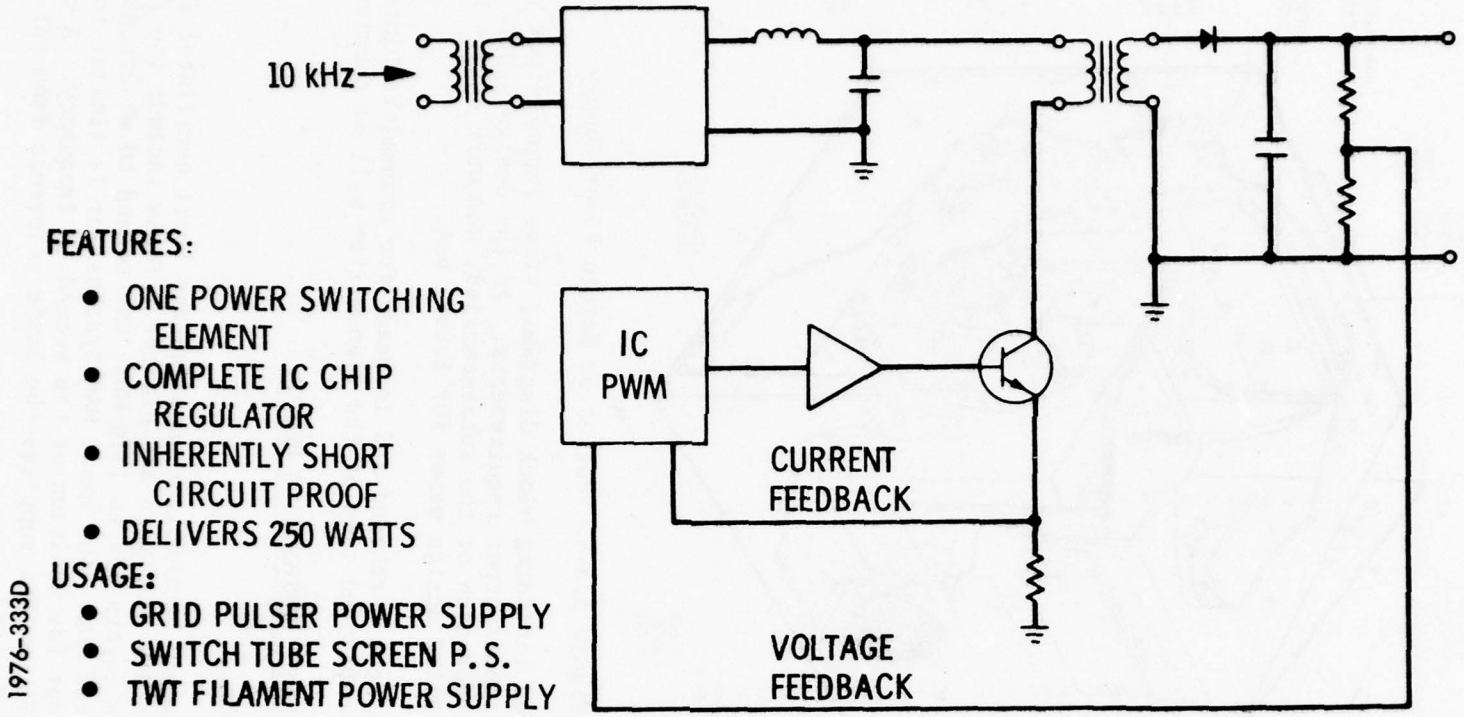


Figure 3.3-9. Flyback Inverter Power Supply

The block diagram in Figure 3.4-1 shows the basic configuration used. All fixed frequencies are generated by direct multiplication and filtering from the reference. The main receiver tunable frequencies are obtained from a dual phase locked loop configuration. The fine frequency step size is 6.0 MHz yielding 32 discrete operating frequencies across the 1215-1400 MHz RF band.

Because of the addition of the second LO output, it is expected that the synthesizer for the MAR will consist of four field replaceable modules, the coarse phase locked loop, the fine loop, the multiplier reference, and the second LO generator.

3.4.2 BITE

Built-in test (BITE) will identify failure of any module, with its replacement requiring no tuning or adjustment. Power detectors and comparators monitor input and output signals of each module, and when the levels drop below minimum, a fault signal is generated.

3.5 MAR RECEIVER-EXCITER DESIGN

3.5.1 Radar Receiver Description

The block diagram of the MAR Receiver-Exciter is shown in Figure 3.5-1. The MAR radar receiver requires six separate channels to process

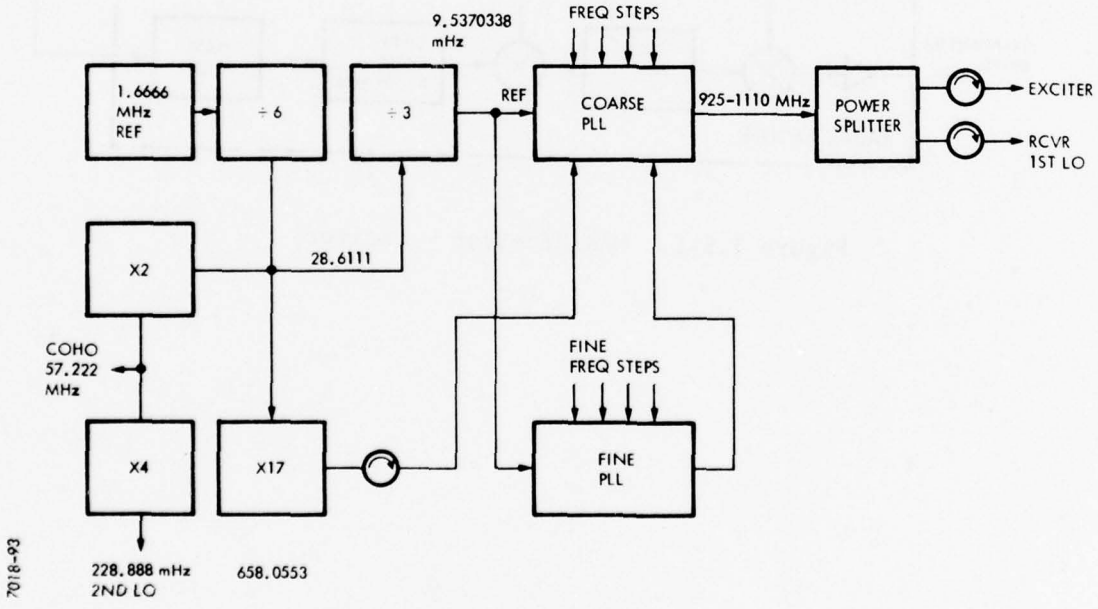


Figure 3.4-1. MAR Frequency Synthesizer

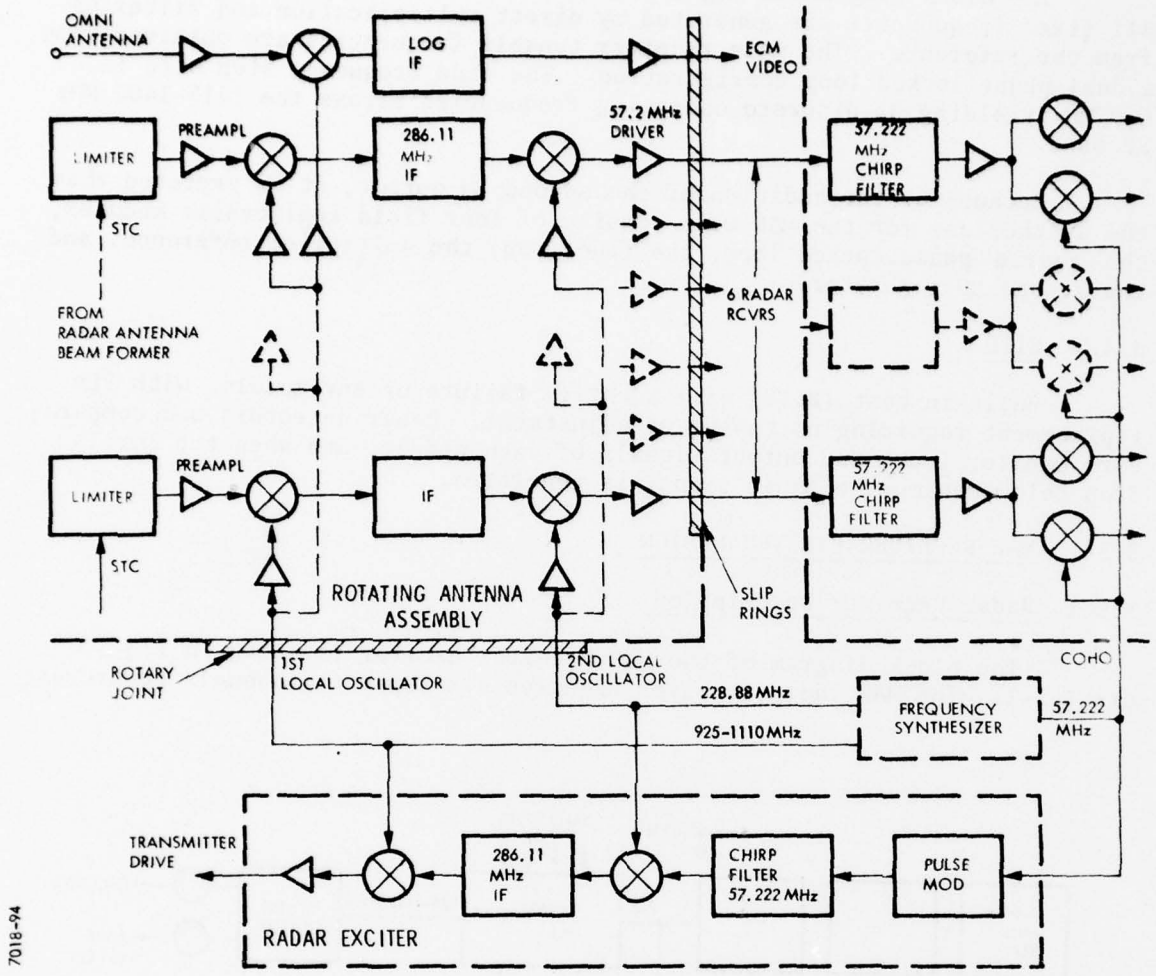


Figure 3.5-1. MAR Receiver - Exciter

the return signals. Each receiver channel differs from the UAR by the addition of one more conversion, to bring the received signal down to a 57.2 MHz IF.

The receiver front ends through the second conversion are situated on the rotating antenna assembly and the 57 MHz if outputs are transmitted down to the RADAR equipment room via slip rings. The rest of the receiver, i.e. the chirp lines and the IQ demodulators are located in the RADAR equipment room. This arrangement minimizes the number of high frequencies transmitted via slip rings.

The first and second local oscillator frequencies from the Synthesizer are transmitted via rotary joints to the rotating antenna assembly where they are power-split into 6 channels, then buffered and amplified to keep spurious and interchannel interference to a minimum.

Each radar receiver channel contains a saw dispersive delay line which decodes and correlates the received waveform. IQ demodulation is accomplished by dual balanced phase detectors with quadrature COHO signals.

Each receiver is packaged in three field replaceable modules. The input components through the RF preamp comprise one module, the first and second IF mixers and drivers comprise the second module and the chirp saw filter and IQ demodulator, the third.

3.5.2 ECM Receiver

The ECM Receiver gets its input from the omni antenna and generates log video for comparison with the main antenna received signals. The receiver is located on the antenna assembly and consists of filter, limiter, preamp, first mixer, and log amplifier. One down conversion via the first LO sets input to the log IF at 286 MHz. The ECM video output of the log amp is transmitted to the processor via slip rings.

3.5.3 Radar Exciter Description

The Radar Exciter provides the pulsed chirp signal to the transmitter. The final signal is generated by an up-conversion process which is the reverse of the reception signal flow. The COHO frequency of 57.22 MHz is pulse modulated, and then transformed into an fm pulse by the chirp filter. The second and first LO signals are used to up-convert this pulse to the proper radar transmit frequency.

3.5.4 BITE

The six MAR radar receiver channels and the ECM receiver contain a total of 19 field replaceable modules; all of which have internal BITE. All the input LO and COHO signals are monitored for power level. An RF pulse sample from the exciter is applied to all receiver inputs. The IP or video outputs of each module are monitored for the proper pulse amplitude by a detector comparator. Any fault detections are transmitted to the digital processor. The exciter BITE is similar to that described for the UAR.

3.6 MAR Signal Processor Design

The MAR signal processor design is an extension of the UAR signal processor concept to provide three dimensional data from a multibeam radar. Both the filter concept (near-optimum eight-filter bank), and the modularity concept of the UAR processor have been adopted for the MAR processor. The major differences in design of the two processors are as follows:

(a) The MAR system uses a wider band waveform (3 MHz as opposed to 0.75 MHz), processes signals to a greater range (200 miles as opposed to 60 miles), and processes signals from six beams simultaneously. Hence, several times as much hardware must be used in the MAR processor.

(b) Elevation data extraction requires an amplitude comparison of signals received via adjacent beams. This use of amplitude data implies preservation of amplitude throughout the various stages of signal processing to a greater extent than that required in the UAR processor.

The block diagram (Figure 3.6-1) shows representatives of filter modules, similar to the UAR modules, in simplified form. For example: initialization switches in the summing loop are omitted; the approximation to $\sqrt{x^2 + y^2}$ and the cell averaging CFAR are combined as a single block. The cell averaging CFAR is of the same type used in the UAR processor, with the exception that the estimate of the mean noise level is used to normalize the output noise amplitude rather than to set a threshold level.

Since there are six beams and eight filters per beam, a total of 48 filter modules are required. A method of automated switching of the zero doppler filter in response to ground clutter is required prior to the "greatest of" operation; otherwise, output in clutter areas would consist of clutter responses rather than target responses. A clutter map is provided for this function and a second clutter map is applied to the composite filter output to block any residue that may result from processing high level clutter.

Following output of the "greatest of" selector, there are two basic alternatives for configuring the target detection and angle extraction processes. The alternative illustrated in Figure 3.6-1 is based upon complete preservation of amplitude data for a time period corresponding to azimuth scan through one beamwidth. Since there are approximately three batches of eight pulses, storage of two batch outputs is required. In addition to supplying necessary data for amplitude-comparison, angle-estimation algorithms, this storage can also be used for linear noncoherent integration. The second alternative, requiring less memory, employs binary integration in the target detection process. Only amplitude data for signals crossing the first threshold need be stored for use in angle data extraction.

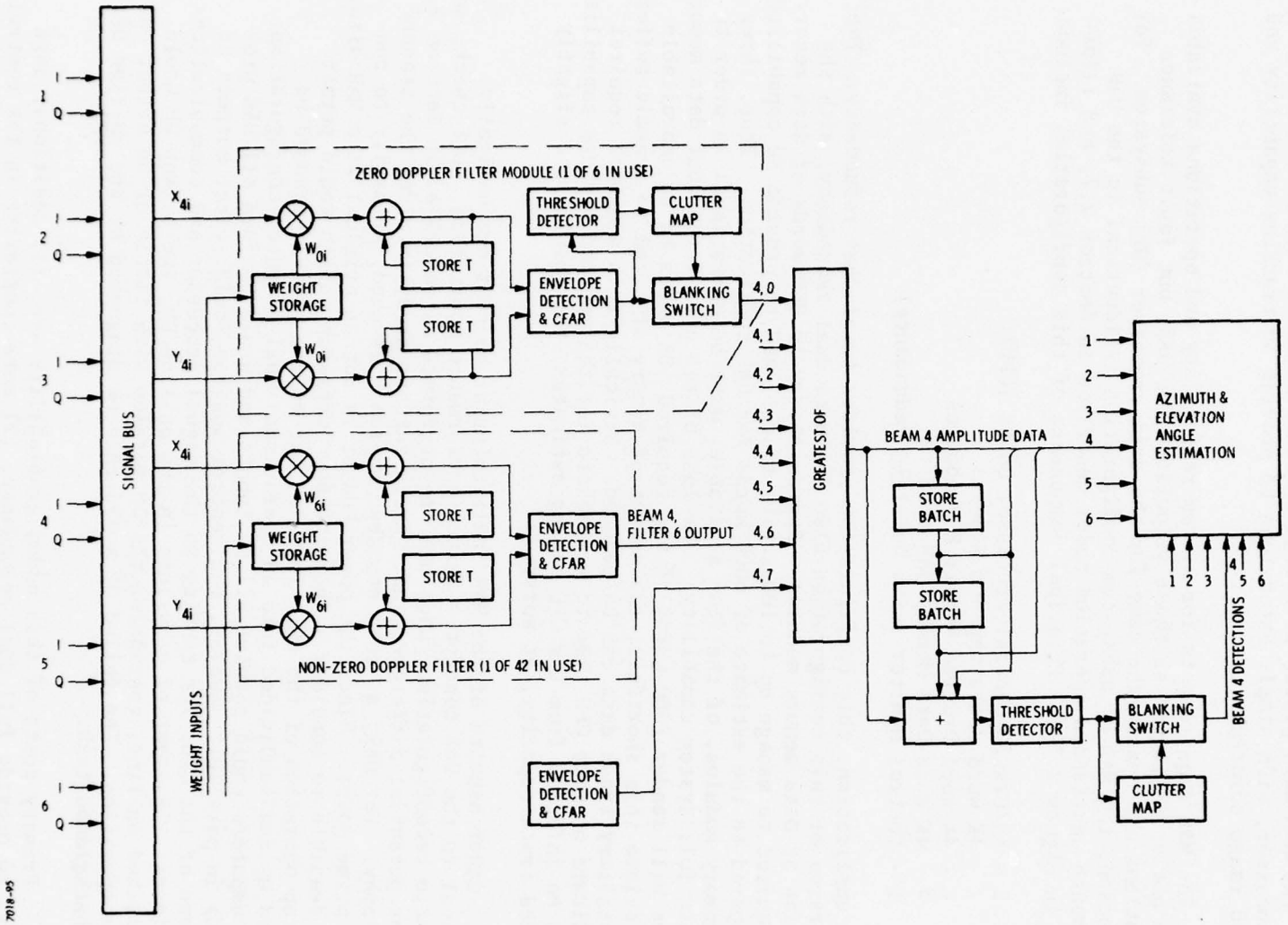


Figure 3.6-1. The MAR Signal Processor Preserves Amplitude Information for the Extraction of 3D Target Coordinates.

3.7 MAR Data Processor Design

The MAR data processor design embodies the same concepts as the UAR data processor, with simple extensions to provide 3D tracking capability and extended range coverage.

The MAR requirements for system reliability and operationa availability are not as stringent as those stipulated for UAR, but fault tolerance implications are nearly the same for the data processor (DP) subsystem. For this reason, the MAR DP subsystem configuration is identical to the UAR three-month unattended operation model described in Section 2.7, and illustrated in Figure 2.7-2. Principal components of this configuration include:

2 - AN/UYK-30 Central Processor Units (CPU)
2 - 4K word Bootstrap ROM modules
6 - 4K word Program Memory ROM modules
4 - 4K word Data Memory RAM modules
1 - Control Monitor (with built-in redundancy).

In UAR application, this configuration provides total dual redundancy. The MAR version of this configuration also features dual redundancy, with the exception of data memory modules. Approximately 10,000 words of data memory are required to manage up to 100 active tracks, and to provide 3D capability, as compared to the estimate of 6000 words for UAR application. Thus, three data memory modules, of the four available, must be operational in order to maintain full system capability. The loss of two out of the four data memory modules will render 2000 words of the required 10K words to be unavailable. To alleviate this shortfall, the amount of memory allotted to dynamic buffers and auxiliary track data can be reduced. Basically this approach requires expenditure of more CPU time to compensate for the reduced storage capability. As can be inferred from the CPU timing estimates, the result is a slightly degraded track capacity, at worst.

Other aspects of the MAR fault tolerant concept are basically identical to the UAR concept. System performance monitoring, self-check, and automatic reconfiguration functions are performed as described in Section 2.7. The one potential difference that merits further study involves the standby philosophy. For UAR, a "cold standby" approach is used, primarily to conserve prime power. Since the power budget is not as critical at a MAR site, it is feasible to consider a "hot standby" approach, which would permit non-stop operation of the DP. That is, the entire subsystem would be powered up and subdivided into an operational dual computer configuration. Both computers would receive all DP inputs and would perform all MAR processing in parallel; however, the control monitor would select outputs of only one of the CPUs for routing to the signal processor and communications interfaces. In event of a failure in the on-line DP, the backup DP would be switched on-line, continuing the DP mission with little or no effect on system operation. The failed DP would then be diagnosed by the on-line DP, as a background task.

Primary costs of this added availability are, (1) additional data memory, to provide full dual redundancy, (2) more complexity in the control monitor device, and (3) more complexity in the operational program.

The MAR target processing function is a simple extension of that described in Section 2.7 for the UAR 2D application. Should MAR accuracy requirements dictate, the detection amplitude data furnished by the signal processor will be used to provide a maximum likelihood estimate of target position. Although this may result in a slight increase in target report processing time, this can be accommodated easily due to the low CPU utilization factor described later in this section. The smoothing and prediction equations are extended to the z-coordinate for close-in targets, but this is of marginal utility for longer range target tracks. Correlation windows are computed in just two dimensions (x and y), however the z-coordinate is used to determine the final association between a target report and a specific track.

Worst case timing estimates for the MAR target processing function may be obtained by simple extrapolation from the UAR timing estimates presented in Section 2.7.4. The principal factors are:

	MAR	UAR
Frame Time	12 seconds	6 seconds
Active Tracks	100	20
Coordinate System	3D	2D

To make this extrapolation, we assume that the number of false detections due to clutter and noise may increase for the MAR due to increased coverage volume, but certainly far less than the corresponding increase in required track capacity. The increase in processing time, due to use of a 3D coordinate system, is less than 50 percent greater than corresponding 2D processing. The CPU time consumed by target report processing, correlation, and track maintenance functions are assumed to be approximate linear functions of total track capacity for the specified UAR and MAR coverage volumes. Thus, the target processing time estimate for MAR is developed as follows:

Total UAR Target/Track Processing per Scan $\leq$ 48 ms

$\frac{\text{MAR}}{\text{UAR}}$ Detection and Track Capacity Ratio ≤ 5

$\frac{\text{3D}}{\text{2D}}$ Processing Time Ratio ≤ 1.5

$\therefore$ Total MAR Target/Track Processing per Scan $\leq 48 \times 5 \times 1.5$

$= \underline{360 \text{ ms}}$

Average MAR Target/Track Processing $= \frac{360}{12} = 30$ ms/sec

$= 3\%$ CPU utilization

The performance monitor processing time is unchanged from UAR, estimated as 70 ms/sec, or 7 percent of CPU processing capacity. Assuming no more than a fivefold increase in general executive and data manipulation functions, an additional 25 percent CPU utilization may be required for this processing.

$$\therefore \text{Total average MAR CPU Utilization} \leq 3 + 7 + 25$$

$$= 35 \text{ percent}$$

Thus, ample processing capability exists to handle significant fluctuations in detection rate and potential functional growth requirements.

The MAR memory module requirements were listed previously. These were extrapolated from the UAR estimates listed in Table 2.7- , by noting that:

(1) Program memory requirements increase by less than 2000 words to handle the 3D capability. Since the total is still less than 12K words, no additional memory modules are required.

(2) Approximately 4K words of additional data memory are required to handle the 3D capability and additional track capacity, for a total of 10K words. Additional memory modules are not required to meet the MAR operational availability requirements, unless a hot-standby fault-tolerance concept is adopted.

APPENDIX A

RECOMMENDED DEVELOPMENT PROGRAM

FOR

M/N TRANSMITTER

APPENDIX "A"

RECOMMENDED DEVELOPMENT PROGRAM FOR M/N TRANSMITTER

Scope - Develop two critical items on the M/N Transmitter.

1) Develop and test two prototypes of an M/N power combiner. The design goals are shown in Table A-1.

2) Develop and test two prototypes of a bipolar transistor module. The design goals are shown in Table A-2.

Purpose:

1) The successful development of the M/N power combiner will have a direct impact on ultimate performance, reliability and life cycle cost of the UAR transmitter. Total transmitter reliability can be increased by four orders of magnitude and its life cycle cost can be reduced by several orders of magnitude.

   The concept of the M/N transmitter appears fairly straightforward. In practice, however, its physical implementation will require a complex theoretical synthesis and several generations of prototypes. Using available technology, 12 months of development time will be required to insure a deliverable combiner prototype. Since the primary function of the M/N combiner is to increase reliability of the transmitter, a successful completion of the combiner development should be followed by a reliability validation program. All redundant features of the combiner should be thoroughly tested under all environmental conditions such as temperature, humidity, shock, and vibration. Items determined to be inherently unreliable will require redesign and further test.

   At completion of the evaluation programs for both the combiner and transmitter module running in parallel over a period of 12 months, planning for design and development of a complete transmitter will be more exact and realistic in determining performance goals and schedule.

2) The transmitter power output at 2 kW is predicated on the availability of a 120-watt bipolar transistor module. The key item for this module is a 24-cell structure which TRW anticipates developing at the start of 1977. Therefore, a purchase contract will be established with the above vendor as a positive assurance of receiving end items in 1978. After the transistors are delivered, they can be evaluated in a relatively straightforward configuration. A total of 12 months appears reasonable to obtain test results of the 120-watt module.

Present methods of predicting transistor life are based on the equation developed by Black. Validation of its life projection is, however, somewhat limited. In addition to metal life considerations, equally important evaluations should be applied to random failures of the multiple cell transistor. Integrated elements of the transistor, such as the MOS capacitor, ballast resistor and bonding wires, require extensive evaluation. Additional improvements to some of these elements may be necessary to meet the rigorous requirements. As mentioned above, the transistor module reliability evaluation should be conducted concurrently with that of the M/N combiner.

TABLE A-1. M/N POWER COMBINER DESIGN GOALS

Frequency	1215 - 1400 MHz
Input Ports	24
Output Ports	1
Power Handling	2 kW
Insertion Loss	0.4 dB
VSWR	1.5 to 1

TABLE A-2. TRANSISTOR AMPLIFIER DESIGN GOALS

Frequency	1215 - 1400 MHz
Gain	14 dB
Power Output	120 watts peak, 6 watts average
Collector Efficiency	55 percent
Pulsewidth	50 μsec

APPENDIX B

DUAL BAND SEGMENT PLA DEVELOPMENT PROGRAM

APPENDIX B

DUAL BAND SEGMENT PLA DEVELOPMENT PROGRAM

Scope

To develop and test a prototype periodically loaded array (PLA) for use as a line feed for the UAR reflectors. The design goals are indicated in Table B-1.

Purpose

Cost and weight of the frequency scanning line feeds for the UAR antenna will have significant impact on the overall system cost since twelve are required at each site. It is highly desirable to cover the specified ±30 degree angular region in two separate segments of the overall frequency band (see Table B-1). "Serpentine" delay lines are easily capable of performing this function by choosing a design that is one guide wavelength longer at the upper segment. However, "serpentines" require a heavy, bulky structure that are less attractive to use as a feed for a reflector. A more optimum device would consist of a straight waveguide loaded in some manner to obtain a sufficient amount of delay necessary to duplicate characteristics of the larger "serpentine." Recent studies at ITT Gilfillan have been directed toward use of a periodically loaded array (PLA) for frequency scanning. This device consists of normally below-cutoff waveguide that is capacitively loaded to form a propagating line with characteristics similar to that of the "serpentine." Sufficient research has been completed to prove the feasibility and low cost advantages of the PLA; however, dual band segment capability has not been investigated to date.

Thus, it is recommended that additional R&D be directed toward achieving a low cost, dual-band segment PLA for the UAR L-band application. Lower cost, lower profile "serpentine" techniques should also be investigated in this study as a reference as well as techniques which use continuous loading.

It is expected that the resulting optimum approach will achieve a 4:1 cost savings over the standard "serpentine" device, thereby resulting in substantial overall system cost savings. The development program suggested will require 15 months effort, including a three-month study phase.

TABLE B-1. PERIODICALLY LOADED ARRAY DESIGN GOALS

Scan Angle Range	±30 degrees
Frequency Band Segments	1215 to 1300 MHz 1315 to 1400 MHz
Az Beamwidth	2.25 degrees
Sidelobe Level	-30 dB
Dissipative Loss	1.0 dB
Signal Bandwidth	750 kHz
Environmental	As encountered in arctic regions

APPENDIX C

TECHNICAL PROPOSAL

SUBMITTED TO: ITT GILFILLAN

VAN NUYS, CALIFORNIA

NOVEMBER 3, 1976

BY:

TRW SEMICONDUCTORS

AN ELECTRONIC COMPONENTS DIVISION OF TRW INC.

14520 AVIATION BOULEVARD, LAWNDALE, CALIFORNIA 90260

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SECTION I

ANTICIPATED TRANSISTOR PERFORMANCE

RF Performance

The pulsed RF performance of the SB2000 has been examined for other programs.

A six cell transistor provides output powers of 30 watts at greater than 55 percent efficiency when driven with an RF waveshape as shown below.

f (GHz)	P_o (watts)	I_c (amps)	G_p (db)	η_c (%)
1.20	30.5	.93	7.7	58
1.24	31.5	.96	7.9	58
1.28	32.0	.98	7.9	58
1.32	32.0	.98	7.9	58
1.36	31.5	.97	7.9	58
1.40	30.5	.95	7.7	57

V_{cc} = 28.0V P_{in} = 5.14 Watts

A ten cell transistor has been evaluated in the 960MHz to 1200MHz frequency range. The waveshape for this evaluation was 8 micro-second pulses at 40 percent duty cycle.

f (GHz)	P_{in} (watts)	P_o (watts)	I_c (amps)	G_p (db)	η_c (%)
.96	12.6	60	1.49	6.8	48
1.0	10.8	60	1.37	7.4	52
1.05	9.7	60	1.30	7.9	55
1.10	9.6	60	1.29	7.9	55
1.15	9.2	60	1.23	8.1	58
1.21	9.2	60	1.20	8.1	60

V_{cc} = 28.0V

At a 25 percent duty cycle the part could be driven to over 70 watts peak. An optimized shunt inductor would have improved the performance at the low frequencies. From this data it can be determined that 12 cells of the SB2000 will meet the output power, efficiency and gain requirements of the specification. Six cells will meet these requirements for the smaller driver transistor.

At pulse widths greater than about 100 microseconds the thermal temperature rise in the silicon material will stablize at the CW value. Fortunately the thermal time constants of the flange and BeO isolator are much longer (in the order of 5 milliseconds or more). As the thermal impedance of these components is a significant part of the total, some additional output power can be obtained for a given junction temperature.

The distribution of calculated thermal impedances for a 12 cell SB2000 transistor is shown below.

Copper flange	.094	degrees centigrade/watt
BeO	.31	degrees centigrade/watt
Au/Si eutectic	.034	degrees centigrade/watt
Silicon	.692	degrees centigrade/watt
Total	1.13	degrees centigrade/watt

Approximately 36 percent of the thermal resistance has thermal time constants long enough to integrate the peak temperature rise over the entire duty cycle. A one millisecond 16 percent

duty cycle waveshape produces a calculated thermal impedance of .79 degrees centigrade per watt.

Junction temperature requirements will be met because of the efficiency produced by the SB2000 cells. For a peak junction temperature of 140 degrees centigrade, a flange temperature of 30 degrees centigrade allows a 110 degree drop between the two. A part producing 60 watts at 55 percent efficiency with 6 db gain dissipates $\frac{60}{.55} - 60 + 15 = 64.1$ watts. The thermal impedance can be as great as $\frac{110}{64.1} = 1.71$ degrees C/W comparing the required 1.71°C/W to the theoretically calculated 0.79 degrees C/W shows that there is good thermal tolerances for material and manufacturing variations.

The only unanswered question about RF specifications is that of pulse droop. This phenomenon is primarily a function of die temperature. The positive temperature silicon emitter ballast resistors used in the SB2000 dice tend to exaggerate the thermal pulse droop. We believe the 0.2db specification can be achieved with 12 cells of the SB2000.

DC Performance

BV_{CES}

BV_{CES} is primarily a function of the epitaxial layer thickness and resistivity. As the layer is made higher in resistivity or thicker, the collector breakdown voltages are increased

and the saturated output power is decreased. Therefore, the epitaxial thickness and resistivity must be controlled to the tightest practical level to produce a cost effective device. An effective level of control has been exercised on the SB2000 parameter during the entire production history (over 2 years). It is therefore anticipated that a BV_{CES} of 56 volts at 120 milliamperes can be achieved for the large numbers of parts required for this program. Relaxation of this parameter is desirable due to the clamping diodes inherent in the SB2000 die. These diodes are designed to breakdown 5 volts before the transistor junction and completely protect it from avalanche. This is a very cost sensitive parameter.

BV_{EBO}

BV_{EBO} is determined by diffusion profiles. Control of this parameter is important to prevent base-emitter avalanche which degrades device lifetime. A substantial production history has been generated for the SB2000 dice proposed for the parts described by this specification. This history shows that the base-emitter breakdown voltage of 3.5 volts at 1 milliampere can be realized with complete confidence.

SECTION II

PROPERTIES OF THE SB2000 TRANSISTOR CELL

The Transistor Die

The choice of SB2000 for this application is based on several key factors:

1) The emitter periphery/base area ratio is optimum for 1-2 GHz performance.
2) The SB2000 cell is the basic die produced for all TRW Microwave Transistors from .6 to 2.0GHz. It has a successful production history spanning 3 years.
3) The ability to combine cells for high power performance is proven. Each cell is rated at 3 watt CW and 8dB gain at 2GHz. Up to 16 cells have been combined for 50W P_{out} (CW) at 2GHz.
4) The SB2000 features silicon diffused emitter ballasting resistors and collector diodes, providing complete tolerance to mis-match loads for any VSWR, any Phase Angle under it's CW rated condition.
5) The geometry employs a gold metallization system to prevent electromigration difficulties.
6) The reliability of SB2000 is proven. Data & Product analysis from two major full high-rel programs have space-qualified the product. Thermal designs & stable

junctions and gold metallization account for exceeding military and industrial rel requirements.

Description of the basic SB2000 cell:

Cell Size .014" X .025"

Twelve cells is .168" X .025"

Six Cells is .084" X .025"

Emitter Periphery is .232"

Emitter Area is 8.19mil^2

Base Periphery is .039"

Base Area is 42.1mil^2

EP to BA ratio 5.51

Emitter Fingers = 50

Construction - interdigitated

Passivation - Silox glass over entire geometry except bond pads and scribe lines.

Emitter Ballasting - 45 Ω per emitter finger pair; nominally 1.8Ω/Cell, diffused into the silicon collector (patent pending). This feature provides an RF avalanche diode adjusted by geometry and diffusion to breakdown slightly below BV_{CES}. A diode similar to this is diffused on the base side (patent pending).

Metal System - Pt Si - TiW - Au. The final Au layer is 1.5 microns thick. Finger width for base & emitter is .00012". Due to the metal system

used and the proprietary metal definition process the usual step coverage difficulties and finger definition problems have been eliminated.

MTTF - Electromigration - Assuming CW condition of 60 Watts and 30 Watts respectively with 12 cells and 6 cells, V_{CC} = 28V, collector currents for various efficiencies are as follows:

DEVICE	η_c %	I_c (pk)
60 Watt	50	4.29 A
60 Watt	55	3.90 A
60 Watt	60	3.57 A
30 Watt	50	2.14 A
30 Watt	55	1.95 A
30 Watt	60	1.79 A

$$\text{MTTF (hrs)} = \frac{N^2 A^3 e^{\phi/kT}}{I_{e^2} B}$$ Black's Equation

Where for our conditions:

N = number of emitter fingers/cell = 50

A = (.12 mil X 1.5u X 2.54 X 10^{-7}) emitter finger area

B = 1.07 X 10^{-12} metal bulk factor

ϕ = .96 eV activation energy

k = 8.62 x 10^{-5} Boltzmann's constant

T = (273 + t°C) chip temperature

I_e = emitter current/cell (amps)

The curves of Figure 1 predict the life time of each transistor for particular efficiency levels with flange temperature as a variable. Life time predicted for 16% duty cycle and full peak temperature.

Current Density - Assuming dimensions given above and a V_{cc} of 28V, the following current densities will be encountered under various conditions of efficiency with 60 and 30W respectively:

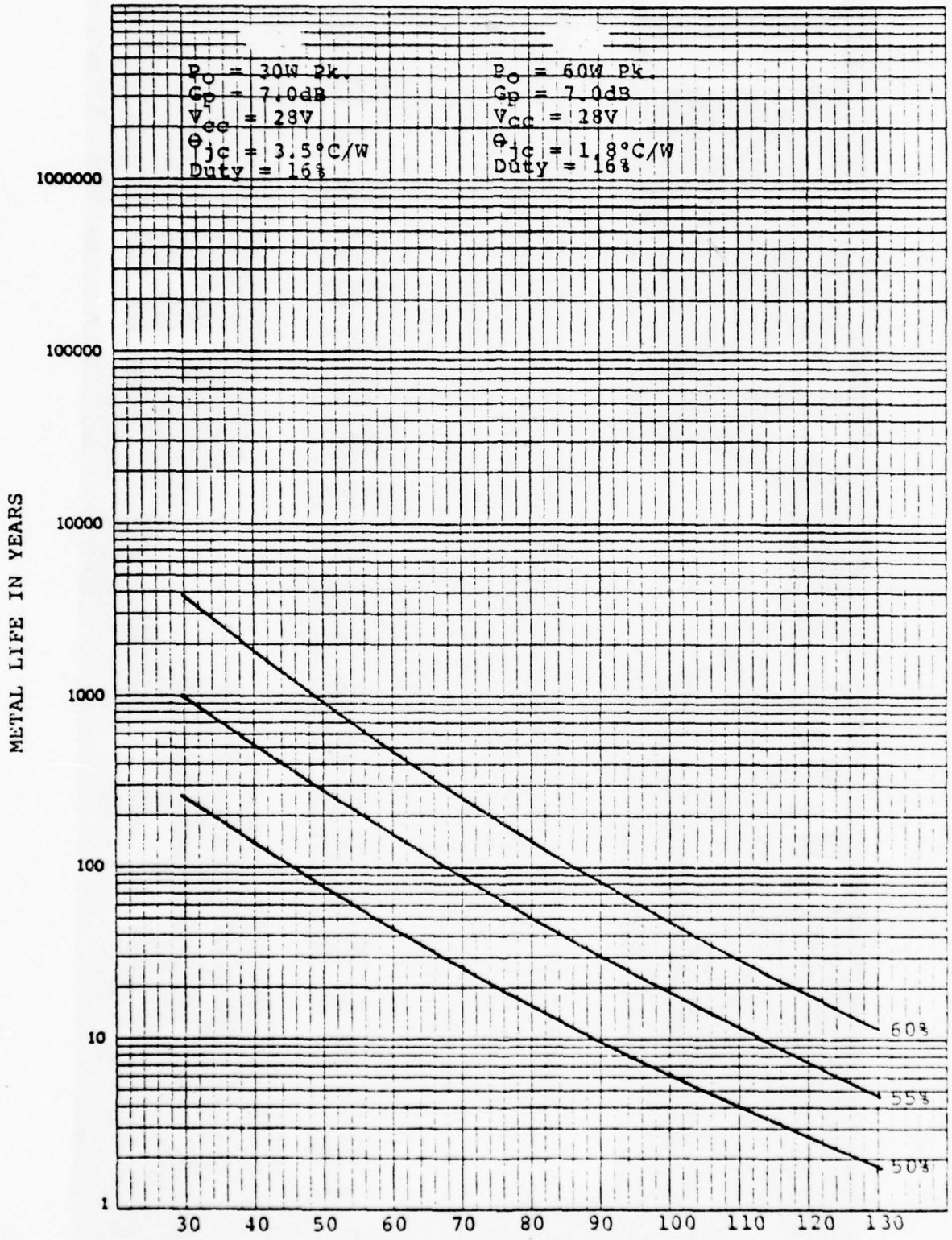
DEVICE	PEAK CURRENT DENSITY	η_c%
60 Watt	1.56×10^5 A/CM^2	50
60 Watt	1.42×10^5 A/CM^2	55
60 Watt	1.30×10^5 A/CM^2	60
30 Watt	1.56×10^5 A/CM^2	50
30 Watt	1.42×10^5 A/CM^2	55
30 Watt	1.30×10^5 A/CM^2	60

This calculation does not pertain to MTTF electromigration since MTTF is actually proportional to conductor area cubed (A^3) and inversely proportional to I_e^2.

Metal Fatigue - Fingers: Weisenberger reported a mechanical phenomenon in which small grain, unpassivated aluminum was noted to be prone to sidewise whisker growth after repeated temperature excursions. Additional work with passivated gold showed no evidence of this phenomena. At last look, 10^9 excursions were recorded without evidence of the spreading phenomena.

MODEL

FIGURE 1



TRW
58
2000

Transistor Design Features

The proposed existing geometry has several unique features developed by TRWS. Specifically they are the use of a diode placed in shunt across the collector emitter for VSWR protection, diffused ballast resistors and a new Au metallization system for increased reliability. A general discussion of the attributes of these techniques is given below.

Ballasting

The use of diffused emitter ballast resistors has several advantages. The tight thermal coupling between the resistors and the active area allows the positive temperature coefficient of the resistors to provide additional ballasting as temperatures increase, as well as providing a low thermal impedance to the heat sink for higher dissipation capability. The diffused resistor also eliminates corrosion as a potential failure mechanism. Figure 2 illustrates another significant advantage of this approach; non-linear current limiting.

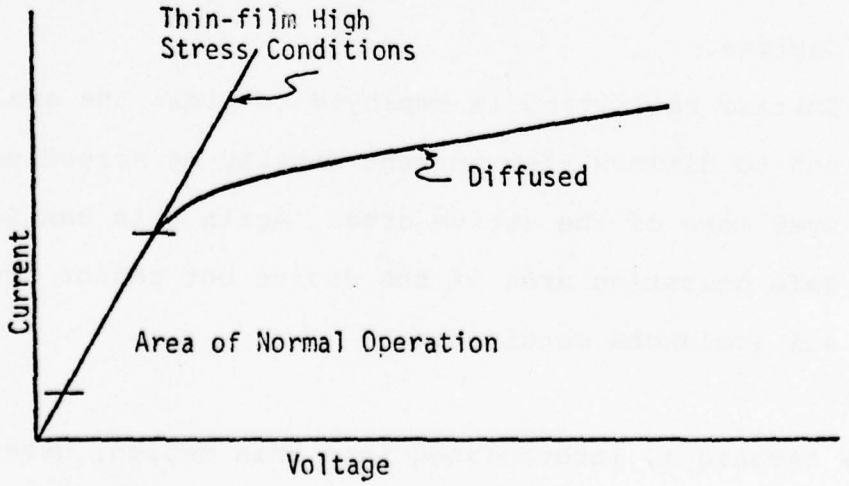


Fig. 2 Current Limiting Characteristics of Ballast Resistors

The effective ballast value that is applied to a highly stressed portion of the device is significantly larger for the diffused resistor, hence, localized hot-spotting is markedly reduced.

VSWR Capability

A major problem encountered with state of the art RF transistors is their susceptibility to catastropic failure when high VSWR conditions are present at the output of the device. High voltages presented to the collector-base junction under infinite VSWR conditions exceed the avalanche breakdown of the device, producing high current densities, intense localized heating, and usually, thermal destruction of the device.

Several techniques are employed to protect devices from this type of failure:

- Collector ballasting is employed to protect the device during avalanche breakdown by limiting the current flow during avalanche breakdown. This technique can produce rugged devices.
- Emitter ballasting is employed to limit the avalanche current and to diminish the current density by spreading the current over more of the active area. Again this can increase the safe operating area of the device but cannot protect against all avalanche conditions.

A new technique, incorporated into this design, uses a diode monolithically placed in shunt across the collector-emitter junction. A schematic is shown in Figure 3. The avalanche

breakdown of the diode is set lower than breakdown of the collector base junction. This is depicted on the graph in Figure 4, now in class "C" common base operation (BV_{CES} condition) when voltage conditions are presented to the output of the device, the diode will avalanche before the collector base junction and all current flow will be through the diode. The diode is able to withstand the large currents which can flow during avalanche breakdown for several reasons.

The high concentration, graded junction used in the P+ diode is less susceptible to non-uniform breakdown than is the abrupt collector base junction in the transistor. Also, the 'clamping' diode is a single junction device and as such does not have an emitter which provides β multiplication of the avalanche current as in an actual transistor. This diode, a simple P+ diffusion, is also that used for the emitter ballast resistors.

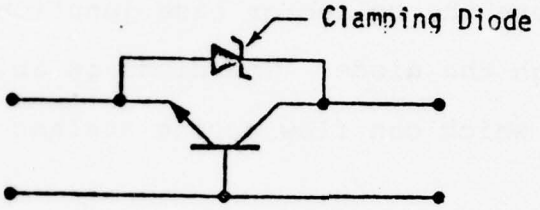


Fig. 3 Schematic of Device with "Clamping Diode" for VSWR Protection.

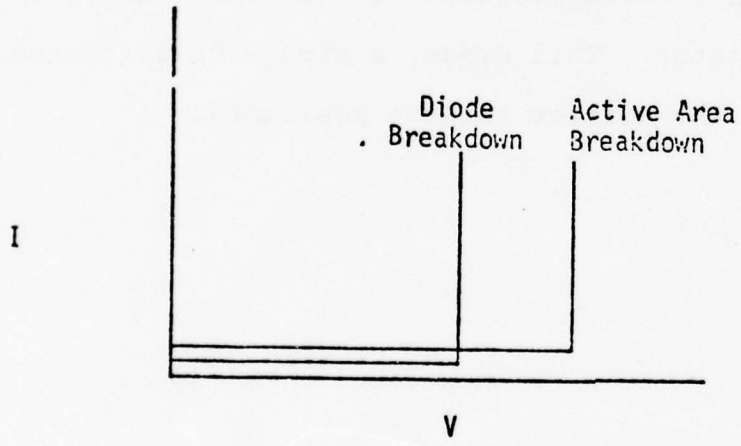


Fig. 4 Breakdown Characteristics of the VSWR Protected Device.

SECTION III

QUALITY CONTROL AND RELIABILITY CONSIDERATIONS

Reliability

The RF Semiconductor Operation at TRW has made a significant investment in reliability tools and funding of study programs affecting RF Transistor Reliability. One of the major reliability study programs performed in the last few years was conducted in the TRW Reliability Physics Lab by Ronald Clarke and Bryan Stallard for Rome Air Development Center. (Contract No. F30602-72-C-0288). The results of this report have been used as a base for our new designs.

In addition to the reliability data produced for the design base, many programs have since used and qualified this product or a close derivative of the design.

o Summary of Reliability Data on SB2000 Design

Program	Type of Test	Summary
RADC Contract	Metal Migration	Good Characterization of Activation Energy etc.
	RF Step Stress	Gold wire bonds - on - gold metal system required for reliable pulse operation.
		Diffused resistors don't crack during pulse operation.
	Hi-Temp Step Stress	Proved stability of metal system.
	Power Cycle Test	Gold wires are fatigue resistant.
CATV Life Test	High Temperature Long Term Life Test on Hybrid Circuits	5,636,000 unit hours with no die related problems.

Program	Type of Test	Summary
GPS	High Rel Space Program	Proved Product Integrity Including HTRB Capability
MAROTS	High Rel Space Program	Proved Product Integrity Including Transient Handling Capability

High Reliability Processing

The RF Operations has made a significant commitment to High Reliability Programs. This commitment includes a High Rel Program Manager.

In addition, the Operation has available among others, the following facilities:

Moisture Resistance Chamber

Vibration Table

Mechanical Shock Equipment

Salt Spray Chamber

HTRB Slots

D.C. Burn-In Racks

X-Ray

Scanning Electron Microscope

Automatic Thermal Shock Chambers

High Temperature Storage Ovens.

Centrifuge

IR Scanners

EDAX dispersive X-Ray

We have included a CATV Reliability Report to show the equipment and controls used for our industrial products. This report also shows photographs of the Quality Control equipment in use.

Also included is a copy of a Technical Paper which discusses Reliability Technology common to microwave.

Quality and Process Control

Quality Control and Assurance of such control is essential in the manufacture of reliable microelectronic hardware. TRW Semiconductors has been a leader in Quality Programs since it was formed over 20 years ago. One of the first large programs was for High Reliability Diodes on the Minuteman Missile Program.

TRW operates an approved MIL-Q-9858 Quality system. Consisting of two tiers of Quality Management.

A. Quality Control Inspection is responsible for the inspection of product and its immediate day to day line control.

B. Quality Assurance is responsible for the technical quality guidance, quality control procedures, quality audits and specification reviews.

C. Vendor control is maintained by tight surveillance and Quality Receiving Inspections.

D. Control Reports are used to maintain tight line control by fast feedback of information to all concerned people.

QUALITY TEST & CONTROLS

Wafer Form

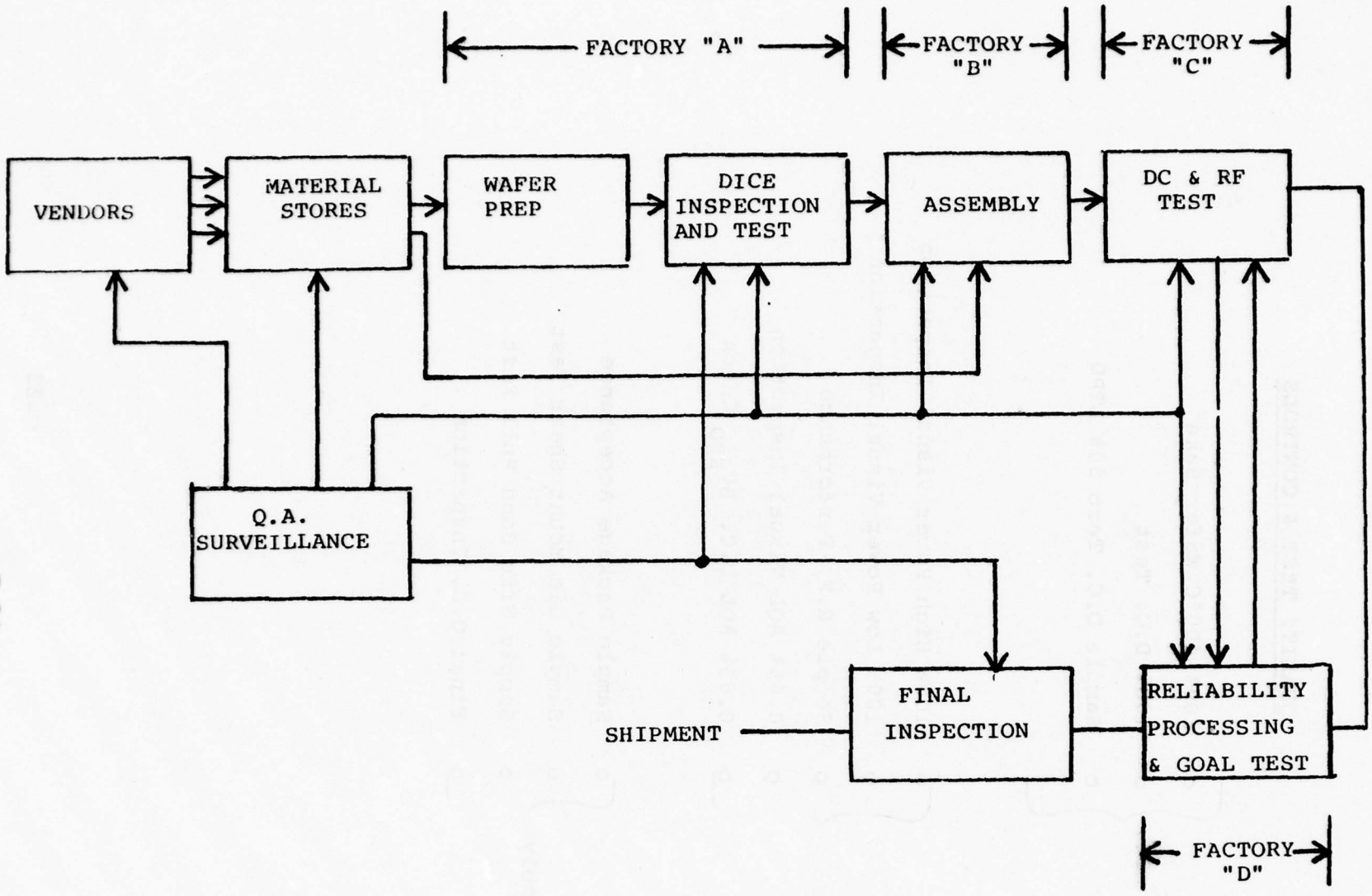
- o 100% 400°C Wafer Bake
- o 100% D.C. Test
- o Sample D.C. Test 50% LTPD

Dice Form

- o 100% High Power Visual Inspection
- o 100% Low Power Visual Inspection
- o Sample R.F. Performance
- o 0.65% AQL Visual Inspection
- o 0.65% AQL D.C. BV_{EBO} Check

Assembly

- o Sample Package Acceptance
- o Sample Die Mount Shear Test
- o Sample Wire Bond Pull Test
- o Final Q.C. Inspection


FACTORY "A"
FACTORY "B"
FACTORY "C"
VENDORS
MATERIAL STORES
WAFER PREP
DICE INSPECTION AND TEST
ASSEMBLY
DC & RF TEST
Q.A. SURVEILLANCE
SHIPMENT
FINAL INSPECTION
RELIABILITY PROCESSING & GOAL TEST
FACTORY "D"

APPENDIX D

CALCULATIONS RELATING TO TRACK INITIATION PERFORMANCE

APPENDIX "D"

CALCULATIONS RELATING TO TRACK INITIATION PERFORMANCE

1. Derivation of Track Initiation Gate Size

The maximum target velocity is specified as 2400 knots. In order to correlate successive detections of a high velocity target, detections must be accepted from an area that encompasses the maximum expected target motion in the time that has elapsed between successive detections. With a six second frame rate, the minimum time between successive detections is 6 seconds, while the maximum time for either the 2/3/4 or the 3/4 criteria is 12 seconds — i.e., a miss on one scan is permitted.

An aircraft on a radial path at 2400 knots traverses 37 range cells in one scan (six seconds). The number of azimuth cells traversed by a crossing target at 2400 knots depends upon the range; for example, at 30 miles a crossing target traverses 3.4 azimuth cells in one scan.

In Figure D-1, the maximum gate size required is shown for two positions of the target at first detection. This maximum gate size could occur after expansion, following a missed detection in the scan, and allows for 2400-knot velocity in any direction. These gate sizes tend to be significantly larger than the average size required for these positions because gate size for the first scan after the initial detection need be only about one-fourth of the area shown: moreover, when the operational function of the radar system is considered, it seems reasonable to expect a reduced maximum velocity vector in some directions. In Figure D-2, reduced gate dimensions are shown as a result of the stated assumption.

A gate size of 740 cells was selected as a conservative estimate of the average gate size.

2. Calculation of the Rate of False Track Initiations Due to Clutter Residue

The doppler filter system (MTI) is designed to provide for detection of targets over clutter at a level corresponding to ≥84 percentile of clutter. A set of clutter maps is provided to eliminate the residue from filters resulting from high level clutter. The maps will eliminate all residue that recurs in a given cell with a high probability from scan-to-scan. The residue that is not eliminated by the mapping operation is that which is highly intermittent from scan-to-scan, i.e., that which has a low probability of recurrence.

An estimate has been made that an average number of clutter points should not exceed four per scan. Furthermore, with the clutter maps designed to censor clutter with a probability of occurrence — greater than approximately 0.05 — it is assumed that for each clutter detection appearing during a scan, the probability of that particular point recurring on any subsequent scan is 0.06.

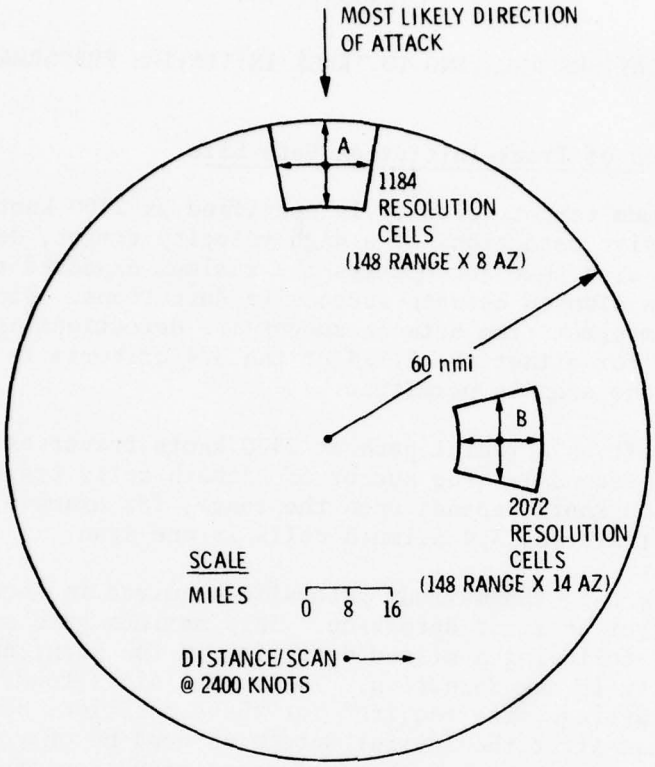


Figure D-1. The Gate Size Required to Accommodate Target Motion in Two Scans is illustrated for two initial detection target motions - assuming target velocity of 2400 knots in any direction.

In the 2/3/4 process proposed for establishing a tentative track, any clutter point appearing on one azimuth scan has the approximate probability of appearing on at least one of the next two scans of 2ρ or $2 \times 0.06 = 0.12$. At the output of the 2/3/4 tentative track criteria, the average rate of false track initiations per scan is approximately $4 \times 0.12 = 0.48$.

In the verification procedure, the same probability of clutter recurrence (i.e., 0.06) is used. In the verification procedure using the three-out-of-five criterion, the probability of verifying clutter is obtained from

$$P_{vc} = \sum_{k=3}^{5} \binom{5}{k} \rho_c^{\,k} (1-\rho_c)^{1-k}$$

where

ρ_c = probability of clutter report = 0.06

P_{vc} = probability of clutter verification.

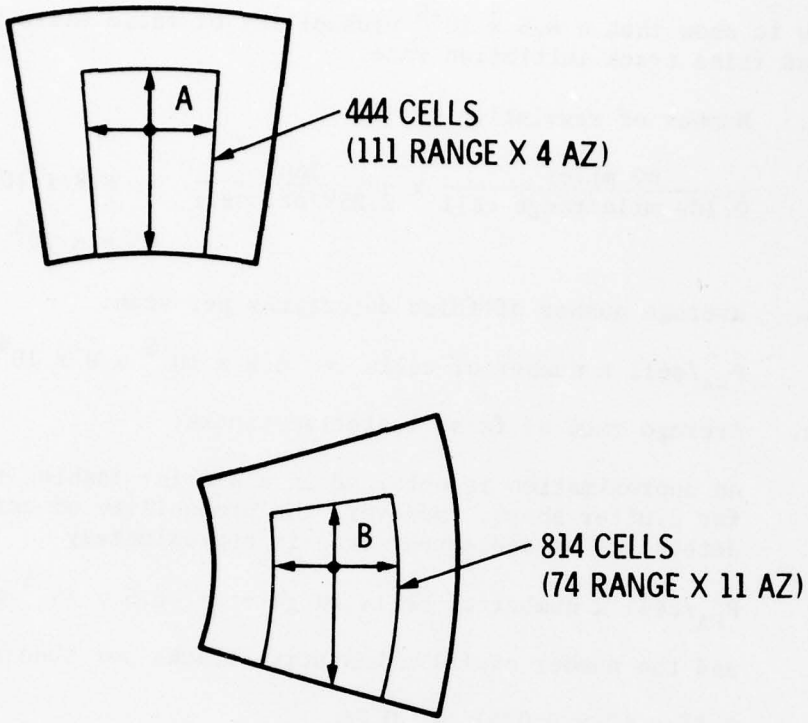


Figure D-2. The Reduction of Gate Size for Both Cases of Figure D-1 is illustrated for an assumption that components of the velocity vector orthogonal and opposite to the most likely direction of attack are 1200 knots (i.e. 1/2 of of the value along the most likely direction).

But since $\rho_c < 1$ a close approximation is obtained

$$P_{vc} \approx \binom{5}{3} \rho_c^3 \simeq 10\, \rho_c^3$$

$$= 0.002.$$

The average rate of false track initiations is then obtained by considering the two processes in sequence obtaining

0.48 per scan x 0.002 = 0.00094 per scan.

Since there is approximately 600 scans per hour, the rate is 0.00094 x 600 = 0.56 false track initiations per hour.

3. Calculation of the Rate of False Track Initiations Due to Noise False Alarms

Although the original computation procedure was based upon derivation of the probability of false alarm to satisfy the requirement of 0.4 false track initiations per hour resulting from noise, the reverse procedure is

elow to show that a 6.5×10^{-5} probability of false alarm per cell yields sired false track initiation rate.

a. Number of resolution cells:

$$\frac{60 \text{ miles}}{0.109 \text{ mile/range cell}} \times \frac{360^{o}}{2.25^{o}/\text{az. cell}} = 8.8 \times 10^{4}$$

$$\approx 9 \times 10^{4} \text{ resolution cells}$$

b. Average number of false detections per scan:

P_{FA}/cell x number of cells $= 6.5 \times 10^{-5} \times 9 \times 10^{4} = 5.85$

c. Average rate of false tentative tracks:

An approximation is obtained in a similar fashion to that used for clutter above. However, the probability of correlating noise detections on subsequent scan is approximately

P_{FA}/cell x number of cells in gate $= 6.5 \times 10^{-5} \times 740 = 0.048$

and the number of false tentative tracks per scan is approximately

$5.85 \times (2 \times 0.048) = 0.56$

d. Average rate of false track following verification:

Using 0.048 as the probability of false detection within a gate and using the same form for noise verification as for clutter stated above, the average number of false track initiations per clutter is

$$P_{VN} = 10\ \rho_n^{3} = 10\ (0.048)^{3} = 0.0011$$

P_{VN} x false tentative track/scan $= 0.0011 \times 0.56$

$$= 0.0062$$

and the false track initiation rate is

$0.0062 \times 600 = 0.37$ per hour.

4. Calculation of Probabilities of Establishing Tentative Track and of Verification

Let

ρ = probability of detection in a single scan

$P_{TT(2/3/4)}$ = probability of tentative track following the sliding 2/3/4 process

We obtain from methods given by Hammers*

$$P_{TT(2/3/4)} = 1 - S_4 = q[q(1-\rho^2)+\rho q^2] + \rho q^2$$

where

$q = 1 - \rho$

S_4 = probability of no detection by the time of the 4th trial

The verification procedure involves use of a fixed m/n gate and, therefore, the probability of verification can be determined from:

$$P_{v(3/5)} = \sum_{k=3}^{5} \binom{5}{k} \rho^k q^{5-k}$$

Calculation using these two equations are shown in Figure D-3.

*Hammers, D.E., Techniques for Automatic Target Detection in Scanning 3D Radar, Advisory Group for Aerospace Research & Devel. for NATO, Symposium on New Devices, Techniques, & Systems in Radar, The Hague, Netherlands, June 76.

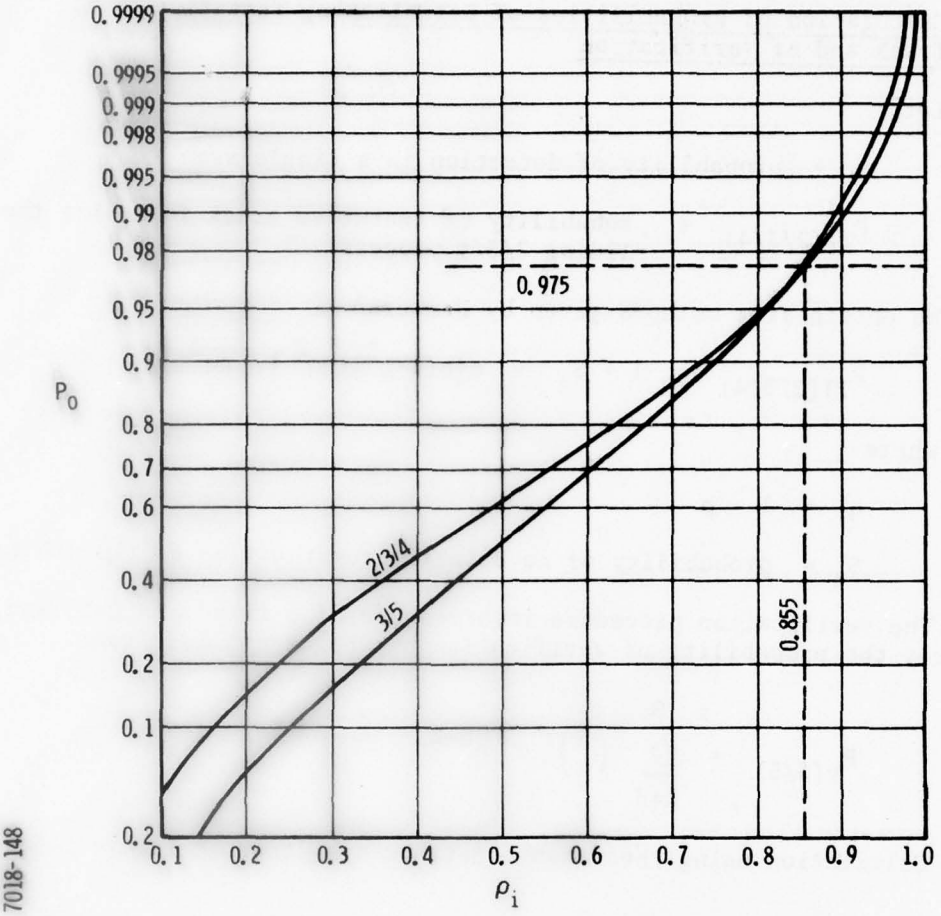


Figure D-3. The probability of the successful output of the two processes (P_o) is plotted as a function of the probability of detection at the input to the two processes ρ_i.

APPENDIX E

FAILURE RATE CALCULATIONS UAR SUBASSEMBLIES

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT: UAR		ASSEMBLY NAME: ANTENNA LESS SW & DRIVER	
GROUP NAME: ANTENNA		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10^6 HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^6 HRS	EXT FR
TRANSISTORS	Silicon		⊥	⊥	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film		⊥	⊥
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
					FIXED CAPACITORS	Tantalum		⊥	⊥
MICROCIRCUITS	SSI		⊥	⊥		Electroly		⊥	⊥
	MSI		⊥	⊥		Other	12	.092	1.104
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF	13	21.760	282.880
	1-Gun CRT		⊥	⊥		≤ 25 Pin		⊥	⊥
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥	DIPLEXERS		12	.100	1.200
	SCIPPER TIRE	12	.100	1.200				⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE: 1/10/77	PREPARED BY	ASSY MTBF: 3491 K HRS	ASSY FAILURE RATE: 286.384 f/10^6 Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT UAR		ASSEMBLY NAME SP13T [illegible]	
GROUP NAME Antenna		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	F/10⁶ HRS	EXT FR	COMPONENTS	TYPE	QTY	F/10⁶ HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film			
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum			
MICROCIRCUITS	SSI					Electroly			
	MSI					Other			
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF	1H	21,760	304,640
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin			
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads	13	[illegible]	431,640	CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer				Pin Diode Switch D		13		273
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE 11/2.71	PREPARED BY	ASSY MTBF 1357 K HRS	ASSY FAILURE RATE 736,513 F/10⁶ HRS

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026 | ITEM(117FORM): | ASSEMBLY NO:

EQUIPMENT: UAR | ASSEMBLY NAME: OAE F 13 SWITCH DRIVER AMPLIFIER

GROUP NAME: ANTENNA | NEXT ASSEMBLY:

COMPONENTS	TYPE	QTY	F/10⁶ HRS	EXT FR	COMPONENTS	TYPE	QTY	F/10⁶ HRS	EXT FR
TRANSISTORS	Silicon	2	6.197	12.394	FIXED RESISTORS	Compos	8	.214	1.712
	Germanium					Film			
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer	4	1.260	5.040	VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum	1	.036	.036
MICROCIRCUITS	SSI-Dig	1	17.262	17.262		Electroly			
	MSI					Other			
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF	1	11.152	11.152
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin			
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer								
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE: 1/13/77 | PREPARED BY: | ASSY MTBF: 20795 K HRS | ASSY FAILURE RATE: 47.676 ×10⁻⁶ / HRS

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026 | ITEM(117FORM): | ASSEMBLY NO:

EQUIPMENT: UAR | ASSEMBLY NAME: M/N WAY SPLITTER

GROUP NAME: TRANSMITTER | NEXT ASSEMBLY:

COMPONENTS	TYPE	QTY	λ / 10^{-6} HRS	EXT FR	COMPONENTS	TYPE	QTY	λ / 10^{-6} HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film	30	.214	6.420
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum			
MICROCIRCUITS	SSI					Electroly			
	MSI					Other			
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF			
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin			
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer								
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE: 12/14/77 | PREPARED BY: | ASSY MTBF: 155,716 HRS | ASSY FAILURE RATE: 6.420

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026	ITEM(117FORM):	ASSEMBLY NO:
EQUIPMENT: UAR	ASSEMBLY NAME: PRE AMPLIFIER (ONE CHANNEL)	
GROUP NAME: TRANSMITTER, RADAR GIFF	NEXT ASSEMBLY:	

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film			
	SCR					Film Pwr			
	RF L Band	2	270.000	540.000		Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum	2	.086	.172
MICROCIRCUITS	SSI					Electroly			
	MSI					Other			
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke	6	8.904	53.424
ELECTRON TUBES	Receiver				CONNECTORS	RF			
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin			
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer				PIN DIODE SW (REDUN)		4	.021	.084
					RF DIODE		2	67.500	135.000
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE: 12/14/77	PREPARED BY:	ASSY MTBF: 13721K Hrs	ASSY FAILURE RATE: 728 FR's f/10⁹ Hr.

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT: UAR		ASSEMBLY NAME: DRIVER OR FINAL AMPLIFIER	
GROUP NAME: TRANSMITTER		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon RF L BAND	1	270.000	270.000	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film		⊥	⊥
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
					FIXED CAPACITORS	Tantalum	1	.086	.086
MICROCIRCUITS	SSI		⊥	⊥		Electroly		⊥	⊥
	MSI		⊥	⊥		Other		⊥	⊥
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke	3	8.904	26.712
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF	2	21.760	43.520
	1-Gun CRT		⊥	⊥		≤ 25 Pin	1	11.152	11.152
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE: 12/14/27	PREPARED BY	ASSY MTBF: 2845 K HRS	ASSY FAILURE RATE: 351,470 f/10⁹ HRS

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026 | ITEM(117FORM) | ASSEMBLY NO

EQUIPMENT UAR | ASSEMBLY NAME M/N WAY COMBINER

GROUP NAME TRANSMITTER | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon		⊥	⊥	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film	30	214	6420
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
					FIXED CAPACITORS	Tantalum		⊥	⊥
MICROCIRCUITS	SSI DIG	15	17.262	258.930		Electroly		⊥	⊥
	MSI		⊥	⊥		Other		⊥	⊥
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Ln Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin		⊥	⊥
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)				
	Duplexer		⊥	⊥	PIN DIODE SW (REDUND)		58	221	1218
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE 12/1/76 | PREPARED BY | ASSY MTBF 3751 K Hrs | ASSY FAILURE RATE 266,568 f/10⁹ Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026 | ITEM(117FORM) | ASSEMBLY NO

EQUIPMENT UAR | ASSEMBLY NAME CABLING

GROUP NAME TRANSMITTER | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	$f/10^9$ HRS	EXT FR	COMPONENTS	TYPE	QTY	$f/10^9$ HRS	EXT FR
TRANSISTORS	Silicon		⊥	⊥	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film		⊥	⊥
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
					FIXED CAPACITORS	Tantalum		⊥	⊥
MICROCIRCUITS	SSI		⊥	⊥		Electroly		⊥	⊥
	MSI		⊥	⊥		Other		⊥	⊥
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF	5	21.760	108.800
	1-Gun CRT		⊥	⊥		≤ 25 Pin	2	11.152	22.304
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron								
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE 12/14/76 | PREPARED BY | ASSY MTBF 7627 K HRS | ASSY FAILURE RATE 131,104 $f/10^9$ HRS

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT UAR		ASSEMBLY NAME M/N WAY COMBINER	
GROUP NAME IFF XMTR		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10^6HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^6HRS	EXT FR
TRANSISTORS	Silicon		⊥	⊥	FIXED RESISTORS	Compos	4	⊥	⊥
	Germanium		⊥	⊥		Film		214	856
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
			⊥	⊥	FIXED CAPACITORS	Tantalum		⊥	⊥
MICROCIRCUITS	SSI/MSI DIG	5	17.262	86.310		Electroly		⊥	⊥
	MSI		⊥	⊥		Other		⊥	⊥
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin		⊥	⊥
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥	PIN DIODE SW (RSDLND)		20	21	42.0
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE 1/10/77	PREPARED BY	ASSY MTBF	ASSY FAILURE RATE 97.58k Hr/1K

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RELIABILITY PREDICTION

JOB 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT UAR		ASSEMBLY NAME M/W WAY SPLITTER	
GROUP NAME IFF XMTR		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10^6 HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^6 HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film	4	.214	.856
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum			
MICROCIRCUITS	SSI					Electroly			
	MSI					Other			
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF			
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin			
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer								
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	ϕ Shifter								

DATE 1/18/77	PREPARED BY	ASSY MTBF	ASSY FAILURE RATE .856 f/10^6 HRS

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RELIABILITY PREDICTION

JOB: 1024 | ITEM(117FORM) | ASSEMBLY NO

EQUIPMENT: UAR | ASSEMBLY NAME: RADAR RECEIVER

GROUP NAME: RECEIVER/EXCITER | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10⁶ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁶ HRS	EXT FR
TRANSISTORS	Silicon	18	6.197	111.546	FIXED RESISTORS	Compos			
	~~Germanium~~ RF	4	27.006	108.000		Film	93	.214	19.902
	SCR					Film Pwr			
	RF L-Band	2	270.000	540.000		Wire Wnd			
DIODES	Computer	33	1.260	41.580	VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum	10	.086	.860
MICROCIRCUITS	SSI/MSI LIN	2	24.205	48.410		Electroly			
	MSI					Other	46	.092	4.232
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other	8	9.200	73.600
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke	29	8.904	258.216
	RF	6	8.904	53.424					
ELECTRON TUBES	Receiver				CONNECTORS	RF	4	21.760	87.040
	1-Gun CRT					≤ 25 Pin	2	11.152	22.304
	3-Gun CRT					> 25 Pin			
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector	3	390.000	1170.000	DC MOTORS	≤ 6K rpm			
	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
MICROWAVE COMPONENTS	Rotary Jt				OTHER (LIST)				
	Duplexer				PIN DIODE ASSY		4	.021	.084
[illegible]	Isolator	4	50.000	200.000					
	Circulator								
	Modulator								
	[illegible]								

ASSY MTBF: 365,070 Hrs | ASSY FAILURE RATE: 2739.98 × 10⁻⁶ /Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026
EQUIPMENT: UAR
GROUP NAME: RECEIVER/EXCITER
ITEM(117FORM):
ASSEMBLY NO:
ASSEMBLY NAME: SYNTHESIZER
NEXT ASSEMBLY:

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon	30	6.197	185.910	FIXED RESISTORS	Compos			
	Germanium					Film	126	.214	26.964
	SCR					Film Pwr			
	RF	10	27.000	270.000		Wire Wnd			
DIODES	Computer	26	1.260	32.760	VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum	15	.086	1.290
MICROCIRCUITS	SSI/MSI LIN	3	24.205	72.615		Electroly			
	MSI/SSI DIG	13	17.262	224.406		Other	96	.092	8.832
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other	30	9.200	276.000
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke	35	8.904	311.640
	RF	6	8.904	53.424					
ELECTRON TUBES	Receiver				CONNECTORS	RF	8	21.760	174.080
	1-Gun CRT					≤ 25 Pin	2	11.152	22.304
	3-Gun CRT					> 25 Pin			
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer	4	600.000	2400.000		>6K rpm			
	Detector	4	390.000	1560.000	DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer				XSTL		1	22.773	2.277
					VARACTOR		4	67.500	270.000
FERRITE DEVICES	Isolator	11	50.000	550.000					
	Circulator								
	Modulator								
	Ø Shifter								

DATE: 1/17/77
PREPARED BY:
ASSY MTBF: 154,793 Hrs.
ASSY FAILURE RATE: 6460.225 f/10⁹ Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026
EQUIPMENT: UAR
GROUP NAME: RECEIVER/EXCITER
ITEM(117FORM):
ASSEMBLY NO:
ASSEMBLY NAME: RADAR EXCITER
NEXT ASSEMBLY:

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon	8	6.197	49.576	FIXED RESISTORS	Compos		⊥	⊥
	~~Germanium~~ DE	2	27.000	54.000		Film	96	.214	20.544
	SCR		⊥	⊥		Film Pwr		⊥	⊥
	RF L-BAND	4	270.000	1080.000		Wire Wnd		⊥	⊥
DIODES	Computer	34	1.260	42.840	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥				⊥	⊥
					FIXED CAPACITORS	Tantalum	2	.086	.172
MICROCIRCUITS	SSI		⊥	⊥		Electroly		⊥	⊥
	MSI		⊥	⊥		Other	44	.092	4.048
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke	15	8.904	133.560
	RF	8	8.904	71.232					
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF	3	21.760	65.280
	1-Gun CRT		⊥	⊥		≤ 25 Pin	1	11.152	11.152
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥	PIN DIODE SW		1	.021	.021
								⊥	⊥
FERRITE DEVICES	Isolator	3	50.000	150.000				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE: 1/17/77
PREPARED BY:
ASSY MTBF: 594,390 Hrs
ASSY FAILURE RATE: 1682.425 f/10⁹ Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026		ITEM(117FORM):	ASSEMBLY NO:
EQUIPMENT: UAR		ASSEMBLY NAME: IFF RECEIVER	
GROUP NAME: RECEIVER/EXCITER		NEXT ASSEMBLY:	

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon	6	6.197	37.182
	~~Germanium~~ RF	2	27.000	54.000
	SCR			
	RF L-BAND	2	270.000	540.000
DIODES	Computer	8	1.260	10.080
	Rectifier			
	Zener			
MICROCIRCUITS	SSI/MSI/LIN	2	24.205	48.410
	MSI			
	LSI			
TRANSFORMERS	Pwr & Fil			
	Lo Pwr Pls			
	RF	2	8.704	17.408
ELECTRON TUBES	Receiver			
	1-Gun CRT			
	3-Gun CRT			
	Thyratron			
	Klystron			
	Magnetron			
	TWT			
	Amplitron			
	TR-ATR			
MICROWAVE DIODES	Mixer			
	Detector	4	390.000	1560.000
MICROWAVE COMPONENTS	Attenuator			
	Loads			
	Rotary Jt			
	Duplexer			
FERRITE DEVICES	Isolator	1	50.000	50.000
	Circulator			
	Modulator			
	Ø Shifter			

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
FIXED RESISTORS	Compos			
	Film	42	.214	8.988
	Film Pwr			
	Wire Wnd			
VARIABLE RESISTORS	Film			
	Wire Wnd			
FIXED CAPACITORS	Tantalum	4	.086	.344
	Electroly			
	Other	22	.092	2.024
VARIABLE CAPACITORS	Vacuum			
	Other			
INDUCTORS	DC Filter			
	RF & Choke	5	8.904	44.520
CONNECTORS	RF	2	21.760	43.520
	≤ 25 Pin	1	11.152	11.152
	> 25 Pin			
SWITCHING DEVICES	Relay			
	Toggle			
	Rotary			
AC MOTORS	≤ 6K rpm			
	>6K rpm			
DC MOTORS	≤ 6K rpm			
	>6K rpm			
CIRCUIT BREAKERS				
OTHER (LIST)				
PIN DIODE ASSY		4	.021	.084

DATE: 1/17/77	PREPARED BY:	ASSY MTBF: 476,842 Hrs	ASSY FAILURE RATE: 2428.112 f/10⁹ Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026
EQUIPMENT: UAR
GROUP NAME: Receiver/Exciter
ITEM(117FORM):
ASSEMBLY NO:
ASSEMBLY NAME: IFF Exciter
NEXT ASSEMBLY:

COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR
TRANSISTORS	Silicon	6	6,197	37,182	FIXED RESISTORS	Compos		⊥	⊥
	~~Germanium~~ RF	1	27,000	27,000		Film	37	,214	7,918
	SCR		⊥	⊥		Film Pwr		⊥	⊥
	RF L Band	2	270,000	540,000		Wire Wnd		⊥	⊥
DIODES	Computer	14	1,260	17,640	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
					FIXED CAPACITORS	Tantalum	5	,086	,425
MICROCIRCUITS	SSI/MSI A/N	1	24,205	24,205		Electroly		⊥	⊥
	MSI		⊥	⊥		Other	18	,092	1,656
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke	7	8,904	62,328
	RF	2	8,904	17,808					
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin		⊥	⊥
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator	2	50,000	100,000				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE: 1/17/77 | PREPARED BY: | ASSY MTBF: 3376 K Hrs | ASSY FAILURE RATE: 836,162 f/10^9/Hrs

ITT Gilfillon

RELIABILITY PREDICTION

JOB 1026
EQUIPMENT VAR
GROUP NAME RECEIVER/EXCITER
ITEM(117FORM)
ASSEMBLY NO
ASSEMBLY NAME CABLING
NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon		⊥	⊥	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film		⊥	⊥
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
					FIXED CAPACITORS	Tantalum		⊥	⊥
MICROCIRCUITS	SSI		⊥	⊥		Electroly		⊥	⊥
	MSI		⊥	⊥		Other		⊥	⊥
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF	11	31.760	239.360
	1-Gun CRT		⊥	⊥		≤ 25 Pin	7	11.152	76.064
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE 1/7/77 | PREPARED BY | ASSY MTBF 3150 K Hrs | ASSY FAILURE RATE 317,424 f/10⁹ Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026 | ITEM(117FORM) | ASSEMBLY NO

EQUIPMENT UAR | ASSEMBLY NAME IFF TARGET DETECTION UNIT

GROUP NAME SIGNAL PROC | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR
TRANSISTORS	Silicon		⊥	⊥	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film	20	.214	4.280
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
			⊥	⊥	FIXED CAPACITORS	Tantalum	4	.086	.344
MICROCIRCUITS	SSI/MSI DIG	50	17.62	863.100		Electroly		⊥	⊥
	MSI		⊥	⊥		Other	30	.092	2.760
	LSI	2	1065.900	2131.800	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin		⊥	⊥
	3-Gun CRT		⊥	⊥		> 25 Pin	1	340.000	340.006
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE 1/12/72 | PREPARED BY | ASSY MTBF 299,196 Hrs. | ASSY FAILURE RATE 3342.284 f/10^9 Hrs.

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RELIABILITY PREDICTION

JOB 1026 | ITEM(117FORM) | ASSEMBLY NO

EQUIPMENT UAR | ASSEMBLY NAME IFF BUFFER

GROUP NAME SIGNAL PROC | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon		⊥	⊥	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film	30	.214	6.420
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
					FIXED CAPACITORS	Tantalum	4	.086	.344
MICROCIRCUITS	SSI/MSI DIG	36	.17.262	621.432		Electroly		⊥	⊥
	MSI/SSI LIN	14	24.205	338.870		Other	40	.092	3,680
	LSI	2	1065.900	2131.800	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin		⊥	⊥
	3-Gun CRT		⊥	⊥		> 25 Pin	1	340.000	340.000
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE 1/17/77 | PREPARED BY | ASSY MTBF 290,482 Hrs | ASSY FAILURE RATE 3442.576 f/10⁹ Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026 | ITEM(117FORM) | ASSEMBLY NO

EQUIPMENT UAR | ASSEMBLY NAME Jamming Detector

GROUP NAME Signal Proc | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon	18	6.197	111.546	FIXED RESISTORS	Compos			
	Germanium					Film	54	.214	11.556
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer	21	1.260	26.460	VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum	6	.086	.516
MICROCIRCUITS	SSI/MSI DIG	12	17.262	207.144		Electroly			
	MSI/SSI LIN	8	24.205	193.640		Other	38	.092	3.496
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke	6	8.904	53.424
ELECTRON TUBES	Receiver				CONNECTORS	RF	2	21.760	43.520
	1-Gun CRT					≤ 25 Pin	1	11.152	11.152
	3-Gun CRT					> 25 Pin			
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer								
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE 11/1/76 | PREPARED BY | ASSY MTBF 1509 K Hrs | ASSY FAILURE RATE 662.754 f/10⁹ Hrs.

ITT Gilfillon

RELIABILITY PREDICTION

JOB: 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT: UAR		ASSEMBLY NAME: A/D CONVERTER/ENCODER	
GROUP NAME: SIGNAL PROCESSOR		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR
TRANSISTORS	Silicon		⊥	⊥	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film	60	.214	12.840
	SCR		⊥	⊥		Film Pwr		⊥	⊥
			⊥	⊥		Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥				⊥	⊥
			⊥	⊥	FIXED CAPACITORS	Tantalum	20	.086	1.720
MICROCIRCUITS	SSI/MSI DIG	38	17.262	655.956		Electroly		⊥	⊥
	MSI/SSI LINEAR	12	24.205	290.460		Other	60	.092	5.520
	LSI DIG	2	1065.900	2131.800	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin		⊥	⊥
	3-Gun CRT		⊥	⊥		> 25 Pin	1	340.000	340.000
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE: 1/11/77	PREPARED BY	ASSY MTBF: 290,641 Hrs	ASSY FAILURE RATE: 3438.296 f/10^9 HRS

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026 | ITEM(117FORM) | ASSEMBLY NO

EQUIPMENT UAR | ASSEMBLY NAME Control Timing Unit

GROUP NAME Signal Processor | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film	20	214	4,280
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum	4	086	344
MICROCIRCUITS	SSI					Electroly			
	MSI DIG	25	17,262	431,550		Other	30	092	2,760
	LSI DIG	3	1065,900	3197,700	VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF			
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin	1	340,000	340,000
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer								
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE 11/17/77 | PREPARED BY | ASSY MTBF 251,768 Hrs | ASSY FAILURE RATE 3976.634 f/10^9 Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026 | ITEM(117FORM) | ASSEMBLY NO

EQUIPMENT UAR | ASSEMBLY NAME Control Monitor & Proc. Interface

GROUP NAME Signal Proc. | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film	30	.214	6.420
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum	4	.086	.344
MICROCIRCUITS	SSI/MSI DIG	50	17.262	863.100		Electroly			
	MSI					Other	30	.092	2.760
	LSI DIG	4	1065.900	4263.600	VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF			
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin	1	340.000	340.000
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer								
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE 11/17/77 | PREPARED BY | ASSY MTBF 182,607 Hrs | ASSY FAILURE RATE 5476.224 f/10^9 Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026
EQUIPMENT: UAR
GROUP NAME: SIGNAL PROC
ITEM(117FORM):
ASSEMBLY NO:
ASSEMBLY NAME: Com Interface Unit
NEXT ASSEMBLY:

COMPONENTS	TYPE	QTY	F/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	F/10⁹ HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film	30	214	6,420
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum	10	086	860
MICROCIRCUITS	SSI/MSI DTL	70	17,262	1208,340		Electroly			
	MSI/SSI MOS	30	24,205	726,150		Other	60	092	5,520
	LSI	2	1065,900	2131,800	VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF			
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin	1	340,000	340,000
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer								
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE: 1/12/77
PREPARED BY:
ASSY MTBF: 226,290 Hrs
ASSY FAILURE RATE: 4419.098 F/10⁹ Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026	ITEM(117FORM):	ASSEMBLY NO:
EQUIPMENT: UAR	ASSEMBLY NAME: PROCESSOR UNIT (QUAN 8)	
GROUP NAME: SIGNAL PROC.	NEXT ASSEMBLY:	

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film	40	214	8,560
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum	10	086	860
MICROCIRCUITS	SSI/MSI DIE	100	17,262	1726,200		Electroly			
	MSI					Other	60	092	5,520
	LSI	4	1065,900	4263,600	VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF			
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin	1	340,000	340,000
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer								
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	ϕ Shifter								

DATE	PREPARED BY	ASSY MTBF	ASSY FAILURE RATE
11/7/77		157,610 Hrs.	6344.740 f/10⁹ Hrs

AD-A045 543 ITT GILFILLAN VAN NUYS CA F/G 17/9
UNATTENDED/MINIMALLY ATTENDED RADAR STUDY. VOLUME II. RADAR DES--ETC(U)
AUG 77 F30602-76-C-0383
UNCLASSIFIED ITTG-TP-0002/L-7018-VOL-2 RADC-TR-77-270-VOL-2 NL

4 OF 4
ADA045 543

END
DATE FILMED
11-77
DDC

ITT Gilfillon

RELIABILITY PREDICTION

JOB: 1026 | ITEM(117FORM): | ASSEMBLY NO:

EQUIPMENT: VAR | ASSEMBLY NAME: CLUTTER MAP (QUAN 2)

GROUP NAME: SIGNAL PROC | NEXT ASSEMBLY:

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon		⊥	⊥	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film	20	.214	4.280
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
					FIXED CAPACITORS	Tantalum	4	.086	.344
MICROCIRCUITS	SSI/MSI	75	17.262	1294.650		Electroly		⊥	⊥
	MSI		⊥	⊥		Other	30	.092	2.760
	LSI	2	1065.900	2131.800	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin		⊥	⊥
	3-Gun CRT		⊥	⊥		> 25 Pin	1	340.000	340.000
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE: 11/17/77 | PREPARED BY: | ASSY MTBF: 264,982 Hrs | ASSY FAILURE RATE: 3773.634 f/10⁹ Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB	1026
EQUIPMENT	UAR
GROUP NAME	SIGNAL PROC
ITEM(117FORM)	
ASSEMBLY NO	
ASSEMBLY NAME	CORRLATION DETECTOR
NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film	20	.214	4.280
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum	4	.086	.344
MICROCIRCUITS	SSI/MSI	25	17.762	431.550		Electroly			
	MSI					Other	30	.092	2.760
	LSI	2	1065.900	2131.800	VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF			
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin	1	340.000	340.000
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer								
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE	1/12/77	PREPARED BY	
ASSY MTBF	343.555 Hrs.	ASSY FAILURE RATE	2910.237 $\times 10^{-9}$ Hrs

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RELIABILITY PREDICTION

JOB 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT UAR		ASSEMBLY NAME ROM	
GROUP NAME Data Proc		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10⁶ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁶ HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film			
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum			
MICROCIRCUITS	SSI/MSI DLG	112	17.262	1933.344		Electroly			
	MSI					Other	52	.092	4.784
	LSI				VARIABLE CAPACITORS	Vacuum			
	1024B ROM	84	49.830	4185.720		Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF			
	1-Gun CRT					≤ 2			
	3-Gun CRT						1	340	342.720
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer								
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE 1/17/77	PREPARED BY	ASSY MTBF 154,706 Hrs	ASSY FAILURE RATE 6463.94 $\times 10^{-9}$/Hrs

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RELIABILITY PREDICTION

JOB 1026 | ITEM(117FORM) | ASSEMBLY NO

EQUIPMENT UAR | ASSEMBLY NAME RAM

GROUP NAME DATA PROC | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR
TRANSISTORS	Silicon		⊥	⊥	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film		⊥	⊥
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
					FIXED CAPACITORS	Tantalum	6	.086	.516
MICROCIRCUITS	SSI/MSI DIG	62	17.262	1070.244		Electroly		⊥	⊥
	MSI		⊥	⊥		Other	45	.092	4.140
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
	1024B RAM	85	87.350	7424.750		Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin		⊥	⊥
	3-Gun CRT		⊥	⊥		> 25 Pin	1	349.000	340.000
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE 11/7/77 | PREPARED BY | ASSY MTBF 113,126 Hrs. | ASSY FAILURE RATE 8839.650 f/10^9 Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT UAR		ASSEMBLY NAME CPU	
GROUP NAME DATA PROC		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon		⊥	⊥	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film		⊥	⊥
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
					FIXED CAPACITORS	Tantalum		⊥	⊥
MICROCIRCUITS	SSI		⊥	⊥		Electroly		⊥	⊥
	MSI		⊥	⊥		Other		⊥	⊥
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin		⊥	⊥
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥	AN/UYK-30	1	50000.000	50000.000	
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE 11/7/77	PREPARED BY	ASSY MTBF 20,000 Hrs	ASSY FAILURE RATE 50,000 f/10⁹ Hrs

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RELIABILITY PREDICTION

JOB 1026 | ITEM(117FORM) | ASSEMBLY NO

EQUIPMENT UAR | ASSEMBLY NAME Power Supply, Unreg

GROUP NAME Power Supplies | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon	11	6.197	68.167	FIXED RESISTORS	Compos	20	.013	.260
	Germanium		⊥	⊥		Film	34	.214	7.276
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd	2	.548	1.096
DIODES	Computer	8	1.260	10.080	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier	30	5.100	153.000		Wire Wnd		⊥	⊥
	Zener	2	10.725	21.450					
					FIXED CAPACITORS	Tantalum	54	.086	4.644
MICROCIRCUITS	SSI		⊥	⊥		Electroly		⊥	⊥
	MSI		⊥	⊥		Other	28	.072	2.016
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil	4	6.601	26.404	INDUCTORS	DC Filter	3	6.601	19.803
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin	1	11.152	11.152
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE 1/19/77 | PREPARED BY | ASSY MTBF 3073 K HRS. | ASSY FAILURE RATE 325.348 f/10⁹ HRS

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026 | ITEM(117FORM): | ASSEMBLY NO:

EQUIPMENT: UAR | ASSEMBLY NAME: REGULATOR, LV

GROUP NAME: POWER SUPPLIES | NEXT ASSEMBLY:

COMPONENTS	TYPE	QTY	f/10^6HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^6HRS	EXT FR
TRANSISTORS	Silicon	4	6.197	24.788	FIXED RESISTORS	Compos	12	.013	.156
	Germanium		⊥	⊥		Film	6	.214	1.284
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd	4	.548	2.192
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier	2	5.100	10.200		Wire Wnd	1	15.250	15.250
	Zener	1	10.725	10.725					
					FIXED CAPACITORS	Tantalum	2	.086	.172
MICROCIRCUITS	SSI		⊥	⊥		Electroly		⊥	⊥
	MSI		⊥	⊥		Other	4	.092	.368
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
	REGULATOR	1	24.205	24.205		Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Ln Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin	1	11.152	11.152
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron								
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE: 1/12/77 | PREPARED BY: | ASSY MTBF: 995 K HRS | ASSY FAILURE RATE: 100.49 F/10^9 HRS

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1036		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT UAR		ASSEMBLY NAME SP4T TRANSMIT RECEIVE SW 1 OF 2	
GROUP NAME TRANSMITTER - RECEIVER		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10^{6}HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^{6}HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film			
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum			
MICROCIRCUITS	SSI					Electroly			
	MSI					Other			
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF	5	21.760	108.800
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin			
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads	4	33.200	132.800	CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer				PIN Diode SW (REDUND)		4	.021	.084
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE	PREPARED BY	ASSY MTBF	ASSY FAILURE RATE 241.684 f/10^6 HRS

ITT Gilfillon

RELIABILITY PREDICTION

JOB: 1026
EQUIPMENT: VAR
GROUP NAME: VAR SYSTEM
ITEM(117FORM):
ASSEMBLY NO:
ASSEMBLY NAME: CABLING & CONTROL
NEXT ASSEMBLY:

COMPONENTS	TYPE	QTY	f/10⁶HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁶HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film			
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum			
MICROCIRCUITS	SSI					Electroly			
	MSI					Other			
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF	12	21 760	261 120
	1-Gun CRT					≤ 25 Pin	10	11 152	111 520
	3-Gun CRT					> 25 Pin			
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle	12	15 006	120 006
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer								
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE: 11/9/77
PREPARED BY:
ASSY MTBF: 1809 K Hrs
ASSY FAILURE RATE: 552,690 f/10⁶ Hrs

APPENDIX F

MAR SUBASSEMBLY FAILURE RATES

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT MAR		ASSEMBLY NAME Phase Shifter & Driver Ckt	
GROUP NAME ANTENNA		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10⁶ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁶ HRS	EXT FR
TRANSISTORS	Silicon	8	6.197	49.576	FIXED RESISTORS	Compos			
	Germanium					Film	32	.214	6.848
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer	16	1.260	20.160	VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
	PIN	8	20.000	160.000	FIXED CAPACITORS	Tantalum	4	.086	.344
MICROCIRCUITS	SSI DIG	4	17.262	69.048		Electroly			
	MSI					Other			
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF	5	21.760	108.800
	1-Gun CRT					≤ 25 Pin	2	11.152	22.304
	3-Gun CRT					> 25 Pin			
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer								
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE 1/21/77	PREPARED BY	ASSY MTBF 2287 K HRS	ASSY FAILURE RATE 457.090 @ 10^9 HRS

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026		ITEM(117FORM):	ASSEMBLY NO:
EQUIPMENT: MAR		ASSEMBLY NAME: SECTOR STEERING	
GROUP NAME: ANTENNA		NEXT ASSEMBLY:	

COMPONENTS	TYPE	QTY	f/10⁶ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁶ HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos	7	.013	.091
	Germanium					Film	66	.214	14.124
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer	4	1.260	5.040	VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
	LED	2	20.000	40.000	FIXED CAPACITORS	Tantalum	4	.086	.344
MICROCIRCUITS	SSI/MSI	127	17.262	2192.274		Electroly			
	MSI					Other	30	.092	2.760
	LSI				VARIABLE CAPACITORS	Vacuum			
	ROM 4K/4B	2	49.830	99.660		Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF			
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin	1	340.000	340.000
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector	1	390.000	390.000	DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads	3	332.000	996.000	CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer								
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	ϕ Shifter								

DATE: 1/21/77	PREPARED BY:	ASSY MTBF: 245080 HRS	ASSY FAILURE RATE: 4080.273 f/10⁶ HRS

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT MAR		ASSEMBLY NAME ANT CABLING & CONTROL	
GROUP NAME ANTENNA		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film			
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum			
MICROCIRCUITS	SSI					Electroly			
	MSI					Other			
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF	2	21,760	43,520
	1-Gun CRT					≤ 25 Pin	10	11,152	111,520
	3-Gun CRT					> 25 Pin	1	340,000	340,000
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay	5	29,500	147,500
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS		5	95,779	478,895
	Rotary Jt				OTHER (LIST)				
	Duplexer				TEMP SENSOR		1	157,900	157,900
					TRANSDUCER		1	150,000	150,000
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	ϕ Shifter								

DATE 1/21/77	PREPARED BY	ASSY MTBF 1009 K HRS	ASSY FAILURE RATE 990,440 F/10⁹ HRS

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT MAR		ASSEMBLY NAME PEDESTAL	
GROUP NAME ANTENNA		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10⁶ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁶ HRS	EXT FR
TRANSISTORS	Silicon		⊥	⊥	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film		⊥	⊥
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
					FIXED CAPACITORS	Tantalum		⊥	⊥
MICROCIRCUITS	SSI		⊥	⊥		Electroly		⊥	⊥
	MSI		⊥	⊥		Other		⊥	⊥
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other			
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin	8	11,152	69,216
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt	1	100,000	100,000	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥	GEAR BOX, DRIVE	1	630,000	630,000	
					MOTOR	1	240,000	240,000	
FERRITE DEVICES	Isolator		⊥	⊥	GEAR BOX, DTO	1	600,000	600,000	
	Circulator		⊥	⊥	SLIP RINGS	1	5700,000	5700,000	
	Modulator		⊥	⊥	ENCODER		600,000	600,000	
	Ø Shifter		⊥	⊥					

DATE	PREPARED BY	ASSY MTBF	ASSY FAILURE RATE
			0009,216 f/10⁶ HRS

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026 | ITEM(117FORM): | ASSEMBLY NO:
EQUIPMENT: MAR | ASSEMBLY NAME:
GROUP NAME: TRANSMITTER | NEXT ASSEMBLY:

COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR
TRANSISTORS	Silicon	108	6.197	669.276	FIXED RESISTORS	Compos	451	.013	5.863
	Germanium		—	—		Film	436	.214	93.304
	SCR	42	5.500	231.000		Film Pwr	28	332.000	9296.000
	RF L-Band	8	270.000	2160.000		Wire Wnd	32	.548	17.536
DIODES	Computer	139	1.260	175.140	VARIABLE RESISTORS	Film	20	49.234	984.680
	Rectifier	1733	5.100	8838.300		Wire Wnd	3	1.525	4.575
	Zener	116	10.725	1244.100					
	PIN 50% DC	104	10.000	1040.000	FIXED CAPACITORS	Tantalum	103	.086	8.858
MICROCIRCUITS	SSI/MSI DIG	99	17.262	1708.938		Electroly	37	41.000	1517.000
	MSI/SSI LIN	93	24.205	2251.065		Other	198	.092	18.216
	~~ROM 256B~~ ROM 256B	4	16.560	66.240	VARIABLE CAPACITORS	Vacuum		—	—
	RAM 1024B	8	87.350	698.800		Other		—	—
TRANSFORMERS	Pwr & Fil	15	6.601	99.015	INDUCTORS	DC Filter	6	6.601	39.606
	Lo Pwr Pls	30	1.781	53.430		RF & Choke	6	8.904	53.424
ELECTRON TUBES	Receiver		—	—	CONNECTORS	RF	16	21.760	348.160
	1-Gun CRT		—	—		≤ 25 Pin	33	11.152	368.016
	3-Gun CRT		—	—		> 25 Pin	1	340.000	340.000
	Thyratron		—	—					
	Klystron		—	—	SWITCHING DEVICES	Relay	4	29.500	118.000
	Magnetron		—	—		Toggle		—	—
	TWT	1	30000.000	30000.000		Rotary	7	42.000	294.000
	Amplitron		—	—		Special	5	43.000	215.000
	TR-ATR		—	—	AC MOTORS	≤ 6K rpm	1	290.000	290.000
MICROWAVE DIODES	Mixer		—	—		>6K rpm	3	5120.000	15360.000
	Detector		—	—	DC MOTORS	≤ 6K rpm		—	—
MICROWAVE COMPONENTS	Attenuator		—	—		>6K rpm		—	—
	Loads	4	332.000	1328.000	CIRCUIT BREAKERS		11	95.779	1053.569
	Rotary Jt		—	—	OTHER (LIST)			—	—
	Duplexer		—	—	XSTL		1	20.000	20.000
					PUMP		1	1290.000	1290.000
FERRITE DEVICES	Isolator		—	—	NUMERIC DIG DISPLAY		4	121.100	484.400
	Circulator	1	4009.000	4009.000	SPARK GAPS		4	3680.000	14720.000
	Modulator		—	—	THERMISTORS		11	100	1100.000
	Ø Shifter								

DATE: 1/20/77 | PREPARED BY: | ASSY MTBF: 9745 HRS | ASSY FAILURE RATE: 102,612.511 f/10^9 HRS

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026 | ITEM(117FORM): | ASSEMBLY NO:
EQUIPMENT: MAR | ASSEMBLY NAME: RECEIVER/EXCITER
GROUP NAME: | NEXT ASSEMBLY:

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon	216	6,197	1338,552	FIXED RESISTORS	Compos		⊥	⊥
	~~Germanium~~ RF	48	27,000	1296,000		Film	1440	,214	308,160
	SCR		⊥	⊥		Film Pwr		⊥	⊥
	RF L-Band	36	270.000	9720.000		Wire Wnd		⊥	⊥
DIODES	Computer	450	1,260	567,000	VARIABLE RESISTORS	Film	22	49,234	1083,148
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener	14	10,725	150,150				⊥	⊥
	PIN	54	20,000	1080.000	FIXED CAPACITORS	Tantalum	102	,086	8,772
MICROCIRCUITS	SSI/MSI LIN	18	24,205	435,690		Electroly		⊥	⊥
	MSI		⊥	⊥		Other	936	,092	86,112
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other	148	9,200	441,600
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke	324	8,304	2684,696
	RF	96	8.904	854.784					
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF	32	21,760	696,320
	1-Gun CRT		⊥	⊥		≤ 25 Pin	4	11,152	44,608
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector	18	390,000	7020,000	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator	8	50,000	400,000				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Φ Shifter		⊥	⊥				⊥	⊥

DATE: 1/21/77 | PREPARED BY: | ASSY MTBF: 35,191 Hrs | ASSY FAILURE RATE: 28,415.792 f/10⁹ Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT MAR		ASSEMBLY NAME SYNTESIZER	
GROUP NAME		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	$f/10^9$ HRS	EXT FR	COMPONENTS	TYPE	QTY	$f/10^9$ HRS	EXT FR
TRANSISTORS	Silicon	180	6,197	1115,460	FIXED RESISTORS	Compos			
	Germanium					Film	756	.214	161,784
	SCR					Film Pwr			
	RF	60	27.000	1620,000		Wire Wnd			
DIODES	Computer	156	1,260	196,560	VARIABLE RESISTORS	Film	12	49,234	590,808
	Rectifier					Wire Wnd			
	Zener	12	10,725	128,700					
					FIXED CAPACITORS	Tantalum	90	.086	7,740
MICROCIRCUITS	SSI/MSI DIE	78	17,262	1346,436		Electroly			
	MSI/SSI PKG	18	24,205	435,690		Other	576	.092	52,992
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other	180	9,200	1656,000
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke	210	8,904	1869,840
	RF	36	8.904	320.544					
ELECTRON TUBES	Receiver				CONNECTORS	RF	48	21,760	1044,480
	1-Gun CRT					≤ 25 Pin	4	11,152	44,608
	3-Gun CRT					> 25 Pin			
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer	8	600,000	4800,000		>6K rpm			
	Detector	8	390,000	3120,000	DC MOTORS	≤ 6K rpm			
						>6K rpm			
MICROWAVE COMPONENTS	Attenuator				CIRCUIT BREAKERS				
	Loads				OTHER (LIST)				
	Rotary Jt								
	Duplexer				XSTL		6	20,000	120,000
					VARACTOR		24	67,500	1620,000
FERRITE DEVICES	Isolator	22	50,000	1110,000					
	Circulator								
	Modulator								
	Ø Shifter								

DATE 1/21/77	PREPARED BY	ASSY MTBF 46,812 HRS	ASSY FAILURE RATE 21,361.64 $f/10^9$ HRS

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026 | ITEM(117FORM): | ASSEMBLY NO:

EQUIPMENT: MAR | ASSEMBLY NAME: RADAR DIGITAL PROCESSOR

GROUP NAME: | NEXT ASSEMBLY:

COMPONENTS	TYPE	QTY	f/10^6 HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^6 HRS	EXT FR
TRANSISTORS	Silicon	5	6.197	30.985	FIXED RESISTORS	Compos	159	.013	2.067
	Germanium					Film	323	.214	69.122
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer	37	1.260	46.620	VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum	459	.086	39.474
MICROCIRCUITS	SSI/MSI DTL	6385	17.262	110,217.870		Electroly			
	MSI/MSI LSN	300	24.205	7261.500		Other	2750	.092	271.400
	~~4081~~ RAM USED	120	27.980	3357.600	VARIABLE CAPACITORS	Vacuum			
	RAM 1024B	1626	87.350	142,031.100		Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF			
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin	61	340.000	20,740.000
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle	59	15.000	885.000
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt				OTHER (LIST)				
	Duplexer				XSTL		1	20.000	20.000
					ROM 256B		252	16.560	4173.120
FERRITE DEVICES	Isolator				ROM 1024B		252	49.820	12,557.640
	Circulator								
	Modulator								
	Ø Shifter								

DATE 1/2/177 | PREPARED BY | ASSY MTBF 3314 Hrs | ASSY FAILURE RATE 301,703.018 f/10^6 Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT: MAR		ASSEMBLY NAME: A/D CONVERTER	
GROUP NAME		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR
TRANSISTORS	Silicon	48	6,197	297,456	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film	496	,214	106,144
	SCR		⊥	⊥		Film Pwr		⊥	⊥
	FET	32	4,830	154,560		Wire Wnd		⊥	⊥
DIODES	Computer	16	1,260	20,160	VARIABLE RESISTORS	Film	16	49,234	787,744
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener	20	10,725	214,500					
					FIXED CAPACITORS	Tantalum	32	,086	2,752
MICROCIRCUITS	SSI/MSI B/G	120	17,262	2071,440		Electroly		⊥	⊥
	MSI/SSI L/H	36	24,205	871,380		Other	152	,092	13,984
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin		⊥	⊥
	3-Gun CRT		⊥	⊥		> 25 Pin	2	340,000	680,000
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE: 1/21/77	PREPARED BY	ASSY MTBF: 19,566 Hrs	ASSY FAILURE RATE: 5220,120 f/10^9 HRS

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RELIABILITY PREDICTION

JOB 1026 | ITEM(117FORM) | ASSEMBLY NO

EQUIPMENT MAR | ASSEMBLY NAME RF HEAD

GROUP NAME | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon	91	6,197	563,927	FIXED RESISTORS	Compos	130	.013	1,690
	~~Germanium~~ RF L-BAND	42	270,000	11340,000		Film	376	.214	80,464
	SCR	3	5,500	16,500		Film Pwr		—	—
	FET	24	4,830	115,920		Wire Wnd		—	—
DIODES	Computer	98	1,260	123,480	VARIABLE RESISTORS	Film	9	49,234	443,106
	Rectifier	8	5,100	40,800		Wire Wnd		—	—
	Zener	6	10,725	64,350					
	PIN	120	20,000	2400,000	FIXED CAPACITORS	Tantalum	38	.086	3,268
MICROCIRCUITS	SSI/MSI DIG	38	17,262	655,956		Electroly		—	—
	MSI/SSI LIN	9	24,205	217,845		Other	489	.092	44,988
	LSI		—	—	VARIABLE CAPACITORS	Vacuum	4	3,750	15,000
						Other	6	9,200	55,200
TRANSFORMERS	Pwr & Fil		—	—	INDUCTORS	DC Filter		—	—
	Lo Pwr Pls	2	1,781	3,562		RF & Choke	58	8,904	516,432
	RF	11	8,904	97,944					
ELECTRON TUBES	Receiver		—	—	CONNECTORS	RF	193	21,760	4198,680
	1-Gun CRT		—	—		≤ 25 Pin	23	11,152	256,496
	3-Gun CRT		—	—		> 25 Pin		—	—
	Thyratron		—	—					
	Klystron		—	—	SWITCHING DEVICES	Relay	2	29,500	59,000
	Magnetron		—	—		Toggle	6	15,000	90,000
	TWT		—	—		Rotary		—	—
	Amplitron		—	—					
	TR-ATR		—	—	AC MOTORS	≤ 6K rpm		—	—
MICROWAVE DIODES	Mixer	3	600,000	1800,000		>6K rpm	1	5120,000	5120,000
	Detector	5	390,000	1950,000	DC MOTORS	≤ 6K rpm		—	—
MICROWAVE COMPONENTS	Attenuator	6	332,000	1992,000		>6K rpm		—	—
	Loads	2	332,000	664,000	CIRCUIT BREAKERS				
	Rotary Jt		—	—	OTHER (LIST)			—	—
	Duplexer		—	—	LED 5089, DC		18	10,000	180,000
								—	—
FERRITE DEVICES	Isolator Low PWR	11	50,000	550,000				—	—
	Circulator		—	—				—	—
	Modulator		—	—				—	—
	Ø Shifter		—	—				—	—

DATE 11/21/77 | PREPARED BY | ASSY MTBF 19,942 HRS | ASSY FAILURE RATE 50,145.108 f/10⁹ HRS

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RELIABILITY PREDICTION

JOB 1026 | ITEM(11/FORM) | ASSEMBLY NO

EQUIPMENT MAR | ASSEMBLY NAME PDP

GROUP NAME | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon		⊥	⊥	FIXED RESISTORS	Compos	3	.013	.039
	Germanium		⊥	⊥		Film		⊥	⊥
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer		⊥	⊥	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
					FIXED CAPACITORS	Tantalum	5	.086	.430
MICROCIRCUITS	SSI		⊥	⊥		Electroly		⊥	⊥
	MSI		⊥	⊥		Other		⊥	⊥
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
	CURRENT	6	1.781	10.686					
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin	8	11.152	89.216
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay	1	29.500	29.500
	Magnetron		⊥	⊥		Toggle	4	15.000	60.000
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS		10	95.779	957.790
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE 1/21/77 | PREPARED BY | ASSY MTBF 874,337 Hrs | ASSY FAILURE RATE 1147.661 $/10^9$ Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB: 1026
EQUIPMENT: MAR
GROUP NAME:

ITEM(117FORM):
ASSEMBLY NO:
ASSEMBLY NAME: Power Supply, LV (Quan 12)
NEXT ASSEMBLY:

COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁹ HRS	EXT FR
TRANSISTORS	Silicon	6	6,197	37,182	FIXED RESISTORS	Compos	22	,013	,286
	Germanium		⊥	⊥		Film	12	,214	2,568
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd	2	,548	1,096
DIODES	Computer	8	1,260	10,080	VARIABLE RESISTORS	Film	1	49,234	49,234
	Rectifier	9	5,100	45,900		Wire Wnd		⊥	⊥
	Zener	2	10,725	21,450					
					FIXED CAPACITORS	Tantalum	8	,086	,688
MICROCIRCUITS	SSI LIN	1	24,205	24,205		Electroly		⊥	⊥
	MSI		⊥	⊥		Other	6	,092	,552
	LSI		⊥	⊥	VARIABLE CAPACITORS	Vacuum		⊥	⊥
						Other		⊥	⊥
TRANSFORMERS	Pwr & Fil	2	6,601	13,202	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin	1	11,152	11,152
	3-Gun CRT		⊥	⊥		> 25 Pin		⊥	⊥
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥				⊥	⊥
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE: 1/21/77 | PREPARED BY: | ASSY MTBF: 4575 K Hrs | ASSY FAILURE RATE: 217,595 f/10⁹ Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026 | ITEM(1177FORM) | ASSEMBLY NO

EQUIPMENT MAR | ASSEMBLY NAME ANTENNA

GROUP NAME TFF | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10⁶HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10⁶HRS	EXT FR
TRANSISTORS	Silicon				FIXED RESISTORS	Compos			
	Germanium					Film			
	SCR					Film Pwr			
						Wire Wnd			
DIODES	Computer				VARIABLE RESISTORS	Film			
	Rectifier					Wire Wnd			
	Zener								
					FIXED CAPACITORS	Tantalum			
MICROCIRCUITS	SSI					Electroly			
	MSI					Other			
	LSI				VARIABLE CAPACITORS	Vacuum			
						Other			
TRANSFORMERS	Pwr & Fil				INDUCTORS	DC Filter			
	Lo Pwr Pls					RF & Choke			
ELECTRON TUBES	Receiver				CONNECTORS	RF	4	21,760	87,040
	1-Gun CRT					≤ 25 Pin			
	3-Gun CRT					> 25 Pin			
	Thyratron								
	Klystron				SWITCHING DEVICES	Relay			
	Magnetron					Toggle			
	TWT					Rotary			
	Amplitron								
	TR-ATR				AC MOTORS	≤ 6K rpm			
MICROWAVE DIODES	Mixer					>6K rpm			
	Detector				DC MOTORS	≤ 6K rpm			
MICROWAVE COMPONENTS	Attenuator					>6K rpm			
	Loads				CIRCUIT BREAKERS				
	Rotary Jt	1	100,000		OTHER (LIST)				
	Duplexer				SLIP RINGS		1	5700.00	5700.00
FERRITE DEVICES	Isolator								
	Circulator								
	Modulator								
	Ø Shifter								

DATE 11/22/77 | PREPARED BY | ASSY MTBF 169,864 Hrs | ASSY FAILURE RATE 5,887,040 f/10⁶ Hrs

ITT Gilfillan

RELIABILITY PREDICTION

JOB 1026		ITEM(117FORM)	ASSEMBLY NO
EQUIPMENT MAR		ASSEMBLY NAME IFF RCVR/EXCITER	
GROUP NAME IFF		NEXT ASSEMBLY	

COMPONENTS	TYPE	QTY	f/10^6 HRS	EXT FR
TRANSISTORS	Silicon	72	6.197	446.184
	~~Germanium~~ RF	18	27.000	486.000
	SCR			
	RF L-Band	24	270.000	6480.000
DIODES	Computer	132	1.260	166.320
	Rectifier			
	Zener	8	10.725	85.800
	PIN	48	20.000	960.000
MICROCIRCUITS	SSI/MSI MM	18	24.205	435.690
	MSI			
	LSI			
TRANSFORMERS	Pwr & Fil			
	Lo Pwr Pls			
	RF	24	8.904	213.695
ELECTRON TUBES	Receiver			
	1-Gun CRT			
	3-Gun CRT			
	Thyratron			
	Klystron			
	Magnetron			
	TWT			
	Amplitron			
	TR-ATR			
MICROWAVE DIODES	Mixer			
	Detector	24	390.000	9360.000
MICROWAVE COMPONENTS	Attenuator			
	Loads			
	Rotary Jt			
	Duplexer			
FERRITE DEVICES	Isolator	18	50.000	900.000
	Circulator			
	Modulator			
	Ø Shifter			

COMPONENTS	TYPE	QTY	f/10^6 HRS	EXT FR
FIXED RESISTORS	Compos			
	Film	474	.214	101.436
	Film Pwr			
	Wire Wnd			
VARIABLE RESISTORS	Film	12	49.234	590.808
	Wire Wnd			
FIXED CAPACITORS	Tantalum	54	.086	4.644
	Electroly			
	Other	243	.092	22.356
VARIABLE CAPACITORS	Vacuum			
	Other			
INDUCTORS	DC Filter			
	RF & Choke	72	8.904	641.808
CONNECTORS	RF	24	21.760	522.240
	≤ 25 Pin	2	11.152	22.304
	> 25 Pin			
SWITCHING DEVICES	Relay			
	Toggle			
	Rotary			
AC MOTORS	≤ 6K rpm			
	>6K rpm			
DC MOTORS	≤ 6K rpm			
	>6K rpm			
CIRCUIT BREAKERS				
OTHER (LIST)				

DATE 11/1/77	PREPARED BY	ASSY MTBF 46,644 HRS	ASSY FAILURE RATE 21,438.566 f/10^6 HRS

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RELIABILITY PREDICTION

JOB 1026 | ITEM(117FORM) | ASSEMBLY NO

EQUIPMENT MAR | ASSEMBLY NAME IFF Data Processor

GROUP NAME IFF | NEXT ASSEMBLY

COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR	COMPONENTS	TYPE	QTY	f/10^9 HRS	EXT FR
TRANSISTORS	Silicon	12	6,197	74,364	FIXED RESISTORS	Compos		⊥	⊥
	Germanium		⊥	⊥		Film	300	.214	64,200
	SCR		⊥	⊥		Film Pwr		⊥	⊥
						Wire Wnd		⊥	⊥
DIODES	Computer	36	1,260	45,360	VARIABLE RESISTORS	Film		⊥	⊥
	Rectifier		⊥	⊥		Wire Wnd		⊥	⊥
	Zener		⊥	⊥					
					FIXED CAPACITORS	Tantalum	40	.086	3,440
MICROCIRCUITS	SSI/MSI DTL	2680	17,262	46,262,160		Electroly		⊥	⊥
	MSI/MSI ECL	110	24,205	2662,550		Other	1100	.092	101,200
	~~RAM 256B~~	20	27,980	559,600	VARIABLE CAPACITORS	Vacuum		⊥	⊥
	RAM 1024B	80	87,350	6988,000		Other		⊥	⊥
TRANSFORMERS	Pwr & Fil		⊥	⊥	INDUCTORS	DC Filter		⊥	⊥
	Lo Pwr Pls		⊥	⊥		RF & Choke		⊥	⊥
ELECTRON TUBES	Receiver		⊥	⊥	CONNECTORS	RF		⊥	⊥
	1-Gun CRT		⊥	⊥		≤ 25 Pin		⊥	⊥
	3-Gun CRT		⊥	⊥		> 25 Pin	20	340,000	6800,000
	Thyratron		⊥	⊥					
	Klystron		⊥	⊥	SWITCHING DEVICES	Relay		⊥	⊥
	Magnetron		⊥	⊥		Toggle		⊥	⊥
	TWT		⊥	⊥		Rotary		⊥	⊥
	Amplitron		⊥	⊥					
	TR-ATR		⊥	⊥	AC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE DIODES	Mixer		⊥	⊥		>6K rpm		⊥	⊥
	Detector		⊥	⊥	DC MOTORS	≤ 6K rpm		⊥	⊥
MICROWAVE COMPONENTS	Attenuator		⊥	⊥		>6K rpm		⊥	⊥
	Loads		⊥	⊥	CIRCUIT BREAKERS				
	Rotary Jt		⊥	⊥	OTHER (LIST)			⊥	⊥
	Duplexer		⊥	⊥	RAM 256B		110	16,560	1821,600
								⊥	⊥
FERRITE DEVICES	Isolator		⊥	⊥				⊥	⊥
	Circulator		⊥	⊥				⊥	⊥
	Modulator		⊥	⊥				⊥	⊥
	Ø Shifter		⊥	⊥				⊥	⊥

DATE 1/22/77 | PREPARED BY | ASSY MTBF 15,294 HRS | ASSY FAILURE RATE 65,382,474 F/10^9 HRS

MISSION
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Printed by
United States Air Force
Hanscom AFB, Mass. 01731