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MAY, 1977

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ELECTRON BEAM FABRICATION OF SURFACE ACOUSTIC WAVE TRANSDUCERS

ADVANCED METALS RESEARCH CORPORATION

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AIR FORCE SYSTEMS COMMAND
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APPROVED: Alan J Budreau

ALAN J. BUDREAU
Project Engineer

APPROVED: William C. Schell

ALLAN C. SCHELL
Acting Chief
Electromagnetic Sciences Division

FOR THE COMMANDER: John P. Huss

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A Lanthanum Hexaboride Gun was added to the electron beam fabrication system. Systems programming was advanced. The elements of a cooperative exposure effects model were developed and instituted in the programming. Exposure techniques were developed to optimize resolution and edge definition.

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EVALUATION

1. This is the Final Technical Report on the contract. It covers research done on the scanning electron beam fabrication of surface acoustic wave (SAW) devices during the full period of performance. Progress was made in both the programming of the necessary data for fabrication of such devices and in the fabrication itself. Improvements were made in the equipment.

2. SAW devices are finding increasing use in military and other systems due to their advantages of small size and weight, low cost, and reliability. Scanning electron beam fabrication, with its two inherent advantages of high resolution and direct control by computer output, will allow SAW devices to operate at higher frequencies and speed up turn around time in research applications.

Alan J Budreau

ALAN J. BUDREAU
Project Engineer

FOREWORD

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This contract was a continuance of an effort to develop the techniques necessary to fabricate surface acoustic wave transducers using an electron beam lithography system. Theoretical performance of the electron optical column and resist processing techniques were described in detail in final technical report RADC-TR-76-289. This report describes the results of the second phase of the contract and also includes a detailed technical discussion of the operating sub-systems.

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I. INTRODUCTION

This final report includes the equipment utilization report as well as a detailed discussion of the operation of the electron beam fabrication system. Because the general description of the system and its electron optical performance were described in an earlier report (1) they are not repeated here. This report is a detailed discussion of the operating system so that it may be operated by qualified personnel.

Electron beam fabrication techniques are now widely utilized by research laboratories and these techniques are the only means of generating surface acoustic wave transducer patterns of the high resolution necessary for high frequency devices.

II. THEORY OF OPERATION

The electron beam fabrication system consists of three separate sub-systems: 1) An electron optical column and stage, 2) an analog electron optical control and display unit, and, 3) a digital control system. It is anticipated that some maintenance will be required and that the assistance of qualified service personnel will be available. To be able to troubleshoot and maintain the system will require a thorough operational knowledge of each sub-system. To provide an operational knowledge of the system, the unit is described from a functional perspective.

A) Pattern Formation

The basic pattern is formed by an electron beam impinging on a substrate covered with a suitable electron resist. The exposed areas are determined by a combination of stage motion, magnetic beam deflection, and beam blanking. Since it is difficult to maintain a finely focused electron beam over large areas the beam is positioned by a combination of sample movement and beam deflection. The total area over which the beam can be located is $100cm^2$. The beam may be deflected over an area of approximately $4mm^2$ without movement of the sample.

The general procedure is to make complete SAW transducers within one deflection field of the beam, defined as a scan field, and to make neighboring devices by subsequently moving the stage holding the substrate. The beam is blanked off during repositioning so that the exposure is confined to the desired areas.

The transducers are exposed and the stage is moved in this fashion as is required until the program for that substrate is completed. Through combinations of beam deflection and stage movement all points on the $100cm^2$ addressable area of the stage may be exposed.

The substrate table is a motorized stage with two normal axes, each of which is capable of locating the stage over a 100mm travel. The individual axes are lead screw driven under the control of stepping motors. Each axis is independently monitored by a laser interferometer which is configured to monitor stage movements in 791 angstrom ($\lambda/8$) steps. Since there is a 100mm translational capability each axis contains 1,264,222 individually accessible addresses on each axis or approximately 4×10^{12} discrete points over the surface. Any of these discrete address locations is uniquely described by a 21 bit binary word which is incremented or decremented by the interferometer as the stage is moved.

The magnetic deflection field of the electron beam is also digitally addressed and contains $(2^{14}-1)^2$ addressable points. Unlike the stage position, however, which is fixed by the resolution of the interferometer, the total size of the magnetic deflection field is adjustable and can be varied continuously so that the total field size may be set from approximately .75mm to 2mm on a side. This allows virtually infinite selections of

address structures for pattern definition within the limits given.

Two basic alternatives exist for positioning the beam to expose a pattern. The beam may be scanned over the entire deflection field and blanked on and off in response to program information to delineate the pattern. This raster scan approach has certain advantages but suffers from the major disadvantage that the beam must be deflected over the entire surface area whether the entire surface is being exposed or not. An alternate, more efficient approach is to position or vector the beam only to the areas which require exposure. A number of various vector scan approaches has appeared in the literature (2). The AMR pattern generator uses a simplified version in which a pattern is broken down into sub-rectangles and each rectangle is exposed seperately. The pattern must be described one rectangle at a time on the program tape.

B) Rectangle Exposure

Any pattern may be described in two dimensions, x and y, the choice of which axis is chosen as X is unimportant from the point of view of the sample being exposed. From the point of view of the system on the other hand, the axes are strictly defined in terms of the way the rectangle is formed.

Each rectangle in the exposure is defined in terms of the 14 bit binary addresses which locate the four corners of the

pattern element. The scanning sequence as defined by the pattern generator is that the beam is digitally stepped in the X direction one addresses at a time until a line is complete and then the next y line is scanned in the x direction. This sequence, illustrated in figure 1, continues until the full rectangle is exposed, i.e. until the X line at address Y_2 is exposed. Once this rectangle is finished, the pattern generator calls for new values of X_1, Y_1, X_2, Y_2, and proceeds to make the next element. Although there appears to be no fundamental difference between the x and y axes in the machine, practical electronic problems do exist. When the deflection system calls for a large movement of the beam such a retracing, time must be allowed for the deflection system to settle to its correct value. Each time the beam finishes an x line, a dead time is inserted in the digital counting sequence which provides a window allowing the deflection system to recover. This time is fixed for the worse case transistion and constant independent of the x line length. Many exposures are lines, i.e. rectangles where one dimension is much greater than the other. If the pattern is set up such that the long dimension is Y and the short dimension is X, the exposure will take much longer than if the axes are reversed. For this reason a pattern should be positioned so that the lines have their long dimension in the X direction whenever possible.

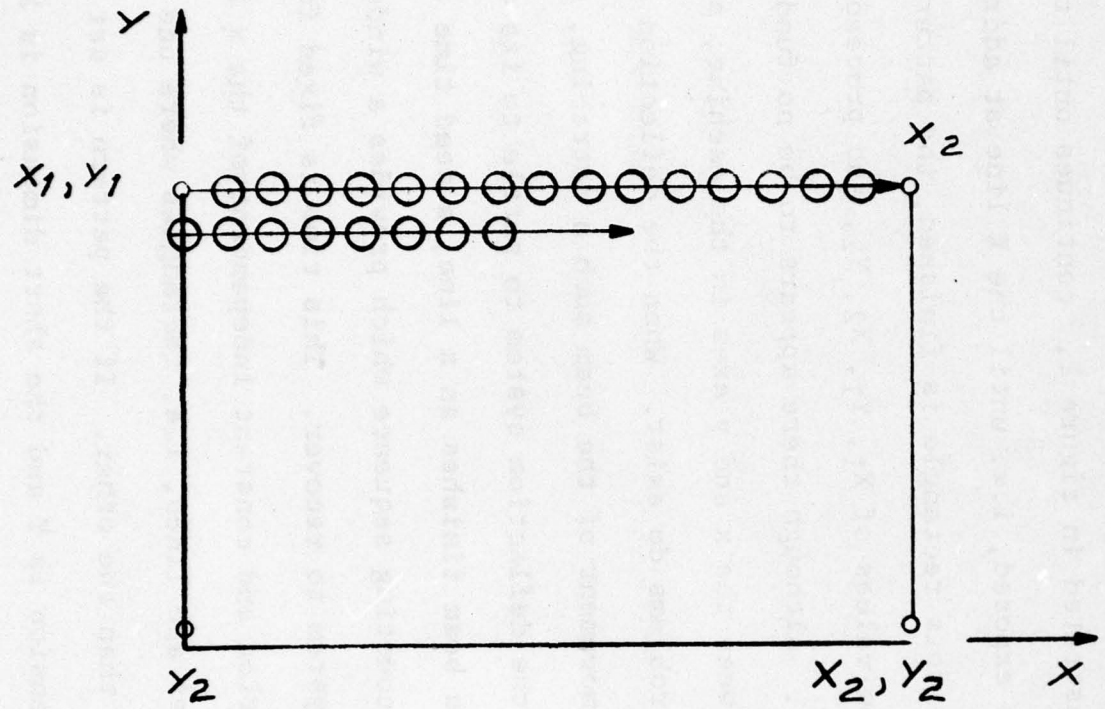


FIGURE 1: TYPICAL SCAN SEQUENCE

One additional limit exists on the digital sizes of the rectangles. For proper hardware operation every X line must be at least 2 bits long, Y lines can be only 1 bit ($Y_1 = Y_2$). The smallest pattern element which can be addressed therefore is 2 bits in X and 1 bit in Y. The largest is the full digital field ($2^{14} - 1$ locations on each axis).

C) Exposure

The actual dose required by a pattern element is dependent on such parameters as rectangle size, spacing, resist thickness, and accelerating potential. The pattern generator however has no information about the correct exposure and this information must be contained in the system software. Some capability must be provided for the system to vary the exposure and this is provided by varying the dwell time of the beam at each address location. The pattern generator is limited in that the beam dwell times can only be varied by factors of 2. A total factor of 256 in factors of 2 is provided in the hardware. If a finer exposure is required the same element can be repeatedly exposed at different dwell times until the appropriate exposure is built up. These exposure values are contained in the data blocks which contain the rectangle dimensional information.

D) Substrate positioning

The stage is controlled by a laser interferometer which determines the position of the stage in 791$\overset{o}{A}$ steps. The location of a particular device on the substrate surface is also contained on the program tape and is usually included with the block of data that describes the first rectangle of the pattern. When the stage location is loaded from the tape the stage is commanded to move to the assigned position. As the stage moves to its assigned location its actual position is monitored by the interferometer. The table moves at a high rate if its actual location and assigned location differ by a large amount. The stage travel rate is decreased by factors of two until the actual address is reached. Once the address is reached the stage drive is turned off and the stage position is monitored for one second to determine the exact location. Since the stage will always overshoot the desired position by a small amount (typically 1 micron) the overshoot is monitored and a correction signal is sent to the deflection system to correct for the error.

E) Data Loading

The preceding paragraphs have described the different types of information required for the system to form a pattern in the resist surface. This data contains a maximum of seven information words: rectangle size (4 14 bit words), stage address (2 21 bit words), scan rate (1 3 bit word). Since the system

has only a very limited memory, data for every new rectangle or stage motion must be loaded from tape. Each group of data, a block, may contain all or none or any combination of the data words described above, and each block also contains a coded execution statement which commands the system to perform the function described by the data in the block. Since the system memory is static, it is only necessary to load new information in a particular data block. Any words loaded in previous blocks will be retained and used in subsequent blocks until the words are changed. The actual formatting of these data words are described in more detail in the hardware description.

F) Field Alignment

When exposing more than one level of a device and when precise address structure is required, a means must be provided to set and align the scan field position and dimensions. This is accomplished by scanning and visually displaying easily identifiable marks at the extremities of the deflection fields. These marks may be either fixed calibration grids (see (1)) or benchmarks located on a substrate during the first exposure. To set a scan field address structure initially, the calibration marks are scanned in the A & B mode (x field) and the field gain is adjusted until the appropriate grid lines are in view. To do a y field calibration, the C & D mode is selected and the extremes of the y field are selected.

For alignment of subsequent exposures on multiple level

devices, the benchmarks are exposed during the first masking layer and the field is aligned to these marks at the beginning of each later exposure.

III. SYSTEM HARDWARE

The electron optical controls and electron optical column are described elsewhere (3). The digital control system is unique to the electron beam fabrication system and so will be described in detail.

The various modular elements were pictured and described in an earlier report (1). The following sections will describe the detailed operation of the individual circuits. All of the circuits used to implement the control system functions are 54/74 series TTL logic. These devices are characterized by a positive logic convention with a logical 1 = 4.0 volts and a logical 0 = 800mV. (Nominally high = 5V, low = 0V). All measurements of voltage and signal levels should be made using a compensated high impedance oscilloscope probe.

A) Scan Generator

The digital scan generator contains all of the circuits necessary for processing the pattern rectangle data and generating the signals necessary for deflecting the electron beam. Analog signals are produced which drive deflection amplifiers, which in turn generate currents to deflect the electron beam through a magnetic deflection system.

The functions of the scan generator are subdivided into functional groups which are associated with each axis. These

functions are located on five digital circuit boards and 1 analog board which are all located in the scan generator chassis. The basic functionality of each axis is similar and is described with the aid of figure 2.

As has been discussed each beam location is addressed serially, i.e. the beam dwells at a point and then moves to next point, until an entire line is scanned. The rate of beam stepping, or more precisely,the beam dwell time,is determined by the clock frequency which is controlled by the program. The lower the clock frequency the longer the dwell time per point. The system clock is calibrated so that its fastest rate results in a beam dwell time/point of 4 micro-seconds (250 KHz). Each lower scan frequency increases the beam dwell line by a factor of 2 from the previous one. A listing of these dwell times is shown in table 1.

The scan line has a resolution of 14 bits (16,383 addressable points), and a line can be as short as 1 bit or as long as 16,383 bits. The digital length is fixed and located by the start and finish coordinates. These are 14 bit words typically called X_1 and X_2 for the X line. They are read off tape and stored in a memory called a start register and a stop register. When commanded, the contents of the start register are loaded into a counter and become the digital address of the beginning

RATE	DWELL (μS)
A	4
B	8
C	16
D	32
E	64
F	128
G	256
H	512

TABLE 1: BEAM DWELL

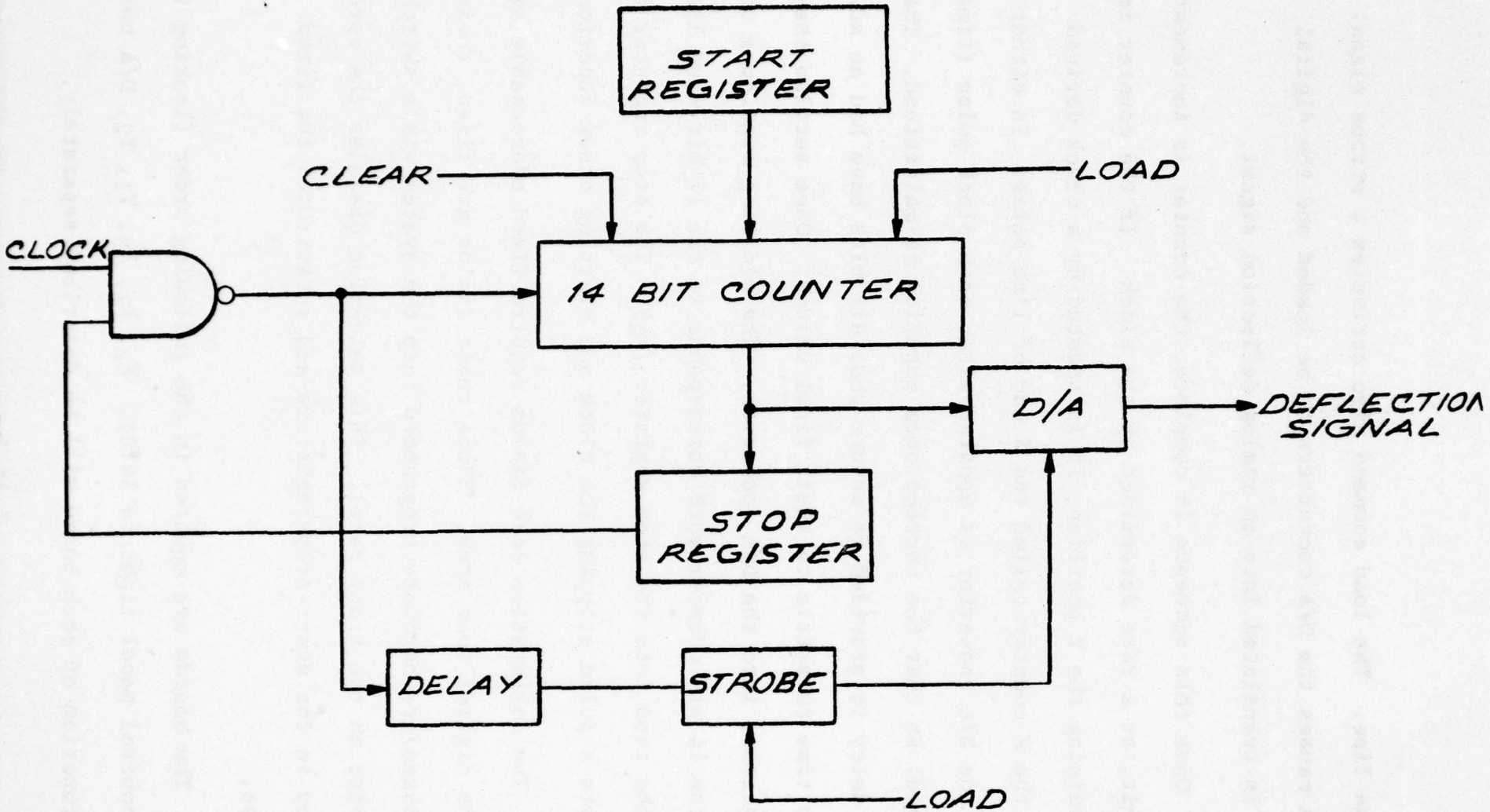


FIGURE 2: COUNTER BLOCK DIAGRAM

of the line. The load command also activates a strobe signal which causes the D/A converters to be loaded and the digital word is translated into an analog deflection signal.

Once this sequence is complete, the counter is incremented one bit, at a rate determined by the clock. If the counter is determining the Y position, it is updated by a clock derived from the X counter called the X end of line pulse. In either case the D/A converter is updated after each clock pulse (time delayed) so that the correct beam position is maintained. The time delay is provided to assure that all bits have had an adequate time to settle to their final values. Once settled they are strobed into the D/A converter. The clocking continues until the 14 bit counter word corresponds to the 14 bit word loaded off the tape into the stop register (X_2). The stop register then outputs a pulse stopping the clock and starting other functions.

The calibration scan fields require fixed addressable areas of the digital scan area. Since these fields are fixed, their addresses are hardware programmed into the system via a switch selector on the front panel. This selection disables the words stored in the start-stop registers and substitutes the fixed values.

The boards are mounted in the following order (looking from the control panel right to left). X_1, X_2, X_3, Y_1, Y_2, D/A board. The function of each board will be described separately.

A.1 X1 Board

The X1 board (shown schematically on DX-31420-036) contains the start-stop registers for the X scan and the board wired addresses for the calibration mode scans.

I.C. 1-1 and 1-2 are the X1 or start registers and contain the 14 bit word which describes the start of the X line. Data is loaded serially into these memories on pins 1 and 2. The data is loaded by clocking the memories (pin 8) at the appropriate time. Since these memories are each 8 bit registers (although the 2 MSB's are not used) it requires 16 clock pulses to load the data. (These pulses are derived from the tape reader logic which will be described later).

I.C. 2-1 and 2-2 are the stop register memory. As with the start register, the LSB of the address appears on 2-1-13 and the MSB on 2-2-5.

They are buffered by a series of NAND gates 1-3 to 4-2. These gates act together to either pass on the address data to the counters or to inhibit it. The buffers are enabled/disabled by the scan mode select switch on the front panel, S1. When S1 selects the Auto Scan position, the inputs of I.C. 1-5 are forced low and its high output enables the buffers. In any of the other positions, however, the buffers are disabled and their outputs remain high. In the Auto Scan mode, which is the mode selected for pattern writing, the buffer gates outputs are fed to the input register gates 2-4 to 4-5. In the auto mode,the outputs of these

gates are identical to the word stored in the memory since 2 inversions have occurred.

The other switch positions are for selecting the calibration scan modes and do so by selecting hard wired words for X_1 and X_2, fixing the start and stop registers independent of the data on the tape. The size of the scan fields have been selected to be 256 bits on each axis so that they are 1.5% of the entire digital field. The locations of these fields were described in (1). The 3 combinations are: 1) two fields on the X axis at the field extremes (A&B), 2) two fields on the Y axis at the field extremes (C&D), 3) one field at the center (CH). It should be noted that although there are five separate fields, there are only 3 different addresses for each of the start and stop registers. For example, in A&B and CH modes Y_1 and Y_2 are the same, in C&D and CH modes X_1 and X_2 are the same.

The addressing scheme is best understood by considering the following example. The full digital field (14 bits) can be written in octal notation as $(37777)_8$. Each calibration field is 256 bits (0 to 255) or $(377)_8$. The X address for the A&B fields is determined by noting that for field A the X_1 value is at the edge of the field, plus 1 bit or $(00001)_8$, adding $(377)_8$ to this yields $(00400)_8$ for the X_2 address. These addresses are broken into binary form and each bit is programmed to the appropriate gate. Each of the 3 switch positions, A&B, C&D and CH forces the output

of one of the sections of 1-6 high. In A&B for example, 1-6-10 is high which enables 1-5-12 and 2-6-3. The output of each of these gates is routed to selected buffer gates as called for by the address code described above. Output 2-6-6 goes to 2-4-2 and 6-13-13. When the A subfield is being scanned, the LSB (2-4-12) is held high since the A line is held at 0, independent of the states of the other inputs to 2-4. All other bits are 0's. This condition is assured because all other fixed address lines are 1's. There are five code lines which can be selected: A, B, CH, CD and *. As noted, the X_1 and X_2 address in the C&D mode are the same so that no distinction is required when in the C&D mode. Many of the address bits are the same for many modes so the * rail is used for inputs which are common to different modes. For example, the * is low (active address) whenever the B rail is low via 2-6 and 1-5. This also is true for the CH and CD modes for X_1, X_2 addressing.

A.2 X_2 Board

The X_2 board (shown schematically on DX-31420-036) contains the master clock and the scan rate decoder. The clock consists of a collector coupled (astable) multivibrator, Q_1 and Q_2, which is tuned to 250KHz. It can be disabled for troubleshooting purposes by a switch on the front panel. The clock is fed directly to a 4-bit binary counter (IC 4-5 & 5-5) where the master frequency is divided by factors of two to a low frequency of approximately 2 KHz.

Each of these lower frequencies (which appear on pins 3-7) is distributed to a separate 4 input nand gate. If the other 3 inputs of the gate (IC 4-6 thru 6-5) are high that particular sub frequency will be passed on to the mixing gate, 3-6. Only one of the eight frequencies will be decoded by 3-6. If desired, the clock frequency can be manually selected by switch 32 which bypasses the decoders. In either case the frequency (which is a symmetrical square wave) is converted into a pulse train of the same frequency by 1-4.

In general, the clock frequency is selected by the program through the decoders. Which decoder is selected depends on the non-clock inputs. These inputs are controlled by 4-4 and 3-5. IC 4-4 stores a 3 bit binary word which has been read from the tape. Since there are 8 possible scan rates only 3 binary bits are required to describe all cases ($2^3 = 8$). If for example all 0's are stored in 4-1 (LSB is pin 4, MSB pin 6) the fastest scan rate is selected. This is the case because all 0's from 4-1 forces all 1's from 3-5. The decoding inputs of 4-6 (pins 2, 4, 5) are connected directly to 3-5. When these three are high, the gate is enabled and the fastest clock is selected. If any of these inputs were low the gate would be disabled. In a similar fashion, the other seven decoders are enabled by codes 001 to 111.

A.3 X_3 Board

The X_3 board (shown schematically on DX-31420-037) contains the X scan counter and stroke circuits.

The main 14 bit counter consists of IC's 3-1, 5-1, 6-1, and 7-1. IC's 5-1 through 7-1 are 4 bit syncronous presetable binary counters with clear. When commanded (by a low pulse) applied to pin 11, the X_1 word is loaded into the counters. Since these devices are only 4 bit counters, they are supplemented by 2 flip-flops (IC 3-1) to fill out the 14 bit field. These individual flip-flops provide the capability of variable bit density field by allowing choice of 13 and 12 bit fields through the selection of switch S3. In either case the counter can be preset to any 14 bit word and cleared to 0 when commanded. In general the counters are cleared prior to the start of a program and for test purposes. Typically an X_1 start address is loaded at the beginning of every X scan line, and is reloaded as many times as is necessary to complete the full rectangle.

The clock (whose frequency has been selected on X_2) is applied to 4-1-3. Whether it is allowed to actually increment the counter depends on the state of flip-flop 7-6-15. When its output is high the clock buffer 4-1 is enabled and the counter is incremented. On every clock pulse the counter state changes by 1 bit and IC 2-5 is gated. IC 2-5 is a monostable circuit which generates approximately 100 us delay before gating IC 1-5 another monostable which supplies the stroke to the X D/A converter. In this way the converter is updated with each new X word.

This incrementing sequence continues until the counter contents equal the X_2 word stored in the memory. This comparison is made by IC's 4-2 through 3-3. These exclusive "or" gates have a 1 output when either input is a 1. Since one input is from the X_2 register and the other input is an inverted version of the register contents (processed by 5-2 through 6-2), each subcomparator outputs a 1 whenever the X_2 register and the counter are equal for that particular bit; when they are unlike the subcomparator output is 0. Since the subcomparators compare every bit, the end line is only decoded when all the bits are equal and are strobed by the clock. Under these circumstances, an end line low pulse appears on 5-4-8. This pulse sets flip-flops 7-5-15 which simultaneously blanks the electron beam (via I.C. 7-4 and 8-4) and resets the clock enable flip-flop 7-6-15. This resetting of 7-6-15 disables the clock buffer 4-1. The clock to the counter is disabled until further signals are received. The counter will remain fixed at the X_2 value and the board will be dormant. I.C. 6-6 generates a pulse at the X end of line to be distributed to other sections of the system.

In summary, two commands must be received by the X_3 board to activate it. They are: X_1 load and begin X line. Their timing is shown in figure 3.

In general, the CRT is blanked whenever the electron beam is blanked and the CRT blanking signal is routed via I.C. 8-4.

When the system is being operated in the analog mode as a SEM, the beam blanking is disabled by holding 8-4-2 low. This has no effect on the CRT blanking since the CRT is not under digital control in this mode. During the calibration sequence the CRT is blanked by a control signal routed by I.C. 8-5-11 which generates the black crosshair on the CRT screen.

A.4 Y_2 Control Board

The Y_2 Control Board (shown schematically on DX-31420-039) performs the "housekeeping" functions for the scan generator. This circuit receives and transmits the signals which control the function of the scan generator. The operation of this subsystem is best understood by following a typical signal flow.

Assume that a rectangle has been written and the next block of data requires the movement of the stage. Once the stage is moved to the assigned address and the motion is complete and settled, a pulse is received by IC 4-1 and IC 4-2. This pulse is the command to the scan generator to write the next rectangle. It should be noted that these pulses are received whether the stage is commanded to move or not. If the stage has not been commanded to move, these pulses will appear approximately 1 second after the tape is read. These stage complete pulses set both flip-flops of I.C. 2-4. When these flip-flops are both set, a d.c. set level is transmitted to 1-5-3 and 4-5-8 setting these flip-flops. This d.c. signal is routed via IC 3-4 which can also

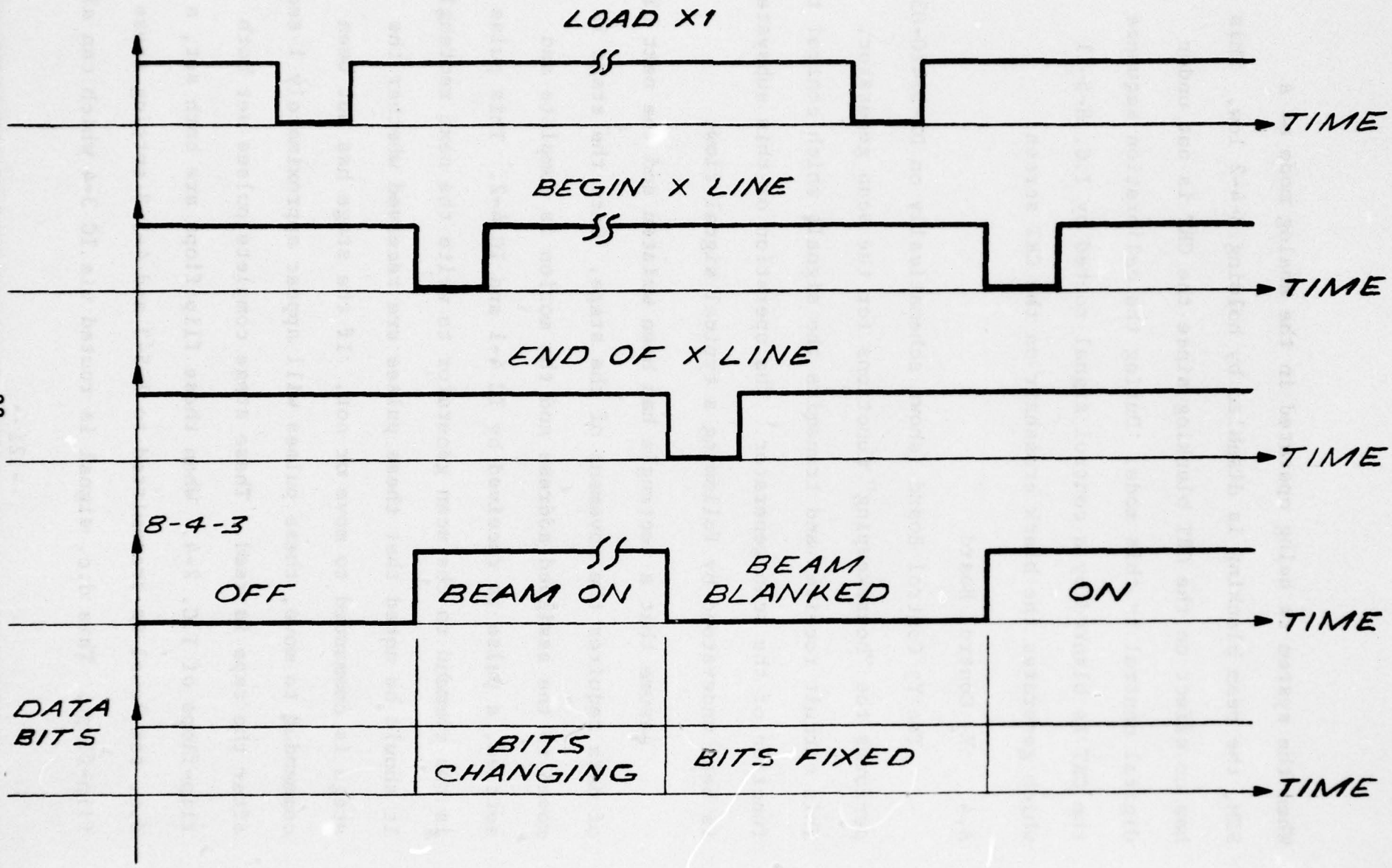


FIGURE 3: X3 BOARD TIMING

be controlled by the on-off start switch on the front panel (S5). This switch provides a manual means of providing the scan generator with end of stage motions commands. Leaving this switch in the on position forces the 2 flip-flops into a permanently set position and is not a proper operating mode of the system.

The setting of these two flip-flops (1-5 & 4-5) causes two events: first 3-5-3 goes high and 4-5-2 goes low setting 4-5-15 to a high. This event allows signals appearing on 3-5-5 to increment the two binary counters 5-4 and 5-3. The signal transmitted to the counters is a divided version of the 250 KHz master clock which is obtained by decoding the outputs of IC 5-2 and 5-1. In general, the signals which are selected for transmission to the counter are the C/128 and C/256 frequencies of the master clock (selected from IC 5-2 pins 6 and 7). This provides basic count frequencies of 2 KHz and 1 KHz. Which of these basic frequencies is chosen depends on the state of 3-2, a flip-flop which changes state at the end of every X line. These timing clocks are routed to the counters via 3-1, 6-1,and 1-6.

As long as both inputs at IC 3-5 (3 & 4) are high, the timing clocks are sent to the counter. The states of this counter are decoded by IC 5-5, 6-5, 7-5 and 7-4, each outputting a low pulse at a point in the timing sequence. I.C. 5-5 for example decodes the first count of the counter (0000001). When I.C. 7-3-12 is enabled this pulse causes flip-flop 8-3 to change states. The initial state of 8-3 is unimportant; it is only necessary that it

change state. IC 6-5 decodes the second bit of the counter and produces a low pulse of 1/2 clock period during the fourth clock cycle; this pulse is used for two functions: 1) loading the X counter with the information stored in the start register, and 2) it either loads the Y counter with the contents of the Y start register or routes a clock signal to the Y counter. The Y counters are updated by one bit at the end of each line. Which of these functions occurs depends on the status of the load-clock flip-flop 1-5. In the assumed conditions of the example, the load function would occur since this would be the first line of the rectangle to be written. On subsequent Y lines the clock output would be enabled. I.C. 7-5 decodes a pulse generated later in the clock sequence, the 111 pulse. If, for example, the clock frequency were 2KHz, this pulse would be .5 ms long and occur 55.5 ms after the count sequence was initiated. This decode sequence is illustrated in figure 4. I.C. 7-4 decodes pulse 128 in the sequence which occurs later than 111.

The relative timing of these last two pulses is critical to the housekeeping functions of the scan generator. The 111 pulse (IC 7-5) resets 2 flip-flops, I.C. 1-5-15 and 4-3-15. The original preset of 1-5-15 which occurred after receipt of the stage complete pulse was one of the commands which allowed the counter sequence to begin. The 111 pulse removes the d.c. set pulse

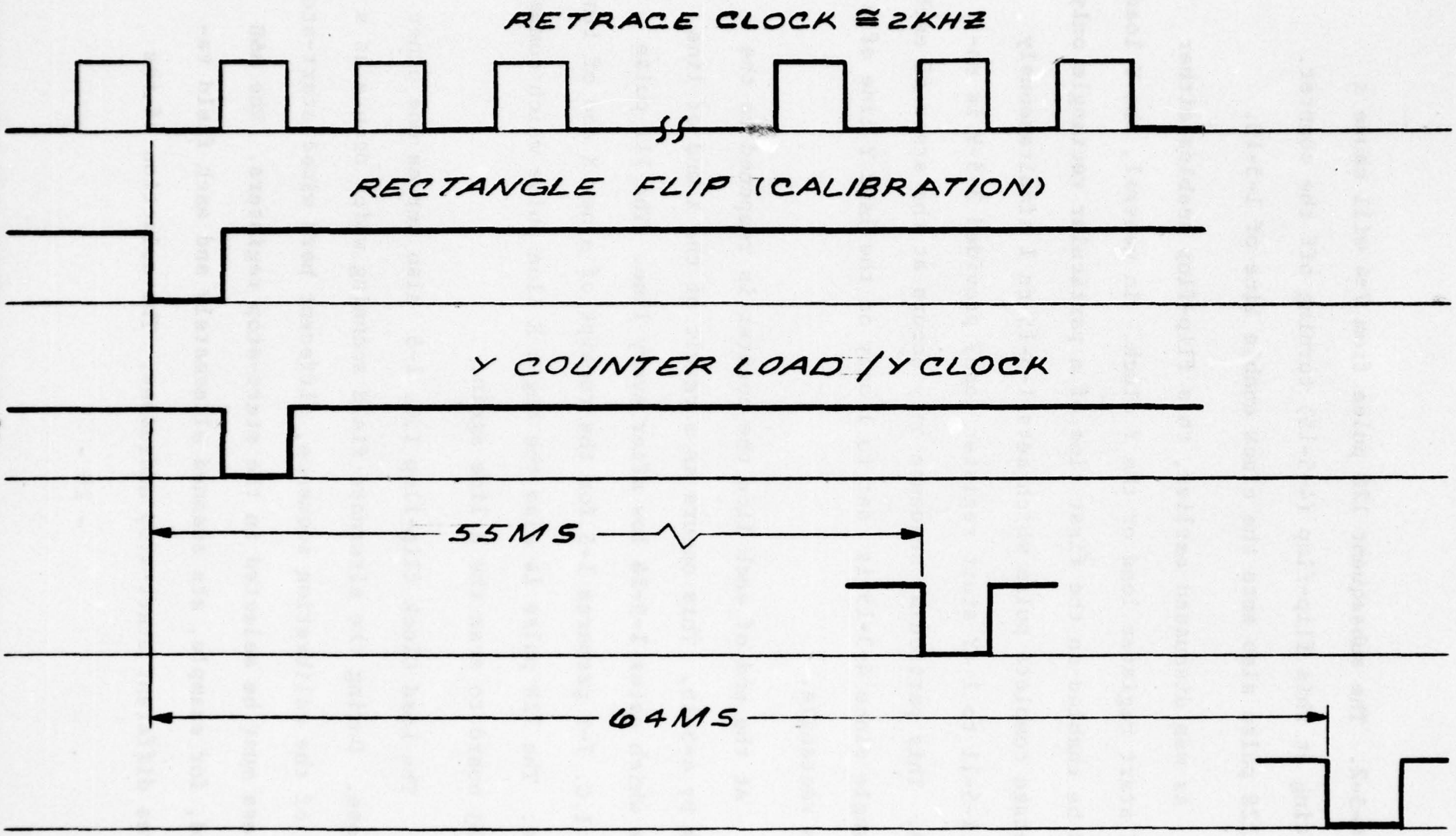


FIGURE 4: Y_2 TIMING

from 4-5-2. The subsequent 128 pulse from 7-4 will cause a resetting at this flip-flop (4-5-15) turning off the counter. This 128 pulse also sets the clock enable line of 1-5-10.

As was discussed earlier, this flip-flop enables either the Y start register load or the Y clock. In general, the Y load would be enabled on the first line of a particular rectangle only. The stage complete pulse which sets 1-5-15 to 1 simultaneously sets 1-5-11 to 1 (Y start register load) provided 3-5-9 is enabled. This particular sequence only occurs at the start of each rectangle since 4-3-15 is set to 1 only on the last Y line of a given rectangle.

At the end of each line the counter is reopened to the clock by 4-5-15. This occurs as a result of the X end of line pulse which gates 1-5-14 low after every line. The 111 pulse from I.C. 7-5 prepares 1-5 for the receipt of a new X end of line pulse. The 128 pulse is also the begin X line pulse which commands the X_3 board to scan the X line again.

The Load Clock flip-flop I.C. 1-5 also serves one other purpose. During the alternate field scanning which occurs as a part of the calibration sequence, different hard wired start-stop address must be selected in the start-stop registers. The A&B field, for example, are scanned alternately and each field requires different start-stop addresses. The selection of the

address is performed by I.C. 8-3 via the pulse decoded by IC 5-5. This occurs only when 7-3-12 is a 1, or when the Y load is enabled. In other words, the alternate rectangle is selected during the first count sequence and the flip-flop is disabled thereafter.

As may be seen at this point, the count sequence is initiated after either a stage complete (new data block) pulse is received or an X end of line is received. In either case the counter is started and the decoding sequence is begun. Both the Y clock and X_1 load pulses occur early in the sequence followed much later (as long as 64ms) by the begin X line command. In both the Y clock and X_1 load cases the D/A converter is loaded with the new X or Y values and the deflection system responds. The long delay between the actual loading and the beginning X line allows the deflection system time to respond. Because the clock frequency alternates on every X line (via the selection at I.C. 3-2, which changes states after every X line), the time delay, or dead time, between lines alternates between approximately 32ms and 64ms. This causes a partial cancellation of any spurious frequency effects which occur due to strong magnetic coupling and provides for improved edge definition. These long dead times are essential to eliminate any lags in line ends after a large change is made. It is this long delay which occurs after every X line that makes a judicious choice of the X direction for the long dimension of any features.

This alternating delay time provides a very useful function during pattern writing. During calibration, however, these line delays are excessive and result in exceptionally slow scan rates. To aleviate this situation, a dead time clock at a higher rate is used. This faster clock is derived from I.C. 5-1-3, and is routed to 3-5 (the clock buffer gate) via I.C. 6-1. I.C. 6-1-13 is enabled by I.C. 7-1, I.C. 7-1 input goes directly to I.C. 3-5-1 which obtains its information from the scan mode switch on the front panel. When in the Auto Scan (pattern writing mode) this line is high, which disables 6-1-13 and enables 6-1-5 allowing the alternate slow clock to pass. In any of the calibration modes, however, the pulse states are reversed and the fast clock is allowed through and the slow clocks are disabled. This increases the available scan rates in the calibration modes by a factor of 4.

The final housekeeping function performed by the Y_2 board is the tape advance. Since each rectangle requires new data off the tape, the tape must be advanced after the end of each rectangle. The tape advance pulse is generated by I.C. 3-5-12 and occurs when: 1) the scan mode selector is in Auto Scan (pin 1 high), 2) a Y_2 stop register is decoded (setting 4-3-15 to 1), and 3) and X end of line pulse occurs. The X end of line pulse is routed to the tape reader via I.C. 3-5 and advances the tape

to the next block of data. In the calibration mode the tape is not advanced since 3-5-1 is disabled. In this case, the Y start register is reloaded and the field is scanned again. The tape advance pulse also causes a reset of 4-5-10. This also has the effect of disabling the clock buffer gate I.C. 3-5, and prepares 4-5 for reception of a subsequent stage complete command.

The functions of the Y_2 board are very complex but can be summarized by noting the functions:

a) Generate counter load pulses

b) Generate begin X line

c) Rectangle select for calibration modes

d) Provide variable dead times

e) Decode tape advance functions

f) Strobe Y D/A converters

A.5 Y_1 Counter Board

The Y_1 board (shown schematically on DX-31420-038) performs a function identical to the X_3 counter board. It also contains the start and stop registers (I.C. 1-1, 1-2, 2-1, 2-2) for the counter, the register address buffers I.C. 1-6 through 5-3 and the hand wired addressing for the Y_1 and Y_2 used in the calibration modes. The counter functions identically to the X counter and all equivalent functions are comparable.

A.6 Analog Board

The analog board of the scan generator (shown schemati-

cally on DX-31420-040) houses all of the analog signal elements such as the digital to analog converters.

The main function of the board is to convert the 14 bit digital address of the beam into an analog signal capable of driving the deflection amplifiers. The main converters are Analog Devices type DAC 16QG, which are actually 16 bit converters. The two least significant bits are not used but are available for future use if desired. These converters require only a 14 bit digital input and output a bipolar 10V full scale signal. The converters are mounted on the front of the board as subcards.

The analog ouput of these converters are not routed directly to the deflection amplifiers but are summed with 2 additional d.c. signals. The output circuit is shown schematically in figure 5. One of the d.c. signals is obtained from a potentiometer on the front panel (offset) which allows precise positioning of the entire field in response to calibration features on the substrate. The other d.c. correction is obtained from the stage monitoring circuits where signals are generated to correct for errors in calculated and actual stage positions. As was mentioned earlier, the field size is variable. Although the field is always 14 bits the deflection angle is adjustable by the gain pot on the front panel;the largest field is at a gain setting of 10.0. As shown in figure 5, a limiting resister (500Λ) is in series with the gain potentiometer. This limiter is to prevent the deflection

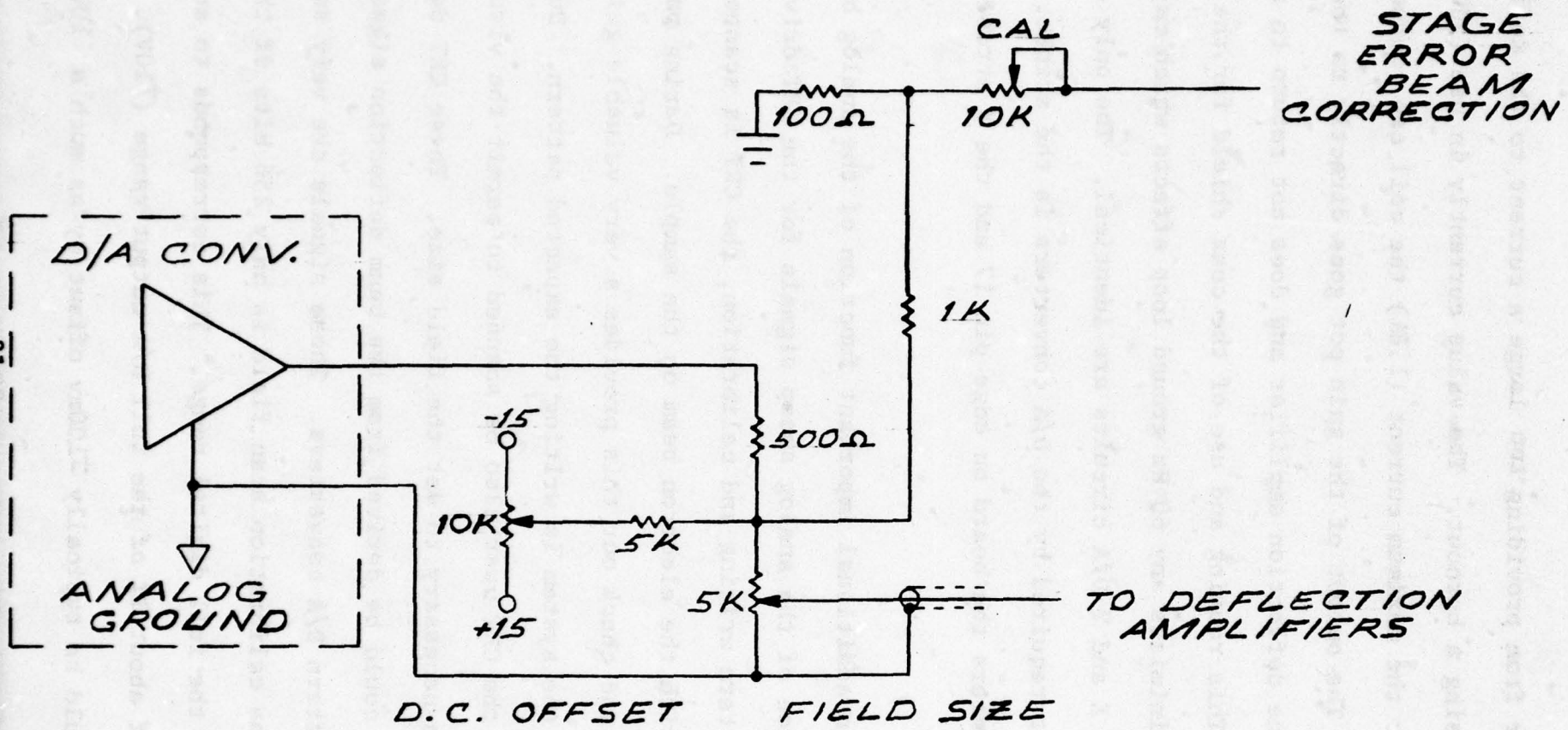


FIGURE 5: ANALOG OUTPUT CIRCUIT

amplifier from providing too large a current to the deflection coil causing a burnout. The value currently in use (500Ω) provides for the maximum current (1.8A) the coil can conduct without damage. The output of the gain pot goes directly to the BNC input of the deflection amplifier and does not return to any circuit board. This routing and use of the coax shield for the signal ground minimizes any 60 Hz ground loop effects which may be present. Both the X and Y D/A circuits are identical. The only other digital input required by the D/A converters is the strobe. The X strobe enters the board on edge pin 17 and the Y strobe on edge pin 38.

An additional important function of the analog board is the generation of the analog sweep signals for the CRT drive. During both pattern writing and calibration, the CRT is scanned syncronously with the electron beam on the sample. During pattern writing and check out this provides a very valuable guide to whether the system is writing the expected pattern. During calibration the CRT must also be scanned to permit the visual identification necessary to set the field size. These CRT deflection signals could be derived from the beam deflection signals of the main pattern D/A converters. These signals are very small, however, since the calibration scan field is only 256 bits of the 16,383 bits of the full digital range. This corresponds to an analog swing of about 1% of the full D/A output range (±10V). These signals would be typically ±100mv offset by as much as 10VDC. The

typical CRT drive signal is approximately $\pm$ 5V for a full screen image. To minimize the noise of the display and eliminate the need of a large amplification factor for the small D/A signals, independent subfield D/A converters are provided for generation of the CRT rasters. These converters are 8 bits and are located on the rear of the board. The circuitry for both X and Y drives is similar so only the X will be described.

Each calibration scan field is 256 LSB's wide or 8 bits. A field is always this size independent of its location (A or B or CH). The only difference between these fields is the d.c. offset. In view of this the fields can be generated by running an 8 bit counter (I.C. 9 and I.C. 10) syncronously with the main (14 bit) X counter, converting this output to a deflection signal with another D/A converter (P.C. subcard 2) and adding d.c. offsets to the waveforms appropriate to the field being scanned. I.C. 9 and I.C. 10 form the basic 8 bit counter whose output is converted by the subcard 2 D/A converter. The counter inputs are the same clock that drives the main X counter and are brought in from the X_3 board. Whenever the X counter is counting, the 8 bit subfield is counting and the converter is generating an output (although this output is only used during the calibration sequence). This subcounter is cleared by the X main counter end of line pulse. The syncronism between the subcounter and the main counter is maintained because both counters count 256 pulses per

line; even though the main counter may have different start and stop values the difference between the start and stop is always 256 bits.

The subfield converter is scaled and D.C. offset by A1. The CRT deflection signal is then routed to the output amplifier and switch. The circuit is shown in more detail in figure 6. The inverting input of the output amplifier A_2 is controlled by 4 CMOS switches, I.C. 6. The switches may connect any or all of the given inputs to the amplifier. If, for example, S1 is closed and S2-S4 are open the subfield drive signal will be connected to A2 and coupled out to the SEM console. If both S1 and S2 are closed, a CRT drive signal is sent out which contains a d.c. offset proportional to the setting of the A set potentiometer. This will tend to shift the CRT raster to one side of the center of the screen. By opening S2 and closing S3, the raster can be shifted to the other side of the screen, thus generating the A and B CRT fields. These fields of course are artificial in the sense that they are not true versions of the sample deflection signals.

Which signal is delivered to the CRT drive depends on the front panel mode selection. The switches are opened and closed according to the information decoded by I.C.'s 1, 2 and 3 which obtain their data from the front panel selection and the rectangle select flip-flop on the Y_2 board.

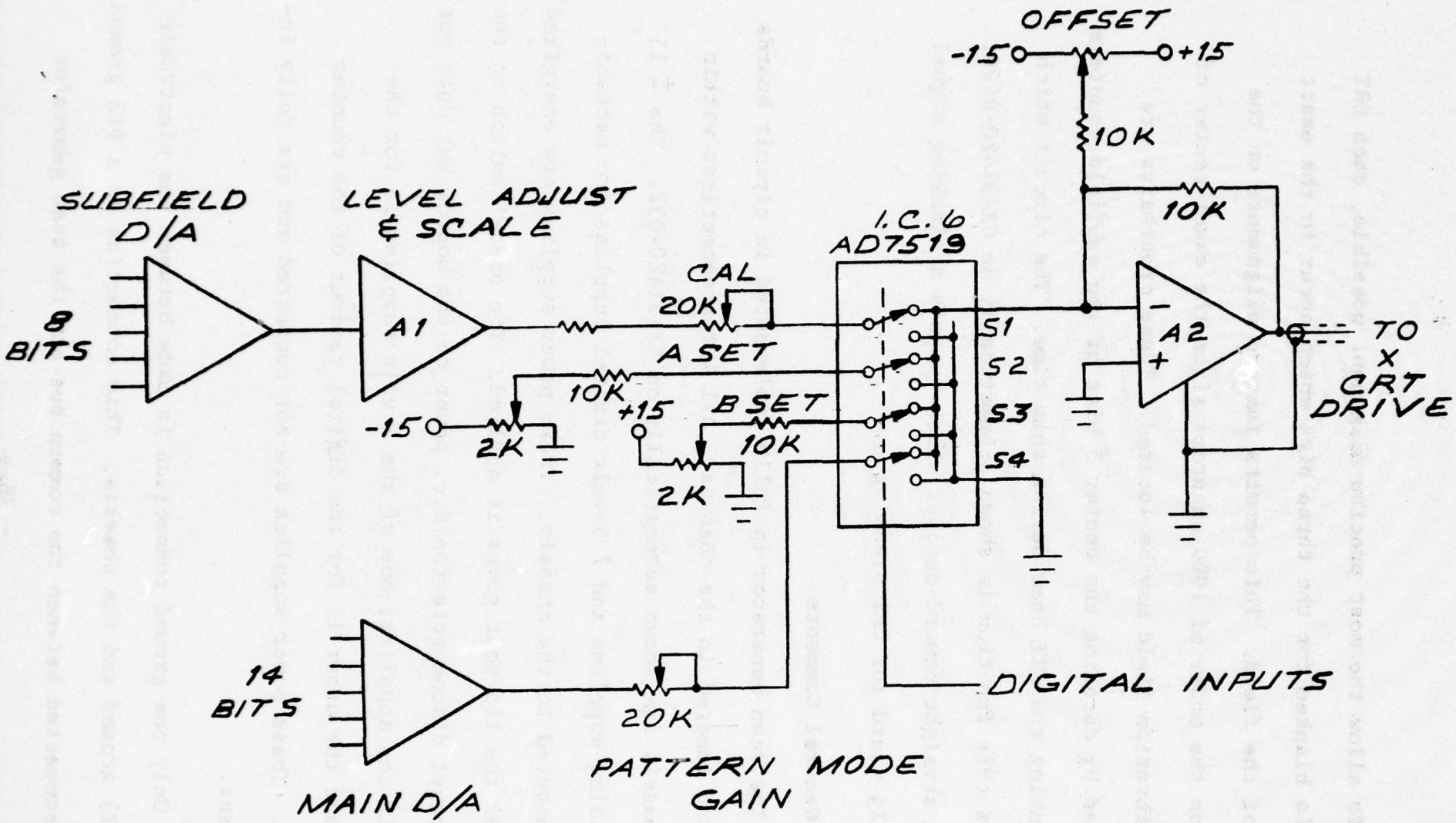


FIGURE 6: CRT DRIVE OUTPUT CIRCUIT

To allow the most precise alignment possible, each CRT raster is blanked for the three bits which occur in the exact center of the field. This permits feature alignments on the sample on the order of 1000 angstoms since the exact center of the calibration field may be located. These crosshairs are generated by decoding the center 3 bits of the subfield counters and blanking the CRT beam during this time. The circuit which performs this function is shown schematically on CX-31420-040B. It is a straightforward decoder which outputs a blanking signal to the X_3 board for CRT blanking.

A.7 General Comments

The scan generator is fully implemented in circuit boards which are located in the chassis. All interconnections within this chassis are shown schematically on EX-31420-032. The $\pm$ 15 volt analog supplies and 2 5-volt digital supplies are mechanically mounted to the chassis. These power supplies are energized whenever the 115 volt power is applied. The on-off switch on the front panel disconnects the d.c. power to the boards but does not turn off the supplies; one of the 5 volt supplies is for the logic and the other is for the digital readout of the counter states. These power supplies are not connected and are fully independent.

Only one ground connection is made between the electronic (signal) ground and the chassis. This connection is a #12 ground braid connected between the common bus and the scan generator

chassis. All of the grounds in the digital chassis are referenced at this point and no other ground connections exist between the signal ground and chassis ground. This ground is joined to the column ground and SEM control chassis ground at this point. No other common connections exist.

B) Digital Stage Control

Similar to the scan generator, the digital stage control houses the systems for positioning the stage and monitoring its motions. The circuitry for managing the tape drive and reading information from the tape is also contained in the stage drive chassis. The interferometer system is an independent subsystem but its output signals are accumulated in the stage control.

B.1 Data Format

All data for writing patterns and manipulating the stage are loaded from the paper tape via the paper tape reader and the tape reader logic. The tape is in 8 bit ACSII code with odd parity. The code listings which are used by the systems are shown in Table 2. Other binary codes exist in the ASCII set which are not used by the system. Certain ASCII characters such as "line feed" and "return" are not recognized by the tape reader and are passed by when they appear on the tape, allowing arbitrary output formatting so that a tape code can be easily read on a teletype. Other characters should be avoided since they

will cause errors in the execution of a program.

The actual codes for the tape programming are contained in bits 0-6 (bit 0 is the least significant) while bit 7 is the parity or error checking bit. With an odd parity code this bit is a one whenever the sum of all the one's in the remaining code is an odd number. The parity bit for the letter C is 1 since three one's appear in the remaining code for the letter C. When the sum of one's is an even number the parity bit is zero.

Three distinguishable codes exist and are recognized as such by the tape reader logic. These codes are data, address, and execute/stop. Which type of information is in a particular block is determined by bits 6, 5, 4 of the word. If bits 6, 5, 4 are 010, then the command is a stop/execute.. Code 101 is for an address and 100 or 011 is the code for a data word. Each line of tape, therefore, contains one parity bit and three code recognition bits. The remaining four least significant bits contain the data in the word.

Only two stop/execute codes are used. They are $ and * in the teletype keyboard. The $ or end of block command instructs the system to operate on the last data loaded into the memories, e.g. move the stage, or write a rectangle. A * commands the system to stop all functions (although it does not turn the instrument or any of its controls off) and the system will not

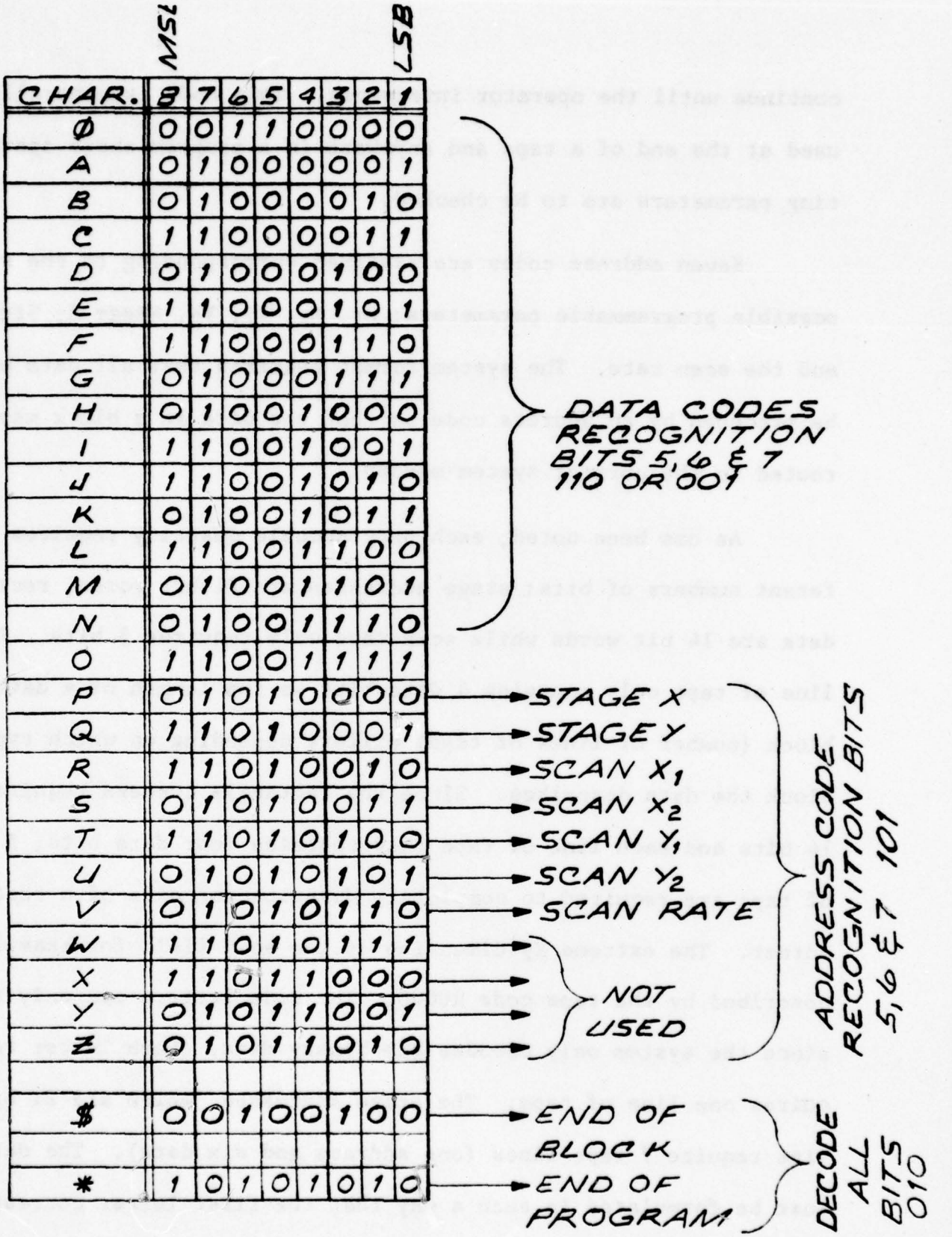


TABLE 2: ASCII CODE LIST

continue until the operator intervenes. This code is generally used at the end of a tape and anywhere in a program where operating parameters are to be checked.

Seven address codes are assigned corresponding to the seven possible programmable parameters: X_1, X_2, Y_1, Y_2, Stage X, Stage Y, and the scan rate. The system format requires that all data blocks be preceded by an address code so that the data in a block may be routed to the correct system memory.

As has been noted, each programmable quantity requires different numbers of bits: stage addresses are 21 bit words, rectangle data are 14 bit words while scan rate only requires 3 bits. Every line of tape only contains 4 data bits so the length of a data block (number of lines of tape) differs depending on which type of block the data describes. Since the rectangle corners require 14 bits and each line of tape only contains four data bits, 5 lines of tape are required to completely describe one axis of a rectangle corner. The extreme X_2 dimension of the scan field for example is described by the tape code R0000. The code letters are only memory since the system only decodes the binary data. Each letter requires one line of tape. The stage addresses, which are 21 bits line require 7 tape lines (one address and six data). The data must be formulated in such a way that the first letter corresponds to the least significant bits while the next letter (i.e. line of tape) contains the next least significant. Since none of the

complete data words are even multiples of four, part of each data word is disregarded. The two most significant bits of the data word for the rectangle corner for example are not used since the word is only 14 bits long and the two most significant are outside of this field. When used as the fourth character of a scan address, the letters B, F, J, and M all have the same value since the last two bits are identical for these letters and they are the only ones used. The 3 most significant bits of a stage address are disregarded while the most significant bit of a scan rate command is disregarded.

B.2 Tape Reader and Logic

The tape is read by a typical commercial 8 track tape reader which uses optical sensors to locate hole/no hole at a particular tape location. Each of the 8 tracks is a TTL level to the tape reader logic. In turn, a new line of tape is advanced when the tape drive receives pulse from the tape reader.

The tape reader logic card is situated in the stage control module and is located at the right end of the chassis. A block diagram of the tape reader logic is shown in figure 7. The tape reader logic performs one major function: reading and distributing the tape data. As noted previously the tape is formatted such that the four LSB's are data, the next three are address recognition, and the MSB is a parity check bit. The logic interrogates and processes these bits differently according to the

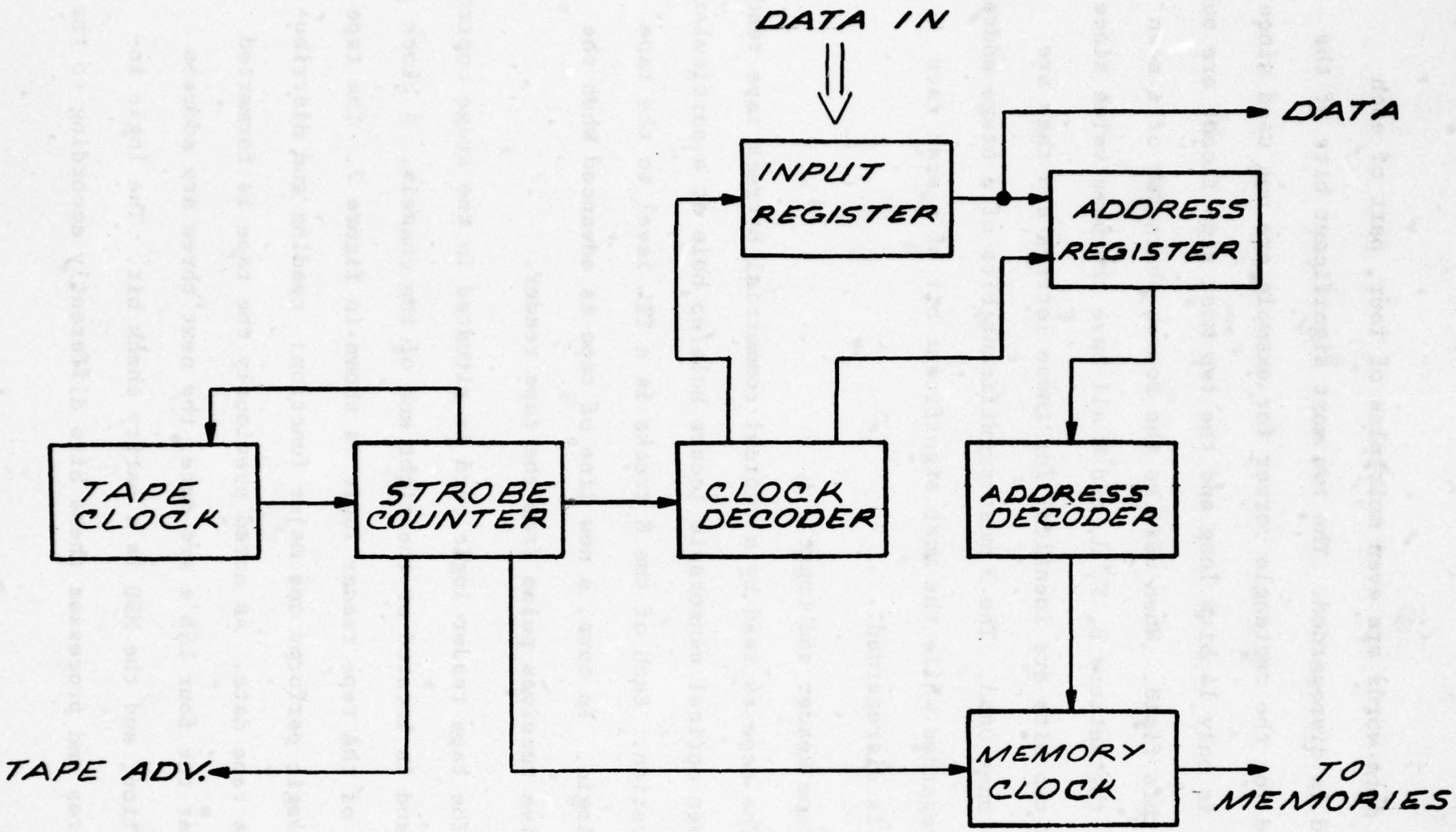


FIGURE 7: TAPE READER LOGIC

function. The circuits operate syncronously at the command of the tape reader clock which operates continuously and is gated into the system when required. The function of the system is most easily understood by following the flow of data off tape and through the tape logic into its particular memory location.

Assume for example that the following two letters appear on the program tape: VC. These letters would of course occupy two lines of tape and the tape would be coded as follows:

Parity	Add	Data	
MSB		LSB	
0	1 0 1	0 1 1 0	V
1	1 0 0	0 0 1 1	C

The parity bit for V (the MSB) is 0 since the number of ones in the code is four, which is an even number.

Regardless of the actual data or address code, all tape data is first loaded into an intermediate buffer consisting of IC 2-1, 2-2, 3-1 and 3-2. The flow would be as follows: The tape would be advanced by a pulse from 4-4-2. This would then present the 8 bit digital code for the letter V to IC's 1-1 and 1-2. These eight gates are transferred by a pulse from 4-4-4 which occurs later than the tape advance pulse by 16ms. This delay assures that the tape has advanced completely to the next line and the data is stable. These strobes (command pulses) are two of six derived from the strobe counter which provides the

timing for the tape reader logic.

Once the input register is loaded, the parity bit is checked for error. The parity is checked by I.C. 4-1 which makes the check when commanded by a strobe from 4-4-6 which occurs 1ms after the load strobe. If a parity error is detected, 6-3-15 is set to one which activates the front panel parity error light. The parity error also causes the reset of 2-6-11 (via 4-4 and 6-5) which terminates the strobe counter sequence by disconnecting the clock through 3-6-6. Thus the tape will not be advanced further without additional operator assistance. Furthermore, the tape reader will remain at the incorrect code so that it may be visually checked by the operator for error. If no error is detected, the strobe counter continues.

The next strobe is generated by 6-6-8 under certain conditions. Three of the inputs to 6-6 are taken from the data input register bits 4, 5, 6 (the address recognition bits). Two inputs of 6-6 are data of bits 4 and 6 and one input is the data of bit 5. When the address code is 010, IC 6-6 is enabled and decodes the third strobe. The 010 address code only occurs for end of block ($) and end of program (*) statements. When enabled, the strobe from 6-6 accomplishes three functions: 1) stops the strobe counter by resetting 2-6-11 via 6-5 and 4-4,2) sets the end of block flip-flop 7-4;3) sets the data ready flip-flop

7-5. If an end of program code is received, the end of program flip-flop is set (7-4-5) via 7-6, 5-3 and 4-2.

The final two strobes only occur when an address or data code is recognized. Strobe 5 (from 4-4-8), when active, attempts to set 6-1-14 and 6-1-11 to one. If the data word is an address then 5-2-6 and 5-1-8 are enabled setting both flip-flops. This allows both 6-2-12 and 6-2-6 to be active. These two gates couple clock pulses derived from strobe 6 (4-4-10) to the data register and address registers. Strobe six is unique in that it actually consists of four pulses which are the last 4 clock counts that fill up the strobe counter. These four strobes shift the contents in the data and address registers to the right four places.

In the example, the code "V" would activate both the data register clock as well as the address register clock since it is an address command. The four LSB's of the "V" code, 0110, which will instruct the system to load the next line on tape in the scan rate memory, are first loaded into 2-2 and 3-2. The four strobe six pulses shift this data right into 3-3 and 2-3 the address register. This data is also shifted out via 5-3-6 to the other sections of the machine but is disregarded since no memory has been ordered to receive it.

The next tape clock pulse sets the strobe counter to zero and the strobe counter sequence begins again. The first strobe advances the tape and loads the code for the letter "C" which is on the next tape line. The strobe sequence will be identical to

that for the V with the exception that the data code in bits 4, 5, 6 will not allow 6-1-11 to be set (by disabling 5-1-8). The 4 strobe six pulses are now routed out via 6-2-8 rather than 6-2-6. This has the affect of leaving the contents of the address register fixed at the last value (V in this case). The contents of this address register are routed to the address decoder IC 1-3. Depending on the 4 bit input code, one of seven output lines is set to zero while all others remain at one. The 0110 is decoded at output 7. With 7 low the scan rate clock gate 1-5-8 is enabled and couples the 4 strobe six pulses to the scan rate memory. Simultaneously the data register clock is running and the data is clocked to the memory via 5-3-6. Since the memory inputs are all connected in parallel, it is the clock when applied which determines which memory receives the data.

In summary, either the data register clock is enabled with or without the address register clock, depending on the word. The tape logic has no way of determining how many lines of tape are read for a particular address and either can occur if the tape format is incorrect. For example, the scan addresses which are 14 bits require 4 lines of tape for the full word. If by error a fifth line contained another data word, it would be loaded into the memory after the correct four lines pushing the 4 LSB's out of the memory.

A typical timing sequence is shown in figure 8.

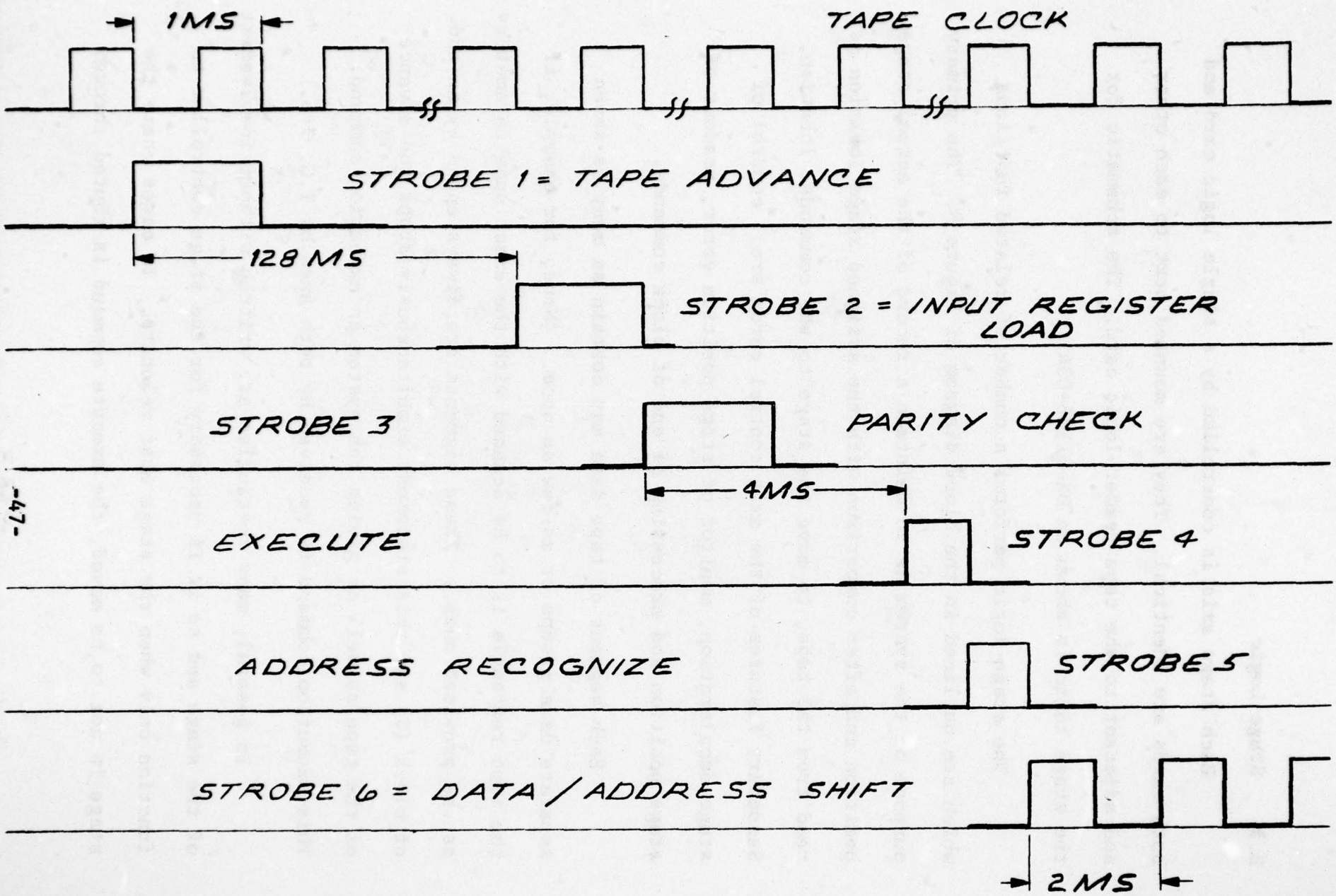


FIGURE 8: TYPICAL TAPE READER TIMING

B.3 Stage Logic

Each stage axis is controlled by a single logic card and both cards are identical. They are mounted next to each other and adjacent to the tape reader logic card. The schematic for the stage logic is shown on DX-31126-034.

The stage logic performs a number of related functions which are outlined in the block diagram of Figure 9. The primary purpose of the system is to maintain a record of the actual stage position and, after comparison with the assigned stage location as read from the tape, to move the stage to the commanded location. Secondary features of the axis control cards are: control of stage deceleration, monitor of stage position error, readout of stage position and processing of end of block commands.

Each segment of tape data may contain as many as seven separate data groups or as few as none. (None, for example, if the same rectangle is to be scanned with the exact same parameters as the previous ones.) These segments are always ended by an end of block ($) and this statement simultaneously stops the advance of the tape as well as giving the system an execution command. This execution command is received by both axes by I.C. 9-5.

In general, many rectangles are written without involvement of the stage and so it is necessary for the stage controller to function only when the stage must relocate. In cases where the stage is not to be moved, the execute command is routed through

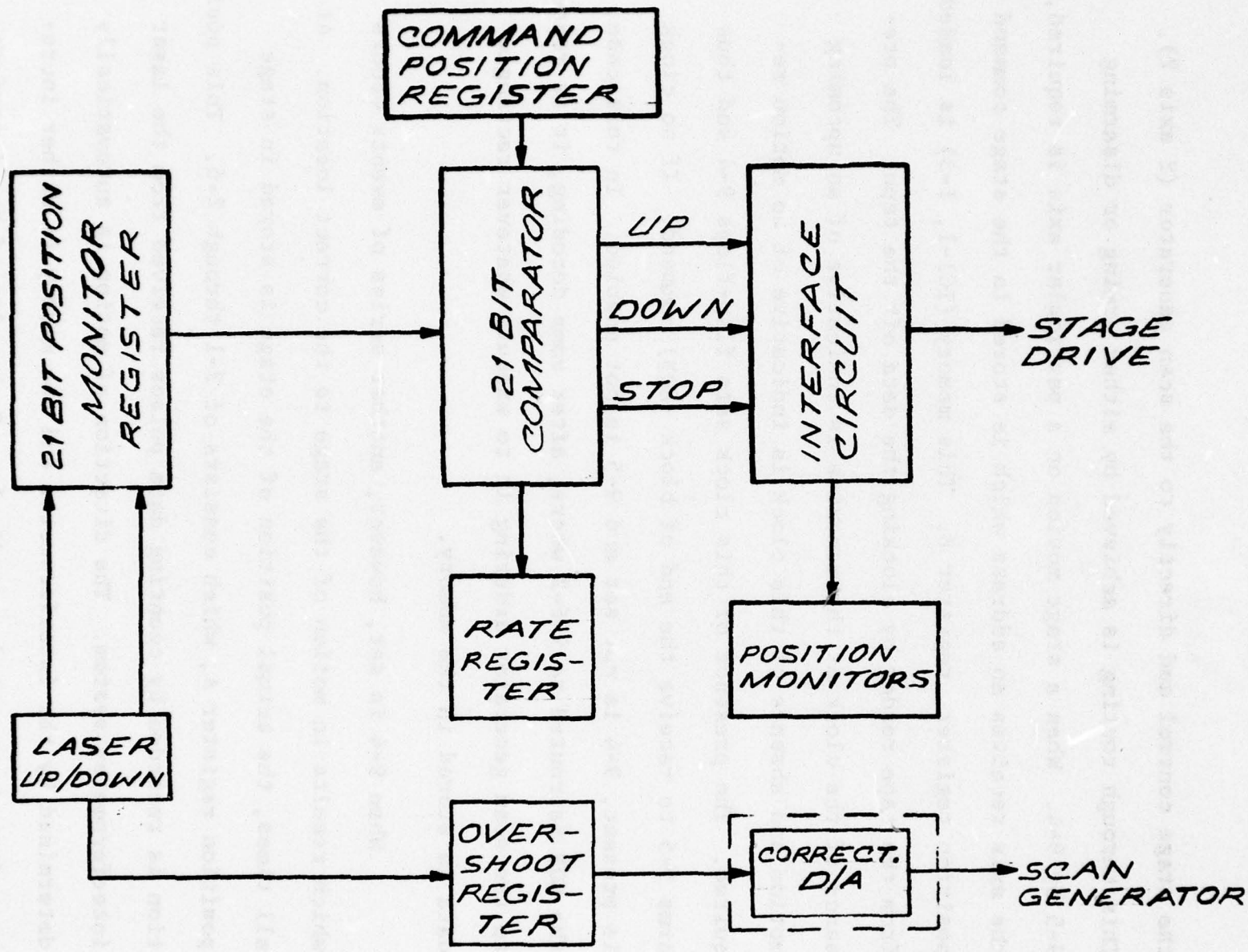


FIGURE 9: STAGE CONTROL BLOCK DIAGRAM

the stage control and directly to the scan generator (Y axis 2). This through routing is achieved by either arming or disarming 9-5 by 9-4. When a stage motion on a particular axis is required, the axis receives an address which is stored in the stage command position register, register B. This memory (IC1-1, 1-3) is loaded from the tape reader by clocking the data off the tape. The presence of the clock at the memories is indicative of an upcoming motion and absence of this clock is indicative of no motion required. The presence of this clock sets flip-flops 9-4 and thus arms 9-5 to receive the end of block (EOB) command. If no clock is present, 9-4 is not set and 9-5 is not enabled. In this case, the EOB is routed to 9-6-2 where, after some decoding, it is routed to the scan generator ordering it to execute whatever rectangle data is stored in the memory.

When 9-4 is set, however, another series of events occurs which results in motion of the stage to the correct location. At all times, the actual position of the stage is stored in stage position register A, which consists of 2-1 through 2-6. This position is recorded by counting data pulses received from the laser interferometer system. The direction of motion is automatically determined by the interferometer and the memory is either incremented or decremented accordingly. Each pulse of the interferometer corresponds to a motion of one-eighth wavelength of the interferometer laser beam. The helium neon laser has a wavelength of .6328 microns so that each pulse corresponds to .0791 microns.

The full motion of the stage (100mm) can therefore be described by a 21 bit word.

When an end of block command is received, the data in Register A (actual location) and Register B (desired location) is digitally compared by IC 3-1 through 3-4, 4-3 and 4-4. If the actual position is less than the desired position (B>A), 5-4 is decoded; if the converse is true (A>B) 4-5 is decoded. In either case one section of 6-1 is set and the appropriate (up/down) signal is decoded by 8-6, 6-4 and 6-5 and transmitted to the stage drive.

The EOB command also causes the stage deceleration flip-flops to be reset (7-1, 8-1 and 9-1). The comparison of the two registers occurs in 4 bit segments. If the motion is so large that the four MSB's are unlike (a motion of approximately 6mm), the stage moves at the maximum rate toward the desired location. As soon as the four MSB's are identical, 7-1-15 is reset and the stage movement speed is decreased by a factor of two. As soon as the next four bits are equal, 7-1-11 is reset and the stage is decreased by another factor of two. The equaling of each successive 4 bits reduces the rate by 2 until the two 21 bit numbers are identical. At this point, 5-5 is decoded and the stage motors are stopped.

While the stage is moving, it is necessary for the interferometer to be operational. If an error occurs in the laser

system, the interferometer pulse converter sends a signal to the card which is received by 8-6-9 and controls the flow of drive pulses to the stage stepping motors. If no errors occur, the stage is supplied with drive pulses from 6-4.

The stage can be moved manually by appropriate switch selections on the front panel. With the auto/manual in manual, pulses from a manually variable clock can be directed to the motors by 6-4.

One additional function is performed by the control chassis consisting of 8-6 and 6-4. To minimize EM interference during pattern writing, the stage motors are de-energized when the stage is not moving. This on command is transmitted by 8-6-8.

The approximate position of the stage is read out as a decimal number on the front panel. This number is actually a count of the number of stage pulses delivered to the motors divided by four, and recorded by IC 4-6, 5-6, 6-6 and 7-6. Since each stage step is 2.5 microns and the counter displays every fourth pulse, the least significant digit of the readout is ten microns (.01 mm).

The stage control card must also monitor the error in stage position. This error occurs because of the finite stage step and the design of the system which does not require a hunting motion to get to the desired location. (This of course would be futile since each stage step corresponds to 31.6 interferometer pulses and the stage cannot therefore exactly reach a 21 bit address.)

This error is monitored by a separate 8 bit register 8-5 and 8-6. The full value of this register would correspond to approximately 20 microns of position error. The register is cleared at the beginning of each stage movement and is incremented/decremented by interferometer pulses as soon as the 21 bit numbers in the A and B register are identical. These counters are enabled in a count sequence for one second after the 21 bit comparison is made by 7-5-15. Once the stage has settled to its final position, 7-5-15 is reset and the error is held in the counter. The 8 bit value is converted to an analog correction voltage by a D/A converter and added to the deflection signal. The reset signal is also routed to the scan generator to begin the rectangle scan.

B.4 Auxiliary Circuits

The fourth card in the stage control contains support circuitry for the operating system and the D/A converters for stage error correction. They are shown schematically on DX-31126-035. This board contains 3 control clocks: 1) tape reader, 2) stage manual clock, and 3) stage automatic control clock. The stage delay timers, Q_3 and Q_4, are also located on this board.

The stage auto clock is down counted by IC 4-6 and 5-6, and the output frequency depends on the input code from the deceleration flip-flops on each stage board.

C) Support System

The remaining electronic components of the electron beam fabrication system consist of power supplies, motor drivers, deflection amplifiers, and the laser interferometer processing circuits. Both the stage control and the digital scan generator have independent power supplies which are contained in their respective chassis. All of the other system components noted above are purchased components and repair of these parts is better referred to the appropriate manufacturer on a module by module basis.

IV. SYSTEM PROGRAMMING

The large number of parameters involved in electron beam lithography make it essential that the electron beam exposure system be as automated as possible. For this reason a programming concept was developed which requires little interpretation by the operator and allows the device designer to obtain program tapes which will produce repeatable results without knowledge of the details of electron lithography procedures. To achieve this goal, the software was designed in a way that raw data about transducer dimensions can be used as program input and a data tape is produced which may be used to directly fabricate a transducer.

This approach was implemented during the contract period. Most of the elements were described as part of an earlier report (1) with the exception of the exposure programming which was refined. Each finger of a transducer is fabricated by a series of superimposed scans so that

the total charge density is equal to an optimally determined value. The concept of cooperative exposure was outlined in detail in an earlier report (1).

In essence, an exposure must be designed which accounts for the locations of nearby elements as well as the size of the feature itself. The actual exposure of submicron lines in a field of other such lines is less than the exposure required if that line is standing alone.

The optimum objective of a full cooperative exposure effects model would be the precise calculation of the scanning sequence and the exposure to achieve the desired line widths and spacings. This model must calculate the effects of adjacent exposures and include this value in the calculation of the exposure for a given element.

The initial goal was to develop a complete model, one which would determine the optimum beam locations as well as the total exposure for a line. For example, it is well established (1) that the total linewidth of a line exposed in resist by the electron beam is typically 3-5 times larger than the diameter of the beam. Further, the width of exposed lines is also a function of the deposited charge. The actual linewidth is the result of the absorption of the minimum absorbed density at the line edge. This absorption function is three dimensional but only the location of the minimum linewidth is necessary when the devices are fabricated using the "lift-off" technique. A number of models discussing cooperative exposure effects have appeared (see (1)).

All of these models calculate an energy/unit volume distribution in the resist and with a knowledge of the development technique to be used are able to predict an approximate developed resist profile. These models are complex and difficult to use, however, since the effects of all parameters are included and the result is an energy distribution curve.

An easier to use result would calculate a minimum charge/unit area. The minimum charge density (dose) is then easily related to the scanning rates and beam currents. To use dose as a guide requires consistency in all other parameters such as KV, resist thickness, and development process. Since these parameters are generally fixed for convenience, a model using dose as the calculated variable is a useful tool.

Cooperative exposure most generally is the exposure at a point in the resist due to the beam intentionally exposing a point at some other locations. This effect is described in detail by the references cited in (1) and is due to electrons backscattered from the substrate as well as electrons forward scattered through the resist. Forward scatters are generally deflected through small angles whereas backscatters are returned through angles from 0^{o} to 90^{o}. Figure 10 shows the paths of these electrons. If there were no scattering, the polymer bonds would only be broken along a straight line path followed by the electron as it is slowed in the area covered by the beam. The scattering, however, causes energy absorption at large distances from the point of the beam and this is a function of the substrate since the number of backscatters is directly proportional to the average atomic weight of the substrate,

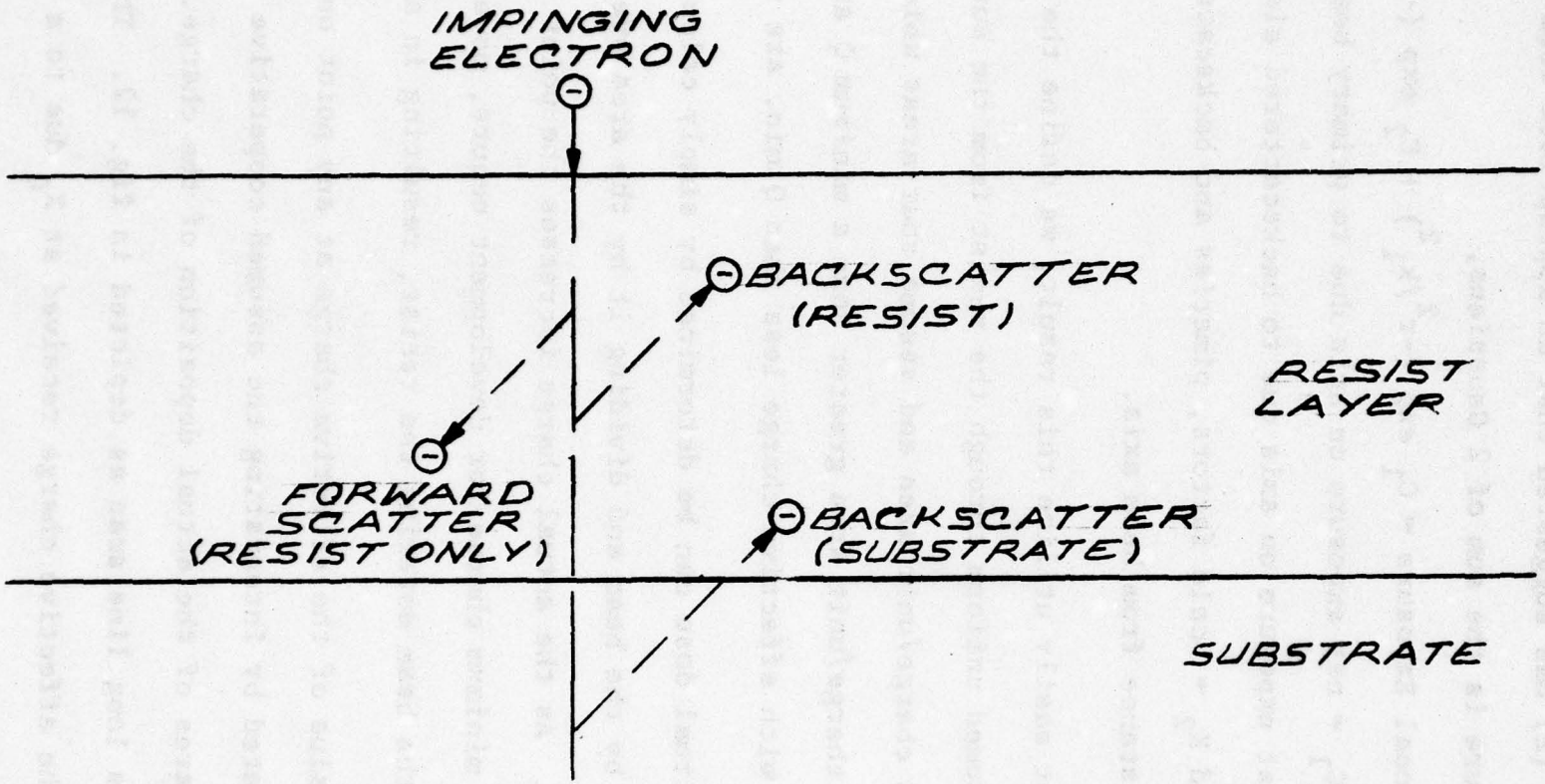


FIGURE 10: PATHS OF SCATTERED ELECTRONS

i.e. one would expect wider lines on LTO than LNO.

Chang (2) has suggested that an appropriate form of the cooperative exposure is the sum of 2 Gaussians.

Fractional Exposure = $C_1 \exp(-r^2/k_1^2) + C_2 \exp(-r^2/k_2^2) = E(r)$ (1)

where C_1 = net exposure on axis due to primary beam

C_2 = net exposure on axis due to backscattered electrons

K_1, and K_2 = Scale factors, pimaries and backscatters

r = distance from beam axis.

To most easily utilize this result, we define the exposure at a point (assumed uniform through the resist from the surface to the substrate) in charge/unit area and assume that areas which have an effective charge/unit area greater than a minimum Q are fully developed and those with effective charge less than Q min. are not developed.

The actual dose can be determined by simply calculating the charge deposited by the beam and dividing it by the area over which it is deposited. As the actual charge increases the point at which Q min, the effective minimum charge for development occurs, moves further from the point of the beam entering the resist, resulting in a wider line.

The value of the effective charge at any point on the surface can be calculated by integrating the assumed cooperative exposure curve over the area of the actual deposition of the charge. As an example, consider a long line scan as depicted in fig. 12. The model must determine the effective charge received at X_0 due to a beam of diameter X_B whose nearest edge is located at X_1. The cooperative exposure curve

is a point function and the net exposure from the edge nearer the point (X_1) is greater than the exposure due to the further edge (X_2).

Actually proper exposures are undercut (see Fig. 11) so that exposure is not uniform through the resist. But for electrode structures evaporated through the resist only the minimum linewidth is important and the undercut is not considered. To find the total exposure:

$$E_{xo} = \int_{X_1}^{X_1 + X_B} E(x)dx$$

where E(x) is given by (1) above.

If we assume the charge deposited by the beam to be uniform (which it is not), then $E(x_d)$ can be interpreted as the area under E(x) curve from X_1 to $X_1 + X_B$. Clearly as X_1 increases this area decreases and for $X_1 >> K_1$, or K_2 the contribution is negligible. At this distance the effects of cooperative exposure are saturated and further exposures at points more distant have no effect on the point of observation.

This calculation can be extended to the case of a uniform long distribution and calculate the net effective dose from an assumed uniform (line) charge deposition. Figure 13 shows the details for the following discussion. The actual exposure at any point X_i is the sum of the incremental cooperative exposures from all points along the (assumed) uniform distribution dx_j. The form of the exposure is -

$$Q(X_i) = Q(X_j) \times F(X_i - X_j)$$

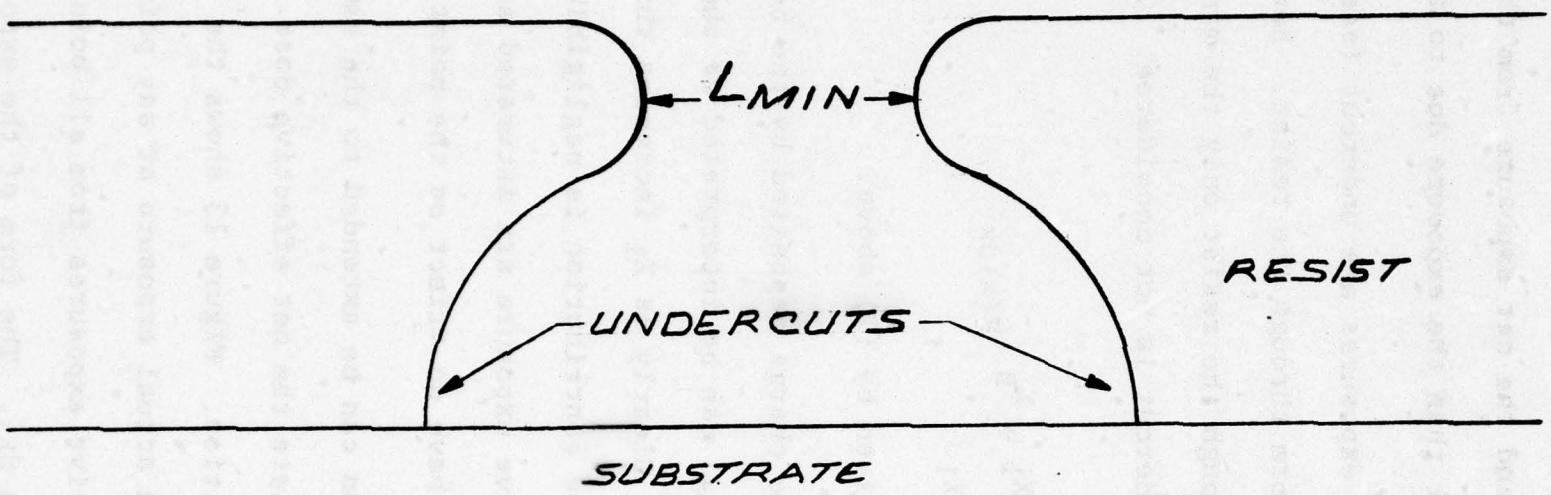


FIGURE 11: CROSS SECTION OF EXPOSED LINE

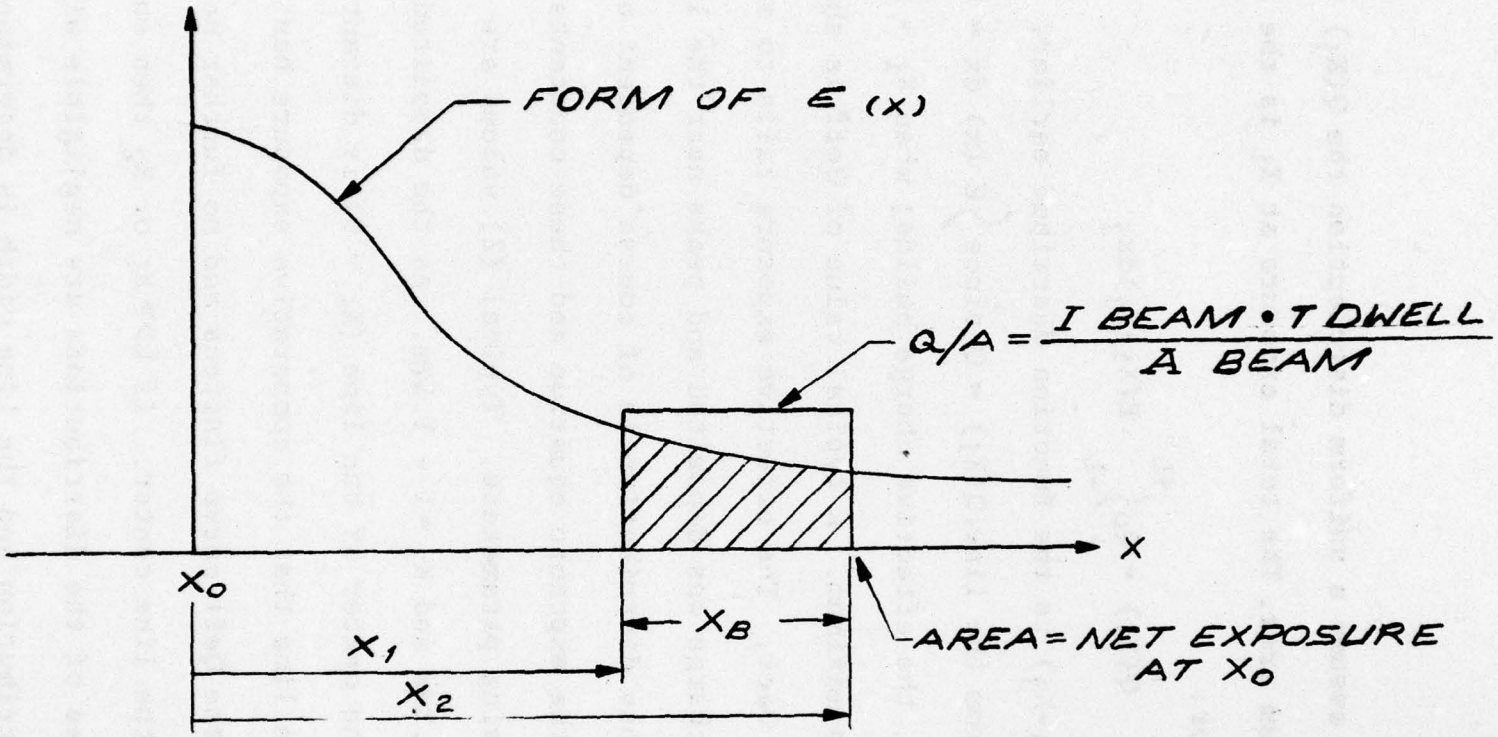


FIGURE 12: COOPERATIVE EXPOSURE CURVE

If we assume a uniform distribution the $Q(X_j) = Q_o$ = i beam x T Dwell/beam area. The total exposure at X_i is the sum of all the X_j increment or:

$$Q(X_i) = Q_o \int_{-L}^{+L} E(X_i - X_j) dx_j$$

where $E(X_i - X_j)$ is the function described earlier. Again for points far away from the line, $Q(X_i) = 0$ since $\int E(x)\, dx = 0$. As the line is approached, the effective charge builds; when $X_i = 0$ net effective charge is a maximum. A typical value of Qeff is shown on the same diagram as Qact. The effective exposure tails to zero far away from where the charge was deposited and peaks near the line center. The shape of this distribution is of course dependent on the four constants in the exposure equation and these constants are functions of the processing parameters. Typical (2) values are $C_1/C_2 = 1.5 - 3$, $K_1 = .1 - .2\mu m$ and $K_2 = 1 - 1.5\mu m$. As the deposited charge increases the center of the line ($X_i = 0$) is distant enough from the edge of the line that the cooperative exposure has saturated and the center of the Qeft curve flattens and no further net exposure is received at the line center. If $L >> K_1$ or K_2 then the drop off in Qeff at the edges of the distributions are negligible with respect to the actual distribution and the line width is determined by the charge distribution and essentially unaffected by cooperative exposure (the saturated case).

A certain minimum Q/A is assumed for adequate development. An example of this is shown superimposed on the Qact and Qeff curves.

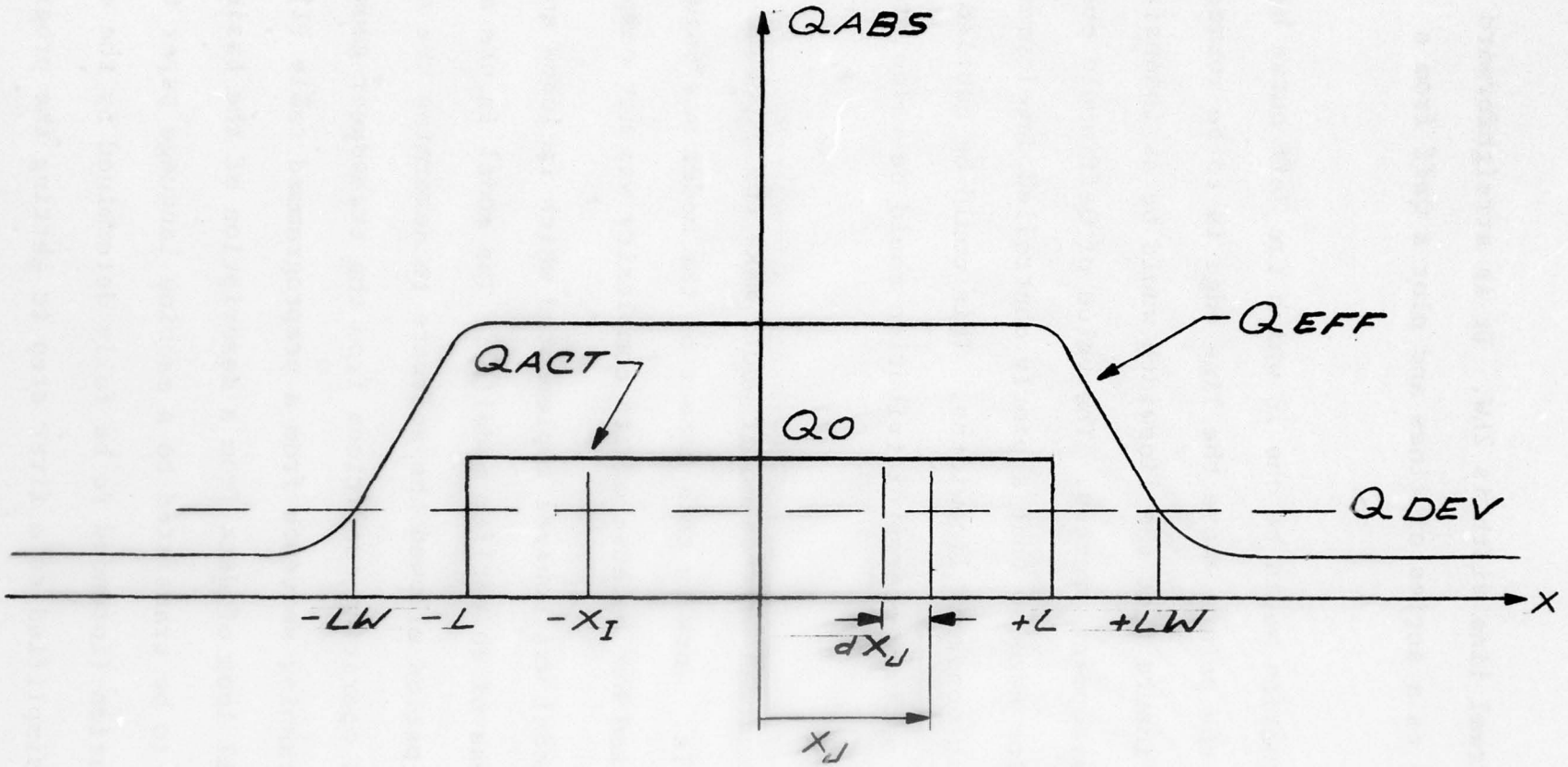


FIGURE 13: EFFECTIVE EXPOSURE DUE TO COOPERATIVE EFFECTS

For this case, the actual line width is 2LW. It is straighforward to apply the calculation to a series of lines and plot a Qeff from a given Qact.

The optimum situation would be one in which the Qeff curve has the largest slope at the points where the line edge is to be formed. This condition would insure that the linewidth would be as insensitive as possible to the deveopment process. The value of Qeff would change rapidly around the line edge so that a poorly controlled development process would maintain constant linewidths. This could be carried one step further and the optimum charge distribution could be calculated to the best Qeff.

A full implementation of this model would make the exposure process as precise as possible. Work on this aspect of the model was begun during the contract period but because of its complexity was not completed.

A simplified model was however implemented which included and extended the basic ideas of an earlier model(1). The model in use at the end of the contract period allowed the software to determine the optimum electron optical operating conditions from the transducer geometry and determine the scanning sequence from a preprogrammed table (1). This permitted a full loop of data from a description of the basic transducer geometry to be translated to a machine language paper tape. The exposure calculation (intended to be fully determined by the calculations above) was simplified as a first step to getting the program operational.

The full cooperative model will account for line overlap, electrodes at the end of a transducer, and any other geometry which might be required. A simplified exposure calculation which assumes the typical circumstances of equal finger spacings and widths was used.

The values used in this exposure calculation assume the following parameters fixed:

1. Electron energy = 20KV
2. Resist Thickness = 4000Å
3. Beam Diameter = LW/3
4. LNO Substrate
5. 60 second develop in 3:1 IPA:MIBK

Variation of any of the parameters effects the validity of the constants used in the exposure calculation. The exposure table (number of scans/finger), devised earlier, was used (1). In this model, the number of scans depends on the linewidth. For large, fully exposed areas, the effects of cooperative exposure are assumed saturated.

To make the exposure curve consistent, the charge density was determined empirically by trial exposures. The exposure for all elements is the actual dimension of the element being exposed. This definition eliminates the inconsistencies which arise in determination of beam diameter so that the actual beam diameter does not become a crucial value in the calculation. The actual beam current and beam diameter are programmed and calculated based on the electron optical considerations outlined in (1). For large areas, such as pads, the

area is simply the length x width; for the electrode elements it is the linewidth. The line exposure can also be expressed as a charge/unit length which is obtained from the charge/unit area calculation by multiplying by the linewidth.

The actual quantitative curve is shown in Figure 14 for the conditions listed above. This curve approximated by an exponential function which was empirically determined from experimented data and published results (2). The form is:

$$\text{Exposure } (C/cm^2) = 10^{-4}\ C/cm^2 (.8 + 1.2 \exp(-L.W./1\mu m))$$

The constant of 1 micron for the exponential provides a good approximate fit to the curve. This curve states essentially that the proper exposure for large feature (pads) is approximately 8×10^{-5} Coul/cm^2 and that for an exposure of 1 micron fingers requires an exposure of 1.2×10^{-4} Coul/cm^2 or an increase of approximately 1.5 times. This result is only valid for the specific conditions of exposure listed above.

It is difficult to make the electron beam completely free of spurious deflections, and in fact this problem presented considerable difficulty during the first contract and elimination of spurious deflections was a major goal. Although spurious deflections cannot be completely eliminated, their effects can be minimized by integrating the exposures as long as they are not in phase with the scanning process (which is the case since these phenomena are associated with the 60Hz

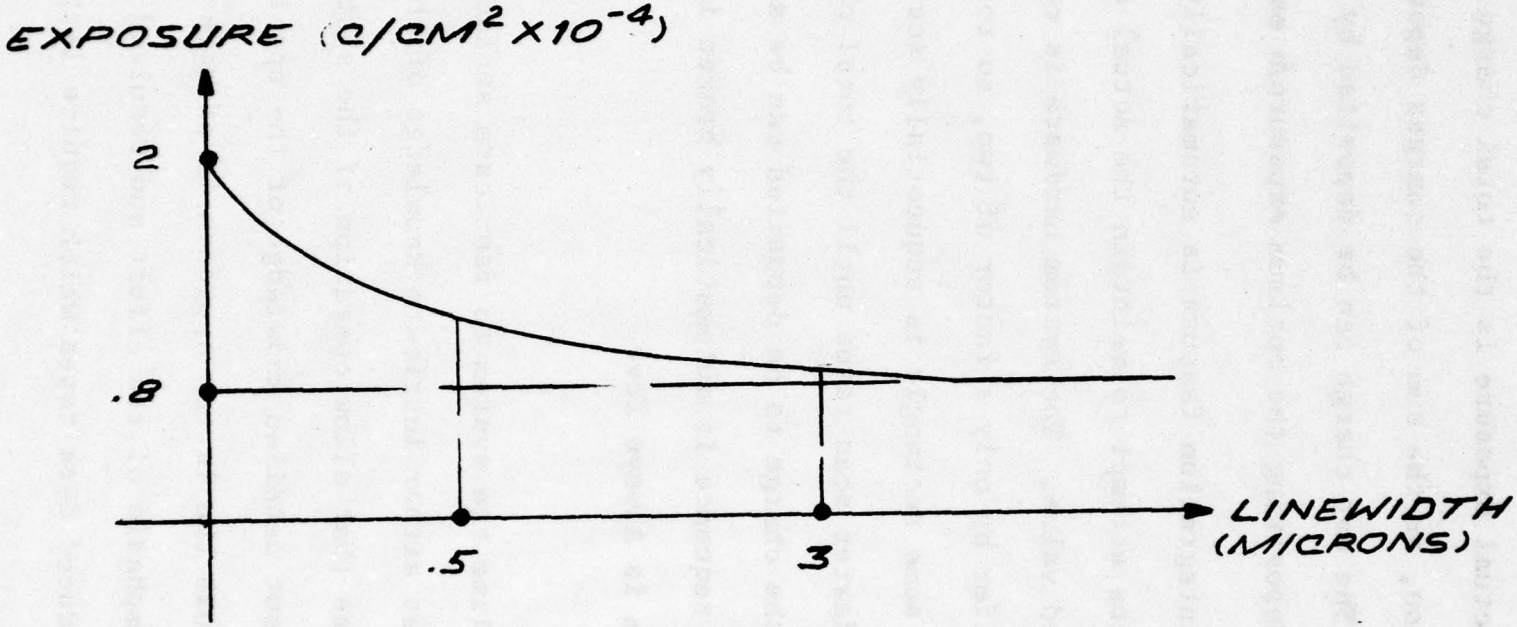


FIGURE 14: OPTIMUM EXPOSURE CURVE

power lines). The actual exposure is the total charge deposited at a particular location, or the sum of the charges deposited with each pass of the beam. The net charge can be deposited by scanning the location n times, depositing the optimum exposure/n each time.

This charge integration feature is automatically accomplished by the program in its attempt to maintain the actual exposure within 2% of the calculated value. The system hardware is capable of handling exposures which differ by only a factor of two, so to achieve a desired exposure the same rectangle is sequentially scanned at progressively faster and faster scan rates until the total charge is deposited. In the event that the charge to be deposited can be achieved in less than 3 passes, the sequence is automatically broken into fewer passes so that the minimum is always five.

V. RESULTS

To fully utilize the system to fabricate surface acoustic wave transducers requires either intricate knowledge of the fabrication procedures or guidlines that allow operation of the system which permits its operation without detailed knowledge of the specifics of electron lithography. Beacuse the latter approach is of more general value, it was the major emphasis of the effort and resulted in a programming approach which produced data tapes which require little or no operator interpretation.

To allow the program sequences to be used effectively, the number of parameters in the process was limited and held constant. The

details of these parameters were outlined in (1). Proper exposure requires the following parameters:

1. Resist Thickness = 4000$\mathring{A}$
   a) Obtained by spinning 4wt% PMMA in AZ thinner for 30 sec. on LNO substrate.
2. Exposure Voltage = 20KV
   a) Chosen to optimize the compromise between backscatter effects and electron column performance.
3. Metallization = 200$\mathring{A}$
   a) Necessary for electrical contact to the electrically insulating SAW substrate.
4. Development - 60 sec. in 3:1 IPA:MIBK mixture.
   a) A relatively weak developer which permits some inaccuracy in the development.

With these parameters fixed, the optimum relation for exposure of equally spaced lines was determined as was shown in Figure 14.

The actual operational details of the system are not of general interest and have been included as a separate memorandum under separate cover. Figure 15 shows a typical example of a specimen data sheet on which are recorded the operational parameters of an exposure. The values in the blanks are the standard operational parameters which are kept fixed from exposure to exposure. Details of system maintenance are also not of general interest and these have also been included as a separate memorandum.

ELECTRON BEAM MICROFABRICATION SYSTEM

DEVICE EXPOSURE DATA

Sample No:_____

Requestor:_____

Date:_____

Sample Description:_____

_____

Sample Orientation:_____

Program:_____ Scan Rate:_____

Pattern:_____

Resist/Solvent: / Batch:_____

Spin Rate: 3000 Time: 30 Sec

Prebake:_____ Premetal: 2000$\overset{\circ}{A}$ Al

Vacuum System:_____

SEM Resolution:_____ Last Maintained:_____

System Cal -Xgain:_____ Ygain:_____ Xctr:_____

Yctr:_____ Beam Corr Cal - Xbeam:_____ Ybeam:_____

KV:_____ Gun Emission - Start: 50 a End:_____

Specimen Current - Start:_____ End:_____

Spot Size:_____ Focus Mag:_____

Charge Density:_____ C/cm_____ C/cm^2

Apertures - Final:_____ Col: 300 Gun: 300

Developer: 3:1 / IPA:MIBK for 60 Secs

Line Length: (14 1b.)_____ Line width:_____

Post bake:_____ $^{\circ}$C for_____ hrs.

Post metal: 200$\overset{\circ}{A}$ Cr, 800$\overset{\circ}{A}$ Al

Striping:_____ for_____ secs.

Comments:_____

_____

The major emphasis of the second phase of the contract was the refinement of the system operation and training of personnel. The early efforts at device fabrication revealed system problems which would preclude the fabrication of the transducers for which the machine was intended. The two major problems that existed were: poor stability of the beam current and spurious deflections of the beam making high resolution exposure impossible.

It has been noted earlier (1) that high resolution electron beam exposures require a tight control on exposure. This control requires that the exposing electron beam maintain a stability of approximately 1% over the entire exposure time which may be up to a few hours. Early efforts with the original tungsten source proved futile since long warm-ups (over 1 hour) were required for moderate stability (2-5%/hour) and even after extensive warmups, the beam was not stable enough as the filament aged. Further the stability varied widely since the beam stability is a sensitive function of the position of the filament with respect to the Wehnelt cap and varies from filament to filament. To get any reasonable stability requires changing of filaments on the order of every 10-15 hours of operation. This filament exchange is usually accompanied by an extensive cleaning process which typically requires 4-6 hours. This difficulty prompted the initiation of the installation of a new electron gun system which utilized a LaB_6 cathode. A number of articles have appeared in the literature (see (1)) and the field experience of LaB_6 cathodes has been excellent. Because of their

mechanical mounting and their better electron emission characteristics, these cathodes provide not only a more stable beam but a beam which is approximately 5-10 times brighter than a tungsten source.

The installation of the source required, unfortunately, approximately six weeks of machine downtime, since the entire upper column had to be replaced to accommodate the local ion pump which is necessary for LaB_6 operation. This new pumping arrangement provides a considerably cleaner vacuum environment which contributes greatly to the increased stability of the source. Unfortunately a number of complications arose during the installation that contributed to more downtime than was anticipated.

Once installed and operating successfully the beam current stability was increased by a factor of 5 to approximately .5%/hour. Brightness of the source was not measured empirically, but similar electron optical operating conditions to the tungsten gun produced electron beams with approximately 5-10 times the current at a comparable spot size.

This installation was very successful and resulted in considerably less operator monitoring of the system.

The problem of 60Hz interference was attacked at the end of the earlier contract period primarily by the regrounding of the entire system to eliminate the performance degredation due to 60 Hz ground loops and poor signal grounds and returns. As reported earlier, this reduced 60 Hz line ripplies to approximately $1500\overset{\circ}{A}$ peak to peak and made possible fabrication of devices with line widths down to $5000\overset{\circ}{A}$. Further

attempts to eliminate residual 60 Hz interferences were the installation of a Mu metal lens magnetic shield and the complete regrounding and isolation of the A.C. power distribution system. The new wiring configuration is shown in Figure 16. Two separate line isolation transformers are used to distribute 60Hz power to the system. A single 208 volt transformer provides power only for the diffusion pump heater and has no reference to the earth ground system. This floating secondary prevents any 60Hz current from flowing in the system frame due to the leakage of the diffusion pump heater which is not perfectly insulated from the diffusion pump body.

The 115 volt power requirements are served by the second transformer whose 230V secondary is broken into two 115V circuits. These circuits are used to drive all of the power supplies in the system and has its low voltage leg referenced to a three pole earth ground system. This arrangement assures that the system is maintained at earth potential and is isolated from power line transients which occur due to other equipment on the same 115V circuits.

The final problem of magnetic shielding due to stray magnetic fields in the vicinity of the electron beam is more difficult to control. The entire length of the column from the gun to the final pole piece is Mu metal shielded and the magnetic lenses themselves act as shields. The area outside the final lens between the final lens and the sample is not well shielded, however, and a shield was designed to protect this area. The arrangement of this shield is shown in Figure 17.

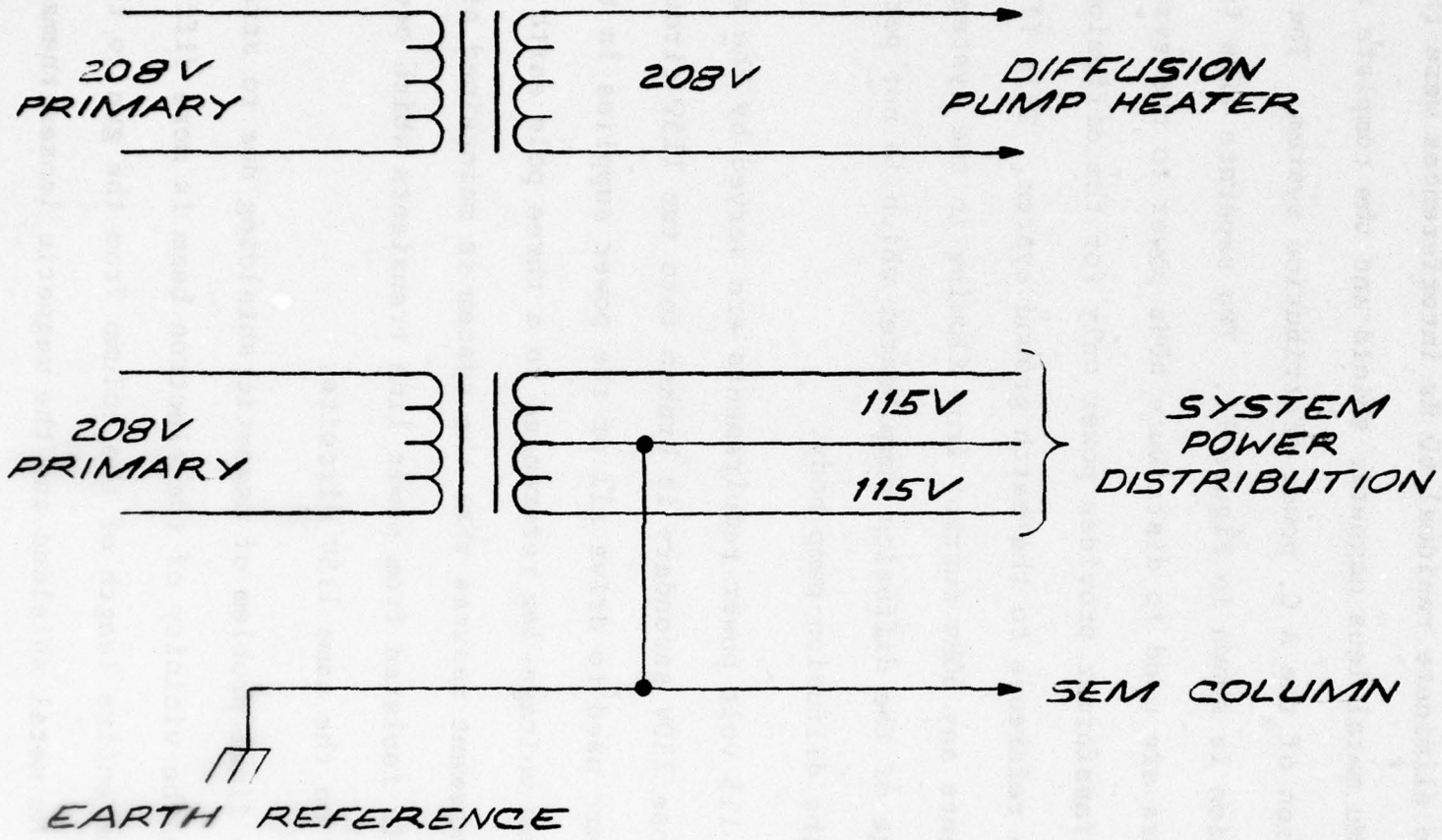


FIGURE 16: 60Hz POWER WIRING

The shield was designed during the contract period but not received and installed until after the contract ended.

The improvement in 60Hz performance and edge resolution is shown in Figure 18, which is a section of a device with line widths of 7000$\mathring{A}$. No noticeable edge ripples are observable.

A major vacuum failure occurred during the contract period which required approximately 2 weeks to repair. Although this was unfortunate, considerable training experience was gained by Air Force personnel in system maintenance. Approximately 35% of the contract effort was dedicated to training of the personnel who will operate and maintain the system. This proved to be very valuable since the instrument is very complex and requires considerable maintenance for successful operation.

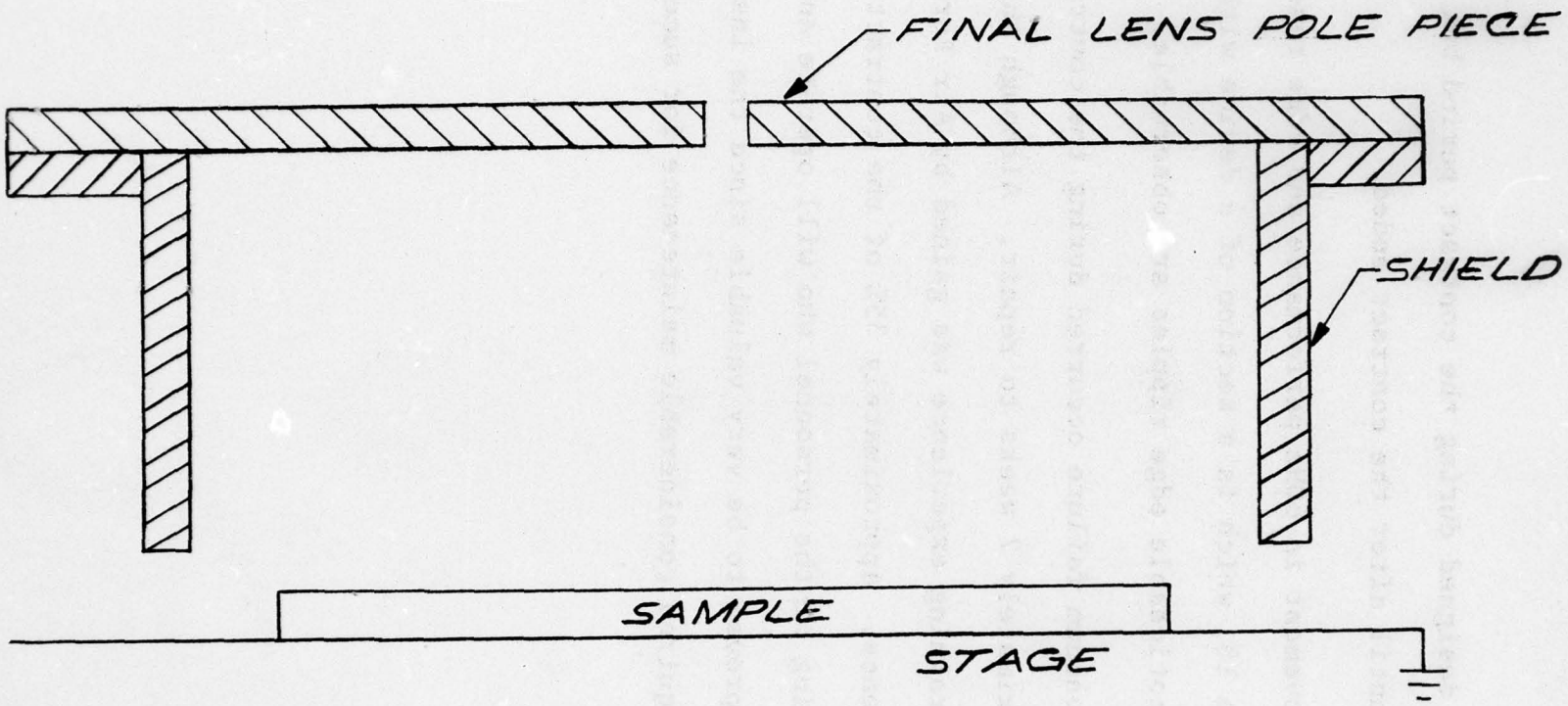
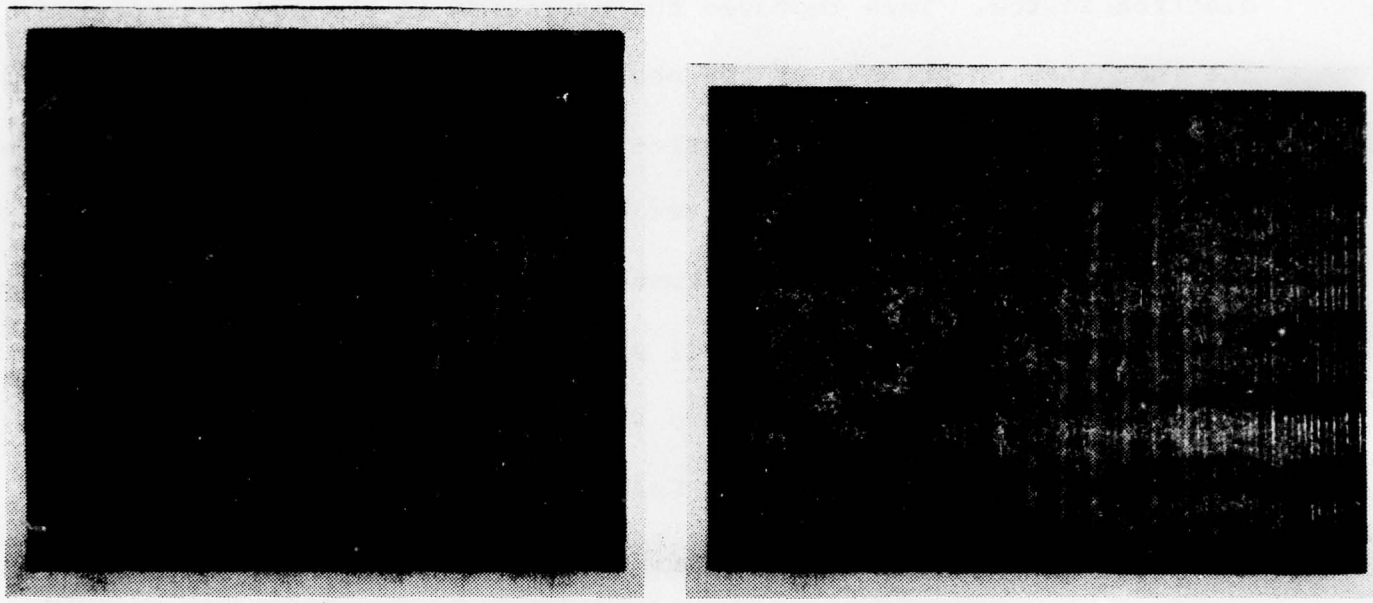


FIGURE 17: SHIELD ARRANGEMENT



OPTICAL MAGNIFICATION = 1300X
LINEWIDTHS = 7000$\overset{\circ}{A}$

FIGURE 18 7000$\overset{\circ}{A}$ DEVICE

VI. FUTURE MODIFICATION

The earlier report detailed the recommended system modification that would allow the better utilization of the equipment. One of these suggestions was implemented with the installation of the LaB_6 electron source. This improved the operation of the gun as expected. The increased brightness of the new source produced 5-10 times the current in beams of comparable size to those from the original tungsten gun. This improvement is only reflected as an overall speed improvement of a factor of two, due to the limited response capability of the deflection electronics. To achieve the full speed capability offered by the new source, the deflection amplifiers should be replaced by a wider band, high slew rate type such as the Celco MRDA-20.

The improvement in gun stability with the LaB_6 source is excellent but the remaining elements of the column (lenses and centering coils) should be redesigned for higher d.c. stability and eventually integrated into a feedback system to keep the electron beam centered on the axis and achieve the ultimate in current stability.

System flexibility could be increased considerably if the scan generator were redesigned around a microprocessor. This would permit implementation of such desirable features as fully compensated, cooperative exposure effects (by varying scan rates within an element), automated system alignment, and memorization of the row data required to produce device patterns. (Most easily accomplished by expanding the memory capability of the system).

The stage control should be modified to permit the laser interferometer system to operate more continuously, as well as in a self checking mode. The hardware delays associated with stage motions should be eliminated when stage movements are not required.

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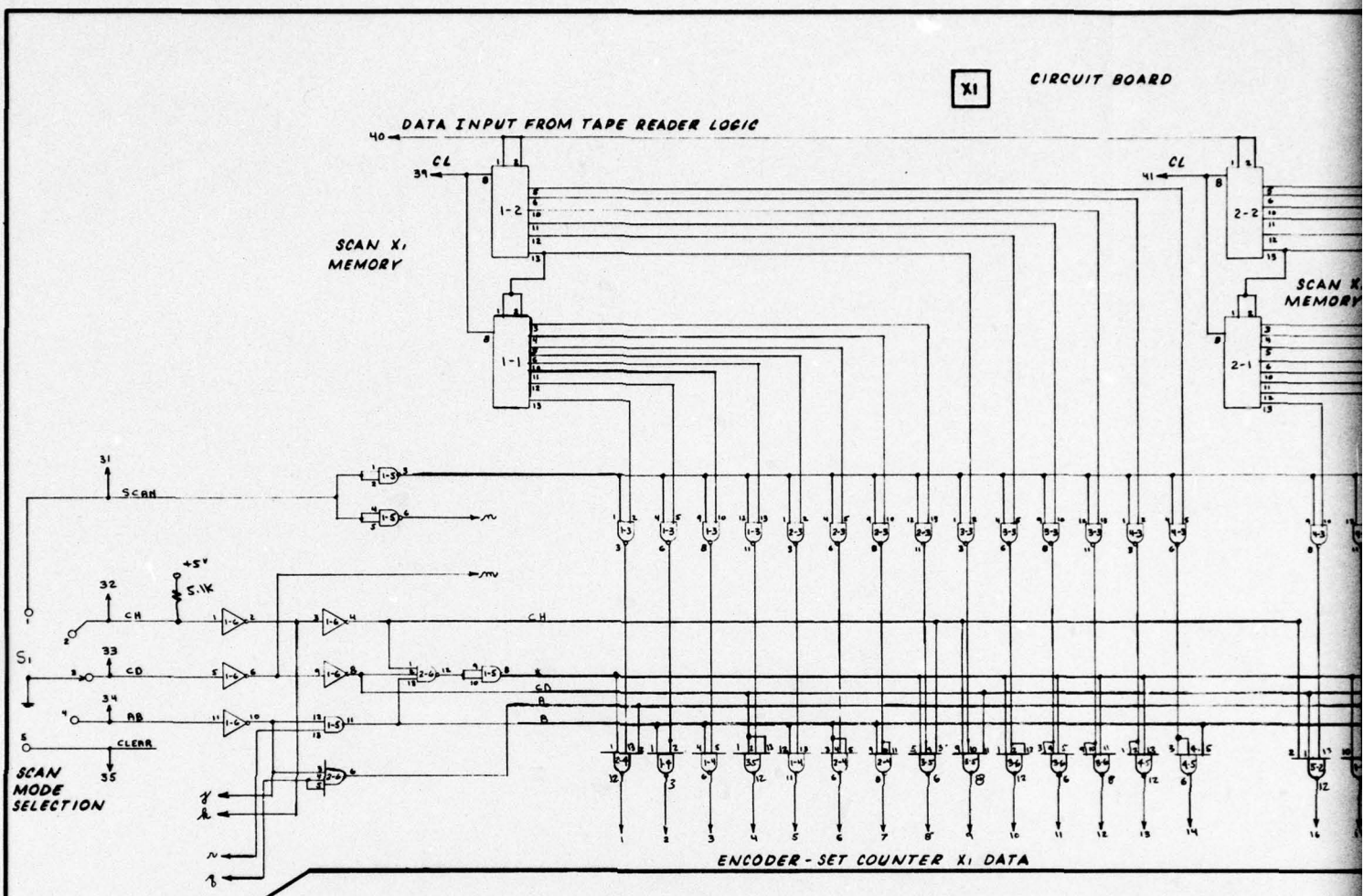
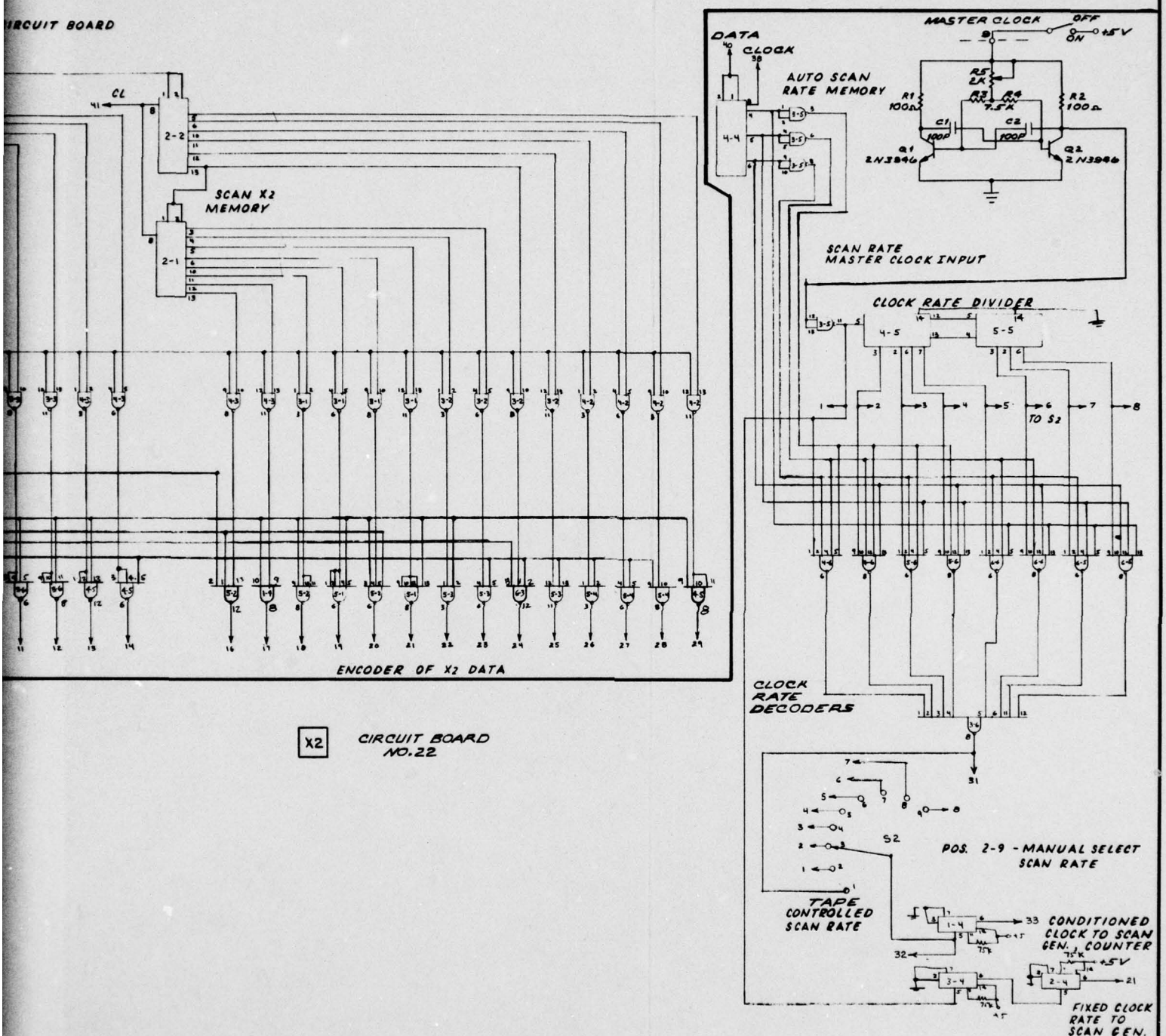
2. Chang, T.H.P., "Proximity Effect In Electron-Beam Lithography", J. Vac Sci & Tech., 12, 1271 (Nov.-Dec., 1975).

3. AMR 1000 Scanning Electron Microscope Operators Manual and AMR 1000 Service Manual, Advanced Metals Research Corporation, Bedford, Mass.


X1
CIRCUIT BOARD
DATA INPUT FROM TAPE READER LOGIC
40
CL
39
41
SCAN X1 MEMORY
1-2
1-1
2-2
2-1
SCAN X
MEMORY
31
SCAN
32
CH
+5V
5.1K
S1
33
CD
34
AB
CLEAR
35
SCAN MODE SELECTION
CH
CD
A
B
ENCODER - SET COUNTER X1 DATA



X2 CIRCUIT BOARD NO. 22

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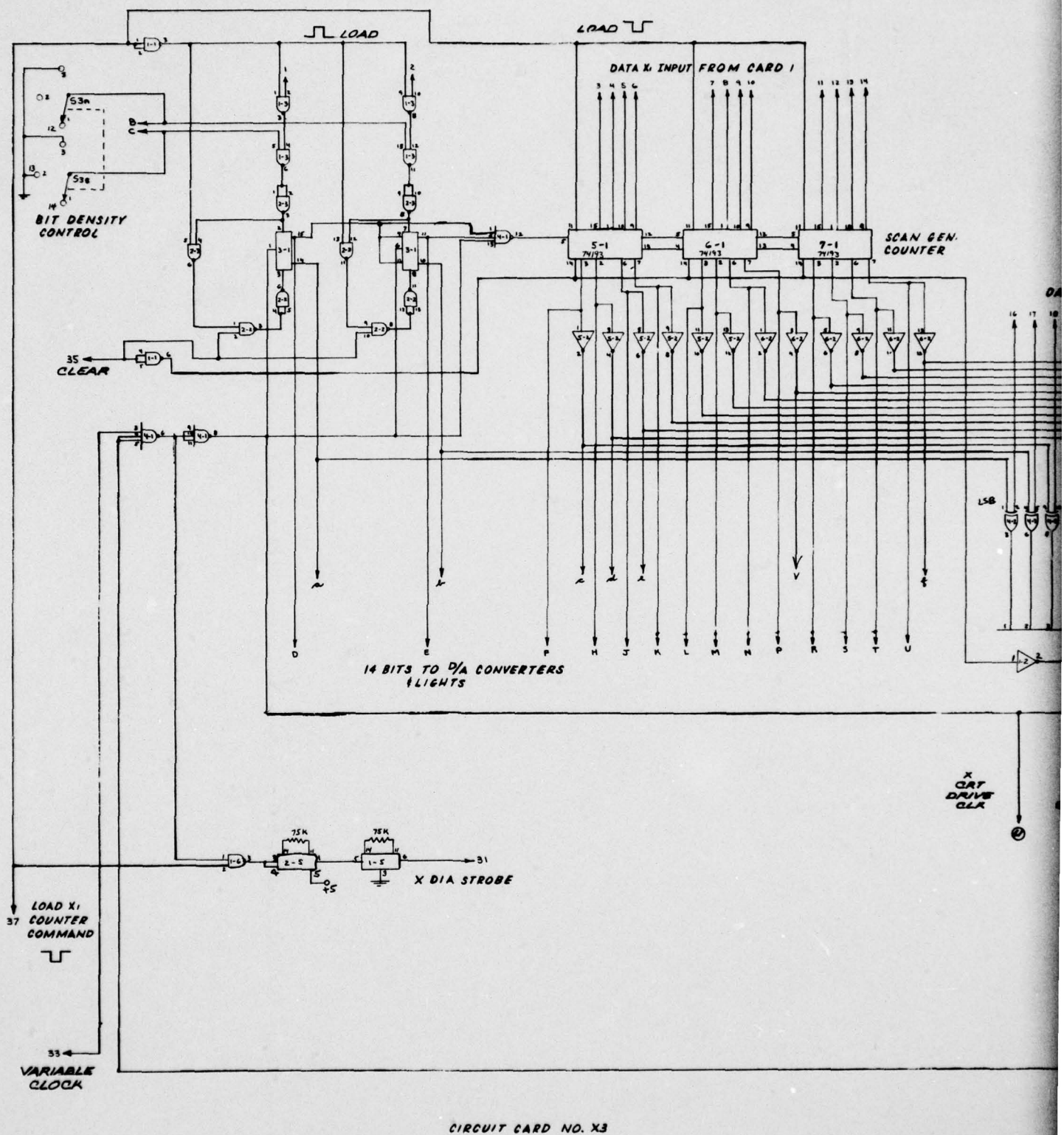
		UPDATE	REMARKS	TOLERANCES (EXCEPT AS NOTED) DECIMAL ± .005 FRACTION ± 1/64 ANGULAR ± 1/4° REMOVE ALL BURRS	DWN. W.R. DATE 8-74 APP. DATE	TITLE SCAN GENERATOR X AXIS - 1 & 2 MATL. MICROFABRICATION SYSTEM			
		8/6/74	DATE	NEXT ASSY	SCALE	NO REQD	REV.	NO. DX-31420-036	



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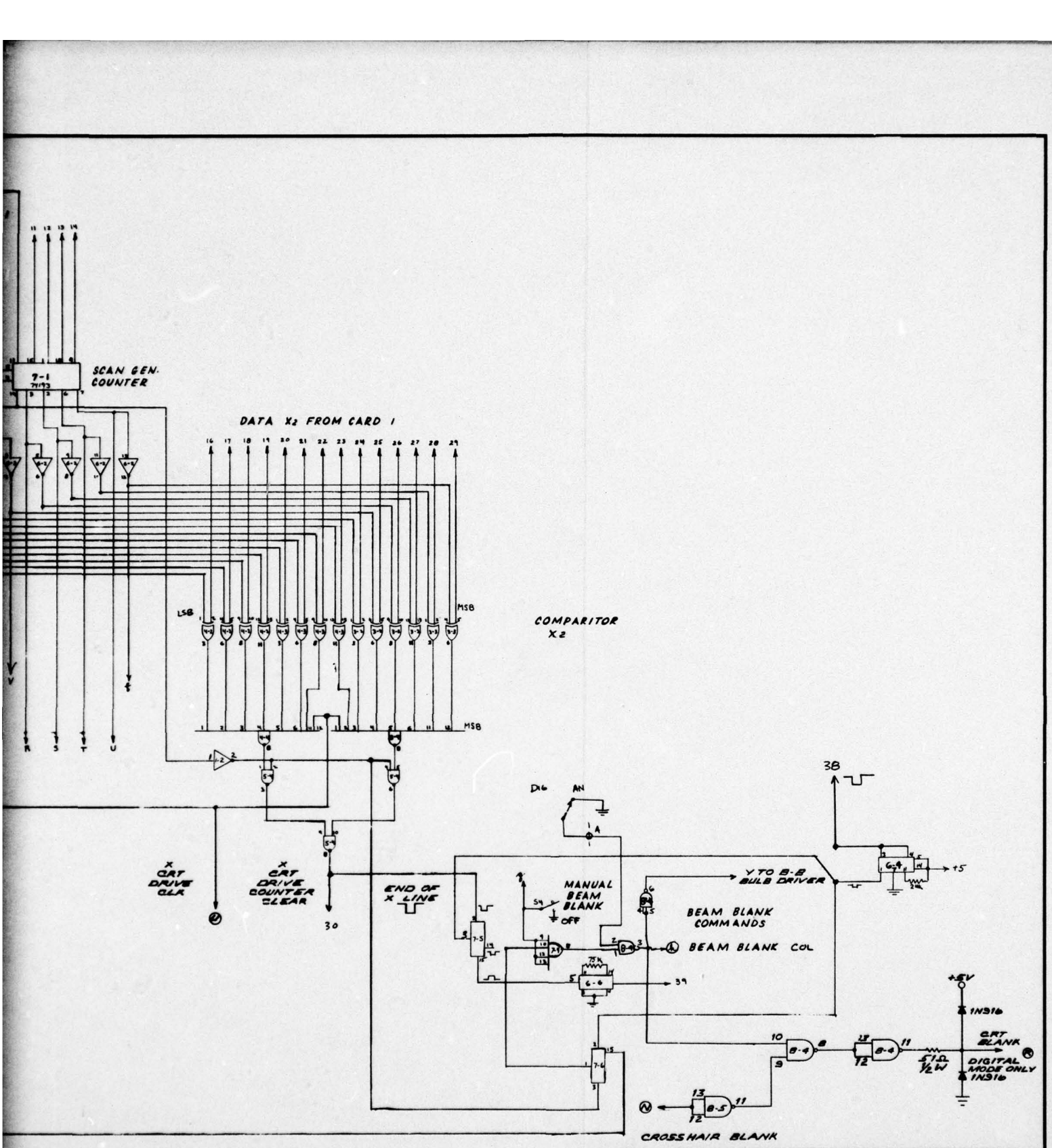


REV.	REMARKS	DATE
A	DRAWING UPDATE	1/2/74
B	UPDATE	4/5/74
C		7/8/74

AMR — ADVANCED METALS RESEARCH CORP. BURLINGTON MASS.

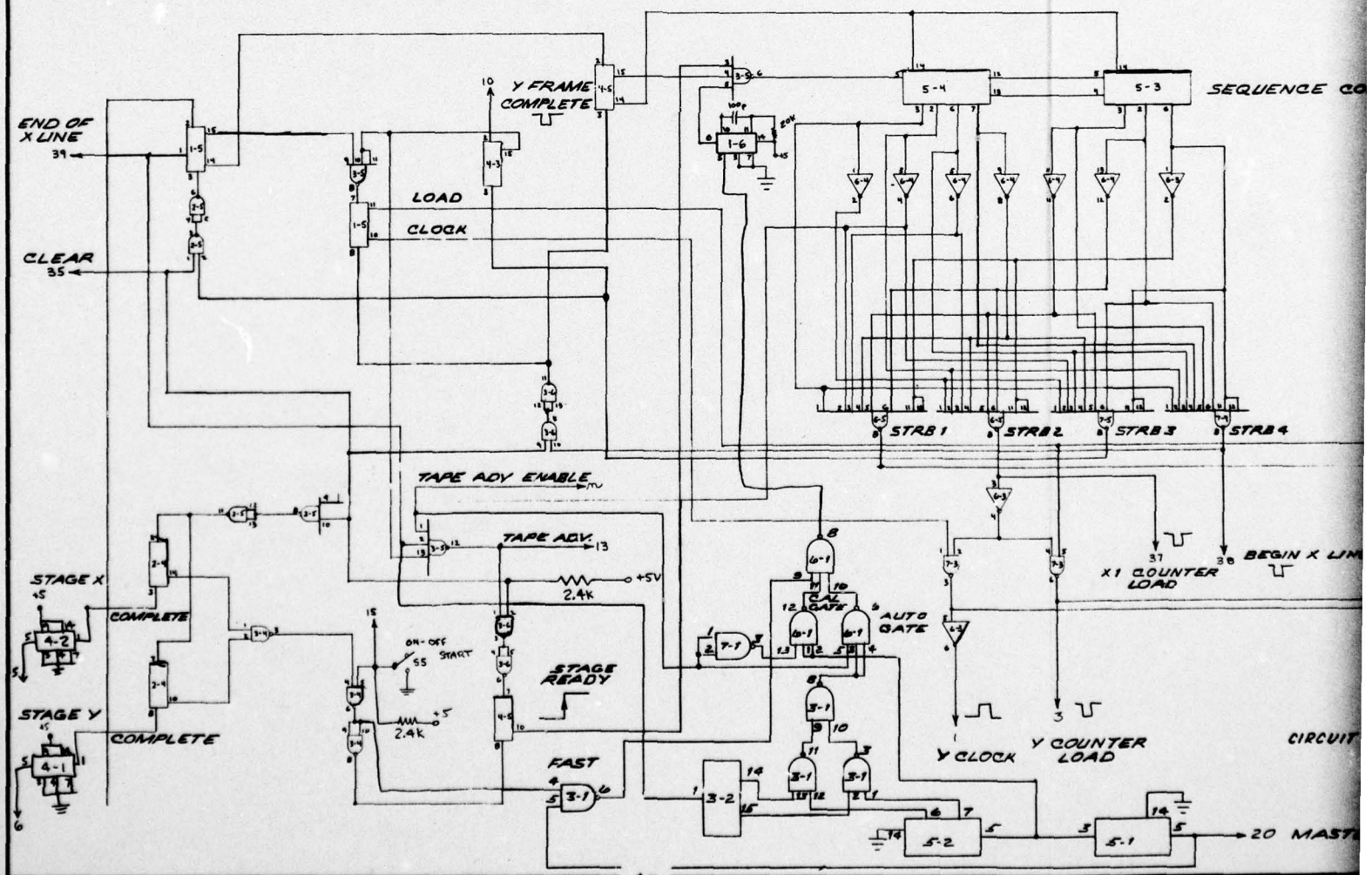
TOLERANCES (EXCEPT AS NOTED): DECIMAL ± .005; FRACTION ± 1/64; ANGULAR ± 1/4°; REMOVE ALL BURRS

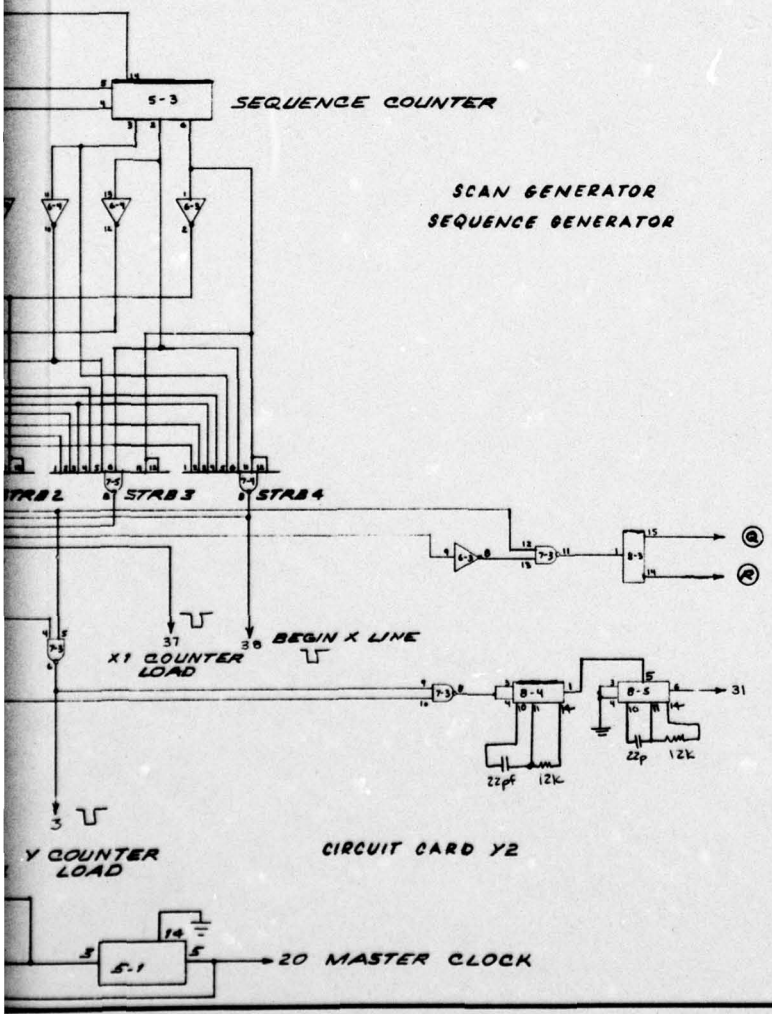
DWN. W. R. — DATE 8-74 — APP'D — DATE

TITLE: SCAN GENERATOR - X AXIS - 3

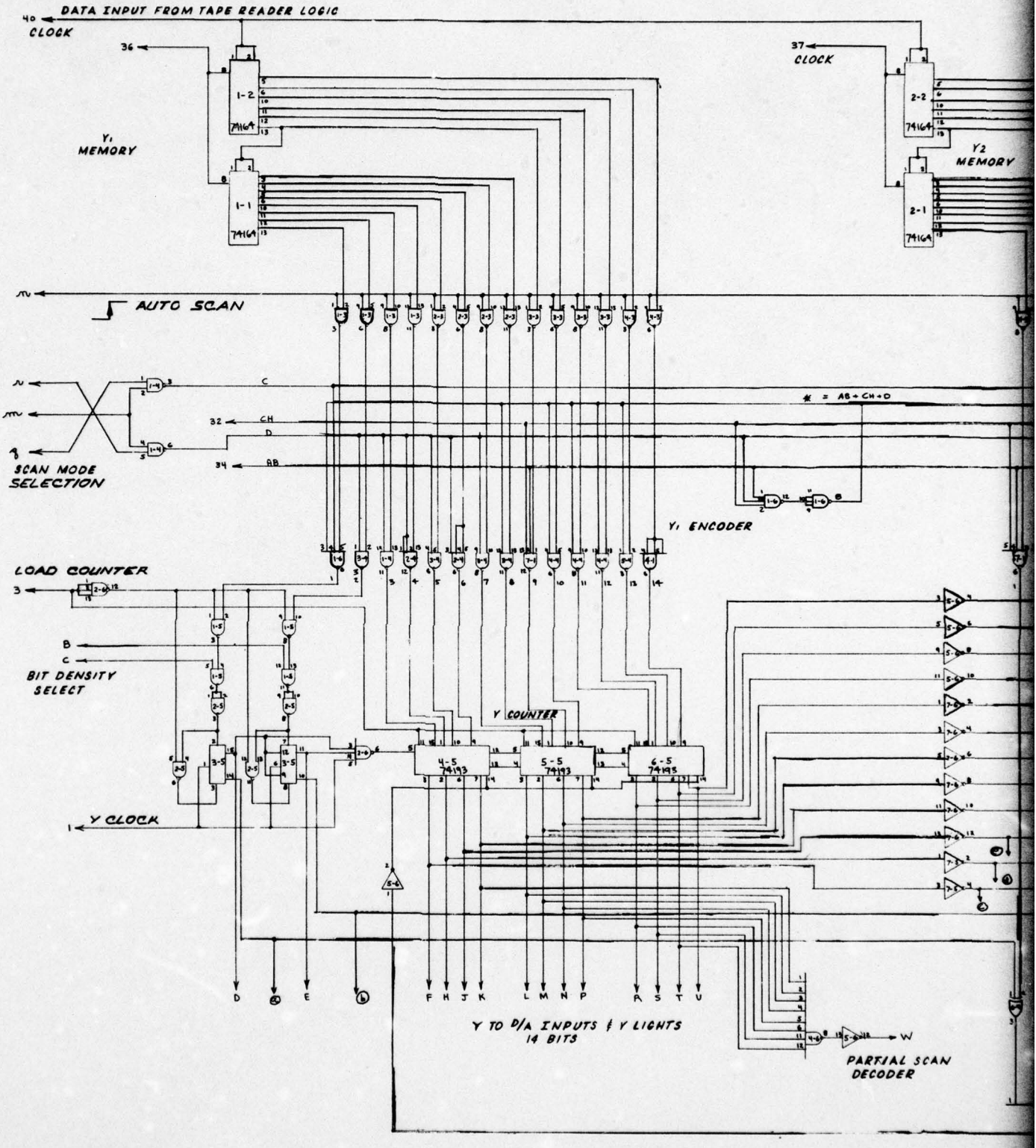
MATL.: MICROFABRICATION SYSTEM

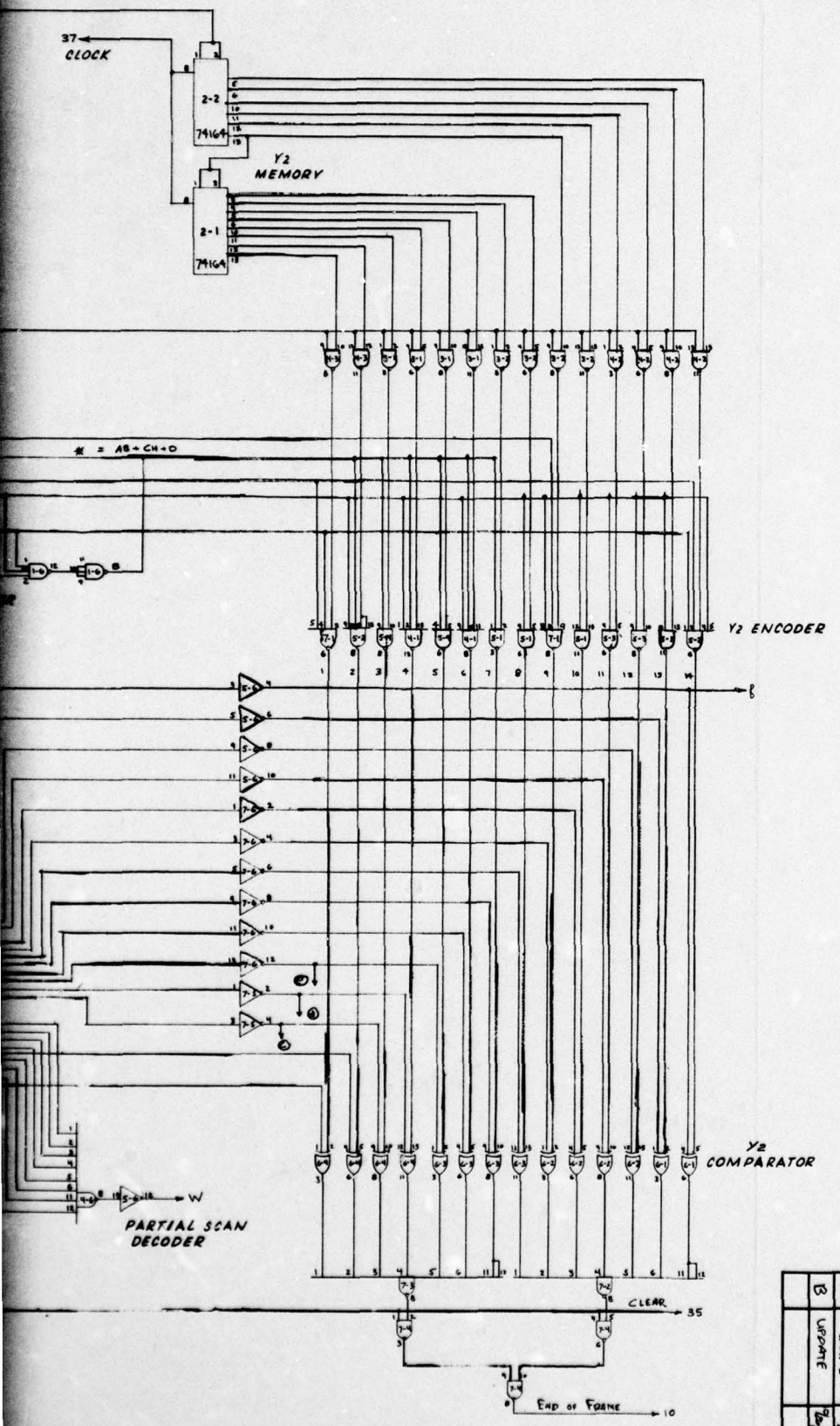
NEXT ASSY — SCALE — WT/1000 — REV. — DR. 0X-31430-037





			REV.	A	AMR	ADVANCED METALS RESEARCH CORP. BURLINGTON MASS.			
			REMARKS	UPDATE	TOLERANCES (EXCEPT AS NOTED) DECIMAL ± .005 FRACTION ± 1/64 ANGULAR ± 1/2° REMOVE ALL BURRS NEXT ASSY	DWN. W.R. DATE 7-74 APP'D DATE	TITLE SCAN GENERATOR - Y AXIS - 2 MATL. MICROFABRICATION SYSTEM		
			DATE	7/24/74		SCALE	NO REQD	REV.	NO. DX-31420-039





CIRCUIT CARD NO. 24

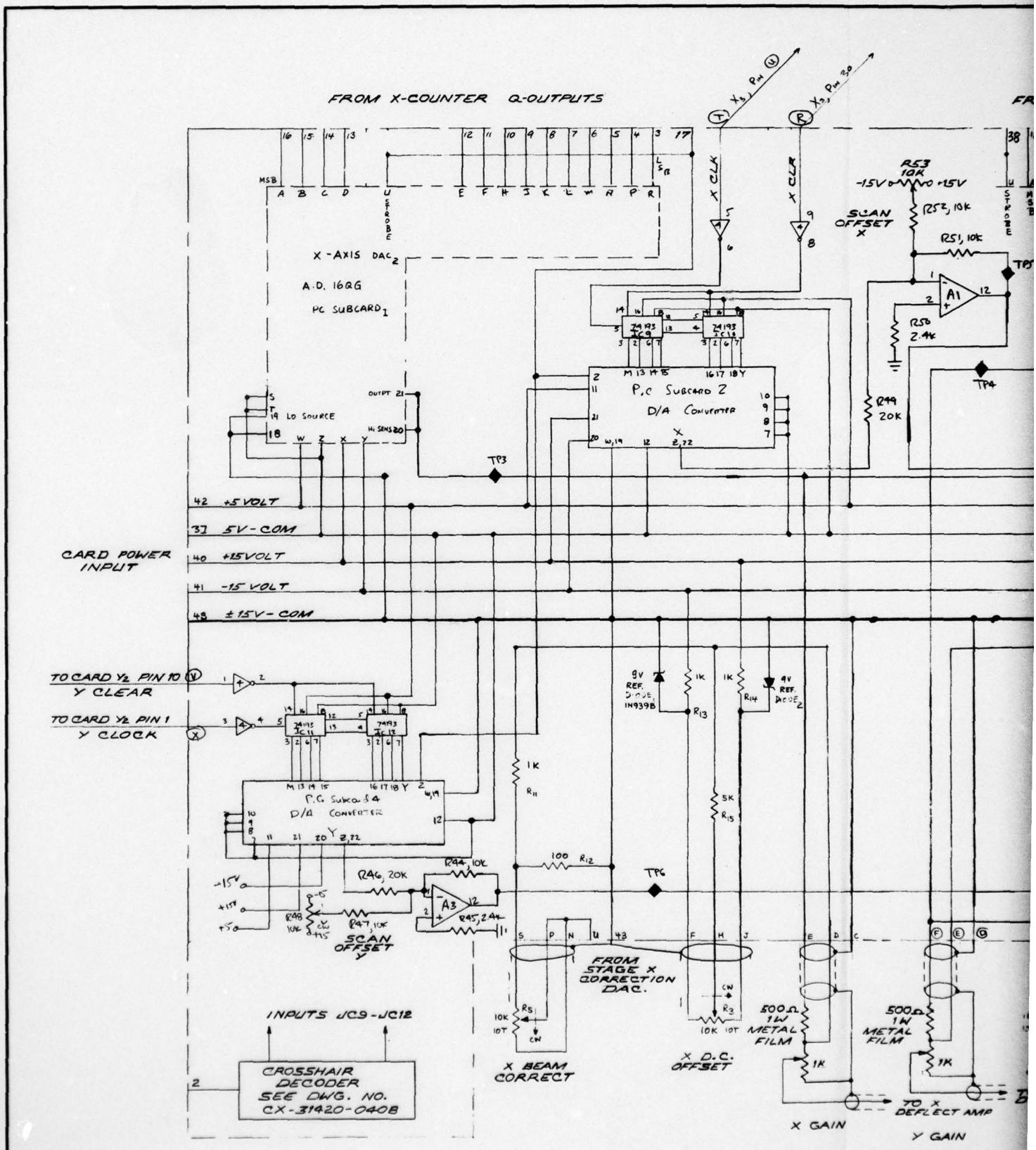
REV.	DESCRIPTION	DATE
B	UPDATE	7/16/75
A	DRAWING UPDATE	7/8/74

AMR — ADVANCED METALS RESEARCH CORP. BURLINGTON MASS.

TOLERANCES (EXCEPT AS NOTED)
DECIMAL ± .005
FRACTION ± 1/64
ANGULAR ± 1/4°
REMOVE ALL BURRS
NEXT ASSY

DWN. W.R
DATE 6-74
APP
DATE
SCALE | NO REQD

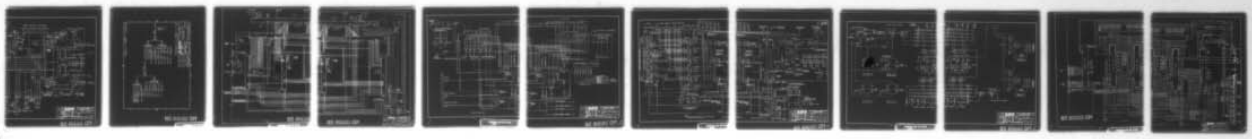
TITLE: SCAN GENERATOR Y AXIS-1
MATL.: MICROFABRICATION SYSTEM
REV. | NO. DK-31430-038



AD-A045 592 ADVANCED METALS RESEARCH CORP BEDFORD MASS F/G 9/1
ELECTRONIC BEAM FABRICATION OF SURFACE ACOUSTIC WAVE TRANSDUCER--ETC(U)
MAY 77 J A DOHERTY F19628-76-C-0179

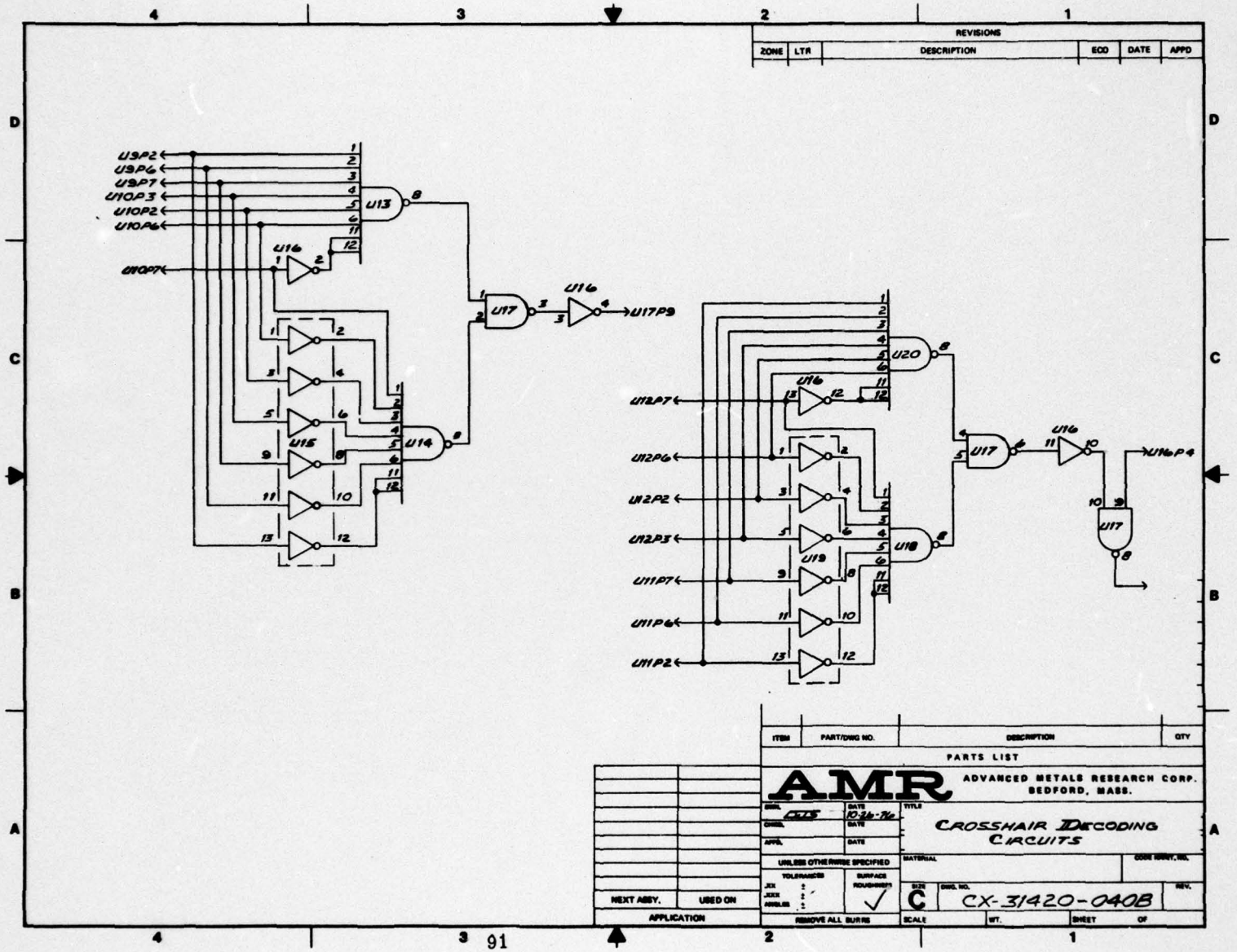
UNCLASSIFIED RADC-TR-77-164 NL

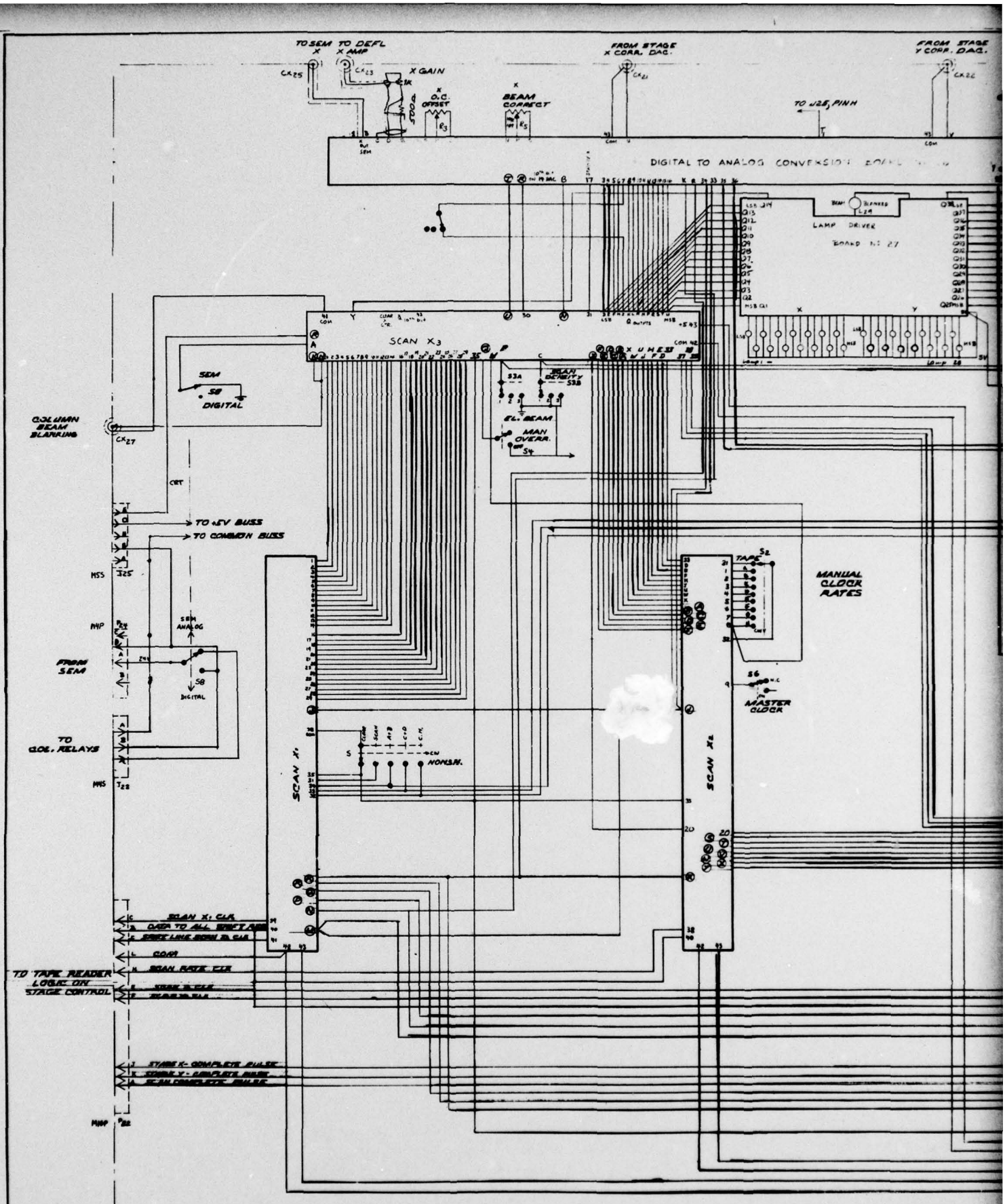
2 OF 2
AD
A045592

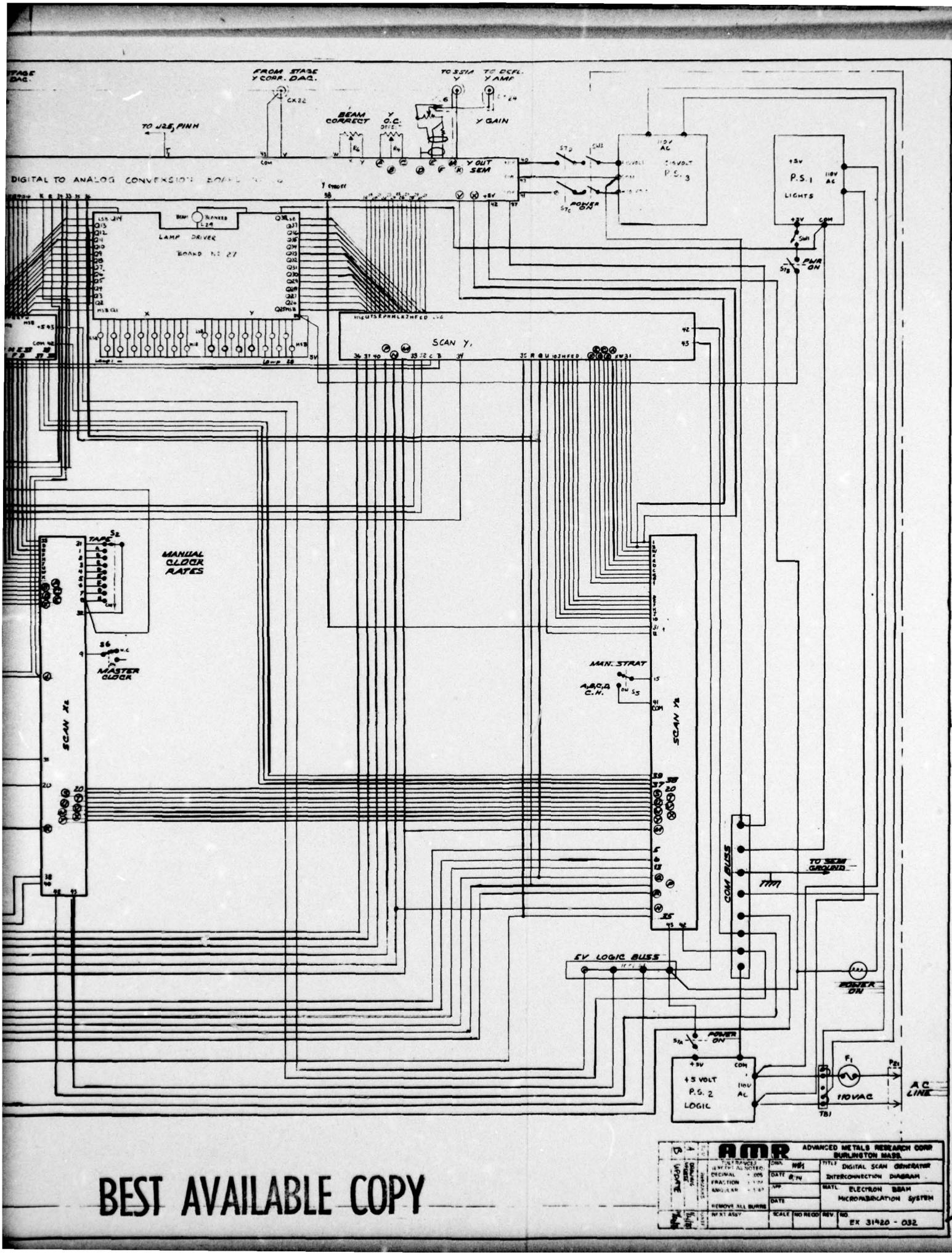


END
DATE
FILMED
11-77
DDC

BEST AVAILABLE COPY



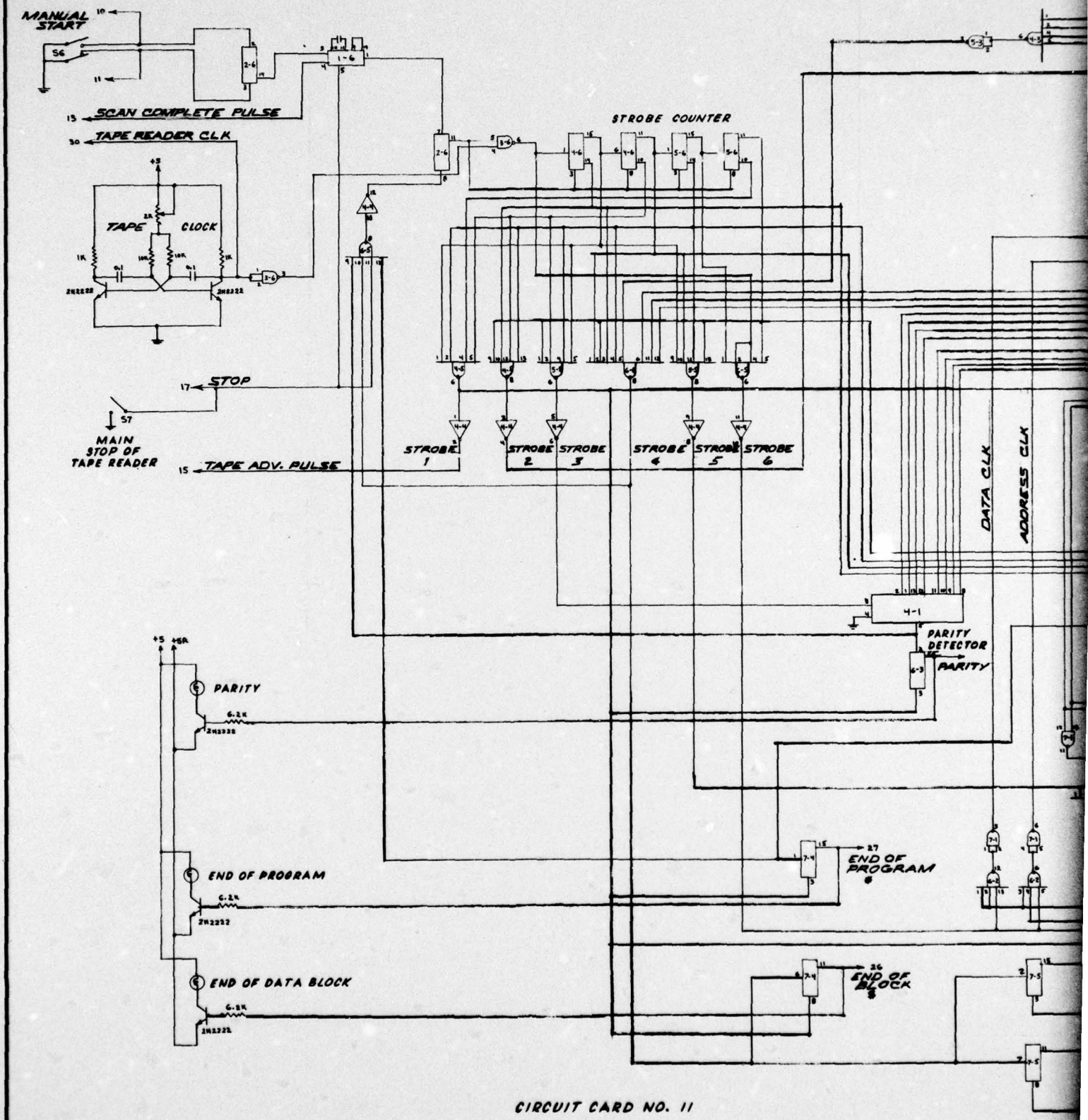




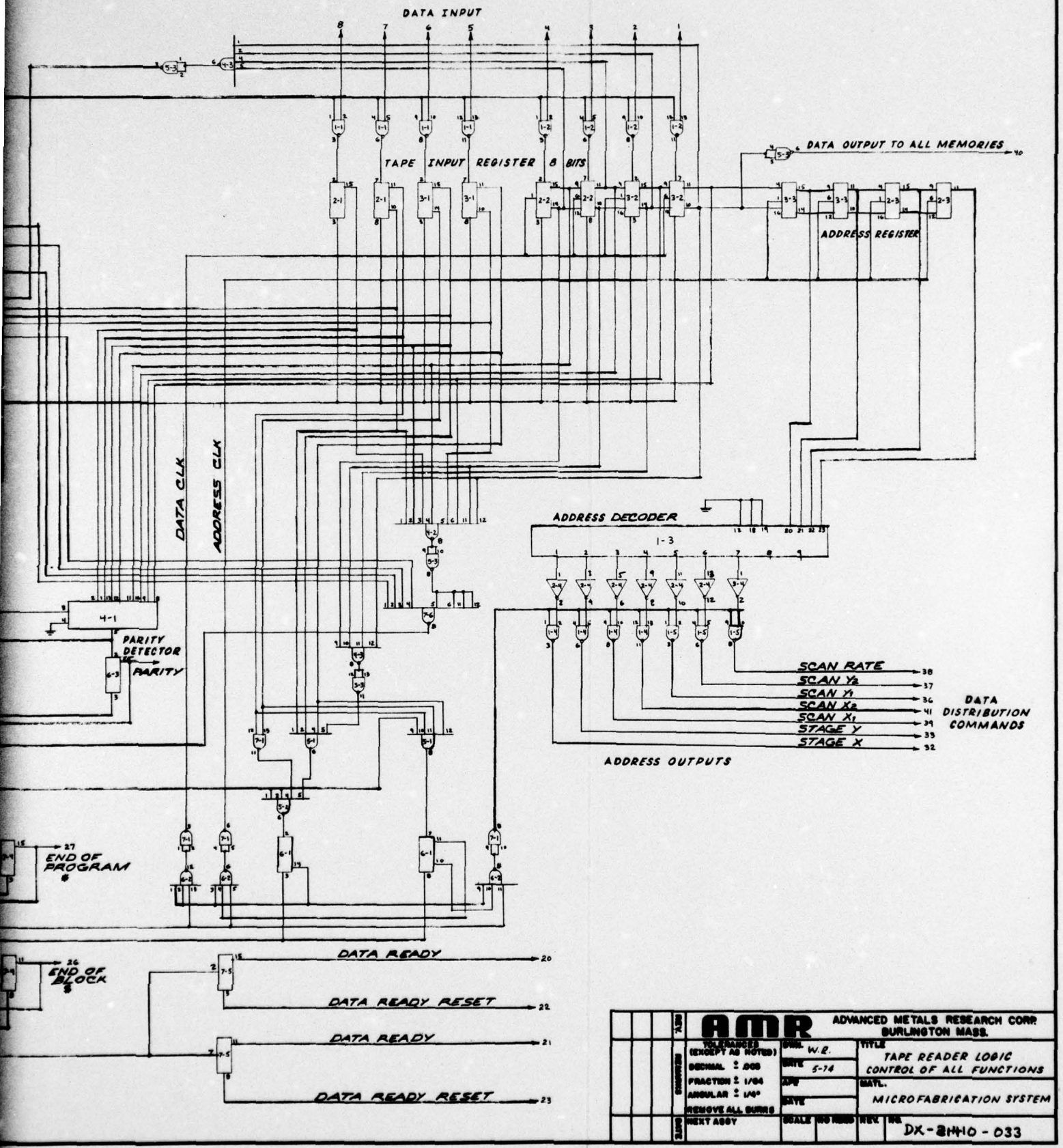
BEST AVAILABLE COPY

AMR	ADVANCED METALS RESEARCH CORP BURLINGTON MASS.		
DWN. WB1	TITLE DIGITAL SCAN GENERATOR INTERCONNECTION DIAGRAM		
DATE 8/74			
APP.	MATL ELECTRON BEAM MICROFABRICATION System		
DATE			
REMOVE ALL BURRS	SCALE NO REQD	REV.	NO. EX 31420 - 032

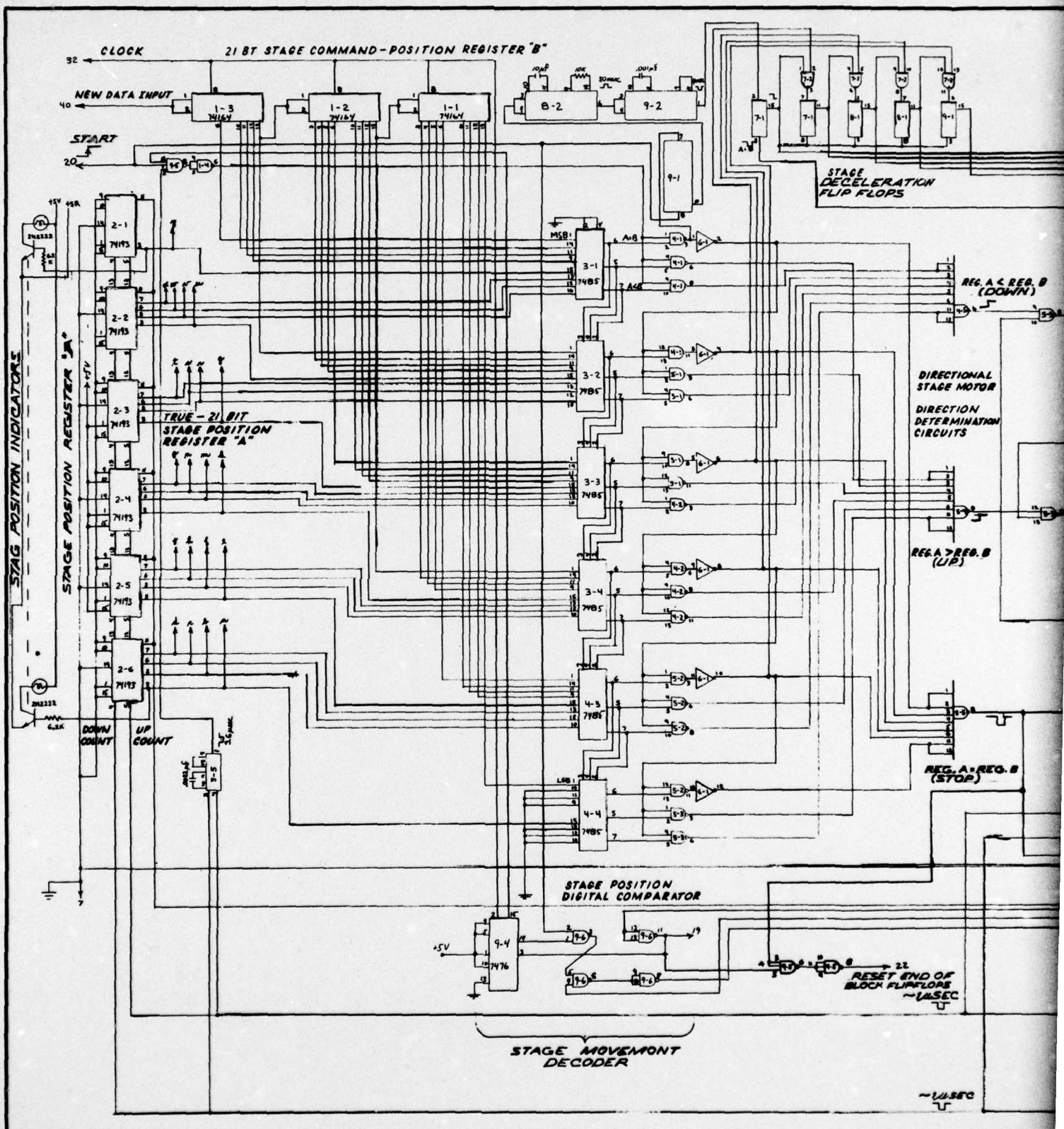
2



CIRCUIT CARD NO. 11

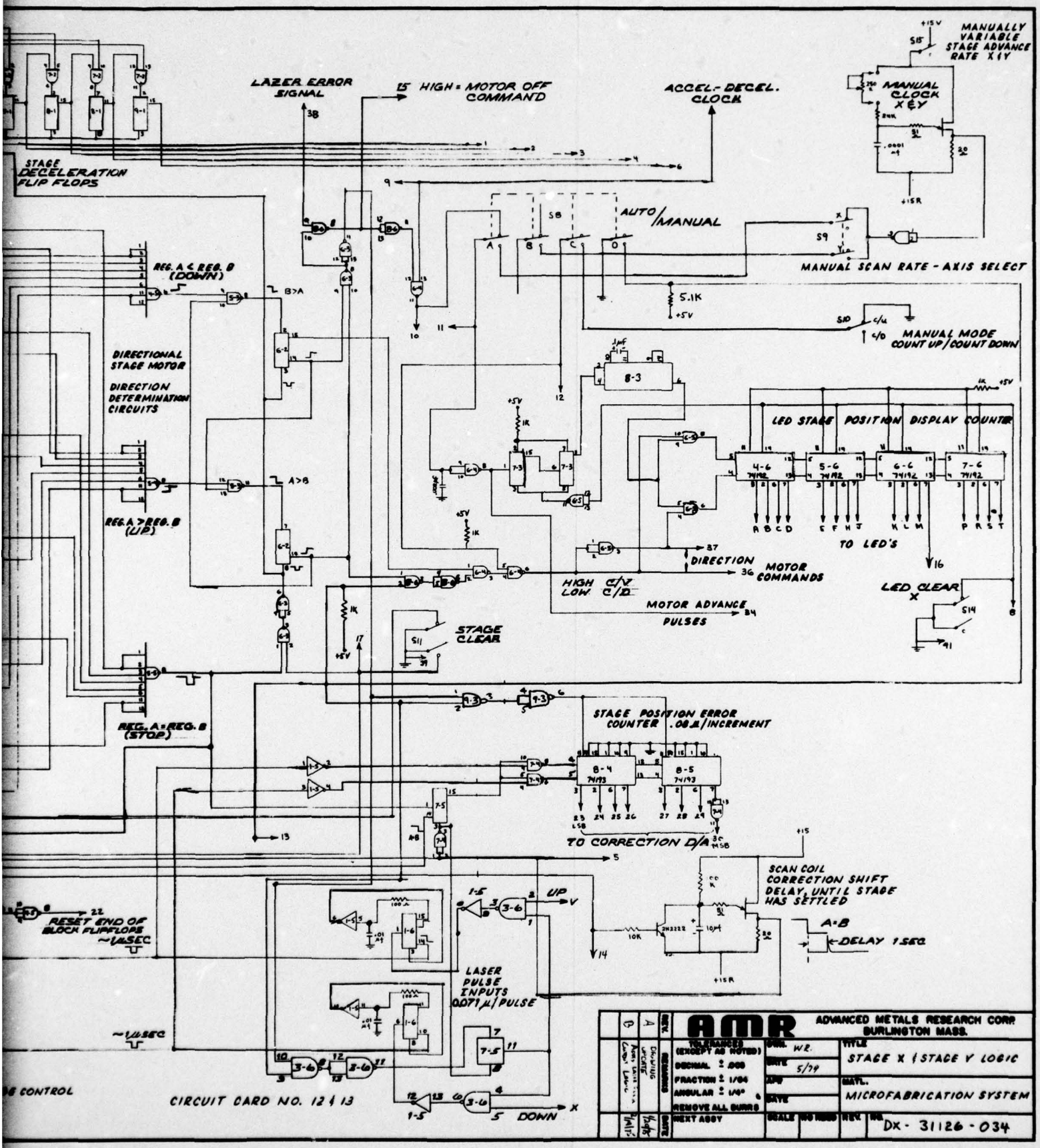


AMR	ADVANCED METALS RESEARCH CORP. BURLINGTON MASS.
TOLERANCES (EXCEPT AS NOTED) DECIMAL ± .005 FRACTION ± 1/64 ANGULAR ± 1/2° REMOVE ALL BURRS	DWN. W.R. DATE 5-74 APP. DATE
NEXT ASSY	SCALE NO NEED
TITLE: TAPE READER LOGIC CONTROL OF ALL FUNCTIONS	MATL.: MICROFABRICATION SYSTEM
REV.	NO. DX-8H10-033



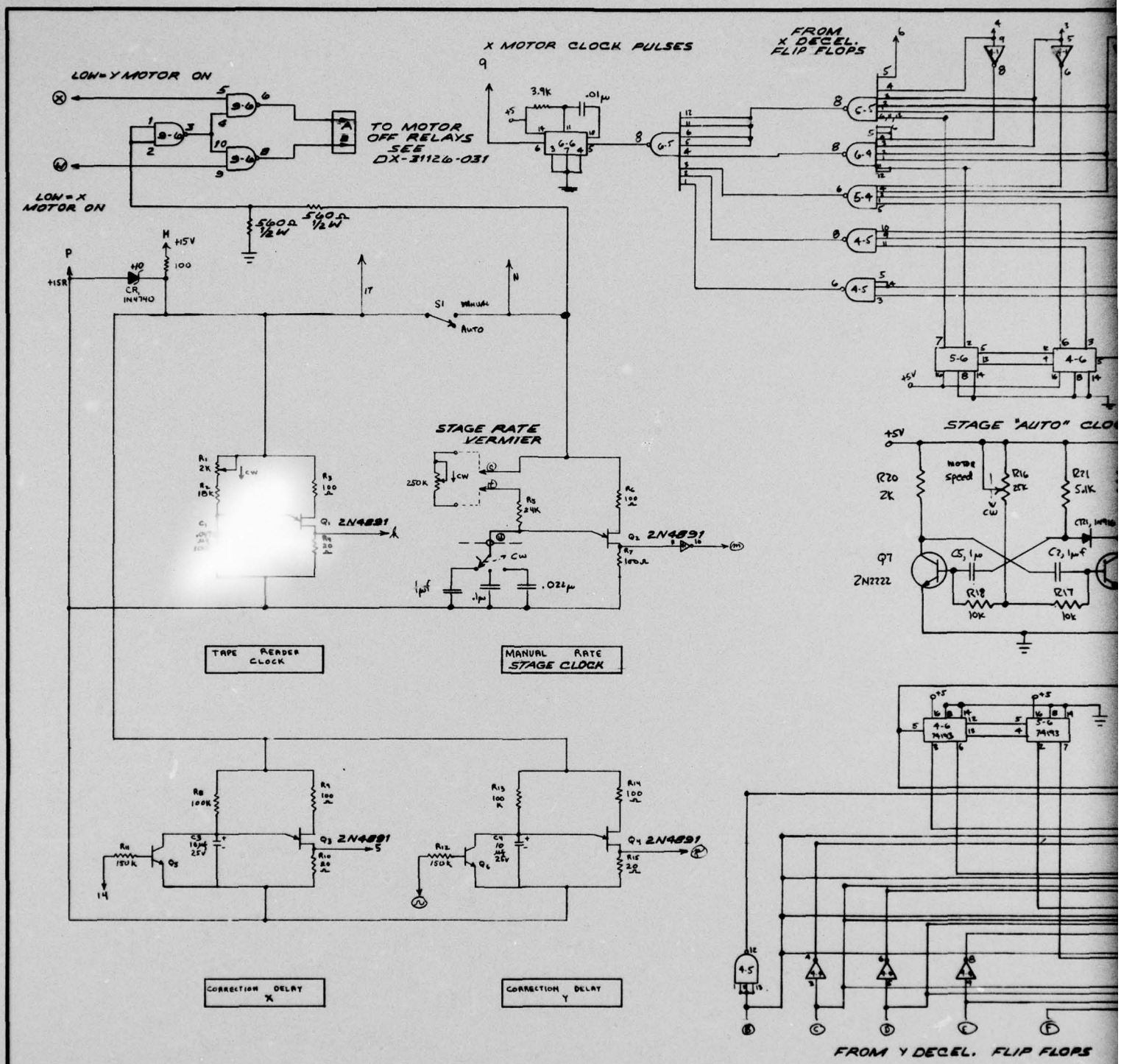
NOTE:
DIAGRAM IDENTICAL FOR X & Y STAGE CONTROL
ONE CIRCUIT CARD PER AXIS

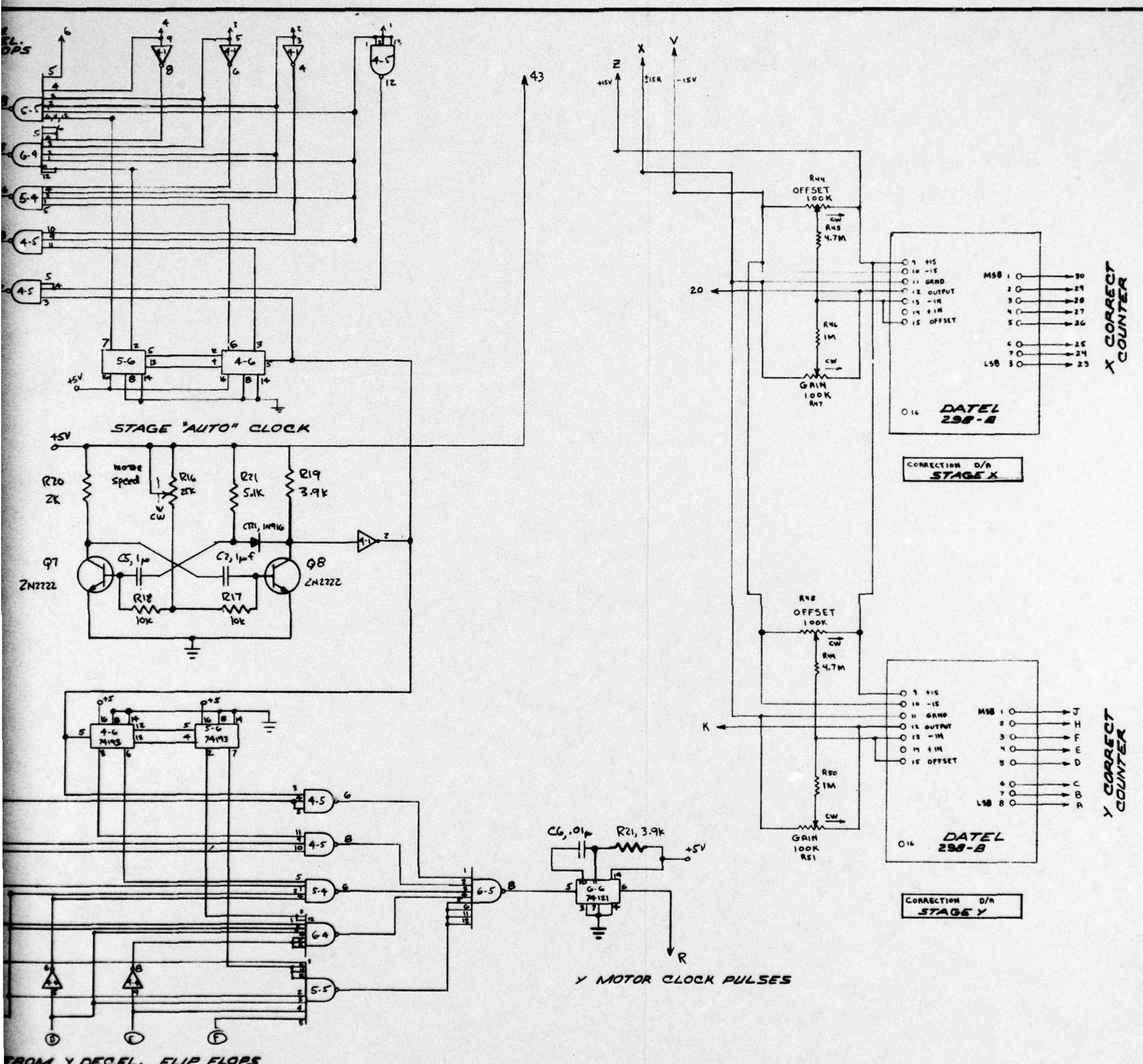
CIRCUIT



REVISIONS		AMR	ADVANCED METALS RESEARCH CORP. BURLINGTON MASS.		
DRAWING APPR.		TOLERANCES (EXCEPT AS NOTED) DECIMAL ± .005 FRACTION ± 1/64 ANGULAR ± 1/2° REMOVE ALL BURRS	DWN. W.R. DATE 5/79 APP. DATE	TITLE STAGE X & STAGE Y LOGIC	
				MATL. MICROFABRICATION SYSTEM	
		NEXT ASSY	SCALE NO. REQD	REV.	DWG. NO. DX-31126-034

BEST AVAILABLE COPY 2





REV.	REMARKS	DATE
A	DRAWING UPDATE	1/1/75
B	STAGE DRIVE CKT MOD ADDED	2/6/75

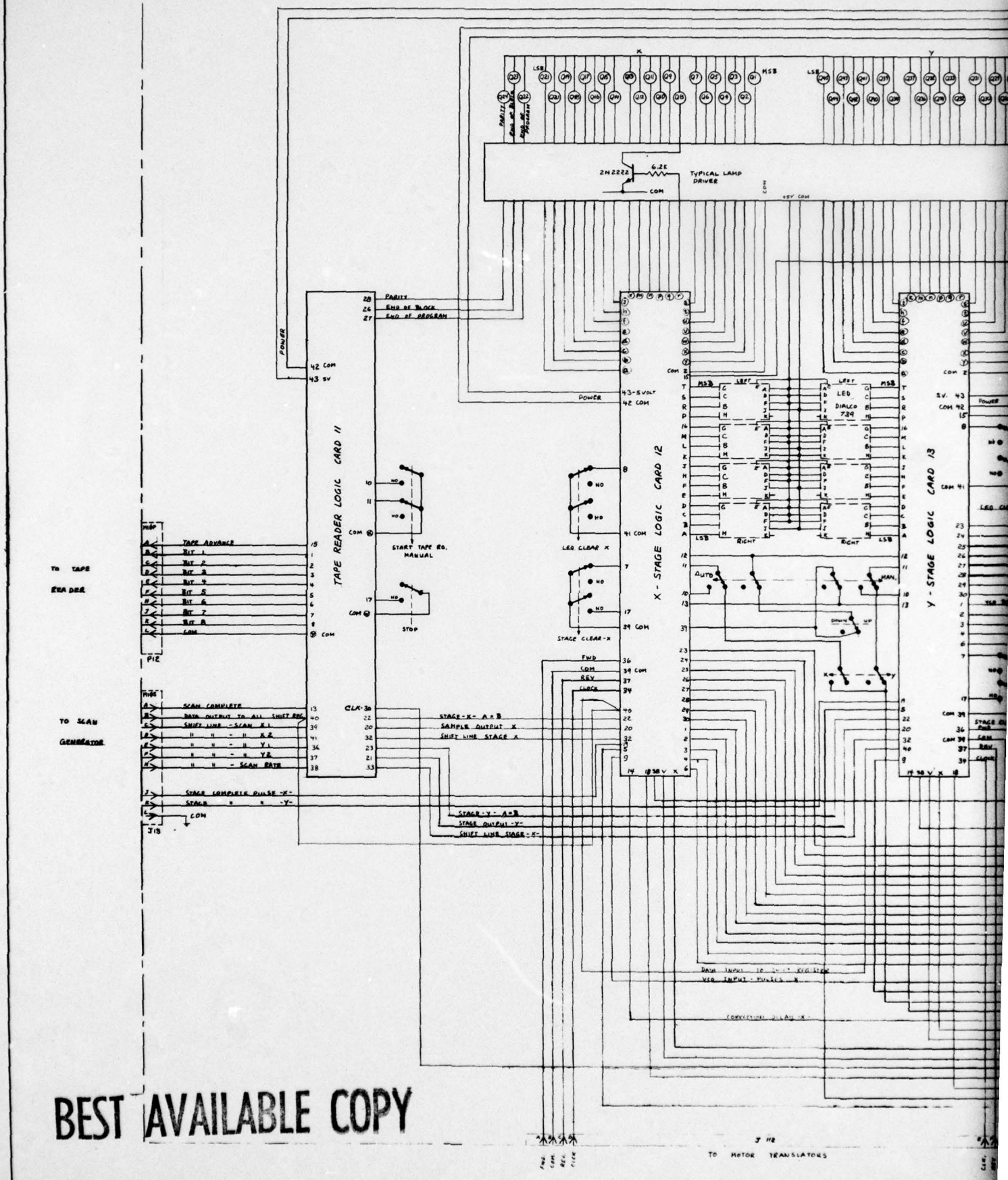
AMR ADVANCED METALS RESEARCH CORP. BURLINGTON MASS.

TOLERANCES (EXCEPT AS NOTED)
DECIMAL ± .005
FRACTION ± 1/64
ANGULAR ± 1/4°
REMOVE ALL BURRS
NEXT ASSY

DWN. W.R.
DATE 3/74
APD
DATE

TITLE: AUX. CARD TAPE READER & STAGE
MATL.: MICROFABRICATION SYSTEM
SCALE | NO REQD | REV. | NO. DX-31136-035

BEST AVAILABLE COPY 2



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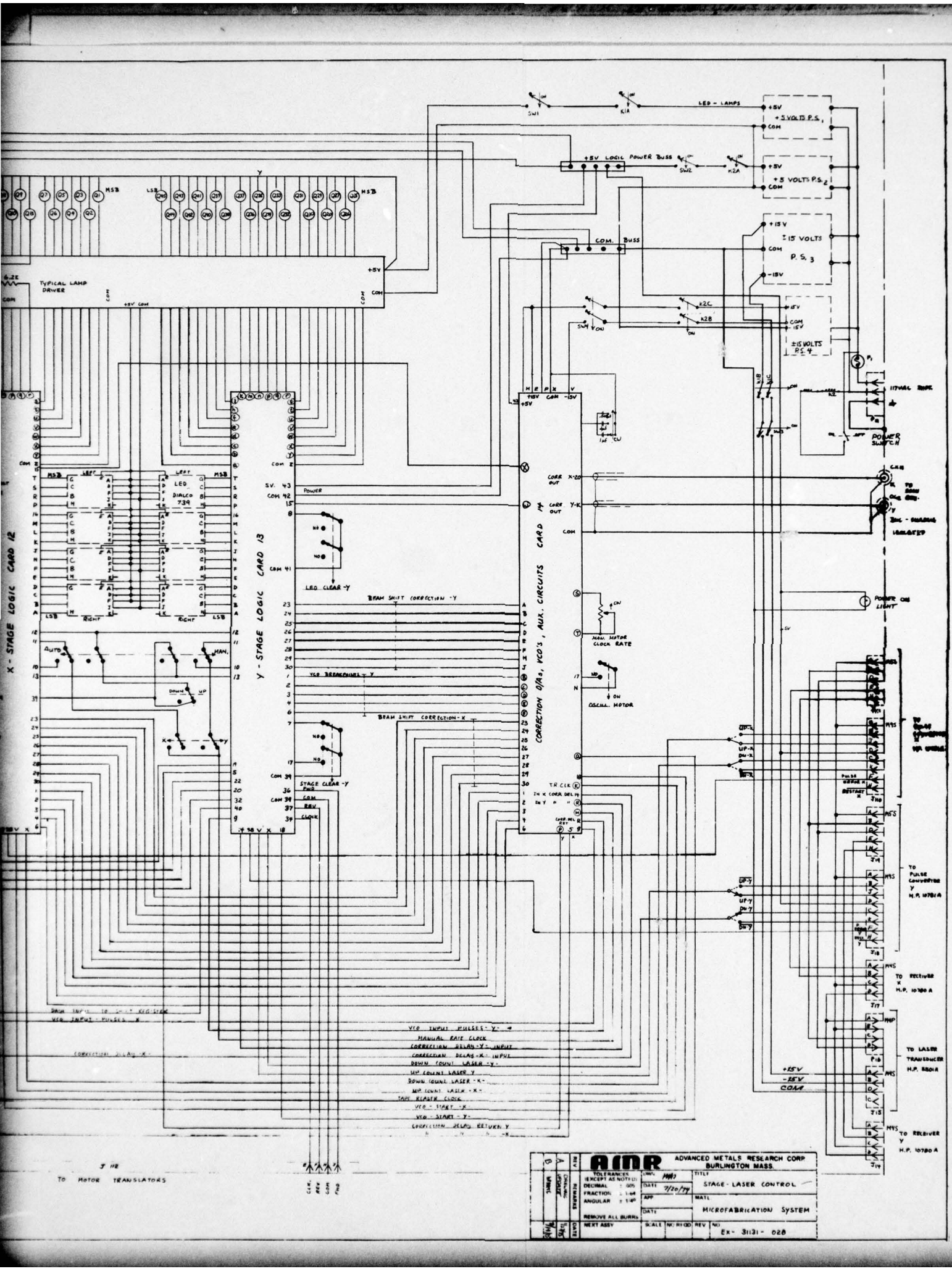

REV	DESCRIPTION	DATE	AMR ADVANCED METALS RESEARCH CORP. BURLINGTON MASS.				
			TOLERANCES (EXCEPT AS NOTED)	INIT. MMJ	TITLE STAGE - LASER CONTROL		
			DECIMAL ± .005	DATE 7/20/79			
			FRACTION ± 1/64	APP	MATL MICROFABRICATION SYSTEM		
			ANGULAR ± 1/2°	DATE			
			REMOVE ALL BURRS	NEXT ASSY	SCALE NONE	REV	NO. EX- 31131- 028

2

METRIC SYSTEM

BASE UNITS:

Quantity	Unit	SI Symbol	Formula
length	metre	m	...
mass	kilogram	kg	...
time	second	s	...
electric current	ampere	A	...
thermodynamic temperature	kelvin	K	...
amount of substance	mole	mol	...
luminous intensity	candela	cd	...

SUPPLEMENTARY UNITS:

plane angle	radian	rad	...
solid angle	steradian	sr	...

DERIVED UNITS:

Acceleration	metre per second squared	...	m/s
activity (of a radioactive source)	disintegration per second	...	(disintegration)/s
angular acceleration	radian per second squared	...	rad/s
angular velocity	radian per second	...	rad/s
area	square metre	...	m
density	kilogram per cubic metre	...	kg/m
electric capacitance	farad	F	A·s/V
electrical conductance	siemens	S	A/V
electric field strength	volt per metre	...	V/m
electric inductance	henry	H	V·s/A
electric potential difference	volt	V	W/A
electric resistance	ohm		V/A
electromotive force	volt	V	W/A
energy	joule	J	N·m
entropy	joule per kelvin	...	J/K
force	newton	N	kg·m/s
frequency	hertz	Hz	(cycle)/s
illuminance	lux	lx	lm/m
luminance	candela per square metre	...	cd/m
luminous flux	lumen	lm	cd·sr
magnetic field strength	ampere per metre	...	A/m
magnetic flux	weber	Wb	V·s
magnetic flux density	tesla	T	Wb/m
magnetomotive force	ampere	A	...
power	watt	W	J/s
pressure	pascal	Pa	N/m
quantity of electricity	coulomb	C	A·s
quantity of heat	joule	J	N·m
radiant intensity	watt per steradian	...	W/sr
specific heat	joule per kilogram-kelvin	...	J/kg·K
stress	pascal	Pa	N/m
thermal conductivity	watt per metre-kelvin	...	W/m·K
velocity	metre per second	...	m/s
viscosity, dynamic	pascal-second	...	Pa·s
viscosity, kinematic	square metre per second	...	m/s
voltage	volt	V	W/A
volume	cubic metre	...	m
wavenumber	reciprocal metre	...	(wave)/m
work	joule	J	N·m

SI PREFIXES:

Multiplication Factors	Prefix	SI Symbol
1 000 000 000 000 = 10^{12}	tera	T
1 000 000 000 = 10^{9}	giga	G
1 000 000 = 10^{6}	mega	M
1 000 = 10^{3}	kilo	k
100 = 10^{2}	hecto*	h
10 = 10^{1}	deka*	da
0.1 = 10^{-1}	deci*	d
0.01 = 10^{-2}	centi*	c
0.001 = 10^{-3}	milli	m
0.000 001 = 10^{-6}	micro	μ
0.000 000 001 = 10^{-9}	nano	n
0.000 000 000 001 = 10^{-12}	pico	p
0.000 000 000 000 001 = 10^{-15}	femto	f
0.000 000 000 000 000 001 = 10^{-18}	atto	a

* To be avoided where possible.

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