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INVESTIGATION OF TECHNOLOGICAL PROBLEMS IN GaAs

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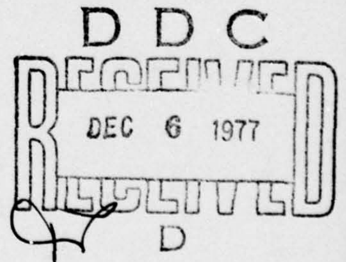

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This report presents the results of an investigation of technological problems associated with the growth and preparation of GaAs with emphasis on problems related to microwave devices. The work was carried out by a team which successfully combined the benefits of industry and university research, having the Science Center, Rockwell International as the prime contractor with three universities and a crystal growth laboratory as subcontractors. The subcontractors were the California Institute of Technology, Cornell University, Stanford University, and Crystal Specialties, Inc.

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One of the most significant accomplishments of this program is the high uniformity and reproducibility of doping profiles achieved by ion implantation into semi-insulating substrates. Such results have brought GaAs ion implantation into maturity as a technique for preparation of device quality layers. These results are not only expected to lead to increased use of ion implantation for discrete FET device fabrication, but also to pave the way for the development of a planar GaAs IC technology.

In bulk growth of semi-insulating GaAs the range of Cr concentration which produces optimum results has been determined (3×10^{15} to $5 \times 10^{16} cm^{-3}$). By minimizing Si contamination, such moderate Cr addition is sufficient to achieve electrical compensation in nearly 100% of the growth runs. Overall yield still shows some fluctuations due to boat wetting problems, but it has reached peaks of 80%. Transport property measurements have showed that a deep donor, probably oxygen, participates in the electrical compensation in conjunction with the Cr acceptor. A Mn acceptor has been found responsible for the p-type conductivity of low resistivity layers formed on semi-insulating GaAs by heat treatment in epitaxial reactors. Distinctions between the effects of heat treatment in epitaxial reactors and in post-implantation anneal have been identified, showing that different preselection tests for semi-insulating substrates are required, depending on whether they are to be used for epitaxial growth or ion implantation.

In LPE growth of semi-insulating buffer layers, a study of the interactions between the growth system components has shown that the melt bakeout temperature is the most critical parameter for achieving high resistivity in undoped layers. With Cr addition, a resistivity as high as 10^6 ohm-cm has been obtained. LPE growth of submicron ($\sim 0.5 \mu m$) FET layers with a "restricted melt" technique has shown excellent uniformity and reproducibility, with 4% standard variation of thickness over $2.5 cm^2$ ($0.5 \mu m$ thick) layers, and 6% standard deviation of average thickness and carrier concentration over five consecutive runs. LPE high purity buffer layers with total ionized impurity concentration of $2 \times 10^{14} cm^{-3}$ and 77K mobility of $160,000 cm^2/Vsec$ have been grown in a system with multilayer capability.

In high-dose Se and Te implantation, annealing conditions for optimum activation were determined, leading to peak doping as high as $4 \times 10^{18} cm^{-3}$. Backscattering studies of the annealing behavior of amorphous layers caused by ion implantation revealed a reordering process different from the simple epitaxial growth of Si and Ge.

Schottky barrier gate FETs were used as test vehicles to measure the quality of the implanted layers. FETs fabricated on Se doped layers made by direct implantation into semi-insulating substrates showed excellent RF performance: 14 dB maximum available gain and 2.6 dB minimum noise figure with 8 dB associated gain were measured at 10 GHz for transistors having gate lengths of $1 \mu m$ and ¼mm gate widths. This performance nearly matches the best results reported for laboratory devices of similar geometry made by VPE. Therefore, full advantage may be taken of the exceptional levels of reproducibility and uniformity attainable by ion implantation without compromising on device performance. In addition, implanted transistors are relatively free of drift problems frequently observed in epitaxial transistors.

Experimental measurements of the low frequency noise of IMPATT diodes have been used to extract parameters useful for device design, such as intrinsic response time and multiplication factors under operating conditions. Measurements of ionization rates as functions of the electric field showed a strong dependence on doping concentration which has been qualitatively interpreted in terms of delays in promotion of the accelerated electrons into the higher conduction bands.

FOREWORD

The research covered in this report was carried out in a team effort having the Rockwell Science Center as the prime contractor with three universities and a crystal growth company as subcontractors. The effort was sponsored by the Materials Science Office of the Defense Advanced Research Projects Agency through R.A. Reynolds and C.M. Stickley. The contract was monitored by S.A. Roosild with the Solid State Sciences Division of the Rome Air Development Center/ETSD. Program managers were A. Joseph and F. Blum. The principal investigators for each organization were:

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TABLE OF CONTENTS

PAGE

1.0 INTRODUCTION 1

2.0 HIGHLIGHTS 5

2.1 Semi-Insulating Substrate Material Growth 5
2.2 Semi-Insulating Material Evaluation 5
2.3 Epitaxial Material Growth and Characterization 7
2.4 Ion Implantation and Ion Beam Analysis 8
2.5 MESFET Performance 9
2.6 Avalanche Parameters 10

3.0 SEMI-INSULATING SUBSTRATE MATERIAL 11

3.1 Bulk Growth of Semi-Insulating GaAs; Crystal Specialties 11

3.2 Evaluation of Semi-Insulating Substrate Material 23

3.2.1 Bulk Electrical Properties of Semi-Insulating GaAs-Science Center 24
3.2.2 Potential Profiles at Semi-Insulated Substrates-Epilayer Interfaces - Science Center 47
3.2.3 Inclusions in Semi-Insulating GaAs-Cornell University 61
3.2.4 Effects of Heat Treatment on Semi-Insulating GaAs-Science Center 65

4.0 LIQUID PHASE EPITAXIAL MATERIAL GROWTH AND CHARACTERIZATION 81

4.1 Preparation and Properties of Semi-Insulating LPE-GaAs-Stanford University 82

4.2 Submicron LPE Growth Techniques-Science Center 113

4.3 Growth of FET Active and Buffer Layers by LPE-Cornell University 126

5.0 ION IMPLANTATION AND ION BEAM ANALYSIS 154

5.1 Reproducibility of Low-Dose Se Implants-Science Center 155

5.2 High Dose Se and Te Implantation-Science Center & Caltech 162

TABLE OF CONTENTS (cont'd)

Page

5.3 Sulphur Implantation-Science Center and Caltech 180

5.4 Reordering of Implanted Amorphous GaAs-Science Center and Caltech 189

5.5 Contact Metalization Systems-Caltech 197

6.0 CORRELATION BETWEEN MATERIAL PARAMETERS AND DEVICE PERFORMANCE 212

6.1 MESFET Performance-Science Center 212

6.2 Determination of Material Parameters From Low Frequency Noise Measurements on IMPATT Diodes-Cornell University 224

6.3 Electrolytic Oxidation and Etching Techniques-Cornell University 248

6.4 GaAs Ionization Coefficients-Cornell University 252

7.0 PUBLICATIONS 279

8.0 REFERENCES 281

LIST OF ILLUSTRATIONS

Page

Fig. 1 Schematic of a three zone horizontal Bridgmann system. 13

Fig. 2 Top and bottom view of a Bridgmann grown semi-insulating GaAs crystal 15

Fig. 3 Graphic representation of n, p, N_d^+ and N_a^- as functions of the position of the Fermi level in the energy gap; (a) for the deep-acceptor model, (b) for the deep-donor-deep-acceptor model 28

Fig. 4 Resistivity vs. temperature data 36

Fig. 5 Plot of $\rho T^{3/2}$ vs. 1/T' for the low-Cr data of Fig. 2. The temperature scale was corrected for the effect of the thermal variation of the energy gap, T' = T E_g(298K)/E_g(T). The solid line is the result of a linear least square fit 38

Fig. 6 Result of a non-linear least square fit of the mid-Cr data for $E_c - E_d$ = 0.64 eV. Fitting parameters: N_a/N_d = 0.98; $E_c - E_a$ = 0.90 eV. The dots represent the experimental points 40

Fig. 7 Plot of the mean square error ε and the fitting parameters N_a/N_d and $E_c - E_a$ against the parameter $E_c - E_d$ in the non-linear least square fit of the mid-Cr data . . 41

Fig. 8 Result of a non-linear least square fit of the high-Cr data for $E_c - E_d$ = 0. Fitting parameters: N_a/N_d = 1.04; $E_c - E_a$ = 0.83 eV. The dots represent the experimental points. The dashed lines represent the separate contributions of electrons and holes 43

Fig. 9 Plot of the mean square error and the fitting parameters N_a/N_d and $E_c - E_a$ against the parameter $E_c - E_d$ in the non-linear least square fit of the high-Cr data 44

LIST OF ILLUSTRATIONS (Cont'd)

Page

Fig. 10 Measured potential profiles across a p^+, n, n^+ junction ($p=10^{18}cm^{-3}$, $n=7.5x10^{14}cm^{-3}$). (a) V vs x for reverse bias between -5 and -25 V. (b) $V^{\frac{1}{2}}$ vs x; dots: experimental points; lines: linear least-mean-square fits. (reprint from Ref. 23) 50

Fig. 11 SEM micrograph of a typical specimen for AES-SEM measurements 51

Fig. 12 Measurement of sample thickness by cathodoluminescence. (a) Normal scanning electron micrograph taken with a secondary electron detector; (b) Same as (a) in the cathodoluminescence mode using a photomultiplier with S-1 photocathode as detector 53

Fig. 13a Square root of the potential across a p-i-p specimen made with low-Cr (boule 1718) SI GaAs. Bias voltages: ▽-40V; ○-10V; △-5V applied to the left contact; ●-10V applied to the right contact 54

Fig. 13b Square root of the potential across an n-i-n specimen made with high-Cr (boule 2000) SI GaAs. △: left side (sample top) biased +3V; ○: left side (sample top) biased +6V; ●: right side (sample bottom) biased +6V . . 55

Fig. 14 I-V characteristics of n-i-n and p-i-p samples (a) High-Cr SI GaAs (boule 2000). (b) Low-Cr SI GaAs (boule 1718) 57

Fig. 15 Voltage and induced current profile across the high-Cr p-i-p sample: a) right side biased positive, b) left side biased negative 60

LIST OF ILLUSTRATIONS (Cont'd)

Page

Fig. 16 a) Chromium impurity pattern in a high-Cr SI GaAs substrate (Crystal Specialties 2000), b) Silicon impurity pattern in SI GaAs 63

Fig. 17 Sheet resistance vs heat treatment temperature for several semi-insulating GaAs samples (identified by boule numbers) 67

Fig. 18 Photoluminescence spectra of an annealed and an unannealed sample from the same wafer (from boule 2109) measured at 77K. The spectra were corrected for the spectral response of the system 69

Fig. 19 Intensity of the photoluminescence peaks (at 77K) and resistance between two contacts plotted against thickness of material removed in sequential etching steps 70

Fig. 20 Photoluminescence spectrum of a heat treated sample measured at 25K. The spectrum was corrected for the spectral response of the system 72

Fig. 21 Free hole concentration (per unit area) multiplied by $T^{-1.5}$ vs 1000/T for a sample from boule 2109 heat treated at 775°C for 90 minutes 73

Fig. 22 Sheet resistivity after anneal at 850°C for 30 minutes with a Si_3N_4 cap vs sheet resistivity after anneal in H_2 atmosphere at 750°C for 2 hours. The data points are identified by boule numbers 77

Fig. 23 Photoluminescence Spectrum at 25 K of a capped and annealed SI GaAs sample. The spectrum was corrected for the spectral response of the system 79

LIST OF ILLUSTRATIONS (Cont'd)

Page

Fig. 24 The temperature gradient growth cells 84

Fig. 25 Time-temperature cycle of the growth procedure for SI LPE GaAs 86

Fig. 26 Photomicrograph of the cross-section of an LPE layer grown on a Cr-doped GaAs substrate 87

Fig. 27 Dependence of background donor and acceptor impurities on accumulated bakeout time at two bakeout temperatures. Growth system: SiO_2-BN-H_2 90

Fig. 28 Carrier density vs bakeout temperature for three different growth systems:
C: Fused quartz-graphite-hydrogen (SiO_2-C-H_2) system.
BN(C): Fused quartz-boron nitride (on graphite cradle)-hydrogen (SiO_2-BN(C)-H_2) system.
BN: Fused quartz-boron nitride-hydrogen (SiO_2-BN-H_2) system 91

Fig. 29 Photoluminescence spectra of acceptor impurity levels in a SI LPE layer grown in a SiO_2-BN(C)-H_2 system. (e,A°): Recombination of a conduction band electron with an acceptor-bound hole. (D°,A°): Pair recombination 97

Fig. 30 Dependence of the free-carrier density and resistivity of undoped and Cr-doped layers on the bakeout temperature for a SiO_2-C-H_2 growth system 100

Fig. 31 Dependence of the resistivity of undoped and Cr-doped layers on the bakeout temperature for the SiO_2-BN(C)-H_2 system 102

LIST OF ILLUSTRATIONS (Cont'd)

Page

Fig. 32 Photoluminescence spectra of a semi-insulating Cr-doped LPE layer grown in the SiO_2-BN(C)-H_2 system compared with bulk Cr-doped SI GaAs 105

Fig. 33 Conductivity vs temperature for Cr-doped semi-insulating and undoped high-resistivity LPE layers 107

Fig. 34 Schematic diagram of the transient capacitance measurements setup and the capacitance variation with time corresponding to different bias states. W_G is the space charge region width of the Schottky barrier gate 110

Fig. 35 The temperature dependence of the corrected time constant (τT^2) of the transient capacitance for unbuffered n-type FET active layers 111

Fig. 36 Schematic representation of the restricted melt growth system 115

Fig. 37 Exploded view of LPE GaAs boat incorporating a restricted and unrestricted melt 116

Fig. 38 Layer thickness vs growth time for restricted and semi-infinite melts 119

Fig. 39 Surface morphology of LPE layers as a function of temperature gradient 121

Fig. 40 A presentation of the smooth surfaces of five successive LPE growths of thin film GaAs 122

Fig. 41 Histogram of the thickness of a typical LPE GaAs wafer . 125

Fig. 42 Photomicrograph (Nomarski phase contrast) of a layer grown at 735°C on a substrate which had undergone only a standard cleaning procedure 129

LIST OF ILLUSTRATIONS (Cont'd)

Page

Fig. 43 Photomicrograph (Nomarski phase contrast) of a layer grown at 735°C on a substrate that had undergone a porous oxide-HCl treatment in addition to standard cleaning. Growth parameters were unchanged from that shown in Fig. 42 129

Fig. 44 Plots of growth rate at 780°C as a function of growth time both with and without a supercooling of 3°C 133

Fig. 45 Predicted As profile in Ga melt at the end of growth with various growth parameters at 780°C. d_0 represents the grown layer thickness after a time interval t at a cooling rate of 1°C/min with and without a supercooling of ΔT 135

Fig. 46 Doping profile of a layer grown at 735°C using a source-seed crystal with no supercooling 137

Fig. 47 Thickness vs growth time at 780°C, calculated (solid lines) and experimental 138

Fig. 48 Thickness vs growth time at 750°C, calculated (solid lines) and experimental 138

Fig. 49 Thickness vs growth time at 735°C. Calculated (solid lines) and experimental 139

Fig. 50 Total ionized impurity concentration vs baking time . . . 147

Fig. 51 Ionized impurity concentration versus reciprocal temperature 150

Fig. 52 Electron concentration profiles for Se implants into "good" semi-insulating GaAs substrates 157

Fig. 53 Electron concentration profiles for various GaAs substrates implanted at 350°C with 1.8×10^{12} 400 keV Si ions/cm^2 and annealed at 850°C for 30 min with a silicon nitride cap 159

LIST OF ILLUSTRATIONS (Cont'd)

Page

Fig. 54 Comparison of electron concentration profiles for 300 keV Se implants into SI substrate material from three different boules. The performance of these boules in qualification tests is discussed in the text. The dose was $3x10^{12}$ ions/cm^2 for 2917 and 3183 and $3.15x10^{12}$ ions/cm^2 for 2440 161

Fig. 55 Sheet electron concentration vs implanted dose for 400 keV Se and Te implants carried out at 350°C. Annealing conditions for the various samples are indicated on the figure 166

Fig. 56 Electron concentration and mobility profiles for semi-insulating GaAs samples implanted with 400 keV Se ions at 350°C to a dose of $1x10^{14}cm^2$. Annealing was carried out at 900°C for 10 minutes with the annealing cap indicated on the figure 167

Fig. 57 Carrier concentration and mobility profiles for Te implanted samples annealed with different caps 168

Fig. 58a Electron concentration and mobility profiles for semi-insulating GaAs samples implanted with 400 keV Se ions at 350°C to the doses indicated on the figure. Annealing was carried out at 900°C for 10 minutes using an aluminum oxy-nitride cap 170

Fig. 58b Electron mobility vs electron concentration for some of the samples of Fig. 58a. Data points are omitted for clarity... 171

Fig. 59 Doping efficiency vs annealing temperature for semi-insulating GaAs samples implanted at 350°C with 400 keV ions to the dose 173

Fig. 60 Carrier concentration and mobility profiles for Se implanted samples annealed by the capless technique or with an aluminum-oxy-nitride (labeles AlN) cap. . . . 174

LIST OF ILLUSTRATIONS (Cont'd)

Page

Fig. 61 Photoluminescence spectra from SI GaAs samples implanted with 400 keV Se ions at 350°C to a dose of $1 \times 10^{12} cm^2$. Annealing was carried out using an aluminum oxy-nitride cap at the temperatures and for the times indicated on the figure 176

Fig. 62 Sheet electron concentration, and photoluminescence intensity of the 1μm and 0.89μm peaks of Se-implanted samples vs anneal temperature. The Se doses and the anneal caps used are indicated on the figure 177

Fig. 63 Electron concentration profile for a GaAs sample implanted with 9×10^{12} 100-keV S ions/cm^2 at 350°C and annealed at 850°C with a silicon nitride cap, compared with the S distribution calculated from LSS range parameters 181

Fig. 64 Distribution of the maximum observed electron concentration and the depth at which the electron concentration reached 10% of this maximum for a GaAs sample implanted with 7×10^{12} 100 keV S ions/cm^2 at 350°C and annealed at 850°C with a silicon nitride cap 182

Fig. 65 Electron concentration profiles for GaAs samples implanted with the indicated doses of 400 keV S ions at the indicated temperatures and annealed at 850°C with a silicon nitride cap 184

Fig. 66 X-ray spectrum obtained from a GaAs sample implanted with 1×10^{15} 100 keV S ions/cm^2 at 350°C using a 400 keV proton beam incident in a random direction 186

LIST OF ILLUSTRATIONS (Cont'd)

Page

Fig. 67 Normalized S K X-ray and backscattered proton yield vs tilt angle for the <110> and <111> axes of a GaAs sample implanted with $1x10^{15}$ 100 keV S ions/cm^2 at 350°C, using a 400 keV proton beam for the analysis . . . 188

Fig. 68 Random and <110> aligned backscattering spectra from <100> GaAs samples implanted with Zn and annealed for 15 min at the indicated temperatures 191

Fig. 69 Random and aligned spectra from Se implanted GaAs samples annealed as indicated. <111> GaAs and <111> aligned spectra 193

Fig. 70 Random and aligned spectra from Se implanted GaAs samples annealed as indicated. (b) <100> GaAs and <100> aligned spectra 194

Fig. 71 TEM of GaAs implanted with 400 keV Se ions and annealed at 200°C for 1100 minutes. (a) Dark field image illustrating crystalline substructure in implanted layer. g: <111> streak. (b) Selected area diffraction pattern, [110] zone normal with intense <111> streaking 196

Fig. 72 2 MeV ^4He backscattering spectra of a SiO_2/740Å Ge/2300Å Au/470Å Ni sample. The spectra of the substrate has been omitted and the vertical arrows indicate the energy of He particles scattered from surface atoms of the corresponding elements. (a) as-deposited, (b) annealed at 450°C for 5 minutes, and (c) same as (b) but Ge-Ni layer etched off in dilute HNO_3 199

Fig. 73 Energy spectra of 2 MeV ^4He ions backscattered from a SiO_2/910Å Ni/1020Å Au/1700Å Ge sample. The spectra of the substrate has been omitted and the vertical

LIST OF ILLUSTRATIONS (Cont'd)

Page

arrows indicate the energy of the particle scattered from surface atoms of the corresponding elements. (a) as-deposited, (b) annealed at 450°C for 5 minutes . . 202

Fig. 74 Energy spectra of 2 MeV ^{4}He ions backscattered from a SiO_2/3360Å Ge/1150Å Au/930Å Ni. The spectra of the substrate has been omitted and the vertical arrows indicate the energy of the particles scattered from surface atoms of the corresponding elements. (a) as-deposited, (b) annealed at 450°C for 5 minutes . . 204

Fig. 75 2 MeV ^{4}He backscattering spectra of a SiO_2/3470Å Ge/1710Å Ni/1290Å Au sample. The spectra of the substrate has been omitted and the vertical arrows indicate the energy of the particles scattered from surface atoms of the corresponding elements. (a) as-deposited, (b) annealed at 450°C for 5 minutes . . 205

Fig. 76 15 MeV O backscattering through 150° from Ge-Au-Ni evaporated on SiO_2 and on <100> GaAs, and annealed at 450°C for 15 minutes. The bars indicate the energy for scattering from the surface from the main natural isotopes from each element 207

Fig. 77 2 MeV He^+ backscattering through 170° from <100> GaAs samples with 220Å evaporated Au, annealed in vacuum and air 209

Fig. 78 2 MeV He^+ backscattering through 170° from a sample with the structure SiO_2/Pt/Au/Ge (-160Å/990Å/630Å). The contribution from each element has been found by backscattering from samples with one element shadowed off. (a) as-deposited. (b) annealed at 450°C for 5 min. in vacuum 210

LIST OF ILLUSTRATIONS (Cont'd)

Page

Fig. 79 Time constant effects in noise figure in GaAs FETs . . . 214

Fig. 80a Test set for measuring low-frequency transconductance of GaAs FETs 216

Fig. 80b Measured transconductance vs time characteristics for ion implanted, CVD and LPE GaAs FETs. 217

Fig. 81 a) Experimental setup
b) Noise equivalent circuit 233

Fig. 82 Fit of the experimental short cirucit current noise data of a uniform silicon IMPATT by Eq. (30) . . . 234

Fig. 83 Short circuit noise current at 30 MGz of a C-band, hard punch-on, LO-HI-LO, GaAs Read structure showing evidence of microplasmas 236

Fig. 84 Comparison of high current noise behavior 237

Fig. 85 Short circuit current noise data and theoretical fit of Eq. (30) for a GaAs flat profile IMPATT; for this diode $M_{pk} \approx 200$ and the saturation current is an order of magnitude larger than that of the silicon diode shown in Fig. 82 238

Fig. 86 Variation of multiplication and saturation current in an IMPATT diode as a function of the bias current . . 242

Fig. 87 Calculated mean square current fluctuation vs bias current for 30, 60, and 180 MGz 244

Fig. 88 Experimental mean square current fluctuation vs bias current at 30 MHz for diode Si 2-22 245

Fig. 89 Experimental mean square current fluctuation vs bias current at 420 MHz for diode Si 2-22 247

Fig. 90 Short circuit noise of a flat profile GaAs diode vs bias current at 30 and 420 MHz 247

LIST OF ILLUSTRATIONS (Cont'd)

Page

Fig. 91 Cell voltage vs time as a function of current density for buffered and unbuffered solutions 250

Fig. 92 Cell voltage vs time showing the direct proportionality of film growth rate to current density for a buffered solution 251

Fig. 93 a) Boundary conditions, for the non-punch-through diodes,
b) for the punch-through diodes 256

Fig. 94 Diode structure used in multiplication measurements . . . 259

Fig. 95 Experimental set-up for the multiplication measurements 261

Fig. 96 (a) Photoresponse of a diode, biased at M-1, (b) biased at M≈3 illustrating a non-uniform field building up at the top right corner of the diode 263

Fig. 97 Photoresponse of a diode, (a) biased at M≈1; (b) biased at M≈2; uniformity of multiplication over the whole area of the diode is better than 15% 264

Fig. 98 A plot of avalanche coefficients vs inverse of square of electric field before any adjustment was made 267

Fig. 99 Adjusted α and β vs inverse of square of electric field 269

Fig. 100 Normalized M_n and M_p vs reverse bias voltage for the high doping range diode 271

Fig. 101 Normalized M_n and M_p vs reverse bias voltage for the low doping range diode 272

Fig. 102 Plot of breakdown voltages vs donor doping for a one-sided abrupt junction 273

Fig. 103 GaAs band structure (from Ref. 104) 275

LIST OF TABLES

Page

Table 1 Flow chart of bulk Ga growth process 14

Table 2 Experiments performed to investigate boat wetting 19

Table 3 Impurity concentrations (in cm^{-3}) from mass spectrographic analysis 32

Table 4 Results of resistivity-Hall measurements at room temperature. 34

Table 5 The effect of saturation temperature on LPE GaAs Layers. 92

Table 6 The effect of H_2 flow rate on LPE GaAs layers 94

Table 7 Electrical properties at 300K of undoped and Cr-doped epitaxial layers grown in the SiO_2-BN-H_2 system . 103

Table 8 Data from five LPE layers grown under identical conditions 123

Table 9 Electrical properties of layers grown at 750°C 144

Table 10 Electrical properties of layers grown at 735°C 145

Table 11 Properties of layers grown at 700°C; due to GaAs crust on melt at growth temp 146

Table 12 Electrical parameters of layers grown at 665°C 151

Table 13 Cr-doped GaAs samples annealed at 850°C for 30 min. . 158

Table 14 Summary of RF measurements on FETs at 10 GHz 219

Table 15 Effect of a buffer layer on the rf performance of MESFETs 222

Table 16 RF performance of ion implanted MESFETs (#1003) 223

Table 17 Summary of IMPATT Data 240

Table 18 Summary of experimental conditions for ionization . . coefficient measurements. 266

Table 19 Summary of ionization coefficients 270

1.0 INTRODUCTION

Rapidly increasing needs for high speed communication systems and saturation of low frequency communication bands are responsible for an increasing demand for microwave devices capable of operation at X-band and above. The severe limitations of most silicon devices at the higher microwave frequencies make it imperative to look for other materials. The higher low field mobility and saturation velocity of GaAs compared to Si, plus the reduction of parasitic capacitance permitted by semi-insulating GaAs substrates, make GaAs an excellent material for high speed operation. However, GaAs technology is not as mature as silicon technology. At the inception of this program, there were serious difficulties in several areas of GaAs device technology despite the success of demonstration devices. Reproducibility problems were common in all key material areas such as substrate properties, submicron epitaxial layer growth and ion implantation doping. Problems were also apparent in such critical device areas as ohmic contacts and surface passivation.

In an attempt to attack some of the basic technologic problems, a broad research program was initiated. This program was very successful in combining the benefits of industry and university research. These two types of research which are usually conducted separately were joined in a team effort by having the Science Center as the prime contractor and three universities and a crystal growth laboratory as subcontractors. The Science Center offered a good balance between material growth, basic material research and device development, plus a direct

link with system demands and applications through Collins Radio and other electronic divisions of the Rockwell Corporation. The universities brought unique talents, Caltech in the field of ion implantation and ion beam analysis, Cornell in epitaxial growth and device physics, and Stanford in epitaxial growth. The inclusion of Crystal Specialties, a commercial manufacturer of bulk crystals, made substrate growth an integral part of the program.

The metal Schottky barrier field-effect transistor (MESFET), was chosen as a focal point test vehicle for the program. This is one of the most promising microwave devices, and it is also one that poses challenging material requirements due to its stringent specifications for ultra thin active layers and its sensitivity to substrate and surface problems. Although most of the efforts in this program were devoted to fundamental material problems, MESFET devices were fabricated at the Science Center using processing techniques developed under an IR&D FET program, and evaluated as one final test of progress made in the areas of material technology.

The major material areas covered by the program were growth and characterization of semi-insulating substrates, liquid phase epitaxial growth of ultra thin FET active layers and buffer layers, and formation of FET active layers and highly doped layers by ion implantation. All these research areas were intimately related to the MESFET device development. In addition, a small effort on the study of avalanche phenomena, of interest for IMPATT diode applications was also maintained. Major progress was made in all the research activities. This is summarized in the following section containing the highlights of the program.

A key result of this program is the high uniformity and reproducibility of doping profiles (10% in peak doping and depth) of FET layers made by Se implantation. Such results were accomplished employing a sputtered Si_3N_4 capping and annealing process and by developing a substrate preselection test. Note that the implantation is made directly into the semi-insulating substrate without any buffer layer. Avoiding a buffer layer simplifies fabrication, reduces cost, and assures better surface flatness. The above results are coupled with the achievement of good activation and high doping level with high dose Se and Te implants. (~ $4x10^{18} cm^{-3}$ maximum electron concentration and 65% activation for a close of $1x10^{14}$ Se ions/cm^2 at 400 keV). These achievements have brought GaAs ion implantation into maturity for device use, as demonstrated by the excellent performance of FET devices fabricated on ion implanted active layers. Test vehicle 1μm Schottky gate FETs fabricated from the ion implanted layers were found to have highly reproducible dc and RF properties and excellent low noise microwave performance (at 4, 10 and 15 GHz, minimum noise figures of 1.4, 2.6 and 3.4 dB, respectively with associated gains of 14, 8 and 7.5 dB respectively). This performance nearly matches the best results reported for laboratory devices of similar geometry made by VPE. Therefore, full advantage may be taken of the exceptional levels of reproducibility and uniformity attainable by ion implantation without compromising on device performance. In addition, implanted transistors are relatively free of drift problems frequently observed in epitaxial transistors.

In view of the success of this program in the development and application of a GaAs ion implantation technology, increased use of ion implantation for discrete FET devices is expected. Besides this immediate application, the importance of a reliable GaAs ion implantation technology must be weighed against the lack of a viable GaAs diffusion technology. Under this circumstance, ion implantation is the only technique capable of localized doping, a key step in the development of planar GaAs processing. The progress in ion implantation should, therefore, clear the way for development of a planar GaAs IC technology.

2.0 HIGHLIGHTS

Highlights of the results achieved in the various research areas will be presented in this section. The organization is similar to that of the main body of the report.

2.1 Semi-Insulating Substrate Material Growth

Crystal Specialties has played a dual role. (1) Supplying substrate materials for all the activities in this program, and (2) investigating growth of bulk semi-insulating GaAs. Semi-insulating GaAs crystals are grown by the horizontal Bridgmann technique. Typical ingots weigh ~ 1000 grams and yield ~ 2 square inch (100) wafers. An optimum range of Cr concentration has been determined ($3x10^{15}$ to $5x10^{16} cm^{-3}$). By using O to minimize silicon contamination, electrical compensation of the semi-insulating crystals is achieved in nearly 100% of the growth runs with such moderate Cr addition. Presently, the most important remaining yield limiting factor is boat wetting. Adherence of the crystal to the boat produces strain leading to polycrystalline growth. Although several causes of boat wetting have been identified, wetting is still responsible for yield fluctuations. A quite satisfactory monthly yield of 80% has been reached, but it has not been maintained for a long period of time. The average yield is ~ 50%.

2.2 Semi-Insulating Material Evaluation

This activity, carried out at the Science Center, covers two areas. In the first area, the study of bulk electrical properties, trans-

port measurements on bulk grown semi-insulating (SI) GaAs single crystals with three different Cr concentrations showed that the "conventional" model for the electrical sompensation, in which deep Cr acceptors compensated residual shallow donors was incorrect. A more elaborate model which included both a deep acceptor and a deep oxygen donor was proposed to consistently interpret the experimental data.

Also in the area of the study of bulk properties, a technique capable of yielding absolute concentrations of donors and acceptors has been developed. This technique combines standard current injection measurements with a technique for profiling the electrical potential at a semiconductor junction based on the measurement of shifts of Auger electron peaks in a scanning electron microscope. Preliminary results indicate that the donor and acceptor concentrations in Si GaAs are two orders of magnitude lower than the densities of impurities measured by mass spectroscopy, suggesting low electrical activity of the impurities.

In a second area, the study of surface stability, a Mn acceptor has been found in the p-type low resistivity layers formed on SI GaAs after heat treatment in epitaxial growth reactors. It has also been found that heat treatment in epitaxial reactors and heat treatment of samples capped as they would be for post-implantation annealing, lead to different effects, the low resistivity layers formed being p-type in the epitaxial case and n-type in the implantation case. It was also observed that substrates which qualified for epitaxial growth would not necessarily qualify for ion implantation.

2.3 Epitaxial Material Growth and Characterization

Liquid phase epitaxial (LPE) growth was carried out at Stanford University, the Science Center and Cornell University. The goal of Stanford's work was to grow semi-insulating buffer layers. Emphasis of this work was on understanding the interactions between the growth system components, the melt bakeout temperature and the incorporation of impurities in the layer. It was found that a precise bakeout procedure for the Ga melt before the growth was the most critical factor and that chemical reactions between the growth system components determined the compensation and concentration of the various impurities in the melt. Optimum growth conditions were determined for three growth systems. Cr-doping yielded semi-insulating layers after the critical bakeout temperatures had been identified. A resistivity as high as 1×10^6 ohm-cm was obtained with the system employing a BN growth cell in a graphite cradle. Transient capacitance measurements on FET layers showed absence of traps near the active layer-buffer layer interface in contrast with the observation of traps near the active layer-substrate interface when no buffer was used.

The Science Center work addressed the problem of growing ultra thin epitaxial layers. Layers grown using a "restricted melt" technique developed under this contract showed excellent uniformity and reproducibility. The typical standard deviation of thickness over 2.5cm^2 layers was 4% (for 5000Å layers). From wafer to wafer, five layers grown sequentially had 6% standard deviation of both their average thickness and their average carrier concentration.

The goal of the LPE effort at Cornell was to develop buffered FET structures. The approach relied on high purity undoped buffer layers, with emphasis on developing a multilayer growth capability. High purity buffer layers were grown using a graphite boat, by baking the boat and melt for an appropriate time after each exposure to the atmosphere. Total ionized impurity concentrations of $2x10^{14} cm^{-3}$ with 77K mobility of 160,000 cm^2/V-sec were reached. Uniform submicron FET layers were also grown. Careful removal of native oxides prior to growth was found to be critical for reproducible growth rates.

2.4 Ion Implantation and Ion Beam Analysis

Several areas were covered by this research effort, in close cooperation between the Science Center and Caltech. Implantation and annealing were done at the Science Center while ion beam analysis and layer evaluation were carried out mainly by the Caltech group.

A test employing Kr bombardment to preselect semi-insulating substrates for ion implantation doping has been developed. Reproducibility of carrier concentration profiles in preselected substrates from five different boules implanted with low doses ($2-3x10^{12}$ ions/cm^2) of Se ions was $\pm$ 10% in peak doping level and depth. This is an important result which facilitates the use of ion implantation directly into semi-insulating substrates to obtain reproducible n-type layers. All of the tested substrate boules grown from the elements (5 boules) passed the preselection tests, while only 13% of the boules regrown or grown using prereacted material were found qualified for implantation.

In high-dose Se and Te implantation, annealing conditions for optimum activation of the implanted ions were determined. Peak doping densities as high as $4 \times 10^{18} cm^{-3}$ with ~ 65% activation for a dose of 10^{14} ions/cm^2 at 400 keV were obtained by Se implantation. This result is important for the formation of low resistance contacts to devices using ion implantation. Based on results of photoluminescence measurements, correlations between doping efficiency and formation of Ga vacancy-selenium complexes were established.

High energy (400 keV) sulfur implants have shown greater doping efficiency than is obtained at low energy (100 keV). This is attributed to a lower probability of outdiffusion of the S during annealing when it is initially deeper in the GaAs, as is the case for a high energy implant.

Backscattering has been used to study the anneling behavior of amorphous layers caused by ion implantation revealing a reordering process different from the simple epitaxial regrowth found in Si and Ge. Backscattering techniques have also been employed in an investigation of the Au-Ge-Ni and Au-Ge-Pt systems commonly used for ohmic contacts on GaAs, showing that annealing causes Ge to combine with Ni or Pt even when there is Au between them.

2.5 MESFET Performance

At the Science Center, submicron Schottky barrier gate FETs (MESFETs) were fabricated for the evaluation of the material technologies. Excellent RF performance has been obtained on devices fabricated on Se

layers implanted into semi-insulating substrates at 4, 10 and 15 GHz, minimum noise figures of 1.4, 2.6 and 3.4 dB respectively, with associated gains of 14, 8 and 7.5 dB respectively, were measured for nominal 1μm gate length and 230μm gate width transistors. This performance is superior to that of LPE transistors fabricated under this contract; it is as good as that of the best 1μm gate commercially available devices, and it nearly matches the best performance reported for laboratory devices of similar geometry. In addition, the implanted transistors were relatively free from drift problems exhibited by epitaxial transistors. Implantantation into high purity buffer layers did not lead to improvements. On the contrary, buffered devices were inferior to devices made on layers directly implanted into qualified substrates.

2.6 Avalanche Parameters

At Cornell University, experimental measurements of the low frequency noise of IMPATT diodes have been successfully used to extract parameters such as intrinsic response time and multiplication factors under operating conditions of the diode, which can be exploited to improve device design. Measurements of ionization rates are strongly dependent on the doping concentration. An explanation based on the delay in promoting electrons to higher conduction bands before they have enough energy to produce secondary pair generation has been proposed.

3.0 SEMI-INSULATING SUBSTRATE MATERIAL

The performance of the FET devices is very dependent on the semi-insulating (SI) substrate due to the large surface to volume ratio of the device active layer. The substrate plays an even more critical role when the device active layer is made by ion implantation into the semi-insulating substrate without any buffer layer. In view of these circumstances, a significant amount of contractual effort has been invested in problems associated with the semi-insulating substrate. This activity has been carried out mainly at Crystal Specialties and the Science Center. The material was grown at Crystal Specialties. Most of the evaluation was done at the Science Center. This evaluation consisted not only of specific characterization procedures but also of feedback from the epitaxial growth and ion implantation activities, and ultimately, from the performance of FET devices.

This section is divided into two subsections. Section 3.1 covers bulk growth of SI GaAs, while Sec. 3.2 covers material evaluation, including the study of fundamental properties of the material and the development of new characterization techniques.

3.1 Bulk Growth of Semi-Insulating GaAs; Crystal Specialties

The objective of this research activity is to investigate the growth of semi-insulating substrate material, to improve the quality and yield of bulk grown GaAs single crystals, and to study the problems related to the electrical compensation of the material.

Semi-insulating (SI) GaAs is grown at Crystal Specialties by the horizontal Bridgmann technique. This technique shows advantages such as low cost of production, uniform crystal shapes and generally superior quality of the material produced. Figure 1 shows a schematic of the three-zone horizontal Bridgmann system used at Crystal Specialties. The ampoule containing the Ga and As is placed in the grower, and the growth zone is heated to 1240°C. After the melt and growth zones are stabilized the arsenic zone is slowly heated to 640°C. At this temperature the As sublimes and react with the molten Ga to form GaAs. The furnace is then removed toward the back end of the crystal at a rate of about 0.5 inch/hour. The furnace movement causes the temperature gradient to move, thus causing the molten GaAs to solidify onto the crystal seed. Table 1 is a flow chart of the overall production process used at Crystal Specialties. The preparation of materials and loading are done in a clean room. For the vacuum heat treatment and bakeout a turbo-molecular pump is employed. A liquid nitrogen trap is used to prevent any oil contamination.

Figure 2 shows a top and a bottom view of a Bridgmann grown single crystal which weighs approximately 1000 grams. A crystal of this size produces approximately 200 two square inch wafers of substrate material. Larger crystals could be grown if necessary. Semi-insulating single crystals of this size are routinely grown at Crystal Specialties. However, the yield is still irregular. Maintaining high yield requires to have two problems under control. One is to obtain good single crystals. The other is to achieve high resistivity.

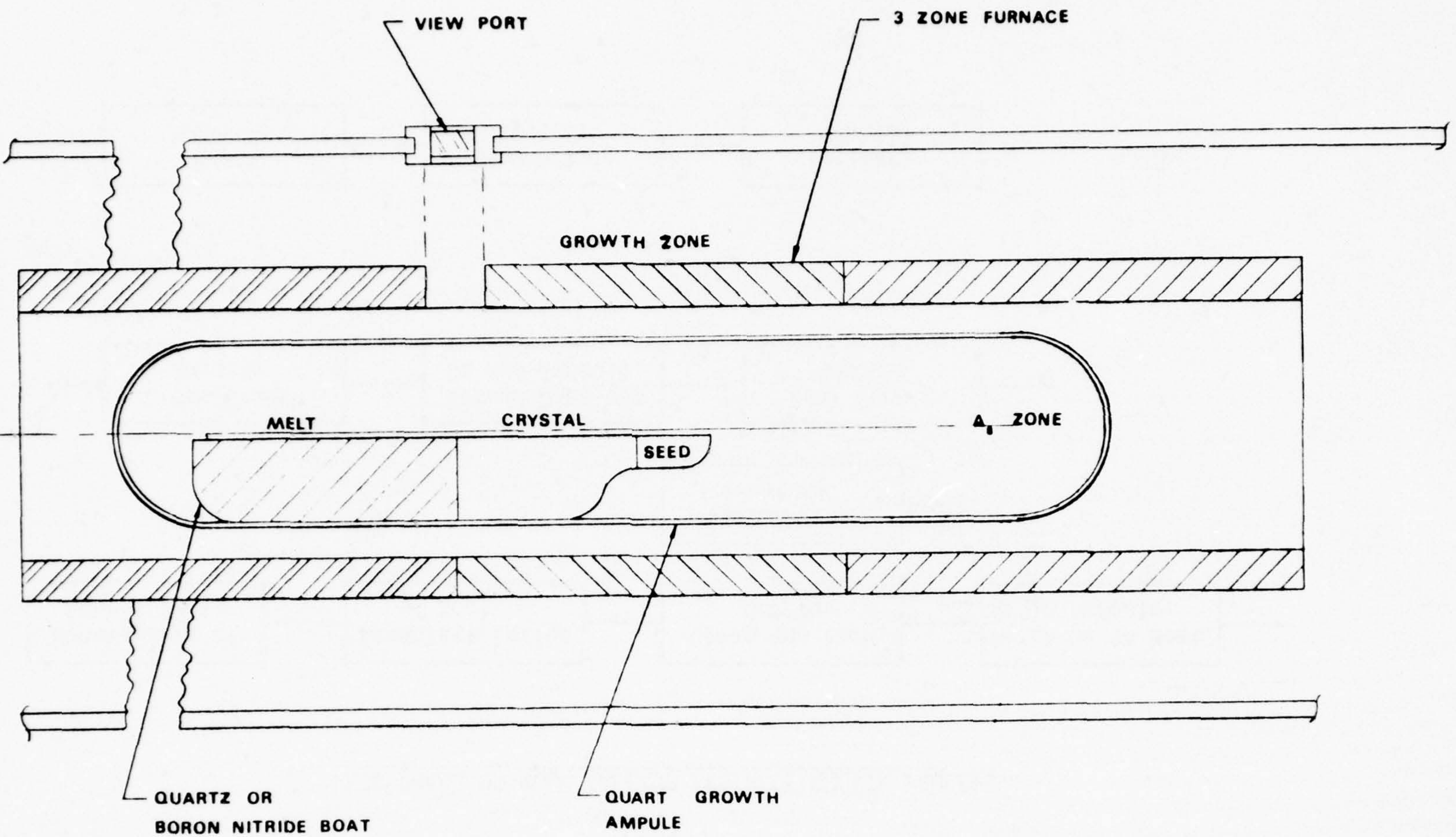
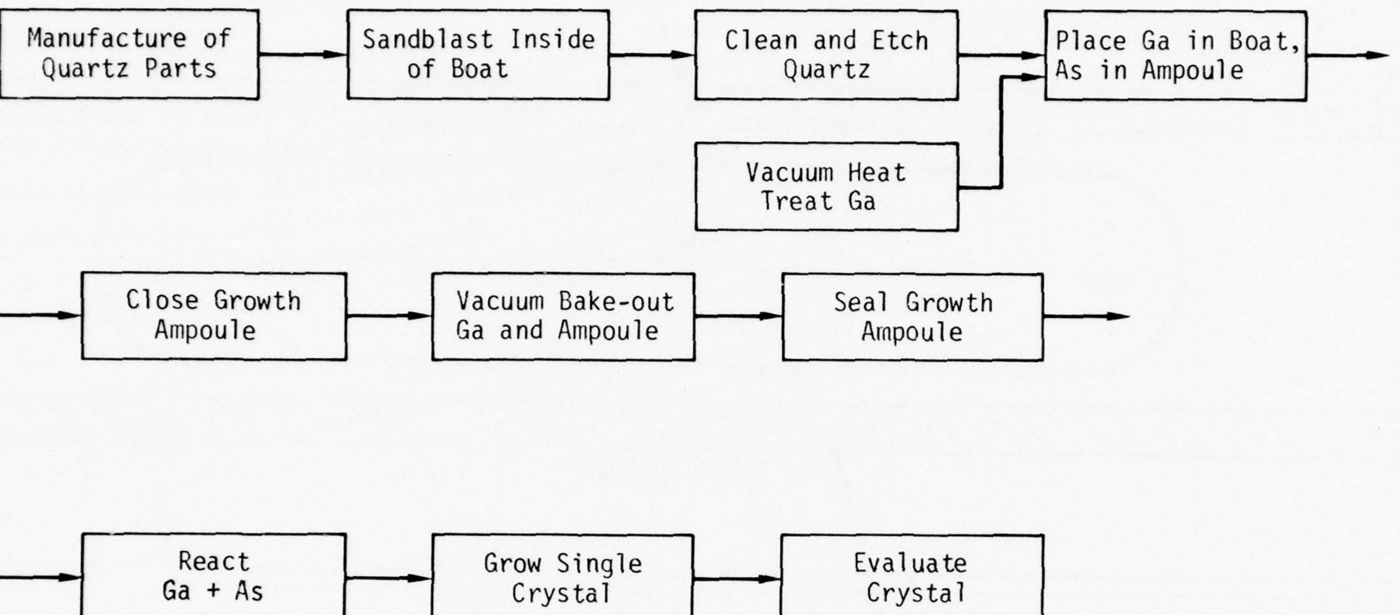


Fig. 1 Schematic of a three zone horizontal Bridgmann system

TABLE 1

FLOW CHART OF BULK GALLIUM ARSENIDE GROWTH PROCESS



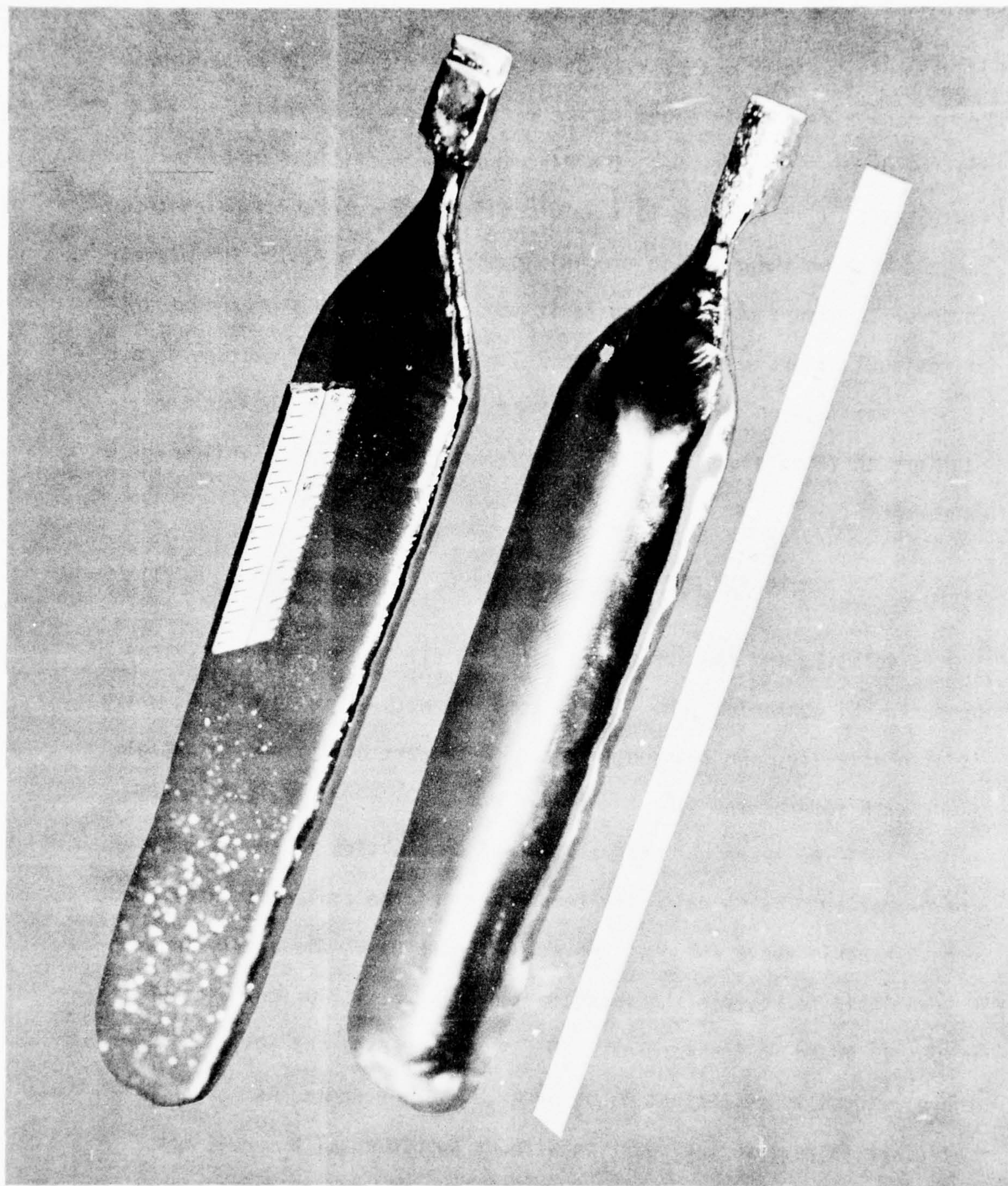


Fig. 2 Top and bottom view of a Bridgmann grown semi-insulating GaAs crystal.

The high resistivity of SI GaAs is obtained by compensation. Cr, a deep acceptor, is added to the melt to compensate residual shallow donors.[1] However, the distribution coefficient of Cr is low (6.4×10^{-4}),[2] limiting to $\sim 5 \times 10^{16} cm^{-3}$ the Cr concentration that can be used without incurring in precipitates (see Sec. 3.2.3). Therefore, in order to insure compensation it is mandatory to keep the concentration of residual donors sufficiently low. The major source of shallow donors is Si contamination from the quartz boat and growth ampoule. At the high growth temperature (1250°C), quartz breaks down in the following manner:

$$2SiO_2 \rightleftharpoons 2SiO + O_2 \qquad (1)$$

SiO is volatile and some of the Si finds itself in the GaAs melt, thus producing Si contamination. The O_2 combines with Ga to form Ga_2O_3 which is also volatile, and transports to the cool part of the growth ampoule along with some of the SiO.

The technique used at Crystal Specialties to suppress Si contamination[3] is to raise the temperature of the cool portion of the growth ampoule above 1000°C. Above 1000°C the Ga_2O_3 dissociates making O_2 available to reverse the reaction shown in Eq. 1. Oxygen can be purposely added in the form of Ga_2O_3, As_2O_3, or as a gas (O_2). However, there is usually sufficient Ga_2O_3 or As_2O_3 in the Ga and As source materials to reverse the reaction without supplemental O_2 additions. Since the As end of the ampoule must be kept below 600°C until all the As has reacted with the Ga melt, some Si is incorporated into the melt during this initial period. The final content is usually about $10^{15} cm^{-3}$,

which is quite tolerable. A Cr concentration higher than $3x10^{15}cm^{-3}$ is sufficient to insure compensation. To be on the safe side, a Cr concentration of $\sim 10^{16}cm^{-3}$ is normally used, but occasionally SI boules have been grown with Cr concentrations as low as $8x10^{14}cm^{-3}$.

The yield of compensated crystals (taken as the fraction of successfully grown single crystals which have $\rho > 10^7$ ohm/cm) has been increased from $\sim$ 40% at the beginning of this contract to virtually 100%. This improvement is thought to be the result of lower Si contamination achieved by improved pumping and outgassing of the ampoule.

While lack of electrical compensation has been eliminated as a cause of growth failure, the overall yield is still limited by the yield of single crystal material. Improvement of the crystalline quality of the material has been achieved by altering the ampoule backfilling procedure. Early in the program a gas such as N or He was metered into the evacuated ampoule. The amount of gas used was sufficient to produce one atmosphere at the growth temperature of GaAs. This gas was used to suppress vibration or turbulence of the molten GaAs caused by As escaping in the form of bubbles from the cooler portion of the melt. It was found however, that the gases used to suppress the turbulence also caused polycrystalline growth in the form of twinning. It is possible that the inert gas caused twinning because it was soluble in the molten GaAs, and H was therefore incorporated into the solidifying crystal, thus causing stress in the crystal lattice. A considerable improvement of overall yield (from 40% to 80%) occurred when overpressure of As was used instead of the backfill gas. However, it has not been possible to maintain the yield at such a high level.

The most severe problem affecting single crystal yield is boat wetting. This is a common problem of the horizontal method. Boat wetting is a condition where the growing crystal adheres to the quartz boat. As the boat and crystal begin to cool, the difference in contraction rates between the quartz and the GaAs causes a stress in the growing crystal. If the stress force is sufficient, the crystal lattice slips resulting in high dislocations, lineage, or a polycrystalline ingot.

In an attempt to identify the causes of boat wetting, a number of experiments have been conducted. Table 2 summarizes all the experiments that would increase boat wetting while others were attempts to inhibit wetting of the boat.

Moisture has been identified as a major cause of boat wetting. Intentional addition of H_2O to the GaAs melt causes gross and consistent boat wetting (Table 2). When Amersil quartz, which has high content of H_2O and OH is used for boat material, gross boat wetting also occurs. The high content of H_2O and OH in Amersil quartz is due to the use of a hydro-oxygen flame as heat source in the manufacturing process. General Electric 204 or 214 quartz has much lower H_2O and OH content because a carbon-arc is used instead of a hydro-oxygen flame in the manufacturing of the quartz tubes. The low OH content of the GE quartz makes it among the best thus far evaluated.

It has been suggested that heat treating the boats in high vacuum might reduce H_2O adsorbed on the surface of the quartz. No decrease in boat wetting was noted when boats were baked in a vacuum or in an inert gas atmosphere at 1000°C for 16 hours. Heat treating boats in air, however, increased boat wetting considerably. This increase in wetting

TABLE 2

Experiments Performed to Investigate Boat Wetting

Experiment	Number of Runs Made	Results
Ge 204 & 214 quartz; (melted with a carbon arc).		Variable boat wetting
Amersil quartz (melted with a hydro-oxygen flame).	10	Gross and consistent boat wetting
Heat treat Ge 204 quartz boat for 16 hrs @ 1000°C in vacuum. (1×10^{-6} Torr).	3	No noticeable improvement
Heat treat Ge 204 quartz boat for 16 hrs @ 1000°C in inert gas.	3	No noticeable improvement
Heat treat GE 204 quartz boat in air for 16 hrs @ 1000°C.	3	Gross and consistent boat wetting
Addition of H_2O to the load.		Gross and consistent boat wetting
Fabrication of boat while dry nitrogen is passed through quartz tubing.	3	No noticeable improvement
Growth of crystals in a low humidity room.	2	No noticeable improvement
Dry HCl etch of GaAs & boat after loading (at 800°C).	4	Consistent but light boat wetting
Etching of boat with 10% HF etch.	4	Gross and consistent boat wetting
Gallium from various suppliers.	∿ 3 each	No noticeable improvement
Arsenic from various suppliers.	∿ 3 each	No noticeable improvement
Doping of melt with aluminum (0.5 ppm).	2	Gross and consistent boat wetting
Coat boat with hexadecanol.	1	Gross boat wetting
Improve H_2O supply.		No noticeable improvement
Improve vacuum system.		No noticeable improvement

is thought to be due to increased adsorption of H_2O from the atmosphere on the surface of the quartz.

Since heat treating the quartz boat in air caused an increase in boat wetting, the possibility that H_2O could also be adsorbed at the surface of the boat during fabrication was explored. An experiment was performed where the quartz tubing was filled with dry nitrogen during glass blowing, thus eliminating any chance of H_2O adsorbtion from the air. However, when crystals were grown in these boats, no reduction of boat wetting occurrence was observed. A possible reason why there was no difference between the behavior of boats fabricated with and without being filled with dry nitrogen was that the H_2O adsorbed during the normal fabricating process was removed by the final sand blasting procedure.

It has been speculated that H_2O could diffuse through the quartz tube during the growth process. The fact that boat wetting occurs more often during the high humidity periods of the summer months lends credence to this idea. To test it, a furnace was placed in a room which could be dehumidified. The humidity was lowered from a relative humidity of 46% to a relative humidity of 11%. At the same time the temperature was reduced from 80°F to 45°F. The result was no change in the boat wetting condition. This test rules out diffusion of H_2O through the hot quartz ampoule as a leading cause of boat wetting.

It is standard practice for all quartz manufacturers to etch their quartz with a 10% solution of HF in H_2O. Since a 10% HF etch of the boat after sandblasting caused consistent gross wetting, it was suspected that etching of the quartz tubing by the manufacturer would also cause wetting. Quartz tubing which had not been HF etched was

therefore purchased from GE. However, crystals grown in boats fabricated from this tubing showed about the same degree and occurrence of boat wetting as crystals grown in the boats from the standard quartz. Probably, sandblasting of the boats removed the surface layer which had been exposed to the HF etch by the manufacturers.

Airborne contaminants or oxides formed on the Ga or GaAs loads have been considered as potential causes of boat wetting. To try to remove these contaminants, pre-reacted GaAs was etched in dry HCl gas after loading. The etching was done at 300, 600, and 800°C. The etch was performed by evacuation of the ampoule, heating it with the load to the desired temperature, and then backfilling the ampoule with dry HCl. After etching the ampoule was evacuated again and sealed off for growth. In each case there was not noticeable improvement as to boat wetting. It even appeared that the wetting was slightly more severe.

Impurities in the quartz could also cause boat wetting. One of the prime impurity suspects is aluminum since the quartz tubing contains about 50 ppm of Al_2O_3. In order to explore the effects of Al, melts were purposely doped with 0.5 ppm of Al. The effect was gross wetting. Therefore, variations in the Al_2O_3 content in the quartz are possibly a cause of variations in boat wetting conditions.

Since the amount of Al required to produce gross boat wetting (0.5 ppm) is close to the mass spectrographic detection limit in Ga, and since most Ga is a byproduct of Al refining, traces of Al in the Ga must be considered as another possible cause of boat wetting. Source materials from different manufacturers were compared. Ga from Alusuisse, Alcoa, Canyonlands, Cominco, and Eagle Picher, as well as As from

Hoboken, AS&R, Canyonlands, and Cominco have all been used. No conclusive results as to boat wetting were reached from these experiments. However, lack of any clear distinction in wetting of crystals which used material from different suppliers does not rule out the possibility that they all have a common problem. Therefore, Al in Ga as a cause of boat wetting still remains a distinct possibility which has to be further investigated.

Finally, the possibility that hydro-carbons produced by internal combustion engines could also be a cause of boat wetting was considered. I-Hexadeconol ($CH_3(CH_2)_{15}OH$) a hydro-carbon used as a base in hand creams and cosmetics, and found as a component of auto smog, was used to contaminate a boat. The contamination was caused by holding the boat over an open jar of heated I-Hexadeconal. Crystals grown from boats contaminated by I-Hexadecanol showed gross boat wetting.

In summary, the large series of experiments described had indicated that OH and H_2O adsorbed on the surface of quartz are major causes of boat wetting. Another potential cause, Al impurities in the Ga, has been identified, but further investigation will be required to determine whether it is a critical factor. The effect of hydro-carbons will also require further investigation. It must be noted that all these causes of boat wetting have been identified by increasing their effect.

However, a method of reducing boat wetting in a reproducible manner has not been found. This implies that either a major cause of boat wetting still remains to be identified, or that several factors among those analyzed above are interrelated.

The situation can be summarized as follows: The problem of electrical compensation has been solved by keeping the Si contamination low, thus allowing one to achieve compensation with the addition of only a moderate amount of Cr. When boat wetting does not occur, the overall yield is as high as 80%, and the crystals grown during these periods have low dislocation densities. Etch pit counts well below $10^4 cm^{-2}$ are found. Yet there is an uncontrolled problem of boat wetting which still hampers what would otherwise be a steady and reliable supply of semi-insulating substrate material. This problem requires further investigation.

3.2 Evaluation of Semi-Insulating Substrate Material

The evaluation of semi-insulating (SI) GaAs is much more difficult than the evaluation of low-resistivity semiconductors. Besides instrumental problems related to the high impedance of the samples, there are fundamental limitations. For example, due to the fact that SI GaAs is a compensated semiconductor, Hall and Van der Pauw measurements yield only concentration ratios instead of absolute concentrations of donors and acceptors, while capacitance measurements are limited by the large relaxation time of the material. Such fundamental restrictions, which severly restrict the use of the most common semiconductor characterization procedures, pose a formidable

challenge to any effort to evaluate Si GaAs. Despite the difficulties involved, significant progress has been made in understanding some of the fundamental properties of the material and in developing new characterization techniques. In the next section a study of transport properties will be presented. This study will show that not only Cr but also a deep donor, probably oxygen, interacts in the electrical compensation. In Sec. 3.2.2, a new method developed for the study of junctions of SI GaAs will be presented. This method, based on an application of Auger electron spectroscopy to the measurement of electrical potential profiles, can yield much needed absolute values of donor and acceptor concentrations in the material. In Sec. 3.2.3, a SIMS study of inclusions in SI GaAs, which will determine an upper limit for the acceptable Cr concentration, will be presented. In Sec. 3.2.4, the effects of the heat treatments of the substrates which occur in epitaxial growth and ion implantation processing will be analyzed.

3.2.1 Bulk Electrical Properties of Semi-Insulating GaAs-Science Center

In the early stages of development of semi-insulating (SI) GaAs, before Cr doping was used Blanc and Weisberg [4] proposed that oxygen, commonly used as an inhibitor of dissociation of the SiO_2 ampoule [3] was the principal compensating impurity. The validity of this model was

subsequently demonstrated by the doping experiments of Haisty et al.[5] After Cronin and Haisty[1] made the preparation of SI GaAs more reproducible by intentionally adding Cr, a deep acceptor, there has been a considerable drop of interest in the electrical compensation mechanism. In fact, no in-depth study of Cr-doped GaAs comparable to the work previously done on non-Cr-doped material has been reported. It has become tacitly accepted that the high resistivity of the material can be explained by compensation of residual shallow donors by the deep Cr acceptors.[6,7] This appears to be an over-simplification which ignores the use of oxygen in the growth of SI GaAs (see Sec. 3.1) and the proven role of O as a compensating impurity.[3,5] Published results of transport measurements[6-9] are not sufficient to clarify the problem.

To shed light on the compensation mechanism in Cr-doped SI GaAs, a series of transport measurements (Hall and resistivity versus temperature) was made to compare electrical behavior of samples with varying Cr concentration. The goal was to determine whether behavior differences could be explained by a simple model in which a deep Cr acceptor was solely responsible for electrical compensation. As the experimental data are analyzed, it will become clear that such a model is incorrect. An extension of Blanc and Weisberg's model[4] for non-Cr-doped SI GaAs, involving both a deep O donor and a deep Cr acceptor will be proposed to properly interpret the experimental data.

A general expression for the resistivity ρ of a semiconductor with two impurity levels, a donor and an acceptor, can be derived by

a simple calculation.[10] This leads to:

$$\rho^{-1} = (q\mu_e N_c/G)\exp\left[-(E_c - E_o)/kT\right] + q\mu_h N_v G \exp\left[-(E_o - E_v)/kT\right] \quad (2)$$

where

$$E_o \equiv (E_d + E_a)/2 \quad (3)$$

and

$$G \equiv \exp\left[(E_o - E_f)/kT\right] =$$

$$= (1/2g_a)\left\{-(1 - N_a/N_d)\exp\left[(E_d - E_a)/2kT\right] + \right.$$

$$\left. + \left[(1 - N_a/N_d)^2\exp\left[(E_d - E_a)/kT\right] + 4(N_a/N_d)g_d g_a\right]^{\frac{1}{2}}\right\} \quad (4)$$

Standard notation[11] *has been used in Eqs. (2) - (4).*

Eqs. (2) - (4) express the electrical resistivity as a function of temperature, and the density, energy level and degeneracy of donors and acceptors. These equations are valid regardless of whether the impurities are shallow or deep, and whether the donor and acceptor level are close to each orther or not. Although the above equations were derived for two impurity levels, they will be applied when more than two levels are involved. There is little loss of generality in assuming that only one donor and one acceptor have dominant contributions to the ionized impurity densities.

Two alternative models for the impurity level scheme of Cr-doped semi-insulating GaAs will be compared. First, the conventional model in which the only deep level is an acceptor, and second, a more elaborate model is proposed in which there is both a deep donor level and a deep acceptor level.

A. Deep Acceptor Model

In this model residual shallow impurities, which are mostly Si donors, are compensated by Cr acting as a deep acceptor. The acceptor densigy N_a must always be larger than the residual donor density N_d, otherwise the Fermi level would lie close to the donor level and be near the conduction band. Figure 3(a) describes the model. The density of free electrons, n, the density of free holes, p, the density of ionized donors, N_d^+, and the density of ionized acceptors, N_a^- are plotted in Fig. 3 on a logarithmic scale as functions of the position of the Fermi level in the band gap.[11] The Fermi level is at point F, the intersection of the curves for N_d^+ and N_a^-, to satisfy charge neutrality.[10,11] Since the concentrations of free electrons, n, and free holes, p, represented by points N and P, respectively in Fig. 3(a) are much smaller than N_d^+ and N_a^-, they are neglected in the charge neutrality condition.

Cr-dopes SI GaAs can display either n- or p-type conduction at room temperature.[7,9] It is difficult to account for such dual behavior with the deep acceptor model. Since the position of the Cr-acceptor level E_a is fixed, the only parameter varying from one crystal to another is the compensation ratio N_a/N_d. In principle, as N_a/N_d takes

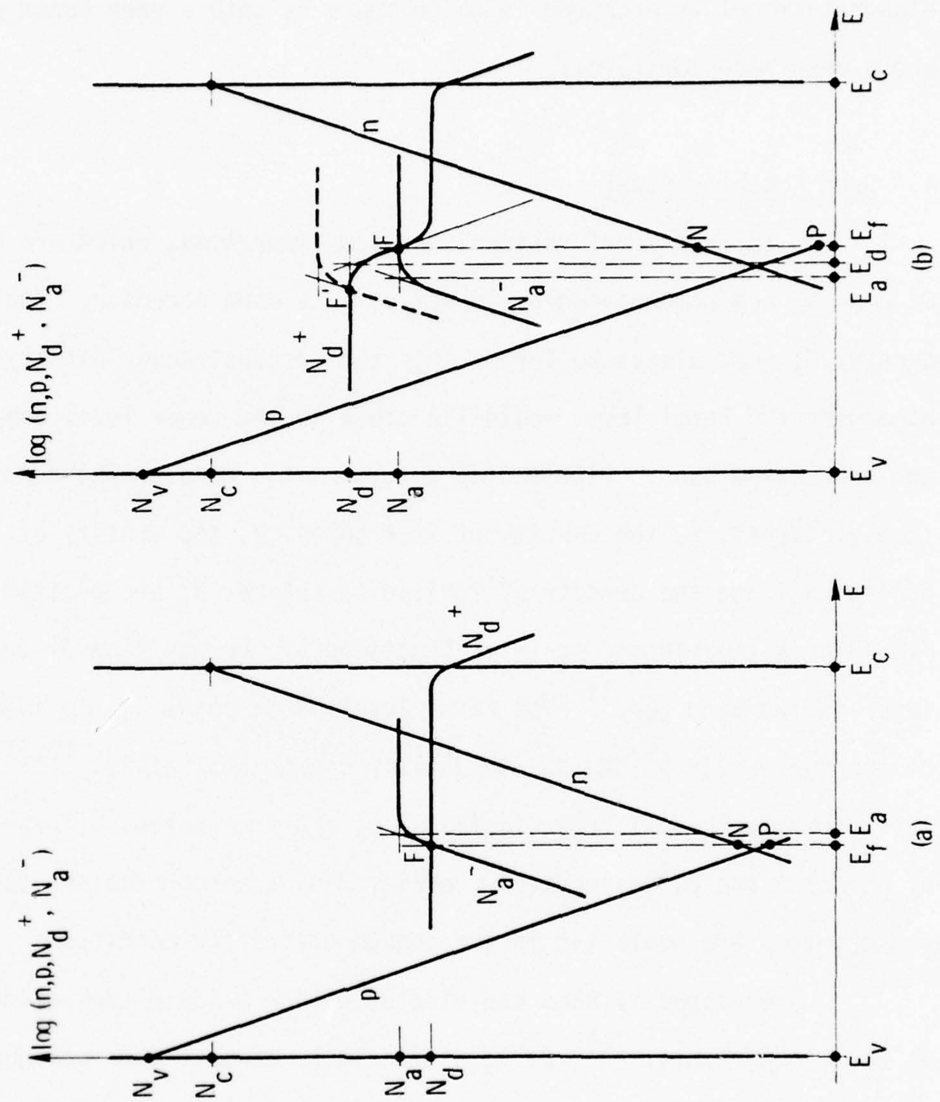


Fig. 3 Graphic representation of n, p, N_d^+ and N_a^- as functions of the position of the Fermi level in the energy gap; (a) for the deep-acceptor model, (b) for the deep-donor-deep-acceptor model.

on different positions in the energy gap, making the electron and hole concentrations (points N and P in the figure) change in opposite directions, leading to electron or hole conduction dominance. In reality, however, the range over which N_a/N_d may vary is narrow, only a few orders of magnitude, and is severely limited by practical restrictions on the concentrations of Cr that can be incorporated into the material (Secs. 3.1 and 3.2.2).

For the analysis of some of the experimental results, an analytical expression for the electrical resistivity of n-type samples will be needed. Dropping the second term, the hole current, from the right hand side of Eq. (2) and also neglecting the second term in the square root of Eq. (4) since $(E_d - E_a)/kT \gg 1$ for this model, Eqs. (2) and (4) reduce to a simple expression for the resistivity ρ

$$\rho = (q\mu_e N_c g_a)^{-1}(N_a/N_d - 1)\exp\ (E_c - E_a)/kT \quad . \tag{5}$$

This simplification assumes that all the donors are ionized ($N_d^+ \simeq N_d$), because the Fermi level is located many kT's below the shallow donor level.

B. Deep-Donor-Deep-Acceptor Model

In this model, there are both deep Cr acceptors and deep donors associated with oxygen impurities. As discussed earlier in this section, the main reason for considering a two-deep-level model, despite its complexity, is that O present in the growth ampoule as an inhibitor of quartz dissociation (Sec. 3.1) is likely to participate as a dopant in the electrical compensation. The two-deep-level model proposed here is an extension of

the model proposed by Blanc and Weisberg[4] and demonstrated by Haisty et al[5] for oxygen doped SI GaAs. The main difference is that in Blanc and Weisberg's model the role played here by our deep Cr-acceptor level is played by a shallow acceptor. Therefore, in the Blanc and Weisberg model, the density of deep donors must always be higher than the density of acceptors. In contrast, in our model the acceptor level is deep, allowing the density of deep donors N_d to be larger or smaller than the density of deep acceptors N_a.

Our model is described by Fig. 3(b). The curve that represents N_d^+ is obtained by superposition of a simple curve for the shallow donors and a similar curve for the deep donors. The Fermi level is at F, the point of intersection of the curves for N_d^+ and N_a^-, so that the condition of charge neutrality, is satisfied. Figure 3(b) was drawn for the case when $N_d > N_a$. In this case, the Fermi level (point F) is above E_d in the energy gap, its position depending on the ratio between the densities of deep donors and deep acceptors N_d/N_a. The case when $N_a > N_d$ can be visualized in Fig. 3(b) by raising the curve that represents N_a^- above that for N_d^-, to the position shown with a dashed line. The intersection of N_d^+ and N_a^-, which again determines the Fermi level, is now at F' below E_a in the energy gap. Therefore, depending on whether $N_d > N_a$ or $N_a > N_d$, the Fermi level may move from above E_d to below E_a. The range over which the Fermi level may vary as a function of realistic impurity concentrations is broader than in the former model, making this model more suited for explaining the existence of either n- or p-type Cr-doped SI material.

For the analysis of some of the experimental results, an expression for the electrical resistivity of n-type material will be needed, as with the previous model. The only simplification of Eqs. (2) and (4) without loss of generality is dropping of the second term from the right hand side of Eq. (2). However, in the limiting cases when either $N_a >> N_d$ or $N_d >> N_a$, the second term in the square root of the right hand side of Eq. (4) can be considered of second order with respect to the first. Retaining only first order terms in Eq. (4), and substituting into Eq. (2), leads to:

$$\rho = (q\mu_e N_c g_a)^{-1}(N_a/N_d - 1)\exp\left[(E_c - E_a)/kT\right] \; ; \; N_a >> N_d \qquad (6)$$

$$\rho = (q\mu_e N_c)^{-1} g_d (N_d/N_a - 1)^{-1}\exp\left[(E_c - E_d)/kT\right] \; ; \; N_d >> N_a \; . \qquad (7)$$

These simplifications assume that all the donors are ionized ($N_d^+ \simeq N_d$) when $N_a >> N_d$, or that all the acceptors are ionized ($N_a^- \simeq N_a$) when $N_d >> N_a$. Eq. (6) is identical to Eq. (5) derived for the deep-acceptor model because once it is assumed that all the donors are ionized, the position of the Fermi level does not depend on whether the donors are deep or shallow.

Samples were prepared from three boules of SI GaAs at Crystal Specialties, each having a different Cr concentration. Table 3 shows the results of a mass spectrographic analysis of the two boules with the highest and lowest Cr concentration. The low-Cr samples contain $5x10^{15} cm^{-3}$

Table 3

Impurity Concentrations (in cm^{-3}) From Mass Spectrographic Analysis.

Element#	Boule 1718 Low-Cr	Boule 2000 High-Cr
N	$2x10^{15}$	$2x10^{15}$
Al	$2x10^{15}$	$2x10^{15}$
Si	$3x10^{15}$	$1x10^{15}$
S	$2x10^{15}$	$4x10^{15}$
K	$2x10^{15}$	$2x10^{15}$
Cu	$2.8x10^{16}$	N.D.
Cr	$5x10^{15}$	$5.8x10^{16}$

Cr atoms, which is just above the $3\times10^{15}cm^{-3}$ threshold of Cr concentration required for high resistivity material (Sec. 3.1). The high-Cr samples contain $5.8\times10^{16}cm^{-3}$ Cr atoms, which is considered the upper bound for Cr concentration, since the high-Cr samples showed incipient Cr precipitation in secondary ion mass spectroscopy measurements (Sec. 3.2.3). The mid-Cr samples (from boule 2312) contained $1.2\times10^{16}cm^{-3}$ Cr atoms, estimated from the amount of Cr added to the melt.

Room temperature measurements of resistivity and Hall constant were made on the high-, mid- and low-Cr samples, using a Van der Pauw configuration. Table 4 summarizes the results. All the samples have high resistivity, between 3.4×10^{8} ohm-cm and 1.1×10^{9} ohm-cm. The low-Cr material is n-type with a free electron density $n = 3.6\times10^{6}cm^{-3}$ and a Hall mobility of 520 cm^2/V-sec. The mid- and high-Cr materials have a negative Hall constant as if *they were n-type, with low apparent Hall mobility* μ_H, indicating mixed conduction. From a mixed conduction analysis of the data,[12] and assuming that the mobility ratio $b \equiv \mu_e/\mu_h$ is equal to 10 (see Ref. 7), the values of N, p, μ_e and μ_h listed in Table 4 are obtained.

If the resulting values of n, p, μ_e and μ_h for the high-Cr material are used to calculate the conductivity, the hole contribution $qp\mu_h$ is only 1.4 times larger than $qn\mu_e$. In summary, there is a gradual shift from n-type to p-type conduction as the Cr concentration of the samples increases. This observation is in agreement with both models described earlier in this section because in both models an increase of the density of Cr acceptors tends to displace the Fermi level toward the valance band.

Table 4

Results of resistivity-Hall measurements at room temperature.

	Low-Cr	Mid-Cr	High-Cr
ρ(ohm-cm)	3.4×10^{8}	1.1×10^{9}	3.8×10^{8}
$R_H(cm^3C^{-1})$	-1.8×10^{12}	-9.5×10^{11}	-1.2×10^{11}
$\mu_H(cm^2V^{-1}sec^{-1})$	5200	850	320
Type	n	p	p
$n(cm^{-3})$	3.6×10^{6}	9.2×10^{5} a	4.6×10^{5} a
$p(cm^{-3})$		1.3×10^{7} a	2.7×10^{7} a
$\mu_e(cm^2V^{-1}sec^{-1})$	5200	2500 a	5200 a
$\mu_h(cm^2V^{-1}Sec^{-1})$		250 a	520 a

(a) Calculated assuming $b = \mu_e/\mu_h = 10$ (see Ref. 7)

In order to sort between the two models, the resistivity of the samples was measured as a function of temperature. These data are plotted in Fig. 4. Notice that the resistivity decreases very rapidly when the temperature increases, to the extent that it falls into the 10^3 - 10^4 ohm-cm range at 200°C.

Before applying Eqs. (2) to (7) to fit the ρ vs T data, the implicit temperature dependence of the equations through the parameters N_c, N_v, μ_e, μ_h, E_d and E_a must be considered. The temperature dependence of N_c and N_v, just proportional to $T^{3/2}$, is corrected for by plotting $\rho T^{3/2}$ instead of ρ. As to the mobilities μ_e and μ_h, Look [7] observed that the Hall mobility of a Cr-doped semi-insulating GaAs crystal was constant in a temperature range similar to that of our experiment. Assuming that such behavior applies to our samples as well, the mobilities μ_e and μ_h will be treated as temperature independent. As to the relative energy positions of the impurity levels $E_c - E_d$, $E_c - E_a$, etc., it is assumed that they remain proportional to the energy gap as it changes with temperature. Instead of correcting the energies for thermal variations, the correction is made on kT, taking advantage of the fact that the energy differences are always divided ty kT in the equations. Lacking information on the values of the degeneracy factors g_d and g_a for deep impurity levels in GaAs, [13] the values $g_d = g_a = 1$ are chosen.

A. Low-Cr Case

In comparing the low-Cr data of Fig. 4 with the predictions of the models, only the contribution of the electrons to the electrical conduction needs to be considered because the material is n-type as indicated

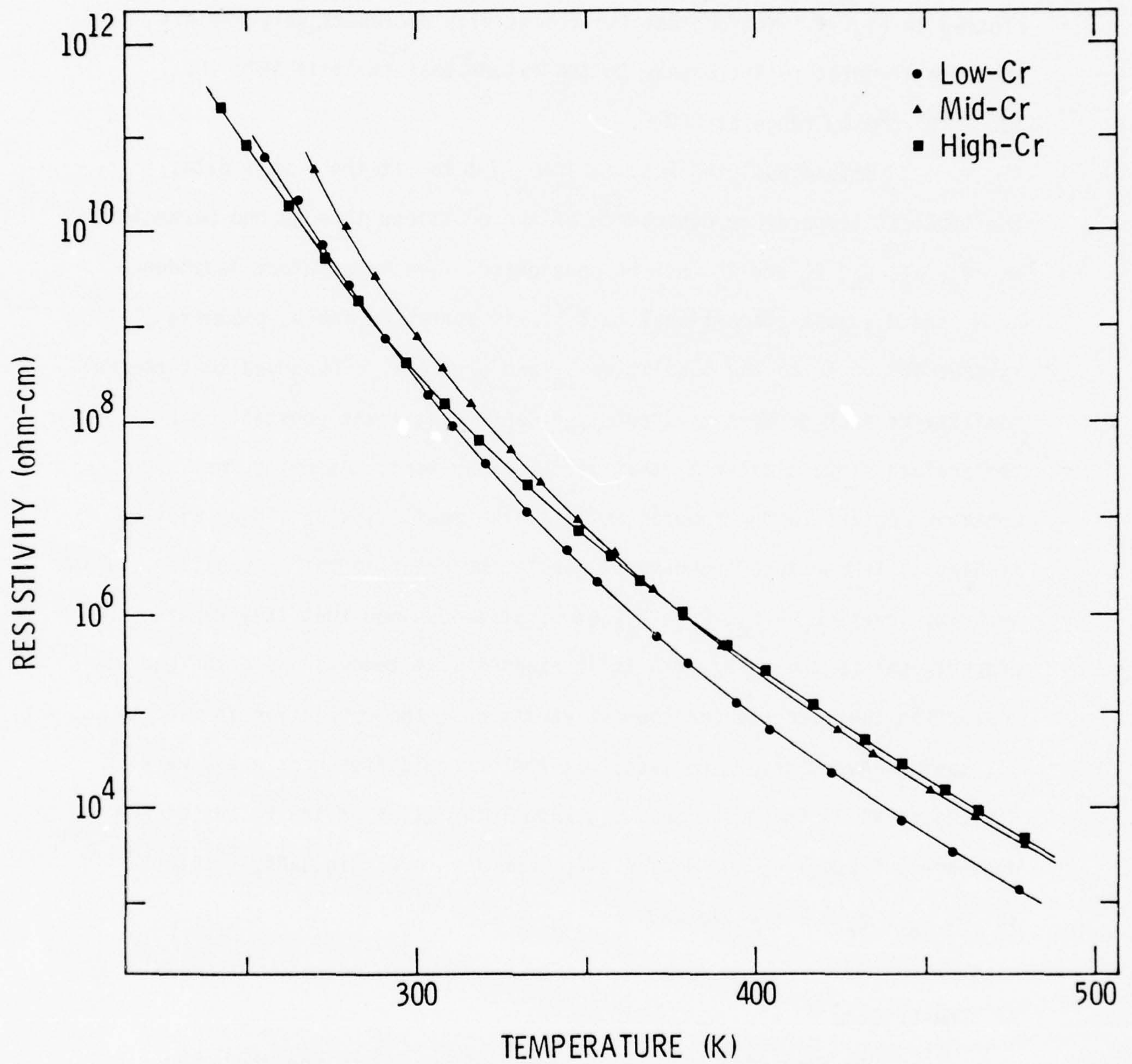


Fig. 4 Resistivity vs. temperature data.

by the Hall measurement discussed earlier. Under this circumstance, Eq. (5) subject to the condition $N_a > N_d$ applies for the deep-acceptor model, while Eqs. (6) and (7) apply for the deep-donor-deep-acceptor model. All three equations predict pure exponential behavior of the resistivity. The temperature corrections discussed earlier in this section are performed by replotting in Fig. 5 the data from Fig. 4 with new scales log $\rho T^{3/2}$ and $1/T'$. A linear least square fit of the low-Cr data is shown with solid lines in Fig. 5. The fit is excellent indicating that the criteria used in deriving the equations and correcting the data were appropriate. The low-Cr data are fit by:

$$\rho = 1.08T^{-3/2}\exp(8380/T')\text{ohm-cm} \quad , \tag{8}$$

where T and T' are in degrees kelvin.

Comparing Eq. (8) with Eqs. (6) and (7) for the deep-donor-deep-acceptor model, Eq. (7) becomes identical to Eq. (8) by choosing $N_d/N_a = 14$ and $E_c - E_d = 0.72$eV. This is the situation described in Fig. 3(b), with the Fermi level at point F, near the deep donor level. The value $E_c - E_d = 0.72$eV is in excellent agreement with the position of a deep donor level in O-doped GaAs determined from measurements of thermal activation energy,[5] luminescence,[14] and photocapacitance.[15] It is possible to make Eq. (5) for the deep-acceptor model identical to Eq. (8) by choosing $N_a/N_d = 1.07$ and $E_c - E_a = 0.72$eV. This is approximately the situation described by Fig. 3(a), with the Fermi level, determined by point F, between the deep acceptor level and the conduction band. However, this alternative would not lead to a consistent interpretation of the results for all three Cr concentrations.

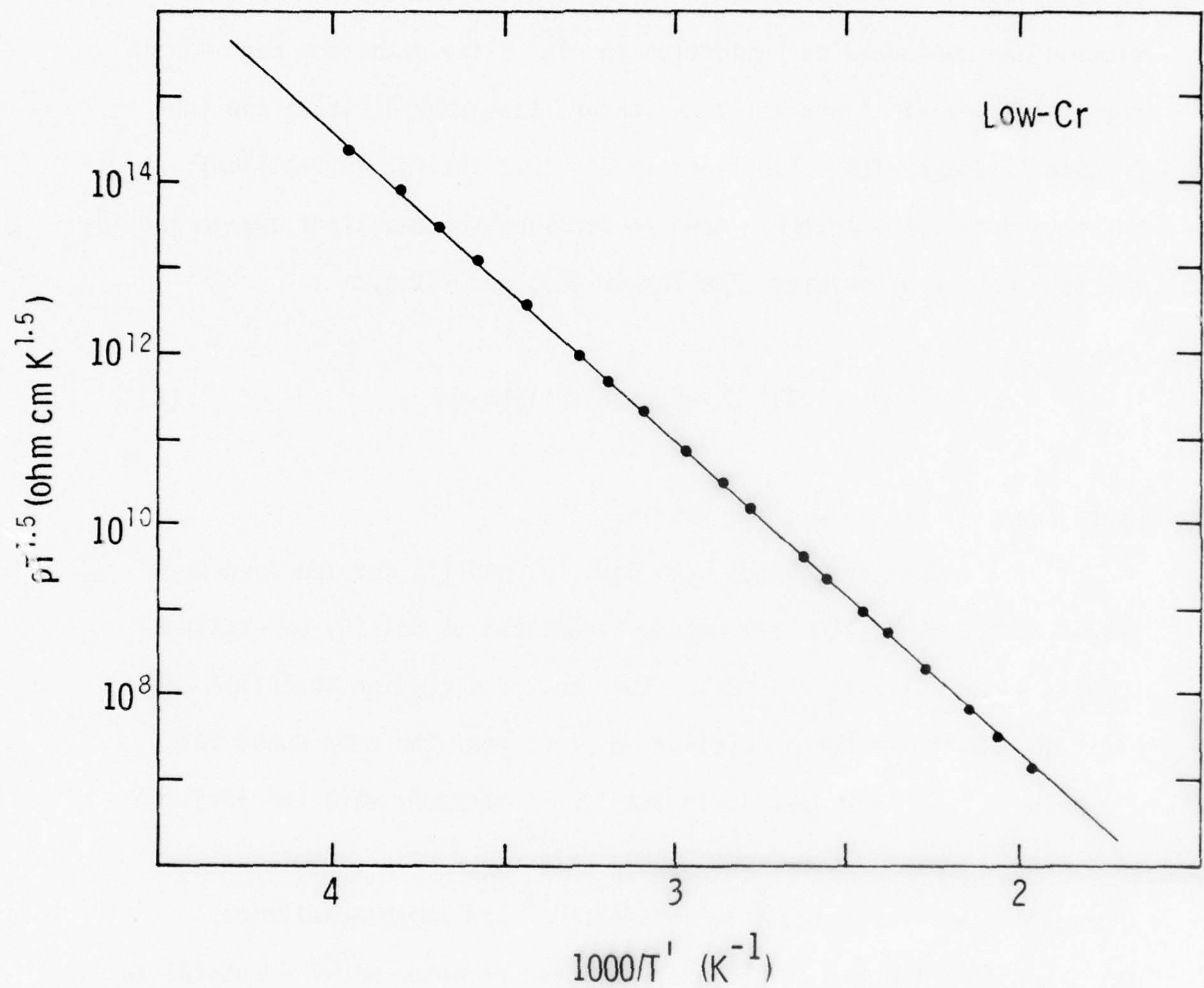


Fig. 5 Plot of $\rho T^{3/2}$ vs. 1/T' for the low-Cr data of Fig. 2. The temperature scale was corrected for the effect of the thermal variation of the energy gap, $T' = T\,E_g(298K)/E_g(T)$. The solid line is the result of a linear least square fit.

B. Mid-Cr Case

Since the mid-Cr material exhibits mixed conduction (see Table 4), the full expression of the resistivity given by Eqs. (2) - (4) must be used, requiring a non-linear least square fit. The following procedure is used to find the optimum fit to log $\rho T^{3/2}$ vs 1/T'. After replacing in Eqs. (2) and (4), the numerical values of N_c and N_v and the mobilities (Table 4), and assuming $g_d = g_a = 1$, a fit is made using N_a/N_d and $E_c - E_a$ as the adjustable parameters for a given value of $E_c - E_d$. This is repeated several times to find the value of $E_c - E_d$ which gives the minimum error. The excellent fit shown in Fig. 6 is obtained with $E_c - E_d$ = 0.64 eV, N_a/N_d = 0.98 and $E_c - E_a$ = 0.90 eV. The value $E_c - E_a$ = 0.90 eV is 0.06 eV higher than the energy of the Cr level determined by optical experiments.[16-19] The value of $E_c - E_d$ is 0.06 eV lower than the value determined in the low-Cr case. Such differences are a measure of the overall error margin of this work, a satisfactory margin given the simplifying assumption on the temperature dependence of some of the parameters and on the degeneracy of the levels.

Figure 7 shows how the results of the non-linear fit procedure depend on the value assigned to $E_c - E_d$. The mean square deviation ε is plotted against $E_c - E_d$ along with the resulting values of N_a/N_d and $E_c - E_a$. The curve for ε shows how sensitive the fit is to the position of the donor level. The minimum for ε at $E_c - E_d$ = 0.64 eV proves that for a good fit of the experimental data, the deep-donor-deep-acceptor model must be used. If $E_c - E_d \sim 0$ is chosen in Fig. 7 (i.e., shallow donors), which is the assumption of the deep-acceptor model, the error ε would increase by a factor of almost two and $E_c - E_a$ would become incompatible with the photoluminescence data on the Cr level.[16,17]

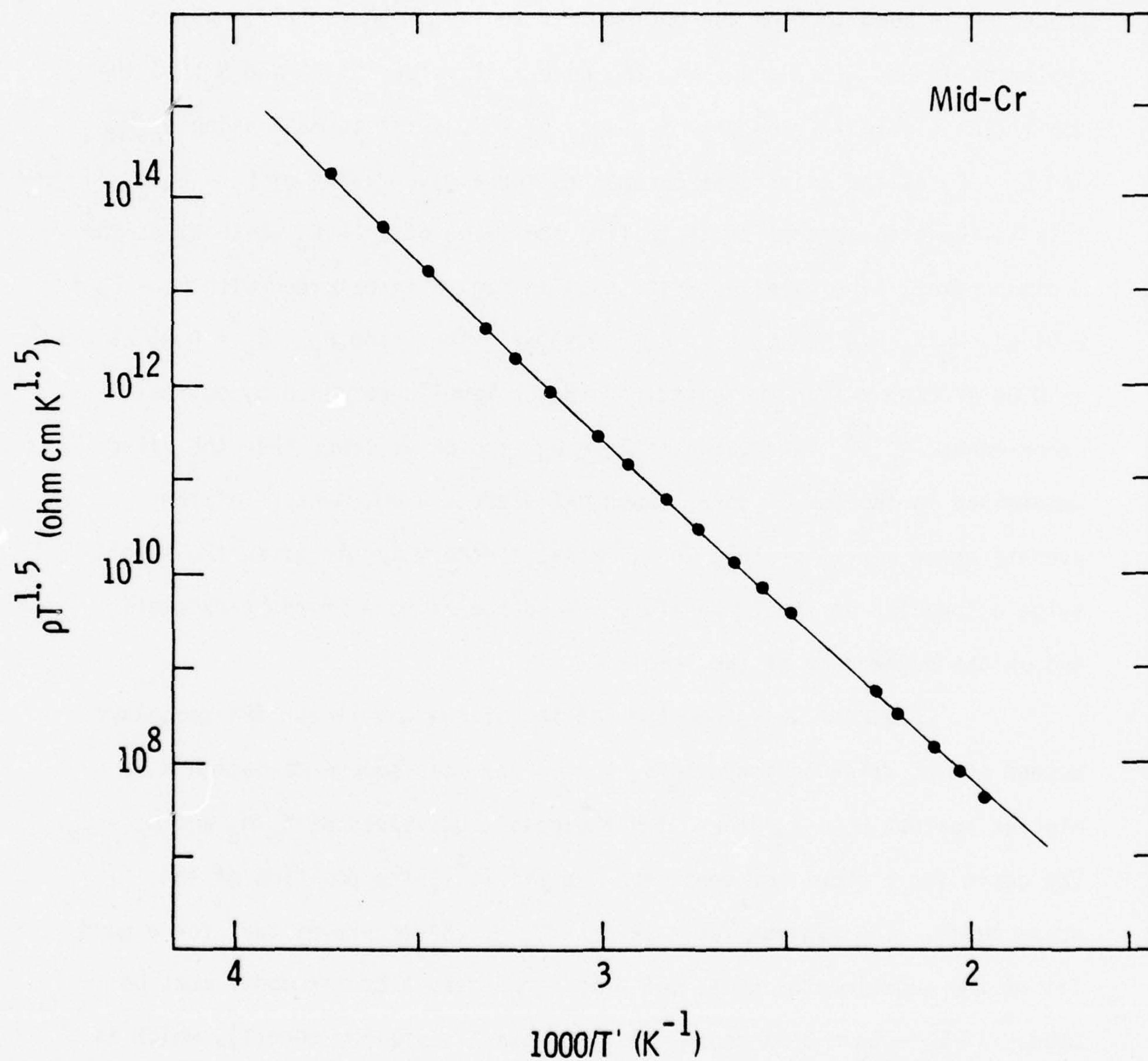


Fig. 6 Result of a non-linear least square fit of the mid-Cr data for $E_c - E_d = 0.64$ eV. Fitting parameters: $N_a/N_d = 0.98$; $E_c - E_a = 0.90$ eV. The dots represent the experimental points.

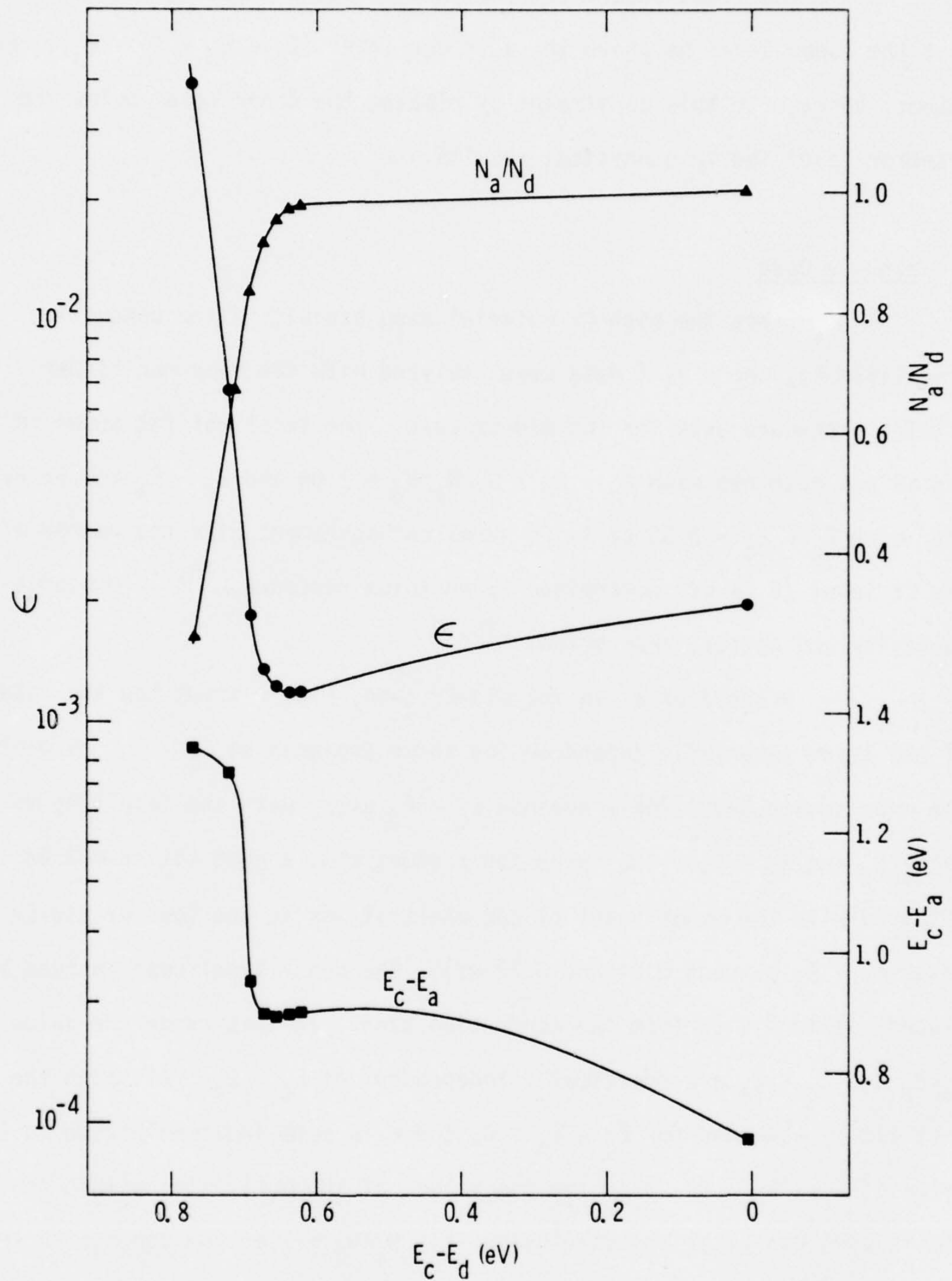


Fig. 7 Plot of the mean square error ϵ and the fitting parameters N_a/N_d and $E_c - E_a$ against the parameter $E_c - E_d$ in the non-linear least square fit of the mid-Cr data.

The least square fit analysis was done imposing the constraint that the donor level be above the acceptor level ($E_c - E_d \leqslant E_c - E_a$). An attempt to reverse this constraint by placing the donor level below the acceptor level led to unphysical results.

C. High-Cr Case

Since the high-Cr material also exhibits mixed conduction (see Table 4), the ρ vs T data were analyzed with the same non-linear fitting procedure used for the mid-Cr case. The excellent fit shown in Fig. 8 was obtained with $E_c - E_d = 0$, $N_a/N_d = 1.04$ and $E_c - E_a = 0.83$ eV. The value $E_c - E_a = 0.83$ eV is in excellent agreement with the energy of the Cr level (0.84 eV) determined by photoluminescence,[16,17] photoconductivity and optical abdorption.[18,19]

Proceeding as in the mid-Cr case, Fig. 9 shows how the results of the lease square fit depend on the value assigned to $E_c - E_d$, by plotting the mean square deviation ε agains- $E_c - E_d$ along with the resulting values of N_a/N_d and $E_c - E_a$. The curve for ε shows that a good fit cannot be obtained with the donor level placed where it was in the low- or mid-Cr case ($E_c - E_d$ between 0.64 and 0.72 eV). The donor level must instead be placed within 0.4 eV from the conduction band. In this range the values of N_a/N_d and $E_c - E_a$ are practically independent of $E_c - E_d$. Although the best fit is obtained for $E_c - E_d = 0$, there is some indetermination in the value of $E_c - E_d = 0$. Changing the values of the mobilities within reasonable limits does not alter the conclusion that $N_a/N_d > 1$ or the conclusion that the donors are located within 0.4 eV from the conduction band where the curves in Fig. 9 are almost flat. Not being aware of any deep donor species within 0.4 eV from the conduction band, leads to conclude that the donor level is shallow.

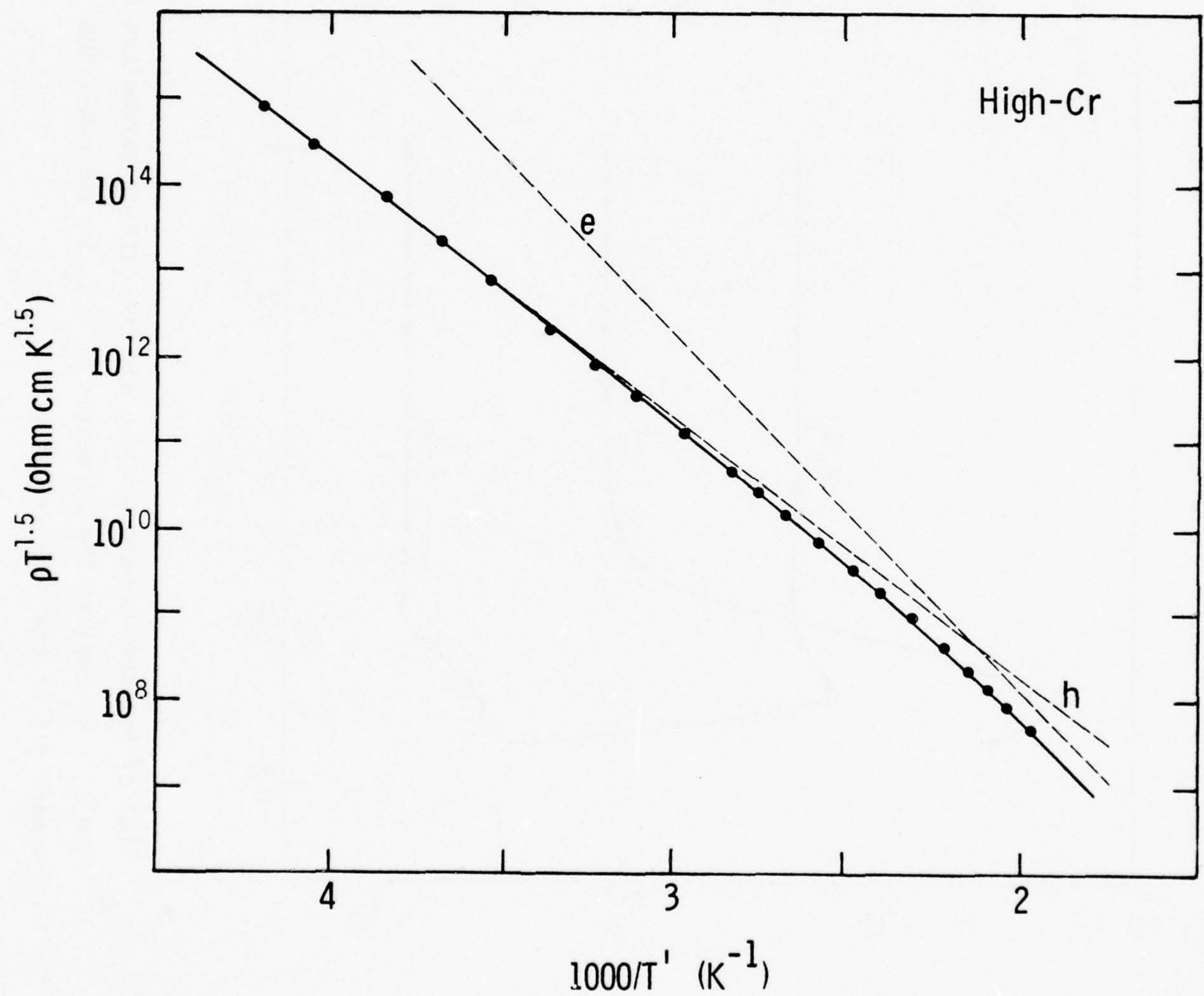


Fig. 8 Result of a non-linear least square fit of the high-Cr data for $E_c - E_d = 0$. Fitting parameters: $N_a/N_d = 1.04$; $E_c - E_a = 0.83$ eV. The dots represent the experimental points. The dashed lines represent the separate contributions of electrons and holes.

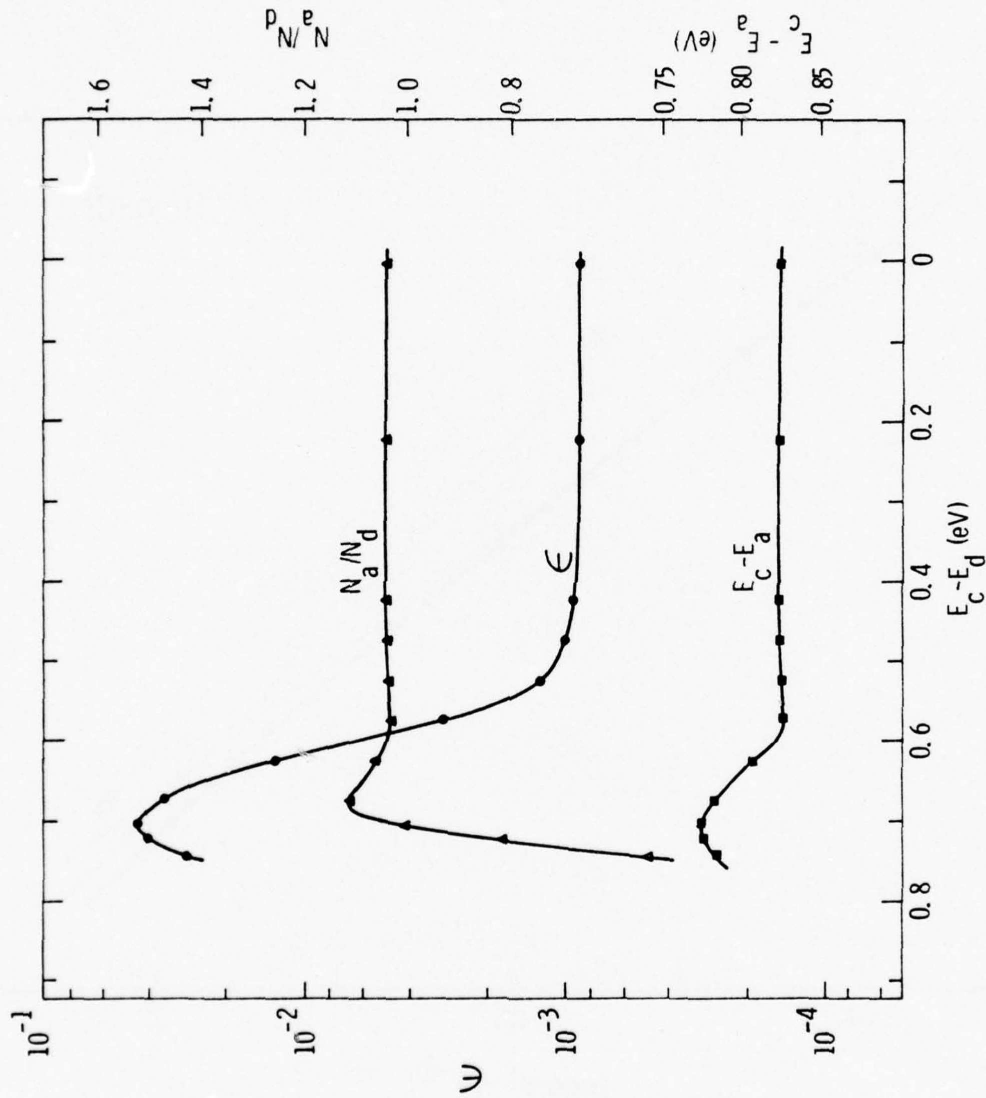


Fig. 9 Plot of the mean square error ε and the fitting parameters N_a/N_d and $E_c - E_a$ against the parameter $E_c - E_d$ in the non-linear least square fit of the high-Cr data.

When the results from the three samples are compared, it becomes clear that the low- and mid-Cr cases follow a simple trend well in agreement with our deep-donor-deep-acceptor model. The low-Cr sample is n-type with dominant deep O donors and N_d/N_a = 14. As the Cr concentration is increased, in the mid-Cr case, N_d/N_a decreases to near 1, and the two dominant deep levels, the deep O donors and the deep Cr acceptors are identified. The high-Cr case does not follow the predicted trend. A further decrease of N_d/N_a and a still dominant role of the same two deep impurities would be expected when going from the mid- the high-Cr case. Instead, N_d/N_a remains nearly 1, and while the dominant acceptor is Cr as expected, the dominant donor specie is shallow.

The anomalous behavior of the high-Cr sample can be explained with the aid of the mass spectrographic data of Table 3 . In the first place, what would be the simplest explanation for the prominent role of the shallow donors,namely that the high-Cr samples have more Si impurities than the other samples, must be discarded. According to the mass spectrographic data (Table 3), the low- and high-Cr samples have nearly equal concentrations of Si impurities. We therefore suggest that the O concentration of the high-Cr sample is anomalously low leaving the shallow donors as the prominent donor specie. Large fluctuations in O concentration can easily occur because this concentration is very sensitive to growth conditions (Sec.3.1). Unfortunately, this hypothesis can not be contrasted with the mass spectrographic data because spark mass spectroscopy O measurements are unreliable. It is possible to account for the high-Cr N_d/N_a remaining

almost unchanged despite the increased Cr concentration from the mid- to high-Cr sample and the just proposed decrease of O donor concentration, by the lack of Cu in this specimen (Table 3). Since Cu acts as an acceptor,[20] it participates in the total balance between donors and acceptors. The lack of Cu in the high-Cr case would counterbalance the increase of Cr acceptors and the decrease of O donors.

In conclusion, it has been shown that with some knowledge of the material composition and of impurity energy levels, it is possible to interpret and model the electrical compensation of SI GaAs by means of ρ vs T measurements. SI GaAs crystals with several Cr concentrations have been compared. The interpretation of the data from the low- and mid-Cr material requires a deep donor level located between 0.64 and 0.72 eV from the conduction band. The presence of this deep donor level implies that the "conventional" model with deep Cr acceptors compensating residual shallow donors is not correct. A three level model for Cr-doped SI GaAs was proposed, the three levels being the residual shallow donor and deep Cr acceptor levels, plus an additional deep donor level. This model can interpret all the experimental data. Based on comparisons with O-doped GaAs, it is proposed that the deep donor level is associated with oxygen impurities. An intrinsic limitation of this work, common to transport measurements on compensated semiconductors, is that it can only yield compensation ratios. Efforts to determine separate values of N_a and N_d by profiling the electrical potential at junctions of SI material with n- and p-type layers will be discussed in the next section.

3.2.2 Potential Profiles at Semi-Insulated Substrate-Epitaxial Interfaces - Science Center

The electrical properties of the junction formed between the active layer of an FET device and the semi-insulating (SI) substrate are of great importance in modeling the device operation. If the electrical characteristics of the impurities in SI GaAs were well known, the electrical properties of this junction could be predicted. Unfortunately, simple methods to determine the absolute concentrations of shallow and deep impurities in SI GaAs are lacking. One of the techniques capable of determining concentrations of deep impurities in high resistivity materials, namely, the observation of current injection phenomena, depends very heavily on good knowledge of the injecting contacts for the interpretation of the results.

Our application of high spatial resolution Auger electron spectroscopy (AES) to determine the potential profiles across p-i-p and n-i-n GaAs structures (i stands for SI GaAs) under dc voltage bias to thereby study the electrical properties of p-i and n-i junctions will now be described. This technique has interest for the study of the FET active layer-substrate interface. If depletion regions are identified, values of N_d-N_a in the semi-insulated substrate can be determined.

In AES, an exciting beam of electrons of several keV energy (the primary)beam is directed at the surface of a solid and the resulting secondary electron spectrum is energy-analyzed with an electron spectrometer. Over the energy range of 0-1500 eV the secondary electron spectrum exhibits discrete peaks (hence, Auger electron spectrum) whose positions

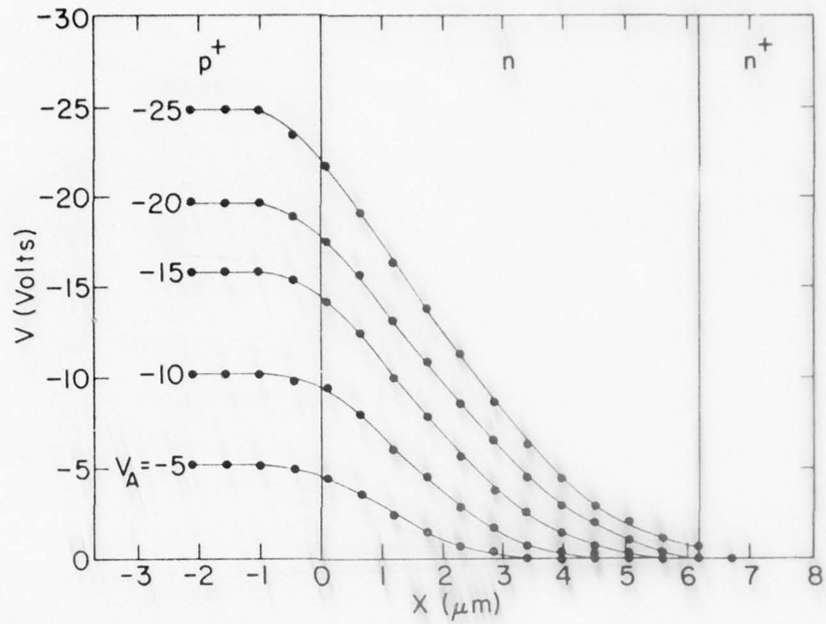
are characteristic of the particular elements present in the surface region excited. It has been demonstrated, however, that a given Auger electron peak will shift linearly in energy in direct correspondence to an electrical potential applied to a specimen.[21] If the relative shift of a peak at different points across a dc-biased specimen is measured using high spatial resolution AES, the potential profile across the specimen can be obtained.

Our experiments employ an ultra-high-vacuum scanning electron microscope (SEM) constructed in this laboratory for high spatial resolution (< 1μm) AES work. Operating parameters for the AES-SEM system during the experiment were 20 kV beam voltage, 20 nA beam current, and 9×10^{-10} Torr chamber pressure. Spatial resolution in the potential measurements and the micrographs is ~ 0.75μm. The accuracy of the potential measurement is ~ 1V.

The procedure is to first use the system as a SEM to obtain a secondary electron micrograph of the specimen over a region of interest. Next, the finely-focused (< 1μm) primary beam of the SEM is computer-controlled to digitally step in a sequence of discrete points along a chosen line on the specimen. At each point, the derivative[22] of the Auger electron peak of C (or, for some sequences, O) is recorded. (Any specimen examined by AES, even in an ultra-high-vacuum system such as ours, will normally have C and O peaks unless specially cleaned under vacuum). The shift in energy of the Auger electron peak when voltage is applied to the specimen is measured for every point. The shifts are then calibrated against the shifts caused by known potentials applied to a metal electrode. The potential at each point on the line scan can, then, be associated with the specimen geometry recorded on a secondary electron micrograph. A test (conducted on IR&D funds) on a

well-characterized GaAs p-n junction, showed excellent agreement with the predicted profiles for different bias voltages,[23] as shown in Fig. 10. The value of $N_d - N_a$ calculated from the slopes of the $V^{1/2}$ vs X curves agreed within 20% with the result of a C-V measurement.[23] These results indicate that the primary electron beam specimen interaction does not radically affect the measurement, and that the surface potential profile is similar to that of the bulk. This demonstrates the reliability of this new and powerful technique for the study of semiconductor junctions.

The AES-SEM technique was applied to the same low-Cr and high-Cr materials which had been characterized by the transport measurements described in Sec. 3.1.1, made on samples from Crystal Specialties boules 1718 and 2000. The specimens for this experiment were taken from positions in the boules near those of the samples used for the transport measurements as a precaution against variations of impurity densities along the boules. The n- and p-type contacts for the n-i-n and p-i-p samples were prepared by liquid phase epitaxial growth of heavily doped layers on each side of the SI substrate material. Epitaxial contacts were chosen despite the difficulties involved in two-sided epitaxial growth because they form well defined interfaces. After the first contact layer was grown, the substrates were thinned to 60-80μm by lapping and etching, and a second layer was grown on the side opposite to the first layer. Circular Cr-Au contacts were evaporated onto one side, and the other side was completely covered with Cr-Au. Mesas were etched, centered on the circular contacts, until nearly full separation of the diodes. Separation was completed by cleaving. Figure 11 shows an SEM micrograph of an n-i-n sample.



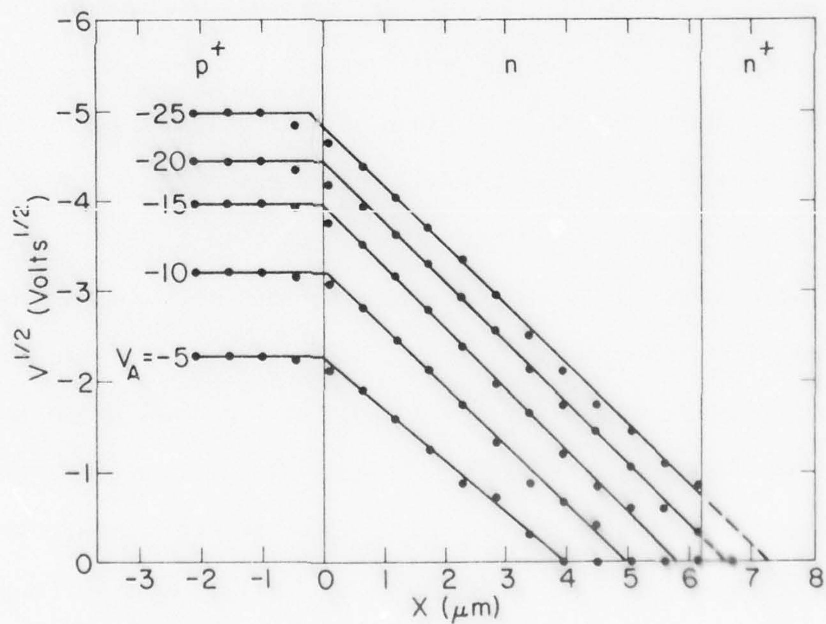


Fig. 10 Measured potential profiles across a p^+, n, n^+ junction ($p=10^{18}cm^{-3}$, $n=7.5\times10^{14}cm^{-3}$). (a) V vs x for reverse bias between -5 and -25 V. (b) $V^{\frac{1}{2}}$ vs x; dots: experimental points; lines: linear least-mean-square fits. (reprint from Ref. 23)

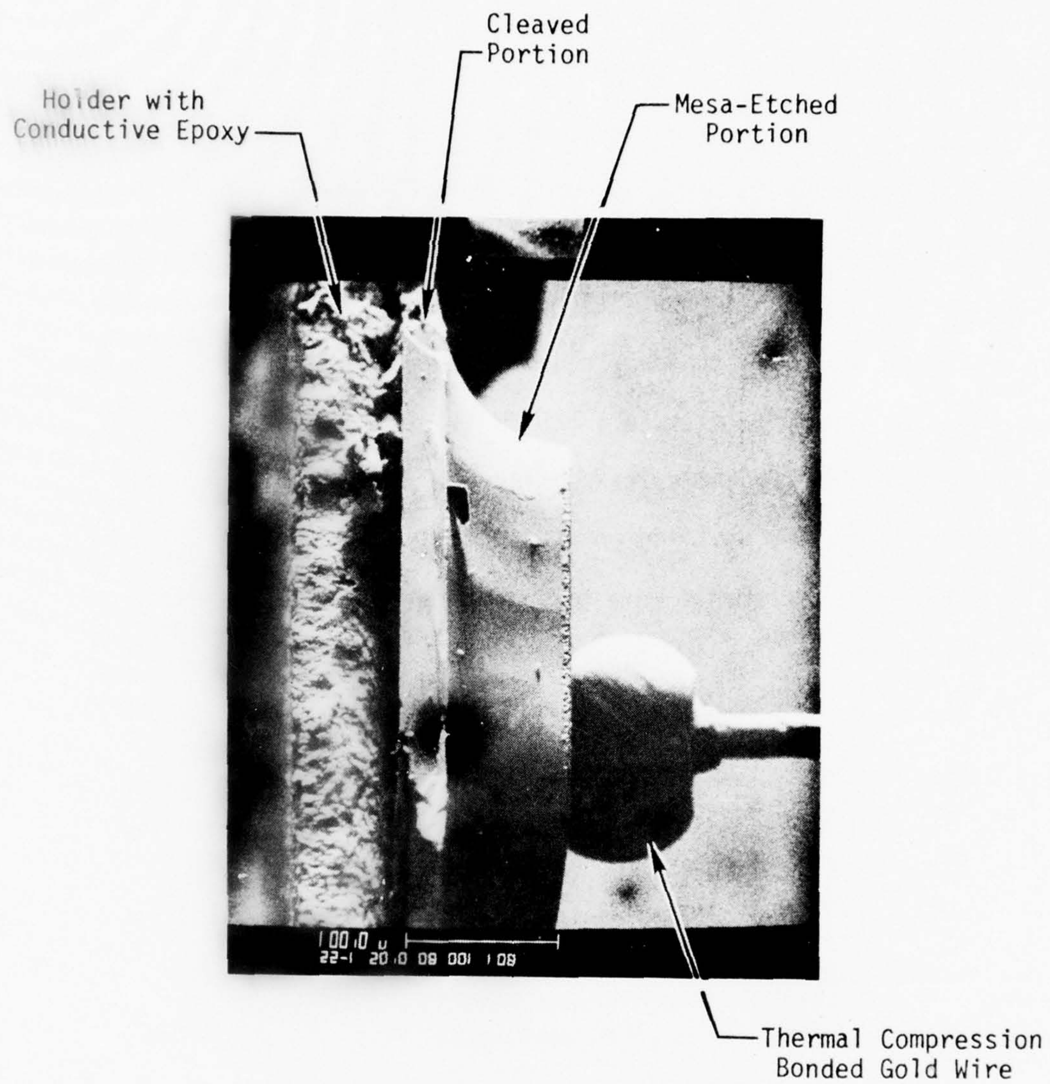


Fig. 11 SEM micrograph of a typical specimen for AES-SEM measurements

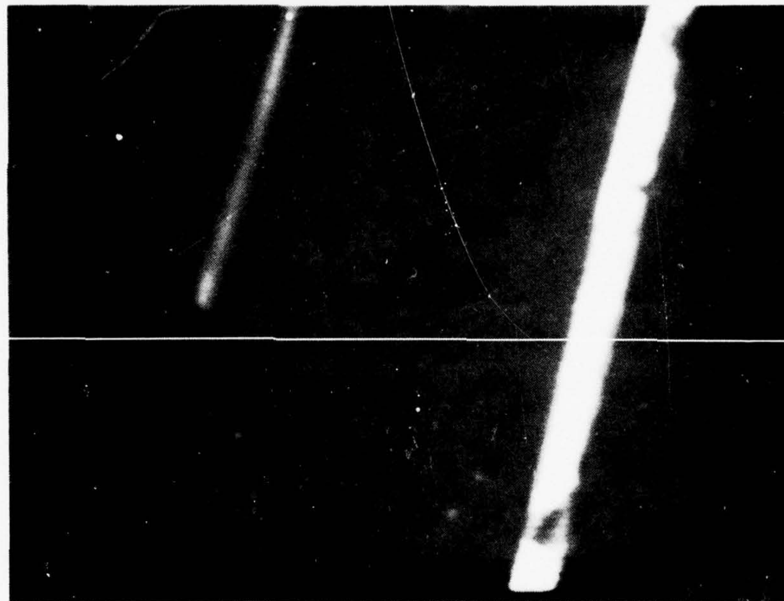
Cathodoluminescence in the SEM was used to determine without ambiguity the location of the interfaces between the substrate and the epilayers. This application of cathodoluminescence takes advantage of the low intensity of band gap luminescence of SI GaAs, in contrast with the normal luminescent intensity of the epitaxial layers. Figure 12 shows two SEM photographs of the specimen in the same position and with the same magnification. In one picture a secondary electron detector is used to see the specimen, while in the other picture a photomultiplier with an S-1 photocathode is used to identify the epitaxial layers. The validity of this technique was confirmed by staining on a disposable sample.

AES-SEM measurements were performed on all samples. The experimental results identify two distinct cases: a) the low-Cr p-i-p and hign-Cr n-i-n case; b) the low-Cr n-i-n and high-Cr p-i-p case. These two cases will be discussed separately.

a) Low-Cr p-i-p and High-Cr n-i-n Case

Figures 13(a) and 13(b) show the potential profiles of the low-Cr p-i-p sample and the high-Cr n-i-n sample for several bias voltages and for both polarities. The voltage profiles resemble those of the reverse biased diode shown in Fig. 10, therefore indicating the existence of a depleted contact in each case. In the low-Cr (n-type) p-i-p sample (Fig. 13a), the voltage drops near the p-type cathode, that is; a) when the left side (sample top) is biased negative, the voltage drops near the left side; b) when the right side is biased negative, the voltage drops near the right side. Notice that the vertical

(a)



(b)

Fig. 12 Measurement of sample thickness by cathodoluminescence. (a) Normal scanning electron micrograph taken with a secondary electron detector; (b) Same as (a) in the cathodoluminescence mode using a photomultiplier with S-1 photocathode as detector.

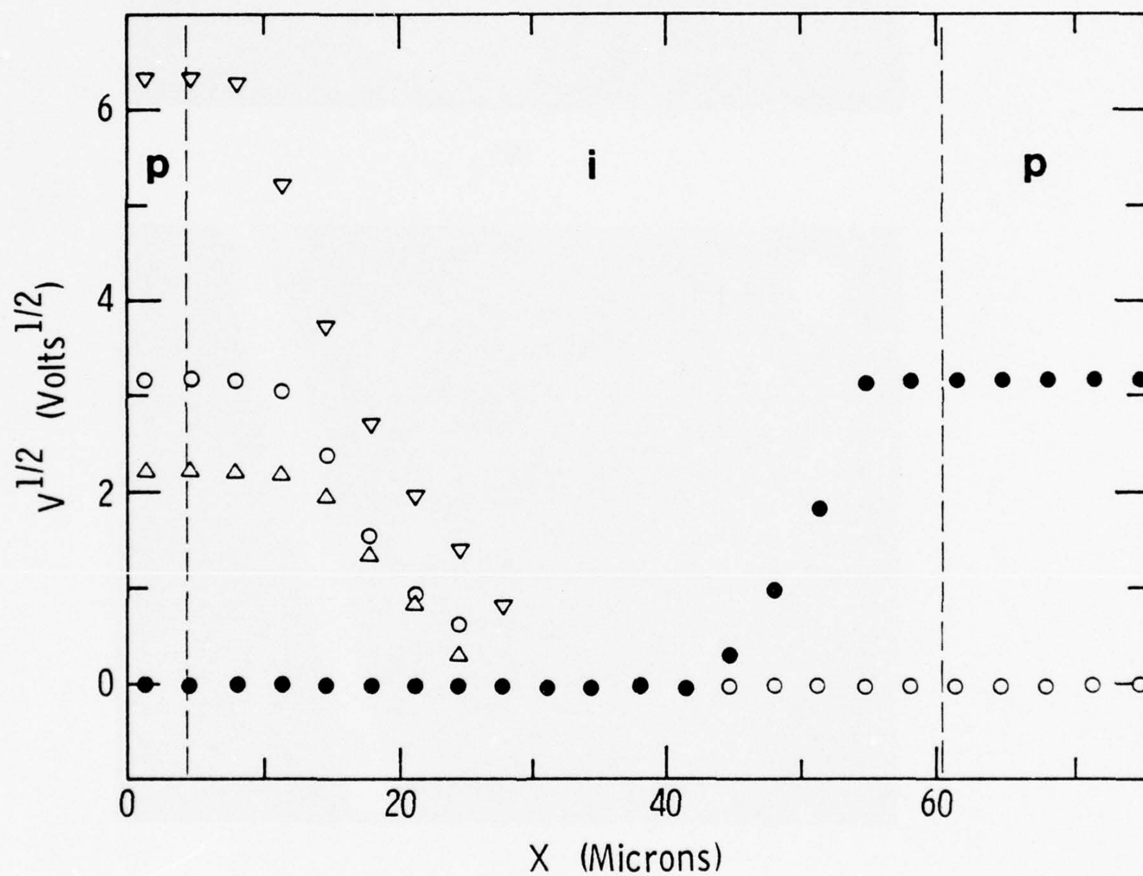


Fig. 13(a) Square root of the potential across a p-i-p specimen made with low-Cr (boule 1718) SI GaAs. Bias voltages: ▽ 40V; ○ 10V; △ 5V, left contact negative; ● 10V, right contact negative.

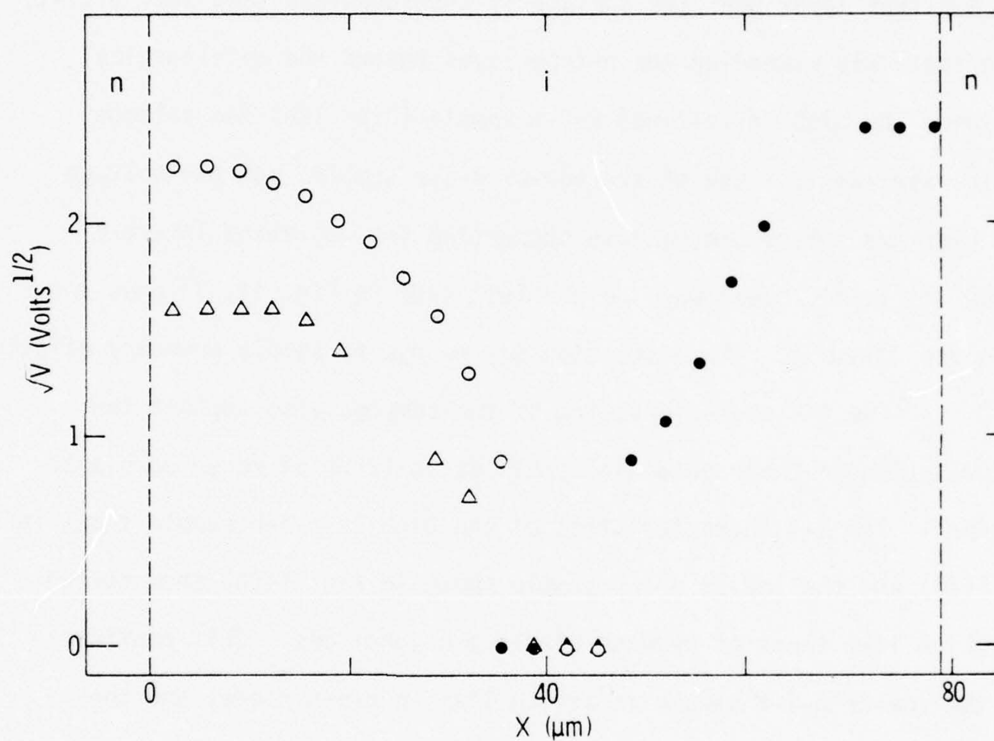
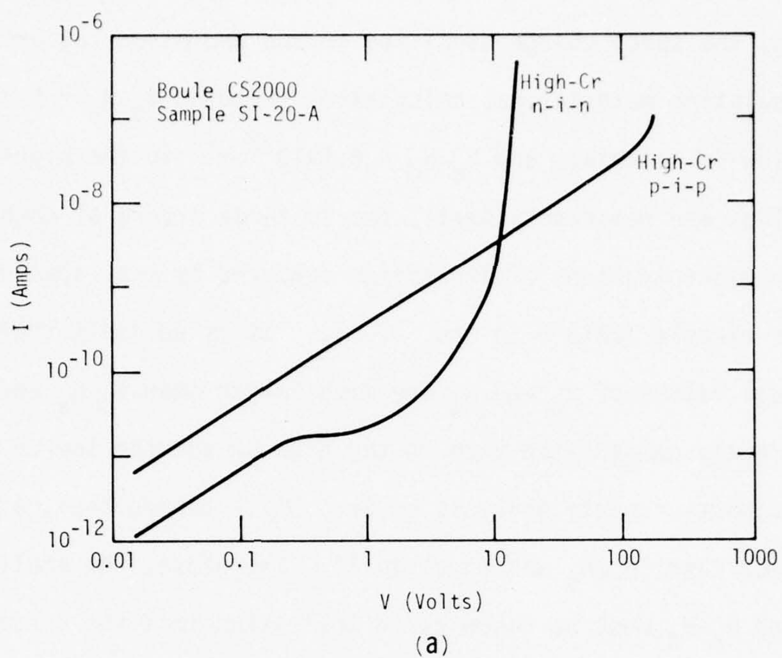


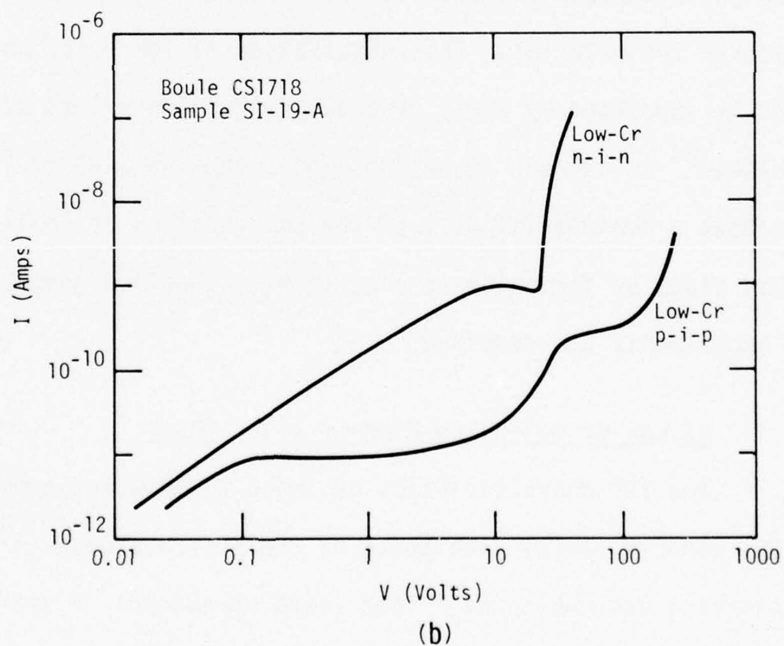
Fig. 13(b) Square root of the potential across an n-i-n specimen made with high-Cr (bould 2000) SI GaAs. Δ: left side (sample top) biased +3V; ○: left side (sample top) biased +6V; ●: right side (sample bottom) biased +6V.

scale in Fig. 13(a) represents $V^{\frac{1}{2}}$. $V^{\frac{1}{2}}$ varies linearly as expected for a depleted junction in uniformely doped material. The voltage remains constant past the metallurgical junction (indicated by the dashed lines) before it starts to drop. This effect is attributed to the heat treatment the substrate has suffered in the epitaxial growth furnace. Heat treatment forms a p-type layer near the surface of the substrate (see Sec. 3.2.4), thus effectively extending the p-type layer beyond the metallurgical junction. The high-Cr (p-type) n-i-n sample (Fig. 13b) has voltage profiles similar to those of the low-Cr p-i-p sample, but the voltage drops near the n-type anode, also supporting the depletion interpretation. It is not clear why, on the left side in Fig. 14, $V^{\frac{1}{2}}$ does not vary quite linearly. The distortion may be due to sample geometry effects.

The I-V characteristics of the samples also support the interpretation of their potential profiles in terms of reversed biased junctions. The I-V characteristics of the high Cr n-i-n sample shown in Fig. 14(a) and the low-Cr p-i-p sample shown in Fig. 14(b) show current saturation like those of reverse biased p-n junctions. This confirms that the low-Cr n-i-n sample is acting like an n-π-n diode, and the high-Cr p-i-p sample is acting like a p-v-p diode. Such a conclusion is in agreement with the results of Sec. 3.2.1, where it was shown that the low-Cr material exhibited n-type conductivity and the high-Cr material exhibited p-type conductivity. The breakdown voltages in the I-V characteristics agree with the punch-through voltages estimated from the potential profiles.



(a)



(b)

Fig. 14 I-V characteristics of n-i-n and p-i-p samples. (a) High-Cr SI GaAs (boule 2000). (b) Low-Cr SI GaAs (boule 1718).

From the slopes of the voltage profiles, by applying Poisson's equation, the space charge densities in the depletion regions of the semi-insulating material was calculated, yielding $N_d-N_a = 5.7x10^{13}cm^{-3}$ in the low-Cr material, and $N_a-N_d = 6.5x10^{12}cm^{-3}$ in the high-Cr material. Both values are remarkably small, two to three orders of magnitude smaller than the concentrations of impurities measured by mass spectroscopy (see for example Table 3 in Sec. 3.2.1). It is unlikely that the individual values of N_d and N_a are much larger than N_d-N_a and that they are perfectly compensated both in the high-Cr and the low-Cr material. The transport property analysis of Sec 3.2.1 showed that, at least in the low-Cr case, N_d/N_a was equal to 14. Therefore, the small values of N_d-N_a and N_a-N_d must be taken as an indication that the concentrations of donors and acceptors are much lower than the concentrations of impurities in the material. This observation of low donor and acceptor densities is supported by early observations of low values of trap filled limit voltage[24] in current injection experiments on SI GaAs.[25] It is possible that a fundamental part of the compensation of semi-insulating GaAs takes place by formation of electrically inactive complexes.[26] Further experiments are required.

b) Low-Cr n-i-n and High-Cr p-i-p Case

The I-V characteristics of these samples are compared in Fig. 14(a) and Fig. 14(b) with those of the previous case. The I-V characteristics are ohmic until they reach breakdown. A near ohmic behavior is precisely what one would expect since these are n-ν-n and p-π-p diodes. One might also expect a more less linear drop of the electrical

potential across the i region between the contacts. However, the voltage profiles are quite nonlinear, as shown in Fig. 15 for the high-Cr p-i-p case. When the left side is positively biased (Fig. 15a), the voltage remains nearly constant across the sample until it drops sharply near the negative contact. When the polarity is reversed (Fig. 15b) the profile also reverses, so that the main voltage change always occurs near the cathode. Similar profiles were observed in the low-Cr n-i-n case, in this case the voltage step being located near the anode. In the high-Cr p-i-p case the current induced by the SEM beam has been measured, and it is also shown in Fig. 15. This induced current profile qualitatively agrees with the voltage profile. The induced current is large where the electric field is large. This is taken as a verification of the AES-SEM measurement.

We have no simple interpretation for the potential profiles of the low-Cr n-i-n and high-Cr p-i-p samples. Failure of the Auger technique to faithfully measure the voltage should be ruled out in view of the recent demonstration on a well-characterized p-n junction discussed earlier in this section.[23] Impurity diffusion from the heavily-doped epi-layers is unlikely because the potential drop occurs 20μm from the interfaces. Free carrier diffusion from the interfaces due to the large Debye length in SI GaAs has been ruled out by calculation. Very deep carrier diffusion would give too high a current through the sample compared to the measured I-V curves. The most likely cause for the rapid potential change is the inhomogeniety introduced in the i-layer by the heat treatment in the epitaxial growth furnaces (see Sec. 3.2.4). This hypothesis

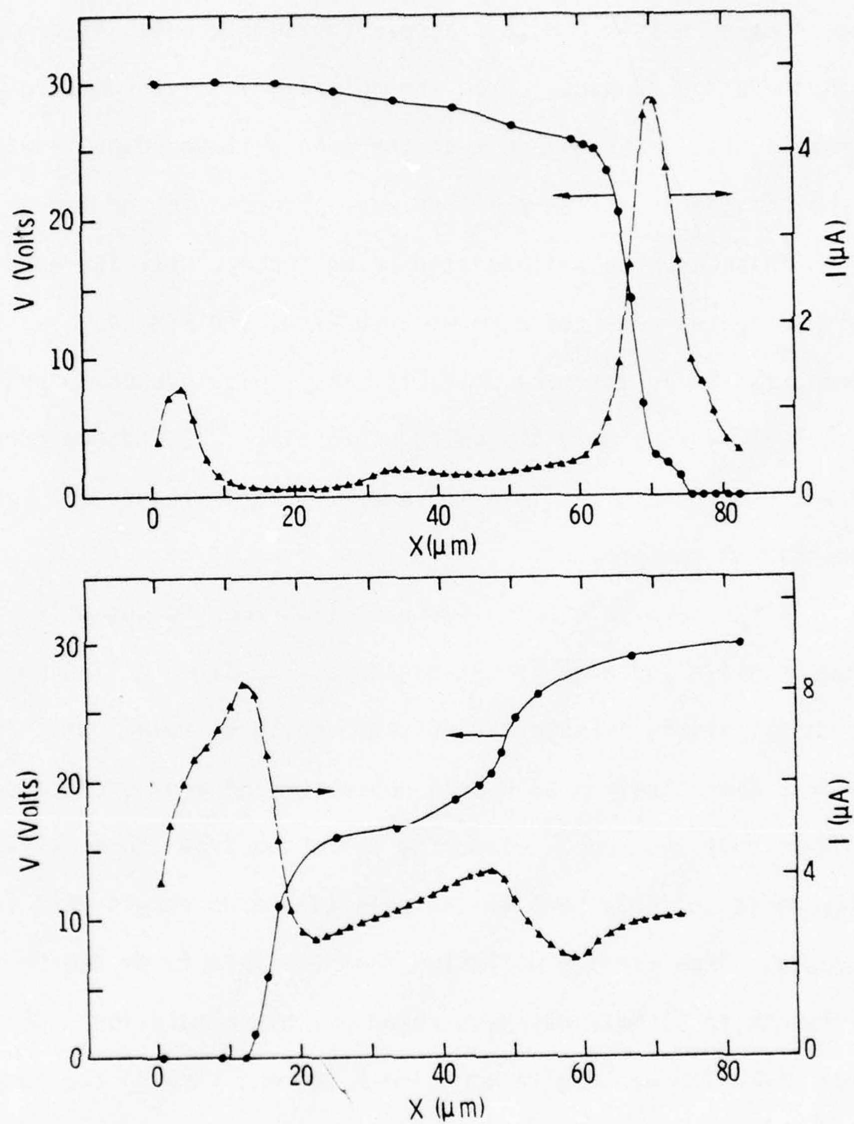


Fig. 15 Voltage and induced current profile across the high-Cr p-i-p sample: a) right side biased positive, b) left side biased positive.

should be tested by repeating the measurements on samples prepared with alloyed contacts, allowing fabrication temperatures much lower than epitaxial growth.

In summary, a technique for the measurement of electrical potential profiles across semiconductor junctions using an AES-SEM has been developed. This technique is valuable for the study of the n-type FET active layer-substrate interface. In the case of a SI substrate with p-type conductivity (high-Cr), a large electric field was observed in the substrate near the interface due to depletion by the n-type layer. Large electric fields at the interface may enhance noise generation. In the case of a SI substrate with n-type conductivity (low-Cr) a high electric field region also appeared in the substrate, but it was detached from the interface. A portion of the substrate near the interface remained at the potential of the n-type layer. In the case when the substrate was depleted the AES-SEM technique yielded values of N_d-N_a. The very low values of N_d-N_a observed indicate that the densities of donors and acceptors are much lower than the densities of impurities in the material suggesting that electrically inactive complexes may play a significant role in the compensation of SI GaAs.

3.2.3 Inclusions in Semi-Insulating GaAs - Cornell University

Secondary ion mass spectrometry (SIMS) has been employed to conduct a study of uniformity of concentration of chromium, and other impurities, in semi-insulating (SI) GaAs substrates. The instrument

being used was a CAMECA Model IMS-300 Ion Microprobe-Ion Microscope with imaging capability. The instrument sensitivity was ∿ 1ppm. The ion beam had a 1μm transverse spatial resolution.

Several SI GaAs samples have been tested, with particular interest in a high-Cr sample (Crystal Specialties, 2000) with a Cr concentration of $5.8 \times 10^{16} cm^{-3}$, and a low-Cr sample (Crystal Specialties, 1718) with a Cr concentration of $5 \times 10^{15} cm^{-3}$. These samples were taken from the same wafers used to fabricate the p-i-p and n-i-n specimens described in Sec. 3.2.2. Studies of Ga and As showed the expected uniform, featureless concentration over the polished surfaces on both samples. Studies of Cr in the lightly-doped sample showed no Cr above the sensitivity limit, ∿ 1ppm. In the high-Cr sample, however, isolated small inclusions of chromium were easily detected, and are shown as the three small, diffuse white spots in Fig. 16a (bottom, center, and upper right). The chromium over the rest of the surface was below the sensitivity limit. The field of view in Fig. 16 is 250μm in diameter. Notice that no inclusions had been detected by visual inspection of the wafer after polish. Other very heavily Cr-doped samples showed Cr inclusions, but inclusions were not observed on samples with $1 \times 10^{16} cm^{-3}$ Cr concentration or less. The onset of Cr inclusions at moderate doping is probably due to the low solubility of Cr in GaAs,[2] combined with constitutional supercooling during solidification.

The above observations set an upper limit of ∿ $5 \times 10^{16} cm^{-3}$ for the usable Cr-concentration in SI GaAs, considering the high-Cr sample (boule 2000) to be on the threshold of Cr inclusions. With this rather

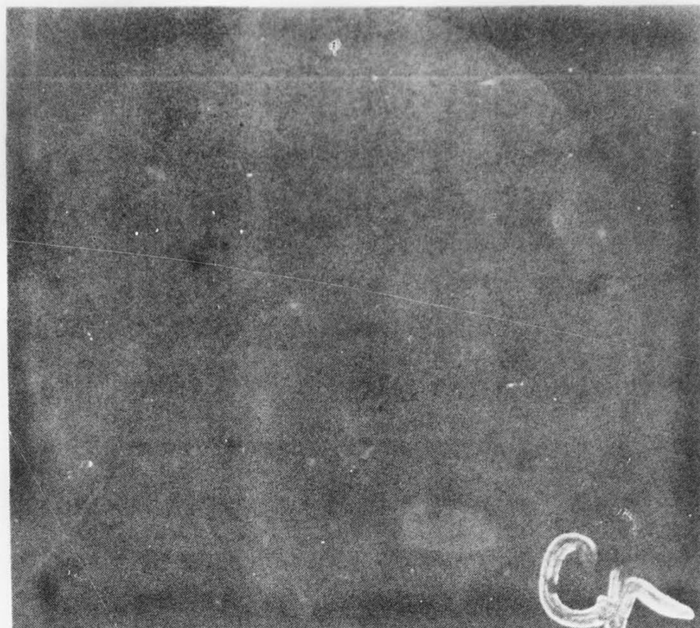


Fig. 16(a) Chromium impurity pattern in a high-Cr SI GaAs substrate (Crystal Specialties 2000).

Fig. 16(b) Silicon impurity pattern in SI GaAs.

low ceiling of Cr concentration, the usable Cr range in SI GaAs becomes quite narrow, between $\sim 3\times10^{15}cm^{-3}$ required to insure electrical compensation (see Sec. 3.1) and $\sim 5\times10^{16}cm^{-3}$ determined by the onset of inclusions.

The only other impurity detected by the SIMS analysis is Si. Figure 16b shows a silicon pattern over a 250μm field of view on a SI GaAs sample. Si inclusions were present in most Si samples. However, in SI substrates with extremely low Cr concentration ($N_{Cr}<10^{15}cm^{-3}$), the silicon inclusions were nearly eliminated. This low level of Si inclusions is probably related to the fact that the overall Si content of the sample must be low in order to be electrically compensated with such a low Cr concentration. This result further stresses the need of minimizing Si contamination during growth of SI GaAs (see also Sec. 3.1).

SIMS measurements were used to study some of the effects of heat treatment. Samples were first examined with the SIMS, then heat treated for 10 hours in H_2 atmosphere at 700°C, and, finally, reexamined under the SIMS. Substrates very heavily doped with Cr ($N_{Cr}>10^{17}cm^{-3}$ with visible Cr inclusions), showed a large accumulation of chromium on the surface after heat treatment. This did not occur on substrates with more normal Cr doping ($N_{Cr} < 5\times10^{16}cm^{-3}$).

3.2.4 Effects of Heat Treatment on Semi-Insulating GaAs - Science Center

GaAs substrates with low resistivity can usually be heated in epitaxial growth furnaces until they reach the required growth temperature without suffering appreciable changes of their electrical properties. Semi-insulating (SI) substrates are much more sensitive to such heat treatments because they are compensated semiconductors. [1] It has been shown that even moderate heat treatment cycles similar to those that take place in LPE growth may, in some cases, lower the sheet resistance of semi-insulating substrates by several orders of magnitude. Such resistance changed produce disastrous effects on the performance of GaAs microwave FET devices fabricated on those semi-insulating substrates. [27] Ion implantation is not free from heat treatment problems either because the implanted substrates has to be annealed in order to remove implantation damage (see Sec. 5). Although this anneal is done at temperatures much higher than those of epitaxial growth, the sample is usually covered by a protective cap. Still the effect of this heat treatment must be tested, as changes in substrate properties may be responsible for anomalies in the doping profiles of implanted layers.

This section will first discuss the effects of heat treatment in a hydrogen atmosphere, as in epitaxial growth. A survey of materials will be presented. Transport property measurements and photoluminescence data will be used to show that impurity doping plays a role in the formation of the low resistivity layers. Secondly, heat treatment with the surface of the

substrates exposed to H_2 will be compared with heat treatment with a protective cap, showing that the two types of heat treatment lead to different substrate behavior, and that substrates qualified for epitaxial growth are not necessarily qualified for ion implantation.

A large cross section of SI GaAs material grown at Crystal Specialties has been tested for heat treatment behavior. Small pieces from the 0.5mm thick wafers were polished, cleaned, chemically etched to remove damage, and finally annealed for 90 minutes at temperatures of 700, 750 and 775°C. This heat treatment was done in the same leak tight furnace used for LPE growth (see Sec. 4.2). During the anneal, the furnace was flushed with Pd-purified H_2. This procedure exactly simulates both the substrate preparation and the heat treatment typical of LPE growth.

In Fig. 17 the sheet resistivity of samples from six boules is plotted against heat treatment temperature. The rapid decrease of sheet resistance when the heat treatment temperature is increased indicates that it is desirable to keep the growth temperature as low as possible when growing LPE layers on semi-insulating GaAs. No correspondence was found between the sheet resistance of the heat treated samples and their Cr-concentration.

The low resistivity layers formed are always p-type. This observation based on I-V characteristics of samples with asymmetric contacts has been verified on the more conductive samples by Hall measurements.

Samples from boule 2109 were chosen for study by ESCA. The ESCA spectra of samples which had not been annealed, annealed at 750°C, and annealed at 775°C turned out to be identical. The main chemical species observed were Ga and As in stoichiometric concentration. O and C were also observed, as might be expected. Since ESCA determines the chemical composition

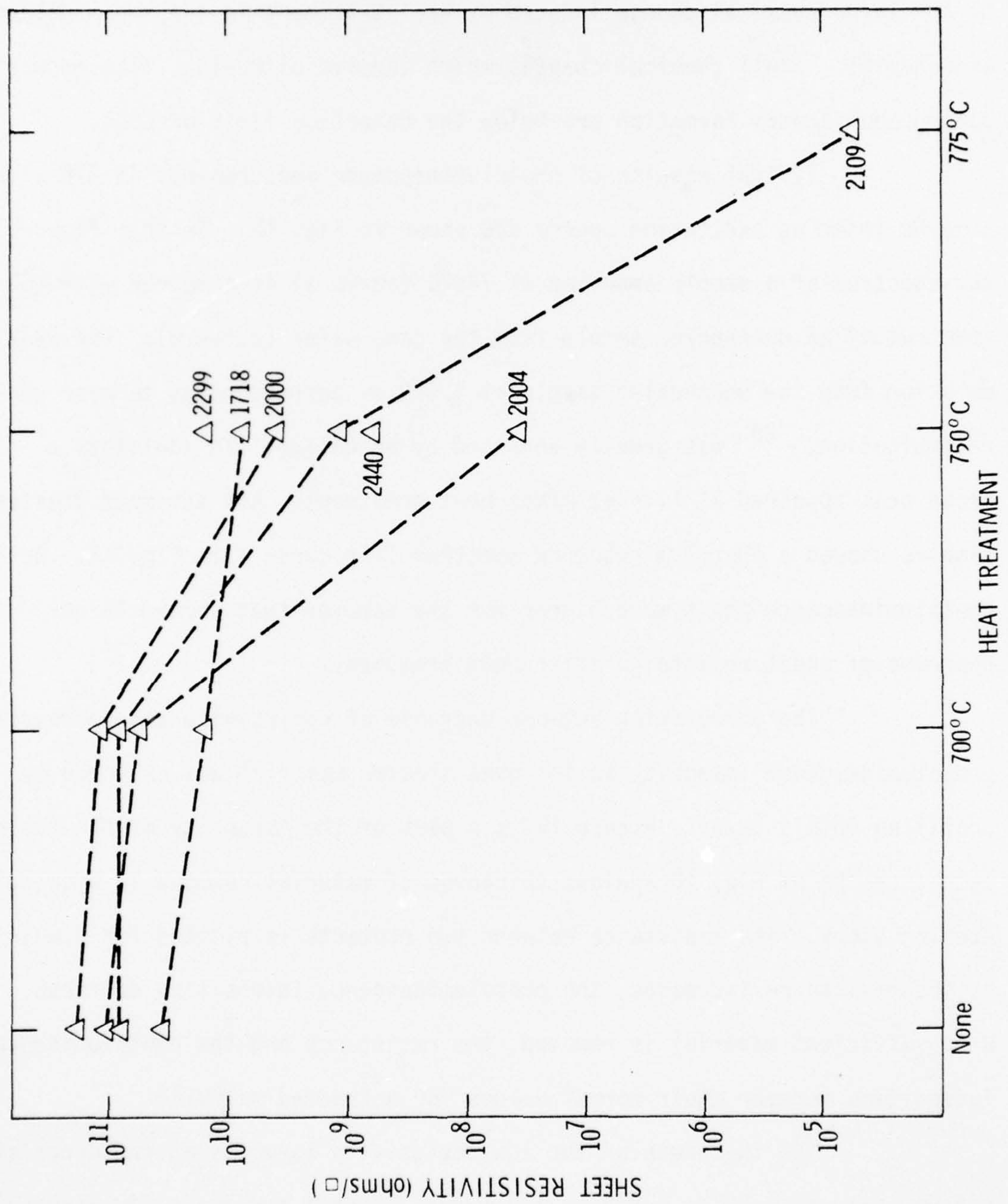


Fig. 17 Sheet resistance vs heat treatment temperature for several semi-insulating GaAs samples (identified by boule numbers).

within the first 20-30Å of the sample, this result rules out the possibility of any large chemical change induced by heat treatment in the top monolayers of material. Small chemical changes which involve diffusion, like impurity doping and vacancy formation are below the detection limit of ESCA.

Typical results of photoluminescence measurements at 77K with a He-Ne laser as excitation source are shown in Fig. 18. In this figure, the spectrum of a sample annealed at 775°C (curve a) is compared with the spectrum of an unannealed sample from the same wafer (curve b). The weak emission from the unannealed sample at 1.508 eV corresponding to near gap recombination,[28] was greatly enhanced by annealing. In addition, a broad peak appeared at 1.39 eV after heat treatment. All the heat treated samples showed a photoluminescence spectrum like curve a in Fig. 18. Both photoluminescence peaks were higher for the samples that showed larger decrease of sheet resistance after heat treatment.

The correlation between decrease of resistivity and increase of photoluminescence intensity in the heat treated material was explored by profiling into a layer. Figure 19 is a plot of the intensity of the luminescence peaks of Fig. 18 against thickness of material removed in sequential etching steps. The resistance between two contacts is plotted for comparison. As the resistance increases, the photoluminescence intensities decrease. When sufficient material is removed, the resistance and the photoluminescence intensities recover their normal values for untreated material.

The thickness of the low resistivity layer is on the order of 0.3μm. From this value and from the length of heat treatment (90 minutes), a

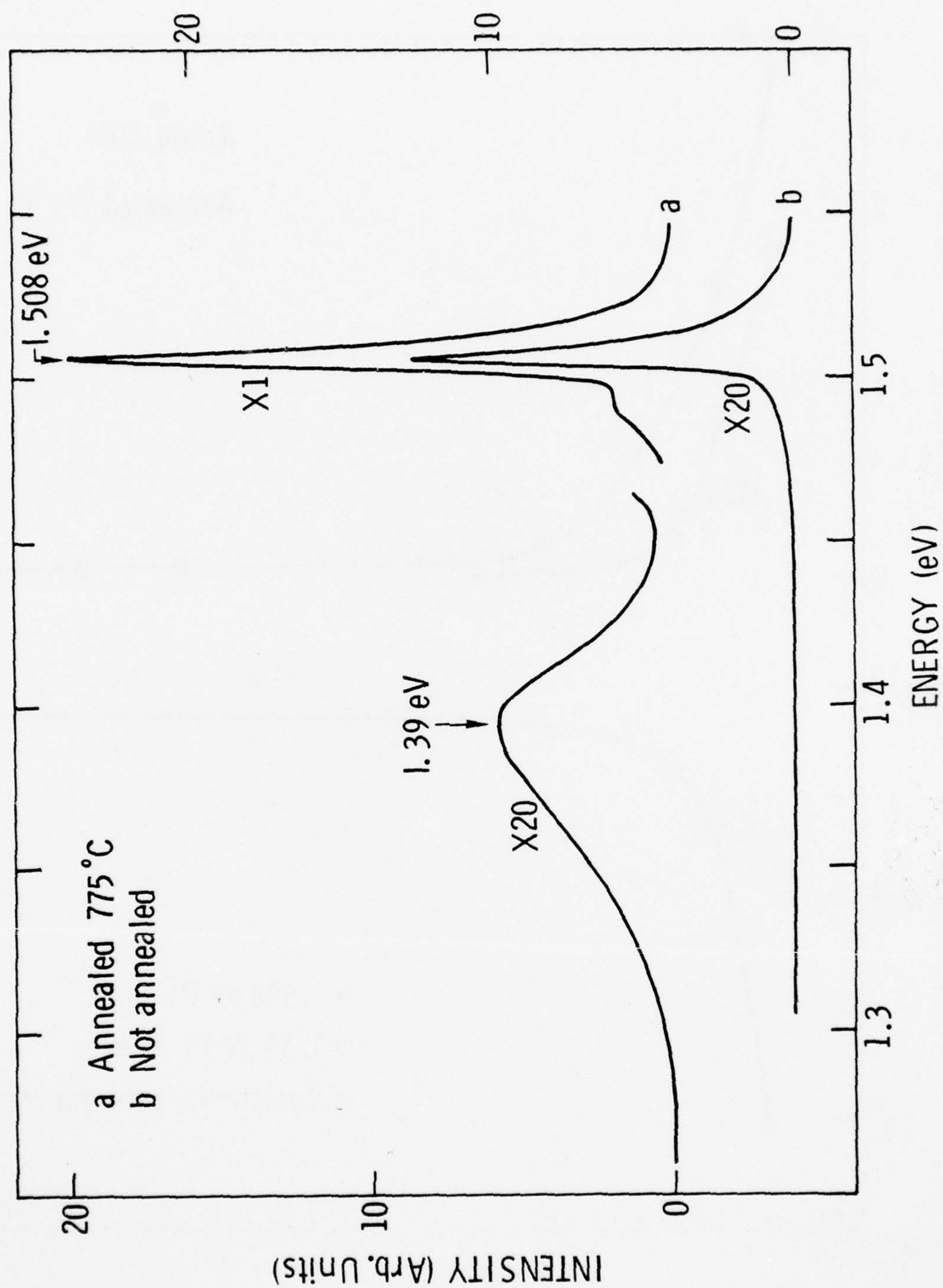


Fig. 18 Photoluminescence spectra of an annealed and an unannealed sample from the same wafer (from boule 2109) measured at 77K. The spectra were corrected for the spectral response of the system.

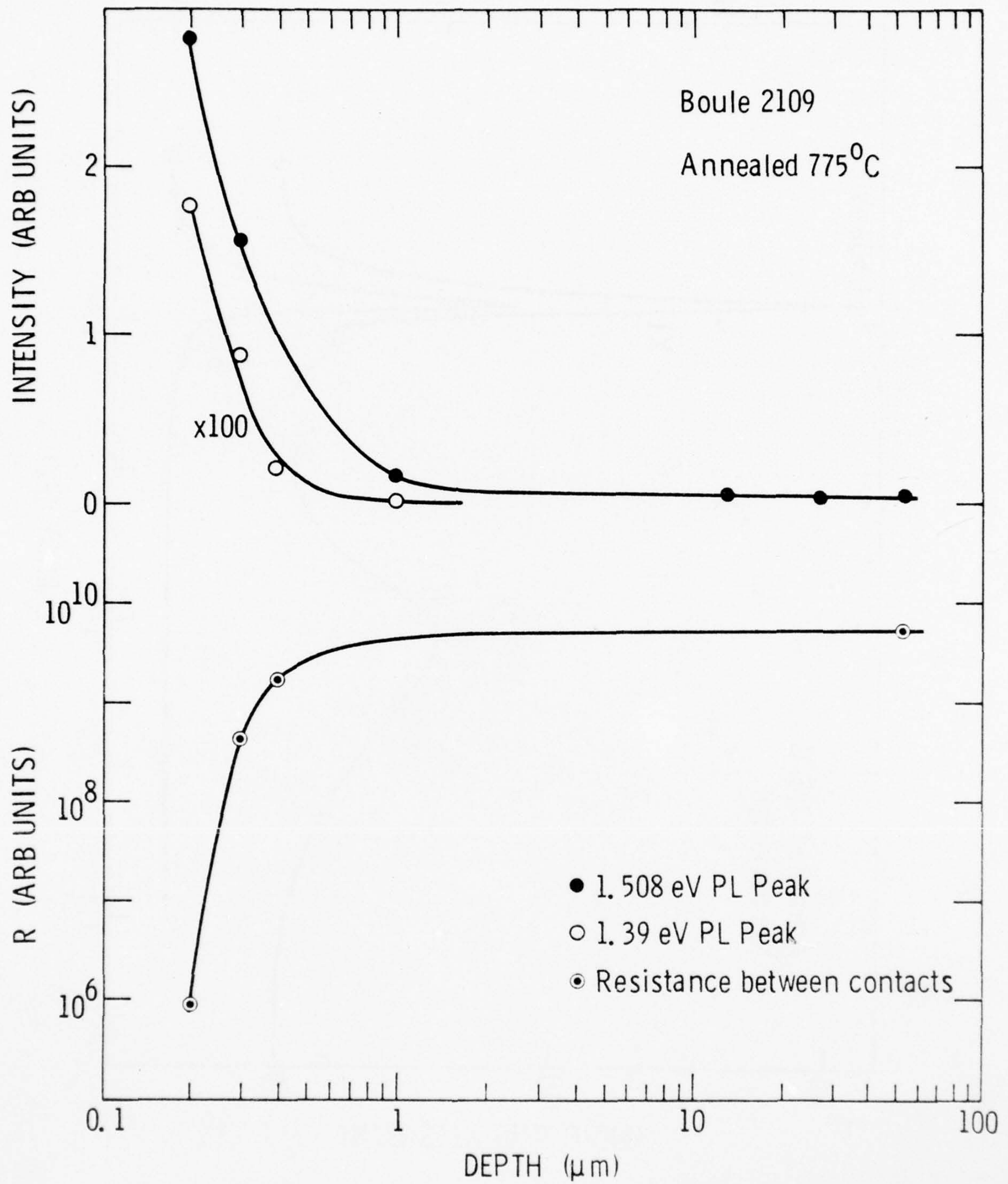


Fig. 19 Intensity of the photoluminescence peaks (at 77K) and resistance between two contacts plotted against thickness of material removed in sequential etching steps.

diffusion coefficient of $\sim 2.1\times10^{-13}\text{cm}^2\text{sec}^{-1}$ at the annealing temperature of 775°C was calculated for the centers responsible for the p-type conduction.

The two peaks in the 77K photoluminescence spectra of the heat treated samples (Fig. 18) could be resolved by lowering the measurement temperature. Figure 20 shows the photoluminescence spectrum at 25K for the heat treated sample of Figs. 18 and 19. In the gap region it is now possible to distinguish the free excition recombination peak at 1.514 eV signaling the position of the energy gap, [29] and a large peak at 1.491 eV. The energy of this peak, 27 meV lower than the gap energy, is characteristic of conduction band to acceptor recombination or exciton bound to acceptor recombination. The broad peak which appeared at 1.39 eV in the 77K spectrum (Fig. 18) split into several structures at 25K (Fig. 20). The structures are easily identified as a main peak at 1.409 eV, and a set of phonon replicas at lower energy.

The temperature dependence of the resistivity and Hall constant were measured in order to determine which of the two energy levels observed in the photoluminescence spectrum was responsible for the p-type conductivity of the surface layer. This measurement was made between room temperature and liquid nitrogen temperature using a Van der Pauw configuration.

The free hole concentration per unit area p, multiplied by $T^{-1.5}$ in order to compensate for the temperature dependence of the effective density of states, is plotted in Fig. 21 against the inverse of temperature. At low temperature, the $p\,T^{-1.5}$ product decreases exponentially corresponding to the freeze out of free carriers. This exponential variation

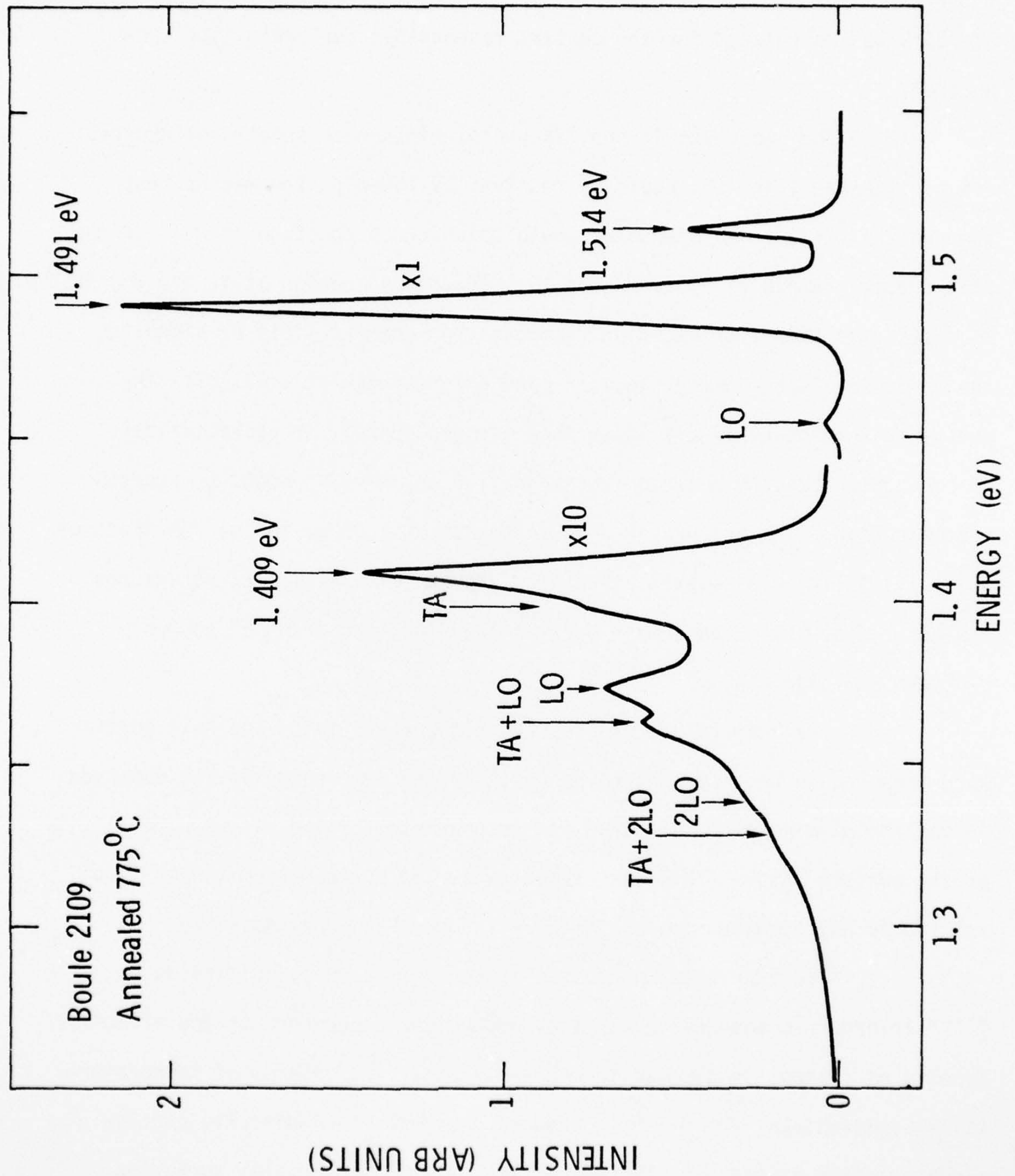


Fig. 20 Photoluminescence spectrum of a heat treated sample measured at 25K. The spectrum was corrected for the spectral response of the system.

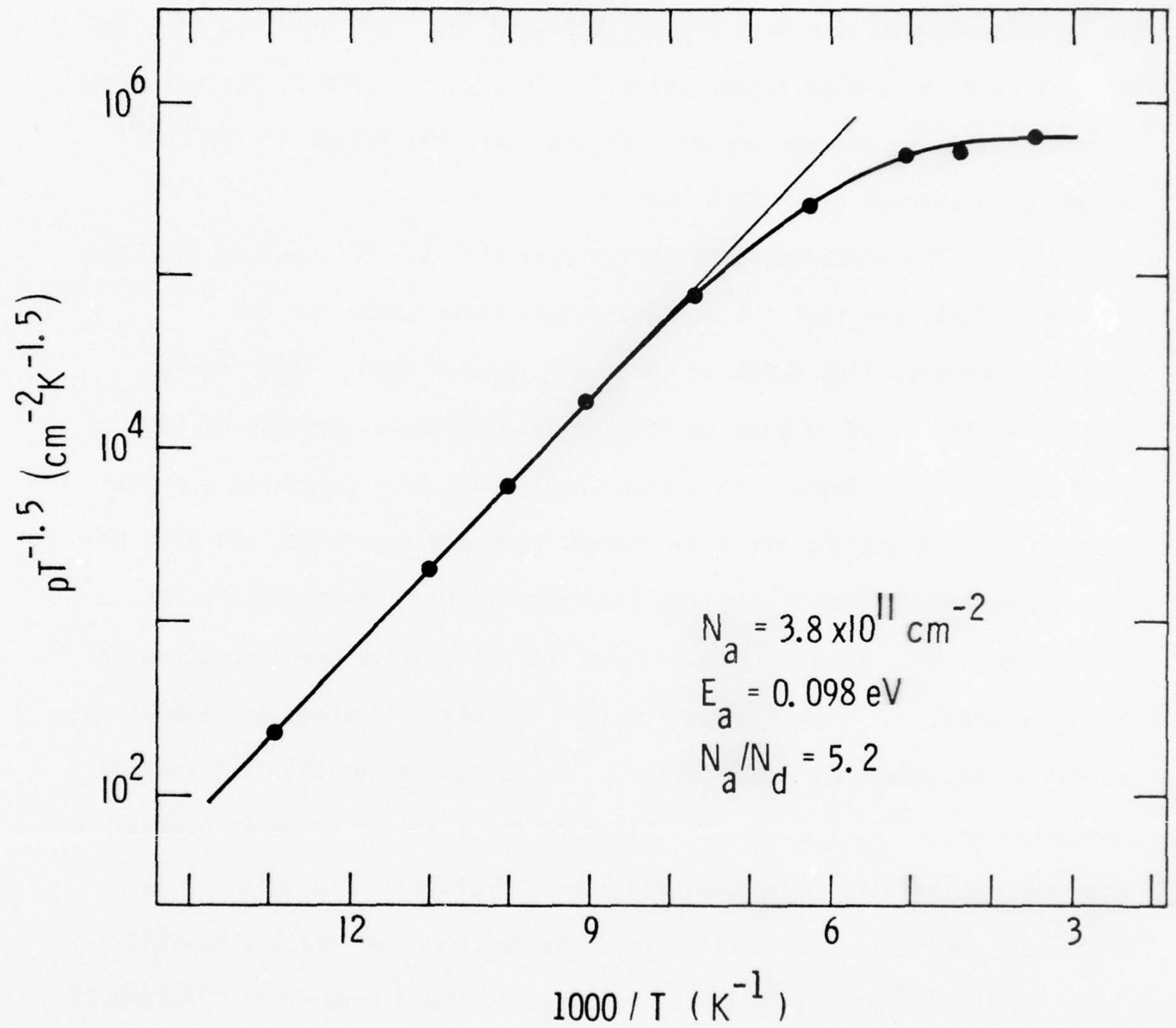


Fig. 21 Free hole concentration (per unit area) multiplied by $T^{-1.5}$ vs 1000/T for a sample from boule 2109 heat treated at 775°C for 90 minutes.

appears as a straight line in the semilogarithmic plot. A linear least square fit indicated by the straight line in Fig. 21 yields the depth of the acceptor level E_a = 0.098 eV and the compensation ratio N_a/N_d = 5.2.[11] An acceptor density per unit area $N_a = 3.8x10^{11} cm^{-2}$ was obtained from the saturation of p at high temperatures. This acceptor density per unit area corresponds to an average acceptor density per unit volume of $\sim 10^{16} cm^{-3}$ assuming an average depth of 0.3μm.

The measurement of resistivity and Hall constant as functions of temperature show that the acceptor level responsible for the p-type conversion lies 0.098 eV above the valence band. This result identifies the 1.409 eV peak in the photoluminescence spectrum of Fig. 20 with this acceptor level. This peak corresponds to a manganese acceptor. In fact, a peak at exactly the same energy, with the same width and with the same strength of lattice coupling (measured by the intensities of the phonon replicas), has been observed in the photoluminescence spectrum of Mn-doped GaAs.[30] This identification has been confirmed by several Mn doping techniques such as diffusion,[30] epitaxial growth,[31] and ion implantation.[32] The identification of the acceptor as Mn is compatible with the resistivity and photoluminescence profiles. The value of the diffusion coefficient determined from the thickness of the low resistivity layer ($2.1x10^{-13} cm^2$/sec at 775°C) is close to the diffusion coefficient of Mn in GaAs at that temperature ($7x10^{-13} cm^2$/sec).[33]

A Mn acceptor has been identified in GaAs grown by molecular beam epitaxy (MBE) under As-rich conditions by Ilegems et al.[34]

They suggested that stainless steel was the source of Mn. Presence of Mn in our heat treatment furnace is more difficult to explain, since there are no hot stainless steel components. The only components in our system are the quartz furnace, the graphite boat on which the samples are placed (facing up), Pd-purified flowing hydrogen gas, and stainless steel tubing for the hydrogen gas. Since these components are all unlikely sources of Mn doping, an alternative is that Mn may be present in SI GaAs and be activated by the heat treatment. Mass spectroscopy analysis of some of the SI samples used in the heat treatment experiments did not detect Mn. However, the detection limit was marginal ($\sim 3 \times 10^{15} cm^{-3}$). The value of the diffusion coefficient determined above ($2.1 \times 10^{-13} cm^2/sec$ at 775°C) is very close to the value of the diffusion coefficient determined by Chiang and Pearson [35] for Ga vacancies ($1.7 \times 10^{-13} cm^2/sec$ at 775°C). Since Mn tends to occupy Ga sites, [34] this agreement makes a hypothesis of vacancy induced activation of Mn present in the material very attractive. Further experiments on varying the annealing conditions will be required in order to test this hypothesis.

The acceptor peak at 1.491 eV in the photoluminescence spectrum of Fig. 20 has not been identified yet. This peak may be due to C, but care must be excercised in making any interpretation because several impurities (Be, Mg, C, Zn) introduce acceptor levels at this energy. [36]

The effects of heat treatment conditions similar to those of post-implantation anneal on SI substrates have also been investigated. Samples from a cross section of SI GaAs grown at Crystal Specialties have been tested. The tests consisted of simulating the ion implantation processing

of the substrates without implant. Small pieces from the SI GaAs wafers were cleaned, etched, covered with a Si_3N_4 cap, and annealed at 850°C for 30 minutes in a hydrogen flushed furnace. The cap was then removed, and the sheet resistivity was measured. The sheet resistivity resulting from this test is plotted in Fig. 22 for material from several boules against the sheet resistivity measured after the test described earlier in this section, where the samples had been annealed in H_2 at 750°C without surface protection. In Fig. 22 , thin lines have been drawn at 10^{11} ohm/□ parallel to both axis to represent the typical sheet resistivity of untreated samples. Thin lines have also been drawn at 10^7 ohm/□, representing a conventional boundary between material qualified and material unqualified for ion implantation or epitaxial growth depending on the test performed. Only three boules out of seven fall in region C of Fig. 22 , which corresponds to material acceptable for both ion implantation and epitaxial growth. The other four boules fall into region B, which corresponds to material qualified for epitaxial growth, but not for ion implantation. Lack of points in regions A and B does not necessarily represent a trend of the material because only material qualified for epitaxial growth was tested for ion implantation qualification. The conclusion one extracts from the results of Fig. 22 is that qualification test on substrates for ion implantation must be done independently of whether the material is qualified for epitaxial growth. In Sec. 5.1, the correspondence between the effects of capped anneal on SI substrates and the reproducibility of implanted profiles will be discussed. It will be shown that an even better substrate qualification

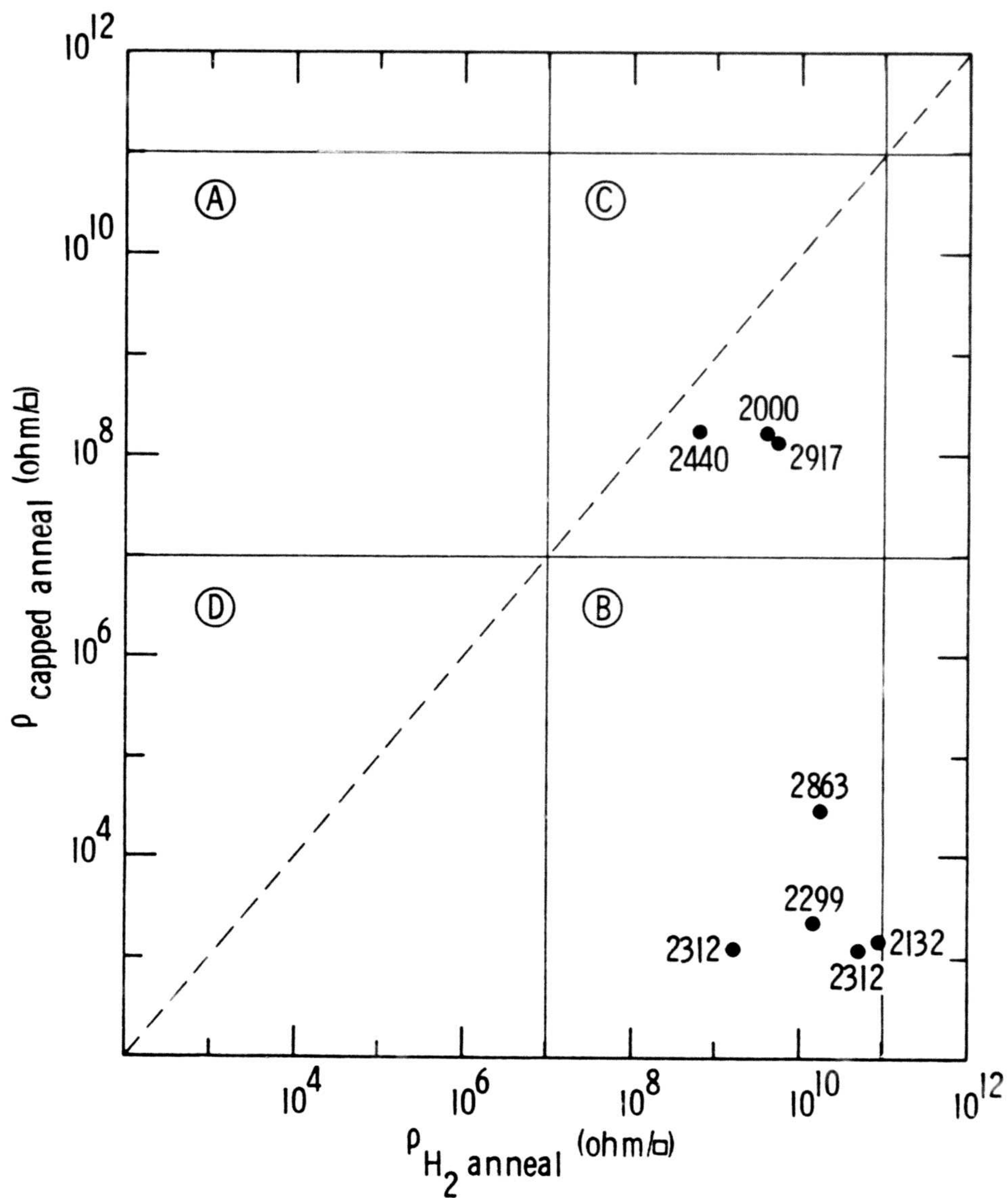


Fig. 22 Sheet resistivity after anneal at 850°C for 30 minutes with a Si_3N_4 cap vs sheet resistivity after anneal in H_2 atmosphere at 750°C for 2 hours. The data points are identified by boule numbers.

test can be done by Kr bombarding the substrates before capping and annealing, so that not only the heat treatment, but also the damage produced by ion implantation is simulated.

The electrical properties of the low resistivity surface layers formed after capped anneal differ from those of layers formed by annealing in H_2 without protection. The low resistivity surface layers of the capped annealed SI substrates are all n-type, while in the other case, the layers are always p-type, as discussed earlier in this section. A photoluminescence spectrum of a capped annealed sample measured at 25K is shown in Fig. 23. As in the case of heat treatment in H_2, this spectrum has two main peaks and their phonon replicas. The near gap features are almost identical in the two cases (see Fig. 20). This is probably due to the fact that at 25K the donor level is not resolved from the conduction band. The low energy peaks in the spectra of Fig. 20 and 23 are at different positions. In the capped and annealed material (Fig. 23) this peak is at 1.361 eV. This energy is characteristic of a Cu acceptor.[37]

The Cu impurity identified in the capped and annealed samples can not be the main dopant because Cu is an acceptor,[37] while the low resistivity layers are n-type. One may speculate that perhaps Si from the Si_3N_4 cap diffuses into the GaAs, but this is rather unlikely because the Si_3N_4 cap is usually nitrogen rich. Further experiments will be needed in order to identify the cause of n-type conductivity.

In summary, a survey of heat treatment effects on SI GaAs has been presented. The effects of heat treating SI GaAs samples either

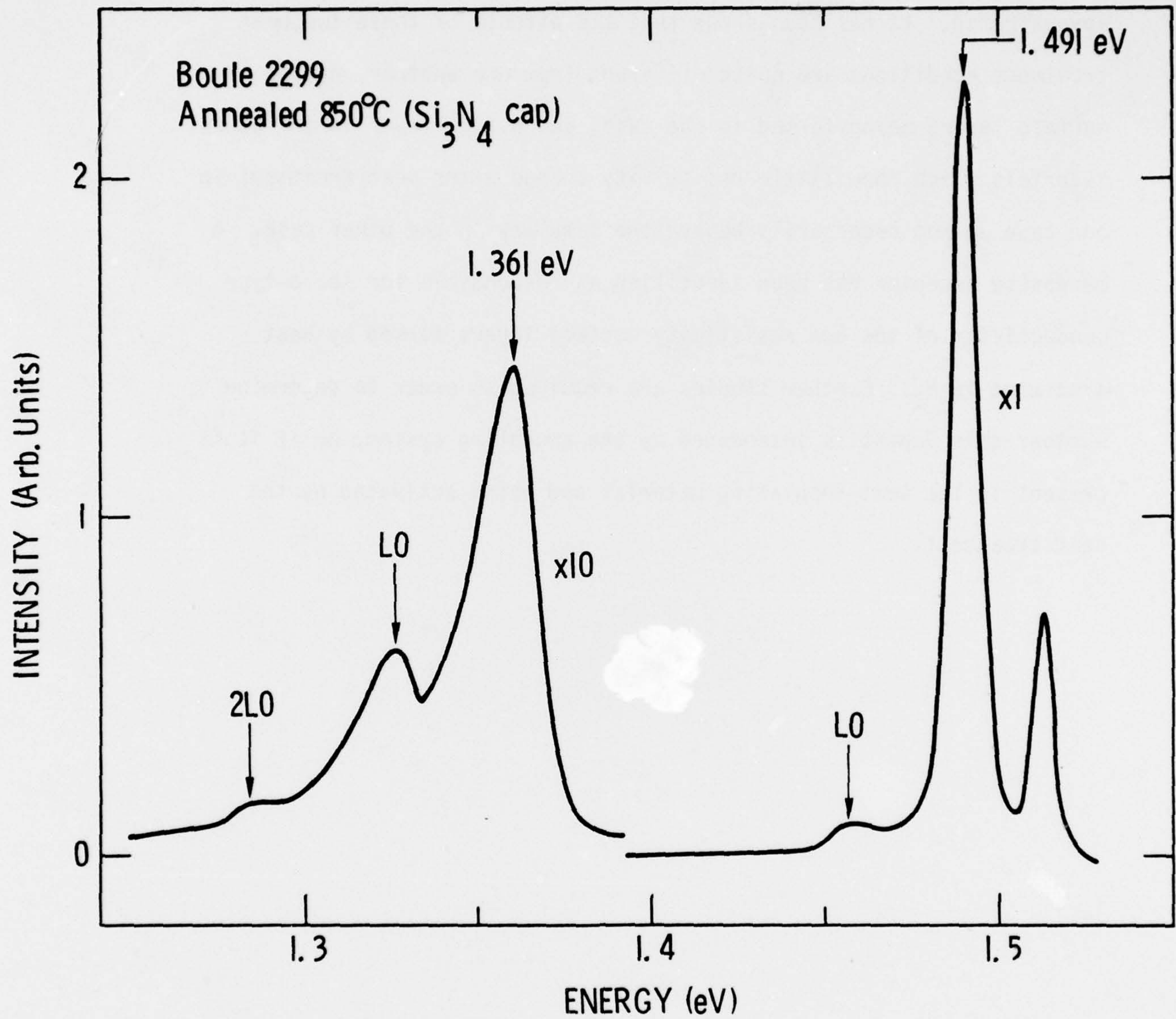


Fig. 23 Photoluminescence spectrum at 25 K of a capped and annealed SI GaAs sample. The spectrum was corrected for the spectral response of the system.

with their surface exposed to H_2 as in epitaxial growth reactors, or with a protective Si_3N_4 cap as in post-implantation anneal have been investigated. It has been shown that the effects of these two heat treatment conditions are quite different from one another, p-type surface layers being formed in one case, and n-type layer in the other. Materials which show little resistivity change after heat treatment in one case do not necessarily behave the same way in the other case. A manganese acceptor has been identified as responsible for the p-type conductivity of the low resistivity surface layers formed by heat treatment in H_2. Further studies are required in order to determine whether this dopant is introduced by the annealing system, or if it is present in the semi-insulating material and being activated by the heat treatment.

4.0 LIQUID PHASE EPITAXIAL MATERIAL GROWTH AND CHARACTERIZATION

The liquid phase epitaxial (LPE) growth investigations under this contract have, over a period of time, evolved into three projects involving Stanford University, the Science Center, and Cornell University. Stanford's work has had, since the inception of the contract, the primary goal of growing high resistivity (>10^4 ohm-cm) epitaxial layers for potential use as a substrate buffer for active device layers. Crucial to achieving this goal was an understanding of the interactions between the growth system components, the melt bakeout temperature, the chemical composition of the melt, and subsequent impurity incorporation in the layer. Based on the understanding of these interrelated factors, Stanford's approach has been to control the chemical composition of the melt through a series of systematic bakeouts at a specific temperature and to use Cr to help chemically and electrically compensate donar and acceptor species. Layer exceeding resistivities of 10^6 ohm-cm have been produced.

The Science Center's work addressed the problems of growing ultra-thin epitaxial layers directly on GaAs semi-insulating substrates. Field Effect Transistors were used as the vehicle to access the quality of the layers, and the substrate-epitaxial layer interface. From this work evolved a novel state-of-the-art growth technique

incorporating a "restricted" melt and a vertical temperature gradient. Emphasis has been placed on demonstrating the uniformity and reproducibility of this method. The LPE facilities at the Science Center have also been involved in substrate annealing studies, and in epitaxial growth for preparation of samples for measurement of intrinsic material properties and substrate interface effects.

The role of Cornell University has been to develop LPE technologies for growth of buffered layer FET structures. This required approaches different from those used at both the Science Center and Stanford. Active layers were grown in a more conventional manner to facilitate the incorporation of buffer layer growth. The Cornell approach for buffers was to use high purity undoped layers rather than high resistivity compensated layers as grown at Stanford.

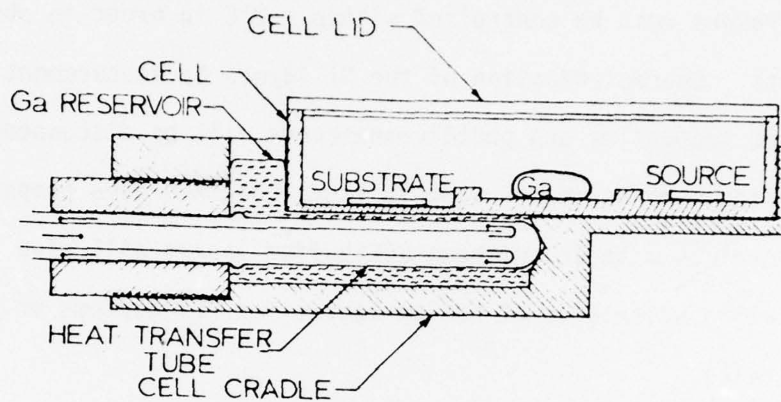
4.1 Preparation and Properties of Semi-Insulating LPE GaAs Stanford University

The growth of high resistivity liquid-phase epitaxial (LPE) GaAs layers requires close-compensation of shallow donors and acceptors arising from residual impurities in the source materials and from chemical reactions between the growth system components. Three different LPE growth systems will be discussed. These in order of investigation are: SiO_2-C-H_2, SiO_2-BN(C)-H_2 and SiO_2-BN-H_2 systems. It will be shown that the chemical reactions in each of these systems can be controlled by systematic bakeouts of the arsenic-saturated gallium melts before each growth. Low bakeout temperatures provide n-type layers while high bakeout temperatures give

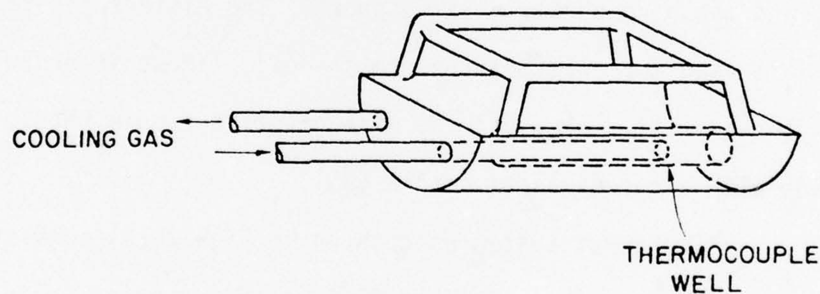
p-type layers, and a critical intermediate bakeout temperature, unique to each system gives high resistivity layers with N_a/N_d close to 1. Once the optimum growth conditions are established, resistivities up to 5×10^6 ohm-cm can be reached by addition of Cr. The proper bakeout temperature must be controlled within $\pm$ 2°C in order to obtain reproducible results. Characterization of the SI layers by measurement of transport related properties and photoluminescence will be discussed. Transient capacitance measurements made to study the interface properties of FET type devices with and without LPE buffer layers will also be presented, indicating advantages of buffer layers for FET devices on SI GaAs substrates.

Three different horizontal tilt liquid phase epitaxial growth systems were used in this study. The features common to these systems are: The furnace, the temperature controller, the fused-quartz reactor tube, and the high purity H_2 atmosphere. The differences reside in the materials used to construct the growth cell. These in order of study were graphite (c), boron nitride with graphite cradle BN(C), and boron nitride with a fused-quartz cradle (BN).

The first system used shown in Fig. 24(a) consisted of a high purity graphite growth cell (from POCO) floating on a liquid Ga reservoir contained in a graphite cradle. This system will be referred to as the fused quartz-graphite-hydrogen (SiO_2-C-H_2) system. In the second stage of this study, a pyrolytic boron nitride growth cell was used in place of the graphite cell. The BN cell (from Union Carbide), however, was still placed in a grapnite cradle and this system will be referred to as the fused quartz-boron nitride (graphite cradle)-hydrogen (SiO_2-BN(C)-H_2)



a. Graphite growth cell and cradle



b. Fused-quartz cradle

Fig. 24 The temperature gradient growth cells.

system. In the third stage of the work, the graphite was completely eliminated from the system. A fused quartz cradle (GE 204 quartz) shown in Fig. 24(b) was used to replace the graphite cradle and this system will be referred to as the fused quartz-boron nitride-hydrogen (SiO_2-BN-H_2) system.

The time-temperature cycle of a typical growth procedure is shown in Fig. 25. Six grams of Ga and about 2 times more than the amount of GaAs source needed for saturation are baked out together in the growth system, without a substrate. This is done before each growth, at a prescribed temperature in the range of 600 to 850°C for 15 hours, as indicated from A to B in Fig. 25. At position c the substrate is cleaned and loaded into the growth room temperature. After the growth system is purged with H_2 for at least two hours the melt is then saturated at the desired temperature (700°C for most of the growths). A temperature gradient is induced during warm-up (position D) to insure that the As-saturated Ga melt and substrate remain at the same temperature. After 30 minutes at the stabilized saturation temperature (E to F), the programmer is turned on to provide a cooling rate of 4.5°C/min. When the temperature of the melt is 1°C below the saturation temperature (position G), the furnace is tilted in order to roll the As-saturated Ga onto the substrate to start the growth. After the temperature has cooled to 400°C, position H in Fig. 25, the furnace is cooled quickly to room temperature. The grown layer is then unloaded from the melt. The liquid Ga droplets adhering to the surface of the epitaxial layer are removed by swabbing with a Q-tip soaked with methanol. The layer is then boiled in HCl and finally rinsed with methanol and isopropyl alcohol. Figure 26 shows the cleaved and stained edge of an epitaxial layer as observed under an optical microscope. The thickness of this layer is 14μm. As can be seen, the interface is planar and the layer thickness is quite uniform.

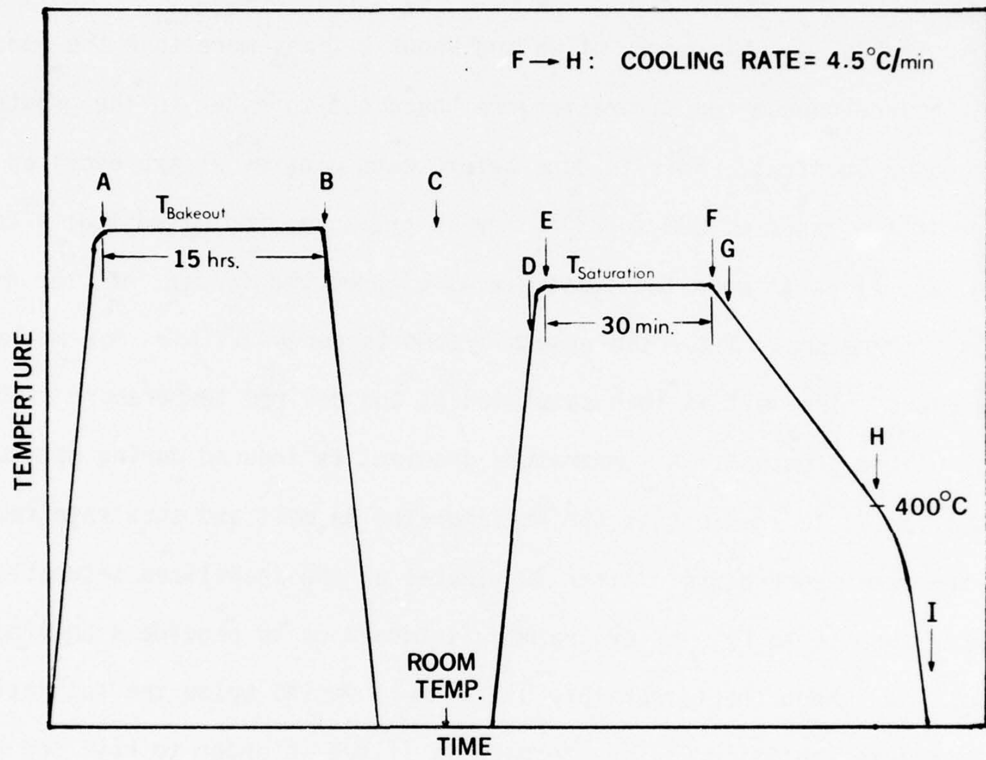


Fig. 25 Time-temperature cycle of the growth procedure for SI LPE GaAs

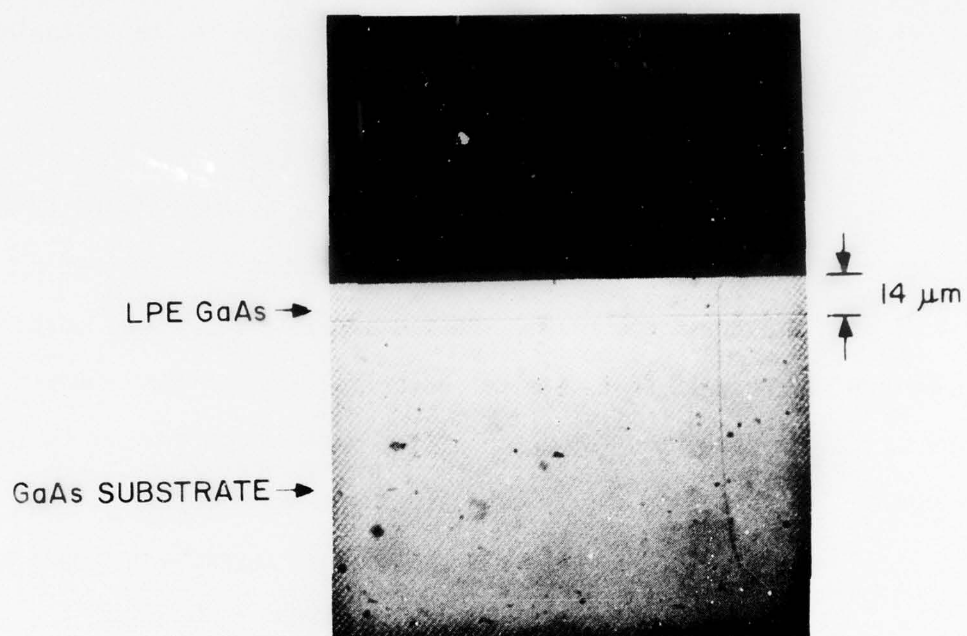


Fig. 26 PHOTOMICROGRAPH OF THE CROSS-SECTION OF AN LPE LAYER GROWN ON A Cr-DOPED GaAs SUBSTRATE.

To study the chemical reactions between the growth system components and their effect on the electrical properties of the grown layers, the growth system components, bakeout temperature of the As-saturated Ga melt, saturation temperature and hydrogen flow rate were varied. The effects of these growth conditions are discussed in the following:

1. Effects of the Bakeout Temperature

For a particular system, the electrical properties of the epitaxial GaAs layers are controlled principally by the bakeout of the As-saturated Ga melt in the growth system. Bakeout temperatures are typically in the 600-850°C range. During bakeout, impurities appear to accumulate in the melt from chemical reactions between the growth system components. To study the influence of the bakeout temperature on these reactions, the following growth conditions were held constant:

(a) melt: As-saturated Ga with no intentional dopants.

(b) bakeout period: 15 hours before each growth.

(c) saturation temperature: 700°C (Except for the SiO_2-C-H_2 system where the bakeout and growth temperatures are the same).

(d) saturation period: 30 minutes.

(3) hydrogen flow rate: 0.6 ℓ/min for both bakeout and saturation steps.

(f) cooling rage: 4.5°C/min.

The epitaxial GaAs layers grown from Ga melts had reproducible electrical properties when identical growth conditions were used. However,

such reproducibility was reached only after systematic bakeouts of the As-saturated Ga melt and growths for an accumulated period of 50-100 hours at each bakeout temperature, as shown in Fig. 27. This effect is believed to be due to the removal of volatile impurities in the source materials such as oxygen and sulphur, by extraction into the Ga melt,and volatilization into the H_2 stream during the bakeout until steady state is reached.

The bakeout temperature has the most dramatic effect on the free-carrier density as shown in Fig. 28. Low bakeout temperatures yield n-type layers while high bakeout temperatures yield p-type layers. A critical intermediate bakeout temperature, unique to each particular growth system, yields high resistivity layers with the lowest free carrier density. The transition bakeout temperatures for the SiO_2-C-H_2, SiO_2-BN(C)-H_2 and SiO_2-BN-H_2 systems were found to be 775, 700 and 675°C, respectively. Optimum compensated epitaxial GaAs layers grown in each of these systems without deep level impurity doping have room-temperature free carrier densities of 2×10^{14}, 9×10^{13} and $3 \times 10^{13} cm^{-3}$, respectively. The bakeout temperature was usually controlled with an accuracy of $\pm$ 0.5°C. However, a margin of $\pm$ 2°C is sufficient in order to obtain reproducible results.

2. Effects of the Saturation Temperature

The saturation or growth temperature has a smaller effect on the electrical properties of the layers than the bakeout temperature. The saturation period acts as a short-term bakeout, since the temperature is maintained for only 30 minutes preceding each growth. Table 5 shows, for the same bakeout temperature, the effects of the saturation temperature on the electrical properties of epitaxial layers grown from the SiO_2-C-H_2 and SiO_2-BN(C)-H_2 systems.

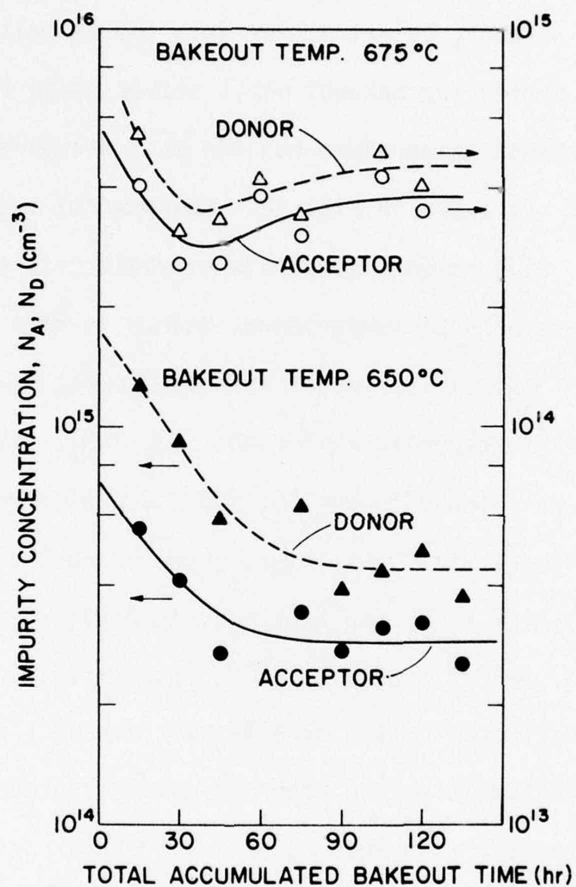


Fig. 27 Dependence of background donor and acceptor impurities on accumulated bakeout time at two bakeout temperatures. Growth system: SiO_2-BN-H_2.

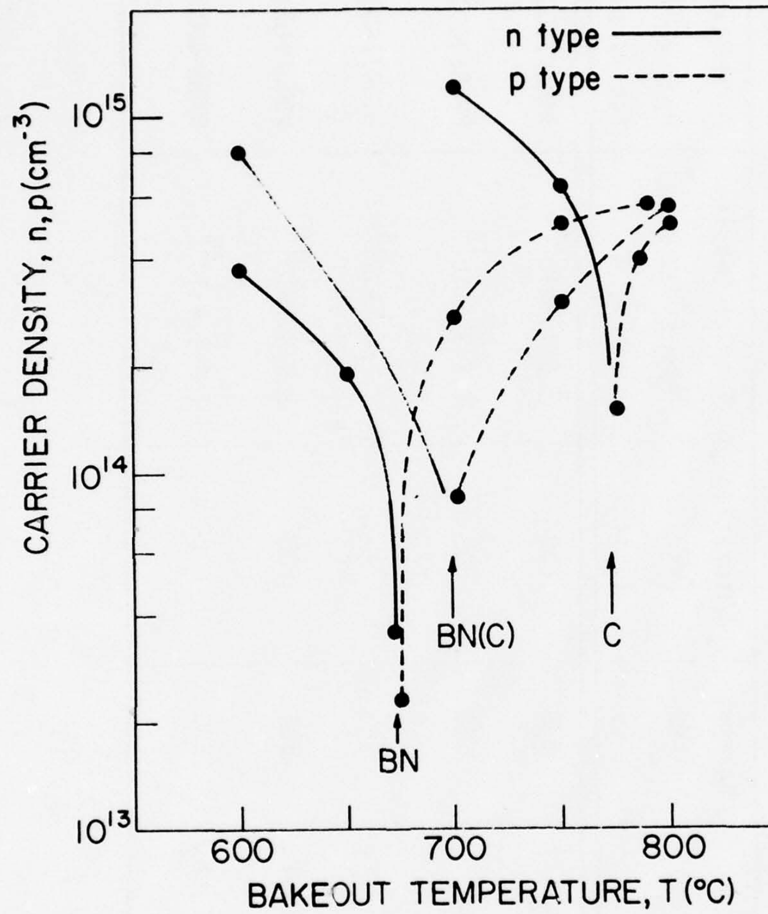


Fig. 28 Carrier density vs. bakeout temperature for three different growth systems:

C: Fused quartz-graphite-hydrogen (SiO_2-C-H_2) system.

BN(C): Fused quartz-boron nitride (on graphite cradle)-hydrogen (SiO_2-BN(C)-H_2) system.

BN: Fused quartz-boron nitride-hydrogen (SiO_2-BN-H_2) system.

Table 5

The Effect of Saturation Temperature on LPE GaAs Layers.

Growth No.	Growth System	Bakeout Temp. (°C)	Saturation Temp. (°C)	Carrier Density $n_{300\ K}/n_{77\ K}$ (cm^{-3})	Mobility $\mu_{300\ K}/\mu_{77\ K}$ ($cm^2/V\text{-}sec$)	$(N_a + N_d)$ at 77 K (cm^{-3})
104	SiO_2-C-H_2	650	650	$2.6/1.8 \times 10^{15}$	4500/36000	4.9×10^{15}
108	SiO_2-C-H_2	650	600	$5.2/3.5 \times 10^{15}$	5200/36000	5.6×10^{15}
809	SiO_2-BN(C)-H_2	600	750	$2.7/2.5 \times 10^{14}$	8100/76000	1.2×10^{15}
1102	SiO_2-BN(C)-H_2	600	700	$2.9/2.9 \times 10^{14}$	8600/91000	8.7×10^{14}
1109	SiO_2-BN(C)-H_2	600	600	$1.4/1.4 \times 10^{15}$	6700/4000	4.2×10^{15}

Saturation temperatures of 700°C and above, growths No. 809 and 1102 in Table 5 yielded almost identical carrier densities. Lower saturation temperatures, growths No. 104, 108 and 1109, yielded higher carrier densities. This is believed to be caused by the temperature being too low to decompose the oxide film which had formed on the melt and to remove the oxygen which had been absorbed in the Ga melt and in the growth system during the loading. Although saturation temperatures of 750 and 700°C yielded nearly the same carrier density, layers grown at 700°C had higher free-carrier mobilities at 77°K and lower total ionized impurity concentrations, N_a+N_d, than those of the layers grown at 750°C. This appears to be due to the lower segregation coefficient of impurities and to the lower concentrations of impurities produced during the saturation period at low saturation temperatures.

The above results show that 700°C is the most appropriate saturation temperature for the growth of high resistivity LPE epitaxial layers. Therefore, 700°C was chosen for most of the growths in this study.

3. Effects of H_2 Flow Rate

The study of the effects of H_2 flow rate on the electrical properties was carried out in the SiO_2-C-H_2 system with H_2 flow rates in the range of 0.6 to 1.2 ℓ/min. The electrical properties of epitaxial layers grown from undoped melts baked out at 775 and 800°C under different H_2 flow rates are given in Table 6. The total ionized impurity densities (N_a+N_d) were obtained from the relationships between carrier mobility and carrier concentration.[38]

TABLE 6

THE EFFECT OF H_2 FLOW RATE ON LPE GaAs LAYERS*

GROWTH No.	Bakeout Temp. (°C)	H_2 Flow Rate (ℓ/min)	Carrier Density at 300 K (cm^{-3})	Mobility at 300 K (cm^2/V-sec.)	(N_A+N_D) at 300 K (cm^{-3})	Conductivity Type
403	775	0.6	$1.6x10^{14}$	5140	$3.1x10^{15}$	n
508	775	1.2	$3.0x10^{14}$	230	$5.0x10^{17}$	p
404	800	0.6	$4.6x10^{14}$	370	$1.7x10^{16}$	p
504	800	1.0	$1.2x10^{15}$	270	$2.0x10^{17}$	p

* Growth System: SiO_2-C-H_2

At the bakeout transition temperatures (775°C), the layers changed from n- to p-type when the H_2 flow rate was increased from 0.6 to 1.2 ℓ/min. The total ionized impurity concentration increased from 3.1×10^{15} to $5 \times 10^{17} cm^{-3}$. At 800°C, both layers were p-type, but both the hole concentration and the total ionized impurity concentration were higher for the higher flow rate. It appears that high H_2 flow rates tend to enhance the chemical reactions between system components and the transport of the reactants, mainly acceptor impurities, to the Ga melt.

The above results suggest that the dominant impurities in the Ga melt with no intentionally added dopants are the products of chemical reactions in the growth system. The incorporation and segregation of these impurities at the liquid-solid interface during growth are affected by the growth temperature, the cooling rate and the concentrations of these impurities in the melt. For most of the growths in this study both the growth temperature and the cooling rate were kept constant. Therefore, the concentrations of these impurities in the epitaxial layer are principally related to their concentrations in the Ga melt.

The critical role of the bakeout temperature may be due to: (a) removal of volatile impurities in the source materials; and (b) introduction of acceptor impurities, which are the products of the chemical reactions between the growth system components, into the melt and their subsequent incorporation into the layer during growth. The concentrations of these acceptor impurities would tend to increase with the bakeout temperatures.

Therefore, at low bakeout temperatures, the acceptors introduced by the bakeout would be much less than the residual donor impurities, and the layer would be n-type. Above the bakeout transition temperature there would be more acceptors than residual donors making the layer p-type.

The identities and concentrations of electrically active impurities in the epitaxial GaAs layers can be partially inferred from photoluminescence data. The photoluminescence spectrum of a high-resistivity (1×10^4 ohm-cm) layer grown from the SiO_2-BN(C)-H_2 system measured at 2°K [39] is shown in Fig. 29. From these data, the main acceptor impurities present in the layer are identified as silicon and carbon. From the relative intensities of the acceptor-to-conduction band transition peaks (e, A°) due to Si and C, it appears that the Si concentration is higher than the C concentration, and therefore, that Si is the dominant acceptor impurity in the layers grown from the SiO_2-BN(C)-H_2 system.

The dominant residual donor appears to be related to oxygen. For high temperature melt grown GaAs, oxygen is usually added to suppress silicon contamination, and it introduces deep donors.[3] However, studies of oxygen doping in LPE growth of GaAs [40] showed that oxygen behaved differently in low temperature growths. Oxygen may act like a shallow donor, as it is a group VI element with chemical properties similar to sulphur, and it is possible that in the presence of a large Ga excess, oxygen may substitute on As sites and gives rise to a shallow donor level.

Based on the overall bakeout and growth procedures, the impurities incorporated into the layer depend on three stages of interactions:

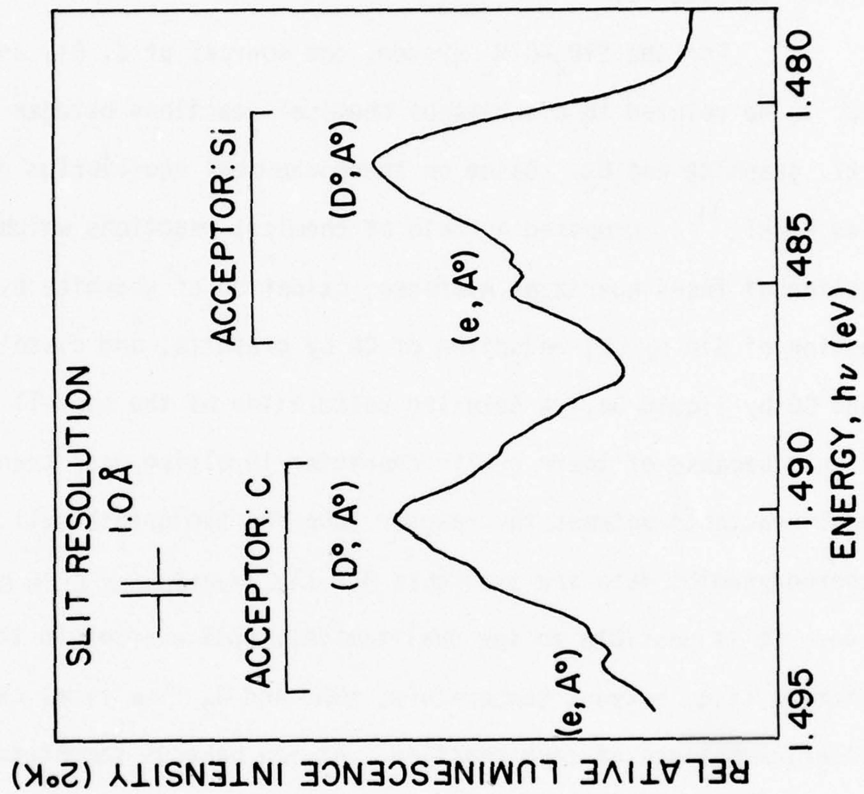


Fig. 29 Photoluminescence spectra of acceptor impurity levels in a SI LPE layer grown in a SiO_2-BN(C)-H_2 system. (e,A°): Recombination of a conduction band electron with an acceptor-bound hole. (D°,A°): Pair recombination.

(a) chemical reactions between the growth system components, (b) dissolution and formation of impurity complexes in the melt, and (c) incorporation and segregation of impurities at the liquid-solid interface during the growth. Each of these interactions are kinetically limited, i.e. dependent on time and temperature.

For the SiO_2-C-H_2 system, the sources of C, Si, and O impurities appear to be related to a series of chemical reactions between fused-quartz, graphite and H_2. Based on thermochemical equilibrium calculations, Mattes et al.[41] proposed a chain of chemical reactions which involved: Reduction of fused quartz by hydrogen, oxidation of graphite by water vapor, reduction of SiO by CO, reduction of CO by graphite, and dissolution of Si and CO by liquid Ga. A detailed calculation of the overall reactions is difficult because of their cyclic character involving mass transport of several reactants between the reactor tube and the growth cell, and because no thermodynamics data are available for the reaction of C in Ga solution. However, it is possible to see qualitatively that changes in the growth conditions (i.e. bakeout temperature, time and H_2 flow rate) can affect the equilibrium balance of each reaction. At low bakeout temperatures the reactions are slow and the oxides are more stable. Hence, there are likely to be more stable complexes or electrically inactive centers in the layer. At high bakeout temperatures the reactions are faster and many of the oxides are reduced. Thus, there are likely to be more electrically active centers to change the carrier density in the layer. The H_2 flow can shift the equilibrium balance of the reactions, and a higher H_2 flow rate will increase the rate of mass transport of reactants to the Ga solution.

For the SiO_2-BN(C)-H_2 system, with a graphite cradle present in the system, the above reactions can still take place. However, in this system the less reactive BN growth cell used to prevent the Ga melt from directly contacting graphite reduces the C contamination. As graphite is completely eliminated in the SiO_2-BN-H_2 system, the reactions between the system components are limited to reduction of quartz by hydrogen, reduction of SiO by Ga, and oxidation of Ga by water vapor. Still, in each case the rate-limiting reaction is clearly the reduction of fused quartz by hydrogen. Therefore, the increases in acceptor concentration due to bakeout seem to be of the same order of magnitude. The differences in the bakeout transition temperatures appear to be due to different values of background net ionized donor concentration, $(N_d - N_a)$, in these systems.

The effect of adding Cr to the melt will now be analyzed for each growth system.

1. The SiO_2-C-H_2 System

In the graphite cell system, when 0.7 atm.% Cr was added to the Ga melt and baked out at 700°C, the electron or hole concentration in the layer increased for bakeout temperatures far from the bakeout transition temperature on either side (see Fig. 30). However, for layers grown from Cr-doped melts baked out near the transition temperature range, the carrier concentration decreased sharply and the resistivity reached a peak of 300 ohm-cm when the Cr-doped melt was baked out at the transition temperature of 775°C.

The very large increase in carrier concentration at low bakeout temperature is believed to be due to shallow impurities contained in the Cr source which could be removed by a few hours of pre-bakeout at 800°C.

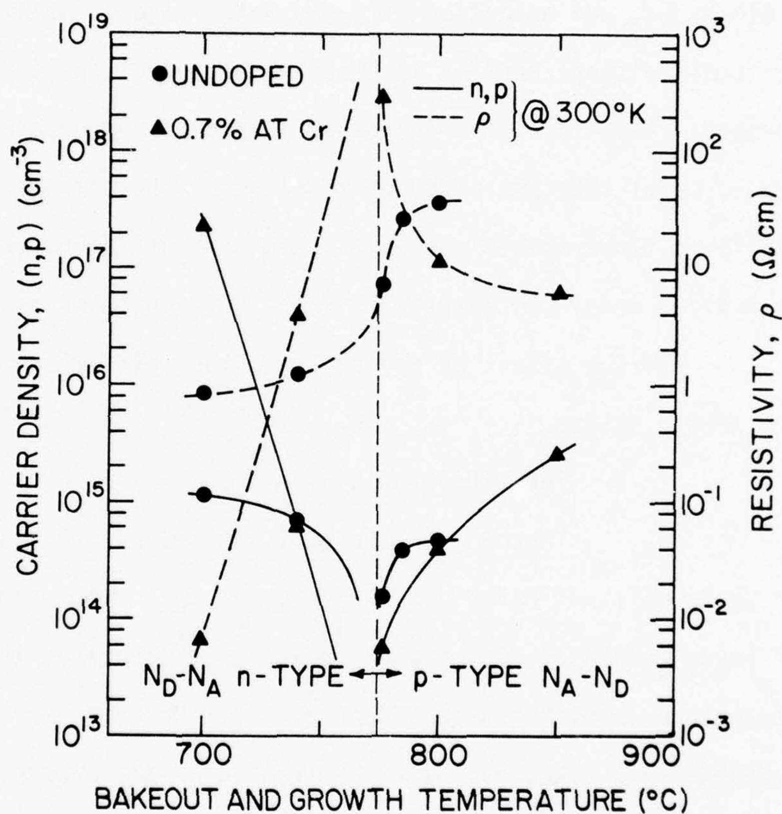


Fig. 30 Dependence of the free-carrier density and resistivity of undoped and Cr-doped layers on the bakeout temperature for a SiO_2-C-H_2 growth system.

2. The SiO_2-BN(C)-H_2 System

For the BN cell in the graphite cradle system, Cr doping has very little effect at temperatures different from the transition temperature (700°C), as shown in Fig. 31, provided a one hour pre-bakeout at 800°C is done after Cr is added to the melt. However, when 0.5 atm.% Cr was added to the melt and baked out at the transition temperature of 700°C, semi-insulating layers with resistivities higher than 10^4 ohm-cm, were obtained. The free carrier concentrations in these SI were lower than $10^{11}cm^{-3}$. The electrical properties of these semi-insulating layers will be discussed in more detail later.

3. The SiO_2-BN-H_2 System

For the BN cell system, epitaxial layers grown from Cr-doped melts, baked out at the transition temperature (675°C), have carrier concentrations in the range of $7x10^{12}cm^{-3}$. The highest resistivity obtained is $1.7x10^3$ ohm-cm. The electrical properties of epitaxial layers grown before and after doping with Cr are listed in Table 7.

This system produced the lowest free carrier concentration. ($\approx 3x10^{13}cm^{-3}$). These Cr-doped epitaxial GaAs layers have high sheet resistances, all exceeding 10^5 ohms/□, and they are quite suitable as FET buffer layers.

Note that in this system the addition of Cr had little effect, reducing the carrier concentration only by a factor of 4. It appears that under these growth conditions, there is limited incorporation of deep level impurities due to the relatively low bakeout temperature.

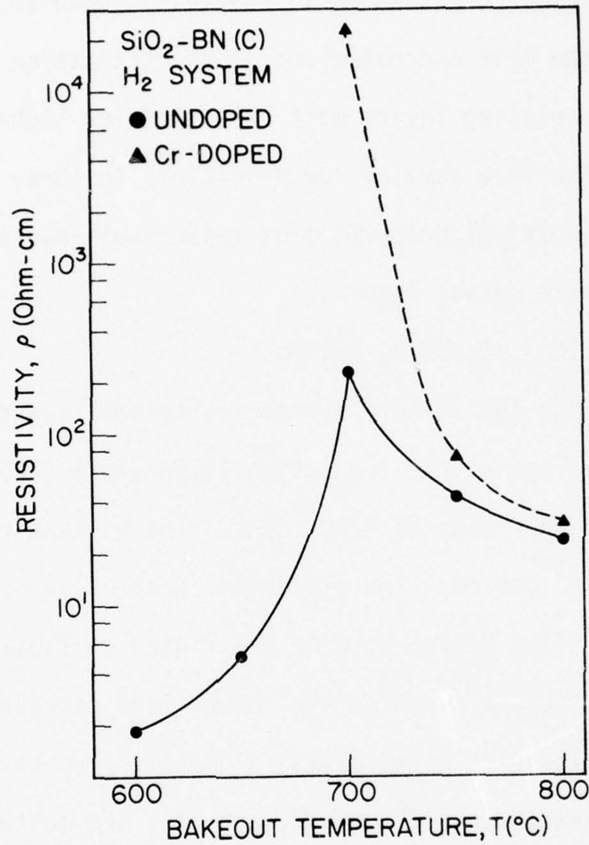


Fig. 31 Dependence of the resistivity of undoped and Cr-doped layers on the bakeout temperature for the SiO_2-BN(C)-H_2 system.

TABLE 7

ELECTRICAL PROPERTIES AT 300 K OF UNDOPED AND Cr-DOPED EPITAXIAL LAYERS GROWN IN THE SiO_2-BN-H_2 SYSTEM*

Growth No.	Dopant	Carrier Density (cm^{-3})	Mobility (cm^2/V-sec)	Resistivity (ohm-cm)	Sheet Resistance R_s (ohm/□)
2105	--	3.3×10^{13}	8200	23	1.5×10^{4}
2113	Cr	7.3×10^{12}	500	1730	1.2×10^{6}
2203	Cr	2.1×10^{13}	260	1100	7.3×10^{5}
2204	Cr	7.1×10^{12}	4600	191	1.3×10^{5}
2205	Cr	8.0×10^{12}	4200	186	1.3×10^{5}

*Growth Conditions: Bakeout Temp.: 675°C ; Growth Temp.: 700°C

H_2 Flow Rate: 0.6 ℓ/min ; Cooling Rate: 4.5°C/min

An important conclusion from the study of Cr doping of LPE high resistivity is that Cr is effective only at the critical bakeout temperature of each growth system. The reason can be found in the low segregation coefficient of Cr in GaAs which is $\sim 3.6\times10^{-7}$, at LPE growth temperatures.[42] It is estimated that 0.5 atm.% Cr in the melt lead to an active Cr concentration in epitaxial layers of only $\sim 1\times10^{14}cm^{-3}$. The net background donor concentration, (N_d-N_a), must be reduced to less than $10^{14}cm^{-3}$ before deep Cr acceptors can produce effective compensation. This can only be achieved by systematic bakeouts of the Ga melts at the transition temperature of each growth system.

The photoluminescence spectrum at 6K of a SI Cr-doped LPE layer grown in the SiO_2-BN(C)-H_2 system is shown in Fig. 32 and compared with the spectra of Cr-doped bulk GaAs samples.[43] All the spectra show a broad peak at 0.83 eV attributed to the Cr-acceptor level.[16] One difference, however, is that a peak appeared near 0.56 eV in the two bulk GaAs materials, but it is hardly detectable in the LPE layer. The photoluminescence spectrum of the LPE layer also show a sharp peak at 0.37 eV which has been assigned to an Fe level.[44] The spectrum of Fig. 32 confirms that Cr introduces in the LPE SI layers the same deep acceptor level observed in bulk grown material.

For an accurate measurement of the parameters of the high resistivity LPE layers, it is necessary to take into account the conductivity of the thick SI substrate. Therefore, a differential Van der Pauw technique has been used to measure the electrical properties of some of the high resistivity layers.

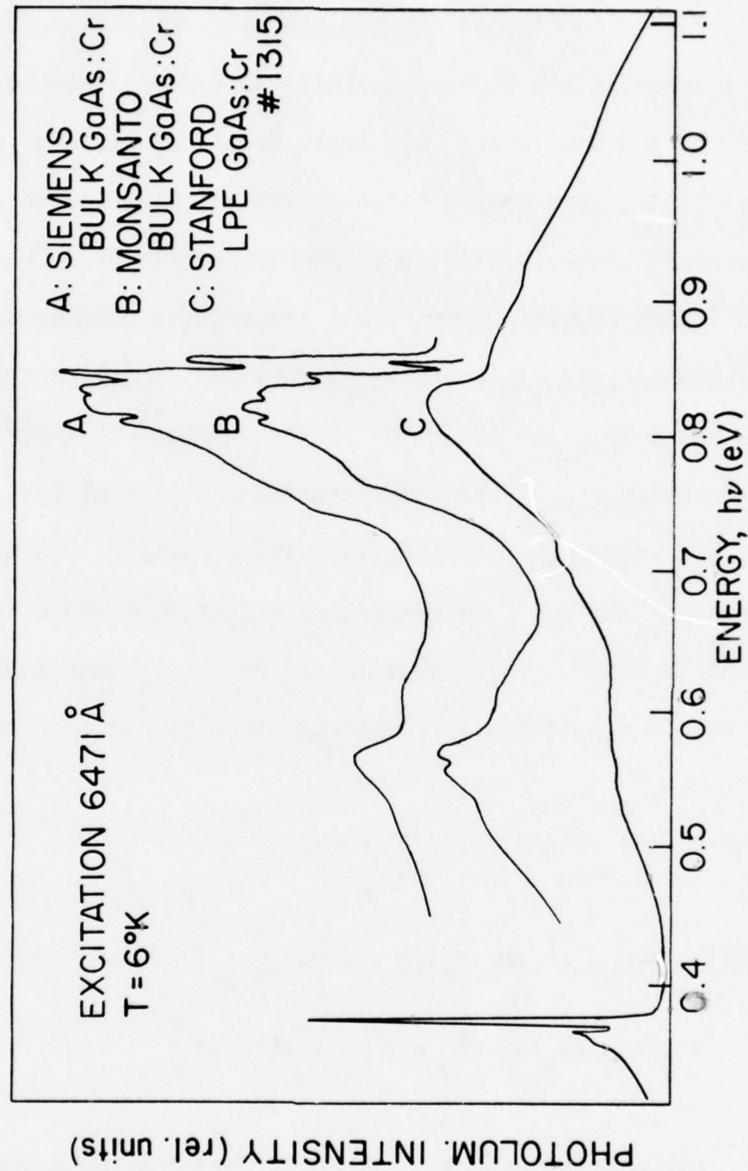


Fig. 32 Photoluminescence spectra of a semi-insulating Cr-doped LPE layer grown in the SiO_2-BN(C)-H_2 system compared with bulk Cr-doped SI GaAs.

Differential Van der Pauw measurements were made on two semi-insulating Cr-doped LPE layers grown in the SiO_2-BN(C)-H_2 system, samples No. 1315 and No. 1320. In Fig. 33 the conductivity, determined by differential Van der Pauw measurements, is plotted against 1/T for: a) sample No. 1315 based on removal at a 3.5μm layer; b) sample No. 1320, based on removal of a 7μm layer; c) the same sample based on removal of a second 3.5μm layer; d) an undoped high-resistivity (∿ 200 ohm-cm) layer. The conductivity of the Cr-doped layers showed a very strong temperature dependence while the conductivity of the undoped layer (curve D) remained almost constant in the temperature range from 300 to 420°K. This indicates that for undoped layers, the high resistivity is due to close compensation of shallow donors and acceptors. The room temperature resistivity of sample 1320 obtained from the differential Van der Pauw measurements (curves B and C in Fig. 33) is in the 10^6 ohm-cm range. This value is two orders of magnitude higher than that obtained by simple Van der Pauw measurements ignoring the substrate conductivity.

The σ vs T data of Fig. 33 were fit to:

$$\sigma(T) = (qN_v\mu_h/2)(N_a/N_d-1)\exp\left[-(E_a-E_v)/kT\right] + \\ + \left[2qN_c/(N_a/N_d-1)\right]\exp\left[-(E_c-E_a)/kT\right] \qquad (9)$$

derived from Eq. (4) applied to a deep acceptor compensating a shallow donor, as in the deep acceptor model of Sec. 3.2.1 (See also Fig. 3a).

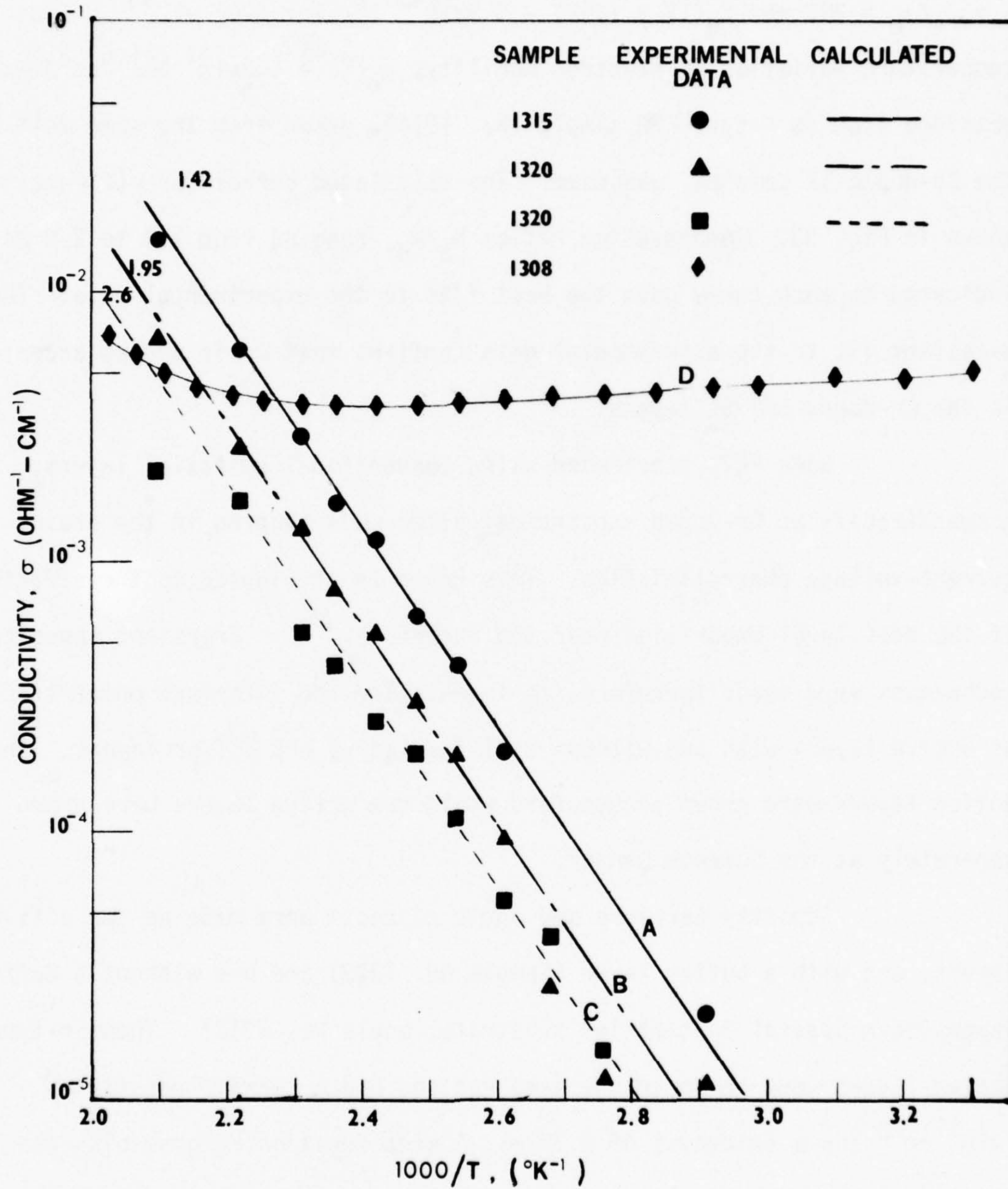


Fig. 33 Conductivity vs temperature for Cr-doped semi-insulating and undoped high-resistivity LPE layers.

For the purpose of using Eq. (9) to fit the experimental data, the following parameters were assumed: $E_a - E_v = 0.84$ eV, $m_e = 0.072\ m_o$, $m_h = 0.5\ m_o$, $b = \mu_e/\mu_e = 20$, and $E_g(T) = 1.522 - 5.8\times10^{-4}\ T^2/(T + 300)$ eV.[45] The temperature variation of electron mobility, $\mu_e(T) = 4.3\times10^7\ T^{-1.5}cm^2/V\text{-sec}$, obtained from an n-type LPE sample (No. 1814), grown from the same melt as the Cr-doped SI samples, was used. The calculated curves for $\sigma(T)$ are shown in Fig. 33. Compensation ratios N_a/N_d, ranging from 1.4 to 2.6 as indicated on each curve gave the best fits to the experimental data. The excellent fit to the experimental data confirms that Cr is a deep acceptor in the Cr-doped LPE SI layers.

GaAs FETs fabricated using conventional epitaxial layers, grown directly on Cr-doped substrates, often show looping in the drain current-voltage characteristics. This has been attributed to the effects of the deep level impurities near the interface.[46] Transient capacitance techniques were used, therefore, to investigate the interface properties of active layers with and without semi-insulating LPE buffer layers. The buffer layers were grown at Stanford while the active layers were grown separately at the Science Center.

Schottky barriers and ohmic contacts were made on two active layers, one with a buffer layer (Sample No. 1323) and one without a buffer layer (on a Crystal Specialties substrate, boule No. 2312). These n-type active layers were grown in the same run and had a carrier density of $1\times10^{17}cm^{-3}$ and a thickness of 0.35μm. A step function reverse bias was applied to the Schottky barriers and the depletion capacitance variation vs time under different initial bias conditions were recorded by an x-y

recorder (Fig. 34). The distance between the interface and the depletion region edge was adjusted by applying different values of reverse bias.

Without a buffer layer between the active layer and the substrate (Sample XS2312), when the bias was switched from zero to a reverse value the capacitance decayed with a very long time constant, taking more than 50 sec to reach a steady-state value (Fig. 34). This capacitance decay phenomenon was more prominent as the depletion region came closer to the interface at the Cr-doped substrate. From the emission time constant vs the reciprocal of the measurement temperature (Fig. 35), an activation energy of 0.58 eV was obtained in the temperature range of 255 to 273K, with a trap density of $10^{16}cm^{-3}$ near the interface.

Transient capacitance measurements made on a second active layer (No. 3x45Hb) also grown directly on a SI substrate (Crystal Specialties boule No. 2000), showed the same trapping level. In the temperature range of 295 to 350K, an additional deep trap with an activation energy of 0.81 eV and a trap density of $2x10^{15}cm^{-3}$ was obtained (Fig. 35).

In contrast with the unbuffered samples, the sample containing a buffer layer between the active layer and the substrate (Sample No. 1323), showed no long time constant capacitance decay when tested under the same conditions. The capacitance reached its steady-state value simultaneously with the bias change (Fig. 34).

The sign of the capacitance change in the unbuffered samples indicates that both the 0.57 and 0.81 eV levels are hole traps. Since there is no minority carrier injection at a Schottky barrier under zero

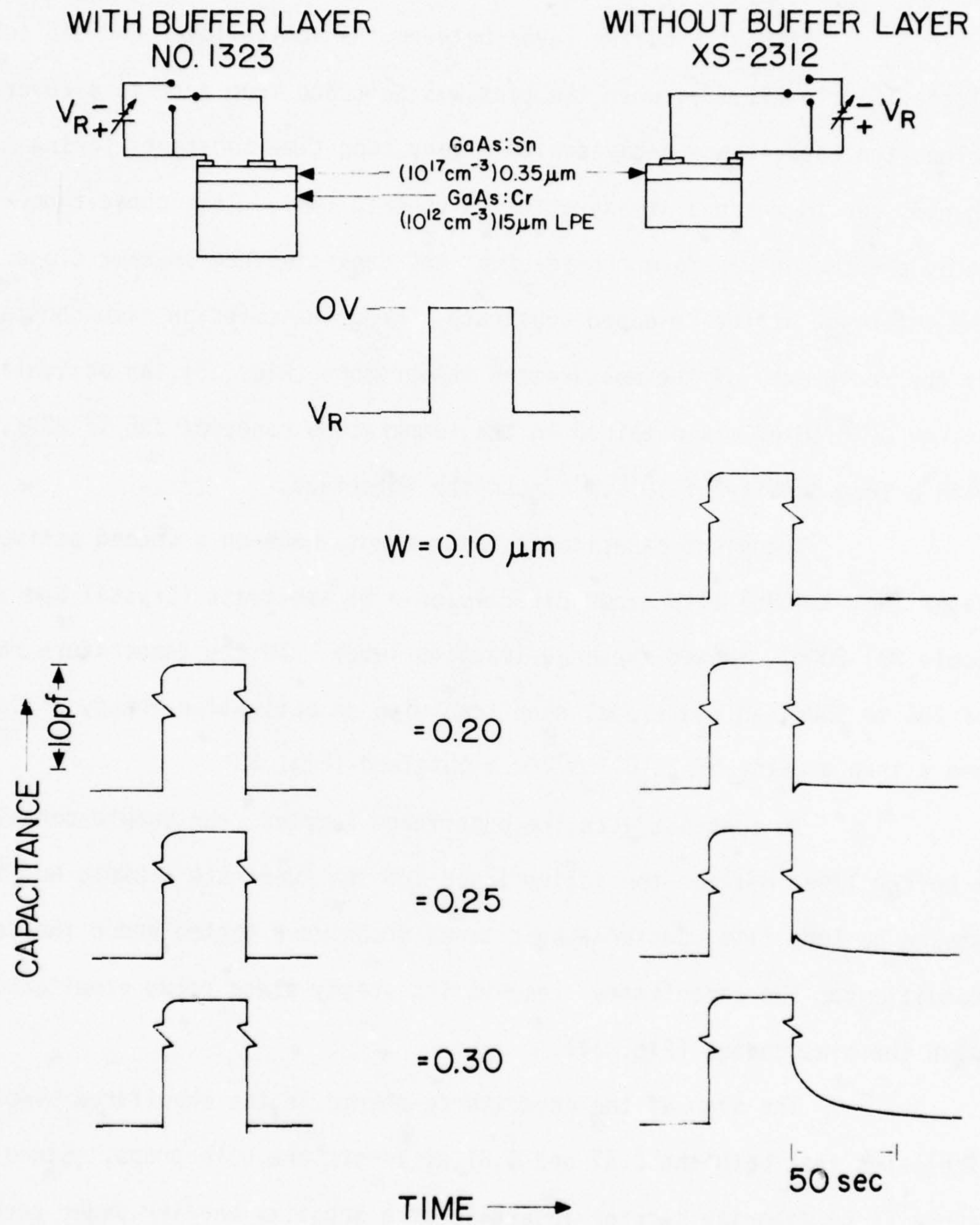


Fig. 34 Schematic diagram of the transient capacitance measurements setup and the capacitance variation with time corresponding to different bias states. W_G is the space-charge region width of the Schottky barrier gate.

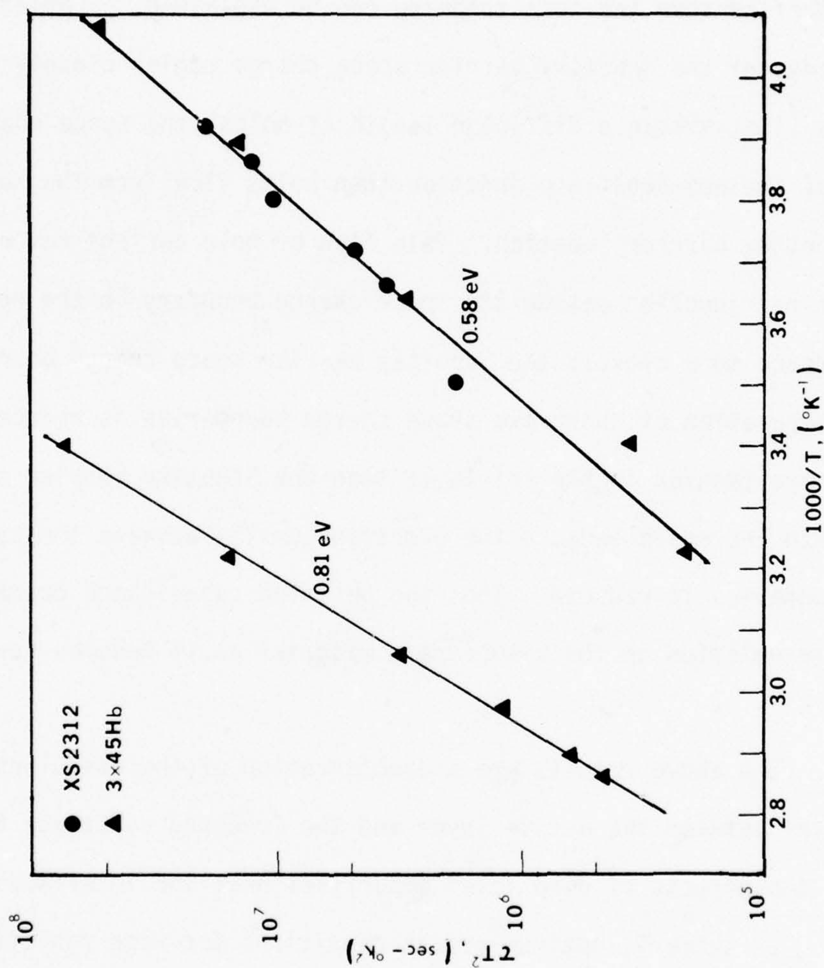


Fig. 35 THE TEMPERATURE DEPENDENCE OF THE CORRECTED TIME CONSTANT (τT^2) OF THE TRANSIENT CAPACITANCE FOR UNBUFFERED n-TYPE FET ACTIVE LAYERS.

bias conditions, there is no obvious mechanism for filling the hole traps. Experimentally, however, this apparent minority carrier trapping was observed only when the depletion edge of the Schottky barrier closely approache the epi-substrate interface. If one assumes an n-π junction at the interface then the hole trapping can be explained.[47] Briefly, when the edge of the Schottky barrier space charge region closely approaches (i.e. within a diffusion length of holes) the space charge boundary of the epi-substrate junction then holes flow from the substrate to the Schottky barrker junction. This flow of hole current reverse biases the n-π junction making its space charge boundary in the epi-layer approach more closely the Schottky barrier space charge boundary. When the separation of these two space charge boundaries is reduced to several Debye lengths in the epi-layer then the Schottky barrier space charge width increases because the electron density between the space charge boundaries is reduced. Thus the observed capacitance decrease is due to hole emission in the π-substrate material as it becomes reverse biased.[48]

The above results are a demonstration of the usefulness of a buffer layer between the active layer and the Cr-doped substrate to eliminate the effects of deep level impurities near the interface.

In summary, optimum growth conditions for high resistivity undoped LPE layers were determined, the most critical parameter being the melt bakeout temperature. The optimum bakeout temperatures for SiO_2-C-H_2, a SiO_2-BN(C)-H_2 and a SiO_2-BN-H_2 systems were found to be 775,700 and 675°C,

respectively. With these bakeout temperatures, the shallow donors and acceptors were very closely compensated, and high resistivity LPE layers with sheet resistance in the range of 10^5 ohms/□ were grown. Further improvements were obtained by the addition of Cr in the Ga melts. Cr formed a deep acceptor level. Addition of Cr produced semi-insulating LPE layers of up to 10^6 ohm-cm resistivity and 10^9 ohms/□ sheet resistance.

Interface properties of FET LPE layers with and without SI LPE buffer layers were studied by transient capacitance techniques. In the buffered FET structure, no trapping effects were observed. In the unbuffered devices, two hole traps near the substrate interface, were found with activation energies of 0.58 and 0.81 eV. This indicates that SI LPE layers can be useful as buffers to insulate the active layer from defects in the Cr-doped substrate.

4.2 Submicron LPE Growth Techniques - Science Center

Problems relating to surface morphology, uniformity and reproducibility have been the major stumbling blocks to widespread use of liquid phase epitaxy for growth of submicron thick layers for microwave device applications. At the Science Center, these problems have been addressed in developing a new LPE growth technique which has successfully been applied to the growth of GaAs FET layers. The uniformity and reproducibility of thickness and carrier concentration obtained with this method represent the state-of-the-art in LPE growth technology.

The embodiment of this LPE technique is best demonstrated in Fig. 36. This is a simplified cross-section view of a graphite boat taken through the melt compartment positioned as it would appear during growth. The As saturated Ga melt is confined to a thickness on the order of 1mm by a GaAs roof or ceiling. This configuration by insuring that the solution remains saturated, results in a much lower As gradient at the growing interface, and greatly reduces convection currents in the melt. The net result is a lower, more uniform, and repeatable growth rate, as will be shown. A temperature gradient normal to the seed crystal surface is created by a flow of N_2 cooling gas through a quartz box below the graphite platform. This gradient tends to localize the solid-liquid interface [49] and increase the nucleation density. [50] It will be shown that a gradient is instrumental in obtaining smooth continuous layers of under 2500Å in thickness. The salient features of this scheme are thus: 1) A restricted melt, with 2) A GaAs roof, which establishes an As boundary condition close to the growing interface, and 3) A temperature gradient.

Boat design is a highly important factor to the success of growing reproducibly thin, uniform epitaxial layers with good surface morphology. Shown in Fig. 37 is an exploded view of a precision machined graphite boat which incorporates the features which are found important in liquid phase epitaxy. The boat consists of a graphite slab with a substrate recess and a three compartment slider which is held to the slab with graphite rails. Although this boat contains provisions for only two melts, this system has been scaled up to six melt compartments with no deleterious effects. The center compartment contains a "plug" of graphite

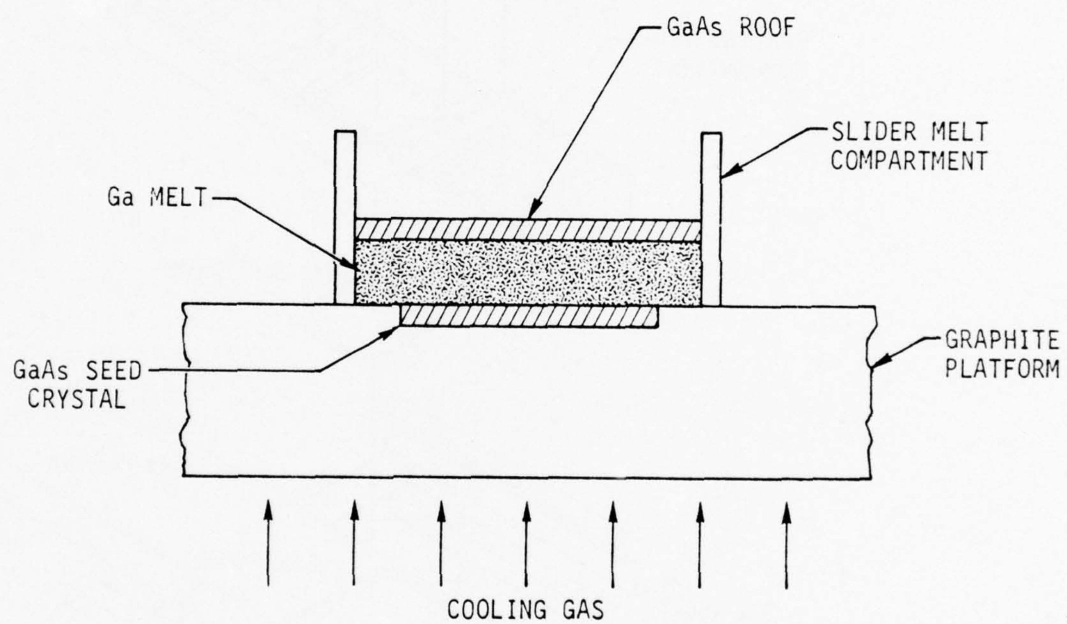


Fig. 36 Schematic representation of the restricted melt growth system

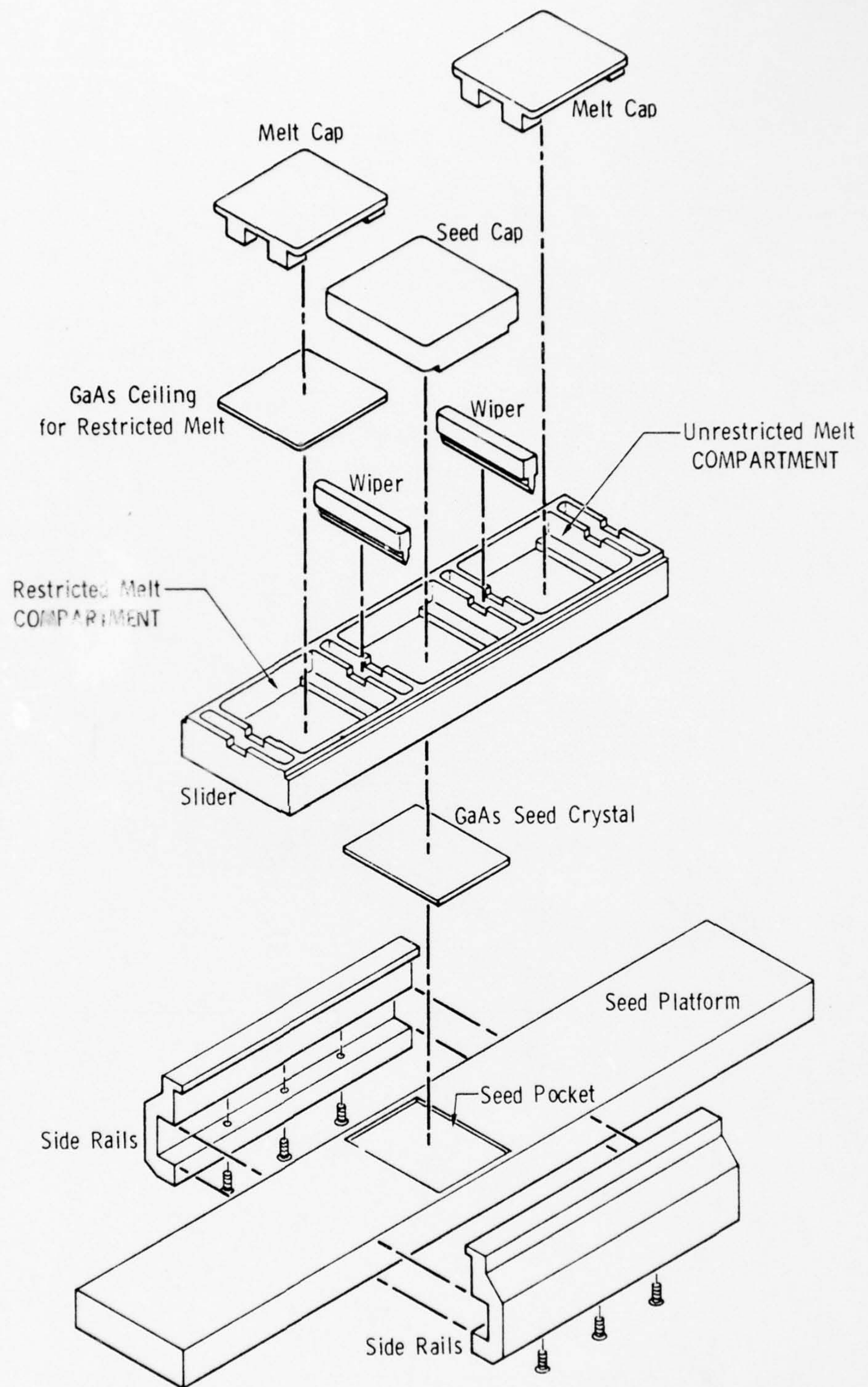


Fig. 37 Exploded view of LPE GaAs boat incorporating a restricted and unrestricted melt

which resides over the slice during the growth saturation period. This presents a thermal mass to the GaAs surface which more closely approximates the thermal condition at the beginning of growth. The two melt compartments on either side of the seed crystal have a lateral cross-section which is considerably larger than the seed substrate area. This is an effective means to prevent edge build-up of epitaxial material which interferes with device photolithographic processing; it also results in uniform layer thickness to the periphery of the wafer edge. The melts are provided with graphite covers to prevent the tendency of Ga to "ball" due to increased surface tension at elevated temperatures. Our observations of epitaxial growth from unrestricted melts in transparent furnaces lead us to the conclusion that for large area melts (approaching 1 in.) such a cover is helpful in preventing nucleation stripes which result from the unsupported melt "wiggling" like a blob of "Jello" on a flat plate. When assembled in the growth system, a quartz "cooling" box extends under the entire graphite platform. Nitrogen gas passed through this box draws heat out of the bottom of the graphite slab effecting a vertical temperature gradient normal to the substrate. The magnitude of the gradient is controlled by the N_2 flow rate. By extending the cooling box under the entire graphite platform, a flat lateral temperature profile can be maintained while the vertical gradient is being imposed.

The boat design of Fig. 37 has the provision for both an unrestricted as well as a restricted meal; the latter having a height, ℓ, determined by a machined graphite ledge on which the GaAs melt ceiling

resides. In order to quantify the term "restricted", the melt height, ℓ, must be compared to the characteristic diffusion length L of As in liquid Ga at the growth temperature. This is given by $L = \sqrt{Dt}$, where D is the diffusion coefficient of As in Ga [51] and t is the growth time. For the restricted case, $\ell < L$, it can be shown that the As concentration profile in the melt in the vicinity of the seed crystal is nearly linear, as compared to a power law dependence for semi-infinite melts. [52] The resulting lower As gradient at the liquid-solid interface for the restricted case results in increased stability of the growth front, as well as lower growth rates. For restricted melts, the layer thickness is predicted to be a linear function of growth time, while a three-halves power time dependence is predicted for unrestricted melts. [53]

Figure 38 shows the GaAs epitaxial layer thickness as a function of growth time for both melt configurations. All other growths parameters were held constant. Note that the layer thickness follows a linear time dependence for the restricted melt, as predicted, while the unrestricted melt initially shows a $t^{3/2}$ dependence. A departure, noted for the unrestricted melt data past growth times of approximately 15 minutes, is believed due to the onset of homogeneous nucleation in the relatively large melt volume. This phenomenon competes with nucleation on the seed crystal, lowering the effective growth rate. Such spontaneous effects are uncontrollable, resulting in unreproducible layer thicknesses. No such effects are noted for the restricted melts. This is expected due, in part, to the relatively small melt volume and presence of a GaAs source crystal.

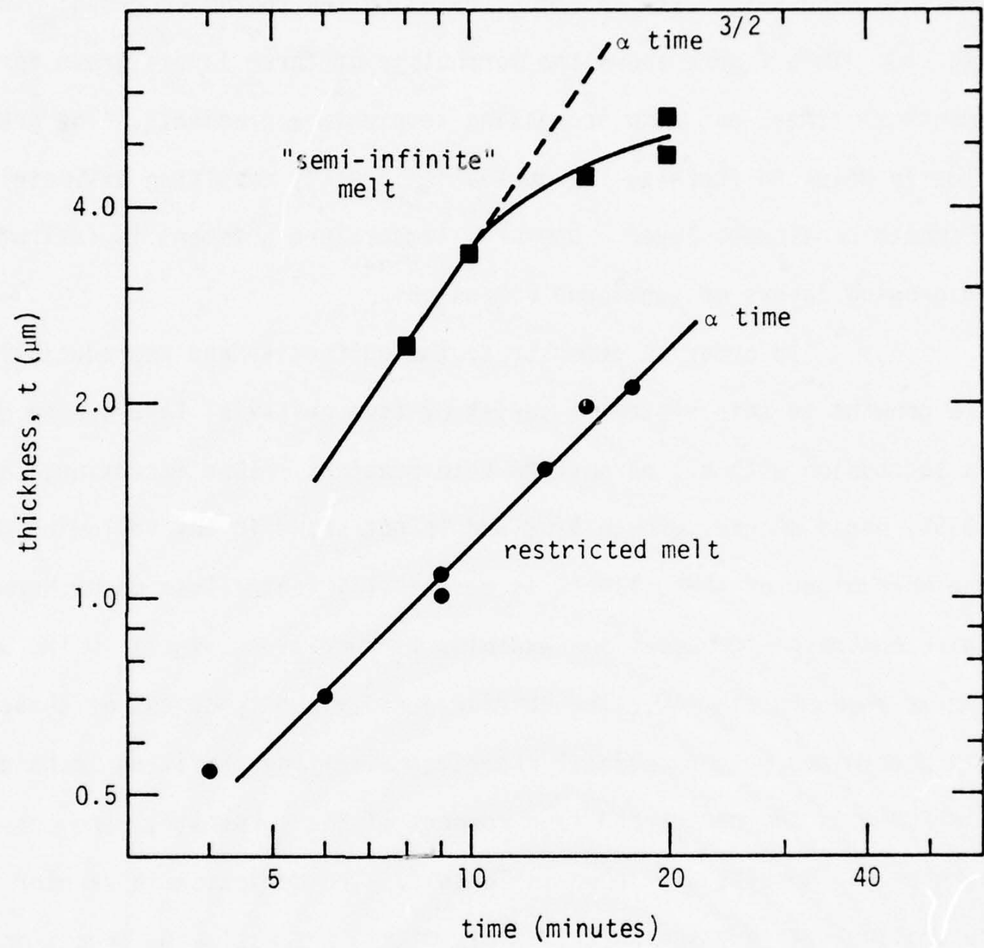
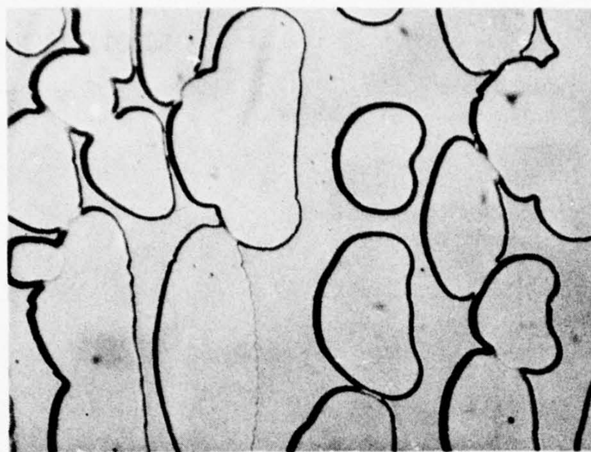
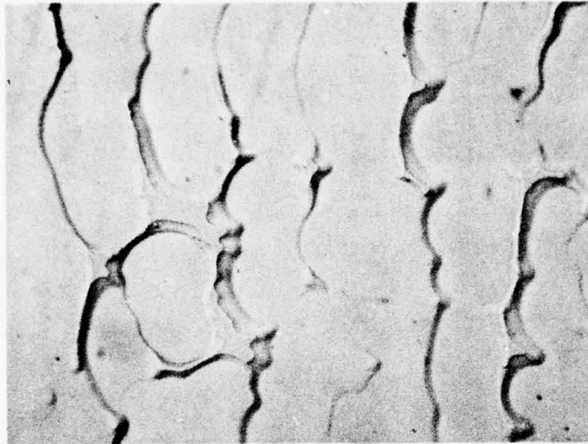


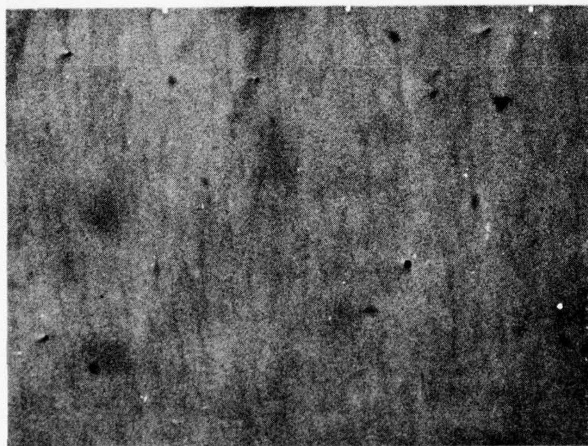
Fig. 38 Layer thickness vs growth time for restricted and semi-infinite melts

Using this system, layers as thin as 2000Å have been reproducibly grown. It has been determined that the presence of a temperature gradient is extremely beneficial in nucleating continuous layers with such small thicknesses. This is demonstrated by the photomicrograph in Fig. 39. This figure shows the morphology of three layers grown for identical times, but with increasing temperature gradients. The gradient clearly helps to increase the nucleation density resulting ultimately in a smooth continuous layer. Use of a temperature gradient is instrumental in growing layers of submicron dimensions.

In order to demonstrate the uniformity and reproducibility of LPE growths in this system, a series of five epitaxial layers were grown in succession with all parameters held constant. (One exception, layer F8J51, had a shorter growth time and is not shown in the following data). The morphology of these layers is essentially featureless under Normarski phase contrast microscopy and exhibits mirror-like surfaces to the unaided eye as shown in Fig. 40. The carrier density and thickness of these wafer was determined by conventional capacitance-voltage profiling techniques. Five points, the center and four corners of the substrate, were measured in each case. Results are shown in Table 8. The deviation in carrier concentration over any one wafer, 4%, is within the estimated precision of the measurement. The average value of N_d is repeatable from run to run within 6%. Deviation of thickness over single wafers varies from 4 to 11%, while the repeatability is again about 6%. These tests may be slightly pessimistic as the wafer edges are not necessarily representative of the average characteristics across a given slice. A more realistic statistical evaluation of the thickness uniformity of one of these layers, measured at 52







Increasing Temperature Gradient

100 Microns
Scale--All Photos

Fig. 39 Surface morphology of LPE layers as a function of temperature gradient.

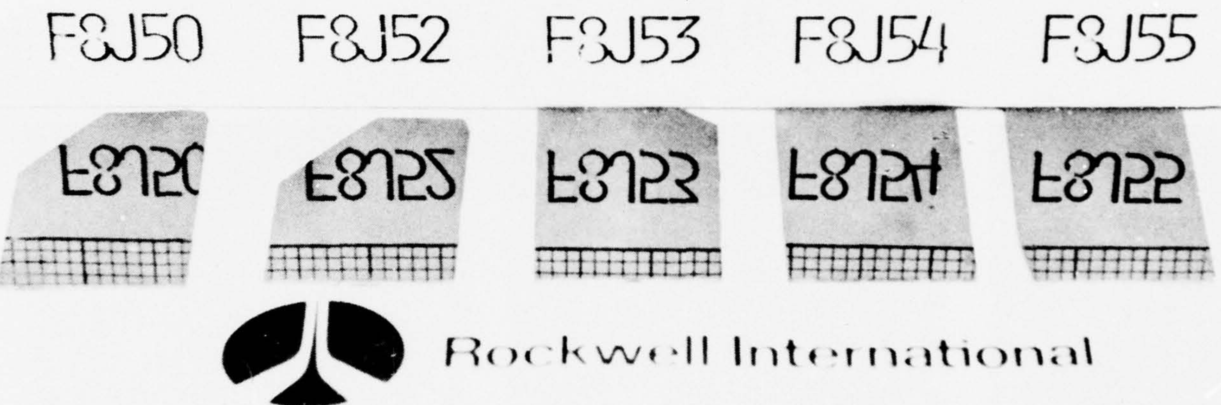


Fig. 40 A presentation of the mirror-like surfaces of five submicron thick GaAs layers.

Table 8 Data from Five LPE Layers Grown Under Identical Conditions

Run No.	Carrier Concentration N_d (cm^{-3})	Thickness t (μm)	$N_d t$ Product (cm^{-2})
F8J50	6.8 (.2) x 10^{16}	.46 (.04)	3.1 (.3) x 10^{12}
F8J52	6.3 (.2) x 10^{16}	.46 (.05)	2.7 (.2) x 10^{12}
F8J53	6.1 (.2) x 10^{16}	.51 (.05)	3.1 (.4) x 10^{12}
F8J54	5.7 (.1) x 10^{16}	.54 (.05)	3.1 (.3) x 10^{12}
F8J55	6.1 (.1) x 10^{16}	.48 (.02)	3.0 (.2) x 10^{12}
Average of the Means	6.2 x 10^{16}	.49	3.0 x 10^{12}
Standard Deviation	0.4 x 10^{16}	.03	0.2 x 10^{12}

NOTES:
1. Data are derived from capacitance - voltage measurements and represent the averages of five points measured at the center and four corners of the wafer. Standard deviations are given in parenthesis.
2. Wafer area ~ 2.5 cm^2

points equally spaced across the entire surface of the 2.5 cm^2, wafer is given in the histogram in Fig. 41. A standard deviation of under 200Å is demonstrated.

To put these data in perspective for FET applications, the product of carrier concentration and thickness is also shown in Table 8. The $N_d t$ product is a more realistic property to monitor than either N_d or t as it is related to saturation current density in an FET device. The product is also less sensitive to certain systematic errors in the capacitance-voltage measurement from slice to slice which tend to move the apparent t and N_d results in opposite directions. The uniformity of $N_d t$ over single wafers is on the order of 6-12%, while the average characteristics are reproducible to within 6%.

In summary, it has been shown that use of a restricted melt with a GaAs boundary in conjunction with a vertical temperature gradient has resulted in a significant advancement of the state-of-the-art of submicron thick layer epitaxial growth of GaAs.

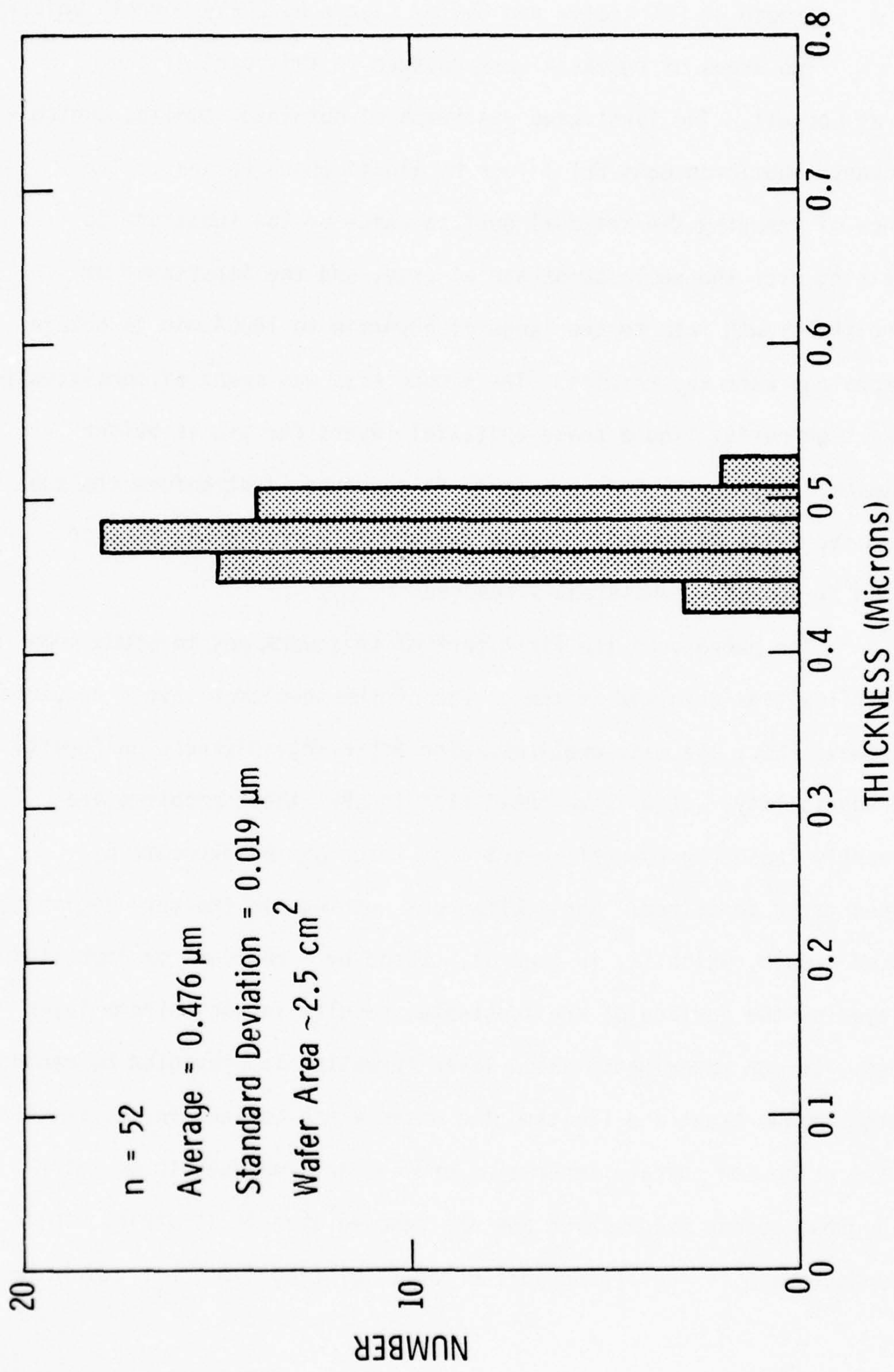


Fig. 41 Histogram of the thickness of a typical LPE GaAs wafer

4.3 Growth of FET Active and Buffer Layers by LPE - Cornell University

Two areas of research were covered in this part of the program at Cornell. The first area was means of obtaining smooth, controlled-thickness submicron GaAs FET layers by liquid phase epitaxy. The importance of removing the residual surface oxide on the substrate to allow wetting over the whole substrate at once, and the importance of confining the growth rate to the range of 500Å/min to 1000Å/min to obtain good morphology were key results. The second area was means of consistently obtaining high purity liquid phase epitaxial layers for use as buffer layers to be grown on the GaAs substrate in sequence, just before the submicron active layer is grown. Liquid nitrogen electron mobilities of 160,000 cm^2/V-sec were consistently reached.

The purpose of the first part of this work was to study some of the difficulties involved in the growth of the submicron layers required for microwave FETs, the main problems being achieving thickness uniformity and reproducibility. It will be shown that in LPE these problems are predominantly caused by nonuniform wetting, which can be overcome by techniques to be described. Nonsimultaneous wetting in the very beginning moments of growth, which is, in general, caused by a residual or deposited oxide layer on the surface of the substrate, results in non-uniform layer thickness. In our experiments oxide layer formation is prevented by making the system vacuum tight and limiting the water vapor content in the reactor. Any native oxide and surface impurities present are imbedded in an intentionally grown porous oxide layer and are removed when it is stripped off with 50% aqueous HCl. Stripping just prior to placing the substrate into

the boat allows us to start with an oxide-free surface. A source-seed crystal is located on the slider forward of the main substrate to assure precise saturation of the melt; only such saturation permits a uniform growth rate over the total surface of the substrate. By following the above techniques, submicron FET layers can be grown by LPE with as good thickness uniformity as by VPE and with significantly better reproducibility.

The reactor had a horizontal sliding boat inside a 64mm OD quartz tube heated by a three-zone resistive furance. The slider boat setup consisted of two pieces held together with precision graphite pins, with the upper part resting on the slider. This configuration allows practically negligible clearance between the bottom surface of the upper half and the substrate. The resultant wiping action upon removal of the substrate after growth eliminates localized GaAs deposition from Ga-rich melt droplets on the grown layers. This feature is of great importance in obtaining uniform thicknesses and a sharp, flat interface between successive layers, in the case where a buffer layer is to be grown.

To achieve a flat surface, the saw damage was removed by gently lapping to remove 50μm of material from both sides, with 5μm diameter grit. Then both sides were mechanically-chemically polished with 1 part chlorox in 15 parts D.I. water, exerting a pressure of 200-400 gm on the material, and taking away at least 50μm of material to a final thickness of about 250μm. A chemical etch was done in $H_2SO_4:H_2O_2:H_2O$ (5:1:1) at room temperature for 4 minutes before the substrate was loaded into the reactor.

As stressed earlier, wetting is the single most dominant factor in achieving uniform submicron epitaxial layers. Once simultaneous wetting on the surface is achieved it is then only a question of parameter selection and control (growth rate, growth temperature and saturation technique) to accomplish repeatable thickness. Any irregularities in the wetting during the early part of the growth will have a magnified effect in the thickness, because the locally wetted areas of the melt will be deficient in As concentration relative to the non-wetted areas (where deposition does not take place). This in turn allows a relatively longer growth time and larger growth rate on the nucleation centers, with a transverse surface diffusion of As to the deposition sites near the interface.

Since better wetting is achieved when the reactor is leak tight, and since high hydrogen flow rates also seem to improve wetting, one would conclude that oxide deposition on the substrate surface prior to epilayer deposition has responsibility in preventing uniform wetting.. The etch in 5:1:1 leaves a thin oxide layer (about 30-50Å) and does not remove some organic based impurities. Experiments at 735°, 750° and 780°C have been carried out to investigate the initial growth phase and the degree of wetting. Shown in Fig. 42 is a layer grown at 735°C on a substrate which had undergone a standard cleaning process. Supercooling of 1/4°C was applied to initiate a downward temperature ramp and the substrate was quickly slid under the melt, being kept there for 5 sec while the slope of the ramp

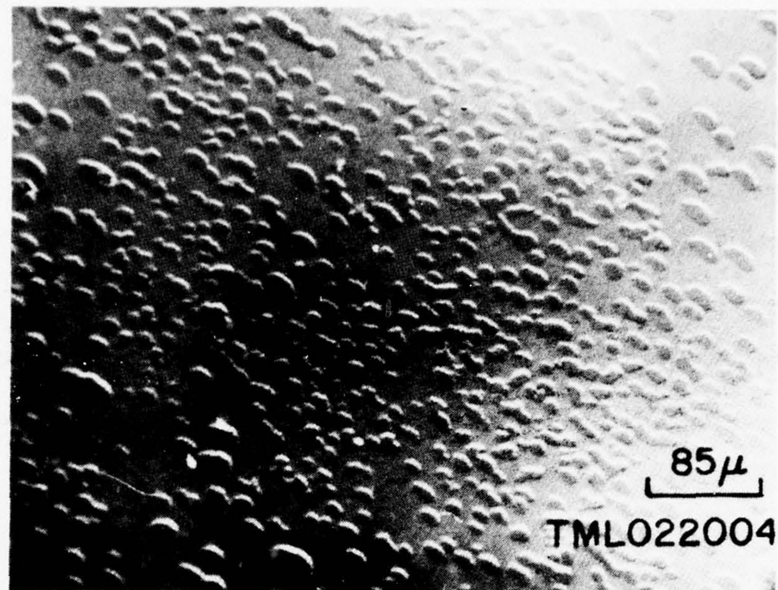


Fig. 42 Photomicrograph (Nomarski phase contrast) of a layer grown at 735°C on a substrate which had undergone only a standard cleaning procedure

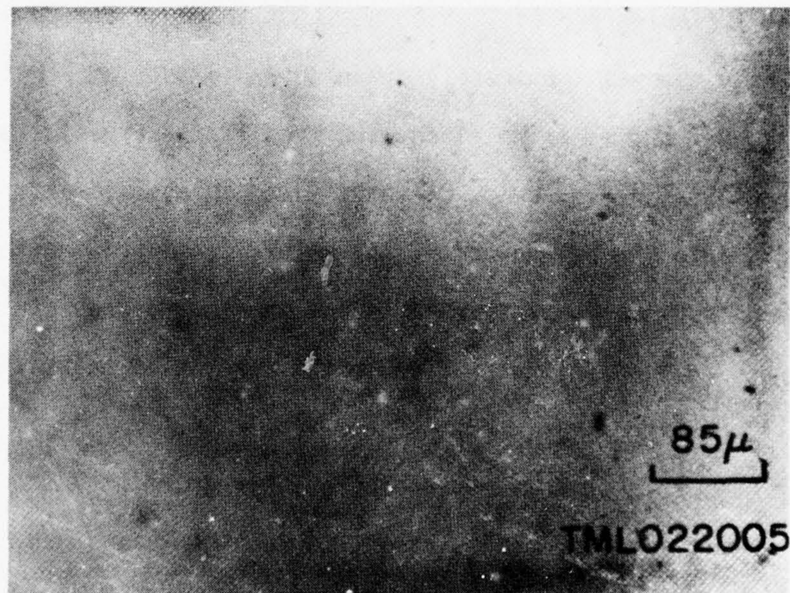


Fig. 43 Photomicrograph (Nomarski phase contrast) of a layer grown at 735 C on a substrate that had undergone a porous oxide-HCl treatment in addition to standard cleaning. Growth parameters were unchanged from that shown in Fig. 42

cooling was maintained at 1°C/min. It is clear that the growth was only initiated on small islands. There was not growth at all on most of the substrate. Similar experiments (at 750° and 780°C) indicate that the wetting becomes better as the growth temperature increases. This indicates that the residual oxide layer is removed during the relatively high temperature bakeout period and the transverse expansion of the nucleation centers is aided by the faster growth rate.

In view of published results on removal of oxide layers,[54-56] means to improve the technique of removing the oxide layers (including the native oxide) during the preparation phase were investigated. The best results were achieved by growing an approximately 150Å amorphous and porous oxide layer in room temperature DI water for 20 min. and uniformly removing it in HCl. The stripping process, which uses 50% aqueous HCl for a minimum of 5 min, not only removes the freshly grown porous oxide layer but also removes any residual native oxide along with much of the organic impurities on the outer surface. A very quick DI water rinse is applied and the substrate is loaded into the reactor after the water is blown off with high purity gaseous nitrogen. The substrate is not exposed to free air for more than about 20 sec (gaseous nitrogen flow in the reactor is maintained during loading as well).

In Fig. 43, a photomicrograph of a layer grown at 735°C on a substrate which had gone through porous oxide-HCl treatment is shown. Growth was initiated after a supercooling of 1/4°C and 5 sec growth time at a cooling rate of 1°C/min was allowed. Notice the remarkable improvement in the wetting; the layer is very uniform and nearly featureless. Based on

the growth parameters, the thickness is estimated to be below 150Å. The same experiment has been repeated at 750° and 780°C. It can be condluded that to achieve uniform sub-micron epilayers for FETs, the crucial "wetting" parameter can be controlled with porous oxide-50% HCl process.

As pointed out earlier, once the wetting is controlled, the other important parameters are the saturation of the melt solution and the growth rate. In the growth of thick layers such as Gunn diode layers, a deviation of 1° -2°C in the saturation of the melt with As will have a small effect on the final layer thickness since the total temperature drop of around 20°C takes place. By contrast, for the growth of submicron epilayers, the total temperature drop can be as low as 1.5°C (780°C, with cooling rate α = 1°C/min, supercooling ΔT = 0). Therefore, it is clear that one cannot afford any under- or over-saturation of the melt. The saturation was studied by placing a polished source-seed crystal beneath the melt after a bakeout time of 2x (melt height) ^{2}/diffusion coefficient during which the temperature was kept practically constant. The source seed was removed after 10 min,and examination showed that a very non-uniform back-dissolving occurred. Non-uniformity can be caused by strains and imperfections in the bulk material but, nevertheless, it is very likely that the bottom of the melt was undersaturated and in a non-uniform manner. Therefore, it is necessary to have a source-seed crystal (first used by Dawson) [51,54] preceeding the main substrate to trim out the As concentration of the melt at the bottom. Only then can one achieve repeatable thicknesses by controlling the growth rate on oxide-free substrates. The layers grown without

a source-seed crystal have thicknesses ranging from negative values (back-dissolving) up the the intended values.

The growth rate is the third factor that is of vital consequence to the parameters of the grown layer. Submicron layers with thicknesses of about 0.2μm have been grown at temperatures of 780°, 750°, 735°, and 700°C. The ramp cooling rate was in all cases α = 1°C/min and in certain cases supercooling of ΔT = 3°C was applied. Our experiments show that with high growth rate control over the thickness repeatibility becomes poorer. Moreover, surface imperfections, such as cusps and undulations become more pronounced. The growth rate has been calculated at 780°C including the temperature dependence of As diffusion coefficient and is shown in Fig. 44 both with and without a supercooling of 3°C. It is very clear that the difference between the two conditions is very large. The much higher growth rates associated with supercooling place nearly impossible requirements on the actual growth time, especially for submicron layers. For example, a small hesitation of 2 sec pushing the slider will mean about 2 sec of traveling time under the melt and 13 sec of actual stationary contact time (at 780°C with ΔT = 3°C). During this 2 sec, about 15% of the total growth would take place causing steps in the thickness.

Experiments were done at 780°C with only ramp cooling (α = 1°C/min) observing considerable improvement in thickness control and surface morphology. A further improvement in both occurs when a 0.2μm (or less) thick layer is grown on the source seed and subsequently a 0.2μm layer is grown on the main substrate.

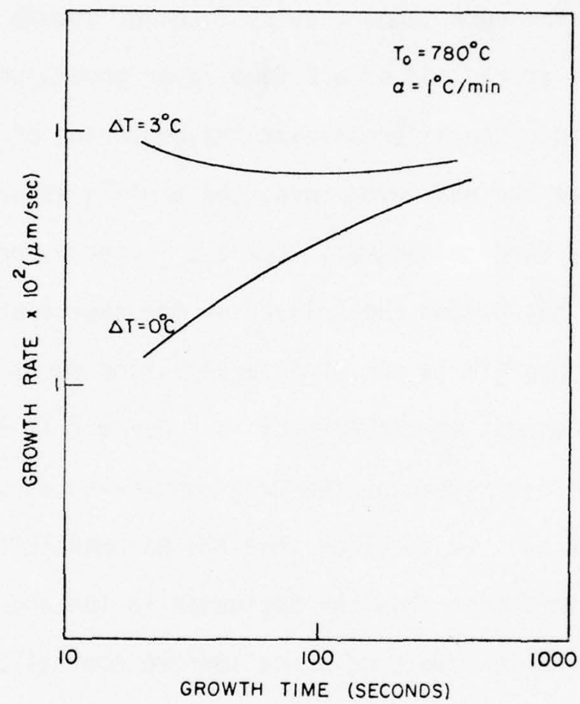


Fig. 44 Plots of growth rate at 780° C as a function of growth time both with and without a supercooling of 3° C

These phenomena can be explained by examining the As concentration profile, the slope of which at the substrate-solution interface determines the growth rate. Shown in Fig.45 is a set of calculated As profiles vs segment number at 780°C. Segment number 0 corresponds to the substrate-liquid interface at t = 0 and segment number 50 corresponds to the opposite surface of the solution (the melt height = 1cm); As profile is calculated for each segment every 2 sec of growth time. Curve b shows the As profile at the end of a 0.25μm layer growth when a supercooling of 3°C was applied. The As profile at the beginning of the growth is much steeper than at the end; even then, the profile is very steep, making the thickness very hard to control. Curve a is the As profile at the end of the growth of the 0.22μm thick layer on the source seed with no supercooling. The profile is not steep even during early growth because there are no sudden excess As concentrations. Curve c is As profile at the end of the 0.24μm layer grown on the main substrate (as opposed to the beginning profile, curve a). It is clear that the As profile follows a very nice and controllable variation from the beginning to the end. To still further decrease the growth rate (and hence improve controllability), the growth temperature was dropped from 780°C which had been the normal growth temperature down first to 750°C, later 735°C, and presently to 700°C. It was possible to lower the growth temperature so much because with the HCl treatment the substrates wet very uniformly even at 700°C.

Preliminary studies show that the layers can be grown more repeatably at 700°C than at higher growth temperatures. The optimum average

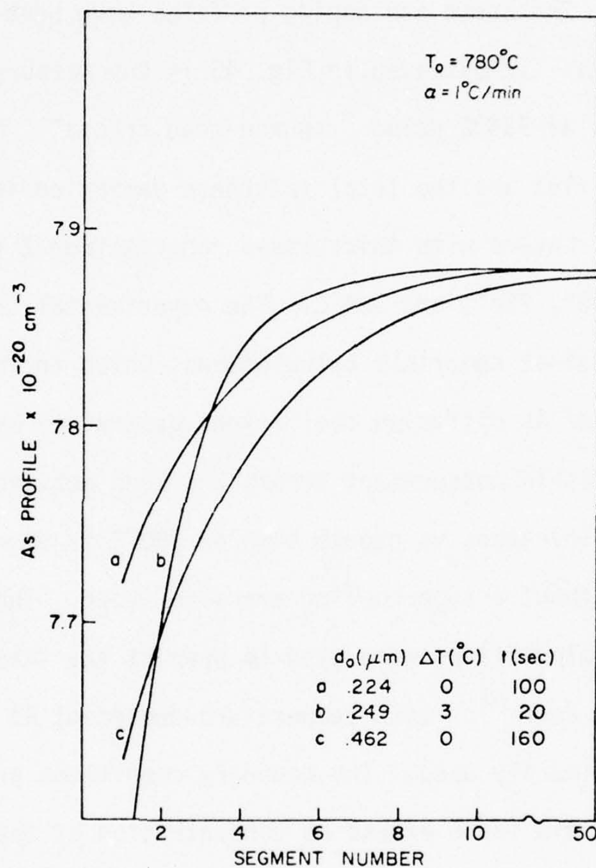


Fig. 45 Predicted As profile in Ga melt at the end of growth with various growth parameters at 780° C. d_0 represents the grown layer thickness after a time interval t at a cooling rate of 1° C/min with and without a supercooling of ΔT

growth rate to achieve minimum cusp density has been experimentally determined to be about 800Å/min. The density of the cusps decreased considerably ($10^5 cm^{-2}$ at 780°C and $10^2 cm^{-2}$ or less at 700°C), as well as timing errors, because the growth rate was slower, taking almost 3 min to grow 0.2μm thick layers.

Thickness and doping profiles have been deduced from C-V measurements. Illustrated in Fig. 46 is the measured doping profile of a layer grown at 735°C using a source-seed crystal. Notice that the doping profile is flat and the total thickness variation is small.

Layers with thicknesses ranging from 2 to 5μm have been grown at 700°, 735°, 750°, and 780°C. The experimental thickness data have been compared against numerical calculations, which included the temperature dependence of As diffusion coefficient determined by Rode,[51] and close agreement within measurement errors has been achieved. In Fig. 47, the calculated thickness vs growth time at 780°C is shown. Four data points with and without a supercooling are also shown. Two distinct methods of numerical calculations were used to predict the thickness. The technique reported by Rode [51] with temperature-dependent As diffusion coefficient has been primarily used. The boundary conditions are identical to those reported by him (zero excess As concentration at the interface and zero spatial derivative of excess As concentration at the top of melt). The melt height in our experiments is 10mm.

In Fig. 48 and 49, the same curves as those shown in Fig. 47 are repeated for 750° and 735°C, respectively. A thickness reproducibility from layer to layer of ± 0.015μm, and a thickness uniformity as low as

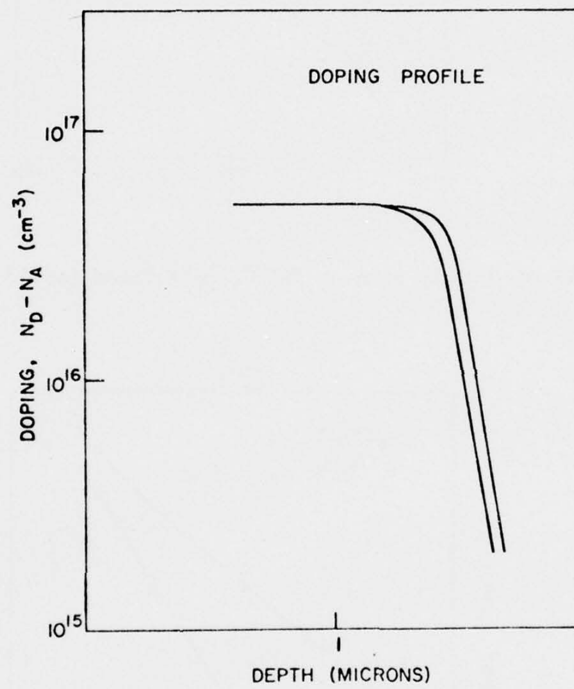


Fig. 46 Doping profile of a layer grown at 735°C using a source-seed crystal with no supercooling

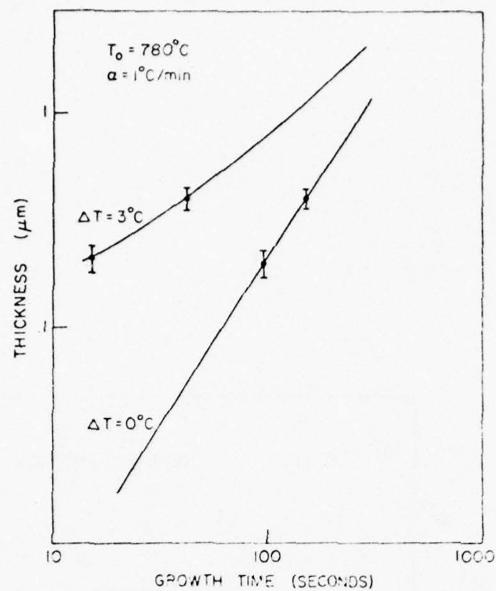


Fig. 47 Thickness vs. growth time at 780°C, calculated (solid lines) and experimental.

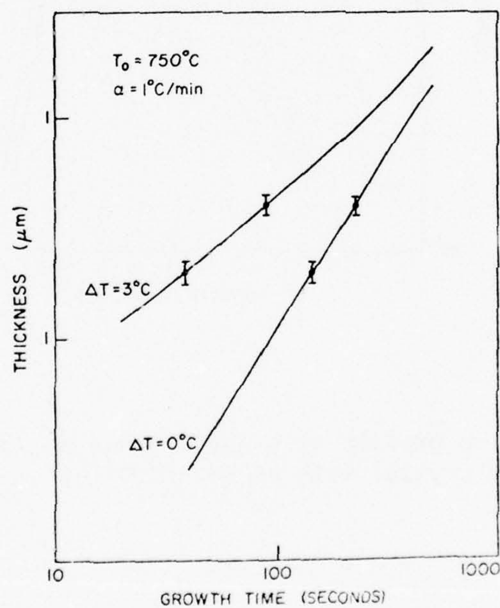


Fig. 48 Thickness vs. growth time at 750°C, calculated (solid lines) and experimental.

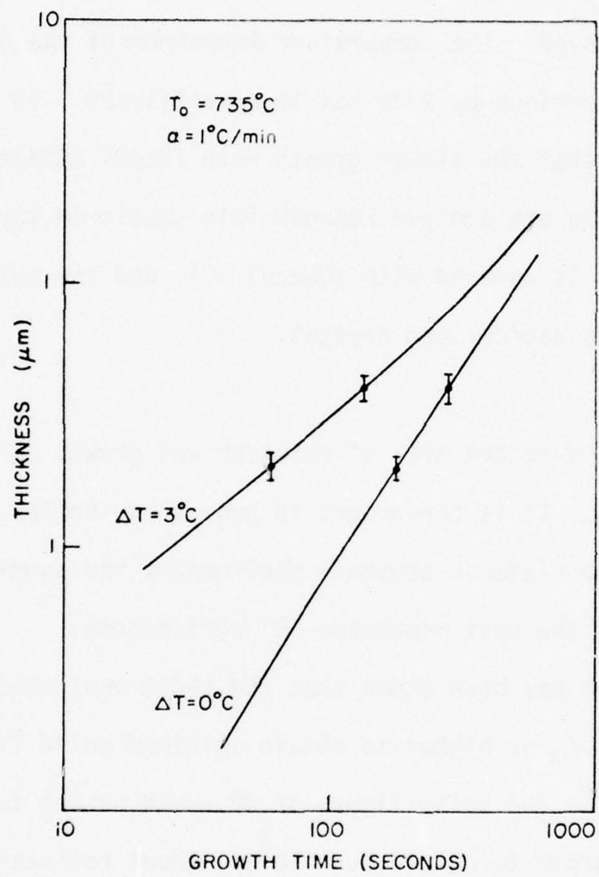


Fig. 49 Thickness vs. growth time at 735°C. Calculated (solid lines) and experimental.

$\pm$ 4% over a portion of the layer that excludes the edge lip, can be achieved with these techniques.

In summary, the controlled-growth mechanism and the factors affecting it have been examined in detail for the growth of submicron FET layers. Remarkably good agreement between theory and experiments has been achieved. The temperature dependence of the As diffusion coefficient determined by Rode has been reaffirmed. It has also been demonstrated that the slower growth rate (about 800Å/min) at lower growth temperature one can achieve reproducible submicron layers when any oxide layer present is removed with aqueous HCl, and the melt saturation is trimmed with a source-seed crystal.

The second area of research was growth of high purity GaAs buffer layers. It is convenient to grow these buffer layers on the semi-insulating substrate in sequence just before the submicron active layer is grown, for the best microwave FET performance.

It has been shown that the sheet resistance of a buffer layer should be $10^6 \Omega/\square$ or higher to obtain minimum noise figure in microwave FET devices.[56] The noise figure in dB would be one third higher for $10^4 \Omega/\square$. In order to obtain such $10^6 \Omega/\square$ sheet resistance, electron concentrations ranging from 10^{12} to $10^{13} cm^{-3}$ are required. Such carrier concentrations are achieved in vapor phase epitaxy by slowing down the growth rate, so that a compensating, fast-diffusing acceptor is allowed to diffuse into the buffer from the semi-insulating substrate. Such VPE buffers would be n-type and range from 120,000 cm^2/V-s - 200,000 cm^2/V-s mobility at 77K if they were grown rapidly. In the liquid phase epitaxy

to be described below, 160,000 cm^2/V-s mobility at 77K is achievable using a long baking time (24 hrs) at 700°C during runs from a given melt. This yields less than $1x10^{14}cm^3$ electron concentration without intentional compensation. Typically 10^{13} - $10^{14}/cm^3$ electron concentration can be obtained easily by LPE by this method.

The approach here is different from that taken at Stanford for growth of semi-insulating buffer layers (Sec. 4.1). At Stanford, it was found that self-compensation of impurities ahd hence low net ionized impurity concentration, occured after baking the melt for a long period of time at a temperature characteristic of each growth system, which was 775°C for systems employing a graphite boat. A similar "notch" temperature has been observed at Cornell. However, the goal of Cornell's work was to achieve low total ionized impurity concentration. This was best accomplished by baking the melt for a relatively long period of time during the saturation and growth cycle and by keeping the temperature low, typically at 700°C, so that a lower concentration of impurities were incorporated into the system. The loading, baking and growing procedures are also different in the two approaches. At Stanford, the melt is baked for 15 hours at the notch temperature, so that the impurities in the melt became chemically compensated. The system is then cooled down, the substrate is loaded, and the layer is grown after a 30 minute bake to resaturate the melt. The saturation and growth time are intentionally kept short compared to the 15 hour bakeout, so that the melt compensation is not significantly disturbed. Furthermore, the melt is shielded by a GaAs crust during the growth cycle. In the high purity approach taken

by Cornell and described here, exposure of the boat and melt to the atmosphere during substrate loading requires a long bake to remove CO and other contaminants through and around the melt. This is done in a slightly unsaturated condition, so that there is no crust on the melt which might trap volatile impurities. The long bake purges the melt of impurities until a low equilibrium level is reached.

The main precautions required in order to repeatably get the limiting LPE purity with graphite boats and pure H_2 gas flowing in a quartz tube can be summarized in ten rules:

1. Bake the boat in vacuum at 1400-1500°C until the pressure drops.
2. Clean the quartz tube in aqua regia.
3. Bake the boat in H_2 at 850°C.
4. Bake the boat in H_2 with a discardable Ga melt at 800°C.
5. Bake each melt in a slightly undersaturated condition (12 hrs 750°C, 24 hrs. 700°C) each run. Use of a glovebox to avoid exposure of the boat and melt to the atmosphere during substrate loading might reduce the required baking time.
6. Bake melt at temperature above the melt oxide formation temperature in 700°C gor Ga in graphite.
7. Use source GaAs material with high mobility (over 7000 cm^2/V-s).
8. Keep the H_2O partial pressure low (1ppm at 750°C and .5ppm at 700°C are limits).

9. Keep the exposure of the boat and melt to the atmosphere at a minimum (only a few minutes).

10. Keep the boat and melt in H_2 and as hot as possible (bake over 780°C to recover purity if in cold H_2 for days).

Numerous layers with thicknesses ranging from 5 to 15μm have been grown at 750, 735, 700 and 665°C to investigate the dependence of background impurities on the baking and growth temperatures. The thickness uniformity across each layer surface was better than 15%. No noticeable meniscus lines or terraces have been observed, but there were a very few isolated cusps. The etch pit density on the surface of the buffer layer was always lower than that on the substrate. Usually there was about a 5:1 reduction for thin buffer layers, but for thick buffer layers there was nearly a 10:1 reduction in etch pit density. Although generally only the buffer layer was grown, the presence of a melt doped with Sn and growth of an active layer did not noticeably change the net donor concentration in the buffer layer. The growth of buffer layers at temperatures as low as 665°C is possible because the aqueous HCl treatment of the substrate prior to loading yields very unifrom wetting. A strong correlation between the total impurity concentation and both baking time between the runs and growth temperature has been observed.

In table 9 through 11 are the electrical properties of layers growh at 750, 735 and 700°C. The total ionized impurity concentration vs baking time is plotted in Fig. 50 for each growth temperature. As can be seen from the tables and Fig. 50, each time the reactor is opened for

Table 9

Electrical properties of layers grown at 750°C; (cooling rate α=0.1°C/min).

Layer No.	Mobility at 77 K (cm^2/V-sec)	$N_d - N_a$ (cm^{-3})	$N_d + N_a$ (cm^{-3})	Baking time (h)	Layer thickness (μm)
CS011904	70,600	1.3×10^{15}	1.5×10^{15}	6.5	5
LD012501	105,000	3×10^{14}	6.5×10^{14}	10.5	11
LD012502	60,300	2.2×10^{13}	2.1×10^{15}	16.5	11
LD042503	107,000	1.23×10^{14}	6.4×10^{14}	20.5	11
LD052504	160,000	4.3×10^{13}	1.9×10^{14}	9	11

Table 10

Electrical properties of layers grown at 735°C (cooling rate α=0.1°C/min).

Layer No.	Mobility at 77 K (cm^2/V-sec)	$N_d - N_a$ (cm^{-3})	$N_d + N_a$ (cm^{-3})	Baking time (h)	Layer thickness (μm)
TML022002	100,000	3×10^{14}	7.4×10^{14}	12.5	5
TML022006	73,000	4×10^{14}	1.5×10^{15}	8.5	5
CS012101	77,600	1.8×10^{14}	1.3×10^{15}	11.5	11
CS012102	97,500	1.8×10^{14}	7.5×10^{14}	13.5	11
LD042103	120,000	1.5×10^{14}	4.8×10^{14}	20	14

Table 11

Properties of layers grown at 700°C; due to a GaAs crust on the melt at the growth temperature, LD052601 exhibited very low mobility (cooling rate α=0.1°C/min).

Layer No.	Mobility at 77 K (cm^2/V-sec)	$N_d - N_a$ (cm^{-3})	$N_d + N_a$ (cm^{-3})	Baking time (h)	Layer thickness (μm)
LD042301	132,000	1.4×10^{14}	3.5×10^{14}	17.5	8.5
TML022305	71,000	3.7×10^{14}	1.6×10^{15}	12	8.5
TML022308	135,000	1.8×10^{14}	3.3×10^{14}	17	8.5
TML022402	170,000	1.2×10^{14}	2.2×10^{14}	25.5	8.5
LD042302	163,000	0.9×10^{14}	2×10^{14}	34	8.5
LD052601	23,200	9.5×10^{13}	1×10^{16}	26.5	8.5

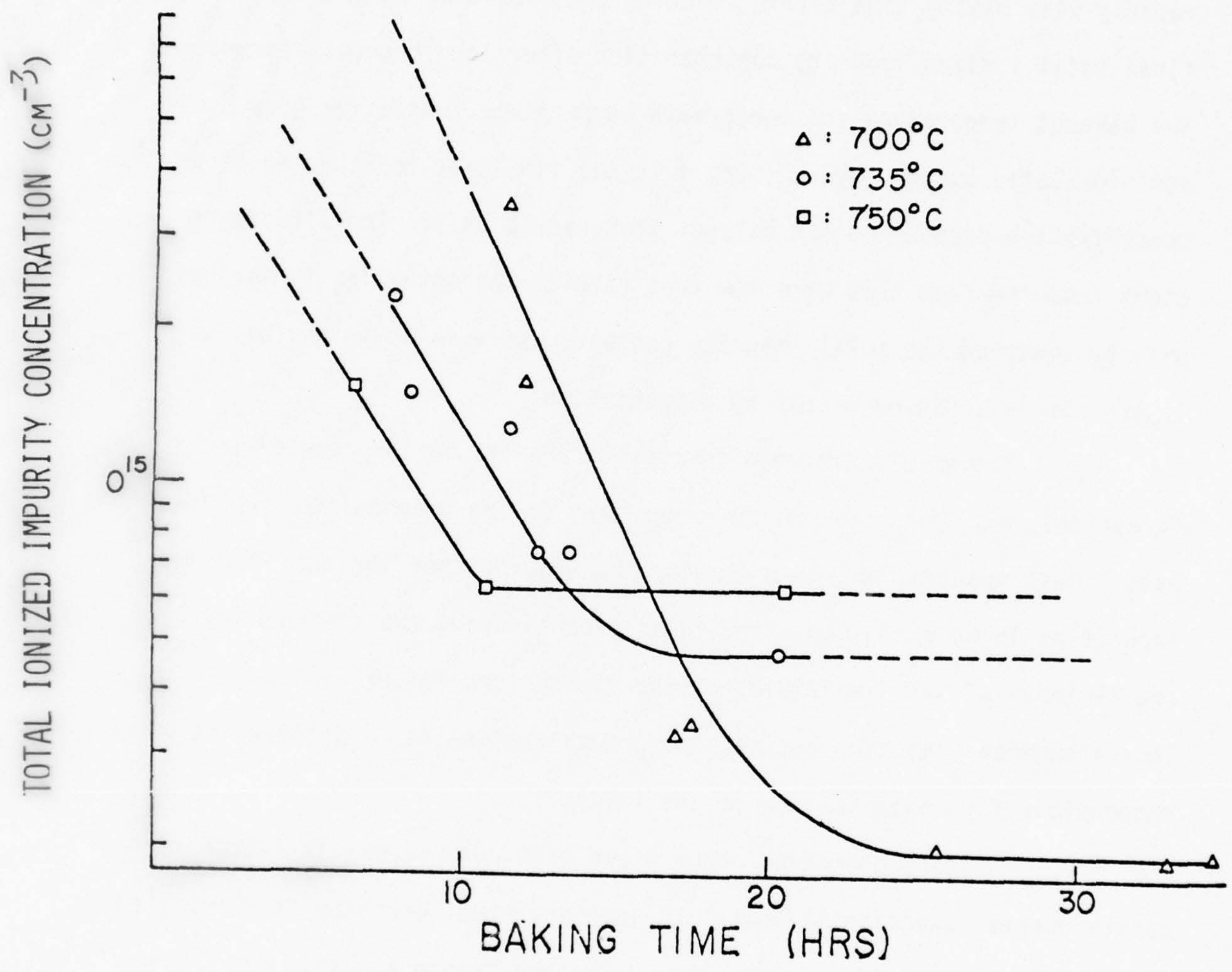


Fig. 50 Total ionized impurity concentration versus baking time.

loading, additional impurities are introduced and trapped inside. It takes between 10 hs of baking at 750°C and 24 hs of baking at 700°C to outgas most of these impurities. The impurity concentration drops off rapidly with baking time before reaching equilibrium. Note that here the final total ionized impurity concentration after long bakeout depends on the bakeout temperature and the growth temperature, while for growth of semi-insulated buffer layers (Sec. 4.1) the final net ionized impurity concentration depends on the bakeout temperature only. The difference stems from the fact that here low free carrier concentration is achieved only by lowering the total impurity content, while in semi-insulating layers, it is achieved mainly by compensation.

The only extraneous components present in the reactor are C (graphite), H_2, SiO_2, O_2 and the impurities in the original Ga and source GaAs. Mass spectrum analyses done by the manufacturer indicate that the impurities in Ga are minor, particularly considering the distribution coefficients of such impurities at the growth temperature employed. Thus a chemical reaction between the growth components is believed to be responsible for contamination of the layers.

Hicks and Greene[58] have grown very pure layers in a high purity quartz (Spectrosil) boat. In such a system, graphite is eliminated, so one need not consider C impurity. Hicks and Greene analyzed the thermodynamics of the chemical reactions and found a theoretical expression for Si contamination from the quartz walls and the boat. By growing with such a system, Hicks and Manley[59] have reported the highest mobility layers ever grown. In addition, they observed a reduction in Si contamination with increasing water vapor content. The only significant difference

between this latter apparatus and ours is the porous graphite boat. This, therefore, suggests the possibility of direct C contamination. But, this can be ruled out by our measured dependence on between-run baking time, which also implies that the role of introduced O_2 is crucial. To check this supposition, a test layer was grown with two 15 hs baking cycles at 700°C separated by a 5hs cool period, but without the reactor being opened to air. Performance of this layer exactly duplicated that of one grown under the same conditions with a continuous 30 h baking time. Our tests suggest that the O_2 somehow transports C to the melt in the form of CO. This effect could be reduced by using vitreous carbon. Unfortunately, the vitreous carbon cannot be machined into a sliding boat.

Experimentally determined equilibrium values of total donor density (N_d) plus total acceptor density (N_a) at 750, 735 and 700°C are presented in Fig. 51 as a function of reciprocal temperature. The Si contamination calculated by Hicks and Greene[58] for 0.5ppm water vapor content and the difference between this curve and our results are also shown. This difference is probably caused by carbon forming CO at the growth temperature being used. The carbon hypothesis is supported by Mullin's detection,[60] using photoluminescence, of a major acceptor line in GaAs grown in a graphite boat.

If the $N_d + N_a$ line in Fig. 51 is extrapolated to 665°C (dashed line), one would expect a value of $8 \times 10^{13} cm^{-3}$ for $N_d + N_a$ and 200,000 cm^2/V-sec for the mobility at 77K. However, as shown in Table 12, the layers grown at 665°C have exhibited mobilities of 91,000 cm^2/V-sec or lower at 77K. The discrepancy is believed to be caused by the temperature not being high enough to decompose the thin oxide crust on the melt

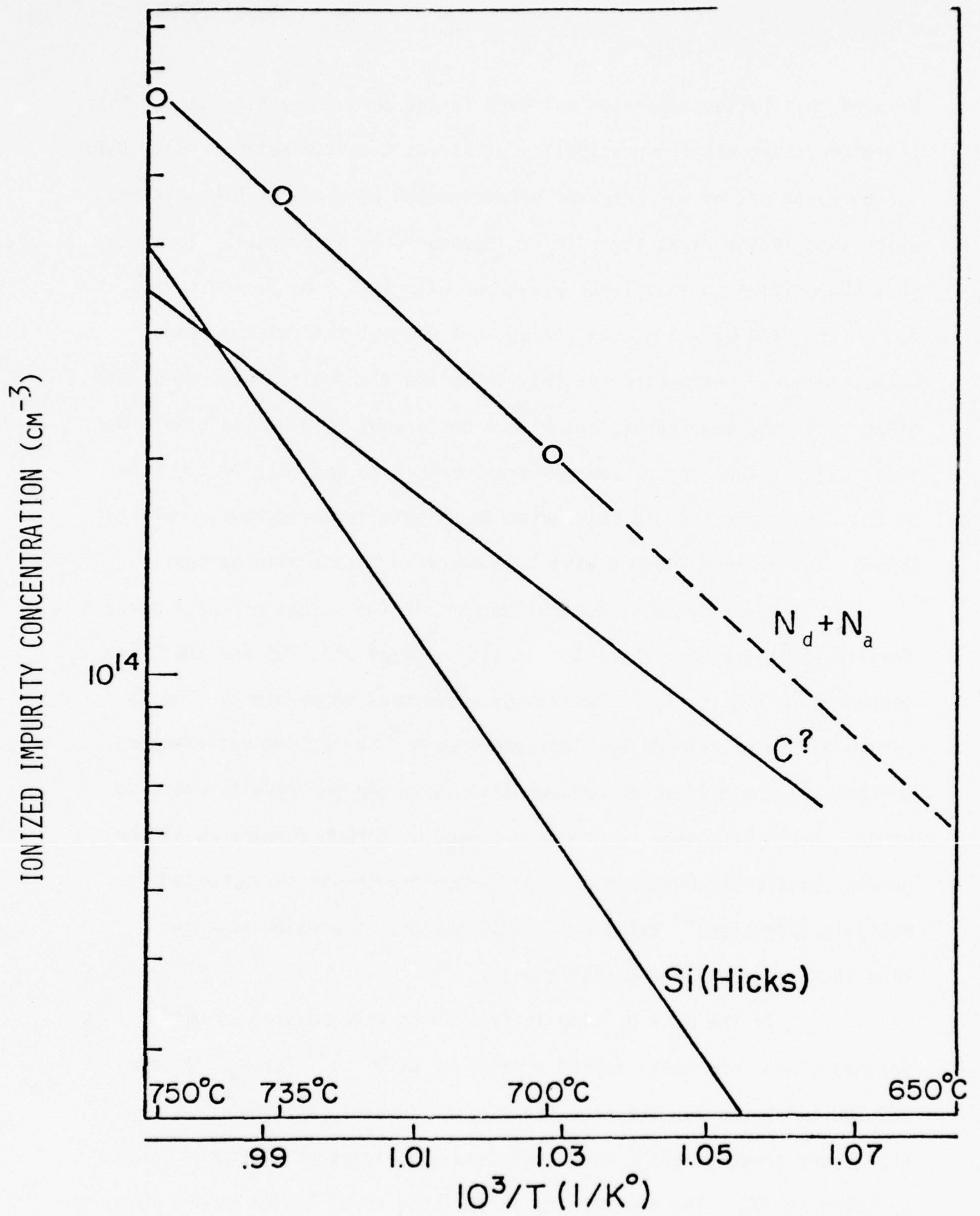


Fig. 51 Ionized impurity concentration versus reciprocal temperature.

Table 12

Electrical parameters of layers grown at 665°C; TML02301 was grown by a two-step baking process: 6.5 hs at 750°C and 18hs at 665°C (cooling rate α=0.1°C/min)

Layer No.	Mobility at 77 K (cm^2/V-sec)	$N_d - N_a$ (cm^{-3})	$N_d + N_a$ (cm^{-3})	Baking time (h)	Layer thickness (μm)
LD053001	91,000	1.6×10^{14}	9×10^{14}	28	5
LD053002	65,000	1.2×10^{14}	1×10^{15}	52	5
TML023501	30,000	7×10^{13}	7×10^{15}	6.5 + 18	5

top surface, which confines the impurities inside the melt. O_2 adsorbed by the porous graphite boat during loading, and present in the reactor due to SiO_2 dissociation, is responsible for the formation of this oxide crust. Shaw[61] has shown that such an oxide layer decomposes in H_2 atmosphere at temperatures above 700°C in agreement with out observations. In order to try to break this oxide layer, an epitaxial layer (TML023501, see Table 12) was grown at 665°C after baking the melt at 750°C for 6 1/2 hs and at 665°C for 18 hs, but the resulting impurity concentration was still high. In addition, a layer grown at 700°C (LD 052601, see Table 11) from a melt deliberately covered by a GaAs crust at the growth temperature showed very low mobility. One therefore infers that the melt should "breeze" to outgas the volatile impurities. More experiments need to be done below 700°C to be conclusive concerning the proper procedure to avoid the oxide layer difficulties.

In summary, GaAs grown by LPE in a graphite boat has been shown to be n^- type if the melt has been baked between runs in a H_2 atmosphere for sufficient time. After baking for 10 hs or more at 750°C, mobilities of 105,000 cm^2/V-sec at 77K were repeatably achieved. After baking for 24 hs or more at 700°C mobilities of 163,000 cm^2/V-sec at 77K were repeatably obtained. Below 700°C the impurities are not purged from the melt due to the presence of an oxide layer on its surface. The presence of a melt doped with Sn does not seem to cause any difficulties in maintaining high mobility in the buffer layer. Therefore, uniform submicron active layers for FET devices can be grown immediately after the buffer layers in the same operation.

In light of Stanfords' success in lowering the net free carrier concentration by Cr-doping (Sec. 4.1), it may be possible to use Cr-doping in order to obtain n-type material with a net free carrier concentration lower than $10^{14} cm^{-3}$ by the techniques presented in this section.

5.0 ION IMPLANTATION AND ION BEAM ANALYSIS

Our ion implantation work has been concerned with the doping achieved by implantation of the n-type dopants S, Se and Te in GaAs at low and high doses. The purpose of the low dose implantation work was to attain the capability of producing n-type layers on semi-insulating GaAs which were suitable for FET fabrication. Both S and Se have been used as dopants for this purpose and FETs have been fabricated from many of the n-type layers produced by low dose implantations. The electrical profiles resulting from low dose implants directly into semi-insulating substrate materials are sensitive to the quality of this substrate material. The question of substrate qualification tests and the reproducibility of Se implantation results in good substrate material is discussed in Sec. 5.1. In Sec. 5.2 the results achieved with high dose Se and Te implantations are presented. This work has demonstrated that it is possible to use implantation to achieve doping levels which will be quite useful in reducing the contact resistance to devices such as FETs. Our work with S implantation is discussed in Sec. 5.3. While the doping efficiency obtained with S implantation is lower than with S or Se, it appears to be useful for applications requiring doping to depths beyond those which can be achieved with Se or Te. In order to achieve good activation of high dose n-type implants, it seems to be necessary to carry out the implantation at an elevated temperature. We believe this requirement is associated with preventing the formation of amorphous layers during implantation. Some work has been carried out on the recrystallization of amorphous layers on GaAs in an effort to determine

whether or not a hot implantation for high dose implants could be avoided. This work is described in Sec. 5.4. Finally, in Sec. 5.5, work using ion beam analysis methods to study the processes which occur when Ni-Au-Ge or Pt-Au-Ge contact metalizations are alloyed on GaAs is discussed.

5.1 Reproducibility of Low-Dose Se Implants - Science Center

In order to employ ion implantation into semi-insulating (SI) GaAs substrates for device fabrication, it is important that the doping produced by implantation not be affected by changes in the substrate. In addition, in a planar device technology, it is essential that unimplanted portions of the substrate do not become conducting during post implantation annealing so that device isolation will be maintained. Two tests have been employed in order to determine whether or not SI substrate material was suitable for ion implantation doping. One test involved annealing a capped sample at the temperature used for the annealing of implanted samples. A second test utilized ion bombardment with an inert gas to simulate the disorder introduced during the implantation of the dopant. The bombarded sample is then capped and annealed at the same temperature as is used for the annealing of doped samples (usually 850°C). The test without ion bombardment is analogous to the heat treatment test used to evaluate substrate material for epitaxial growth (see Sec. 3.2.4). The test involving ion bombardment is more severe but appears to be essential in determining whether or not substrate material will yield reproducible implantation results.

Good reproducibility of implantation doping profiles was found when the implantation was done into substrates which remained semi-insulating

after both types of qualification test described in the preceeding paragraph (to be referred to as "good" semi-insulating GaAs). Figure 52 shows profiles obtained for low energy Se implants into two samples from each of 5 different boules of good SI GaAs. The annealing was carried out at 850°C for 30 min using a reactively sputtered silicon nitride cap (see Sec. 5.2). The maximum doping level and the thickness of the doped layer are reproducible within ± 10%. Se implanted layers on qualified SI substrates have been extensively used in the fabrication of FETs. The properties of these FETs are discussed in Sec. 6.1.

Material from some boules of semi-insulating GaAs was found to be incapable of passing either qualification tests. Results for samples from three different boules of "bad" material are summarized in Table 13. This material showed n-type conducting layers following either the heat treatment or the bombardment test. Boule number 2132, which exhibited the largest change, was material specially prepared to have a very high Cr content (approximately $5x10^{17}cm^{-3}$). The conductivity of the n-type layers formed during the annealing test is somewhat higher in the Kr bombarded samples than in those which received no bombardment prior to capping and annealing. Electron concentration profiles results obtained from Se implants into some of this "bad" material are compared with profiles obtained by implantation into "good" SI material and into a low electron concentration epitaxial layer in Fig. 53. The doping level for the sample from boule #2132 is much higher than that for any of the other samples. Since the SI material normally used for implantation does not contain the very high Cr level of this material, this result will not be discussed further. The profiles

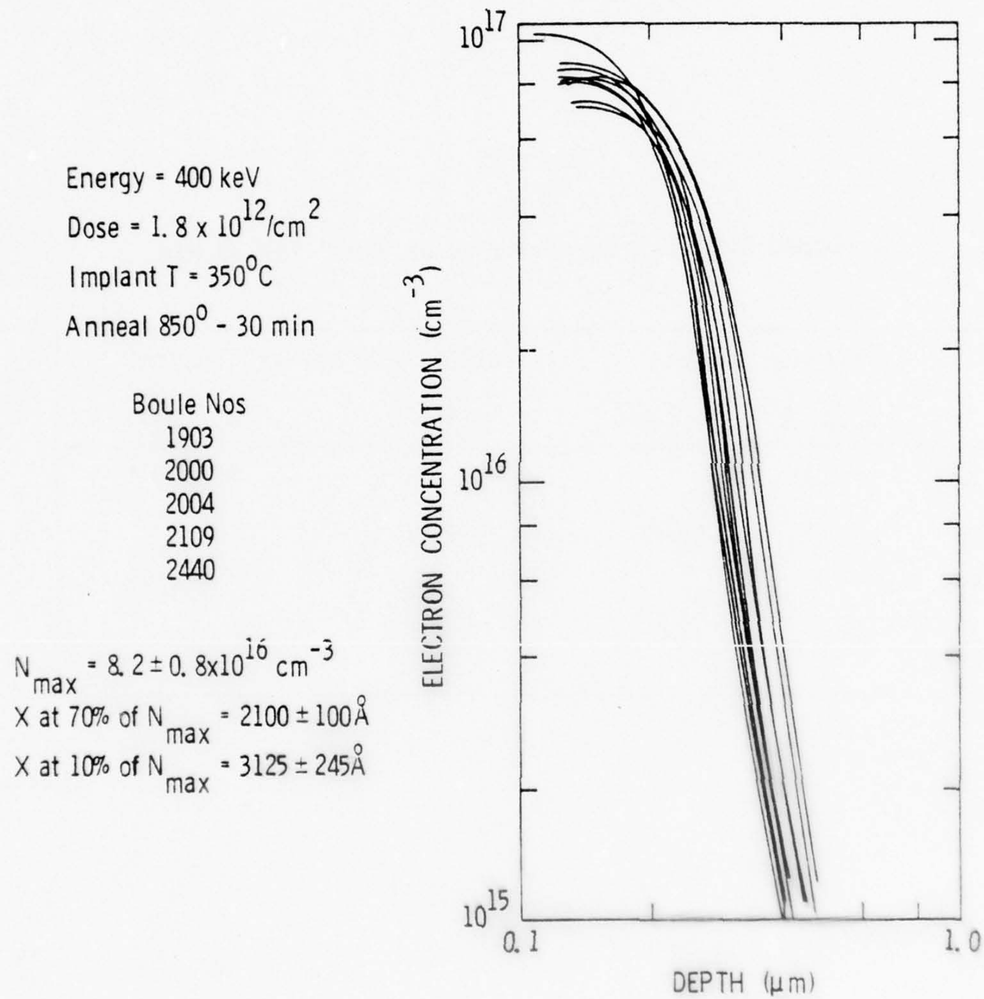


Fig. 52 Electron concentration profiles for Se implants into "good" semi-insulating GaAs substrates.

Table 13

Cr-Doped GaAs Samples Annealed at 850°C for 30 Min.

	Without Implant		1.8×10^{12}-400 keV Kr ions/cm^2	
	ρ_s (Ω/□)	N_s (cm^{-2})	ρ_s (Ω/□)	N_s (cm^{-2})
2132	~ 1500		482	4.2×10^{12}
2299	2250	5×10^{11}	~ 1500	
2312			1220	1×10^{12}
Typical	Good Material		~ 6×10^{8}	

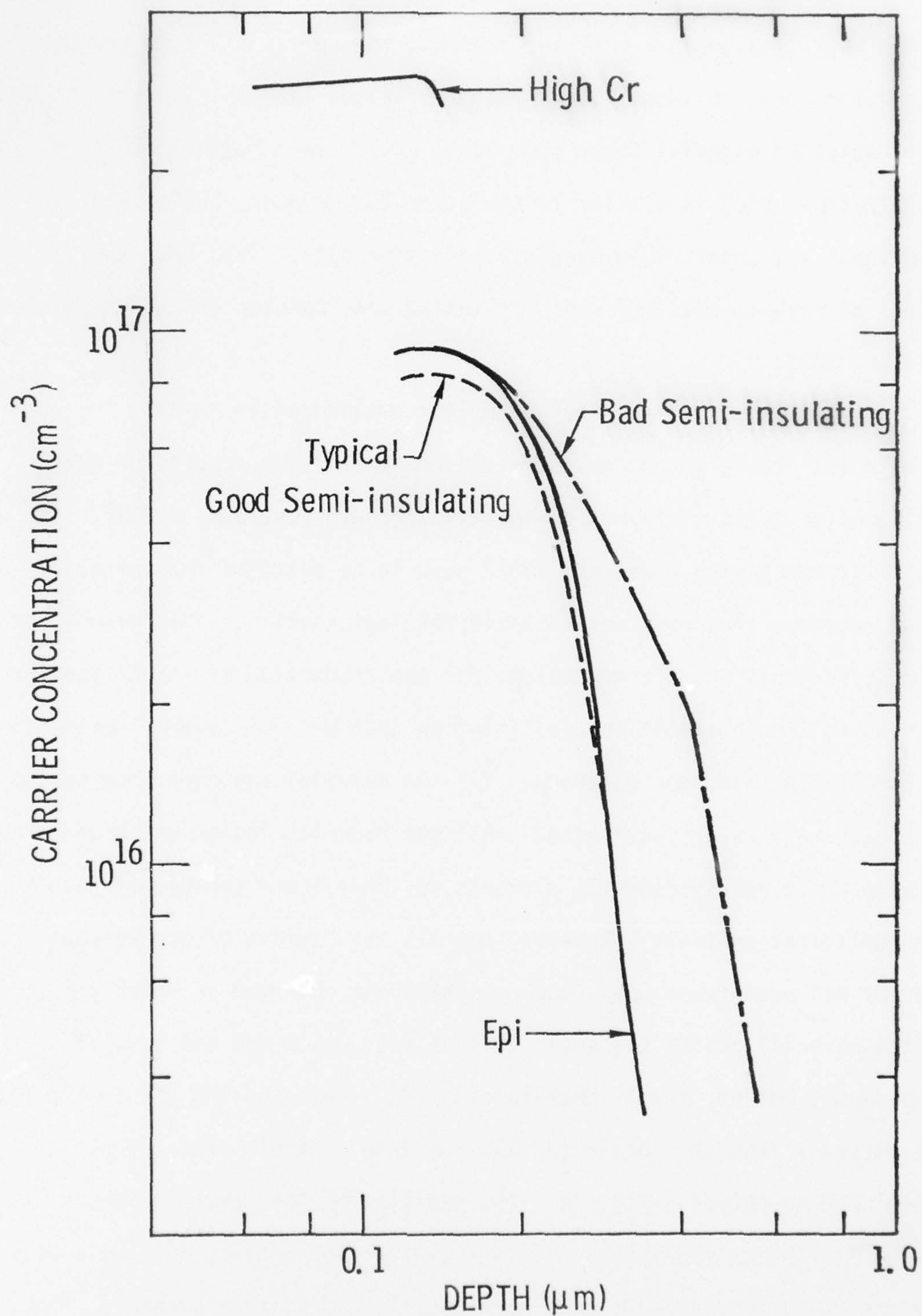


Fig. 53 Electron concentration profiles for various GaAs substrates implanted at 350°C with 1.8×10^{12} 400 keV Si ions/cm^2 and annealed at 850°C for 30 min with a silicon nitride cap.

for implants into good SI material and into the epitaxial layer are seen to be quite close to each other. The profile for the implant into the bad semi-insulating material taken from boule #2312 has a maximum electron concentration which is similar to the other two samples, but it exhibits a prominent and undesirable deeply penetrating tail. This deep tail was typical of results obtained when implanting into samples from "bad" boules #2312 and 2299.

The results of these implant qualification tests for material from a given boule are different from the results of the qualification tests employed for epitaxial growth (see Sec. 3.2.4). In particular substrates #2299 and #2312 seem to be suitable for epitaxial growth, whereas they were not suitable for implantation. The reasons for these differences and the mechanisms for the production of the n-type layer observed in the implantation qualification test are not clear at present. One correlation has been observed. All bad material has been from boules which were regrown or pre-reacted. All the material tested which was from boules grown directly from the elements has been found capable of passing both qualification tests. However, not all the regrown or pre-reacted material has been found bad. One case has been observed in which pre-reacted material passed the qualification test which did not involve ion bombardment, but not the Kr bombardment test. Data for 300 keV Se implants into material from this boule (#2917) and into a sample from a good boule (#2440) are compared in Fig. 54. The profile for the sample from boule 2917 shows a tail which penetrates more deeply than the profile for the sample from the "good" boule 2440. Another special case is that of boule #3183, also pre-reacted, which was found to pass both qualifications tests. The

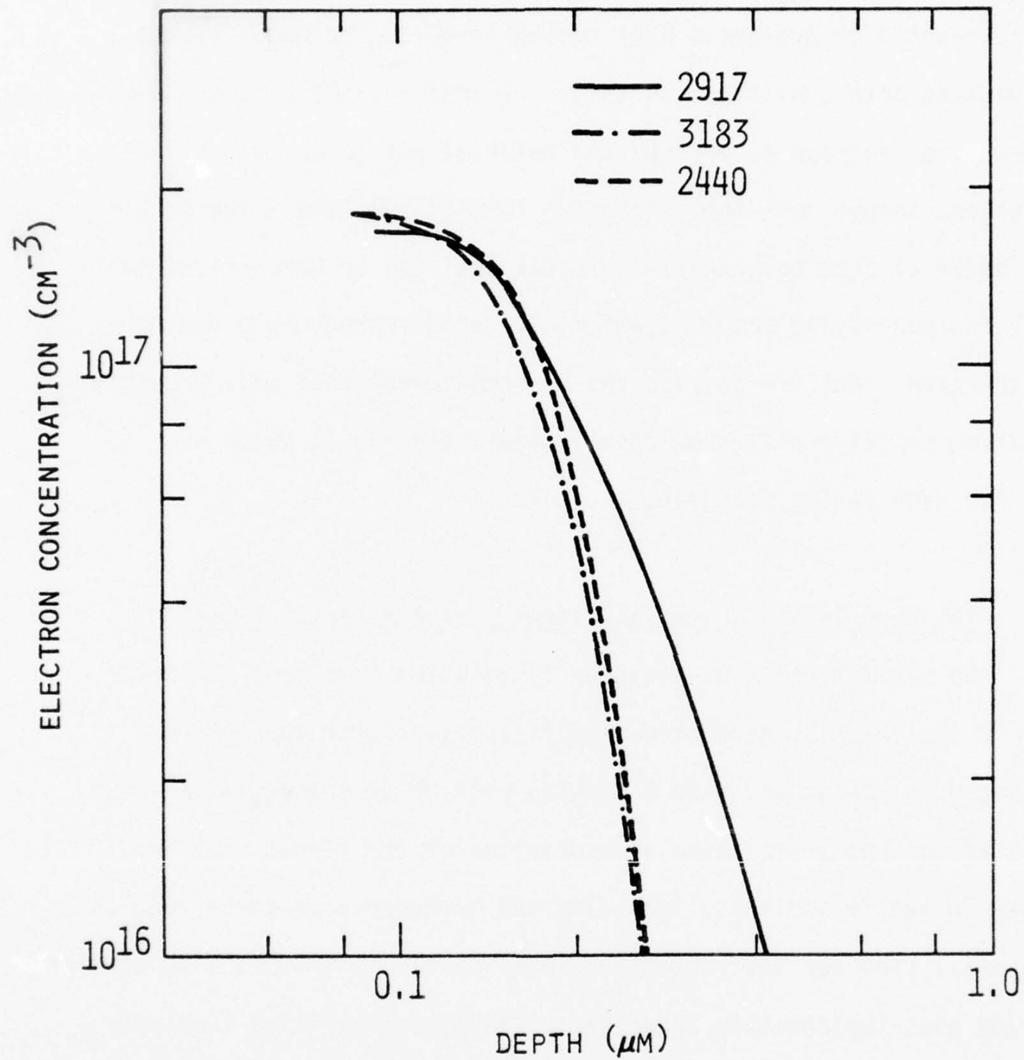


Fig. 54 Comparison of electron concentration profiles for 300 keV Se implants into SI substrate material from three different boules. The performance of these boules in qualification tests is discussed in the text. The dose was $3x10^{12}$ ions/cm^2 for 2917 and 3183 and $3.15x10^{12}$ ions/cm^2 for 2440.

electron concentration profile for a Se implant into this material was found to be very similar to that for the implant into a sample from the "good" boule 2440, as shown in Fig. 54. This is the only case out of 8 boules of pre-reacted or pre-grown GaAs tested in which the material was capable of passing both qualification tests. Therefore, there seems to be a strong tendency for regrown or pre-reacted material not to be suitable for ion implantation, though this does not occur 100% of the time. The results obtained on material from boule 2917 indicates that the Kr bombardment test is essential in identifying material which will show reproducible doping by ion implantation. Failure to pass the Kr bombardment test will probably mean that doping profiles will show deeply penetrating tails which are undesirable for many device purposes.

5.2 High Dose Se and Te Implantation - Science Center & Caltech

The maximum electron concentrations which have been achieved using Se or Te implantation have been significantly greater than those obtained using S implantation. The S results will be described in Sec. 5.3. This section of the report contains a description of the results obtained for high dose Se and Te implants, including the dependence of these results upon the material used for the protective layer or cap to prevent dissociation of GaAs during post-implantation annealing. The semi-insulating substrate material used in this work has passed both the qualification tests discussed in Sec. 5.1. Carrier concentration and mobility profiles are presented for both Te and Se implanted samples annealed under different conditions and implanted with different doses. Data on the dose dependence of the doping efficiency, as a function of anneal temperature for Se implants are presented, and some photoluminescence results obtained from Se and Te implanted samples are discussed.

Implantation substrates used in this work were < 100 > oriented and were obtained from polished semi-insulating GaAs wafers supplied by Crystal Specialties. The polished samples were cleaned in hot acetone and etched in 3:1:1 sulfuric acid: hydrogen peroxide: water for approximately 2 min before implantation. All implantations were carried out at a temperature of 350°C and were usually performed at an energy of 400 keV. Samples were tilted so that the Te beam was incident at about 10° to the < 100 > direction in order to minimize axial channeling, but no particular care was taken with the planar alignment of the samples in most cases.

Post-implantation annealing was carried out in the temperature range between 750 and 900°C with the implanted surface of the sample covered with a silicon nitride or an aluminum oxy-nitride layer to prevent dissociation of the GaAs during annealing or a special capless annealing technique was used. Silicon nitride films about 2500Å thick were deposited by rf reactive sputtering of a silicon target in 100% nitrogen gas at a pressure of about 10^{-2} Torr and at a power density of approximately 3 watts/cm^2. The deposition reate was approximately 100Å/min, and the target to substrate distance was 5 cm. Helium ion backscattering measurements performed on a number of silicon nitride layers deposited in this manner on carbon substrates indicate that the nitride layers were slightly nitrogen rich with a nitrogen to silicon ratio of about 1.5. The oxygen content was usually found to be about 2-3% of the nitrogen content. The density of the layers was determined by using the backscattering data and thickness measurements made by ellipsometry techniques. The results showed densities as high as 3.1 grams/cm^3.

Silicon nitride layers deposited on implanted GaAs samples usually showed good adherence during annealing of the samples to temperatures as high as 950°C.

The aluminum oxy-nitride films were approximately 3000Å thick formed by rf sputtering of an AlN target in argon gas at a pressure of 10^{-2} Torr and a power density of 2.7 watts/cm^2. The gap between target and substrate was 5 cm and the deposition rate was approximately 150Å/min. Helium ion backscattering measurements made on films deposited on carbon substrates showed that the oxygen content of these films was approximately 82% of the nitrogen content. Due to the high oxygen content, we refer to these films as "aluminum oxy-nitride" rather than "aluminum nitride."

A capless annealing technique, developed under our IR&D research program[62] has been applied to the annealing of samples implanted with high Se doses. In this capless annealing process, a thin layer of crushed GaAs is placed in the bottom of a graphite boat followed by a thicker layer of finely pulverized ultra-high purity graphite. After a suitable baking cycle in which the graphite powder is presumably saturated with As, the GaAs slice to be annealed is embedded in the graphite powder and heated to the desired anneal temperature in palladium purified H_2.

After annealing and removing the silicon nitride or aluminum-oxy-nitride layer in HF, if a cap was used, a Van der Pauw pattern was etched into the surface of the sample using standard photoresist techniques. Contacts were made by alloying Au-Ge-Ni dots at a temperature of about 450°C. The deposited contact layer was 12% Ge on Au covered by a thin Ni layer.

Electron concentration and mobility profiles were determined by using an anodization-stripping technique together with sequential Hall coefficient and resistivity measurements. The anodization technique has been developed at an earlier stage of this contract.[63]

The sheet electron concentration for a number of Te or Se implanted samples annealed with either a silicon nitride or an aluminum-oxy-nitride cap is plotted as a function of implanted dose in Fig. 55. It can be seen in this figure that the doping efficiency (ratio of sheet electron concentration to implanted dose) decreases with increasing dose for both Te and Se implants. However, at a given dose and for a given annealing cap, the doping efficiency is lower for Te implants than it is for Se implants. It can also be seen that for samples annealed at 900°C the doping efficiency was higher for both Se and Te implanted samples when an aluminum-oxy-nitride cap was used than it was when a silicon nitride cap was used. The contrast in results using silicon nitride or aluminum-oxy-nitride caps is also illustrated in Figs. 56 and 57 which show electron concentration and mobility profile data for samples implanted with $1x10^{14}$ Te or Se ions/cm^2 and annealed using one of these two materials for the cap. In both cases, the maximum electron concentration was higher when an aluminum-oxy-nitride cap was used. For a given cap, the Se implanted samples exhibited a higher peak electron concentration than did the Te implanted samples. The electron mobility for both Te and the Se implanted samples was higher when the annealing was carried out with an aluminum-oxy-nitride cap than when it was carried out using a silicon nitride cap.

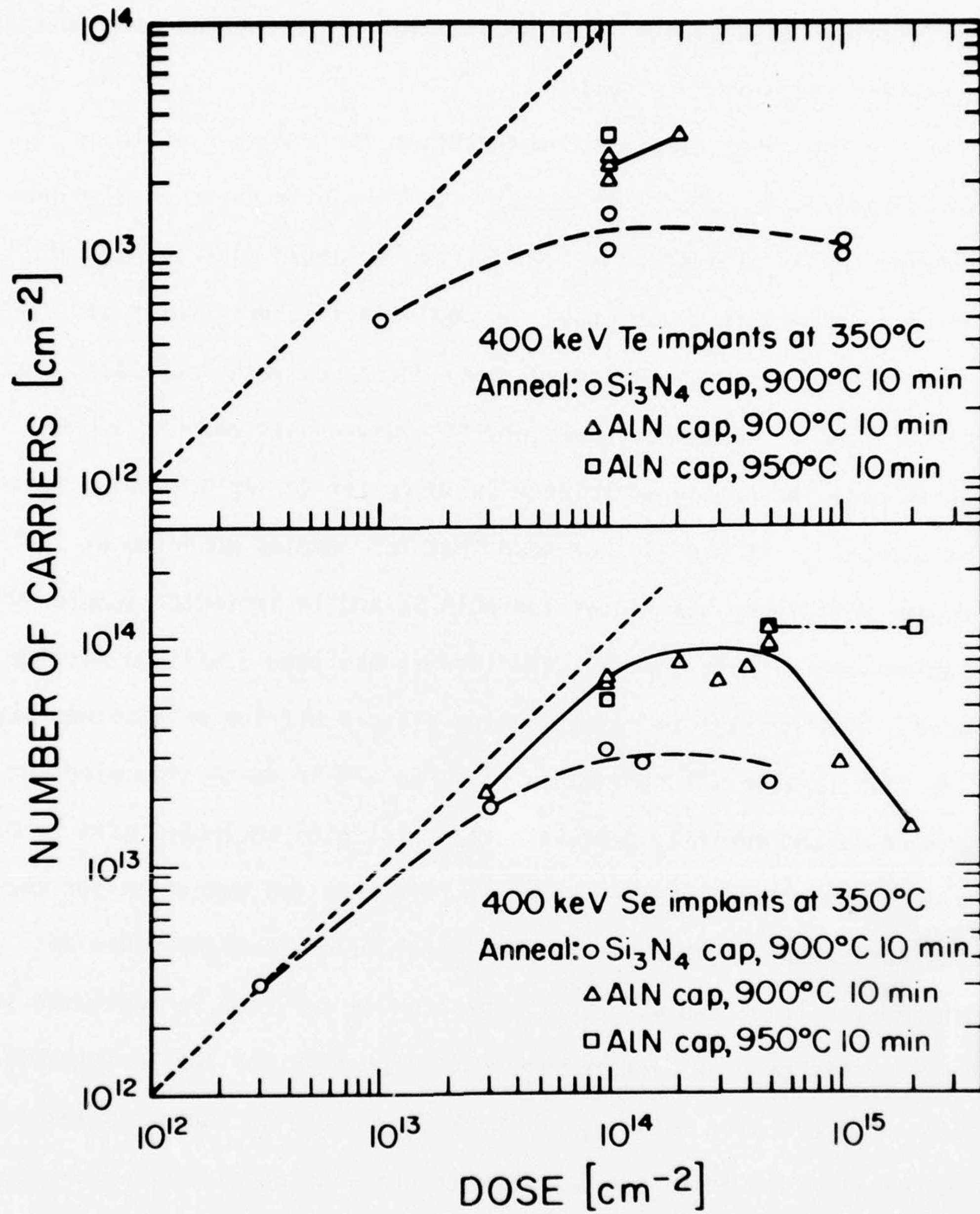


Fig. 55 Sheet electron concentration vs. implanted dose for 400 keV Se and Te implants carried out at 350°C. Annealing conditions for the various samples are indicated on the figure.

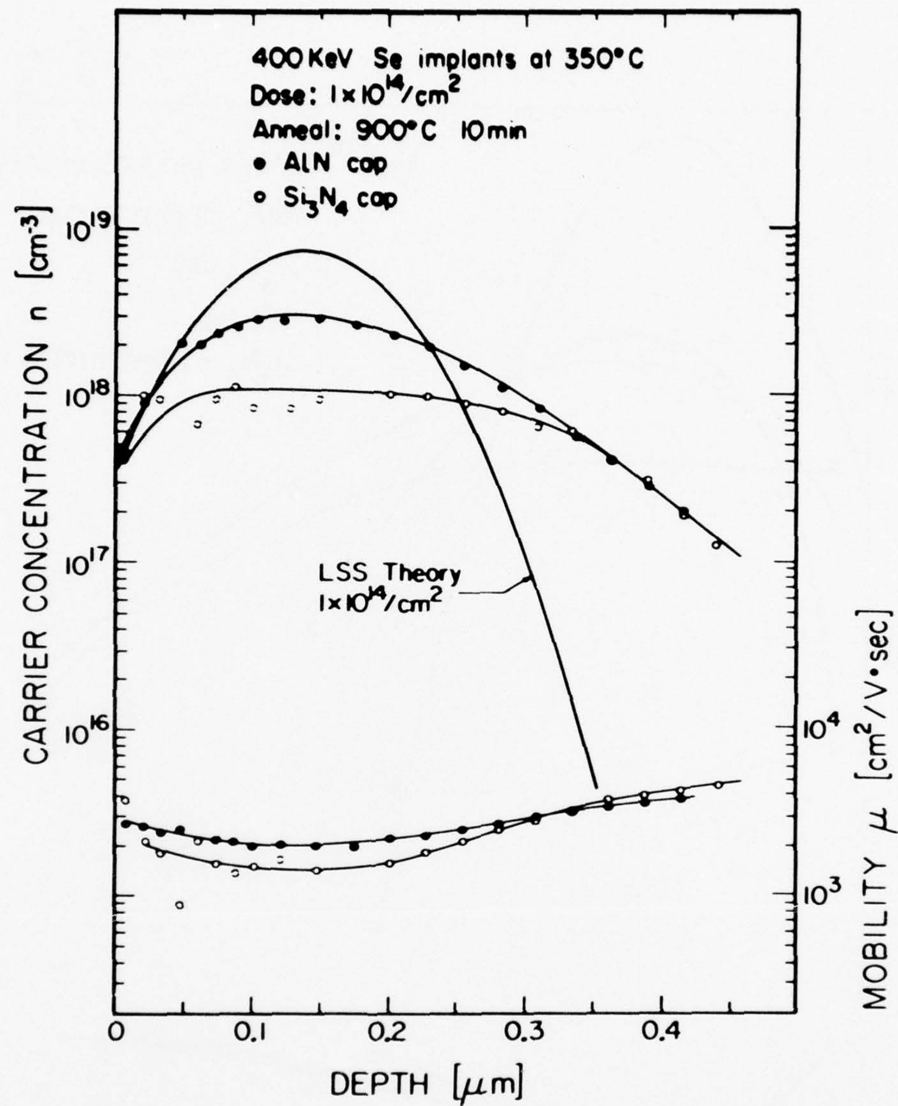


Fig. 56 Electron concentration and mobility profiles for semi-insulating GaAs samples implanted with 400 keV Se ions at 350°C to a dose of $1\times10^{14}cm^2$. Annealing was carried out at 900°C for 10 minutes with the annealing cap indicated on the figure.

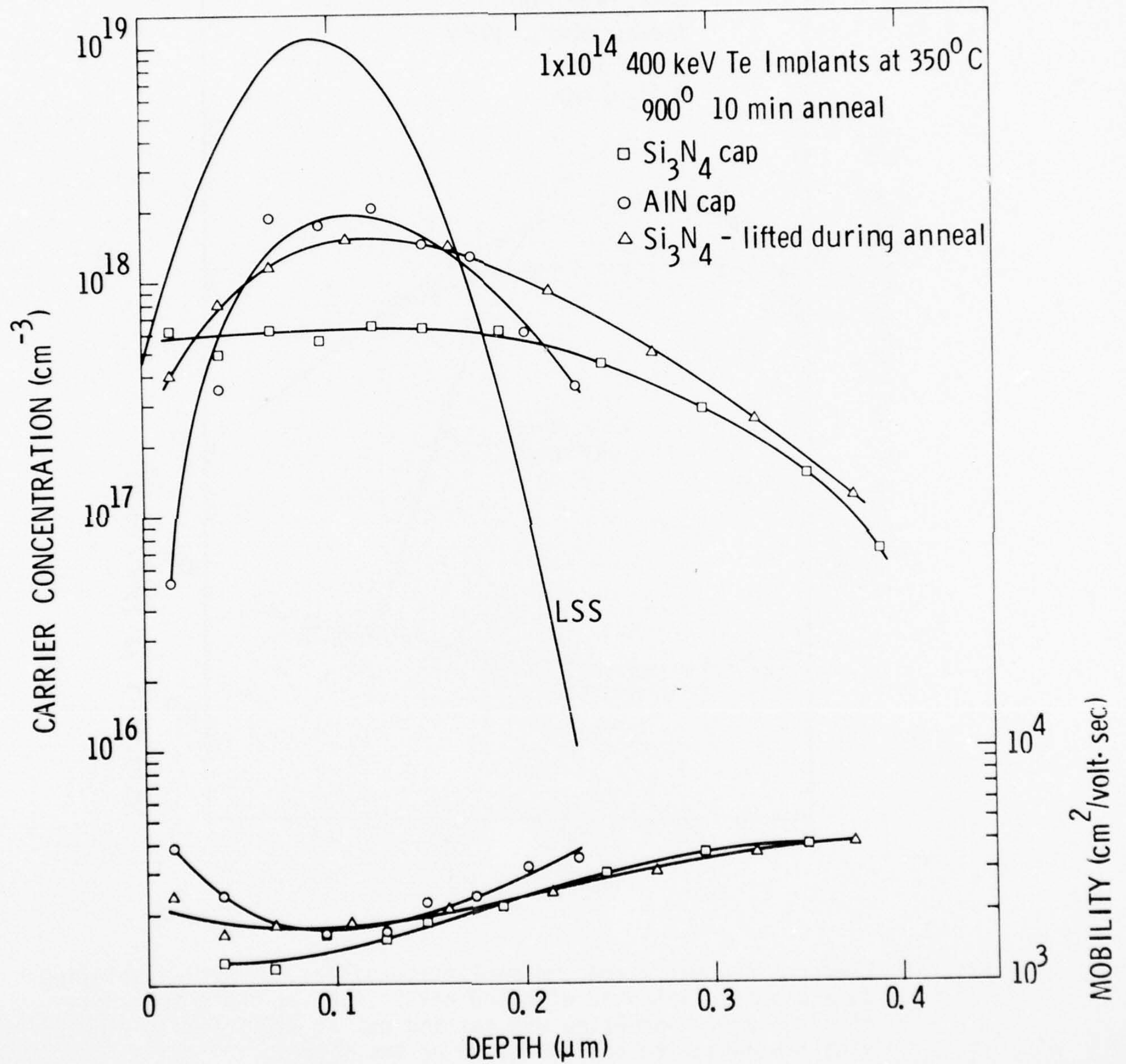


Fig. 57 Carrier concentration and mobility profiles for Te implanted samples annealed with different caps.

Electron concentration and mobility profiles for samples which were implanted with different doses of 400 keV Se ions and were annealed at 900°C using an aluminum-oxy-nitride cap are shown in Fig. 58(a). The doping extends to depths which are somewhat greater than the profile for the implanted Se predicted from LSS range parameters.[64] This is probably due to diffusion of the implanted Se during post-implantation annealing. For doses between 3×10^{13} and 5×10^{14} ions/cm^2, the profile exhibits a peak near the projected range of the implanted Se (1370Å) and the maximum electron concentration rises with the increasing Se dose. For these doses the electron mobility at depths beyond the peak doping closely approaches the values of Sze and Irvin[65] for uncompensated GaAs, as shown in Fig. 58(b). Near the surface the mobility is lower for a given electron concentration than it is at depths beyond the peak. This is the region which was most heavily damaged during implantation. These data suggest that there are defects remaining in this heavily damaged region, but at greater depths the GaAs is almost uncompensated. For the two higher doses of 1×10^{15} and 2×10^{15} ions/cm^2, the peak in the electron concentration occurs at a depth considerably beyond the projected range of the implanted Se. The electron concentration in the vicinity of 1370Å is appreciably below that for any of the other doses for which data are shown. This may be due to the presence of damage which was not removed by the 900°C anneal. The data in Fig. 58(b) for a dose of 2×10^{15} ions/cm^2 also suggest the presence of defects, since the mobility at a given electron concentration is appreciably lower than for the lower dose implants.

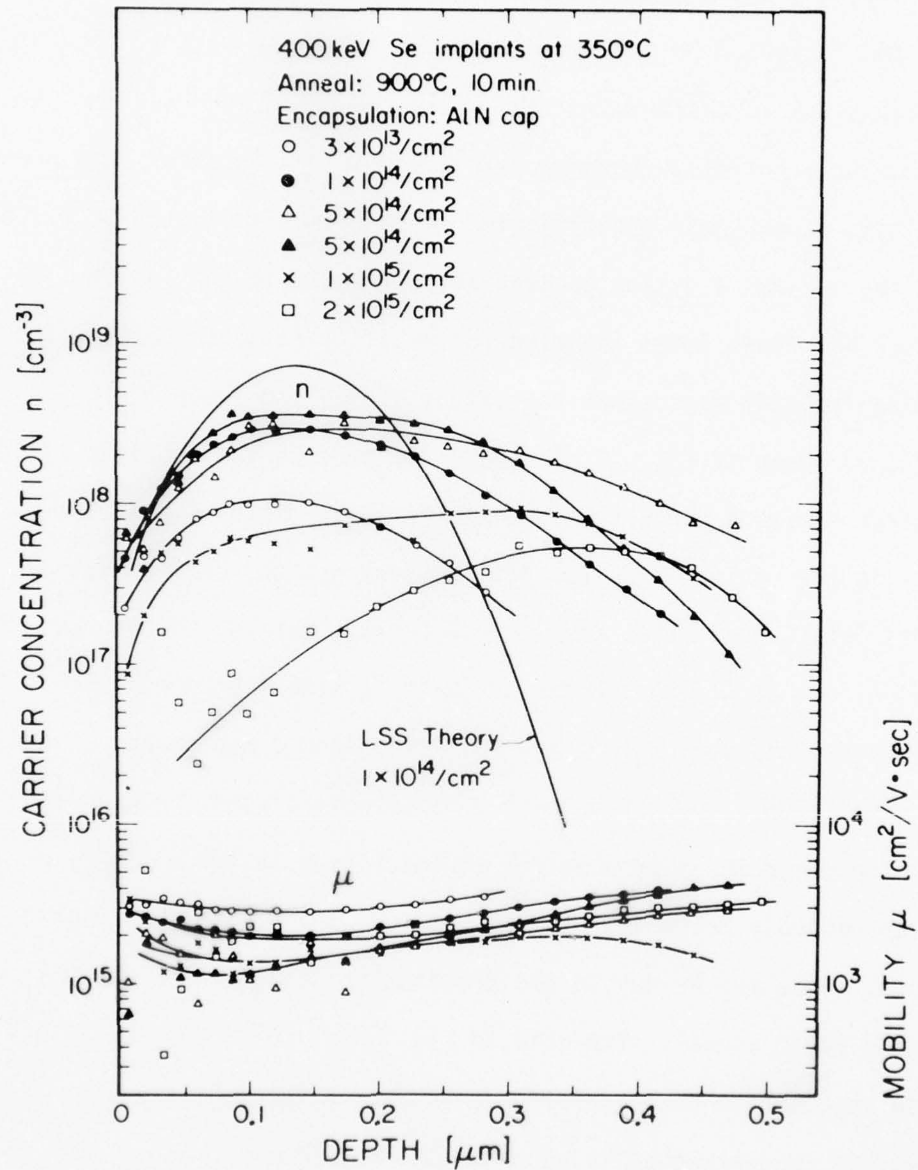


Fig. 58a Electron concentration and mobility profiles for semi-insulating GaAs samples implanted with 400 keV se ions at 350°C to the doses indicated on the figure. Annealing was carried out at 900°C for 10 minutes using an aluminum oxy-nitride cap.

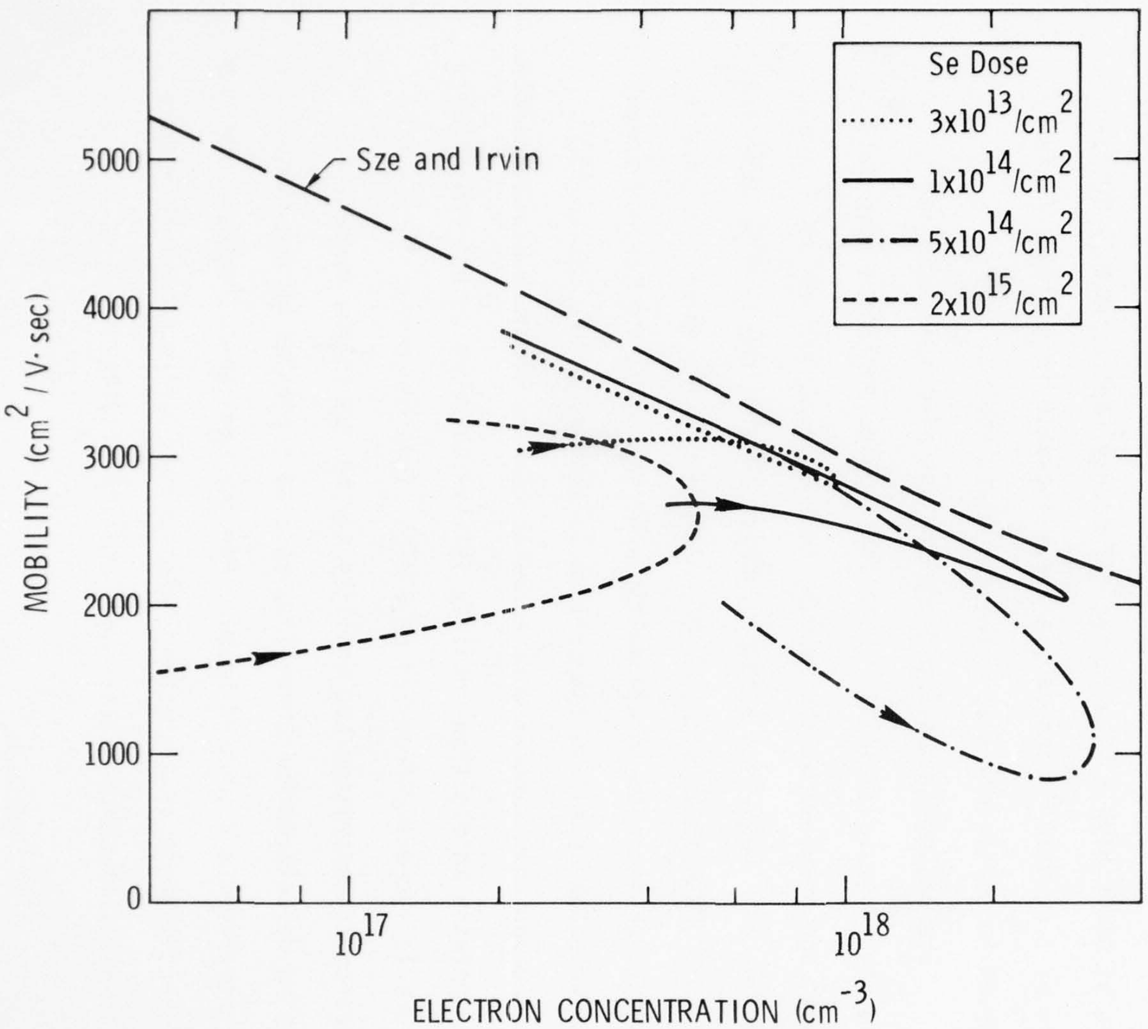


Fig. 58b Electron mobility vs electron concentration for some of the samples of Fig. 58a. Data points are omitted for clarity. The arrows show the direction of increasing dept. The curve labeled "Sze and Irvin" shows the data on mobility vs impurity characterization of Ref. 65.

Annealing samples implanted with doses of $2x10^{15}$ ions/cm^2 to 950°C results in a significant increase in the doping as can be seen in Fig. 59 which shows the doping efficiency plotted as a function of annealing temperature for various doses of Se ions. The data show that as the dose increases, a higher annealing temperature is required to achieve the maximum observed doping efficiency. For a dose of $3x10^{13}$ ions/cm^2, annealing at 850°C give a high doping efficiency (approximately 60%). For doses of 1 or $5x10^{14}$ ions/cm^2, a large increase in doping efficiency was observed in the anneal step between 850 and 900°C.

The capless annealing technique has also been used for annealing high dose Se implants. Data for samples implanted with $2x10^{14}$ Se ions/cm^2 and annealed by the capless technique at 850° or 900°C are shown in Fig. 60. Data from a sample implanted with the same Se dose and annealed at 900°C with an aluminum-oxy-nitride cap are shown for comparison. There is a large increase in the doping achieved using the capless anneal technique when the annealing temperature is increased from 850 to 900°C just as occurred when samples were annealed with an aluminum-oxy-nitride cap. An increase in electron mobility is also observed as the annealing temperature is increased from 850 to 900°C. This concurrent increase in both electron concentration and mobility may be due to the removal of compensating defects during annealing, as also suggested by the photoluminescense results discussed below. For the same anneal temperature, the two different methods of protecting GaAs surface during annealing result in similar electron concentration and mobility profiles.

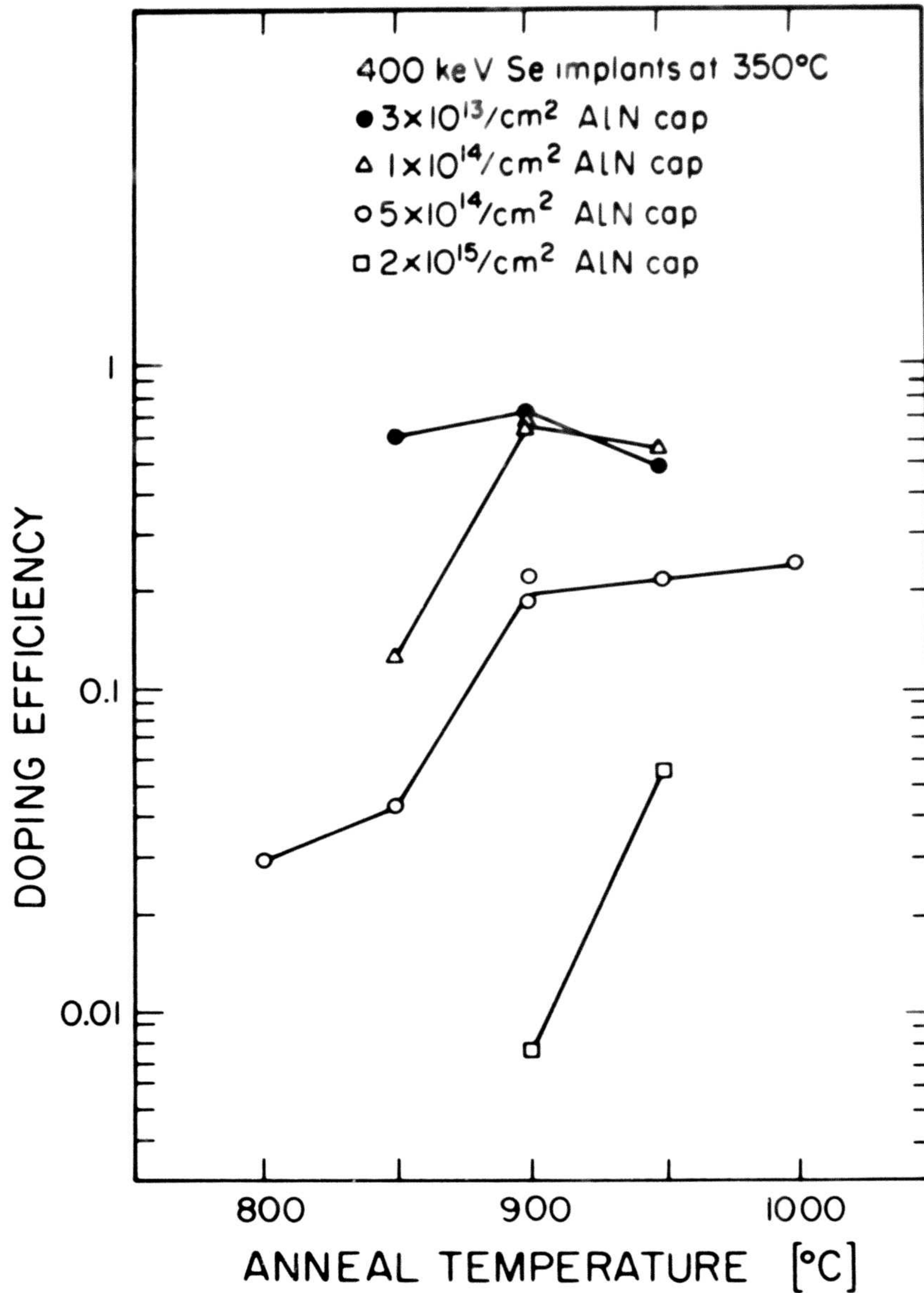


Fig. 59 Doping efficiency vs. annealing temperature for semi-insulating GaAs samples implanted at 350°C with 400 keV ions to the doses indicated on the figure. Annealing was carried out using an aluminum oxy-nitride cap.

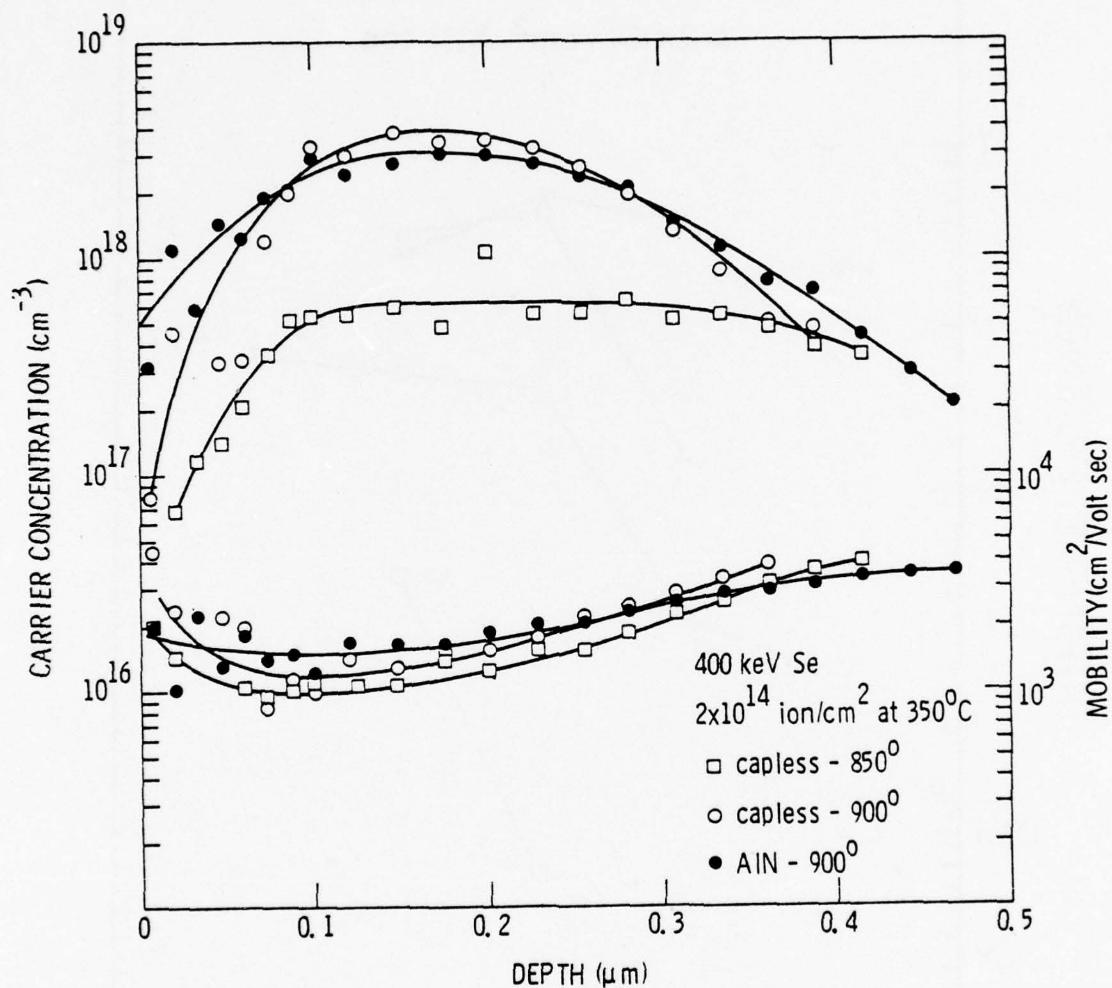


Fig. 60 Carrier concentration and mobility profiles for Se implanted samples annealed by the capless technique or with an aluminum-oxy-nitride (labeled AIN) cap.

Photoluminescence data for Se implanted samples shown in Fig. 61 indicate that the large increase in doping efficiency observed in samples implanted with about 10^{14} Se ions/cm^2 and annealed either with an aluminum-oxy-nitride cap or by the capless technique is due to the removal of Ga vacancy-Se complexes when the annealing is carried out at the higher temperature. The luminescence peak at the wavelength of 1μm, shown in this figure for the samples annealed at 850°C, is believed to be due to such complexes.[66] The intensity of this peak is greatly decreased following the 900°C anneal and a new peak located at about 0.89μm appears in the spectrum. Similar photoluminescence spectra are observed when the sample is annealed using the capless technique. However, when a silicon nitride cap is used, a luminescence peak is still observed at 1μm following a 900°C anneal and no peak is observed at 0.89μm. The dependence of the sheet electron concentration and the intensity of t[illegible] and 0.89μm luminescence peaks on anneal temperature is shown in Fig. 62 for several different combinations of implantation dose and annealing cap. In all the cases, the intensity in the 1μm region is observed to decrease with increasing anneal temperature. The anneal temperature at which the 0.89μm peak is first observed in samples annealed with an aluminum-oxy-nitride cap is a function of the implantation dose. A higher anneal temperature is required as the implantation dose in increased. The relationship between the appearance of 0.89μm luminescence peak and the activation of high doses of implanted n-type dopants is not clear at present. Experiments in which samples were annealed under low or high As pressure suggested that this luminescence peak might be associated with the introduction of As vacancies into the GaAs. However, evidence is presented in Sec. 3.2.4 of this report which indicates that this

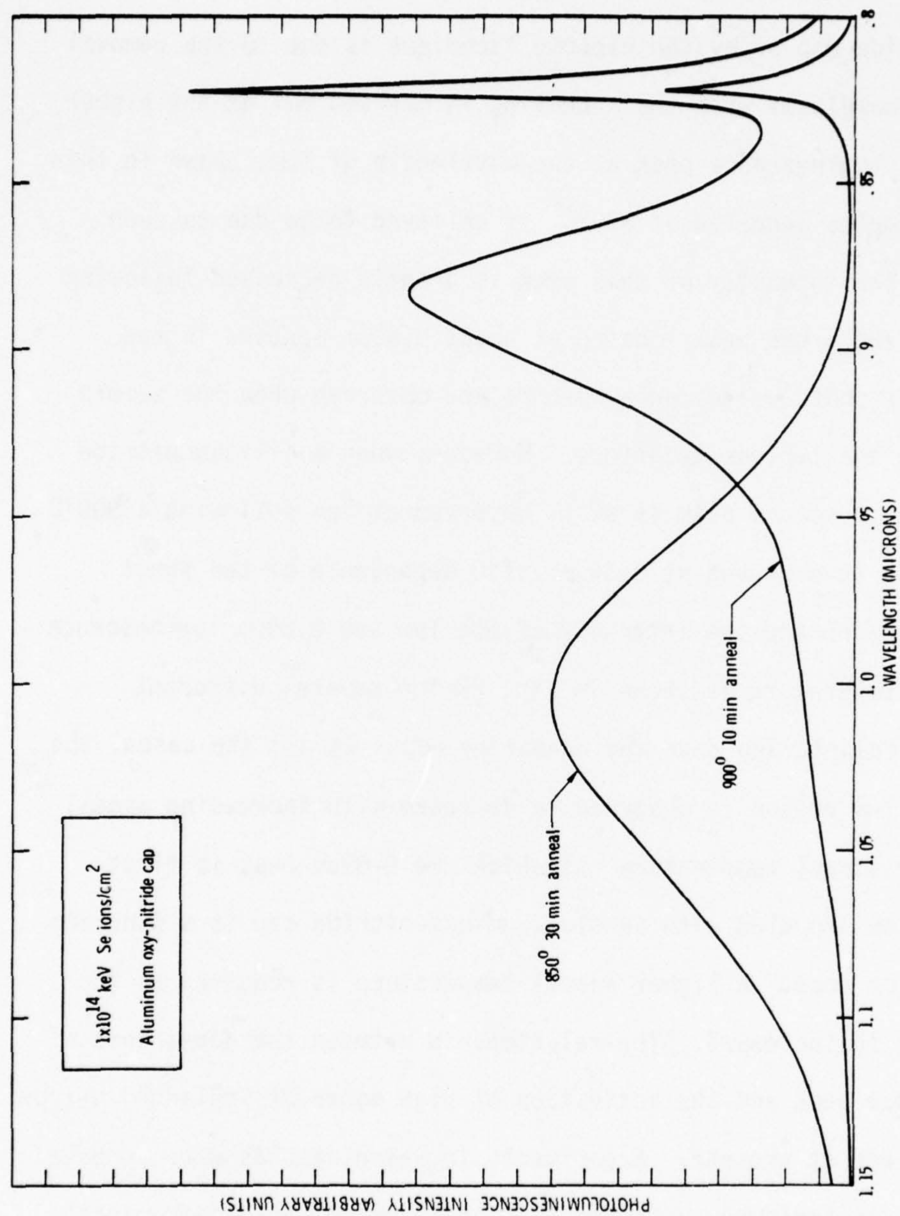


Fig. 61 Photoluminescnece spectra from SI GaAs samples implanted with 400 keV Se ions at 350°C to a dose of 1x10^{12}cm^2. Annealing was carried out using an aluminum oxy-nitride cap at the temperatures and for the times indicated on the figure.

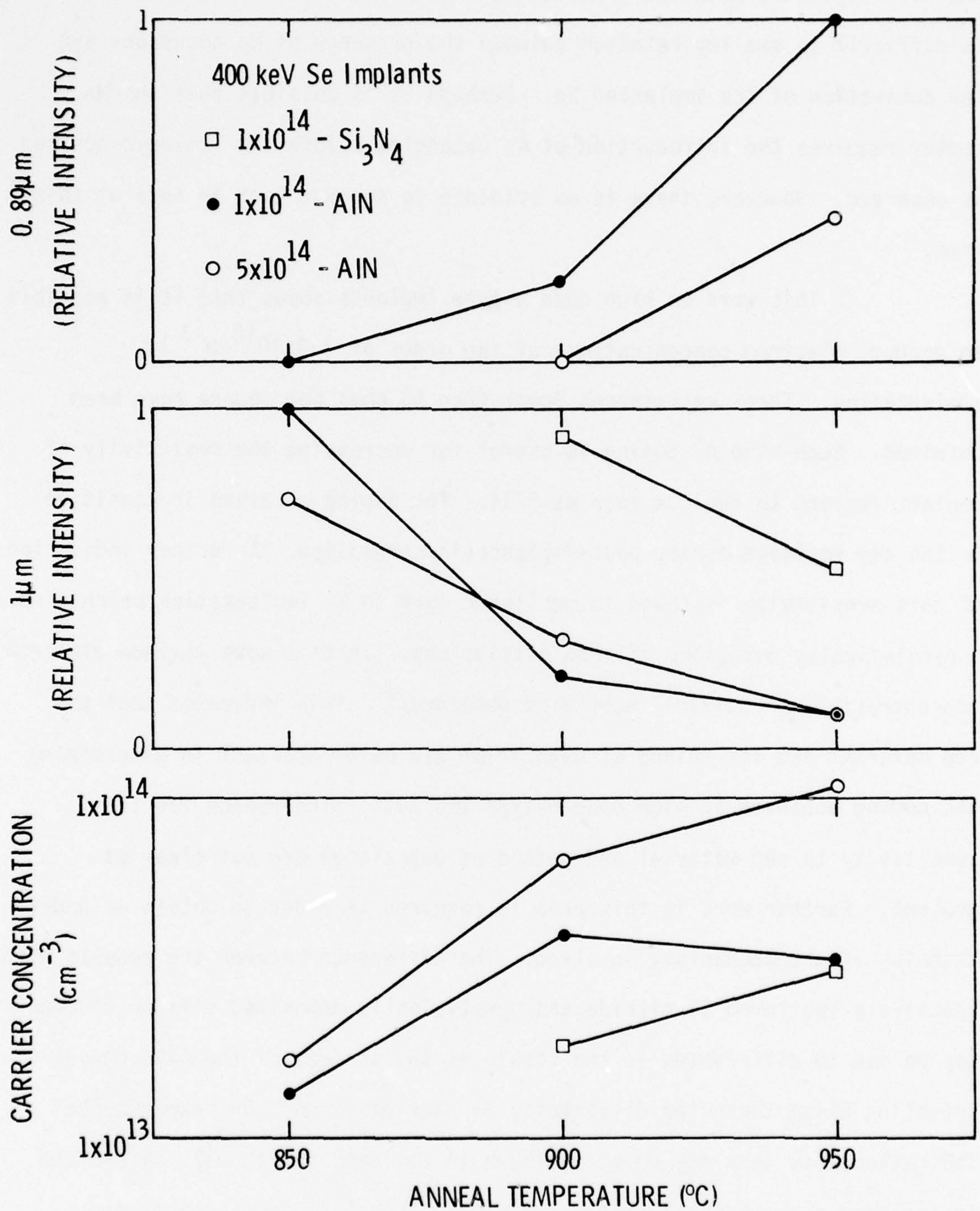


Fig. 62 Sheet electron concentration, and photoluminescence intensity of the 1μm and 0.89μm peaks of Se-implanted samples vs anneal temperature. The Se doses and the anneal caps used are indicated on the figure.

peak is associated with the presence of Mn acceptors in the material. It is difficult to see any relation between the presence of Mn acceptors and the activation of the implanted Se. Perhaps it is possible that the Mn center requires the introduction of As vacancies before the luminescence can be observed. However, there is no evidence to support such an idea at this time.

This work on high dose n-type implants shows that it is possible to produce electron concentrations of the order of $1\text{-}4\times10^{18}\,cm^{-3}$ by implantation. Sheet resistances lower than 50 ohms per square have been obtained. Such high n^+ doping is useful for decreasing the resistivity of contact regions to devices such as FETs. The doping obtained is sensitive to the cap employed during post-implantation annealing. A further indication of this sensitivity is found in published work on Se implantation which used a pyrolytically deposited silicon nitride cap. In this work maximum electron concentrations of 3.4×10^{18} were also obtained.[67] This indicates that the cap material and its method of deposition are both important in determining the doping achieved in high dose n-type implants. The reason for this sensitivity to cap material and method of deposition are not clear at present. Further work in this area is required in order to obtain an understanding of the mechanisms involved. The difference between the results with reactively sputtered Si nitride and pyrolytically deposited silicon nitride may be due to differences in the strain at the surface of the GaAs during annealing using these two differently Si nitride films. One experimental indication that this may be so is shown in the data of Fig. 57. A profile is included there for a Te implanted sample annealed with a reactively sputtered silicon nitride cap which lifted during the annealing process.

However, the cap did not rupture and still afforded some protection of the GaAs surface during annealing although any strain effects which might have been present with a cap that adhered were eliminated. The maximum electron concentration achieved with this sample was greater than that measured for samples for which the cap adhered completely during annealing.

Another area which is not well understood at present has to do with the maximum electron concentration that it has been possible to reproducibly obtain using high dose n-type implants. The maximum measured electron concentration was about 40-54% of the maximum predicted Se concentration ($\sim 7x10^{18}cm^{-3}$) achieved in bulk grown GaAs crystals in which the Se concentration is equal to $7x10^{18}cm^{-3}$. However, as the implantation dose is increased, the maximum electron concentration does not rise significantly above the level achieved with the dose of $1x10^{14}$ ions/cm^2 even though maximum doping levels near $1x10^{19}/cm^3$ have been achieved in bulk doped crystals.[68] The reasons for this limitation of the doping level are not clear at present. Te implantation work into high purity epitaxial layers and into semi-insulating substrates from different suppliers indicate that for high dose implants the substrate does not have a significant effect upon the doping level obtained. It is likely that the results for high dose Se implants would exhibit a similar independence of substrate effects. Experiments have been carried out utilizing Ga implantation in addition to Te implantation of a dopant that is expected to reside on the As sublattice. No significant effects of Ga implantation were observed in our work. However, there is one case in the literature where it is claimed that Ga implantation has produced a significant increase

in the doping level.[69] Perhaps further investigation of the effects of Ga implantation in addition to implantation of an n-type dopant would be worthwhile.

5.3 Sulphur Implantation - Science Center and Caltech

The doping profile measured in S implanted samples annealed with a sputtered silicon nitride cap are considerably deeper than the distribution for the implanted S calculated from LSS range parameters. This is illustrated in Fig. 63, which shows the electron concentration profile for a sample implanted with 100 keV S ions to a dose of $9 \times 10^{12} cm^2$. The maximum electron concentration is about an order of magnitude lower than the expected peak S concentration and the doping efficiency is of the order of 20%. The results of S tracer diffusion measurements carried out under IR&D support [70] indicate that the deep penetration of the dopant is due to S diffusion during post-implantation annealing and that the low doping efficiency is a result of a substantial out-diffusion of the implanted S from the sample. The reproducibility of doping profiles from low dose 100 keV S implants was found to be as good as the reproducibility of low dose Se implantation profiles. The doping over a given wafer has also been found to be quite uniform. Figure 64 shows the distribution in the maximum electron concentration and in the depth at which the electron concentration reaches 10% of this maximum, obtained by measuring a large number of Schottky barriers over a single S implanted wafer. Nearly all the values of n_{max} are contained within a range of $\pm$ 5% on either side of the average value. The spread in the depth (10% of n_{max}) is equally narrow. This

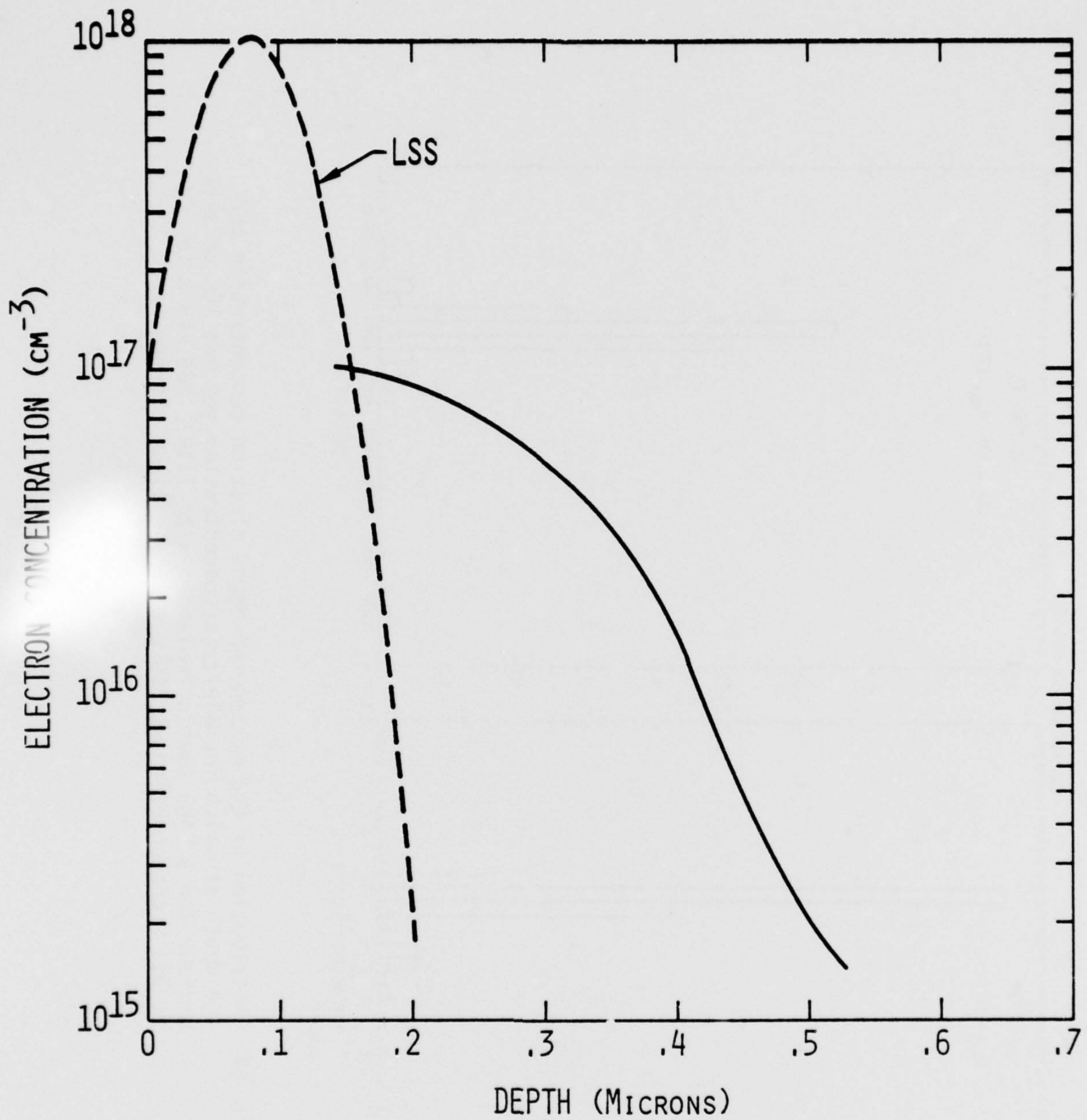


Fig. 63 Electron concentration profile for a GaAs sample implanted with 9×10^{12} 100-keV S ions/cm^2 at 350°C and annealed at 850°C with a silicon nitride cap, compared with the S distribution calculated from LSS range parameters.

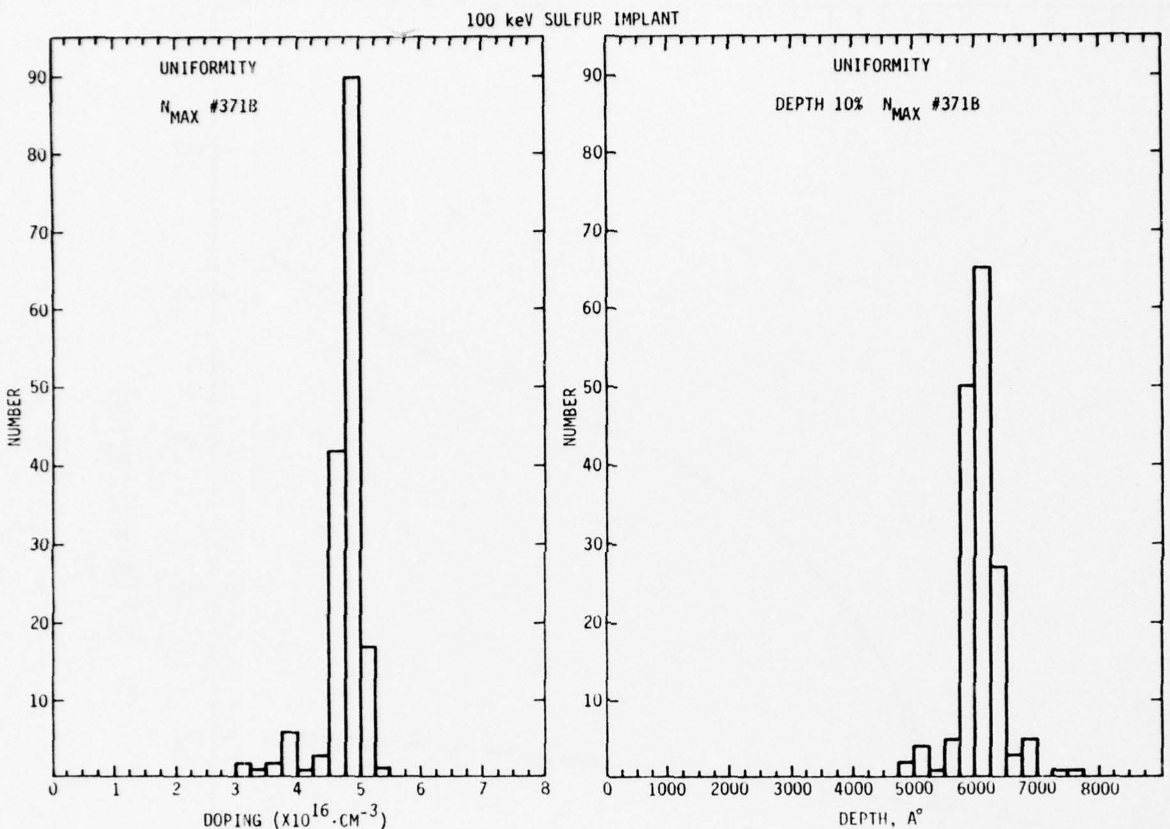


Fig. 64 Distribution of the maximum observed electron concentration and the depth at which the electron concentration reached 10% of this maximum for a GaAs sample implanted with 7×10^{12} 100 keV S ions/cm^2 at 350°C and annealed at 850°C with a silicon nitride cap.

uniformity in doping profiles correlates well with observed uniformity in the characteristics of FETs fabricated in S implanted layers.

The implantation of S at energies higher than 100 keV has also been investigated. Figure 65 shows electron concentration profiles obtained using a layer removal and sequential Hall coefficient and resistivity measurement technique on S samples implanted with 400 keV S ions.[63] Data are shown for doses of $3x10^{13}$ ions/cm^2 and $1x10^{14}$ ions/cm^2 and for implants carried out at room temperature and at 300°C. The profiles for the samples implanted with $3x10^{13}$ ions/cm^2 seem not to be dependent upon implantation temperature. However, for a dose of $1x10^{14}$ ions/cm^2, there is a substantial difference between the profiles for the sample implanted at room temperature and the sample implanted at 350°C. This difference probably occurs because at higher implantation dose, an amorphous layer is produced during room temperature implantation. The doping efficiencies for the samples implanted at 350°C were 44% for the dose of $3x10^{13}$cm^2 and 38% for the dose of $1x10^{14}$cm^2. This is significantly greater than the doping efficiency observed for even lower doses when the implantation was performed at an energy of 100 keV. We believe this is the consequence of the out-diffusion which occurs during the annealing of S implanted samples. The increase in doping efficiency with increased implantation energy would be expected to occur, because at the higher implant energy, the S is initially distributed more deeply in the sample so that the probability of out-diffusion is significantly reduced.

Channeling effect measurements have been carried out on S implanted samples in an effort to determine the lattice location of the implanted S. The experiments have been performed using a 400 keV proton

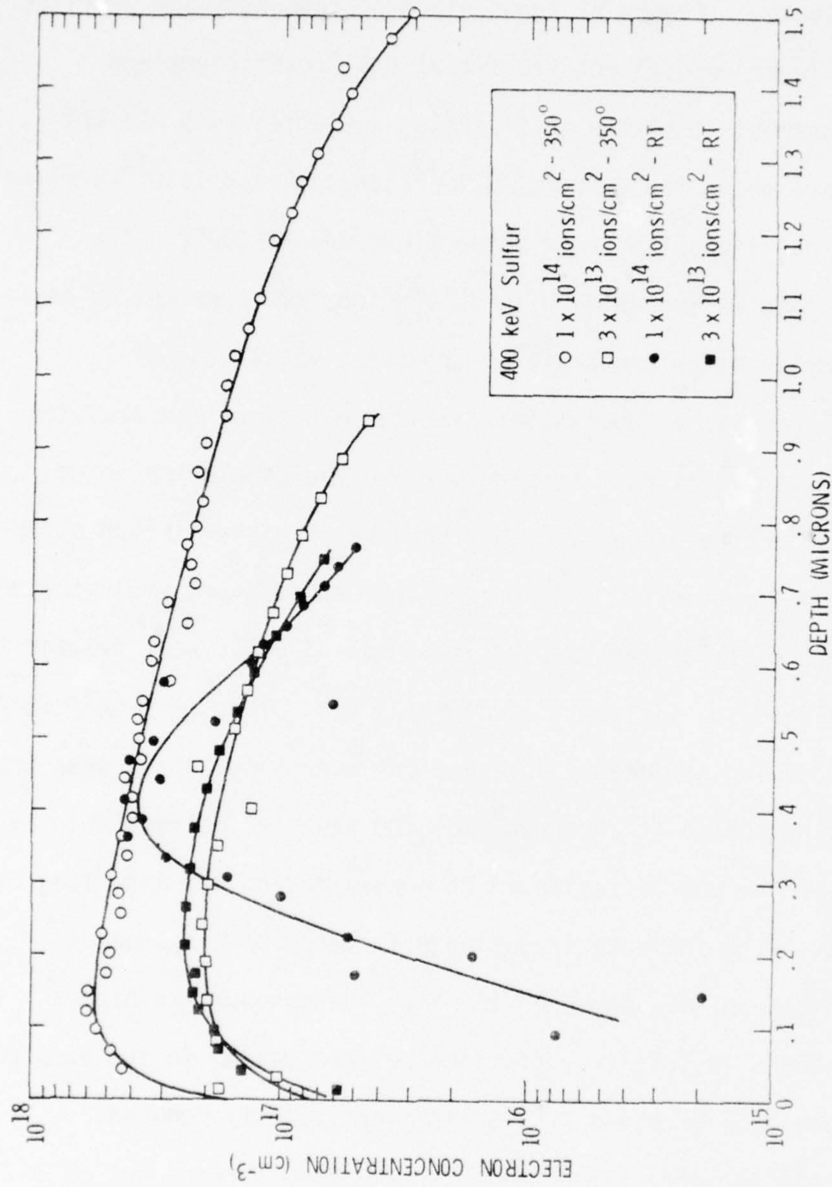


Fig. 65 Electron concentration profiles for GaAs samples implanted with the indicated doses of 400 keV S ions at the indicated temperatures and annealed at 850°C with a silicon nitride cap

beam. Measurements of the energy spectrum of the proton induced x-rays were carried out using a Li drifted Si x-ray detector. The interaction of channeled protons with implanted S atoms could be measured by determining the intensity of the x-ray yield. Measurements have been carried out on samples after implantation at 350°C in order to determine whether or not a substantial fraction of the implanted S might be in interstitial positions. If this were the case, it might help account for the large S diffusion observed in implanted GaAs.

A typical x-ray spectrum obtained from a GaAs sample implanted with $1x10^{15}$ 100 keV S ions/cm^2 is shown in Fig. 66. The analysis was done with a 400 keV proton beam incident in a random direction. X-ray peaks due to As, Si on the sample surface and implanted S are seen. A 2 mil thick mylar absorber was used over the end window of the x-ray detector. This results in a very large attenuation of the Ga and As L x-rays relative to the sulphur K x-ray. This procedure is necessary in order to avoid pile-up effects which would obscure the sulphur x-ray peak. The sulphur x-ray peak is superimposed on a very broad background. This background is thought to be due to Bremstrahlung generated by knock-on electrons originating from bound states of the Ga and As atoms.[71] In order to determine the intensity of the S x-ray yield, it was necessary to subtract this background. This was accomplished with the aid of spectra obtained from unimplanted GaAs samples with similar orientations of the sample relative to the incident proton beam.

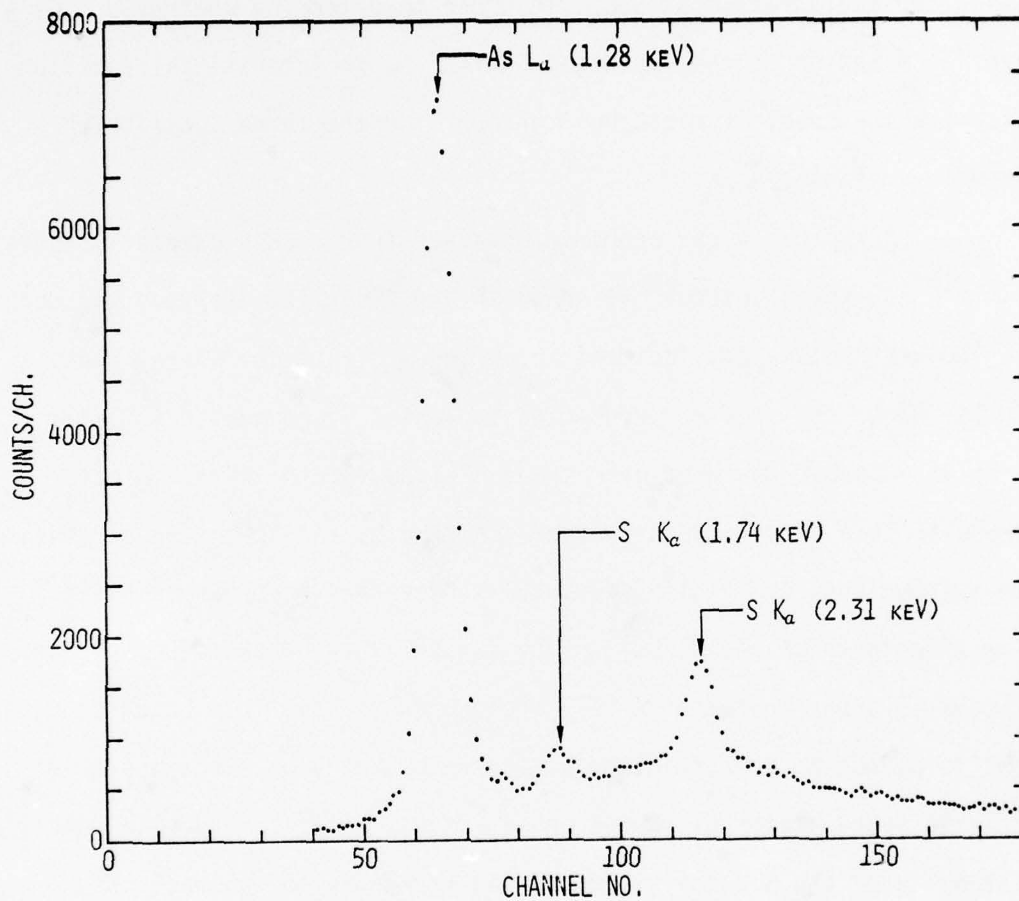
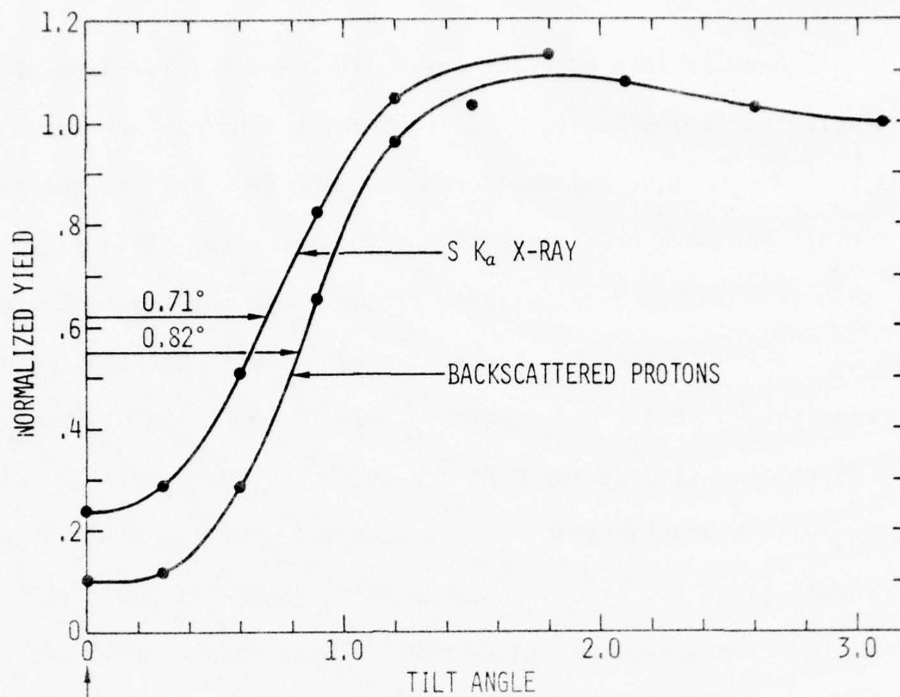


Fig. 66 X-ray spectrum obtained from a GaAs sample implanted with 1×10^{15} 100 keV S ions/cm^2 at 350°C using a 400 keV proton beam incident in a random direction

Angular scan data for the < 110 > and < 111 > axes of a sample implanted at 350°C with $1x10^{15}$ 100 keV S ions/cm^2 are shown in Fig. 67 both for protons backscattered from the GaAs and for the sulphur x-ray yield. For both axes, the minimum sulphur x-ray yield is somewhat higher than the minimum backscattered proton yield and the half width of the dip in S yield is smaller than that of the dip in backscattered proton yield. Analysis of these data indicate that the fraction of S ions lying along a given axis is 0.85 and 0.81 for the < 110 > and < 111 > axis, respectively. An angular scan has not been made for the < 100 > axis. However, data taken for exact incidence along that axis indicate the 0.88 of the S atoms lie along the <100> rows. These results indicate that the implanted S is highly substitutional following implantation at 350°C. There could be some interstitial component of the implanted S. However, the existing data can be interpreted as indicating that the S is almost entirely substitutional, and that the small deviations in half width of the back-scattered and x-ray dips is due to a small amount of strain in the GaAs lattice. The minimum proton backscattered yield in < 110 > and < 111 > directions is somewhat higher than that expected from a good GaAs crystal which is consistent with the possibility of a strained GaAs lattice. It is probably not possible to reach any more definitive conclusion about the possibility of a substantial interstitial S component following implantation by the use of channeling effect lattice locations techniques.



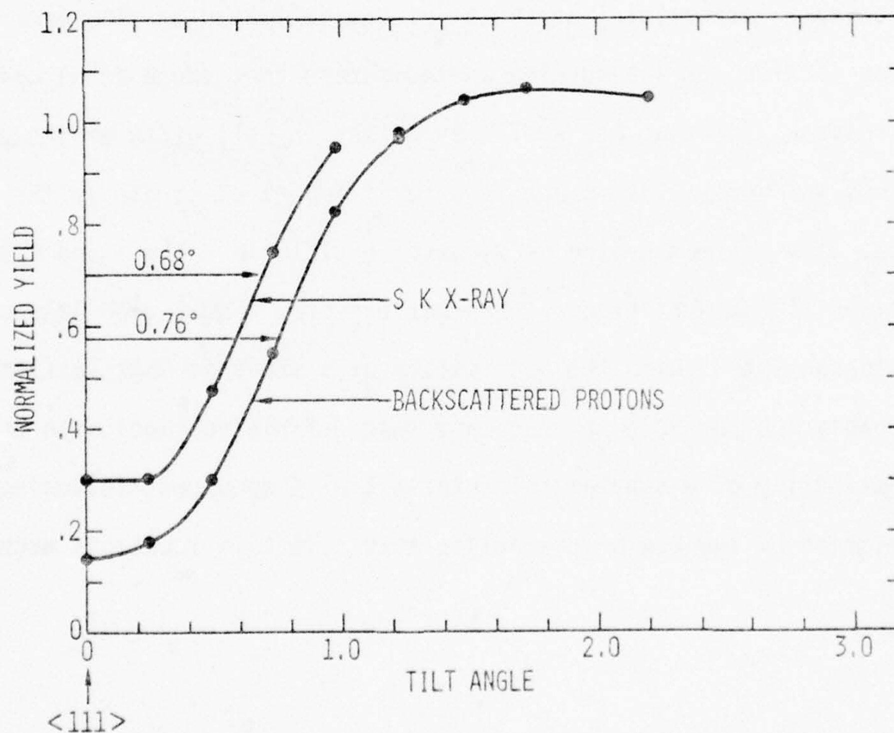


Fig. 67 Normalized S K X-ray and backscattered proton yield vs tilt angle for the <110> and <111> axes of a GaAs sample implanted with 1×10^{15} 100 keV S ions/cm^2 at 350°C, using a 400 keV proton beam for the analysis

5.4 Reordering of Implanted Amorphous GaAs - Science Center and Caltech

There is a significant difference between GaAs and Si in the electrical behavior of implanted amorphous regions. In Si, high electrical activity is found after annealing in the temperature range where the amorphous layer reorders.[72] Significantly higher anneal temperatures are required to achieve high electrical activity in hot substrate implantation process as compared to room temperature implantation where an amorphous layer is formed. Almost the reverse is true for high dose implantation in GaAs. Hot substrate implantation is required to achieve high electrical activity.[73] In low temperature implantation where an amorphous layer is formed, much lower electrical activity is found at the same anneal temperatures as those used for hot substrate implantations.

These results suggest that there is a major difference between the anneal behavior of amorphous layers of Si and that of GaAs. The purpose of the present work was to investigate the reordering of implanted amorphous layers on GaAs following the precautions observed in studies of Si.[74] Amorphous layers were formed by implantation at LN_2 temperatures, minimizing the recovery of damage during implantation. This use of implantation at LN_2 temperature therefore made it possible to produce an amorphous layer with a lower implanted dose than at room temperature, so that impurity concentrations did not exceed solubility values. Both n^- and p-type dopants were used to determine if the impurity type had an influence on the annealing behavior. In $< 111 >$ oriented Si the anneal behavior is strikingly different than in $< 100 >$ Si and the amount of disorder depends on the anneal procedures.[75]. Therefore, $< 111 >$, $< 100 >$

and $\langle 110 \rangle$ substrates were used to investigate possible orientation effects. Both isothermal and isochronal anneal sequences were used to determine if the amount of disorder were dependent on the anneal procedure. The intent was to determine if the difference in recrystallization behavior between GaAs and Si was real or was an artifact due to the choice of implantation conditions, substrate orientation or annealing procedure.

Channeling effect measurements with 1 MeV ^{4}He ions were used to investigate the recovery of the amorphous layer. Measurements were also made with 400 keV H^+ ions. Energy to depth conversions for ^{4}He analysis were made using the stopping cross-sections of Ziegler and Chu[76]. Transmission electron microscopy and glancing angle x-ray diffraction were employed to obtain information on the structure of the regrown layer.

Figure 68 shows random and $\langle 100 \rangle$ GaAs samples implanted with Zn and annealed at various temperatures for 15 min. The spectrum for an as-implanted sample indicates that the implanted layer becomes amorphous over a depth of about 720Å. The spectrum for a sample annealed at 200°C shows that some recovery of crystallinity occurs at the interface between the amorphous layer and the underlying crystal. This is indicated by a shift in the rear edge of the aligned spectra toward the surface. After 300°C annealing, the backscattering yield decreases but is still high compared to the unimplanted samples, showing that the implanted layer contains a high level of disorder. Complete recovery was observed after 600°C annealing. The annealing of the amorphous layer produced in $\langle 100 \rangle$ and $\langle 110 \rangle$ GaAs by 400 keV Se implants shows almost the same behavior as in Fig. 68. Some recovery was observed at the interface between the amorphous layer and the underlying crystal for annealing at 200°C. The

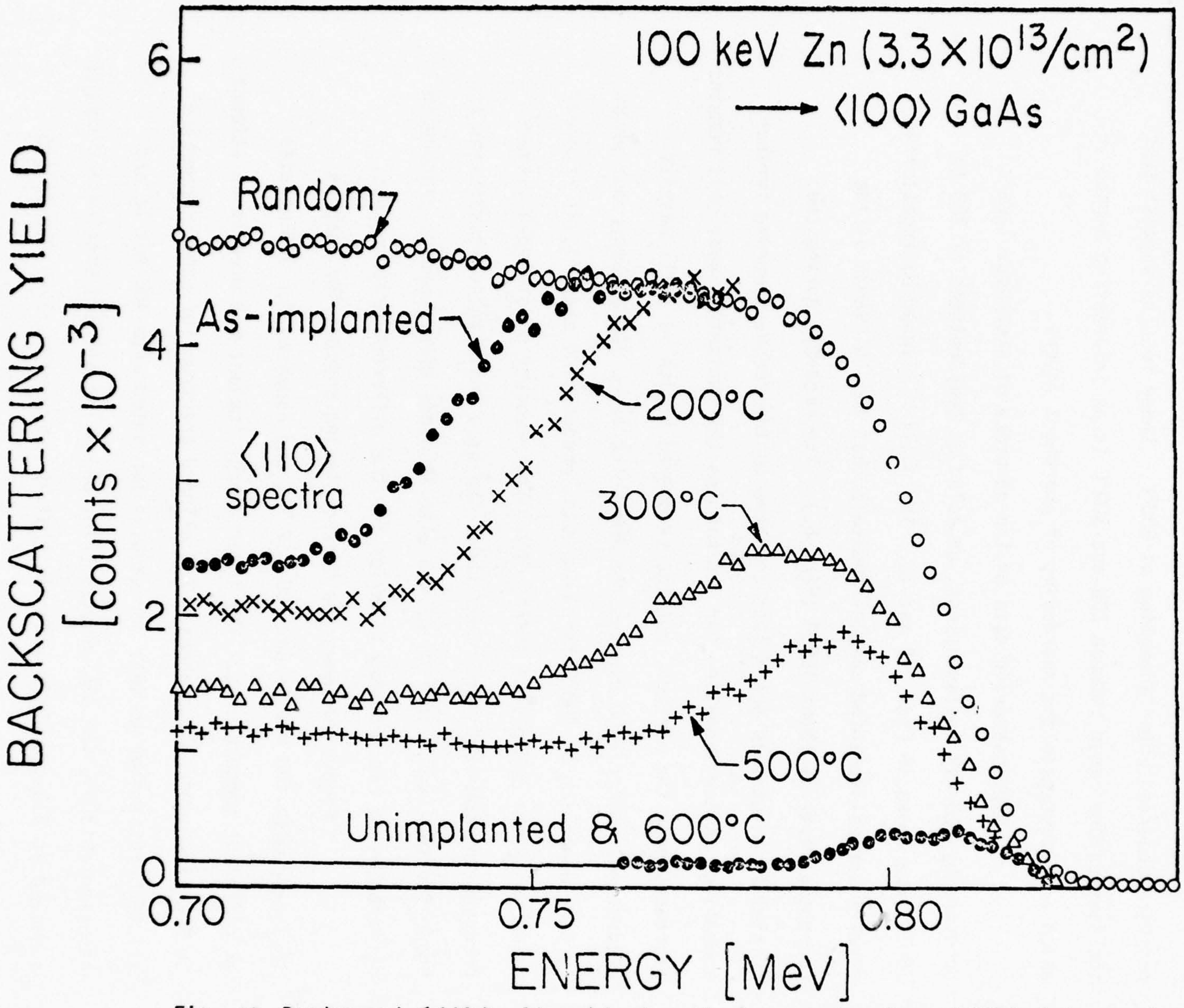


Fig. 68 Random and < 110 > aligned backscattering spectra from < 100 > GaAs samples implanted with Zn and annealed for 15 min at the indicated temperatures.

amorphous layer disappeared after annealing at 300°C and significant recovery occurred after annealing at 600°C. These results suggest that the temperature range between 200 and 300°C is an interesting region in which to investigate the reordering of amorphous layers.

Backscattering data on the recovery of amorphous layers produced by 400 keV implantations, annealed at temperatures of 200 to 300°C, are shown in Figs. 69 and 70. The < 111 > aligned backscattering spectra for as-implanted samples indicate that the thickness of the amorphous layer is about 1600Å (Fig. 69). The recovery during the initial 15 minutes is again fast compared to the recovery during further annealing. After annealing for 375 minutes the implanted layer only remains amorphous near the surface, but the recovered region is still heavily disordered. After 1100 minutes the implanted layer is no longer amorphous. Further annealing at 300°C for 30 minutes produces no significant recovery as shown by the solid line in Fig. 69. The recovery of amorphous layers produced in <100> and <110> GaAs under the same implantation conditions as shown for the sample in Fig. 69 was also studied; there were no pronounced differences in the recovery behavior for the different orientations.

Figure 70 shows the backscattering spectra for samples implanted with 400 keV Se and 100 keV Se_2 and annealed for 343 minutes at different temperatures. The lower energy implant was used in an attempt to make the surface amorphous. The aligned spectrum for samples annealed at 200°C is similar to that for samples implanted with 400 keV Se and annealed at 300°C for 375 minutes (Fig. 69). The aligned spectra for samples annealed at 220 and 250°C indicate that the amorphous layer disappears,

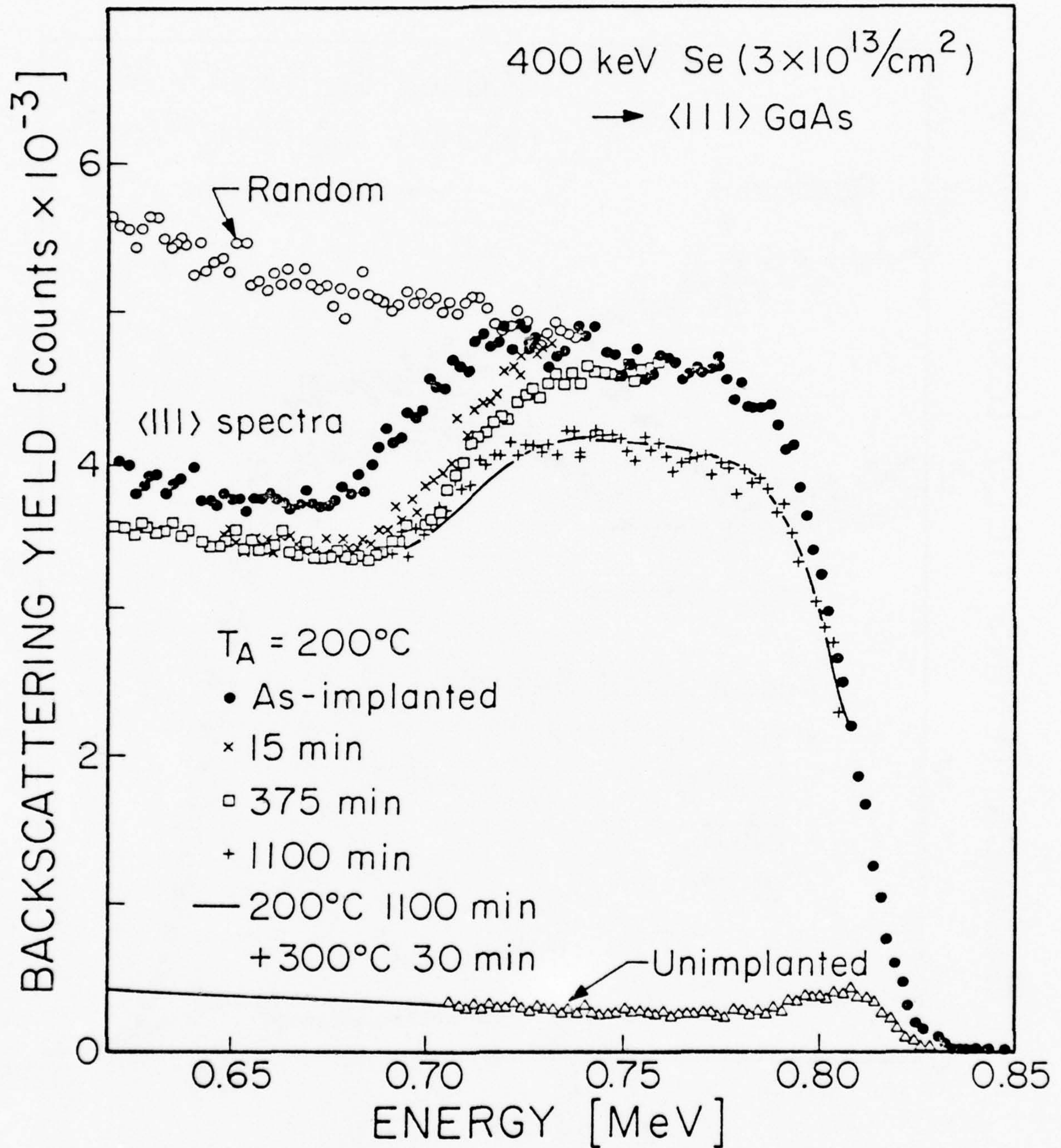


Fig. 69 Random and aligned spectra from Se implanted GaAs samples annealed as indicated. < 111 > GaAs and < 111 > aligned spectra.

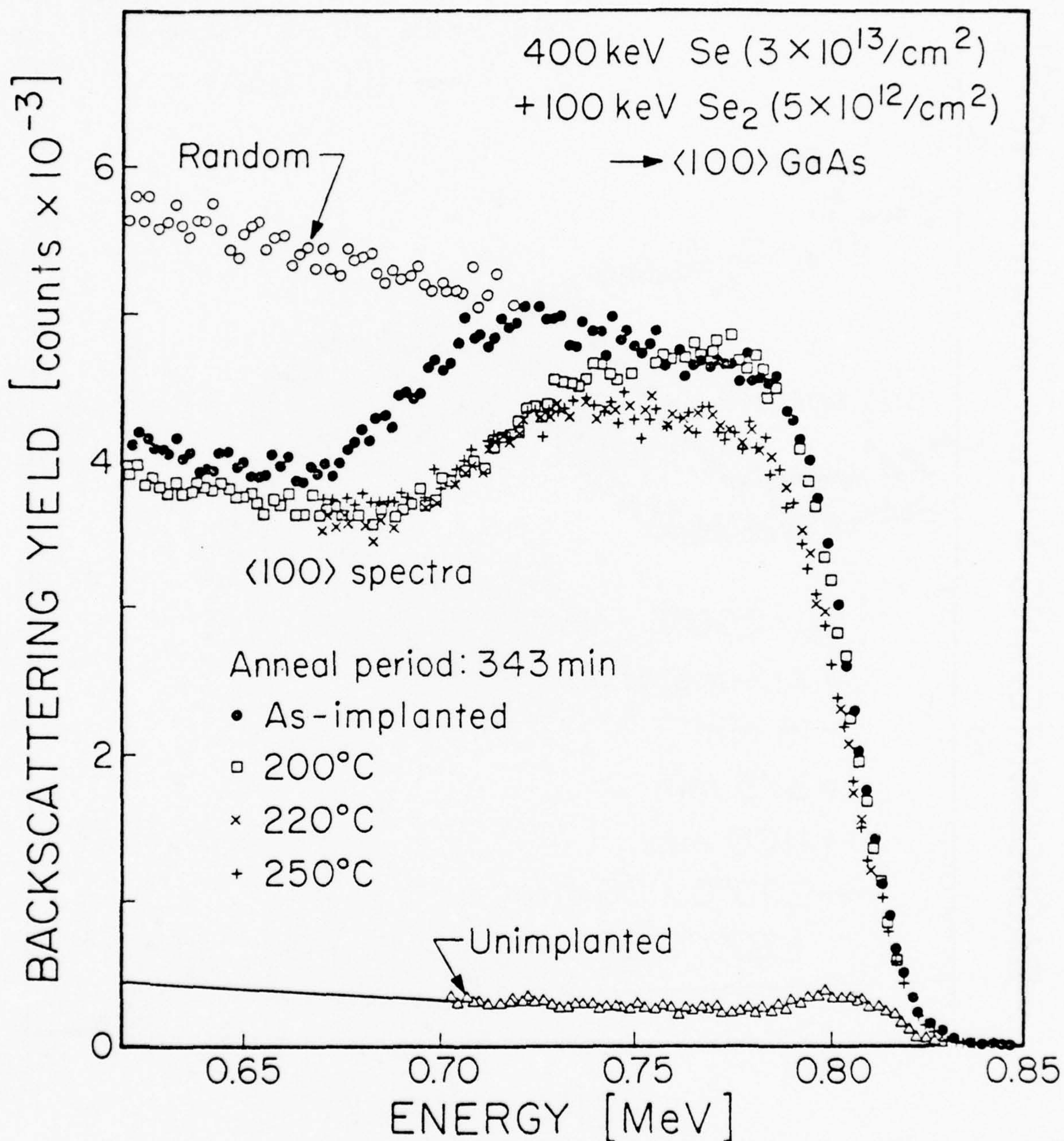


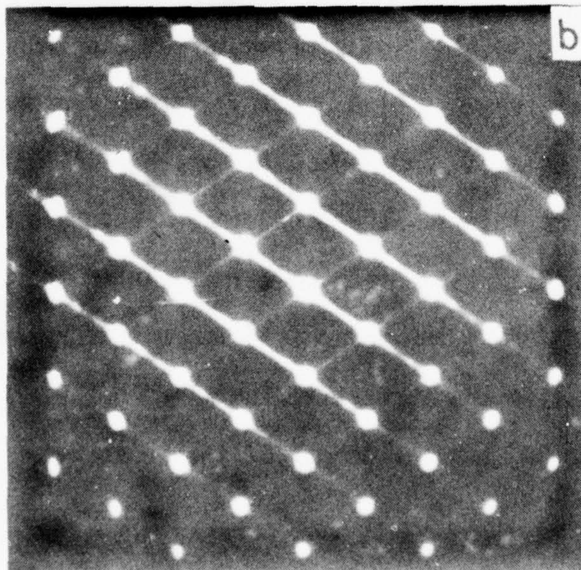
Fig. 70 Random and aligned spectra from Se implanted GaAs samples annealed as indicated. < 100 > GaAs and < 100 > aligned spectra.

but a high level of disorder still remains in the implanted layer. These spectra are almost the same as those observed after annealing at 200°C for 1100 minutes or 300°C for 30 minutes, as shown in Fig. 69.

Transmission electron microscopy and glancing angle x-ray diffraction measurements have been employed in an effort to characterize the disorder present in annealed implanted layers. The samples were implanted with 400 keV Se ions and exhibited backscattering spectra similar to that represented by the solid curve in Fig. 69. The glancing angle x-ray diffraction measurements showed blurred spots in the diffraction pattern. This indicated the presence of substructure in the annealed layer. The absence of rings and extra spots in the diffraction pattern shows that the regrown layer is not polycrystalline and it is epitaxial with the underlying substrate.

The epitaxial nature of the regrown layer and the presence of substructure was shown directly in TEM micrographs and selected area electron diffraction patterns. An example of the substructure is shown in Fig. 71. Extensive streaking in <111> directions in the electron diffraction pattern in Fig. 71b arises from the high density of thin regions (substructure) lying along {111} planes, one variant of which is illustrated in Fig. 71a. It is possible that this substructure may be antiphase domains, resulting from homogeneous nucleation of crystalline GaAs in the amorphous layer. Evidence for epitaxy was the observation that the crystallographic direction of the normal to the surface of the regrown layer was [100] which is parallel to the [100] surface normal of the substrate.

Fig. 71 TEM of GaAs implanted with 400 keV Se ions and annealed at 200°C for 1100 minutes. (a) Dark field image illustrating crystalline substructure in implanted layer. g: < 111 > streak. (b) Selected area diffraction pattern, [110] zone normal with intense < 111 > **streaking.**



In conclusion, there is a significant difference between the annealing behavior of implanted amorphous layers in GaAs and in Si. It is clear that the difference is real, and that the different implantations and annealing procedures used in this study are sufficient to exclude the possibilities that the substrate orientation, impurity or annealing cycles are responsible. Such effects have led to anomalous results in the recrystallization of implanted Si. In the case of GaAs, the recovery of the amorphous layer shows no significant orientation dependence and the regrown layer exhibits a high amount of disorder. In Si the recovery shows a strong orientation dependence and there is low residual disorder following reordering of the amorphous layer for <100> samples. The isochronal annealing data for GaAs show that reordering occurs over a relatively broad temperature interval in contrast to the reordering of Si. Although amorphous GaAs recrystallizes in an epitaxial fashion, our results indicate that in GaAs the reordering of the implanted amorphous layer does not follow the simple epitaxial growth found in Si. It is possible that the different behavior of GaAs is due to local variations of its stoichiometry in the implanted region. At low temperatures (200 to 300°C) the amorphous layer can recrystallize, but the temperature may be too low to permit the motion of Ga and As necessary to adjust the local stoichiometry.

5.5 Contact Metallization Systems - Caltech

To form ohmic contacts to GaAs an alloy of various metals and a dopant for GaAs is deposited on the GaAs substrate and heated above the melting point of the metal-dopant eutectic. A portion of the GaAs is then

dissolved in the alloy and, upon cooling, the dopant is incorporated in the epitaxially regrown layer. The Au-Ge alloy system is most generally used.

Usually a top layer of Ni or Pt is evaporated on the Au-Ge to prevent island formation. Low alloying temperatures are chosen to reduce (a) the damage to the GaAs during cooling and (b) the loss of As during the heating cycle. Both Ni and Pt form compounds with Ge at these temperatures and could act as a "sink" for the Ge.

The Au-Ge-Ni system was first studied on a SiO_2 substrate in order to separate the backscattering from Au, Ge and Ni from backscattering from the substrate. In a second stage, the Au-Ge-Ni system was applied on GaAs substrates. Finally, a Au-Ge-Pt system was investigated.

Backscattering spectometry is well suited to analyze how these films are changed by the annealing cycles to which they are subjected, because the results are quantitative and the depth distributions are not obtained by sputtering. Recent investigations have shown that rare gas sputtering modifies the composition of binary alloys and compounds in the near-surface region because of unequal sputtering of the constituent atoms.[105] Analytical techniques such as Auger Electron Spectroscopy may lead to erroneous conclusions in such cases.

(a) Ge-Au-Ni System on SiO_2

The 2 MeV ^4He backscattering spectrum of a sample having the structure SiO_2/740Å Ge/2300Å Au/470Å Ni is shown in Fig. 72, where the backscattering yield is plotted vs the energy of the scattered He-particles. In this and all the following backscattering figures the lower energy part of the spectrum which contains the signal of the SiO_2-substrate has been omitted for simplicity. Figure 72a shows the backscattering spectrum of

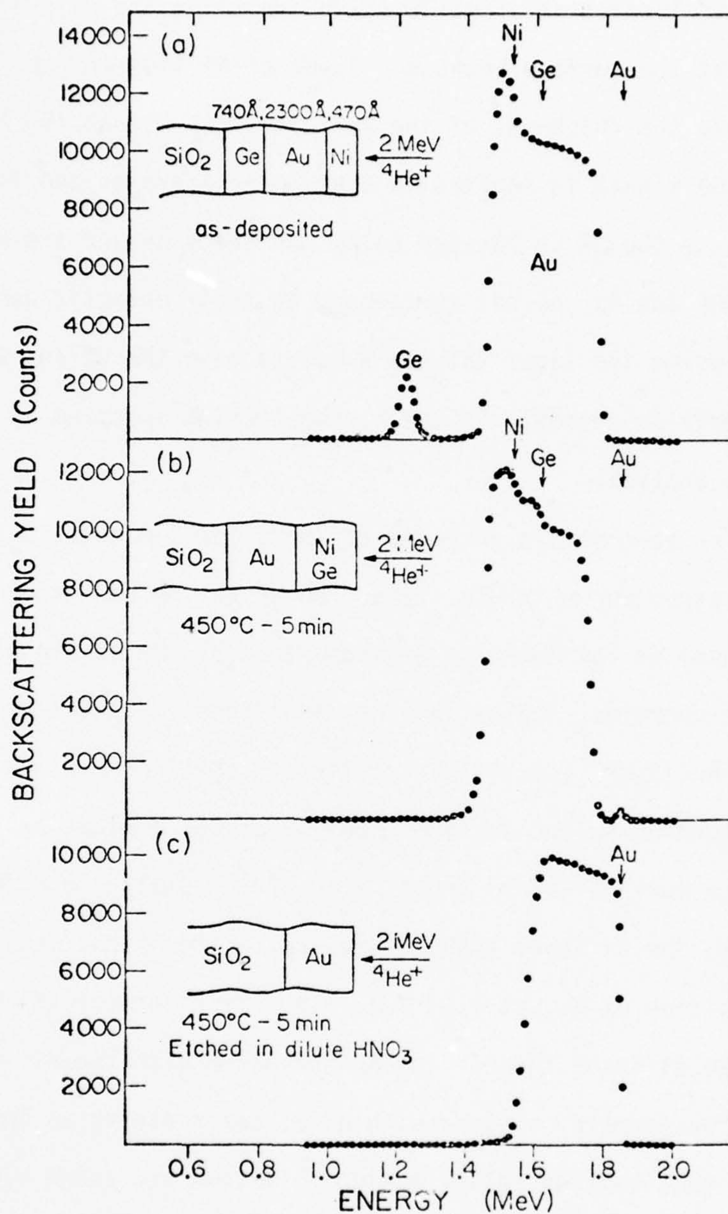


Fig. 72 2 MeV ^{4}He backscattering spectra of a SiO_2/740Å Ge/2300Å Au/470Å Ni sample. The spectra of the substrate has been omitted and the vertical arrows indicate the energy of He particles scattered from surface atoms of the corresponding elements. (a) as-deposited, (b) annealed at 450°C for 5 minutes, and (c) same as (b) but Ge-Ni layer etched off in dilute HNO_3

the as-deposited sample. The vertical arrows indicate the energy of He-particles scattered from the surface atoms of the corresponding elements. The Au signal is located at energies which are below the reference energy for a Au atom at the surface because a layer of Ni lies on top of the Au film. Due to the thickness of the Au layer, the Ni and the Au signals overlap. The Ge signal is shifted to even lower energies and is well separated because the Ge is located below the thick Au and the Ni layer. The amount of Ge and Au do not correspond to their eutectic composition. The aim in choosing the layer thickness was to have the Ge and Au signals separated as well as possible in the backscattering spectrum in order to facilitate the analysis.

The same sample annealed at 450°C for 5 minutes has the backscattering spectrum shown in Fig. 72b. The annealing had major effects: (a) the Ge signal at low energies disappeared, (b) the Au signal moved to slightly lower energies, indicating that additional mass has accumulated on top of the Au layer, (c) the backscattering spectrum showed a step at the energy corresponding to the surface location of Ge, indicating that Ge had appeared in the surface layer, and finally, (d) a small amount of Au had penetrated into the Ni layer above it, as reflected by the small signal at surface position of Au, at 1.83 MeV. The first three facts immediately suggest that Ge diffused through the Au and mixed with the Ni. Since it is known that Ge forms a compound with Ni at temperatures as low as 150°C, it is assumed that some nickel-germanide formation has taken place. However, it is not possible to calculate the atomic composition ratio of the germanide because the backscattering spectrum has overlapping signals. To prove that no Ge is dissolved in the Au but that Ge has been completely

absorbed by the Ni, which is on top of the Au layer, the Ge-Ni layer was etched off in dilute HNO_3. Au is not attacked by this etchant. The backscattering spectrum of the etched samples, given in Fig. 72c, shows no evidence of any Ge dissolution in Au within its resolution limit of better than 0.5%. The trailing edge of the Au peak is not as sharp as the front edge, indicating that the Au layer is somewhat nonuniform. This was verified by SEM analysis.

(b) Ni-Au-Ge System on SiO_2

It is interesting to see whether Ge diffuses in the other direction too, i.e., if it diffuses from a location at the surface of the sample through the Au to form compounds with a Ni film lying on the SiO_2 substrate. Therefore, samples of the composition SiO_2/910Å Ni/1020Å Au/1700Å Ge have been prepared. The backscattering spectrum of the as-deposited sample is shown in Fig. 73a. It can be seen that there is some overlap between the Au and the Ge signals because Au, the heavier element, is below the Ge, the lighter element. The backscattering spectrum of the same sample annealed at 450°C for 5 minutes is given in Fig. 73b. The spectrum clearly shows that the Au is now at the surface and that practically no Ge remains there. Thus Ge diffused through the Au to form compounds with the Ni. The trailing edge of the Au as well as the front and trailing edges of the Ge-Ni compound are not sharp, indicating that the layers are very nonuniform. This is not surprising since in this case the Ni was not on the top and balling of the Au-Ge alloy may have occurred during the annealing cycle.

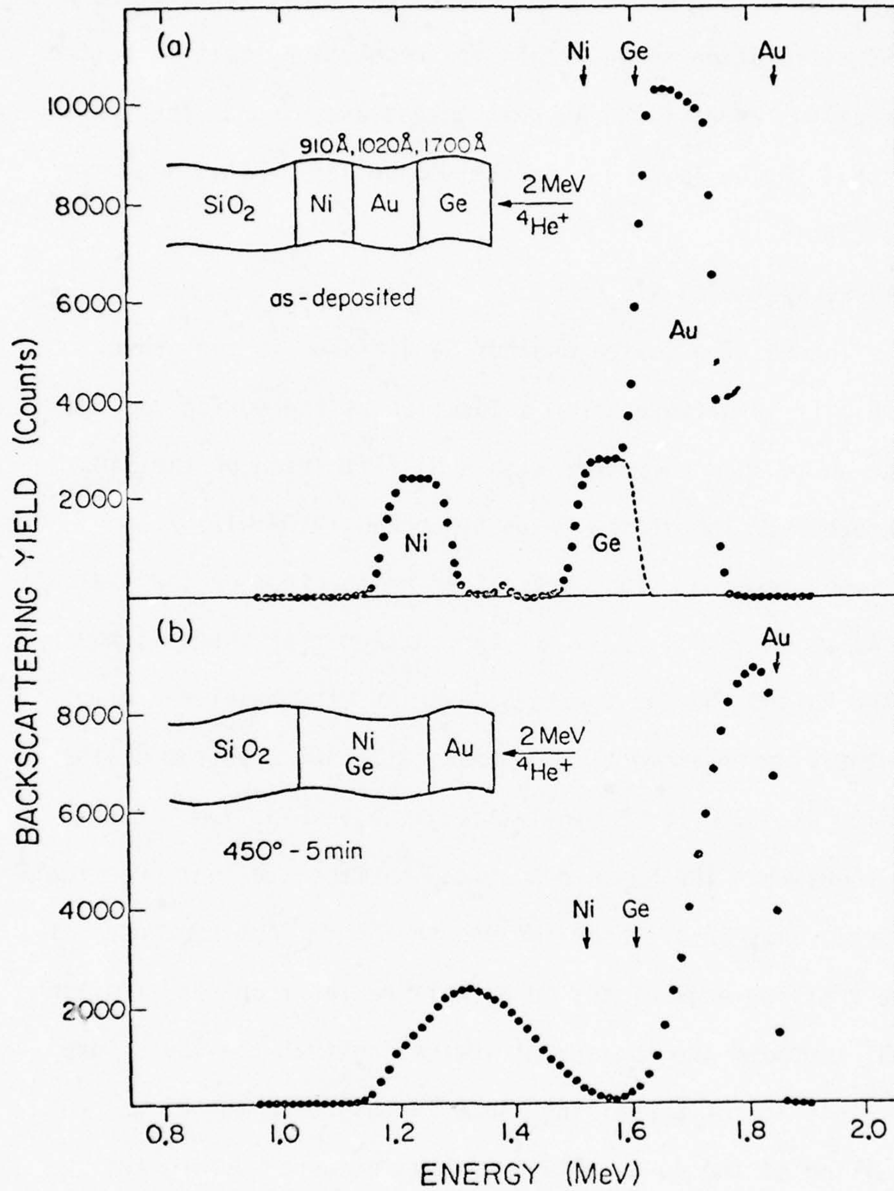


Fig. 73 Energy spectra of 2 MeV ^{4}He ions backscattered from a SiO_2/910Å Ni/1020Å Au/1700Å Ge sample. The spectra of the substrate has been omitted and the vertical arrows indicate the energy of the particle scattered from surface atoms of the corresponding elements. (a) as-deposited, (b) annealed at 450°C for 5 minutes.

(c) Ge-Ni-Au System on SiO_2

In the first two systems, where the Ge and the Ni were separated by a Au layer, Ge diffused through the Au to form compounds with the Ni, whether the Ge was the bottom or the top layer. Apart from the small amount of Au diffusion into the Ni in the case of the Ge-Au-Ni system (see Fig. 72b) the role of the Au seems to be a passive one in that it serves mainly as transport medium for the Ge. This can be shown by evaporating a sample in the sequence SiO_2/3470Å Ge/1710Å Ni/1290Å Au. The backscattering spectrum of the as-deposited sample is given in Fig. 74a. Due to the small mass difference between Ge and Ni, their signals overlap. However, the Au peak is well separated from the others because Au is now the top layer. Figure 74b shows the backscattering spectrum of the same sample annealed at 450°C for 5 minutes. It can be seen that Ge and Ni react while the Au film is not visibly changed by the heat treatment. A sample annealed at 320°C for 1 hour showed the same result. Thus Au is a passive element in the reaction between Ge and Ni.

(d) (Thick Ge)-Au-Ni System on SiO_2

In all the combinations of Au, Ge and Ni considered so far, the atomic percentage of Ge evaporated was less than the atomic percent of Ni. Thus, there was always enough Ni present to consume all the Ge as NiGe during their interaction. The question arises as to what happens when the amount of Ge is greater than that needed to form NiGe. The answer is given by the energy spectrum of 2 MeV ^4He ions backscattered from a SiO_2/3360Å Ge/1150Å Au/930Å Ni sample (Fig. 75). The thicknesses were chosen so that the atomic percentage of Ge is larger than that for Ni. Figure 75a shows the backscattering spectrum of the as-deposited sample, while the spectrum

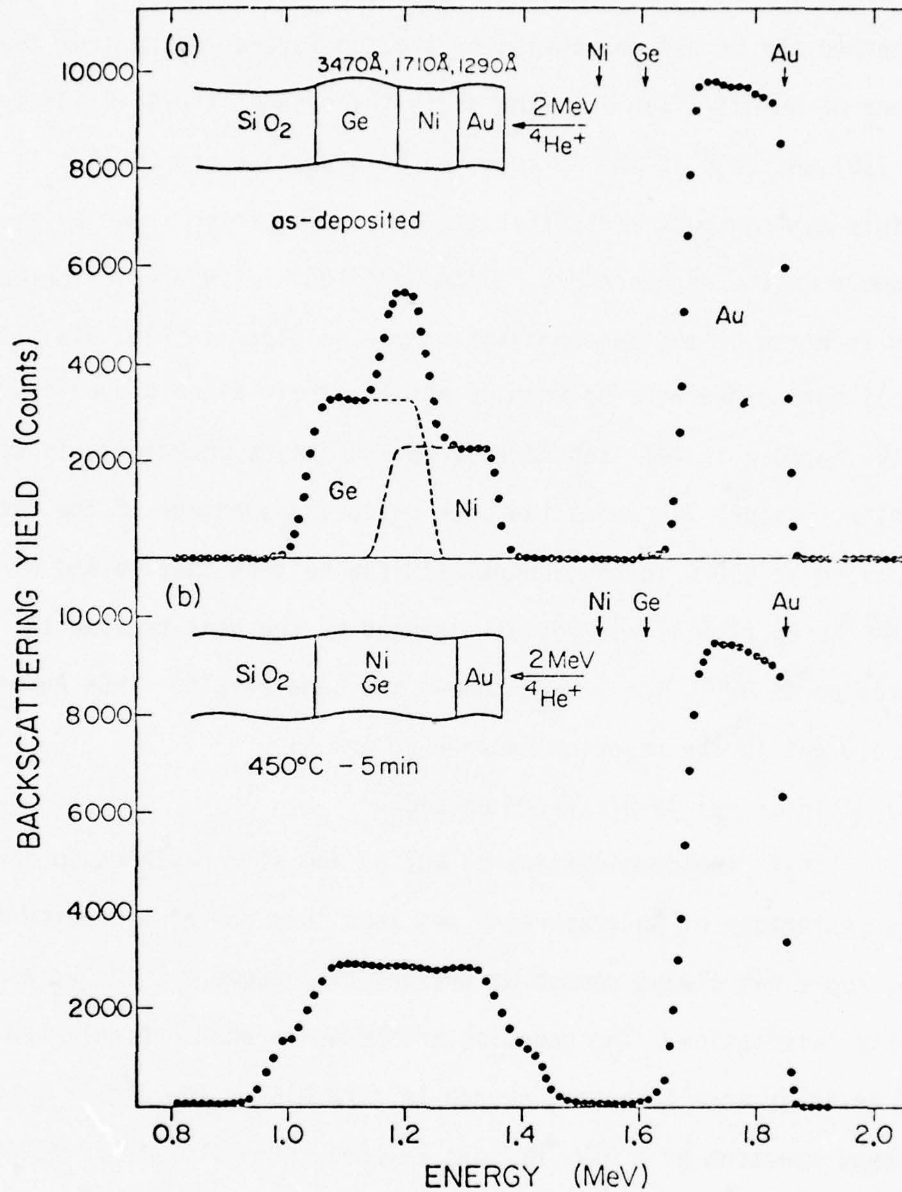


Fig. 74 Energy spectra of 2 MeV ^{4}He ions backscattered from a SiO_2/3360Å Ge/1150Å Au/930Å Ni. The spectra of the substrate has been omitted and the vertical arrows indicate the energy of the particles scattered from surface atoms of the corresponding elements. (a) as-deposited, (b) annealed at 450°C for 5 minutes

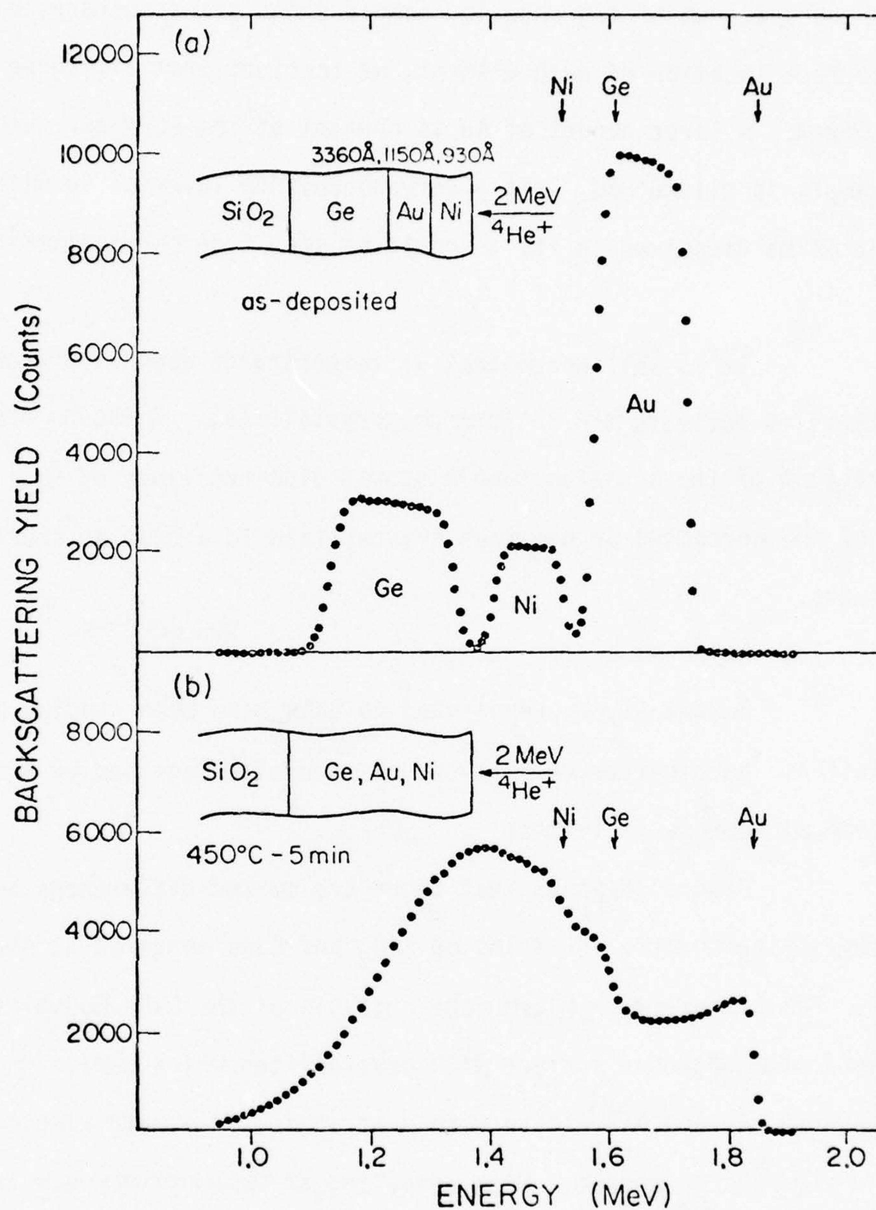


Fig. 75 2 MeV ^{4}He backscattering spectra of a SiO_2/3470Å Ge/1710Å Ni/1290Å Au sample. The spectra of the substrate has been omitted and the vertical arrows indicate the energy of the particles scattered from surface atoms of the corresponding elements. (a) as-deposited, (b) annealed at 450° C for 5 minutes.

of the same sample annealed at 450°C for 5 minutes is given in Fig. 75b. Since the spectrum of the annealed sample shows steps corresponding to the surface location of each element, we conclude that all three elements have mixed. A large amount of Au is present at the surface. Etching of the sample in dilute HNO_3 left a very nonuniform layer of Au with a large amount of Ge dissolved in it, as could be seen from backscattering analysis.

It is well known that at temperatures above 350°C amorphous Ge starts to nucleate and to form polycrystallites. Glancing angle x-ray diffraction of the annealed sample showed distinct lines of Ge. At least some of the unreacted Ge has thus crystallized in a time as short as 5 minutes.

(e) Au-Ge-Ni System on GaAs

AuGeNi layers evaporated on GaAs have been studied by x-ray difraction, backscattering analysis of energetic ions and by SEM with electron microprobe facilities.

Figure 76 shows that there are marked differences between backscattering spectra for films on SiO_2 and GaAs annealed at 450°C for 5 min. SEM and electron microprobe analysis of the GaAs-AuGeNi sample showed a nonhomogenous surface with crystallites which were rich in the elements Ge, As and Ni. These were distributed in a matrix which was rich in the elements Au and Ga. Upon annealing at temperatures near the Au-GaAs eutectic (450°C) one may assume that Ga and As will dissolve into the Au and diffused out to react with the GeNi compound respectively. This reaction between Au and GaAs may be dependent upon the annealing ambient,

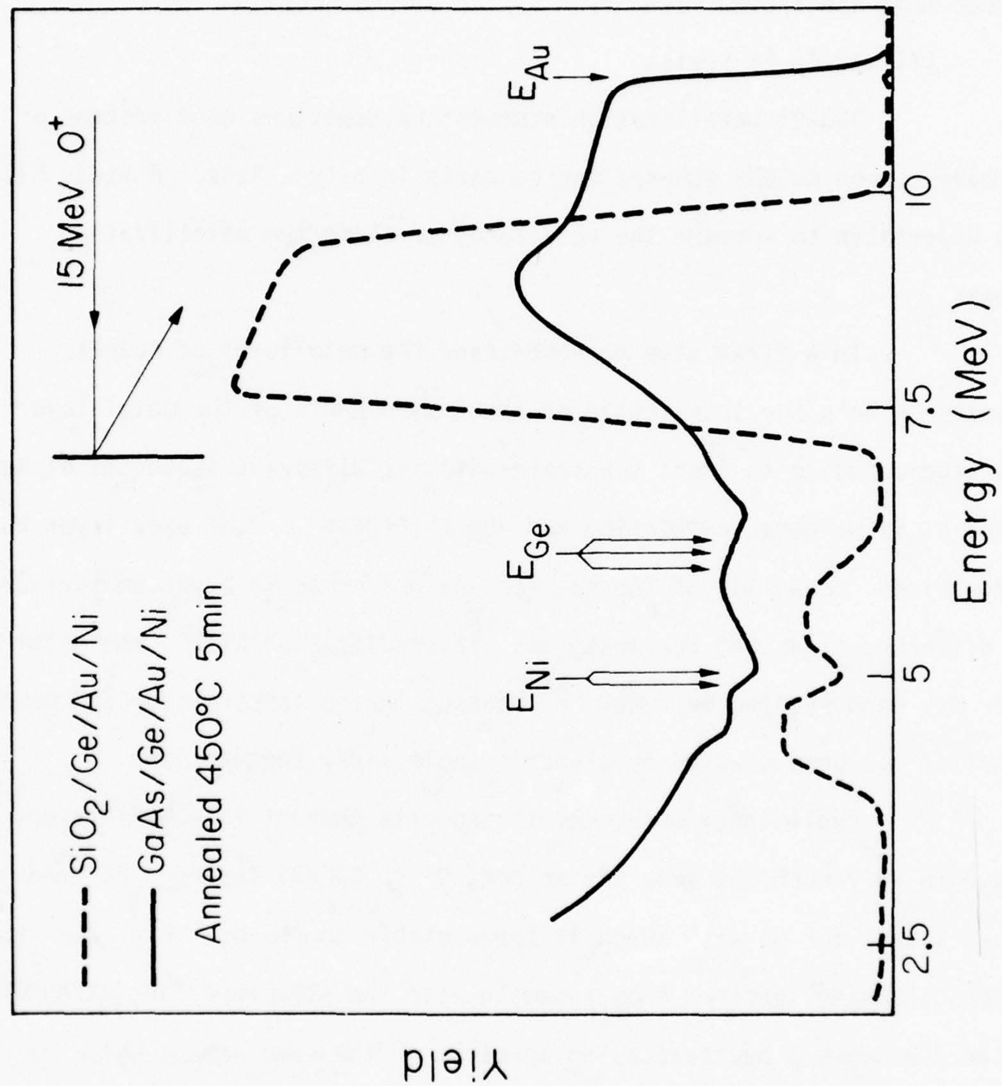


Fig. 76 15 MeV O backscattering through 150° from Ge-Au-Ni evaporated on SiO_2 and on <100> GaAs, and annealed at 450°C for 15 minutes. The bars indicate the energy for scattering from the surface from the main natural isotopes from each element.

which is indicated by Fig. 77. This figure shows backscattering spectra of two Au evaporated <100> GaAs samples. In the case where the sample is annealed at 422°C in vacuum,one can see that a dramatic reaction has taken place. When the annealing was performed in air there was much less reaction between GaAs and the Au film.

(f) Au-Ge-Pt System

AuGePt metallization schemes are sometimes used instead of the more common AuGeNi schemes for contacts in n-type GaAs. A study has been undertaken to compare the metallurgy of these two metallization schemes.

In a first step to understand the metallurgy of AuGePt contacts on GaAs the interaction of the 3 components of the metal layer have been studied using an inert substrate (SiO_2). Different sequences of Au, Ge and Pt films were evaporated and the thickness of each layer has been varied. Annealing of the samples was performed in a vacuum furnace for different times and temperatures. Inter-diffusion within the metal layer has been studied by 2 MeV He^+ backscattering spectroscopy and compound formation has been studied by glancing angle x-ray spectroscopy.

Preliminary measurements indicate that Pt in AuGePt-layers behave in very much the same way as does Ni in AuGeNi layers. Pt tends to act as a sink for Ge with which it forms stable compounds. Fig. 78a shows a backscattering spectrum from a sample with the structure SiO_2/Pt/Au/Ge. Figure 78b shows a backscattering spectrum of the same sample which has been annealed at 450°C for 5 minutes. One notices that the Au-edge has shifted to higher energies and a broad peak is found around 1.4 MeV. One

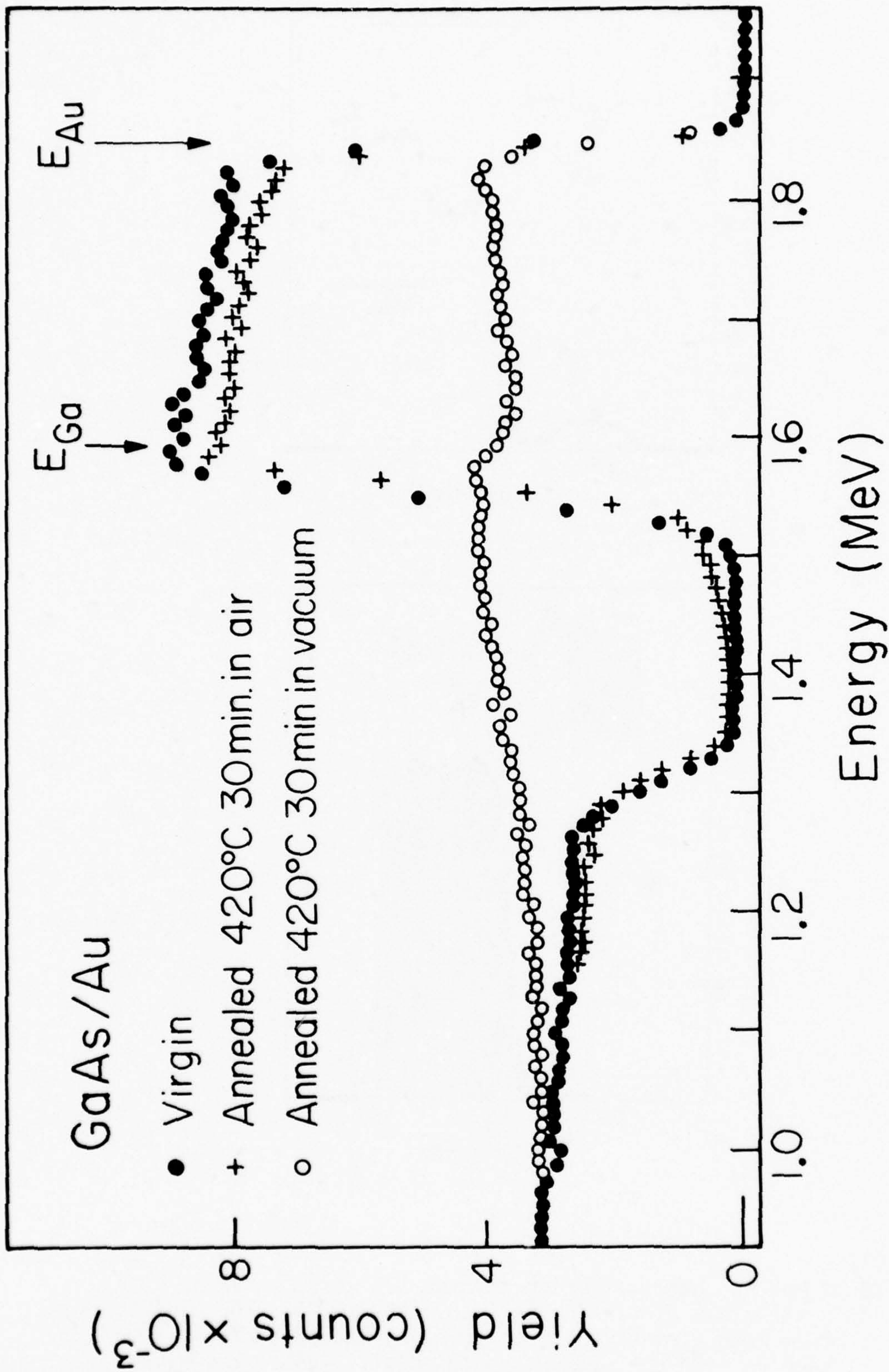
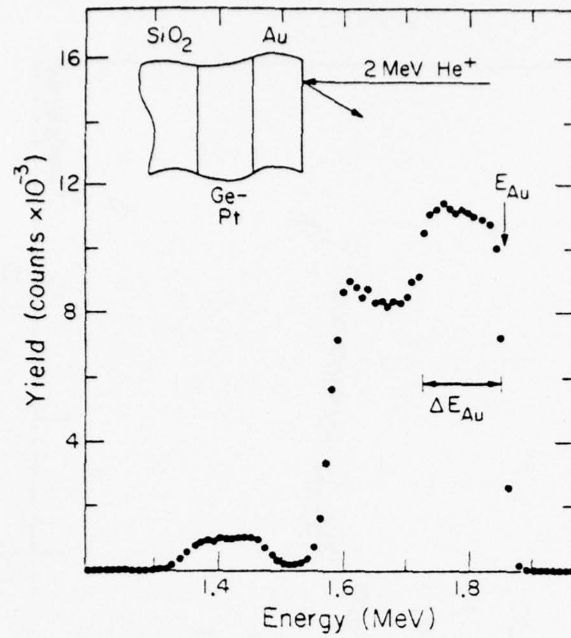


Fig. 77 2 MeV He^+ backscattering through 170° from <100> GaAs samples with 220Å evaporated Au, annealed in vacuum and air.



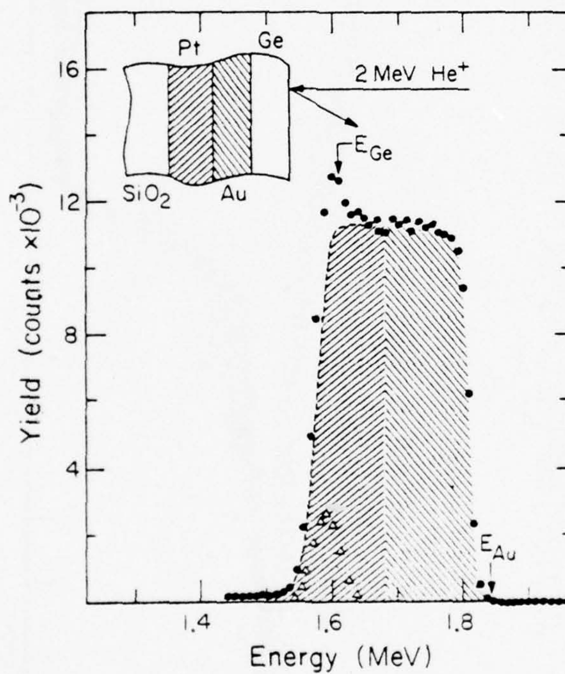


Fig. 78 2 MeV He^+ backscattering through 170° from a sample with a structure SiO_2/Pt/Au/Ge (-160Å/990Å/630Å). The contribution from each element has been found by backscattering from samples with one element shadowed off. (a) as-deposited (b) annealed at 450°C for 5 min. in vacuum.

interpretation of these measurements is that Ge has diffused through the Au layer and formed compounds with Pt. The energy width of the unreacted portion of the spectrum, indicated by ΔE_{Au} in Fig. 78b, is very close to the width of the original evaporated Au-film, indicating that almost all the Ge is trapped in the GePt compound. Similar results have been obtained for other sequences of evaporation for the three elements. The layers seem to be laterally nonuniform when the Ge to Pt ratio exceeds 1. The larger the ratio the more nonuniform are the layers.

In summary, backscattering techniques have been used to investigate metallization schemes for GaAs. Backscattering measurements before and after anneal of Au-Ge-Ni layers deposited on SiO_2 in different sequences show that Ge and Ni mix together to form compounds. If they are separated by a Au layer Ge diffuses through the Au to combine with the Ni. It is more difficult to determine the behavior of the Au-Ge-Ni system on GaAs using the backscattering technique. This behavior appears to be more complicated because of a reaction between Au and GaAs. The Au-Ge-Pt system behaves similarly to the Au-Ge-Ni system when it is annealed on an SiO_2 substrate.

6.0 CORRELATION BETWEEN MATERIAL PARAMETERS AND DEVICE PERFORMANCE

In the preceding sections of this report, material technologies pertinent to microwave FET devices have been discussed. In the following section, the performance of GaAs MESFETs will be evaluated in order to assess progress achieved in the material technologies. The emphasis will be placed on comparing technology alternatives like epitaxial vs ion implanted active layer, or buffered vs unbuffered substrate. A conclusion emerging from such comparisons will be that ion implantation in GaAs has become a mature technology, capable of producing state-of-the-art FET devices, with certain advantages over epitaxial technologies. In the context of device analysis, efforts have been dedicated to problems related to IMPATT devices. In Sec. 6.2, an analysis of IMPATT parameters will be presented as a tool to obtain material parameters useful in device design. In Sec. 6.3, an anodization and etching technique will be discussed. Finally, in Sec. 6.4, measurements of ionization coefficients in GaAs will be presented and discussed.

6.1 MESFET Performance - Science Center

Ion implantation has evolved into a reliable technique for the fabrication of MESFET active layers, with excellent uniformity (inherent to this technique), and also excellent reproducibility when the substrates are properly preselected (see Sec.5.1). It is therefore important to compare ion implantation with epitaxial material technologies by actually putting them to test on devices. Two aspects of device performance will be considered, namely, rf performance and parameter drift vs time. It will be shown that

low power MESFETs fabricated from selenium implanted active layers have less drift problems than epitaxial transistors, and their rf performance comes close to matching the theoretically predicted performance.

In the study of drift, the variation of noise figure with gate bias has been investigated. MESFETs fabricated on LPE and ion implanted active layers have been compared. The epitaxial layer was grown onto a substrate (Crystal Specialties #1718, see Sec. 3.2.1) which passed a qualification test for epitaxial growth (see Sec. 3.2.4). The ion implanted MESFETs were fabricated on a layer made by Se implantation into a semi-insulating (SI) substrate (Crystal Specialties #2004) which passed a corresponding qualification test for ion implantation (see Sec. 5.1). Noise figures at 10 GHz were measured on both types of transistors. The optimum noise figures were near 4 dB for both transistors. The most interesting observation is how a perturbation of the gate bias voltage affects the noise figure, as shown in Fig. 79. Originally, the gate is biased for optimum noise figure. A positive or negative voltage step is applied to the gate producing a change in the noise figure. When the gate bias voltage is returned to its original value the noise figure also relaxes towards its original value. However, the settling times are different for the two types of transistors. Fig. 79 shows that the ion implanted transistor recover faster than the epitaxial transistors, the effect being more dramatic in the case of a negative gate bias step.

The long transient observed in the noise figure of the epitaxial transistors can be attributed to interface states at the active layer - SI substrate interface or to surface effects. The implanted transistors are less subject to these problems due to the nature of the implantation process.

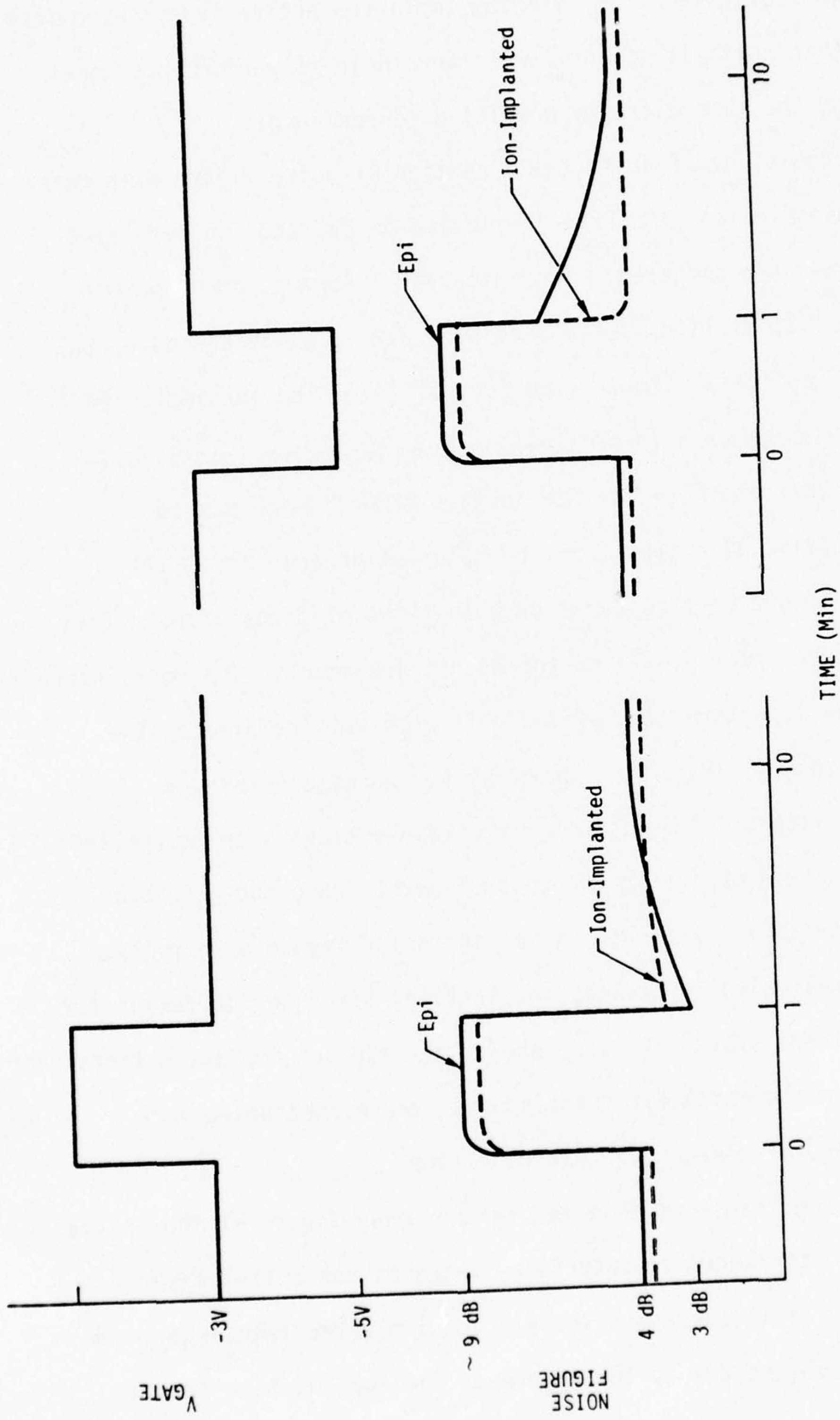


Fig. 79 Time constant effects in noise figure in GaAs FETs.

Monitoring the drift of rf device parameters, such as gain and noise figure, requires a considerable effort because of the need for continued measurements over extended times using expensive gear. In order to simplify the tests, a new approach for monitoring drift has been tried.

Our approach is based on our observation that the drift of microwave parameters and the drift of the low frequency (10 KHz) transconductance are correlated. It has also been observed that the initial rate of drift after turn on is an effective indicator of long term drift effects. Therefore, measurements were made of the change in the low frequency transconductance, g_m, of devices for the first 10 minutes after turn on using the test setup shown in Fig. 80(a). The gate bias was switched from a high current condition (i.e. $V_{gs} = 0$) to the gate bias voltage that gives minimum noise for rf frequencies. The voltage step was therefore negative, reducing the device current to approxametly 15% of full current.

The above tests have been applied to devices fabricated on epitaxial material (liquid phase and vapor phase) and implanted material. Results are shown in Fig. 80b where the relative transconductance is plotted against time for representative devices. The implanted device shows a very short settling time and the smallest change in transconductance. The device made from vapor phase epitaxial material (bought from a commercial vendor) shows slow drift from its initial post switching value. Such drift is even more noticeable for the LPE device. The transconductance of the epitaxial transistors goes through an upward spike immediately after switching the gate bias. The drift of the LPE transistor was monitored for a long period of time. The transconductance continued to decrease reaching a 30% change after 24 hours.

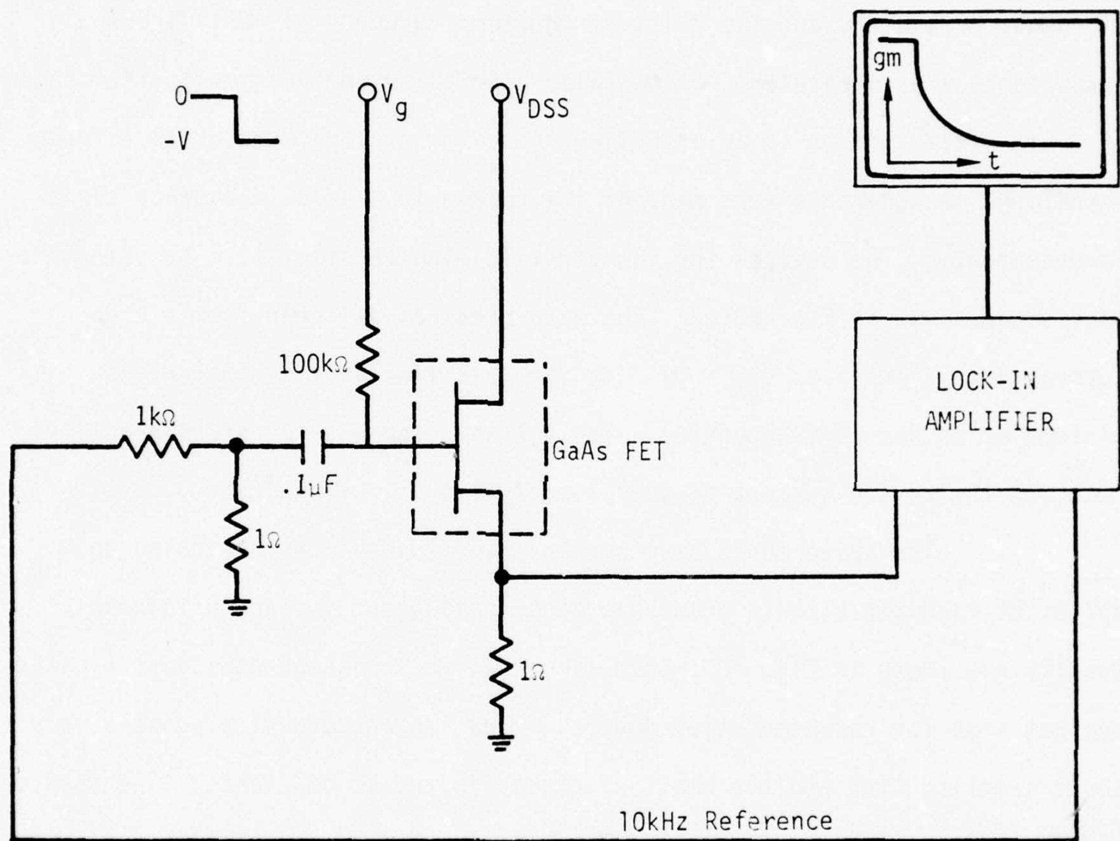


Fig. 80a Test set for measuring low-frequency transconductance of GaAs FETs.

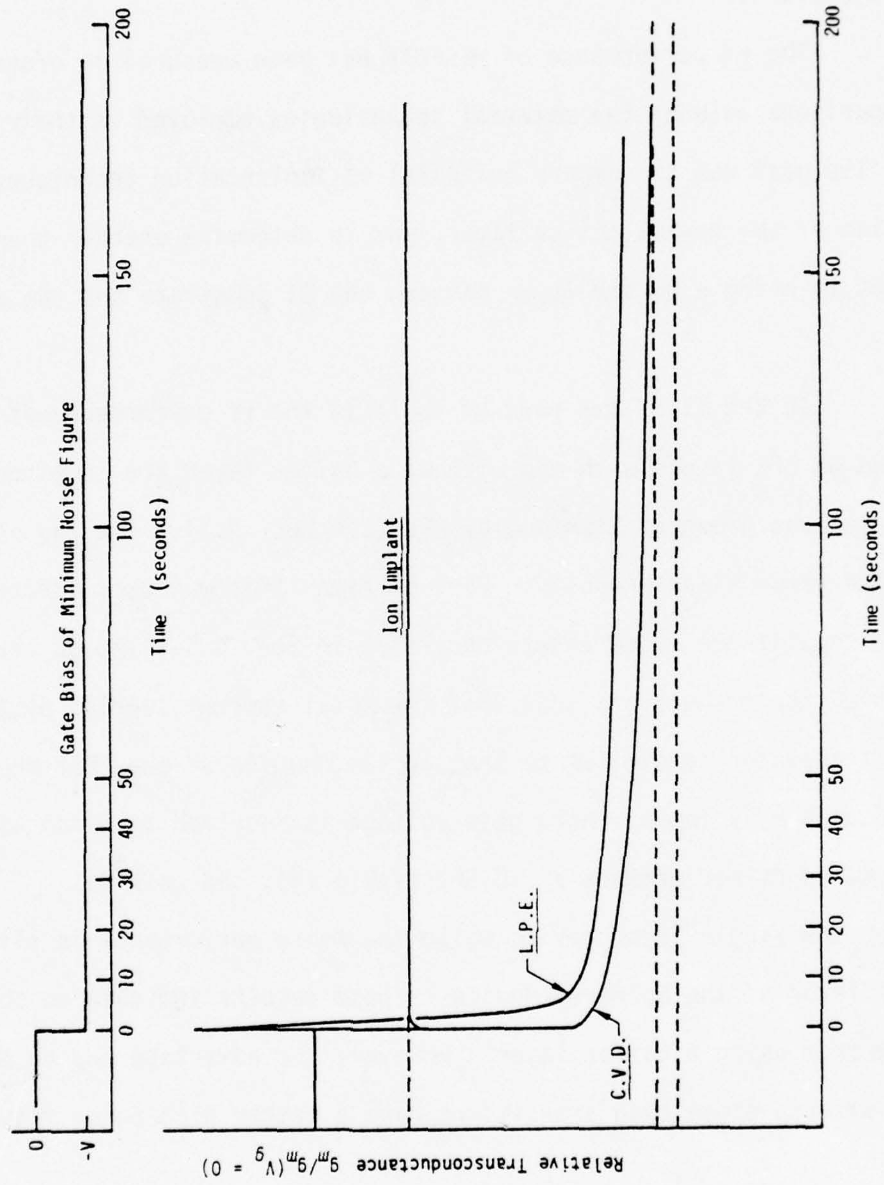


Fig. 80b Measured transconductance vs. time characteristics for ion implanted, CVD and LPE GaAs FETs.

These results show again an advantage of implanted transistors over epitaxial transistors in that the implanted transistors appear free of slow transients.

The rf performance of MESFETs has been measured in order to draw comparisons between the material technologies employed in their fabrication. The goal was to compare epitaxial vs implantation techniques for fabrication of the device active layer, and to determine whether there are advantages in using a buffer layer between the SI substrate and the active layer.

In the first two rows of Table 14 the rf performance of transistors fabricated on LPE layers with and without a buffer layer are compared. The buffer layer was grown at Stanford by LPE (see Sec. 4.1). The two active layers were grown simultaneously. Part of each layer was used for the transient capacitance measurements described in Sec. 4.1. The dc characteristics of the transistors show that the total current carried by the buffered transistor is similar to that in the unbuffered one, but the transconductance is lower. More gate voltage is required to pinch off the device. As to rf performance at 10 GHz (Table 14), the gain is better for the single layer device while the noise performance is slightly better in favor of the buffered device. These results indicate no obvious advantage from using a buffer layer. However, the advantage may be masked by other effects since both transistors have a rather high noise figure.

Table 14: Summary of RF Measurements on FETs at 10 GHz

Transistors	MAG	N.F. (steady state)	N.F. (initial)	Associated Gain at Min. N.F.
130F8-S Sn doped LPE layer on substrate	8 dB	7.95 dB	7.9 dB	5.0 dB
130F8-B Sn doped LPE on buffer layer	8 dB	6.1 dB	6.0 dB	2.5 dB
912 S implanted in buffer layer	9 dB	5.0 dB	4.6 dB	3.5 dB

Although the results were similar, the unbuffered transistor had slightly higher S_{21} (2.2 vs 2.0 at 10 GHz) and lower S_{12} (0.06 vs 0.10 at 10 GHz) than the buffered transistor. The gain and noise figures at 10 GHz for both transistors are shown in Table 15. Although both transistors can be rated as high performance devices, the unbuffered device has larger gain and lower noise figure than the buffered one. This result indicates that presently available LPE buffer layers are inferior to high-quality SI substrate material for ion implantation purposes, in spite of the progress achieved in LPE technology.

It is important to compare epitaxial vs implanted transistors. Early comparisons between LPE and ion implanted transistors on this program favored the latter. Therefore, the main efforts in the later phases of this development have been devoted to realize ion implanted FETs. A similar comparison with VPE transistors was not possible because this technology was not available under this program. However, it is possible to draw conclustions from the rf performance of transistors made by Se implantation directly into a SI substrate, which was shown in Table 15 and is described for three frequencies (4,10 and 15 GHz) in Table 16. The rf performance of the ion implanted transistors shown in Table 16 is superior to that of LPE transistors fabricated under this contract, it is as good as that of the best 1μm gate commercially available devices, and it nearly matches the best performance reported for laboratory devices of similar geometry.[57]

From the above result, it can be concluded that MESFETs employing active layer fabricated by Se implantation into SI substrate are fully competitive to transistors made on epitaxial layers with respect to

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Table 15

Effect of a buffer layer on the rf performance of MESFETs fabricated by ion implantation.

	Max. Gain 10 GHz	Min. Noise Fig. 10 GHz	Assoc. Gain
940 LPE buffer layer	7.5 dB	3.5 dB	6.2 dB
1003 Cr doped melt grown substrate	14.0 dB	2.6 dB	8.0 dB

Table 16

RF performance of ion implanted MESFETs (#1003)

Frequency GHz	Max. Gain dB	Min.Noise Fig. dB	Assoc. Gain dB
4		1.4	14
10	14	2.6	8
15	12	3.4	7.5

rf performance. In addition, implanted transistors have shown to be less drift prone than epitaxial devices. Such advantage in device performance, and a potentially lower cost due to the high degree of uniformity and reproducibility, allow us to predict a wide use for ion implanted MESFETs. In addition, the ion implanted MESFET open exciting new possibilities for high-speed integrated circuits by combining the virtues of the excellent microwave response of the MESFET and a planar ion implantation technology with a high degree of uniformity. Switching speeds approaching 10 GHz are theoretically possible within power-speed products compatible with MSI. Alternatively, switching speed may be traded off for power dissipation to achieve LSI complexities at speeds about 1-2 GHz.

6.2 Determination of Material Parameters From Low Frequency Noise Measurements on IMPATT Diodes - Cornell University

At Cornell University, experimental measurements of avalanche diode parameters and of the classical ionization rates have resolved a long standing problem in the modeling of GaAs avalanche devices (see Sec. 6.3). These measurements show that the intrinsic avalanche response time, which is directly related to the rate of secondary pair production, is approximately an order of magnitude higher than expected theoretically, and that the classically determined ionization rates show an apparent dependence on the impurity concentration. The understanding of basic mechanisms, which has been achieved in this program, is that the hot electron distribution takes an unexpectedly long time to equilibriate, and it is believed that a limiting interband scattering time is the

responsible factor in delaying the acceleration of electrons to the threshold for ionization.

The technological importance of this understanding of basic mechanisms is that modeling and design techniques for developing high efficiency, high power devices must use a theoretical approach which contains an appropriate paramaterization. By the term "appropriate parameterization" it is meant that quantities such as the multiplication and the intrinsic response time must be experimentally determined for use in device optimization. It must be emphasized that theories which start from classically measured ionization rates and an electric field distribution are inappropriate for optimizing the design of GaAs avalanche devices. Finally, the 'Quasistatic Approximation' has been used to model the admittance and determine critical device parameters of GaAs avalanche devices.

An admittance model of GaAs flat profile IMPATTs and Read structures was developed using the 'Quasistatic Approximation" of Kuvas and Lee.[77] A unique feature of this theory is that it provides an analytic expression of the diode admittance in terms of physical parameters of the diode that are measurable at frequencies of a few hundred megahertz or less. It thus provides a framework for bypassing the calculation of M and τ_1 from the first principles, although such a calculation can be made for semiconductors for which the ionization rates can be represented as functions of the local electric field. Successful results are presented in modeling the microwave admittance of GaAs avalanche diodes and in identifying those material parameters responsible for performance limitations with particular emphasis on limiting the high temperature generation rate in high performance devices.

From various microwave measurements and from short circuit current fluctuation measurements over a frequency range of 30-400 MHz, we can determine the saturation current and the multiplication over the operating range of the diode, and can further obtain two independent measurements of the intrinsic response time τ_1. The two independent measurements of the intrinsic response time were deemed necessary because τ_1 in GaAs was found to be almost an order of magnitude larger than expected. Parallel measurements in silicon diodes were found to be in agreement with theoretically expected values. Perhaps the best reason for accepting this high value of the intrinsic response time is the fact that the microwave admittance of the diode can be modeled using measured parameters and the high measured value of τ_1. Thus, it is now apparent that a calculation that starts from the basic ionization rates will, at least implicitly, calculate a response time that is much too small to correspond to a real diode.

The essential physical reason for this high value of τ_1 can be found in the conduction band structure of GaAs. An examination of that band structure reveals that an electron accelerated in the $\langle 100 \rangle$ direction has to transfer to a higher conduction band in order to reach the threshold energy for ionization. An interband transfer time of the order of a picosecond could account for the high observed value of τ_1. Thus, considering the short transit time of an electron through the avalanche region, the distribution function does not equilibriate. A somewhat similar situation accounts for the velocity overshoot effect in the GaAs FET. This unexpected complication of the conduction band structure is also reflected in the ionization coefficient measurements (see Sec. 6.4).

Apart from understanding the physics of the diode, there is one outstanding material-fabrication problem illuminated by these measurements, and that is the high saturation current measured in all of the diodes reported on. Saturation currents of 0.1 A/cm^2 or greater are almost certainly the most important factor limiting the diodes high power performance.

(a) Theory

In studying the low frequency noise of steady p-n junction avalanches, Haitz pointed out the sensitivity of such measurements to the quality of the junction.[78] He showed that inhomogeneities over the surface of the diode tended to produce very irregular noise as a function of the bias current. Although a number of detailed analyses of noise have been made, the emphasis has been on the microwave performance of the diodes.[79-81] In addition, there have been several reports noting the proportionality of the low frequency noise to the reciprocal of the bias current for moderately large currents.[82,83] Experimentally, however, one observes the short circuit noise current to increase sharply at the onset of breakdown, reaching a peak at a few milliamperes, and then to decrease smoothly with increasing current if the diode is reasonably uniform. In a qualitative sense, one may understand the decreasing current fluctuations as being due to the compensating effects of space charge in the drift region. However, no attempt has been made to analyze the noise behavior as a function of current from the onset of breakdown to normal operating bias currents in order to extract useful parameters of the diode.

An analysis of the short circuit noise current is presented here, and it is shown how experimental data may be fitted to uniquely

determine the multiplication, M, and saturation current I_s, at the noise peak. Uniform diodes are shown to fit the theory very closely, and for mildly pathological diodes, these parameters can still be obtained with reasonable accuracy.

The total short circuit noise current may be written as the sum of three terms:

$$J_{total} = J_a + J(d_1) + j\epsilon\omega d_1, \qquad (10)$$

where J_a is the primary avalanche noise current, $J(d_1)$ is the additional current response of the avalanche caused by the voltage across the drift region, and $j\epsilon\omega d_1$ is the displacement current. d_1, the field fluctuation arising from the short circuit noise current in the drift region, is given by:

$$d_1 = -(1/\epsilon v_s w) \int_{x_1}^{w} [J_a+J(d_1)](w-x)\exp[-j\omega(x-x_1)/v_s]dx, \qquad (11)$$

where ϵ is the dielectric constant, ω is the angular frequency, v_s is the saturated drift velocity, w is the depletion width, and x_1 is the width of the avalanche zone. Eq. (11) is derived from the balance equation of Read.[84] For a double drift diode, Eq. (18) would be modified by the addition of a similar integral over the electron charge in a region (0, x_1') to the left of the avalanche zone.

Performing the integration in Eq. (11), one obtains:

$$\varepsilon\omega d_1 = j[J_a + J(d_1)](1-f)(1-x_1/w), \tag{12}$$

where the transit angle delay is given by:

$$f = [\sin\psi - j(1 - \cos\psi)]/\psi, \tag{13}$$

and ψ is the transit angle of carriers in the drift region. The avalanche current generated in response to the ac field d_1 is:

$$J(d_1) = \varepsilon\omega_1\beta\theta/(1 + j\theta) , \tag{14}$$

where in the notation of the "quasi-static" approximation

$$\beta = MJ_s|a_1|/\varepsilon\omega^2, \; a_1 = \partial(1/M\tau_1)/\partial\xi_c, \text{ and } \theta = M\omega\tau_1 .$$

Substituting Eq. (14) into (12) gives the avalanche field perturbation caused by the primary noise current:

$$\varepsilon\omega d_1 = j(1-f)J_a/[1 - j(1-f)\beta\theta(1-x_1/w)/(1+j\theta)]. \tag{15}$$

The total short current noise current is then given by:

$$J_{total} = J_a\{(1+j\theta)[f(1-x_1/w)+(x_1/w)]/[1+J\theta-j(1-f)\beta\theta(1-x_1/w)]\} . \tag{16}$$

Taking the mean square value of J_{total}, one obtains in the limit of small transit angle:

$$<i^2> = <i_a^2>[(1+\theta^2)[1-\psi^2(1+3x_1/w)(1-x_1/w)/12]/$$
$$\{[1+\beta\theta\psi(1-x_1/w)/2]^2+\theta^2[1-\beta\psi^2(1-x_1/w)/3]\}] \quad , \quad (17)$$

where the mean square primary avalanche noise current is taken from Naqvi:[85]

$$<i_a^2> = 2eI_{sn}M_n^3\Delta f[1-(1-k)(1-M_n^{-1})^2]/(1+\theta^2)$$
$$+2eI_{sp}M_p^3\Delta f[1-(1-k^{-1})(1-M_p^{-1})^2]/(1+\theta^2) \quad . \quad (18)$$

k, the ratio of the hole and electron ionization coefficients, is assumed to be unity throughout the remainder of the discussion. This is justified by the fact that the multiplication at the peak is independent of k, so that fitting to experimental data will not be affected by this assumption.
Eq. (17) now takes the form:

$$<i^2> = 2eI_sM^3\Delta f[1-\psi^2(1+3x_1/w)(1-x_1/w)/12]/$$
$$\{[1+\beta\theta\psi(1-x_1/w)/2]^2+\theta^2[1-\beta\psi^2(1-x_1/w)/3]\} \quad , \quad (19)$$

which in the limit of small current reduces to:

$$\lim_{I\to 0}<i^2> = 2eI_sM^3\Delta f[1-\psi^2(1+3x_1/w)(1-x_1/w)/12]/(1+\theta^2) \quad (20)$$

For large current Eq. (17) becomes:

$$\lim_{I\to\infty} <i^2> = 8e\varepsilon^2v_s^2A^2\Delta f/I|a_1|^2\tau_1^2(w-x_1)^2(1-x_1/w)^2 \quad (21)$$

Note that the short circuit noise current is inversely proportional to the dc current, $I = MI_s$, and the slope is given by:

$$B = 8e\varepsilon^2 v_s^2 A^2 \Delta f / |a_1|^2 \tau_1^2 (w - x_1)^2 (1 - x_1/w)^2 \quad , \tag{22}$$

where A is the area of the diode.

In order to discuss fitting Eq. (19) to experimental data, it is convenient to explicitly introduce the bias current:

$$\langle i^2 \rangle = a' I^3 / [(1 + b' I^2)^2 + c' I^2 (1 - d' I)] \quad , \tag{23}$$

where

$$a' = 2e\Delta f / I_s^2 \tag{24}$$

$$b' = (a'/B)^{1/2} \tag{25}$$

$$c' = (\omega\tau_1 / I_s)^2 \tag{26}$$

$$d' = 2\psi b' / 3c'^{1/2} \tag{27}$$

Differentiating Eq. (23) with respect to the current and setting the result equal to zero, one obtains:

$$b' I^2 = (1 + c'/2b') + [(1 + c'/2b')^2 + 3]^{1/2} \tag{28}$$

By taking the noise measurements at a sufficiently low frequency, one can always make $c'/2b'$ negligible. Thus,

$$b' I_{pk}^2 = 3 \tag{29}$$

at the noise peak. And, since b' is inversely proportional to I_s, one comes to the result that $I_{pk} M_{pk}$ is a constant which can be evaluated from the high current limit in Eq. (21):

$$I_{pk}M_{pk} = 3(B/2e\Delta f)^{1/2} \quad . \tag{30}$$

Multiplication and saturation current can be extracted from experimental data using the slope of $\langle i^2 \rangle$ versus (1/I) to obtain the product in Eq. (30). Since I_{pk} is experimentally determined, M_{pk} and I_s at the peak are known. Eq. (23) can then be used to describe the mean square short circuit avalanche noise current over the entire range of bias current.

(b) Experiment

The mean square short circuit avalanche noise current of several IMPATT diode structures has been measured at 30 MHz as a function of dc current using the experimental setup shown in Fig. 81a. The diode noise equivalent circuit shown in Fig. 81b is assumed, where the thermal resistance R_{th} and spreading resistance R_{sp} are negligible at 30 MHz. Since the space charge resistance R_{sc} is typically 20 ohms or greater, choosing the load resistance R_L equal to 0.2 ohm closely approximates a short circuit. This greatly simplifies interpretation of the experimental data since measurement of the diode impedance is not required. Calibration of the system is achieved by substituting a signal generator for the IMPATT diode noise source.

An example of the experimental noise behavior typical of a uniform avalanche is presented in Fig. 82. The diode is a silicon X-band IMPATT. At moderately high current the short circuit noise varies inversely as I, and at low current there are no pronounced irregularities in the noise data. One would expect that silicon would be more uniform than GaAs, and thus fit the theory more closely. This is indeed the case, as seen in the figure. The saturation current density is approximately .007 A/cm^2, and, although this is a low value for silicon IMPATTs, it is still about three orders of magnitude

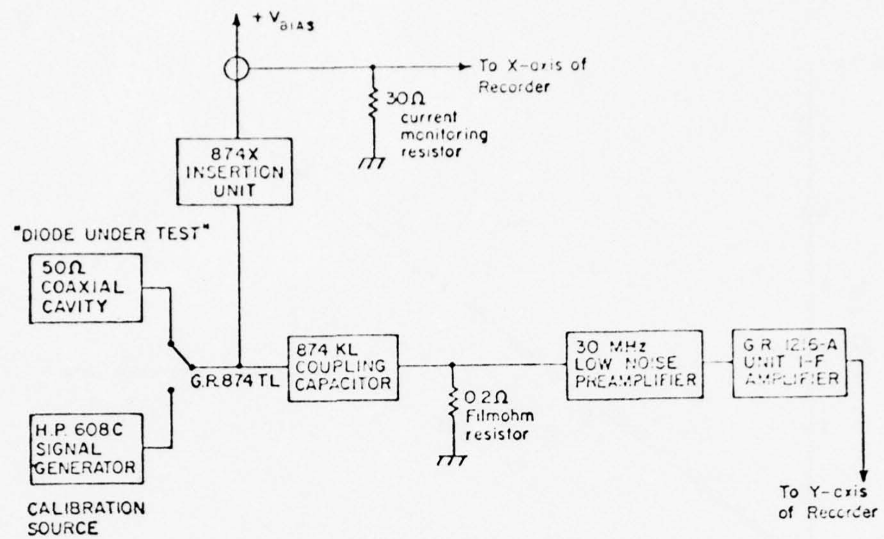


Fig. 81a Experimental setup

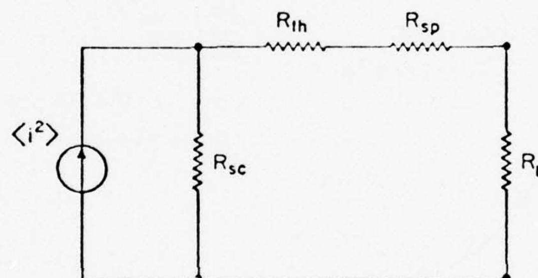
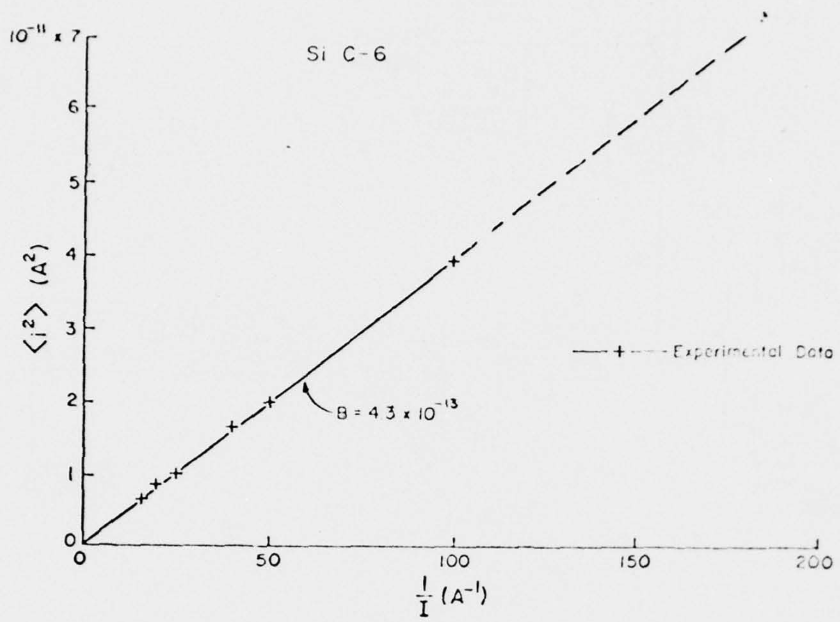


Fig. 81b Noise equivalent circuit



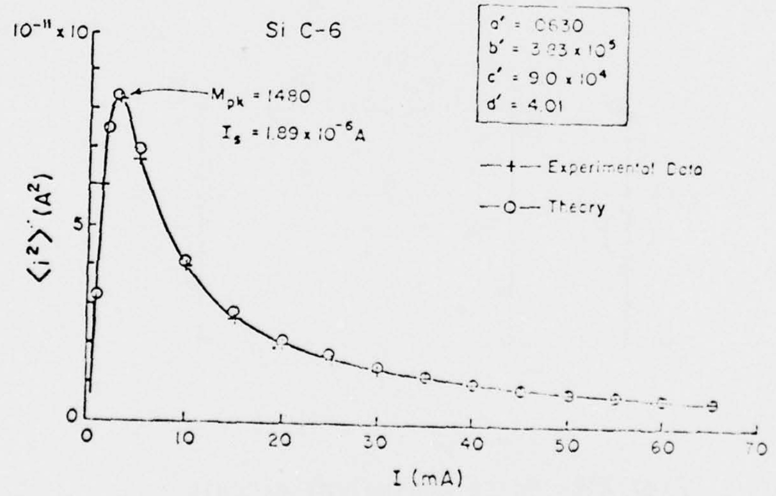
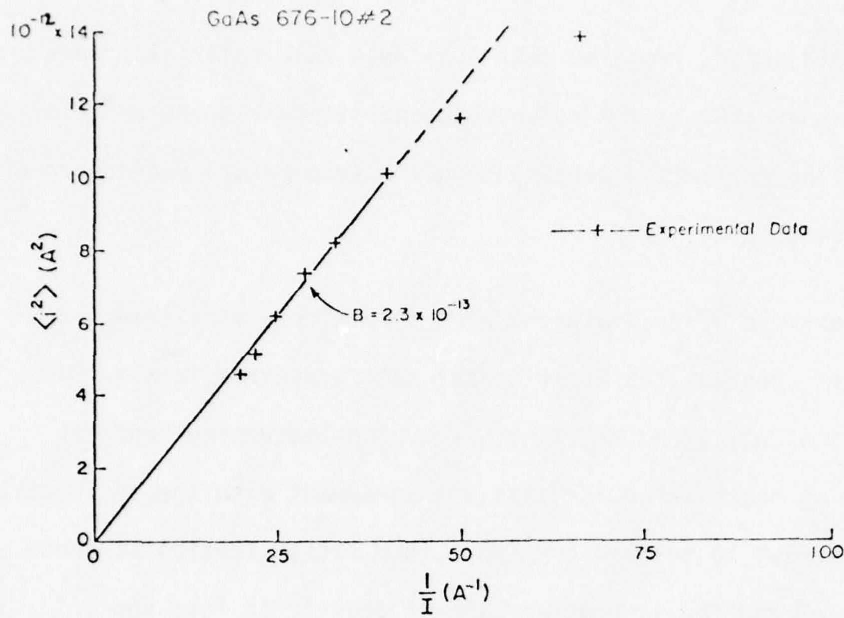


Fig. 82 Fit of the experimental short circuit current noise data of a uniform silicon IMPATT by Eq. (30).

higher than one would expect from the best available bulk material. The multiplication is about 1500 at the noise peak,and it may rise an order of magnitude at operating currents depending upon the temperature dependence of the saturation current.

As an example of an avalanche with some microplasma irregularities at low current,consider the experimental data presented in Fig. 83. The diode is a C-band GaAs Read IMPATT with low-high-low doping profile. Note that in spite of these irregularities,the agreement with theory is still quite good. In contrast to the silicon diode, the multiplication is about 440 at the noise peak,and the saturation current density is four and one half times larger. The relatively high saturation current appears to result in lower noise, however.

Several diodes of both materials displayed an anomolous high current noise behavior,as shown in Fig. 84 for three silicon IMPATTs. Although the noise current varies inversely as I in all cases, the intercept is observed to deviate from the origin. This deviation may be the result of "excess" noise in the case of Si 2-22,and a current component which is not multiplied by the avalanche in the case of Si N3-AA. Since a slope is unambiguously defined in any event, the theory can still be applied to obtain a reasonable estimate of the multiplication and saturation current. As an example of the type of fit which can be obtained, consider the data presented in Fig. 85 for a flat doping profile GaAs IMPATT. The intercept of a plot of $\langle i^2 \rangle$ versus (1/I) is observed to intersect the (1/I) axis. Leakage current is believed to be responsible for the anomolous high current behavior in this case, since no avalanche noise is observed for this diode



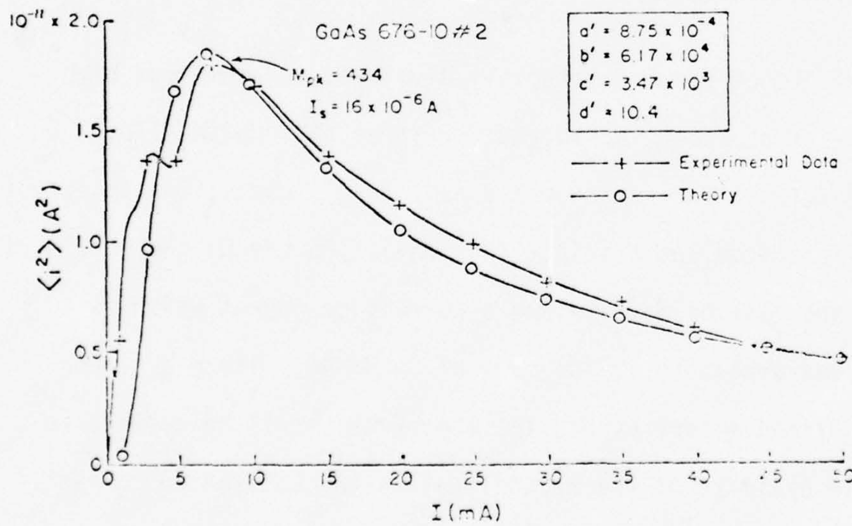


Fig. 83 Short circuit noise current at 30 MGz of a C-band, hard punch-on, LO-HI-LO, GaAs Read structure showing evidence of microplasmas.

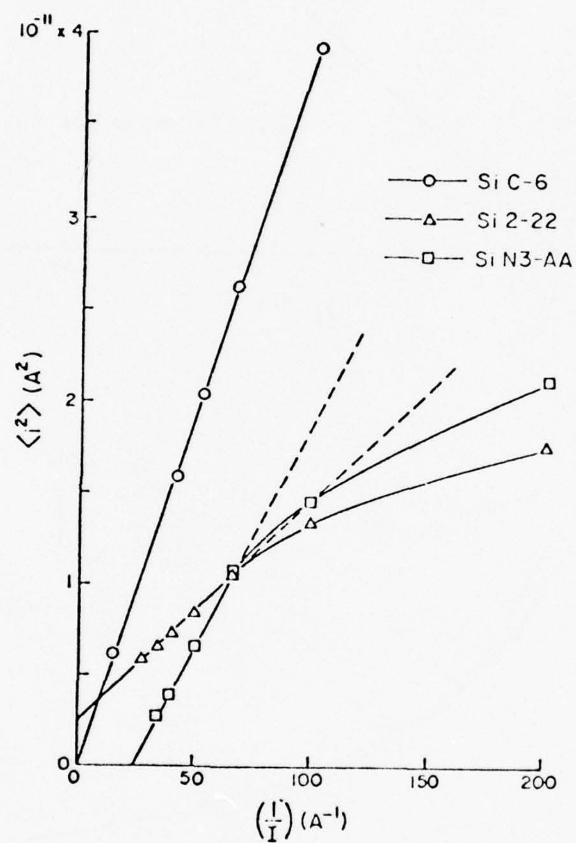
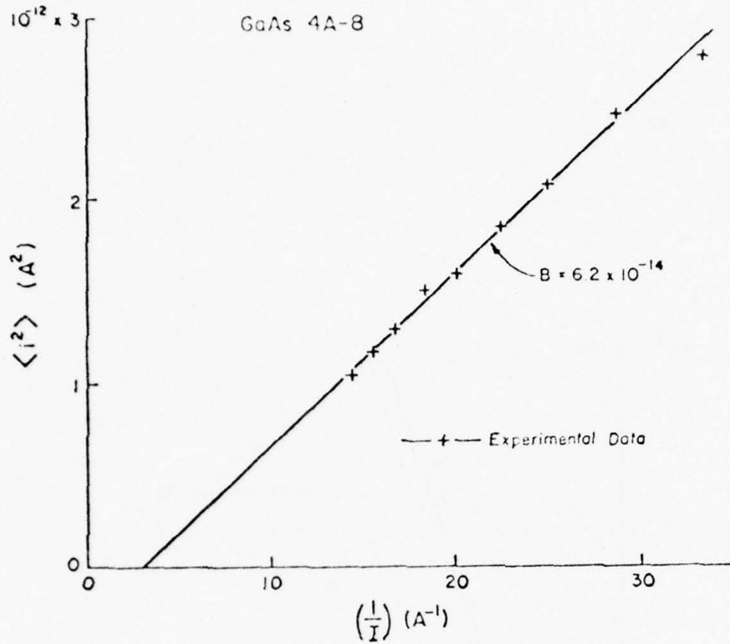


Fig. 84 Comparison of high current noise behavior



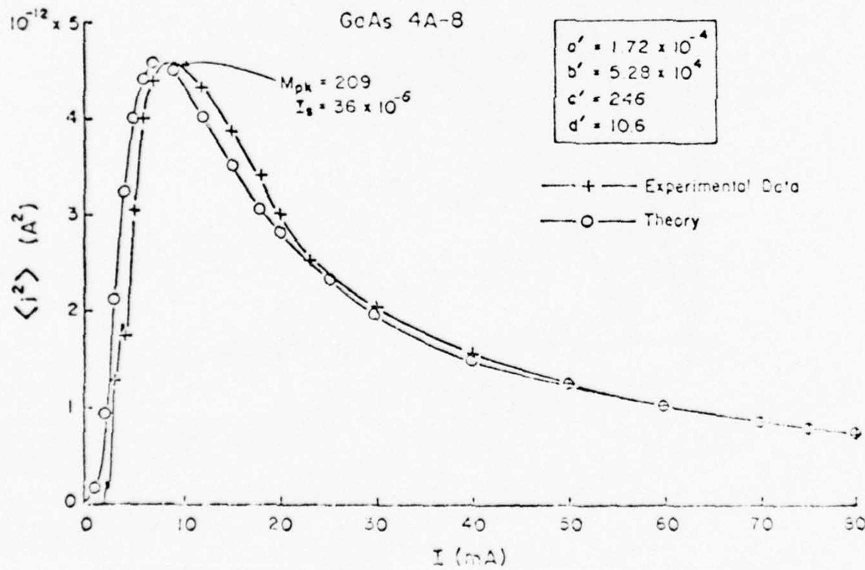


Fig. 85 Short circuit current noise data and theoretical fit of Eq. (30) for a GaAs flat profile IMPATT; for this diode $M_{pk} \approx 200$ and the saturation current is an order of magnitude larger than that of the silicon diode shown in Fig. 82

up to 3 mA of reverse bias current. The theoretical fit based on the experimental slope is still very close. Table 17 presents a summary of results obtained by applying the theory to experimental data.

The results clearly show that M is sufficiently low for many avalanche structures to significantly alter their microwave performance. For values of multiplication much less than 1000, it can be shown that the phase angle by which the particle current lags the avalanche excitation is less than 90 degrees. This degrades the diode negative conductance and shifts the avalanche resonance to a higher frequency.[86] In addition, low values of multiplication may make the diode unstable with respect to thermal runaway.

A tacit question that has not been addressed explicitly is how the multiplication and saturation current characteristic of the operating range of the diode are related to the values obtained at the noise peak. A related question is why the large variation in junction temperature seemingly does not effect the fitting of the experimental curves. The answer to both of these questions lies in the fact that very quickly after the noise peak is past the mean square current fluctuations become proportional to the reciprocal of the bias current. Thus only the product of the strongly temperature dependent multiplication and saturation current can be observed. The only other strongly temperature dependent parameter is the scattering limited velocity and its temperature dependence is not strong enough to seriously affect the fitting of the experimental curves.

Table 17

Summary of IMPATT Data

	Diode	M_{pk}	$I_s (\mu A)$
Silicon	c-6 (flat profile)	1480	1.89
	2-22 (flat profile)	1470	0.95
	N-3AA (I^2HL)	616	8.0
GaAs	676-10#2 (LHL)	434	16.0
	4-A8 (flat profile)	209	36.1
	666 (I^2HL)	112	204.0

An explicit picture of how the multiplication and saturation current vary over the operating range of the diode can be obtained utilizing the results of the noise analysis. If one assumes that at the noise peak the junction temperature is essentially at room temperature, the junction temperature at higher bias currents can be calculated from the thermal impedance of the mount and the electrical dissipation. The particular temperature dependence of the saturation current can be separately measured below breakdown so that the saturation current as a function of the bias current can be calculated. Dividing the bias current by the saturation current then yields the multiplication. The results of such a calculation are shown in Fig. 86 for one of the silicon diodes. Although the multiplication is relatively high at low bias currents, it falls to a value less than a hundred at a bias corresponding to approximately half its rated power output.

The intrinsic response time of the avalanche has a negligible effect upon the noise measurements at 30 MHz. At higher frequencies the effect of τ_1 is to reduce the noise monotonically. The analytical determination of the intrinsic response time is relatively simple. An expression was previously derived for the short circuit noise current in an avalanching diode, Eq. (23). Examination of Eq. (23) shows that the only frequency dependent term is c'; the intrinsic response time is obtained by merely inverting Eq. (23) and differentiating with respect to ω^2,

$$\tau_1^2 = \frac{a''I}{(1 - d'I)} \frac{d}{d\omega^2} \left(\frac{1}{\langle i^2 \rangle} \right) , \qquad (31)$$

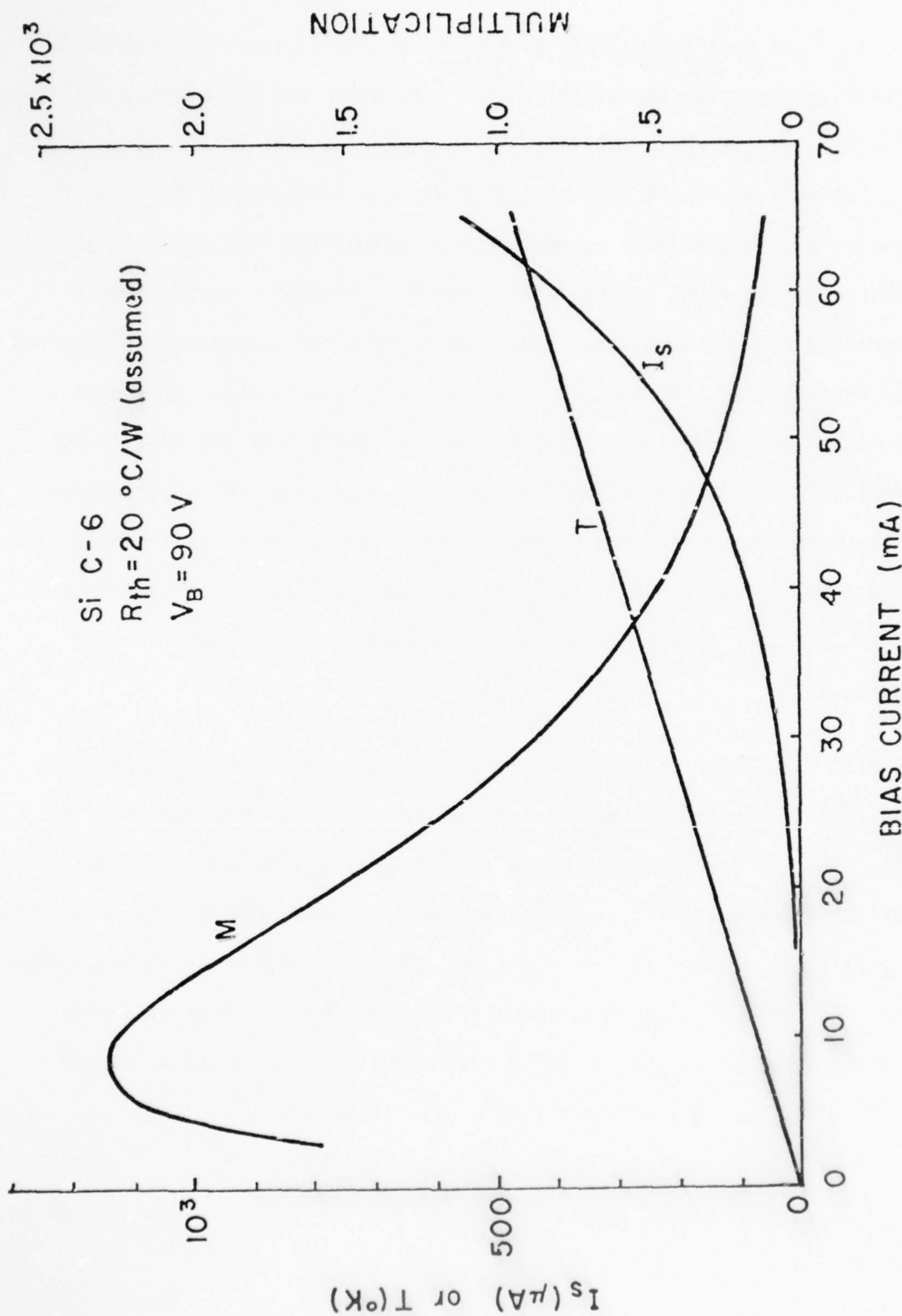


Fig. 86 Variation of multiplication and saturation current in an IMPATT diode as a function of the bias current

where $a'' = 2e\Delta f$. The change in Eq. (23) with frequency is illustrated in Fig. 87 where an intrinsic response time of 3 ps has been assumed.

The following two graphs, Figs. 88 and 89 show recorder tracings of the short circuit noise current of a silicon diode at 20 and 420 MHz. Applying Eq. (31) to the data of Figs. 88 and 89 yields an intrinsic response time of 4 ps. A numerical calculation of the intrinsic response time using the "Quasistatic" approximation[76] gives $\tau_1 = 2.7$ ps without taking into account high field diffusion effects. Including diffusion would increase the response time giving reasonable agreement between theory and experiment. Having shown reasonable agreement in silicon it is now possible to proceed to the data on GaAs diodes,where it will be seen that although the parameters derived from the noise and microwave admittance measurements are in good agreement,the measured intrinsic response time is much higher than theoretical estimates.

Figure 90 shows the short circuit noise current at 30 and 420 MHz for a flat profile GaAs C-band diode. The intrinsic response time derived from this data gives $\tau_1 = 15.1$ ps. Qualitatively one can see that the steeper field dependence of the ionization rates in GaAs,which reduces the effective avalanche width in a flat profile diode by almost a factor of four,will give a calculated response time of a picosecond or less. Thus the discrepancy between experiment and theory is quite large. In Sec. 6.4 on ionization rates a new phenomenon is discussed that is probably responsible for this discrepancy in the intrinsic response times.

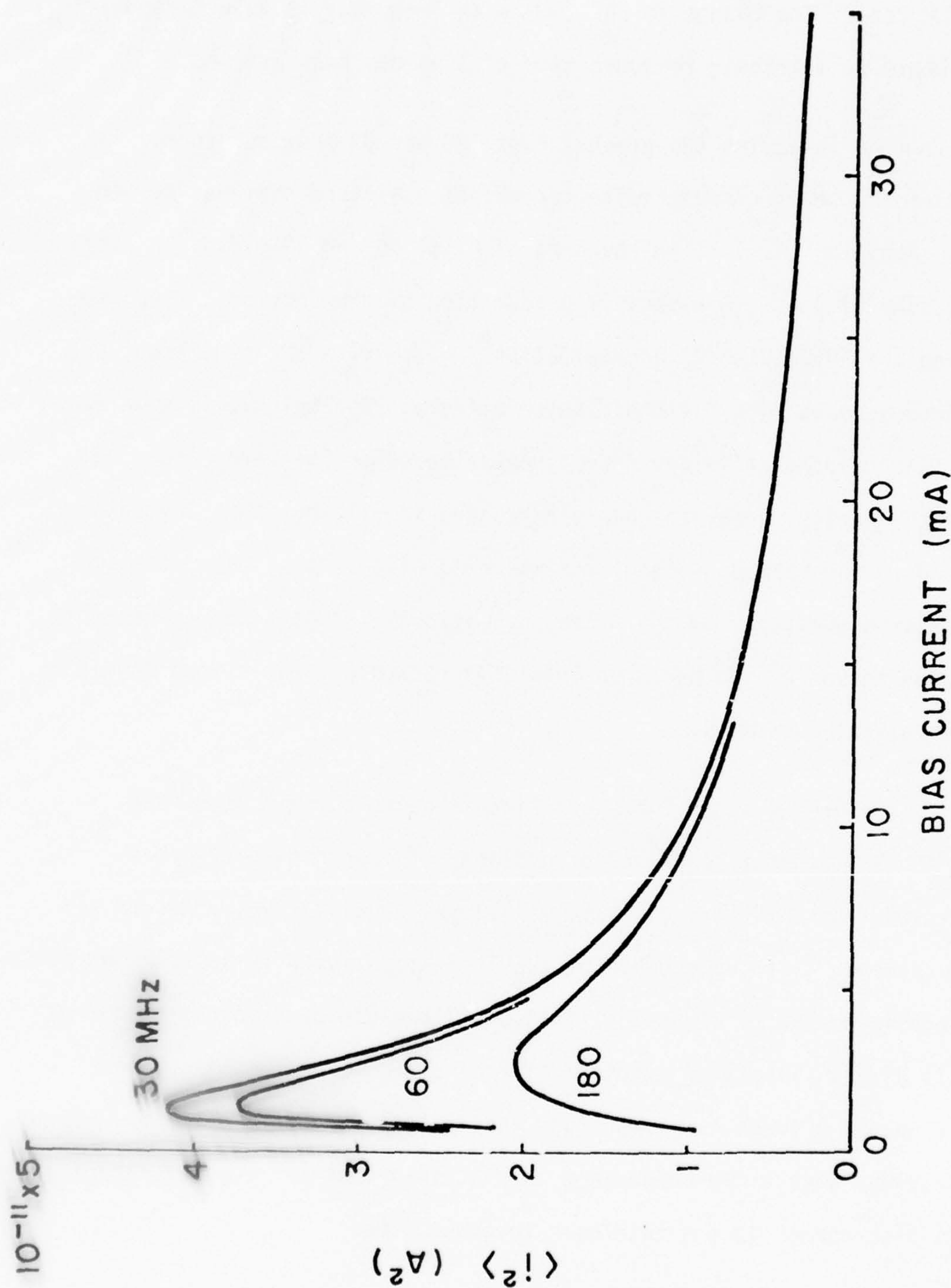


Fig. 87 Calculated mean square current fluctuation vs bias current for 30, 60, and 180 MHz.

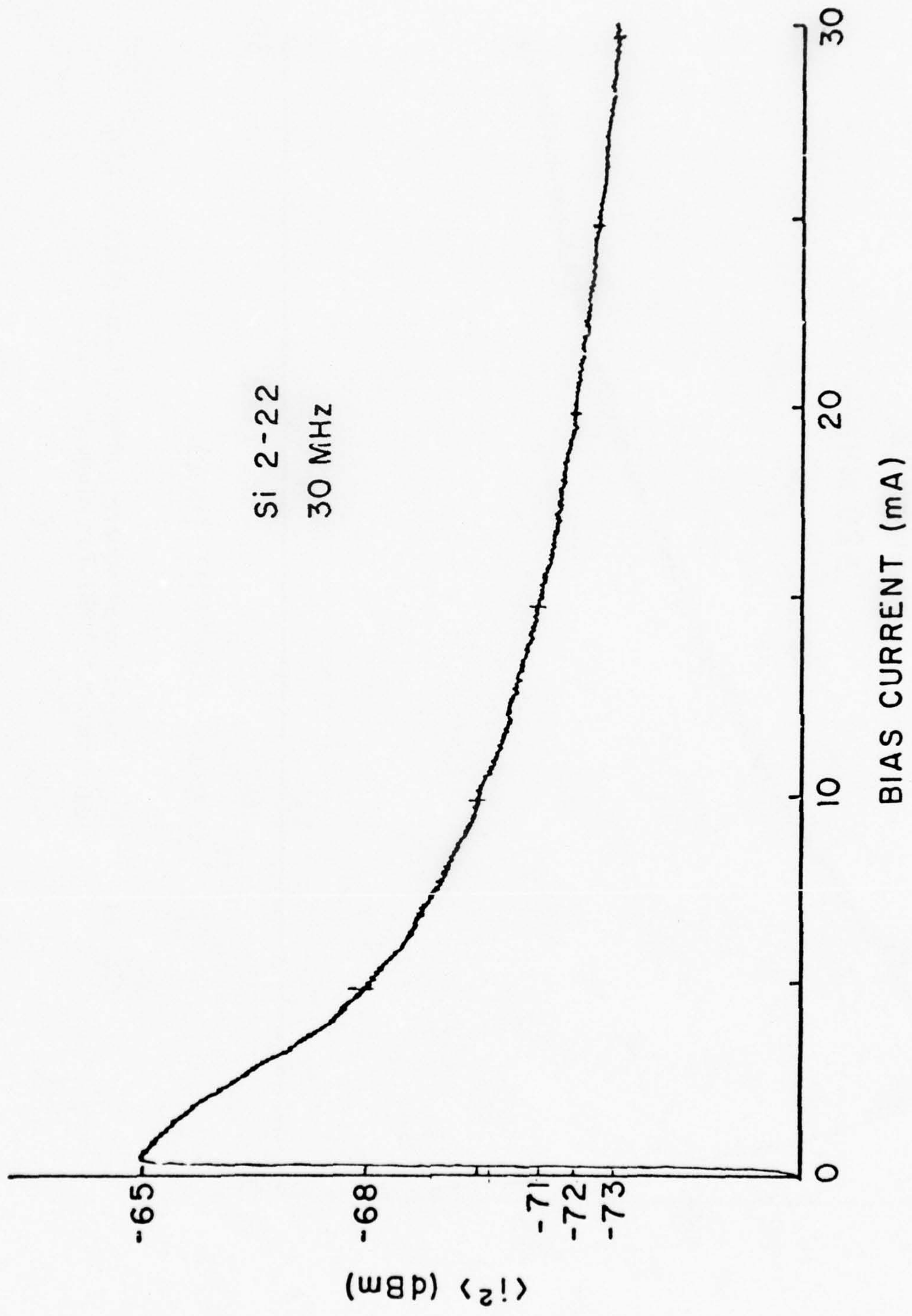


Fig. 88 Experimental mean square current fluctuation vs bias current at 30 MHz for diode Si 2-22

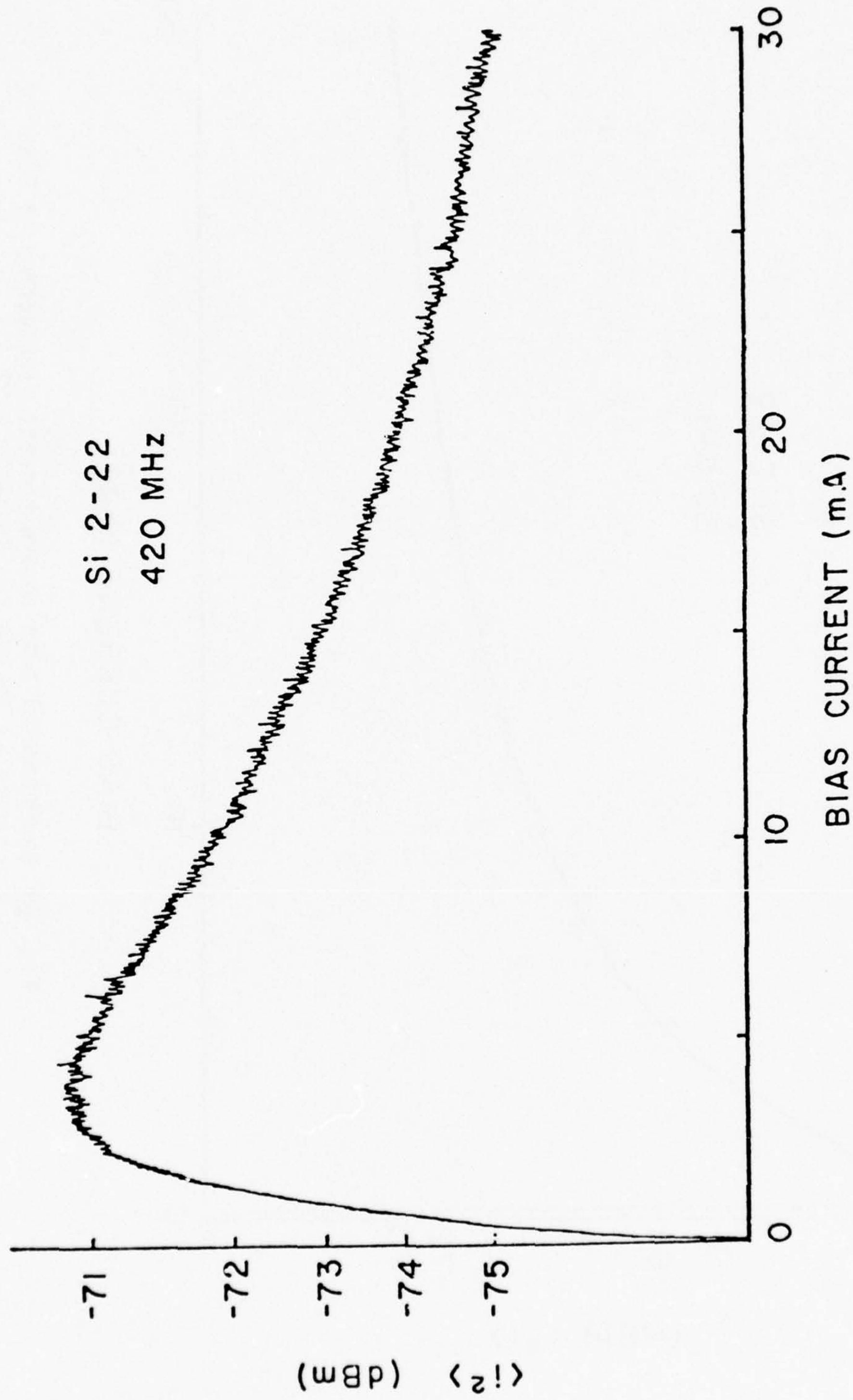


Fig. 89 Experimental mean square current fluctuation vs bias current at 420 MHz for diode Si 2-22

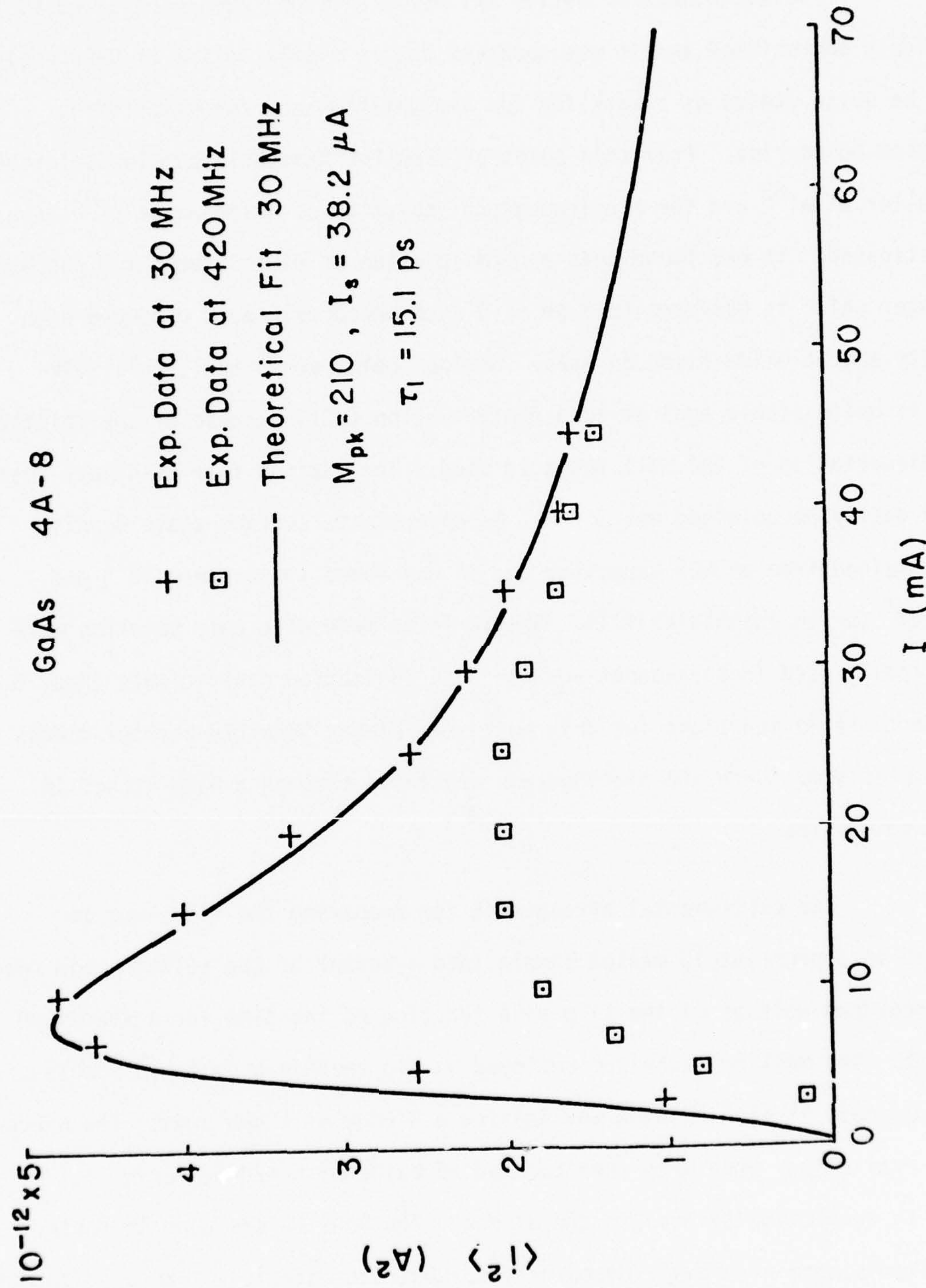


Fig. 90 Short circuit current noise of a flat profile GaAs diode vs bias current at 30 and 420 MHz

6.3 Electrolytic Oxidation and Etching Techniques – Cornell University

The usefulness of native oxides in silicon integrated circuits is widely appreciated, and it was apparent that a similar oxide of GaAs would also be quite useful as a mask for ion implantation and for stabilizing junction boundaries. From this point of view, the N-methylacetamide solution of Muller et al[63] and the ethylene glycol solution of Hasegawa et al[87] were investigated. It was found that a 0.1M solution of dibasic ammonium phosphate in water which is buffered to a pH of 4 with phosphoric acid produced high quality anodic oxide films on GaAs. Besides being economical, this solution is quite stable against acid contamination (HCl) because of the relatively low dissociation of the salt and acid used. The maximum film thickness that could easily be obtained was 3600Å. An approximate surface state density was obtained from an MOS capacitor, and it was found lie between 10^{11} and $10^{12}/cm^2$ for an unannealed film. Anodic films made with this solution were principally used in subsequent work on GaAs ionization coefficients (Sec. 6.4). The most stable junctions for this work were planar Schottky barrier diodes using platinum. Here the platinum was sputtered through a hole etched in the anodic oxide.

The experimental arrangement for preparing the films was to immerse an appropriately masked sample into a beaker of the solution and record the breakdown voltage of the film as a function of the time for a specified current. The masking technique employed was to anodize a polished sample of GaAs and mask it with Apiezon wax leaving a window of known area. The window and a contacting area were then cleared of oxide with hydrochloric acid prior to anodizing the area in the window. The GaAs wafers used in these experiments were of heavily doped n-type substrate material. The anodization

was carried out with the sample illuminated by a microscope lamp which served to reduce the contact potentials, but was otherwise not deemed necessary to obtaining good anodic films.

The first films were formed in an unbuffered solution (pH≈7). The cell voltage versus time for several current densities is shown in Fig.91. Note that for the lowest current density the cell voltage does not increase linearly with time, indicating a slight dissolution of the oxide. An oxide film of several thousand Angstroms was observed to dissolve if left overnight in the unbuffered solution.

Buffering the solution to a pH of 4 with phosphoric acid reduces the solubility of the film to a completely negligible value. The cell voltage versus time for this buffered solution, as also shown in Fig. 91 for 0.3 mA/cm^2, is quite linear down to the lowest measured current densities (~ $20 \mu A/cm^2$). Figure 92 shows that the rate at which the oxide film is formed is linearly proportional to the current density although the rate changed with solution concentration. Film thickness was measured by a Zeiss interference microscope and it agreed with published data.[87,88] The breakdown field in the oxide was observed to be at least $5 \times 10^6 V/cm$. Somewhat thicker films could be grown in a boiling solution as has been described by Spitzer, et al.[89]

An electrolytic etching technique has been developed to thin down the substrate for ionization rate measurements to 10-20μm to permit the injection of minority carriers into the substrate side of the diode. In this case a 1:4 solution of perchloric:acetic acid was used.[90] At a current density of 0.3-0.4A/cm^2 and a cell voltage of 20-30 volts a brightly polished

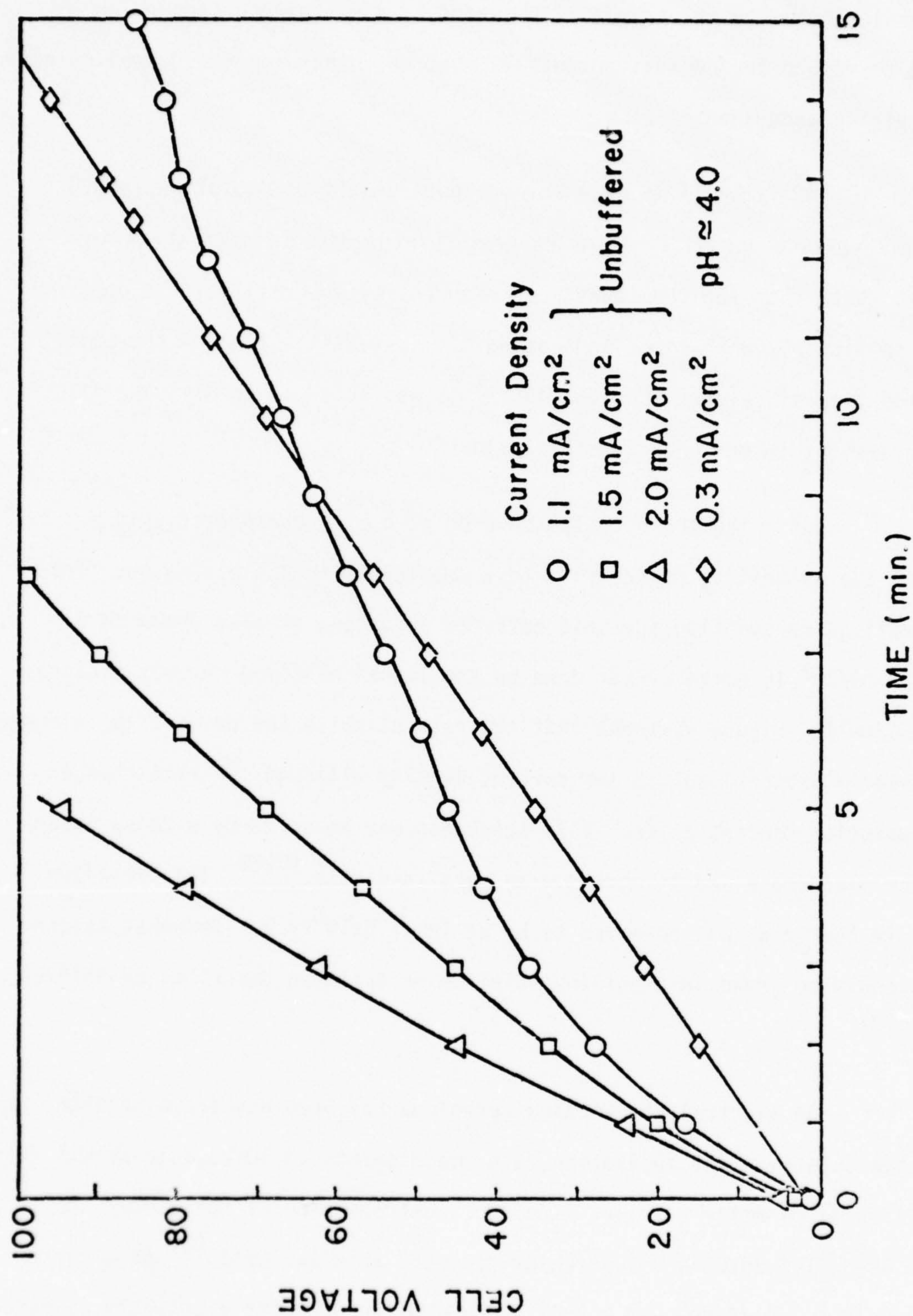


Fig. 91 Cell voltage vs time as a function of current density for buffered and unbuffered solutions

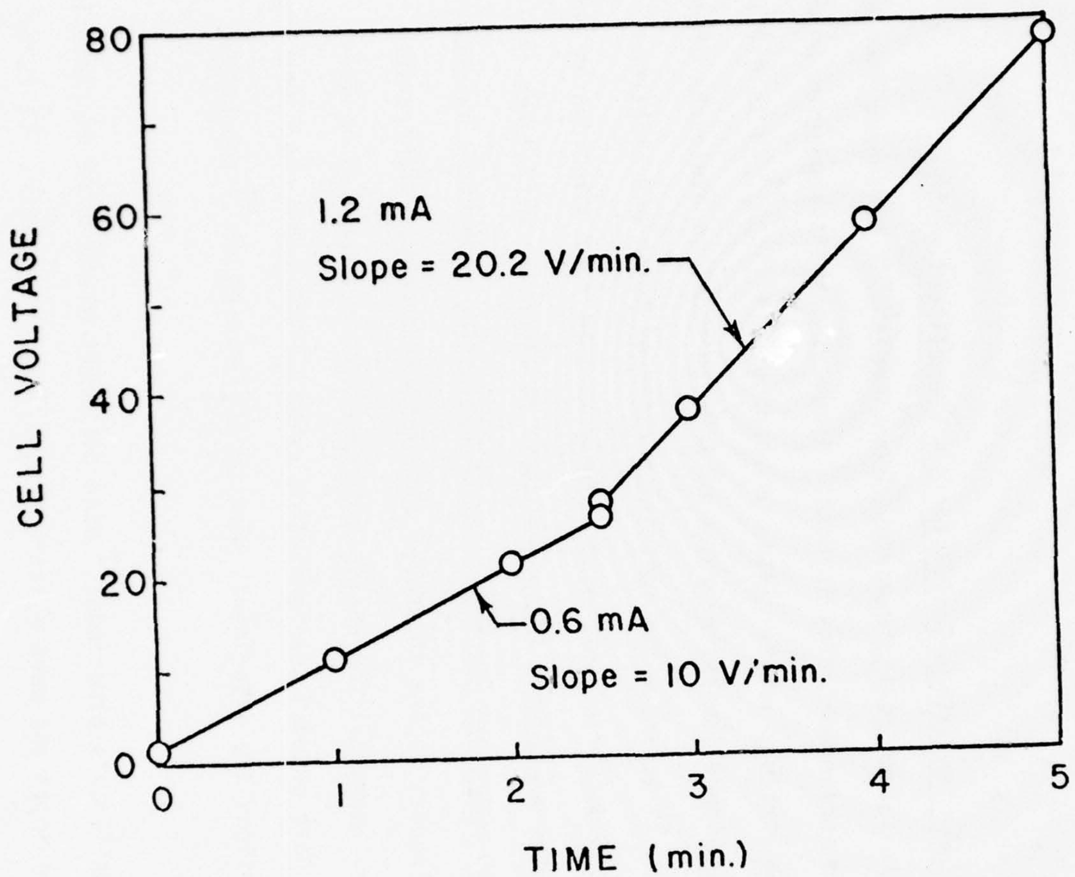


Fig. 92 Cell voltage vs. time showing the direct proportionality of film growth rate to current density for a buffered solution.

etched surface was obtained. By means of pulse etching, very fine control can be obtained, so that the substrate can be completely etched away from the lightly doped epitaxial layer permitting direct examination of the interface.

6.4 GaAs Ionization Coefficients - Cornell University

In recent years, numerious experiments[91-93] have been done on measuring the ionization rates in GaAs. However, the discrepancies among data are uncomfortably large. Also, as opposed to silicon,[94] it is difficult to use the published ionization rates of GaAs to model an avalanche diode successfully. In general, the ionization rates of holes and electrons inside a semiconductor are not equal. Only in some rare coincidences the ionization rates are equal; these are cases in which the difference in energy loss by holes and electrons due to scattering mechanisms balance out the differences in the threshold energies for secondary ionization. Unfortunately, among all the analyses of experiments conducted on GaAs most of them have assumed the ionization rates of holes and electrons are equal. Exceptions are experiments done by Stillman et al.[93] and Logan et al.[91]

Stillman's experiment[93] used different wavelengths of radiation to inject pure holes and pure electrons in a Schottky barrier. It is by far the best method to produce pure carrier injection. However, the breakdown voltages predicted by his ionization rates are lower than the experi-

mentally observed ones. On the other hand, Logan's experiments[91] used complementary junction pairs (p^+n and n^+p) to measure M_n and M_p separately. Besides the fact that the scattering environments are different in different junctions, the field profiles are completely turned around. Since $M_n(v)$ will not be the same in p^+n and n^+p junctions, with exact mirror image field distribution, it is difficult to infer $M_n \simeq M_p$ as indicated in these experimentally observed breakdown voltages and those predicted by their measured ionization rates[91]. (38V observed breakdown versus 66V calculated from their α and β for $N_d = 1\times10^{16}cm^{-3}$.)

In the present experiment, a wide doping range (2.9×10^{15} - $5.1\times10^{16}cm^{-3}$) has been examined and attempts have been made to present ionization rates determined at multiplication values of $1 \lesssim M \lesssim 3$ that are consistent with the observed breakdown voltages. Data which are not consistent in this regard are not used. Special efforts have been made to produce pure hole and pure electron injection in the same junction. Care was taken that the measurements made on diodes were free from microplasmas and strong field inhomogeneity. Since the deduction of the ionization rates α and β involve differentiation of the experimental multiplication curves, the effect of noise is amplified. The accuracy of α and β can be greatly improved by recalculating M_n and M_p to match the experimental curves. A good agreement between the two implies the α and β calculated are selfconsistent with the experimental data. Finally, using the adjusted ionization rates, the breakdown voltages were projected and they were compared with the breakdown voltages observed on a curve tracer.

Baraff theoretically calculated the ionization coefficients using a generalized distribution function[95]. The assumptions in his calculation included isotropic energy dependent scatterings, energy independent mean free path for phonon collisions, and simple parabolic conduction bands. The fact that the ionization rates of electrons α and holes β cross over as observed in the present experiment cannot be predicted by Baraff's theory, has led to consideration of interband scattering which limits the effective electron ionization rate in narrow junctions. Anderson and Crowell[96] predicted that the ionization threshold energy for electrons in <100> GaAs is 2.1eV, which according to Cohen and Bergstresser[97], lies in the second conduction band. Thus an electron accelerated in the 100 direction must undergo a transition to the second conduction band in order to reach the threshold energy for ionization. A qualitative explanation of the effect of this scattering will be given. Also a discussion on the difficulties and uncertainties of the experiment will be presented.

(a) Theory

The deduction of ionization coefficients α and β from multiplication data M_n and M_p are not straightforward. They involve the difficulties in solving the integral equations. McKay[98] used the Townsend theories of avalanche breakdown in gases to derive the avalanche process in semiconductor. He assumed the ionization coefficients of holes and electrons are the same and calculated the ionization rates for linear and parabolic field distributions. Miller[99] considered the general case that $\alpha \neq \beta$ with a linear field

distribution. The equations which give consistency in field distribution are given by Lee et al[94]:

$$1 - \frac{1}{M_n} = \int_0^w \alpha \exp\left[-\int_0^x (\alpha - \beta) dx' \right] dx \qquad (32)$$

$$1 - \frac{1}{M_p} = \int_0^w \beta \exp\left[\int_x^w (\alpha - \beta) dx' \right] dx \qquad (33)$$

$$\ln \frac{M_n}{M_p} = \int_0^w (\alpha - \beta) dx \qquad (34)$$

where M_n = multiplication with pure electron injection

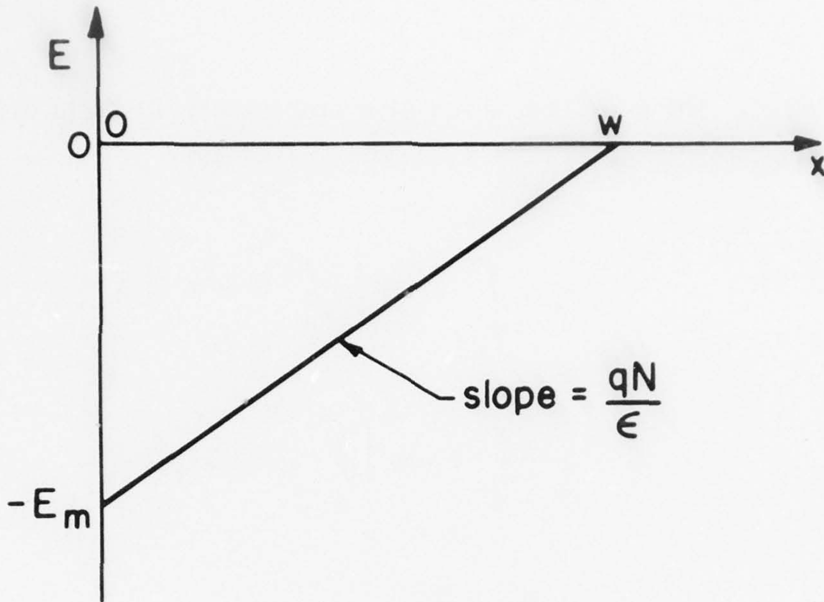
M_p = multiplication with pure hole injection

α = ionization coefficient of electrons

β = ionization coefficient of holes

w = depeltion width of a one sided abrupt junction.

Only the punch-through and non-punch-through one-sided abrupt junctions will be considered in the following. For the linear field distribution of step junctions in n-type diodes, the boundary conditions in Fig. 93a were used. The relations of $\alpha(E_m)$ and $\beta(E_m)$ with M_n and M_p can be deduced from equations (32), (33) and (34):



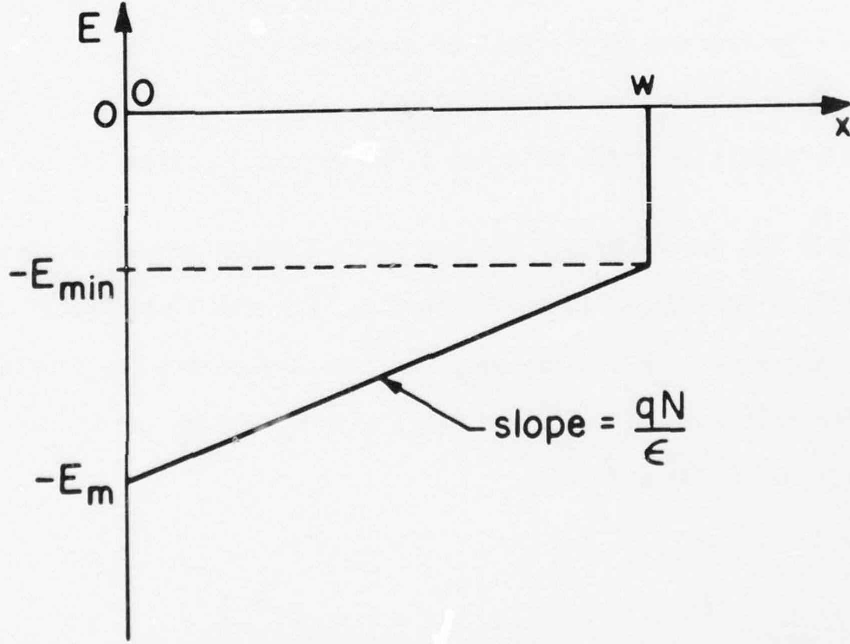


Fig. 93 (a) Boundary conditions, for the non-punch-through diodes, (b) for the punch-through diodes

$$\alpha(E_m) = E_m \left[\frac{d(\ln M_n)}{dV} - \frac{M_n - 1}{M_n} \cdot \frac{d(\ln M_p)}{dV} \right] \quad (35)$$

$$\beta(E_m) = \frac{E_m}{M_n} \frac{d(\ln M_p)}{dV} \quad (36)$$

where E_m = maximum electric field.

For the punch-through case, the boundary conditions are shown in Fig. 93b. The relations of $\alpha(E_m)$ and $\beta(E_m)$ with M_n and M_p are:

$$\alpha(E_m) = \frac{qNw}{\varepsilon} \left[\frac{d(\ln M_n)}{dV} - \frac{M_n - 1}{M_n} \cdot \frac{d(\ln M_p)}{dV} \right] + \frac{M_p}{M_n} \alpha(E_{min}) + \frac{M_n - 1}{M_n} \cdot [\alpha(E_{min}) - \beta(E_{min})] \quad (37)$$

$$\beta(E_m) = \frac{qNw}{\varepsilon} \frac{1}{M_n} \frac{d(\ln M_p)}{dV} + \frac{M_p}{M_n} \beta(E_{min}) + \frac{M_p - 1}{M_n} . [\alpha(E_{min}) - \beta(E_{min})] \quad (38)$$

where $E_{min} = E_m - \frac{qNw}{\varepsilon}$ = minimum electric field. For practical purposes, $\alpha(E_{min})$ and $\beta(E_{min})$ were neglected. Since in all the experiments conducted $E_m - E_{min}$ were at least 1×10^5 V/cm, α and β would be at least two orders of magnitude down. Neglecting $\alpha(E_{min})$ and $\beta(E_{min})$, one obtains for the punch-through case:

$$\alpha(E_m) = \frac{qNw}{\varepsilon} \left[\frac{d(\ln M_n)}{dV} - \frac{M_n - 1}{M_n} \frac{d(\ln M_p)}{dV} \right] \quad (39)$$

$$\beta(E_m) = \frac{qNw}{\varepsilon} \frac{1}{M_n} \frac{d(\ln M_p)}{dV} . \quad (40)$$

It is obvious that equations (39) and (40) can be applied only when the electric field punches through before any observable multiplication occurs. If neglecting $\alpha(E_{min})$ and $\beta(E_{min})$ in equations (37) and (38) is intolerable, the error will show up on the regeneration of M_n and M_p as described below. However, corrections can be made on α and β to minimize the errors.

(b) Experiment

In order to make as accurate a measurement as possible on the ionization rates, it is essential to have pure carrier injection in a diode which has uniform multiplication over the whole area. It is also important to check the deduced data with the experimental ones to minimize systematic errors.

The diodes were made on n-type epitaxial layers grown on n^+ substrates. The dopings of the active layers ranged from $2.9 \times 10^{15} cm^{-3}$ to $5.1 \times 10^{16} cm^{-3}$. The structure of the diode is illustrated in Fig. 94. The residual thickness of the flat bottom well on the substrate side is approximately 1 mil. An electrolyte composed of four parts of acetic acid and one part of perchloric acid (see Sec. 6.3) was used to anodically etch out the well. The cell voltage during etching was kept at 20V. Approximately 600Å of platinum was sputtered on the active layer side to form a Schottky barrier. Platinum was used instead of aluminum to form the Schottky barriers because the sintered platinum barriers have consistently higher breakdown voltages than the aluminum barriers. Although aluminum has the advantages

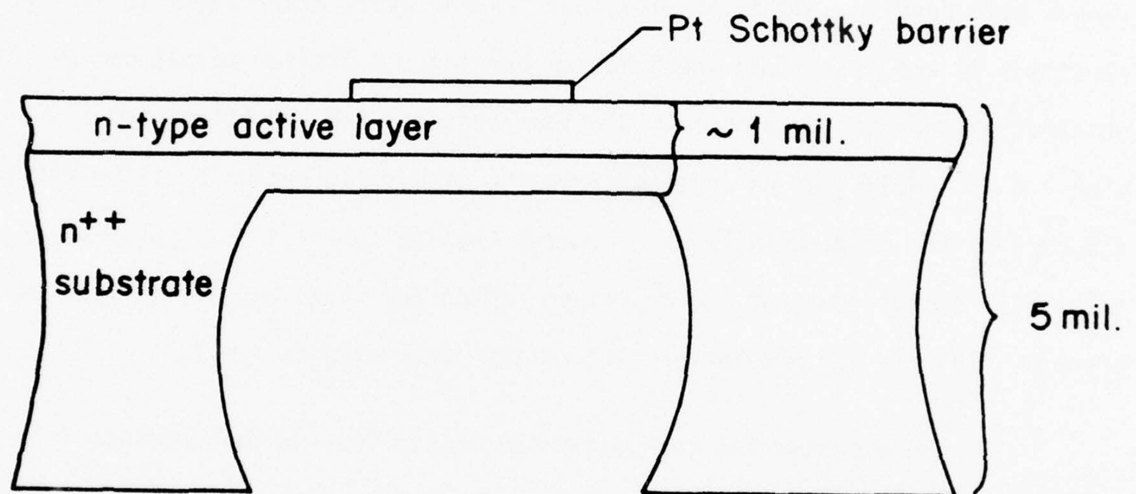


Fig. 94 Diode structure used in multiplication measurements.

of forming a chemically stable interface on GaAs[100], the reverse characteristics of the diodes are quite sensitive to prior surface preparation. Sintered platinum forms the compound $PtAs_2$ which is a degenerated p-type semiconductor[101]. Therefore, these barriers are less sensitive to residual surface states at the interface.

Pure electron injection can be achieved by illuminating the diode with light energy between 0.9 eV to 1.4 eV. Within this energy range, the radiation cannot have band to band excitation, but the energy is high enough to excite electrons in the metal over the Schottky barrier. A similar result can be obtained by irradiating an opaque platinum contact with radiation higher than 1.4 eV. Holes can be injected into the high field region by illuminating the back of the diode with light of energy greater than 1.4 eV. The generated holes will diffuse towards the depletion region and start the multiplication process. This is the reason for etching the diode down to 1 mil.

The experimental set-up for the multiplication measurements is similar to that of Ref. 94 and is illustrated in Fig. 95.

The field homogeneity inside the diode is crucial to the accuracy of the measurement. Since the ionization coefficients are strong functions of the electric field, a small fluctuation of the field inside the diode will affect the multiplication factor. In fact,

$$\Delta\left(\frac{1}{M}\right)\Bigg|_{E = E_0} = K \frac{\Delta E}{E_0} \qquad (41)$$

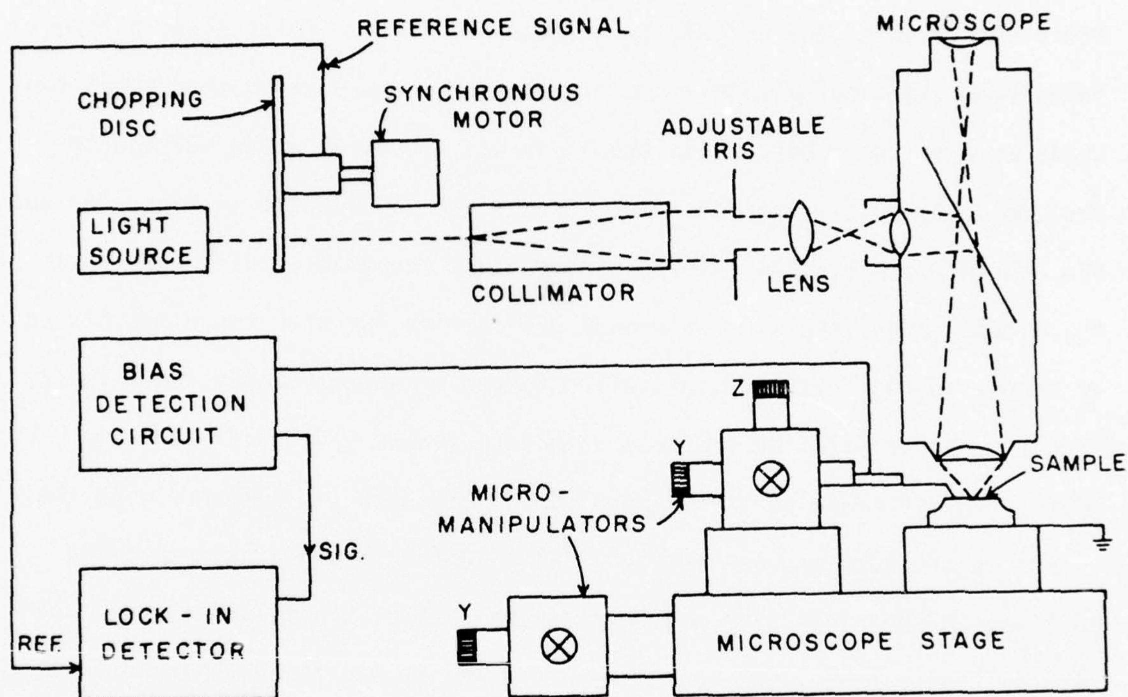


Fig. 95 Experimental set-up for the multiplication measurements.

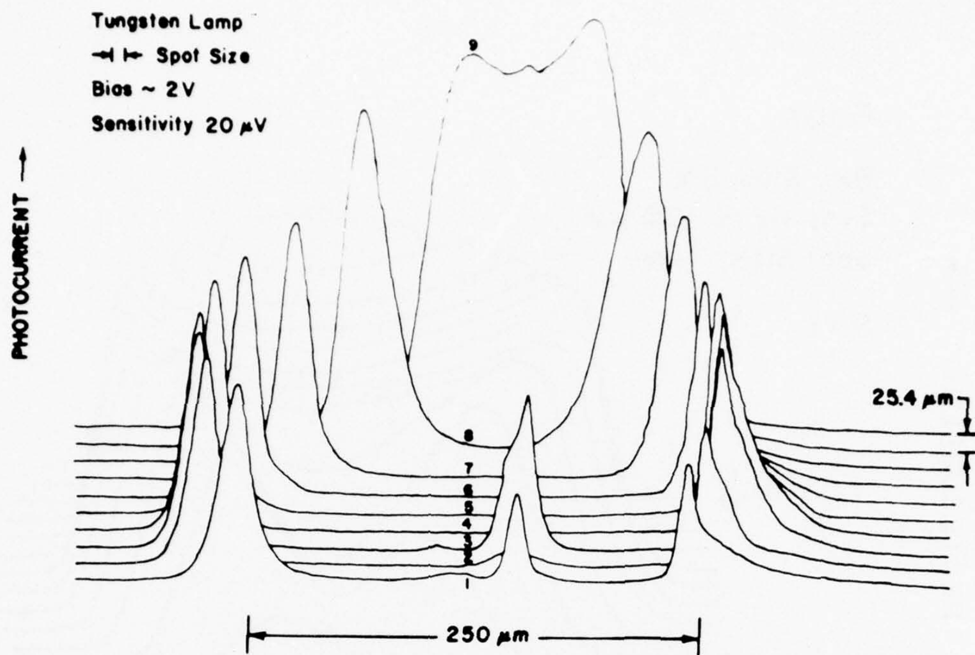
where ΔE = change of electric field

E = electric field at which multiplication equals M_0

K = constant, approximately 5 for $M_0 \gtrsim 2$.

It is obvious that from equation (41) a small field fluctuation inside a diode will result in a large multiplication fluctuation if M is large. Therefore, it is possible to study the uniformity of multiplication inside the diode to infer the uniformity of electric field. To do this, a fine focus beam with approximately 8μm diameter spot was scanned throughout the whole area of the diode, while the diode was biased at a low voltage to produce unity multiplication. Such traces are illustrated in Figs. 96a and 97a, and they are used as references for light response at different parts of the diode. Then, the same procedure was carried out with the diode biased at higher voltage with multiplication factor of approximately two. These traces compared with the previous reference traces gave multiplication factors in different parts of the diodes. Fig. 96b (as compared with the reference of photoresponse in Fig. 96a) illustrates a non-uniform field built-up on the right side of the diode, while Fig. 97b illustrates a diode with multiplication fluctuation less than 15% (i.e., field fluctuation less than 3%).

Several measurements of the multiplcation versus reverse bias were made. The doping of the active layers ranged from $2.9 \times 10^{15} cm^{-3}$ to $5.1 \times 10^{16} cm^{-3}$, covering field values from $2.2 \times 10^5 V/cm$ to $4.7 \times 10^5 V/cm$. The light source for illumination was a mercury arc lamp. Interference filters



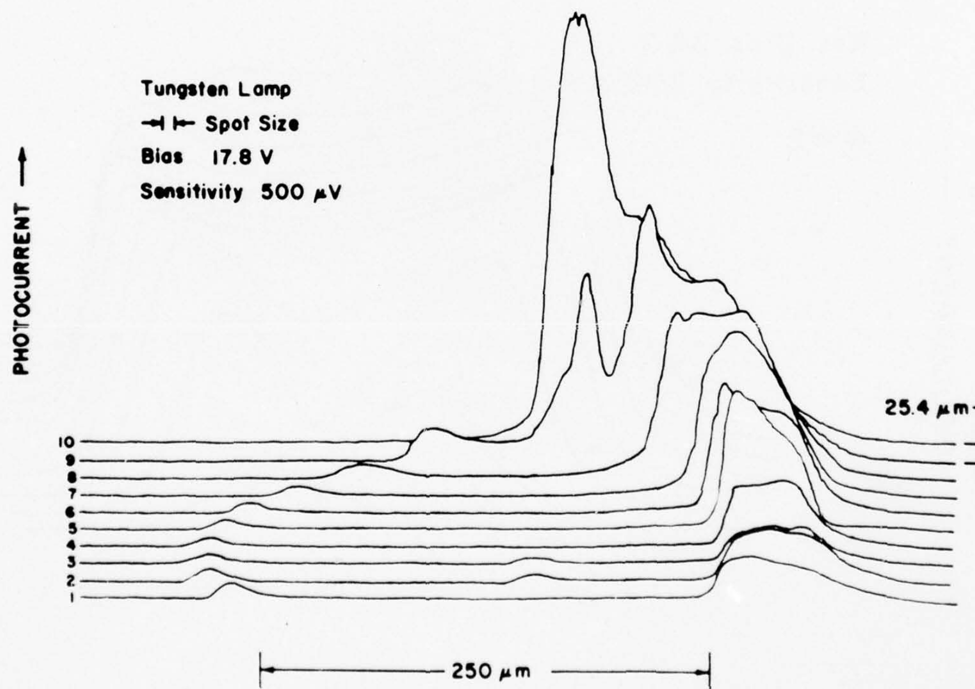


Fig. 96 (a) Photoresponse of a diode, biased at M-1, (b) biased at M≈3 illustrating a non-uniform field building up at the top right corner of the diode

were used to provide a narrow band light source.In some cases, a Helium Neon laser was used as a strong light source to inject holes. Table 18 summarizes the conditions of experiment done on various samples.

After the curves M_n and M_p versus voltage were obtained, base-line corrections[102] such as space charge widening effect and Schottky lowering effect were made on appropriate samples. Then the multiplication data were numerically calculated according to equations (39), (40), or (35), (36) for the punch-through and non-punch-through diodes respectively. The calculated α and β were plotted with the inverse of the electric field square in Fig. 98.

To minimize the systematic errors in calculations, the α and β for each diode were fitted to curves in the following form:

$$\alpha = A \exp\left[-(a/E)^2\right] \quad (42)$$

where A and a are two constants for best fitting. The deduced α and β were numerically integrated to reproduce M_n and M_p. These calculated M_n and M_p were then checked with the experimental ones to ensure self-consistency.

To further clarify the data in Fig. 98, the hole ionization coefficients were aligned by best fitting the data in all doping ranges to the form of equation (42). (The argument for the validity of this attempt will be given later.) The electron ionization coefficients were then aligned

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Table 18

Summary of experimental conditions for ionization coefficient measurements

Sample	Doping	Junction	Excitation		Punch-through Voltage	Breakdown Voltage
			Electron	Hole		
A	2.9×10^{15}	Pt Schottky	5770Å on Pt	6328Å from back	34V	130V
B	1.2×10^{16}	Pt Schottky	5770Å on Pt	5770Å from back	Non-punch-through	50 V
C	5.0×10^{16}	Pt Schottky	5770Å on Pt	6328Å from back	Non-punch-through	19V
D	5.1×10^{16}	P^+ -n Epi-layer	5770Å on Pt^+	5770Å from back	Non-punch-through	18V

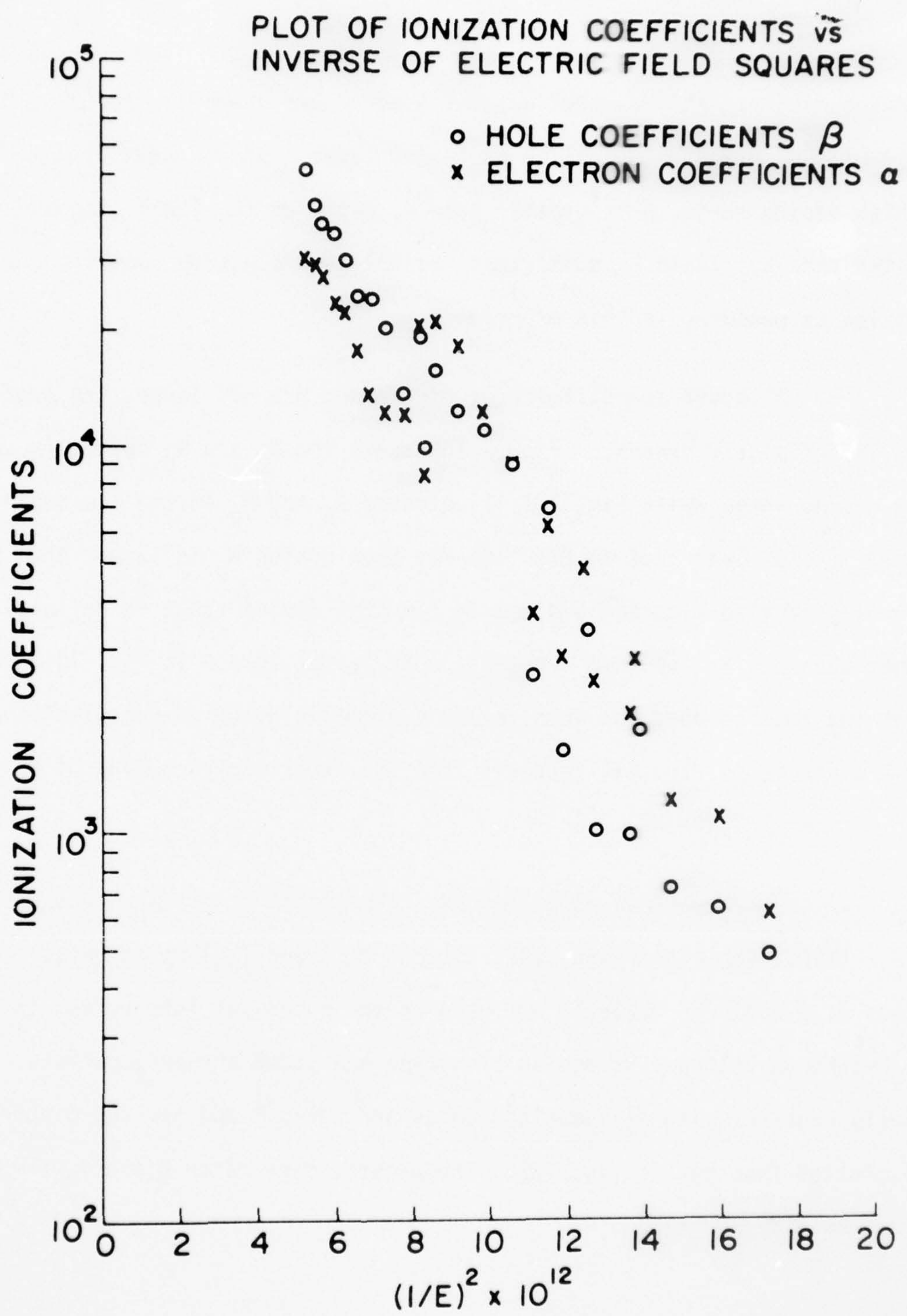

Fig. 98 A plot of avalanche coefficients vs inverse of square of electric field before any adjustment was made

correspondingly. The adjusted data of α and β are shown in Fig. 99. The shift of the curves of α will be explained later. It is clear that at high doping range, β is greater than α, while at the low doping end, α is greater than β. Table 19 summarizes the hole and electron ionization coeffieints measured in this experiment.

Although the differences of α and β are not large, the cross-over is definitely present. Figure 100 shows the M_n and M_p curves in the high doping range while Fig. 101 illustrates M_n and M_p in the low doping range. It is clear that in Fig. 100 for high doping M_p is larger than M_n. Referring back to equation (34), β in the high doping range is definitely larger than α. By the same argument, α is larger than β in Fig. 101. The above information does not involve any systematic error in calculating α and β since it is directly read off from the experimental curves of M_n and M_p.

The breakdown conditions for the junctions are $M_n \to \infty$ and $M_p \to \infty$ (i.e., the right hand sides of Eqs. (32) and (33) go to unity). The values of α and β in Table 18 are used in the numerical integration to find the breakdown voltages vs doping of n-type one-sided abrupt junctions. The results together with Stillman's,[93] Logan and Sze's[91] and Sze and Gibbons'[103] are plotted together in Fig. 102. The present data match closely with the experimentally observed ones.

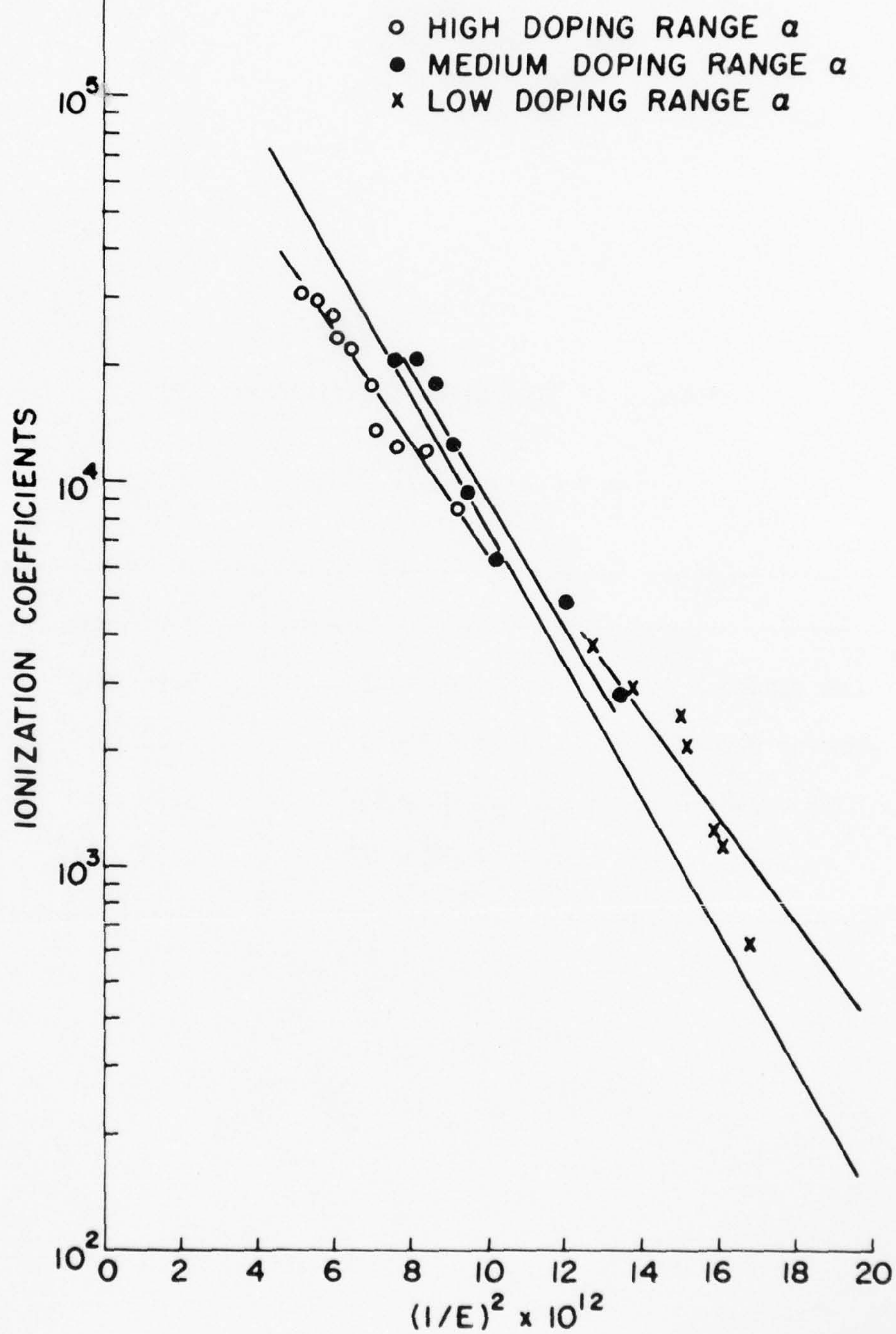

Fig. 99 Adjusted α and β vs inverse of square of electric field.

Table 19

Summary of Ionization Coefficients

$$\alpha = A \exp [-(a/E^2)]$$

	A	a
Low doping α	1.97×10^5	5.58×10^5
Medium doping α	4.54×10^5	6.28×10^5
High doping α	1.83×10^5	5.79×10^5
β	4.10×10^5	6.34×10^5

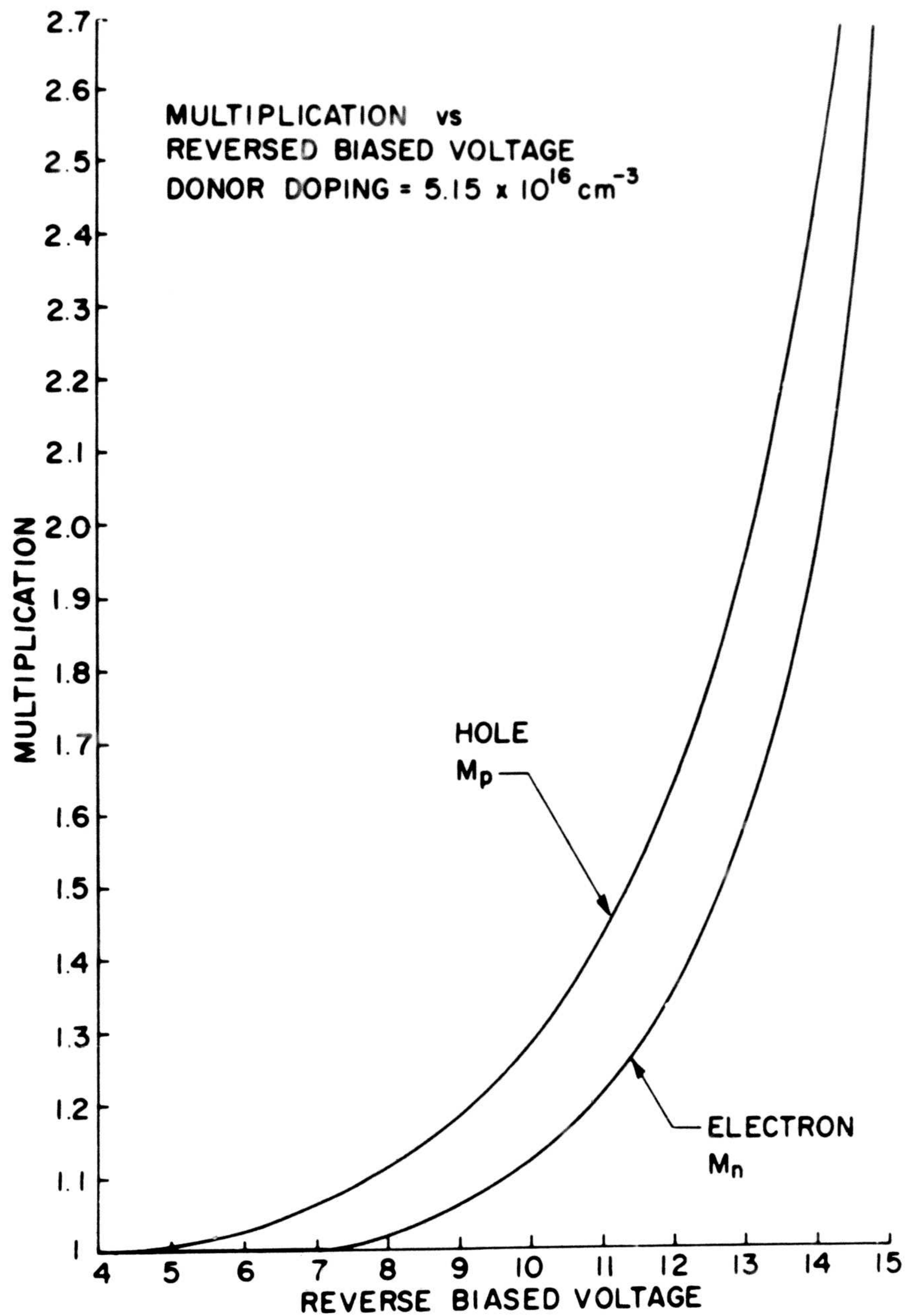

Fig. 100 Normalized M_n and M_p vs reverse bias voltage for the high doping range diode.

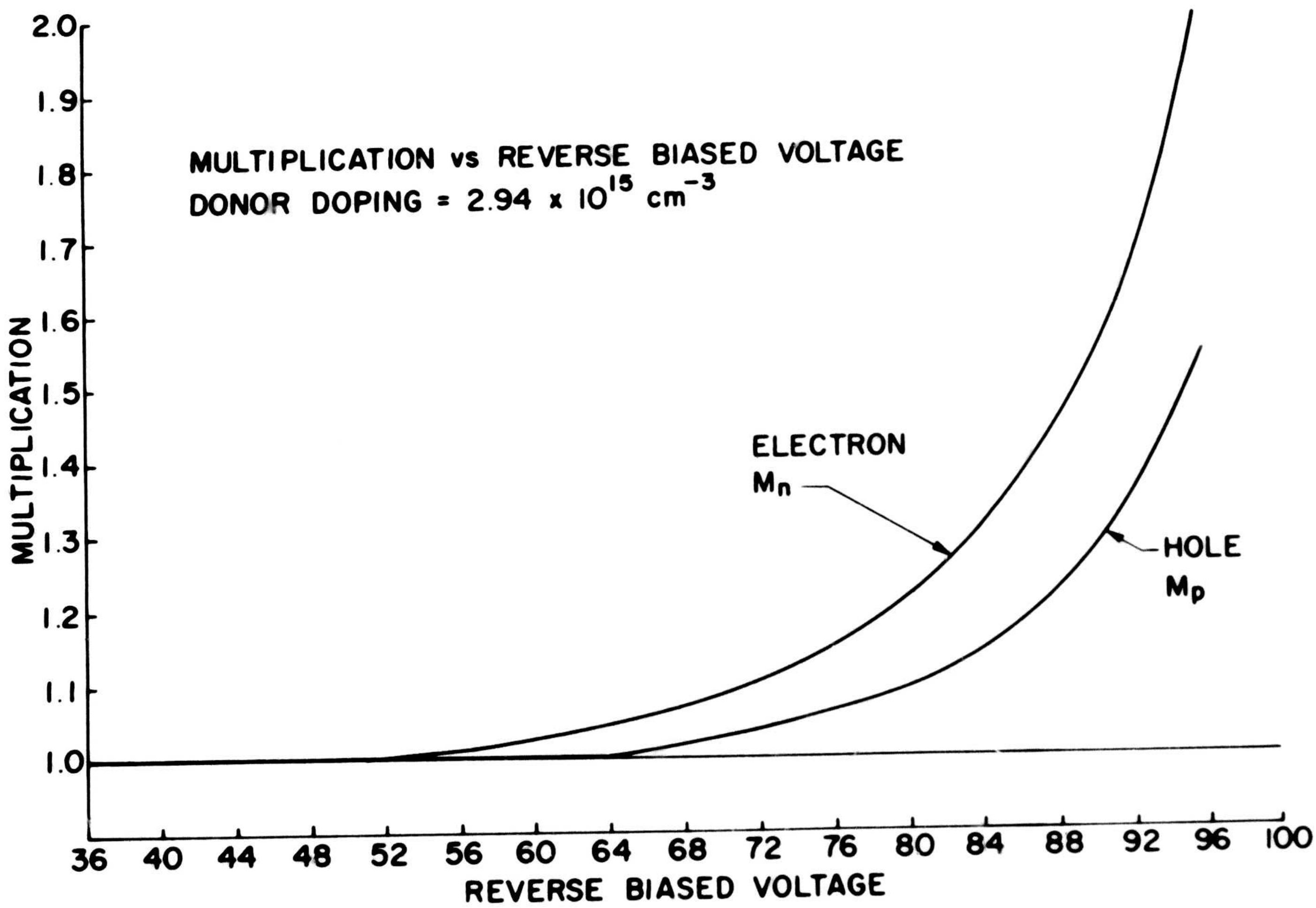

Fig. 101 Normalized M_n and M_p vs reverse bias voltage for the low doping range diode.

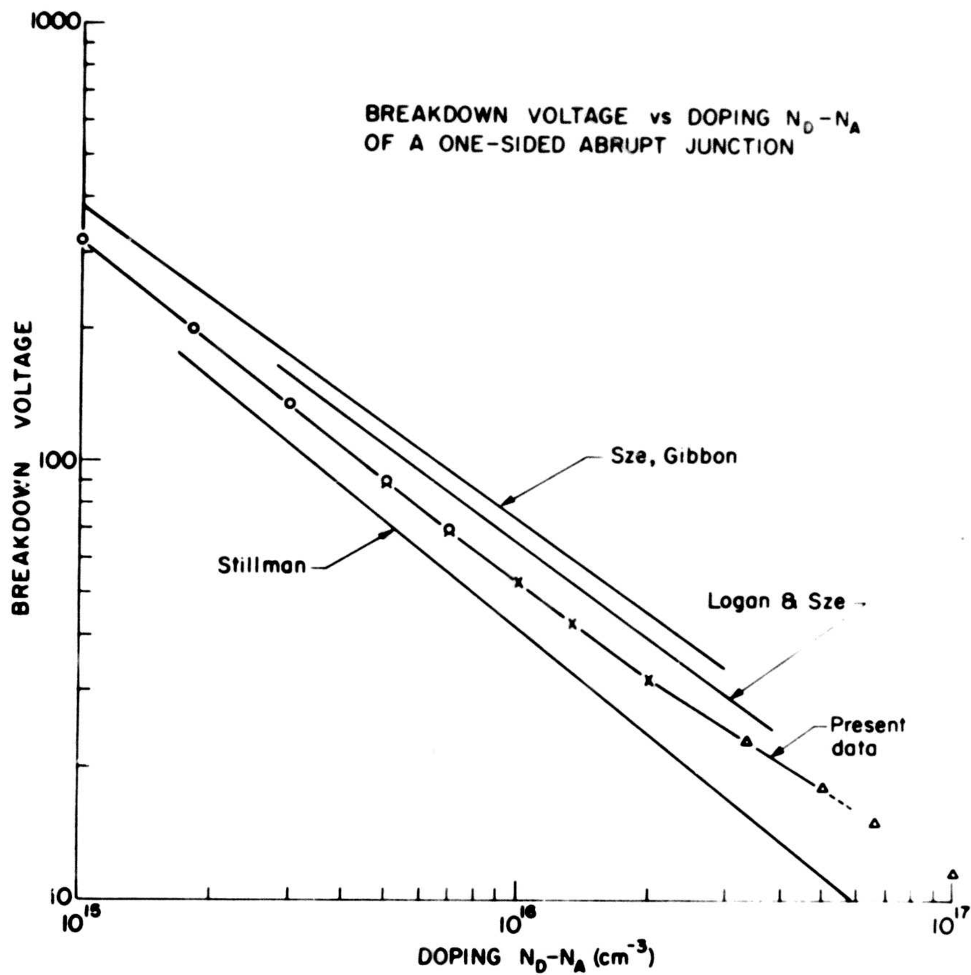

Fig. 102 Plot of breakdown voltages vs donor doping for a one-sided abrupt junction.

(c) Discussion

It is clear from the described experiments that the ionization rates of holes and electrons cross over. Since, none of the theories predicted this effect, it is of interest to discuss here the α and β crossover. The treatment below is only qualitative. To prove it, the inter-conduction band scattering time would have to be known. In fact this experiment gives an estimate of this scattering time.

Anderson and Crowell[96] have calculated that the threshold energies for secondary ionization in <100> GaAs are 1.7 eV and 2.1 eV for holes and electrons respectively. One would be tempted to think that the ionization rate of holes is larger than that of electrons. This is not so if the mean free path of holes for phonon scattering is shorter than that of electrons. In other words, holes will lose more energy to the lattice in reaching the threshold energy. Therefore, it is possible for the electron to have a higher ionization rate despite the fact that it has a higher threshold energy. This is certainly the case for the lightly doped materials in which the transit time of the electron through the high field is long compared to the interband scattering time.

A closer look at the band structure of GaAs in the <100> direction, as shown in Fig. 103,[104] reveals that the threshold energy for electrons lies on the second conduction band. Consequently, the electrons starting the secondary ionization process will have to be scattered to the

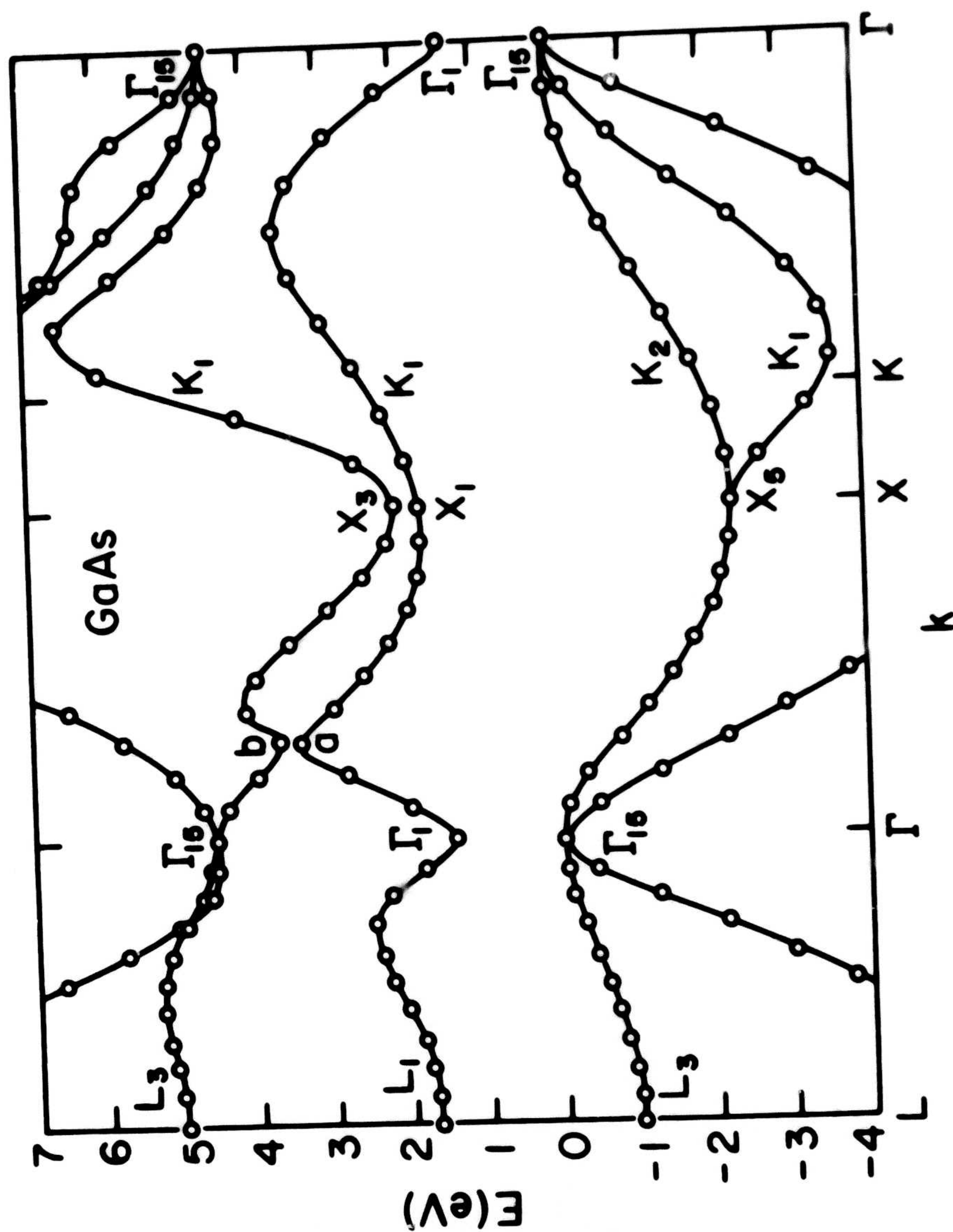

Fig. 103 GaAs band structure (from Ref. 104)

secondary conduction band. As the electrons are heated up in the Γ_1 valley by an applied field, they can go through several trajectories. The first possibility is that of an electron which is scattered into the X_1 or L_1 valley by means of intervalley scattering, then goes through an Umklapp process, and eventually arrives at "a" in Fig. 103. Then, either by tunneling or band to band scattering it arrives at "b". Another possibility is that the electron has escaped any intervalley scattering, reaches "a" directly under the influence of the applied field, and then either tunnels or is scattered into the second conduction band. In either case, the electron has to go through a tunneling or interconduction band scattering process in order to gain enough energy for secondary ionization.

The tunneling probability from point "a" to point "b" in Fig. 103 was investigated. The formula for tunneling probability per unit time, s, was given by Kane[104]:

$$s = \frac{2\pi}{\hbar} \left| M_{nn'} \right| \rho(E) \tag{43}$$

where

$$M_{nn'} = \frac{\pi \sqrt{m_r E_G}}{3hq\kappa} \exp \frac{-\pi h |q^2| E_G^{1/2}}{4F m_r^{1/2}} \tag{44}$$

and

$$\rho(E) = \frac{\kappa}{2\pi F} \tag{45}$$

where m_r = reduced mass; 3.09×10^{-32} kg was used at "a" and "b"

E_G = energy band gap; 0.24 eV from "a" - "b"

F = force acting on an electron

$g \approx \sqrt{E_G m_r}/h^2$

$\kappa = 5.557/4 \times 10^9 m^{-1}$.

Using the above values, at an electric field of 4×10^5 V/cm, the tunneling time was found to be 1.82×10^{-12} s, and at an electric field of 6×10^5 V/cm, the tunneling time was 4.33×10^{-13} s.

On the other hand, the band to band scattering time is estimated to be at least the intervalley scattering time which is in the order of 10^{-13} s. This interband scattering is judged to be more important than tunneling in the field range covered by these experiments.

As the doping of the active layer goes up, the effective avalanche zone will decrease correspondingly. The transit time through the high field region is in the order of 10^{-12} to 10^{-13} sec, depending on the doping. As the doping goes up, the transit time decreases to a value which is comparable to the band to band scattering time.

As a result, more and more electrons pass through the high field region without being scattered to the second conduction band. Consequently, the number of electrons which have high enough energy to produce secondary ionization will decrease. In other words, the ionization rate of electron is suppressed on the high doping side; as shown in Fig. 99 the ionization rate of holes is larger than that of electrons.

The hole ionization rate, contrary to that of electrons, will not be suppressed by the short transit time in a very narrow junction. For holes the ionization threshold energy lies within the same valence band and there is no requirement for band to band scattering. Therefore, the ionization coefficients of hole should line up along the whole field range independent of epitaxial layer doping.

It is also interesting to note that at a high enough field for which tunneling will dominate interband scattering, the electron ionization coefficient will no longer be suppressed. Theoretically, the electron ionization rates could again surpass the hole ionization rate.

7.0 PUBLICATIONS

The scientific and technical results of this research effort have been disseminated through publications and presentations in conferences. A list of such publications is given. For sake of brevity, oral presentations are omitted. Only papers which have already been published or accepted for publication in journals or conference proceedings are listed. The listing follows the organization of the report.

Sec. 3

1. R. Zucca, "Electrical Compensation in Semi-Insulating GaAs," J. Appl. Phys. 48, 1987 (1977).
2. J.R. Waldrop, R. Zucca, and C.P. Wen, "Depletion Effects in Semi-Insulating GaAs," Appl. Phys. Lett., 26, 322 (1975).
3. R. Zucca, "Effects of Heat Treatment on Semi-Insulating GaAs," Proc. North Am. Conf. on GaAs and Rel. Comp. St. Louis (1976).

Sec. 4

1. L. Mattes, Y -M. Houng and G.L. Pearson, "Growth and Properties of Semi-Insulating GaAs,", J. Vac. Sci. and Techn. 12, 869 (1975).
2. H. Morkoc and L.F. Eastman, "The Growth of Uniform Submicron GaAs Layers by Liquid Phase Epitaxy," J. Electrochem. Soc., 123, 906 (1976).
3. H. Morkoc and L.F. Eastman, "Purity of GaAs Grown by LPE in a Graphite Boat," J. Cryst. Growth, 36, 109 (1976).

Sec. 5

1. F.H. Eisen, B. Welch, K. Gamo, T. Inada, H. Mueller, M-A. Nicolet and J.W. Mayer, "Sulfur, Selenium, and Tellurium Implantation in GaAs", Applications of Ion Beams to Materials 1975, ed. by G. Carter, J.S. Colligon and W.A. Grant (The Institute of Physics, London, 1976) p. 64.
2. K. Gamo, T. Inada, S. Krekeler, J.W. Mayer, F.H. Eisen and B.M. Welch, "Selenium Implantation in GaAs", Solid State Elect. 20, 213 (1977).
3. F.H. Eisen, B.M. Welch, H. Muller, K. Gamo, T. Inada and J.W. Mayer, "Tellurium Implantation in GaAs", Solid State Elect. 20, 219 (1977).

4. K. Gamo, T. Inada, J.W. Mayer, F.H. Eisen and C.G. Rhodes, "Reordering of amorphous Layers in GaAs," Rad. Eff., to be published.

5. M. Wittmer, R. Pretorius, J.W. Mayer and M-A. Nicolet, "Investigation of the Au-Ge-Ni System Used for Alloyed Contacts to GaAs," Solid State Elect., to be published.

Sec. 6.

1. J.A. Higgins, B.M. Welch, F.H. Eisen and G.D. Robinson, "Performance of Sulfur-Ion Implanted FETs", Elect. Lett. 12, 17 (1976).

2. J.A. Higgins, B.M. Welch, F.H. Eisen and G.D. Robinson, "Performance of Selenium-Ion Implanted GaAs FETs," Electron. Lett. 12, 462 (1976).

3. J.A. Higgins, B.M. Welch, F.H. Eisen and G.D. Robinson, "Performance of Selenium Ion Implanted GaAs FETs," Proc. North Am. Conf. on GaAs and Rel. Comp., St. Louis (1976).

4. J. Berenz, M. Tomassini, C.A. Lee and G.C. Dalman, "Determination of IMPATT Diode Multiplication and Saturation Current from 30 MHz Noise Measurements", Proc. Fifth Biennial Cornell Elect. Engineering Conf., p. 407 (1975).

5. D. Law and C.A. Lee, "A New Aqueous Solution for the Anodic Oxidation of GaAs", J. Electrochem. Soc. 123, 768 (1976).

8.0 REFERENCES

1. G.R. Cronin and R.W. Haisty, J. Electrochem. Soc., 111, 874 (1964): R.W. Haisty and G.R. Cronin, Proc. 7th Internat. Conf. Semicond., Parid, Dunod (1964), p. 1161.

2. R.K. Willardson and W.P. Allred, in Proc. Int. GaAs Symposium, Reading, England (1966), p. 55

3. N.G. Ainslie, S.E. Blum and J.F. Woods, J. Appl. Phys. 33, 2391 (1962); J.F. Woods and N.G. Ainslie, J. Appl. PHys., 34, 1469 (1963).

4. J. Blanc and L.R. Weisberg, Nature 192, 155 (1961).

5. R.W. Haisty, E.W. Mehal, and R. Stratton, J. Phys. Chem. Sol. 23, 829 (1962).

6. T. Inoue and M. Ohyama, Sol. State Comm. 8, 1309 (1970).

7. D.C. Look, J. Phys. Chem. Solids 36, 1311 (1975).

8. J. Harper, H.E. Matthews and R.H. Bube, J. Appl. Phys. 41, 3182 (1970).

9. A.T. Philadelpheus and P.C. Euthymiou, J. Appl. Phys. 45, 955 (1974).

10. R. Zucca, J. Appl. Physics, 48, 1987 (1977).

11. W. Shockley in Electrons and Holes in Semiconductors, Van Nostrand (1950), p. 465.

12. See for example, L.H. Putley, The Hall Effect and Related Phenomena, Butterworth, London (1960).

13. E.M. Ganapol'skii, Sov. Phys. Sol. State 16, 1868 (1975); GH Strauss and J.J. Krebs, Proc. European Symposium on GaAs (1976).

14. W.J. Turner, G.D. Pettit, and N.C. Ainslie, J. Appl. Phys. 34, 3274 (1963).

15. J.C. Carballes, and J. Lebailly, Sol. State Comm. 6, 167 (1968).

16. H.J. Stocker and M. Schmidt, J. Appl. Phys. 47, 2450 (1976).

17. W.H. Koschel, S.G. Bishop and B.D. McCombe, Sol. State Comm. 19, 521 (1976).

18. R.F. Broom, J. Appl. Phys. 38, 3483 (1967); N.M. Kolchanova, D.N. Nasledov, M.A. Mirdzhalilova and V.Y. Ibraginov, Sov. Phys. Semicond. 4, 294 (1970); A.L. Lin and R.H. Bube, J. Appl. Phys 47, 1859 (1976).

19. C.H. Jones and A.R. Hilton, J. Electrochem. Soc. 113, 504 (1966); D. Bois and P. Pinard, Phys. Rev. B9, 4171 (1974).

20 A.G. Milnes, Deep Impurities in Semiconductors, Wiley (1973), 48.

21. NC MacDonald, Appl. Phys. Lett., 16, 76 (1970).

22. J.R. Waldrop and H.L. Marcus, J. Test Evaluation 1, 194 (1973).

23. J.R. Waldrop and J.S. Harris, J. Appl. Phys. 46, 5214 (1975).

24. M.A. Lampert and P. Mark, Current Injection in Solids, Academic Press, New York (1970).

25. R.W. Haisty and P.L. Hoyt, Solid State Electr., 10, 795 (1967).

26. M.E. Weiner and A.S. Jordan, J. Appl. Phys. 43, 1767 (1972).

27. J. Barrera, Proc. Fifth Biennial Cornell Electrical Engineering Conference, Cornell University, Ithaca, New York, p. 135 (1975).

28. M.D. Sturge, Phys. Rev. 127, 768 (1962).

29. M.I. Nathan and G. Burns, Phys. Rev. 129, 125 (1963).

30. T.C. Lee and W.W. Anderson, Sol. State Comm. 2, 265 (1964).

31. W. Schairer and M. Schmidt, Phys. Rev. B10, 2501 (1974).

32. M.S. Lin, K. Gamo, K. Masuda and S. Namba, Jap. J. Appl. Phys. 15, 53 (1976).

33. M.S. Seltzer, J. Phys. Chem. Sol. 26, 243 (1965).

34. M. Ilegems, R. Dingle and L.W. Rupp Jr., J. Appl. Phys. 46, 3059 (1975).

35. S.Y. Chiang and G.L. Pearson, J. Appl. Phys. 46, 2986 (1975).

36. D.J. Ashen, P.J. Dean, D.T.J. Hurle, J.B. Mullin, A.M. White and P.D. Greene, J. Phys. Chem. Solids 36, 1041 (1975).

37. H.J. Queisser and C.S. Fuller, J. Appl. Phys. 37, 4895 (1966).

38. C.H. Wolfe, G.E. Stillman and W.T. Lindley, J. Appl. Phys. 41, 3088 (1970).

39. Courtesy of W. Bludau.

40. R. Solomon, in Proc. 1968 GaAs Symposium (Inst. of Phys. and Phys. Soc., London, 1969) p. 11; M. Otsubo, K. Segawa and H. Miki, Jap. J. Appl. Phys. 12, 797 (1973).

41. B.L. Mattes, Y.M. Houng and G.L. Pearson, J. Vac. Sci. Technol. 12, 869 (1975).

42. D.V. Lang and R.A. Logan, J. Elect. Mat. 4, 1053 (1975).

43. Courtesy of B. McCombe

44. H. Strack, in Proc. 1966 GaAs Symp, Inst. on Phys. and Phys. Soc. London (1967), p. 1161.

45. M.B. Panish and H.C. Casey, Jr., J. Appl. Phys. 40, 163 (1969).

46. P.L. Hower, W.W. Hooper, D.A. Tremere, W. Lehrer, and C.A. Bittmann, in Proc. 1968 GaAs Symposium , Inst. of Phys. and Phys. Soc., London, (1969) p. 187.

47. K. Lehovec and R. Zuleeg, in Inst. Phys. Conf. Ser. No. 24, 292 (1975).

48. Y.M. Houng, Ph.D. Thesis, Stanford University, January, 1977.

49. B.L. Mattes and R.K. Route, J. Crystal Growth 27 133 (1974).

50. J.T. Longo, J.S. Harris, E.R. Gertner and J.C. Chu, J. Crystal Growth 15 107 (1972).

51. D.L. Rode, J. Crystal Growth 20 13 (1973).

52. I. Crossley and M.B. Small, J. Crystal Growth 11 157 (1971).

53. R.L. Moon, J. Crystal Growth 27 62 (1974).

54. L.R. Dawson, J. Crystal Growth, 27, 86 (1974).

55. M. Spitzer, B. Schwartz and G.D. Weigle, J. Electrochem. Soc., 122, 397 (1975); D.L. Rode, B. Schwartz and J.V. DiLorenzo, Solid-State Electron. 17, 1119 (1974).

56. B. Schwartz, J. Electrochem. Soc. 118, 657 (1971).

57. B.S. Hewitt, H.M. Cox, H. Fukui, J.V. DiLorenzo, W.V. Schlosser and D.E. Iglesias, in Proc. 1976 GaAs Symp., Inst. of Physics and Phys. Soc., London (1977).

58. H.G.B. Hicks and P.D. Greene, Proc. 1970 GaAs Symp., Inst. of Physics and Phys. Soc. London (1970), p. 92.

59. H.G.B. Hicks and D.F. Manley, Solid State Comm. 7, 1463 (1969).

60. J.B. Mullin, Private Communication, Royal Radar Establishment, UK.

61. D.W. Shaw, J. Crystal Growth 8, 118, (1971).

62. A.A. Immorlica and F.H. Eisen, Appl. Phys. Lett. 29, 94 (1976).

63. H. Muller, F.H. Eisen and J.W. Mayer, J. Electrochem. Soc. 122, 651 (1975).

64. J.F. Gibbons, W.S. Johnson and S.W. Mylroie, Projected Range Statistics, Dowden, Hutchinson and Ross, Inc. Stroudsburg, Pennsylvania (1975).

65. S.M. Sze and J.C. Rivin, Solid State Electron. 11, 599 (1968).

66. W.E. Williams and H.B. Bebb, in Semiconductors and Semimetals, R.K. Willardson and A.C. Beer, eds. Academic Press, New York (1972), p. 321.

67. J.P. Donnelly, W.T. Lindley and C.E. Hurwitz, Appl. Phys. Lett. 27, 41 (1975).

68. L.J. Vieland and I. Kudman, J. Phys. Chem. Solids, 24, 437 (1963).

69. J.M. Woodcock, Appl. Phys. Lett. 28, 226 (1976).

70. F.H. Eisen and B.M. Welch, Proceeding Fifth International Conference on Ion Implantation in Semiconductors and Other Materials (Plenum Press, to be published).

71. J.F. Chemin, I.V. Mitchell and F.W. Saris, J. Appl. Phys. 45, 532 (1974).

72. J.W. Mayer, L. Eriksson and J.A. Davies, Ion Implantation in Semiconductors (Academic Press, New York, 1970) p. 65.

73. J.S. Harris, F.H. Eisen, B. Welch, R.D. Pashley, D. Sigurd and J.W. Mayer, Appl. Phys. Lett. 21, 601 (1972).

74. L. Csepregi, J.W. mayer and T.W. Sigmon, Phys. Lett. 54A, 157 (1975).

75. L. Csepregi, W.K. Chu and H. Muller, J.W. Mayer and T.W. Sigmon. Rad. Effects 28, 227 (1976).

76. J.F. Ziegler and W.K. Chu, Atomic Data and Nuclear Data Tables 13, 463 (1974).

77. R. Kuvas and C.A. Lee, J. Appl. Phys. 41, 1743 (1970).

78. R.H. Haitz, J. Appl. Phys. 38, 2935 (1967).

79. H.K. Gummel and J.L. Blue, IEEE Trans. Electron Devices, 14, 569 (1967).

80. R.L. Kuvås, IEEE Trans. Microwave Theory and Techniques, 21, 127 (1973).

81. J.J. Goedbloed, Phillips Res. Reports, Suppl. 7 (1973).

82. J.A. Ringo and P.O. Lauritzen, Sol. State Electr. 15, 625 (1972).

83. D.H. Lee, Proc. IEEE, 61, 666 (1973).

84. W.T. Read, Jr., B.S.T.J. 37, 401 (1958).

85. I.M. Naqvi, Sol. State Electr. 16, 19 (1973).

86. C.A. Lee, R.L. Batdorf, W. Wiegmann, and G. Kaminsky, J. Appl. Phys., 38, 2797 (1967).

87. H. Hasegawa, K.E. Forward, and H. Hartnagel, Electr. Lett. 11, 53 (1975).

88. R.A. Logan, B. Schwartz, and W.J. Sandburg, J. Electrochem. Soc. 120, 1386 (1973).

89. S.M. Spitzer, B. Schwartz, and G.D. Weigle, 122, 397 (1975).

90. J.G. Harper and M.S. Astor, Electrochem. Soc. Electr. Div., Ext. Abstracts 8, 161 (1959).

91. R.A. Logan and S.M. Sze, J. Phys. Soc. Jap. Suppl. 21, 434 (1966).

92. R. Hall and J.H. Leck, Int. J. Electron. 25, 529 (1968).

93. G.E. Stillman, C.M. Wolfe, J.A. Rossi and A.G. Foyt, Appl. Phys. Lett., 24, 471 (1974).

94. C.A. Lee, R.A. Logan, R.L. Batdorf, J.J. Kleimack and W. Wiegmann, Phys. Rev. 134, A761 (1964).

95. G.A. Baraff, Phys. Rev. 128, 2507 (1962).

96. C.L. Anderson and C.R. Crowell, Phys. Rev., B5, 2267, (1972).

97. M.L. Cohen and T.K. Bergstresser, Phys. Rev., 141, 789 (1966).

98. K.G. McKay, Phys. Rev. 94, 877, (1954).

99. S.L. Miller, Phys. Rev. 99, 1234 (1955).

100. H.B. Kim, G.G. Sweeney and T.M.S. Heng, The Institute of Physics Conference Series, #24, The Institute of Phys., London, (1975), p. 307.

101. M.H. Fermor, S. Furnseth and A. Kjekshus, J. Less. Common Metals, 11, 376 (1966).

102. M.H. Woods, W.C. Johnson and M.A. Lampert, Solid State Electr. 16, 381 (1973).

103. S.M. Sze and G. Gibbons, Appl. Phys. Letters, 8, 111, (1966).

104. E.O. Kane, J. Phys. Chem. Solids, 12, 181 (1959).

105. Z.L. Liau, W.L. Brown, R. Homer and J.M. Poate, Appl. Phys. Lett. (in press).

METRIC SYSTEM

BASE UNITS:

Quantity	Unit	SI Symbol	Formula
length	metre	m	...
mass	kilogram	kg	...
time	second	s	...
electric current	ampere	A	...
thermodynamic temperature	kelvin	K	...
amount of substance	mole	mol	...
luminous intensity	candela	cd	...

SUPPLEMENTARY UNITS:

Quantity	Unit	SI Symbol	Formula
plane angle	radian	rad	...
solid angle	steradian	sr	...

DERIVED UNITS:

Quantity	Unit	SI Symbol	Formula
Acceleration	metre per second squared	...	m/s
activity (of a radioactive source)	disintegration per second	...	(disintegration)/s
angular acceleration	radian per second squared	...	rad/s
angular velocity	radian per second	...	rad/s
area	square metre	...	m
density	kilogram per cubic metre	...	kg/m
electric capacitance	farad	F	A·s/V
electrical conductance	siemens	S	A/V
electric field strength	volt per metre	...	V/m
electric inductance	henry	H	V·s/A
electric potential difference	volt	V	W/A
electric resistance	ohm		V/A
electromotive force	volt	V	W/A
energy	joule	J	N·m
entropy	joule per kelvin	...	J/K
force	newton	N	kg·m/s
frequency	hertz	Hz	(cycle)/s
illuminance	lux	lx	lm/m
luminance	candela per square metre	...	cd/m
luminous flux	lumen	lm	cd·sr
magnetic field strength	ampere per metre	...	A/m
magnetic flux	weber	Wb	V·s
magnetic flux density	tesla	T	Wb/m
magnetomotive force	ampere	A	...
power	watt	W	J/s
pressure	pascal	Pa	N/m
quantity of electricity	coulomb	C	A·s
quantity of heat	joule	J	N·m
radiant intensity	watt per steradian	...	W/sr
specific heat	joule per kilogram-kelvin	...	J/kg·K
stress	pascal	Pa	N/m
thermal conductivity	watt per metre-kelvin	...	W/m·K
velocity	metre per second	...	m/s
viscosity, dynamic	pascal-second	...	Pa·s
viscosity, kinematic	square metre per second	...	m/s
voltage	volt	V	W/A
volume	cubic metre	...	m
wavenumber	reciprocal metre	...	(wave)/m
work	joule	J	N·m

SI PREFIXES:

Multiplication Factors	Prefix	SI Symbol
1 000 000 000 000 = 10^{12}	tera	T
1 000 000 000 = 10^{9}	giga	G
1 000 000 = 10^{6}	mega	M
1 000 = 10^{3}	kilo	k
100 = 10^{2}	hecto*	h
10 = 10^{1}	deka*	da
0.1 = 10^{-1}	deci*	d
0.01 = 10^{-2}	centi*	c
0.001 = 10^{-3}	milli	m
0.000 001 = 10^{-6}	micro	μ
0.000 000 001 = 10^{-9}	nano	n
0.000 000 000 001 = 10^{-12}	pico	p
0.000 000 000 000 001 = 10^{-15}	femto	f
0.000 000 000 000 000 001 = 10^{-18}	atto	a

* To be avoided where possible.

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