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MITRE PREPROCESSOR

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REVIEW AND APPROVAL

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DATA EDITING
PREPROCESSOR
REAL-TIME SIGNAL PROCESSOR
THRESHOLD DETECTION
TV SENSOR INTERFACE

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

A high-speed, special-purpose preprocessor has been designed and developed by The MITRE Corporation for the GEODSS (Ground-based Electro-Optical Deep Space Surveillance) system during the experimental test and evaluation phase of this program. The preprocessor is part of a MITRE developed snapshot MTI technique presently being tested and evaluated at the GEODSS Experimental Test Site (ETS) in Stallion,

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20. ABSTRACT (concluded)

New Mexico. The preprocessor provides the interface between a low light level TV sensor and the MITRE multi-minicomputer processor. The primary functions performed by the preprocessor are: (1) input signal processing, (2) buffer memory data storage, (3) output data processing, and (4) preprocessor and TV sensor timing and control. This report provides a detailed system level description of the preprocessor concept, function and implementation. Detailed schematics and logic diagrams of the preprocessor are documented separately.

ACKNOWLEDGMENTS

This report has been prepared by The MITRE Corporation under Project No. 6290. The contract is sponsored by the Electronic Systems Division, Air Force Systems Command, Hanscom Air Force Base, Massachusetts.

The basic requirements for the preprocessor were generated by J.E. Barry and H.E.T. Connell. S.J. Meehan provided the basic digital design of the input processor.

The detailed mechanical design and development of the preprocessor was performed by F.D. Page with assistance from L.S. Chiodi, J.E. Doucette, R. Gamache, J. Wooldridge, and the technicians in the Signal Processing Techniques Group. F. Page and L. Chiodi also assisted in the unit and system testing of the preprocessor. L. Chiodi was responsible for the installation and initial checkout of the preprocessor at the ETS site.

Overall project leadership was provided by J.E. Barry, H.B. Goldberg, and P.M. Ware. Consultation and technical design were coordinated with R.D. Haggarty, R.W. Jacobus and E.A. Palo.

PREFACE

The basic concept of the preprocessor began with R.W. Jacobus and was further developed by J.E. Barry. The first preprocessor was designed and implemented by D.R. Bungard and P. Buote in 1974. Its purpose was to gather data from typical star backgrounds for subsequent digital signal processing and analysis at MITRE. Recorded data of actual satellites and star backgrounds observed with the AFAL 25 inch telescope/image tube system at John Bryant State Park, Dayton, Ohio, was used as inputs to demonstrate the present snapshot MTI system's capability to handle real data. The present preprocessor and multi-minicomputer processor provide real time MTI processing of image data from the Ground-based Electro-Optical Deep Space Surveillance System (GEODSS) sensor.

GEODSS is a network of telescopes which will systematically scan the night sky in search of distant man-made objects. The detection method is based on the relative angular motion of the man-made object with respect to the very distant star background which maintains a fixed pattern to the observer. The GEODSS sensor is a light-sensitive device which consists of a two-dimensional matrix of sensing elements. The effects of light on this surface are measured by an electron beam which systematically scans the matrix in a raster pattern. The data presented to the MTI computer by the GEODSS sensor essentially consists of the x, y coordinates and a measure of brightness for each light source in the telescope field-of-view.

The MTI technique implemented on the multi-minicomputer network by MITRE detects moving targets by comparing a sequence of exposures from the same telescope field of view. Exposure pairs are subtracted point by point to eliminate the motionless stars, while targets remain. In this method, the telescope is stabilized for a relatively short exposure — typically 1/4 second — and then successively moved and restabilized on each of a series of contiguous fields of view. This continues for a relatively long period — typically 10 seconds — after which the telescope returns to the first field and takes a second series of "snapshots" of the same series of fields. The process is repeated once more and then each resulting set of three time-separated snapshots of each field of view is processed to eliminate fixed stars and then searched for tracks formed by the regularly displaced images left by a satellite. This method, referred to as Snapshot MTI, is one of several methods being studied for GEODSS by MITRE, TRW/ITEK and Lincoln Laboratories (reference 5).

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SECTION I

INTRODUCTION

This section provides a brief introduction of the MITRE preprocessor and GEODSS sensor. After the introduction, an outline of the remainder of the report is presented.

The MITRE preprocessor, as shown in Figure 1, provides the interface between a low light level TV sensor and the MITRE Multi-Minicomputer Processor. This specially designed preprocessor converts the video signal from the TV sensor into digital form and performs initial signal processing tasks to minimize the data processing requirements of the multi-minicomputer processor. Data reduction and editing logic in the preprocessor provide the capability to eliminate most of the spurious and redundant data. After input thresholding, which consists of an analog-to-digital conversion of the input video signal, the preprocessor is a special purpose digital hardware device implemented to perform several digital signal processing tasks. The basic feature of the preprocessor is the use of digital signal processing of the image data to provide accurate, stable, flexible and reliable data reduction at input data rates that far exceed the capabilities of a general purpose computer.

The preprocessor is necessary because of speed (capable of operating at input rates in excess of 30 MHz) and yet reduces and temporarily stores the data to be compatible with the minicomputer I/O rates. While the minicomputers do the detailed MTI processing, it is the preprocessor that allows the system to operate at reasonable scan rates.

The advantages of using digital techniques in the implementation of the preprocessor are:

- Stability and reliability are inherent in the digital approach.
- Flexibility - the characteristics of the preprocessor can be varied to accommodate varying target and system parameters.
- Compatibility with the digital input of the multi-minicomputer processor.
- Ease of simulation and test - the signal processing functions to be performed by the preprocessor can be readily simulated in the multi-minicomputer processor. Simulated data can then be generated by the multi-minicomputer processor to test the preprocessor which would otherwise require very complex test equipment.

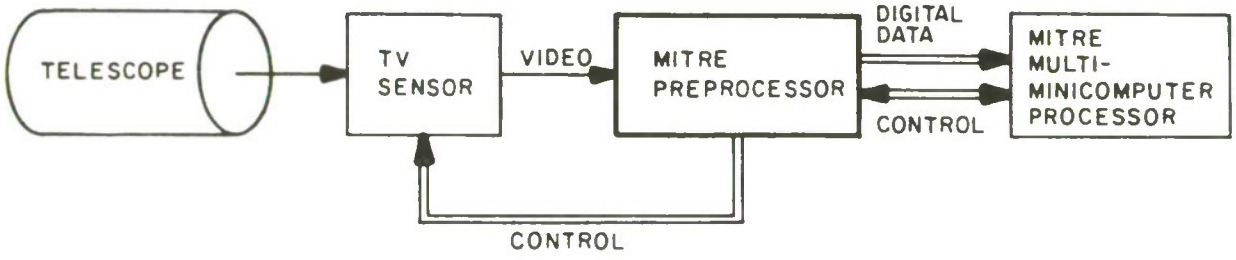

FIGURE 1. MITRE/GEODSS SYSTEM BLOCK DIAGRAM

The TV sensor at the GEODSS ETS site is a Westinghouse model TEM 432 low light level TV camera. In Table I are listed several of the characteristics which describe this TV sensor. The MITRE multi-minicomputer processor is described in detail in references 2, 3, 4 and 5.

The remainder of the report is divided into five sections. In Section II a detailed summary and overview of the basic concepts and functions of the preprocessor are presented. Section III discusses the detailed design and implementation of the preprocessor.

The integration of the MITRE preprocessor and multi-minicomputer processor with the GEODSS ETS system is described in Section IV. Section V includes a description of the peripherals associated with the MITRE/GEODSS system. The report concludes with Section VI which summarizes the laboratory test results and signal processing capabilities of the preprocessor which are applicable to a wide variety of other tasks.

The reader who is interested in the detailed design of the preprocessor is referred to reference 2 which includes detailed schematics and logic diagrams of the preprocessor.

TABLE I

TV SENSOR CHARACTERISTICS

WESTINGHOUSE LOW LIGHT LEVEL
TEM-432 CAMERA SYSTEM

- Scan Rates (Non-Interlaced External Operating Mode)

Vertical:	60, 30, 15 Hz
Horizontal:	15.75 KHz, 26.25 KHz

- Number of Lines/Frame: 525, 875, 1050
- Video Preamp Bandwidth: $\pm$ 1 db at 10 MHz
$\pm$ 3 db at 15 MHz
- Video Preamp Noise Current: < 5 nA RMS at 10 MHz
- Video Bandwidth Selection: 3 MHz, 5 MHz, 7.5 MHz or full video bandwidth of 15 MHz
- Integration: 1 to 999 Frames
- Readout: 1 to 9 Frames

SECTION II

SUMMARY AND OVERVIEW

This section provides a summary of the basic concepts and functions of the preprocessor. The primary functions performed by the preprocessor, as shown in Figure 2, are: (1) input processing, (2) buffer memory data storage, (3) output processing, and (4) preprocessor and camera timing and control. A photograph of the preprocessor front panel is shown in Figure 3. Data and status indicators and control switches are provided for monitoring and controlling the preprocessor. A summary of the preprocessor performance characteristics is included in Table II. In Table III are listed the available scan rates and control signal characteristics provided by the preprocessor for externally driving the TV Sensor.

The following discussions provide a comprehensive description of each of the basic functions: input processing, memory, output processing, control and peripherals.

Input Processing

Input processing consists initially of thresholding and high speed sampling of the video signal in each resolution element to provide a digital representation of the image data. The raw video is converted into digital form by comparing the video signal in a resolution element against three thresholds designated T1, T2 and T3 where T3 is the lowest threshold. Figure 4 illustrates these thresholding and digitizing functions. Threshold T3 is set to eliminate most or all of the night sky background in the video. If the video is below T3 then no data is taken. This minimizes the volume of data which must be processed. The second threshold T2 is used to determine whether or not the detected objects exceed the brightness of the dimmest potential satellite sought by the system. The first threshold T1 is set near the saturation level of the image tube and is used for bright object detection. The threshold references are digitally controlled from front panel switches as shown in Figure 3.

The threshold comparators set a two bit code indicating which of the thresholds the video exceeds. If the video does not exceed the lowest threshold T3, the data point is deleted. The analog (video) data is therefore quantized by these thresholds to 4 levels producing a 2-bit digital output amplitude word. The rationale for the utility of these thresholds is discussed in Section IV of reference 2.

The input processor also provides the capability to edit the input data; that is, delete or insert data in the input data stream. Data editing of the digitized image data is first performed by an X,

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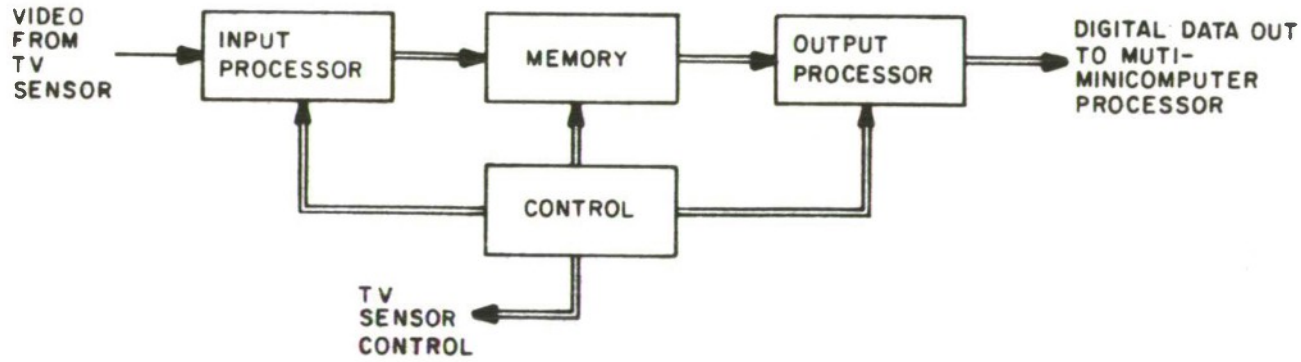

FIGURE 2. MITRE PREPROCESSOR BLOCK DIAGRAM

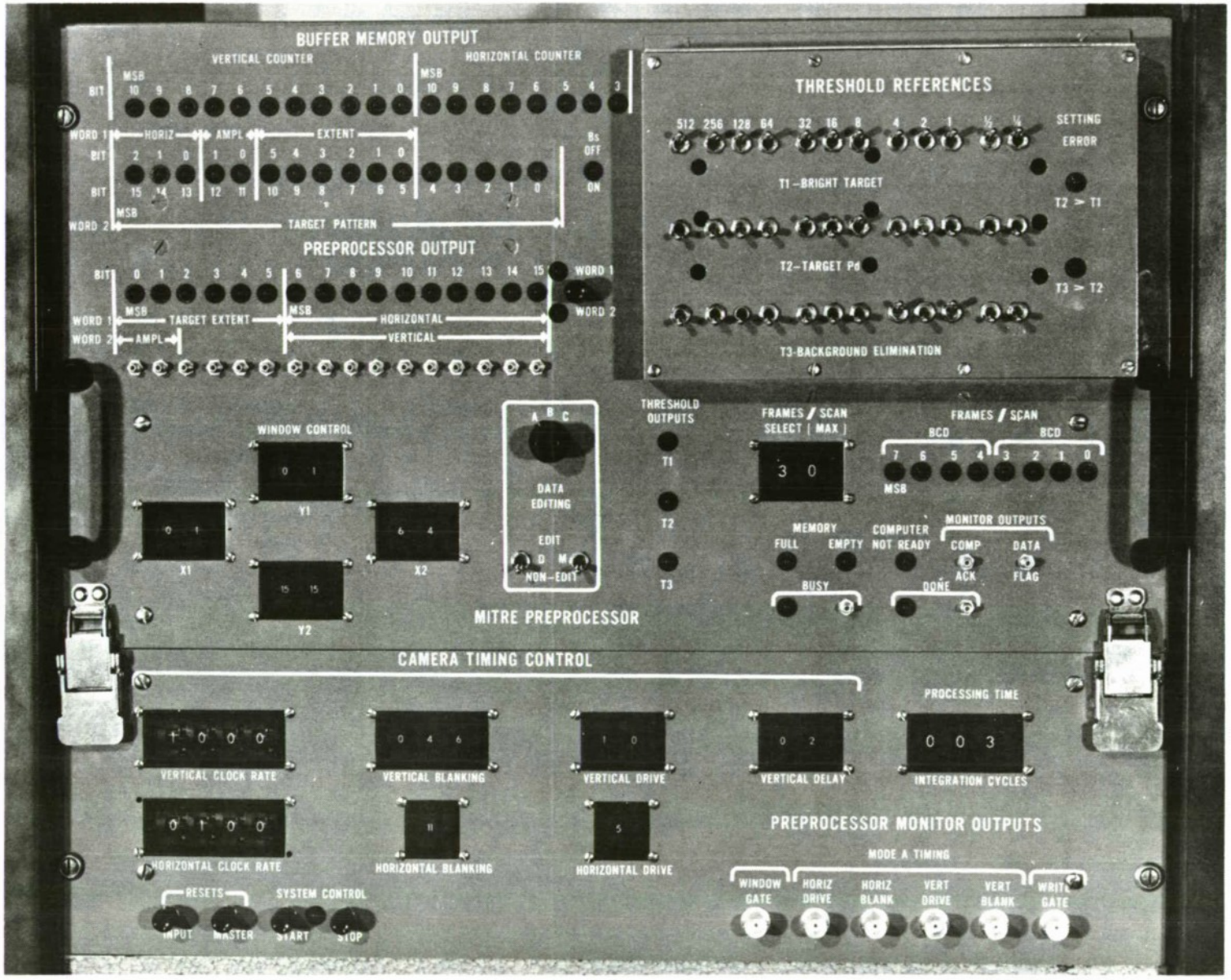

FIGURE 3. PREPROCESSOR FRONT PANEL

TABLE II

MITRE PREPROCESSOR CHARACTERISTICS

• SAMPLING RATE:	TO 30 MHz
• VIDEO BANDWIDTH:	WILL ACCEPT SIGNALS OVER THE FREQUENCY BAND OF DC TO 15 MHz
• MEMORY (FIFO)	
CAPACITY:	256 WORDS X 36 BITS
INPUT DATA RATE:	5 MHz (MAX)
OUTPUT DATA RATE:	DETERMINED BY MINICOMPUTER- 1.25 MHz for 16 BIT DATA WORD FOR DATA GENERAL ECLIPSE MINICOMPUTER
• SIGNAL DETECTION LEVEL:	$\pm$ 2mV WITH RESPECT TO REFERENCE THRESHOLD LEVEL
• SNAPSHOT PROCESSING: TIME INTERVAL	$n \times (r + i) \times \frac{1}{\text{TV Sensor Frame Rate}}$

where n = 1 to 999 preset by preprocessor

r = 1 to 9 (Number of TV Sensor readout frames)

i = 1 to 999 (Number of TV Sensor integration frames)

and r and i are preset by the TV Sensor.

TABLE III

TV SENSOR CONTROL

- HORIZONTAL SCAN RATE = $\frac{\text{SAMPLING CLOCK}}{N}$

  where the SAMPLING CLOCK = 0 to 30 MHz in .01 Hz steps and N is adjustable from 1 to 9999.

- VERTICAL SCAN RATE = $\frac{\text{HORIZONTAL SCAN RATE}}{N}$

  where N is adjustable from 1 to 9999

- HORIZONTAL BLANKING PULSE WIDTH: Adjustable from 1 to 15 usec in 1 usec steps
- HORIZONTAL DRIVE PULSE WIDTH: Adjustable from 1 to 15 usec in 1 usec steps
- HORIZONTAL DRIVE DELAY: Fixed at 1 usec
- VERTICAL BLANKING PULSE WIDTH: Adjustable from 1 to 4095 usec in 1 usec steps
- VERTICAL DRIVE PULSE WIDTH: Adjustable from 1 to 255 usec in 1 usec steps
- VERTICAL DRIVE DELAY: Adjustable from 1 to 255 usec in 1 usec steps

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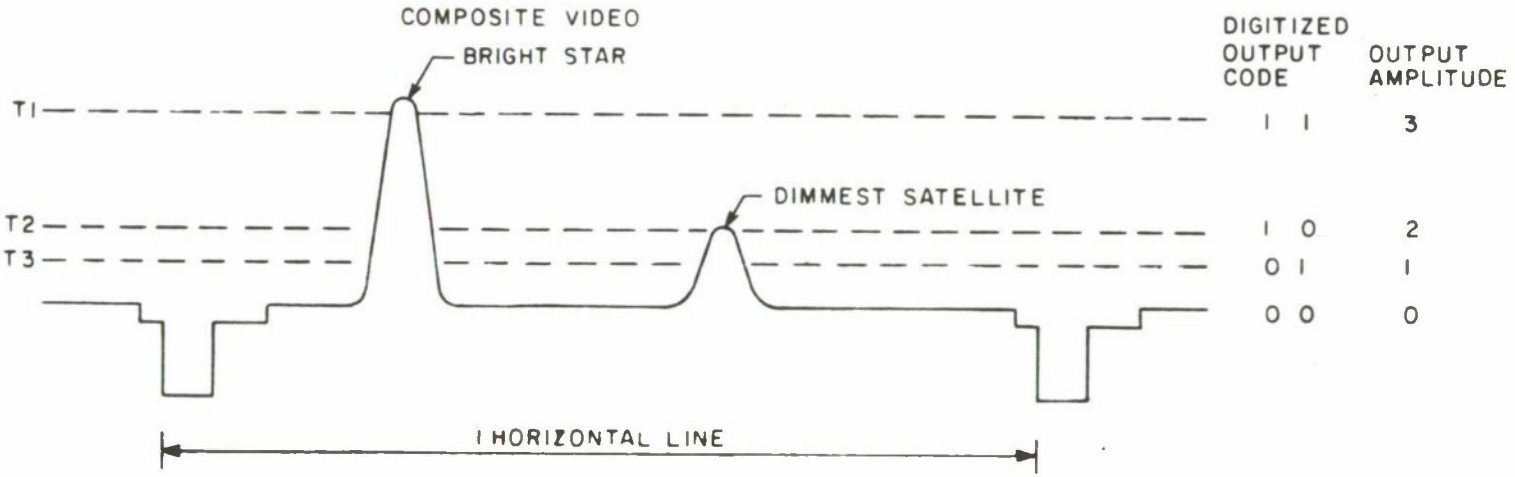


THRESHOLD	PURPOSE	TYPICAL LEVEL
T1-HIGHEST THRESHOLD	BRIGHT STAR DETECTION	NEAR SATURATION OF TV SENSOR
T2-MIDDLE THRESHOLD	TARGET P_d (PROBABILITY OF DETECTION)	16th VISUAL MAGNITUDE
T3-LOWEST THRESHOLD	BACKGROUND ELIMINATION	BACKGROUND LIGHT LEVEL

FIGURE 4. THRESHOLDING AND DIGITIZING

Y window gate which is generated in the preprocessor to provide control over the incoming data. This window gate permits (1) inhibiting TV sensor generated edge transients from overloading the system, (2) reducing the amount of data to be temporarily stored and processed and (3) selecting a target of interest or area of interest to be processed. Other data editing algorithms include amplitude and target extent discrimination of the input data samples which prevent large noise or spurious signals from being processed.

To reduce the amount of data to be processed by the multi-minicomputer processor, extended targets covering many resolution cells such as bloomed stars are represented by a single equivalent data point for each target on each horizontal line. To accomplish this the preprocessor determines the following parameters for each target: amplitude, extent, and X, Y position coordinates.

Two types of targets are defined by the preprocessor and designated here as scattered and non-scattered targets. Non-scattered targets contain image data in consecutive resolution elements (resels) with target extents typically greater than 8 resels. An example of a non-scattered target is an extended target such as a bloomed star. Scattered targets contain image data with extents less than 7 resels and usually consist of several isolated targets.

Memory

The memory consists of a first-in-first-out (FIFO) buffer that reduces the data rate from the input processor to a speed compatible with the multi-minicomputer processor. Special memory timing is provided to control the reading and writing operations. The buffer memory accepts bursts of information at a high input data rate and transfers it out to the minicomputer at a slower regular rate. The FIFO is a read/write random access memory or data storage unit that automatically keeps track of the order in which data was entered into memory and reads the data out in the same order. Writing data into memory has a higher priority than reading data from memory. Between write operations, the minicomputer continually reads out data from memory, if it is not empty, without waiting for the memory to fill up. The maximum memory input and output data rates are approximately 5 MHz. However, the output data rate is determined by the Data General Eclipse minicomputer. The direct memory access data channel of the Eclipse minicomputer is capable of accepting a 16 bit data word at a maximum rate of 1.25 MHz. Since each target detection is represented by a 32 bit data word in the buffer memory, two 16 bit computer words are required to read out one data word from the buffer memory. Memory empty and memory full status indicators are provided to monitor the condition of the memory. These memory status indicators are shown in Figure 3. The buffer memory output data is also displayed on the front panel.

Output Processing

The output processor performs the functions of data formatting, multi-plexing, interfacing of the buffer memory to the Eclipse minicomputer and scattered target processing.

Data formatting and multiplexing of the data from the buffer memory are performed by digital multiplexers. Data transfers between the preprocessor and the Eclipse minicomputer are handled in a direct memory access (DMA) mode. DMA transfers are employed to accommodate the extremely high data rates and also to minimize the time required for I/O processing. When a data transfer is to be made, a DMA cycle is requested by the preprocessor and, when granted, data is transferred directly to the Eclipse minicomputer memory.

The parameters for scattered targets are computed with different logic than that used for non-scattered targets. High speed binary counters are used to calculate the extent and X, Y position for non-scattered targets. A programmable read only memory (PROM) is used to perform these calculations for scattered targets. The PROM is stored with the parameters of all expected target patterns. Since scattered targets are processed in 8 resolution element increments, the PROM contains the pre-calculated parameters for the 256 possible target patterns. The incoming target pattern of zeros and ones, in this 8 bit word, therefore provides the memory address to the PROM. Determining the parameters of a particular scattered target therefore only involves reading a specific data word from the PROM which takes typically 35 nanoseconds.

Control

The control unit consists of timing logic to externally synchronize the scanning of the TV sensor to the high speed sampling clock. The control unit also provides all of the other timing, gating and triggers required for this interface. The requirements of coherent and stable operation are met by the use of a frequency synthesizer which is driven from an oven controlled crystal oscillator. The sampling clock and all other timing signals are derived from the output of this synthesizer.

To externally drive the TV sensor, the following EIA standard, non-interlaced, TV signals are provided: horizontal drive, vertical drive, composite blanking and composite sync. A very versatile and variable rate TV sync generator using programmable counters provides the TV sensor synchronization. The sampling clock frequency is divided down in a programmable counter to generate the horizontal clock rate. The vertical clock rate is then derived from the horizontal clock by a programmable lines/frame counter. All TV sensor

timing control signals are adjustable in 1 usec increments by front panel thumbwheel switches as shown in Figure 3. The combination of the variable rate sync generator and the variable frequency synthesizer provide the flexibility to change the sampling rate and TV scan rate to accommodate varying target and system parameters. The control unit also generates a write gate signal to process and record data in a snapshot mode of operation.

Peripherals

There are also several peripheral units, as shown in Figure 5, associated with the preprocessor and multi-minicomputer processor. An image storage/scan converter and video display monitor provide storage and display of the composite video signal from the TV sensor. Another monitor provides a display of the digitized and processed data from the preprocessor. These displays provide a real time presentation for monitoring system performance and for selecting the optimum threshold levels and data editing algorithms. A synthesizer and pulse generator provide the basic clock or frequency standard for the preprocessor. Signal and power isolation networks are provided for noise and interference rejection during field testing and evaluation at the GEODSS ETS site.

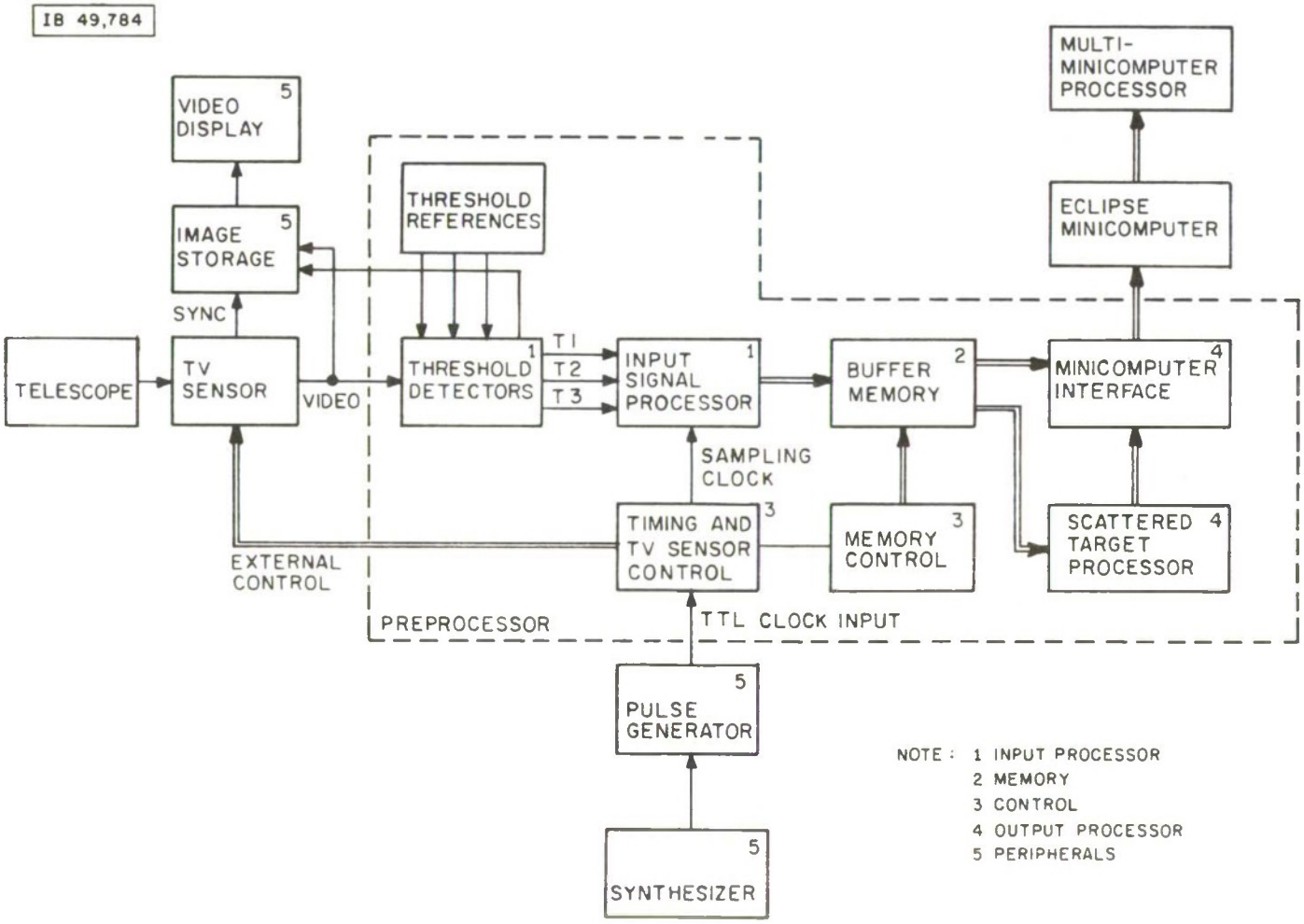


FIGURE 5. MITRE PREPROCESSOR DETAILED BLOCK DIAGRAM

SECTION III

THE MITRE PREPROCESSOR IMPLEMENTATION

This section provides a detailed description of the design and implementation of the preprocessor. The five basic elements of the preprocessor as shown in Figure 5 are (1) input processor, (2) memory, (3) control, (4) output processor and (5) peripheral units.

Input Processor

The input processor performs the following signal processing functions:

a. Thresholding
b. High Speed Sampling and Serial to Parallel Data Conversion
c. Data Reduction and Editing
d. Scattered and Non-Scattered Target Designations
e. Target Parameter Computations
f. Real Time Display

Thresholding

Analog (video) data from the TV sensor must be converted to digital form for subsequent digital signal processing. This is accomplished by (1) time sampling the input analog signal at a rate which is greater than or equal to twice its bandwidth, and (2) quantizing in amplitude the analog signal with a sufficient number of levels to be consistent with the required resolution and accuracy for this application. Quantization consists therefore of converting the analog input into a set of discrete output levels which are represented by a binary code. The data is represented as a sequence of discrete samples of the input signals.

The analog (video) signal is converted to digital form by comparing it with three thresholds designated T_1, T_2 and T_3, where T_3 is the lowest threshold. The threshold reference levels are independently preset between 0 and 1V in steps of 1 mV by switches on the front panel. The actual detection level will be within $\pm$ 2 mV of the reference levels. The original threshold references, which were independently controlled, required a considerable amount of setup time especially during the acquisition of a fast moving target (satellite). Since the differences between thresholds T1 and T2 and between T2 and and T3 are relatively constant regardless of the video signal level, the threshold references have been modified to provide the capability of changing all three reference levels simultaneously. Threshold

reference T1' is now equal to the sum of the original three thresholds T1, T2 and T3. Threshold T2' is equal to T2 + T3 while threshold T3 was not changed. It is now only required to vary threshold T3 to change all threshold reference levels simultaneously and still maintain the voltage differences between T1, T2 and T3. The rejection of the changing sky background level is now accomplished by only varying threshold T3.

After the threshold comparisons are performed, a two bit code is set indicating which of the thresholds the video exceeds. This output code which represents the amplitude or intensity of the input signal is shown in Figure 4 for a typical video input signal; approximate threshold reference levels are also indicated. Only video signals that exceed the lowest threshold T3 are processed.

With three thresholds, eight output codes are possible as shown in Figure 6. However, only four of these codes are possible for the condition T1 $\geq$ T2 $\geq$ T3 which is required to provide correct amplitude information. High speed combinational logic is included to convert the three threshold signals to a 2 bit binary word. The logic equations implemented for this 3 line to 2 line decoding are,

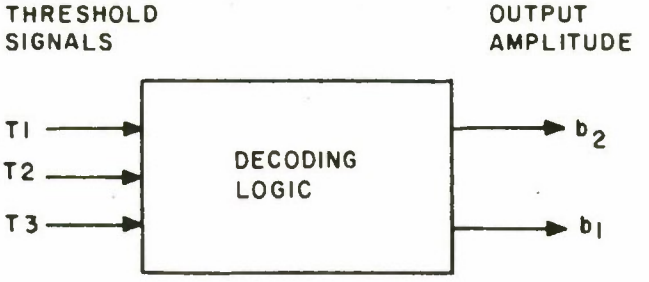
$$b_2 = T_1 + T_2$$

$$b_1 = T_1 + T_3 \cdot \bar{T}_2$$

where b_2 and b_1 refer to bit 2 and bit 1, respectively, and bit 2 is the most significant bit (MSB) of the 2 bit amplitude word. The analog (video) data is therefore quantized by the threshold detectors and combinational logic to 4 discrete levels.

The analog-to-digital conversion of the input data is performed by the threshold detectors shown in Figure 7. Each threshold detector consists of a very high speed voltage comparator which has an analog input and digital output. It accepts two analog inputs (video and threshold reference) and generates a ZERO or ONE output depending on which input is larger. It is therefore a basic, one-bit, analog-to-digital converter.

Comparators are generally wideband, high gain, open loop, devices designed for speed which therefore have a tendency to produce rf oscillations. It is also extremely difficult to obtain a comparator that is fast and still offers simultaneously good input characteristics of high input impedance and low offset voltages.



THRESHOLDS			OUTPUT		INPUT	
T1	T2	T3	b_2	b_1	SIGNAL LEVEL	
0	0	0	0	0	*	NO SIGNAL
0	0	1	0	1	*	T3 EXCEEDED
0	1	0	1	0		
0	1	1	1	0	*	T2 AND T3 EXCEEDED
1	0	0	1	1		
1	0	1	1	1		
1	1	0	1	1		
1	1	1	1	1	*	T1, T2 AND T3 EXCEEDED

* POSSIBLE CODES FOR $T1 \geq T2 \geq T3$

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FIGURE 6. THRESHOLD DECODING

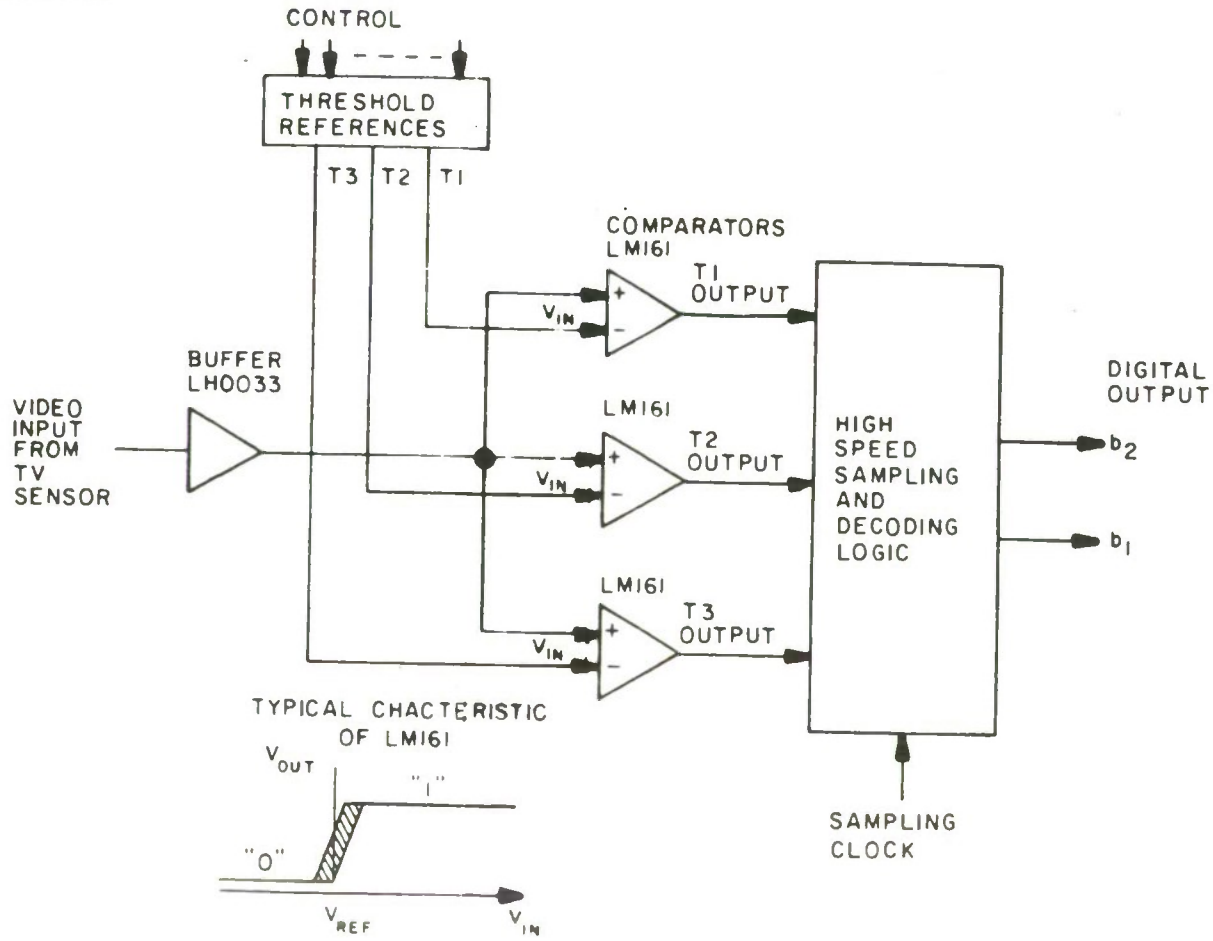


FIGURE 7. THRESHOLD DETECTORS AND HIGH SPEED SAMPLING AND DECODING LOGIC

In selecting the comparator, the two major factors that were considered were accuracy and speed. Other factors which also had to be considered were logic compatibility, power supply requirements, offset voltage drift and input impendance.

The comparator accuracy is primarily controlled by two factors - the true offset voltage error and the gain error which is the amount of signal required to cause the comparator to switch. As defined by most manufacturers, the "input-offset error" accounts for both of these error terms. Usually, the comparator with the lowest offset voltage has the best resolution but not necessarily the best stability.

Several high speed comparators were tested and evaluated. The circuit layout and component selection for most of the very high speed emitter-coupled logic (ECL) comparators was extremely critical. The LM161 voltage comparator (TTL output) manufactured by National Semiconductor was finally selected for this application because of its relatively high speed (20 nsec), low input offset voltage (typically 1 mV) and good stability.

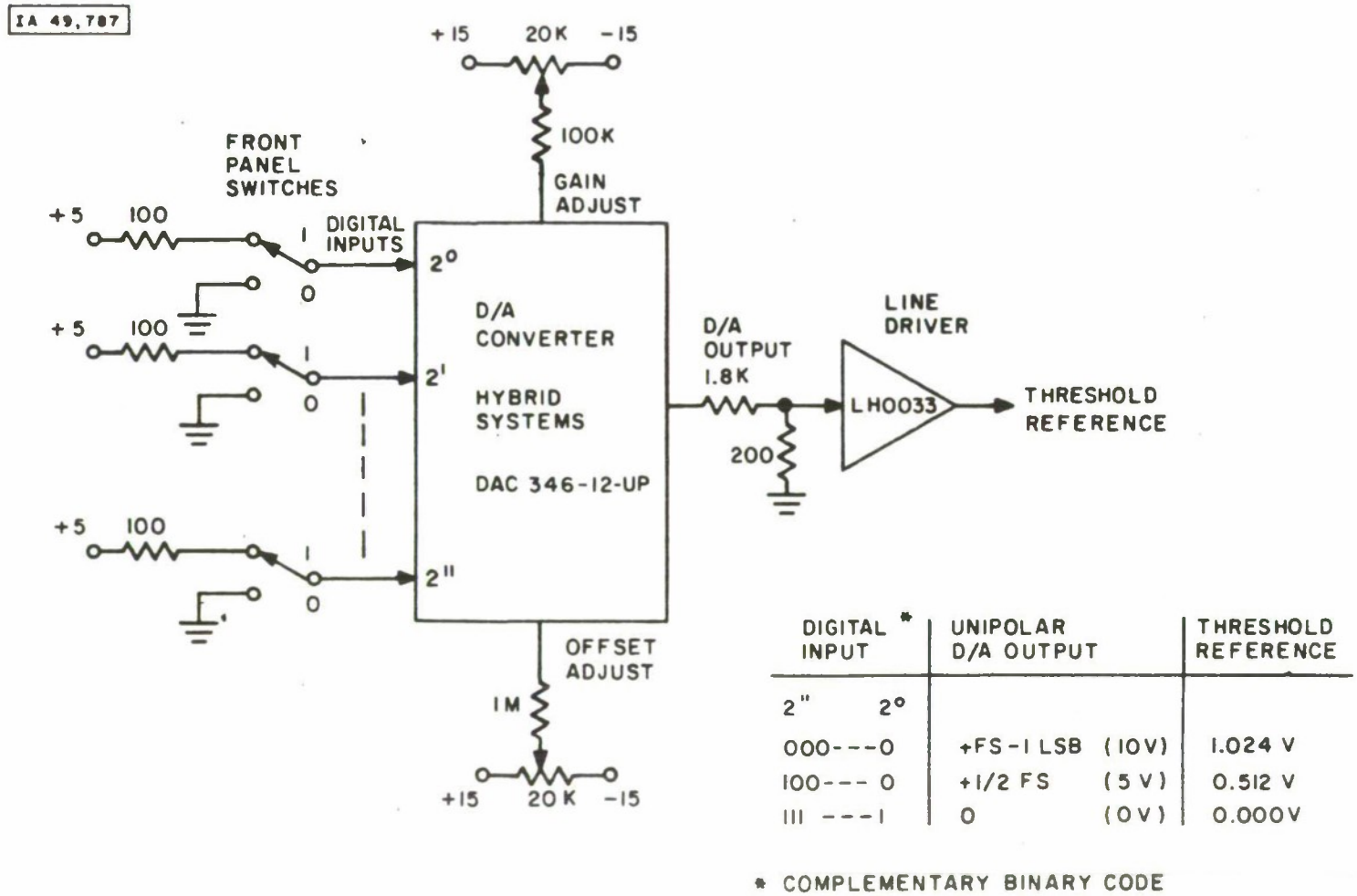
Digital-to-analog converters are used to establish the reference inputs to the threshold detectors. A typical threshold reference circuit is shown in Figure 8. The D/A converter converts the digital input code into its equivalent voltage level. All three threshold references are controllable from front panel switches.

The D/A converter for each threshold reference is a 12 bit, ultra-stable, hybrid integrated circuit manufactured by Hybrid Systems Corporation. The key features of the D/A converter are: 12 bit linearity, low drift of 1 PPM/^{o}C and built in reference ladder switches. The digital input code for the D/A converter is complementary binary and is included on Figure 8.

The line driver is a National Semiconductor LH0033 linear integrated circuit. The LH0033 is a high speed, FET input, voltage follower capable of providing $\pm$ 100 mA of continuous output current at frequencies from DC to over 100 MHz.

High Speed Sampling and Serial to Parallel Data Conversion

To accommodate the wideband video signals (up to 15 MHz) from the TV sensor, high speed sampling of the video is performed at rates up to 30 MHz providing a resolution of 33 nsec. Since the maximum input data rate of the buffer memory is typically 5 MHz, a high speed data converter is required before the buffer memory.



DIGITAL * INPUT	UNIPOLAR D/A OUTPUT		THRESHOLD REFERENCE
2" 2°			
000---0	+FS-1 LSB	(10V)	1.024 V
100---0	+1/2 FS	(5 V)	0.512 V
111---1	0	(0 V)	0.000V

* COMPLEMENTARY BINARY CODE

FIGURE 8. THRESHOLD REFERENCE

The serial to parallel converters as shown in Figure 9 provide the high speed sampling and storage of the input data. This conversion enables a reduction in the data rate of signals entering the buffer memory. An 8:1 serial to parallel conversion is accomplished in a two step process (2:1 and 4:1) with the high speed serial and parallel registers as configured in Figure 9. The input data is sequentially clocked into the registers on the low-to-high transition of the clock input. The gate at the input of the serial register permits control over the incoming data. The input data is ANDED with a window gate. This gating process is described in more detail in the data reduction and editing section of this report.

To operate the serial and parallel registers at sampling rates up to 30 MHz required the use of high speed Schottky registers or latches. The input data is sequentially entered into the serial shift register at the input clock rate while the input data to the parallel register is entered at 1/8 the input clock rate. The output data from the parallel register is then transferred to the buffer memory at the reduced rate of 1/8 the input sampling rate. An 8:1 reduction in the data word rate is thereby achieved.

Data Reduction and Editing

Data reduction and editing logic in the preprocessor provide the capability to eliminate most of the spurious and redundant data. The preprocessor is also capable of inserting data into or deleting data from a block of information passing through it. The preprocesor provides data editing of the input data samples according to the five algorithms described below. These algorithms are configured as shown in Figure 10. Data editing algorithms S and D precede algorithms A B, or C. All data editing algorithms are selected by front panel thumb switches. These algorithms can best be explained by the examples in the following paragraphs.

Algorithm S provides a digital selection of a portion of a frame to be processed. The primary reasons for using this algorithm are:

a. To inhibit TV sensor generated edge transients from overloading the system.

b. To reduce the amount of data which is temporarily stored and processed.

c. To select a target of interest or area of interest to be processed.

Algorithm S is accomplished with an X, Y window gate generated within the control unit of the preprocessor. This is a composite gate con-

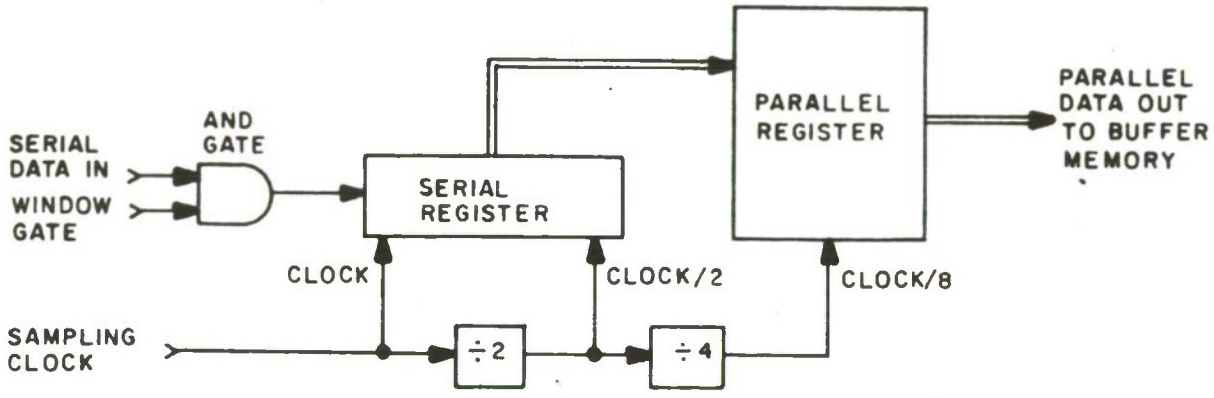


FIGURE 9. SERIAL TO PARALLEL DATA CONVERSION

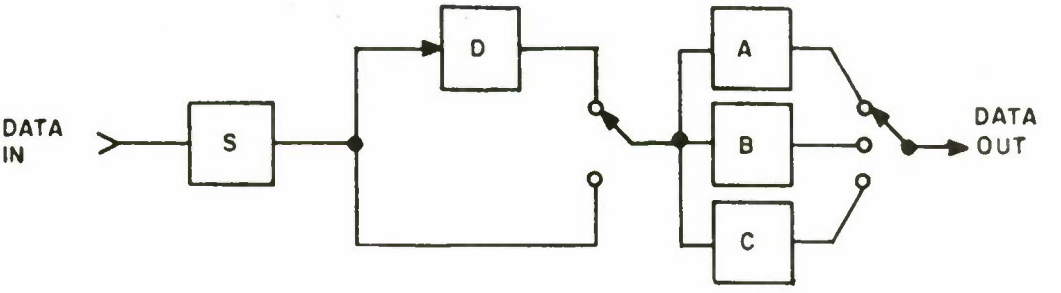


FIGURE 10. DATA EDITING

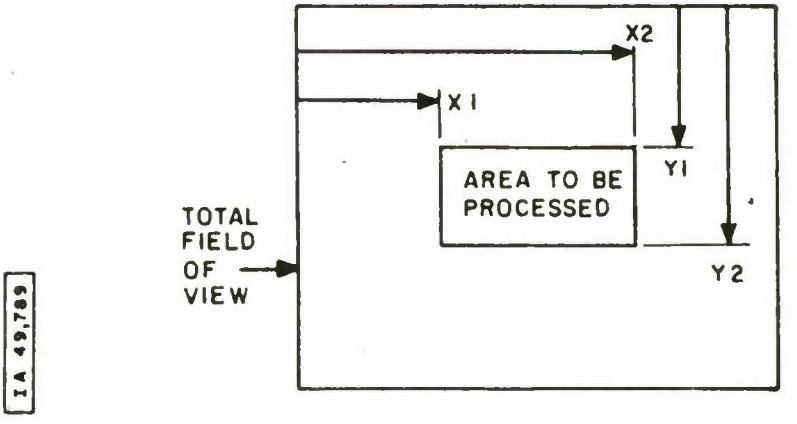


FIGURE 11. ALGORITHM S WINDOW GATING

sisting of both line and frame gates. The window gate is ANDED with the input data to provide control over the incoming data. The X1, X2 and Y1, Y2 position coordinates as shown in Figure 11 are selected in increments of 8 resels from front panel switches. For sampling intervals of 33 nsec/resel, the window area is therefore selectable in 264 nsec increments.

Algorithm D prevents the storage and processing of large, narrow width, noise or spurious signals. This algorithm provides amplitude and target extent discrimination of the input data samples. If the target amplitude exceeds threshold T1 (highest threshold) and the target extent (ΔX) is equal to 1 (zeros on either side of the signal), the input signal is inhibited. All other input data samples are passed through unaltered. This algorithm is illustrated by the top two graphs in Figure 12. The output signals from this data editing logic are shown for algorithm D either bypassed or selected. This algorithm provides discrimination against noise since very strong targets will be dispersed over many resels and thus a single very strong input level can be dismissed as noise.

Algorithm A performs no data editing functions after algorithms S and D. This provides the capability to pass the data directly from D to the output unaltered.

Algorithm B performs target extent discrimination of the input data samples. Only targets with extents (ΔX) of 2 or more resels are processed regardless of the input amplitude. This algorithm is illustrated by the two middle graphs in Figure 12. This algorithm performs the function of algorithm D for all signal levels.

The primary purpose of all the data editing algorithms is to reduce the amount of data to be processed by the multi-minicomputer processor. If the amplitude level of a target falls below the lowest threshold level for one sampling interval or resel it will be classified as two targets. Algorithm C provides the capability to fill in this gap in the data and thus present only one target to be processed. This algorithm is illustrated by the bottom two graphs in Figure 12.

Scattered and Non-Scattered Target Designations

Two types of targets are defined by the preprocessor and designated here as scattered and non-scattered targets. A few examples of these targets are illustrated in Figure 13. Non-scattered targets contain image data of any extent or length in consecutive resolution cells which start from either the top or bottom of the C register as shown in the illustration. The C register provides temporary data storage of the input samples. Scattered targets contain image data

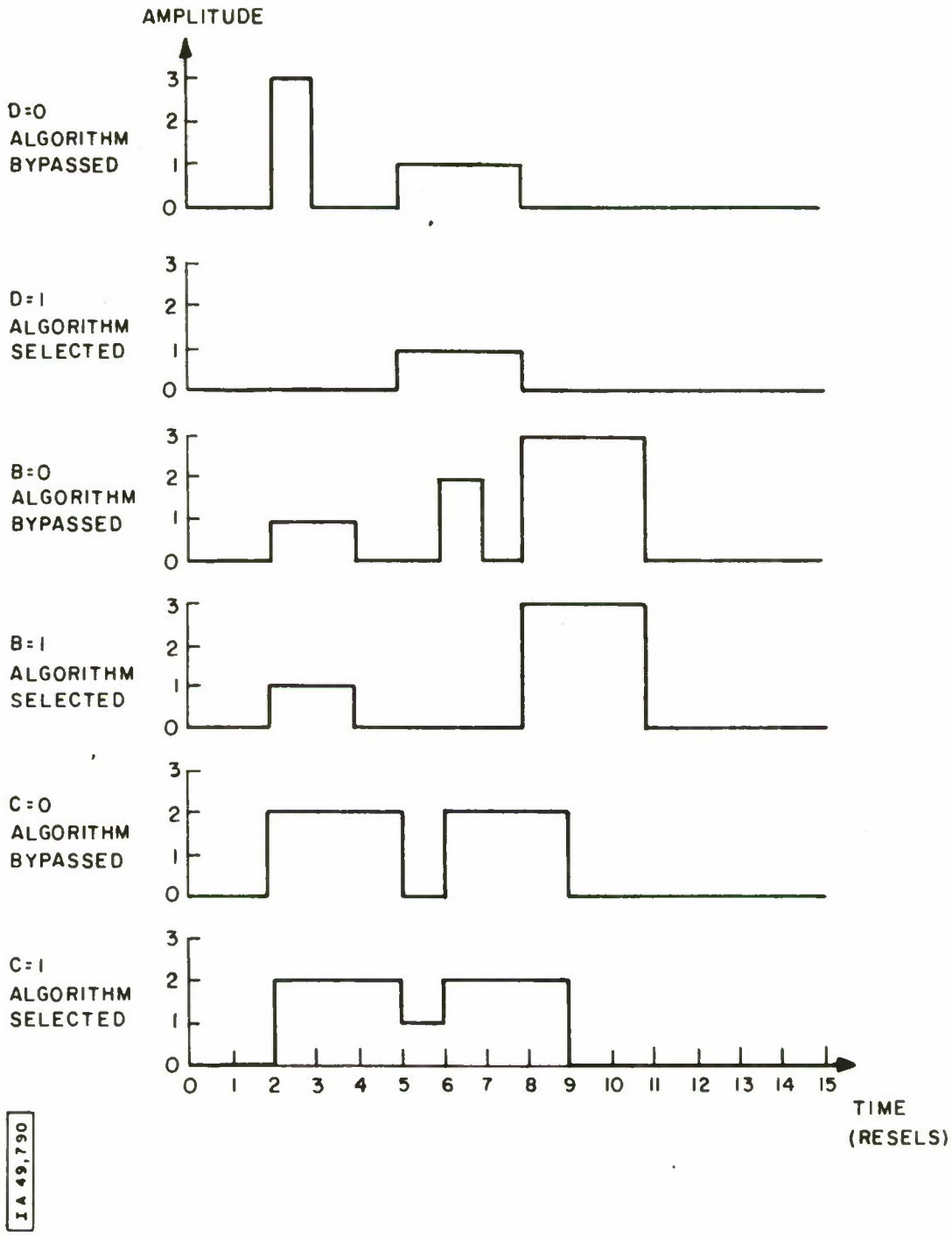


FIGURE 12. DATA EDITING TIMING DIAGRAM

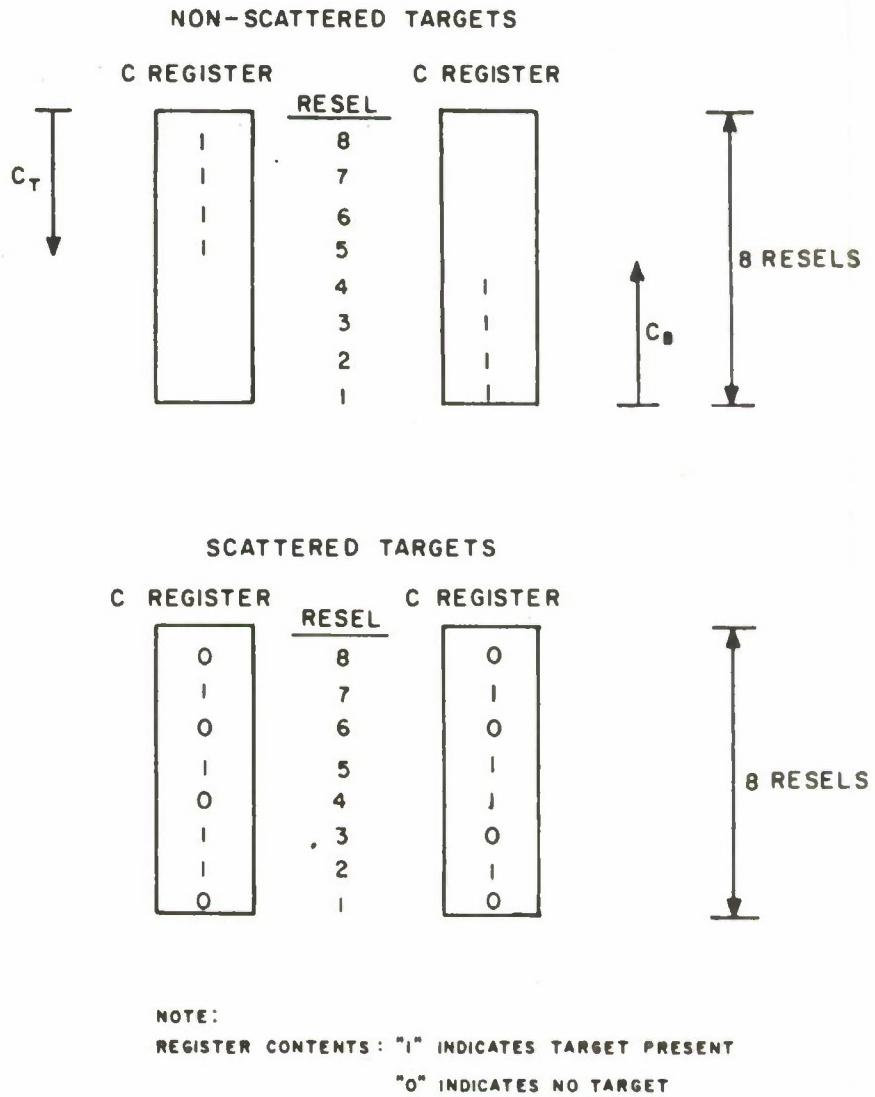


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FIGURE 13. NON-SCATTERED AND SCATTERED TARGET EXAMPLES

with extents less than 7 resolution cells and consist of several isolated targets. Scattered targets also contain at least one zero on both sides of at least one target in resolution cells 2 through 7. Also, if the previous target was scattered, then the present target is considered scattered unless the C register is full.

In Figure 13 the value of C_T is a binary number between 0 and 7 which represents the number of consecutive resolution cells that are filled from the top of the C register. The value of C_B is also a binary number between 0 and 7 except it is measured from the bottom of the C register. In this example, C_T and C_B are both equal to four. These values are used in determining the extent of a non-scattered target. They are inputs to the extent counter, shown in Figure 14, which is discussed in the following paragraphs.

Target Parameter Computation (Non-Scattered Only)

As described earlier, the preprocessor performs high speed sampling and quantizing of the video signal from the TV sensor. However, in order to reduce the amount of data to be temporarily stored and processed by the multi-minicomputer processor, initial centroid processing of the data is performed. All targets are represented by a single equivalent data point on each horizontal line. Several parameters are determined for each target (star or satellite) which completely describe it and require processing fewer data words. Associated with target amplitude and extent parameters are X, Y coordinate information describing the target's position which is necessary for MTI processing.

A functional diagram of the high speed counters that compute the target parameters for non-scattered targets is shown in Figure 14. The two inputs to the extent counter, C_T and C_B, were defined earlier in Figure 13. Scattered target parameters are computed by the scattered target processor which is described in this section. The measurement of target extent for non-scattered targets is described in Appendix A. The rules for recording or storing data for both scattered and non-scattered targets are included in Appendix B.

In Figure 15, a typical video input signal is shown along with the preprocessed output data. Also shown in this figure is a typical representation of a target displayed on a monitor. Each resolution cell is sampled by the preprocessor and if the data samples exceed threshold T_3, the data is stored temporarily in high speed registers while the parameter computations are performed. In this example, the processing of only one horizontal line is illustrated. The same process is performed for each horizontal line. For this particular example, the targets have the following parameters:

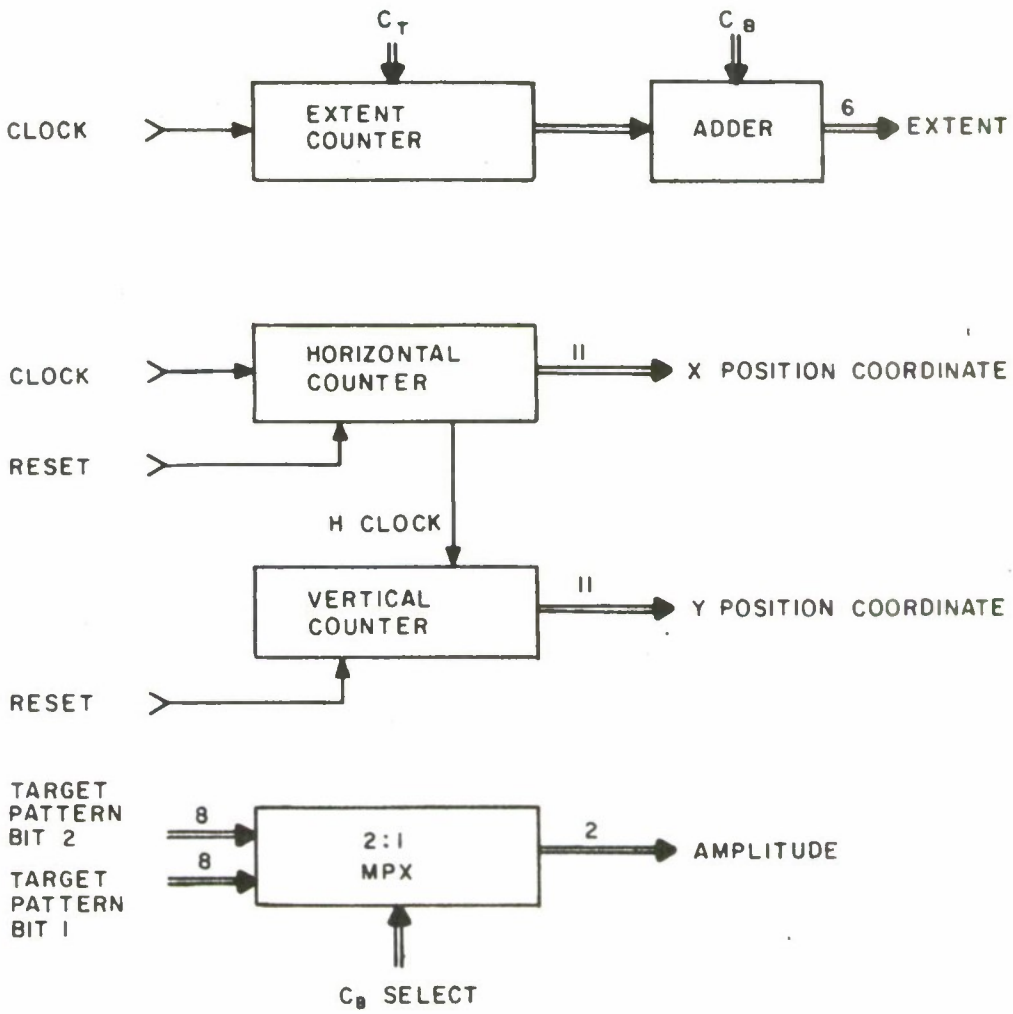

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FIGURE 14. NON-SCATTERED TARGET PARAMETER COMPUTATION LOGIC

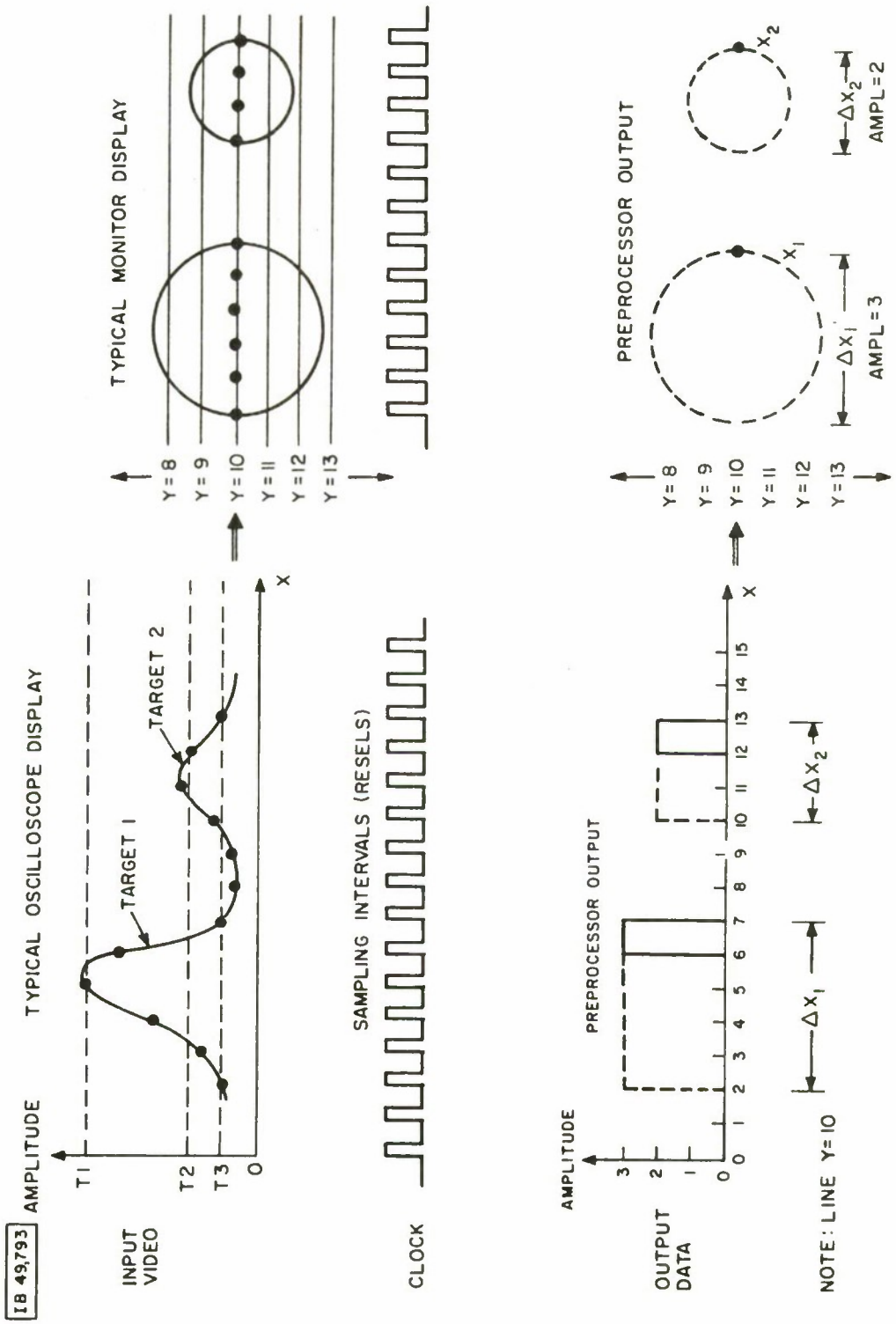

FIGURE 15. TYPICAL VIDEO INPUT SIGNAL/PREPROCESSOR OUTPUT DATA

Parameter	Target 1	Target 2
Amplitude	3	2
Extent	5	3
X position	7	13
Y position	10	10

As shown in Figure 15, the output amplitude is the largest amplitude of the video during the excursion of each target and the extent is the width of the target measured at the T3 threshold level. The X position of each target is the final horizontal position of the target that is at or above the T3 threshold level. The Y position corresponds to the particular TV scan line and is the same for these two targets since they are on the same line. As shown in this example, the amount of data to be processed has been considerably reduced - a 6 to 1 reduction for target 1 and a 4 to 1 reduction for target 2. The amount of data reduction is directly proportional to the size of the target.

Memory

A buffer memory is required to interface the preprocessor with the Eclipse minicomputer of the multi-minicomputer processor due to the different data rates and asynchronous operation of these two subsystems. The buffer memory must be able to accept information at a high input data rate and to transfer it out to the minicomputer at a slower regular rate. The buffer memory must also provide temporary storage of high speed data bursts.

To accomplish these functions, the buffer memory has been based on a first-in-first-out (FIFO) design. A functional diagram of the buffer memory is included in Figure 16. The FIFO is a read/write memory or data storage unit that automatically keeps track of the order in which data was entered into memory and reads the data out in the same order. The FIFO acts here as a variable length memory between two subsystems that operate at different speeds. The FIFO therefore provides an effective storage capacity that is much larger than the actual FIFO capacity. If the average rate of input data bursts is less than the output data rate, an infinite storage capacity is achieved.

The FIFO buffer memory has been implemented with random access memory (RAM) chips. Counters are used to generate the write and read addresses. Input and output registers are also employed for latching or storing the data. Since the random access memories have a single set of address lines to select the memory location, the address lines have to be shared for both read and write operations. Therefore, it is not possible to write into the memory while reading an output. A multiplexer is used to select the appropriate address counter for a write or read operation and the counter is incremented at the end of

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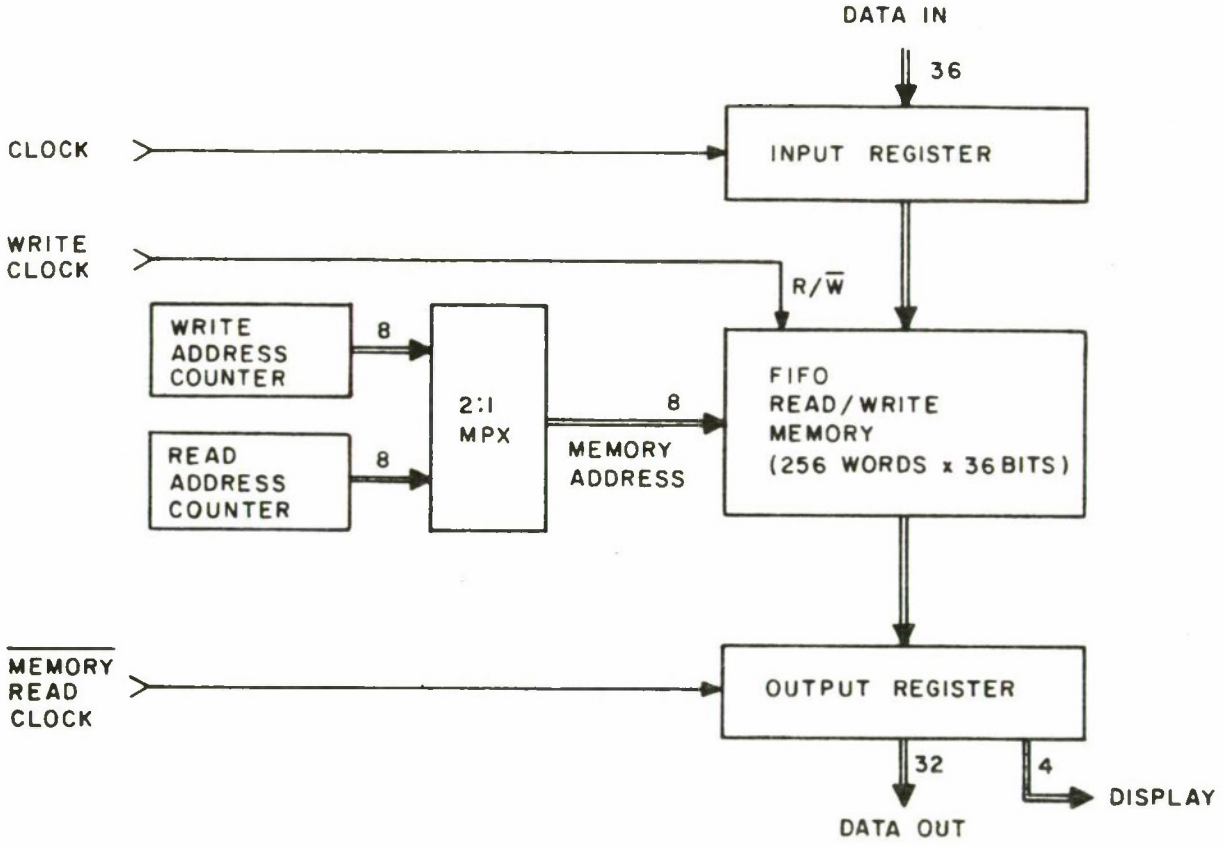

FIGURE 16. BUFFER MEMORY

the cycle, so that the next write or read opeation will occur at the next counter address. Since the location of the next write or read operation is held in independent counters, writing and reading can be randomly intermixed. However, a write operation has higher priority than a read operation. Between write operations, the minicomputer continually reads out data from the memory, if it is not empty, without waiting for the memory to fill up.

The high speed FIFO memory consists of 16 Signetics 82S09 bipolar random access memory chips; each 82S09 chip is a 576 bit, Schottky clamped TTL, random access memory organized as 64 words by 9 bits per word. The capacity of the FIFO memory consisting of these 16 chips is 256 words by 36 bits. The memory can therefore accept data bursts of up to 256 words. The output data from the memory is the complement of the input data. Maximum input and output data rates are approximately 5 MHz. However, the output data rate for this application is determined by the Data General Eclipse minicomputer which is capable of accepting a 16 bit data word at a maximum rate of 1.2 MHz. Two 16 bit computer words are required to read out each data word from the memory.

It should be noted that only the most significant data stored in the buffer memory (2 x 16 = 32 bits) is transferred to the Eclipse minicomputer. The other 4 bits of data which is primarily status information is displayed on the front panel. It would have required three computer words to transfer all 36 bits of data from the memory, which would slow down the data rate to the multi-minicomputer processor.

Input and output registers of the memory provide temporary data storage. The output register stores the data until the minicomputer is available to take away the data. The input and output registers consist of 6 high speed 74S174 latches.

Typical timing waveforms are shown in Figure 17 for inputting and outputting data from the buffer memory. A record time pulse is generated for all targets that exceed T3, the lowest threshold. The record time pulse initiates a write operation. At the end of this pulse a read operation begins. The read operation continues, as long as there is valid data in the memory, until another write operation is initiated. Both address counters are initially reset to zero at the beginning of each TV frame. During the early part of the write cycle, an address is sent to the FIFO specifying the location of the word to be written. The first word entered is stored in address zero. Since the positive edge of the write clock increments the write address counter, each data entry will automatically increment the counter to the next memory location. The data is stored in memory approximately 50 nsec after the high to low transition of the write clock. During the read operation, the read clock transfers the data from the FIFO into the output register and also increments the read counter.

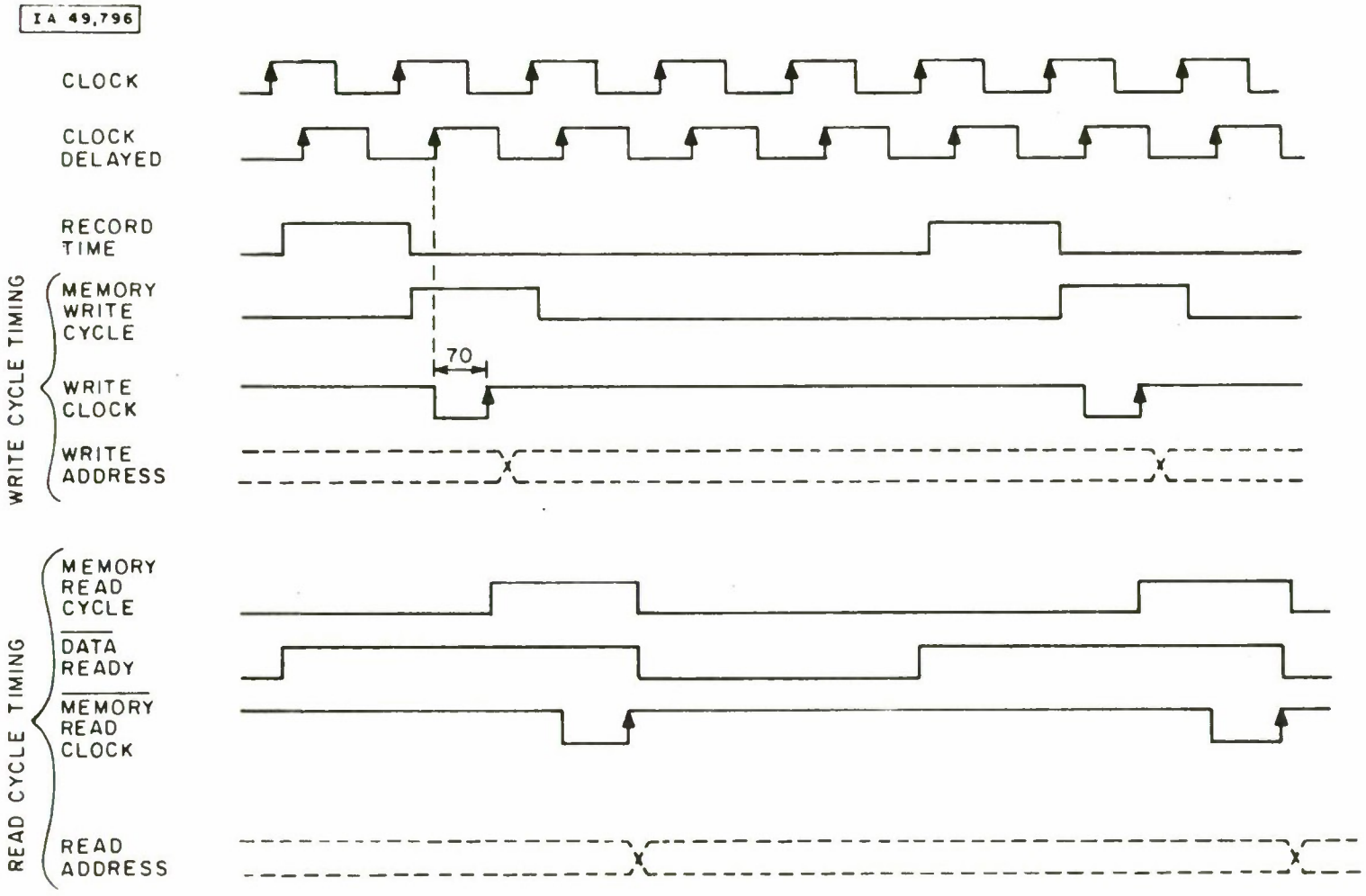

FIGURE 17. MEMORY TIMING

Data is stored in the buffer memory in two different formats as shown in Figure 18, one for non-scattered targets and another for scattered targets. This data is then rearranged and sent to the Eclipse minicomputer using a two word (16 bits per word) format. This data formatting and multiplexing are performed in the output processor.

Status indicators or flags are provided by the preprocessor to indicate the condition of the buffer memory. A memory empty flag is provided to show that there is no valid data in the memory. The memory empty control signal permits a write operation, if data is available, but inhibits a read operation. The memory full flag inhibits new data from overwriting good data already in the memory before it has been transferred to the minicomputer. The memory full control signal therefore permits a read operation but inhibits a write operation.

An identity comparator is used to compare the write and read address counters. When the address counters are at the same binary number, the memory is empty. When the write address counter reaches its maximum count and the read counter is zero, the memory is full. If the input data exceeds the capacity of the buffer memory, the new data is discarded until the present data has been taken away by the minicomputer. A memory full indicator is provided on the front panel to display this condition.

Output Processor

The output processor as shown in Figure 19 performs the following signal processing functions:

a. Data formatting and multiplexing
b. Scattered target processing
c. Preprocessor and Eclipse minicomputer interface

Data Formatting and Multiplexing

Since the input data word of the Eclipse minicomputer is only 16 bits, the 32 bit output word from the buffer memory is multiplexed and transferred to the Eclipse minicomputer using two 16 bit words. The data is also reformatted as shown below. This multiplexing and reformatting of the output data from the buffer memory is accomplished with digital multiplexers as shown in Figure 19. Each detection is represented by two 16 bit words. The data format is as follows:

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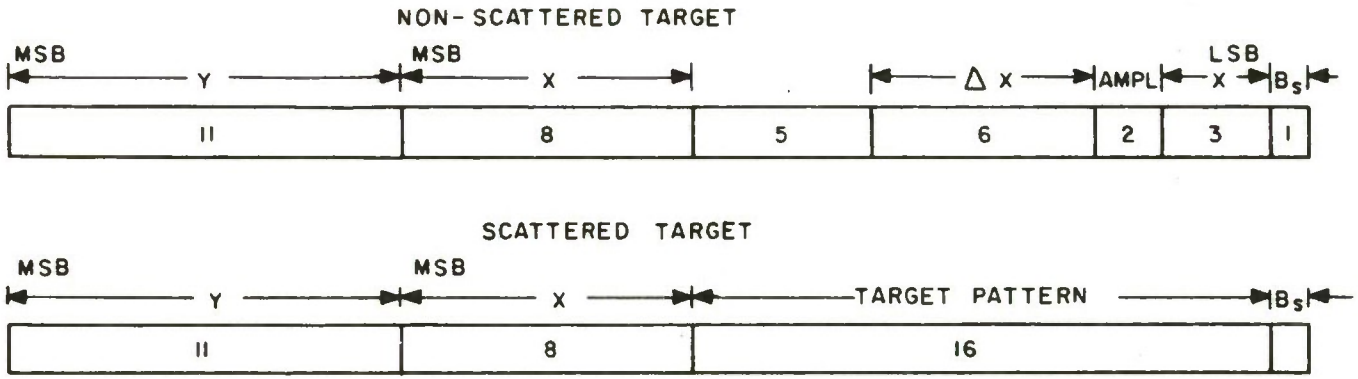


FIGURE 18. BUFFER MEMORY DATA FORMATS

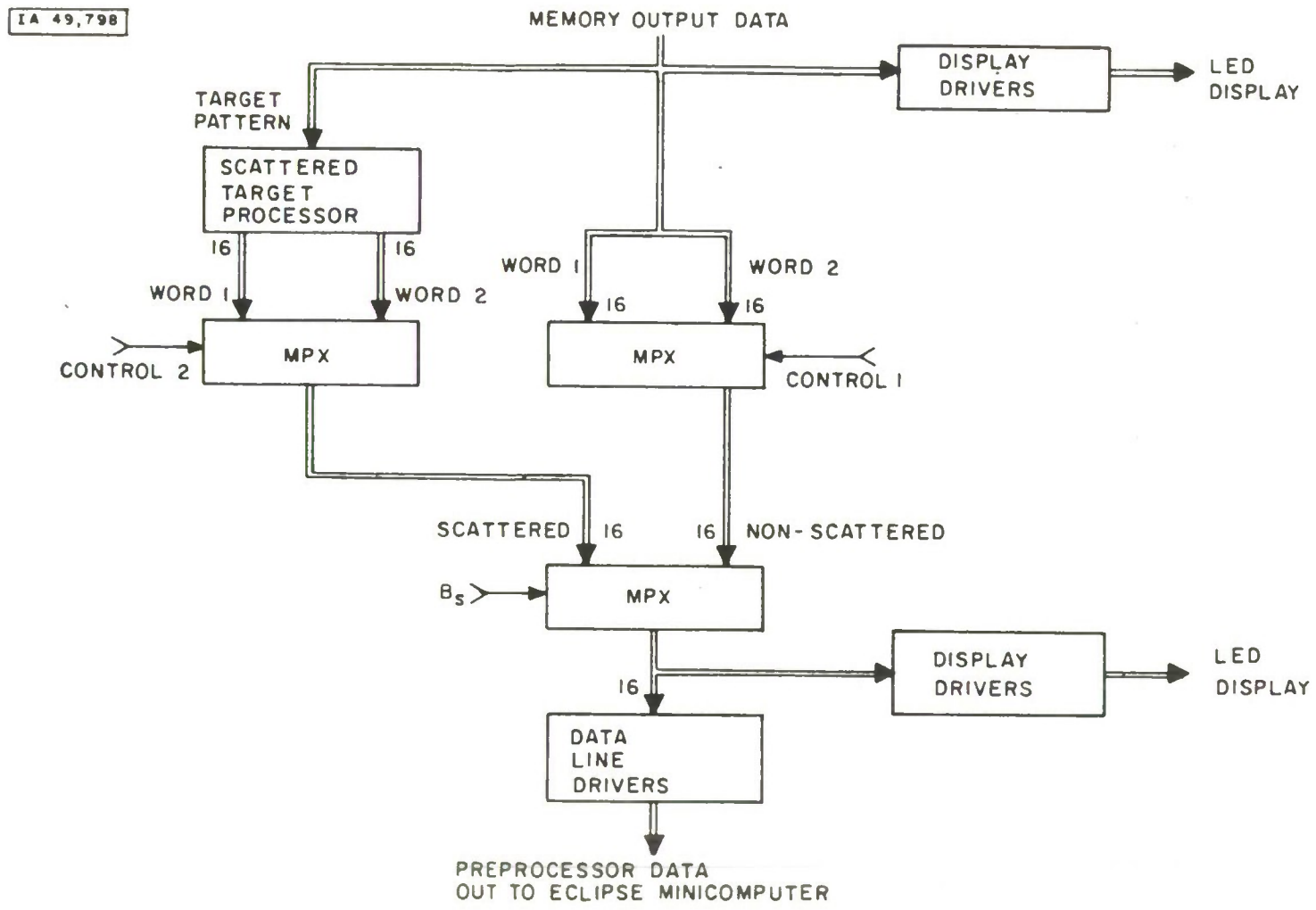
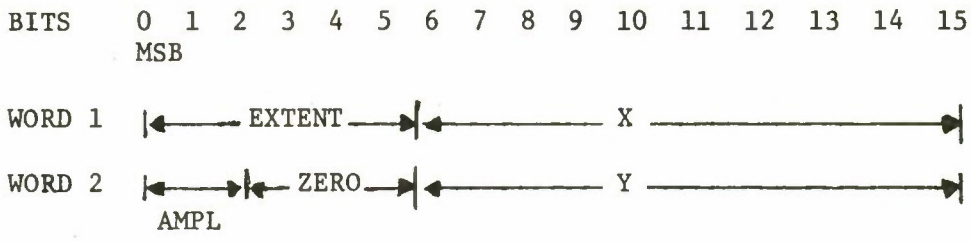


FIGURE 19. OUTPUT PROCESSOR



Word 1 contains the target extent data, ΔX, in the first 6 bits and the X position coordinate in the remaining 10 bits. Word 2 contains the target amplitude in the first 2 bits and the Y position coordinate in the last 10 bits.

Control signals 1 and 2 select the order that the data words are sent to the minicomputer. Word 1 is always sent first followed by word 2. Control signal B_S performs the selection between scattered or non-scattered targets. For a scattered target $B_S = 1$ and therefore $B_S = 0$ for a non-scattered target.

Scattered Target Processing

A functional block diagram of the scattered target processor is shown in Figure 20. As defined earlier, a scattered target consists of one or more isolated targets with extents less than 7 resolution cells. A typical example of a scattered target is shown in Figure 21.

The parameters for scattered targets are computed with different logic than that used for non-scattered targets. High speed binary counters are used to calculate the extent and X, Y position for non-scattered targets. A programmable read only memory (PROM) is used to perform these calculations for scattered targets. The PROM is stored with the parameters of all expected target patterns. Since scattered targets are processed in 8 resolution element increments, the PROM contains the pre-calculated parameters for the 256 possible target patterns. The incoming target pattern of zeros and ones, in this 8 bit word, therefore provides the memory address to the PROM. Determining the parameters of a particular scattered target therefore only involves reading a specific data word from the PROM which takes typically 35 nanoseconds. As shown in Figure 21, the extent of the scattered target is defined as ΔX.

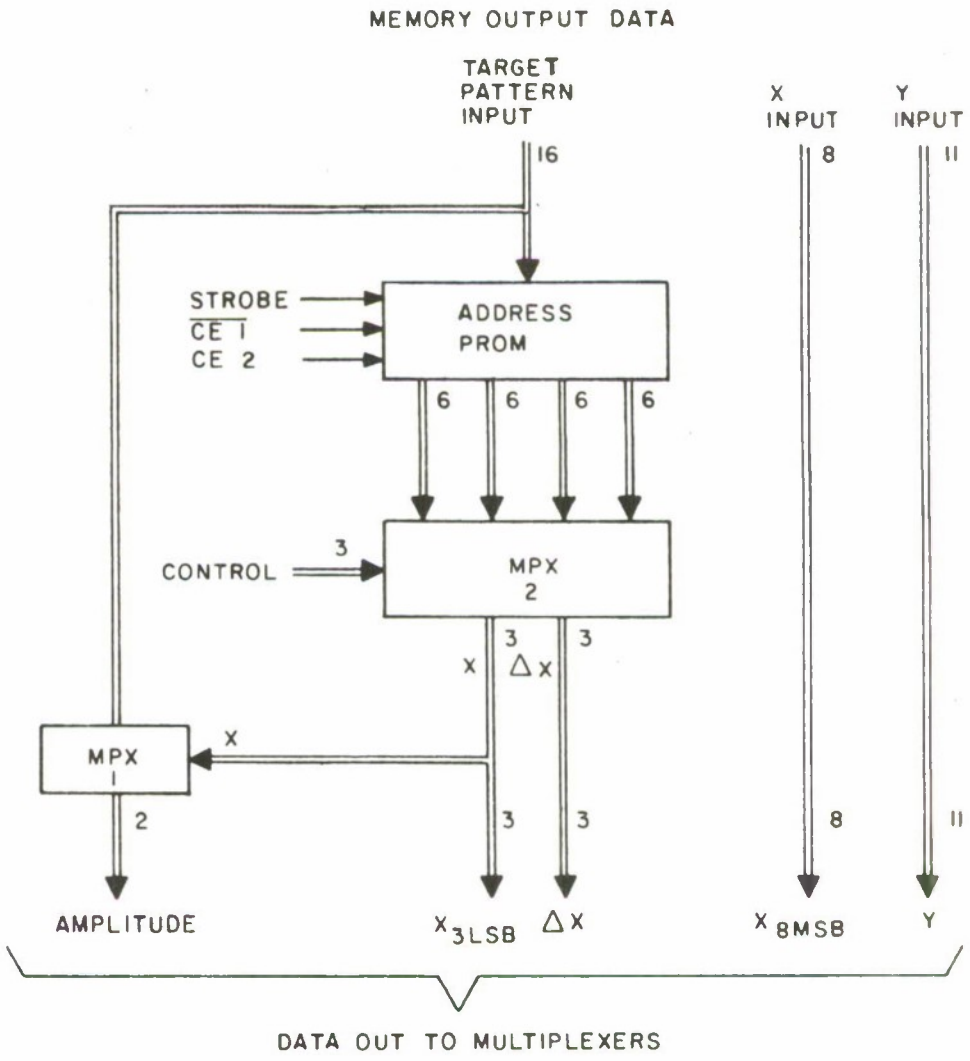


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FIGURE 20. SCATTERED TARGET PROCESSOR

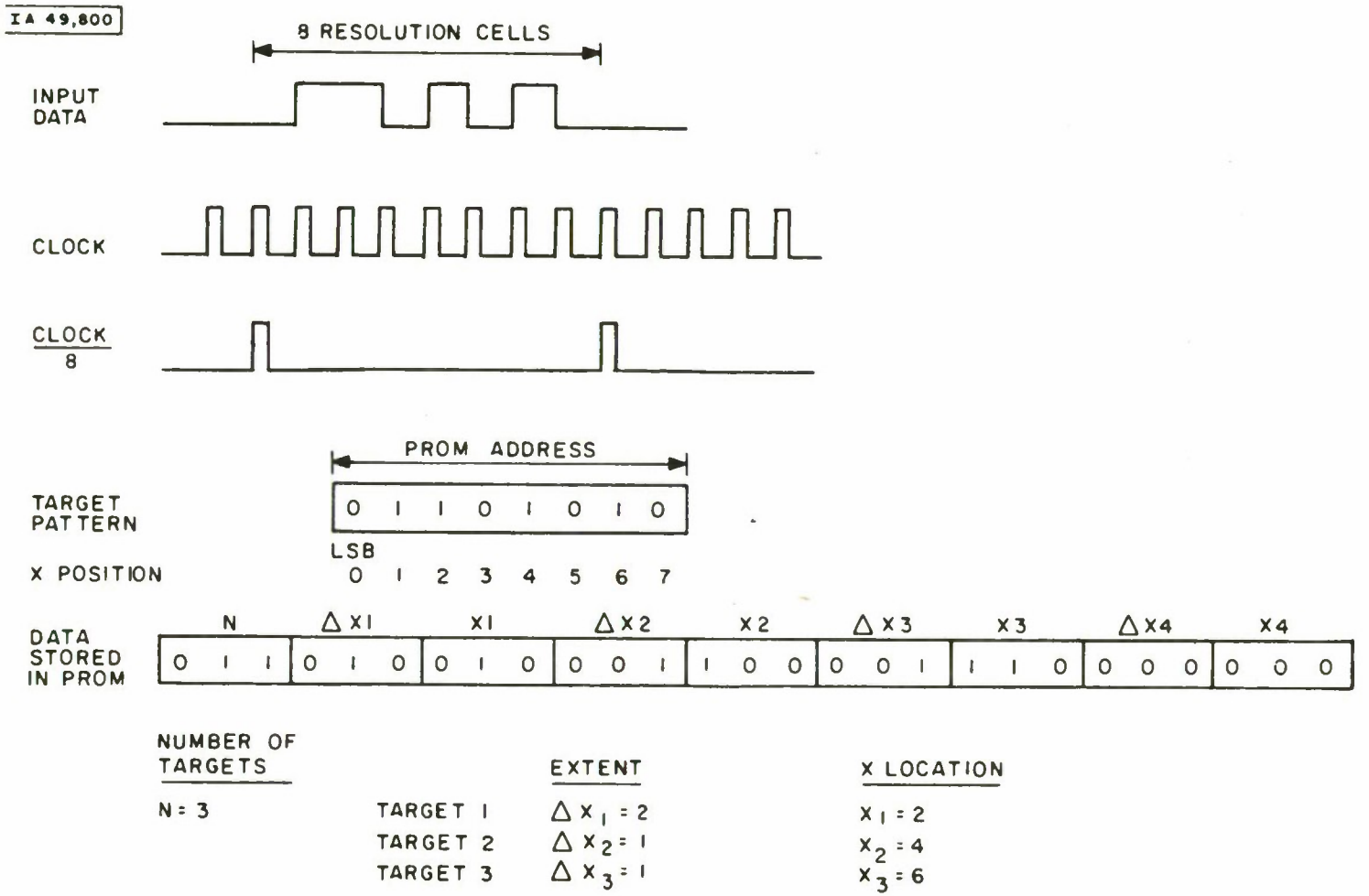

FIGURE 21. SCATTERED TARGET EXAMPLE

The scattered target processor determines the amplitude, extent and the least significant 3 bits of the X position which is defined as X_{3LSB}. The most significant bits of the X position (X_{8MSB}) and the Y position coordinate are transferred directly from the memory to the data multiplexers.

The scattered target processor includes five Signetics 82S115 PROMS. Each 82S115 includes on chip data output registers, address decoding and two chip enable inputs. The 82S115 PROM is organized as a 512 word by 8 bit memory with tri-state outputs provided for data bus organizations. For this application, the PROMS are operated in a transparent read mode where the stored data is addressed by applying a binary code to the address inputs while holding the strobe high.

The 82S115 PROM is a 4096 (512X8) bipolar, fusible link, read only memory that can be easily programmed by the user. The address of each successive location in the PROM is set on one set of switches and the instruction to be entered at the location is set on another set of switches. A high energy pulse is used to blow out a small nichrome fusible link inside the PROM at the address location where logic ones are desired. Logic zeros appear where the links remain intact.

Preprocessor/Eclipse Minicomputer Interface

The transfer of data from the preprocessor to the Eclipse minicomputer is controlled by interface logic provided in the Eclipse minicomputer and in the MITRE preprocessor. In Figure 22 are shown the control and data paths for this interface. Data transfers between the preprocessor and the Eclipse minicomputer are handled in a direct memory access (DMA) mode. Direct memory access transfers are employed to accommodate the extremely high data rates and also to minimize the time required for I/O processing.

The definitions of terms used in this section, as well as in other sections, are included in the glossary. More detailed information concerning the Eclipse minicomputer interface is included in reference 1.

The Eclipse I/O and Preprocessor I/O interfaces are described in detail in Appendix C. An introduction and overview of the Data General minicomputer high speed interface or data channel is included in Appendix D.

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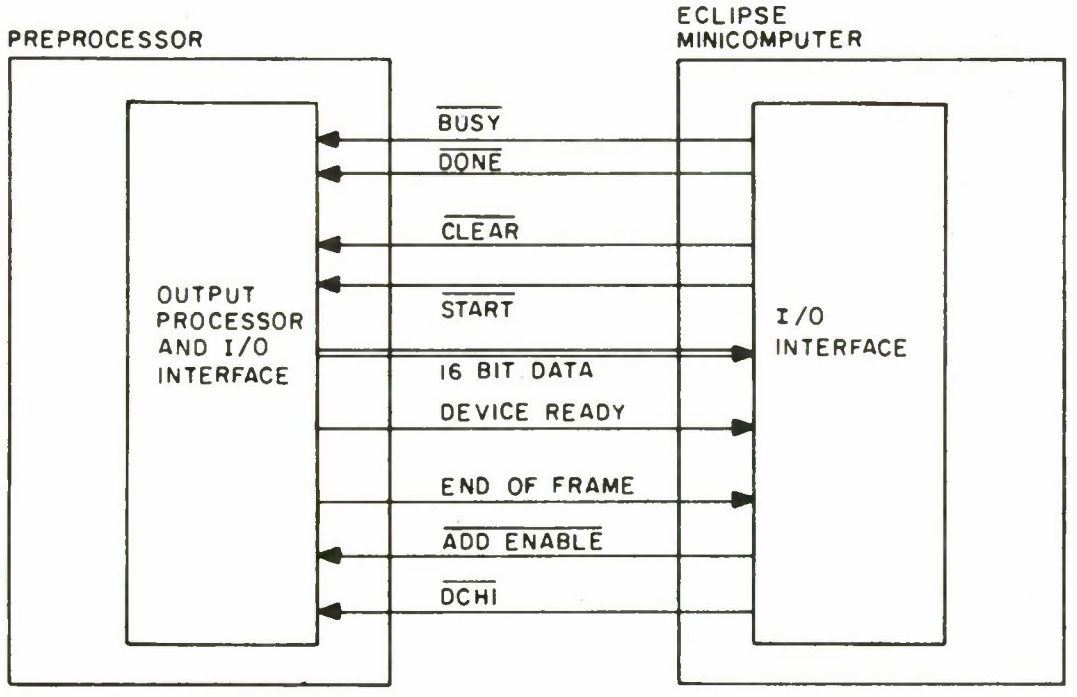

FIGURE 22. PREPROCESSOR/ECLIPSE CONTROL AND DATA PATHS

Control

A special purpose, crystal-controlled timing generator using programmable counters has been designed and developed that provides all of the preprocessor and TV sensor timing and control signals. The control unit contains a very stable frequency synthesizer from which all timing, gating and triggers are generated. All of the counters are programmed by front panel thumb switches.

The primary functions performed by the control unit are system timing and TV sensor synchronization. System timing consists of the generation of (1) the sampling clock and all other reference clocks, (2) the X, Y window gate, (3) the snapshot processing gate, (4) the frames/scan gate, and (5) start/stop control and system reset signals. The synchronization of the scanning of the TV sensor with the high speed sampling clock is achieved by deriving the external drive signals from the output of the frequency synthesizer. Using this clock input, the control unit maintains the proper sequence of events required for each processing task.

The generation of the sampling clock and other reference clocks, as shown in Figure 23, is performed in synchronous counters. These signals are derived from the output of the frequency synthesizer. The X, Y window gate is generated as shown in Figure 23 by comparing the X1, X2 control inputs with the horizontal counter output and the Y1, Y2 control inputs with the vertical counter output. The X, Y window gate provides control over the incoming data as described earlier in the discussion on data reduction and editing. The start/stop and system reset control logic is shown in Figure 24. Starting, stopping or resetting the preprocessor can be controlled manually from the front panel or automatically from the multi-minicomputer processor.

The following EIA standard, non-interlaced, TV signals are provided to externally drive the TV sensor: horizontal drive, vertical drive, composite blanking and composite sync. The variable rate TV sync generator, as shown in Figure 25, provides these external drive signals. The sampling clock is divided down in a programmable counter to generate the horizontal clock or scan rate. The vertical scan rate is then derived from the horizontal clock by a programmable lines/frame counter. All TV sensor control signals as shown in Figures 26 and 27 are selectable in 1 μsec steps using the front panel thumb switches. The combination of the variable rate sync generator and the variable frequency synthesizer provides the flexibility to change the sampling rate and TV scan rate to accomodate varying target and system parameters.

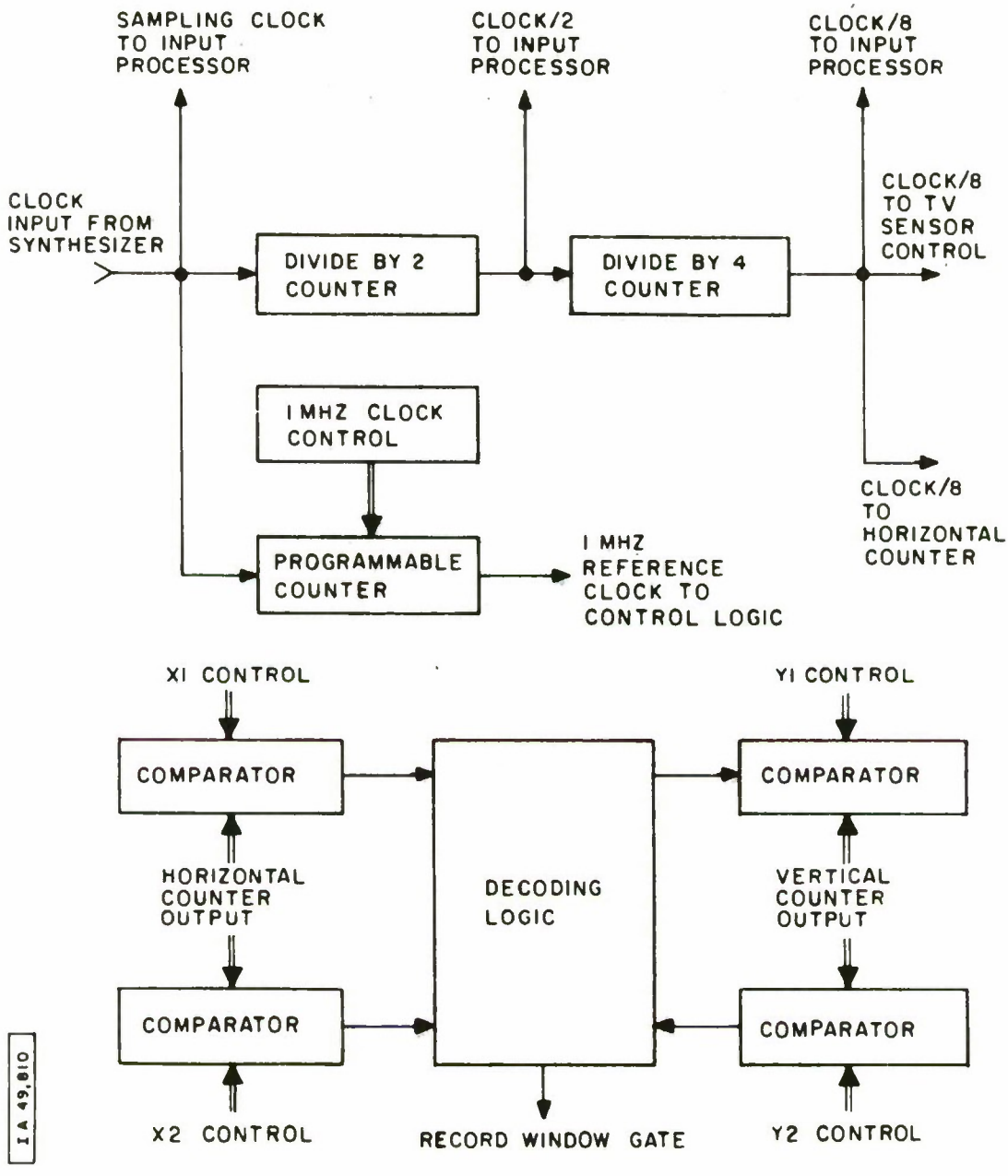

FIGURE 23. REFERENCE CLOCKS/WINDOW GATE LOGIC

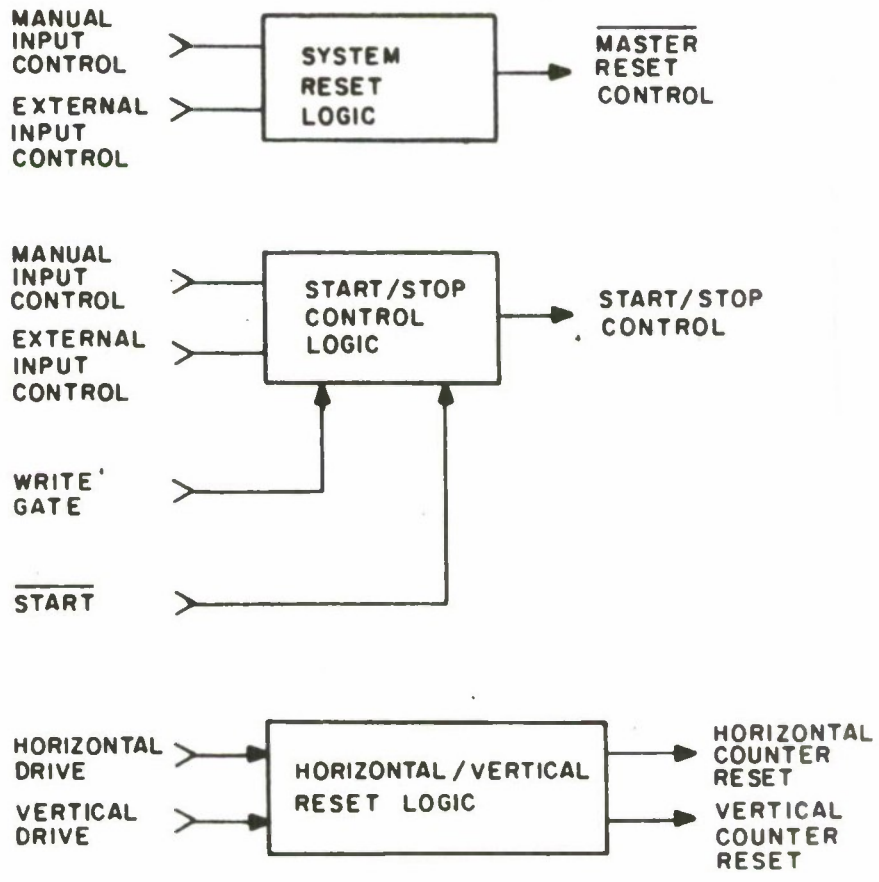

FIGURE 24. START/STOP CONTROL AND SYSTEM RESET LOGIC

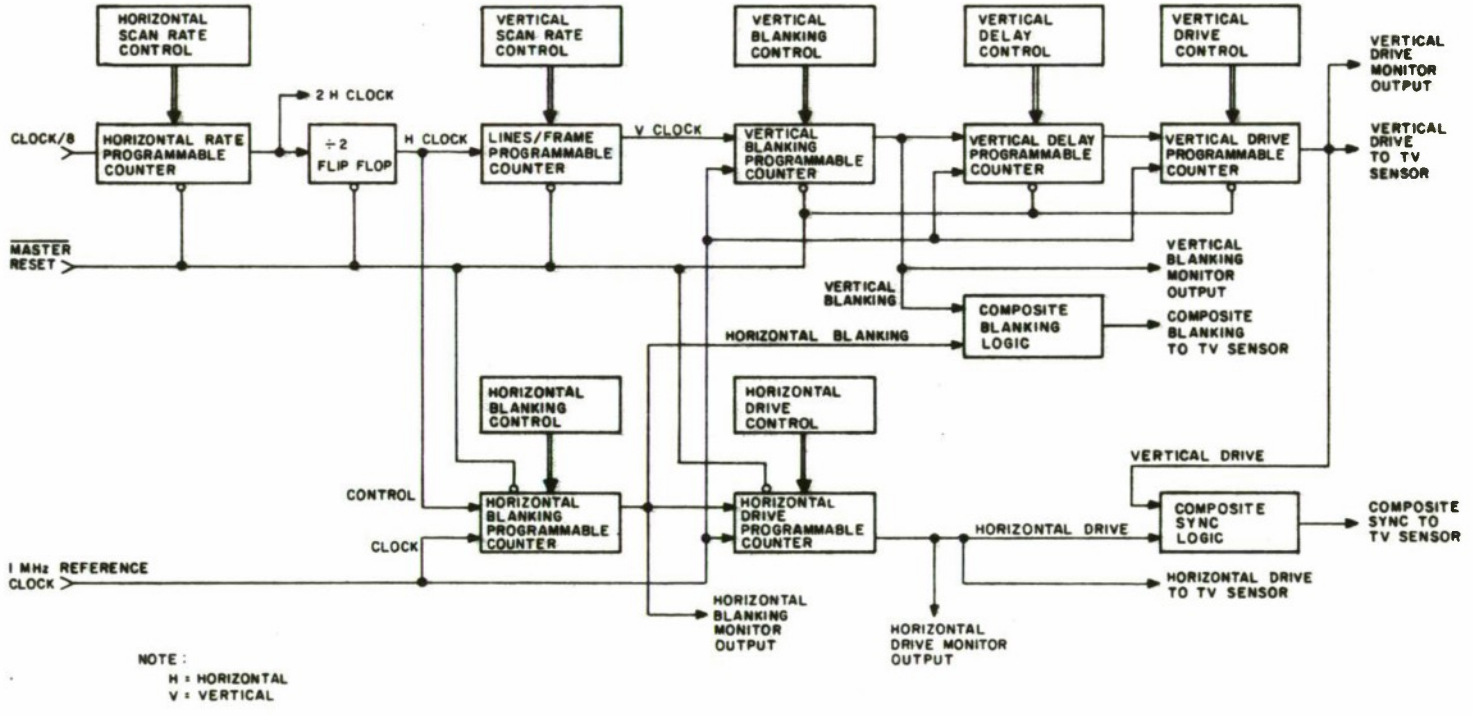

FIGURE 25. VARIABLE RATE TV SYNC GENERATOR

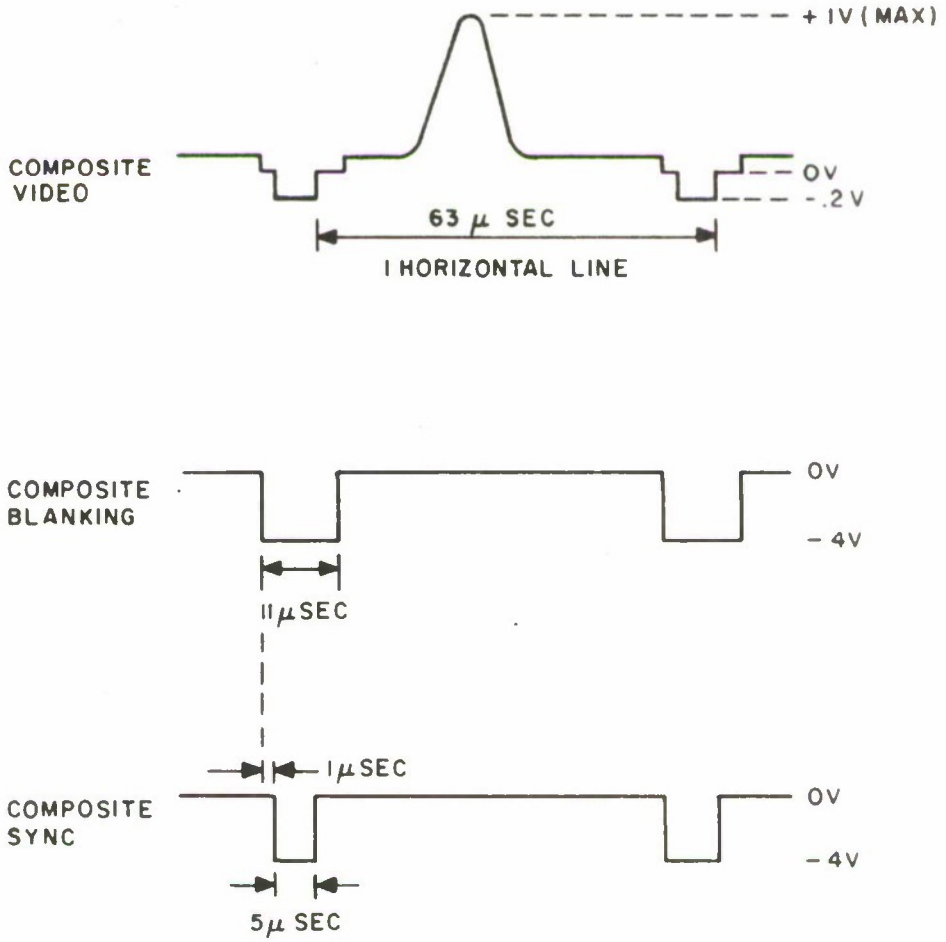

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FIGURE 26. TV COMPOSITE VIDEO AND CONTROL SIGNALS

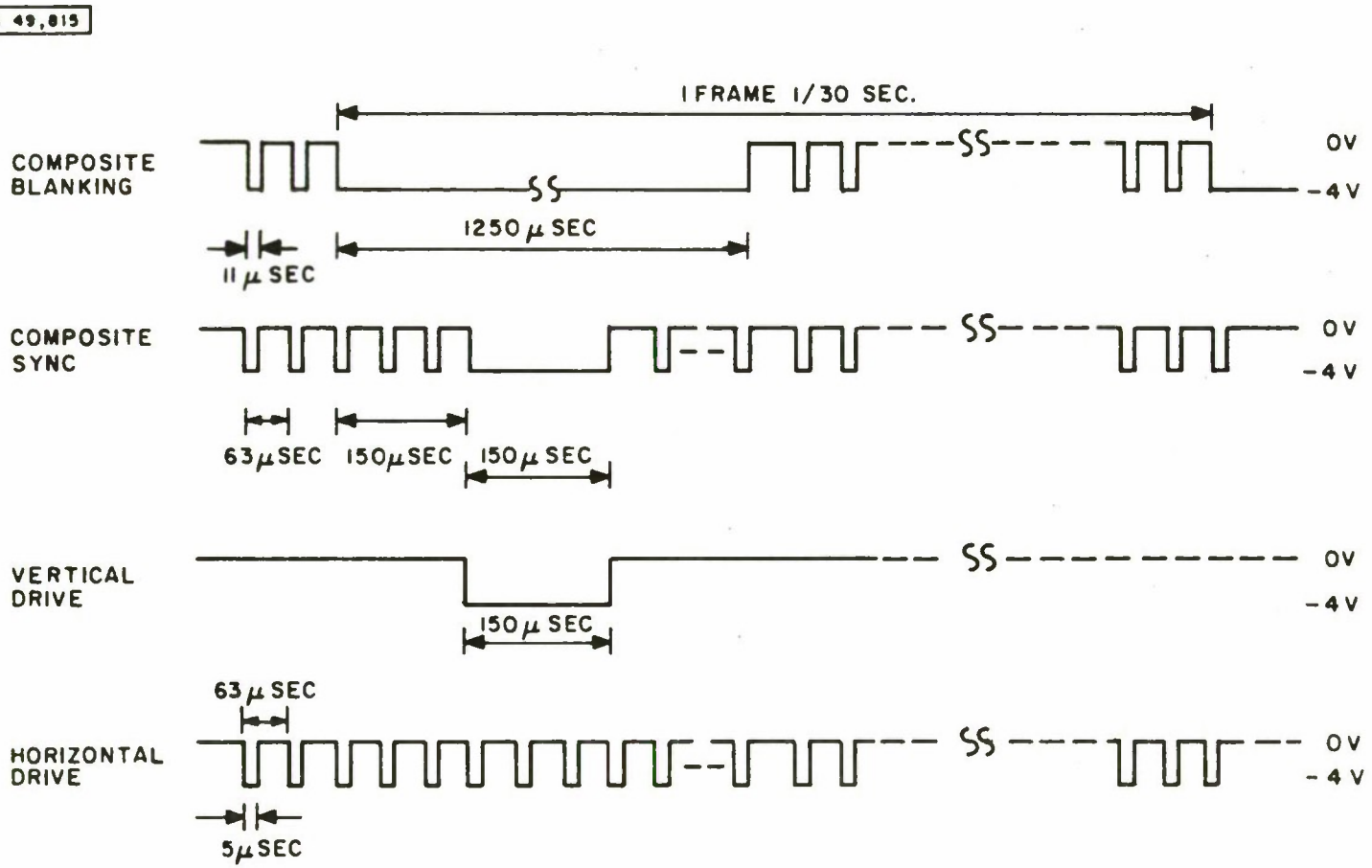

FIGURE 27. TV CONTROL SIGNALS

The control unit also generates the necessary signals to process data in a snapshot mode of operation. As shown in Figure 28, the integration time of the TV sensor is adjustable from 1 to 999 frames and the readout time is also adjustable from 1 to 9 frames. A write gate signal is generated by the TV sensor at the beginning of the readout time. This write gate signal is used by the snapshot processing logic in Figure 29 to generate the write gate' signal which consists of every nth write gate signal. The time between write gate' signals is the snapshot processing time interval of the GEODSS/MITRE system which is controlled by front panel thumb switches. This processing time interval was defined in Table II.

A preprocessor frame consists of a multiple number of TV sensor or camera frames. Therefore, the preprocessor frame rate is equal to the reciprocal of the snapshot processing time interval. During this processing time interval, the telescope is controlled by the ETS computer in a sidereal track mode. At the beginning of the next processing time interval, the telescope is moved to a new position, one field of view away.

During a scan interval the telescope is stepped through a particular area in one field of view increments and is then returned to the starting position and repeated. The scan interval, as shown in Figure 30, is determined by the mth write gate' signal (m processing time intervals) which is selected by the frames/scan thumb switches. The frames/scan counter output is displayed on the front panel and is used to control the storage of data in the PEP-500 which is part of the real time display.

Logic is also provided to detect the "computer not ready" error condition. If the "computer ready" signal (START) has not been received but the preprocessor is ready to begin a read cycle, a "computer not ready" error condition is displayed on the preprocessor front panel.

The following list of signals are displayed on the front panel of the preprocessor for monitoring system performance: buffer memory data outputs, preprocessor data outputs, threshold outputs, busy and done status indicators of the Eclipse minicomputer, buffer memory full and empty status, threshold reference level indications, and computer acknowledge and data flag signals.

Fabrication

Several of the major mechanical and electronic design considerations which were involved in the fabrication of the preprocessor are presented. The mechanical structure shown in Figure 31 was developed to provide for easy checkout, testing and modification of the preprocessor. The mechanical structure consists of a complex, split

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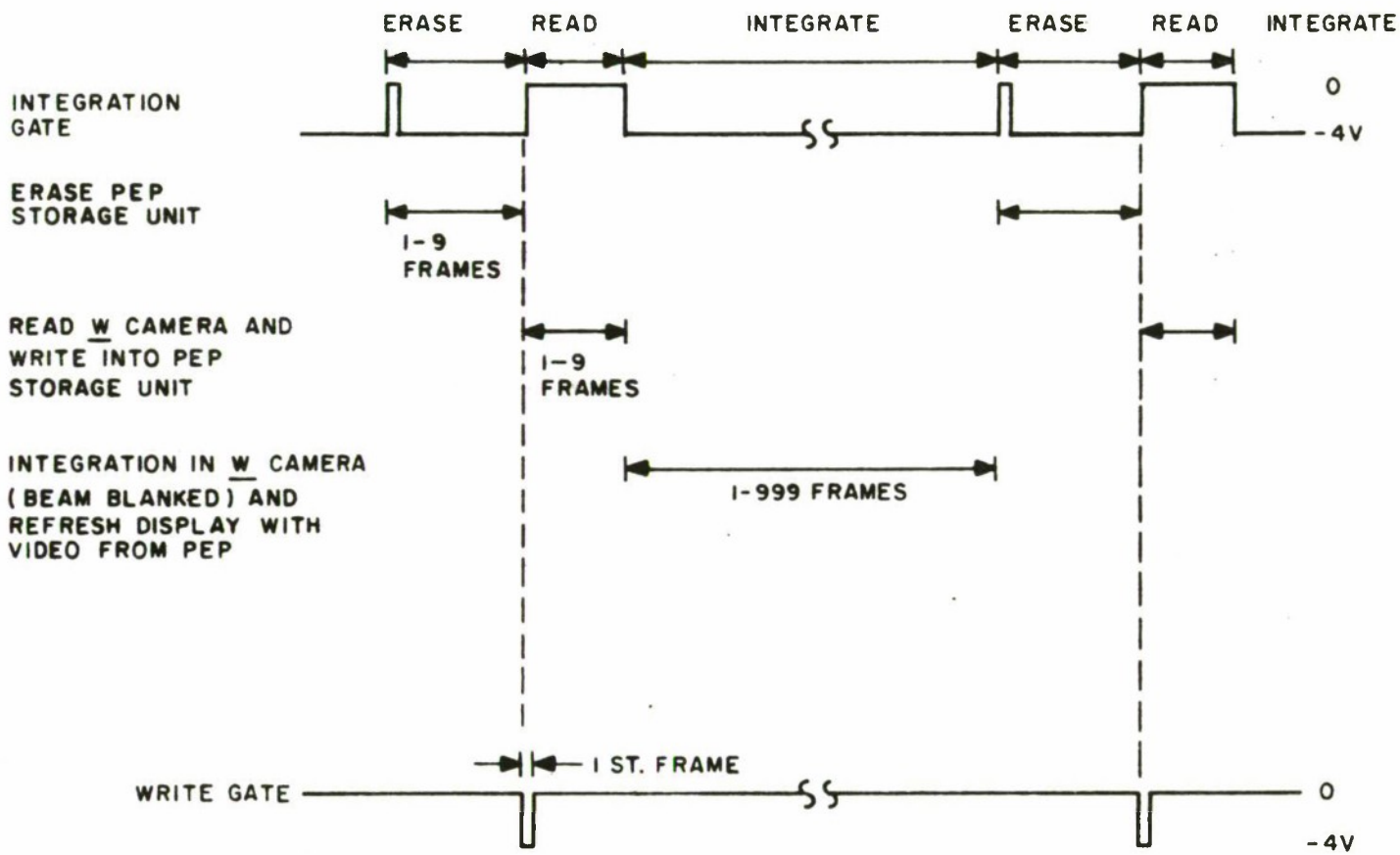

FIGURE 28. TV CAMERA TIMING - INTEGRATION MODE

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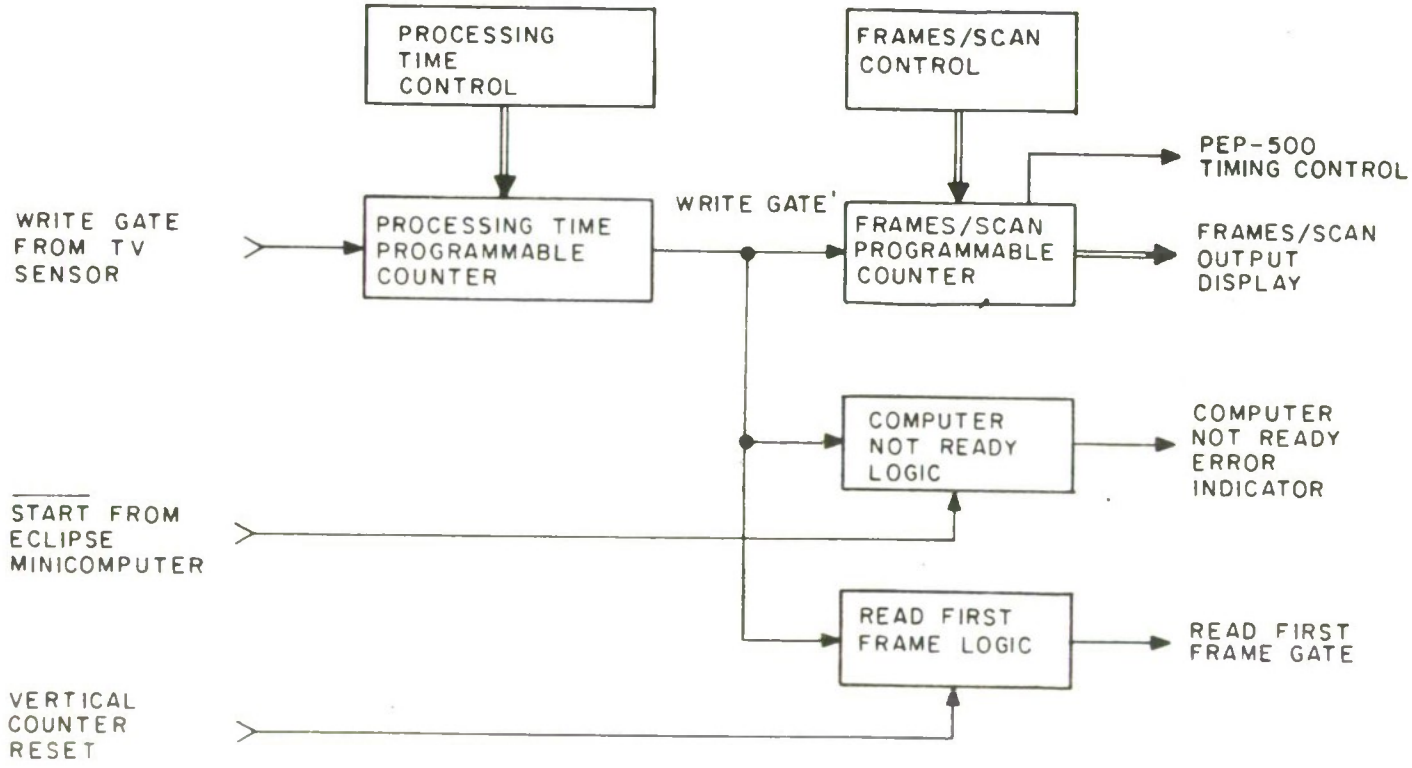

FIGURE 29. SNAPSHOT PROCESSING LOGIC

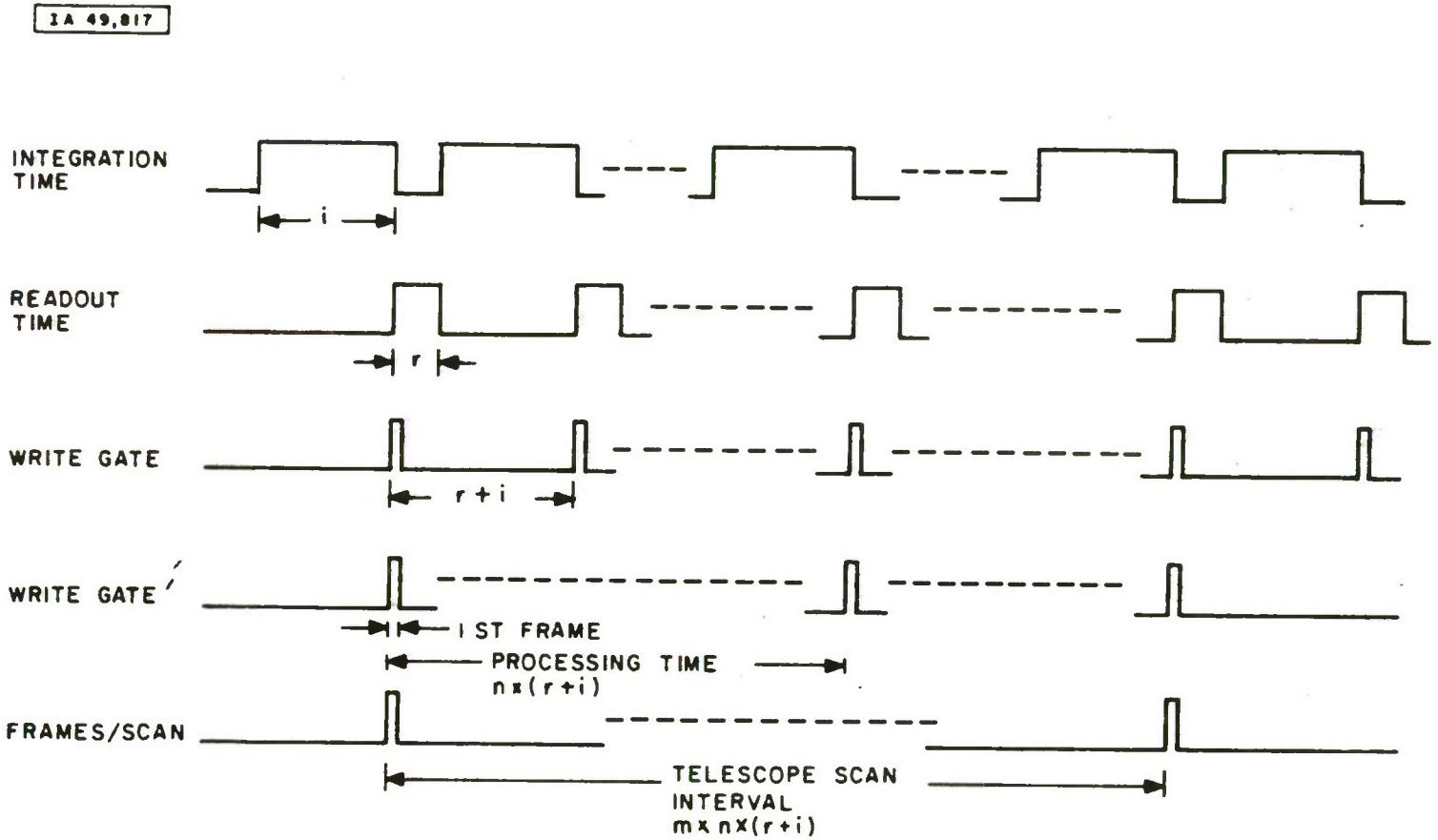

FIGURE 30. SCAN INTERVAL TIMING

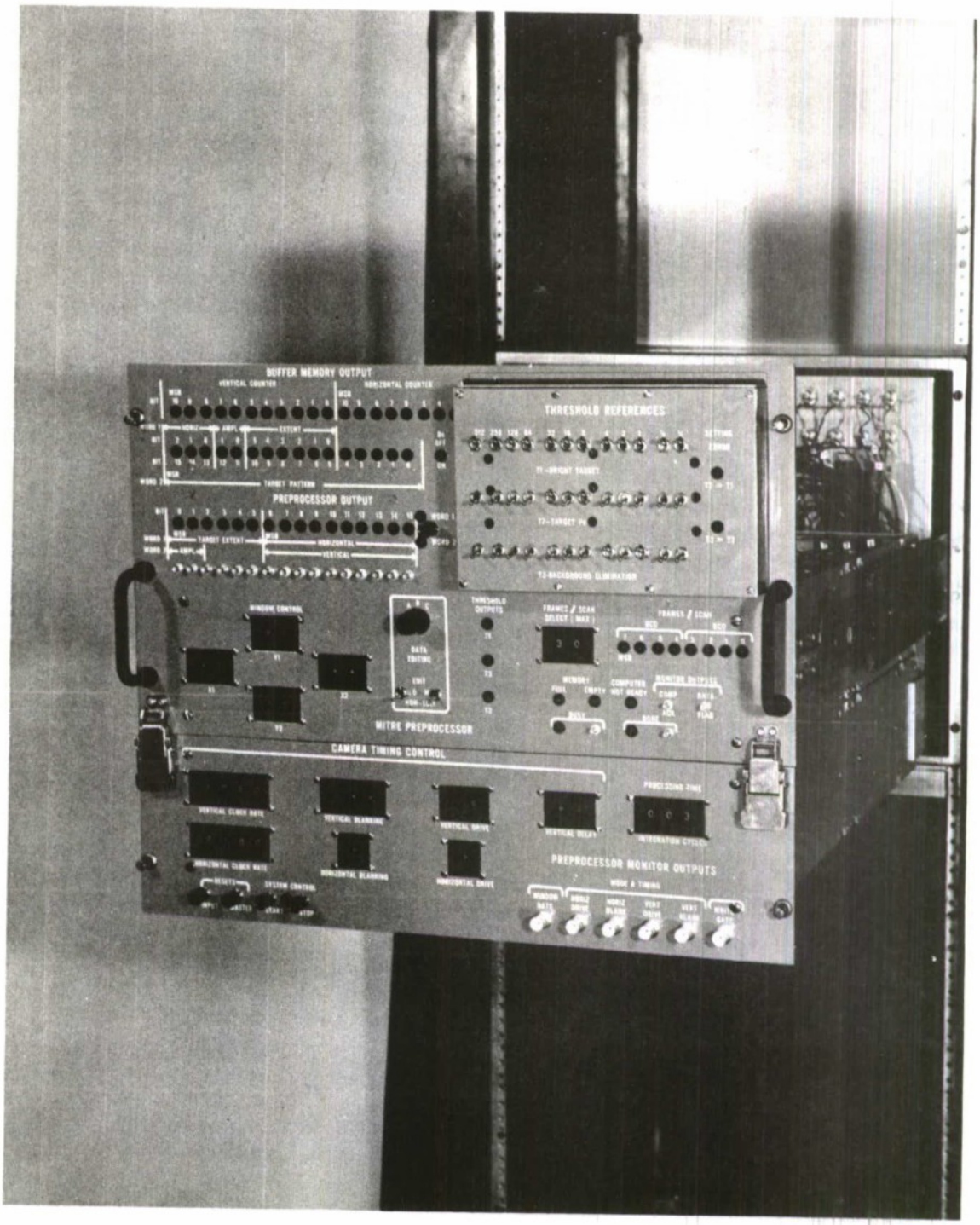

FIGURE 31. MITRE PREPROCESSOR

drawer assembly which is similar to a previous MITRE design. However, the hinge mechanism was redesigned to allow the drawer to fit into a standard 19 inch rack. This split drawer assembly is illustrated in Figures 32 and 33. Several of the boards are rotated from their normal position to show the wiring and ease with which testing and checkout can be accomplished. Shown in these figures are the five boards for mounting the integrated circuits. These figures also show the huge amount of wiring which was involved on each board and in the interconnection cables between boards. Twisted pair cables were used for all interconnections between boards to provide isolation between signals. Wirewrapping of the digital integrated circuits was selected because of the flexibility and ease with which modifications could be implemented. There was a mixture of manual and automatic procedures used in the wire-wrapping of these boards.

The fabrication of the preprocessor also included consideration of the board size and construction, back plane wiring, ground and power distribution, availability of check points and front panel controls. The threshold detectors and threshold reference circuitry were constructed using printed circuit techniques with these units enclosed in shielded brass boxes. These units are mounted to the front panels as shown in Figure 33. The use of rf construction techniques was required for noise and interference rejection due to the sensitivity of the threshold detectors.

The preprocessor has been implemented with state-of-the-art components such as Shottky TTL devices, bipolar RAMS and PROMS. The following general design rules were used in the implementation of the preprocessor.

a. Shottky TTL integrated circuits were used in most of the digital logic for high speed and compatibility with the minicomputer input.

b. All clock signals were buffered and twisted pair transmission lines used for distribution of these signals.

c. The outputs of decoders and combinational logic were strobed to avoid transients that typically occur on the outputs of these devices.

d. Typical monostable multivibrators which use RC elements were avoided because of the instabilities and limited noise immunity of these circuits. A digital monostable was used which consists of a flip flop and delay circuit.

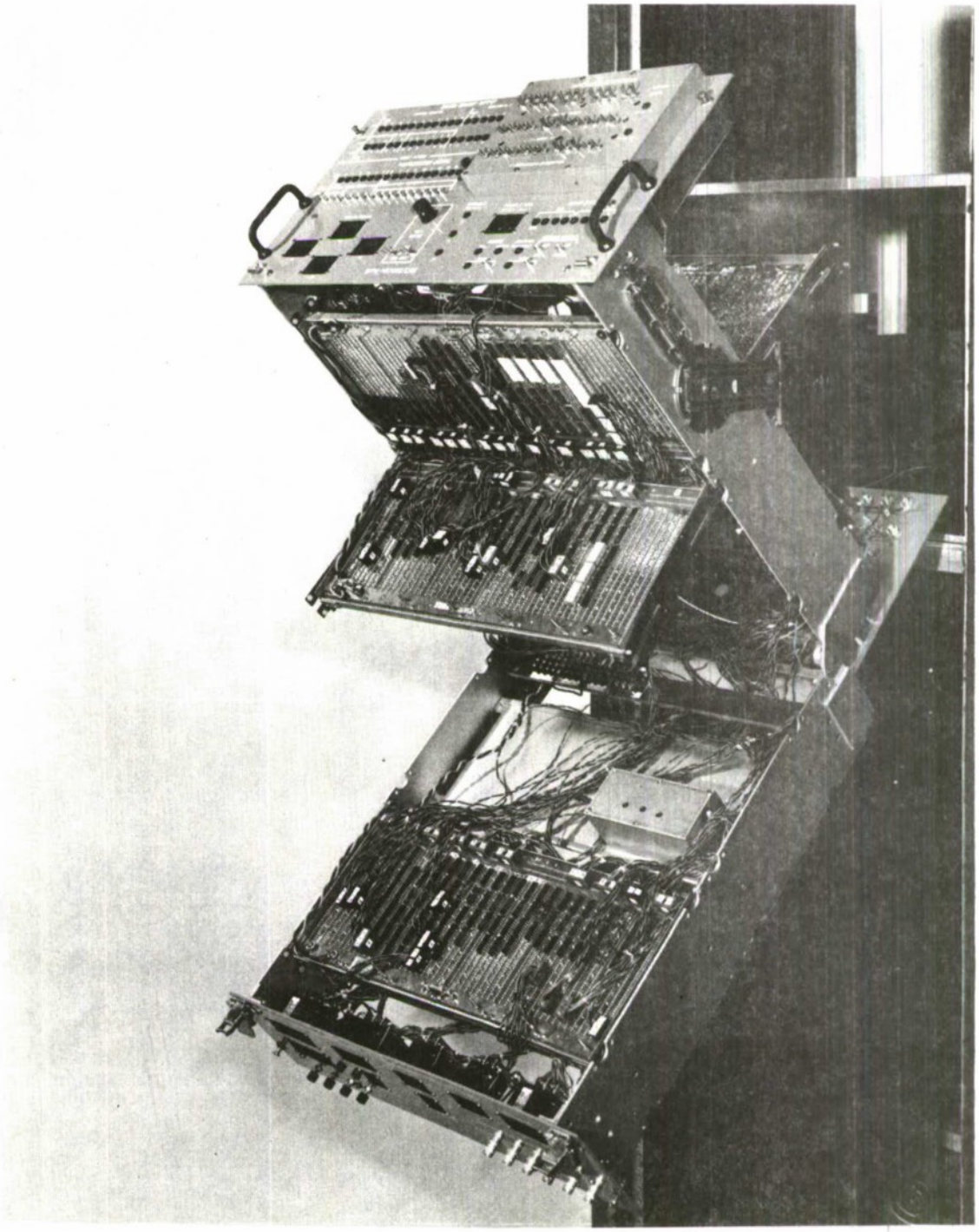

FIGURE 32. MITRE PREPROCESSOR ILLUSTRATING SPLIT DRAWER ASSEMBLY

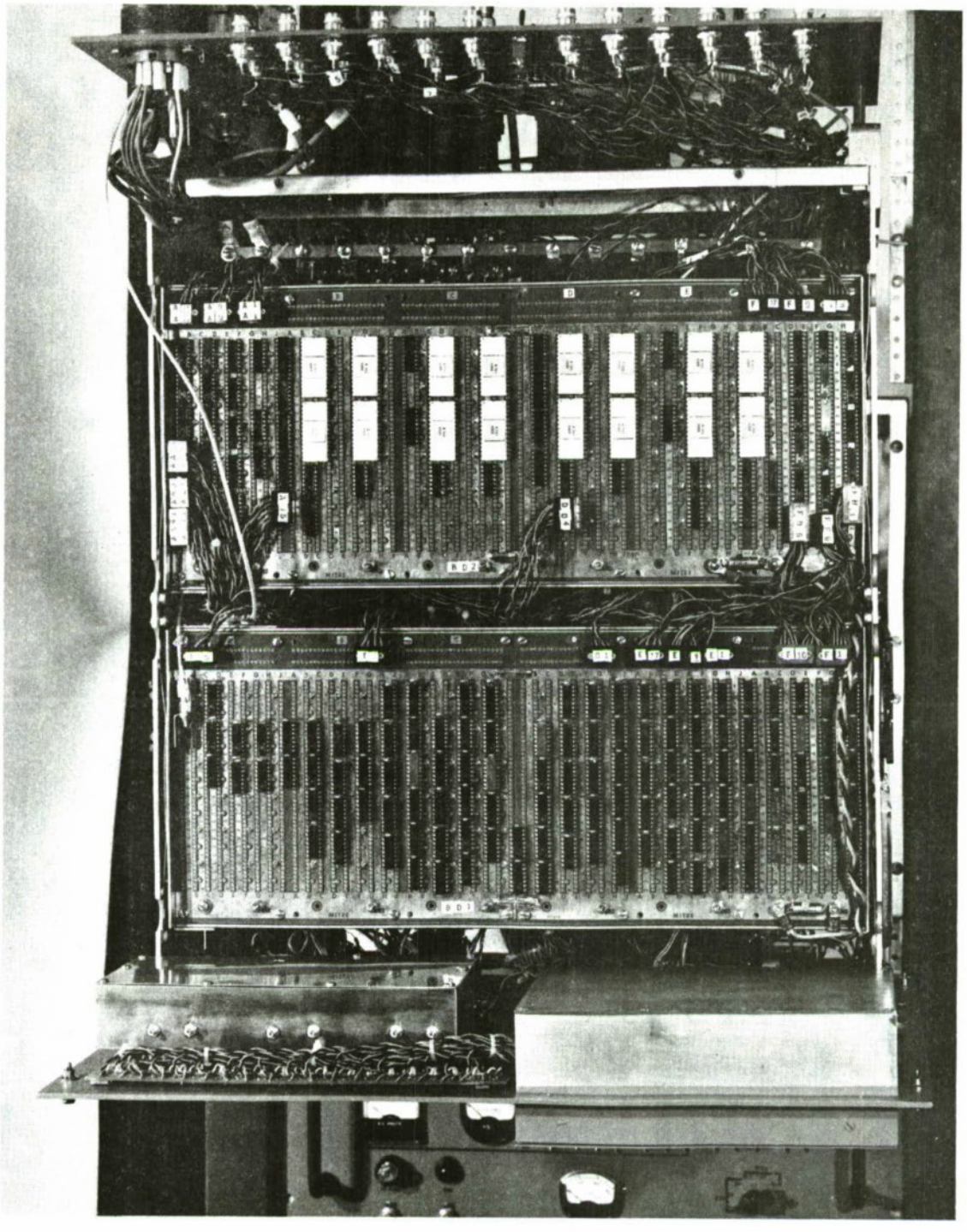

FIGURE 33. MITRE PREPROCESSOR, TOP VIEW

SECTION IV

MITRE/GEODSS ETS SYSTEM INTEGRATION

The integration of the MITRE preprocessor and multi-minicomputer processor with the GEODSS ETS system requires interfacing with the TV sensor and ETS computer. The MITRE/ETS system block diagram in Figure 34 illustrates these interfaces. All interface signals are isolated and dc restored to eliminate the effects of power line and spurious noise interference. The external synchronization of the TV sensor is provided by the preprocessor control unit as described in Section III.

The ETS computer/MITRE PIM interface is shown in Figure 35. A timing diagram is included in Figure 36. The primary function of this interface is to indicate whether the telescope is either in the sidereal track mode or slewing mode. During the slewing mode, the multi-minicomputer processor inhibits the transfer of data from the preprocessor.

As shown in Figure 36, the sidereal level signal from the ETS computer is used to generate the sidereal and slewing pulses. For this interface, the PIM keeps checking IDAT0 and IDAT1 (the two most significant data bits) to determine the telescope condition. When the telescope is in the sidereal track mode, IDAT0 = 1 and IDAT1 = 0. When the telescope is being moved to a new position, the telescope is in the slewing mode and IDAT0 = 0 and IDAT1 = 1. Each time the telescope is moved, a sidereal or slewing pulse is generated which clocks the data, IDAT0 and IDAT1, into the input register of the PIM. Following the inputting of this data, the DONE status flip flop is set to 1. The next $\overline{\text{START}}$ signal clears DONE and sets BUSY. The DIA signal is then generated by the PIM processor to strobe the data (IDAT0 and IDAT1) onto the I/O bus for program use in checking the status of the telescope. A device code of 25_8 (Octal) has been selected for this interface.

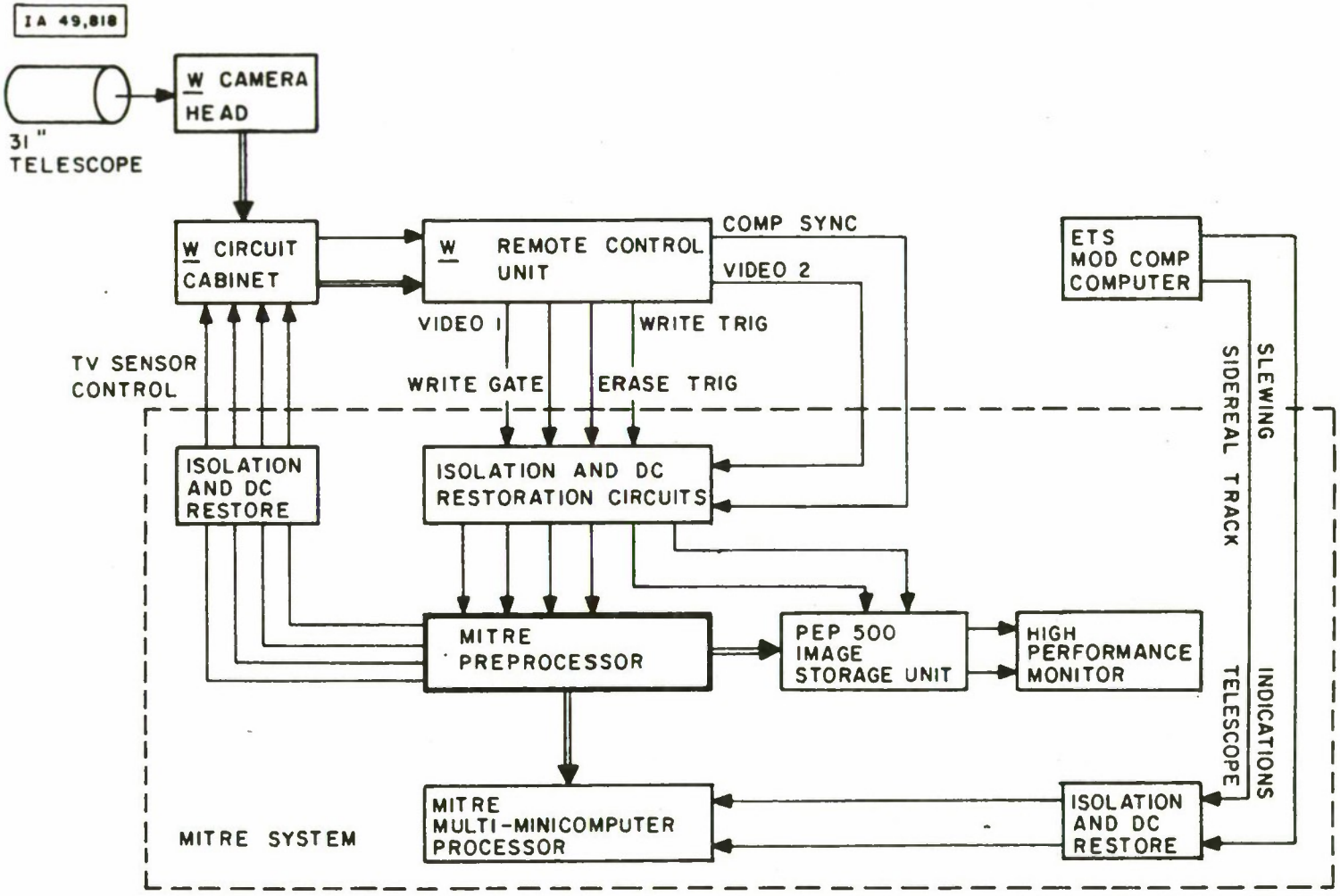

FIGURE 34. MITRE/GEODSS ETS SYSTEM INTERFACE

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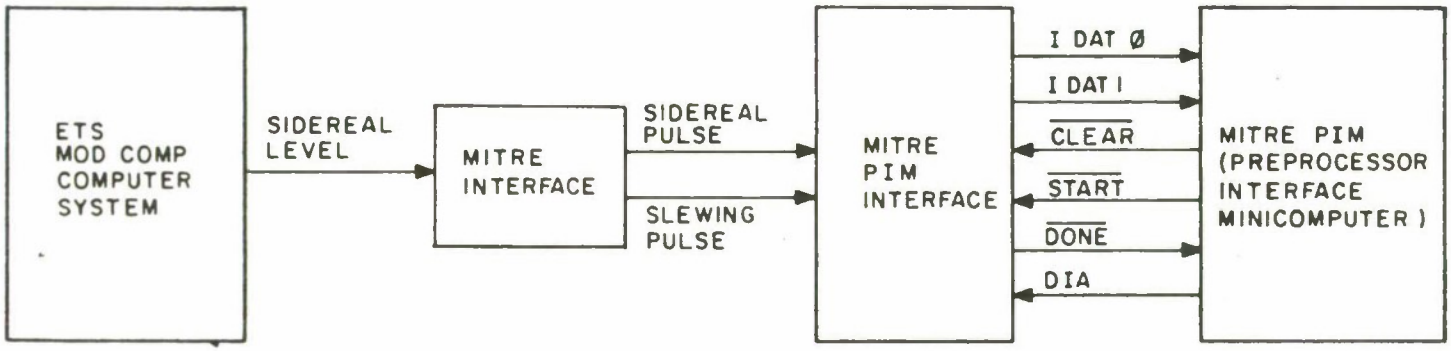

FIGURE 35. ETS COMPUTER/MITRE PIM INTERFACE

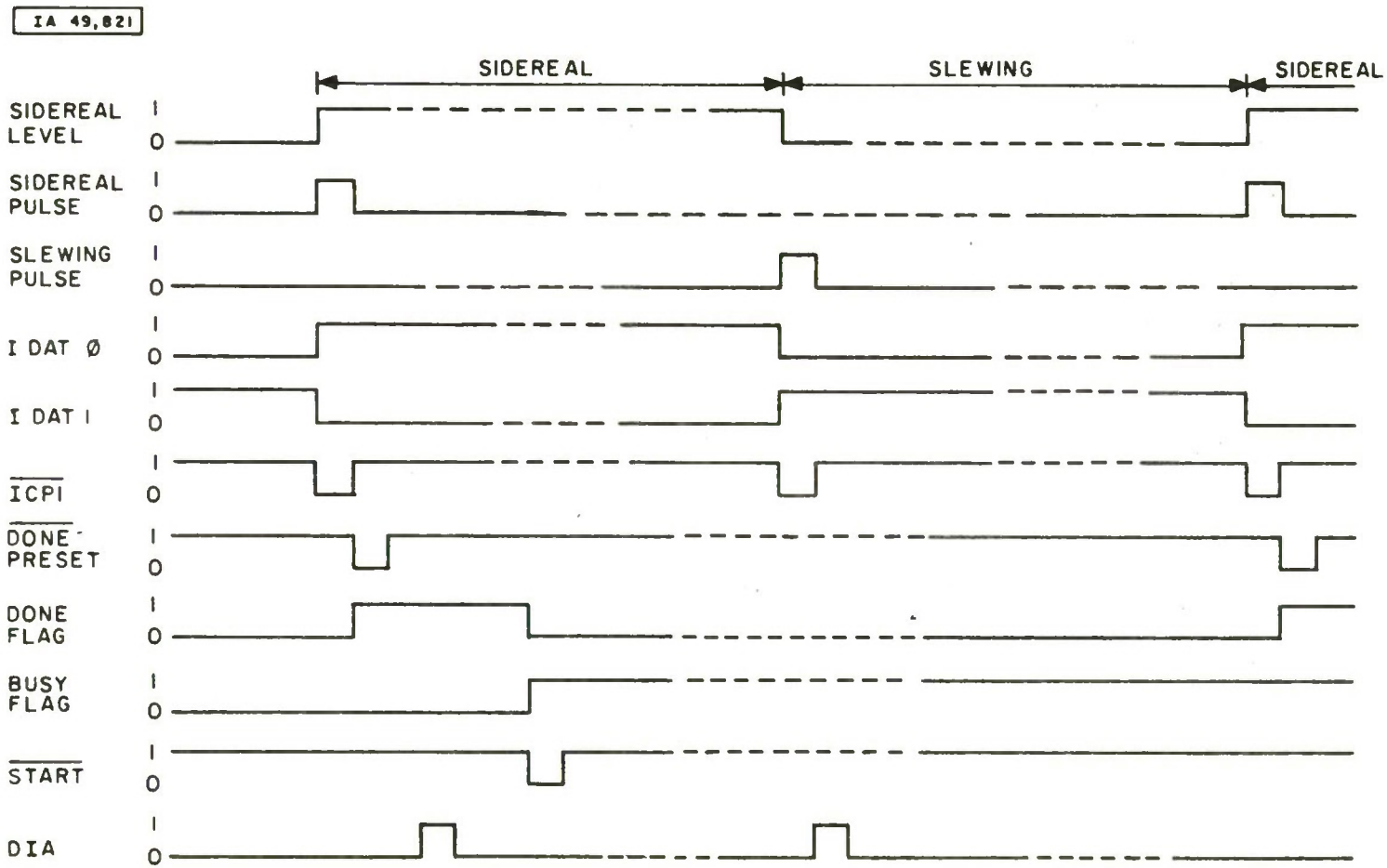

FIGURE 36. ETS COMPUTER/MITRE PIM INTERFACE TIMING

SECTION V

PERIPHERAL UNITS

The functions of the peripheral equipment which is part of the MITRE/GEODSS system are described in this section. As shown in Figure 5, the peripheral units consist of:

a. Image storage and scan coverter

b. Video display

c. Real time display

d. Frequency synthesizer

e. Pulse generator

The image storage and scan converter and video display provide the capability to monitor the video input signal in a "snapshot" mode of operation. Since the MITRE/GEODSS system will be operating in an integrate/read/process and display mode, there will be between 1/2 to 64 seconds of elapsed time between readouts. To provide a continuous display of these integrated signals, the image storage and scan converter is operated in a slow scan mode. In the slow scan mode, the image data is written or stored at a slow raster rate but is read out to the display at the standard TV rates. The image data is acquired from the TV sensor in a frame grabbing or snapshot mode, stored on the image tube, and then continually read out to refresh the display. The image storage and scan converter selected for this application is model 500 from Princeton Electronic Products (PEP) while the high performance video display is model HD-1501 from Sierra Scientific Corporation.

The real time display of the preprocessor output data is provided for monitoring system performance and for selecting the optimum threshold levels and data editing algorithms. The display of edited or non-edited data is selectable by a front panel switch. The real time display is implemented with the PEP-500 image storage unit and Sierra Scientific monitor to provide a non-flickering display during TV camera integration and telescope slewing.

The frequency synthesizer, HP 5100A/5110A, provides the very stable clock or standard for the preprocessor from which all timing signals are derived. The synthesizer provides any output frequency from DC to 50 MHz, selectable in steps as small as 0.01 Hz. The output frequency is derived from a precision single frequency source

through a direct synthesis technique which translates the long-term stability and spectral purity of the source to the selected output. The short term stability of the output frequency is on the order of 3×10^{-11} for a one second averaging time. If a more stable reference is required, an atomic standard or other standard can be used to externally drive the synthesizer.

The pulse generator, model EH137, provides the TTL clock input to the preprocessor which is synchronized to the sine wave output of the frequency synthesizer.

SECTION VI

CONCLUSIONS

A high speed preprocessor has been successfully designed and implemented. Although the preprocessor was specifically developed for the GEODSS system, the signal processing techniques developed here are useful in a wide variety of other applications. The preprocessor is capable of high speed processing, storage and conversion of wideband signals to speeds and bandwidths which are compatible with present minicomputers and microprocessors. The preprocessor uses programmable read only memories (PROMS) which have become an important part of many digital systems because of a combination of their low cost, high speed, design flexibility and data non-volatility. The parameters for scattered targets in this application are permanently stored in PROMS. Reprogramming is accomplished very simply by inserting different PROMS. Other complex processing functions can therefore be incorporated with little effort and without rewiring the logic.

Laboratory testing of the preprocessor with the TV sensor and multi-minicomputer processor was successfully completed at MITRE prior to shipment of the system to the GEODSS ETS site for field testing and evaluation. The laboratory tests were conducted using the MITRE star simulator with both the Westinghouse model TEM432 and Sylvania model 200 low light level TV cameras. The Sylvania camera was only used temporarily until the Westinghouse camera was available. The preprocessor control unit has successfully synchronized the scanning of the Westinghouse TV sensor in all of the available formats as listed in Table II.

Data reduction and editing are important features of the preprocessor, especially the X-Y window gate which is used to eliminate transients, from the TV sensor from being processed. Another important feature is the flexible TV sync generator which provides the capability to change the sampling rate and TV scan rate to accommodate varying target and system parameters.

REFERENCES

1. Data General Corporation, How to Use the Nova Computers, Southboro, Mass., 1974.

2. J.E. Barry, Moving Target Indication Using the Snapshot Algorithm, ESD-TR-76-157, Electronic Systems Division, AFSC, Hanscom AF Base, Mass., September 1976 (AD A031152).

3. D.D. Coffin and H.E.T. Connell, MTI Processor Software, ESD-TR-75-352, Electronic Systems Division, AFSC, Hanscom AF Base, Mass., February 1976 (AD A021778).

4. D.D. Coffin and H.E.T. Connell, The Multi-Minicomputer Processor, ESD-TR-75-351, Electronic Systems Division, AFSC, Hanscom AF Base, Mass., February 1976 (AD A021777).

5. H.E.T. Connell, A Multi-Minicomputer Network for Optical Moving Target Indication, M76-201, The MITRE Corporation, Bedford, Mass., March 1976.

APPENDIX A

MEASUREMENT OF TARGET EXTENT FOR NON-SCATTERED TARGETS

The measurement of target extent for non-scattered targets is performed as follows:

a. The extent counter is incremented if the C register is full unless the target is preceded by a scattered target.

b. The extent counter is preset to C_T if the C register is not full or if the C register is full and preceded by a scattered target.

c. A target located at the bottom of the C register (C_B) is considered to be a scattered target if it was preceded by a scattered target or one considered scattered if $C_B \neq 8$.

d. If a scattered target is preceded by a non-scattered target, C_B is not passed onto the B register.

APPENDIX B

RULES FOR RECORDING OR STORING DATA

The rules for recording or storing data for both scattered and non-scattered targets are as follows:

a. Record whenever a scattered target is present ($B_S = 1$).

b. Record whenever $B_T \neq 0$ or 8, $C_B \neq 0$ or 8 and the C register is not full. B_T is similar to C_T except it is determined by data in the B register.

c. Record whenever the B register is full and $C_B = 0$.

d. Record whenever the extent counter is full ($\Delta X = 48$).

e. For extended targets with extents >48, record the data each time the extent counter is full and until the target amplitude falls below threshold level T3.

APPENDIX C

ECLIPSE I/O AND PREPROCESSOR I/O INTERFACES

Eclipse I/O Interface

When interfacing the Data General Eclipse minicomputer with an external device, the user is usually required to supply I/O data and control logic. The general purpose interface board supplied by Data General includes the basic interface control logic discussed in Appendix D. This interface board also includes space which is reserved for customer or user logic which may be required to connect the external device to the I/O bus.

The interface logic and I/O control signals required to interface the preprocessor to the Eclipse minicomputer are included in Figures C-1 and C-2. The ADD ENABLE signal which is defined in Appendix D is used to generate WC CLOCK 1, CAE2, ICP1 and DCHA. The ADD ENABLE signal therefore provides the following control functions (1) incrementing the word counter, (2) strobing the memory address onto the I/O bus, (3) clocking the input data into the input register and (4) providing a data transfer acknowledgement to the preprocessor.

Initialization of the memory address counter and word counter is performed by the following signals:

a. $\overline{\text{DATA IN B}}$ signal is generated by the Eclipse processor to place the contents of the address counter on the I/O bus for program use.

b. $\overline{\text{DATA OUT B}}$ signal is generated by the Eclipse processor to initialize the address counter with the starting address.

c. $\overline{\text{DATA OUT A}}$ signal is generated by the Eclipse processor to initialize the word counter with the number words to be transferred.

The $\overline{\text{DCHI}}$ signal provides the following control functions, (1) incrementing the address counter, (2) strobing the data onto the I/O bus and (3) providing a data channel input (DCHI) control signal to the preprocessor. To allow computer control of this interface, the BUSY status flag is used to control the setting of the DCH SYNC flip flop which initiates the DMA data in cycle.

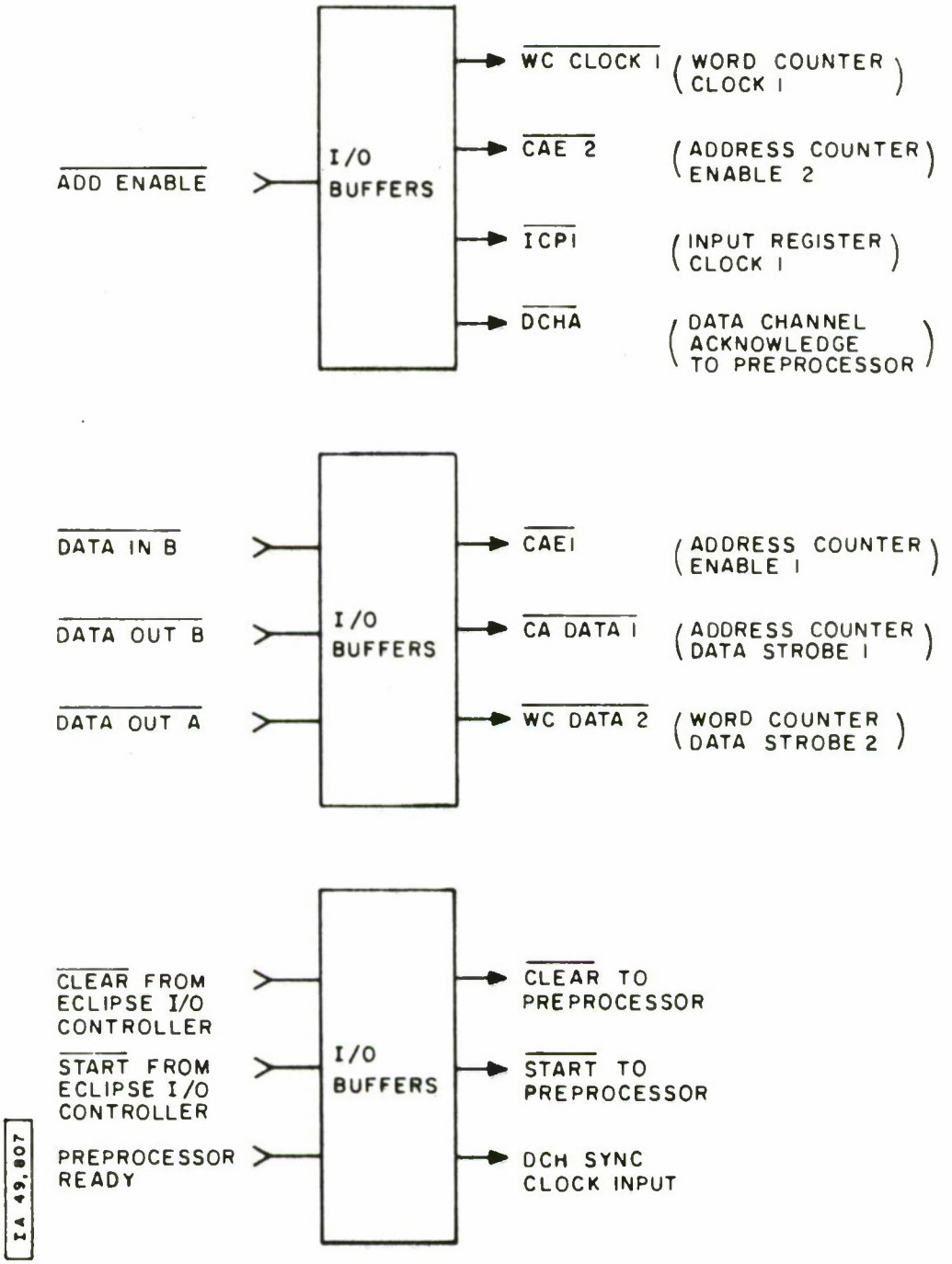

FIGURE C-1. ECLIPSE I/O INTERFACE

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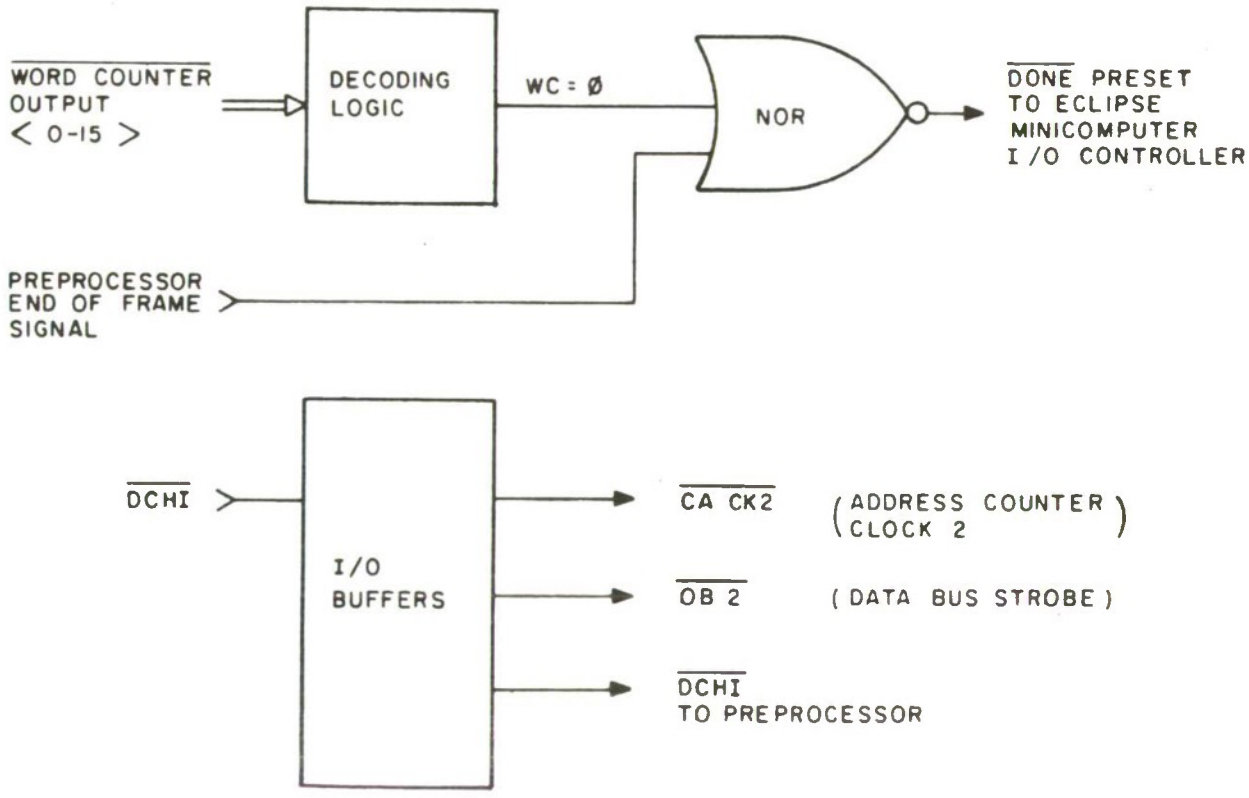

FIGURE C-2. ECLIPSE I/O INTERFACE CONTINUED

Preprocessor I/O Interface

A functional block diagram of the preprocessor interface is shown in Figure C-3. The actual data channel transfer sequence is a bidirectional communication between the preprocessor and the Eclipse minicomputer. A timing diagram for the complete interface is included in Figure C-4. The MEMORY READ CLOCK sets the DATA READY flip flop which generates a preprocessor ready signal. The DATA READY flag prevents reading the memory again until after the present data is transferred to the minicomputer. The preprocessor ready signal sets the DCH SYNC flip flop in the Eclipse I/O controller which initiates a DMA data input operation. After transferring this data to the input register of the Eclipse I/O controller, DATA READY is set to 1 by DCHI which is a computer acknowledgement that it has received the data and is ready to receive the next word. This data input operation is repeated until the word count is satisfied or an end of frame signal is received from the preprocessor.

After transferring the two 16 bit data words for each detection to the Eclipse minicomputer, the output of the counter which keeps track of the number of targets is compared with the number of expected targets. When the number of targets transferred is equal to the expected number of targets, a target done signal is generated.

In order to transfer data at maximum speed, the next DMA request cycle is initiated before the completion of the previous DMA cycle. Therefore, if data is not available from the buffer memory for transfer, it is necessary to stop the next DMA request cycle. This is accomplished with the $\overline{E}$ control signal which prevents control signal C' from setting DCH SYNC.

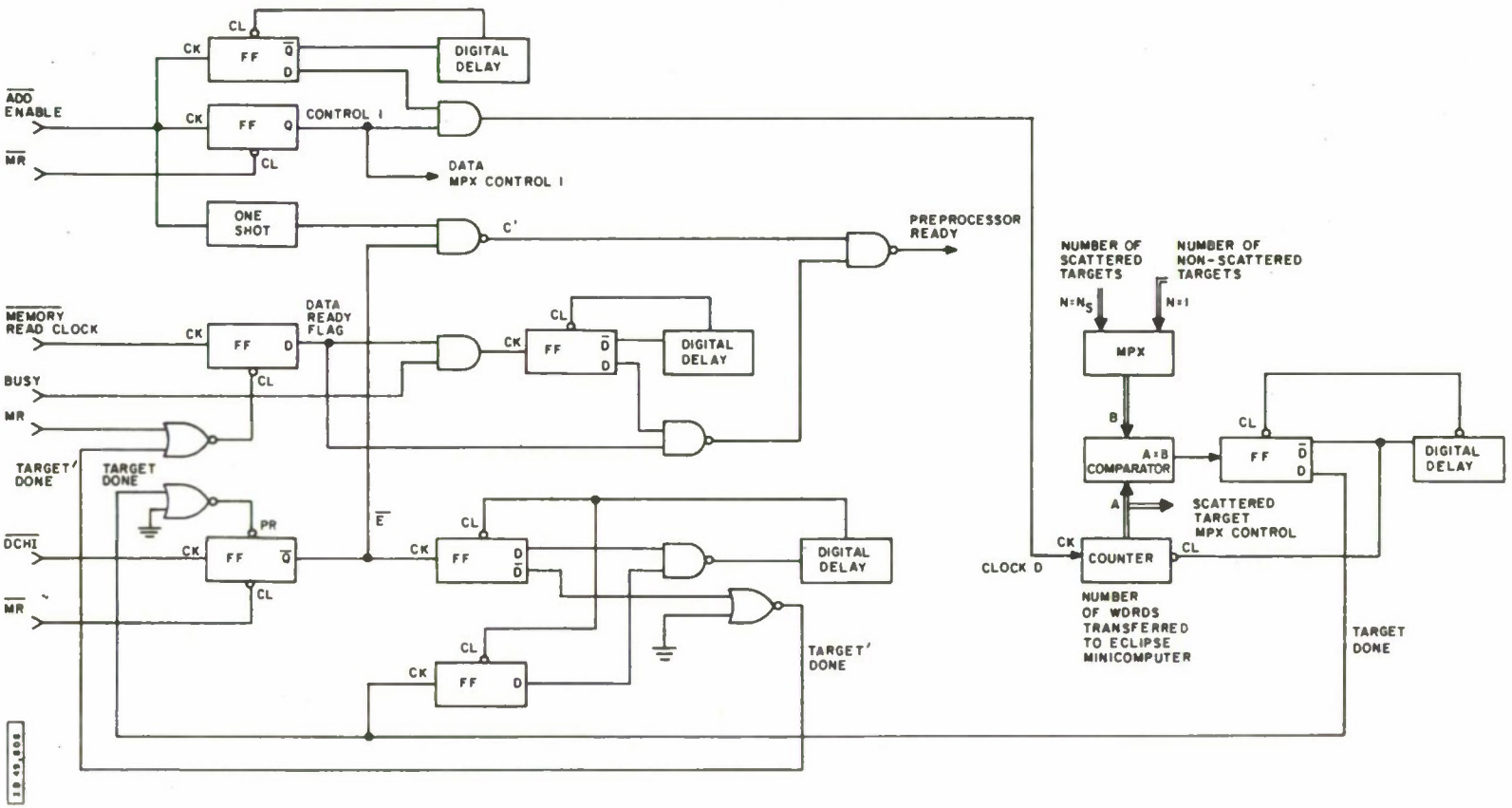

FIGURE C-3 PREPROCESSOR I/O INTERFACE

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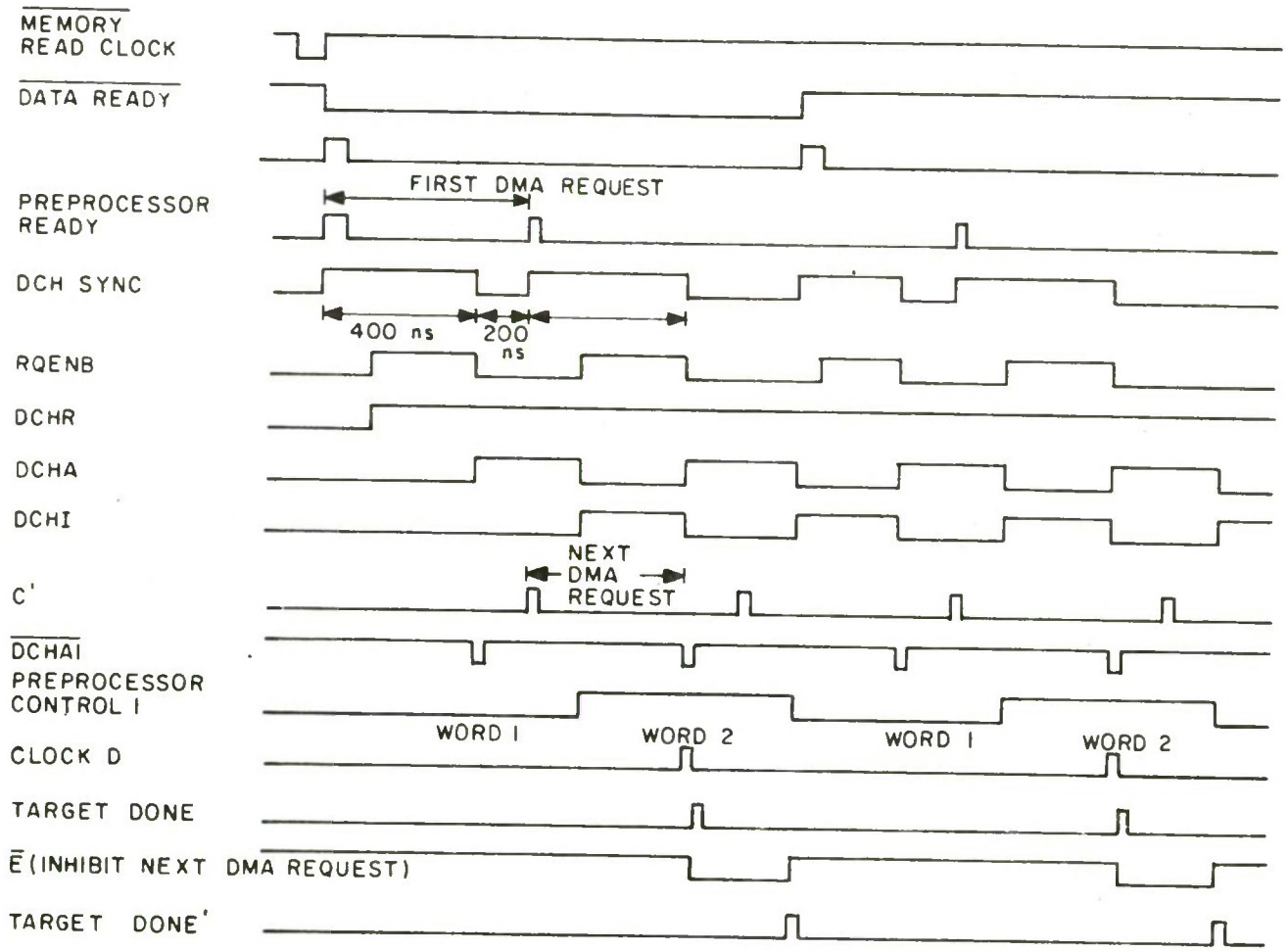

FIGURE C-4. PREPROCESSOR/ECLIPSE I/O INTERFACE TIMING

APPENDIX D

INTRODUCTION TO DATA GENERAL HIGH SPEED INTERFACE OR DATA CHANNEL

This appendix provides an introduction to the Data General high speed interface or data channel. The logic that performs the data transfers is referred to by Data General as a data channel rather than an interface.

The data channel consists of several data registers, control registers and status flags with which data communication is established. With these registers and flags, data is transferred from the preprocessor to the minicomputer while also monitoring the status of the interface. A status flag is a single stage register or flip flop which contains a single bit of information while a register consists of a number of bits of information.

Since it is required to transfer large amounts of data at extremely high rates from the preprocessor, the data channel is used in a direct memory access (DMA) mode. In direct memory access control, data from the preprocessor is transferred directly to the Eclipse minicomputer memory. The Eclipse processor initiates the DMA transfer by supplying a starting memory address and word count. When a data transfer is to be made, a DMA cycle is requested by the preprocessor and, when granted, data is transferred directly to memory. This is the fastest and most efficient transfer method but it is the most expensive. It is also necessary to include circuitry for supplying the memory address, keeping track of how many transfers have been made, and when the operation is complete.

The data channel contains a memory address counter to control the location in memory to which data is transferred. The memory address counter is loaded by the program with the address of the first word to be transferred. During each transfer, the data channel I/O controller increments the memory address counter by 1. A word counter is also included to keep track of the number of transfers performed. The word counter is loaded by the program with the two's complement of the number of words to be transferred. Each time a word is transferred, the controller automatically increments the counter by 1. When the word count equals zero or when an end of frame signal is received from the preprocessor, the controller terminates the DMA cycle.

For handling data channel requests, the I/O interface or data channel contains a data channel control network and a BUSY/DONE network.

The BUSY and DONE flags are the two basic flags in the data channel for indicating the status of the interface. To start a DMA or data channel request cycle, the program sets the BUSY flag. When the DMA operation is completed, the controller sets the DONE flag and clears the BUSY flag. These status signals are shown in Figure D-1. The START pulse sets the BUSY flag and clears the DONE flag initiating the I/O operation. At the completion of the operation, a DONE preset signal is generated in the I/O controller which sets DONE and clears BUSY. Figure D-1 illustrates a simplified version of the BUSY/DONE network. BUSY and DONE signals are displayed on front panel indicators of the preprocessor for monitoring system operation. Outputs for an oscilloscope display of these signals are also provided.

The data channel control network is shown in Figure D-2. A timing diagram for the high speed data channel cycle is shown in Figure D-3. When the preprocessor requires access, it sets the DCH SYNC flip flop which allows the leading edge of the next RQENB clock to place the data channel request signal DCHR on the bus. This is accomplished by setting the DCH REQ flip flop. Associated with these flip flops is a priority circuit which allows the next DCHA signal to set the DCH SEL flip flop. The output from the DCH SEL flip flop generates the mode signals for the desired DATA IN transfers. At the end of DCHA, the Eclipse processor strobes the memory address into its memory address counter. The memory address counter supplies the address so that access is made to consecutive locations in memory. The Eclipse processor then supplies DCHI which holds the contents of the input register on the bus. At the end of DCHI, the processor strobes the data into the memory buffer and begins the next DMA cycle by generating RQENB which turns off DCHR. During this data channel cycle, the Eclipse processor stores the data in the addressed memory location. DCHA also clears DCH SYNC so it is available for a second data channel request. It should be noted that clearing BUSY also clears DCH SYNC so that the preprocessor can not gain access after the program has turned it off.

As shown in Figure D-3, the present I/O controller clears DCH SYNC with ADD ENABLE which is equal to DCHA·DCHP·DCHR·DCH SEL. This means that the DCH SYNC flip flop cannot be set again until the end of the DCHA signal. This limits the speed that data can be transferred into the minicomputer. In order to operate at the maximum input data rate of the Eclipse minicomputer (1.2 MHz), a DCHA1 signal was generated to clear DCH SYNC before the end of the DCHA signal which required modifying the Data General logic.

If the preprocessor is requesting DMA at the maximum rate, the Eclipse processor will execute a number of consecutive data channel cycles. The timing diagram in Figure D-4 shows the sequence of events

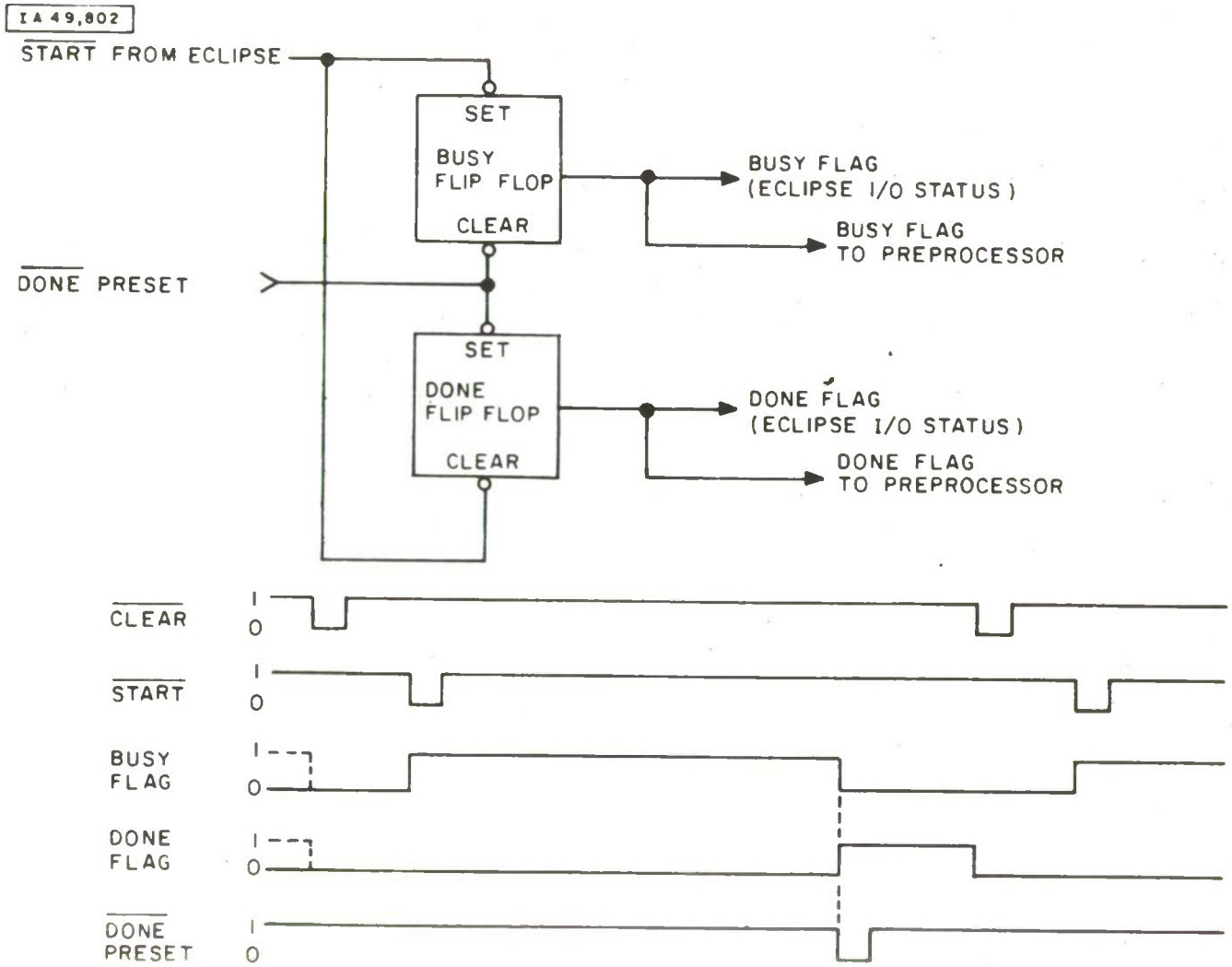

FIGURE D-1. BUSY/DONE STATUS SIGNALS

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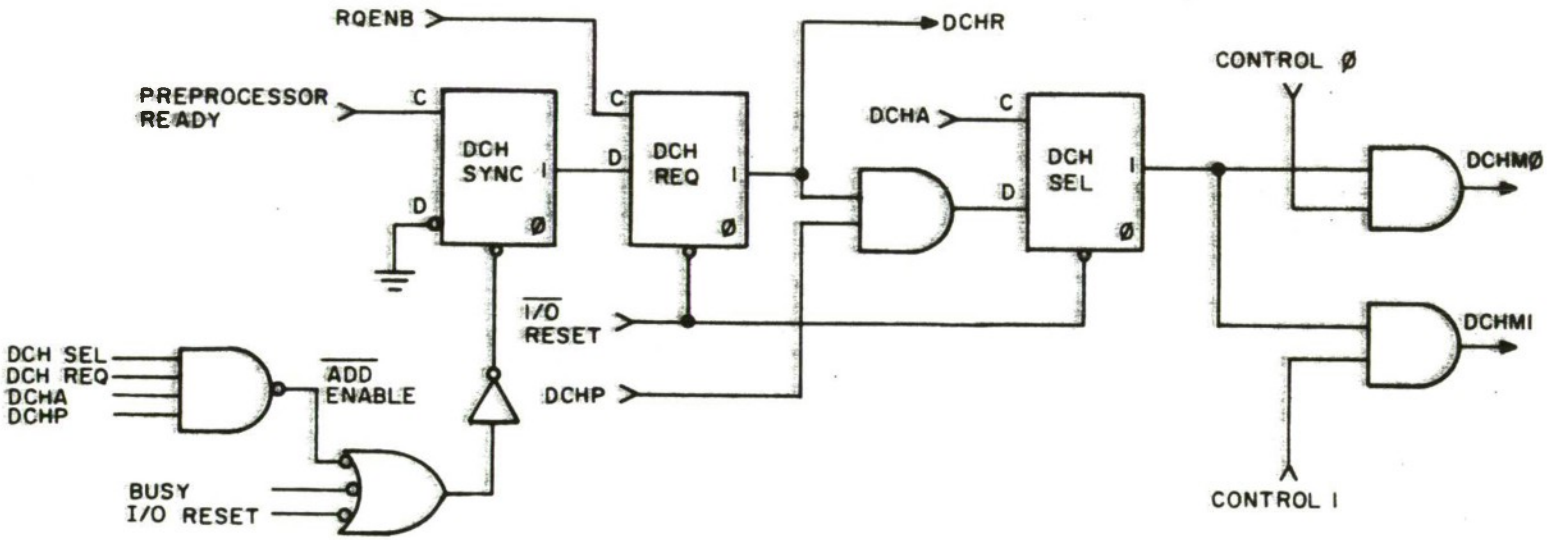

FIGURE D-2. DATA CHANNEL CONTROL NETWORK

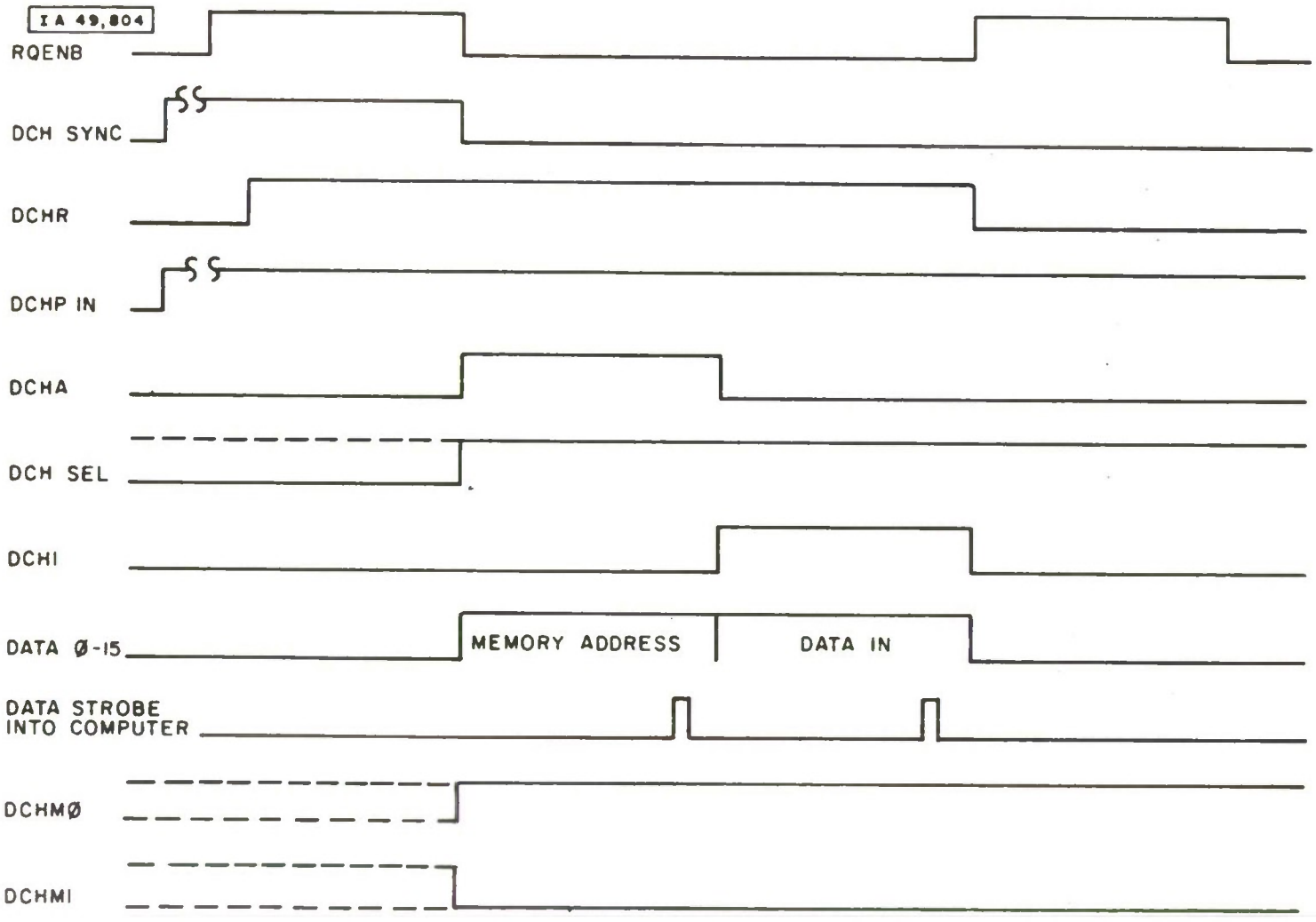

FIGURE D-3. HIGH SPEED DATA CHANNEL TIMING

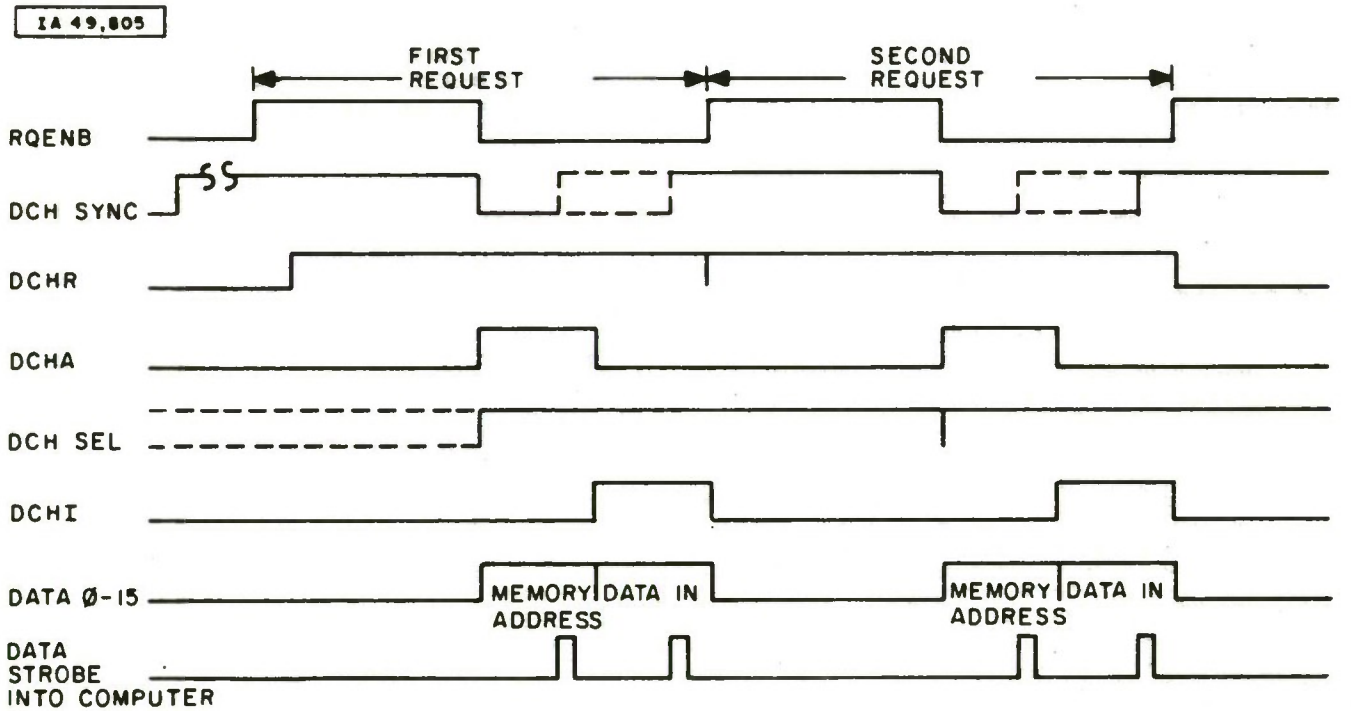

FIGURE D-4. HIGH SPEED DATA CHANNEL TIMING - CONSECUTIVE DATA IN CYCLES

for consecutive data in cycles. If the DCH SYNC flip flop is clear at the leading edge of RQENB in the data channel cycle, then RQENB clears DCH REQ. But if DCH SYNC is already set again, DCH REQ simply stays set indicating a second data channel request.

The Eclipse data channel includes circuitry that connects the interface logic to the data and control lines on the bus. The input and output data registers and address and word counters are shown in Figure D-5. The input register receives parallel data (16 bit words) from the preprocessor. The output data from this register is gated onto the data bus with either enabling signal $\overline{OB1}$ or $\overline{OB2}$. Address and word counters are also included which were described earlier. A device code of 37_8 (Octal) has been selected for this interface.

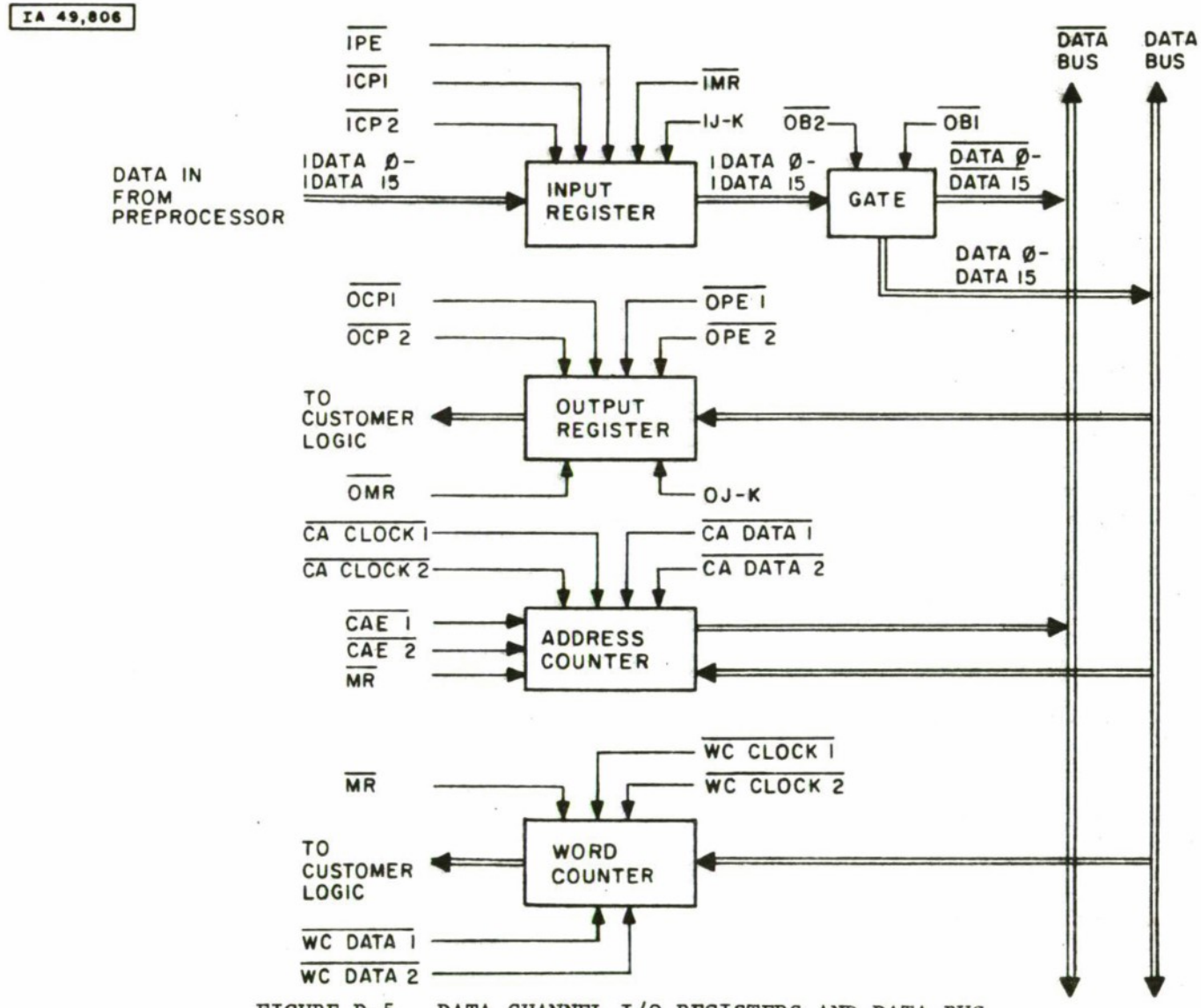

FIGURE D-5. DATA CHANNEL I/O REGISTERS AND DATA BUS

GLOSSARY

DCH	Data Channel
DCHA	Data Channel Acknowledge
DCHI	Data Channel In
DCHMØ, DCHMI	Data Channel Mode
DCHP	Data Channel Priority
DCH REQ	Data Channel Request
DCH SEL	Data Channel Select
DMA	Direct Memory Access
ETS	Experimental Test Site, located at the Stallion Station of the White Sands Missile Range, New Mexico
FIFO	First-In-First-Out
GEODSS	Ground-based Electro-Optical Deep Space Surveillance System
I/O	Input/Output
MTI	Moving Target Indication
PIM	Preprocessor Interface Minicomputer
PROM	Programmable Read Only Memory
RESEL	Resolution Element
RQENB	Request Enable