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MANUFACTURING METHODS AND TECHNOLOGY (MM AND T) MEASURE FOR FAB--ETC(U)
OCT 77 B B ADAMS, S W KESSLER, R E REED DAAB07-76-C-8120
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REPORT DOCUMENTATION PAGE

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18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Thyristor	Power Switching Component	Transcalent Thyristor
High Current SCR	Power Conditioning Component	Production Engineering
Heat-Pipe Cooling	Solid State Device	Electrical Testing of SCR

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This fourth Quarterly Report describes the progress on the MM&TE program for Transcalent (Heat-Pipe cooled) thyristors. Production engineering measures for the device and the pertinent state-of-the-art on the sample devices are included. Final test results on the engineering sample devices shipped and initial test results on the first confirmatory samples are listed.

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20. (Continued)

The present status includes the shipment of the engineering sample devices, issuance of the Test Report, plus the initiation of the fabrication of the confirmatory sample devices and the engineering analyses of the test results on all of these devices.

Plans for the next Quarter include continuation of the confirmatory sample devices, preparation of the Test Plan for these confirmatory samples, as well as the further increase in the production capacity for the pilot run phase.

(12)

MANUFACTURING METHODS AND TECHNOLOGY (MM&T) MEASURE FOR FABRICATION OF SILICON TRANSCALENT THYRISTOR

Fourth Quarterly Progress Report

Period Covered: 1 July 1977 to 30 September 1977

Object of Study: The objective of this manufacturing methods and technology measure is to establish the technology and capability to fabricate Silicon Transcalent Thyristors.

Contract No. DAAB07-76-C-8120

Approved for public release; distribution unlimited

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ABSTRACT

This fourth quarterly technical report on the MM&TE Contract DAAK07-76-C-8120 for Transcalent (Heat-Pipe cooled) SCR Thyristors describes the completion and delivery of the five engineering sample devices and the corresponding Test Report. Progress on device refinements for the Confirmatory Samples is described. Also described are the problems encountered and the results achieved in the testing of the remaining characteristics, including the measurement of some environmental capabilities for the first time.

Actual test results for the engineering samples are included to verify that the device design conforms to almost all of the electrical, mechanical and thermal specifications. An evaluation of the marginal dv/dt characteristics and possible solutions is also included.

Additional preparations for production are described as well as some refinements to the electrical test equipment. A revision to the PERT chart was prepared and submitted on 29 August 1977.

Plans for the next quarter include commencement of the fabrication and evaluation of the Confirmatory Sample thyristors, including preparation of the Test Plan. Mr. W. Peltz, ECOM, and Dr. R. Eaton, MERADCOM, visited the vendor's plant on 27 September to review the status of the program. A proposed modification to the specification was discussed prior to submission of the written request.

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PURPOSE

The purpose of this production engineering contract is to establish the technology and capability to fabricate heat-pipe cooled semiconductor power devices, silicon Transcalent Thyristors, Type J-15371. The subsequent pilot production of these devices is a part of the contract. This report covers the efforts performed by the contractor in the third quarterly period to modify the R&D device for production, establish process and fabrication methods as well as to modify and construct the varous types of test equipment required to adequately characterize the thyristor. Plans for future work are also presented, corrective action is delineated for problems that have been encountered and other information is discussed to help assure that the purpose of the contract is accomplished.

This contractual MM&TE program will establish the production techniques, establish quality control procedures and verify a pilot production capability for the J-15371 thyristor, conforming to the drawing attached to AMENDMENT 1 of SCS-477. Electrical, mechanical, thermal and environmental inspections are a part of the program as well as extensive documentation requirements, per DD1423. No high volume production facilities existed at the start of this contract for the Transcalent type of solid-state power device. However, production planning constitutes Step II of the contract. Thus, the time required to produce future large quantities of the J-15371 will be reduced for either current military requirements or future emergency requirements. Reduction of the reproductive costs are also an important objective.

The J-15371 thyristor is a 400 amperes RMS, forced air cooled solid-state power control device, utilizing integral heat-pipes for improved cooling efficiency, lighter weight and smaller size than the conventional devices with their external heat-sinks attached. Improved reliability results from these innovations. A blocking voltage capability of 800 volts minimum at 125^{o} Celsius is a requirement. Original R&D efforts were conducted successfully by RCA under Contract No. DAAK02-69-C-0609, for MERADCOM, Ft. Belvoir, VA. Potential applications include power conditioning, power switching, phase control, voltage variable power supply and motor speed control equipments.

GLOSSARY

All abbreviations, symbols and terms used in this report are consistent with the Electronics Command Technical Requirements SCS-477, dated 5 December 1974. This Technical Requirements document, in turn, references MIL-S-19500 for the abbreviations and symbols used therein except, as follows:

V_{GR} = Reverse Gate Voltage

I_{GR} = Reverse Gate Current

Note: The format used for this report is that specified in the DD 1423, namely, ECIPPR No. 15, Appendix C, augmented by MIL-STD-847A. Sub-section numbering is based on Appendix C and the applicable test methods are those referenced in MIL-STD-750B.

NARRATIVE AND DATA

1. Device

a. Description of the Structure - Refer to pages 9-13 of the First Quarterly Report for a description of the Transcalent Thyristor device, the applicable reports, and the applicable patents as well as the advantages of this heat-pipe cooled technical approach. Refer to Figure 1 in the Second Quarterly Report for the cross-section drawing of the J-15371 with the external dimensions added.

b,c. Defining the Problem Areas and Work Performed to Resolve the Problem

(1) Conversion of Design for Production - The Transcalent Thyristor design achieved under R&D Contract No. DAAK02-69-C-0609 was described in the FTR, October, 1972. Subsequent refinements have been incorporated under Contract N62269-73-C-0635 and by RCA-funded engineering projects. Additional engineering is being applied under the MM&TE program to convert the design to one more suitable for production, as described in the First, Second and Third Quarterly Reports covering the period 27 September 1976 to 30 June 1977 and below for the most recent quarterly period.

(a) Engineering Sample Phase

Fabrication of the engineering samples was completed in the previous report period. Testing of the eleven (11) total candidate devices (from which the five (5) engineering samples were selected) was concluded in July. The remaining electrical, thermal and mechanical and environmental tests were performed. Test results for these engineering samples are summarized in Section 5 of this report. Note that the devices meet almost all of the specifications not only for the acceptance of the engineering samples, but also for the confirmatory samples.

These tests were concluded in time for the shipment of the five (5) engineering samples in mid-July, per the 11 May 1977 PERT chart revision. The Test Report was also prepared and submitted in mid-July, 1977.

Government acceptance of these submissions was issued 15 August 1977 by Mr. Gordon E. McMain, Procuring Contracting Officer. Authorization to proceed with the fabrication of the Confirmatory Samples was included in the same letter.

The devices submitted in fulfillment of the Engineering Sample requirement (Serial Nos. N4, N5, N6, N8 and N11) were manufactured by RCA in Lancaster, PA, during the first half of 1977. The silicon wafers used in these devices were all diffused by RCA at either the Lancaster, PA, or Somerville, NJ, plant locations. The five samples were selected on the basis of their conformance to the specifications as well as for having completed the lengthy testing sequence in time for shipment.

The selection of other devices from this group could have delayed shipment until August or September, depending on the additional tests to be performed.

These five devices are believed to be representative of the range of fabrication variables that may be encountered on subsequent devices, except for any subsequent device design refinements that may become necessary. As reported in the separate Test Report for the Engineering Samples, all five (5) devices passed the Acceptance Tests for Engineering Samples as well as the other tests (applicable to the subsequent Confirmatory Samples) except for the dv/dt test at maximum temperature. Analysis of this characteristic is included below under "(c) Exponential Rate of Voltage Rise (dv/dt)."

(b) Confirmatory Sample Phase

Initial candidates for the confirmatory sample phase were constructed during the report period. Serial Nos. N12 and N13 passed all of the 25°C and 125°C tests of the Group A Inspections, Sub-Groups 1, 2, 3 and 4, except that Gate Condition B (Resistor) was used to pass the Exponential Rate of Voltage Rise Test (dv/dt) of Sub-Group 3. Both devices also passed Group B, Sub-Group 1 and Group C, Sub-Groups 3 and 5 tests. However, after being subjected to the 25°C below zero Group B, Sub-Group 2 tests, both devices degraded in blocking voltage capability. Refer to Section 2b,c(1)(g) of this report for an analysis of these failures and the corrective action taken.

Serial Nos. N16 and N17 were subsequently fabricated from a new diffusion lot in which the emitters were intentionally diffused shallower than in earlier lots of wafers. This shallower emitter provided a lower p-base resistivity or increased conductivity between the shorting dots and the gate structure. This change improved the dv/dt capability of the devices, but with

a corresponding increase in the gate currents. During the report period, both devices passed most of the tests of Group A, Sub-Groups 1, 2, 3 and 4, except that the gate current in Sub-Group 4 exceeded the maximum limit. This was expected. Note, however, that the dv/dt test was passed by both of these devices with the specified gate condition D (open circuit). Some of the significant test results of these two devices are summarized in TABLE 1 as evidence of their good performance.

They also passed the Group C, Sub-Group 5 thermal resistance test.

Unfortunately, after the latter test, No. N17 was found to be degraded in voltage. It will be analyzed in the next report period and corrective action taken. Serial No. N16 will continue with the remaining Group A as well as the Group B and C Inspections in the next report period.

Additional devices will be fabricated for this contract phase as soon as additional wafers are diffused, some in an attempt to duplicate the superior dv/dt characteristics of N16 and N17.

(c) Exponential Rate of Voltage Rise (dv/dt)

i. General Considerations - The test report on the engineering sample devices, delivered in July, 1977, noted that all specification limits were met with the one exception of the Exponential Rate of Voltage Rise (dv/dt) at the elevated temperature of 125°C. Several iterations of the shorting dot pattern have now been tried along with modified diffusion processing. Much of this effort has been described in the monthly and the previous quarterly reports under the contract. Improved dv/dt characteristics have resulted.

Unfortunately, the specified minimum value of 200 volts per microsecond at a case temperature of 125 $^{+0}_{-3}$°C has been achieved only under modified test conditions of the gate termination, the gate trigger characteristics or with a reduced forward blocking voltage. Extensive tests have resulted in the conclusion that this parameter is apparently limited by the basic physics of the thermal carrier generation in the large area solid state power devices. This state-of-the-art limitation has been further confirmed by the reduced dv/dt ratings of large area, phase control devices as published by four other solid state manufacturers. Refer to TABLE 2.

TABLE 1

ELECTRICAL CHARACTERISTICS
OF SCR TYPE J-15371, SERIAL NOS. N16 & N17

Device No.	V_{GT} @ 25°C (v)	I_{GT} @ 25°C (mA)	I_{GT} @125°C (mA)	V_{FM} @25°C (v)	dv/dt @125°C (v/μs)	i_{FBOM} @25°C (mA)	i_{FBOM} @125°C (mA)
Spec:	5 dc max.	500 max.	--	2.0 max.	200 min	15 max.	60 max.
N-16	1.1	780	400	1.1	281	0.5	38
N-17	1.2	720	320	1.1	281	0.6	47

TABLE 2

TYPICAL COMMERCIAL dv/dt RATINGS
AT T_C = 125°C AND GATE CONDITION D (OPEN)

Device No.	Mfr.	Applied Voltage	dv/dt Spec.
420PB	A	80% of rated V_{DRM}	100 V/μs min.
470PB	A	" " " "	100 min.
550PB	A	" " " "	100 "
C501	B	" " " "	100 "
C520	B	50% of rated V_{DRM}	100 "
C520	B	100% of rated V_{DRM}	15 "
C530	B	50% of rated V_{DRM}	100 "
C530	B	100% of rated V_{DRM}	15 "
C600	B	67% of rated V_{DRM}	100 "
C601	B	67% of rated V_{DRM}	100 V/μs min.
C602	B	67% of rated V_{DRM}	100 " "
H800-H2000	C	80% of rated V_{DRM}	100 " "
G300-G950	C	80% of rated V_{DRM}	100 " "
J3000	C	80% of rated V_{DRM}	100 " "
444Tx	D	*	20 V/μs typ.
458Tx	D	*	20 " "
464Tx	D	*	20 " "
466Tx	D	*	20 " "

*Case Temperature, Applied Voltage and Gate Condition not specified in manufacturer's published data.

The present MM&T specification for the J15371 Transcalent thyristor is a much higher 200 volts per microsecond at 100% of the rated V_{DRM}, for comparison. This Transcalent specification apparently exceeds the state-of-the-art for phase control thyristors. Also, this high temperature dv/dt characteristic was not measured under the previous R&D contract for Transcalent devices and the specification for the MM&T contract thus appears to be an overly optimistic extrapolation of room temperature data. Refer to Figure 1 for the variation of dv/dt with temperature.

ii. Theoretical Considerations - A cross-section of the Transcalent Thyristor, SCR type wafer is shown in Fig. 2. Junction J_1 is the reverse blocking junction, J_2 is the forward blocking junction, and J_3 is the cathode-to-gate junction. The emitter area is the area beneath J_3 and is limited by the diameter of the trigger finger. Also, shown in the cross-section are numerous emitter-to-base shunts (shorting dots) where the P-base region extends up to the metallized surface of the wafer.

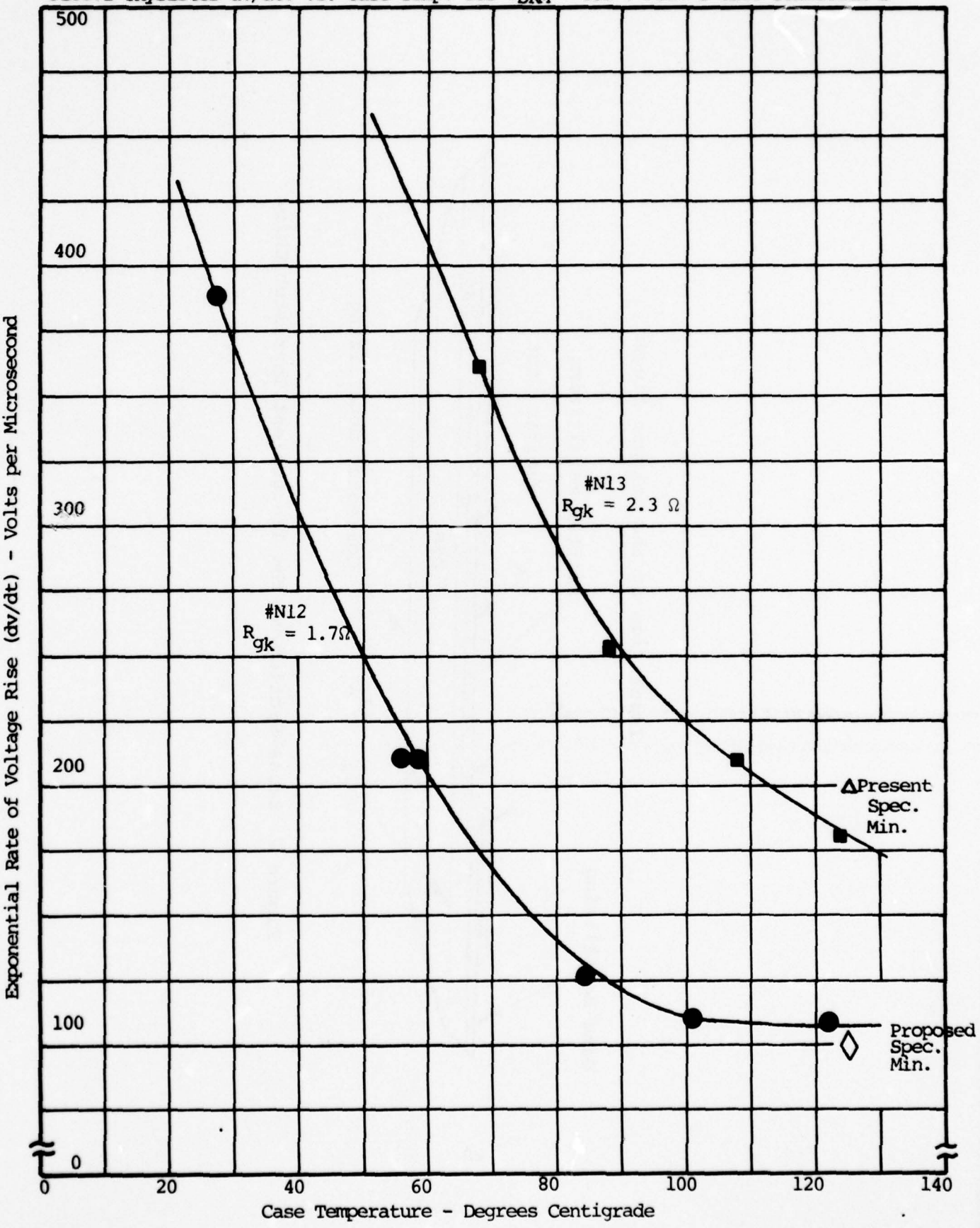
When there is a rapid rate of change of the voltage (dv/dt) applied to junction J_2, the formation of the depletion region generates a displacement current which may trigger the device into conduction. Thermally generated carriers at elevated temperatures add to this total current.

It is necessary to consider the flow of the displacement current from two different areas. One area is beneath the emitter junction, J_3, and the other area is the remaining area around J_3. If the wafer is 1.15 inches in diameter, the emitter area is 3.58 cm^2 and all of the remaining area is 3.12 cm^2 or 47 percent of the total area of the P-base in the wafer.

The applied voltage gradient is such that the displacement current flows to the emitter. That current which is generated beneath junction J_3 flows to the emitter metallizing through the shorting dots without triggering the thyristor into conduction. The current from the remaining area of the P-base flows to the outer edge of the emitter at the trigger finger around J_3. This current may not be adequately bypassed by the shorting dots and thus may turn-on

Figure 1

J15371 Thyristor dv/dt. vs. Case Temp. for V_{DRM} = 800 V Peak & Gate Condition B



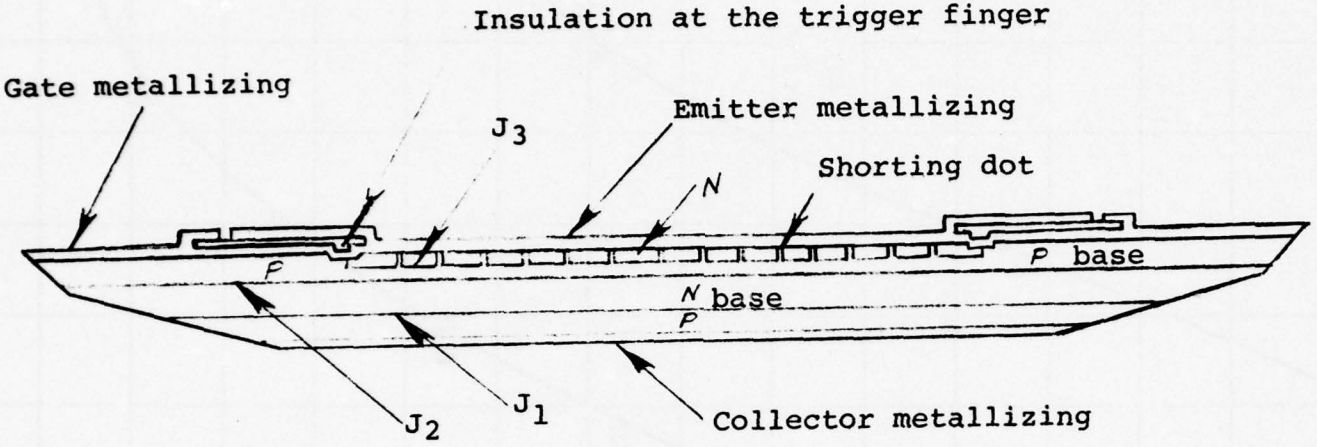


Figure 2 Cross-Section of the Transcalent Thyristor Chip

the thyristor when the voltage rises to about 0.6 of a volt. There is apparently no effective way to internally short this remaining area of junction J_2 to the emitter metallizing, as evidenced by the previous iterations of the shorting dot patterns. The results with the optimized shorting dot pattern, as described in the Second Quarterly Report, are listed in Table 3 for various gate-to-cathode terminations.

All devices in TABLE 3, except Serial Nos. N10 and N11, have 0.010 inch diameter shorting dots. N10 and N11 have 0.004 inch diameter dots of the same pattern. Figure 3 shows a definite correlation between the dv/dt values and the gate trigger current values of these thyristors diffused with the latest shorting dot pattern. Thus, as noted above, a new lot of wafers was intentionally diffused for higher gate current and the first two devices (N16 and N17) from this lot have just been tested and both meet the present high dv/dt specification at 125°C with an open gate (Condition D).

Additional devices will have to be fabricated in the future using this same schedule to verify that this correlation is repeatable with a high yield. Also, the gate current specification must be revised to a 1.0 ampere maximum to allow for the corresponding change in the gate trigger current characteristics, I_{GT}.

iii. Alternative Corrective Actions - Besides the modified diffusion schedule, noted above, other alternatives are being investigated for improving the dv/dt. As shown in TABLE 3, an external resistor can be connected between the gate and the emitter metallizing areas of the wafer to accomplish this function. Alternate methods for incorporating such a resistor have been explored during this report period. This phenomenon is the reason that a one-ohm resistor has had such a marked effect on increasing the dv/dt and high voltage blocking capabilities reported on earlier devices.

The effects of the shunting resistance were demonstrated with devices No. N12 and N13, using external resistors. At a T_C of 123°C, a V_{DRM} of 170 volts and without an external shunt, the dv/dt of N12 was only 11 v/μs. With a one-ohm shunt and a V_{DRM} of 800 v, the dv/dt was increased to 253 v/μs! This effect and those of other shunt values are plotted in Figure 4 for

TABLE 3

SUMMARY OF dv/dt and GATE CHARACTERISTICS
of TRANSCALENT THYRISTORS

	N10	N11*	N12	N13	N16	N17	Units
dv/dt at 25°C:							
Open Gate	1,010	415	181	633	633	460	v/μs
R = 1.0 ohm	--	1,010	422	633	--	--	v/μs
dv/dt at 125°C:							
Open Gate	190	55	11	63	281	281	v/μs
R for 500 mA	--	--	210	181	--	--	v/μs
R = 1.0 ohm	843	632	253	361	--	--	v/μs
Gate Trigger Current at 25°C:							
Open Gate	160	50	80	400	780	720	mA

*Shipped as an Engineering Sample in July, 1977.

Figure 3

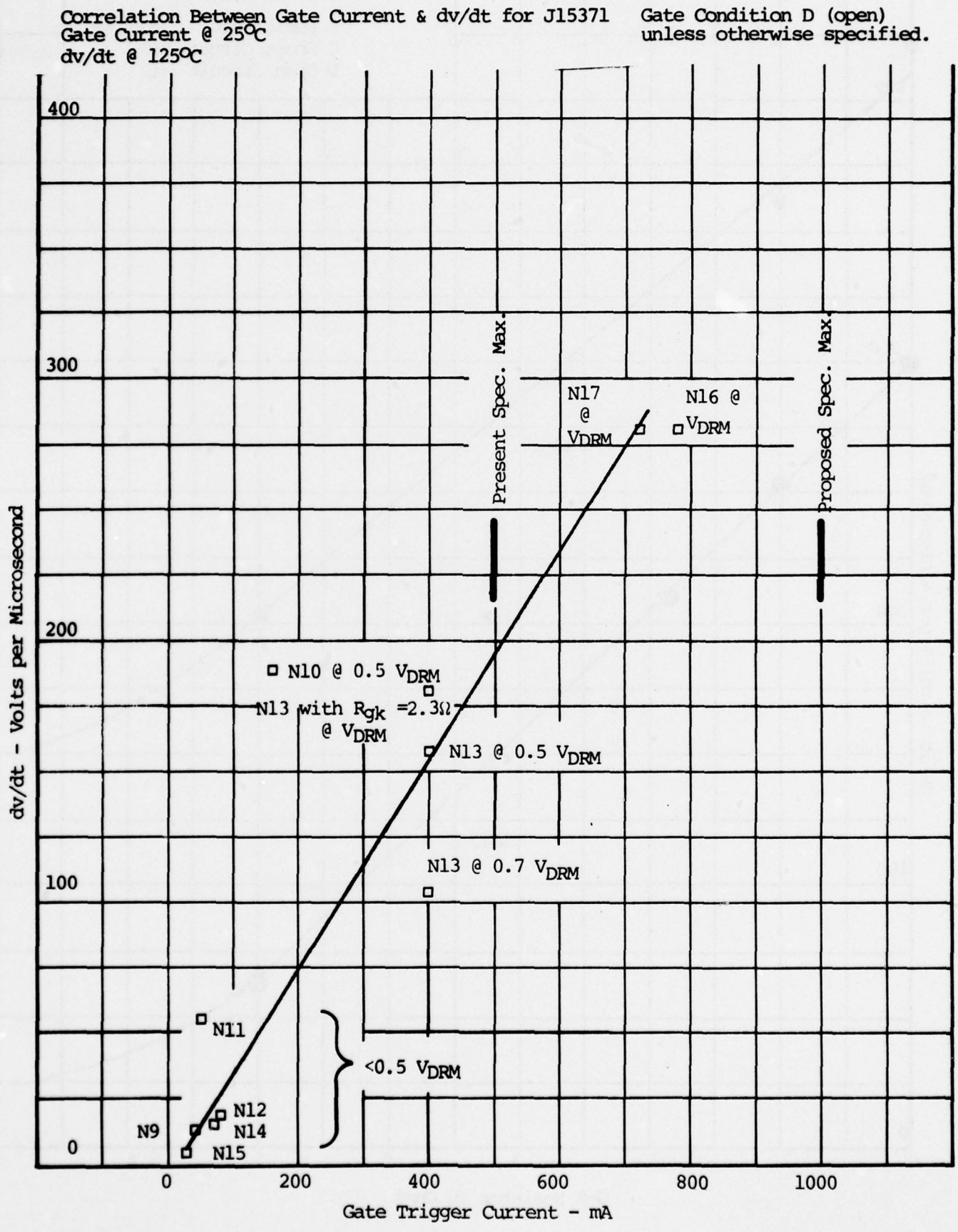
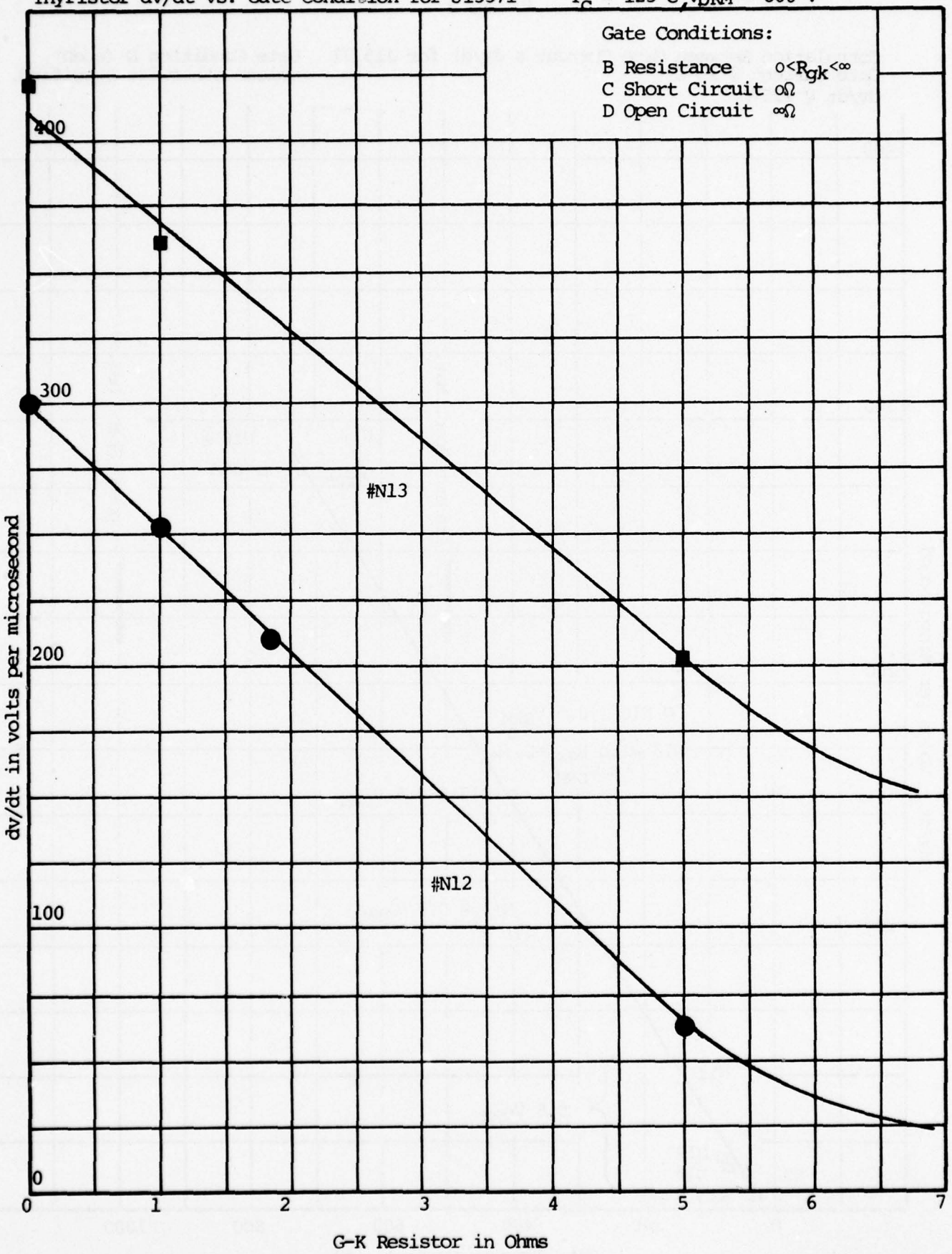

Correlation Between Gate Current & dv/dt for J15371
Gate Current @ 25°C
dv/dt @ 125°C
Gate Condition D (open) unless otherwise specified.
400
300
200
100
0
dv/dt - Volts per Microsecond
Present Spec. Max.
Proposed Spec. Max.
N17 @ VDRM
N16 @ VDRM
N10 @ 0.5 VDRM
N13 with Rgk =2.3Ω @ VDRM
N13 @ 0.5 VDRM
N13 @ 0.7 VDRM
N11
<0.5 VDRM
N12
N14
N9
N15
0
200
400
600
800
1000
Gate Trigger Current - mA

Figure 4

Thyristor dv/dt vs. Gate Condition for J15371 $T_C = 125^{\circ}C, V_{DRM} = 800$ V



various shunt values. All points are at a T_C of 125°C and a 100% V_{DRM} of 800 volts.

Note that the gate current will be increased by this system "fix." Typical values are from 100 to 600 mA increases in the forward gate currents, depending on the resistor used. A one-ohm resistor, for example, will increase the gate current by 600 mA if the gate trigger voltage, V_{GT}, is 0.6 volt. Such a value, when added to the normal gate trigger currents of the SCR, is greater than the 500 mA maximum gate current allowed by the contract specification. However, higher gate current devices are preferred by some systems designers because of the devices' reduced sensitivity to false triggering from noise, transients and other spurious signals.

Reverse gate currents will also be higher at the specified 5 volts negative D.C. measurement condition and a pulse measurement may thus be preferred to reduce the dissipation during the measurement.

Experiments were also performed to determine whether this shunt resistor can be chosen to satisfy both the dv/dt and the I_{GT} limits. To find the shunting resistance which exactly met the 500 mA maximum gate current specification, a variable resistor was used to maintain a fixed total gate current of 500 mA. This 500 mA value was maintained as the values of the resistance and the gate voltage were adjusted until N12 triggered. This thyristor triggered at a shunting resistance of 1.85 ohms. With the 1.85 ohms shunting the gate-to-emitter junction, the dv/dt was measured and found to be 210 v/μs at 125°C, as listed in TABLE 3.

The same experiment was performed with N-13. The shunting resistance to maintain a 500 mA gate current was found to be 2.44 ohms. At 125°C, the dv/dt of N-13 was 101 v/μs. If this resistor was decreased slightly to 2.3 ohms, the dv/dt measurement increased to 181 v/μs, as listed in TABLE 3.

Experiments are also underway to determine whether this resistor can be an integral part of the Transcalent Thyristor. Consideration was thus given to making the resistor a part of the heat-pipe/insulator package. The most promising approach was to paint a thick film resistor on the external surface of the ceramic insulator between the gate pin and the flange which fastens the ceramic envelope to the emitter heat-pipe. Samples of resin-based resistivity coatings were obtained from Electro-Science Laboratories, Inc. To obtain nearly the proper resistance, it was found necessary to mix two coatings to the ratio of 90-10%. The resin of the largest portion was designed to have a resistivity of 10 ohms per square and employed carbon as the conductive medium. The other resin was mixed with silver powder which lowered the resistivity of the carbon film.

The upper temperature limit for curing the resins was 220°C which precluded applying the resistor inside the package prior to bonding the heat-pipes to the wafer. When the coating was cured at 200°C, it produced a hard and smooth gray film between the metal contacts. This film was hard enough that if the resistance was less than desired, some of the coating could be trimmed-off with a precision sand blaster to tailor the resistor to the desired value.

The dv/dt characteristics of an experimental SCR No. N-14 were determined for a resistance that yielded a 500 mA gate current (1.73 ohms). A resistor of near this value was painted onto the ceramic of N-14 and its dv/dt characteristics were remeasured. At room temperature, the dv/dt doubled to 506 v/μs. At a case temperature, T_C, of 127°C, the dv/dt improved to more than six times that of the open gate test.

Subsequently, a method has been perfected for applying and trimming this resistive coating inside of the ceramic insulator where it is protected from hostile environments.

iv. Recommendations for dv/dt - It is concluded that this apparent state-of-the-art limitation should be recognized by a specification revision under the MM&T contract for both the confirmatory and pilot run phases. However, it is recognized that the modified limits must still be selected to provide adequate device performance for the government in the intended systems.

From the system designer's perspective, there are snubber circuits and resistive terminations that can be used externally to the thyristor to provide an additional dv/dt capability. As noted above, less sensitive gates are sometimes preferred. Also, the selection of higher voltage thyristors improves the dv/dt reliability at the normal, lower operating voltages of the system.

Thus, under separate cover, it is planned to submit a proposed revision to the specification. Three revisions appear desirable for satisfying this dv/dt performance characteristic. Refer to test method 4231, MIL-Std-750B and TABLE I, Group A Inspection, Sub-Group 3 of SCS-477 for a description of the dv/dt test. The gate characteristics, Methods 4221 and 4219, are included in all three groups of SCS-477.

(i) Reduce the dv/dt minimum specified value and the applied voltage at which it is measured,

(ii) Modify gate condition D (open circuit) to gate condition B (resistive termination). Note that B includes D (infinite resistance) and will still permit the testing of the better devices with an open gate circuit, and

(iii) Increase the gate trigger current limit to accommodate those devices that improve the dv/dt with the trade-off of higher I_{GT}. This approach includes both the shunt resistance and the modified diffusion schedule methods of improving the dv/dt.

Following the accumulation of data under these revised conditions in the Confirmatory Sample and Pilot Run phases, a revised procurement specification could then be prepared at the conclusion of the MM&T contract. The limits in this specification would be based on the larger statistical sample of data available at that time. Higher dv/dt limits will undoubtedly be possible at that time. These could then be used for any future procurements of production Transcalent thyristors.

d. Conclusions

The successful completion of the Engineering Sample phase verified the soundness of the basic design. This completion also verified that the wafer diffusion transition difficulties have been resolved. Unfortunately, much of the time delay incurred on the engineering samples will impact on the confirmatory sample phase of the contract, especially with the added efforts devoted to the dv/dt limitations. The proposed revision to the latter specification should avoid any further program schedule slippages since the engineering samples have met all other specifications. Thus, the confirmatory samples will be fabricated assuming approval of the proposed revisions will be forthcoming. This was the concensus at the 27 September 1977 coordination meeting.

e. Drawings

Drawings of the piece parts and sub-assemblies of the device were included in the First Quarterly Report with revisions to these engineering drawings subsequently included in the Second Quarterly Report.

2. Process, Equipment and Tooling

a. Purpose of Each Step

(1) Device Processing and Tooling

Figure 4, Engineering Drawing No. 3025577, in the First Quarterly Report showed the flow of parts through the various assembly steps and a descriptive title was listed for each operation. Also shown were the subassembly drawings and fixture drawing numbers for each operation. In both the First and Second Quarterly Reports the procedures for using the fixtures were included with a photograph of each fixture. This information continues to be used for the device fabrication and processing.

(2) Electrical and Environmental Test Equipment

The flow chart of the electrical and environmental testing sequence was given in Figure 7, Drawing No. 3025578, of the First Report. The name of the test was given as well as the special conditions and the MIL-STD-750B method number. Long-time tests had the time interval indicated in the figure. This chart remains valid for the program.

b,c. Problem Areas and Work to Resolve Problems

(1) Device Processing and Tooling

Fabrication processes that are known to limit the production quantities are being improved by improving the yields, by increasing the quantity per operation, by reducing the labor required and by more complete documentation of the processes.

(a) Standardizing Documentation

In preparation for pilot production, various RCA system documentations needed to be accomplished. Consequently, the incorporation of parts, assemblies and fixtures into the RCA specification (Standardizing) system has been initiated. System drawings of the thyristor assemblies have been made and a workbook prepared for use by the production tube builders.

This thyristor production workbook has been reviewed and updated with any corrected drawings inserted. Process sheets also have been written for the fabricating of each assembly. The standardization of this device will continue in the next period.

The value of the above procedure lies in that it assures production methods and manufacturing control of heat-pipe assemblies will be used on future devices. Parts ordering and inventoring can also be transferred to the Production Control activity.

(b) Wafer Diffusion Facilitation

There are now eight wafer diffusion furnaces in operation in the Transcalent Laboratory. The furnaces which are operated at temperatures up to 1300^{o}C have silicon carbide process tubes. Silicon carbide tubes are not prone to devitrification as is the case with quartz tubes. Silicon carbide is also more immune to damage by thermal cycling.

By having eight furnaces available for the diffusion of wafers, it is now possible to dedicate each furnace to a single operation and thus avoid the cross-contamination that was a problem previously. The furnace operations which have a dedicated diffusion tube are, as follows:

i. Phosphorus deposition,

ii. Phosphorus oxidation,

iii. Boron deposition,

iv. Boron diffusion,

v. Simultaneous diffusion,

vi. Simultaneous oxidation,

vii. Boron oxidation, and

viii. Emitter diffusion.

These separate facilities reduce the possibility of cross-contamination of the silicon wafers during the various diffusion processes and are thus expected to improve the blocking voltage capabilities of future devices. Larger lot sizes are being started to improve the yields and to reduce the labor content per wafer.

(c) Exhaust System Refinements

The exhaust and bake-out system for the high voltage center chamber of the device was limited to two devices per processing cycle of one-half day. A system refinement was designed and the machined parts fabricated for increasing the exhaust system capability from two to six ports. The new exhaust system will be completed in the next report period to triple the present exhaust and back-fill process capability to six thyristors simultaneously.

(d) Brazing Fixture Procurement

To increase the number of sub-assemblies that can be brazed simultaneously (in keeping with the goals set by the MM&T contract) it is planned to double the quantity of heat-pipe brazing fixtures. The purchase orders have been written and the outside vendor has initiated fabrication. Delivery is expected within the next period. These fixtures are being capitalized by RCA for use on the MM&T and other Transcalent device programs.

(e) Stampings Vendor Change

A new vendor has been selected for manufacturing the stamped or drawn metal parts. Another vendor was used to make the engineering samples but they were unable to hold the tolerance specifications as is necessary to further increase the yield of vacuum-tight assemblies. The new vendor claims that all of the parts can be manufactured to the specifications and at a lower unit part cost. An on-site inspection of the new vendor was favorable and orders have been placed for several important stamped parts. These parts are the cathode flange, the weld ring, the cathode weld flange, and the anode weld flange.

These parts have been standardized and thus, the parts have been ordered through the production control system which requires production grade tooling, incoming inspection and controls. The new parts are expected to be delivered from the outside vendor in the next period.

(f) Sub-Assembly Relocation

The heat-pipe sub-assembly work area has been physically relocated into a power device manufacturing area. The work is still being performed by an hourly experimental tube builder at the new site. However, this move represents the first step toward the planned in-factory transistion to lesser skilled employees. For example, meetings between factory, quality control and engineering personnel have been initiated relative to the heat-pipe sub-assembly production. These meetings will continue in the next report period.

(g) Welding Process Variations

During this report period, two new thyristors failed at test when the silicon delaminated or separated in the plane of the wafer. This is a phenomena which has never been observed with previously made devices. A complete review of the processing was performed to explain the device failures. One item found was that both devices, N12 and N13, which cracked had been welded by a new operator using greater arc current and a modified tacking technique. The weld, when analyzed and measured, was found to be about 50 percent greater in depth than on earlier welded units.

It is thus believed that the deeper Heliarc welding variation introduced residual stresses into the package, causing the silicon to crack. To prevent a recurrence of this problem, the welding schedule used successfully by the previous operator for the engineering samples has been standardized and inscribed into the welding fixture.

Since this corrective action has been taken another unit, N17, has also cracked. This device was welded by using the correct welding schedule. Because of this failure, all processes and handling conditions are being reexamined for another possible cause of the cracking. Tensile and bending moment tests are also planned to help analyze the stresses that exist.

(2) Electrical, Thermal and Environmental Test Equip.

(a) Status

All test equipments operated satisfactorily for the evaluation of the engineering samples. However, some refinements have been incorporated, as described below, to improve the evaluation of the Confirmatory Samples.

Some of the environmental tests required the transit of the engineering sample devices to another location where suitable facilities were available. These tests included the Salt Atmosphere (at RCA, Camden, NJ) and the Constant Acceleration Tests (at AVCO, Boston, MA). Details of these test results are included below in Section 5.

All of the electrical test equipments were listed in Table 1 of the Second Quarterly Report. In the same report, the tests performed in each equipment were listed in Table 2. Actual test results are listed in Section 5, "Data and Analysis" of this report. Test procedures were included in the Appendices of the Second and Third Quarterly Reports.

Functional block diagrams for each of the test sets were included in Appendix C of the First Quarterly Report. Photographs of the electrical test equipments were included in Figures 3 through 12 of the Third Quarterly Report.

Layouts of the various test equipments were included in the Appendix of the "Report of Test on Silicon Transcalent Thyristor Engineering Samples," dated 15 July 1977 and issued separately.

(b) Surge Current Test Set

The surge current test set was revised slightly to correct some erratic start-up behavior in the heating current supply. Additional work is required for automatic recycling but this work does not affect the thyristor evaluation of present samples.

A calibration check of this equipment disclosed that a meter used to measure the average heating current applied to the thyristor under test (DUT) was inaccurate in that actually a current of 262 amperes instead of the required 250 amperes were being applied. All units tested, to date, have passed this more severe test at the abnormally high heating current. The meter was subsequently repaired to indicate the correct value. This equipment and the surge test were described in the Third Quarterly Report, Item (f), page 28.

(c) Blocking Voltage Life Test Set

A second oven and blocking voltage supply system was set-up to make the initial oven available for other tests that require elevated temperatures and high voltages. In fact, a third oven is being modified also for the blocking voltage life test of additional devices. This test was described in the Third Quarterly Progress Report, Item (d), on page 25.

(d) Turn-Off Time Test Set

This test equipment was improved by adding a sharp rise-time, synchronizing trigger pulse circuit and a pulse amplifier for the DUT to allow for units requiring higher gate currents. Higher gate currents were diffused, as described above, to improve the dv/dt characteristics. This equipment and test were described in the Third Quarterly Report, Item (e), page 28.

(e) Exponential Rate of Voltage Rise (dv/dt)

Figure 9 in the Third Quarterly Report showed the dv/dt test set. The resistance of the high voltage RC network for charging a capacitor at an exponential voltage rate is variable. The range of R required exceeded that originally installed in the test set. A larger potentiometer was subsequently installed to allow variations of the applied dv/dt rate from less than 30 to over 500 volts per microsecond. This facilitated the extensive dv/dt measurements at various temperatures, reported elsewhere in this report.

At each temperature and peak voltage value, faster and faster rise times were applied to the DUT by reducing R. The dv/dt value is determined as that limiting value just prior to the value where DUT begins to conduct due to the spontaneous turn-on caused by the displacement currents in the internal capacitance of the device.

(f) Test Equipment Calibration Schedules

Electrical test equipment calibration dates are listed in Table 4. These dates supercede those listed in the Test Procedures included in the Appendices of the Second and Third Quarterly Reports.

A schedule has also been established for the recalibration of these equipments on a regular basis with a complete printed service request to be issued as authorization to recalibrate each equipment. In the next report period, the first computer call-out for the recalibration of the various measuring devices will take place. This call-out occurs automatically at four to six months intervals. The calibration is carried out by the RCA Meter Laboratory Calibration and Standards Dept.

TABLE 4

ELECTRICAL TEST EQUIPMENT CALBIRATION SCHEDULE

Test Set	MIL-Std-750B Test Method	Test Description	Date of Most Recent Calibration
Blocking Current	1001.1	Barometric Pressure (reduced)	July 13, 1977
Blocking Current	4206.1	For. Blocking Current, A.C. Method	July 13, 1977
Blocking Current	4211.1	Rev. Blocking Current, A.C. Method	July 13, 1977
Gate Trigger Voltage or Current	4219	Rev. Gate Current	#
	4221.1	Gate Trigger Voltage or Current	#
Blocking Voltage Life Test	Para. 4.6.1	Blocking Voltage Life Test	Sep. 21, 1977
	Alternate 1001.1	Barometric Pressure (reduced)	Sep. 21, 1977
Other Electrical Test Equipment - (Separate Test Set for Each Method)	4224	Pulse Circuit Com-Turn-Off Time	July 22, 1977 & May 19, 1977
	4066.2	Surge Current	July 13, 1977

#Meters calibrated prior to installation in the cabinet in the first or second quarter of the contract. Recalibration in the test equipment is scheduled for the next quarter in preparation for the testing of the confirmatory samples.

TABLE 4 (Continued)

ELECTRICAL TEST EQUIPMENT CALIBRATION SCHEDULE (Continued)

Test Set	MIL-Std-750B Test Method	Test Description	Date of Most Recent Calibration
Other Electrical Equipment (Cont.)	3151	Thermal Resistance, General	Aug. 20, 1977
	4231.2	Exponential Rate of Voltage Rise	July 13, 1977
	4226.1	Forward "ON" Voltage	Sep. 14, 1977
	4201.2	Holding Current	#
	Para.4.6.2	Thermal Fatigue Test	#

#Meters calibrated prior to installation in the cabinet in the first or second quarter of the contract. Recalibration in the test equipment is scheduled for the next quarter in preparation for the testing of the confirmatory samples.

Environmental test equipment calibrations in the RCA-Lancaster environmental laboratory are also performed at four to six months intervals. The latest calibration dates are listed in Table 5.

d. Conclusions

The process, equipment and tooling have been designed, fabricated and used to fabricate and evaluate the engineering sample devices. More devices were fabricated than were shipped in fulfillment of the Engineering Sample requirement. This approach enabled a wider variety of process changes and device characteristics to be evaluated, replaced failed devices with operable units and provided units for the information only test of constant acceleration capability and other tests, such as, the dv/dt evaluation performed subsequently to the shipment of the five engineering sample devices.

The through-put of some of the equipment has been increased for the confirmatory sample phase and the larger pilot run. Causes of two failures of the initial confirmatory samples were analyzed and corrected.

The modified processes, tooling and equipment described in this and the prior reports have succeeded in producing and evaluating the engineering sample devices in accordance with SCS-477 and paragraph F.47. This evaluation was completed during this report period. Any additional limitations that become evident will be corrected in the confirmatory sample phase.

Orders have been placed for additional fixtures that will be necessary to fabricate the larger quantity of pilot run samples under this contract. The heat-pipe sub-assembly work area was relocated to the Power Devices manufacturing area.

e. Drawings and Photographs of Tooling and Equipment

Copies of the drawings of the special tools and fixtures were included in the First Quarterly Report along with Block Diagrams of the test equipment. Tools and fixtures that were revised were included in the Second Quarterly Report. Photographs of these items were included in both reports.

Photographs of the electrical test equipment were included in the Third Quarterly Report with text references that describe each equipment item.

TABLE 5

ENVIRONMENTAL TEST EQUIPMENT CALIBRATION SCHEDULE

MIL-Std-750b Test Method	Test Description	Test Equipment	Date of Most Recent Calibration
1051	Thermal Shock (Temperature Cycling)	Humidity & Temp Cabinets	May & June, 1977
		Altitude & Temp Cabinets	June & Sep, 1977
		Temperature, only Cabinets	April & Aug, 1977
1021	Moisture Resistance	Humidity & Temp Cabinets	May & June, 1977
2016	Shock	Accelerometer & Charge Amplifier	July & Sep, 1977
		Oscilloscope	August, 1977
2056	Vibration, variable frequency	Exciter System & Console	August, 1977
		Frequency Counter	August, 1977
		Oscilloscope	August, 1977
		Accelerometer and Charge Amplifier	July & Sep, 1977
1001	Reduced Barometric Pressure	Vacuum Gauge	July, 1977
1041	Salt Atmosphere	RCA, Camden, NJ, facility	(To be determined)
2006	Constant Acceleration	AVCO, Boston, MA, facility	Next calib. 12/77
Para.4.6.2	Thermal Fatigue	(Refer to Table 4)	

Testing procedures for the electrical test equipment were included in Appendix C of the Second Quarterly Report and in the Appendix of the Third Quarterly Report.

3. Flow Chart of Manufacturing Process Yield

Manufacturing process yields are to be determined during the Pilot Run.

4. Equipment and Tooling Costs

This information is not included since such a data requirement is generally not applicable to a Firm Fixed Price Contract on equipment and tooling that is purchased and furnished by the contractor.

5. Data and Analysis

a. Inspections

(1) Engineering Sample Devices

Group A, B and C Inspections as specified in SCS-477 were concluded during the report period on the engineering sample devices. The minimum acceptance criteria are those specified in Section F.47 of the contract, as follows:

TABLE I - GROUP A INSPECTION

Sub-Group 1	Visual and Mechanical Inspection
Sub-Group 2	Forward Blocking (at 25°C)
Sub-Group 3	Forward Blocking Current (at 125°C)
Sub-Group 4	On-State Voltage (at 100°C) and Holding Current (at 25°C)

All engineering test samples were tested for compliance with Section 3 in accordance with Section 4 of SCS-477. In a few cases, sample quantities were tested rather than all eleven devices.

To date, all mechanical, electrical, thermal and environmental tests have been completed on the engineering sample devices. Actual results are listed on the Test Data Record Forms, TABLE 6a, b, c and d. These same tests have begun on the initial Confirmatory Sample devices. Results to date, are included in TABLES 7a, b, c and d.

(2) Confirmatory Sample Devices

These devices will be inspected in accordance with paragraph 4.4 of the sampling plan included in this paragraph of SCS-477. The requirements of paragraph F.48 of the contract and 1.2.6 and 3.1.8 of ECIPPR No. 15 will also be observed.

Initial tests on the first four confirmatory samples are listed in TABLES 7a, b, c and d.

TABLE 6a TEST DATA RECORD FORMS - ENGINEERING SAMPLE DEVICES

ITEM: SILICON TRANSCALENT THYRISTOR, J15371 CONTRACT: DAA B07-76-C-8120

SPEC: SCS-477 5 DECEMBER 1974 & MFR: RCA (EO&D) LANCASTER, PA.

AMENDMENT - 1 31 AUGUST 1976 BUYER: COMM.SYS.PROCUREMENT BRANCH (USAECOM),FT.MONMOUTH,N.J.

GROUP	A											
SUBGROUP	1	2	2	4	4	4	3	3	3	3	4	4
NO.UNITS TESTED	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
TEST	Visual & Mech.	Reverse Current	Forward Blocking	Gate Trig.V	Gate Trig.I	Holding Current	Reverse Current	Forward Block'g	Gate Trig.V	Exp.Rate V Rise	Turn-off Time	On State Voltage
MIL-STD-750 METHOD	2071	4211	4206	4221	4221	4201	4211	4206	4221	4231	4224	4226
TEST CONDITION	Visual Inspt.	25°C					125°C				25°C	
SYMBOL	-	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	I_H	i_{RBOM}	i_{FBOM}	V_{GT}	dv/dt	t off	V_{FM}
MAX.	-	15mA	15mA	5Vdc	500mAdc	500mAdc	60mA	60mA	5.0Vdc		150µs	2.0V
MIN.	-									200V/µs		
1st, 2nd & 3rd Qtrs. 1977 Date Tested UNIT NO.	A R C E C J	800 V pk Rev.	800 V pk.				800V pk Rev.	800V pk		800 V pk. Gate Cond* B D	100 A pk 800 V pk Rev.	250 A avg.
N1	✓	0.3	0.4	1.1	545	4	53	75	0.5		34	1.3
N2	✓	0.2	0.3	1.1	620	4	40	>72	0.5	— 50	36	1.3
N3	✓	0.3	0.3	1.0	535	4	70	>64	0.5	152 152	32	1.2
N4	✓	0.2	0.2	0.6	23	12	5	6 Δ	0.3	31 1	68	1.4
N5	✓	0.2	0.2	0.7	53	9	5	10	0.3	21 3	46	1.5
N6	✓	0.2	0.2	0.6	30	9	3	6	0.3	26 1	48	1.5
N7	✓	0.2	0.2	0.6	73	14	3	6	0.3	27 5	73	1.6
N8	✓	2.7	0.3	0.6	30	9	12	13 Δ	0.3	1,012 28	54	1.4
N9	✓	0.3	0.5	0.6	40	1	3	4 ΔΔ	0.2	50 14	90	1.2
N10	✓	0.3	0.5	1.1	160	8	28	41	0.5	843 190	36	1.3
N11	✓	2.0	0.6	0.8	50	6	25	37 Δ	0.4	632 55	38	1.4

*Test performed at T_C = 125 $^{+0}_{-3}$°C but with reduced voltage on some devices. were much higher.

Note: Details of test conditions are given in spec.

ΔΔGate Condition A ΔGate Condition B

TABLE 6b

CONTR'S. TYPE: J15371 DATE TEST COMPLETED: SAMPLE NOS. Page 2 of 4

MFR'S. TYPE: J15371 DATE TEST BEGUN: February, 1977 FR. N1 TO N11

B														
1	1. Final Measurements			2			3. Final Meas.		4. Final Measurements					
10%	10%	10%	10%	100%	100%	100%	10%	10%	10%	10%	10%	10%		
Surge Current	Reverse Current	Forward Block'g	Rev. Gate Current	Gate Trig. V	Gate Trig. I	On-state Volt.	Temp. Moist	Cycle & Resist	Blocking per para.	Voltage 4.6.1	Life	Test		
4066	4211	4206	4219	4221	4221	4226	1051	1021	4211	4206	4211	4206		
► 25°C	25°C →			-25°C →			4211	4206 →	25°C →		125°C →			{case temp, T_C
I_{FM}	i_{RBOM}	i_{FBOM}	I_{GR}	V_{GT}	I_{GT}	V_{FM}	i_{RBOM}	i_{FBOM}	i_{RBOM}	i_{FBOM}	i_{RBOM}	i_{FBOM}		
	15mA	15mA	1.0Adc	10Vdc	1000 mAdc	2.3V	15mA	15mA	15mA	15mA	60mA	60mA		
10 Surges 4,000 A pk. 250 A avg.;	800V pk 800 V pk.	800V pk	5 Vdc			250 A Avg.	10 & 5 cycles -25 to +125°C 100% Humidity		500 hr. 800 V pk ac 125°C					
N1	20.6**	51.5**	0.5	1.3	760	1.5	0.2**	0.2**	0.3##	0.4##	53##	75##		
N2	0.2	0.3	2.2	1.4	880	1.7	0.2	0.3	0.3##	0.3##	--	--		
N3	20.6**	4.1**	2.5	1.3	720	1.5	41.2**	10.3**	--	--	--	--		
N4	0.2	0.2	0.2	0.7	40	1.4	0.2	0.2	0.2	0.2	5	8Δ		
N5	0.2	0.2	0.4	0.8	70	1.4	0.2	0.2	0.2	0.2	5	5		
N6	0.4	0.3	0.2	0.7	40	1.5	<0.1	<0.1	0.2	0.2	3	7		
N7	0.2	0.3	0.5	0.8	90	1.6	0.4	0.2	--	--	--	--		
N8	3.7	0.2	0.2	0.8	50	1.4	3.3	0.2	--	--	--	--		
N9	0.3	0.5	0.3	0.7	50	1.1	0.2	0.5						
N10	0.3	0.6	0.8	1.2	250	1.3	<0.1	<0.1	0.4##	4.6##	52##	41##		
N11	2.1	0.9	0.3	1.1	90	1.3	2.1	0.9	--	--	--	--		

**Device degraded in blocking voltage on another test, but no further degradation occurred on this test.

ΔGate Condition B

##Operated almost 200 hours at 70% to 100% peak voltage and T_C approx. 100°C. Tests terminated to install other devices.

GROUP	C									
SUBGROUP	1					2.Final Measurements				
NO.UNITS TESTED	100%	100%	100%	100%	100%	10%	10%	10%	10%	10%
TEST	Physical Dimens.					Shock,	Vibration,	Constant	Accel.	
MIL-STD-750 METHOD	2066					2016	2056	2006		
TEST CONDITION	Figure 1					4211	4206	4221	4221	4226
SYMBOL	A	B	C	D	E	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	V_{FM}
MAX.	5.00"	3.475"	0.700"	1.857"		20mA	20mA	5Vdc	500mAdc	2.5V
MIN.		3.425"	0.600"		6.00"					
UNIT NO.						500 G, 1 ms 5 G, 100-1000 Hz (Values after Shock and Vibration)		For information only - Not a spec. requirement 500 G		
N1	4.81	3.468	0.668	1.815	8.75	41.2**	3.6**	(Can't trigger gate) —		
N2	4.76	3.442	0.669	1.821	8.75	0.3/340#	0.3/6.7#	1.0/0.8#	400/300#	1.4/>3.0#
N3	4.80	3.470	0.677	1.807	8.75	268**	18.6**	(Can't trigger gate) —		
N4	4.73	3.462	0.634	1.806	7.25	0.2	0.2	0.6	30	1.3
N5	4.72	3.452	0.626	1.810	7.25	0.2	0.3	0.6	50	1.4
N6	4.72	3.464	0.622	1.806	7.25	0.2	0.2	0.6	20	1.6
N7	4.68	3.423	0.627	1.819	7.25	0.2	28.9**	0.7	60	1.7
N8	4.74	3.466	0.641	1.819	7.38	3.2	0.2	0.6	30	1.4
N9						0.3#	0.5#	0.6#	30#	1.2#
N10						0.2	0.4	0.9	160	1.4
N11	4.76	3.474	0.649	1.809	7.25	1.9	1.4	0.8	50	1.4

**Device degraded in blocking voltage on another test

#After all three tests of Sub-Group 2, other data were measured after shock and vibration tests.

TABLE 6d

	3.Final Measurements					4.Final Measurements					5		
	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	100%		
	Reduced Barometric Pressure					Salt Atmosphere, Thermal Fatig.					Thermal Resistance		Device Status
	1001					1041	para. 4.6.2				3151		9/30/77
	4211	4206	4221	4221	4226	4211	4206	4221	4221	4226			
	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	V_{FM}	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	V_{FM}	θ_{J-c}		
	20mA	20mA	5Vdc	500mAdc	2.5V	20mA	20mA	5Vdc	500mAdc	2.5V	0.15°C/Watt		
	15 mm Hg 800 V pk					24 hrs			200 cycles 250 A avg. "ON"		250 Adc		
											Initial	After -25°C	
N1	11.3**	67.0**	0.8	140	1.4	26.8Δ	30.9Δ	0.9Δ	140Δ	1.3Δ	0.19	0.39	Failed
N2	0.2	0.3	1.1	640	1.4	0.3Δ	0.3Δ	1.1Δ	640Δ	1.4Δ	0.14	0.12	Failed
N3	—	—	—	—	—	28.9Δ	10Δ	1.1Δ	550Δ	1.4Δ	0.15	0.12	Failed
N4	0.2	0.2	0.6	30	1.5	0.2	0.2	0.6	20	1.4	0.08	0.12	Shipped
N5	0.2	0.2	0.6	50	1.6	0.3Δ	0.3Δ	0.6Δ	45Δ	1.4Δ	0.13	0.12	Shipped
N6	0.2	0.2	0.6	20	1.6	0.1	0.2	0.6	25	1.4	0.16	0.15	Shipped
N7	0.2	45**	0.7	70	1.6	0.5Δ	>20Δ	0.7Δ	70Δ	1.6Δ	0.14	0.15	Degraded
N8	3.3	0.2	0.6	30	1.4	2.7	0.2	0.6	35	1.4	0.11	0.12	Shipped
N9	0.2	0.5	0.6	30	1.2	0.1Δ	0.4Δ	0.6Δ	30Δ	1.0Δ	0.11	0.11	Operable
N10	0.2	0.5	0.9	160	1.4	0.2Δ	0.4Δ	0.9Δ	160Δ	1.4Δ	0.08	0.09	Operable
N11	1.9	0.7	0.8	50	1.3	1.9	0.6	0.8	50	1.4	0.09	0.08	Shipped

ΔFollowing Thermal Fatigue Test. Other data are Final Measurements following both tests of Sub-Group 4.
**Device degraded in blocking voltage on another test, but no further degradation occurred on this test.

b. Discussion of Inspection Results

The test results on the eleven devices built during the engineering phase reveal an obvious consistency and reproducibility of most of the electrical, mechanical, environmental and thermal characteristics. The basic device design is thus judged to be adequate. Specific comments, analysis and discussion of the test results are listed below by inspection sub-group in SCS-477. Refer to TABLEs 6a, b, c and d for both the specifications (spec.) and the actual measured values.

(1) TABLE I - Group A Inspections

(a) Sub-Group 1

All devices are acceptable at Visual and Mechanical inspection.[@Δ]

(b) Sub-Group 2

The room temperature forward[@] and reverse blocking currents at 800 volts are all well within the spec.[Δ]

(c) Sub-Group 3

Improvement in the forward[@] and reverse leakage current characteristics has occurred at 125°C. The gate voltages are well within spec. and the dv/dts at the high temperature of 125°C are obviously an area for further improvement efforts, as discussed in Section 1 of this report.[Δ]

(d) Sub-Group 4

The gate trigger voltages, holding currents[@] and on-state voltages[@] are all in spec. The gate currents on later devices show considerable improvement, but changes to improve the dv/dt characteristics may increase the I_{GT} too. The turn-off times were well within the spec. on all of the devices.[Δ]

[@]Minimum acceptance criteria for engineering samples.

[Δ]Remarks refer to the engineering samples test results. They are also generally true for the initial confirmatory sample test results.

(2) TABLE II - Group B Inspections

(a) Sub-Group 1

The surge current tests of all eleven devices verified that they all passed this rigorous 10 surges, pre-heated test with reapplied reverse blocking voltage.$^{\Delta}$ This test was not included in the previous R&D Contract.

(b) Sub-Group 2

All test results at 25 degrees C below zero were in spec. In addition, the thermal resistance was measured on all devices both before and after this test to detect any hidden damage that might have been caused by the frozen starts. Ten of the eleven devices tested showed no damage (refer to TABLE 6d). Only the first device had its blocking voltage as well as its thermal resistance degraded by this test.

(c) Sub-Group 3

These environmental tests of temperature cycling and moisture resistance were performed for the first time during the engineering phase. No degradation occurred to any of the eleven devices.

(d) Sub-Group 4

Performance of this 500 hours, 800 volts, 125^{o}C life test was successfully completed on a statistical sample of three devices with three more tested for almost 200 hours each without degradation. These six were thus selected (somewhat randomly) as representative of the entire lot of devices. This test was not performed in the previous R&D Contract.

(3) TABLE III - Group C Inspections

(a) Sub-Group 1

Nine of the eleven devices had their physical dimensions measured. Refer to Figure 1 in the Second Quarterly Report for the locations of the dimensions A through E. It is obvious that the mechanical design conforms to the Figure 1 dimensions.

TABLE 7a TEST DATA RECORD FORMS - CONFIRMATORY SAMPLE DEVICES

ITEM: SILICON TRANSCALENT THYRISTOR, J15371 CONTRACT: DAA B07-76-C-8120

SPEC: SCS-477 5 DECEMBER 1974 & MFR: RCA (EO&D) LANCASTER, PA.

AMENDMENT - 1 31 AUGUST 1976 BUYER: COMM.SYS.PROCUREMENT BRANCH (USAECOM),FT.MONMOUTH,N.J.

GROUP	A											
SUBGROUP	1	2	2	4	4	4	3	3	3	3	4	4
NO.UNITS TESTED	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
TEST	Visual & Mech.	Reverse Current	Forward Blocking	Gate Trig.V	Gate Trig.I	Holding Current	Reverse Current	Forward Block'g	Gate Trig.V	Exp.Rate V Rise	Turn-off Time	On State Voltage
MIL-STD-750 METHOD	2071	4211	4206	4221	4221	4201	4211	4206	4221	4231	4224	4226
TEST CONDITION	Visual Inspt.	25°C →				→	125°C →			→	25°C →	
SYMBOL	-	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	I_H	i_{RBOM}	i_{FBOM}	V_{GT}	dv/dt	t off	V_{FM}
MAX.	-	15mA	15mA	5Vdc	500mAdc	500mAdc	60mA	60mA	5.0Vdc		150µs	2.0V
MIN.	-									200V/µs		
3rd Qtr, 1977 Date Tested UNIT NO.	A R C E C J											
N12	✓	0.2	0.2	0.8	80	1	2	6	0.4	253*		1.1
N13	✓	0.2	0.1	1.1	400	1	3	5	0.6	361*		1.2
N16	✓	0.4	0.5	1.1	780	8	13	38	0.6	281Δ	46	1.1
N17	✓	0.3	0.6	1.2	720		24	47	0.7	281Δ		1.1

*Tested @ $T_C = 125\ ^{+0}_{-3}$°C, V_{AA} = 800 v and Gate Condition B.

ΔTested @ $T_C = 125\ ^{+0}_{-3}$°C, V_{AA} = 800 v and Gate Condition D.

Note: Details of test conditions are given in spec.

TABLE 7b

CONTR'S. TYPE: J15371 DATE TEST COMPLETED: SAMPLE NOS.Page 2 of 4

MFR'S. TYPE: J15371 DATE TEST BEGUN: FR. TO

B													
1	1.Final Measurements			2			3.Final Meas.		4.Final Measurements				
10%	10%	10%	10%	100%	100%	100%	10%	10%	10%	10%	10%	10%	
Surge Current	Reverse Current	Forward Block'g	Rev.Gate Current	Gate Trig.V	Gate Trig.I	On-state Volt.	Temp. Moist	Cycle & Resist	Blocking per para.	Voltage 4.6.1	Life	Test	
4066	4211	4206	4219	4221	4221	4226	1051	1021	4211	4206	4211	4206	
➤ 25°C	25°C →			-25°C →			4211	4206 →	25°C →		125°C →		{case temp, T_C
I_{FM}	i_{RBOM}	i_{FBOM}	I_{GR}	V_{GT}	I_{GT}	V_{FM}	i_{RBOM}	i_{FBOM}	i_{RBOM}	i_{FBOM}	i_{RBOM}	i_{FBOM}	
	15mA	15mA	1.0Adc	10Vdc	1000 mAdc	2.3V	15mA	15mA	15mA	15mA	60mA	60mA	
10 Surges 4,000 A pk													
N12 10+	0.2	0.2	0.5	(Frozen but not tested)									
N13 12	0.2	0.2	0.4	1.1	100	1.2							
N16													
N17													

TABLE 7c

GROUP	C									
SUBGROUP	1					2.Final Measurements				
NO.UNITS TESTED	100%	100%	100%	100%	100%	10%	10%	10%	10%	10%
TEST	Physical Dimens.					Shock,	Vibration,	Constant	Accel.	
MIL-STD-750 METHOD	2066					2016	2056	2006		
TEST CONDITION	Figure 1					4211	4206	4221	4221	4226
SYMBOL	A	B	C	D	E	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	V_{FM}
MAX.	5.00"	3.475"	0.700"	1.857"		20mA	20mA	5Vdc	500mAdc	2.5V
MIN.		3.425"	0.600"		6.00"					
UNIT NO.								For information only - Not a spec. requirement		
N12										
N13										
N16										
N17										

	3.Final Measurements					4.Final Measurements					5
	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	100%
	Reduced Barometric Pressure					Salt Atmosphere, Thermal Fatig.					Thermal Resistance
	1001					1041	para. 4.6.2				3151
	4211	4206	4221	4221	4226	4211	4206	4221	4221	4226	
	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	V_{FM}	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	V_{FM}	θ_{J-c}
	20mA	20mA	5Vdc	500mAdc	2.5V	20mA	20mA	5Vdc	500mAdc	2.5V	0.15°C/Watt
	15 mm Hg 800 V.pk										250 Adc
											Initial
N12	0.2	0.2	0.8	80	1.3						0.13
N13	0.2	0.2	0.8	70	1.2						0.14
N16											0.14
N17											0.11

(b) Sub-Group 2

Shock and Vibration tests on this thyristor configuration were performed for the first time during the MM&T Contract. Nine of the eleven devices passed. The first and third were previously degraded in prior tests and may thus have been weakened for the shock and vibration tests. The Constant Acceleration test (information only) was run for the first time on devices N2 and N9. The latter survived while the former failed, as evidenced by the final measurements of i_{RBOM} and V_{FM}. The facilities of AVCO, Boston, MA, were used for the Constant Acceleration Test.

(c) Sub-Group 3

All eleven devices were successfully tested at the reduced barometric pressure of 15 mm of Hg.$^{\Delta}$ Final measurement parameters verify that there was essentially no change from the initial values listed in TABLE 6a, except for previously degraded blocking characteristics. This test was not included in the previous R&D Contract.

(d) Sub-Group 4

Thermal fatigue was measured on all of the devices. Both N3 and N7 degraded. The other nine passed this 200 cycle test. A sample of four devices was selected randomly for the Salt Atmosphere tests. All four passed and this sample size was considered to be adequate to assure that the remaining samples would pass, too. The facilities of RCA, Camden, NJ were used for the salt test.

(e) Sub-Group 5

The thermal resistance of all eleven devices was measured both before and after the frozen (-25°C) start tests. Ten of the eleven were satisfactory after the frozen start tests.$^{\Delta}$

$^{\Delta}$Remarks refer to the engineering samples test results. They are also generally true for the initial confirmatory sample test results.

A more comprehensive discussion of these test results was included in the Test Report submitted with the Engineering Samples.

c. Selection of Five Samples for Delivery

(1) Group Selection

Five possible groups of five samples each (selected from the total of eleven devices) was shown in TABLE 2 of the Third Quarterly Report. The five engineering samples selected for shipment were from Group V. Other operable samples were retained for additional tests or analyses of failures.

The five shippable samples were selected on the basis of their conformance to the specifications as well as for their timely completions of the lengthy testing sequence. These samples are all operable and are believed to be representative of the range of fabrication variables that may be encountered in subsequent devices. Serial Nos. of the devices shipped on 14 July 1977 were N4, N5, N6, N8 and N11. They fulfill SLIN 0001AA of the contract.

The applicable PERT chart revision had indicated a mid-July shipment of the Engineering Samples. Group V met this schedule.

The five Engineering Sample thyristors submitted for government evaluation were tested in accordance with the instructions of Part II, Section F.47 of the contract; as well as paragraphs 1.2.12, 3.1.7 and 3.5.5 of ECIPPR No. 15. The test results presented in this report are believed to verify the successful transition from the R&D phase to a production design suibable for the use of production methods to reproduce.

(2) Summary of Results

Specifically, the following summary of technical progress is presented as verification.

Code: P - Passed, including any final measurements required.

F - Failed

A - Acceptance judged from the other samples submitted to this test.

Refer to TABLE 8.

TABLE 8

SUMMARY OF ENGINEERING SAMPLES
PERFORMANCE vs. SPECIFICATIONS

Inspection	Device Serial No.				
Acceptance Requirements	N4	N5	N6	N8	N11
Vis. & Mech.	P	P	P	P	P
i_{FBOM} @ 25°C	P	P	P	P	P
I_H @ 25°C	P	P	P	P	P
i_{FBOM} @ 125°C	P*	P	P	P*	P*
V_{FM} @ T_C = 100°C	P	P	P	P	P
Group A, Sub-Groups 1-4					
i_{RBOM} @ 25°C	P	P	P	P	P
V_{GT} @ 25°C	P	P	P	P	P
I_{GT} @ 25°C	P	P	P	P	P
i_{RBOM} @ 125°C	P	P	P	P	P
V_{GT} @ 125°C	P	P	P	P	P
dv/dt @ 125°C	F	F	F	F	F
t_{OFF} @ 25°C	P	P	P	P	P
Group B, Sub-Groups 1-4					
I_{FM} (Surge)	P	P	P	P	P
V_{GT} @ -25°C	P	P	P	P	P
I_{GT} @ -25°C	P	P	P	P	P
V_{FM} @ -25°C	P	P	P	P	P
Thermal Shock	P	P	P	P	P
Moisture Resis.	P	P	P	P	P
Block V. Life Test @ 125°C	P*	P*	P*	A	A
Group C, Sub-Groups 1-5					
Physical Dimen.	P	P	P	P	P
Shock	P	P	P	P	P
Vibration	P	P	P	P	P
Constant Accel.**	A	A	A	A	A
Barom. Press. Reduced	P	P	P	P	P
Salt Atmosphere	P	A	P	P	P
Thermal Fatigue	P	P	P	P	P
θ_{JC}	P	P	P	P	P

*Gate Condition B
**Information only test, not an acceptance requirement per contract para. F3, Item 7.

Actual test data are included in TABLEs 6a, b, c and d of this report. The items sample tested, above, are also designated for sampling in both the confirmatory sample and pilot run phases of the contract. A 20% sample (1 device) and a 10% sample (4 devices) are designated for those phases, respectively.

Note that 98% of the 222 total tests performed on these five devices were passed by the engineering samples submitted. This total does not include the "A" but only the "P" items, above.

The 222 total tests included all of the final measurements of the key electrical characteristics as specified following six groups of major tests. The final measurements determined whether there was any deterioration of the thyristors during these major tests. No deterioration occurred, as shown in the Tables of the Test Report.

In summary, the reverse and forward blocking currents were measured at room temperature and at 800 volts peak. They all remained essentially unchanged. The same was true of the 125°C measurements of the reverse and forward blocking currents which were also required after the Blocking Voltage Life Test. All current values were within the specifications.

The gate trigger characteristics as well as the on-state voltages remained essentially unchanged throughout the testing sequence. Also, the reverse gate current is required as one of the final measurements after the surge current test. It, too, was well within the specification limit on all five devices.

d. Corrective Action

Corrective actions taken previously were successful in improving the high temperature, forward blocking current and the gate current values on the later engineering sample devices. The change in passivating coating was successful in preventing voltage degradations. Additional improvements or specification modifications will be necessary before the confirmatory sample phase to resolve the dv/dt deficiency. Yields must be further improved prior to pilot run, although improvements in heat-pipe sub-assembly yields have already been accomplished. The need for added through-put of various limiting facilities is also being studied and corrected.

6. Specification

One specification change suggested previously is the addition of a thermal resistance test in Table II, Sub-Group 1. This preliminary determination of heat-pipe efficiency could then be used to detect any internal damage, or delamination that may be caused by the frozen start ($-25^{o}C$) test of Sub-Group 2. This added test was performed on all of the engineering sample devices and is being performed also on the initial confirmatory sample devices.

The other specification change is related to the dv/dt limits and test conditions, as described in Section 1 of this report. This request will be submitted separately.

A further tightening of the specifications of SCS-477 is not recommended at this time for the following reasons:

a. A larger statistical sample should be produced before deviations are determined and the three sigma limits are established for a normal distribution.

b. The further refinement of Transcalent Thyristor (for improved dv/dt) may affect other electrical parameters, such as, the gate characteristics, the blocking current values, the surge capabilities and/or the on-state voltage values. Revised limits should be based on the final device configuration utilized for the Confirmatory and Pilot Run samples.

c. Present limits are generally consistent with the ratings of competitive, conventional devices. In some cases the Transcalent Thyristor test limits are more stringent.

7. Requirement for Pilot Run

Not applicable until later in the contract.

8. Total Cost for Pilot Run

Data not available until the pilot run is completed.

9. Program Review

The PERT chart as revised and submitted to ECOM in mid-May, 1977 was used as the basis for the shipment of the five engineering samples and the test report in mid-July, 1977.

The remaining PERT chart schedule was reviewed to assess the impact of this delay on the subsequent Confirmatory Samples and Pilot Run phases of the contract. A subsequent revision to the PERT chart was prepared and submitted on 29 August 1977, showing a mid-March, 1978 completion date for the Confirmatory Samples. This completion date allows also for the annual vacation shutdown of the Lancaster plant in the last two weeks of July.

This latest revision and the dv/dt limits, above, were reviewed with Mr. W. Peltz and Dr. R. Eaton, III during the 27 September 1977 coordination meeting at the contractor's facility in Lancaster, PA.

CONCLUSIONS

The engineering program was successfully completed in the first ten months of the contract with the delivery of five samples and the corresponding test report. All were accepted by the Government PCO. The additional time required to achieve Lancaster-diffused wafers equivalent to Somerville's original quality delayed the delivery schedule. Subsequent devices will be delayed accordingly, as listed in the revised PERT chart, submitted separately 29 August 1977.

Effort expended in the fourth quarter was successful in correcting the wafer difficulties so that the program can proceed without further delays. Early authorization of the Confirmatory Sample phase will help to avoid any further delays. Verification that the SCR design meets all but one specification requirement adds assurance that the Confirmatory Sample phase should also be successful. Corrective action as well as a proposed specification modification should alleviate the limitation on subsequent devices. RCA is thus confident of meeting the full MM&TE specification requirements for the confirmatory sample and pilot run devices.

Fabrication of the Confirmatory Samples has begun under the authorization dated 15 August 1977. Preparations for production will be evaluated during this phase to reveal any limitations that need to be corrected prior to the pilot run.

PROGRAM FOR THE NEXT QUARTER

1. Prepare and submit the Confirmatory Sample Test Plan following approval of the proposed modification to the dv/dt specification,

2. Complete calibrations of the electrical and thermal test facilities,

3. Since the Government acceptance of the Engineering Samples, commence fabrication and evaluation of the Confirmatory Sample devices,

4. Submit a written request for modification of the dv/dt specification with complete justification for the request, and

5. Continue to resolve any facility limitations in preparation for the Pilot Run phase.

IDENTIFICATION OF PERSONNEL

The professional and skilled technical personnel who actually worked on the MM&TE project during the first three quarters have varied backgrounds, as listed in the biographical resumes included in the First, Second and Third Quarterly Reports. One additional resume is included in this report for an additional member of the technical staff assigned to the project in the Fourth Quarter.

In addition, numerous supporting personnel including managers, secretaries, purchasing agents, marketing specialists, environmental technicians, machinists, electricians, experimental tube builders, etc., have contributed to the progress made in the first twelve months of the contract.

B. B. Adams - Member, Technical Staff

Mr. Adams joined the RCA Electron Tube Division at Lancaster in 1957 as a design and development engineer. He has been instrumental in the mechanical design of rf circuitry, cold probe test gear and special devices utilized in the development of a variety of super power tubes and circuits. He has also provided consultation and engineering support for various government research and development as well as production projects.

As Project Engineer, Mr. Adams was responsible for the mechanical design of the RCA Developmental A-2696 and A-15193 Coaxitrons. Both of these tube types were required to meet stringent environmental conditions and extensive environmental testing. He has also been responsible for the design of a variety of high power cavities.

He was responsible for the mechanical design of the Coaxitron Amplifier interstage and driver input circuits. His assignment included the mechanical and environmental design as well as both the mechanical and electrical testing phases of the project. He holds a patent on the novel cathode suspension system used in the Coaxitron. This system allows the unit to survive the severe shock and vibration criteria stipulated by the contract. In addition, he was responsible for placing the driver and interstage circuits into the factory and for solving the production problems involved.

Mr. Adams received his Bachelor of Science degree in Mechanical Engineering from Pennsylvania State University and has pursued a course of graduate studies in Engineering. He is a licensed professional engineer in the Commonwealth of Pennsylvania, a member of Tau Beta Pi, Pi Tau Sigma and the American Society of Mechanical Engineers.

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