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ECOM-0039-3

MM&T Program for the Establishment of Production Techniques for High Power Bulk Semiconductor Limiters

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By

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ABSTRACT

X-band bulk limiters have been fabricated using high resistivity silicon ρ = 15,000 Ωcm from Wacker Chemical Co. and Hughes Industrial Product Division. Bulk limiters from both the sources exhibited power handling capability of 15-25 kW but a cracking problem was experienced with Hughes' wafers.

Batch process and ball-bonding processes have been introduced to manufacture the bulk limiters at a low cost with good yield. Various parameters are being optimized to achieve both bandwidth and RF power goals of the contract.

PURPOSE

The objective of this program is to establish a production capability to manufacture High Power Bulk Semiconductor Limiters per U.S. Army Electronics Command Technical Requirements SCS-486.

The specification covers X-band high power bulk semiconductor limiter and low power multistage clean up limiter. Four fundamental requirements are detailed in the specifications. They are, (1) recovery time, (2) high power capability, (3) insertion loss, and (4) VSWR.

A total of fifteen (15) engineering sample limiters, twenty (20) confirmatory sample limiters and fifty (50) pilot run production limiters will be supplied. A pilot line capable of producing 100 bulk semiconductor limiters per month will be demonstrated. Reports and documentation as required in Sections E, F, G, and H of DAAB07-76-Q-0040 and as detailed in Section 3.5 of ECIPPR No. 15, dated December 1976, will be provided.

The program divides into the following four phases, Phase I - Engineering Samples (300 days), Phase II - Confirmatory Sample Production (240 days), Phase III - Pilot Line Production (180 days), and Phase IV - Final Documentation (30 days). The total program duration is 750 days.

During Phase I of this program, a number of factors in fabricating bulk semiconductor limiters are being investigated. These include iris formation, circuit configuration, material characterization and chip mounting. Efforts during Phase I will be directed toward selecting a single limiter design capable of meeting the objectives of SCS-486.

The optimum device design will be chosen at the end of Phase I. In Phases II, III, and IV a single device design will be produced.

The major effort of this program will be realization of a single bulk limiter design which meets all the objectives of SCS-486. Individually, any of the goals described can be currently obtained. Recognizably, it is the development of a single component design which achieves all of the desired performance parameters that is the formidable engineering and manufacturing endeavor.

I. OBJECTIVE

The objective of the current Manufacturing Methods and Technology Engineering program is to establish the producibility of the X-band bulk semiconductor limiter and the X-band bulk semiconductor lower power diode multistage limiter by mass production techniques. Achieving the performance goals of the program represents a formidable engineering task. These goals, from SCS-486 are summarized below.

A. Function Description

The high power, solid state, limiter described herein will operate in the frequency band 9.0 - 9.65 GHz. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed tuned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a common semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

B. Mechanical Characteristics

The bulk semiconductor limiter structure will have the following performance objectives:

Weight:	7.0 oz max
Input Flange:	mates with UG-40B/U choke flange
Output Flange:	mates with UG-135/U cover flange
Mounting Position:	any
Cooling:	conduction

C. Electrical Characteristics

The bulk semiconductor limiter will have the following objectives:

Peak RF input power:	30 kW, Du = .001
1 μsec pulses continuous:	10 kW, Du = .01
Insertion loss:	0.7 dB (max)
Low level VSWR:	1.4:1 (max)
Recovery time:	0.8 μsec (max)
Flat leakage:	50 mW (max), for 30 kW, .001 duty cycle, 1 μsec pulse
Spike leakage:	750 mW (max), for 30 kW, .001 duty cycle, 1 μsec pulse
External bias:	none

D. Absolute Rating Objectives

PARAMETER	SYMBOL	MIN	MAX	UNIT
Frequency	F	9.0	9.65	GHz
Peak Power	P		30	kW
Average Power	P_a		100	W
Ambient Temp	T_A	-55	+85	^oC
Altitude	--		50,000	ft

II. INTRODUCTION

This report covers the period from 23 December 1976 through 22 March 1977. During the period, high power semiconductor limiter work was concentrated in the areas of semiconductor wafer fabrication, broadband matching circuitry and increasing the bandwidth of the high power bulk limiter stage.

Significant improvements in the semiconductor fabrication procedures have been accomplished during the quarter. Batch fabrication scheme was introduced to improve the manufacturability of bulk limiters. The delicate diffusion bonding of the bulk limiter chip to 10 mil gold wire was replaced by ball bonding the gold wire to 3 mil etched gold posts defining the active element area. Difficulties had been encountered in depositing reproducible evaporated chrome gold films. Earlier attempts of depositing chrome-gold and titanium-gold by diode sputtering methods were unsuccessful due to radiation damage. Recent experiments of depositing titanium (10%) tungsten (90%) and gold by MRC-903 low energy Magnetron Sputtering System gave encouraging results. TiW-Au being a high temperature metallization will further improve the power handling capability of bulk limiters.

An attempt was made to operate the bulk limiter under DC bias condition. The purpose of testing bulk limiter with DC bias applied was to see if the isolation and hence the power handling capability could be increased. The theoretical and experimental results are discussed in detail in Section III. The results indicated that DC bias could not be used to increase the power handling capability of the bulk limiter.

From the circuit tests of the three-stage limiter package, it was determined that the input bulk stage would require a 3 dB bandwidth of over 1.32 GHz and a power handling capability of 30 kilowatts in order to achieve the program goals. It was found, that this cannot be achieved with a single 3 mil thick bulk limiter element. Consequently, bulk limiters were made using two elements, one in each slot of double two slot limiter irises. These limiters showed good limiting performance and more than adequate bandwidth. However, a problem was encountered in that burnout could not be predicted from recovery time measurements as was possible with single slot limiters. The other problems with this scheme are matching bulk limiters with similar DC and RF characteristics, assembly, reproducibility, and cost. Presently, we are trying to achieve these goals in a single chip configuration by using thicker high resistivity wafers.

The subsequent sections of this report describe in greater detail the work performed and results achieved to date.

III. BULK CHECKERBOARD LIMITER DC AND BIASED MICROWAVE CHARACTERISTICS

A. DC Biased Operation of Checkerboard Contents

1. Introduction

The spacial arrangement of p and n doped regions in a checkerboard contact has been seen to impart unique characteristics to devices made with checkerboard contacts. In some situations such as under RF drive, the qualitative effect of the checkerboard contact is quite predictable, as to how it will affect performance of a specific device structure. In other situations, the reasons for a particular observed phenomenon are difficult to explain even though the phenomenon is subject to a more straightforward evaluation in devices with simple diffused contacts. Such is the case with the current voltage characteristics of a silicon chip with checkerboard contacts on either surface of the chip. It is the purpose of this description to present the results known to occur with such a device as well as a model describing qualitatively a set of physical conditions present within the device during DC biased conduction.

2. Review

A checkerboard contact is, by definition, a periodic array of p and n doped regions on the surface of a semiconductor (silicon) which are inherently shorted together either internally or by metallization. As shown in Figure 1, a checkerboard intrinsic checkerboard device, (CIC), is fabricated like a PIN diode except that it has checkerboard contacts on both device surfaces.

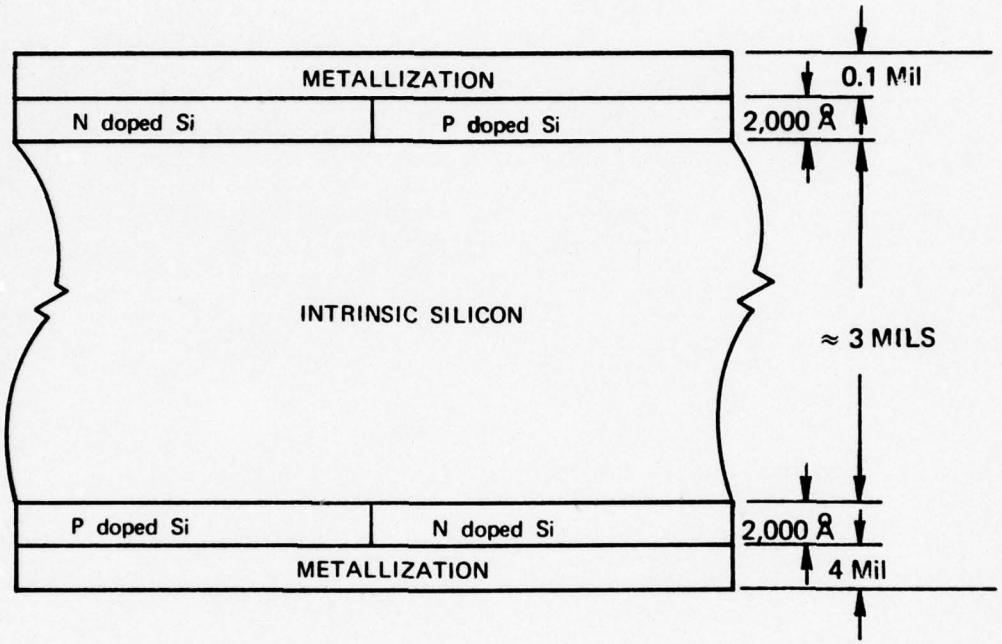

FIGURE 1 SECTION OF A CHECKERBOARD LIMITER ELEMENT

Characteristics noted in the CIC devices include:

a) Rapid carrier recombination of non-equilibrium carriers at the contact surfaces of the device. This is demonstrated by rapid recovery of CIC microwave limiters to transmission state conductivity.

b) Injection of holes and electrons (neutral plasma) from checkerboard contacts biased only by microwave frequencies. This is observed in low power limiter turn-on.

c) Uniform microwave induced plasma distribution in CIC limiters. Non-filamentary breakdown is demonstrated by power capabilities observed.

d) Current voltage characteristics showing apparent space charge limited current flow and double injection current flow modes.

The characteristics noted in Figure 1 were observed in CIC structures with 3 mils thick intrinsic regions and a doping pattern consisting of a 1 mil square unit cell p doped except for a 1/2 mil square n doped region. Due to the method of fabrication used, the p doped regions were depressed into the silicon surface relative to the n doped regions. Similar characteristics have been noted on occasion using a "true" checkerboard doping pattern (equal areas of p and n doped regions). Currently, bulk limiter elements using true checkerboard patterns are being used.

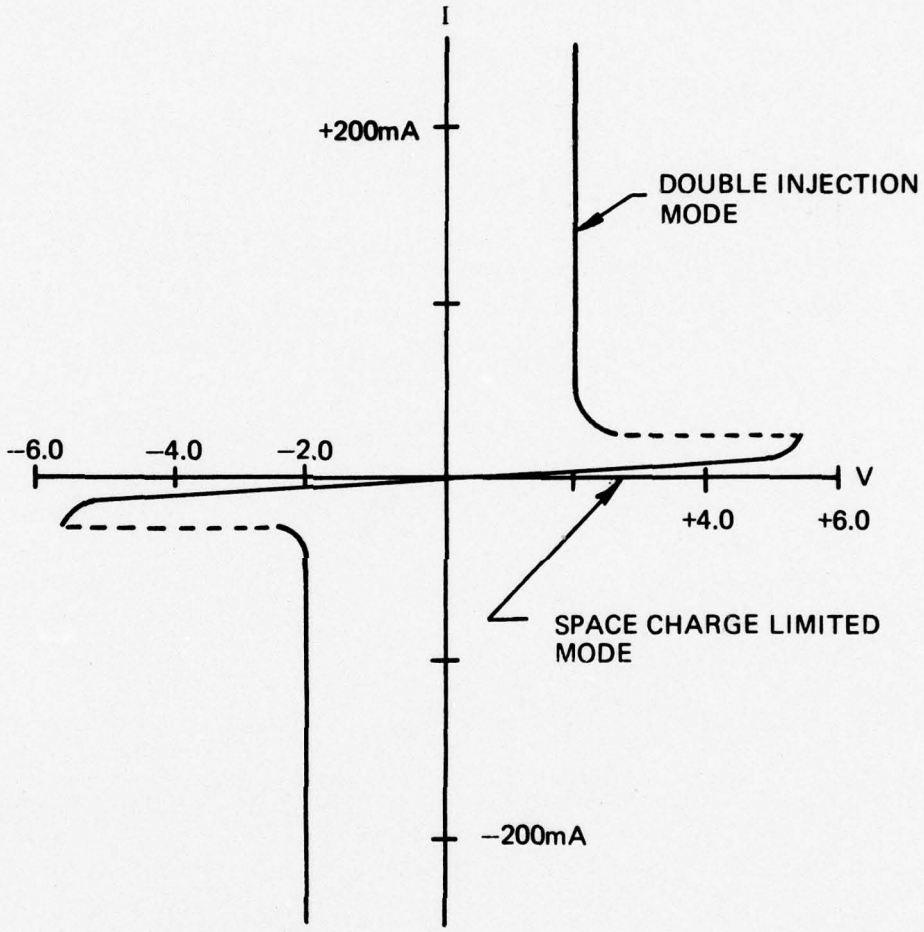

FIGURE 2 EXPERIMENTAL CIC DEVICE I VERSUS V CHARACTERISTICS

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3. Analysis - Zero Biased Conditions

Without applied current or voltage, the device is straight forward to analyze. First, as the device is in thermodynamic equilibrium, there is no net flow of carriers of either type anywhere within the device. The Fermi level in all portions of the device (metal, p doped, n doped, and intrinsic silicon) is the same. There is no net carrier generation or recombination anywhere in the device. Thus, if Ψ is the electric potential relative to the intrinisc Fermi level,

$$n(x,y,z) = n_c e^{\frac{-q(E_c - \Psi)}{kT}} \tag{1}$$

$$p(x,y,z) = n_v e^{\frac{-q(\Psi + E_v)}{kT}} \tag{2}$$

everywhere within the semiconductor and

$$np = n_c n_v e^{\frac{-q}{kT}(E_c + E_v)} = n_i^2 \tag{3}$$

from Maxwell Equations

$$\nabla \cdot E = +\frac{\rho}{\epsilon_r \epsilon_o} \tag{4}$$

where ρ is the net space charge (mobile holes and electrons and immobile dopant ions) and $\epsilon_r \epsilon_o$ is the dielectric constant of silicon. As the electric field can be expressed as the negative gradient of the voltage,

$$E = \nabla\Psi \tag{5}$$

The equations describing zero bias operations (equilibrium) reduce to:

$$-\nabla^2\psi = \frac{p-n + N_D^+ - N_A^-}{\epsilon_r\epsilon_o} \tag{6}$$

$$= \frac{n_v e^{\frac{-qEv}{kT}}}{\epsilon_r\epsilon_o} e^{\frac{-q\psi}{kT}} - \frac{n_c e^{\frac{-qEc}{kT}}}{\epsilon_r\epsilon_o} e^{\frac{-q\psi}{kT}} + \frac{N_D^- - N_A^+}{\epsilon_r\epsilon_o} \tag{7}$$

or

$$\nabla^2\psi = +\frac{2n_i}{\epsilon_r\epsilon_o}\left(\sinh\frac{q\psi}{kT}\right) + \frac{N_A^- - N_D^+}{\epsilon_r\epsilon_o} \tag{8}$$

The solution to the differential Equation (8) is not straightforward and cannot be obtained in closed form. Thus, to obtain a solution, even in one dimension, numerical methods must be employed. Note that solutions to abrupt, linearly, and exponentially graded junctions are obtained by neglecting the hyperbolic sine term of Equation (8), and therefore, can easily be solved in closed form. However, in the intrinsic silicon case PIN, CIC, etc., the sinh term is dominant and closed form solutions do not exist.

Without knowing the numerical solution for cariers density versus distance into the intrinsic region, several conclusions about an abruptly doped CIC device can be made. They are:

a) The electric potential in the p doped regions is about 0.5 volts below that deep in the intrinsic region.

b) The electric potential in the n doped regions is about 0.5 volts above that deep in the intrinsic region.

c) The space charge which causes the potential difference is:

   1) negative fixed ions and mobile holes at the p-i interface, respectively;
   2) positive fixed ions and mobile electrons at the n-i interface, respectively;
   3) negative and positive fixed ions at the p-n checkerboard boundaries, respectively.

d) Accumulation layers extended into the CIC or PIN device much further than a typical depletion width of p-n junction.

e) At the shorted surface junction (p-n) of a checkerboard contact a thin high field depletion region exists much like a tunnel junction.

Thus, the equilibrium potential (relative to the intrinsic Fermi level) is as shown in Figure 2, along each of the section lines shown. Figure 3 shows an approximation of space charge density along lines A,B, and C of Figure 2. The sketches are logarithmic and show schematically the space charge distribution under equilibrium conditions.

4. The CIC Structure Under Applied Bias Condition

Figure 1 shows observed current voltage relationships on a 40 X 40 mil chip of 3 mil thickness. The only place on the curve where thermal equilibrium exists is at the origin. Note that the characteristic is single-valued as a function of current and multi-valued as a

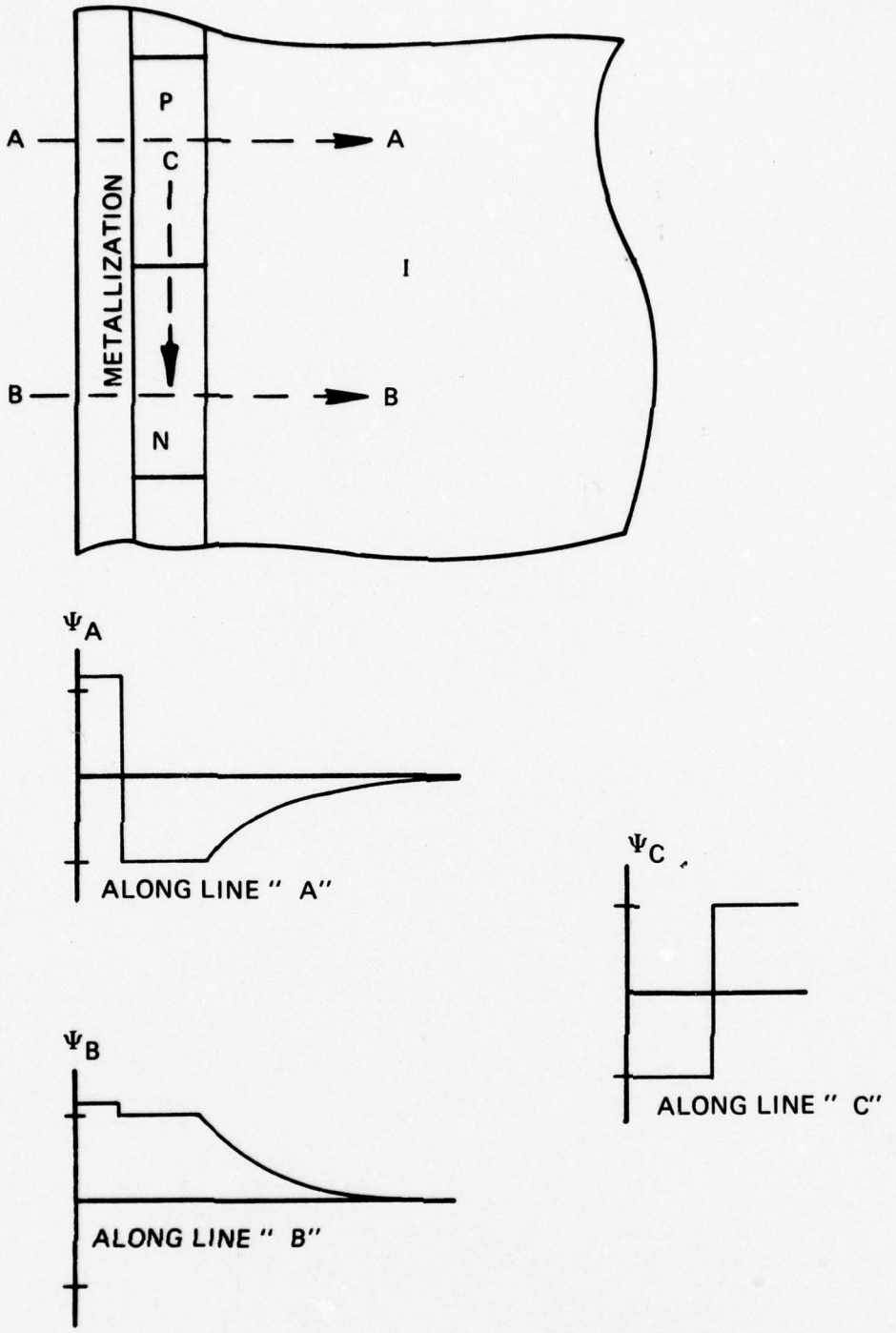

FIGURE 3 EQUILIBRIUM POTENTIAL DISTRIBUTION IN CIC DEVICE

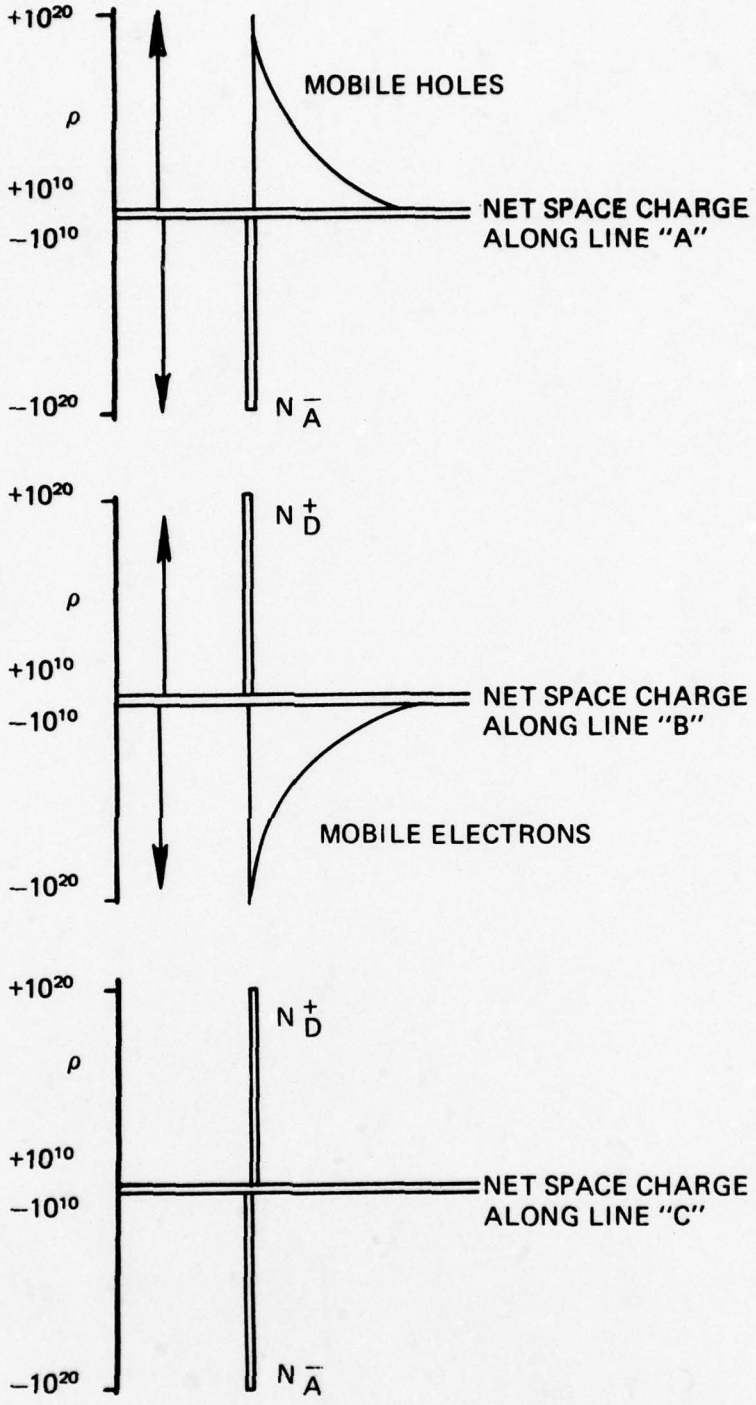

FIGURE 4 EQUILIBRIUM SPACE CHARGE DISTRIBUTION IN CIC DEVICE OF FIGURE 2

function of voltage. At low currents of either polarity, the characteristic is labeled space charge limited current flow. This mode of conduction is a high impedance mode where the voltage drop is across the intrinsic region of the device. Both holes and electrons contribute to current flow, but the density of holes at the negative contact and the density of electrons at the positively biased contact are both very small due to the recombination of carriers caused by the shorted checkerboard junctions. Hence, the neutralizing effect on space charge due to holes and electrons is small and current flow is space charge limited. The distribution of space charge in the low current mode is a small perturbation on the equilibrium charge distribution level. The positively biased contact has slightly more positive charge (near p doped regions) or slightly less negative charge (near n doped regions) than at equilibrium. The reverse situation holds at the negatively biased contact.

Substantial neutralization of the negative space charge of mobile electrons by the positive space charge of mobile holes does not occur until breakdown at the maximum voltage point shown in Figure 1. At currents larger in magnitude than the maximum voltage current, the CIC device "breaks down" into an essentially constant voltage plasma conduction mode. Experimentally the voltage is found to equal two volts in this mode. The breakdown between space charge modes and plasma conduction modes occurs because the rate of hole injection at the positive contact exceeds the rate of hole recombination at the negative contact in the space charge mode provided that the current level is sufficient. The same situation must also be valid for electrons at the negatively biased contact. Hence a buildup of carriers, both holes and electrons, occurs in the middle of the device with a drastic redistribution of net space charge occurring within the device until a steady state distribution of carriers will occur when the hole current injected at the positive contact just equals

the hole current at the negative contact plus the recombination current within the intrinsic region. In this condition, it is also true that the electron current entering at the negative contact equals the electron current at the positive contact plus the recombination current in the intrinsic region.

Figure 4 shows a sketch of the electric potential, electric field and net space charge in a CIC device biased into the plasma mode. The contact at the left is biased at a positive 2.0 volt level with respect to the contact at the right. The intrinsic Fermi level has been chosen as the zero voltage reference level. The potential function shows that both holes from positive p contact and electrons from the negative n contact must be injected over a potential barrier in order to enter the intrinsic region. All holes or electrons which surmount the barrier energy are drifted by the electric field into the intrinsic region. The diffusion current of the injected carrier toward its injecting contact is nil; this is true for both types of doping on the contact surface.

Figure 5 shows the potential distribution, electric field, and space charge along line E of Figure 4. Line E goes through both doped regions that are "reverse" biased by the applied electric field. These regions contain a space charge limited drift current of their respective carrier type and are responsible for the majority of carrier recombination (removal) from the intrinsic region of the CIC structure.

It is extremely important to note that the forward biased regions operate by injection of their carrier type over a potential barrier and that the number density at the top of the barrier is very small. Also the height of the barrier is reduced by the accumulation of opposite type mobile charges at the barrier peak. It is a very important consequence of this operating mechanism that immobile positive ions in front of p type metallurgical junction or immobile negative ions in front of the n type

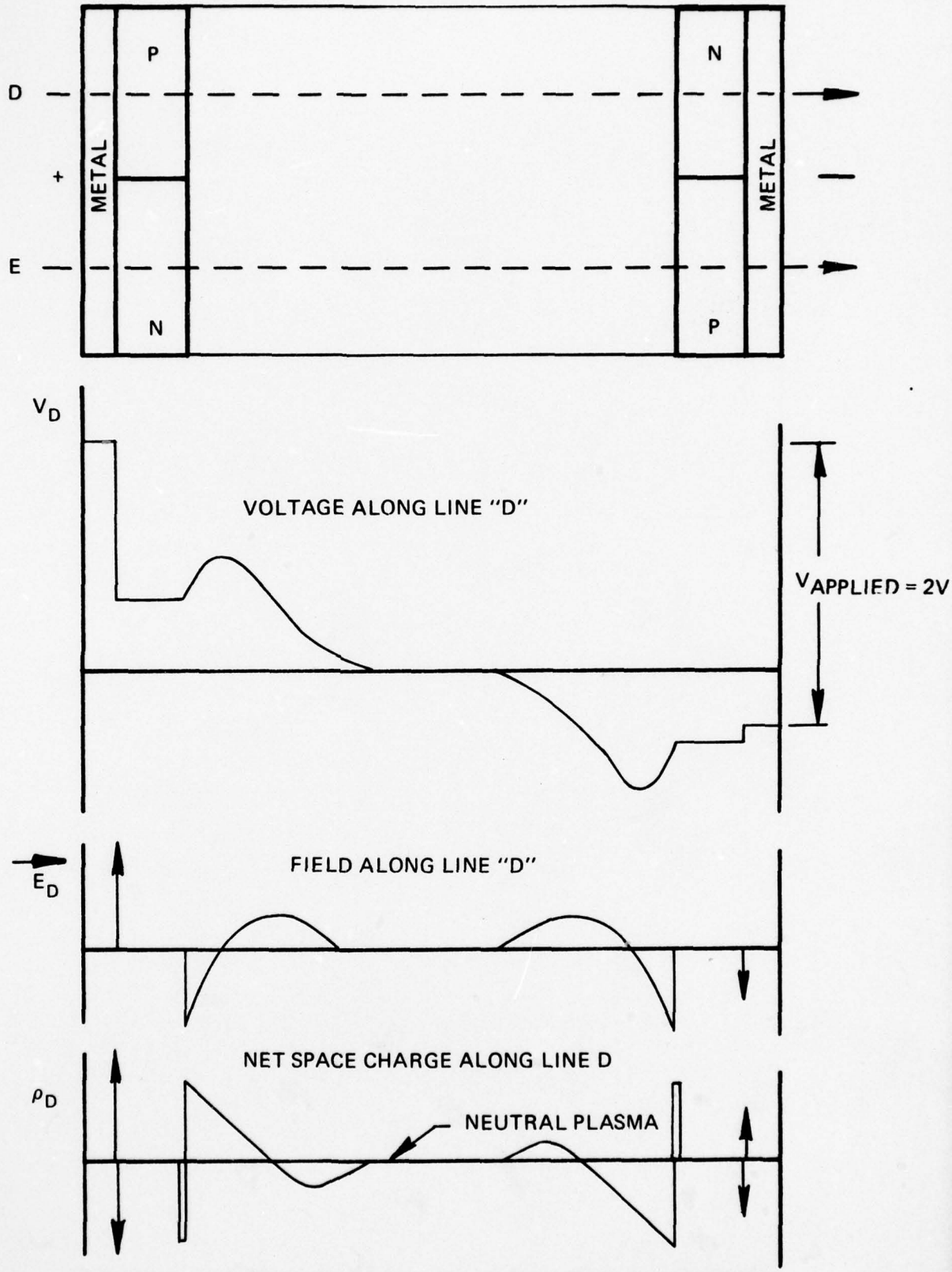

FIGURE 5 VOLTAGE FIELD AND SPACE CHARGE IN PLASMA MODE BIASED CIC DEVICE -- INJECTING CONTACTS

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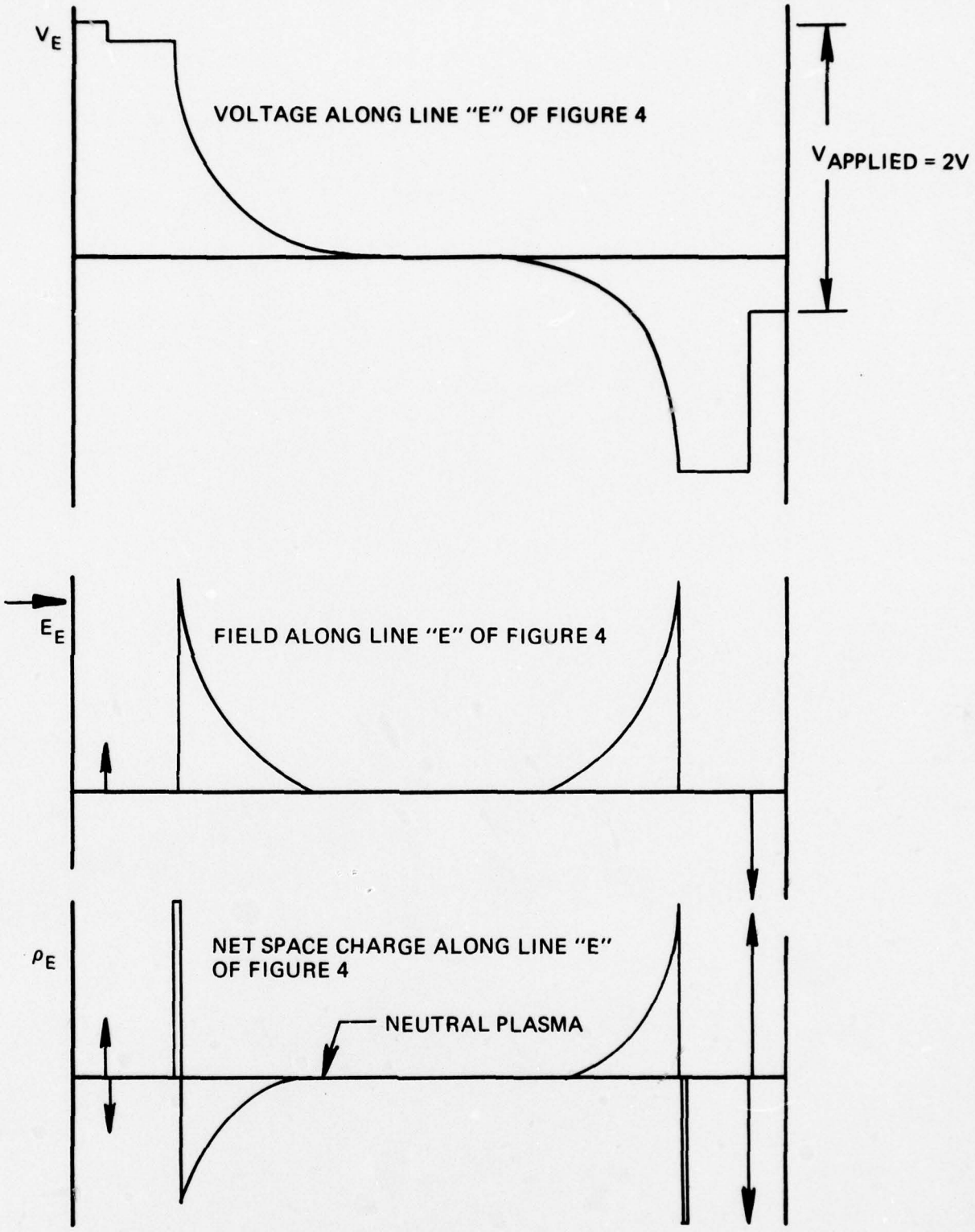

FIGURE 6 VOLTAGE FIELD AND SPACE CHARGE IN PLASMA MODE BIASED CIC DEVICE -- REVERSED BIASED CONTACTS

metallurgical junction will prevent injection of the respective mobile charge. Since it is required that both holes and electrons be injected (over the barrier) into the intrinsic region for plasma mode conduction to occur, plasma breakdown cannot occur if low level n type doping exists below the p regions or visa versa.

The model presented above is a qualitative one which can be used to explain and predict observed phenomena in CIC structures. Some predictions of behavior for CIC devices follows:

a) For CIC structures in long lifetime silicon the current density at which breakdown from space charge to plasma modes occurs should be independent of device thickness (to first order with the same pattern).

b) The maximum voltage before breakdown occurs will increase with thickness if all else remains the same.

c) The plasma mode voltage will not vary significantly with device thickness.

d) As the square size of the checkerboard pattern is changed, it is expected that the current density at the mode transition point will vary in an inverse fashion with square size.

e) Under DC bias conditions in the plasma mode, the bulk plasma density at a given current density will vary in an inverse fashion with square size.

f) If the creation of a DC plasma state is prevented by immobile ions beneath the doped contact (N_A^- below n type or N_D^+ below p type), then microwave plasma injection cannot occur and the recombination process of an avalanche created plasma is inhibited.

B. Biased Checkerboard Limiter Microwave Tests

1. Purpose and Method

The purpose of testing checkerboard limiters with DC bias applied was to see if the isolation and hence power handling capability could be increased by means of added DC bias. The measurements could not be made in the bulk limiter iris circuit because of the requirements for a DC bias connection. Consequently, limiter elements were mounted in pill packages which were then tested in both a network analyzer at the end of a coaxial transmission line and in a waveguide diode limiter mount.

The data was taken using limiter elements from batch BL-7A which had 3/4 mil checkerboard contacts as well as with RRC chips which had 1/2 mil squares on 1 mil centers for a 3 to 1 ratio of phosphorus to boron doped areas.

2. Low Level Network Analyzer Test

Tests of ODS-30 mounted limiter elements were made at low level in a 50 ohm network analyzer circuit. Bias currents were applied to the limiters and return loss was measured at 9.3 GHz. From

return loss measurements, the microwave resistance of the bulk limiter was calculated from the relationships:

$$R_L = -20 \log \left| S_{11} \right|$$

$$R = Zo \frac{1 + S_{11}}{1 - S_{11}}$$

The data is summarized in Table I. All limiter elements were 3 mils thick and had 8 mil diameter diffusion bonded contacts.

The data shows that quite low RF resistance levels can be obtained in the DC biased checkerboard limiter. With the RF resistance calibrated as a function of bias current, the limiter element can be used to calibrate the characteristic impedance of any diode mount at the diode plane.

3. High Power Test Results

The ODS-30 mounted bulk limiter elements were mounted in a single stage diode limiter mount and tuned for transmission and isolation resonance at 9.3 GHz. Low level isolation was measured with applied DC bias to evaluate the impedance of the diode mount. The calculated value was approximately 95 ohms.

High power testing was performed at 500 watts to 1 kW. Unbiased limiters showed very low attenuation values due to the low impedance of the mount. An unexpected result was obtained with biased limiters. At the beginning of the high power pulse, the isolation level was, within measurement error, the same as measured at low power. As the pulse continued, the isolation decreased such that after one microsecond,

	BIAS (mA)	Return Loss (dB)	R (ohms)
BL-7A-2-3	+9.5	14.2	≈50*
	25	8.2	22.0
	50	4.8	13.0
	100	2.3	6.6
	-20	18.9	≈50*
	-25	16.5	38.0
	-50	7.9	21.0
	-100	3.2	9.0
BL-7A-2-2	7	16.8	≈50*
	25	8.1	22.0
	50	4.7	12.8
	100	2.4	6.6
	-25	18.6	64.0
	-32	27.2	≈50*
	-50	13.6	36.0
	-100	5.1	13.8

*Optimum Match

TABLE I

MICROWAVE RESISTANCE FROM NETWORK ANALYZER MEASUREMENTS

the difference between biased and unbiased isolation was typically less than one decibel. Table II shows measured transmitted powers for limiter BL-7A-2-3 at the beginning and end of a high power pulse, with and without DC bias current.

From the high power microwave test results, it appears clear that the microwave fields within the device are somehow lowering the conductivity induced by the DC bias. This result was further verified by replacing the solid state current source with a 30 volt voltage source and a 300 ohm resistor. The voltage was then measured as a function of time into the 57 dBm microwave pulse. The result is shown in Figure 6.

The high power measurement of DC bias voltage substantiates the conclusions drawn from the isolation data. The microwave pulse causes recombination, presumably at the checkerboard doped contacts, of the plasma created by the DC bias current. The plasma is apparently attracted to the contacts by a gradient in the microwave electric field within the device and is recombined by the contact structure.

Thus, DC bias application to a checkerboard limiter element is not an effective means to improve power handling capability.

PIN (dBm)	Pulsewidth	I_{Bias}	P_o (t = 0)	P_o (t = τ)
57 dBm	1.0 μs	+95 mA	43 dBm	52-53 dBm
57 dBm	1.0 μs	0 mA	55 dBm	53.3 dBm
57 dBm	0.5 μs	+100 mA	45 dBm	51.5 dBm
57 dBm	0.5 μs	0 mA	55 dBm	53.0 dBm

Test Conditions: f = 9.3 GHz
Pulsewidth = 0.5 or 1.0 μs
Duty Cycle = 0.001

TABLE II

HIGH POWER BIASED LIMITER TEST RESULTS -- BL-7A-2-3

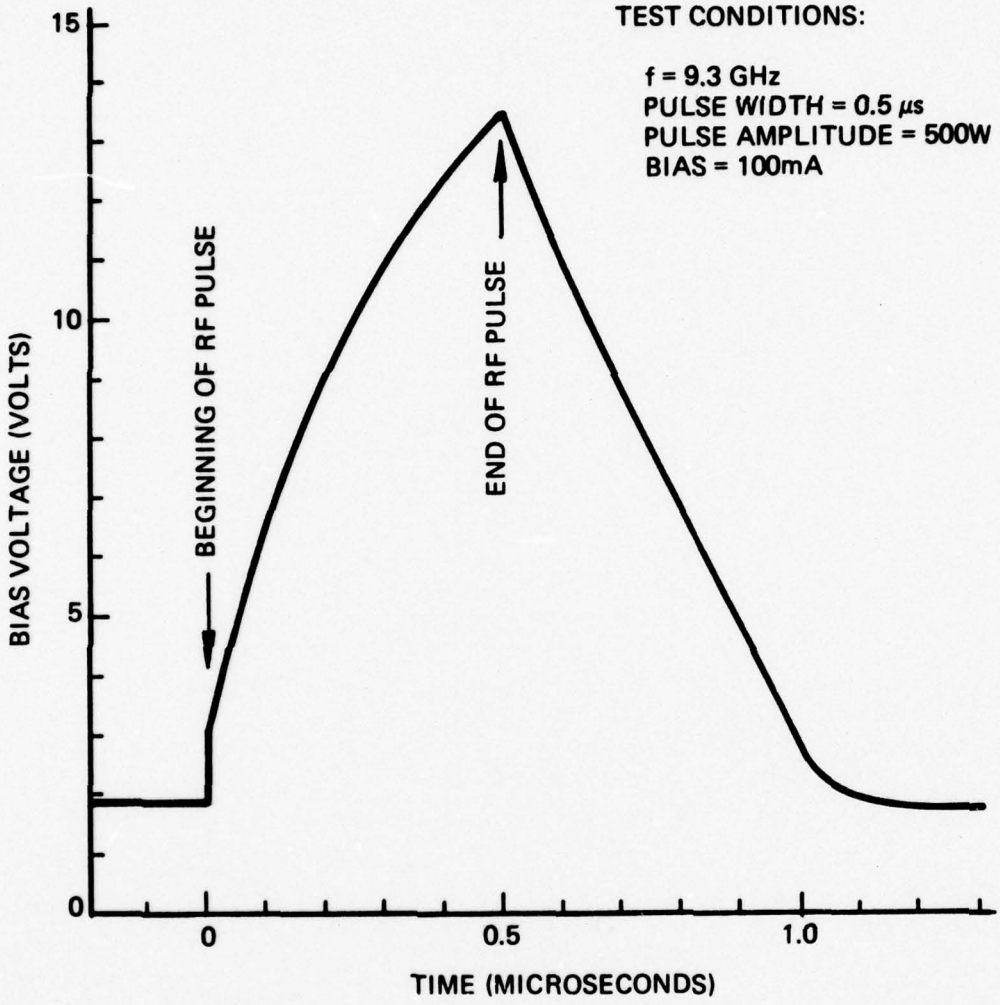

FIGURE 7 BIAS VOLTAGE DURING RF PULSE BL7A-2-3

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IV. FABRICATION AND RF TEST RESULTS

A. Fabrication of Bulk Limiters

1. Wafer Processing

During the last quarter, twenty (20) high resistivity wafers (ρ = 15,000 Ωcm $\langle 111 \rangle$, p type) were processed for bulk limiters. Sixteen (16) wafers were etched and polished to 3.0 mil thickness and the other four (4) wafers to 5.5 mil in thickness. The phosphorous and boron diffusions were done on both sides of the wafers at 1000°C and 950°C, respectively. The 3/4 mil square checkerboard pattern was used prior to the boron diffusion. Boron nitride source was used as the dopant source during the boron diffusion.

Both surfaces of a wafer were then metallized with 500 - 1000 Å layer of chromium and 2000 - 3000 Å layer of gold and then electroplated with pure gold. One surface was plated to a thickness of 0.1 mil while the other was plated to a thickness of 4.0 mils. Then the wafer was cut into 40 mil squares and were separated into individual chips. Bulk limiter chips were diffusion bonded (RRC method) with 8 mil gold wire and then were mesa etched in silicon etch and passivated with silicon nitride and Dow Corning DC-643 junction coating.

2. Metallization Experiments

Difficulties have been encountered in depositing reproducible evaporated chrome-gold films on bulk limiter wafers. The adherence and quality of films varies from run to run. Overnight pump down, increasing bake time to 2 hours at 400°C and evaporating chromium at 80°C showed significant improvements. Titanium-gold and chromium-gold sputtered films were also investigated by using the MRC-90 diode sputtering system. Because of radiation damage in the diode sputtering system, the results were not encouraging. Presently, we are looking into low energy sputtering

systems and electron beam evaporation schemes high temperature metallization such at titanium-platinum-gold and titanium-tungsten-gold are also under investigation. Preliminary results look promising with TiW-Au metallization.

3. Batch Process

A batch fabrication process was introduced to improve the manufacturability of bulk limiters. This scheme eliminates the delicate and time consuming diffusion bonding (RRC method). After chrome-gold metallization, both sides of the wafer were electroplated with 3 mils of gold. The active elements area was defined by etching 10 mils in diameter gold posts on the top side of the wafer. The posts were etched using conventional photolithographic techniques and had a height of 3 mils. The silicon mesa etching process was performed when the elements were still in wafer form.

A new technique for fabricating the dot side contact was developed for use with the batch fabricated elements. Four techniques were considered for making an electrical contact between the gold dot and the opposite side of the iris slot. They were:

a) bellows contact,
b) ball-bonded gold wire,
c) adjustable post contact,
d) forged iris post contact .

Good results were obtained using ball-bonded gold wire (5 mils in diameter) as a replacement for the diffusion bonded posts. The ball-bonded gold wire is dead soft after it is bonded to the batch process gold posts. Therefore, the stresses applied to the silicon dot are limited by the yield point of the soft gold. Hence, breakage during subsequent handling is greatly reduced. The overhang produced by the ball-bonding process proved acceptable under high power conditions because the

three mils thick plated gold dot raised the ball-bond above the surface of the silicon element. This spacing reduced the electric field in the encapsulant to acceptable levels during high power operation. The bulk limiter elements from BL-12A runs were fabricated by the batch process and were assembled in single slot X-band irises and were tested for RF performance. Test data is given in Table III and shows that these limiters are capable of handling 20 kW to 30 kW RF power.

B. Summary of RF Results

Bulk limiters were fabricated by varying the wafer thickness, different metallizations, and by the batch process. These results are summarized in Table IV.

C. Failure Analysis

High power bulk limiters with checkerbaord contacts and conventional chrome-gold evaporated metallization were examined after failure during high power testing. The limiters examined were all 3 mil thick units made from batch process BL-12A.

The initial fabrication run of BL-12A batch process limiters were ball-bonded and silicon nitride passivated. Six units were built and high power tested; BL-12A-1B through BL-12A-6B. Four of those units failed at power levels between 1.0 kW and 15 kW; two were still operating after testing at over 23 kilowatts pulse power. Three of the failed limiters were examined at RRC to determine the probable cause of failure by disecting the limiter and carefully observing and photographing the limiter at various stages of disection. The process used included:

a) microscopic examination of intact limiter as tested,

b) checking low level characteristic,

BL-12A (Using Ball Bonding Gold Wire)							
Number	Resistance (kΩ)	Capacitance (pF)	Frequency (GHz)	3 dB Bandwidth (GHz)	Insertion Loss (dB)	Recovery Time (μsec)	RF Power (kW)
4B	285	0.115	9.310	0.70	1.1	2.5	>24.0*
5B	180	0.232	9.30	0.60	1.3	2.7	>24.0*
13B	210	0.175	9.45	0.70	1.0	2.4	>20.0*
15B	250	0.220	9.6	0.75	0.7	2.0	>20.0*
*Max RF power available from the system							

TABLE III

DC AND RF CHARACTERISTICS OF BULK LIMITERS

Run Number	Source of Material	Metallization	Insertion Loss dB	Recovery Time τ	Bandwidth GHz	High Power kW	Remarks
BL-9A	ρ = 15,000 Ωcm Wacker	Cr-Au	0.7	2.0	0.7	25	Low yield, 2nd Eng. Samples
BL-9B	ρ = 15,000 Ωcm Wacker	Cr-Au					Metal lifted
BL-9C	ρ = 15,000 Ωcm Hughes	Cr-Au	0.8	2.0	0.8	15	Cracking problem
BL-9D	ρ = 15,000 Ωcm Wacker	Ti-Au Sputtered					Radiation damage and metal lifting
BL-10A	ρ = 15,000 Ωcm Wacker	Cr-Au					Metal lifted
BL-10B	ρ = 15,000 Ωcm Wacker	Cr-Au	0.7	2.0	0.65	20	Low yield
BL-10C	ρ = 15,000 Ωcm Wacker	Ti-Au E·B	0.7-0.9	2.0	0.7	20	Low yield
BL-10D	ρ = 15,000 Ωcm Wacker	Cr-Au					Lost in scribing
BL-11A,B, C,D	ρ = 15,000 Ωcm Wacker	Ti-Au Cr-Au Sputtering Experiments					Metal lifting and radiation damage
BL-12A,B,D	ρ = 15,000 Ωcm Wacker	Cr-Au	1.2-0.8	2.0-3.0	0.6-0.75	25	Batch process and ball-bonding expts
BL-12C	ρ = 15,000 Ωcm Hughes	Cr-Au	0.7-0.9	3.0	0.75	20	Some cracking but better than BL-9C
BL-14A,B, C,D,	ρ = 15,000 Ωcm Wacker	TiW-Au experiments					Used for photoplating and metal experiments Cracking problems

TABLE IV

SUMMARY OF VARIOUS BULK LIMITER RUNS

c) microscopic examination of mounted element with encapsulant removed,

d) microscopic examination of limiter element with element removed from iris, and

e) microscopic examination of limiter elements with gold dot chemically etched off.

The three units which were examined in the failure analysis had the characteristics presented in Table V.

The results showed that except for cracked encapsulant on sample BL-12A-6B, which apparently occurred during initial fabrication, the encapsulant prevented arcing in the high field region around the dot contact. Some arcing may have occurred under the cracked encapsulant, but failure was not a result of arcing, if it indeed did occur.

The point of failure in all cases could be seen only in Step (e) above. The failure point was less than 1 mil in diameter in all cases and could be seen as a polycrystalline lump of material building up above the silicon surface. The low level microwave characteristics indicated that an effective short existed through the device. The failure point in BL-12A-1B was about 1 mil in from the edge of the dot contact while failures in BL-12A-2B and BL-12A-6B were at the rim of the dot contact. Figures 7, 8, and 9 are photomicrographs, approximately 200X, of the three semiconductor limiter elements with the contact gold etched off. The chip removed from the center of BL-12A-6B was introduced during sample preparation. The arrows on the photos point to the failure region of each element.

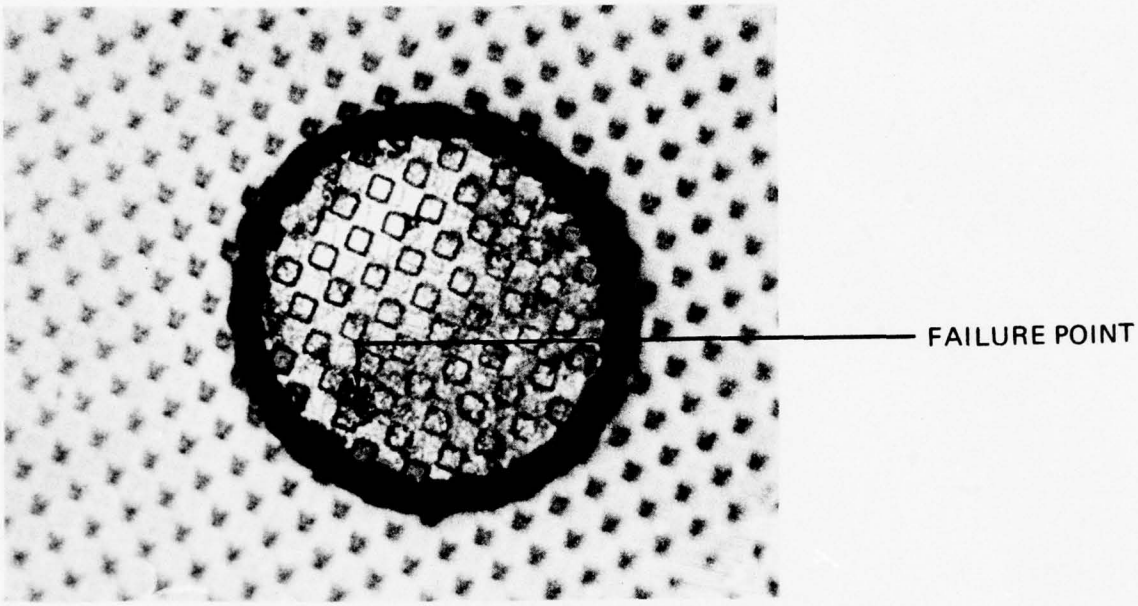
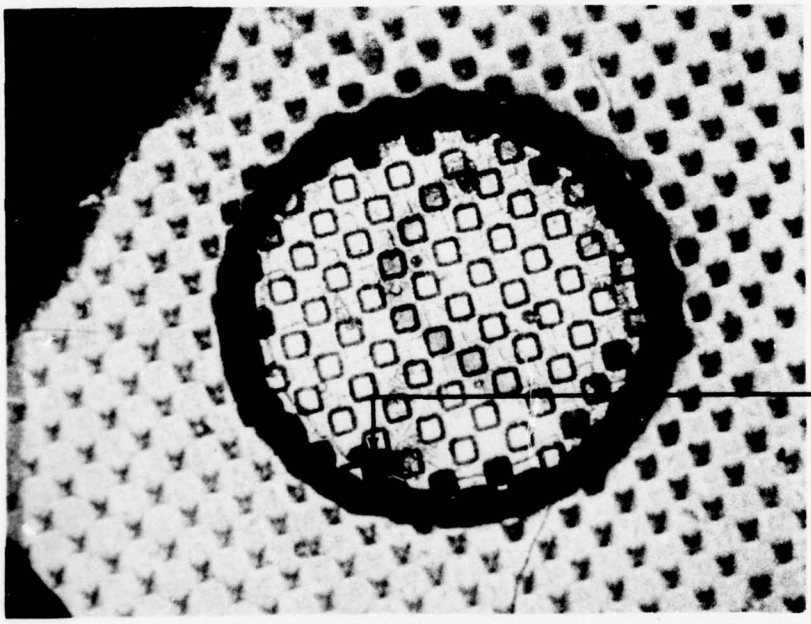


FIGURE 8 PHOTOMICROGRAPH OF BL-12A-1B BULK LIMITER CHIP (DEMOUNTED AND ENCAPSULANT REMOVED)

N-15540

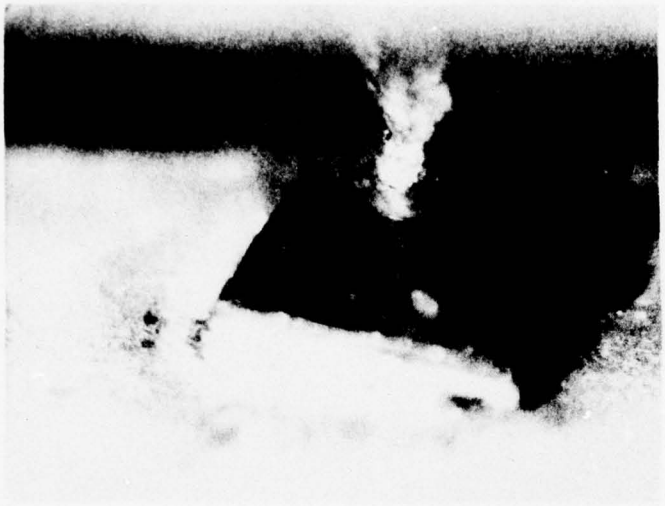
(a) BULK LIMITER CHIP MOUNTED IN X-BAND IRIS



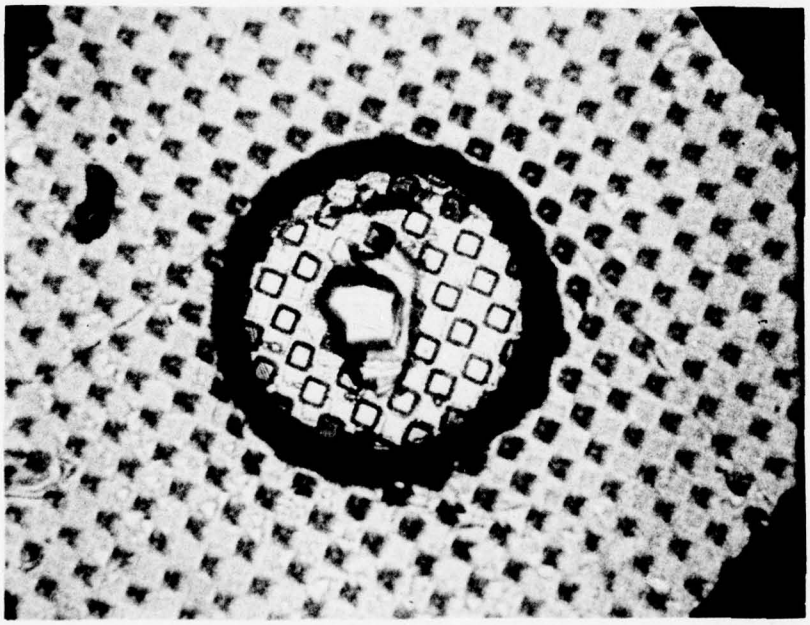
(b) BULK LIMITER CHIP AFTER DEMOUNTING AND REMOVING ENCAPSULANT

FIGURE 9 PHOTOMICROGRAPHS OF BL-12A-2B BULK LIMITER

N-15539



(a) BULK LIMITER MOUNTED IN X-BAND IRIS



(b) BULK LIMITER CHIP AFTER DEMOUNTING AND REMOVING ENCAPSULANT

FIGURE 10 PHOTOMICROGRAPHS OF BL-12A-6B BULK LIMITER

N-15538

A crack in the silicon was noted on sample BL-12A-6B during Step (c) observations. After removal from the iris, a crack was also noted in BL-12A-2B. The crack in the latter sample may have been induced when the sample was removed from the iris and, therefore, may not have been present during high power testing. It was noted that with both cracked samples, the failure point was not located on the crack line. Thus, while the cracks should not be present in good limiter elements, they were not the cause of failure.

All limiters examined in Step (e) showed considerable alloying between the metallization and the silicon chip with irregular patterns of alloying. The alloying undoubtedly occurred during mounting and removal of the element from the iris plate. The alloying that occurred prior to high power test undoubtedly changed the local electrical characteristics of the element and caused premature failure of the device under microwave high power testing. Reasons for the alloying are insufficient thickness and/or uniform coverage of the evaporated chrome layer beneath the gold layer. Alternate metal systems capable of withstanding both higher temperatures and the process requirements of limiter fabrication are under evaluation.

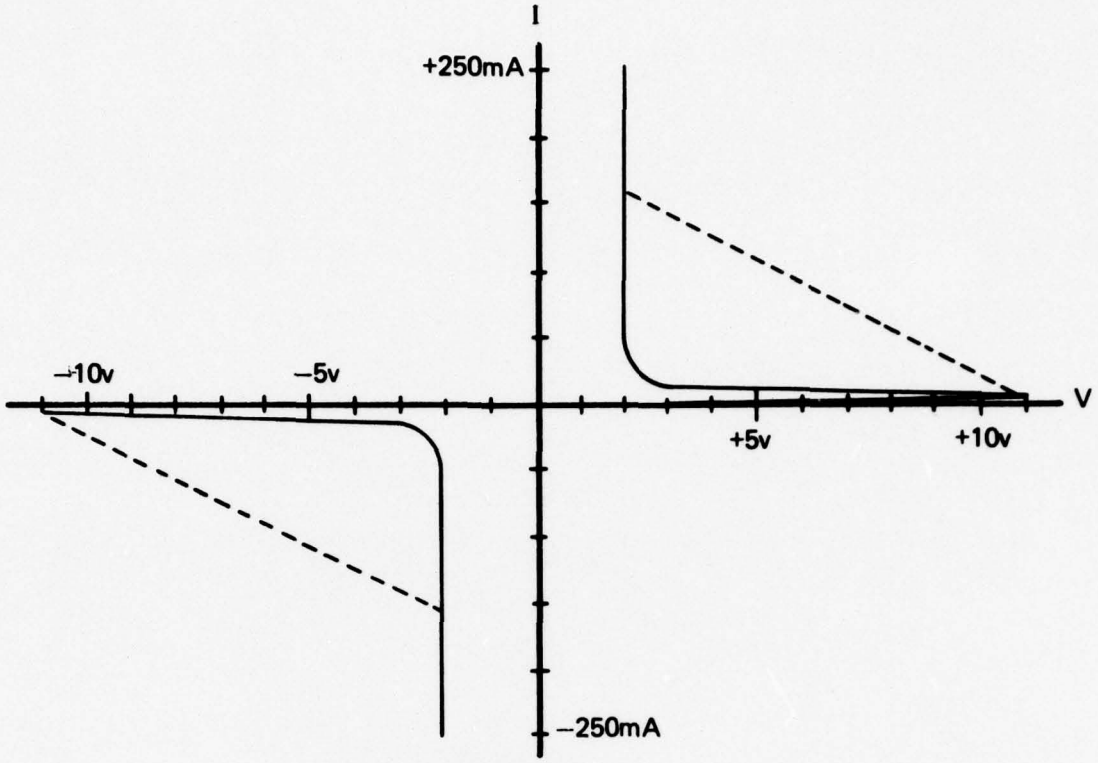
In summary, failure analysis indicated that device failure was undoubtedly caused by metallization system alloying in all three samples examined. It is also possible that large variations in observed recovery times could be related to metallization system failure. Other observations such as checkerboard depth, 3 microns, and mesa depth, 15 to 20 microns, were also made.

D. Metallization Temperature Stress Analysis

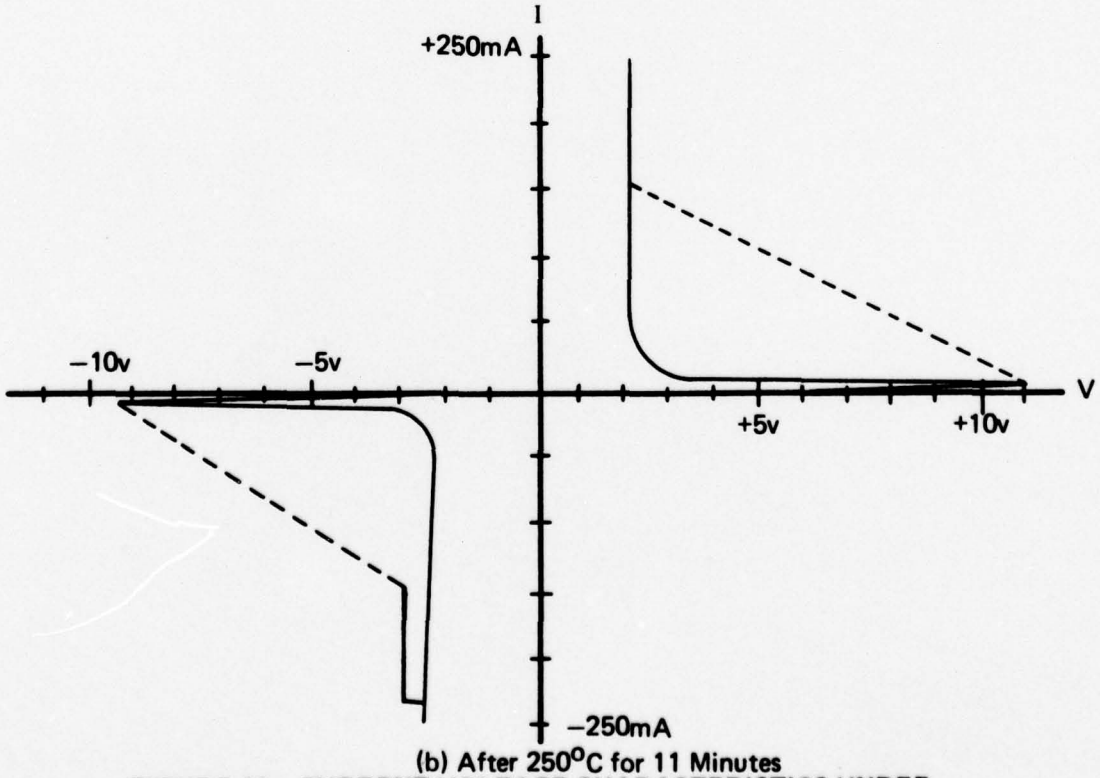
Tests have been performed on bulk limiter chips to determine the effect of temperature stress on the metallization system used. The current-voltage characteristics of the chips were measured both before and after heating in air on a regulated temperature strip heater. It was concluded from the tests that small changes in the current-voltage characteristic occur when annealing is performed below the gold-silicon eutectic temperature. The amount of change in the DC characteristic is quite small. However, the local non-uniformity with a microwave limiter element would be much greater than the averaged values which result from I-V measurements. These local variations caused by metallization failure will cause non-uniform power dissipation and premature device failure.

Chrome-gold (BL-9A) and titanium-gold (BL-10C) metallization systems were tested on 40 by 40 mil checkerboard doped limiter elements. The elements were saw cut and tested as parallel plane devices. There was electroplated gold on both surfaces of each chip. The gold thickness was 0.1 mils on one surface and 3.0 mils on the other. Current-voltage measurements were made using a simple contact probe. Some variation in the measured characteristic was noted with probe pressure. It is believed that this variation was primarily due to better heat sinking at the higher probe pressures.

Typical results obtained for below eutectic heat treatment are shown in Figure 10. The I-V characteristic in Figure 10(b) is prior to any heating. The breakdown voltage is symmetrical at 11.0 and -11.0 volts with 250 mA plasma state voltages of +2.05 and -2.2 volts. In the I-V curves, the thin gold side is regarded as the plus contact. A slight hysteresis in the negative current characteristic was noted after a one minute 250^{o}C heat treatment.



(a) Before Heat Treatment



(b) After 250°C for 11 Minutes

FIGURE 11 CURRENT VOLTAGE CHARACTERISTICS UNDER TEMPERATURE STRESS BL 9A-X2

D-15637

The same sample had the characteristic shown in Figure 10(b) after heat treatment at 250°C for a total of 11 minutes. Note the higher plasma voltages, the reduced breakdown voltages and the large hysteresis in the 3rd quadrant.

Similar results were obtained with BL-10C Ti-Au metallization. With both metallizations, temperatures over 375°C completely destroyed the breakdown characteristic of the checkerboard device. With the Ti-Au metallization, only a few seconds passed before alloying occurred over the entire surface of the thin gold. With the Cr-Au elements, a longer period of a minute or so was required to observe complete formation of the Au-Si eutectic on the thin gold contact.

It is suggested by these results that high temperature metallization on limiter elements would maintain contact uniformity at process and operating temperatures. Thus, product yield and producibility should be greatly enhanced.

S/N	Mean Contact Diameter (mils)	Bandwidth 3 dB	Insertion Loss (dB)	Burnout Level	Recovery At Max Power
BL-12A-1B	9.25 mils	770 MHz	1.2 dB	5 kW	1.8 μs
BL-12A-2B	9.90 mils	600 MHz	1.5 dB	15 kW	2.7 μs
BL-12A-6B	7.32 mils	990 MHz	0.9 dB	1 kW*	1.1 μs

*Arcing noted

TABLE V

FAILURE ANALYSIS DEVICE CHARACTERISTICS

V. PROBLEM AREAS

A. Photoplating in Batch Process

Presently, we are having problems in photoplating the gold post which will be resolved in the near future.

B. Metallization

High temperature metallization schemes are under investigation to improve the adhesion and power handling capability of the bulk limiters.

C. Recovery Time

The recovery times obtained with both single and dual slot bulk limiters have been in the order of 1.5 to 2 microseconds. This may be reduced by geometry changes being incorporated in the batch fabrication work currently underway.

VI. DELIVERIES

During the quarter, we delivered Second Engineering Sample diodes (Item 0001AA) to the U.S. Army Electronics Command. These included five (5) X-band semiconductor bulk limiters and a clean up limiter. The electrical test data of these diodes is given in Table VI.

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS- 3940X1	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 1	OF 3

SPECIFICATION SCS-486 LOT SIZE SALES ORDER NO.

PARAMETERS		f_o		$L_i f_o$		3dB Band-width										
TEST CONDITIONS																
MIN. LIMITS		--		--		--										
MAX. LIMITS		--		--		--										
	SINGLE SLOT BULK LIMITERS WITHOUT ANY CLEAN-UP LIMITER															
S/N B		9300		2.0dB		.660										
S/N Z		9560		0.4		.760										
S/N BL7A-1-A		8860		1.3		.460 [This limiter withstood 40kW when tuned in a package with the clean-up limiter at 9300 ± 50MHz]										
S/N																
S/N	DUAL SLOT BULK LIMITERS WITHOUT ANY CLEAN-UP LIMITER															
S/N 1 Top Slot		9000		0.5		.700										
S/N Bottom Slot		8800		0.7		.960										
S/N Both Slots		9300		0.4		1.750										
S/N																
S/N I Top Slot		8870		0.9		.890										
S/N Bottom Slot		8370		0.8		.800										
S/N Both Slots		9200		0.6		1.690										
S/N																
S/N																
S/N																
S/N																

TABLE VI

SECOND ENGINEERING SAMPLES

TESTED BY: R. Hampsten DATE: 1/24/77 Q. C. APPROVED BY: DATE:

PROD. APPROVED	DATE	MICRONAME ASSOCIATES, INC.	DS - 3940XM	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 2	OF 3

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS		P_o	P_f	R_t		P_o	P_f	R_t		P_o	P_f	R_t
TEST CONDITIONS		tp=1.0μsec; Prr=1x10^{3}Hz Du.=.001 Frequency-9.0GHz				tp=1.0μsec; Prr=1x10^{3}Hz Du.=.001 Frequency-9.3GHz				tp=1.0μsec; Prr=1x10^{3}Hz Du.=.001 Frequency-9.6GHz		
MIN. LIMITS		--	--	--		--	--	--		--	--	--
MAX. LIMITS		30kW	--	0.8μsec		30kW	--	0.8μsec		30kW	--	0.8μsec
		SINGLE SLOT BULK LIMITERS WITHOUT ANY CLEAN-UP LIMITER										
S/N B		27.5kW	31w	1.2μs		25kW	25w	1.8μs		20kW	19w	1.5μs
S/N Z		22.0kW	25w	2.0μs		18kW	40w	2.0μs		17.5kW	31w	2.0μs
S/N												
S/N		DUAL SLOT BULK LIMITERS WITHOUT ANY CLEAN-UP LIMITER										
S/N												
S/N 1 Top Slot		10.0kW	40w	1.5μs		10.0kW	100w	1.0μs		8.0kW	31w	2.0μs
S/N Bottom Slot		10.0kW	40w	1.5μs		10.0kW	60w	1.5μs		8.0kW	60w	2.0μs
S/N Both Slots		10.0kW	200w	1.2μs		10.0kW	160w	1.2μs		10.0kW	160w	1.9μs
S/N												
S/N I Top Slot		10.0kW	20w	1.5μs		10.0kW	25w	1.2μs		10.0kW	25w	1.8μs
S/N Bottom Slot		10.0kW	16w	1.2μs		10.0kW	19w	1.2μs		10.0kW	16w	1.4μs
S/N Both Slots		10.0kW	100w	1.2μs		10.0kW	100w	1.2μs		10.0kW	50w	1.2μs
S/N												
S/N												
S/N												
S/N												

TABLE VI

SECOND ENGINEERING SAMPLES (Cont'd)

TESTED BY: P. Hovannisian DATE: 1/24/77 Q. C. APPROVED BY: DATE:

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS- 39040XM	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 3	OF 3

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS		Li at 9.0GHz		Li at 9.3GHz		Li at 9.65GHz		VSWR at 9.0GHz		VSWR at 9.3GHz		VSWR at 9.65GHz			
TEST CONDITIONS															
MIN. LIMITS		--		--		--		--		--		--			
MAX. LIMITS		0.7dB		0.7dB		0.7dB		1.4:1		1.4:1		1.4:1			
	DUAL SLOT BULK LIMITERS TONED IN PACKAGE WITH CLEAN-UP LIMITER														
S/N															
S/N 1		0.8dB		0.8dB		0.8dB		1.25		1.29		1.10			
S/N															
S/N I		0.8dB		0.8dB		0.8dB		1.24		1.27		1.20			
S/N															
S/N															
S/N															
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S/N															
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S/N															
S/N															
S/N															
S/N															

TABLE VI

SECOND ENGINEERING SAMPLES (Cont'd)

TESTED BY: P. Hovannisian DATE: 1/24/77 Q. C. APPROVED BY: DATE:

FORM 707-C

VII. CONCLUSIONS

X-band bulk limiters have been fabricated using high resistivity silicon with ρ = 15,000 to 20,000 ohm cm, p type uncompensated from Wacker Chemical Company and ρ = 12,000 to 15,000 ohm cm, p type uncompensated from Hughes Industrial Products Division. Bulk limiters from Hughes' wafers also exhibited power handling capability of 15 kW to 20 kW RF power, but the yield from these wafers were extremely poor and a large number of bulk limiter chips were found cracked after diffusion bonding and silicon etching. No cracking problem was experienced with the standard Wacker silicon wafers.

Batch process and ball-bonding schemes have been introduced to manufacture bulk limiters at a low cost with good yield. High temperature metallization experiments are under investigation to improve the adhesion and power handling capabilities of bulk limiters. Wafer thickness, metallization and semiconductor processing are being optimized to achieve both bandwidth and RF power goals of the contract.

VIII. PROGRAM FOR THE NEXT QUARTER

During the next quarter, we will fabricate devices with improved yield and performance by a batch process and ball-bonding technique. Low temperature glass passivation schemes will be implemented to further improve the power handling capability of the bulk limiters.

We have received a high resistivity silicon ingot (ρ = 26,000 - 32,000 Ωcm) <111> orientation grown by Hughes Aircraft for bulk limiter evaluation in the next quarter.

IX. IDENTIFICATION OF PERSONNEL

During this quarter, the following technical personnel contributed to this program.

Title	Manhours
Project Manager	375
Silicon Materials Manager	30
Senior Processing Engineer	60
Processing Engineer	70
Limiter Engineer	90
Engineering Assistant (Fabrication)	600
Engineering Assistant (Test)	300

Electronic Command

Technical Requirements

SCS-486

28 March 1975

High Power Bulk Semiconductor Limiter

1. SCOPE: This specification describes a passive, solid state, receiver protector using a bulk semiconductor limiter in combination with a semiconductor diode limiter. Limiter operation will provide isolation from x-Band pulses up to 30 kw over a variety of test conditions.

2. APPLICABLE DOCUMENTS

2.1 Documents. - The following documents, of issue in effect on the date of invitation for bids, form a part of this specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-E-1	General Specification for Electron Tube
MIL-P-11268	Parts, Materials, and Processes Used in Electronic Equipment

STANDARDS

MILITARY

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-202	Test Methods for Electronic and Electrical Components Parts

MIL-STD-1311A Microwave Oscillator Test Methods

(Copies of specifications, standards and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both the title and number of symbol should be stipulated when requesting copies.)

FSC 5961

REQUIREMENTS:

3.1 Function Description. - The high power, solid state, limiter specified herein will operate in the frequency band 9.0 - 9.65 GHZ. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed tuned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

3.2 Mechanical Characteristics. - The bulk semiconductor limiter structure will conform to the following requirements:

(a)	Weight	20 oz max
(b)	Input flange	mates with UG-40B/U choke flange
(c)	Output flange	mates with UG-135/U cover flange
(d)	Mounting position	any
(e)	Cooling	conduction

3.2.1 Physical Dimensions. - The bulk semiconductor limiter shall conform to Figure 1.

3.2.2 Construction. - Parts and materials will be in accordance with MIL-P-11268.

3.3 Electrical characteristics. - The bulk semiconductor limiter will conform to the following requirements:

(a)	Peak Rf Input power, 1μsec pulses continuous	:	30 kw, Du = .001 10 kw, Du = .01
(b)	Insertion Loss	:	0.7dB (max)
(c)	Low Level VSWR	:	1.4:1 (max)
(d)	Recovery Time	:	0.8μsec (max)
(e)	Flat Leakage	:	50 mw (max), for 30 kw, .001 duty cycle, 1μsec pulse
(f)	Spike Leakage	:	750 mw (max), for 30 kw, .001 duty cycle, 1 μsec pulse
(g)	external bias	:	none

3.4 Absolute Ratings

Parameter	Symbol	Min	Max	Unit
Frequency	F	9.0	9.65	GHZ
Peak Power	P		30	kw
Average Power	Pa		100	w
Ambient Temp.	T_A	-55	+85	°C
Altitude	—		50,000	ft

3.5 Marking. - Each bulk semiconductor limiter shall be marked with the following information:

(a) Manufacturer's model number

(b) Manufacturer's serial number, individually for each limiter.

(c) rf input port.

(d) rf output port.

4. QUALITY ASSURANCE PROVISIONS

4.1 Inspection.

4.1.1 Responsibility for inspection. - The contractor is responsible for the performance of all inspection requirements as specified herein. The contractor may utilize his own facilities or any commercial laboratory acceptable to the government. The government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements. Inspection records of the examinations and tests shall be kept complete and available to the government.

4.1.2 Test equipment c inspection facilities. - Test equi, ent and inspection facilities shall be of sufficient accuracy, quality, and quantity to permit performance of the required inspection. The supplier shall establish calibration of inspection equipment to the satisfaction of the government.

4.2 Classification of inspection. - The examination and testing of limiters shall be classified as follows:

a. First article inspection (see 4.3).

b. Quality conformance inspection (see 4.4.).

4.3 First article inspection. - First article inspection shall be performed by the supplier, after award of contract and prior to production at a location acceptable to the government. It shall be performed on sample units which have been produced with equipment and procedures which will be used in production. This inspection shall consist of QCI-1, QCI-2 and QCI-3 inspection in accordance with 4.4.1, 4.4.2 and 4.4.3.

4.3.1 Sample. - Twenty (20) limiters shall be submitted for first article inspection.

4.4 Quality Conformance Inspection.

4.4.1 Quality conformance inspection - Part 1 (QCI-1). - Every limiter shall be tested in all positions of the Quality Conformance Inspection - Part 1 (QCI-1). No failures shall be permitted.

4.4.2 Quality conformance inspection - Part 2 (QCI-2). - The Quality Conformance Inspection - Part 2 (QCI-2) shall be performed in accordance with MIL-STD-105, Inspection Level S1 with an AQL of 6.5%. In the event of lot rejection, tightened inspection procedures shall be invoked. Normal inspection shall be resumed when two (2) consecutive lots have conformed with QCI-2 tests. If the lot size is less than 50 limiters, the sample size shall be one (1) with an acceptance number of zero (0). For purposes of inspection, the lot size shall be one (1) month's production.

4.4.3 Quality conformance inspection - Part 3 (QCI-3). - Three limiters shall undergo continuous life testing for a min. of 2500 hrs. No failures shall be permitted.

4.5 Detailed listings of quality conformance inspection tests. - Quality conformance inspection tests shall be conducted in accordance with Table I (QCI-1), Table II (QCI-2), and Table III (QCI-3).

4.6 Test Conditions

Parameter Unit	T_A °C	Fo GHZ	Po Watts	μ sec	P_{RR} Pulses/sec	Du	Watts
TC 1	25±3	9.0, 9.375, 9.65±.01	30,000 ± 500	1.0±0.1	1000±25	.001	30
TC 2	25±3	9.0 - 9.65 ± .01	0.001	CW	—	—	—
TC 3	25±3	9.0, 9.375, 9.65±.01	—	1.0±0.1	1000±25	.001	—
TC 4	25±3	9.0, 9.375, 9.65±.01	10,000 ± 250	1.0±0.1	10,000 ±150	.01	100
TC 5	25±3	9.375±.01	30,000 ± 500	1.±0.1	1000 ±25	.001	30
TC 6	—	—	0	—	—	—	—
TC 7	25±3	—	0	—	—	—	—

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Units	Notes
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f		50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s		750	mw	2,3
Insertion Loss	1311A	4416	TC 2	Li		0.7	db	3,4
Low Level VSWR	1311A	4473	TC 2	σ		1.4:1	—	3,4,5
Recovery Time	1311A	4471B (Method B)	TC 1	τ		0.8	μ sec	3,8
Firing Power	1311A	4496	TC 3	P_{FR}		150	mw	3,6,8

Quality Conformance Inspection - Part 1 (Qc 1-1)

Table II

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Unit	No.
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f	—	100	W	1,7
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s	—	400	W	2,7
Maximum Leakage (flat)	1311A	4452A	TC 4	P_f	—	50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 4	P_s	—	750	mw	2,3
Recovery Characteristic(phase)	—	—	TC 5	ΔR_p	—	0.5	degree	3,8,9
Recovery Characteristic (amplitude)	—	—	TC 5	ΔR_a	—	0.1	db	3,8,9
Temperature Cycling(non-oper.)	1131A	1027	TC 6	ΔL_i Δf_3 $\Delta \gamma$	—	0.2 100 0.2	db mw μ sec	10
Vibration	202E	204C Method A	TC 7	ΔL_i Δf_3 $\Delta \gamma$	—	0.2 100 0.2	db mw μ sec	10
Shock	202E	213B Method G	TC 7	ΔL_i Δf_3 $\Delta \gamma$	—	0.2 100 0.2	db mw μ sec	10
Humitity	1311A	1011	TC 6	ΔL_i Δf_3 $\Delta \gamma$	—	0 0 0	db mw μ sec	10

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Unit	Notes
Life Test	1311A	4551A	TC 5	t	2500		hours	11
Life Test End-Point (1)	1311A	4452A	TC 1	P_s		1.0	watt	2,3
Life Test End-Point (2)	1311A	4416	TC 2	L_i		0.9	db	3,4
Life Test End-Point (3)	1311A	4471B	TC 1	γ		1.0	μ sec	3
Life Test End-Point (4)	1311A	4452A	TC 1	P_f		75	mw	1,3
Life Test End-Point (5)	1311A	4496	—	P_{FR}		170	mw	3,6

Quality Conformance Inspection - Part 2 (QC111-3)

OTES:

o maximum flat leakage shall not exceed the specified limits for test frequencies 9 000, 9.375, .9.650GHZ. The incident Rf pulse will have a risetime 50 nanoseconds maximum. Test configuration reference figure 4452 - 1b. The peak power measurement will be accomplished by calibrating the deflection of a sampling oscilloscope as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A.

. The maximum spike leakage shall not exceed the specified limits for test frequencies 9.000, 9.375, 9.650 GHZ. Oscilloscope calibration technique as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A is applicable. Amplitude variation shall be recorded by observing the distribution of spike amplitudes for 1 minute time through open shutter of scope camera.

. Quality conformance test to be made using multi-stage limiter. For example using the high power bulk stage followed by the limiter diode.

. A swept frequency may be used.

. Match Termination used in this test circuit shall have a VSWR of 1.05 or less.

. The firming power shall be defined as a db increase of limiter insertion loss mpared to the "cold" insertion loss.

'. Quality conformance test to be made using bulk semiconductor stage only.

i. For this specification the following abbreviations and symbols in addition to MIL-E-1 abbreviations and symbols shall apply; τ = time (recovery), ΔR_p = variation of phase on recovery (total deviation at a fired time), ΔR_a = variation of amplitude on recovery (total deviation at a fixed time), P_{FR} = firing power.

'. The maximum variation in phase and amplitude as measured by dynamic phase and amplitude test facility shall not vary more than the specified limits over a 1 minute integration time period. Measurement to be made at a point 5μsec from the cessation of 1μsec input pulse.

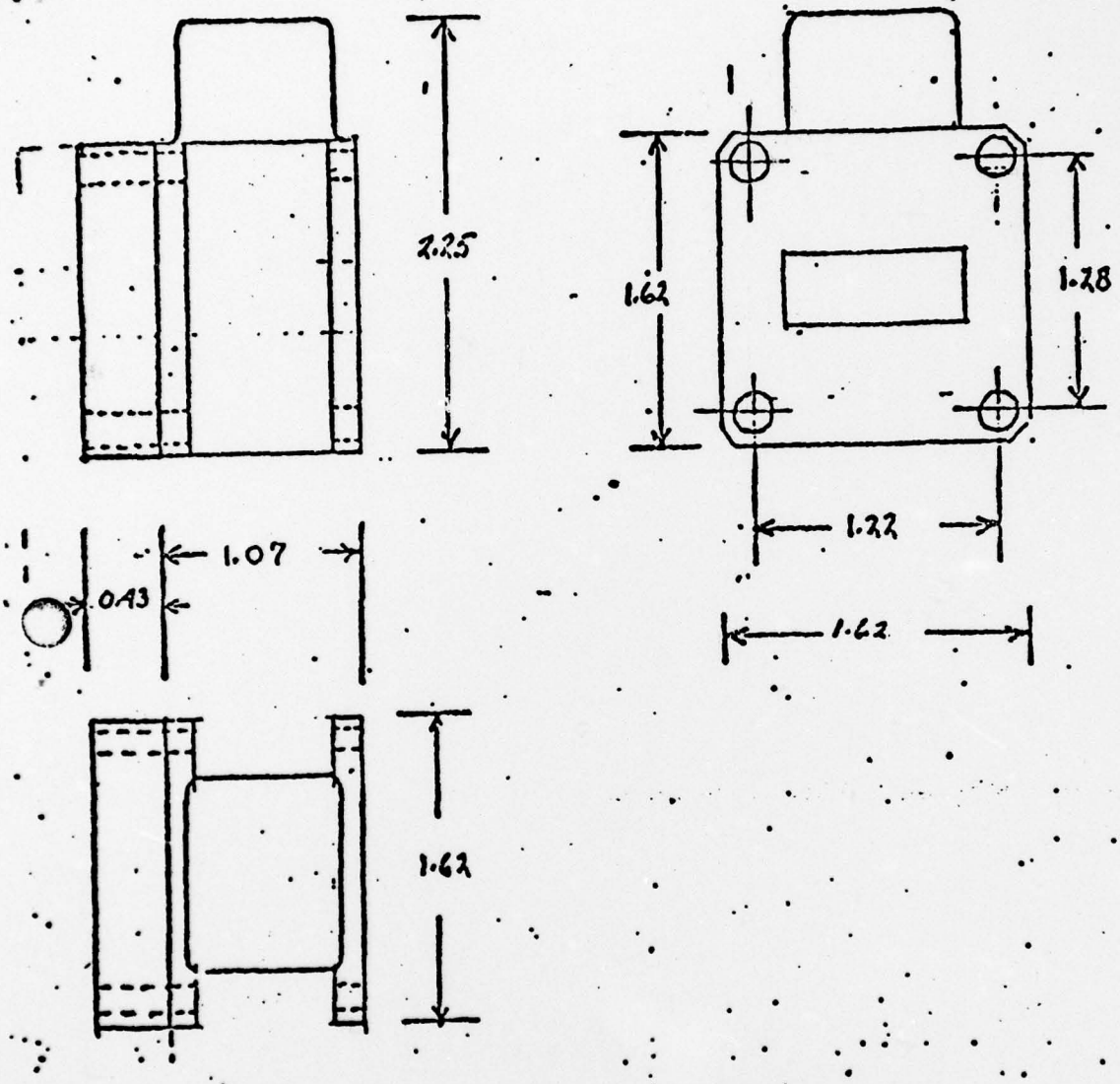
0. Measurement of parameters cited will follow the procedures outlined in QCI -1.

i. The bulk semiconductor limiter shall operate over the entire duration of the life test. The spike leakage (P_s) will be periodically monitored. Life test will be interrupted each 720 ± 20 hours interuals to permit testing of end of life test end points.

5. PREPARATION FOR DELIVERY

5.1 Packaging, Packing and Marking. - Packaging, packing and package marking shall be specified in the contract.

OUTLINE DRAWING



Notes:

a) all dimensions in inches

b) all tolerances ± 0.01 unless otherwise specified

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