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MONOLITHIC 20W 2GHZ TRANSISTOR AND MONOLITHIC 5W 4GHZ TRANSISTO--ETC(U)
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MONOLITHIC 20W 2GHz TRANSISTOR AND MONOLITHIC 5W 4GHz TRANSISTOR

QUARTERLY REPORT NO. 1
16 MAY 1977 - 13 SEPTEMBER 1977
CONTRACT No. DAAB07-77-C-0431

PREPARED FOR:
COMMUNICATIONS SYSTEMS PROCUREMENT BRANCH
PROCUREMENT AND PRODUCTION DIRECTORATE
US ARMY ELECTRONICS COMMAND
FORT MONMOUTH, NEW JERSEY 07703

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Acknowledgement Statement

This project has been accomplished as part of the US Army (Manufacturing and Technology) Program, which has as its objective the timely establishment of manufacturing processes, techniques or equipment to insure the efficient production of current or future defense programs.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Wire bonding experiments on existing microwave dice were performed to determine optimum bonding configurations for microwave transistors. The results of these experiments guided the design of the active portion of the monolithic 2 GHz device, the L-10.

To define a 4GHz material specification, several lots of 4 GHz dice are being processed. The results of experiments on epitaxial resistivity and profile will guide the specification of PIN epitaxial material for the 4 GHz portion of the program.

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SECTION I

1.0 PURPOSE

The purpose of this program is to provide for the development of two separate state-of-the-art solid state devices. They are bipolar microwave power transistors with integral monolithic matching networks to be used in amplifier applications. These devices will be configured in such a way as to allow the direct attachment of the monolithic transistor chip directly to a metal heat sink, thus eliminating the BeO insulator which is typically found in existing microwave power transistor packages.

The two devices to be developed are a 20W/2GHz device and a 5W/4GHz device. These two devices are to operate in the CW mode.

Sufficient quantity of these devices will be fabricated to demonstrate the production feasibility of the basic design and assembly techniques.

SECTION II

TECHNICAL NARRATIVE

2.0 INTRODUCTION

During the first period of this contract effort work was done in primarily two areas.

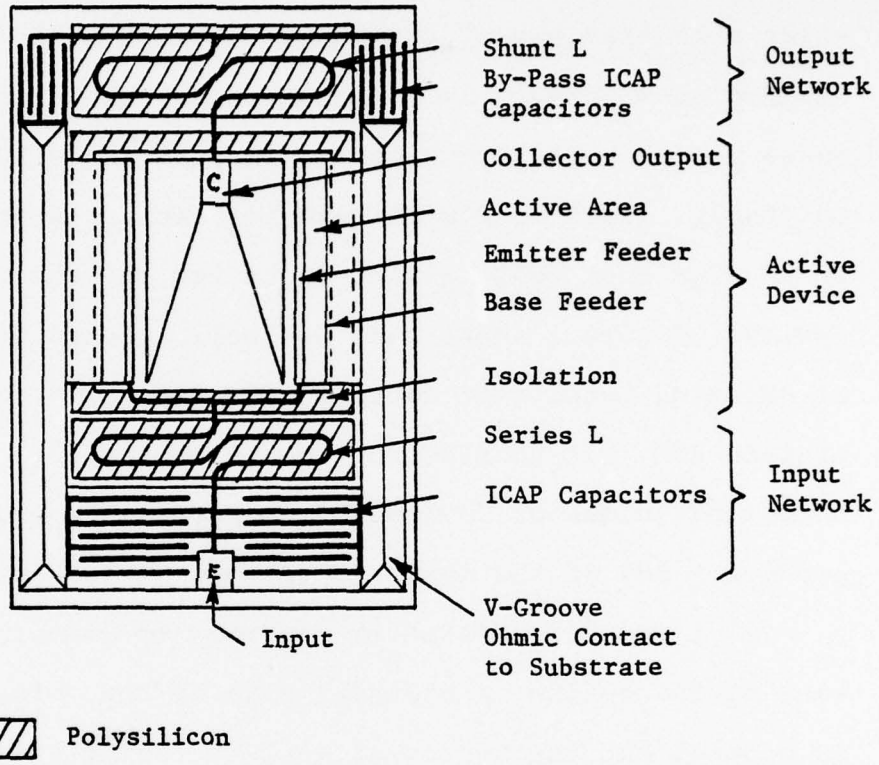
The first is the design of the active portion of the 20W/2GHz device and associated experimentation on existing devices related to that design.

The second is the development and finalization of a material specification for 4GHz high power bipolar transistors. A standard diffusion process for adequate f_t for medium power devices already exists, however, a material specification suitable for high power Class C devices has not been defined.

2.1 20W/2GHz ACTIVE DEVICE DESIGN

The active portion of the 20W/2GHz device was designed and masks ordered in this period. The active portion alone will be fabricated first to provide a vehicle for impedance characterization. An accurate model of the active device is necessary before the specific requirements of the passive matching networks can be calculated, although the general form of the passive structure and the characteristics of its elements have already been determined in work supported by NRL in contract number N00014-75-C-0405.

A projected layout of the active and passive portions in integrated form is shown in Figure 1.



L-10, 10W CW, 2.0 GHz
Size: 47 x 67 mils, with 2 mils scribe line
Area: 3149 mils^2
≈ 968 die/wafer

Figure 1. L-10, 10W CW, 2.0 GHz

The active portion of the device consists of two bases with an interdigitated emitter structure. Specifications for the dimensions can be found in Table 1. The bases are configured in pairs such that two of the bases comprise a "cell." A cell is defined as a separately bondable unit. Since each pair of bases share a common collector connection, a single base cannot be used by itself. Each cell will have its own integrated matching network. Two such cells will be required to make the 20W/2GHz device. Figure 1 shows only one cell. Based on the performance of existing monolithic devices, the two cells combined should produce 25W, not considering combining losses. With typical combining losses of devices of this size, we expect the device to produce $\tilde{>}$ 80% of the maximum possible power, or 20W CW.

A grounding "via" is provided to directly connect each base to the bottom or grounded side of the chip, and the collector is brought out the top. Vertical collector isolation is provided by a PIN epi structure, and horizontal isolation is provided by a polysilicon-filled V-groove.

2.1.1 FEEDER POINT TESTS

In order to determine the optimum point or points of connection to the feeder bars of an individual base or cell, several tests were devised. The tests were empirical in nature.

Typical cells are fed at the center of the feeder bars,

TABLE 1. L-10 SPECIFICATIONS

Bases per cell	2
Base size	2.8 x 26.5 mils
Total number of fingers	310
Total number of emitters	154
Emitter length	2.34 mils
Emitter width	0.07 mils
Ep/Ba ratio	4.85 $mils^{-1}$
Chip size	37 x 42 mils
Estimated power output @ 16mw/mil Ep	11.52 watts
Total emitter ballasting	0.5Ω

however, this physical structure is not directly compatible with monolithic network design philosophy at this time.

The feeder tests were done to find a feeding geometry which is compatible with monolithic design philosophy while providing adequate uniformity of current distribution and performance.

The vehicles used for these tests were an experimental pulse device, the MP-2, and a specially prepared SB-2000. The MP-2 has feeder bars large enough to connect wires at any point along its length. The SB-2000 normally can only be bonded on the bonding pads at the centers of the feeder bars, due to the fact that the feeder bars are too narrow and a wire placed on them would short out the active region. However, the special SB-2000 devices were provided with plated-up feeder bars, as shown in Figure 2. The metal of the feeder bars in this device is about 5μ thick over the length of the feeder. The vertical separation between the finger metallization and the top of the feeder bar is sufficient to allow wires to be bonded to at any point on the feeder without contacting the finger metallization.

Initial testing was done with the MP-2 in L-Band. The MP-2, Figure 3, is a large device intended for short pulse operation, and therefore was not designed with emitter ballasting.

Experimental results showed that this device was very sensitive to the position of the feed point. Several dB of output power would be lost if the bases were fed from any point other

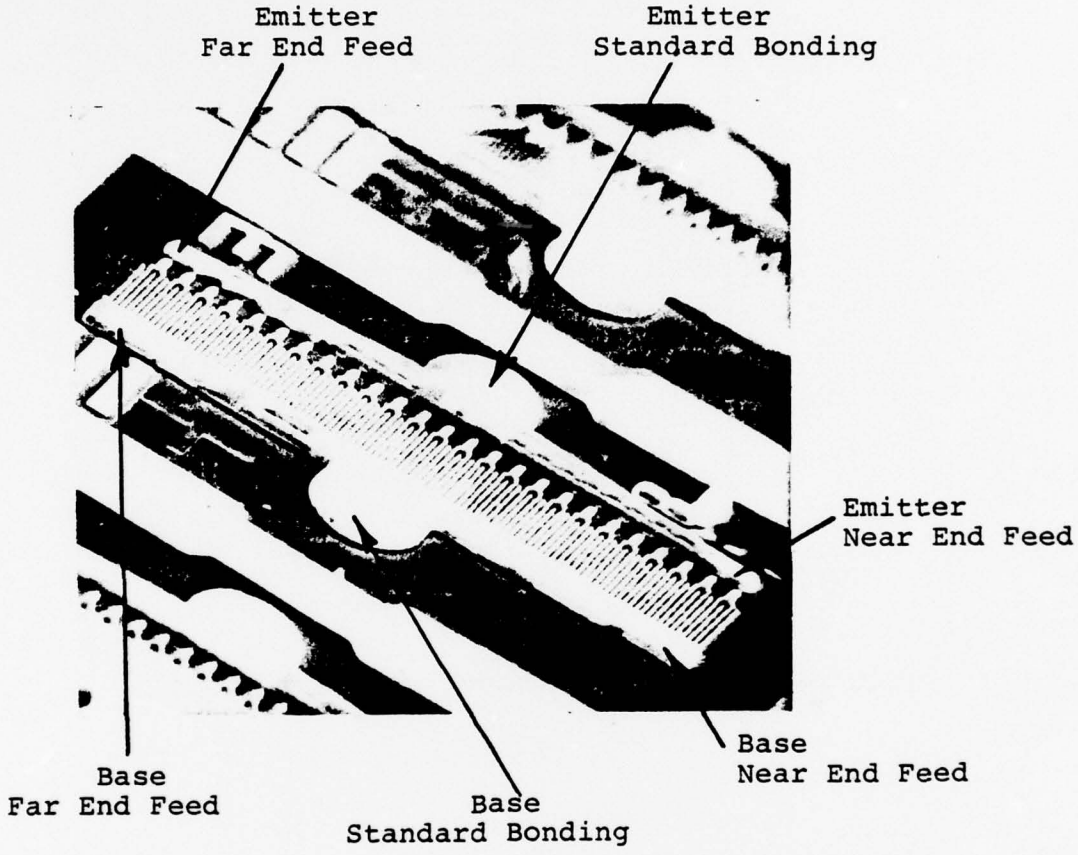


Figure 2. SB-2000 Plated-up Feeder

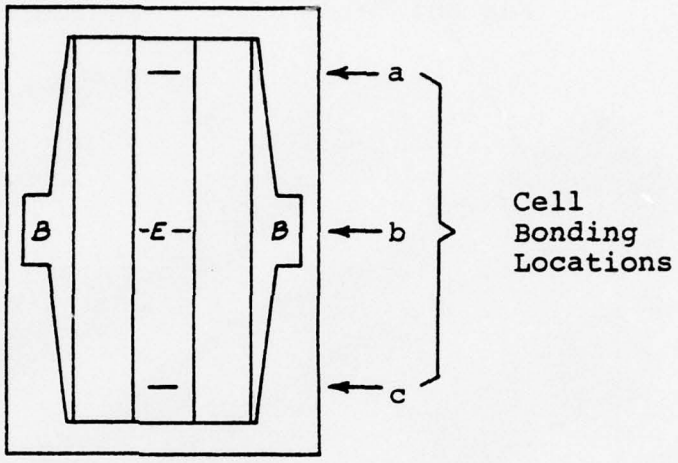


Figure 3. MP-2-5B Device

than the center. Also the emitter was very sensitive. The only acceptable feed point was the far end, point a in Figure 3. If the emitter was fed from the center, point b of Figure 3, about 1dB of output power was lost. About 2dB of output power was lost when the emitter was fed from point c of Figure 3.

The results of these tests were disturbing, as these acceptable feed points were especially inconvenient for a monolithic design.

The tests were repeated with the special SB-2000 device at 2GHz. A standard device is shown in Figure 4, and the variations of emitter feeding are shown in Figures 5 and 6. In these tests the results were somewhat different.

The actual emitter feed point was unimportant. The center provided the best results with the performance dropping off by about 0.3dB at either end. This reduced sensitivity is attributed to the fact that the SB-2000 is heavily emitter ballasted, while the MP-2 has no ballasting.

The results of the base feed points were also interesting, however, less drastic than with the MP-2.

The best overall feed point was at the center with a double stitch bond, Figure 4; that is, a base wire to ground at both the input and output sides of the package. When the base feed point was moved to the near end, Figure 7, a 0.5dB drop of output power was noted. When both base wires were moved to the far end,

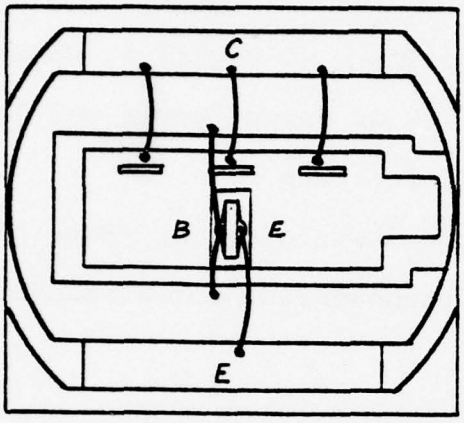


Figure 4. Standard Bonding with Double Stitch Bond

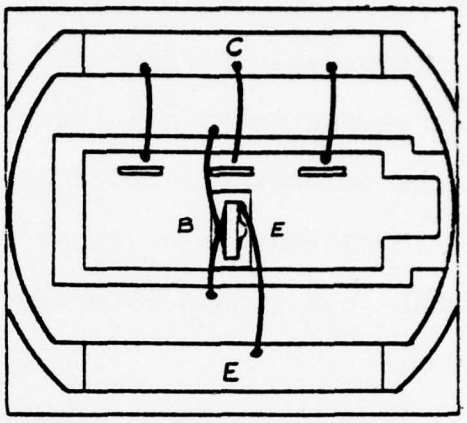


Figure 5. Far End Emitter Feed

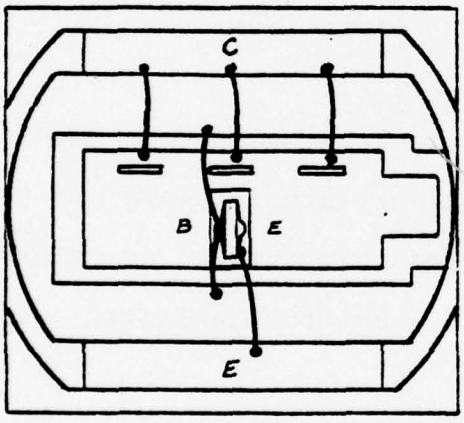


Figure 6. Near End Emitter Feed

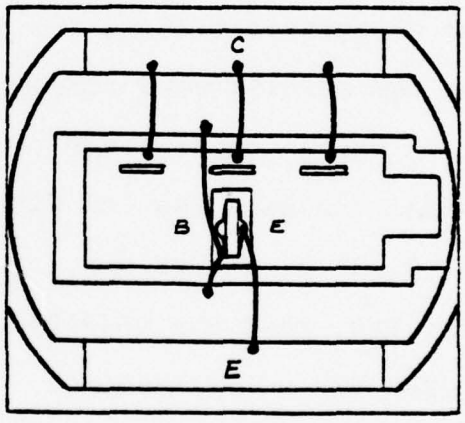


Figure 7. Near End Base Feed with Double Stitch Bond.

Figure 8, similar results were noted.

When a single base wire was used as in Figure 9, the output power dropped drastically by about 1.9dB. Single wire feeds at other points, Figures 10 and 11, provided similar poor results of several dB of lost power.

However, when the base was grounded by short wires from each end, Figure 12, the power of the test device returned to within 0.2dB of its standard configuration value. In this configuration the overall device stability was enhanced so that its drive-up characteristic was better than any other configuration.

2.1.2 MASK DESIGN

On the basis of the feeder experiments, the performance of existing monolithic devices, and the unique layout constraints of monolithic integrated circuits, the L-10 mask set was designed. A detailed layout of the device is shown in Figure 13, and specifications are summarized in Table 1. The L-10 is intended to produce 10W CW at 2.0GHz.

Since the results of the feeder tests indicated that the emitter feed point is not critical, the feeder was designed to be fed at the most convenient point, the near-end. The feeder is designed to be plated-up so that it may be connected anywhere if it proves to be necessary to obtain acceptable performance.

The feeder tests indicated that a center fed base is the

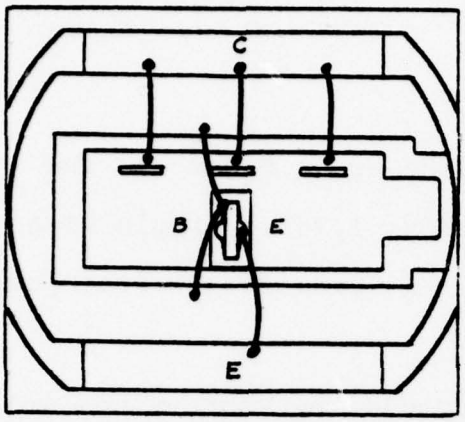


Figure 8. Far End Base Feed with Double Stitch Bond

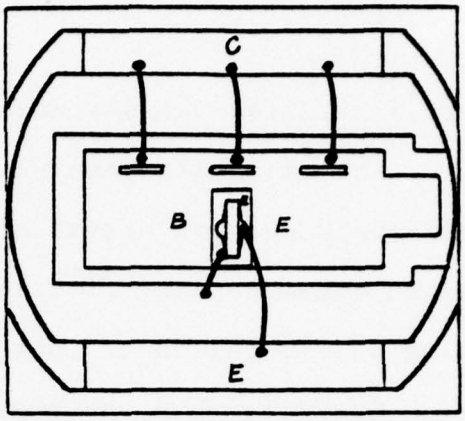


Figure 9. Near End Base Feed with Single Bond

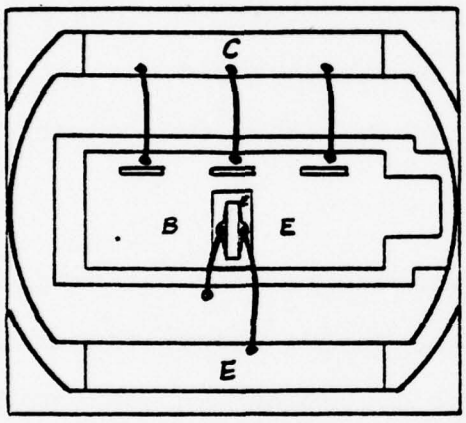


Figure 10. Center Base Feed with Single Bond

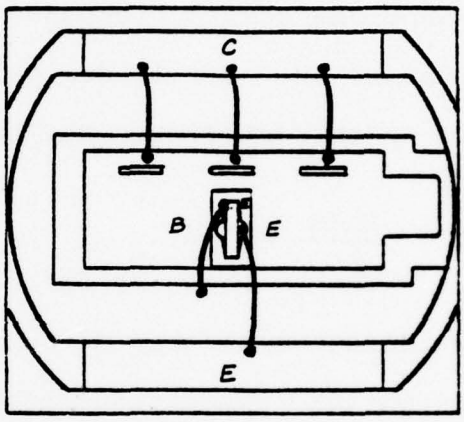


Figure 11. Far End Base Feed with Single Bond

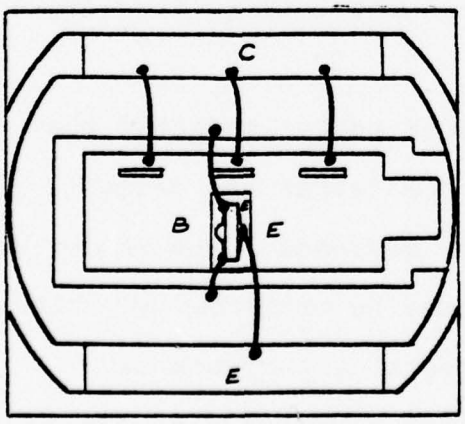


Figure 12. Both End Base Feed with Two Bonds

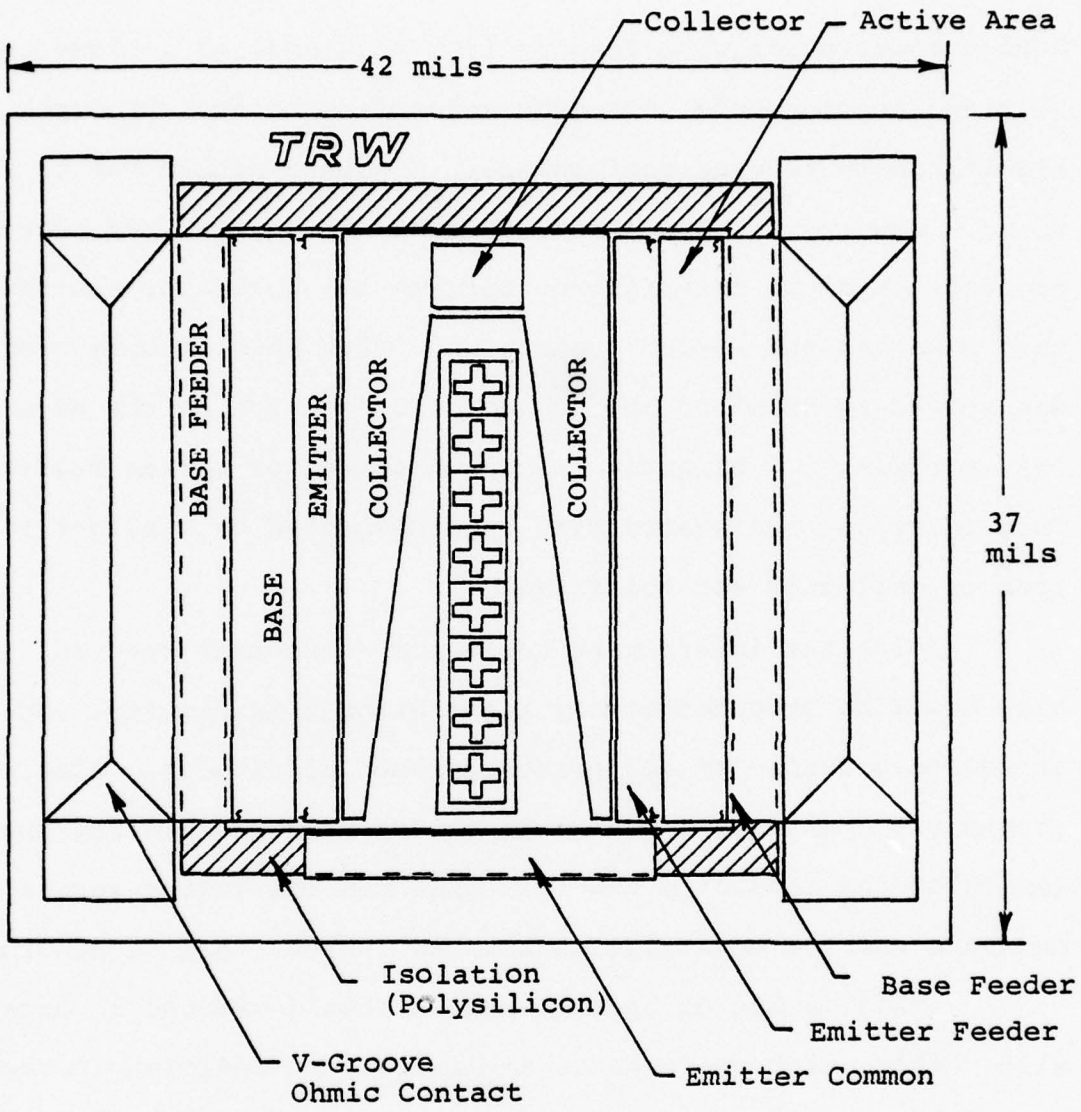


Figure 13. L-10 Device Layout

best configuration with feeding from both ends as a close second. Near end feeding only, the most convenient method, produced significantly reduced performance. A better method had to be found. Feeding the base from any other point than the near end produces physical interference between the collector contact on that side and the feeder connection. This interference problem was solved by deleting the collector connection on the base side. This produces slightly increased collector series resistance. This increased resistance will be compensated by a slight reduction of collector epi thickness.

With the interfering collector connection removed, the base could be grounded at any point without difficulty. In fact, it can be grounded at <u>all</u> points without difficulty. Placing the ground via parallel and next to the base and connecting the full length of the feeder to the via produces the lowest series inductance and the best distribution of current that we can foresee.

This method of base grounding should produce an exceptionally stable, high performance amplifier. In addition in the final monolithic device, the input capacitor and the shunt inductor can be returned directly to the via metallization which causes the large circulating currents in those two elements to virtually bypass the residual small series resistance of the via which is projected to be less than 25 milliohm per via.

The two bases of the cell of the L-10 are situated in a common isolation moat. The use of a common moat increases the isolation capacitance by about 1.0pf over the use of two separate moats. However, since the collector bonding pad is now on top of the isolated collector region instead of a non-isolated region, it contributes no additional capacitance as it would in the two-moat layout.

Drawings for this design were submitted to mask vendors and masks were ordered during this period of work.

2.2 PROGRESS OF 4GHz MATERIAL SPECIFICATIONS

In order to finalize a material specification for 4GHz devices for high power Class C operation, several experimental lots of dice are in process using an existing 4GHz mask set. The mask set is designated SB-4. The die produced are designated SB-4000. The lots in process are designated BL-2, BL-3, BL-4, BL-5, and CCL-1.

BL-2 and BL-3 are being fabricated by the standard diffusion process used in the microwave production plant. The epitaxial material for these lots is a single layer of 0.8Ω-cm phosphorous doped epi of a thickness of 5μ. The substrate is arsenic doped of 0.005Ω-cm. This material and process provide high gain medium power 4GHz devices such as used in 4GHz Class A product. To

produce optimum Class C performance, the material specification must be optimized to provide lower $V_{ce(sat)}$.

BL-2 is at wafer validation. There are four wafers with a high percentage of shorted emitter-base junctions. BL-3 has been through emitter drive and shows low β (2-8) on three wafers. The problems with both of these lots is outside acceptable limits and the cause is under investigation.

BL-4 and BL-5 are being coprocessed and consist of a total of 13 wafers. They use the same epitaxial material, however, material has received a back diffusion at 1200°C to reduce the thickness of the epitaxial layer to about 2μ. This reduced thickness epi is similar in nature to the material which was used in the 5W/5GHz program. These two lots are at base implant and are proceeding through the standard process.

Lot CCL-1 has been through P+ (ballast resistor) diffusion. This lot differs from the others in that it uses a buffered epi. We feel that the addition of a buffer layer will allow the use of very thin epi layers to allow high saturated power while maintaining the ruggedness inherent in the thicker layers. If our predictions are correct and performance and ruggedness are enhanced, then the buffer can be included in the monolithic epitaxial structure.

SECTION III

CONCLUSIONS

3.0 DESIGN

The L-10 mask set has been designed and ordered. This mask set incorporates the latest design innovations and is compatible with future integration into a monolithic configuration.

3.1 PROCESS SPECIFICATIONS

Although the initial lots of dice have suffered from as yet unidentified process problems, the lots in process have an excellent probability for success. The vertical geometry for high gain (junction depth and sheet resistance) 4GHz devices is well defined, with only the starting material parameters yet to be defined to produce consistent high gain in conjunction with high saturated power.

SECTION IV

PROGRAM FOR THE NEXT INTERVAL

4.0 The effort on the program for the next interval will include the delivery of the L-10 mask set and the processing of the first lots of L-10 devices. If no unusual delays are encountered, and at least one working wafer of the L-10 design is available, then testing and characterization of the device will begin. After the device impedance and performance are known, then the design of the output and input network can begin.

Work will continue on the material specification for Class "C" 4GHz devices and should be complete in adequate time for the ordering of monolithic epi material for the 4GHz fabrication phase.

SECTION V

PUBLICATIONS, REPORTS, AND CONFERENCES

A Post Award Conference was held on June 23, 1976.

Attendees were as follows:

Government

Alan H. Saltzberg, ACO
James F. Kelly, Project Engineer
George R. Teller, C. O. Rep.
Jim Warr, Industrial Specialist
Mary J. McMahan, Industrial Specialist
Thomas F. Houston, QAR
Ruby Morris, Contract Administrator

TRW

Bernie Lindgren, Program Manager
Penny Burgess, Contract Administrator
Gary L. Kuttnauer, QA
George W. Schreyer, Applications Engineer
Alan Harrington, Process Engineer

Monthly Report Nos. 1, 2, and 3 were submitted during this quarter.

SECTION VI

IDENTIFICATION OF PERSONNEL

NAME	HOURS
Joseph Courier	25
Alan Harrington	100
C. C. Lee	20
Bernie Lindgren	85
Jim Scheppele	75
George Schreyer	120
George Skelly	75
Frank Bartel	30
Harold Bjornson	30
Ella Matthews	50
Norman Nissen	30
Eugenia Nunez	55
Irene Wood	60
Stephanie Wesche	60
Dorothy May	12

Joseph Courier

Joseph Courier has had sixteen years experience in semiconductor field, with product - process responsibilities. From 1961-1965 he was a Sr. Process Engineer at Silicon Transistor Corporation, where he worked on single diffused high power transistors. He was then employed at General Electric Company from 1965-1970 as a Product Design Engineer, where he worked on the development of the TRIAC and plastic encapsulated power transistors.

In 1970 he became R&D Project Manager at International Rectifier Corporation, where he setup a complete line of Planar & Mesa Thyristor products. In 1973 he joined the Raytheon Semiconductor Division with product responsibilities for PNP/NPN transistor products and Epitaxial area. In 1974 he became Supervisory Engineer for Teledyne Semiconductors with product responsibilities for RF transistor product development.

In 1976 he became Product-Process Engineer at Solid State Scientific, working on development of RF power transistors in the VHF-UHF-MICRO-WAVE (30 MHz - 2.5 GHz) frequency ranges.

He joined TRW Semiconductors as Product-Process Engineer in 1977.

Joseph Courier (continued)

Significant Contributions:

1. Developed single and triple diffusion processes.
2. Designed and developed 25 amps TRIAC. Implemented full product line of isolated devices using Beryllia oxide discs. Achieved one million dollars of cost reductions on high volume product lines.
3. Developed controlled process for the epitaxial growth of P^+ on P type substrates.
4. Introduced field relief design on all PNP types product devices.

Education:

E.E., Northeastern University, 1957

B.B.A., Northeastern University, 1960

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Alan L. Harrington

Mr. Harrington has been engaged in the development and research of photovoltaic, MOS/MNS and bipolar devices for the past seventeen years.

As a member of the technical staff with Pacific Semiconductors from 1960-1962 he was involved with the electrical, optical and chemical study of the surface reactions of semiconductor devices and development of methods for controlling their stability. During this time he was directly responsible for the controlled chemical etching of silicon, anisotropic etching of silicon and preparation of silicon substrate for epitaxial deposition.

While with Litton Systems, Inc., Guidance and Control Systems Division from 1962 to 1973, Mr. Harrington's duties included failure analysis of semiconductor devices, investigation of design, materials, and fabrication of the silicon optical sensor utilized in Litton's GS/C Daylight Star-Tracking System. Hr. Harrington's most recent duties at Litton included design, process setups and fabrication of MOS/MNS combined memory devices. Within this area he was principal investigator in the control, understanding and manufacture of MNS memory devices.

At TRW Mr. Harrington, as a member of the CATV technical staff, is engaged in the development of vertical and horizontal isolation techniques to achieve monolithic broadband ultra-linear VHF and microwave amplifiers.

Alan L. Harrington (Continued)

Publications:

"Bulk-Surface Interactions in Silicon Semiconductor Devices," with M. Millea, American Physical Society, 1958.

"A New Selective Etch for Silicon," with J. Crishal, Stanford Device Research Conference, 1961.

"Diffusion of Gold into Silicon," with M. Millea, Stanford Device Research Conference, 1961.

"A Selective Etch for Elemental Silicon," with J. Crishal, Electrochemical Society, 1962.

"Process and Electrical Analysis of Semiconductor Components," with R. MacDougal.

/pe

October, 1977

DR. CHIA-CHUAN LEE

Dr. Chia-Chuan Lee has had ten years' experience in research and development in solid state devices and electronic materials. From 1975 to 1977 he worked in Hewlett-Packard Company's Microwave Technology Center in Santa Rosa as a project engineer, where he developed power GaAs FET and fine line photolithographic technology and conducted the transfer of new technology from R&D to production. Before then Dr. Lee was a senior member of technical staff of Northrop Research Technology Center and was involved in the research of integrated injection logic technology and IR sensor array program.

Prior to joining Northrop, Dr. Lee was a member of the technical staff of the Microelectronics Division of Rockwell International from 1973 to 1974 and was involved in advanced development of MOS/LSI and SOS devices and their applications. He was engaged in the areas of thin film technology, device analysis and semiconductor materials research.

From 1972 to 1973 he was a technical consultant to the Industrial Technology and Research Institute, Ministry of Economic Affairs of the Republic of China. He was responsible for the research and development in ferrite and $BaTiO_3$ disc capacitor process techniques and electron microscopy of electronic materials.

Dr. Lee received his Ph.D. in materials science from the State University of New York, Stony Brook. He was engaged in

DR. CHIA-CHUAN LEE (Continued)

fundamental studies of crystalline, and his doctoral dissertation was the interactions between lattice vacancies and solute atoms in quenched dilute aluminum alloys. He obtained his M.S. (in physics) from Michigan State University and his B.S. (in physics) from Tunghai University in Taiwan.

Dr. Lee also taught physics and engineering at National Tsing-hua University of the Republic of China in 1972-73, Dowling College of New York in 1969-70, and University of Evansville, Indiana, in 1965-66. He is a member of the APS, AIME, AVS, EMSA, and Sigma Pi Sigma.

Publications and Presentations:

"An All Gold Metal System for Aluminum Gata GaAsFETs," H-P Semiconductor Technology Conference, South Lake Tahoe, Ca., 1977.

"Microelectronics Thin Film Resistor Trimming Development," H-P Technology Center Internal Report, 1977.

"The Reduction of Wafer Warpage in MOS Processing," Ext. Abst. no. 131, Volume 75-2, Electrochemical Society Fall Meeting, Dallas, Texas, 1975.

"Characterization of Silicon-on-Sapphire Films for LSI Technology," Ext. Abst. no. 177, Volume 75-1, Electrochemical Society Spring Meeting, Toronto, Canada, 1975.

"The Electrical Resistivity Due to Crystalline Imperfections in Aluminum Thin Films," Ext. Abst. no. 110, Volume 75-1, Electrochemical Society Spring Meeting, Toronto, Canada, 1975.

"Yield Problems Analysis - NMOS-SOS and CMOS-SOS devices," Rockwell International IL #74-762-CL/SO-118, 1974.

DR. CHIA-CHUAN LEE (Continued)

"Junction Profile of CMOS/SOS N+/P$^-$ Diodes," Rockwell International, IL #74-762-CCL-260, 1974.

"Study of Doping Profile of SOS Wafers," Rockwell International IL #74-762-CCL-250, 1974.

"Application of Secondary Ion Mass Spectroscopy (SIMS) to Process Analysis," Rockwell International IL #74-762-CCL-412, 1974.

"Vacancy Trapping by Solute Atoms in Quenched Dilute Al Alloys," Bull. of German Phys. Society Spring Meeting, Munster, Germany, 1973.

"Phonon Drag Thermopower in Ag Alloys," Phil. Mag. 25, 1161 (1972)

"Resistivity and Thermopower of α-phase Ag-Cd Alloys from 4.2^{o}K to 300^{o}K," Bull. Am. Phys. Soc. Series 11, 16, 143 (1971)

"Thermoelectric Power of Tin from 4.2^{o}K to 280^{o}K," Physica 31, 1491 (1966).

EDUCATION:

B.S., Physics - Tunghai University, Taiwan

M.S., Physics - Michigan State University

PhD, Materials Science - State University of New York, Stony Brook

/pe
October, 1977

Bernard A. Lindgren

Since June of 1976 Mr. Lindgren has been a Program Manager in the R&D Laboratories of the Electronics Group of TRW. He is responsible for developing RF semiconductor technology and managing government contracts.

Prior to that he was Engineering Manager in CATV and was responsible for developing and maintaining state-of-the-art semiconductor technology for CATV business. He also was Sales Manager for two years in CATV and was responsible for developing $1.5M in sales. He joined TRW in 1970.

From 1968 to 1970 Mr. Lindgren was employed at Motorola Semiconductors as a product engineer. He was responsible for RF small signal product lines, which grew from $1.0M to $3M during his two year tenure.

Mr. Lindgren was employed at Fairchild Semiconductors as a development engineer in the R&D Laboratories. His duties consisted of developing low noise PNP, conducting surface state studies that led to time-temperature stability of dc h_{fe}, development of dielectrically isolated matched pair PNP transistors, and development of arsenic base PNP for low noise applications.

Bernard A. Lindgren (Continued)

Education:

B.S.E.E., San Jose State University, 1963

M.S.E.E., University of California Berkeley, 1965

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Jim Scheppele

Mr. Scheppele has nine years of experience in the semiconductor industry.

From 1968 to 1973 he was an associate engineer at TRW Semiconductors, where he worked on thin films, diffusion and oxidation studies and various other materials and processing programs in R&D.

In early 1973 he joined the TRW Systems Microelectronics group as a member of the technical staff, where his duties included studies of sources of low temperature noise in silicon junction FETs.

In late 1973 he moved to Fairchild Semiconductors as a Senior Process Development Engineer, where he was responsible for design and development of a VHF-UHF Cascode MOSFET and for providing process maintenance support to the microwave products line.

In 1975 he went to Avantek Inc. as a Process Engineer with responsibilities for liaison between R&D and production with regard to transfer of new products and processes. In this capacity he set up and operated a liquid phase epitaxial facility for production of GaAs epitaxial films for production of low noise FETs as well as producing pilot quantities of low noise FETS demonstrating N.F. $\lesssim$ 2-2.5dB with $\sim$10dB of associated gain at 4GHz.

He rejoined TRW Semiconductors in 1977 as a Senior Engineer in the R&D Materials and Processing group, with primary responsibilities for thin

Jim Scheppele (Continued)

films and low pressure chemical vapor deposition.

Education: Fullerton Jr. College - A.A. Physics - 1969
Cal State University - B.S. Physics - 1973

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GEORGE W. SCHREYER

Mr. Schreyer graduated from Cal Poly Pomona in 1973 with a B.S.E.E. degree and since that time has been associated with TRW Semiconductors, Lawndale, California. For the first two years at TRW, he was an applications engineer in the Microwave Products group. He was responsible for the development, characterization, and pilot production of the TRW 2000, 3000 and 50,000 series of devices.

He was also responsible for the development of various special devices and several broadband 600-1000 MHz devices and 600-1000 MHz multistage MIC amplifier.

He then transferred to R&D to develop the 5W/5GHz and 40W/2GHz devices under ECOM contract and passive monolithic matching structures under NRL contract. He is currently engaged in refinement of microwave cell combining techniques and monolithic integrated circuit design and fabrication.

Publications:

5W/5GHz, ICCC, 1977

40W/2GHz, MTT Workshop, 1977

Professional Affiliation:

Member IEEE/MTT

Education:

B.S.E.E., Cal Poly, 1973

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George Skelly

George Skelly joined TRW Semiconductors in August, 1977, as process engineer in charge of materials and processing, with emphasis on fabrication and evaluation of epitaxial and polycrystalline silicon films.

Previously he was engineering manager at Semimetals, Westbury, N.Y., where he built and installed a new and advanced epitaxial reactor, instituted numerous process controls including the design of a computer controller reactor. He also designed and produced Schottky barrier and zener diodes from raw material to finished device. For the packaging scheme used, new metallization and processing techniques were required.

From 1964 to 1975 he was part of the technical staff at Bell Telephone Laboratories in Murray Hill, N.J. At Bell Labs he produced the first IMPATT diodes operating at 110GHz. Numerous other contributions included first CCD's utilizing polysilicon gates, out-diffusion studies on heavily doped arsenic substrates, operation of front end of bipolar integrated circuit line, silicon procurement, specification and evaluation, defect studies, X-ray topography instrumentation, optical thin films for lasers, etc.

From 1962 to 1964 Mr. Skelly was development engineer at Burroughs Corporation, Plainfield,N.J. There he pioneered hybrid integrated

George Skelly (Continued)

circuit techniques, introduction of the planar process and packaging of hybrid integrated circuits.

From 1957 to 1962 he was associated with Westinghouse Electric Company, Semiconductor Division, Youngwood, Pa. There he developed passivation procedures for high voltage military diodes, processing procedures for high power transistors, trinistors, and diodes. He also introduced improved moly contacts, methods of plating, improvements in ohmic contacts, solders brazing, and assembly techniques.

Education:

B.S., Chemistry - St. Joseph College, Philadelphia
Graduate studies - Fairleigh Dickinson University, Madison, N.J.
Advanced processing, in-house courses - B.T.L.

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October, 1977

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