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INSTRUMENTATION OF SEQUENTIALLY SHIFTED SHIFTING REGISTER.(U)
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Instrumentation of Sequentially Shifted Shifting Register

by

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FORWARD

This memorandum has been prepared for the information of others working in allied fields at NEL [redacted]

INTRODUCTION

Instrumentation studies for signal-processing systems have led to a proposed device, called a Sequential Matched Filter,[1] which requires a special adaptation of a digital shift register. A shift register consists of a linear array of n one-bit registers containing n bits of stored information which are moved forward one bit register upon the acceptance of each new sample to be stored. New samples are fed serially into the array. A conventional shift register shifts the n bits of information simultaneously at the sample rate; however, in the application under consideration here the desired operation is to handle only one bit of information at a time. The forward transfer of all n bits of information is effected by transferring the information in only one bit register at a time beginning with the n^{th} register and successively transferring the information in the $(n-1)^{th}$, the $(n-2)^{th}$, etc. until all n bits have been transferred one position. This latter operation is hereafter called sequential shifting.

[1] E. C. Westerfield, NEL LORAD Summary Report No. 698, Article 27, "Digital Techniques for Rapid Processing of Signals," page VI-35.

This technical memorandum proposes three possible solutions to the problem of instrumenting a sequential shifting register for use in a sequential matched filter.

Bit Register Elements for use in Matched Filters

Although many types of bi-stable storage elements are available for digital shift registers, as far as the outputs are concerned they can be divided into two general groups with the following characteristics:

Group 1 - The output of this group changes from one stable level for a stored "1" to another stable level for a stored "0". In storage devices of this type (i.e. vacuum tube and transistor flip-flops) two outputs are

available which we will call "a" and "b." If a "1" is stored in such a device the "a" output will be at a high level and the "b" at a low level while a stored "0" will reverse this condition and give a low level at "a" and a high level at "b." This is the type output required in matched filter applications.

Group 2 - The output of this group is produced by the transition from one stable state to the other. Thus the output is a pulse during the transition period and no output at all other times. As used in shift registers, the pulse produced by the transition from the "0" to the "1" state is blocked from the output, leaving only an output pulse during the transition from the "1" to the "0" state thereby indicating the transfer of a stored "one".

Storage elements of this type (magnetic cores, ferro-electric cells, etc) thus have only one output available which produces a positive (or negative) pulse for a stored "1". To use this element in a matched filter two shift registers are necessary, one carrying the signal (positive or "1" signal register) and one carrying an inverted signal (negative or "0" signal register). Thus the positive signal register produces a pulse in the output for each "1" in the signal input and the negative signal register produces a pulse in the output for each "0" in the input signal.

Possible Solutions for Sequential Shifting

Type 1 - Double shift register

The most direct solution, however not necessarily the easiest, would be to generate periodic pulses which could be applied in order to the proper one-bit register of the sequential shifting register. Such a pulse generator could be instrumented from a conventional shifting register made to transfer and recirculate a single "1". Upon the transfer of this "1" into a stage of the conventional register a pulse shaping network would produce an output in the form of the pulse necessary to transfer the information in one bit register

of the sequential shifting register. The conventional register would have one stage shifting each stage of the sequential register and thus after the "1" has transferred through the entire conventional register each stage will have pulsed the corresponding stage of the sequential register and all the information will have been transferred forward one place. A recirculation loop restores the "1" to the initial one-bit register and the sequence of pulses is repeated. This system is illustrated in Figure 1 where the conventional register is labeled shift register #1 and the sequential shift register being driven is labeled shift register #2.

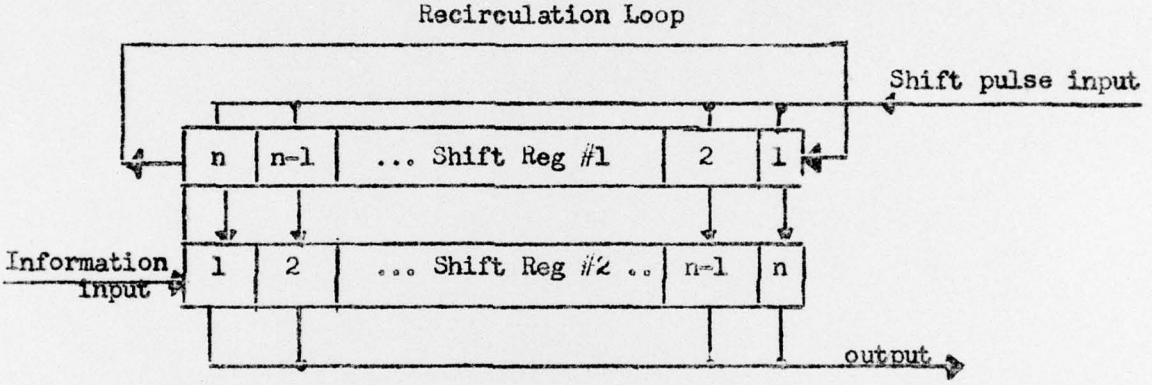

Figure 1

It is apparent from Figure 1 that the "1" circulating in the conventional register transfers in the opposite direction to the desired information flow in the sequential shifting register.

In this type operation the shift pulse repetition rate must be n times the rate at which new information is fed into shift register #2. Thus for an input information rate of 400 bits per second and a 2000 stage shift register, the shift pulse repetition rate must be 800,000 pulses per second.

The disadvantages of this system are that the driving register must be as long as the storage register and the shift pulse repetition rate must be very high.

Type 2 - Conventional Shift Register operated in Series Parallel

Some of the disadvantages of the type 1 sequentially shifted shifting register can be overcome by the mode of operation shown in Figure 2. This system consists of three sets of shift registers, (1) a control register with a recirculating "1", (2) a set of n information storage registers each containing m stages, and (3) a high speed output shift register. All registers are of the conventional simultaneous shift type. The operation of this system can be illustrated as follows: when the "1" in the control register enters stage #1 a pulse is generated and fed to the shift bus of storage register "a" this causes the information in each stage of register "a" to be transferred one stage forward and also into the corresponding stage of the high speed output register. Thus immediately after the 1^{st} shift pulse the 1^{st} to m^{th} bits of information will be in the 1^{st} to m^{th} stages of the high speed output register and the 2^{nd} to m^{th} bits of information will be in the $a_1{}^{th}$ to $a_{m-1}{}^{th}$ stages of shift register a, the $a_m{}^{th}$ stage containing no information.

Before the control register is shifted again the high speed shift register is shifted m times transferring all the information into the output circuit and leaving this register cleared. Between the m^{th} and $(m+1)^{th}$ shift pulses of the high speed shift register, the "1" in the control register is shifted into stage #2 and the pulse generated is applied to the shift bus of register b. All the information in register b is shifted forward one stage and also transferred into the corresponding stages of the output register. In the forward transfer the bit of information in the b_1, stage of register b is transferred into the a_m stage of register a and stage b_m is left with no information. The $(m+1)^{th}$ to $2m^{th}$ shift pulses of the high speed register now shift the information into the output circuits. This process is continued until all the information in the register has been shifted forward one stage

and also into the output circuit via the output register. As the information in register n is shifted forward, a new bit of information is added in stage n_m. The output of the high speed register is a continuous stream of binary information, determined by scanning and reading the condition of each stage of the storage register after a new bit of information has been added to the register.

A type 2 shift register using an input information rate of 400 bits per second and a storage register of 2000 stages could be instrumented with $n = 50$ and $m = 40$ (i.e. 50 shifting registers of 40 stages each). This means that 40 bits of information could be shifted simultaneously and that the 50 sets of 40 bits are shifted in succession. During the interval between the introduction of new bits of information into the storage register all 50 sets must be shifted in succession. This requires 50 pulses in $\frac{1}{400}$ seconds or a shift pulse repetition rate of 20,000 pps on the control register. The high speed output register will require a shift pulse repetition rate m times as high or 800,000 pps. The advantages of this mode of operation are (1) only a relatively short high speed register (40 stages) and only a 50 stage control register are required, and (2) the storage register and control register both operate at relatively low shifting speeds.

Type 2a

Storage registers which have a non-return to zero output for a series of "1s" require some form of steering gates to transfer the information from the desired storage register into the output register. Figure 3 indicates one possible solution to the problem. Each stage of each storage register is coupled to the succeeding stage of its own register and also to the corresponding stage of the high speed output register by identical steering gates.[2]

[2] W. B. Allen and F. J. Smith, NEL LORAD Summary Report No. 698, Article 25, "PseudoRandom Noise Generator (PRNG)," page VI-9.

The shift pulse which is applied to only one of the n storage registers shifts all the information forward one stage in the register and also transfers the information from each stage of that particular storage register into the corresponding stage in the high speed output register. This operation would require that a pulse of short enough duration to properly transfer the information into the high speed register would also shift the low speed register.

Type 2b

If the storage registers are magnetic core or ferro-electric shift registers whose outputs are very short pulses for a stored "1" the steering gate need be only an isolating diode or resistor to prevent interaction between the one-bit registers. If the output pulse length is greater than the interval between shift pulses on the high speed output register, a high speed "and" gate (strobe) will be necessary so that the information can be transferred from the storage registers to the output registers between two consecutive shift pulses of the high speed output registers.

Magnetic Core Matrix Operated as a Sequentially Shifted Shifting Register

Since in a sequentially shifted shifting register the information is handled one bit at a time it seems feasible to use magnetic core matrix memory techniques to store the information. Figure 4 shows a diagram of a core matrix instrumented to operate as a shift register; it consists of two matrices which are identical except for the output signal sense lines. Each matrix has five windings, the two coincidence current read-write lines, the inhibit line, the signal steering sense line and the output sense line. The read-write control circuits are not shown but Chart 1 shows the pulsing sequence of the read-write busses. The information is sampled and feed into the n^{th} stage of each

register and the shifting operation can be seen from the read-write pulse sequence and Figure 4. The new information sample is read into the inhibit amplifiers as the oldest bit of information is being read from core #1 of the matrix. The next write pulse transfers the information from the inhibit amplifier into core n. The second read pulse transfers the information from core #2 to the inhibit amplifier and the second write pulse transfers it into core #1. Thus after n read and n write pulses all of the information has been shifted forward one core in the matrix, (i.e. information bits 2 to (n+1) now occupy cores 1 to n). During this transfer of information each bit of information stored in the cores threaded by the output sense line appears in the output circuit.

As seen in Figure 4, the pattern of the threaded and unthreaded cores in the negative matrix is the inverse of the pattern in the positive matrix and the signal stored in the negative matrix is the inverse of that stored in the positive matrix. Under these conditions if the signal in the positive matrix is coded such that all the threaded cores carry a "1" and the unthreaded cores carry zeros at a given instant, the combined output of the positive and negative matrices will be a continuous stream of n "1s" when the information is shifted one core forward in the register.

For this mode of operation the period of the read-write cycle (for one core) must be less than $\frac{1}{S_r \times n}$ where S_r is the sampling rate and n is the number of cores in the matrix. If the sampling rate is 400 bits per second and the matrix has 2000 cores the read-write cycle must be less than $\frac{1}{400 \times 2 \times 10^3}$ or 1.25 μ second. This is approximately four times faster than presently available cores matrices.

Series-Parallel Operated Matrix Sequential Shift Register

A system for increasing the effective operating speed of the matrix shift register is shown in Figure 5. It consists of a set of m positive signal matrices of n cores each and a set of m negative signal matrices of n cores each, with their associated inhibit amplifiers, signal steering sense lines, output signal lines, and a high speed output shift. Chart 2 and Figure 6 indicate the pulse sequence of the read-write busses and the order in which a bit of information traverses the cores of the positive matrices. The first read pulse transfers the information from the #1 core of the 2^{nd} to m^{th} matrices into the 2^{nd} to m^{th} inhibit amplifiers. Since the signal steering sense line does not pass through the #1 core of matrix #1 it is not sensed, but a new bit of information is fed into the inhibit amplifier #1 through the gate which is opened by the read pulses on busses $a_1 a_1'$. The first write pulse transfers the information from the 2^{nd} to m^{th} inhibit amplifiers into the #1 cores of matrices 1 to (m-1) leaving the first core in the m^{th} matrix empty. At the same time a new bit of information is transferred from inhibit amplifier #1 into the n^{th} core of the m^{th} matrix. The second read pulse transfers the information from the 2^{nd} core in each matrix to the inhibit amplifier. The second write pulse transfers the information from inhibit amplifier #1 into core #1 of matrix #m and from inhibit amplifiers 2 to m into the #2 cores of matrices #1 to (m-1). This leaves the 2^{nd} core in matrix m empty. After n complete read-write pulse cycles all the information will be advanced one core forward in the array of matrices and core n of matrix m will be empty and ready to receive a new sample.

Each time a set of information bits is transferred from the core matrices to the inhibit amplifiers, the same information is transferred to the high speed output shift register by means of the output signal sense lines. Part of this information will be from the positive signal matrices and part of it

from the negative signal matrices, depending on which cores in each set of matrices are threaded by the output sense line. Between each read-write cycle the information in the high speed shift register is transferred to the output circuit. Thus during n read-write cycles the output of the high speed shift register will be a continuous stream of binary information, each bit of information being determined by the state of the respective cores (l_1-n_m) and the pattern by which the output sense lines thread the cores.

Circuitry of this system is more complex than the single matrix mode of operation but the maximum possible information rate is much higher since m bits of information are being advanced simultaneously. For an input information rate of 400 bits per second and $n = 200$, $m = 10$ (2000 bits of storage) a read-write period is $\frac{1}{200 \times 400} = \frac{1}{80000} = 12.5$ μsec. The read-write cycle can be m times as long with this mode of operation and still retain the same input information rate.

Chart #1 - Read-Write Pulse Sequence for Core Matrix Shift Register

Read Operation	Pulse Busses	Write Operation	Pulse Busses
1	a_1, a_1', a_2, a_2'	1	n_1, n_1', n_2, n_2'
2	b_1, b_1', b_2, b_2'	2	a_1, a_1', a_2, a_2'
3	c_1, c_1', c_2, c_2'	3	b_1, b_1', b_2, b_2'
4	d_1, d_1', d_2, d_2'	4	c_1, c_1', c_2, c_2'
5	e_1, e_1', e_2, e_2'	5	d_1, d_1', d_2, d_2'
◦	◦	◦	◦
◦	◦	◦	◦
◦	◦	◦	◦
◦	◦	◦	◦
n	n_1, n_1', n_2, n_2'	n	$n_1-1, n_1'-1, n_2-1, n_2'-1$

Chart #2 - Read-Write Pulsing Sequence for Multiple Plane Core Matrix Shift Register

Read Operation	Pulse Busses	Write Operation	Pulse Busses
1	$a_1, a_1', a_2, a_2', \ldots\ldots a_m, a_m'$	1	$a_1, a_1', a_2, a_2', \ldots\ldots a_{m-1}, a'_{m-1}, n_m, n'_m$
2	$b_1, b_1', b_2, b_2', \ldots\ldots b_m, b_m'$	2	$b_1, b_1', b_2, b_2', \ldots\ldots b_{m-1}, b'_{m-1}, a_m, a'_m$
3	$c_1, c_1', c_2, c_2', \ldots\ldots c_m, c_m'$	3	$c_1, c_1', c_2, c_2', \ldots\ldots c_{m-1}, c'_{m-1}, b_m, b'_m$
◦	◦	◦	◦
◦	◦	◦	◦
◦	◦	◦	◦
◦	◦	◦	◦
◦	◦	◦	◦
n	$n_1, n_1', n_2, n_2', \ldots\ldots n_m, n_m'$	n	$n_1, n_1', n_2, n_2', \ldots\ldots n_{m-1}, n'_{m-1}, (n-1)_m, (n-1)'_m$

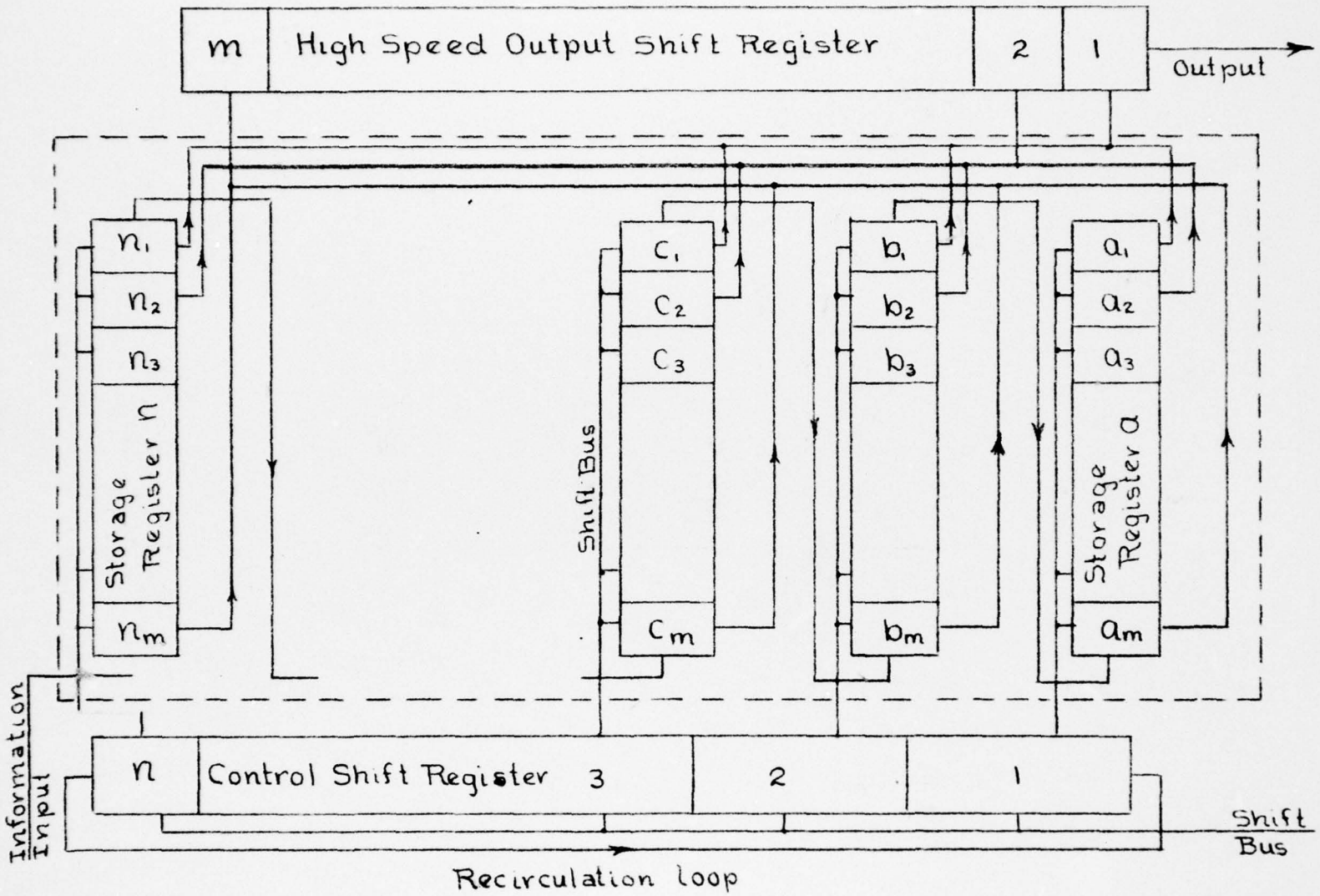

FIG 2 Sequentially Shifted Shifting Register Type 2 Series-Parallel

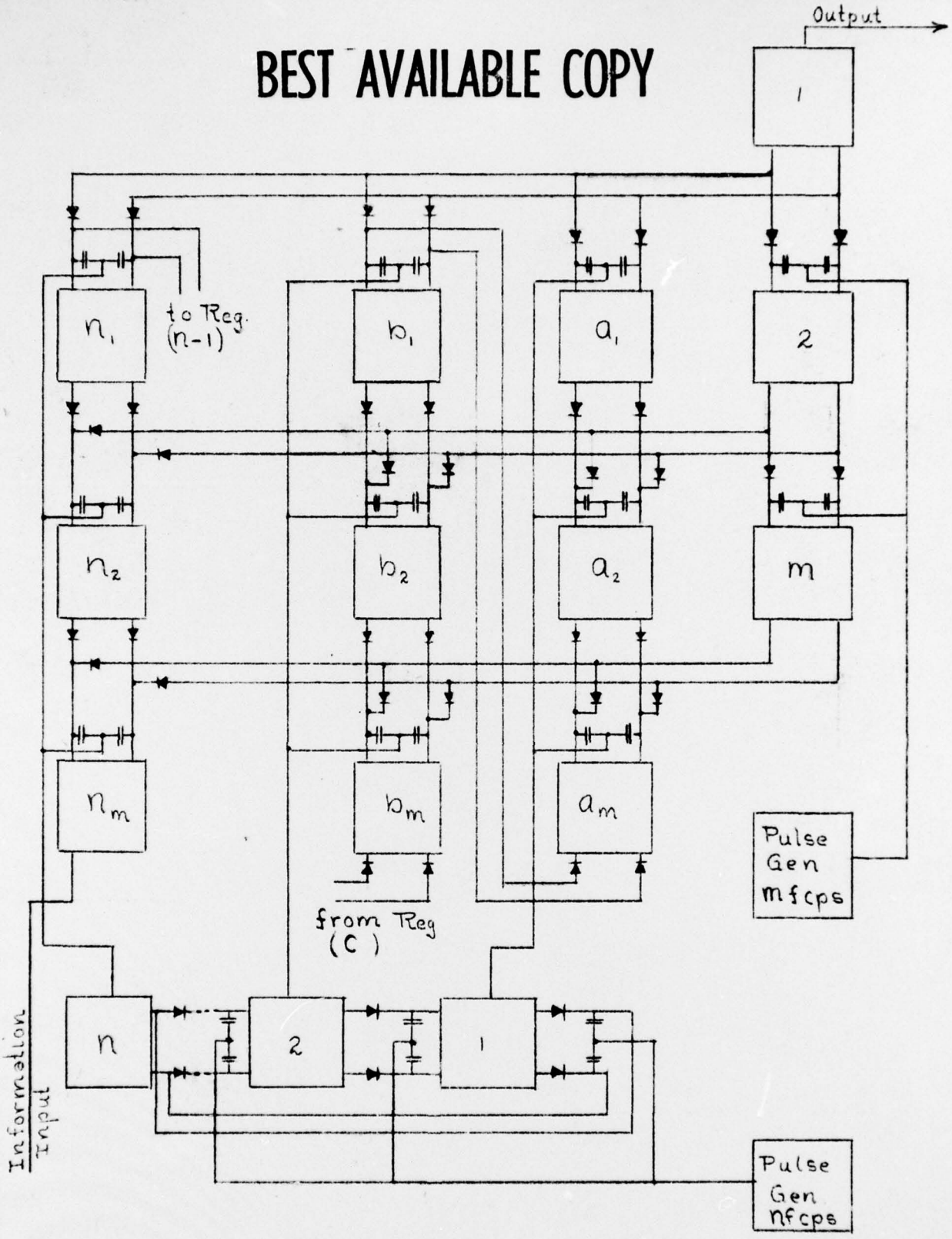

FIG 3 Transfer gates between storage and output registers

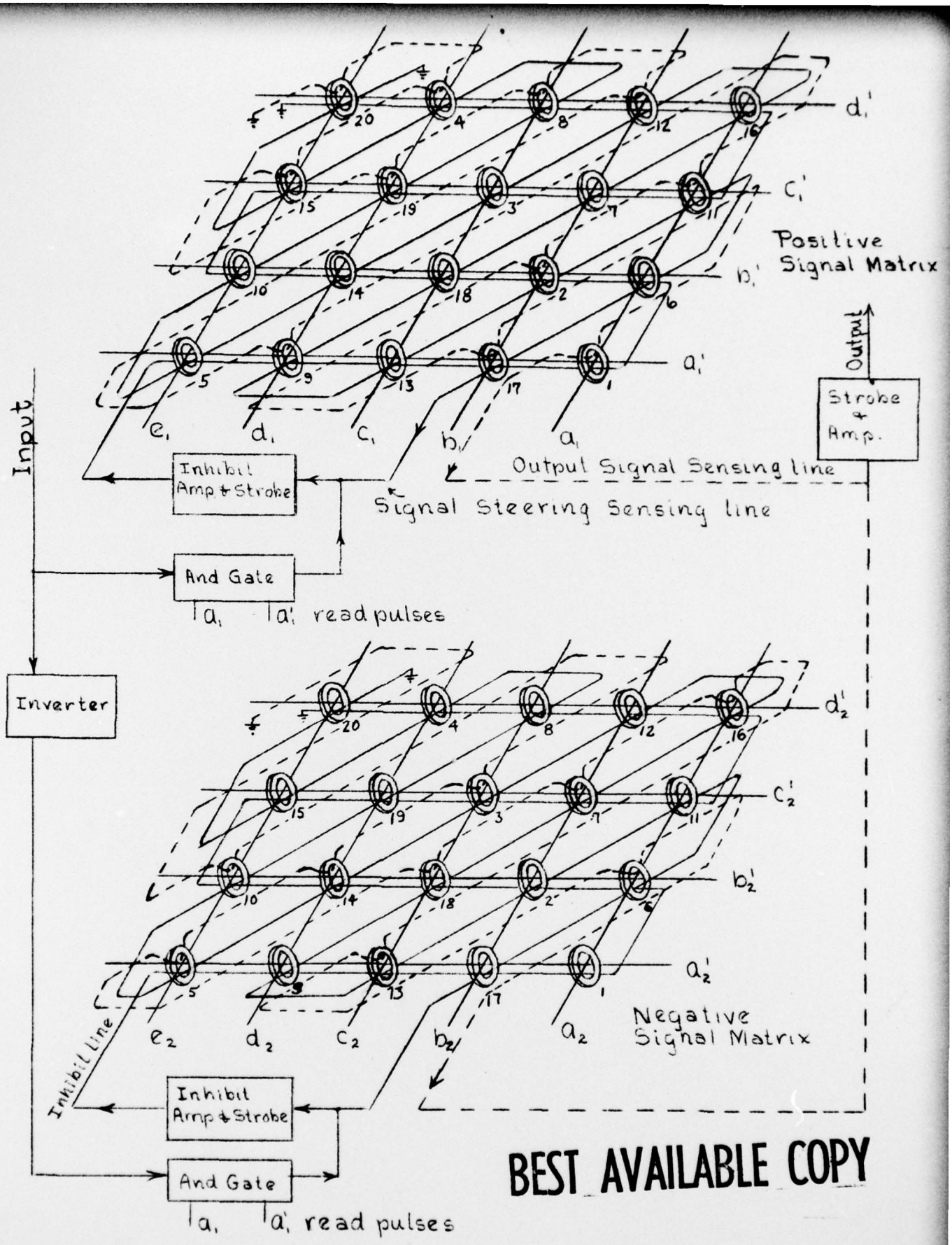

FIG 4 Core matrix shift register single plane positive and negative signal matrix

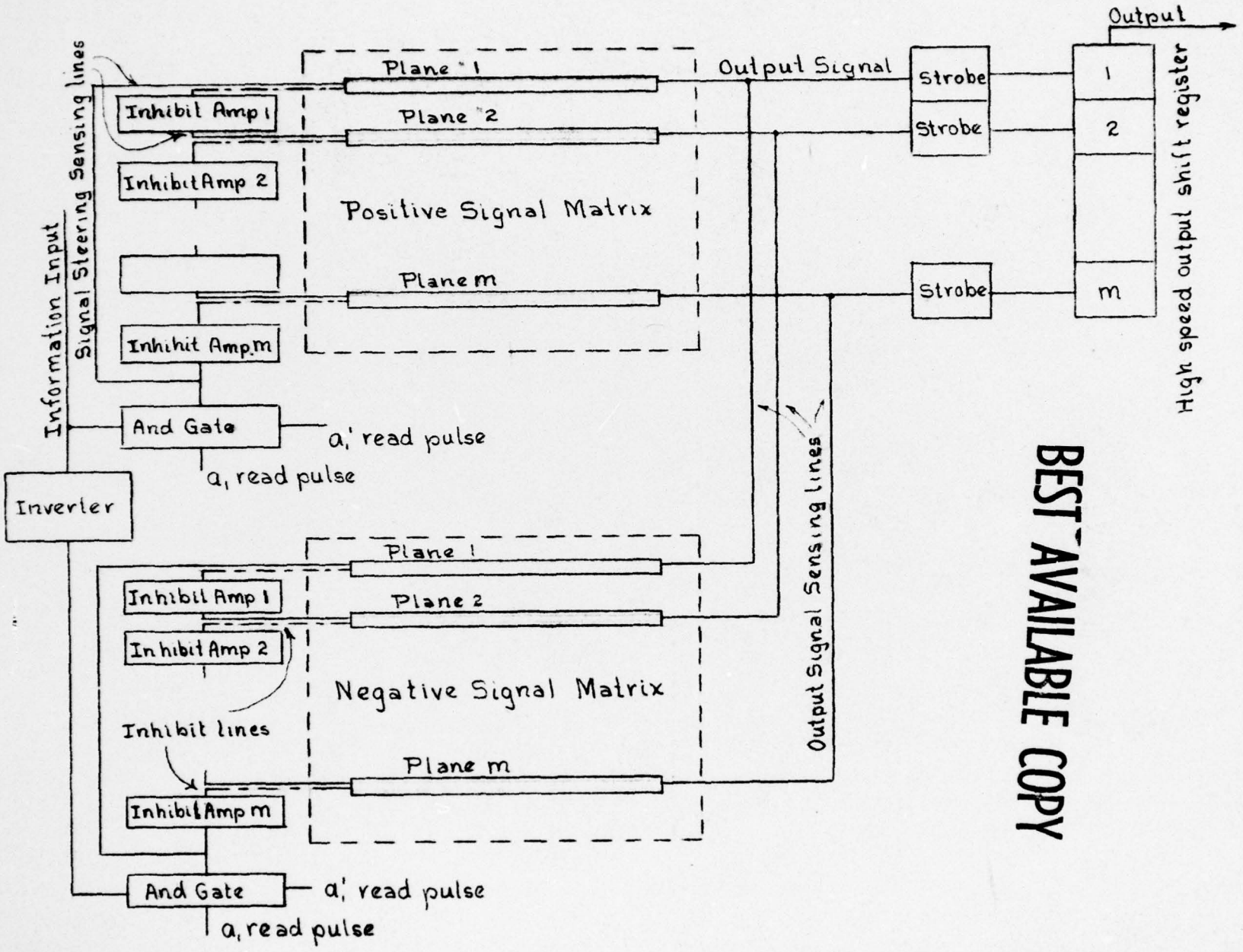

FIG 5 Block diagram of series-parallel core matrix shift Register

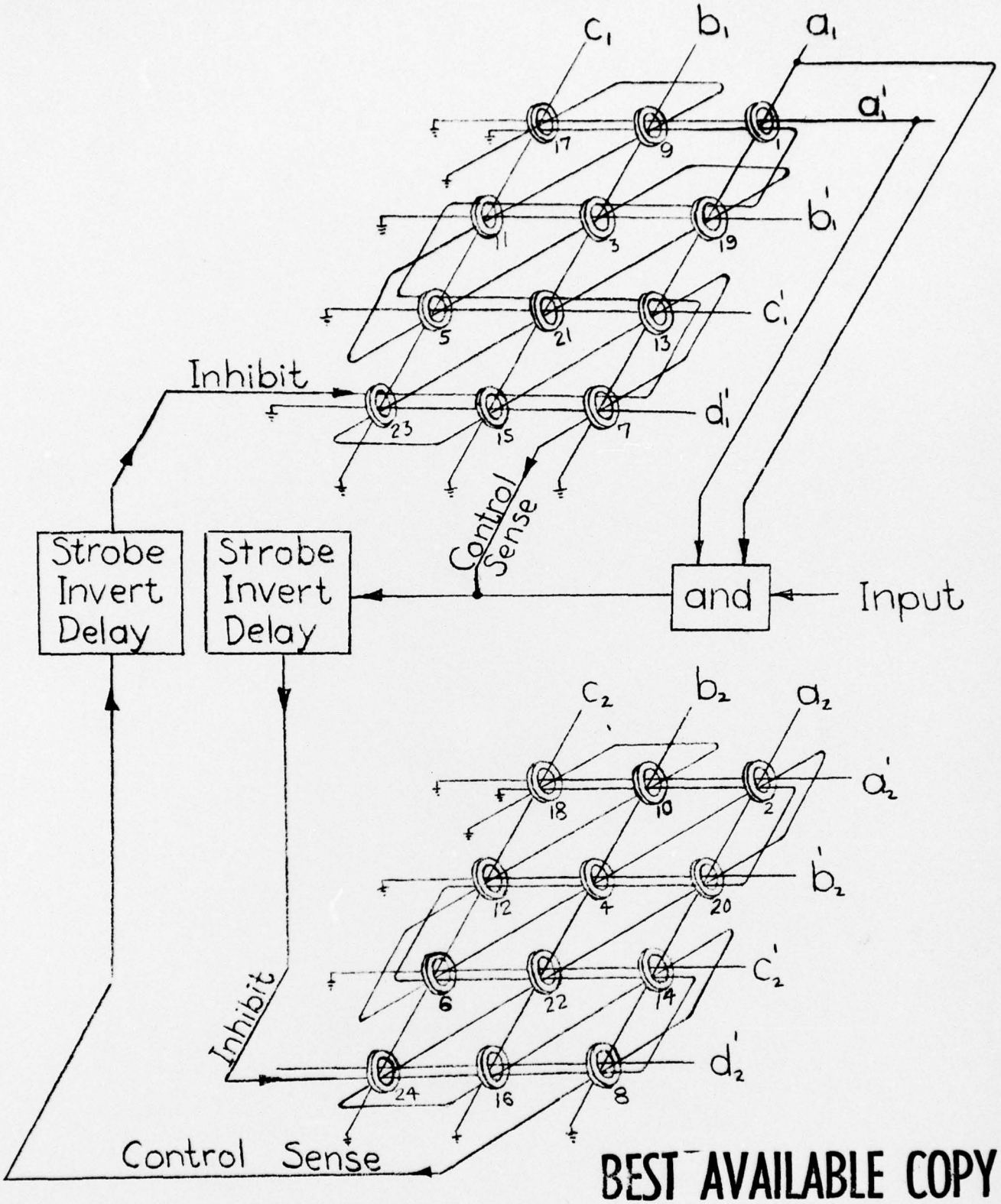

FIG 6 Two planes of multiple plane core matrix shift register showing one possible information path.