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In-House Report
February 1978

DIGITAL SMOOTHING BUFFER

David L. Wortley, 1Lt, USAF

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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Asynchronous time division multiplexers (ATDM's) typically produce large phase excursions as a result of bit stuffing operations. Analog phase locked loops (PLL) are normally employed to smooth these excursions to levels which can be accepted by various sink equipments. For ATDM's which cover a broad range of rates, such as the AN/GSC-24, it is difficult to provide a high level of smoothing across the entire range due to noise and frequency limitations. This project investigated a digital PLL as a potential technique for circumventing

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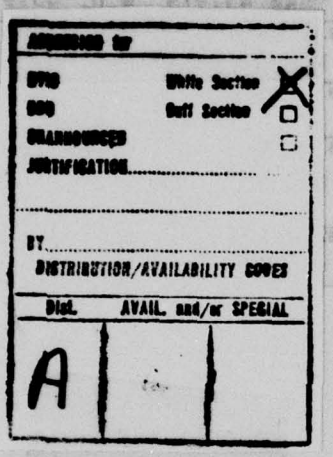
the analog limitations.

A digitally implemented PLL has the potential of providing extended smoothing across a broad range of rates as smoothing becomes a function of the number of stages of circuitry implemented.

The constraints on the project were to determine if a digital second order PLL could be implemented on an AN/GSC-24 size circuit card which would be capable of providing a slew rate of less than 2π radians over a 20,000 bit interval. It was determined that this slew rate goal could be reached over a wide range of data rates but high frequency phase jitter and size limitation have made it undesirable for AN/GSC-24 use.



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Preface

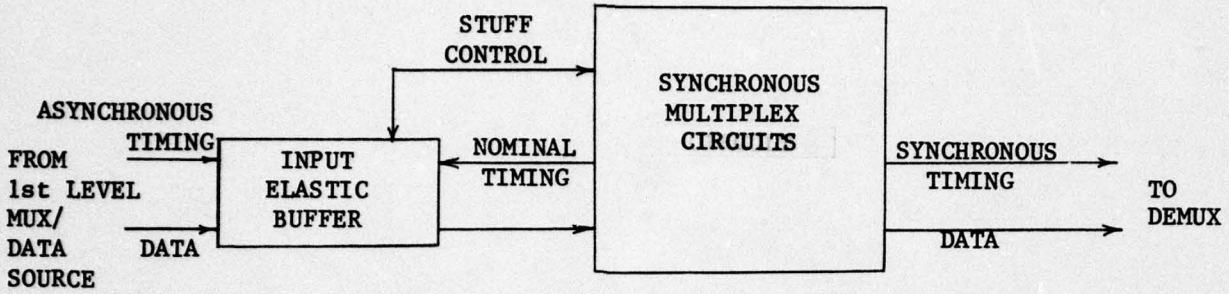
Equipment design and evaluations described in this report were accomplished under Job Order Number 45191911. This work was done in conjunction with the Asynchronous Time Division Multiplexer, AN/GSC-24(V), Project 11490201.

The author wishes to extend his appreciation to Jefferson Love and Dr. Mark Levi for their valuable assistance during this effort.

1. Introduction

The Defense Communications System is currently undergoing a transition from analog to synchronous digital transmission techniques. During this interval hybrid system elements are required to bridge the two technologies. One such element is the Asynchronous Time Division Multiplexer (ATDM). This second level multiplex unit typically combines the outputs of individually timed first level PCM multiplexers into a single synchronous Mission Bit Stream. A standard commercial technique for producing this synchronous conversion is to sample the incoming bit stream at a rate higher than the maximum rate of the input channels. Dummy "stuff" bits are inserted as required to make up the difference in rates. These stuff bits are deleted at the demultiplex side leaving "holes" in the data stream. Another technique, used in the AN/GSC-24(V), is to sample all incoming channels at their nominal rate, then send rate corrections over a separate overhead channel. When the incoming rate is below nominal, selected incoming bits are sampled twice. The overhead channel then carries this information to the demultiplexer where the redundant bit is deleted from the bit stream, leaving a one bit gap. Incoming data rates above the nominal are handled by sending the "extra" bits through the overhead channel to the demultiplexer where they are inserted into the bit stream, causing two bits to occupy one nominal bit time. Both techniques require use of a smoothing buffer to reduce the resulting 2π phase discontinuities to phase slew rates which can be accepted by the first level multiplexers or other sink equipments (primarily modems). Figure 1.1 shows a conceptualized view of an ATDM.

The effects of stuffing depend on the type of device attached at the demultiplexer output. Any device which consists strictly of logic clocked by



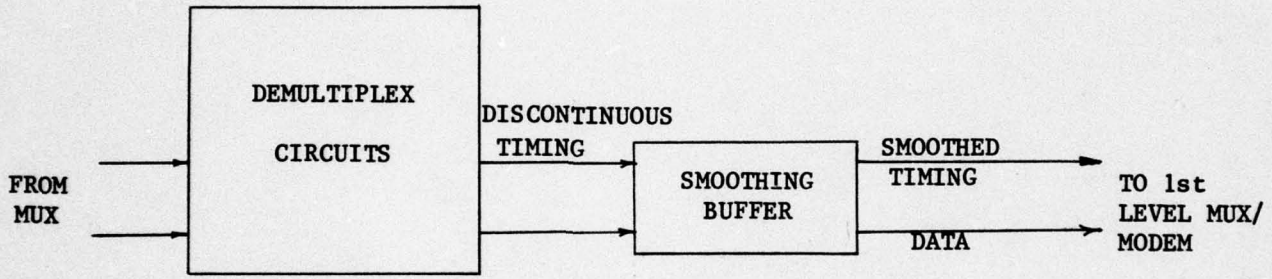


Figure 1.1

Conceptual Diagram of an ATDM

the demux output clock will not have any direct degradation as it simply uses the clock and passes it on to the device at its output. Devices which do show degradation contain some type of timing recovery or tracking circuits as these circuits typically cannot follow the ATDM output phase slew rates. Common devices include modems or those 1st level PCM multiplexers which accept and rate convert digital inputs (TD-968, TD-1192). Two types of degradations occur, degradation in performance for a specified channel Eb/No for modems or increased probability of loss of bit count integrity (BCI) for all devices. A determination of how sensitive a given device is to these output slew rates is not a well known parameter as equipments designed to date have not been placed in these environments. It should be noted that device which simply passes the demultiplexer clock on through should also pass the potential problems to the next lower level of equipments.

It is the function of the smoothing buffer to reduce the phase discontinuous clock from the demultiplexing circuitry into a phase continuous output clock which has a low phase slew rate. In general slew rates are expressed as radians/second or radians per bit, but in this application, since all input phase steps are one bit, a full 2π, it is more convenient to express them in the form, 2π/bit times. Thus, if the smoothing buffer integrates the phase step over 10,000 bit times this would be represented as a slew rate of 2π/10,000 bits.

ERROR RATE VS. Eb/No

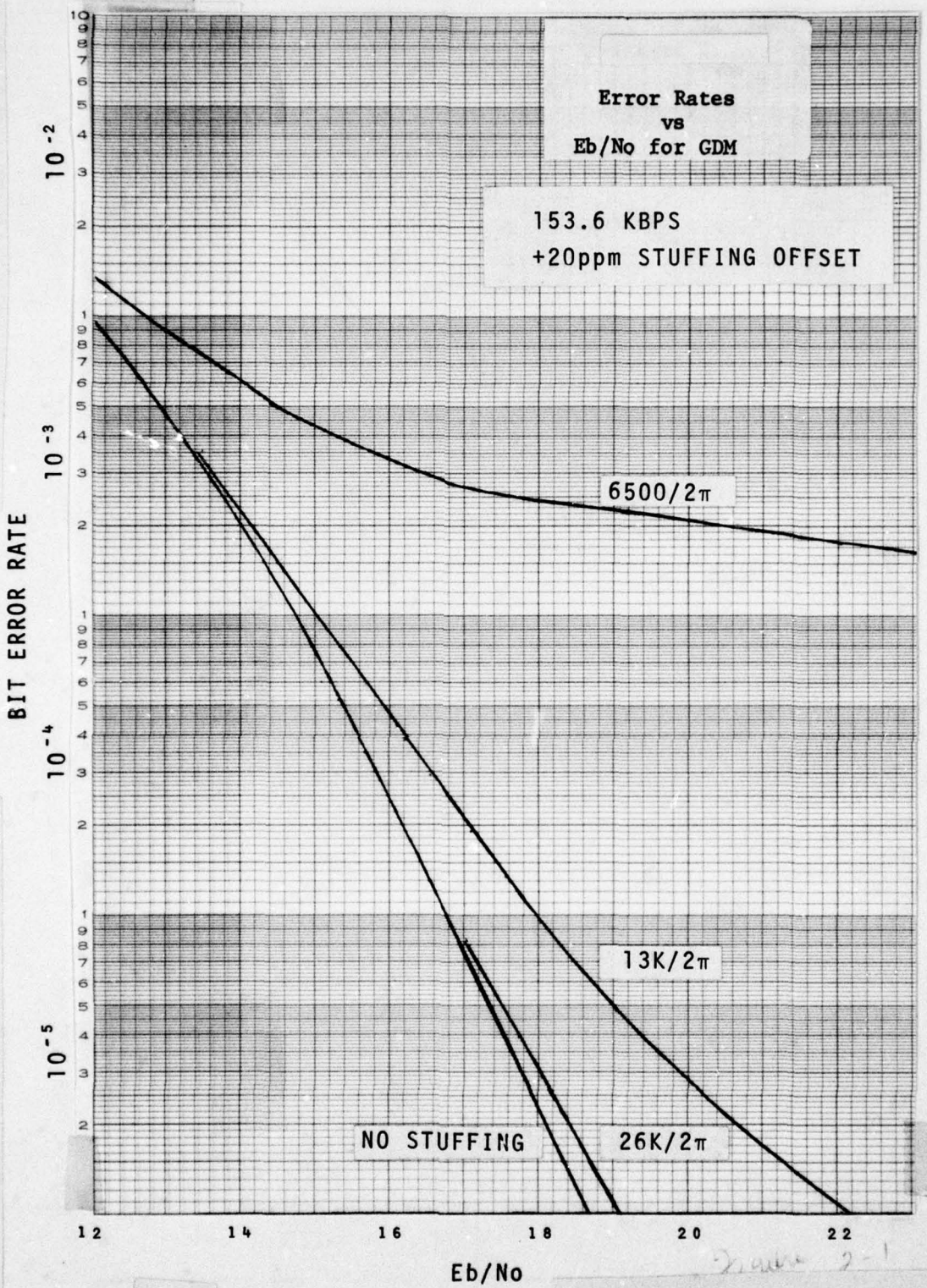


Figure 2.1

2. The AN/GSC-24(V) and the AN/USC-26

The prototype AN/GSC-24(V) ATDM had considerable difficulty interfacing with several channel side equipments. This resulted from the pulse stuffing techniques used to allow asynchronous operation and the smoothing technique selected. The output slew rates were too high for some equipments to accept. As a result the smoothing buffer design was changed in the production version, yet one prime equipment was found which still could not properly interoperate, the AN/USC-26, Group Data Modem (GDM). Its timing recovery phase locked loop has a very tight bandwidth, near 20 Hz. This severely limited its ability to accept large slew rates. Figure 2.1 shows the effect of various slew rates on the GDM.

Further redesign of the ATDM analog smoothing buffer did not appear a feasible alternative as this design had reached its practical limit. A general diagram of the ATDM loop is shown in Figure 2.2. The ATDM smoothing

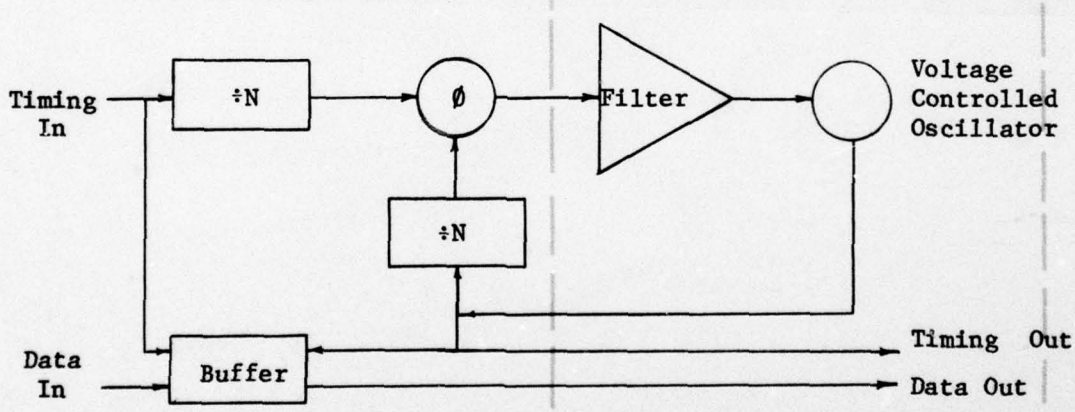


Figure 2.2

ATDM Analog Smoothing Buffer

loop is required to operate on channel rates from 45 b/s to 3 Mb/s. This was divided into 16 ranges where the highest rate in the range is twice the lowest. To obtain this spread in each range the smoothing capability became limited. One of the main tradeoffs was high frequency jitter vs slew rate. Adjusting the loop gain and bandwidth parameters could improve the slew rate but only at the expense of increasing high frequency jitter caused by coupling with adjacent circuitry. No reasonable compromise could be found. Figure 2.3 shows the calculated slew rates output by the ATDM at various rates. A review of Figure 2.1 with the GDM at 153.6 Kb/s shows that the ATDM smoothing would require a factor of five improvement to provide adequate smoothing. Due to time constraints a special purpose smoothing buffer was built for the ATDM-GDM interface which could only operate at the GDM data rates. However, another technique was found which had potential for providing improved smoothing at all ATDM data rates. This technique was a direct digital implementation of a second order analog phase locked loop. It was being implemented in the AN/USC-28, Viterbi Encoded Modem, by Dr. Wong of the Magnavox Research Lab. Only the block diagram and brief notes were available but this was sufficient to design and build a prototype for evaluation.

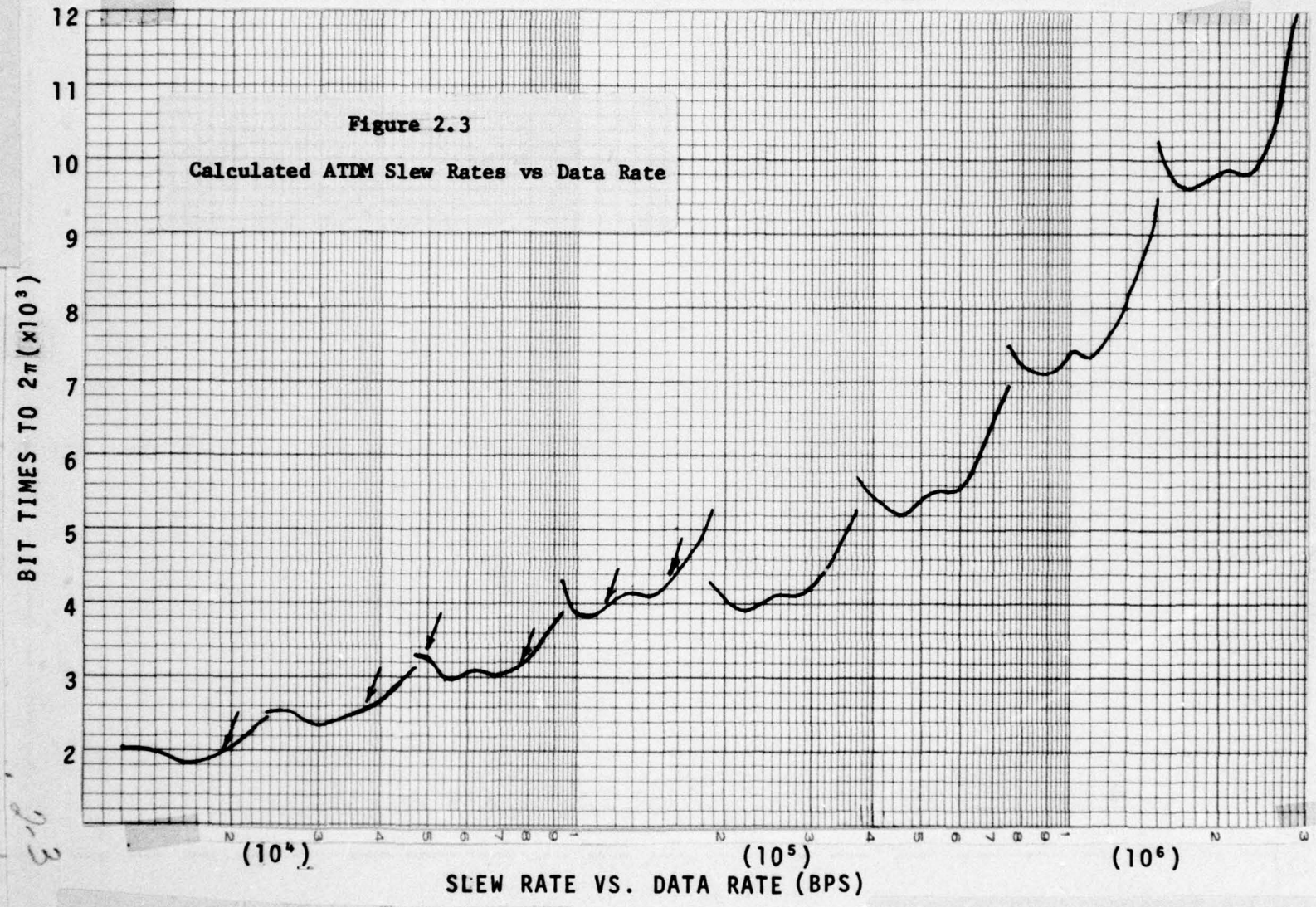


Figure 2.3

Calculated ATDM Slew Rates vs Data Rate

3. Purpose

This project was undertaken to determine the suitability of using a direct digital implementation of a second order phase locked loop to smooth phase excursions produced by the AN/GSC-24(V) demultiplexer. The goal was to determine if smoothing levels could be achieved which would allow interoperation of the ATDM and the AN/GSC-26 modem. To be practical for implementation in the ATDM the smoothing buffer had to be capable of fitting on ½ a standard ATDM circuit card.

4. Digital Smoothing Buffer (DSB) Operation

The purpose of the DSB is to reduce the large phase steps coming from the demultiplexer destuffing actions into phase slew rates acceptable to end equipments. The DSB is built around a direct implementation of a second order analog phase locked loop as shown in Figure 2.1. Figure 4.1 illustrates the major sections of the DSB. Both the analog and digital loops employ phase detectors, filters and a variable oscillator. In the digital design both the filter and variable oscillator functions are divided into separate frequency and phase control sections. The filtering is performed by up/down counters which effectively integrate the output of the phase detector. These counters operate independently. When they overflow or underflow the rate multiplier or incremental phase multiplier is updated. The multipliers respond by increasing or decreasing their output by one step. For the rate multiplier the step is:

$$\pm \frac{1}{2^R \text{ bits/sec}}$$

where R is the multiplier length in stages.

The phase multiplier step is

$$\pm \frac{1}{2^P} \text{ bits}$$

where P is the multiplier length in stages.

The phase detector functions by monitoring the fill level of the data buffer. It is gated at N-bit intervals to indicate whether the buffer is above or below half full. If above half full the U/D counters are incremented. When they overflow the output frequency will be increased by one step and/or the phase advanced by one step. If the buffer is less than half full the counters are decremented. The phase multipler is a divide-by-n counter. When a phase advance or retard is required it divides by n-1 or n+1. Therefore, the phase multiplier further divides the output rate of the rate multiplier. The actual output rate of the DSB is then:

$$f_o = \left(\frac{\text{master}}{\text{clock}}\right) \times \frac{1}{2^S} \times \frac{r}{2^R} \times \frac{1}{2^P}$$

where r is constrained between $\frac{R}{2}$ - R.

The Digital Smoothing Buffer (DSB) concept has many potential advantages over its analog counterpart. The basic advantage is freedom from concern about data rate over a wide range. In an analog based smoothing buffer each change in frequency range requires a different set of filter components. As the VCO is also analog several component substitutions must be made over a range equal to that of the ATDM. A DSB is immune to these problems as its actions depend on the number of clock transitions, not the rate of transition. The smoothing characteristics in one range of rates will then be identical with all other ranges (assuming all ranges are related by an integer multiple). The DSB limitation comes from the maximum master clock rate that can be input

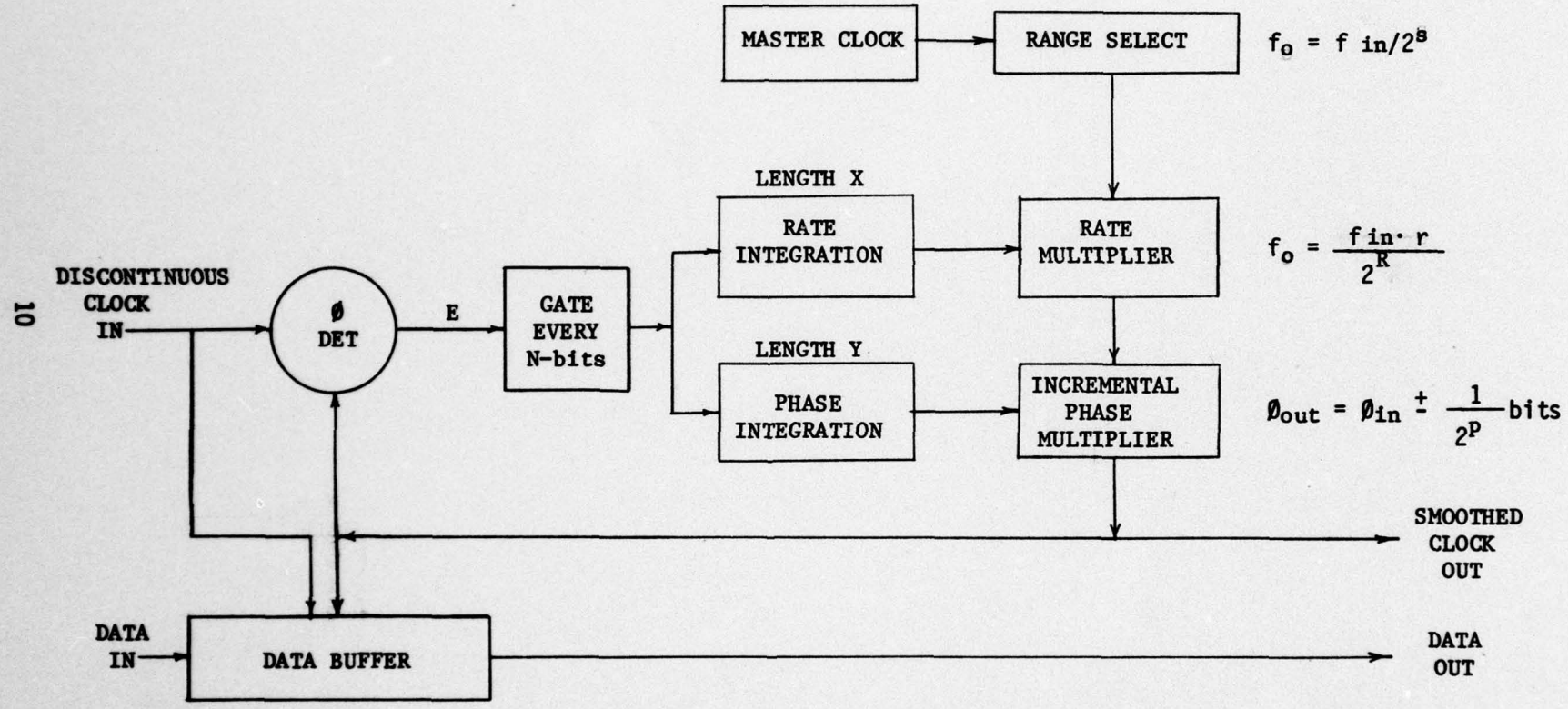


Figure 4.1

Block Diagram of the DSB

to the rate multiplier. To obtain desirable small IPM corrections of 1/24th bit would require a master clock frequency 24 times the highest data rate.

A complete list of specifications for the DSB are included in Appendix A.

5. Program Progression

This project proceeded in two phases. The first phase required development of a computer simulation of the DSB in order to determine the required capabilities and strapping options which must be provided in the hardware. Completion of this phase allowed design of the hardware to begin. The second phase involved checking out the hardware and verifying its performance with an ATDM stuffing simulator designed for this task. The tests were then conducted with the combination of the ADTM, DSB and the GDM.

6. Test Results

The Group Data Modem was tested with the ATDM and the DSB as shown in the Figure below:

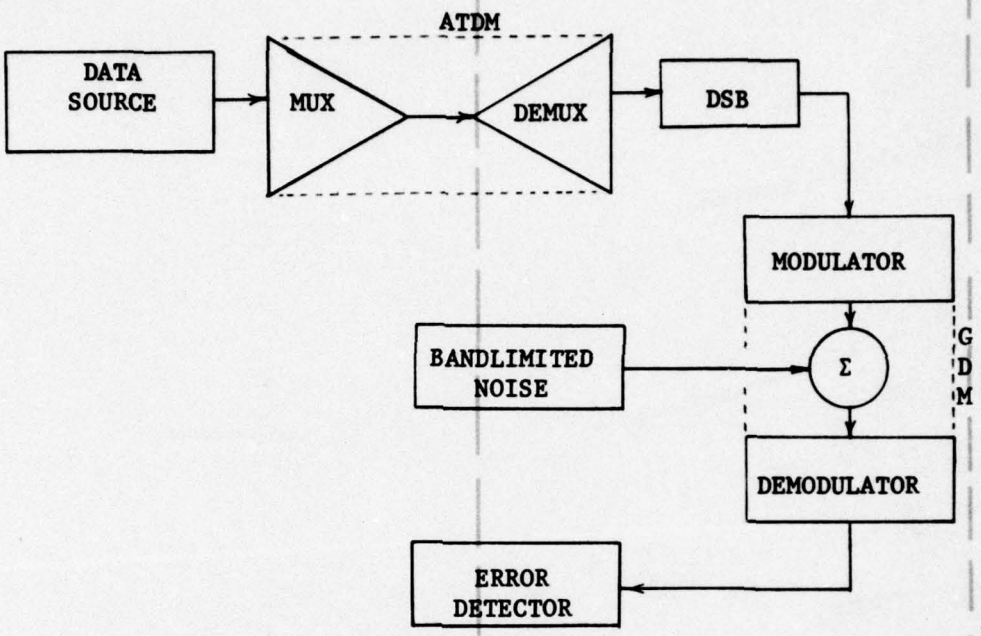


Figure 6.1

ATDM/GDM/DSB Test Configuration

Time for testing with the GDM was very limited. For this reason only the worst case rate of 153.6 Kb/s was examined. Various smoothing levels were tested to determine at what point smoothing would be adequate. The effective degradation is shown in Table 6.1. The reference error rate was taken at 1×10^{-6} errors per bit (approx 18dB Eb/No).

SMOOTHING (Bit Times/2π)	IPM CORRECTION (BITS)	EFFECTIVE GDM DEGRADATION (dB From Back-to-Back)
14,000	1/12	3.0
14,000	1/12	7.0*
20,000	1/20	1.6
25,000	1/28	1.0
31,000	1/36	0.5
31,000	1/36	1.4*
38,000	1/44	0.2
38,000	1/44	1.4*

NOTE: IPM U/D = 4 stages, RM U/D = 8 stages
RM = 18 stages, Samp Int = 1 in 64

Table 6.1

GDM Degradation

*Timing derived from timing mode on GDM. The GDM can either accept the incoming timing or regenerate timing from the incoming data. These figures indicate considerable smoothing is being gained in the regenerate timing from data mode.

It should be noted here that the special ATDM smoothing buffer designed for the GDM produces smoothing to a degradation less than 0.2 dB with a slew rate of 2π in 25,000 bit times. The difference between the two techniques appears to come from the jitter caused by the RM and IPM. The repetition rate of the phase corrections is dependent on the number of stages in the IPM U/D counter and the IPM size. For the rates shown above this repetition rate is in the range of 20 to 100 Hz placing much of this energy within the passband of the modem loop. As these frequencies are directly passed through the modulator side of the GDM it could severely affect the timing recovery/baud

sampling circuitry in the demodulator. Jitter is also generated by the RM. It operates by gating out clock pulses to form a subfrequency of the incoming rate. For example, setting the RM for the ratio 12/16 would give 12 pulses out for every 16 in. The 12 pulses would be the same length as the input pulses but every third pulse would have been deleted. As the ratio changes this pattern and all the subharmonic frequencies would change. For the GDM these components would be over 60 dB down due to the ratio of the data rate to its loop bandwidth, but for some wideband loops the RM jitter could also make a significant contribution. A sensitivity to selected rate offsets was seen in the GDM. These probably resulted from the changing pattern of subharmonics generated by the IPM. Although not serious they do produce slightly more degradation at some offsets.

It should be noted that all the degradations shown resulted even with the combination of the DSB and the normal ATDM smoothing buffer. At this data rate the ATDM buffer smoothes to a level of 3-4000 bits/2π. If this prior smoothing had not taken place, the results above would not have been as good.

7. Summary and Conclusions

The goals of this investigation were to determine the desirability of using this technique as a future enhancement to the ATDM. Several results weigh heavily against this. Performance of the DSB seems severely limited due to the high jitter content of its output. Also it was required to use an IPM setting of 1/44th bit to obtain acceptable smoothing levels. This would dictate a master oscillator frequency of 132 MHz to produce similar smoothing at the 3 Mb/s high limit of the ATDM. Although this could be implemented in ECL logic, the special voltages required are not present in the ATDM to support it nor does this appear desirable in any event. The required integrated circuit count also precludes its implementation. A minimum of 30 integrated circuits would be required without including any provision to initialize the DSB to the correct operating rate.

These factors preclude its use in the ATDM but not its use as a stand alone unit. The potential suitability still exists for low speed data rates where further stages of dividers can be added to reduce jitter or where ECL logic can be used to extend the master clock frequency limitation.

Appendix A

Digital Smoothing Buffer Specifications

Maximum Smoothing: 2π in 85,000 bit times

(Samp Int = 127, IPM U/D = 4 stages, RM U/P = 8 stages
RM = 18 stages, 10% overshoot to 2π step input)

Rate Multiplier:

Minimum Frequency Step : 4 ppm

Length: 18 stages

Up/Down Counter: 0-8 stages

Maximum Clock Input: 19 MHz

Incremental Phase Multiplier:

Phase Step: 1/12, 1/20, 1/28, ... 1/68

Up/Down Counter: 0-8 stages

Sample Interval: 1-127 output clock intervals

Buffer:

Length: 16 bits

Auto-resets to 8 bit level

Initialization:

Manual: 1-262,144 possible start points

Ranges: 12 ranges (2:1 frequency)

Monitors:

D/A Converters: Buffer Level
RM Setting (r)

In Clock

Out Clock

Out Data

Master Clock

Inputs:

Clock/Data: 75 Ω bal, ± 0-3 v

Ext Master Clock: 75 Ω unbal, 0-3 v

Outputs:

Clock/Data: 75 Ω unbal, ± 2 v

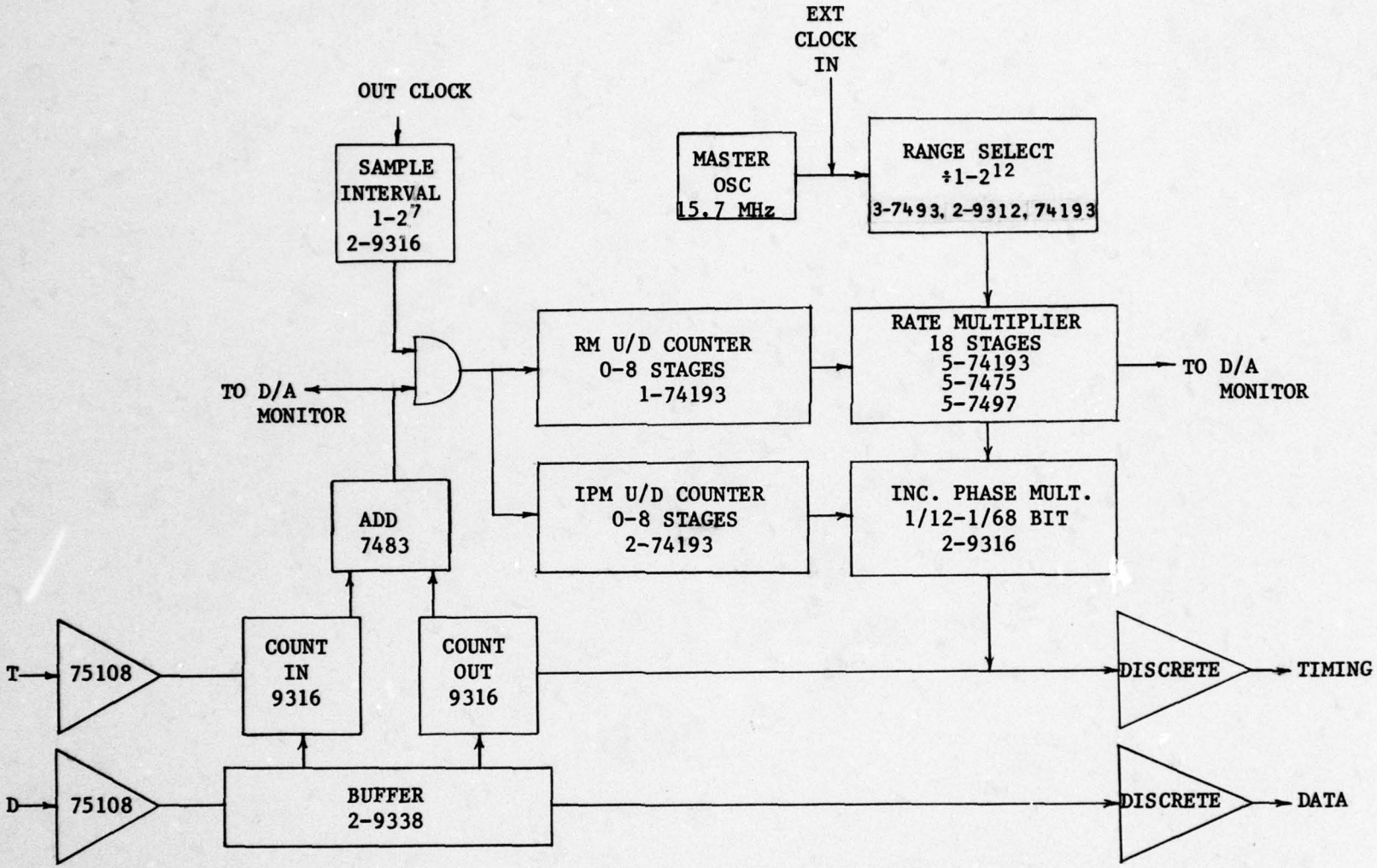


Figure A-1

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