AD-A051 740 AEROSPACE RESEARCH INC BOSTON MASS F/G 17/5
PASSIVE INFRARED MOTION SENSOR (PIMS) (PRELIMINARY). OPERATION --ETC(U)
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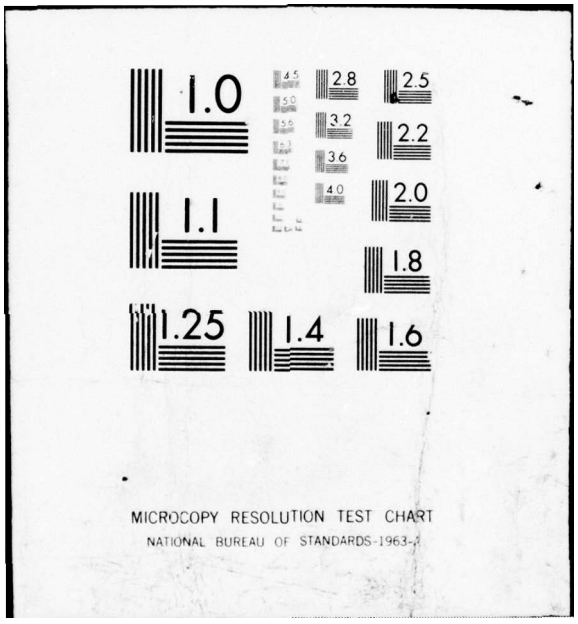
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OPERATION AND

MAINTENANCE MANUAL

PASSIVE INFRARED MOTION SENSOR

(PIMS)

(PRELIMINARY)

Operation and Maintenance Manual.

Prepared for:

Department of the Army
U.S. Army Mobility Equipment Research and Development Center
Ft. Belvoir, Virginia 22060

Contract DAAG53-76-C-0158

Aerospace Research, Inc.
130 Lincoln Street
Boston (Brighton), Massachusetts 02135

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009 900 JOB

1.0 THEORY OF OPERATION

General

Figures 1 and 2 are simplified block diagrams of the Passive Infrared Motion Sensor (PIMS). Figure 3 shows the location of the 17 beams of coverage within the 20 ft. x 30 ft. specified area when the optics are mounted at 7 ft. 4 inches. The system is a motion detector using transient changes in the infrared background, within specified velocities, to generate alarms. A long term infrared source would eventually blend into the overall noise background and not be detected indefinitely. A filter is used to prevent visable light from generating alarms.

Since infrared detection is passive any number of units can be placed in a particular location without interference.

Infrared detection becomes less sensitive when the background temperature approaches that of the target (human intruder).

Some care must be taken upon installation that clutter such as rapidly heating pipes, windows or air ducts are not located within one or more beams.

Due to the long time constants involved in processing frequencies around .1 Hz, it is necessary to allow a 5 minute warmup before alarms can be considered genuine.

Acq Unit R78-0271

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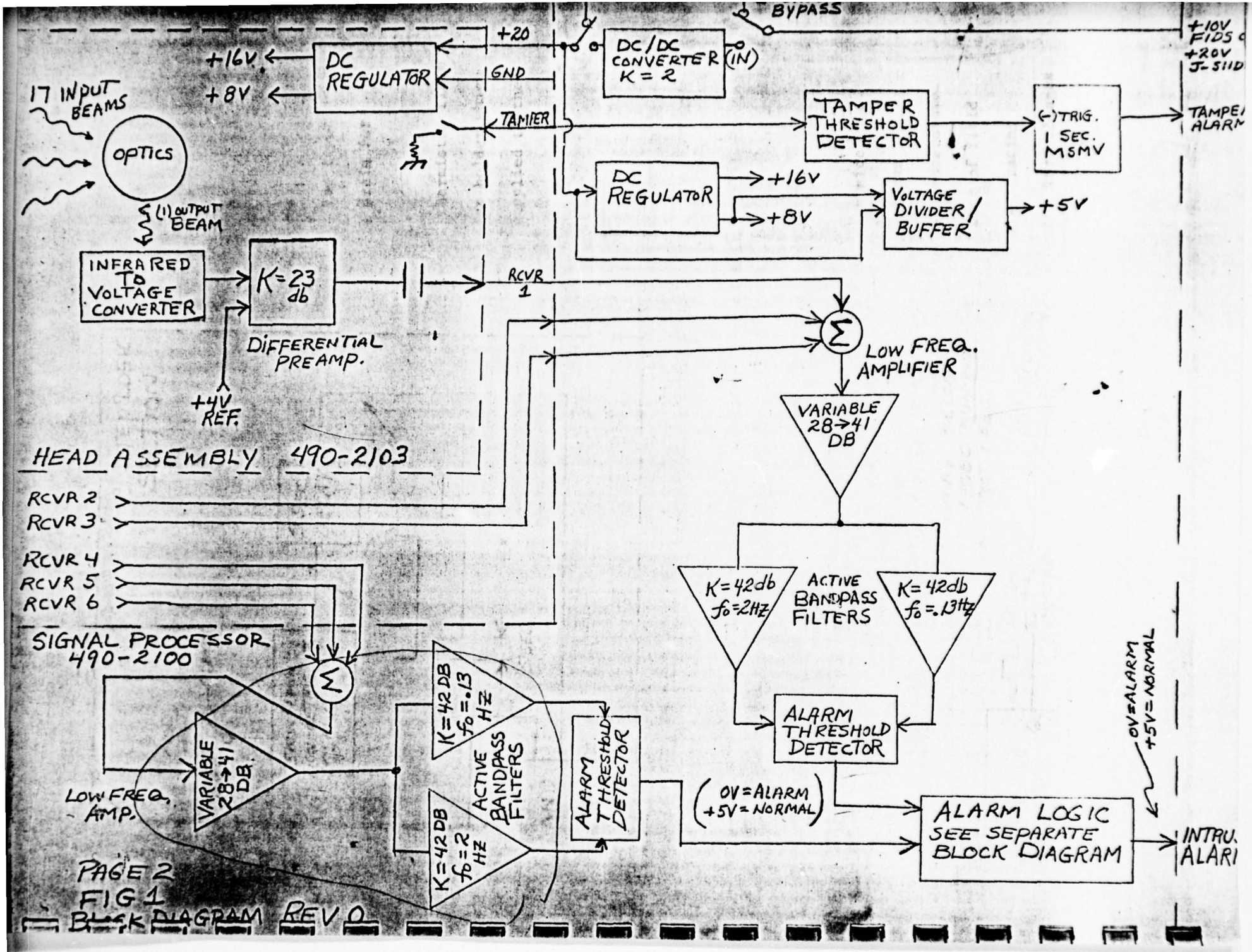
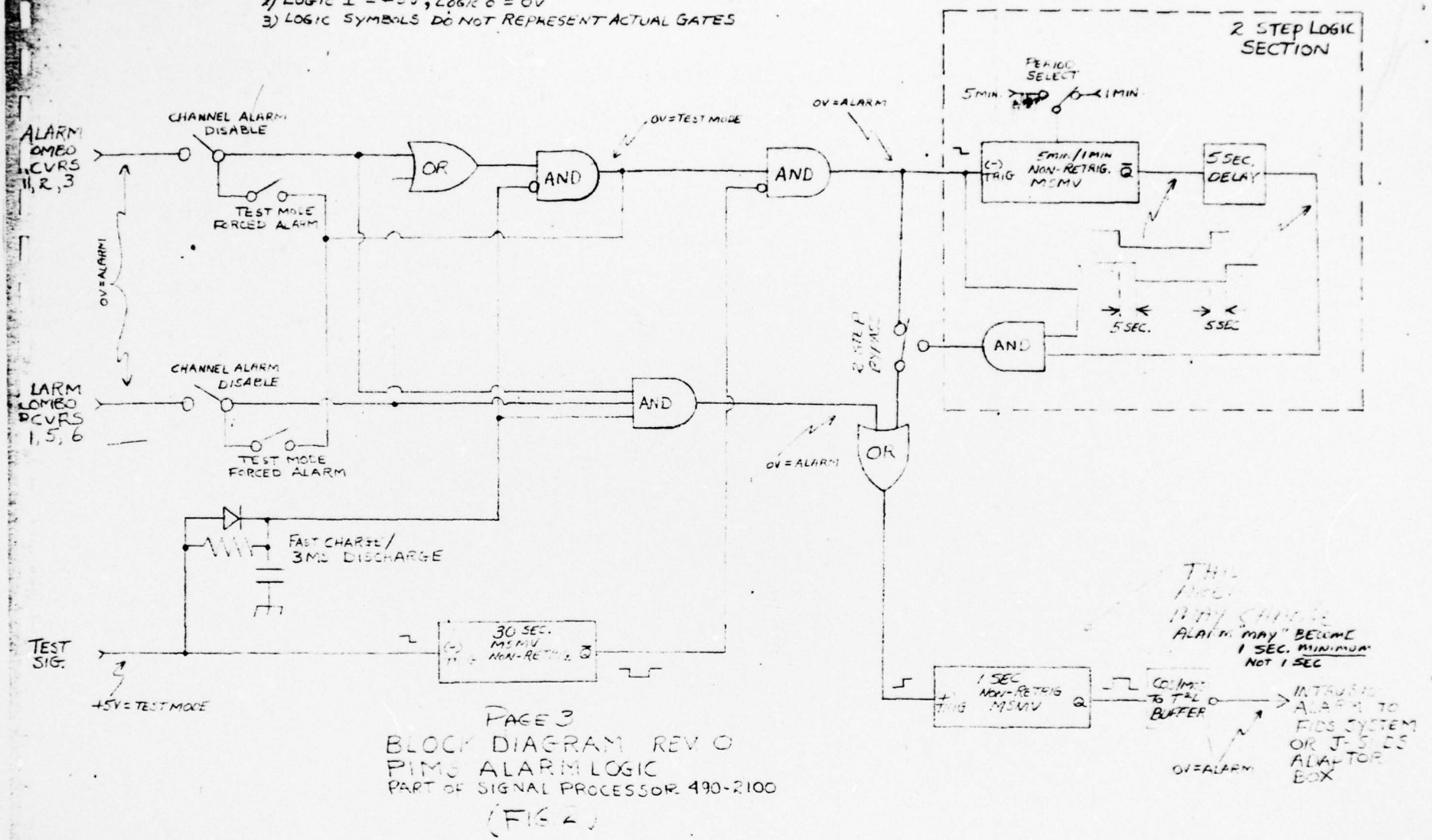


PAGE 2
FIG 1
BLOCK DIAGRAM REV 0

NOTES:

1) SWITCHING SELECTION IS DONE WITH SOLDER JUMPERS
2) LOGIC 1 ≙ +5V, LOGIC 0 ≙ 0V
3) LOGIC SYMBOLS DO NOT REPRESENT ACTUAL GATES



PAGE 3
BLOCK DIAGRAM REV O
PIMS ALARM LOGIC
PART OF SIGNAL PROCESSOR 490-2100
(FIG 2)

2.0 CIRCUIT/OPTICS DESCRIPTION

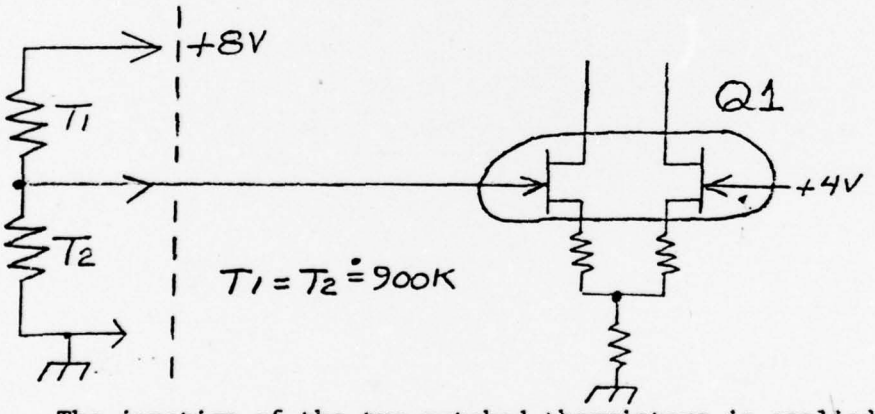
See enclosed schematics for the receiver, signal processor and J-SIIDS adapter box.

2.1 Receiver Card: Assembly 490-2101

The receiver assembly may be mounted up to 500 ft. away from the signal processor. Up to six heads may be tied into each processor card.

The receiver is made up of a +16 Vdc and +8 Vdc regulator. The input voltage is between +18 Vdc and +22 Vdc. Typical steady state current drain for the entire card is 1.5 ma.

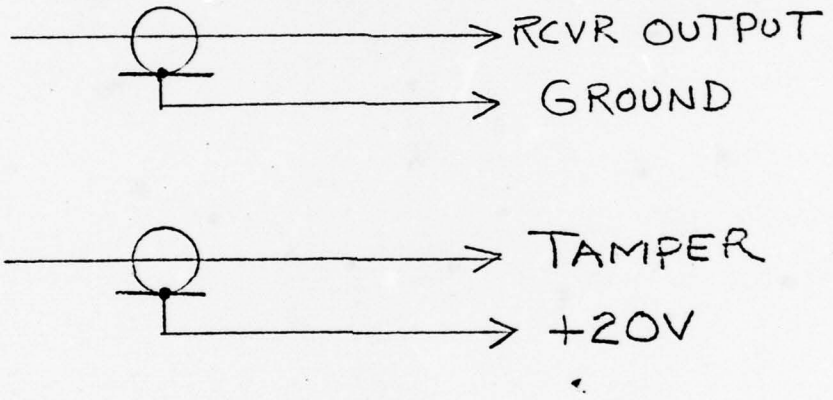
The infrared to voltage converter consists of a dual thin thermistor flake mounted on top of a transistor case. This case is mounted in a tubular holder which in turn mounts to the printed circuit board. A +8 vdc reference is supplied to the thermistor as shown below.



The junction of the two matched thermistors is applied to one side of a differential amplifier. This amplifier has a +4 Vdc reference and can respond in a bipolar manner depending on whether T1 or T2 increases in temperature. The front end of the differential amplifier is made up of a matched pair of field effect transistors, having very high input impedance (>10 meg). The operating point for the fets is set by selecting R5 at the time of factory test. The voltages at E1 and E2 are set to 6.7 vdc.

The drains of Q1 are connected to the inputs of a low power, low noise operational amplifier. The total gain of the fets and operational amplifier is 23 db (Eo/Ein = 14). The operational amplifier is operated from +16 vdc and ground. It is biased for +8 vdc output. A +8v bias allows bipolar operation and also provides a 0v bias across the two tantalum coupling capacitors (+8 v from the signal processor is on the other side of the capacitors.) Low bias means the DC leakage through the capacitors will be minimal.

The head is connected to the processor through two coax wires. (See below).



The tamper line only goes as far as a terminal strip mounted inside the head assembly. The tamper line then runs to a load resistor via the tamper switch. The load resistor is mounted to the terminal strip. In the case of multiple heads the tamper line is daisy chained and the load resistor appears only at the last head. Conditions for a tamper alarm are discussed under the next section. The optics which focus the 17 beams on to the thermistors will be also discussed in a future section.

2.2 Signal Processor - Assembly 490-2100

2.2.1 General

The signal processor is mounted on a 6 inch x 8 inch printed circuit board. Actually the card consists of two separate processing channels each of which can accommodate up to 3 receivers. Each channel has a separate gain control for the summation of heads used. The final intrusion alarm can originate from any receiver input. There are several options that will be discussed as far as the wiring of jumpers on the board.

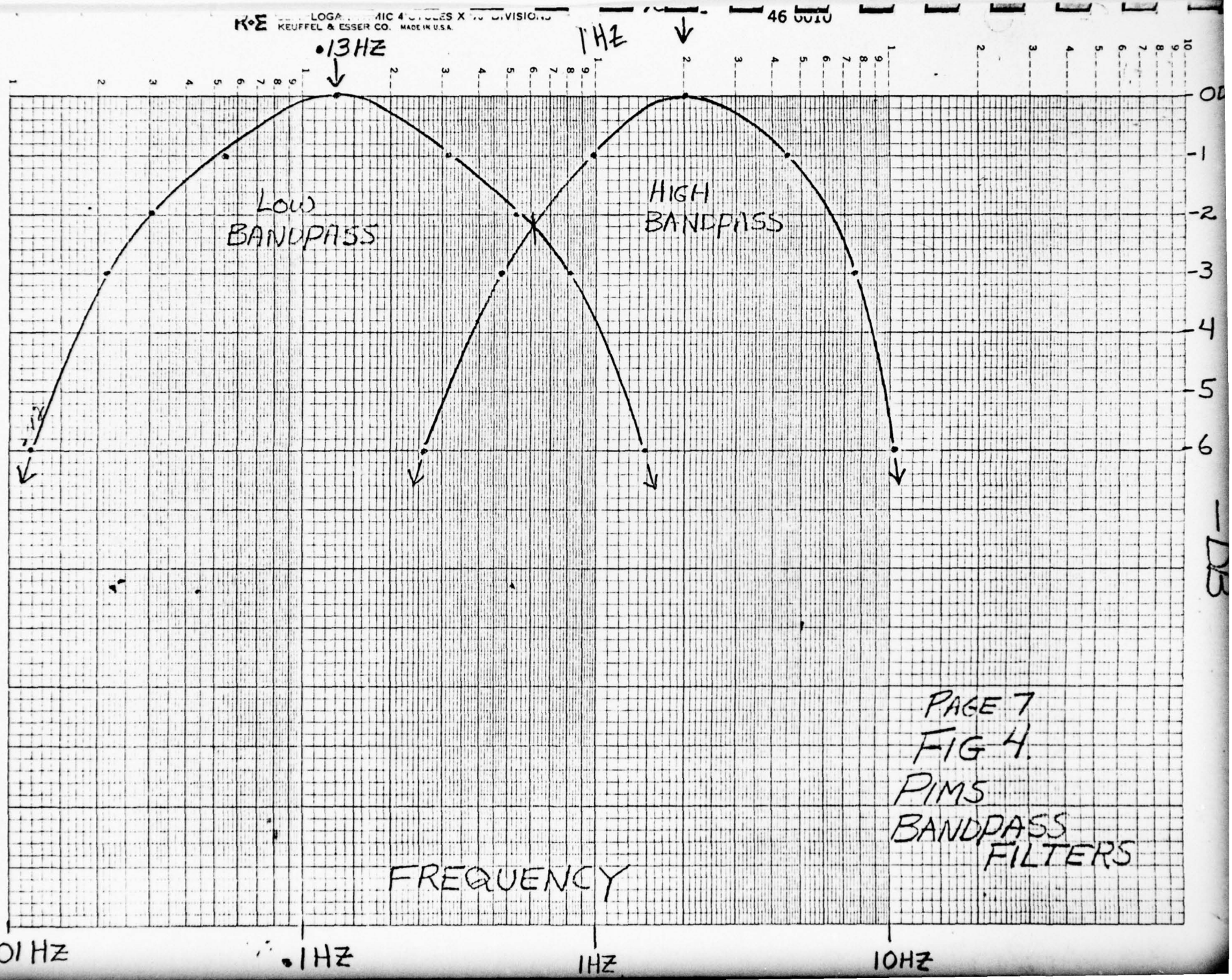
In addition to the two processing channels which contain gain and bandpass filters the processor also contains tamper detection circuits, a +16 V/+8V regulator, a DC to DC converter when +10V is the prime DC power and alarm logic.

2.2.2 Input Amplifier AR1 or AR6

The input stage has a gain adjustment from 28 to 41 DB. The three 130K input resistors form a summing junction in conjunction with the operational amplifier. (DO NOT GROUND UNUSED INPUTS). The DC bias at the output is set to +8V for maximum bipolar operation. The .01 uf capacitors (C4 or C45) lower the bandpass so as to only allow the frequencies inside the two following active bandpass filters to pass. This particularly lowers any 60 Hz pickup from power cables in the area. Clockwise rotation of either potentiometer will increase the gain of the corresponding channel.

2.2.3 Bandpass filters AR2/AR3 and AR7/AR8

Following the variable gain amplifiers is a parallel channel each with a gain of 42 db (in the passband). These amplifiers are also active bandpass filters with roll offs of 12 DB/octave. The center frequency of the High Bandpass is 2 Hz. The center frequency of the Low Bandpass is .13 Hz. (See enclosed plots Fig. 4). Two filters are used in order to improve the signal to noise ratio. Both amplifiers are offset by the regulated +8V. Test points are provided at the top edge of the card in order to monitor the outputs of all four bandpass filters.



PAGE 7
FIG 4.
PIMS
BANDPASS
FILTERS

2.2.4 Threshold [illegible] AR 9 and AR10

In order to determine whether a particular infrared transient constitutes an alarm, a threshold criteria must be set. False alarm rates from real installations are not available yet but extensive lab tests indicate a threshold of greater than +9 Vdc or less than +7 Vdc shall cause an alarm (in conjunction with other logic criterion described later). If the threshold need be changed in the future, 16 resistors on the processor card may be changed.

The threshold detector is made up of resistors to obtain the desired ± 1V range and a quad operational amplifier (LM2901N) specifically designed as a threshold detector. The quad amplifier only draws .8 ma (4 mw unit). The output stage has an open collector and therefore R35 and R76 are pull up resistors. The outputs are "wired OR'ed" so that an alarm is 0 Vdc and no alarm is +5 Vdc (at E20 and E22).

2.2.5 DC Regulator +8V -16V

The specification for the PIMS system states that the input DC power supply may vary from +9V dc to +22 Vdc. In the FIDS configuration the input is from +9V to +11 Vdc in which case the DC to DC converter A1 is wired into use. The DC to DC converter has a gain of two. Several portions of the processor require a voltage less than +22V (example: μA776 max. +18V) and a regulated votage (example: threshold voltage, DC offset to op-amps and +5V for logic).

The regulator has one resistor (R45) which must be selected at initial test. A 1% resistor is chosen that adjusts the +8V supply as close as possible to +8.0 Vdc, Fet Q3 acts as a constant current source so that if the +16 V tries to change then +8V is maintained at the positive input to AR5 and AR4. Q2 is a part of the feedback loop for AR4. The gain of AR4 is + (1 + R44/R42) or 2. The output at E18 is two times +8 or +16Vdc.

2.2.6 Tamper Threshold Detector

The Tamper threshold Detector is designed to generate a 1 sec. alarm at pin 17 of the signal processor. The level will be 0 Vdc for an alarm and +5 Vdc for no alarm. The drive capability shall be a T^2L fan out of 4 max.

When pin 16 is loaded with a 10K, 1% resistor, the tamper alarm will occur if either condition below happens.

1) The tamper line opens (cut or via tamper switch)

2) The tamper line is tied to the +20V at the heads.

3) The tamper line is tied to ground.

4) The tamper line has a parallel resistor tied across which is less than 7.5K ohms.

The tamper line will be daisy chained through from 1 to 6 heads. Each head has a tamper switch. The last head in the chain has the 10K resistor to ground. The normal no alarm condition produces approximately + .72 Vdc on the tamper line.

A logic transition from 1 to 0 at the output of AR11 will trigger the 1 second multivibrator (U7).

2.2.7 Normal Alarm Logic

See Figure 2 for block diagram.

There are several choices as to what logic is employed. This is accomplished by the use of soldered jumpers. A summary of these jumpers appears on the processor schematic. Some of the jumpers do not affect the logic. Also see the section on installation instructions regarding jumper usage.

If the RCVR 1-3 channel is to be enabled then jumper E22 to E23 is used and E23 to E24 is not used. If RCVR 1-3 channel is not to be used E22 to E23 is not used and E23 to E24 is used. (The same applies to RCVR 4-6 channel with its corresponding E20 to E21 and E25 to E26 jumpers). E23 to E24 and E25 to E26 are used to simulate an artificial alarm during the self test mode if there is no head connected to that channel. U1 pin 4 is 0V the test mode.

Assuming there is at least one head connected to each channel the alarm logic is such: If either channel generates an alarm (OV at either E20 or E22) then either U3/E or U3/F produces a logic 1. U1/A is a nor gate (a logic 1 at either input produces a logic 0 at U1 pin 5. If there is no logic 1 at (Test Signal) pin 28, then U1 pin 6 is at Logic 0. Two logic 0's at U1/B produces a logic 1 at U2 pin 3. Since U2 pins 4 and 5 are normally logic 1 (except for 30 seconds after test mode drops out) the output at U2 pin 6 is logic 0 for the alarm condition.

At this point, depending on customer usage, the logic has two possible paths. The first is a normal route throughE1 to E2 jumper with E2 to E32 removed. This bypasses the two step logic. Bypassing the two step logic normally is for conditions of high security or very low clutter. In this condition, U2 pin 11 is held to logic 1 because the test signal is at logic 0. U2 pin 13 is at logic 1 because the normal condition of U5 pin 11 and AR11 pin 14 is a logic 1. In order for U2 pin 13 to be a logic 0, U1 pin 10 must be a logic 1. U1 pin 10 can only be a logic 1 if both U1 pins 8 and 9 are logic 0. The 5 second delay at AR11 pin 14 insures U2 pin 13 will be a logic 1 when the <u>first</u> alarm occurs. So with U2 pins 11 and 13 at logic 1 and U2 pin 12 going from logic 1 to logic 0 (alarm), U2 pin 10 goes from logic 0 to logic 1 and triggers the 1 second alarm multivibrator U6.

The second possible logic path previously mentioned for the first alarm at U2 pin 6 is to initiate the two step logic.

The following requirements are necessary in order to generate the intrusion alarm when the two step logic is not bypassed; i.e., jumper E1 to E2 removed, jumper E2 to E32 used.

1) The 0 logic alarm at U2 pin 6 remains for greater than the 5 second delay period at AR11 pin 14.

OR

2) During the period of the U5 multivibrator (Select 1 minute or 5 minutes) and after the 5 second delay is over, a second alarm (Logic 1 to Logic 0) at U2 pin 6 occurs.

The two step logic prevents noise spikes or one time clutter occurances from generating alarms. In high clutter environments the 1 minute jumper E3 to E4 would be used. If E3 to E4 is not used the second threshold alarm can occur within 5 minutes of the first (after the 5 second delay is over).

2.2.8 Test Mode Logic

See Figure 2 for block diagram.

The test mode is a special situation. An infrared source in placed in one of the beams of either RCVR 1, 2 or 3 and in either RCVR 4, 5, or 6. The infrared devices are controlled by the console operator.

In a situation where only one channel is being used (RCVR 1, 2 or 3) for example and nothing is tied to pins 5, 6 or 7 of the processor card, the following jumper arrangement is required:

E22 to E23 (IN)

E23 to E24 (OUT)

E20 to E21 (OUT)

E25 to E26 (IN)

If only (RCVR 4, 5 or 6) channel is used and there is nothing tied to pins 2, 3 or 4 then the following jumper arrangement is required:

E22 to E23 (OUT)

E23 to E24 (IN)

E20 to E21 (IN)

E25 to E26 (OUT)

The use of the E23 to E24 and the E25 to E26 jumper is an artificial way to generate a "test" alarm when that channel is not connected.

An artificial alarm must be generated because for the test mode to work, U2/A acts as a nand gate (alarms in both channels and being in the test mode) make U2 pin 11 at logic 0 and thereby bypass the normal route or 2 step logic route. When in the test mode pin 28 is at logic 1.

U2 pin 2 and U1 pin 6 becomes logic 1 in less than 1 millisecond after pin 28 is logic 1. A logic 1 on U2 pin 2 enables U2/A and awaits the logic 1 alarms at pins 1 and 8.

The infrared test source takes greater than 1 millisecond to turn on - so U1 pin 6 does not have a race condition to inhibit U1/B. U1/B must be inhibited during test mode or else an alarm will be generated at U2 pin 6 during the test mode (which is not desired).

In order to get from the test mode back to the normal mode some additional logic is required. Since there is a rather long recovery time in the processor before the circuits have stabilized from the test infrared source, it is necessary to temporarily inhibit normal operation for a 30 second period after the test signal (Pin 28) has gone back to logic 0. This is accomplished by forcing U2/B to a logic 1 (no alarm condition) as long as U4 is in its 30 second period.

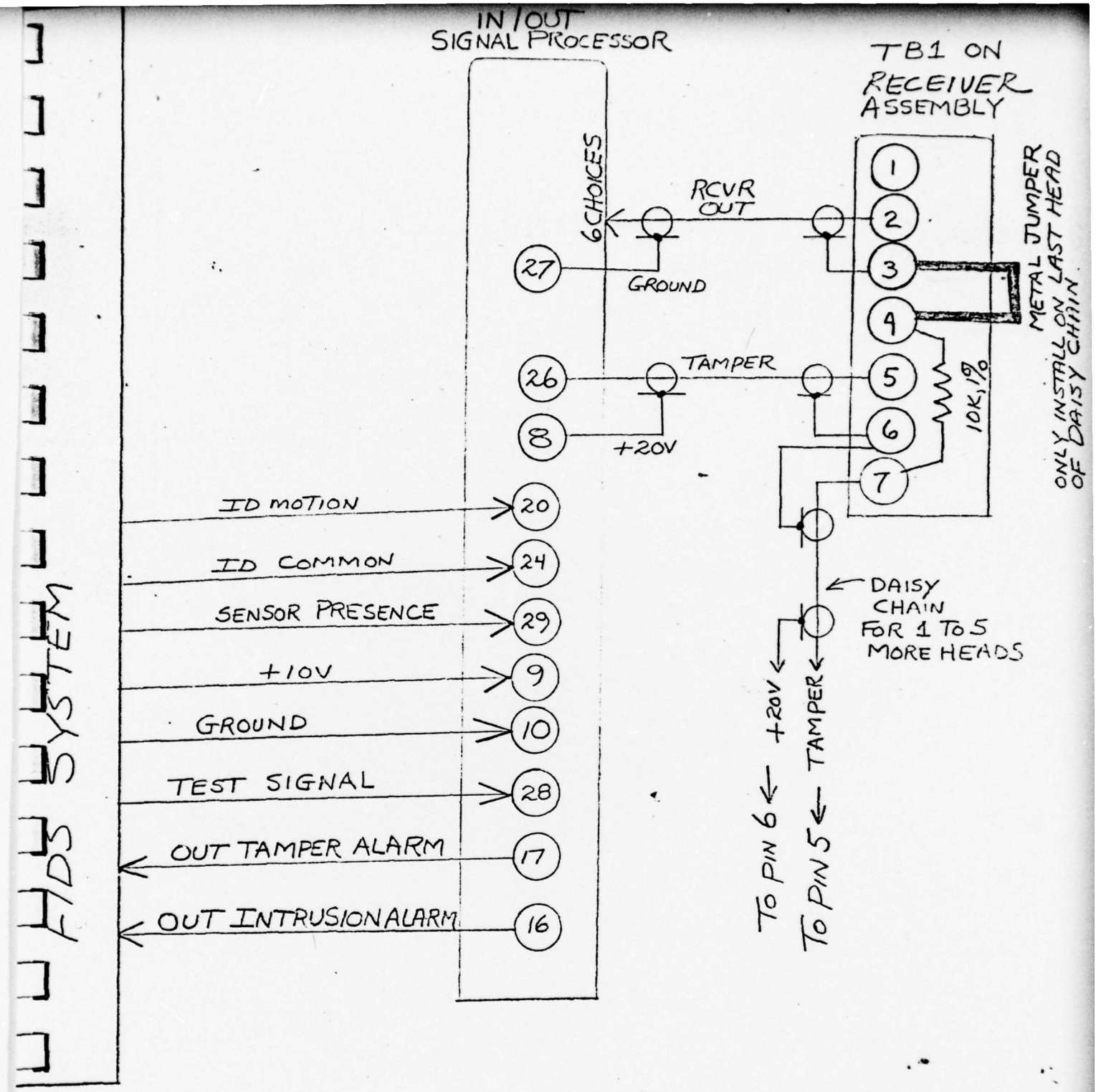
The R94/C21 time constant (3MS) is used to prevent a race condition. This time constant insures that U1/B is forced to a logic 0 for a short extended period necessary to get U4 pin 11 to logic 0.

2.2.9 Optics

See Figures 5 and 3.

The optics consist of a multi-faceted mirror assembly which has 17 fields of view as shown in Figure 3. The mirrors reflect the infrared energy on to a parablic mirror which in turn focuses the energy on to the dual thermist discussed earlier. The mirror assembly has a hard cover with windows to allow t IR energy to enter. The windows are covered with a translucent polyethelene mat that only slightly attenuates the infrared energy. The mirror surfaces are coat with chrome.

A pair of set screws lock the thermistor mount at a designated distance to optimize the focus. The focus is done with an Alan Head screw through the back of the wall plate holding the mirror assembly. The adjustment screw is removed at the factory after the set screws are tightened.



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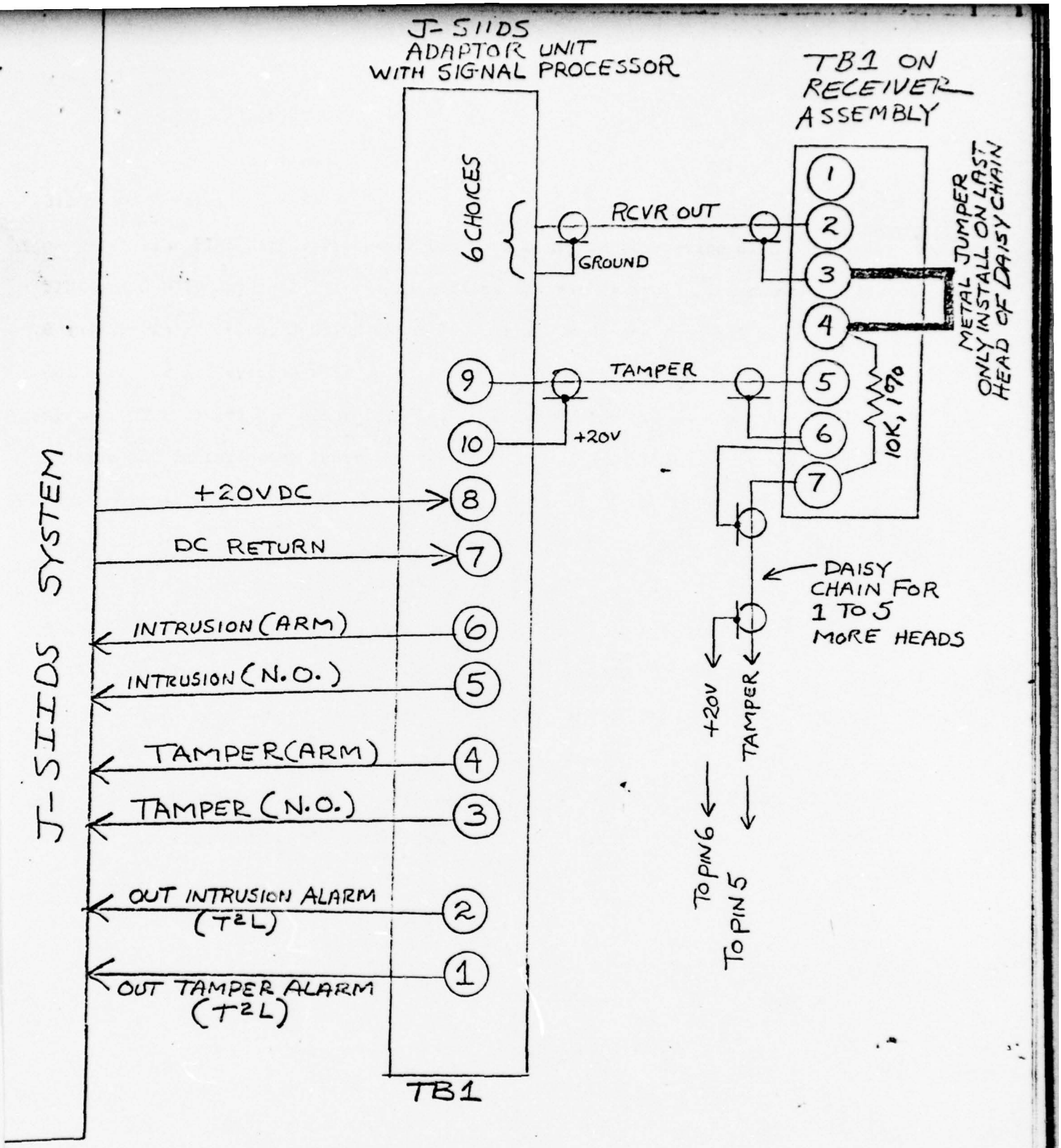
PIMS INTERCONNECTIONS FOR FIDS

FIG. 6



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PIMS INTERCONNECTIONS FOR J-SIIDS

FIG 7

3.0 INSTALLATION INSTRUCTIONS

See Figures 6 and 7

3.1 General Comments

The PIMS Signal Processor has been designed to operate with both FIDS and J-SIIDS systems. Interconnections for either system are shown in Figures 6 and 7. In addition, J-SIIDS has a low current mode and a normal mode. General comments for all systems will be given in addition to special instructions for each system. The signal processor card has 12 soldered jumpers (see schematic, logic section and installation instructions). Wrong usage of these jumpers can cause circuit malfunction or permanent damage to electrical components.

3.2 General instructions (all systems)

3.2.1 Location and Wiring of RCVR Assembly:

The metal plate that supports the RCVR mirror and preamplifier has three holes for screw mounting to a flat vertical wall. Normally the center of the optics are at 7'4" (to obtain beams patterns in Figure 3). The height could be varied from 6ft. to 8 ft. if there are obstructions on the wall, etc.

The Receiver head shall be connected to the FIDS system or J-SIIDS adapter box with two RG-58 coax cables which are under 500 ft. in length. The daisy chain loop shown also uses RG-58 coax. The coax wire shall have Flag lugs (KULKA 600 FL) fabricated to the ends for connection to TB1 of the RCVR and TB1 of the J-SIIDS adapter box. The coax location inside the assembly is shown on Figure 5 (490-2103).

The 10K resistor and the metal jumper come mounted on every head. At the time of installation the metal jumper is retained <u>ONLY</u> on the terminal strip of the last receiver. This ties the 10K to ground at the <u>end</u> of the tamper loop.

The plastic cap that is placed over the thermistor mount should not be removed until just before the cover is to be put in place.

It is suggested that the coax wires be run in metal conduit to provide protection and shielding.

3.2.2 Gain Settings

The signal processor has a gain adjustment for each of its two channels (R8 for RCVR 1, 2 & 3 combo) and (R55 for RCVR 4, 5 & 6 combo). The criteria for setting these pots is based on many factors such as clutter, whether the two step logic is used, level of security and tolerable false alarm rates. Test points E27, E28, E29 and E30 are brought out to the edge of the card in addition to E31 (GROUND). E27 and E29 are low frequency channels. E28 and E30 are high frequency channels. These points can be monitored with a scope (DC input) or a chart recorder (such as a GOULD 156327 57). Peak variations in noise exceeding $\pm$ 1V around the +8V bias will cause alarms (except under some conditions when the two step logic is used).

If it is not clear where to set the gain initially it is suggested to set it at mid range. If after one week there are no false alarms the gain could probably be raised to 3/4 full range. (clockwise rotation for increasing gain).

3.3 Special Instructions for FIDS operation

3.3.1 Signal processor solder jumpers:

The following jumpers shall be used or removed as listed <u>before</u> power is applied.

E5 to E8	OFF
E6 to E7	OFF
E9 to E10	OFF
E10 to E11	ON
E12 to E13	ON
REMAINING JUMPERS	Optional (see schematic)

3.3.2 Power Supply

Insure that the DC voltage that will be connected to pin 9 of the signal processor is +10Vdc ± 1 Vdc.

3.3.3 Test Signal Input

Unless the test mode is desired, insure the voltage to be connected to pin 28 of the signal processor is between 0 and +.5Vdc.

3.4 Special Instructions for Normal J-SIIDS operation

3.4.1 Signal processor solder jumpers:

The following jumpers shall be used or removed as listed before power is applied.

E5 to E8	ON
E6 to E7	ON
E9 to E10	ON
E10 to E11	OFF
E12 to E13	OFF
Remaining Jumpers	Optional (see schematic)

3.4.2 Power Supply

Insure that the DC voltage that will be connected to pin 9 of the signal processor is +20V ± 2 Vdc.

3.4.3 Adapter Box Switch

Insure that the slide switch (S1) on the J-SIIDS adapter box is in the NORMAL Position.

3.5 Special Instructions for Low Current J-SIIDS operation

3.5.1 Signal Processor solder jumpers;

The following jumpers shall be used or removed as listed before power is applied.

E5 to E8	OFF
E6 to E7	OFF
E9 to E10	ON
E10 to E11	OFF
E12 to E13	OFF
Remaining jumpers	optional (see schematic)

3.5.2 Power Supply

Insure that the DC voltage that will be connected to pin 9 of the signal processor is +20V $\pm$ 2 Vdc.

3.5.3 Adapter Box switch

Insure that the slide switch (S1) on the J-SIIDS adapter box is in the LOW CURRENT position.

4.0 TROUBLESHOOTING

4.1 General

Familiarity with the enclosed optics and circuit descriptions is required in order to properly troubleshoot the PIMS system. In the case of optional jumpers on the signal processor, the intended logic conditions should be understood.

Some of the important points to monitor if walk tests do not produce alarms is given below. In the case of the FIDS system an extender board will be necessary to reach various points on the signal processor. Place the plastic cap over the thermistor mount except for Walk tests.

4.2 DC VOLTAGES AFTER 5 MIN WARM UP:

RCVR Board (Schematic 490-3101)

E1 (+ 6.7v ± .2V dc)

E2 (+ 6.7v ± .2V dc)

E8 (+ 20v ± 2V dc)

E3 (+8v ± .2Vdc)

E5 (+16V ± .4Vdc)

terminal c (+4V ± .2 Vdc)

Negative side C9 (+8 Vdc ± .4 Vdc)

4.3 DC Voltages After 5 Min Warmup

Signal Processor (schematic 490-3100) (Not in test mode), Reference reading to E31

E27, E28, E29, E30	+8V ± .4Vdc with up to .5V p-p low frequency noise
E10	+20V ± 2Vdc
E18	+16V ± .4Vdc
E19	+8V ± .2Vdc
E21, E23	+5V ± .5Vdc
E6	+5.5 ± .3Vdc
+Side C7 and C47	+8V ± .4Vdc

E1	+5V ± .5Vdc
E32	+5V ± .5Vdc
+side C60	+5 ± .5Vdc (give a 10 min warmup)
Pin 17	+5V ± .5Vdc
Pin 16	+5V ± .5Vdc
Pin 26	+.72 ± .2Vdc (if tamper loop is not opened)
U1 pin 6	0 to +2Vdc
U1 pin 8	+5V ± .5Vdc
+side C16	+5V ± .5Vdc

4.4 Troubleshooting J-SIIDS Adapter Box

The J-SIIDS adapter box consists mainly of two identical T^2L to relay converters used only in the Normal J-SIIDS mode.

A simple check would be to place an ohmmeter across TB1 pins 6 to 5 after removing the wires to the outside units. If a 0V is present on pin2 of TB1 (by forcing an alarm) then the ohmmeter shall read 100 ohms ± 10 ohms for a minimum of 1 second.

Now after removing the outside wires to TB1 pins 3 and 4 and cheating both S3 and S2 tamper switches an ohmmeter across pins 3 and 4 shall read 100 ohms ± 10 ohms for ONE second if a tamper condition is forced (such as removing cover to RCVR assembly).

When the S1 switch is in the LOW CURRENT mode the relay drivers are not used. The Alarms are just routed to TB1 pins 1 and 2 as T^2L levels (+5V, 0V).

5.0 FORMAL DRAWINGS ENCLOSED

A or B size prints enclosed in this preliminary manual are listed below:

Schematic PIMS (Receiver)	490-3101
Circuit Card Artwork (Receiver)	490-2106
Circuit Card Parts List (Receiver)	PL490-2101
Schematic PIMS (Signal Processor)	490-3100
Circuit Card Artwork (Signal Processor)	490-1109
Circuit card parts list (Signal Processor	PL490-2100
Sensor Assy (ALL MAJOR PARTS OF RCVR)	490-2103
Infra-red System (Beam coverage)	4907002

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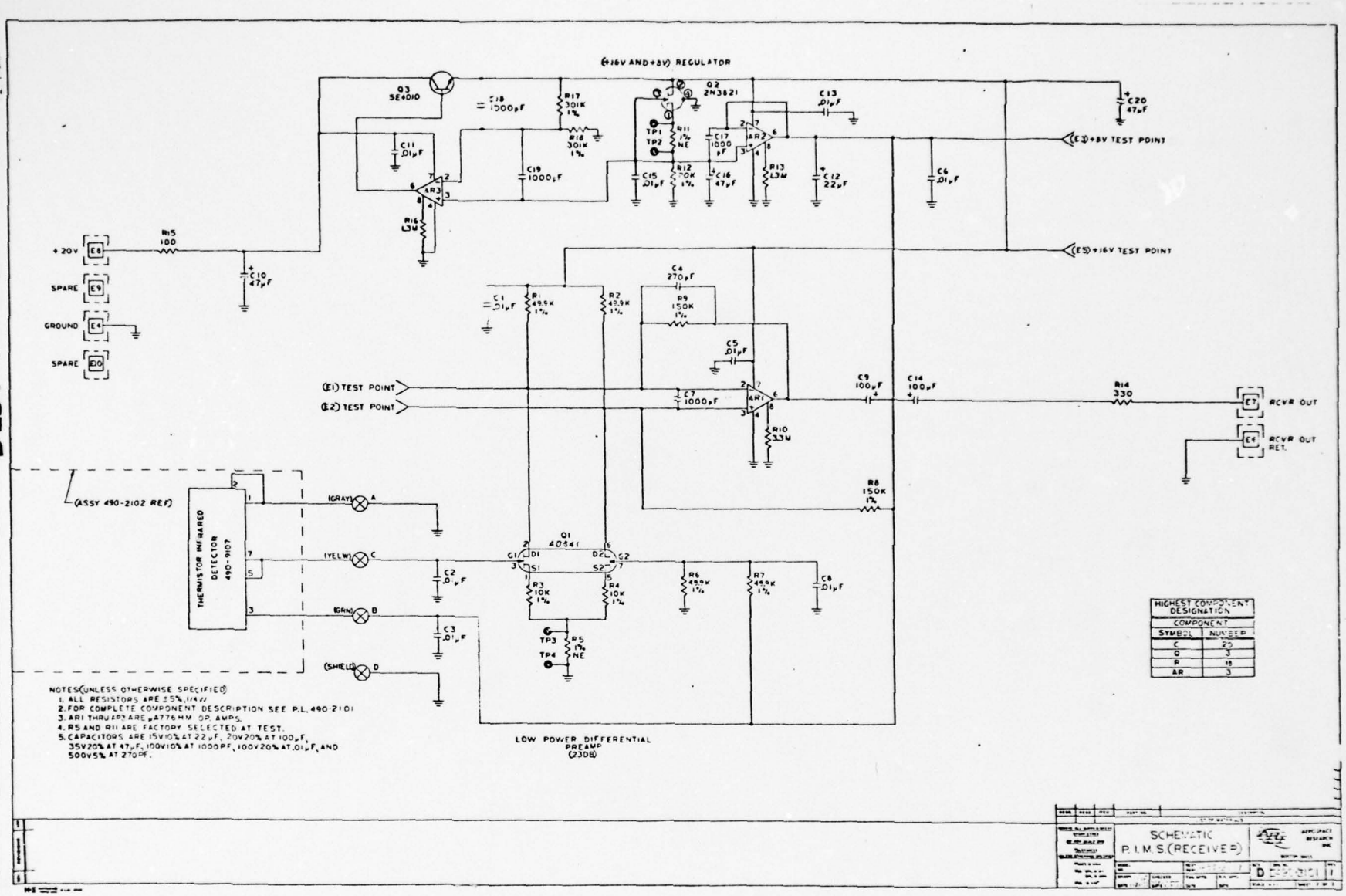
FIG 3

COVERAGE OF SUMMARED, SYSTEM WITH BOTTOM OF BOX MOUNTED 6'10" ABOVE FLOOR
(BEAMS 7'4" ABOVE FLOOR)

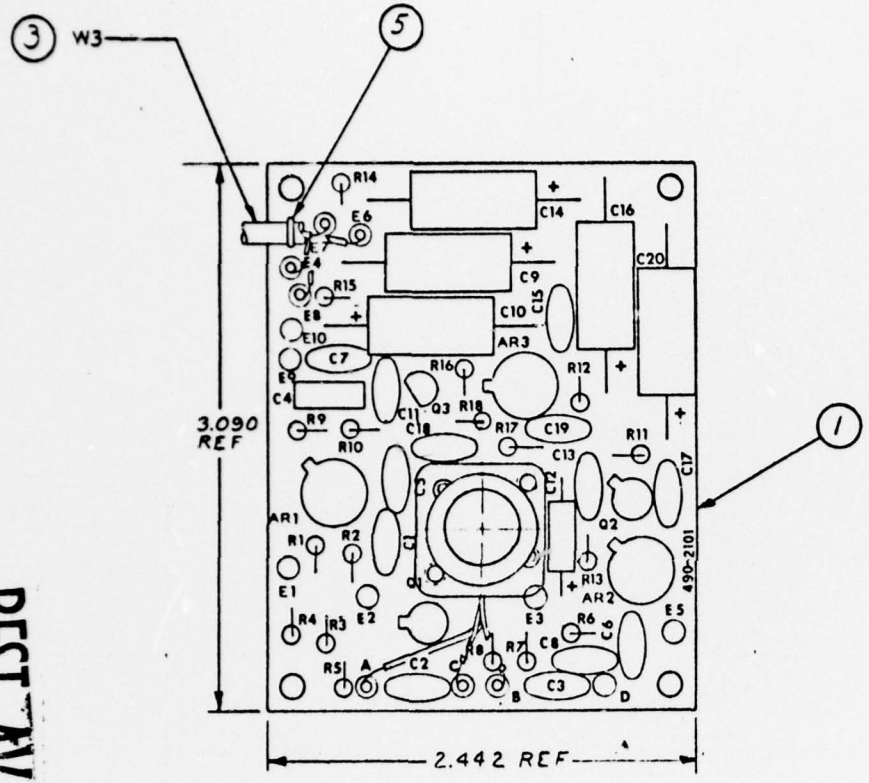


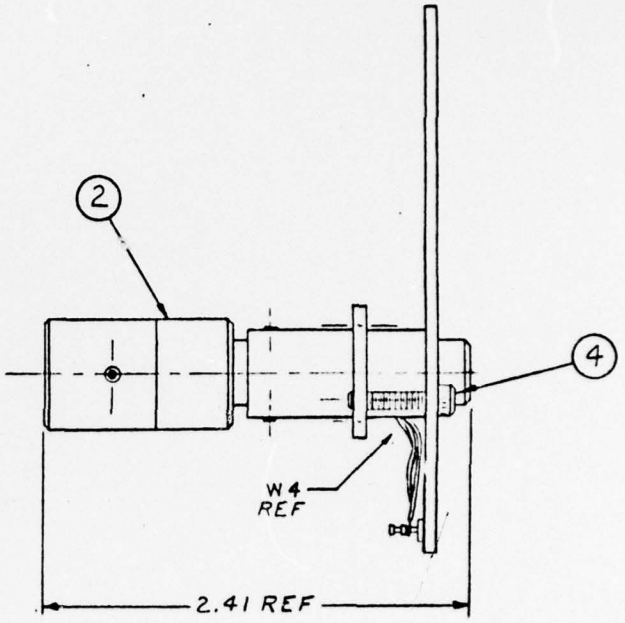
HIGHEST COMPONENT DESIGNATION	
COMPONENT	
SYMBOL	NUMBER
C	20
Q	3
R	15
AR	3

NOTES (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE ±5%, 1/4W
2. FOR COMPLETE COMPONENT DESCRIPTION SEE P.L. 490-2101
3. AR1 THRU AR3 ARE μA776 MM OP. AMPS.
4. R5 AND R11 ARE FACTORY SELECTED AT TEST.
5. CAPACITORS ARE 15V10% AT 22 μF, 20V20% AT 100 μF, 35V20% AT 47 μF, 100V10% AT 1000 PF, 100V20% AT .01 μF, AND 500V5% AT 270 PF.

SCHEMATIC P.I.M.S. (RECEIVER)

D





WIRING TABLE		
FROM	TO	FUNCTION
W3-RED	E8	+20V
W3-BLACK	E4	GROUND
W3-WHITE	E7	RCVR OUT
W3-SHIELD	E6	POWER RETURN
W4 GRAY	A	GROUND
W4-YELLOW	C	DETECTOR
W4-GREEN	B	+8V

REQD	ITEM	PART NO	DESCRIPTION
REF	6	490-3101	SCHEMATIC-RECEIVER
1	5	67606003	TIE-CABLE
2	4		SCREW, CAP 2-56 x 1/2
1	3		CABLE ASSEMBLY W3
1	2	490-2102	DETECTOR HOUSING ASSEMBLY
1	1	490-2101	P.C. ASSEMBLY, RECEIVER

LIST OF MATERIALS

DETECTOR-RECEIVER ASSY.

AEROSPACE RESEARCH INC

MODEL NO. PIMS | NEXT ASSY 490-2103 | SIZE C | DWG NO 490-2106 | REV B

DRAWN 1.A | DATE 2/3/77 | CHKD | DATE 2/8/77 | ENG APPD | DATE | PROD APPD | DATE | SCALE 2:1 | SHEET 1 OF 1

ENGINEERING / MANUFACTURING

PARTS LIST

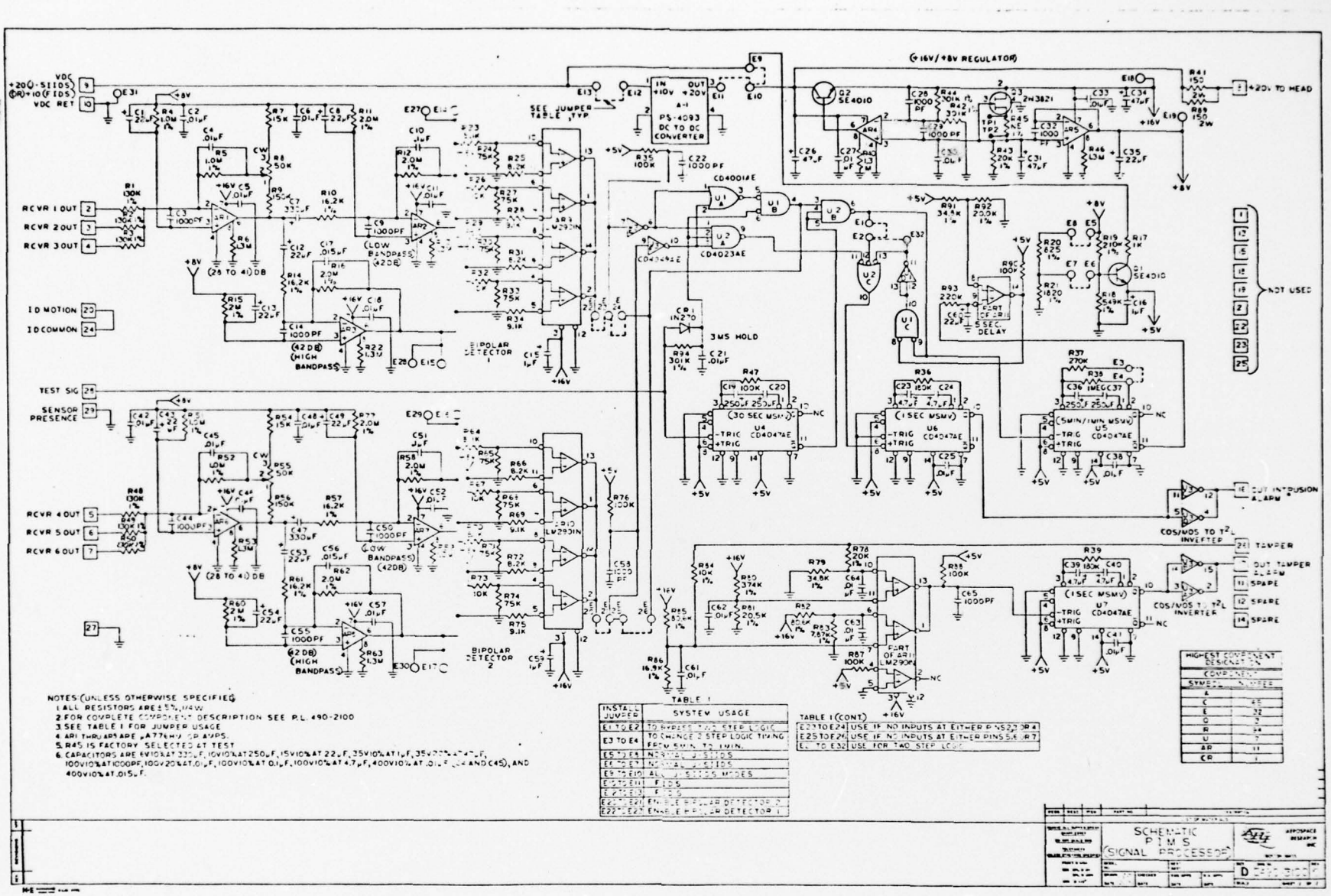
ITEM NO.	IDENT	PARTS LIST	DWG SIZE	PART NO. PRIME	PART NO. REV	PART DESCRIPTION	QTY PER	UNIT OF MEAS CODE	EFFECTIVE CHANGE DOC.	EFFECTIVE CHANGE NUMBER	EFFECTIVE CHANGE CODE	M/B CODE	OPN NO.	SPECIAL PART CHARACTERISTICS
1			C	490-1105		CIRCUIT CARD MASTER	1	EA						
2			A	61[illegible]2113		TERMINAL CARD #22-2	14	EA						A,B,C,D, E THRU L,N
3														
4														(BELDEN #9[illegible])
5			A	6031[illegible]		PROTECTIVE COATING	AR							
6														
7														
8														
9														
10			A	25153001		CAP .01UF 20% 100V	9	EA						C1, 2, 3, 5, 6, 8, 11,
11														C13, 15
12			A	21374006		CAP 270PF 5% 500V	1	EA						C4
13			A	25152004		CAP 1000PF 10% 100V	4	EA						C7, 17, 18, 19
14			A	22341005		CAP 100UF 20% 20V	2	EA						C9, 14
15			A	22361004		CAP 47UF 20% 35V	3	EA						C10, 16, 20
16			A	22331001		CAP 22UF 10% 15V	1	EA						C12
17														
18														
19			A	32024[illegible]37		RES 100 OHM 5% 1/2W	1	EA						R15
20			A	32021051		RES 33[illegible] OHM 5% 1/2W	1	EA						R14
21			A	32021135		RES 1.3 M 5% 1/2W	2	EA						R13, 16
22			A	32024147		RES 3.3 M 5% 1/2W	1	EA						R10

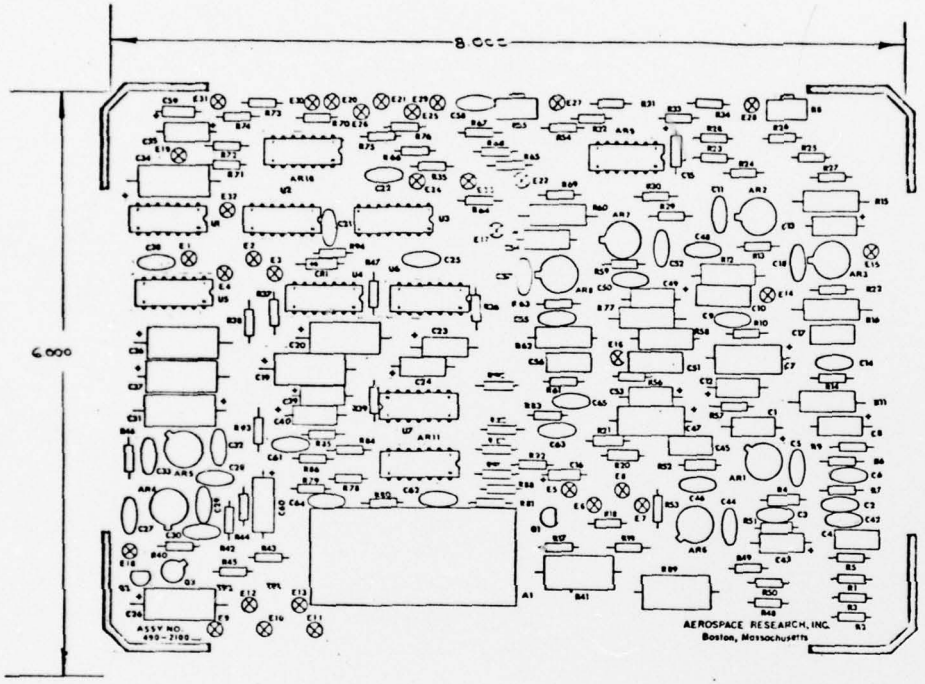
TITLE: CIRCUIT CARD ASSY RECEIVER	USED ON 490-2106	ISSUE NO.	CODE ABBR: A – ADD, C – CHANGE, D – DELETE, AS – AS REQ'D, EA – EACH, IN – INCH, FT – FOOT; B – BUY, M – MAKE, M/B – MAKE & BUY
	CHECKER 2/11/77	ISSUE DATE	
	ENGR APPVL	ZONE ENGR	
MODEL: PIMS	Q.A. APPVL	PLANNER	

AEROSPACE RESEARCH INC.
BOSTON, MASS.

ASSEMBLY NUMBER PL 490-2101 REV

SHEET 1 OF 2





NOTE:
1. SILK SCREEN USING BLACK EPOXY INK

SIGNAL PROCESSOR CIRCUIT CARD ASSY.

PART DESCRIPTION	QTY PER	UNIT OF MEAS CODE	EFFECTIVE CHANGE DOC.	EFFECTIVE CHANGE NUMBER	EFFECTIVE CHANGE CODE	M/B CODE	OPN NO.	SPECIAL PART CHARACTERISTICS
RES (NE) 1% 1/10W	1	EA						R5
RES (NE) 1% 1/10W	1	EA						R11
RES 10K 1% 1/10W	2	EA						R3, 4
RES 20K 1% 1/10W	1	EA						R12
RES 49.9K 1% 1/10W	4	EA						R1, 2, 6, 7
RES 150K 1% 1/10W	2	EA						R8, 9
RES 301K 1% 1/10W	2	EA						R17, 18
ANALOG DEVICES AD841 -	1	EA						Q1
TRANSISTOR SE4010	1	EA						Q3
TRANSISTOR 2N3821	1	EA						Q2
OP. AMP. UA776HM	3	EA						AR1, 2, 3
SCHEMATIC	REF							
ASSEMBLY	REF							

USED ON	ISSUE NO.
CHECKER	ISSUE DATE
ENGR APPVL	ZONE ENGR
Q.A. APPVL	PLANNER

CODE ABBR

A — ADD	B — BUY
C — CHANGE	M — MAKE
D — DELETE	M/B — MAKE & BUY
AS — AS REQ'D	
EA — EACH	
IN — INCH	
FT — FOOT	

AEROSPACE RESEARCH INC.
BOSTON, MASS.

ASSEMBLY NUMBER	REV
PL 490-2101	

ENGINEERING / MANUFACTURING

PARTS LIST

ITEM NO.	IDENT	PARTS LIST	DWG SIZE	PART NO. PRIME	PART NO. REV	PART DESCRIPTION	QTY PER	UNIT OF MEAS CODE	EFFECTIVE CHANGE DOC.	EFFECTIVE CHANGE NUMBER	EFFECTIVE CHANGE CODE	M/B CODE	OPN NO.	SPECIAL PART CHARACTERISTICS
1			D	490-1109		CIRCUIT CARD MASTER	1	EA						
2			A	67602013		TERMINAL CAMBION #2043-2	32	EA						E1 THRU E32
3			A	60812002		PROTECTION COATING	AS	AS						
4			A	67408007		SCREW BH - 440 x 1/2	2	EA						
5			A	69002003		WASHER FLAT #4	2	EA						
6			A	65501007		NUT PLAIN HEX #4-40	2	EA						
7				NEW DWG		PLUG (VARICON #7023)	1	EA						P-1
8				NEW DWG		CARD EJECTOR	2	EA						APPLIED DEVELOPMENT CORP SEE PAGE 481 #CD-3
9														
10														
11			A	22311003		CAP 330μf 10% 6V	2	EA						C7,47
12			A	22321005		CAP 250μf 10% 10V	4	EA						C19,20,36,37
13			A	22331001		CAP 22μf 10% 15V	10	EA						C1,8,12,13,35,43,49,53,
14														C54,60
15			A	22361001		CAP 1μf 10% 35V	3	EA						C15,16,59
16			A	NEW DWG		CAP 47μf 20% 35V	3	EA						C26,31,34
17			A	25152024		CAP 1000 pf 10% 100V	12	EA						C3,9,14,22,28,29,32,
18														C44,50,55,58,65
19														
20			A	25153021		CAP .01μf 20% 100V	21	EA						C2,5,6,11,18,21,25,27,30
21														C33,38,42,46,48,52
22														

TITLE: - CIRCUIT CARD ASSY SIGNAL PROCESSOR

MODEL:

USED ON	ISSUE NO.
CHECKER	ISSUE DATE
ENGR. APPVL	ZONE ENGR
Q.A. APPVL	PLANNER

CODE ABBR

A — ADD
C — CHANGE
D — DELETE
AS — AS REQ'D
EA — EACH
IN — INCH
FT — FOOT
B — BUY
M — MAKE
M/B — MAKE & BUY

AEROSPACE RESEARCH INC.
BOSTON, MASS.

ASSEMBLY NUMBER PL 490-2100 REV 5

SHEET 1 OF 5

ENGINEERING / MANUFACTURING PARTS LIST

ITEM NO.	IDENT	PARTS LIST	DWG SIZE	PART NO. PRIME	PART NO. REV	PART DESCRIPTION	QTY PER	UNIT OF MEAS CODE	EFFECTIVE CHANGE DOC.	EFFECTIVE CHANGE NUMBER	EFFECTIVE CHANGE CODE	M/B CODE	OPN NO.	SPECIAL PART CHARACTERISTICS
3			A	41153021		CAP .01UF 20% 100V	21	EA						C57, 61, 62, 63, 64
4			A	41235021		CAP 0.1UF 10% 100V	2	EA						C50, 51 (PLESSEY)
5			A	NEW NO.		CAP .01UF 10% 400V	2	EA						C4, 45
6			A	NEW NO.		CAP .015UF 10% 400V	2	EA						C17, 56
7			A	NEW NO.		CAP 4.7UF 10% 100V	4	EA						C23, 24, 39, 40
8														
9			A	41130001		DIODE IN270	1	EA						CR1
10														
31														
32			A	32034063		RES 1K 5% 1/4W	1	EA						R17
33			A	085		RES 8.2K	4	EA						R25, 31, 66, 72
34			A	086		RES 9.1K	8	EA						R23, 28, 29, 34, 64
35			A											R69, 70, 75
36			A	087		RES 10K	4	EA						R26, 32, 67, 73
37			A	091		RES 15K	2	EA						R7, 54
38			A	108		RES 75K	8	EA						R24, 27, 30, 33, 65
39														R68, 71, 74
40			A	111		RES 100K	6	EA						R35, 47, 76, 87, 88
41														R90
42			A	115		RES 150K	2	EA						R9, 56
43			A	117		RES 180K	2	EA						R36, 39
44			A	119		RES 220K	1	EA						R93

TITLE: CIRCUIT CARD ASSY SIGNAL PROCESSOR

MODEL:

USED ON | ISSUE NO.
CHECKER | ISSUE DATE
ENGR APPVL | ZONE ENGR
Q.A. APPVL | PLANNER

CODE ABBR

A — ADD	B — BUY
C — CHANGE	M — MAKE
D — DELETE	M/B — MAKE & BUY
AS — AS REQ'D	
EA — EACH	
IN — INCH	
FT — FOOT	

AEROSPACE RESEARCH INC.
BOSTON, MASS.

ASSEMBLY NUMBER PL 490-2100 | REV 5

SHEET 2 OF 5

ENGINEERING / MANUFACTURING

PARTS LIST

ITEM NO.	IDENT	PARTS LIST	DWG SIZE	PART NO. PRIME	PART NO. REV	PART DESCRIPTION	QTY PER	UNIT OF MEAS CODE	EFFECTIVE CHANGE DOC.	EFFECTIVE CHANGE NUMBER	EFFECTIVE CHANGE CODE	M/B CODE	OPN NO.	SPECIAL PART CHARACTERISTICS
45			A	32034121		RES 270K 5% 1/4W	1	EA						R37
46			A	135		RES 1MEG	1	EA						R38
47			A	31064043		RES 150 OHMS 5% 2W	2	EA						R41, 89
48			A	NEW NO.		RES (NE) 1%	1	EA						R45
49			A	33022551		RES 1.0M 1% 1/8W	4	EA						R4, 5, 51, 52
50			A	33012375		RES 7.87K 1% 1/10W	1	EA						RB3
51			A	385		RES 10K	1	EA						PB4
52			A	405		RES 16.2K	4	EA						R10, 14, 57, 61
53			A	407		RES 16.9K	1	EA						R86
54			A	414		RES 20K	3	EA						R43, 78, 92
55			A	415		RES 20.5K	1	EA						R81
56			A	437		RES 34.8K	2	EA						R79, 91
57			A	472		RES 80.6K	2	EA						R82, 85
58			A	512		RES 210K	1	EA						R19
59			A	527		RES 301K	3	EA						R42, 44, 94
60			A	553		RES 374K	1	EA						R80
61			A	552		RES 549K	1	EA						R18
62			A	492		RES 130K	6	EA						R1, 2, 3, 48, 49, 50
63			A	33022281		RES 825 OHMS 1% 1/8W	1	EA						R20
64			A	314		RES 1820	1	EA						R21
65			A	32032152		RES 2M 1% 1/4W	8	EA						R11, 12, 15, 16, 58
66														R60, 62, 77

TITLE: CIRCUIT CARD ASSY SIGNAL PROCESSOR

USED ON

CHECKER

ENGR APPVL

Q.A. APPVL

ISSUE NO.

ISSUE DATE

ZONE ENGR

PLANNER

MODEL:

CODE ABBR

A — ADD
C — CHANGE
D — DELETE
AS — AS REQ'D
EA — EACH
IN — INCH
FT — FOOT

B — BUY
M — MAKE
M/B — MAKE & BUY

AEROSPACE RESEARCH INC.
BOSTON, MASS.

ASSEMBLY NUMBER PL 490-2100

REV 5

ENGINEERING / MANUFACTURING PARTS LIST

ITEM NO.	IDENT	PARTS LIST	DWG SIZE	PART NO. PRIME	PART NO. REV	PART DESCRIPTION	QTY PER	UNIT OF MEAS CODE	EFFECTIVE CHANGE DOC.	EFFECTIVE CHANGE NUMBER	EFFECTIVE CHANGE CODE	M/B CODE	OPN NO.	SPECIAL PART CHARACTERISTICS
67			A	32034138		RES 1.3M 5% 1/4W	8	EA						R6 13 22 40 46
68														R53 59 63
69			A	36245001		POT 50K 10% 1/2W	2	EA						R8, 55
70														
71			A	42150001		TRANSISTOR SE4070	2	EA						Q1 2
72			A	46110003		TRANSISTOR 2N3821	1	EA						Q3
73			A	44630005		I.C. CD4001AE	1	EA						U1
74			A	007		I.C. CD4023AE	1	EA						U2
75			A	008		I.C. CD4047AE	4	EA						U4 5 6 7
76			A	009		I.C. CD4049AE	1	EA						U3
77														
78														
79														
80														
81			A	46110003		I.C. OP-AMP LM776HM	8	EA						AR1 2 3 4 5 6 7
82														AR8
83			A	43520002		I.C. LM2901N	3	EA						AR9 10 11
84														
85			A	46110004		CON DC TO DC MS-4093	1	EA						A1
86														
87														
88														

TITLE: CIRCUIT CARD ASSY SIGNAL PROCESSOR

MODEL:

USED ON	ISSUE NO.
CHECKER	ISSUE DATE
ENGR APPVL	ZONE-ENGR
Q.A. APPVL	PLANNER

CODE ABBR

A — ADD
C — CHANGE
D — DELETE
AS — AS REQ'D
EA — EACH
IN — INCH
FT — FOOT
B — BUY
M — MAKE
M/B — MAKE & BUY

AEROSPACE RESEARCH INC.
BOSTON, MASS.

ASSEMBLY NUMBER PL 490-2100 REV 5

SHEET 4 OF 5

ENGINEERING / MANUFACTURING

PARTS LIST

ITEM NO.	IDENT	PARTS LIST	DWG SIZE	PART NO. PRIME	PART NO. REV	PART DESCRIPTION	QTY PER	UNIT OF MEAS CODE	EFFECTIVE CHANGE DOC.	EFFECTIVE CHANGE NUMBER	EFFECTIVE CHANGE CODE	M/B CODE	OPN NO.	SPECIAL PART CHARACTERISTICS
89			A	490-2102		WIRE-JUMPER J1	1	AS						
90			A	NEW NO.		J2	1	AS						
91			A	NEW NO.		J3	1	AS						
92			A	NEW NO.		J4	1	AS						
93			A	NEW NO.		J5	1	AS						
94			A	NEW NO.		J6	1	AS						
95			A	NEW NO.		J7	1	AS						
96														
97														
98														
99														
100														
101			D	490-3100		SCHEMATIC	REF							
102			D	490-2100		ASSEMBLY	REF							
103														
104														
105														
106														
107														
108														
109														
110														

TITLE: CIRCUIT CARD ASSY SIGNAL PROCESSOR

MODEL:

USED ON	ISSUE NO.
CHECKER	ISSUE DATE
ENGR APPVL	ZONE ENGR
Q.A. APPVL	PLANNER

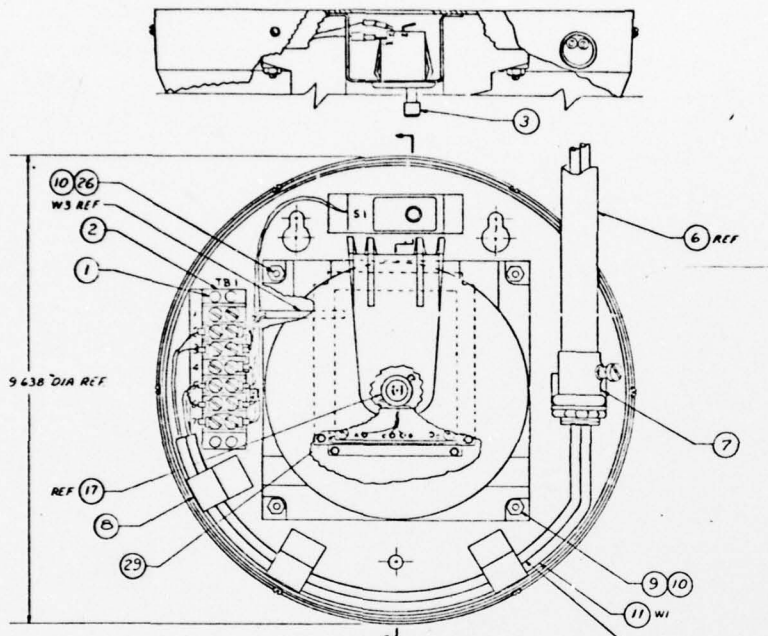
CODE ABBR

A — ADD	B — BUY
C — CHANGE	M — MAKE
D — DELETE	M/B — MAKE & BUY
AS — AS REQ'D	
EA — EACH	
IN — INCH	
FT — FOOT	

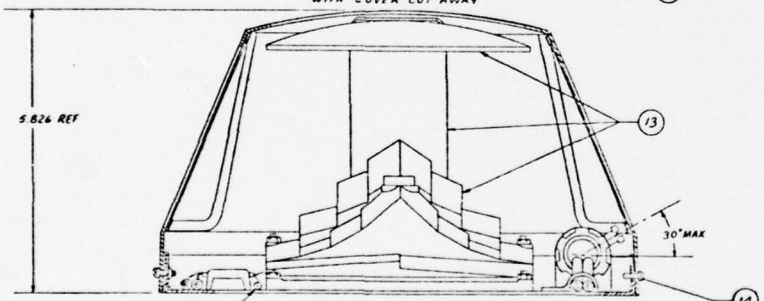
AEROSPACE RESEARCH INC.
BOSTON, MASS.

ASSEMBLY NUMBER PL 490-2100 REV 5

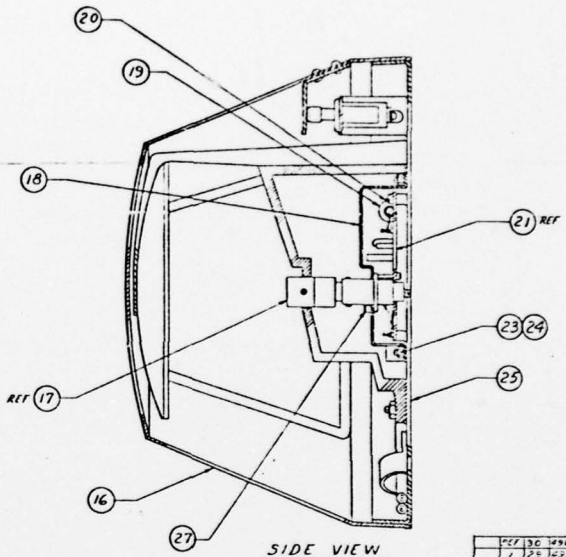
SHEET 5 OF 5



FRONT VIEW
WITH COVER CUT AWAY



BOTTOM VIEW
WITH COVER & BASE SECTIONED AT ℄



SIDE VIEW
SECTIONED AT ℄

WIRING TABLE		
FROM	TO	FUNCTION
W1-CONDUCTOR	TB1-2	RECEIVER OUTPUT
W1-SHIELD	TB1-3	POWER RETURN
W2-CONDUCTOR	TB1-5	TAMPER
W2-SHIELD	TB1-6	+20V
W3-RED	TB1-6	+20V (SEE NOTE 2)
W3-WHITE	TB1-2	RECEIVER OUTPUT
W3-BLACK	TB1-3	POWER RETURN
W3-SHIELD	TB1-3	
S1-NC	TB1-7	TAMPER
S1-COM	TB1-5	TAMPER
TB1-4	TB1-7	TAMPER THRU R1
TB1-2	TB1-9	(USE METAL HOUSE)
TB1-1		SPARE

NOTES:
1. ITEM 6 AND ITEMS 11 & 12, WITH KULKA FLAG LUGS #600 FL ATTACHED AT TB1 TERMINATIONS TO BE SUPPLIED BY CUSTOMER.
2. W3 CABLE ASSY. IS PART OF ITEM 25.
3. LENGTH OF ITEM 22 TO BE DETERMINED AT FOCUS ADJUSTMENT. IF NECESSARY, GRIND FLUSH ALL [illegible]

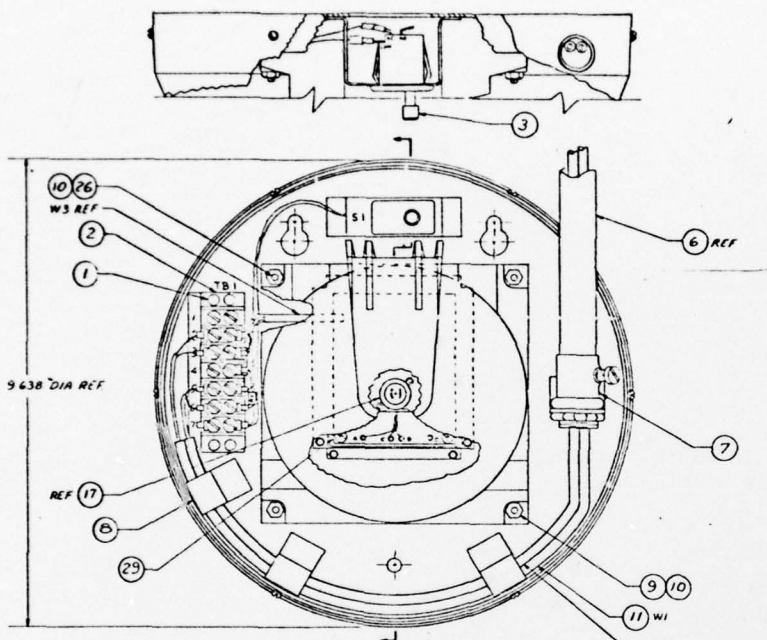
ITEM	QTY	PART NO.	DESCRIPTION
REF	30	490-3101	SCHEMATIC, RECEIVER
1	25	490-2106	DETECTOR, RECEIVER ASSY
1	28		RESISTOR [illegible] R1
2	27		SCREW, CAP, 2-56 [illegible]
2	26		SCREW, MACH, [illegible]
1	25	490-1106	BASE PLATE
8	24		NUT, HEX, [illegible]
8	23		SCREW, MACH, [illegible]
	22		
REF	21	490-2101	P.C. ASSY, RECEIVER (PART OF ITEM 29)
4	20		SCREW, MACH, [illegible]
1	19		GROMMET, [illegible]
1	18	490-1107	SHIELD, R.I. P.C. ASSY
REF	17	490-2102	DETECTOR, [illegible]
1	16	490-1104	COVER
	15		
6	14		SCREW, [illegible]
1	13	481-3001	MIRROR ASSY
REF	12	SEE NOTE 1	CABLE ASSY, [illegible]
REF	11	SEE NOTE 1	CABLE ASSY, [illegible]
4	10		NUT, HEX, [illegible]
2	9		SCREW, MACH, [illegible]
3	8		[illegible]
1	7		CONDUIT, [illegible]
REF	6	SEE NOTE 1	CONDUIT, .32 O.D.
	5		
1	4		
1	3		TAMPER SWITCH, [illegible] S1
1	2		TERMINAL STRIP, [illegible]
2	1		[illegible]

SENSOR ASSY

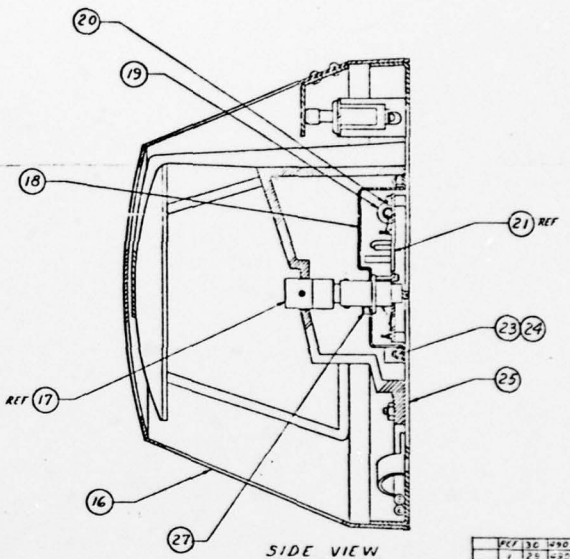
ARESEARCH INC

D E-490-2103 A-3

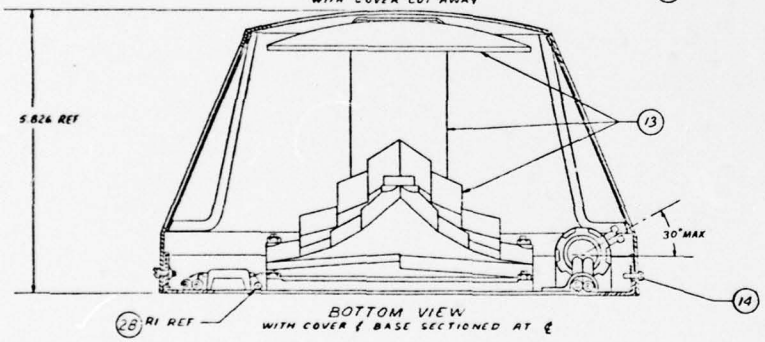
FIG. 5



FRONT VIEW
WITH COVER CUT AWAY



SIDE VIEW
SECTIONED AT ℄



BOTTOM VIEW
WITH COVER & BASE SECTIONED AT ℄

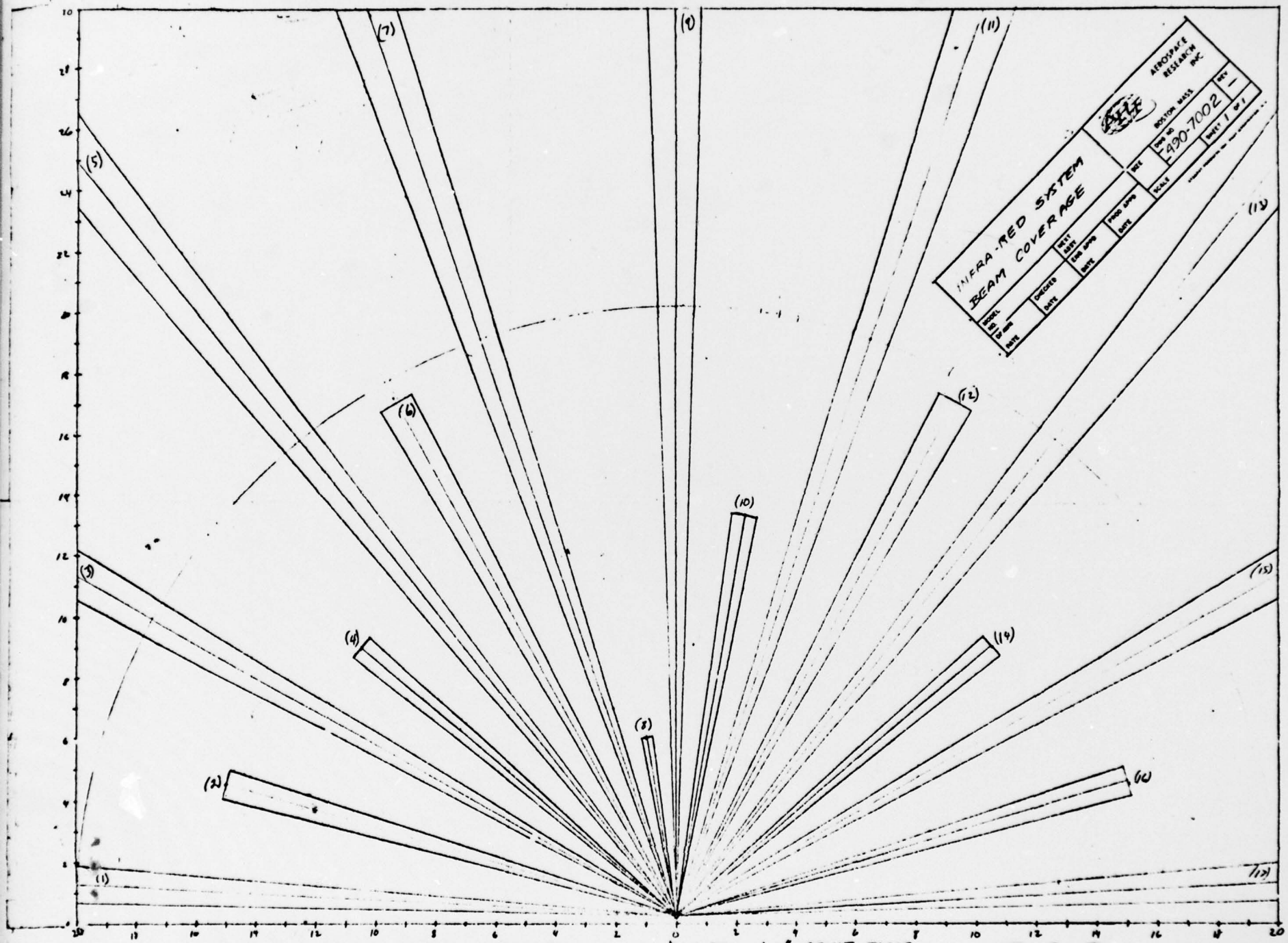
WIRING TABLE		
FROM	TO	FUNCTION
W1-CONDUCTOR	TB1-2	RECEIVER OUTPUT
W1-SHIELD	TB1-3	POWER RETURN
W2-CONDUCTOR	TB1-5	TAMPER
W2-SHIELD	TB1-6	+20V
W3-RED	TB1-6	+20V (SEE NOTE 2)
W3-WHITE	TB1-2	RECEIVER OUTPUT
W3-BLACK	TB1-3	POWER RETURN
W3-SHIELD	TB1-3	
S1-NC	TB1-7	TAMPER
S1-COM	TB1-5	TAMPER
TB1-4	TB1-7	TAMPER (THRU R1)
TB1-3	TB1-4	(USE METAL HOUSE)
TB1-1		SPARE

NOTES:
1. ITEM 6 AND ITEMS 11 & 12, WITH #6 FLAG LUGS & #600 FL ATTACHED AT TB1 TERMINATIONS TO BE SUPPLIED BY CUSTOMER.
2. W3 CABLE ASSY IS PART OF ITEM 25.
3. LENGTH OF ITEM 22 TO BE DETERMINED AT FOCUS ADJUSTMENT. IF NECESSARY, GRIND FLUSH AFTER SPLICING ITEM 13.

	REF	30	490-3101	SCHEMATIC DIAGRAM
	1	29	490-2106	DETECTOR-PIEZO ELEM ASSY
	1	28		RESISTOR [illegible]
	2	27		SCREW CAP [illegible]
	2	26		SCREW MACH [illegible]
	1	25	490-1106	BASE PLATE
	8	24		NUT HEX [illegible]
	8	23		SCREW MACH [illegible]
		22		
	REF	21	490-2101	P.C. ASSY RECEIVER (PART OF ITEM 29)
	4	20		SCREW [illegible]
	1	19		GROMMET [illegible]
	1	18	490-1107	SHIELD R.F. P.C. ASSY
	REF	17	490-2102	DETECTOR [illegible] (PART OF ITEM 29)
	1	16	490-1104	COVER
		15		
	6	14		SCREW MACH [illegible]
	1	13	490-3001	WIRING ASSY
	REF	12	SEE NOTE 1	CABLE ASSY [illegible] W2
	REF	11	SEE NOTE 1	CABLE ASSY [illegible] W1
	4	10		NUT HEX [illegible]
	2	9		SCREW MACH [illegible]
	3	8		PRESS ELIPTITE [illegible]
	1	7		CONDUIT [illegible]
	REF	6	SEE NOTE 1	CONDUIT [illegible]
		5		
	1	4		
	1	3		TAMPER SWITCH [illegible] S1
	1	2		TERMINAL STRIP [illegible]
	6	1		[illegible]

QUALITY APPROVAL		SENSOR ASSY		AIRCRAFT RESEARCH INC.	
				SIZE D	DWG NO. 490-2113 REV A
				SCALE	SHEET 1 OF 1

FIG. 5



COVERAGE OF INFRARED SYSTEM WITH BOTTOM OF BOX MOUNTED 6'10" ABOVE FLOOR
(NOTICE 7'4" ABOVE FLOOR)

FIG 3