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DEC 77 R GELLNER, J WEISEL N00123-76-C-0797
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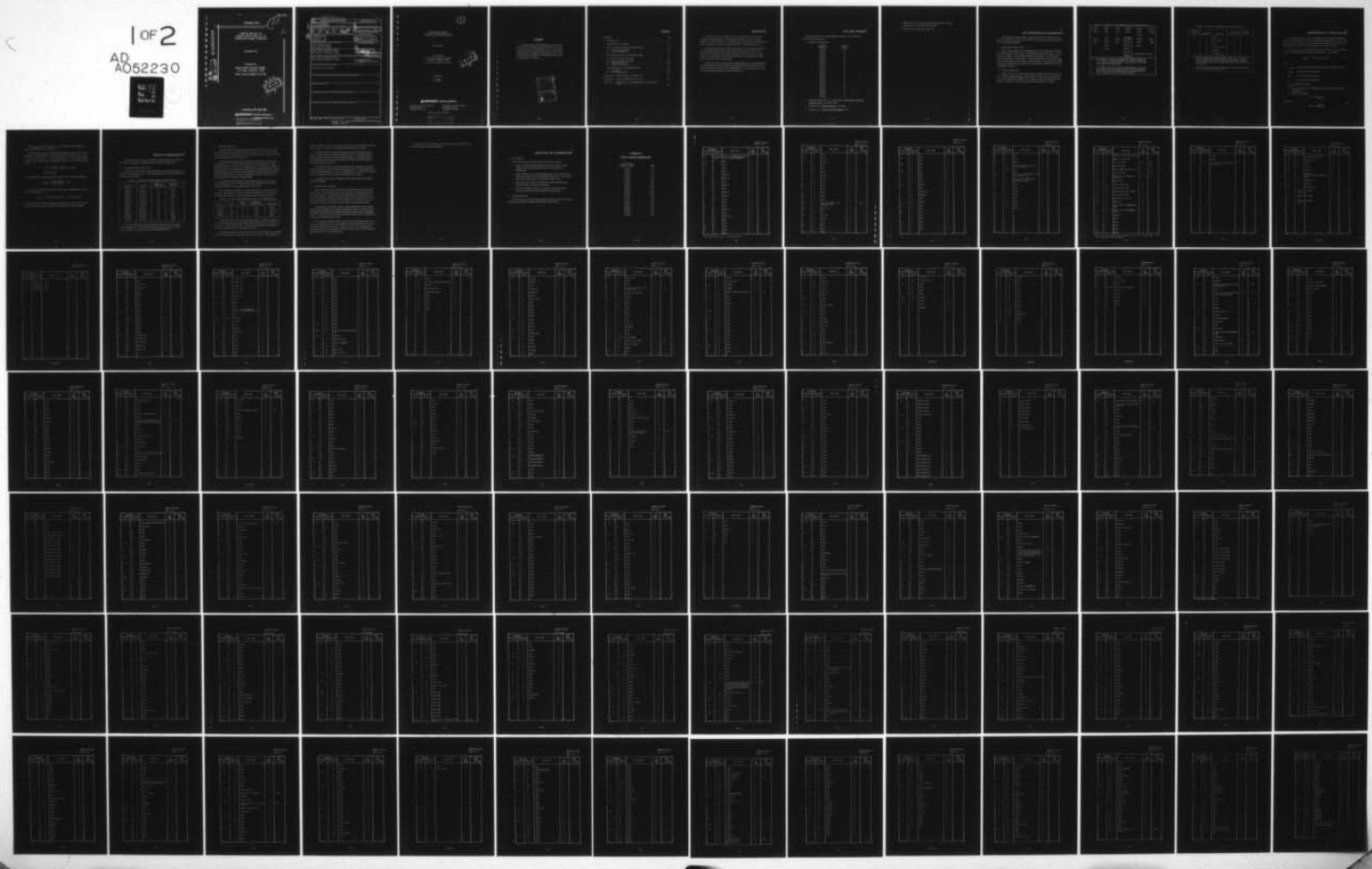

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TECHNICAL NOTE

LOADING ANALYSIS OF CONTROL GROUP CMOS ICs IN TORPEDO MK 46 MOD 5 (NEARTIP)

December 1977

Prepared for

NAVAL OCEAN SYSTEMS CENTER
San Diego, California 92152

Under Contract N00123-76-C-0797

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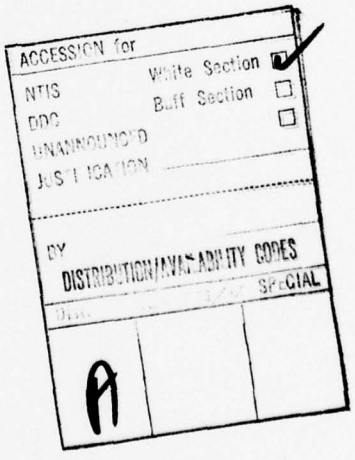
SUMMARY

A loading analysis of CMOS integrated circuits in the Control Group of Torpedo Mk 46 Mod 5 (NEARTIP) was performed for the Naval Ocean Systems Center. The analysis, which included documenting loads and calculating rise times for about 1400 CMOS outputs, revealed no problems related to CMOS fanout or rise time.



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1
INTRODUCTION

As a task under Contract N00123-76-C-0797, ARINC Research Corporation conducted a loading analysis of CMOS integrated circuits in the Control Group of Torpedo Mk 46 Mod 5 (NEARTIP). The purpose of the investigation was to help ensure that the torpedo system will not be degraded because of CMOS loading problems.

This report documents all CMOS fanout numbers and related application factors in the NEARTIP Control Group circuits. Input information to the study included Control Group schematics, change authorizations (CAs) related to revisions of the schematics, direct inputs from Naval Ocean Systems Center personnel, and ARINC Research and Honeywell technical reports.

In this report, applicable documents are listed in Section 2; data compilation and documentation are described in Section 3; the determination of IC output rise time is discussed in Section 4; results of the loading analysis are presented in Section 5; and conclusions and recommendations are given in Section 6.

2 APPLICABLE DOCUMENTS

Source documents for the loading analysis of CMOS ICs in the NEARTIP Control Group are listed below.

a. Control Group Schematics

NEARTIP Schematic	Revision Letter
3235702	D
3235505	F
3235506	E
3235507	D
3235508	D
3235510	E
3235511	D
3235512	D
3235513	E
3235514	E
3235515	E
3235517	E
3235518	E
3235519	E
3235520	E
3235521	E
3235522	E
3235523	E
3235524	D

b. Minneapolis-Honeywell, Inc., letter report, CD4000 Series CMOS Input Capacitance Study, 2 December 1976.

c. Motorola, Inc., MCMOS Handbook, 1974 edition.

d. Textronic, Inc., Textronic Circuit Computer, 1961.

e. ARINC Research Corporation, Design Analysis Reports (DARs), prepared under Contract N00123-76-C-0797.

f. NAVSEA 0967-LP-597-1010, Table VII.

3
DATA COMPILATION AND DOCUMENTATION

For the CMOS IC loading analysis, data from about 475 ICs having about 1425 individual outputs and 5000 loads were recorded. This section describes how the data were compiled and documented.

3.1 CMOS INTERCONNECT DATA

CMOS IC interconnections were identified for every IC output in the 19 schematics of the NEARTIP Control Group. The data include reference designator, section number, pin number, and associated loads for each IC output. The loads include CMOS ICs, resistors, and capacitors. For the identified loads, the reference designator, section number, and pin number are also recorded. These data are presented in Appendix B and illustrated in Table 1 for a portion of the data from Control Group schematic no. 3235514.

3.2 CMOS LOADING DATA

Recorded for every IC output on each of the 19 Control Group schematics were the IC number, output pin number, loads, number of CMOS loads, and rise time (at 70° C) where thought to be significant. These data are presented in Appendix A and illustrated in Table 2 for a portion of Control Group schematic no. 3235514.

TABLE 1. EXAMPLE OF INTERCONNECT DATA FROM APPENDIX B

A5A2	A5B4	A5C6	A5D10	A5E12	A5F15
A6D13	D7A5	D6B9	G7B10	B6D12	(49)
				F7D12	
C8A2	C8B4	C8C6	C8D10	C8E12	C8F15
C6B11	D8C13	A7B5	B6D13	B5A3	(24)
	D7B9		A7A2	A7A2	
	G7B11		B6B5		
			D7A2		
			B6C9	(Schematic No. 3235514)	

(1) Referring to IC C8D10 (block-enclosed for illustrative purposes), "C8" is the IC's reference designator, "D" is the IC section, and "10" is the IC's output pin number. Below the line are five CMOS loads connected to output pin 10.

(2) For CMOS IC A5F15, the value 49 is shown encircled. The 49 is a pin number on the board connector, and the circle indicates that the reference load is physically located on a different NEARTIP board. The total load is documented in Appendix A.

TABLE 2. EXAMPLE OF LOADING DATA FROM APPENDIX A

Reference IC Number	Pin Number	Total Load	Number of CMOS Loads	Rise Time, 10^{-6} sec
C8	2	4013	1	
	4	4023, 12, 13	3	
	6	4023	1	
	10	4011, 23, 11, 12, 11	5	
	12	4027, 23	2	
	15	(4049, 23, 23)	3	

(1) On C8D10 (note enclosed entry in Table 1, which is pin 10 in Table 2), the five CMOS loads are 4011, 4023, 4011, 4012, 4011. If the rise time was significant it would be listed in the last column. Had part of the load been resistive or capacitive, that would be listed in the Total Load column.

(2) Pin 15 has its total load shown in parenthesis, which indicates that the load is on a different NEARTIP board.

4
DETERMINATION OF IC OUTPUT RISE TIME

For calculation of the rise time of IC outputs, much of the input data was provided by the Honeywell letter report, "CD4000 Series Input Capacitance Study", dated 2 December 1976. That report, reproduced herein as Appendix C, provided data on CMOS output transition time, input capacitance, and dynamic impedance.

Rise times of ICs in the NEARTIP system were calculated from the external IC load and the internal dynamic impedance of the IC output. The equation is:

$$T_{R(NT)} = 2.2(Z_{o(int)} + R_{ex})(C_{ex}) \quad (1)$$

where

$T_{R(NT)}$ = Rise time (NEARTIP) from 10% to 90% of the output wave shape

$Z_{o(int)}$ = IC internal dynamic impedance

R_{ex} = Any resistance external to IC

C_{ex} = Any capacitance external to IC.

$Z_{o(int)}$ is calculated as follows:

a. The transition time (T_t) of the chip into a 50 pf load is given in Table 2 of Appendix C.

b. Then, from equation 1,

$$T_t = 2.2\ Z_{o(int)} C_{ex}$$

from which

$$Z_{o(int)} = \frac{T_t}{2.2 \times 50\ pf} \quad (2)$$

With $Z_{o(int)}$ now known and R_{ex} and C_{ex} known from the loading analysis, $T_{R(NT)}$ can be calculated from equation 1.

As an example, consider the NEARTIP CMOS device S/N 4001. From Table 2 of Appendix C, its transition time is 80 nanoseconds with a 50 pf load at 25° C. The transition time increases 0.3%/° C since from equation 2, T_t is directly proportional to $Z_{o(int)}$, values for which appear in Appendix C, page C-4. At 70° C the transition time is:

$$T_t = (80 \times 10^{-9} \text{ sec})\left[\left(1 + \frac{0.3\%}{°C}\right)(70° C - 25° C)\right]$$

$$= 90.8 \times 10^{-9} \text{ sec}$$

or an increase of 10.8 nanoseconds from its value at 25° C. Then, from equation 2,

$$Z_{o(int)} = \frac{90.8 \times 10^{-9} \text{ sec}}{2.2\ (50 \times 10^{-12} \text{ f})} = 825\Omega$$

Assume an external load of 80 pf on the output of the example device. The rise time, from equation 1, is

$$T_{R(NT)} = 2.2(825 + 0)(80 \times 10^{-12} F) = 0.145 \times 10^{-6} \text{ sec.}$$

If this rise time was considered excessive (see discussion, Section 4.2), it would be listed in the Rise Time column of Appendix A and subjected to further analysis.

5
RESULTS OF LOADING ANALYSIS

Results of the loading analysis of CMOS ICs in the NEARTIP Control Group are summarized in this section. Complete data are presented in Appendix A.

5.1 LOADING AND RISE TIME CHART

For CMOS IC outputs having more than nine loads, Table 3 shows the number of loads and the associated rise time. NOSC designated a fanout of nine for CMOS ICs as a design goal for NEARTIP.

TABLE 3. CMOS OUTPUTS WITH MORE THAN NINE LOADS

Drawing No.	IC Number	Number of CMOS Loads	Rise Time, 10^{-6} sec
3235513	B7 Pin 1	12	0.156
3235513	B7 Pin 13	16	0.22
3233514	C7 Pin 6	17	0.36
3235515	C8 Pin 12	11	0.145
3235519	A7 Pin 11	12	0.2
3235519	C8 Pin 12	32	0.6
3235519	F5 Pin 15	13	0.3
3235521	B6 Pin 1	36	1.15
3235521	C8 Pin 2	13	0.36
3235521	D6 Pin 10	20	0.37
3235522	D4 Pin 10	16	0.32
3235522	E7 Pin 2	10	0.301
3235523	D9 Pin 12	10	0.135

Since none of the ICs analyzed have resistive loads that stress their output current capability (most devices are operating at less than 20% of their maximum current rating at 25°C), resistive loads are not included in Table 3.

5.2 RISE TIME ANALYSIS

Clock rates within the NEARTIP Control Group will generally determine what rise time between the IC output and input will be adequate. To ensure proper operation of some ICs, the individual IC may have a specified rise time required at the input. Both of these points will now be addressed.

Excluding the SAC board (Assy No. 3235508), the fastest clock time in the Control Group is 5 kHz. The period for a 5 kHz cycle is 0.20 milliseconds. Using a translation factor of 6, from ref. d of Section 2 (as low as 3 would be acceptable), the minimum rise time for a chip input is $(0.20 \times 10^{-3})/6$ or 0.033 millisecond. Since no rise time greater than 4 microseconds was found in the Control Group, there are no potential clocking problems. In fact, a safety factor of $(0.33 \times 10^{-3})/(4 \times 10^{-6}) = 8$ exists with respect to a possible clocking problem.

The Honeywell report (Appendix C) states that the slowest rise time in the NEARTIP system should be 1.5 microseconds. This calculation was derived from worst-case conditions for all components that affect rise time.

The four ICs with a calculated rise time greater than 1.5 microseconds were examined. The CMOS loads of each were checked to determine if a slow rise time could affect their operation. Table 4 identifies these ICs and their rise times.

TABLE 4. ICs WITH RISE TIMES GREATER THAN 1.5 MICROSECONDS

Dwg. No.	Chip No.	Output Pin No.	CMOS Output Rise Time, μsec	CMOS Loads
3235505	1E	12	3.27	4023
3235505	2A	2	3.30	4011, 12
3235702	C10	1	1.85	4013, 13
3235520	G4	1	3.45	4012

In discussions with an ARINC Research representative, application engineers of RCA and National Semiconductor agree that CMOS devices 4023, 4011, and 4012 are not sensitive to slow input rise times. Factory specification sheets and NEARTIP SIDs do not specify these three CMOS input rise times.

The 4013 chip requires a minimum rise time of 3 microseconds for its clock input. Inputs to the 4013s listed in Table 4 go to the set and reset pins. These inputs do not

require a specific rise time. If the input is present 20 nanoseconds before the clock signal arrives, as is the case in NEARTIP, the chip will operate properly.

The SAC board has an internal oscillator with a resonant frequency of about 240 kHz. Where rise time is important on the SAC board, the chips are interconnected directly to ensure operation at the higher frequency. The highest approximate frequency to enter and leave the SAC board is 5 kHz, which is well within the operating frequency of the board.

The analytical concepts used in the Honeywell report (Appendix C) and in this report are the same. However, ARINC used specific cases in its calculations where Honeywell used an absolute worst case in its calculations. If a worst case had actually occurred, ARINC would have noted and documented it in this report.

In summary, the rise time of CMOS ICs in the control group do not appear to represent a problem.

5.3 CMOS FANOUT ANALYSIS

Table 3 shows that certain CMOS loads in the NEARTIP Control Group range from 10 to 36. The question arises as to how many loads a CMOS IC should have in the NEARTIP system. The Honeywell report (Appendix C) recommends only nine because of rise time constraints. However, it has been shown (Section 4.2) that rise time is not a problem, even on the IC with a fanout of 36. If rise time is the only limitation, then none of the CMOS ICs in the Control Group are fanout-limited.

NAVSEA 0967-LP-597-1010, Table VIII, recommends that a fanout on digital microcircuits be limited to 70 percent of manufacturer rating. If rise time is not a constraint, device manufacturers generally state that a fanout of 100 is acceptable. Since 70% of that value is 70, the worst case fanout of 36 from Table 3 would still have a safety margin of approximately 2-to-1.

From a mission completion point of view, it may be preferential to spread the risk of not completing a mission among different outputs instead of having as many as 36 outputs coming from the same IC. If this is a concern, then a separate study should be implemented to investigate the costs and effectiveness tradeoffs associated with applications of redundant signal paths.

In summary, overloaded outputs on CMOS devices in the NEARTIP Control Group do not appear to represent a problem.

6
CONCLUSIONS AND RECOMMENDATIONS

6.1 CONCLUSIONS

The overall conclusions drawn from this study are the following:

a. Of the 1,425 CMOS circuits analyzed, 13 ICs had a fanout of greater than nine, and four had an output rise time of greater than 1.5 microseconds.

b. A fanout of nine and a rise time no greater than 1.5 microseconds, considered as limiting values by Honeywell (see Appendix C), are not applicable to the CMOS circuits in the NEARTIP Control Group.

c. The design goal for fanout of CMOS devices in the NEARTIP Control Group, also nine, is extremely conservative.

d. All factors considered, there are no problems relating to fanout or rise time in CMOS devices in the NEARTIP Control Group.

6.2 RECOMMENDATION

ARINC Research recommends that no action be taken at this time to reduce the loading effects of CMOS IC outputs in the NEARTIP Control Group.

APPENDIX A

CMOS IC OUTPUT LOADING DATA

Control Group Schematic Number	Page
3235702	A-3
3235505	A-7
3235506	A-9
3235507	A-11
3235508	A-13
3235510	A-17
3235511	A-23
3235512	A-25
3235513	A-27
3235514	A-29
3235515	A-33
3235517	A-41
3235518	A-45
3235519	A-53
3235520	A-59
3235521	A-65
3235522	A-71
3235523	A-79
3235524	A-85

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A6	2||10||6||12||15 *	4012, 1.1K SERIES WITH (3.3K TO -15V, BASE TRANSISTOR)	1	
A10	11	4012	1	
B5	1	4013	1	
	13	4049	1	
B6	2	4013	1	
	4	4015,01	2	
	6	4023,01	2	
	10	4013	1	
	12	4001,25	2	
	15	4011	1	
B7	3	4049,11	2	
	4	4049,11	2	
	10	4013	1	
	11	4015	1	
B8	2	4011	1	
	4	4012,13	2	
	6	4011	1	
	10	4049,13,13	3	
	12	4001	1	
	15	4013	1	
B9	13	4012	1	
C5	2	4023	1	
	13	4012	1	

*The symbol "||" denotes "in parallel with".

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
C5	12	4011	1	
C6	2	(4049)	1	
	4	(4001,49)	2	
	6	4011	1	
	10	4013	1	
	12	4013	1	
C7	3	4001,15	2	
	4	4050	1	
	10	4049	1	
C8	1	4023	1	
	2	4011	1	
	12	4025	1	
C9	9	4013	1	
	10	4013	1	
C10	1	4013,20K SERIES, 33PF PARALLEL, 4013	2	1.85
D5	2	(4001, 01)	2	
	13	4013	1	
D6	5	4012,12	2	
	4	4012,12	2	
	12	4049	1	
D7	9	4013	1	
	6	4012	1	
	10	4013	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
D9	1	4013	1	
	13	4012	1	
D10	1	4011	1	
	13	4013	1	
E5	3	4012	1	
	4	4001	1	
	10	4013	1	
	11	4025	1	
E6	2	4049,12	2	
	4	4001	1	
	6	4001,12,12	3	
	10	(BLANK)	0	
	12	4049	1	
	15	4011,01	2	
E7	1	4049	1	
	13	4023	1	
E8	3	4013	1	
	4	4013	1	
	10	4013	1	
E9	9	4013	1	
	6	4012	1	
F5	1	4013	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
F6	4	4013	1	
	11	4049	1	
F7	1	4015,23	2	
	13	4049,49,49,49,49,12, (100 K parallel 30PF)	6	
	12	4012	1	
F8	1	4001 ,13,12,36K SERIES 33 PF IN PARALLEL, 4013	4	
	13	4013,25, 36K SERIES 33 PF IN PARALLEL, 4013	2	
G5	1	4013	1	
	2	4011	1	
	12	4049,11	2	
G6	2	4001	1	
	4	4001	1	
	6	4025	1	
	10	4013	1	
	15	4013	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
1A	2	1800PF parallel 22K, 4012, 12	2	
1B	4	CD4011,11, (4013,12)	4	
1C	6	1K series 75PF	0	.296
1D	10	1K series 75PF	0	.296
1E	12	CD4023,1800PF parallel, 22K	1	3.27
1F	15	1K series 75PF	0	2.96*
2A	2	CD4011,11,12,12,1800PF parallel 22K	4	3.3
2B	4	CD4011,11,11	3	
2C	6	2.7K parallel 75PF	0	
2D	10	2.7K parallel 75PF	0	
2E	12	CD4023,22K parallel 1800PF	1	
2F	15	2.7K parallel 75PF	0	
3A	3	CD4012,12,12,12,23,23	6	
3B	4	CD4012,12	2	
3C	10	36K in series (INSTRUMENTATION)	0	
3D	11	36K in series (INSTRUMENTATION)	0	
4A	2	CD4050,27	2	
4B	1	CD4027	1	
5A	1	CD4050	1	
5B	13	CD4049	1	
6A	1	CD4050	1	
6B	13	CD4049	1	

*Since there are no CMOS loads connected to 1F pin 15, the rise time of 2.96 microseconds presents no problems.

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
7A	9	CD4050	1	
7B	6	CD4050	1	
7C	10	36K in series with (INSTRUMENTATION)	0	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
2A	3	CD4050,50,50,50,50,50	6	
2B	4	CD4011,11,12	3	
2C	10	27PF	0	
2D	11	CD4040	1	
3A	3	CD4011,11	2	
3B	4	CD4011,11 15K in series 47K parallel 25PF	2	
3C	10	CD4011,11,49	3	
3D	11	CD4011	1	
4B	4	CD4049,49,49	3	
4	F15||D 10||E12	650 OHMS	0	
5	A2||B4|| C6	650 OHMS	0	
5	D10||E12 ||F15	650 OHMS	0	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
1	2||4||6	650 Ω	0	
1	10||12||15	650 Ω	0	
2	2||4||6	650 Ω	0	
2	10||12||15	650 Ω	0	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A4	1	4011	1	
	2	4011,20,27	3	
	12	4011,27,11	3	
A5	4	4023	1	
	5	4023	1	
	7	4023	1	
	14	4023	1	
	12	4023	1	
	13	4023	1	
A6	9	4011	1	
	6	4011	1	
	10	4001	1	
A7	10	4050	1	
	11	4050	1	
	12	4050	1	
	13	4050	1	
A8	2	3 MEG, 2PF	0	
	4	3 MEG, 2PF	0	
	6	3 MEG, 2PF	0	
	10	3 MEG, 2PF	0	
	12	3 MEG, 2PF	0	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A9	2	3 MEG, 2PF	0	
	4	3 MEG, 2PF	0	
	6	3 MEG, 2PF	0	
	10	3 MEG, 2PF	0	
	12	3 MEG, 2PF	0	
A10	4	4013,13,20	3	
	10	4015	1	
B4	3	4013	1	
	4	4013	1	
	10	75K to (INSTRUMENTATION) Direct To (4036, 11, 23, 11)	4	
	11	4049	1	
B5	2||4||6	550 OHMS	0	
B6	3	4020,20	2	
	4	4011	1	
	10	4020,01	2	
	11	4050,50,50	3	
B7	9	4001	1	
	5	4019	1	
	4	4019	1	
	6	4019	1	
	13	4019	1	
	12	4019	1	
	14	4019	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
B7	15	4019	1	
	1	4019	1	
	2	4019	1	
	3	4019	1	
B8	7	4019	1	
	5	4019	1	
	4	4019	1	
	6	4019	1	
	13	4019	1	
	12	4019	1	
	14	4019	1	
	15	4019	1	
	12	4019	1	
B9	10	4050	1	
	11	4050	1	
B10	11	4001,49, (4049,49,49,49,49, 49)	8	
C5	2	4011,01	2	
	4	4020,13,13,15	4	
	6	4011,11 (BLANK)	2	
	10	OSC	0	
	12	4011, OSC	1	
	15	4001, (4011,11)	3	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
C6	3	4011	1	
	4	(4002,49,49,49,49,49,49,49)	8	
	10	4027,27	2	
C7	1	4019,01,19,19	4	
	2	4019,49,01,19,19	5	
	15	4011	1	
C9	10	4050	1	
	11	4050	1	
	12	4050	1	
	13	4050	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A4	9	(BLANK)	0	
	6	CD4049	1	
	10	4049	1	
A6	2	CD4011,23	2	
	4	CD4011,23	2	
	6	CD4011	1	
	10	4023, (4011)	2	
	12	4011	1	
A7	4	4023	1	
	10	4023	1	
	11	4049	1	
B4	3	4049	1	
	4	4013	1	
	10	4049	1	
	11	4013	1	
B5	1	4012	1	
	13	4049,49,49	3	
B6	2	4023	1	
	4	4023	1	
	6	4023	1	
	10	4011,11	2	
	12	(27PF)	0	
	15	4023	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
B7	9	4011,11,12	3	
	6	4023	1	
	10	4012	1	
C2	1	4011,23,11, (27PF, 27PF, 4023, 27PF)	4	.12
	2	4013,49 (4013,01)	4	
	13	(4011)	1	
C3	4	4012	1	
	12	4012	1	
	15	4023	1	
	1	4023	1	
	2	4012	1	
	3	4023	1	
C4	1	4011	1	
	2	4011,11	2	
	12	(BLANK)	0	
C5	6	4012	1	
	10	4011	1	
C6	2,4,6	((650 OHMS)	0	
	10	4011,12,13 (27PF)	3	.01
	12	4012, (BLANK)	1	
	15	4013	1	
C7	9	4013	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
C7	6	4011,12	2	
	10	4023,12,11,12	4	
D2	1	(BLANK)	0	
	13	(BLANK)	0	
	12	4011, (4013,15,13,13,13,13, 11)	8	.01
D3	12	4012	1	
	14	4011	1	
	15	4011,11	2	
	1	4012	1	
D4	1	4011	1	
	13	4011	1	
D5	3	4012	1	
	4	4013	1	
	10	4011	1	
	11	4011	1	
D6	3	4049	1	
	4	4049	1	
	10	4011	1	
	11	4011	1	
E2	9	4049	1	
	6	4049	1	
	10	4049	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
E3	5	4023	1	
	13	4023,23	2	
	12	4023,23	2	
	15	4012	1	
	1	4012,23	2	
	3	4013	1	
E4	1	4049	1	
	13	4049	1	
E5	1	4023,12,11,23	4	
	12	4011	1	
E6	2	4011	1	
	4	4012	1	
	6	(27PF)	0	
	10	(BLANK)	0	
	12	4013,13	2	
E7	1	4013	1	
	2	4013	1	
	12	4020	1	
	13	4011	1	
F3	2	4020,20,13,13	4	
	4	4013	1	
	6	4013	1	
	10	4013	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
F3	12	4049,11	2	
	15	4013,13,13,13	4	
F4	3	4020	1	
	4	4023	1	
	10	4013	1	
	11	4020	1	
F5	13	4949,13	2	
G5	3	4012,11	2	
	4	4013	1	
	5	(BLANK)	0	

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REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
1A	3	4023,23	2	
1B	4	4011	1	
1C	10	4023	1	
1D	11	4023	1	
2A	9	4023	1	
2B	6	4013	1	
2C	10	4023	1	
3A	9	4023	1	
3B	6	4013	1	
3C	10	4049	1	
4B	13	4013	1	
4B	12	4013,4012	2	
5A	2	4023	1	
5B	12	4023	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
1A	2	4023,23	2	
B	4	4023,12,12	3	
D	10	4012	1	
E	12||F 15	15K series 2.2K 30PF	0	
2A	9	29PF	0	
B	6	29PF	0	
C	10	29PF	0	
3A	1	29PF	0	
B	13	29PF	0	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A7	1	4011,13	2	
	13	4049,10	2	
B7	1	MM42030,4011,12,01,11,11,23, 01,12,01,49,13	12	.156
	2	4011,23	2	
	13	4012,11,11,11,23,12,49,11,01, 23,25,11,23,49,13,49,	16	.22
	12	4011	1	
C7	3	4013	1	
	4	4049	1	
	10	BLANK	0	
C8	2	4020,20,20.13,13	5	
	4	4020,13	2	
	10	4001,100K,MM42030	1	
	12	4011,20,13	3	
	15	4013	1	
C9	2	4019,100K	1	
	4	4001,01,49,29,29,01,MM42030, 100K	7	.15
	6	4001,100K	1	
	10	MM42030,100K	0	
	15	4049,11,11,11,49,100K	5	.05
D7	1	4011	1	
	13	4011	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
D8	13	4012	1	
D9	2	4025,25,25,13,100K	4	
	4	4025,13,13,11,13,100K	5	
	6	4023,11,100K	2	
E7	A	4013,49	2	
E8	7	4012	1	
	5	4012	1	
	4	4012	1	
E9	4	4011	1	
	13	4011	1	
F8	2	4011	1	
	10	4013	1	
	12	4011	1	
F7	9	4012	1	
F8	15	4023	1	
E7	10	4049	1	
	4	4011	1	
F8	6	4011	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A5	2	4001	1	
	4	4012	1	
	6	4013	1	
	10	4013	1	
	12	4011	1	
	15	(BLANK)	0	
A6	3	4049,25	2	
	4	4025	1	
	10	4002	1	
	11	4013	1	
A7	9	4013	1	
	6	4023	1	
	10	4013	1	
B5	2	4013	1	
	15	4012,23	2	
	14	4025,15	2	
B6	3	4011	1	
	4	4013	1	
	10	4027,13,13	3	
	11	4013	1	
B7	3	4012	1	
	4	4027	2	
	10	4023	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
B7	11	4002,(4049,23,23)	4	
C5	12	4027	1	
C6	2	4011	1	
	12	4013	1	
	13	4012,23,12,(4011,49,23)	6	
C7	9	4025	1	
	6	4012,01,49,25,(MM420,4050,11, 30,49,02,49,01,12,49,01,49,02	17	.36
C8	2	4013	1	
	4	4023,12,13	3	
	6	4023	1	
	10	4011,23,11,12,11	5	
	12	4027,23	2	
	13	(4049,23,23)	3	
C9	9	(4023,12)	2	
	6	4001	1	
D6	1	4001,11,12 (4011,12,25,49,49)	8	
	2	4027,27,01,11	4	
	13	(4050,25,49)	3	
D7	1	4002	1	
	13	4011	1	
D8	10	4011	1	
D9	1	(30PF,23,23,23,12,12)	0	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
D9	13	(4013,13)	2	
E6	2	4012	1	
	13	4025	1	
E7	1	(4050,01,02,01,27,01,49)	7	.01
	13	4013	1	
E8	3	4012	1	
	10	4002	1	
	11	4011	1	
F7	11	4023	1	
	10	4012	1	
G7	2	4011	1	
	12	(4001)	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A1	1	4030	1	
	2	4013	1	
	13	4013	1	
A2	5	4011	1	
	10	4011	1	
	12	4001	1	
A3	13	4025	1	
	4	4012	1	
	10	4013,25	2	
	11	4012	1	
A4	3	4011	1	
	4	4029,29	2	
	10	4012	1	
	11	4012	1	
A5	1	4027,01,42,42,42,42	6	
	15	4011	1	
	14	4011	1	
A6	3	4012	1	
	4	4012,12	2	
	10	4011,11	2	
	11	4011,01	2	
B1	2	4023	1	
	4	4001	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
B1	6	4023	1	
	12	4013,01	2	
	15	4013	1	
B2	9	4024	1	
	6	4019	1	
	10	4049,13	2	
B3	2	4024	1	
B3	12	4001	1	
B4	1	4019	1	
B5	7	4001,23	2	
	4	4001	1	
	6	4001,13	2	
	10	4002,02,12	3	
	12	4002	1	
	15	4013,11,27,13,15	5	
B6	3	4025	1	
	4	4023	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
B6	10	4027	1	
	11	4025	1	
B7	9	4001	1	
	6	4011,02,49,19,19	5	
	10	4011,11	2	
C2	3	4013,01	2	
	4	4001,02,01,25	4	
	10	4023	1	
	11	4013	1	
	3	4001,25,01	3	
C3	3	4013	1	
	4	4011	1	
	10	4011	1	
	11	4001	1	
C4	1	4013	1	
	13	4019	1	
C5	6	MM42030,MM42030	2	
	11	MM42030,MM42030	2	
	14	MM42030,MM42030	2	
	2	MM42030,MM4203	2	
	7	4029	1	
C6	1	4013	1	
	2	4011	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
C6	13	4013	1	
C7	1	4025	1	
	2	4011	1	
	13	4025,13,13	3	
	12	4001,15	2	
C8	2	4013,29,49,13,15,13,13	7	
	4	4001	1	
	6	4023	1	
	10	4001	1	
	12	4013,13,13,13,13,13 4013,13,13,13,29	11	.145
	15	4019,19	2	
C9	3	(BLANK)	0	
	10	4001	1	
	11	4049	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
D1	4	4012,12	2	
	3	4002	1	
	6	4011	1	
	15	4015	1	
	11	4023,29	2	
D2	1	4013,02	2	
	2	4011	1	
	13	4013	1	
D3	1	4011	1	
	13	4011,12	2	
D4	12	4030	1	
	11	4030	1	
	9	4030	1	
	6	4030	1	
	5	4030	1	
	4	4030	1	
	3	4030	1	
D5	13	4029	1	
	12	4029	1	
	11	4029	1	
	10	4029	1	
D6	1	4019	1	
	13	4019	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
D7	1	4019	1	
	13	4019	1	
D8	3	4025	1	
	9	4025	1	
	12	4025,49,11	3	
	1	4001	1	
D9	3	4001	1	
	10	4011	1	
	12	4001,02	2	
	1	4011,23	2	
E2	1	4015	1	
E2	1	4001	1	
	13	4013	1	
E3	1	4012	1	
	13	4012	1	
E4	3	4002	1	
	4	4002	1	
	10	4002	1	
	11	4013	1	
E6	1	4019	1	
	13	4019	1	
E7	1	4019	1	
	13	4019	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
E8	6	MM42030,42030	2	
	11	MM42030,42030	2	
	14	MM42030,42030	2	
	2	MM42030,42030	2	
E9	3	4012,11,49,49,23	5	
	10	4001	1	
	12	4001	1	
	15	4011	1	
F3	3	4002	1	
	4	4002	1	
	10	4002	1	
	11	4002	1	
F8	13	4029	1	
	12	4029	1	
	11	4029	1	
	10	4029	1	
F7	4	4013,100K,30,42	3	
	5	4013,100K,30,42	3	
	6	4013,100K,30,42	3	
	7	4013,100K,30,42	3	
	8	4013,100K,3042	3	
	9	4013,100K,3042	3	
	10	4013,100K,30,42	3	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
F7	11	4013,100K,42	2	
F4	4	4049,100K,42	2	
	5	4042,100K,49	2	
	6	4011,100K,42	2	
	7	4002,100K,42	2	
	8	4042,100K	1	
	9	4042,100K	1	
	10	4042,100K,42	2	
	11	4049,100K,02,13,11	4	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A5	2	10 K series 30PF parallel 2K	0	.14
	4	4013,13,10K series 30PF parallel 2K	0	.14
	6	4013	1	
	10	4013	1	
	12	4001,01	2	
	15	4001	1	
A7	3	4049	1	
	4	30PF parallel 30PF parallel 130K	0	.18
	10	4049	1	
	11	30PF parallel 130K	0	
B4	4	4013	1	
	10	4013	1	
	11	4013	1	
	2	4025	1	
	12	4013	1	
B7	9	30PF	0	
	6	4023,49	2	
	10	4013	1	
C4	3	4025	1	
	4	4013	1	
	11	4013	1	
	10	4025	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
C5	2	MM42030	1	
	4	4011	1	
	6	MM42030	1	
	10	4015	1	
	15	MM42030	1	
C6	1	4011	1	
	13	MM42030	1	
C7	3	4011	1	
	4	4011	1	
	10	4013	1	
	11	4049	1	
C8	2	4011,13,20,15,13,11	6	
	4	10K series 30PF parallel 2K	0	.14
	6	4011	1	
	10	4023,11	2	
	12	30PF parallel 30PF parallel 30K	0	.18
	15	4049	1	
C9	3	4020	1	
	4	4020	1	
	10	4020	1	
	11	4001,11	2	
D4	2		0	
	13	4001	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
D5	9	MM42030	1	
	12	MM42030	1	
	1	4011	1	
D6	1	4025,01	2	
	13	MM42030	1	
D7	1	MM42030	1	
	13	MM42030	1	
D8	6	4011,12	2	
	13	4011	1	
	12	4012	1	
	14	4012	1	
	1	4012	1	
D9	5	4011	1	
	12	4011	1	
E6	1	4013	1	
	13	4042,20,13,20,15,13	6	
E7	9	10K series 30PF parallel 2K	0	
	6	MM42030	1	
	10	4049	1	
E8	7	4023	1	
	5	4023	1	
	4	4011,4011	2	
	6	4012	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
E8	12	4012	1	
	14	4012	1	
	1	4012	1	
F4	11	100K parallel 4049	1	
	10	100K parallel 4049, 49	2	
	9	4042 parallel 100K	1	
	8	100K parallel 4042	1	
	5	100K parallel 4015	1	
	4	100K parallel 4042	1	
F5	11	100K parallel 4025	1	
	10	100K parallel 4001	1	
	9	100K parallel 4001	1	
	8	100K parallel 4001	1	
	7	100K parallel 4049	1	
	6	100K parallel 4049	1	
	5	100K parallel 4011	1	
	4	100K parallel 4013	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A1	2	24K series 20K parallel 30PF	0	.7
	4	4023,13,13	3	
	6	4011	1	
	10	4013	1	
	12	4012	1	
	15	4023,12,12	3	
A2	4	4002	1	
	3	4002	1	
	12	4002,01	2	
	11	4002,11	2	
A3	2	4011	1	
	13	4011	1	
A4	1	4001,01,23	3	
	2	4025,01	2	
	13	4001,01,23	3	
	12	4025,01	2	
A5	9	4049,13	2	
	6	4013	1	
	10	4013	1	
A6	1	4023	1	
A7	3	4013	1	
	4	4011	1	
	10	4023	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A7	11	4013,25,25,25,13,25,25	7	.01
B2	4	4002,01	2	
	3	4002,01,11	3	
	12	4002	1	
	11	4002,01,11	3	
B3	3	4015	1	
	4	4015	1	
	10	4015	1	
	12	4015	1	
B4	1	4011,01,01	3	
	2	4023	1	
	13	4001,01,11	3	
B5	2	4023,15	2	
	12	4013	1	
B6	2	4023,11	2	
	12	4025,25	2	
B7	3	4025	1	
	4	4049	1	
	10	4013,13	2	
	11	4049,25,15,12,23,12 (4049,01 01)	9	
C2	2	4011	1	
	4	4013,23	2	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
C2	6	4013	1	
	12	(4011)	1	
	15	4013	1	
C3	3	4023	1	
	4	4023	1	
	10	4012	1	
	11	4049,13,27,27,13	5	
C4	1	4011	1	
	12	4013,20	2	
C5	2	4049	1	
	14	4027	1	
C6	9	4049	1	
	10	4011, (4011)	2	
C7	12	4012	1	
	11	4012	1	
	9	4012	1	
	5	4012,12	2	
	4	4012,12	2	
C8	2	4020,13,13	3	
	4	4011	1	
	6	4025,25	2	
	10	4025,25	2	
	12	4012	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
C8	15	(4011)	1	
C9	1	4001	1	
	12	4011,13,01	3	
D2	2	4011	1	
	13	4027, (4001,02)	3	
	12	4011	1	
D3	1	4013	1'	
	13	4011,11,11,11	4	
D4	3	4001	1	
	4	4023	1	
	10	4013	1	
	11	(4001)	1	
D5	2	4013,13	2	
	4	4012	1	
	6	4011	1	
	10	(130K parallel 20PF)	0	
	12	4011	1	
	15	4023	1	
D6	1	4049,13,15,15,15,15,13	7	
	13	4049	1	
D7	9	4013	1	
	6	4013	1	
	10	4049	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
D8	1	4013	1	
	2	4012	1	
	13	4013	1	
D9	2	4011	1	
	13	4011, (4049,49)	3	
	12	4025	1	
E2	3	4011	1	
	4	4011	1	
	10	4011	1	
	11	4011	1	
E3	3	4049	1	
	4	4011	1	
E4	2	4012	1	
	13	4013	1	
E5	13	4011	1	
E6	9	4013	1	
	6	4013	1	
	10	4015	1	
E7	3	4011	1	
	4	4023	1	
	10	4013	1	
	11	4012	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
E8	6	4023	1	
	13	4023	1	
	12	4023	1	
E9	9	4011,23	2	
	6	4013	1	
	10	(4023,23)	2	
F3	1	4049	1	
	13	4049	1	
F4	3	4012	1	
	4	4011,11,12	3	
	10	4015	1	
	11	4049	1	
F5	1	4023	1	
	12	4011	1	
F6	2	4023	1	
	12	4023	1	
F7	1	4013	1	
	13	4013	1	
	10	4013	1	
G4	9	4013,15,49	3	
	10	4023	1	
G5	1	4023	1	
	13	4023	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
G5	1	4023	1	
	13	4023	1	
G6	3	4013,13	2	
	4	4013	1	
	10	4013	1	
G7	2	4011	1	
	12	4011	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A3	5	4023	1	
	6	4023	1	
	11	4023	1	
A4	3	4001	1	
	4	4013	1	
	10	4013	1	
	11	4001	1	
A5	13	4049	1	
	11	4011	1	
	4	4029,29,01	3	
A6	1	4011	1	
	13	4025,15	2	
A7	3	4024	1	
	4	4001	1	
	10	4025,13,13,13,01,11,27,49,15	9	
	11	4025,13,01,13,12,13,27,12,49, 13,49,13	12	.2
B3	9	4024,11	2	
	6	4002	1	
	10	4013	1	
B4	3	4013	1	
	4	4013	1	
	10	4013	1	
	11	4027,13	2	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
B5	2	4001	1	
	4	4023	1	
	6	4011	1	
	10	4013,13	2	
	12	4001	1	
	15	100K,27PF,49	0	
B6	13	4013,11,01	3	
B7	3	4001,01,25	3	
	26	4011	1	
	10	4001	1	
C2	1	4027,01,BLANK	2	
	15	4001	1	
C3	1	4025	1	
	13	4023	1	
C4	1	4050,12,49,MM42030,MM42030	5	
	13	4011,02	2	
	12	4025	1	
C5	2	4001,01	2	
	15	BLANK	0	
C6	9	4013	1	
	6	4049,11	2	
	10	4049	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
C7	3	4015	1	
	4	4013	1	
	10	4024	1	
	11	4011,11,11	3	
C8	2	4049,17,12,12,11,MM42030	5	
	4	4011	1	
	6	4011,13,25,27,15	5	
	10	4011,12	2	
	12	4013,49,13,27,11,13,13,13, 24,13,13,15,13,49,13,23,01, 13,12,24,23,49,49,49,13,49, 49,13,15,15,49,13,13	32	.6
C9	3	4011	1	
	9	4049,12 BLANK	2	
	15	4011	1	
	12	4012	1	
D3	3	4002	1	
	11	4002	1	
	4	BLANK		
D4	2	4001,11	2	
	1	4001,27,02,MM42030	3	
	13	4011,25,27,11, BLANK	4	
	12	4011	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
D5	3	4027,29	2	
	4	MM42031	0	
D6	2	4049,11,49,01,23	5	
	12	4001	1	
D7	3	4042	1	
	4	4042	1	
	10	4042	1	
	11	4001,01,01,11,15	5	
D8	5	4001	1	
	4	4001	1	
E4	1	4029,29	2	
	13	4049,27,50,01	4	
E5	5	MM42031	0	
	6	MM42031	0	
	9	MM42031	0	
	11	MM42031	0	
	12	MM42031	0	
E9	2	4001	1	
	10	4027,49,11,12,12	5	
	9	4013	1	
	11	4025,49	2	
	12	30PF	0	
	1	4001	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
E9	15	4013	1	
D9	2	4027	1	
	10	4011,13	2	
	9	4011,49	2	
	12	4025	1	
	1	4013,11,13	3	
F4	9	4049	1'	
	12	4040	1	
F7	11	4029,42,42,42,100K	4	
	10	4029,42,42,42,100K	4	
	9	4029,42,42,42,100K	4	
	8	4029,42,42,42,100K	4	
	7	4029,01,100K	2	
	6	4029,01,100K	2	
	5	4029,01,100K	2	
	4	4011,15,100K	2	
*F8	7	4029,29	2	
*F8	7	4001,11	2	
F5	2	4011	1	
	4	4013	1	
	6	OSC	0	
	10	OSC	0	

*SAME NUMBER ON SCHEMATIC

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
F5	12	4027	1	
	15	4015,15,13,24,49,49,49,49, 49,49,49,49,49	13	.3
E7	9	4013	1	
E7	10	4013,27	2	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A2	1	4027,12,12	3	
	2	4012	1	
	14	4027,12,12,13	4	
A3	1	4023	1	
	13	4049	1	
A4	10	4013	1	
A5	12	4013	1	
A7	3	4024	1	
	4	4012	1	
	10	(4013)	1	
	11	4013	1	
B1	5	4011	1	
	4	4011	1	
B2	1	4001,13,12	3	
	2	(4012,13,13,13,49,49)	6	
	13	4001	1	
	12	4012,27	2	
B3	4	(4049)	1	
	10	4002	1	
B4	9	4001	1	
	6	4001	1	
B6	3	4012	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
	4	4013	1	
	10	4012	1	
	11	4049	1	
B5	2	4013,01,13,01,11,01	6	
	12	4012	1	
	4	4012,01	2	
	6			
	10	4002	1	
	15	4001,01	2	
B7	3	4001	1	
	4	4013	1	
	10	4029	1	
	11	4012	1	
C1	1	4011	1	
	2	4013	1	
	13	4011	1	
C2	3	4013	1	
	4	4023	1	
	10	4013	1	
	1	4012	1	
C3	1	4049,27,12,15	4	
	13	4049	1	
C4	2	4011	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
	13	4002,11	2	
C5	1	4013	1	
	2	4011	1	
	13	4013	1	
	12	4001	1	
C6	2	4013	1	
	10	4001	1	
	11	4001	1	
C7	1	4015	1	
	13	(4011)	1	
C8	12	4023	1	
	4	(4011)	1	
C9	2	4023,13	2	
	4	4011	1	
	6	4011	1	
	10	4015,15,02,27,27	5	
	12	4001,13,13,30PF	3	
	15	4013,13,13,15	4	
D1	12	4011	1	
D2	1	4011	1	
	13	4011	1	
D3	1	4049	1	
	13	4012	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
D4	9	4013	1	
	6	4002	1	
	10	4002	1	
D5	2	4001	1	
	4	4025	1	
	6	4013	1	
	10	4012	1	
	12	4013	1	
	15	4013	1	
D6	1	MM42030	1	
	13	4015	1	
D7	1	4011	1	
	2	4020	1	
	13	4011	1	
D8	13	4012	1	
D9	9	4015,13	2	
	6	4012	1	
	10	4001,01	2	
E2	3	4023	1	
	10	4012	1	
	11	4013	1	
E3	3	4011	1	
	4	4012	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
	10	4012	1	
E4	13	4023	1	
E5	3	4012	1	
	4	4049,11	1	
	11	4025	1	
E8	4	4049	1	
	12	4001,01	2	
	11	4013	1	
E9	2	4011	1	
	4	4012,01	2	
	6	4013	1	
	10	4001,01,01	3	
	12	4049,15,15,13,20	5	
	15	4012	1	
F9	11	4015,100K	2	
	6	4001,100K	2	
	9	4001,100K	2	
	8	4001,100K	2	
	7	4001,100K	2	
	6	4001,100K	2	
	5	4001,100K	2	
	4	4001,100K	2	
G4	1	36K To 33PF in Parallel with 4012	1	3.45

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
	1	4012	1	
	2	4012	1	
	13	(BLANK)	0	
G5	7	4015	1	
B3	11	4001,12	2	
	3	4025	1	
E7	10	MM42030	1	
	4	4013	1	
	3	MM42030	1	
E4	1	4001	1	
B5	12	4012	1	
A4	9	4001	1	
A6	3	4011	1	
	11	4011	1	
	4	4012	1	
E3	11	4025,49,02	3	
C6	4	4049,13	2	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A2	2	4013	1	
	3	4013	1	
	4	4001	1	
	10	(BLANK)	0	
	11	4013	1	
A4	1	4011	1	
	13	4027,49	2	
A5	2	4013,11,23	3	
	4	4001	1	
	6	4013,11,13	3	
	10	4023	1	
	12	4001	1	
	15	4012	1	
A6	9	4012	1	
	6	4001	1	
A7	4	4013	1	
	10	4013	1	
	11	4023, (4001)	2	
B2	2	4027	1	
	13	(4023)	1	
B3	1	4001	1	
	13	4001	1	
	12	4001	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
B4	3	4011	1	
	4	4013	1	
	10	4023,49,11,(4049,49)	5	
	6	4013,12,12	3	
	11	4013,27	2	
B5	2	4027	1	
	4	4011	1	
	6	4027	1	
	10	4013	1	
	12	4001	1	
	15	4001	1	
B6	1	4012,01,23,12,11,01,01,(4050, 49,01,25,11,13,27,25,49,49, 12,23,49,11,49,49,23,11,11, 12,49,23,49,11,11,49,49,25, 100K,01)	36	1.15
	2	4012,13,27,13,27,13	6	
	12	4023	1	
B7	2	4027,25	2	
	13	4027,25	2	
C4	2	4011,27,23,13	4	
	12	4027,23	2	
C5A	1	4011	1	
	2	4013	1	
	14	4013	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6}SEC
IC #	PIN #			
C6	2	4023	1	
	13	4011	1	
C7	3	4011	1	
	4	4023	1	
	10	4011	1	
	11	4027	1	
C8	1	4001	1	
	2	4011,11, (4049,12,25,12,13,13, 11,11,49,25,02)	13	.36
C9	2	4020,01,13,13,27	5	
	4	4001	1	
	6	4013	1	
	10	4027	1	
	12	4027,12,13	3	
	15	4001	1	
D4	3	4012	1	
D5	6	4027,13	2	
	10	4023	1	
D6	9	4013,27	2	
	6	4012	1	
	10	4049,13,12,23,(4001,49,13, 12,11,49,11,23,11,49,49,12, 13,13,12,02)	20	.37
D7	1	4013	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
	2	4013,13	2	
	13	4011	1	
	12	4011,20	2	
D8	1	4023	1	
	13	4023	1	
D9	9	4023	1	
	6	4023	1	
	10	4049	1	
E4	3	4011	1	
	10	4011	1	
E5	1	4011	1	
	2	4025	1	
	13	4012	1	
E6	1	4013	1	
	13	4013	1	
E7	3	4025	1	
	4	4013,01	2	
	10	4013	1	
	11	4025	1	
E8	1	4013	1	
	2	4001	1	
	14	4027	1	
E9	7	4023	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
	4	4012	1	
	6	4012,23	2	
	13	4023,23,13	3	
	12	4023	1	
F5	6	4012,49,13	3	
	10	4025,01	2	
	9	4012	1	
F6	13	4027,13	2	
F7	2	4023,27	2	
	13	4012	1	
	12	4011,23,13,11,25,(4049,11),11	8	
G4	9	4023,27	2	
	6	(4049)	1	
	10	4023	1	
G7	10	4013	1	
	11	(30PF)	1	
D5	9	(4025,01)	2	
B7	2	4027,23,(4011,11)	4	
	1	4027,11	2	
	12	4027,27,27,27	4	
C8	14	4013	1	
B6	10	4012	1	
A4	13	4013,27	2	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
B5	12	4001	1	
G7	10	4013	1	
B4	3	4011	1	
B5	15	4012	1	
A2	14	4013	1	
A5	12	4001	1	
A7	3	4024	1	
B4	11	4011	1	
E4	4	4013,01	2	
G7	3	4013	1	
	4	4013	1	
E3	11	4011	1	
	9	4011	1	
D3	11	4049,13	2	
D4	4	4020	1	
	10	(BLANK)	0	
D3	4	4023	1	
	10	4023	1	
G5	5	4011	1	
	6	4011	1	
D6	9	4011,01	1	
D4	11	4012	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A3	1	4013,27	2	
A4	1	4020	1	
	13	4013	1	
A5	1	4020	1	
A6	3	4012	1	
	4	4011,49	2	
	10	4002	1	
	11	4023	1	
A7	9	4023	1	
	6	4019	1	
	10	4015,15	2	
B3	3	4013	1	
	14	4027,27	2	
	10	4026	1	
	11	4026	1	
B4	1	4011	1	
	12	4013,27	2	
	13	4013,13	2	
B5	2	4025	1	
	4	4013	1	
	6	4001,27,13,27	4	
	10	4012	1	
	12	4025	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
	15	4011,11	2	
B6	3	(4025)	1	
	4	4012,13,11,25,29	5	
	10	4020	1	
	11	4049	1	
B7	2	(4023)	1	
	13	4012,25	2	
	12	4002,(BLANK)	1	
C2	1	4013	1	
	15	4013	1	
	14	4027	1	
C3	1	4027,11	2	
	2	4011	1	
	13	4001	1	
	12	4027,27	2	
C4	3	4011	1	
	4	4011	1	
	10	4027	1	
	11	4027	1	
C5	1	4025,23	2	
	2	4027,11,(4011,01,01)	5	
	15	4001,02,23	3	
	14	4027,02,11,(4023,01,11)	6	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
C6	1	4001	1	
	2	4020	1	
	13	4001	1	
	12	4020	1	
C7	3	4015	1	
	4	4013	1	
	10	4002,01	2	
	11	4011	1	
C8	2	4027,13,27,27	4	
	4	4019	1	
	6	4020,20,20,13,20	4	
	10	4013,23	2	
	16	4012,15	2	
C9	9	4001	1	
	6	4049	1	
	10	4001	1	
D1	1	4013,13,13,49	4	
	13	4013	1	
D2	3	4019,23	2	
	4	4001	1	
	10	4013	1	
	11	(4049)	1	
D3	2	4013	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
D3	4	4013	1	
	10	4013	1	
	11	4011	1	
D4	9	4011	1	
	6	4027,27	2	
	10	4049,12,12,23,12,(4049,24,49, 49,)11,12,11,11,11,13,19	16	.32
D5	2	4013,13,01	3	
	4	4001,27	2	
	6	4011,25,01,01	4	
	10	4001,02	2	
	12	4023	1	
	15	($\dot{B}$LANK)	1	
D6	1	4012	1	
	13	4011	1	
D7	1	(4049,23)	2	
	13	4049	1	
D8	14	4012	1	
	4	4012	1	
	5	4012	1	
	9	4012	1	
D9	13	4025	1	
	14	4025	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
F3	1	4011	1	
E3	13	4011	1	
E4	9	4027	1	
	6	4013	1	
	10	4013,27	2	
E5	2	4027	1	
	15	4025	1	
E6	1	4012, (4013,11)	3	
	2	4012,12,01,13,23,01,13	7	.162
	13	4001,12	2	
	12	4011,11,(04)	3	
E7	2	4012,13,(4012,25,02,49,25,12,11,49)	10	.301
	13	4001,13, (4049,49,49)	5	
	12	4023,25,25	3	
E8	4	4001	1	
	10	4001	1	
	12	4001	1	
	2	4001	1	
E9	2	4001	1	
	4	4013,01	2	
	6	4013	1	
	10	4002	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
	12	4013	1	
	15	(BLANK)	0	
F3	1	4013	1	
	2	4025	1	
	13	4025	1	
	12	4012	1	
F4	3	4015	1	
	4	4015,12	2	
	11	4025	1	
F5	14	4012	1	
	4	4012	1	
	5	4012	1	
	9	4012	1	
F6	1	4049	1	
	13	4011	1	
F7	4	4011	1	
	10	4011	1	
	11	(4023,11,11)	3	
F8	3	4013	1	
	4	4012	1	
	10	(4049,23,23)	3	
	11	4001	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
G5	13	4012	1	
G7	1	4012, (4012)	2	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A3	1	4025	1	
	13	(INSTRUMENTATION)	0	
A4	9	4002	1	
	6	4002	1	
	10	4002	1	
A5	3	4011	1	
	4	4049,25,02	3	
	10	4013	1	
	11	4023	1	
A6	1	4001,11,23	3	
	2	4011	1	
	13	4011	1	
	12	4013	1	
A7	3	4002	1	
	4	4002	1	
	10	4002	1	
	11	4002,01,25	3	
B3	2	4011	1	
	12	4001	1	
B4	2	4013	1	
	12	4013,23	2	
B5	2	4011	1	
	4	4013	1	
	6	4002	1	
	10	4023	1	
	12	4025	1	
	15	4012	1	
B6	9	4013	1	
	6	4002	1	
	10	4049	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
B7	6	4023	1	
	5	4023	1	
	4	4023	1	
C1	2	4013	1	
	4	4011	1	
	6	4011	1	
	10	4013	1	
	12	4013	1	
C2	4	4023	1	
	11	4049,25	2	
C3	1	4013,49	2	
	13	4011	1	
C4	2	4020	1	
	12	4013,13,13	3	
C5	1	4011	1	
	2	4011	1	
	13	4011	1	
	12	4011	1	
C6	3	4013	1	
	4	4049	1	
	10	4001	1	
	11	4013	1	
C7	9	4013	1	
	6	4011	1	
	10	4011	1	
C8	7	4023	1	
	5	4023	1	
	4	4023	1	
	13	4023	1	
	12	4023	1	
	14	4023	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
C9	2	4001,13	2	
	4	4011	1	
	6	4013,13,13,13,13	5	
	10	4024,25,20,11, 13,13,13,13	8	.11
	12	4011	1	
	15	4002,02	2	
D1	6	4020	1	
	10	4049	1	
D3	1	4002	1	
	13	(INSTRUMENTATION)	0	
D4	3	4023,11	2	
	10	4027,27	2	
	11	4013,11,11,13	4	
	4	4011	1	
D5	3	4002	1	
	4	4013	1	
	10	4002	1	
	11	4025,02	2	
D7	1	4001,01	2	
	2	4011	1	
	12	4001	1	
D8	13	4013	1	
	15	4049,25	2	
D9	2	4002	1	
	4	4002	1	
	6	(4002)	1	
	10	4025,01,02	3	
	12	4001,11,13,13,13 02,13,13,11,02	10	.135
	15	4013,23	2	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
E2	1	4015	1	
	2	4001	1	
	12	4023	1	
	13	4001	1	
E3	9	4013,13	2	
	10	4025	1	
E4	2	4027,27,11	3	
	13	4002,11	2	
E5	1	4013	1	
	2	4027	1	
	15	4013	1	
E6	3	4002	1	
	4	4001	1	
	10	4013	1	
	11	4001,11	2	
E7	1	4012,02	2	
	12	4013,01	2	
E8	1	4001,01	2	
	13	4013,27	2	
E9	1	4002,01	2	
	2	4001	1	
	12	4002	1	
F3	3	4013	1	
	4	4049	1	
	10	4025	1	
	11	4013	1	
F4	3	4049	1	
	4	4002	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
F5	12	4011	1	
	14	4011,12	2	
	15	4012	1	
	13	4012	1	
F6	3	4020	1	
	4	4002	1	
	10	4020	1	
	11	4023,(4011,49)	3	
F7	2	4011	1	
	13	(4002,25,01,01)	4	
	12	4011	1	
F8	2	4002	1	
	4	4011,11	2	
	6	4011	1	
	10	4011	1	
	12	4020,13	2	
	15	4023,11,23	3	
G4	2	4011	1	
	12	4011,23	2	
G6	1	4013,13	2	
	13	4013	1	
G7	3	4011	1	
	4	4013	1	
	10	4011	1	
	11	4049	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
A3	3	4011,11,25,11	4	
	4	4025,25	2	
	10	4027	1	
	11	4024	1	
A4	3	4019,25	2	
	4	4001	1	
	10	4015	1	
	11	4015,49	2	
A5	4	4011,12	2	
	12			
A6	1	4011	1	
	13	4012,(4049)	2	
A7	1	4011	1	
	13	4011	1	
B3	9	4024	1	
	6	4025,02	2	
	10	4019,49	2	
B4	2	4012,11	2	
	12	4023,11	2	
B5	2	4011,11	2	
	4	4015	1	
	6	4012	1	
	10	4030	1	
	12	4019,19,15,01	4	
	15	4025	1	
B6	2	4002	1	
	12	4001	1	
B7	3	(4011)	1	
	4	4027,13,11,49,23	5	

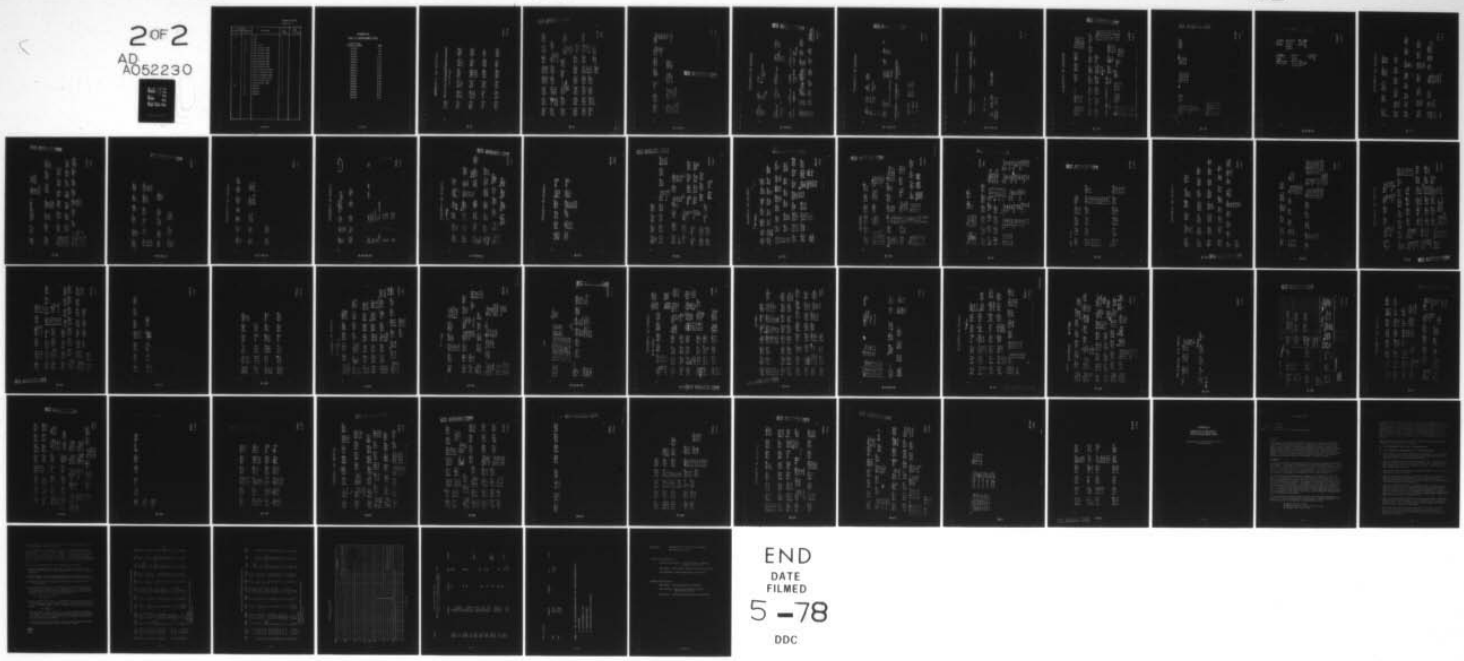
REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
B7	10	4001	1	
	11	4013	1	
C3	1	4013,01,MM4203	3	
	2	4011	1	
	12	4025,12	2	
C4	9	4049,19,19,11	4	
	6	(30PF)	0	
	10	4019	1	
C5	4	4019	1	
	12	4030,12,11	3	
C6	1	4002	1	
	13	4049,(4049)	2	
C7	3	4027,27,27,11	4	
	4	4027,02	2	
	10	4002	1	
	11	4024,12,11	3	
C8	2	4011,24	2	
	4	4002	1	
	6	(30PF)	0	
	10	4001,25	2	
	12	4025	1	
	8	4049	1	
C9	2	4013	1	
	4	4013,13,27	3	
	6	4013	1	
	10	4025	1	
	12	4024,15,49,15,15,15	6	.098
	15	(4011)	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
D1	6	4049	1	
D2	1	4025	1	
	13	4023	1	
D3	9	4011	1	
	6	4012,49	2	
	10	4013	1	
D4	9	4030	1	
	11	4030	1	
	12	4030	1	
D5	9	4025,MM4203	2	
	12	4025,MM4203	2	
	15	4025,MM4203	2	
D6	3	4024	1	
	4	4002	1	
	10	4013,13,11,27	4	
	11	4042	1	
D7	3	4025	1	
	10	4002	1	
	11	4023	1	
D8	2	4027,01	2	
	4	4015	1	
	6	4013	1	
	10	4001	1	
	12	4012	1	
	15	4019	1	
D9	1	4012,(4049,11,23,12)	5	
	15	4023,(4011,01,49,12)	5	
	14	4012	1	

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
E2	9	(4023)	1	
	6	4027	1	
	10	4012	1	
E3	3	4001	1	
	4	4001	1	
	10	4019	1	
	11	4024	1	
E4	3	4025	1	
	4	4025	1	
	10	4025	1	
	11	4024	1	
E6	9	4011,MM42030	2	
	11	MM42030	1	
	12	MM42030	1	
E7	5	4019	1	
	6	4019	1	
	9	4019	1	
	11	4019	1	
	12	4019	1	
E8	13	MM42030	1	
	12	MM42030	1	
	11	MM42030	1	
	10	MM42030	1	
E9	1	4012	1	
	2	4001,12(4049,12,02,01,49)	7	.224
	15	4011,23,19,12 (BLANK)	4	

AD-A052 230 ARINC RESEARCH CORP SANTA ANA CALIF F/G 19/8
LOADING ANALYSIS OF CONTROL GROUP CMOS ICS IN TORPEDO MK 46 MOD--ETC(U)
DEC 77 R GELLNER, J WEISEL N00123-76-C-0797
UNCLASSIFIED W77-1640-TN03 NL

2 OF 2
AD A052230



END
DATE FILMED
5 -78
DDC

REFERENCE		TOTAL LOAD	# CMOS LOADS	RISE TIME 10^{-6} SEC
IC #	PIN #			
F3	3	4027	1	
	4	4049	1	
	10	4049	1	
	11	4001,01,01	3	
F4	11	4001 parallel 100K	1	
	10	4001 parallel 100K	1	
	9	4001 parallel 100K	1	
	8	4001 parallel 100K	1	
	7	4030 parallel 100K	1	
	6	4030 parallel 100K	1	
	5	4030 parallel 100K	1	
	4	4015 parallel 100K	1	
F7	11	4042,01 parallel 100K	2	
	10	4042,27 parallel 100K	2	
	9	4042,27 parallel 100K	2	
	8	4042,11 parallel 100K	2	
	5	4015 parallel 100 K	1	
	4	4049 parallel 100K	1	
F8	13	MM42030	1	
	12	MM42030	1	
	11	MM42030	1	
	10	MM42030	1	

APPENDIX B

CMOS IC INTERCONNECT DATA

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SCHEMATIC NO. 3235702

A6A2 E7B9 | A6B4 | A6C6 | A6D10 | A6E12 | A6F15

1.1K SERIES (46)

B6A2 C5 B11	B6B4 D6 A9 E5 A2	B6C6 D7 C13 E5 D12	B6D10 C5 A3	B6E12 D7 D13 C9 C11	B6F15 E8 B6
B8A2 E8 C9	B8B4 D10 A4 D5 B9	B8C6 A10 D13	B8D10 C8 A6 F7 B8 D5 A4	B8E12 E5 D13	B8F15 C10 B11
C6A2 10	C6B4 12	C6C6 E4 A1	C6D6 G5 A3	C6E12 C10 A3	C6~~F~~
G6A2 E5 C8	G6B4 B7 C9	G6C6 C9 C12	G6D10 G5 B11	G6~~E~~	G6F15 G5 A4

B-3

A6A4

1 OF 3

BEST AVAILABLE COPY

A10D11
E7A3

B5A1
D5B11

B5B8
B6A3

B7A3
C6A3
C7B5

B7B4
C6B5
C7B6

B7C10
F8A5

E7D11
D6A6

B7B13
D7A5

C5A2
D7C11

C5A
13 To D5A2
12 To C7A1

C7A3
D6A7
B7D12

C7B4
E6D9

C7C10
B6D9

C8A
1 To D7B5
F6D13
2 To E7B5

C8B12
C7A2

C9A9
C8A3

C9C10
C9A4

C10A
1 To F8B8
20 LEAR C10A4
33PF

D5A2
23

D5B8
13 To D5A5

D6A
5 To B5A2
D7D10
4 To B5A3
D7C11

D6E12
C6C7

D7A9
D5B10

D7B6
D9A3

D7C10
C5B10

D9A1
F8A3

D9B13
D9A2

D10A1
A10D12

D11A13
19E11

E5A3
E7A2

E5B4
E5C9

E5C10
F5A3

E5D11
C9A6

E6A2
B8C7
B5B10
B7A1
E5B5

E6B4
B7B5

E6C6
B7C6
E5D6
D11A3

E6D10
11

E6E12
9

E6F15
C7C9
B7A2

E7A1
C6D9

E7B13
D7A1

E8A3
F7A4

E8B4
J0B8

E8C10
D5A5

A6A4

2 OF 3

E7D9
F7A3

E7B6
D9B9

E5A1
45

F6B4
C8BC

E6D11
B8F14

F7A
1 To D6B15
C9C13
2 To D6D14
20

F7B
13 To A6F14
A6E11
A6D9
A6C7
A6D5
D10B9
30
12 To D9A4

E4D1
B7C8
F7B11
E9A2
SGK SHEET 5
→ F8A4 1/4 33A

E4B
13 To F7B10
E9A6
36K Sheet
→ F9B10 1/4 33A

G5A
1 To G5D9
2 To F6D5

G5B12
F6D6
G6F14

B-5/13-6

BEST AVAILABLE COPY

A6A4
3 OF 3

SCHEMATIC NO. 3235505

1A2
1800 PF // 22K
5 B9
5 A 3

1B4
3 B6
3 A 2
P1 A01, 9

1C6
1K To B Q1 ≃ 75 PF
(2N3635)

1D6
~~1K To B Q1 ≃ 75 PF~~
1K to B Q5 ≃ 75PF
2N3635

1E12
1800 PF // 22K
7 A2

1F15
1K To Q1 B ≃ 75 PF

2A2
3 D12, 13
1800 PF // 22K
6 A 3
6 B 10

2B4
3 C 8, 9
3 A 1

2C6
2.7K // 75 PF

2D10
2.7K // 75 PF

2E12
22K // 1800 PF
7 B 4

2F15
2.7K // 75 PF
To Base of Q11

3A3
5 B 10
5 A 3
6 A 5
6 B 12
7 A 8
7 B 3

3B4
5 A 4
6 A 4

3C10
36K To P1 A01, 11

3D11
36K To P1 A01, 6

4A2
4 B 5
4 B 10

4B1
4 B 11

4B14
4 A 5

5A1
1 C 7

5B13
2 C 7

6A1
1 D 9

6B13
2 D 9

7A9
1 F 14

7B6
2 F 14

7C10
36K P1 A01, 35

A 6 A 5

1 OF 1

B-7/B-8

BEST AVAILABLE COPY

SCHEMATIC NO. 3235506

2A3	2B4	2B8	2D11
5A3,	2C8	P1A01, 10	4B5
5B5	P1A01, 20		
5C7	A10 4D12	A7G 2105116	
5[illegible]	A10 5B4	27PF	
[illegible]			
5F[illegible]			

3A3	3B4	3C10	3D11	4B4	4D
3B5, 6	2B6	3D12, 13	2A1	4F14	
	3B8	P1A01, 19		4D9	
	15K to ea 15K in area	A10 6C8		4E11	
	47K || 25PF				

4F15 || 4D10 || 4E12	5A2 || 5B4 || 5C6	5D10 || 5E12 || 5F15
650Ω	650Ω	650Ω

U2,3	CD4011	A10 U4	CD4011
		A10 U5	CD4012
U4	CD4049	A10 U6	CD4049
U5	CD4050		

B-9/B-10

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A6A6

1 OF 1

SCHEMATIC NO. 3235507

1A2 || 1B4 || 1C6	1D10 || 1E12 || 1F15	2A2 || 2B4 || 2C6	2D10 || 2E12 || 2F15
650Ω	650Ω	650Ω	650Ω

U1,2 CD 4049

REF	LOAD TYPES	TOTAL LOAD
1A || 1B || 1C	650Ω	
1D || 1E || 1F	650Ω	

B-11/B-12

A6 A7

1 OF 1

SCHEMATIC NO. 3235508

A4A8
1 To B6C8
2 To B4A1
B7 11
C7 A12

A4B12
B4B6
C7A4
B6B5

A5

A6A9
B4A2

A6B6
B4B5

A6C10
A10C9

A7
10 To A8A3
11 To A8B5
12 To A8C7
13 To A8D9

A8A2
C8A1

A8B4
C8B5

A8C6
C8B6

A8D10
C8A7

A8E12
C8A8

A8A2
C8A9

A8B4
C8A10

A8C6
C8A11

A8D10
C8A12

A8E12
C8A13

B4A3
A4A5

B4B4
A4B9

B4C10
75K SERIES
To 13
DIRECT TO
34

B4D11
3

B5C2 // B5B4 // B5C6
550 Ω

B6A3
B7 10
B8 10

B6B4
B6C9

B6C10
B8 11
C6A1

B6D11
B5A3
B5B5
B5C7

B7
9 To C6C9
5 To A7 7
4 To A7 5
6 To A7 3
13 To A7 1
12 To C9 7
14 To C9 5
15 To C9 3
1 To C8 1
2 To B9 7
3 To B9 5

B8
7 To A1 6
5 To A1 4
4 To A1 2
6 To A1 15
13 To C9 13
12 To C1 4
14 To C1 2
15 To C1 15
1 To F1 1
2 To F1 14

B9
10 To A9B9
11 To A12 11

B10 11
C5F14
A10B5
35

C6A3
B6A2

C6B4
36

C6C10
C7B13
C7A6

A6A8

1 OF 3

B-13

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BEST AVAILABLE COPY

A6A8

2 of 3

A10 C10
B10B15

A10 B4
A5 11
A4B10
A4A4

C9
10 To A8E11
11 To A9A3
12 To A9B5
13 To A9C7

C7 #	C6B15
1 To C6A2	B6B6
A7 14	
C9 14	
D7 14	
2 To C5C7	
C6B6	
A11	
C99	
B99	

A5
4 To A6A1
5 To A6A2
7 To A6A3
10 To A6A4
12 To A6B3
13 To A6B5

BEST AVAILABLE COPY

A6A8
3 OF 3

C5A2	C5B4	C5C6
B4D11	A5 10	B4D 13
A10B6	A4B11	B6P 12
	A4A3	(2)
	D10B1	

C5D10	C5En	C5F15
OSC-SERIES	OSCC	C6B5
15K	B6A1	(6)
10K To C5D9 11	1000PF SERIES	
1000PF C5E12	15K To C5D10, C5E11 11	
	10K To C5D9	

SCHEMATIC NO. 3235510

A4A9	A4B6	A4C10	A6A2	A6B4
P1A02,40	A6D10	P1A02,47	A7C10 A4A9	A7D11 B7B6

A6C6	A6D10	A6E12	A7B4	A7C10	A7D11
A7D11	B7B6 P1A02,18	P1A02,35	B7C10	B7C10	A6A2

B4A3	B4B4	B4C10	B4D11	B5A1	B5B13	B6A2	B6B4
B6D3	E5B10	B6E11	E5A4	F5B12	C6A3 C6B5 C6C7	B7A1	B7A2

B6C6	B6D10	B6E12	B6E15	B7A9	B7B6	B7C10
B7A4	D6D13 D6B6	P1A02,25	C7C12	B4A2 B4C8 B5B10	B7C10	B5A5

C2A1	C2A2	C2B13	C3	C4A1	C4A2	C4B12
B4D13 C5B3 P1A02,6	C4B4 D6C9 P1A02,43	P1A02,22	4 TO D4A2 12 TO D4A3 15 TO C5C11 1 TO C5C12 2 TO D4A4 3 TO C5C13	F4B5	B4B5 B4A1	P1A02,37

B4B6

A6A10

1 OF 3

BEST AVAILABLE COPY

C5B6
B5B9

C5C10
F4C9

C6A2||C6B4||C6C6
P1A02,12

C6D10
D5D12
B5B12
D7B11
(P1A02,34)

C6E12
E4B9
(P1A02,39)

C6F15
C4B10

C7A9
F5B10

C7B6
G5A1
F5B9

C7C10
C7A8
B5A4
P5D13
B5B11

D2A1
(P1A02,42)

D2B13
(P1A02,5

D2B12
F4D13
P1A02,7

D3
12 To D4B9
14 To D4B10
15 To D4B11
To D5C9
1 To D4B12

D4A1
F4C8

D4B13
D5B6

D5A3
F5B12

D5B4
E7A5

D5C10
D5B5

D5D11
G5D12

D6A3
E6C7

D6B4
E6D9

D6C10
D6D12

D6D11
D6A2

E2A9
F3C7

E2B6
F3D9

E2C10
C6F14

E3
To E2A1
To E2A2, E2B3
To E4B6, E1B4
To E4B11
To E4B14, E3D5
To D2B11

E4A1
E6E11

E4B13
F3D5

E5A1
C7A2
B5A3
D5A1
C7C11

E5B12
D6B5

E6A2
D6A1

E6B4
E4A5

E6C6
(P1A02,30

A6A10

2 OF 3

E6 D10
P1A02,23

E6 E12
E5 A3
E5 B11

E7 A1
E7 B10

E7 A2
E7 B9

E7 B12
D3 11

E7 B13
D5 A2

E3 A2
C3 10
D3 10
D7 A3
E7 A3

E3 B4
D2 A3

E3 C6
C2 B11

F3 D10
C2 A3

F3 E12
F3 F14
F4 D12

F3 F15
C2 B10
C2 A4
D2 B10
D2 A4

E4 A3
E3 10

F4 B4
C5 B5

F4 C10
D7 A5

F4 D11
E3 11

F5 B13
C6 D9
E7 B11

E5 A3
D4 A5
D5 C4

G5 B4
C4 B11

G5 D11
P1A02,24

B-19/B-20

BEST AVAILABLE COPY

A6 A10

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SCHEMATIC NO. 3235511

1A3 3A2 2A2	1B4 1C9	1C10 2B4	1D11 2B5	2A9 2B3	2B6 4B8	2C10 3B3

3A1 3B4	3B6 4B10	3C10 (P1A01, 18)	4B13 5A3 [P1A01, 26]	4B12 5B11 (P1A01, 17)

5A2 3C12	5B12 3C13

B-21/B-22

A6A11

1 OF 1

SCHEMATIC NO. 3235512

1A2	1B4	1D10	1E12 || 1F15
2B5	2C13	3B12	15K To 2.2K || 30PF
2C11	3A5		
	3B10		

2A9	2B6	2C10	3A1	3B13
29PF	29PF	29PF	29PF	29PF

B-23/B-24

REF	LOADS	TOTAL LOAD
1A2	4023, 23	
B4	4023, 12, 12	
D10	4012	
E12 || F15	15K ~~ohm~~ 2.2K || 30PF	
2A9	29PF	
B6	29PF	
C10	29PF	
3A1	29PF	
B13	29PF	

RT

A 6 A 12

1 OF 1

SCHEMATIC NO. 3235513

* CM 06Y001

A7A1 P1B10,21	A7B13 C7C8 E911	B7A1 P1A19 1	B7A2 C7D12 *F7A1	B7B13 (P1A10, 20 9 11)	B7B12 C7A1
C7A3 B7B9	C7B2 F8D9	C7C10 P1A8, 16	* B7A5	C8A2 D8 10 E9 10 E8 10 B7 3 B7 11	C8B4 D8 11 B7B10	C8 D10 (P1A10, 40)
C9 E12 E7A2 E8 11 B7A4	C9 F15 A7A3	C9A2 P1A10, 30	C9B4 P1A10, 28	C9C6 P1A10, 39	*F8B4 * (P1A10, 10)	C9F15 (P1A10, 27)
D7A1 C7D13 *F7A8	D7B13 C7A2	D8 13 D7B12	D9A2 P1A10, 32	D9B4 (P1A10, 24)	D9C6 P1A10, 15	E7A3 A7B11 F8E11
E8 7 To D7A2 5 To D7A5 4 To D7A3	E9 4 To C7D5 11 To C11 6	F8A2 E7A1	F8D10 A7B8	F8E13 C7C9	*F8F15 F7A2	

*F7A9 B7A-5 | *E7C10 F8B5 | *E7B4 E7C9 | *F8C6 E7B4

B-25/B-26

BEST AVAILABLE COPY

A6 A 13

1 OF 1

SCHEMATIC NO. 3235514

A5A2	A5B4	A5C6	A5D10	A5E12	A5F15
~~C6B11~~	D7A5	D6B9	G7B10	B6D12	(49)
A6D13				F7D12	

C9A2	C9B4	C9C6	C9D10	C9E12	C9F15
C6B11	D9C13	A7B5	B6D13	B5A3	(24)
	D7B9		A7C12	A7A2	
	G7B11		D6B5		
			D7A2		
			D6C9		

B-27

A6A14

1 OF 2

BEST AVAILABLE COPY

A6 A3
C8 F14
C7 B3

A6 B4
C7 B5

A6 C10
D9 A5

A6 D11
C6 A3

A7 A7
D6 B11

A7 B6
A7 C13

A7 C10
C6 D10

B5 A2
D6 A3

B5 B
15 To E7 A2
A7 C11
14 To C9 A1
C5 B15

B6 A3
B6 C8

B6 B4
E6 B10

B6 C10
B5 A4
D6 A2
D6 B10

B6 D11
G7 D6

C5 B12
B5 B13

C6 A2
F7 D13

C6 B
12 To C6 A4
13 To E7 D9
D8 C12
D7 D10
(14)

C7 A9
C9 A2

C7 B6
E7 B12
A6 B6
A5 C7
C9 A8
(46)

E8 A

C9 A9
23

C9 B2
L8 A2

D6 A
1 To L8 C8
B7 B1
E7 A1
10
2 To B5 A6
B5 A5
A6 B5
B6 A

D6 B13
(45)

D7 A1
D9 A4

D7 B13
B7 B6

D8 C10
B7 B5

D9 A1
23

D9 B13
31

B7 A3
D7 A3

B7 B4
B5 B12

B7 C10
A7 A8

B7 D11
D9 B12
26

E6 A2
D7 B12

E6 B13
C9 B4

E8 A3
E7 A3

E8 C10
D9 A2

E8 D11
B7 C8

E7 A1
22

E7 B13
E6 A3

E7 D11
D8 C11

E7 E10
D7 A4

B7 A2
B7 C9

G7 B12
(28)

A6 A14

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B-28

SCHEMATIC NO. 3235515

* CA# 013/003

A1A1 E4D12 | A1A2 A1B9 | A1B13 E4D13 | A2A5 C2D5 | A2A10 C2B6 | A2B12 D1D12 | A2B14 A2B14

A3A3 P1A10,22 | A3B4 ~~C7A4~~ *B4A3 | A3C6 P1[illegible] | A3D11 B3A5 | A4A3 A4B6 | A4B4 E8 1 C5 1 | A4C10 B4A2 | A4D11 B4B11

A5A1 A5A3 B6C9 C9 5 D7 5 E7 5 D9 5 | A5B15 A4C8 | A5B14 A4D13 | A6A3 B4B12 | A6B4 C4B10 B4A5 | A6B10 A6D6 C4B11 | A6D11 C4D12 B6D12 | B2A9 D42

B2B6 D51 | B2C10 B5A3 A1A5 | B3A2 D41 | B4A1 D57 | B4B13 D55 | B5A2 P1A10,47

B5B4 B6C7 | B5C6 B[illegible]D13 B3B4 | B5D10 E2B9,10 C4A3 | B5E12 P1A1 | B5F15 C6A3 C3A2 A5A3 D2B11 A2B1 | B6A3 B7B4 | B6B4 B2A8 | B6C10 A5A6

B6D11 B7B5 | B7A9 B6B6 | B7B6 A4A1 E2B12 C8F14 D5 14 F[illegible]14 | B7C10 A4C9 A4D12 | C2A3 A1A3 A3D12 *C2A3 D1B6 B7C7 D1C8 | C2B4 P1A10,43 B3B12 D1A1 | C2C10 B2A1

C2D11 C7B10

A6 A 15

1 OF 4

B-29

BEST AVAILABLE COPY

BEST AVAILABLE COPY

CA 013/003

C3 A3
B3 A3

C3 B4
C3 A1

C3 C10
C3 P13

C3 D11
D1 D13

C4 A1
D3 B9

C4 B13
D5 5

C5
6 To F43, F13
11 To F42, F72
14 To F41, F71
2 To F424, F721
7 To E35

C6 A
1 To C6 D9
2 To A4 A2

C6 B13
C7 A6

C7 A
1 To B7 B3
2 To C2 C9

C7 B
13 To B7 B4
To C6 A3
To C6 B10
12 To B6 A3
A2 A7

* C8 A1
B2 C12
B4 A3
D4 F10
C4 B7

C8 B4
B6 B5

C8 E12
A1 B1
D7 B11
D7 A3
E7 B11
E7 A3
D4 B11
D4 A3
E4 B11
E6 D2
C7 B11
C6 B11
E6 15
C5 15
D5 F14
D2 A3
A2 A9
A3 A3
D3 E11

C8 D10
B7 C11
A6 C8
A6 B5

C8 C6
B2 B5

C8 F13
F8 9
D5 9

C9
(3 To P1A10, 26)
(10 To P1A10, 3)
(11 To P1A10, 1)

D1 A15
A2 B15

D1 D11
B2 A2
C5 5

D2 A
1 To D2 B9
To E3 B12
2 To A4 D5

D2 B13
B D2 A4

D3 A1
C3 C9

D3 B13
C3 D12
C4 A5

D4
12 To F3 A2
11 To F3 B6
7 To F3 C9
6 To F3 D13
To [illegible]
4 To [illegible]
[illegible] A4 C9

D5
13 To C53
12 To C513
11 To C512
10 To C54

D6 A1
D5 2

D6 B13
D5 15

D7 A1
F8 2

D7 B13
F8 15

*D1D4
B4B4
C4C9

D1C6
A6C8

D1A3
E2A5

A6 A15
2 OF 4

D7
3 To P1 A10, 40
9 To P1A10, 28
12 To P1A10, 15
1 To P1A10, 25

D9
3 To P1A10, 7
10 To P1A10, 39
12 To P1A10, 38
1 To P1A10, 36

E2A1 ~~E2B13~~
~~D1A2~~
A2A1

E2B13
D2A5

A6A15

3OF4

E3A1
C4A2

E3B13
C4A4

E4A3
E3B9

E4B4
E3B10

E4C10
E3B11

E4D11
C7A3

E6D1
D56

E6B13
D54

E7A1
F96

E7B13
F84

E8
6 To F4 20
To F7 20
17 To F4 19
To F7 19
14 To F4 18
To F7 18
2 To F4 17
To F7 17

E9
3 To P1A10, 24
10 To A3C8
12 To A3A2
15 To P1A10, 32

E3A3
E3A2

E3B4
E3A4

E3C10
E3A4

E3D11
E3A5

E8
13 To E8B3
12 To E8B13
11 To E8B12
10 To E8B4

E7
4 To E6A5
To 100K
To F3A1
To D7A4
5 To 100K
To E6B9
To F3B5
To D7A7
6 To 100K
D3A5
F3C6
D7B13

F7
7 To 100K
To D6B9
F3D12
D9A4
8 To E7A3
100K
E4A1
~~E~~94
9 To E7B9
E97
100K
E4B5

E7
10 To D7A5
100K
E9B13
E4B5
11 To D7B9
100K
E9A4

F4
4 To B5D9
100K
D8A4
5 To 100K
D87 B5B1
6 To C3B5
100K
~~B5E11~~
D8B13
7 To 100K
E2A3
D8A4

F4
9 To 100K
C9A4
9 To 100K
C9A7
10 To 100K
C9B13
C9A4
11 To 100K
B5B5
E2B11
D3A5
C3C8

B-31

DB # 3235515

B1A2
B2C12

B1B4
A3B6

B1C6
B2B3

B1E12
A1A3
A3D12

B1F15
C7A4

C8A2
C6B1
C5I5
B5F14
D2A3
A2A9
D3F3
D3E11

C8B4
B6B5

C8C6
B2B5

C8D10
D1A2

C8E12
A1B11
D7B11
D7A3
E7B11
E7A3
D6B11
D6A3
E6B11
E6A3
C7B11
E8C15

C8F15
F8 9
D5 9

B5

B5A2
C1C9
47

B5B11
B6C9

B5C6
B6D13
B3A4

B5D10
E2B9,10
C4A3

B5E12
E2A3

B5F15
C6A3
C3A2
A5A3
D2B11
A2B1

A6A15

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BEST AVAILABLE COPY

SCHEMATIC NO. 3235517

A5A2
P1A10, 24

A5B4
D6A3
D6B11
P1A10, 6

A5C6
B6A4

A5D10
B4C10

A5E12
B4D4
B4C9

A5F15
A7B5

A7A3
A5A3

A7B4
P1A10, 5

A7C10
A5B5

A7D11
P1A10, 7

B4B4
D6A4

B4C10
B6B10

B4D11
E6A3

B6A2
B7C12

B6B12
B6A5

B7A9
P1A10, 45

B7B6
E7A8
A5F14

B7C10
D6B10

C4A3
B7B4

C4B4
D4A3

C4D11
D4B10

C4C10
B7C13

C5A2
F4 20

C5B4
C4D13

C5C6
F7 17

C5D10
B5B1

C5F15
F7 18

C6A1
C9B6

C6B13
F7 3

C7A3
C7C9

C7B4
C7C8

C7C10
C6B11

C7D11
C5A3

C8A2
C9A1
E6B11
C9B5
B5AC
C6AC
C9C8

C8B4
P1A10, 9

C8C6
C7A1

C8D10
E7B5
C7D13

C8E12
P1A19 8

C8F15
C9F5

A6 A17

1 OF 2

B-33 BEST AVAILABLE COPY

C9A3
D9C10

C9B4
D8C10

C9C10
E6 10

C9D11
A7A2
C9A2

D4A2
P1A10,26

D4B13
B4 D12

D5
9 To F7 19
12 To F7 20
1 To C4D12

D6A1
B7A1
P1A19,3

D6B13
F421

D7A1
F721

D7B13
F71

D8
6 To C7B6
To D7A2
13 To C7A2
12 To D7A3
14 To D7A4
1 To D7A5

D9
5 To C9D12
12 To C9D13

E6A1
E6B9

E6B13
D55
D311
E6A4
E211
B5B14
C6B10

E7A9
P1A10,10

E7B6
F43

E7C10
C5D9

E8
7 To E7C11
5 To E7C12
4 To E7C13
To C4B6
6 To D7B9
12 To D7B10
14 To D7B11
1 To D7B12

F4
11 To C5C7
To 100K
10 To D54
To C8F14
To 100K
9 To D57
To 100K
8 To D513 || 100K
5 To B5A7 || 100K
4 To D514 || 100K

F5
17 To B7B5 || 100K
10 To A7A1 || 100K
9 To A7B6 || 100K
8 To A7C9 || 100K
7 To C8E11 || 100K
6 To C8F14 || 100K
5 To C9C9 || 100K
4 To C6B5 || 100K

A6A17

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SCHEMATIC NO. 3235518

A2A
4 TO F3A2
3 TO F3B9

A2B
12 TO F3A3
E3A2
11 TO F3B10
E2D13

A3A2
F4C9

A3B13
C3C8

A4A
1 TO B3A1
B3D12
E6A8
2 TO A5C1
A7C8

A4B
13 TO B3B5
B3C8
E6A8
12 TO A5B5
B7C9

A5A1
D5A3
D3A3

A5B6
A4A3

A5C10
A4B11

A6A1
E6C11

A7A3
D9B10

A7B4
A7C8

A7C10
(25)

A7D11
B6B11
D7A2
A5C13
A5B4
E4B11
D7B5
A5A2

B2A
4 TO F3A4
E3A1
3 TO F3B11
E2B5
E2C4

B2B
12 TO F3A5
11 TO F3D12
E3B6
E2B5

B3A3
A2A9

B3B4
A2B1

B3C10
B2B1

B3D
B2A9

B4A
1 TO C3D13
B3D13
B3B6
2 TO E6F4

B4B13
B3A2
B3C9
C3D12

B5A2
G4C13
G5B13

B5B12
C4B10

B6A2
E9A1
A7B6

B6B12
D7A1
D7B6

B7A3
A5A8

B7B4
C8B5

C3A3
E6A1

C3B4
E6B3

C3A10
D6A5

C3D11
C2B5
A3B10

CLK

C4A1
D4A1

C4B12
D3A5
E8B11

B7C12
B4A8
B4A6

B2D11
C2E11 19
D7C11
F4A7
A6A5
C6C13
L6F9

C5A2
D2A3

C5B14
C5A3

C6A7
A1F14

C6B6
B5B3

C6C10
D4D13
J2

C7
12 TO F7A2
11 TO F7B10
7 TO F7A(3,4)
5 TO F7A5

C7
5 TO F7D9
4 TO F7B(11,12)

C5B12
C5A4
D2A4

A6A18

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BEST AVAILABLE COPY

BEST AVAILABLE COPY

C9A1
B7D12

C9B12
D4C8
C9A4
B7D13

D2A2
D4B6

D2B
13 TO C5B10
12 TO C3C9

D3A1
D3B9

D3B13
E2A2
E2B6
E2C9
E2D12

D4A3
D3A4

D4B4
C6C13

D4C10
C9B9

D4D11
8

D6A1
D5C7
D9A4
B2A14
B2A6
A2A14
A2A6
B3B10

D6B13
C8 F14

D7A9
A4B11

D7B6
B4A3

D7C15
A1A3

D8A
1 TO D4B10
2 TO 24

D8B13
D8A5

D9A2
A7A2

D9B
13 TO D4A2
15
12 TO A5A1

E2A3
C3A1

E2B4
C3A2

E2C10
C3B5

E2D11
C3B6

1

E3A3
C2A3

E3B4
D4C9

E4A2
D6A2

E4B13
E4A5

E5B
13 TO F4B5
1 TO F4B6

E6A9
F6A3

E6B6
F6B11

E6C10
F8A6

E7A3
D4B5

E7B4
C6C11

E7C12
D9B11

E7D11
D6B10

E8
6 TO C6B3
13 TO C6B4
12 TO C6B5

E9A9
G6C8
E9C13

E9B6
D8B11

E9C6
10

F3A1
D5E11

F3B13
C2C7

F4A3
G5B9

F4B4
F4A2
F4C8
G5A4

E5A1
1

E5B12
F4D12

F6A2
E9B4

F6B12
E9B5

F4C10
E5B5

F4D11
A1E11

A6A18

2 OF 4

F1 A1
G7 A3

F2 B8
G7 B11

F8 A10
C9 A3

G4 A9
B5 A4
E5 B14
A1 C7

G4 C10
G4 A2

G5 A1
E9 C11

G5 B13
E9 C12

G6 A3
B5 A3
B6 A3

G6 B4
A3 A3

G6 C10
F5 A5

G7 A2
~~G6 A~~
G6 A7

G7 B12
G6 B5

B-37

A6 A18

3 OF 4

A1A2
24K SERIES
20K 1130PF

A1B4
G4C11
B6A4
A6A3

A1C6
A7C9

A1D10
F5B11

A1E12
G5A2

A1F15
E9A8
G5B12
G5A5

C2A2
D4D12

C2B4
E4A10
E6C13

C2C6
D2B11

C2E12
13

C2F15
D2B10

C8A2
E8 10
D8A3
B5B11

C8B4
F4A1

C8C6
D7A8
A5B3

C8D10
D7B4
A5C12

C8E12
D6B11

C8F15
20

D5A2
C4A3
C4B11

D5B4
D6A3

D5C6
A7A1

D5D10
14

D5E12
E7C8

D5F15
E9B3

B-38

A6A16

4 OF 4

SCHEMATIC NO. 3235519

* Two F 8
[illegible] of E8

A3
5 To B3C11
6 To B3C12
11 To B3C13

A4A3
A4B4

A4B4
C4B11

A4C10
D4B11

A4D11
D4B11

A5B
13 To B5A3
11 To B4B3

A5A4
F8 1
*F8 1
A7B5

A6B11
D7F5

A6B
13 To C6C12
12 To A5B1

A7A3
E5 1

A7B4
A7A1

A7C10
(P1A10, 11)

A7D11
(P1A10, 49)

B3A9
A3 2
D5A2

B3B6
E4B11

B3C10
C3B9

B4A3
C4A3

B4B4
D4A3

B4C6
D4A4

B4D11
C5B12
D6B10

B5A2
A4C8

B5B4
B3B5

B5C6
[illegible]A1

B5D10
C4B10
A6A4

B5E8
A4A2

*2 B5F15
P1A10, 10

B6B13
A6B11
B4D6
A4C9

B7A3
A4D13
A4A1
C6A2

B7B4
P1A19, 26

B7C10
D3B5

C2A1
C2D13
D3A1
P1A10, 18

C2B15
D3D12

C3A1
C6A8

C3B13
B3A8

C4A1
F7 19
P1A10, 19

E7A9

C4B
13 To B7B6
To E4B12
12 To C6A1

C5A2
A1C8
A1D12

*2 C5B15
BLANK
NO OPT4

C6A9
C4A3

C6B6
F5B5
D5C9

C6C10
F5A3

C7A3
A57

~~C7B4~~
D6A4

C7C10
E52

C7D11
C7B6
B4D12
C7C9

A6A19

1 OF 3

* IVO NUMBER

C8A2
PIA10,21

C8B4
D5B5

C8C6
D7D12
C3A6
C6B3
C5A7
A5A6

C8D10
B2C8
B6B12

C8E12
(PIA10,47)

C9
3 TO B7A2
9 TO PIA10,28
15 TO C7D12
12 TO B6B11

D3A3
E4A2

D3D11
E4A3

D3B4
PIA10,3

D4A
2 TO D3A2
TO D5B6
1 TO D3D13
C5A5
PIA10,15

D4B
13 TO B4C9
C6C13
(PIA10,27)
12 TO D5D13

D5A3
C2A3
F8I5

D5B4
F7I8

D5C10
I5B14

D5D11
C4A3
F7I7

D7C10
C95

D7D11
D7C9
D7B6
D7A2
C7D13
D8A7

D8A
5 TO D7D13
4 TO I1A2

D6A2
PIA10,31

D6B12
PIA10,4

D7A3
E95

D7B4
D95

E9
2 TO A7C9
10 TO C5B13
PIA10,8
9 TO C3I4
11 TO C4C11
C5E11
12 TO 21C7116.G
1 TO I1I2I3
15 TO I1L4I0

E4A1
PIA10,43

*E4B13
B5F14
C5B10
PIA10,33

E5
5 TO F720
6 TO F721
9 TO F71
11 TO F72
12 TO F73

*E8

D9
2 TO C5A3
10 TO C7B5
D6B11
9 TO PIA10,25
12 TO PIA10,16
1 TO C3A3
B4D13
D6A3

AGA19

2 OF 3

B-40

A from

E4
9 To F5E11
12 To F5F14

F7
11 To 100K || F8B13, E914, D94, C94
10 To 100K || F8A12, E97, B97 C97
9 To 100K || F84, E913, D913, C913
8 To 100K || *F83, E914, D914, C914
7 To 100K || *F813, D7A1
6 To 100K || *F812, D7B5
5 To 100K || *F84, D7C8
47, 100K || C7A1, D8A6

F7

*F87
F85
F815

E87
A7D6
C7A2

E7C10
D6B10
C5B12

B-41/B-42

OSC

F5A2
D5 3 8

F5B4
D4 B10

F5C6
F5 D9
56K serie
5K serie
[200K || 510P serie FSC7]
[F5 D10 ← 41 F41]

F5D10
F4 1
510 PF (serie 200K)
[11 61K F5D9 ←]
FSC7 ←

F5E12
pin 10, 20

F5F15
D8 B9
A5 A9
C3 B11
A31
pin 10, 29 ←

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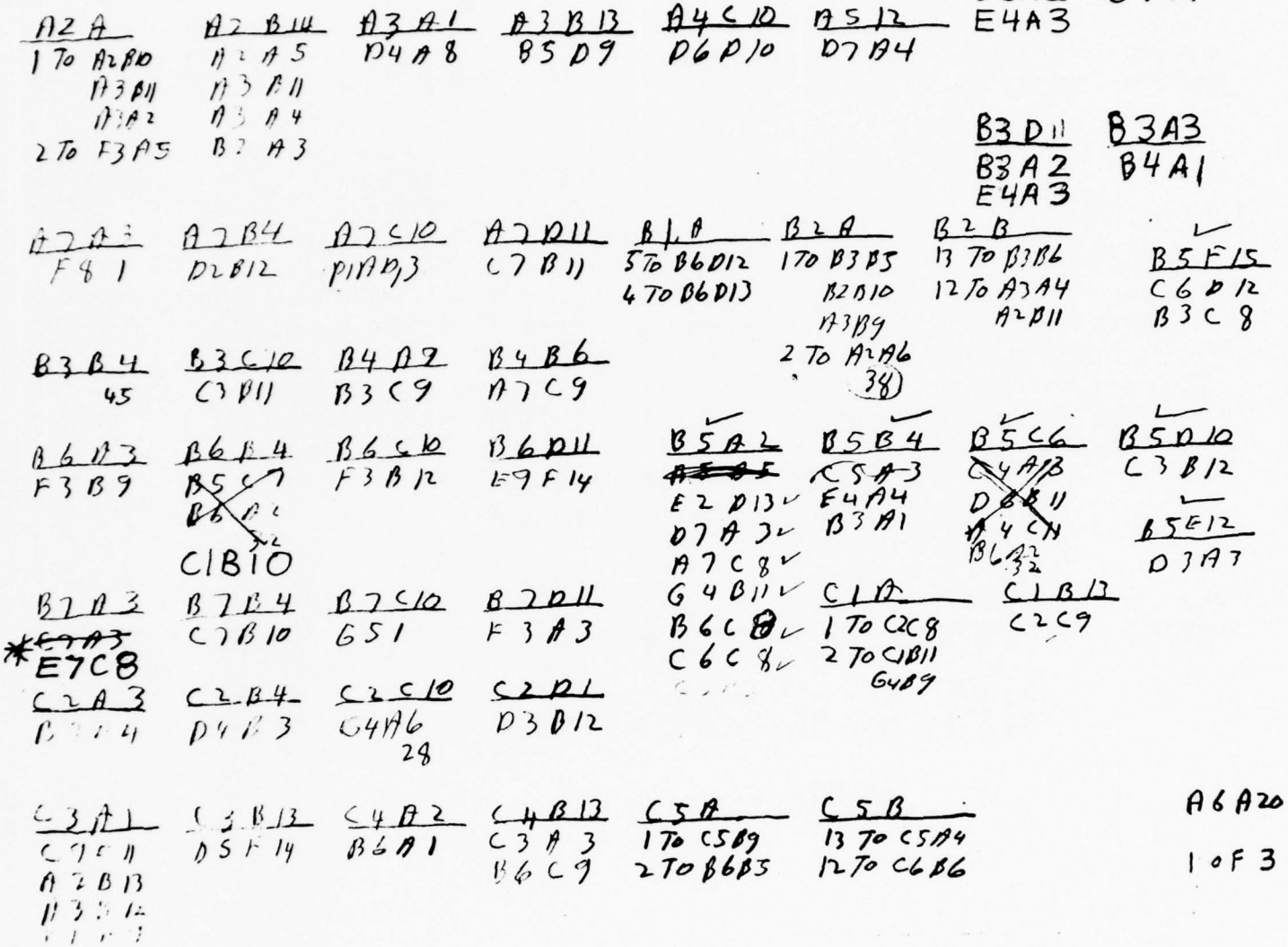
A6A19
3 of 3

SCHEMATIC NO. 3235520

* CA UPDATE

B3D11 B3A3
B3A2 B4A1
E4A3



A6A20

1 of 3

B-43 BEST AVAILABLE COPY

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CA UPDATE

C6A2 D6A3 | C6C10 C6A1 | C6D11 C6A2 | C7A1 C8B15 | C7B13 (6) | C8A4 4, | C8B12 D9C12

C9A2 D7A1 F3E11 D3[illegible] [illegible] B2B9 | C9B4 B7B5 | C9C6 B7C9 | C9D10 C8B14 C8A6 C3B10 [illegible]2A4 A2B12 | E C9E12 E9C7 E8B1 E8B9 C5B13 A5I0 | C9E12 G2NS114 E2C8 G4A3 C1A3 ~~B7A6~~ | C9F13 C4B8 G4B10 C1A6 B1A6 | D1B12 C2B6

D2A1 C2A2 | D2B13 C2A1 | D3A1 D5E11 | D3B13 D3A5 | D4A9 B2A6 | D4B6 C3A2 | D4C10 D8B12 | D5A2 C6C9

D5B4 D4C13 | D5C6 D1B11 | D5D10 D3A2 | D5E12 C4B10 | D5E15 C4B11 | D6A1 F7I9 | D6B13 C8A7 | D7A 1 TO E2C9 2 TO A5 11

D7B8 B7C8 | D8B13 F3A2 | D9A9 C8B1 C8A7 | D9B6 F3A4 | D9C10 A7 D13,13 | E2A3 D4C13 | E2B4 ~~E2D12~~ | E2C10 D2A4

E2D11 C1A4 | E3A3 ~~C1B10~~ E3D13 | E3B4 D3B10 | E3C10 D3B11 | E4B13 D4B4 | E5A3 E4D11 | E5B4 D5C7 C2B5 | E5D11 B4A2

E8A4 E7D9 | E8B [illegible] 11 TO D10 | E9A8 E3C9 | E7B4 D3B9 A7B5 | E9C6 D7B11 | E9D10 E5B5 E5A1 E5D12 | E9E12 ABOVE INC Group | E9E15 D2A5

E3A1 F4A4 | E3B13 D6A4 [illegible] | E3B13 C7C6 | E4A1 B1A7

A6A20 2 OF 3

F7

11 To 100K, E4A6,
6 To 100K, E5B6
7 To 100K, E5A2
8 To 100K, E5D13
7 To 100K, G5 3
6 To 100K, G513
5 To 100K G512
4 To 100K, G54

F8

5 To F720
6 To F721
9 To F701
11 To F7 2
12 To F7 3

G4 A

1 To 36K → to G4A 4
↳ to 33PF
To G4B 8

2 TO G4A 5

G4 B 13
(25)

E5 7
E8B14

*E7C10
E7B5

E7B4
B2A4

E7A3
E7A3

E4A1
C3D12

A5C12
D3F2

A4A9
E2D12

A6A3
A6B5

A6D11
A6B6

A6B4
D2A2

E3D11
B5E11
B4A8
C3A4

C6D4
B5C7
C1A3

B-45/B-46

A6A20

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SCHEMATIC NO. 3235521

CA/066/002

A2A2
B - B11

A3A3
B3A6

A3B4
E7D13

A3C10
43

A3D11
B3A4

A4A1
B4D12

A4B13
F5C12
A2A6
B5E11
A

A5A2
B A3
C9
A8

A5C11
G7D12

A5E6
D7B11
C7B5
C6A5

A5D10
F5 11
D5A1

A5E12
G7A1

A5F15
F6B10

A6A7
A4D9

A6B6
E7C9

A7B4
B6A4

A7C10
B A3

A7D11
G4C13
2

B2A2
A2A3

B2B12
9

B3A1
A3C8

B3B
13 TO A3A2
12 TO A3D13

B4A3
B4D13

B4B4
B3F5

B4C10
G4A2
A5B5
B4 5
37

B4D11
C4B11
C5B13

B5A2
C5A6,5

B5B4
D4A2
E7K8

B5C6
C5A3

B5D10
B7B11

B5E12
D4A1

B5E15
A4D12
F5A11

D4D13

B6A
1 TO F5C13
E10 5
G4A1
F4B3
E4C6
A A1
A3D12
34

B6A2
E6A2
B6B10
C8B13
E2A4
1-F4
B2B10

B6B12
D6A8

B7A2
C8B10
A6A8

B7B13
C8B11
A6A2

C4A2
B4C9
C5B10
D5C12
C4B9

C4B12
C5A11
D5C11

A6A21

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Continued

* CA 038/002

** CA 147/001

C5A
1 TO E4C9
2 TO C6B11

C5B14
C4A3

C6A2
D6C13

C6B13
E4C8

C7A3
D6C11

C7B4
D6C12

C7C10
~~F5B5~~
*D3D13

C7D11
C8A6

C9A
1 TO E7B6
2 TO E4A2
11 IN 13
13

C9B
15 TO F5A3
14 TO E7B10

C9A2
E7 10
D4B11 NEW
D7A3
E5B11
A2B13

C9B4
E7A1

C9C6
D7A5

C9D10
A2A3
~~B2B10~~

C9E12
C8A4
D4B9
B3B10

C9F15
E7A2

D4A3
A4A2

D5B6
C5B12
C4A4

D5C10
D5B6

D6A9
E7D4
C8B12

D6B6
E6B9

D6C10
B5B5
B6A3
D8B12
G4B5
30

D7A
1 TO D7B9
2 TO D7B10
C6A3

D7B
13 TO C7A1
12 TO F5A8
E7 11
*D3B6

D9A
D7C12

D9B13
G4C12

D9A9
D9C11

D9B6
D9C13

D9C10
C9C7

E4A3
~~A4B10~~
*E4B4

E4C10
A7B5

E5A
1 TO F1D12
2 TO A6B5

E5B13
E6B10

E6A1
E5B14

E6B13
F7B10

E7A3
A6B3

E7B4
E5A4
F9B13

E7C10
F7A3

E7D11
D6B6

E9A
1 TO E5A3
2 TO E1B11

E9B14
E6A5

E9
7 TO D9A1
4 TO D1A2
6 TO D8A3
D7B3
13 TO D7A8
D7B4
D4A5
12 TO D7B5

*E4A1
F4B9
F5B3

*F4B
12 TO F4A6

F5B6
F4A3
A5C7
C6A4

*D5A9
E5C10
36

*F5A9
F4B10

A6A21

2 OF 4

B-48

**CA/066/002 *CA 038/002

F6A	F6B13	F7A2	F7B
	C5A4	D6B3	13 TO E6A5
	C6E10	E8E11,10	12 TO B4C8
			D6B4
			F7A5
			C7D12
			11
			*D3B6

G4A9	G4B6	G4C10	G7C10	G7D11
G4C11	48	G4B3	B6B11	42

**C8 3

B-49

A6A21

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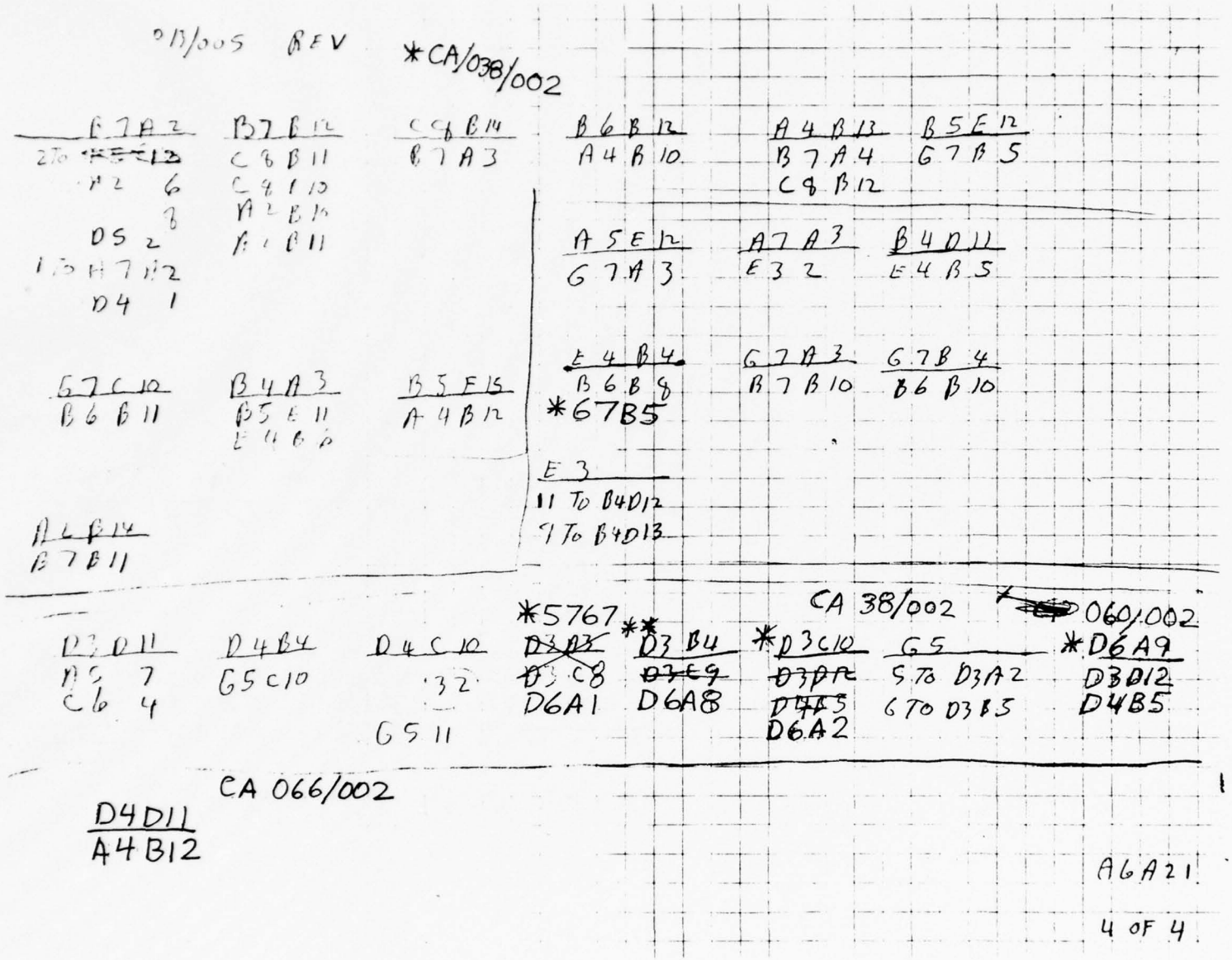

SCHEMATIC NO. 3235522

A2A1
C3F11
C2E13

A3E12
NO OUTPUT

A4A1
A5I1

A4B13
B4B9

A5 1
A4B9

A6A3
A4A5

A6B4
A6A1
B5>A

A6E10
B3A3

A4D11
A1L2

A1L2
A1E3

A7B6
G5 15

A7C10
E8D6
E8B14

B3A3
C3B10

B3B14
C2D12
C2A4

B3C10
E4B3

B3D11
E4B4

B4A1
C4A1

B4B12
B4A4
C3A4

B4B13
E7A1
D4A4

B6A3
42

B6B4
E3D9
D1A3
D3D12
E4C12
B5B5

B6C10
D8 10

B6D11
B5C7

C2A2
32

C2B
13 To D7A5
C9D5
12 To A3A4
14

C2A1
C3A5

C2B
15 To C3A3
14 To C2A3

C3B
1 To C2A7
F7C9
2 To D3D13

C3B
13 To B3B5
12 To C2B11
C2B10

C4A3
C4D12

C4B4
C4C9

C4C10
C5B10

C4D11
C5A6

C5A
1 To C9B3
D4C11
2 To D9B11
A6B6
15

C5B
15 To C7B6
A3A5
A4C12
14 To D9B10
A3B12
A6A2
16

C6A
1 To A4A2
2 To C5A1

C6B
13 To C7A2
12 To A4A11

C7A3
E6A9

C7B4
D6A3

C7C10
D2A1
A3A2

C7D11
F7B5

A6A22

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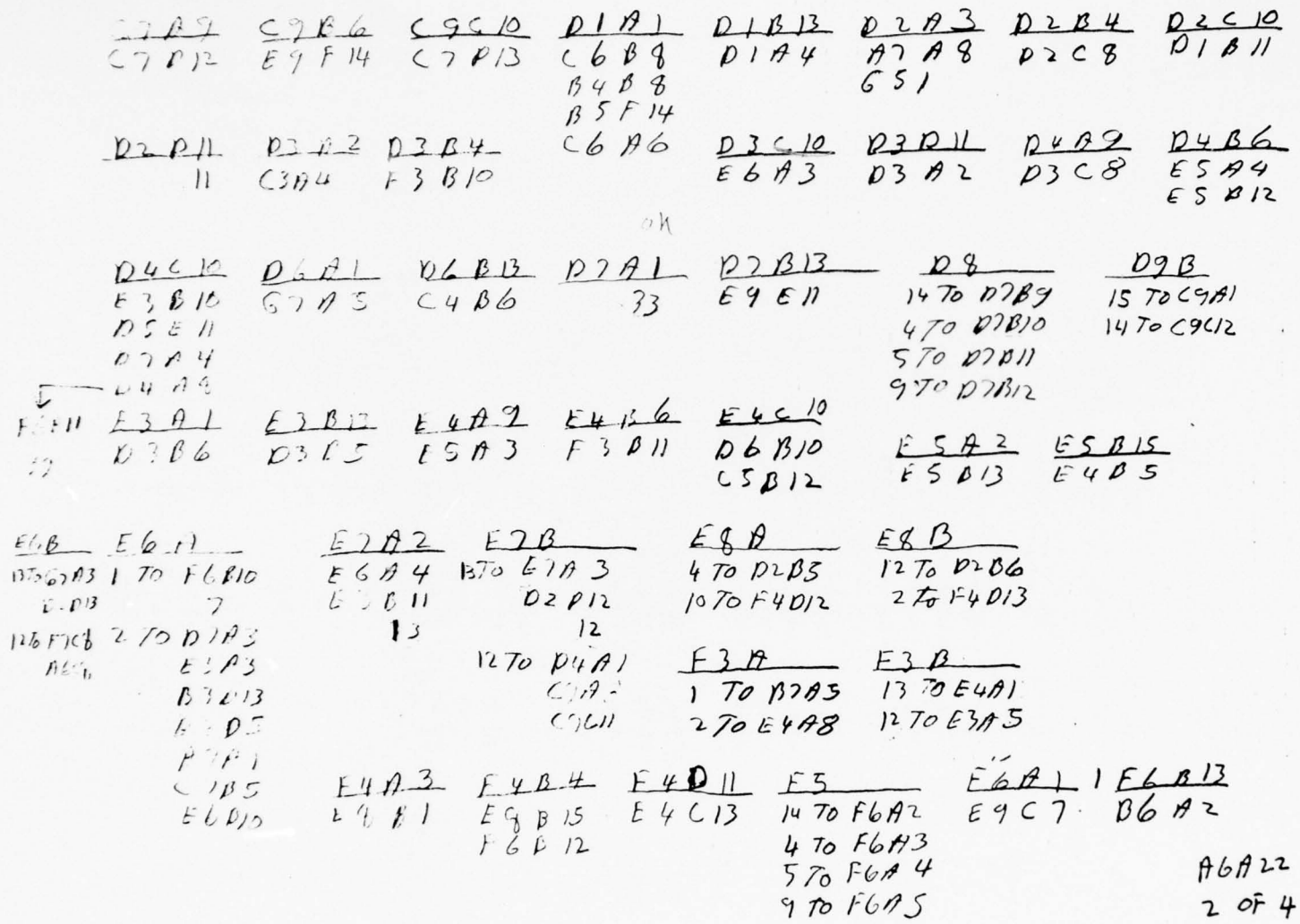

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E2B4 F7D12	E2C10 F7D13	F7D11 38	F8A3 B7A3	E8B4 D7A2	E8C12 (6)	E8D11 F8C8

G5B3
H4A4

C7A1
F7B6
27

B-53

A6A22
3 OF 4

BEST AVAILABLE COPY

B 5 A 2	B 5 B 4	B 5 C 6	B 5 D 10	B 5 E 12	B 5 F 15
E 4 C 11	D 6 B 11	B 3 B 6 C 5 B 13 B 4 A 3 C 5 C 3	A 4 B 10	C 9 B 4	C 4 D 13 C 4 C 8
C 8 A 2	C 8 B 4	C 8 C 6	C 8 D 10	C 8 E 12	C 8 F 16
D 9 B 12 F 3 B 8 C 5 B 9 C 5 A 7	G 5 14	D 8 10 A 5 10 B 4 B 11 F 5 10	F 3 A 3 A 7 B 3	B 7 B 10 E 7 A 4 D 6 A 4	A 4 A 3 E 8 A 7
E 9 A 2	E 9 B 4	E 9 C 6	E 9 D 10	E 9 E 12	E 9 F 15 (44)
D 2 A 2	C 6 B 11 C 7 A 1	C 6 A 14	A 3 B 9	C 6 B 10	
D 5 A 2	D 5 B 4	D 5 C 6	D 5 D 10	D 5 E 12	D 5 F 15 (19)
E 7 B 11 E 6 B 11 F 8 C 6	B 3 A 1 D 9 B 13	B 6 D 12 E 4 A 2 B 3 C 9 B 3 D 12	F 8 D 12 A 3 B 10	D 4 B 3	

A 6 A 22

4 OF 4

SCHEMATIC NO. 3235523

A3A1
D4A2

A3B13
11K
2200PF
20

A4A7
A3B9

A4B6
A3A4

A4C8
A3B10

A5A3
G7D12

A5B4
F8A3
A4B5
D3A2

A5C10
B3B11

D5D11
E3A1

A6A
1 To A7C7
A5C9
A6C12
2 To A5D12

A6B
B7 To C3B12
12 To A6A3

A7A3
A3A2

A7B4
A3A5

A7C10
G6B11

A7D11
D3A3
A4C12
A7B6

B3A2
A5A2

B3B12
D5D13

B4A2
B4B10

B4B12
B3A3
B7 2

B6A9
B4A5

B6B6
D3B11

B6C10
D9C7

B7
6 to B6A1
5 to B6A2
4 to B6A4

C2A4
D1C11

C2B11
C1C7
D1C13

C3A1
F8C7
E2A5

C3B13
A5C18

C4A2
C8 11

C4B12
C4A4
C5A4
C5B10

C5A
1 to C6B5
2 to C6A4

C5B13
A5A1

C5B12
C6D13

C6A3
C5A5

C6B4
B5B5

C6C10
E6A1

C6D11
C5B9

C7A2
C6C3

C7B4
C6C1

C7C10
C6D12

C8
7 To C7C13
C7B3
5 To C7B4
4 To C7C11
C1B5

C8 CONT
13 To C7C12
C7A1
12 To C7A2
14 To C7A8

D1B6
D8 10

D1C10
C1A3

A6A 23

1 OF 4

B-55

BEST AVAILABLE COPY

BEST AVAILABLE COPY

D3A8
D3B9

D3B8
39

D4A3
B6B4
F6B5

D4B4
D4C8

D4C10
E5B12
E5A4

D4D11
G7A1
E4B10
D4B6
D7B1

D5A3
D3B12

D5B4
E4A4

D5C10
A4C11

D5D11
D3C10
A3B11

D7A1
E6B6
D5D12

D7B2
A5B5

D7B12
10
A7A12

D8
13 TO E7B11
15 TO C1B5
D1B3

E2A
1 - C2B15
2 - E6C8

E2B
12 TO E3C13
13 TO E6B5

E3A9
B3B10
A6A4

E3C10
A4A1

E4A2
E5A5
E5A6
D4B5

E4B13
F3D5
D3A5

E5A
1 to E4B11
2 to E5B13

E5B15
E4B9

E6A3
A3A3

E6B4
D5C9

E6C10
E2B8

E6D11
D5B9
A5D13

E7A1
G6E9
C3B7

E7B12
E6A3
E6C9

E8A1
A7D13
A7B5

E8B13
E5A3
E4A3

E9A
1 to D5C8
E4B9
2 TO D5A2

E9B12
E8B10

F3A3
E7A3

F3B4
C1D9

E3C12
D1C12

E3D11
E2B10

F4A3
C1E11

F4B4
D3A4

E5
12 TO F3A2
14 TO F3B1
C3A3
15 TO C3A4
13 TO C3A5

F6A3
F5 11

F6B4
A3B12

F6C10
F5 10

E6B11
E6B3

E7A2
G7A2

E7B
13 TO 9
12 TO F4A2

A6A23

2 OF 4

BEST AVAILABLE COPY

G4D2	G4B12	G6A1	G6B13	G7A3	G7B4	G7C8	G7D11
F4B5	F4C6	F7A3	F6B10	G7B5	F7B10	G7D13	D9B5
		F7B11					

C 1 A 2
E 2 A 4

C 1 B 4
F 3 C 8

C 1 C 6
F 3 D 12

C 1 D 10
G 4 A 6

C 1 E 12
G 4 B 11

C 9 A 2
D 5 B 6
B 6 B 11

C 9 B 4
D 4 D 13

C 9 C 6
D 7 A 6
D 7 B 10
E 9 A 4
E 9 B 10
G 4 A 4

C 9 D 10
B 7 1
D 1 B 4
C 8 10
F 6 C 9
B 4 A 3
C 4 B 11
C 5 A 3
C 5 B 11

C 9 E 12
F 6 A 1

C 9 F 15
G 6 B 6
G 6 A 4

B 5 A 2
C 6 B 6

B 5 B 4
B 4 B 11

B 5 C 6
G 6 A 2

B 5 D 10
B 6 C 13

B 5 E 12
A 4 B 3

B 5 F 15
C 3 B 10

D 9 A 2
E 8 B 11

D 9 B 4
E 8 B 11

D 9 C 6
4 8

D 9 D 10
A 4 A 8
D 5 A 1
E 8 A 5

D 9 E 12
A 7 B 1
C 6 C 9
D 7 A 3
E 2 B 11
E 9 A 3
E 8 A 2
G 4 A 3
G 4 B 10
D 4 C 9
G 6 A 5

D 9 F 15
D 7 A 4
B 6 C 11

F 8 A 2
E 8 A 3

F 8 B 4
F 6 A 2
G 7 B 6

F 8 C 6
F 6 D 13

F 8 D 10
A 5 D 6

F 8 E 12
D 8 11
E 7 B 10

F 8 F 15
B 6 B 5
F 6 B 6
E 3 A 8

B-58

A 6 A 23

4 OF 4

SCHEMATIC NO. 3235524

A3A3
A7D12
B4B11
A3C9
B1B6

A3B4
D3C13
E2C11

A3C10
D9B12

A3D11
E72

A4A3
F84
B3C

A4B4
E3C8

A4C10
A5A6

A4D11
A5A7
B5D9

A5A4
D6A2

A5B12
A6A5

A6A1
D6D12

A6B12
D2A3
1

A7A1
B7D12

A7B13
B7D13

B3A9
E71

B3B6
B3C12
C6B10

B3C12
C7D9
F87

B4A2
A6A4
B7C9

B4B12
C4C13
A4B6

B6A2
C6A5

B6B12
E3B5

B7A3
2

B7B4
E9B12
B6A4
*D6C10
B5A3
C3A4

B7C10
C7A2

B7D11
C3B11

C3A
1 To B6A6
C7D12
F417
2 To A4A1

C3B12
B3B3
A6B12

C4A9
B5E11
E89
F89
D7A1

C4B6
B8

C4C10
F82

C4A4
E4D12

C5C12
B4A5
A6A3
B7C8

C6A1
C6A11

C6B13
B5C7
B1

C7A3
E9B13
D9A3
D9B13
B7A1

C7B4
E9B10

C7C10
C6A4

C7D11
E62
A6A2
A3A1

A6A24

1 OF 4

BEST AVAILABLE COPY

BEST AVAILABLE COPY

D1 6
B 5 F 14

D2 A 1
E 2 A 1

D2 B 13
C 4 B 5

D3 A 7
A 4 C 9

D3 B 6
D 8 D 9
A 6 B 9

D3 C 10
C 3 A 3

D4 9
9 To E 4 B 2
11 To E 4 B 6
12 To E 4 C 9

D5
9 To D3 B3
F 4 17
10 To D3 B4
F 4 19
15 To D3 B5
F 4 20

D6 A 3
E 6 1

D6 B 4
C 6 B 12

D6 C 10
C 3 A 4
B 6 A 4
*B 7 B 4
E 9 B 12

D6 D 11
D 5 5

D7 A 3
B 3 A 1

D7 B [illegible]

D7 C 10
C 6 D 1

D7 D 11
C 4 C 11

D9 A 1
A 7 A 2
21

D9 B
15 To C 4 A 8
22
14 To A 7 A 3

E2 A 9
(45)

E2 B 6
E 9 A 3

E2 C 10
~~F 8 5~~
A 7 A 4

E3 A 3
E 3 B 6

E3 B 4
C 7 C 8

E3 C 10
F 8 5

E3 D 11
D 1 2

E4 A 3
D 3 A 1

E4 B 4
D 3 A 2

E4 C 10
D 3 A 8

E4 D 11
D 4 2

E6
9 To F 4 1
A 4 D 12
11 To F 4 2
12 To F 4 3

E7 [illegible]
5 To [illegible] B 6
6 To [illegible] C 5
[illegible] [illegible] C
[illegible] To [illegible] 4
[illegible] To [illegible] 6

E7
13 To F 14
14 To F 7 1
11 To F 12
10 To F 13

E9 A [illegible]
1 To D 2 A 2
2 To C 7 C 9
D 2 B 10
44

E9 B 15
A 4 C 8
C 4 A 2
F 8 5
A 6 B 10
3

E3 A 3
E 9 A 4

E3 B 4
C 8 C 7

F3 C 10
C 9 F 14

E4 D 11
F 3 A 2
[illegible] C 9
[illegible] B 5

A6 A24

2 OF 4

F4

11 To 100K || F 3 B6
10 To 100K || F 3 C8
9 To 100K || F 3 A1
8 To 100K || F 3 C12
7 To 100K || E 4 A1
6 To 100K || E 4 B 5
5 To 100K || E 4 C 8
4 To 100K || C 5 A 7

F7

11 To 100K || D 5 4
C 7 A 5
10 To 100K || D 5 7
D 9 A 6
9 To 100K || D 5 13
D 9 B 10
8 To 100K || D 5 14
B 7 A 2
7 To 100K || A 5 B 14
6 To 100K || B 5 E 6

F8

13 To F7 17
12 To F7 18
11 To F7 19
10 To F7 20

B-61

A6 A24
3 OF 4

BEST AVAILABLE COPY

B5A2	B5B4	B5C6	B5D10	B5E12	B5F15
D6D13	C5B15	D2D3	E4D13	E8I4	E2C12
B7B5				F8I4	
				A5B15	
				C7A1	

C9A2	C9B4	C9C6	C9D10	C9E12	C9F15
D6A1	C6A2	(9)	C7B6	B3B5	A7A5
D4I			E2A2		

C7A2	C9B4	C9C6	C9D10	C9E12	C9F15
B4A3	B4B10	B6A3	E2C13	P1I	(20)
	C3B10			A5B14	
	E9A7			C9A3	
				C5B1	
				A5A9	
				C5A9	

D8A2	D8B4	D8C6	D8D10	D8E12	D8F15
D9A4	C5B14	E3A2	C7D13	A6B11	E8I
F3D13			D2B11,12		

A6A24

4 OF 4

APPENDIX C

HONEYWELL CD 400 SERIES INPUT CAPACITANCE STUDY

(Reproduction of Honeywell letter report of 2 December 1976)

2 December 1976

TO: R.L. Matthews

FROM: T.L. Overpeck

SUBJECT: CD4000 Series CMOS Input Capacitance Study

SUMMARY

This study was undertaken to determine the input capacitances for CD4000 series CMOS devices used in NEARTIP. Vendor data sheets, MIL-M-38510, and visits to National and Motorola were utilized to compile a listing of input capacitance values. These values, together with device output impedance specifications, were used to compute worst-case pulse rise and fall time values. From this it was found that the gate loading design guideline being used by NUC has a 3:1 safety factor, and there should not be any problems related to capacitive loading of CMOS gates in NEARTIP hardware.

DISCUSSION

The study was begun by compiling a list of vendor data obtained from catalog data sheets. There was a wide disparity of values resulting from this study; for example, on the CD4006 a ratio of 5:1 exists in the CLOCK input capacitance values. Therefore, visits were made to National and Motorola CMOS facilities in order to obtain actual input capacitance data and to obtain first-hand information on the nature and character of CMOS input capacitance.

The data obtained from National and Motorola, plus catalog and MIL-M-38510 data is shwon in Table 1. Note that both National and Motorola supplied data for relatively few devices; however, they consider these values typical of a broad spectrum of product. For example the Motorola 4002 and 4012 data is typical of all gate inputs. In addition to actual data both Motorola and National supplied "estimates" of typical input capacitance for the device types. Motorola was more specific in this, although the value for the 4012 does not correlate with actual data given. National supplied a less specific listing, specifying most devices as 4-5.5 pf, and no data for those devices which would tend to run higher.

National furnished the best treatise on the makeup of input capacitance; a discussion by John Jorgensen, CMOS Design Manager. Input capacitance is composed of the sum of the capacitances associated with the:

- Package (0.8 to 1.7 pf)
- Input protection diode to V_{SS} (1 to 2 pf)
- Inverter stage (1 to 2 pf)

In addition to the above, there are gate-drain and gate-source capacitances associated with the P and N channel transistors of the input inverter stage. The gain of this stage is 10-20, and this results in a capacitance multiplication factor as the device switches through threshold. Figure 1 illustrates this for a 4601 B (CD4001) device switched from a "0" input to "1" input at V_{DD} = 15 V. Integrating under the curve results in C_i = 3.1 pf compared to 5.04 pf measured on a steady-state basis. This characteristic becomes even more pronounced at V_{DD} = 5 V (see appendix A data sheet).

Both National and Motorola were asked the following questions, with both furnishing essentially the same answers:

1. Is C_i affected by V_{DD}? Ans. Not significantly.

2. Is C_i affected by temperature? Ans. Not significantly.

3. What is the typical output impedance of the devices? Ans. No one has ever asked about this - consult data sheets for rise/fall times and output voltage vs. current sinking capability.

4. What is the effect of V_{DD} on output impedance? Ans. Referring to output rise and fall times, if these are given at V_{DD} = 5 V then use t_r and t_f values divided by 4 to obtain 15 V values. If V_{DD} is given as 10 V, then divide by 1.25.

5. What is the effect of temperature on output impedance? Ans. +0.3%/°C. (Represents +13.8% at +71°C.)

6. What are the typical clock rise time or pulse input rise times on the devices which have such requirements? Ans. Consult data sheets. Data shown represent at least a 2:1 safety factor, when operating voltage is factored in as shown in question 4.

7. What is your MIL-STD-883 Level B capability? Ans. Answers to this question differed greatly. National has all product available to 883 Level B. Motorola does not have any product available. They have just acquired the necessary test equipment (temp chambers, dynamic test gear, etc.) and plan to have some product available first quarter 1977. Other product will follow throughout 1977.

8. What is the future availability of types not now produced? (Motorola question only; National produces all, if the 4070 can be substituted for the 4030.) Ans. Motorola does not plan to produce the missing devices. (4019, 4029, 4047, and 4048).

9. Do you have any application notes regarding AC operation of CMOS? Ans. Neither had any specific notes or suggestions to offer, referring instead to previously published notes by RCA and Harris, and to magazine articles.

National and Motorola personnel contacts are listed in Appendix A, along with data sheets furnished by each.

Table 2 illustrates the Motorola, National and RCA catalog data maximum transition times of each CMOS type. These are all specified for a 50 pf load and 15 V operation, except as noted. Therefore, an estimate of output impedance can be derived, and thereby a calculation of the maximum allowable capacitance (or gate loads) for a given rise time requirement can be made. Data for the CD4019 and CD 4029 was obtained from Fairchild CMOS data sheets.

Following is a calculation of a worst-case capacitance load:

- Maximum transition time in Table II: 130 nsec (4013, 4027, 4042) Increase for 71°C: (71°C - 25°C times 0.3%/°C) = 1.138 X 130 = 147.94 = 148 nsec.

- Compute number of RC time constants for 10% to 90% pulse amplitude: 10% = .105 RC; 90% = 2.3 RC; therefore, 10% to 90% rise time is 2.2 RC.

- Compute maximum output impedance: $148 \times 10^{-9} = 2.2 \times R \times 50 \times 10^{-2}$
  $R = 1345$ ohms

- Maximum rise time allowed on CMOS prints is 3 microseconds; applying a 2:1 safety factor this becomes 1.5 microseconds. Compute the maximum capacitive load the 1345 ohm output impedance can drive without degrading the rise time above 1.5 microseconds:

  $2.2 \times 1345 \times C = 1.5 \times 10\text{-}6$
  $C = 507$ pf

- Maximum gate load in Table I: 20 pf (4049) (Motorola estimates this at 17-19 pf, they are changing their data sheet to specify 20 pf, maximum.) Calculate number of CD4049 inputs a CD4013, 4027 or 4042 could drive:

  $$N_g = \frac{507}{20} = 25$$

  The next worst case load in Table I is the 12 pf maximum specified by MIL-M-38510. On this basis 42 loads could be driven. For a typical gate input such as the National CD4020, and rounding 4.7 pf to 5 pf, over 100 loads could be driven.

  Therefore the 9 loads specified by MDC as a design goal is very conservative, representing at worst a 3:1 saftey factor.

Bob

RIO/lw

TABLE 1

CD4000 SERIES CMOS INPUT CAPACITANCE STUDY (CAPACITANCE IN PICOFARADS)

PART TYPE	FAIRCHILD/ CATALOG	HARRIS/ CATALOG	MOTOROLA/ CATALOG	MOTOROLA/ DATA	MOTOROLA/ ESTIMATE	NATIONAL/ CATALOG	NATIONAL/ DATA	NATIONAL/ ESTIMATE	RCA/ CATALOG	S^3/ CATALOG	MIL-M-38510
4001	1.5T, 5M-A	5T	5T, 7.5M	ND	3-5	5T, 7.5M-A	3.0	4-5.5	5T-A	5T-A	12M
4002	1.5T, 5M-A	5T	5T, 7.5M	3.1-3.8	5-7	5T-A	NO	4-5.5	5T-A	5T-A	12M
4006	1.5T, 5M-A	NA	5T, 7.5M	ND	3-5	5T DATA 6T CLOCK	ND	ND	5T DATA 30T CLOCK	5T	7M
4007	1.5T, 5M-A	5T	5T, 7.5M	ND	6-8	5T-A	ND	4-5.5	5T-A	5T-A	12M
4011	1.5T, 5M-A	5T	5T, 7.5M	ND	6-8	5T, 7.5M-A	2.7-3.1	4-5.5	5T-A	5T-A	12M
4012	1.5T, 5M-A	5T	5T, 7.5M	2.9-3.3	8-9	5T-A	ND	4-5.5	5T-A	5T-A	12M
4013	1.5T, 5M-A	5T	5T, 7.5M	ND	3-5	5T, 7.5M-A	ND	4-5.5	5T-A	5T-A	12M
4015	1.5T, 5M-A	7T-A	5T, 7.5M	ND	3-5	5T	ND	4-5.5	5T	7T-A	7M
4019	1.5T, 5M-A	4T A-B 6T K_a,K_b	NA	NA	NA	5T A-B 12T K_a,K_b	ND	ND	5T A-B 12T K_a,K_b	4T A-B 6T K_a,K_b	12M
4020	1.5T, 5M-A	5T	5T, 7.5M	ND	3-5	5T-A	3.6-4.7	4-5.5	5T-A	5T-A	7M
4023	1.5T, 5M-A	5T	5T, 7.5M	ND	7-9	5T-A	ND	4-5.5	5T-A	5T-A	12M
4024	1.5T, 5M-A	5T	5T, 7.5M	ND	3-5	5T, 7.5M-A	ND	4-5.5	5T-A	5T-A	7M
4025	1.5T, 5M-A	5T	5T, 7.5M	ND	4-6	5T-A	ND	4-5.5	5T-A	5T-A	12M
4027	1.5T, 5M-A	5T	5T, 7.5M	ND	3-5	5T, 7.5M-A	ND	4-5.5	5T-A	5T-A	12M No
		5T	NA	NA	NA	5T-A	ND	4-5.5	5T-A	5T-A	NA
	A	5T	NOTE 5 5T, 7.5M	ND	3-5	5T	ND	4-5.5	5T-A	5T-A	12M
4040	1.5T, 5M-A	5T-A	NOTE 5 5T, 7.5M	ND	3-5	5T-A	ND	4-5.5	5T-A	5T-A	NA
4042	1.5T, 5M-A	5T	NOTE 5 5T, 7.5M	ND	3-5	5T, 7.5M-A	ND	4-5.5	5T-A	5T-A	NA
4047	NA	NA	NA	NA	NA	5T, 7.5M-A	ND	4-5.5	5T-A	NA	NA
4048	NA	NA	NA	NA	NA	ND	ND	4-5.5	5T-A	NA	NA
4049	1.5T, 5M-A	15T-A	10T, 15M	17.3-18.6	17-19	5T-A	ND	4-5.5	15T	10T	12M
4050	1.5T, 5M-A	5T-A	10T, 15M	5.75-7.2	5-7	5T-A	ND	4-5.5	5T	5T	12M
4066	1.5T, 5M-A	5T-A	5T-A	3.4-4.3	3-5	5T-A	ND	ND	5T-A	NA	12M

NOTES:

1. T = TYPICAL VALUE
2. M = MAXIMUM VALUE
3. NA = NOT AVAILABLE FROM THIS MANUFACTURER OR NOT ON QPL (MIL-M-38510)
4. A = ANY INPUT
5. AVAILABLE AS THE MC 14070B

TABLE 1

CD4000 SERIES CMOS INPUT CAPACITANCE STUDY (CAPACITANCE IN PICOFARADS)

PART TYPE	FAIRCHILD/ CATALOG	HARRIS/ CATALOG	MOTOROLA/ CATALOG	MOTOROLA/ DATA	MOTOROLA/ ESTIMATE	NATIONAL/ CATALOG	NATIONAL/ DATA	NATIONAL/ ESTIMATE	RCA/ CATALOG	S^3/ CATALOG	MIL-M-38510
[illegible]	[illegible]	5T	5T, 7.5M	ND	3-5	5T, 7.5M-A	3.0	4-5.5	[illegible]		
[illegible]	[illegible]	5T	5T, 7.5M	3.1-3.8	5-7	5T-A	ND	4-5.5	[illegible]		
[illegible]	1.5T, 5M-A	NA	5T, 7.5M	ND	3-5	5T DATA 6T CLOCK	ND	ND	5T DATA 30T CLOCK	5T	7M
4007	1.5T, 5M-A	5T	5T, 7.5M	ND	6-8	5T-A	ND	4-5.5	5T-A	5T-A	12M
4011	1.5T, 5M-A	5T	5T, 7.5M	ND	6-8	5T, 7.5M-A	2.7-3.1	4-5.5	5T-A	5T-A	12M
4012	1.5T, 5M-A	5T	5T, 7.5M	2.9-3.3	8-9	5T-A	ND	4-5.5	5T-A	5T-A	12M
4013	1.5T, 5M-A	5T	5T, 7.5M	ND	3-5	5T, 7.5M-A	ND	4-5.5	5T-A	5T-A	12M
4016	1.5T, 5M-A	7T-A	5T, 7.5M	ND	3-5	5T	ND	4-5.5	5T	7T-A	7M
4019	1.5T, 5M-A	4T A-B 6T K_a,K_b	NA	NA	NA	5T A-B 12T K_a,K_b	ND	ND	5T A-B 12T K_a,K_b	4T A-B 6T K_a,K_b	12M
4020	1.5T, 5M-A	5T	5T, 7.5M	ND	3-5	5T-A	3.6-4.7	4-5.5	5T-A	5T-A	7M
4023	1.5T, 5M-A	5T	5T, 7.5M	ND	7-9	5T-A	ND	4-5.5	5T-A	5T-A	12M
4024	1.5T, 5M-A	5T	5T, 7.5M	ND	3-5	5T, 7.5M-A	ND	4-5.5	5T-A	5T-A	7M
4025	1.5T, 5M-A	5T	5T, 7.5M	ND	4-6	5T-A	ND	4-5.5	5T-A	5T-A	12M
4027	1.5T, 5M-A	5T	5T, 7.5M	ND	3-5	5T, 7.5M-A	ND	4-5.5	5T-A	5T-A	12M
4028	1.5T, 5M-A	5T	NA	NA	NA	5T-A	ND	4-5.5	5T-A	5T-A	NA
4030	1.5T, 5M-A	5T	NOTE 5 5T, 7.5M	ND	3-5	5T	ND	4-5.5	5T-A	5T-A	12M
4040	1.5T, 5M-A	5T-A	NOTE 5 5T, 7.5M	ND	3-5	5T-A	ND	4-5.5	5T-A	5T-A	NA
4042	1.5T, 5M-A	5T	NOTE 5 5T, 7.5M	ND	3-5	5T, 7.5M-A	ND	4-5.5	5T-A	5T-A	NA
4047	NA	NA	NA	NA	NA	5T, 7.5M-A	ND	4-5.5	5T-A	NA	NA
4048	NA	NA	NA	NA	NA	ND	ND	4-5.5	5T-A	NA	NA
4049	1.5T, 5M-A	15T-A	10T, 15M	17.3-18.6	17-19	5T-A	ND	4-5.5	15T	10T	12M
4050	1.5T, 5M-A	5T-A	10T, 15M	5.75-7.2	5-7	5T-A	ND	4-5.5	5T	5T	12M
4066	1.5T, 5M-A	5T-A	5T-A	3.4-4.3	3-5	5T-A	ND	ND	5T-A	NA	12M

NOTES:

1. T = TYPICAL VALUE
2. M = MAXIMUM VALUE
3. NA = NOT AVAILABLE FROM THIS MANUFACTURER OR NOT ON QPL (MIL-M-38510)
4. A = ANY INPUT
5. AVAILABLE AS THE MC 14070B

K+E 4 X 4 TO THE INCH 46 0253
7 X 10 INCHES MADE IN U.S.A.
KEUFFEL & ESSER CO.

FIGURE 1 -

NATIONAL 4601B (CD4001)
C_L vs. V_{IN}

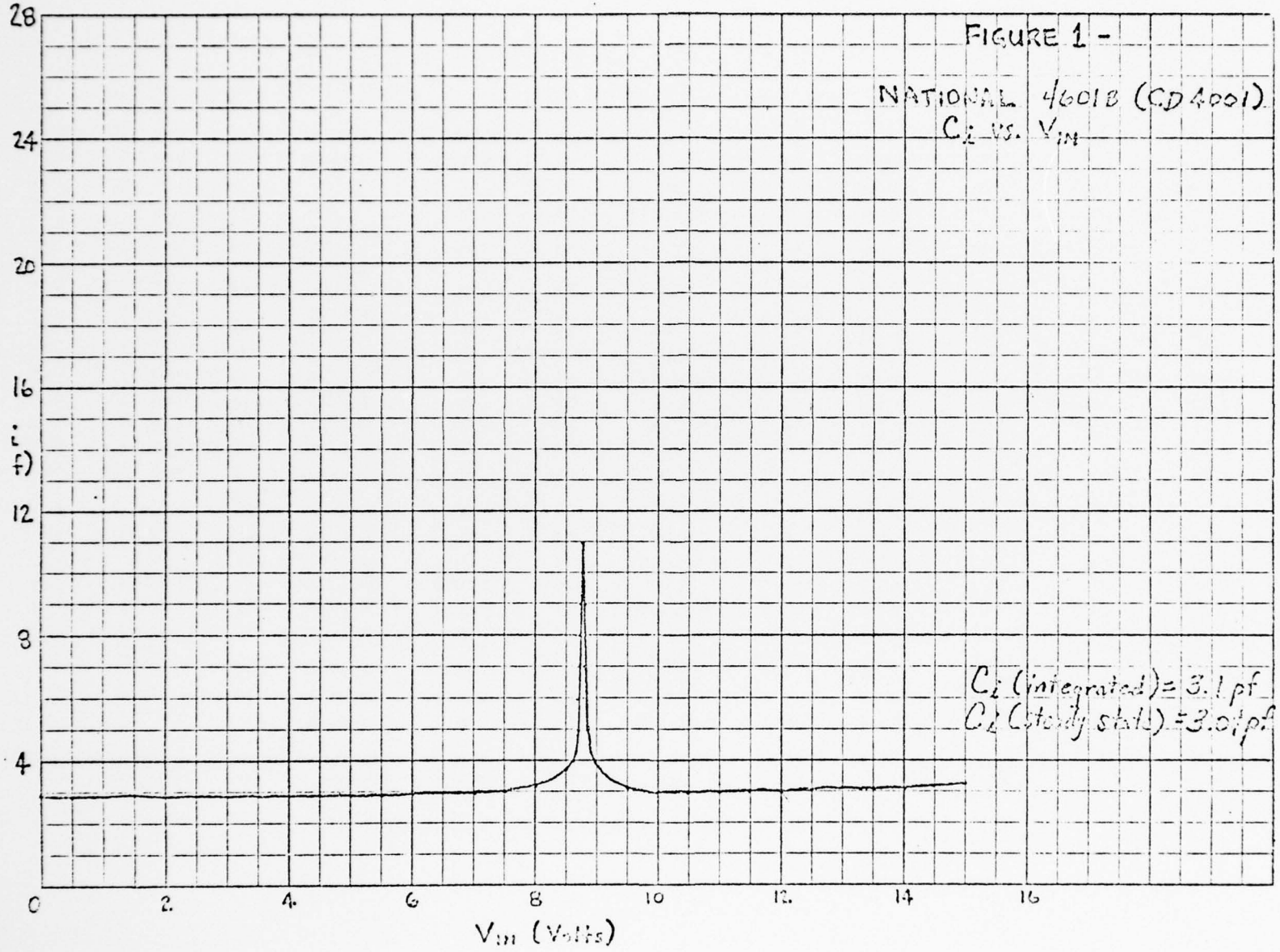

TABLE 2 CMOS OUTPUT TRANSITION TIMES

(TIMES IN NANOSECONDS, MAXIMUM, AT V_{DD} + 15V, C_L = 50 pf
HIGH TO LOW AND LOW TO HIGH UNLESS NOTED)

	MOTOROLA	NATIONAL	RCA	REMARKS
4001	80	80	80	
4002	80		80	
4006	110 LH			[illegible]
	55 HL			
4007	60 LH			
	50 HL			
4011	80	80	80	
4012	80		80	
4013	130 LH	80	80	
	80 HL			
4015	110 LH			
	55 HL			
4019				NOTE 4
4020	110 LH			
	55 HL			
4023	80		80	
4024	110 LH	80		
	55 HL			
4025	80		80	
4027	130 LH	80	80	
	80 HL			
4029				NOTE 5
4030		80		NOTE 2
4040	110 LH			
	55 HL			
4042	130 LH	100	80	
	80 HL			
4047		80		
4048			70	NOTE 3
4049	80 LH		60 LH	
	30 HL		30 HL	

TABLE 2 (CON'T)

	MOTOROLA	NATIONAL	RCA	REMARKS
4050	80 LH 30 HL		60 LH 30 HL	
4066	52 LH 58 HL			

NOTES: 1 - "LH" = LOW TO HIGH TRANISTION TIME; "HL" = HIGH TO LOW TRANSITION TIME

2 - CD4070 TYPE

3 - 10 V OPERATION, "A" TYPE

4 - FIARCHILD DATA 45 NSEC.

5 - FAIRCHILD DATA 23 NSEC LH: 18 NSEC HL

APPENDIX A NATIONAL AND MOTOROLA PERSONNEL CONTACTS AND CMOS DATA SHEETS.

National (Santa Clara, Ca.)

Sharon (Sam) O'Connell - Military/Aerospace Marketing Manager, 408-737-5880

Bob Bennett - CMOS Product Marketing Manager 408-732-5000

John Jorgensen - CMOS Design Manager, 408-737-5683

Motorola (Austin, Texas)

Rick Goeld - Production Manager, 512-928-2600

Bruce Harting - CMOS Product Marketing Engineer, 512-928-2600 ext. 535

Mike Hadley - CMOS Applications Engineer, 512-928-2600