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MANUFACTURING METHODS AND ENGINEERING FOR TFT ADDRESSED DISPLAY--ETC(U)
FEB 78 W L ROGERS, F C LUO, H Y WEY DAAB07-76-C-0027
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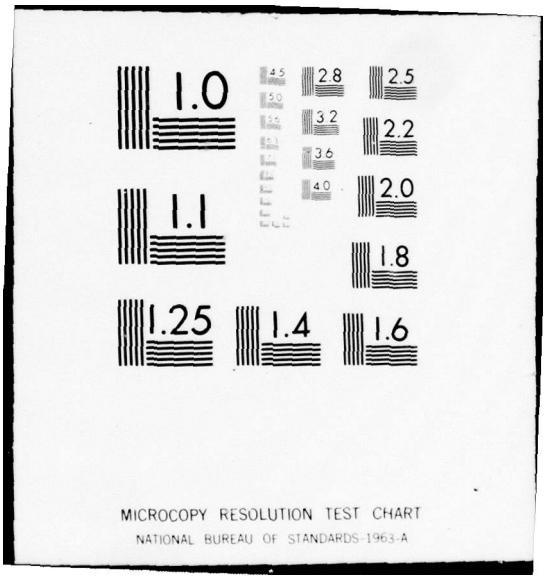
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(6) MANUFACTURING METHODS AND ENGINEERING FOR TFT ADDRESSED DISPLAY.

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for period of

August 7, 1977 to November 7, 1977

(19) Prepared by W. L. Rogers, F. C. Luo, H. Y. Wey, S. D. Burkholder, M. Green, [redacted]

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SIXTH QUARTERLY REPORT ON MANUFACTURING METHODS AND ENGINEERING FOR TFT ADDRESSED DISPLAY

for period of

August 7, 1977 to November 7, 1977

Prepared by W. L. Rogers, F. C. Luo,
H. Y. Wey, S. D. Burkholder, M. Green,
R. E. Stapleton

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Abstract

During this period the major emphasis has been on fabricating a number of high quality displays. The process improvements previously identified as necessary for success were implemented with the result that the objective has been met. Four highly legible half panels were packaged into two engineering samples and tested. One sample incorporates a deposition sequence change which improved drift characteristics.

A total of 38 substrates (starts) were made and evaluated on the basis of quality and transistor characteristics prior to packaging. This data has been summarized and tabulated. Abnormal transistor drift was an important factor contributing to rejects together with marginal mask alignment and mask to substrate contact.

Parallel effort to resolve the problems of transistor drift was begun in the development activity.

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ABSTRACT

During this period the major emphasis has been to fabricate a number of high quality displays. The process improvements previously identified as necessary for success were implemented with the result that the objective has been met. Four highly legible half panels were packaged into two engineering samples and tested. One sample incorporates a deposition sequence change which improved drift characteristics.

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1.0 PURPOSE

The overall objective of this program is to develop mass production methods and techniques for thin film transistor display technology. This novel technology is most amenable to computer control and the methods in development are based on an existing, Westinghouse developed, computer controlled thin film pilot line. Versions of the display in development have been made, with considerable success, in laboratory style equipment and this work continues under direct corporate support. The program includes the development of methods, procedures and optimal recipes followed by the rigorous examination of the displays for performance and life.

2.0 RESULTS AND DISCUSSION

2.1 Introduction

A number of process changes and improvements have been introduced during the past several months and during this report period. The changes have reduced shorts and opens, improved pattern geometry, reduced transistor drift and, in general, improved the overall quality of the circuits. During this report period the pilot line was operated in a pseudo-production mode. The primary objective was to produce a number of high quality displays. In the following sections the process improvements that have been implemented will be discussed together with the results of the production run.

2.2 Summary of Process Improvements/Changes

The following is a listing of important process changes and improvements that have been incorporated in the basic recipe.

Changes introduced to reduce shorts and opens

- Rigorous mask cleaning, physical scrubbing
- Better mask inspection after cleaning
- Use of 2-3 substrates as "mops" to collect surface particulates on masks
- Use of electron-beam gun hearth liners for aluminum, copper, indium and gold
- Additional shielding and improved designs
- Modified masks to reduce thickness of crossover insulator (reduced stress and cracks)
- Improved substrate bake-out procedures
- Sweep electron-beam over edges of Al_2O_3 charge for more uniformly degassed melt

- Optimized all source pre-conditioning procedures for better outgassing
- Clean surface of indium source to remove oxides
- Changed edge contact pad metallization to Al/Cu/Au to insure continuity with Al interconnects
- Sand blast Kovar back-up shields to increase film adherence
- Corrected problem with Sloan controller to eliminate power spikes

Changes Introduced to Improve Pattern Geometry (Alignment, Sharpness)

- Standardized on thinner masks (.0037 inches thick)
- More frequent inspection and replacement of oversize teflon bushings

Changes Introduced to Reduce Transistor Drift

- Adapt direct indium doping method. Deposit 2-3 angstroms of indium on CdSe.
- Modify deposition sequence for multi-layer storage capacitor

2.3 Outline of Production Process

A typical run consists of a single pump-down event. Two circuits are usually produced per run. Additional substrates are loaded into the vacuum chamber to act as "mops". These substrates are engaged with each mask to collect any surface contamination before the two "good" substrates (circuits) are processed. After completing all layers on two good substrates, the vacuum chamber is unloaded. Each substrate is visually inspected at 50X to 100X. Transistor geometry is studied over the entire substrate and any abnormalities are recorded. These may include gate misalignment, shifted top and bottom gates, double images and poor pattern sharpness. Often these defects occur only on one side of a substrate or in a particular section. Other defect catagories are also noted such as pin scratches, substrate cracks, substrate debris usually caused by premature mask peeling (insulator), specks in insulator films, and "rabbit tracks". Rabbit tracks are believed to be caused by sharp projections on the mask surfaces. After visual inspection, the substrates are annealed at

350°C for 10 hours in flowing dry nitrogen. A second visual inspection follows the annealing step to detect any metallic corrosion effects, insulator cracks or peeling.

The next step is to electrically test a small number of transistors at the corners and middle of each substrate. A power and logic transistor in each of these areas is manually probed and connected to a 576 Tektronix curve tracer. Data is taken on a number of parameters including:

- "on" current at Vg = 20V, V_{SD} = 10V
- drain current (leakage) at Vg = 0V, V_{SD} = 20V
- drain current (off current) at Vg = - 20V, V_{SD} = 20V
- voltage breakdown between gate and source/drain
- capability of the power transistor to withstand high drain voltages (> 300 volts)
- transistor "on" and "off" stability

Shorts are then recorded between the gate and ground bus, source and gate bus. Busbar continuity is also checked at this point. Often shorts can be "cleared" if only a few are detected. When a substrate passes all electrical tests, EL phosphor layer is applied. After application of the phosphor, the substrate can be connected to the exerciser to display an array of alphanumeric characters. At this stage a variety of defects can be visually observed such as:

- open busbars
- additional shorts produced by the high ac voltages
- poor ground contacts
- transparent top electrode problems (continuity)
- phosphor problems (connection to the EL circuit electrode)

Techniques are being developed to repair most of these defects. Repairs are often made if the number of defects is small and the location is accessible. After completing all repair work (if needed) the panel is checked on the exerciser and a photograph is taken of the displayed characters for future reference. The inventory of good half panels is

stored in a dry box. The best half panels are selected for final packaging and sealing. The basic steps in the sequence outlined above are as follows:

1. Vacuum deposit circuit matrix
2. Visual inspection of circuit
3. Anneal circuit
4. Visual inspection of circuit
5. Electrical test
6. Clear shorts
7. Apply EL phosphor, test
8. Repair defects (if necessary and feasible)
9. Inventory panels, photograph display
10. Select best panels, final package

2.4 Visual Circuit Inspection

During the period covered by this report a total of 38 substrates were produced in the computer-controlled vacuum deposition facility. Table I lists these substrates in chronological order (top to bottom of table). Four defect categories are tabulated

1. Alignment - good or bad(√)
2. Mask contact - good or bad(√)
3. Scratches - none or yes (√)
4. Glass condition (cracks or breakage) - good or bad (√)

Under "comments" a check indicates the substrate should be rejected at this stage. However, most of these substrates were annealed and electrical measurements made on transistors. This was done to monitor the deposition process to determine if the transistors were within specification. Twenty (20) out of thirty-eight (38) substrates are considered rejects as indicated in Table I because of visual defects.

Table I

Visual Inspection

Substrate No.	Alignment Bad (✓)	Mask Contact Bad (✓)	Scratches Yes (✓)	Glass Condition Bad (✓)	Comments Rejected
215-2					
216-6					
222-2					
223-6			✓		
227-2		✓			✓
228-8		✓			✓
231-2		✓			✓
234-8		✓			✓
237-2					
241-8				✓	✓
243-2					
244-6					
250-2		✓			
251-6			✓		✓
255-2					
256-4				✓	✓
258-1	✓				✓
259-8					
263-4					
264-8	✓		✓		✓
268-4					
269-2	✓				✓
269-8	✓				
272-4					
273-8	✓				✓
277-6					
278-8		✓			✓
283-6		✓			✓
284-8					
286-6	✓	✓			✓
287-8					
293-6		✓			
294-8	✓	✓			✓
300-6	✓	✓			✓
301-8	✓				✓
306-4	✓	✓			✓
307-8		✓			✓
311-6	✓	✓			✓

2.5 Electrical Tests

Table 2 tabulates the 18 substrates that passed the visual tests with respect to key measured electrical parameters. These include shorts, power transistor "on" current, power transistor drain current (leakage @ Vg = 0), logic transistor "on" current and logic transistor drain current (leakage @ Vg = 0). Any parameter that is abnormal (high number of shorts or excessive leakage currents) is considered cause for rejection which is indicated by a check (√) mark in the "comments" column. For example, substrate 216-6 is rejected because of excessive shorts but the transistors are within specifications. Substrate 263-4 has only a few shorts but the power transistors show a wide spread in leakage currents across the substrate (160 to 5000 nano-amperes).

2.6 Packaging Evaluation

Twelve of the eighteen substrates listed in Table 2 passed the electrical tests. A Riston insulator, EL powder phosphor and a transparent top electrode was applied to these circuits. At this stage the circuit is connected to an exerciser to display a set of alphanumeric characters. Table 3 shows the results of an estimate of legibility achieved for each of the substrates. The estimate ranges from 60% to 100%. The best circuits were selected for final sealing and these are designated Engineering Samples #1 and #2. Figures 1 and 2 are photographs of the display quality level achieved for each of these samples. It is evident that the quality is approaching that of a commercial or military standard. However, a number of elemental defects can be seen. Figures 3 and 4 show the same samples with all dots <u>on</u>. In Sample #1 (Figure 3) ∿68 elements are <u>off</u> on side A and ∿118 elements are <u>off</u> on side B. In Sample #2 (Figure 4) the count is approximately 29 and 48 <u>off</u> elements (side A and B). Figures 5 and 6 show the same samples in the erase mode. The <u>on</u> elements can be counted for each side of both samples. These residual defects include:

Table 2

Electrical Test Data

Substrate No.	Shorts	Power TFT			Logic TFT				Comments Reject (✓)
		I_{on}	Leakage (nA)		I_{on}		Leakage (nA)		
		µA	Min	Max	Min	Max	Min	Max	
215-2		Dead							✓
216-6	Yes	300	100	500	120	160	100	500	✓
222-2	Yes	300	400	4000	100	125	100	2000	✓
223-6		300-400	100	150	120	150	100	200	
237-2	Yes	250	20	4000	2	60	20	80	✓
243-2		---	---	---	---	---	---	---	
244-6	Yes	100-300	250	2000	100	150	50	1000	
250-2		120-500	200	1000	150	400	250	6000	
255-2		300	25	500	80	100	200	500	
259-8		60-300	100	300	100	150	100	250	
263-4		300-400	160	5000	100				✓
268-4		300-400	200	500	100	150	60	1000	
269-8		400	350	2000	50	150	200	300	
272-4		300-400	400	2000	150		200	4000	
277-6		400	40	1000	80	150	50	700	
284-8	2	300	200	1000	5	50	1	200	
287-8	1	300-400	100	1000	100	150	40	800	
293-6	Yes	300-400	100	500	100	150	300	2500	✓

Table 3

Packaging Evaluation

Substrate No.	Defects	Legibility	Comments
223-6	Scratched	60%	
243-2		80%	
244-6	Scratched	80%	
250-2	Marked	70%	Rabbit tracks
255-2		95%	Engineering Sample #2
259-8		95%	Engineering Sample #2
268-4		90%	
269-8	Al_2O_3 Specks	80%	
272-4		95%	
277-6	Marked	100%	Rabbit tracks
284-8		95% +	Engineering Sample #1
287-8		95% +	Engineering Sample #1

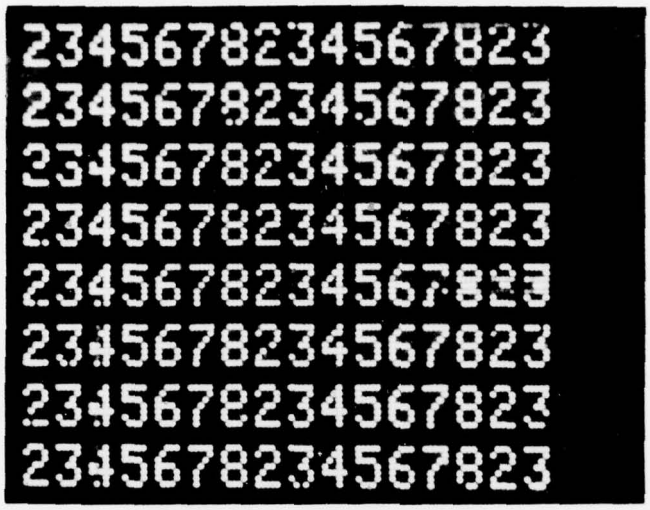

FIGURE 1-A
SAMPLE #1, SIDE A, CHARACTERS ON

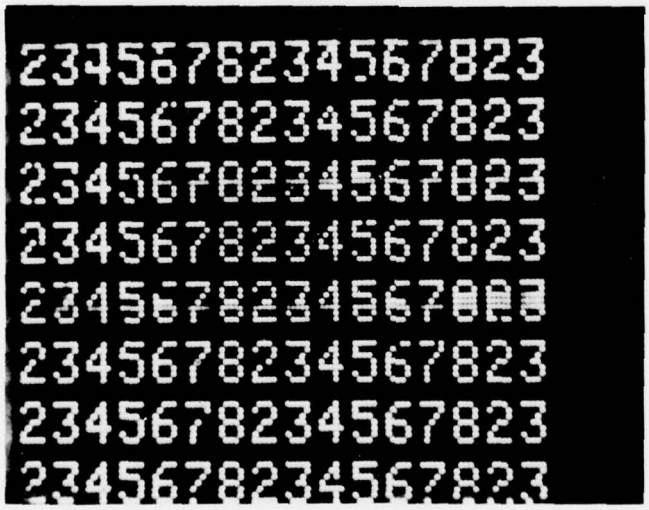

FIGURE 1-B
SAMPLE #1, SIDE B, CHARACTERS ON

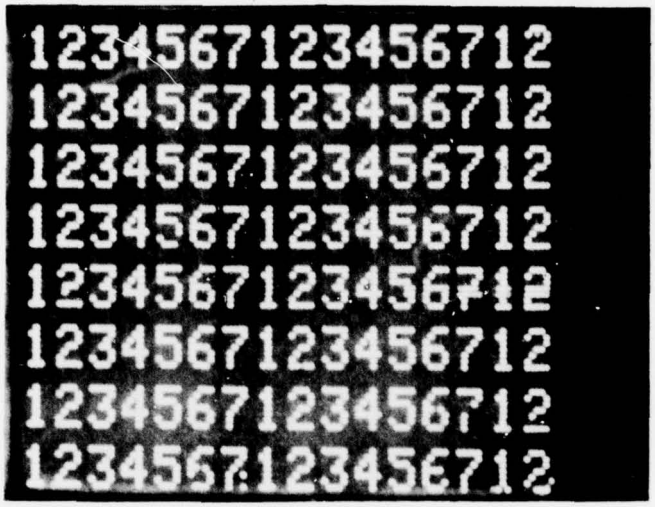

FIGURE 2-A
SAMPLE #2, SIDE A, CHARACTERS ON

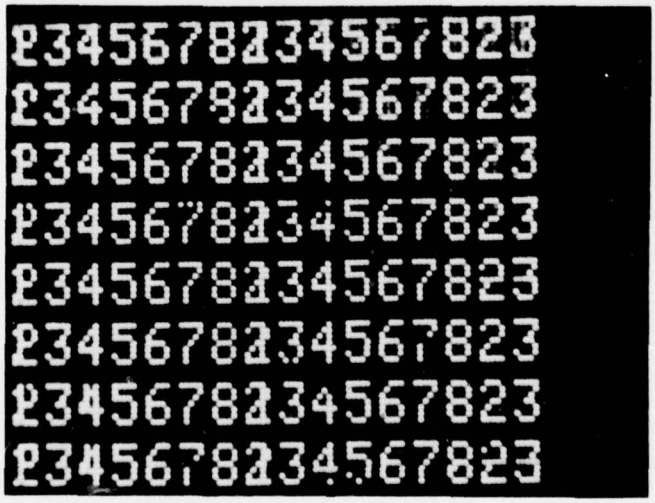

FIGURE 2-B
SAMPLE #2, SIDE B, CHARACTERS ON

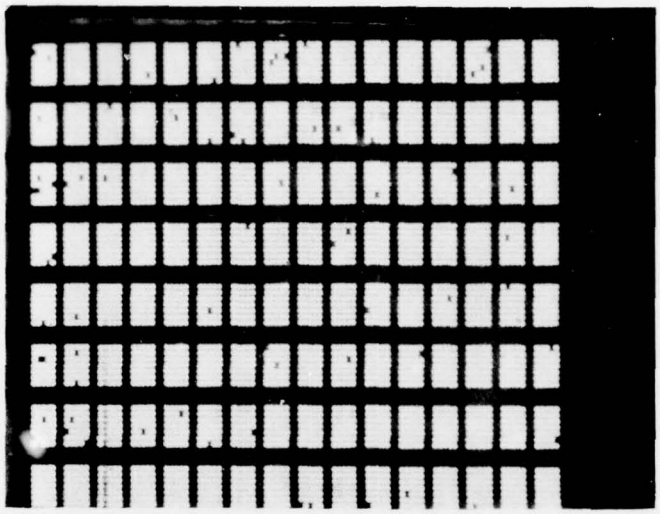

FIGURE 3-A
SAMPLE #1, SIDE A, ALL DOTS ON

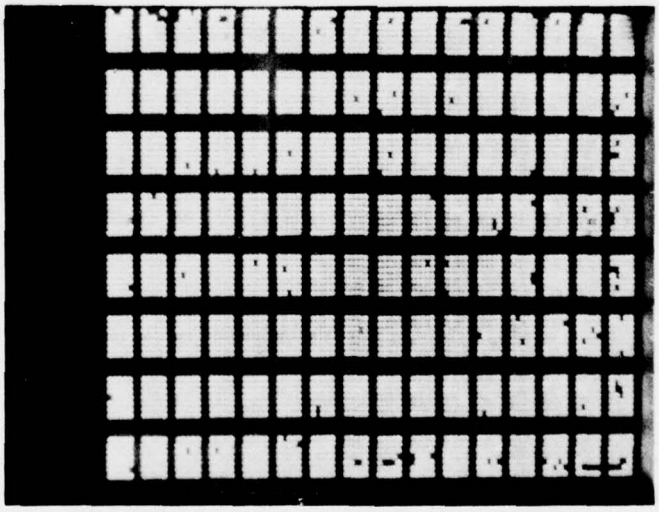

FIGURE 3-B
SAMPLE #1, SIDE B, ALL DOTS ON

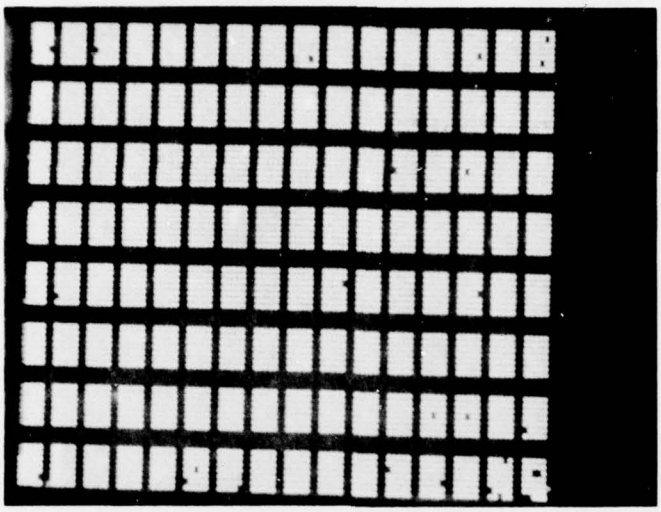

FIGURE 4-A
SAMPLE #2, SIDE A, ALL DOTS ON

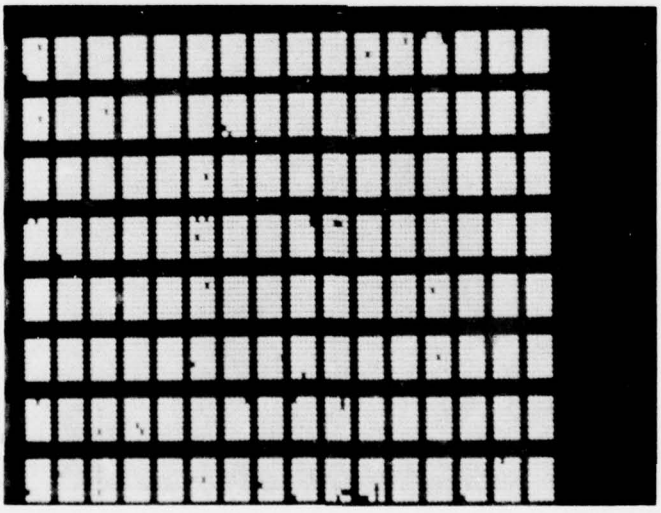

FIGURE 4-B
SAMPLE #2, SIDE B, ALL DOTS ON

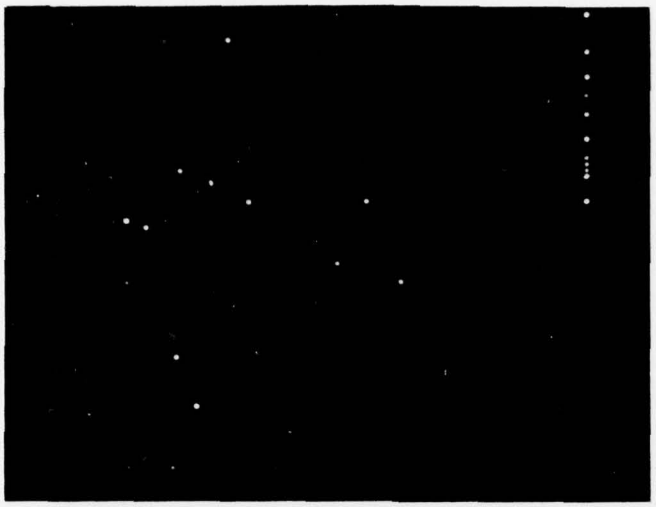

FIGURE 5-A
SAMPLE #1, SIDE A, ERASED MODE

FIGURE 5-B
SAMPLE #1, SIDE B, ERASED MODE

FIGURE 6-A
SAMPLE #2, SIDE A, ERASED MODE

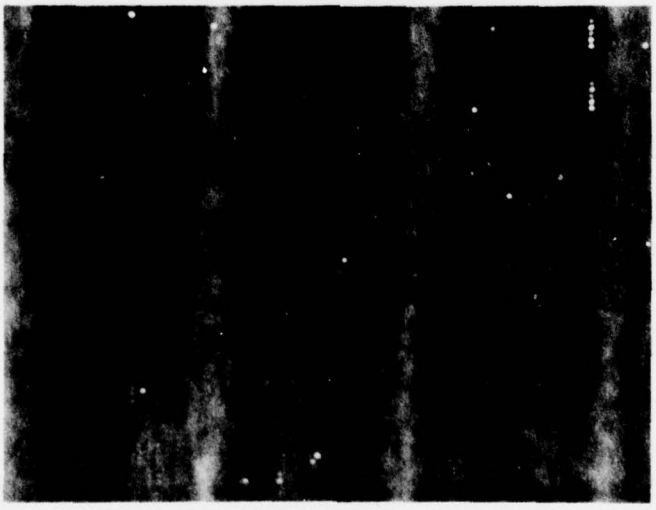

FIGURE 6-B
SAMPLE #2, SIDE B, ERASED MODE

- elements that are permanently on
- elements that are permanently off
- unconnected or broken lines that are either grounded (off) or float (on or off)
- crossover shorts that cause crosstalk

The on elements are caused by a variety of sources, for example:

(a) a short between the power device gate to drain causes a series capacitance condition that lights the elements.
(b) a short across the cell capacitor causes the power device gate to be pinned close to ground; the result is that the TFT is on and hence the EL cell is lit.
(c) a power device channel short permanently lights the EL element.
(d) in addition, if opens occur at the power TFT gate or drain or the logic TFT drain then the result is a lit element
(e) elements are off if, for example, the logic TFT gate is shorted to the drain so that the V_{bias} gate (average - 40V) pulls down the power TFT gate
(f) line opens or line crossover shorts are much more significant with respect to display legibility than are elemental defects.
The exact condition depends on the electrical state of the line at that instant, a logic TFT crossover short (or gate to source) causes arbitrary on or off unmodulatable lines. An open busline will float on, picking up the ac-EL voltage, alternately if it is grounded it will be off.

2.7 Conclusions

From the production run of 38 circuit starts 12 circuits reached the EL phosphor stage and were evaluated for legibility. Opens and shorts explain virtually all display defects. Figure 7 is a bargraph presentation of the status of each of the 38 circuits. It is apparent that the majority of circuits were rejected for obvious visual defects at an early stage in the overall process. These defects can be traced to alignment and mask to substrate contact problems.

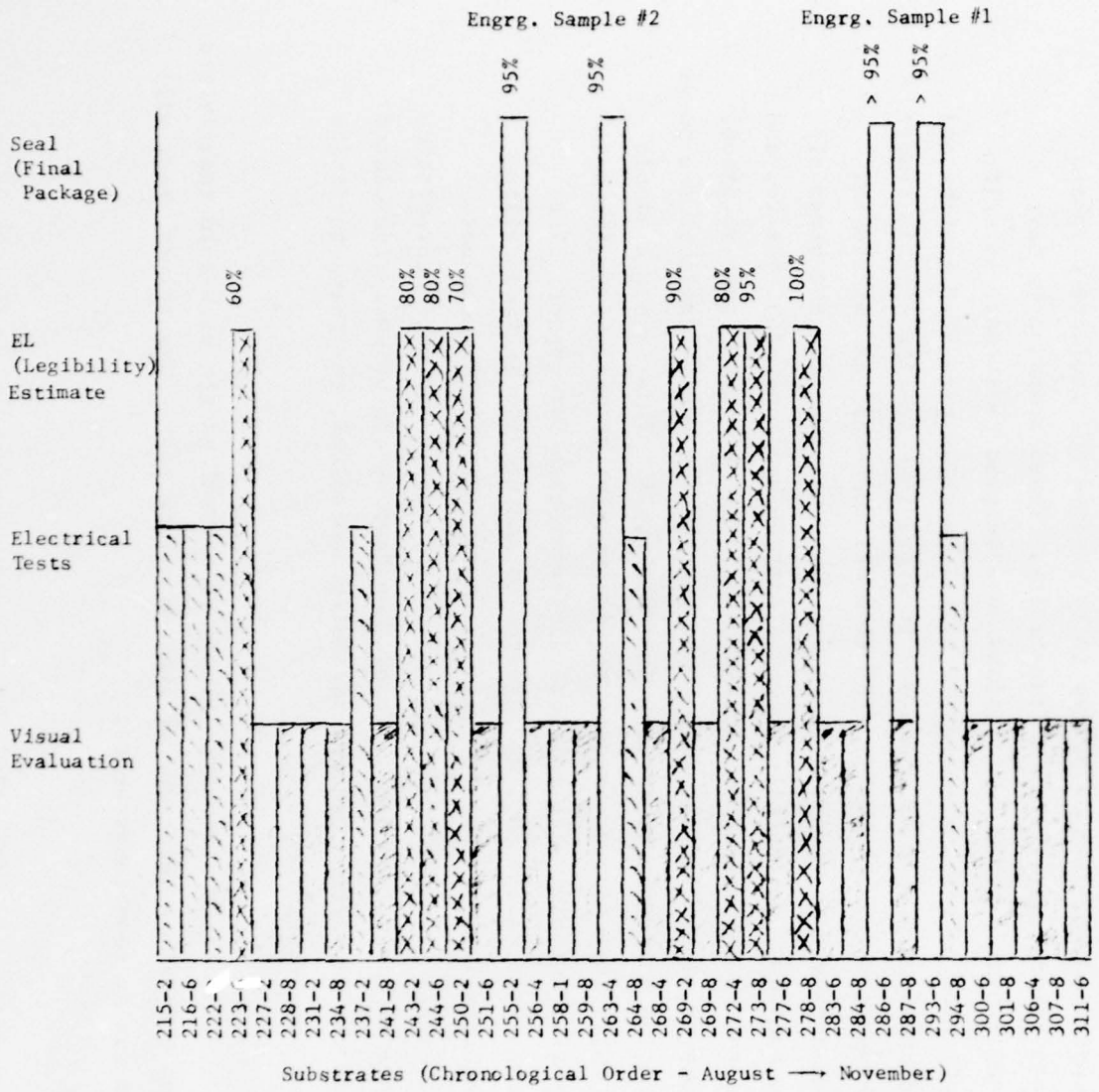

Figure 7

20 Fail Visual
6 Fail Electrical
5 Fail EL Legibility

3. RESULTS OF X-Y PANEL FABRICATION

Work has started on the fabrication of X-Y panels using gold/indium transistor source/drain instead of the present copper/indium. The objective is to produce and evaluate displays that incorporate the gold transistors. These transistors have been shown in other applications to have good resistance to drift (off transistors turn-on under static negative gate bias conditions). Engineering Sample #2 discussed in a previous section of this report showed considerable drift (off elements turn-on); an improvement was achieved in Engineering Sample #1 by re-arranging the order of depositions so that the ground electrode was located at the top and bottom of the elemental storage capacitor. A longer range solution, however, is to replace gold for copper in the source/drain of the power and logic transistor in each elemental cell. This is not a simple substitution process because the interactive effects of indium and cadmium selenide with gold are different than for copper. The transistor recipe must be adjusted to achieve the desired device characteristics. Gold transistors have historically been more difficult to reproduce which is a major reason for not incorporating them in a panel to date. Unless the devices are properly formulated and the deposition process carefully controlled, the characteristics can vary significantly.

It is planned to fabricate several panels with gold transistors and subject at least one of them to a life test. The initial test will be run at room temperature.

4. EXPECTED RESULTS NEXT QUARTER

- Fabricate more stable panels by the X-Y process and on the pilot machine.

- Design and install an improved substrate holder disengagement system and demonstrate operation.

- Start installation of a class 100 clean room area for the pilot machine and associated support operations.

5. PUBLICATIONS AND REPORTS

None

6. IDENTIFICATION OF PERSONNEL

A listing of people and hours charged to this contract in this quarter would only constitute a small amount of the total program since, as is well known to the Army, a major company funded program parallels this effort. All personnel are now carried on the Westinghouse program. They include:

Engineers	Technicians
Dr. David H. Davies	F. S. Youngk
Dr. F. C. Luo	H. B. Shaffer
Mr. R. E. Stapleton	D. Leksell
Mr. S. D. Burkholder	J. J. Gesner
Dr. H. Y. Wey	
Mr. W. L. Rogers	
Mr. T. Csakvary	

All the above are substantially 100% on the program.

Directly charged to the program in this quarter are:

		Hours Charged
Management:	Dr. M. Green	∿ 80

Additional minor efforts were put in by various personnel.