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TIME-DOMAIN TWO-DIMENSIONAL COMPUTER SIMULATION OF THREE-TERMIN--ETC(U)
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Time-Domain Two-Dimensional Computer Simulation of Three-Terminal Semiconductor Devices*

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Abstract

Special schemes for treating device geometry permit the use of the very fast Fourier analysis technique for solving the two dimensional Poisson's equation so that the dynamics of three terminal semiconductor devices can be computer simulated economically. FET's and bipolar devices have been successfully simulated.

I. Introduction

In recent years, computer simulation techniques have become an indispensable tool in solid-state device research and development. This is because the internal physics of these devices and their interaction with external circuits are usually governed by a system of highly nonlinear partial differential equations. The equations are intractable except in certain cases when they can be linearized. However, the linear solution loses some important aspects of the device physics and at best provides qualitative information.

One-dimensional dynamic computer programs provide good simulation for many devices such as Gunn, IMPATT and TRAPATT diodes. In this type of program the algorithms are relatively simple to formulate and the execution time is relatively short. This is because the solution of Poisson's equation can be reduced to the inversion of a bidiagonal matrix [2]. Three-terminal devices such as the bipolar transistor and the FET, due to the nature of their physical geometries require that simulation must account for at least two dimensions. The algorithms for solving Poisson's equation in two dimensions involves inversion of a tridiagonal matrix of large size. The usual technique for computation is the time consuming over-relaxation method. Thus for reasonable computer processing time, most two dimensional semiconductor device simulations are limited to the static case [3]-[5].

Through judicious choice of geometrical representations we have formu-lated a dynamic two-dimensional program for the simulation of three-terminal semiconductor devices. For bipolar devices, the program is two-dimensional in the collector region where carrier motion transverse to the direction of the applied electric field has a profound effect on the device physics. The emitter-base junction, owing to its inherent geometry, is adequately approximated by a one-dimensional R-C transmission line with a distributed current source. This scheme for treating the device geometry permits application of the very fast Hockney's technique [6] to two-dimensional dynamic simulation of the transistor and the CATT [7]. A description of the bipolar program and computational results are given in a companion paper [8]. Due to space limitations, this paper will focus on the simulation of the FET. The latter, being simpler in geometry, is completely simulated dynamically in two dimensions as described below.

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II. Description of the Computer Program

The physical models for FET simulation of both the conventional and the double-sided cases are shown in Fig. 1. The device internal physical effects treated in our program are the following: two-dimensional carrier transport resulting from electric field and diffusion; carrier and charge conservation during transport and avalanche processes; space charge effects resulting from mobile and fixed charges; field and time dependent avalanche process; nonlinear field-dependent carrier velocities, and velocity over-shoot when applicable (See Appendix). The external boundaries are: Ohmic contacts on the source and drain electrodes, Schottky barrier on the gate electrodes, electrode voltages, and conservation of terminal currents.

The equation governing the two dimensional device are:

Poisson's equation

$$\nabla^2\phi = -\frac{q}{\epsilon}(N_D + p - n)$$

and carrier transport

$$\left.\begin{aligned} \nabla\cdot(n\vec{v}_n) + \frac{\partial n}{\partial t} \\ \nabla\cdot(p\vec{v}_p) + \frac{\partial p}{\partial t} \end{aligned}\right\} = {}_n\alpha n|\underline{v}_n| + {}_p\alpha p|\underline{v}_p|$$

The symbols used in the above equations have the usual meaning. We proceed now to qualitatively discuss the procedure for solving the Poisson equation (which includes manipulation of boundary conditions), the continuity equation (which includes the contact problem and the stability criterion) and the definition of forces on carriers and their velocities.

The device is partitioned into 96 X 48 space increments (Δx, Δy) for the solution of Poisson's equation and carrier transport, as shown in Fig. 2. For computer economy, two time increments Δt_p and Δt_t are used for updating the Poisson equation and the transport equation respectively. The time increments are related by an integer such that $N\Delta t_t = \Delta t_p$. Thus in the duration of Δt_p the electric distribution remains constant while the carrier motion is updated N times (N = 2→12).

The use of Hockney's technique raises some complications in the FET simulation because the FET contains both Dirichlet and Neumann boundaries on the x = 0 and 48 edges, while the Hockney technique is applicable to either but not mixed boundaries. In addition, the extent of the boundary is time dependent. In order to alleviate the difficulties the Neumann boundaries, which arises from the gate depletion region (See Fig. 2), are converted to Dirichlet in each time increment. This could be done because no current can flow across the exterior boundaries (x = a) of the depletion region thus the condition $\frac{\partial\phi}{\partial x}\Big|_{x=a} = 0$ prevails. This condition, together with the known doping density and potential at all electrodes permits the evaluation of $\phi_1(a,y,t)$ and $\phi_2(a,y,t)$. Thus the potential $\phi(a,y,t)$ for $o \le y \le b$ is completely specified. The function $\phi(a,y,t)$ is Fourier analyzed for each Δt_p increment. The resultant Fourier components are then applied to appropriate location in Hockney's algorithm. The vertical boundaries at y = o and y = b are considered as planes of even symmetry. This is effected by using only a cosine expansion in the Fourier analysis.

The carrier transport is solved by an explicit technique. Due to the negative differential mobility in GaAs, formation of high field domain takes place under certain conditions. Therefore, it is necessary to use a sufficiently small time increment size Δt_t to resolve the domain formation and decay. The condition used in choosing the size of Δt_t to ensure a stable solution is $\frac{\Delta t_t}{\Delta x} \cdot v_{max} < \frac{1}{\sqrt{2}}$. Further refinements in solving the transport equation is the presentation of the divergent and gradient operators. Either forward or backward difference is used depending on the direction of carrier motion and diffusion force. This technique improves computation accuracy while preserving the symmetry (in the case of the double-sided FET). The ohmic contact at the source electrode is ensured by maintaining the mobile carrier density in the interior cells adjacent to the electrodes equal to the background doping. The surface y = 0 may be non-injecting (Figure 1a) or ohmic (Figure 1b) as desired. The drain electrodes and the surface y = b act as an infinite sink for elections.

Experimental v-E characteristic for GaAs or Si is used in specifying carrier velocities depending on the device material being simulated. However, instead of the electric field alone we define a force which includes diffusion:

$$\vec{f}_n = \nabla\phi - \frac{T}{n}\nabla n \qquad \text{for electrons,}$$

and

$$\vec{f}_p = -\nabla\phi - \frac{T}{p}\nabla p \qquad \text{for holes.}$$

The carrier velocities are:

$$\vec{v}_n = v_n(|f_n|) \cdot \vec{f}_n/|f_n|$$

and

$$\vec{v}_p = v_p(|f_p|) \cdot \vec{f}_p/|f_p|$$

The forces as defined are consistent with the concept of a quasi-Fermi potential. The scalar velocity functions are those available in the literature as v-E characteristics. For electrons in GaAs at very high frequencies (>20 GHz), the effect of the interband delay causing the 'velocity overshoot' is discussed in the Appendix. The subroutine dealing with the effect has been checked against Shur's calculation [9], but in the results presented below the subroutine was not activated.

III. Results and Discussion

Computational results indicate that the 96 X 48 cells provide good resolution in the simulation of the double-sided device. However, they are somewhat inadequate for the conventional device. This is because the conventional device has a semi-insulating substrate of thickness very large compared to any of the active region dimensions. While in the real world the potential at the bottom of the substrate may be set equal to zero without affecting the electric field distribution in the device active region, this is not true in our simulation per Figure 1a. The dimension "a" is divided into 48 equal space increments; consequently the surface x = 0 is not sufficiently far away from the active region for a good approximation as an equipotential surface. The same problem appears to exist in the work of Barnes and Lomax (10).

The speed of our computer program is approximately two orders of magnitude faster than those using the relaxation technique. It takes about one minute to complete one Δt_p (which consists of solving the Poisson's equation once the transport equation N times) in the 96 X 48 mesh points using the Honeywell-600 computer. On the other hand it takes five minutes to compute one time increment in a two dimensional 1000 mesh-point problem using the line relaxation technique on the same computer.

Figure 4 shows the potential distribution in a 'conventional' FET, 0.5μ thick on 1μ insulator substrate grounded at the lower edge. The electrode arrangement is such that the equipotential contours are well displayed. Because of the poor approximation inherent in this configuration discussed above, we prefer to consider the 'conventional' FET as one half of the double-sided FET and simulate only the latter.

Figure 5 shows the potential distribution in a double-sided FET. Since the time, length, doping density follow certain scaling laws while computer time step must satisfy the stability criterion, a 2μ by 8μ space is simulated. Higher frequency operation, except the velocity overshoot effect, can be scaled from the result.

Figure 6 shows time-sequence snapshots of the electron density distribution in the same FET at various times indicated.

Figure 7 shows the drain current as a function of time for two values of the gate voltages. In the Figures 5→7 the drain and gate voltages are applied stiffly at t = 0. Thus the response time of the FET is being studied. The peaks and valleys in the drain current vs. time suggest the Gunn effect in the FET, and this is evident in Figure 6 at times 40→68 psec. Note that there are more than 100 data points for each curve in Figure 7. The very finely sequenced pictures (not included here) strongly suggest two-dimensional Gunn domain ripples in the lower field regions in the source and drain, which might manifest themselves as very high frequency noises.

In conclusion, we have qualitatively discussed our computer simulation for two dimensions, and have presented some results on the GaAs FET. Large signal FET performance as well as the very high frequency effect due to the velocity overshoot will be carried out. Results on bipolar devices are reported on elsewhere.

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APPENDIX

An approximate treatment of the 'velocity overshoot' effect

We first assume that if there was only the light mass electronic energy band in GaAs the velocity-field v(E) characteristic would be such as shown in Figure 8, curve a. Curve b in the Figure represents the equilibrium v(E) characteristic. An electron having a velocity higher than that given by curve b at a constant electric field E_1 above the threshold field E_{th} may be assumed to decay along the vertical dashed line shown in Figure 8 with a time constant $\tau(E_1)$

$$v(t) = v_s(E_1) + \left\{ v_f(E_1) - v_s(E_1) \right\} e^{-t/\tau(E_1)} \qquad ---(1)$$

where v_f is for curve a, v_s for curve b, and it is assumed that at t = 0 the electron velocity is given by $v_f(E_1)$.

Consider an electric field as a function of position and let $E = E_{th}$ at $z = z_o$ and $E > E_{th}$ for $z > z_o$. An electron passing $z = z$ at t = 0 going along the +z direction would acquire a velocity $v(z_1)$ at $z_1 = z_o + \Delta z$.

$$v(z_1) = v_s(E(z_1)) + \left[v_f(E(z_1)) - v_s(E(z_1)) \right] \exp\left\{ - \frac{\Delta z}{v(z_o) \cdot \tau(E(z_1))} \right\} \qquad ---(2)$$

And at $z_i = z_o + i\Delta z$

$$v(z_i) = v_s(E(z_i)) + \left[v_f(E(z_i)) - v_s(E(z_i)) \right] \cdot \prod_{n=1}^{i} \exp\left\{ - \frac{\Delta z}{v(E(z_{n-1})) \cdot \tau(E(z_n))} \right\} \qquad ---(3)$$

The denominator in the exponential term should contain some average values of v and τ between the two adjacent z positions. The choice taken

in (2) and (3) is to facilitate simple updating computation of v as a function of s.

Note that if calculation is performed along the s path with constant increment Δs, then the corresponding Δt will inversely vary as $v(E(s))$. This is in fact a convenient way to calculate the effect of the 'velocity overshoot' on the f_t of the transistor. In the formulation of our computer simulation, however, the space grid size and the time step are fixed, and are chosen such that they satisfy the stability criterion as well as minimizing the pseudo-diffusion effect. Thus only the following approximate form is used for the product term in (3):

$$\prod_{n=1}^{i} \exp\left\{-K/\tau(E(x_n))\right\}$$

where $K = \Delta s/2 \times 10^7$ cm/sec. In addition, for the 2 dimensional simulation of the FET a further approximation is used the path s is along the defined y-direction only.

The data on the curve a of Figure 8 and $\tau(E)$ are obtained from the calculated curves published by Shur (9). It is found that the curve a can be represented analytically by:

$$v = 2.15 \times 10^7 + \left\{E - 3 \times 10^3\right\}^{0.63}$$

and the field dependent relaxation time is given by:

$$\tau = 4 \times 10^{-13} / \left\{E \times 10^{-4}\right\}^{1.2}$$

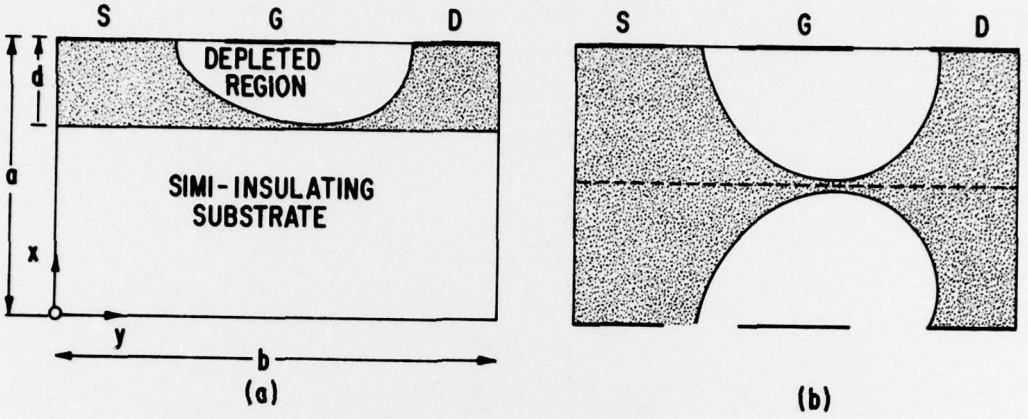

Figure 1 a) Conventional FET b) Double-sided FET

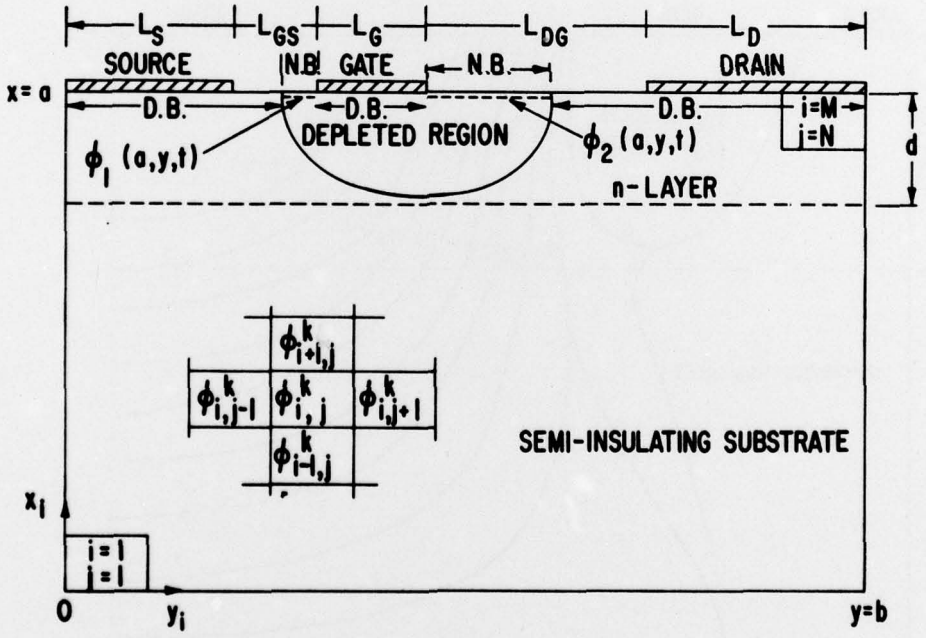

Figure 2

Schematic representation of the FET and assignments of axes and notations. DB = Dirichlet Boundary, NB = Newmann Boundary.

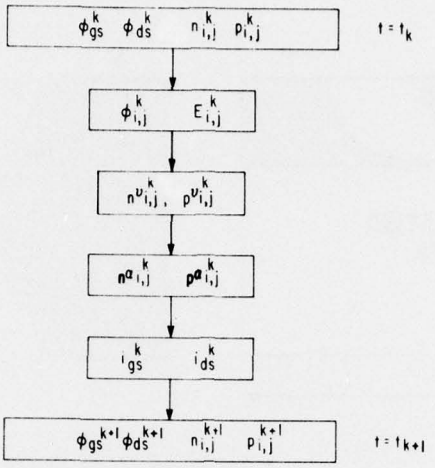

Figure 3 Computational sequence, explicit method. The Poisson solution takes place between the carrier and the potential boxes.

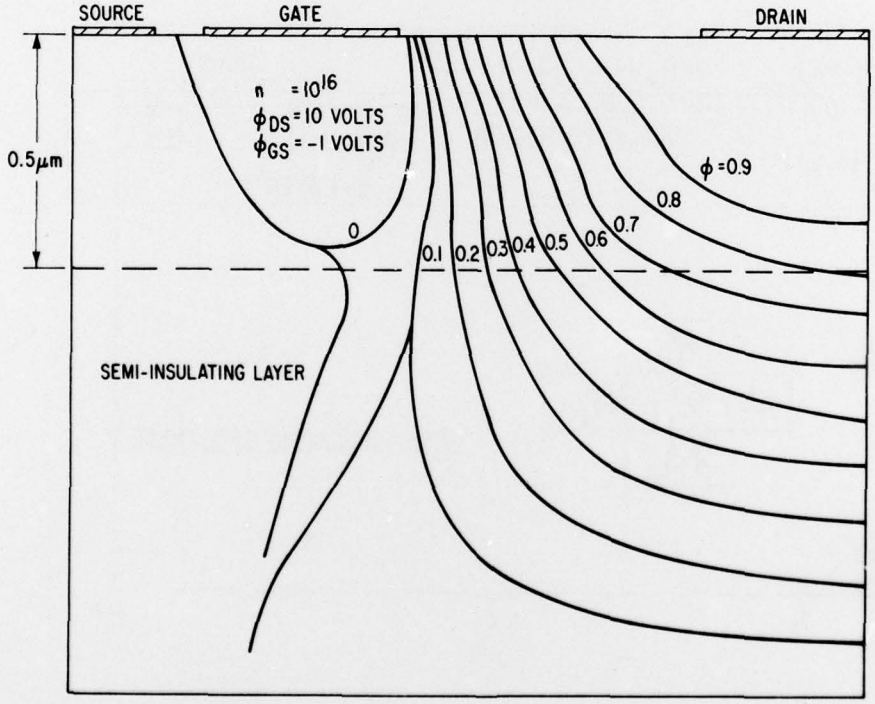

Figure 4 A dc potential distribution in a conventional FET.

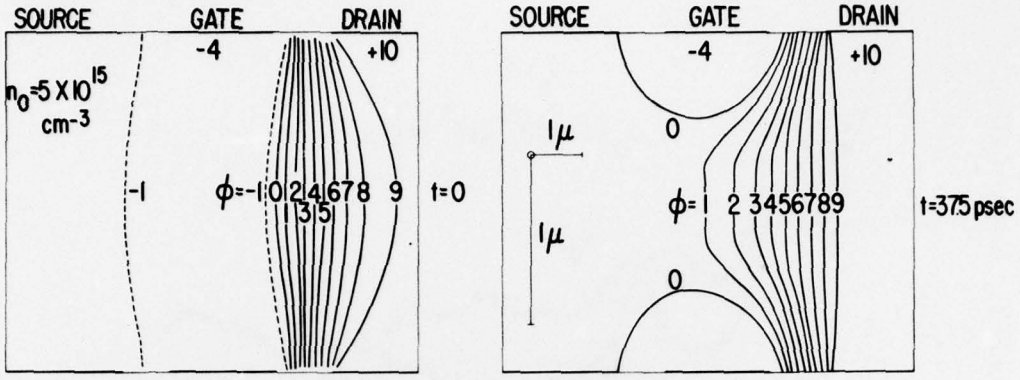

Figure 5 Snapshots of potential distribution at t = 0 and at t→ ∞ for a double-sided FET with the gate and drain voltages stiffly applied at t = 0

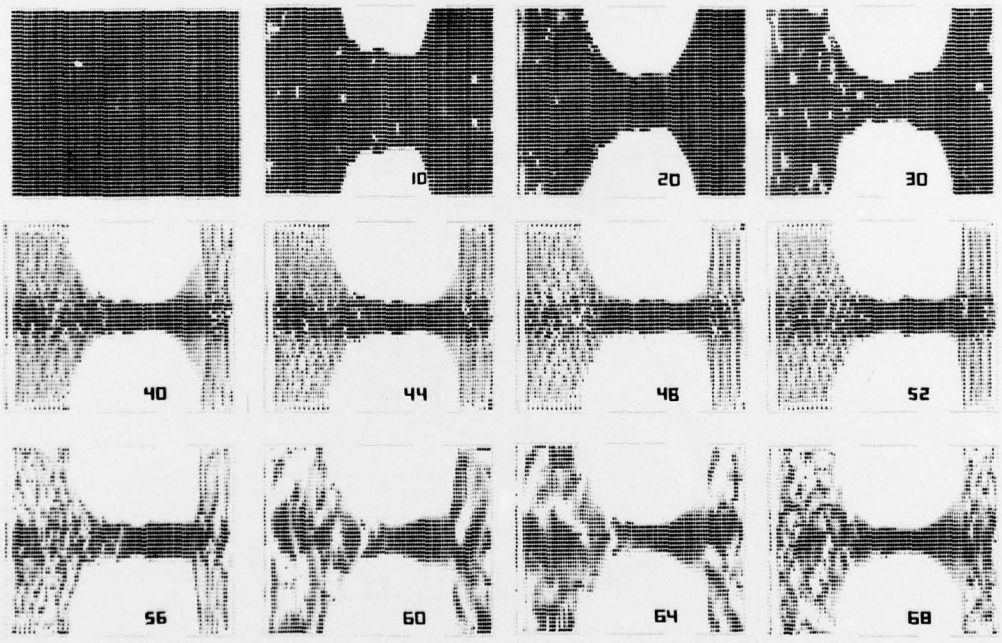

Figure 6 Time sequence (as indicated, in psec) snapshots of the electron density distribution in the same FET as in Figure 5. (The grey scale changes between the "30" and "40" frames). Note the Gunn oscillation, more evident as the shrinking and expanding channel width near the drain, as well as the traveling bulges in the channel. The gate voltage is -4 volts.

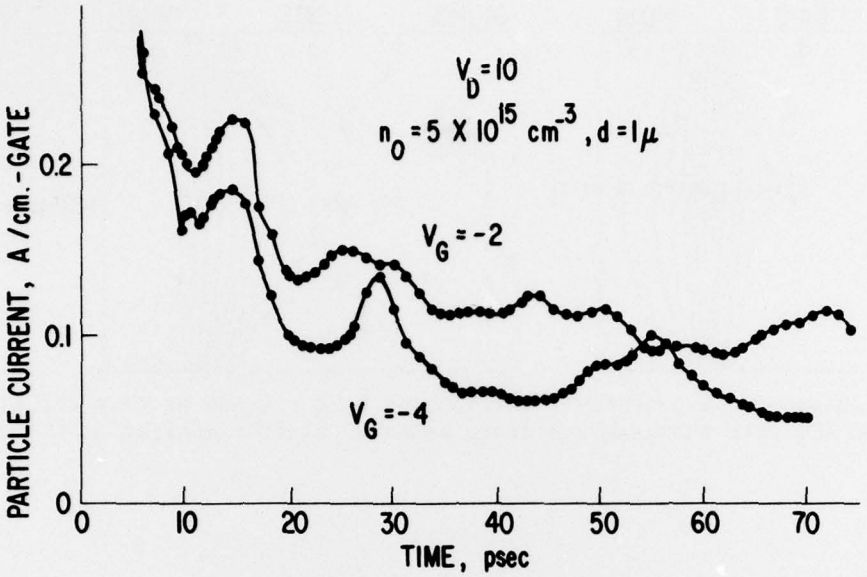

Figure 7 The drain current (passing through the vertical surface beyond the right edge of the gate electrode) as a function of time, for two values of gate voltages on the same FET as in Figures 5 and 6.

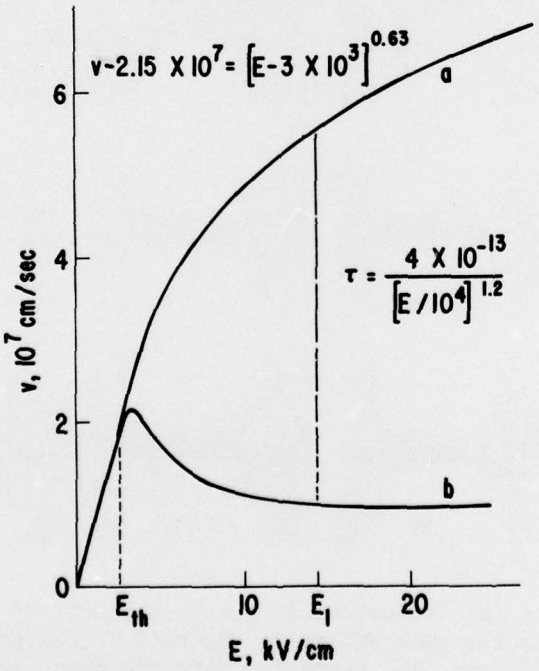

Figure 8 The light-mass velocity branch (curve a) and the equilibrium v(E) characteristic (curve b) of electron in GaAs. Curve a as well as the field dependent time constant of decay are deduced from the data published by Shur.

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