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DESIGN AND FABRICATION OF AUDIO AMPLIFIER UTILIZING MASTER-SLIC--ETC(U)
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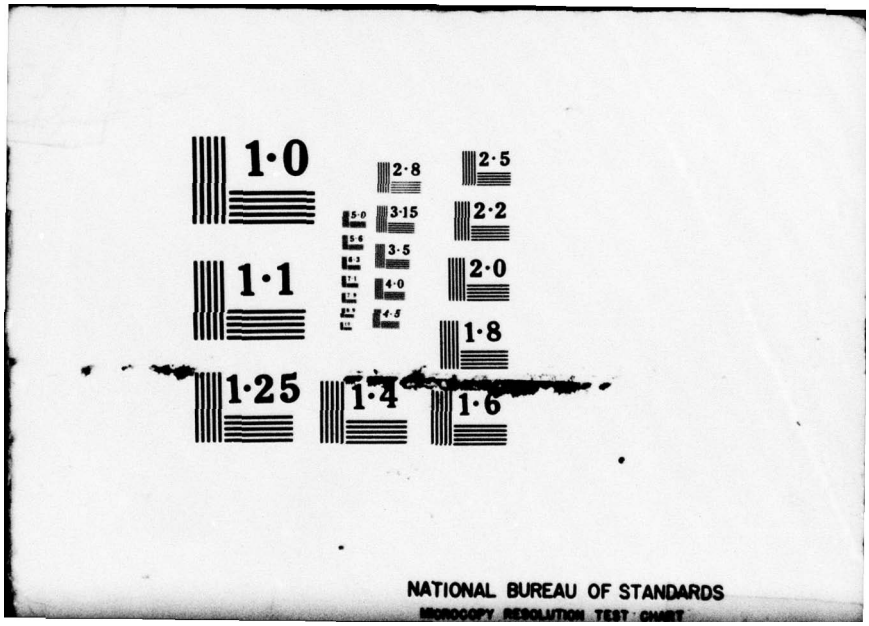
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DESIGN AND FABRICATION OF AUDIO AMPLIFIER UTILIZING MASTER-SLICE INTEGRATED CIRCUIT

July 1968

Prepared for

U. S. NAVY ELECTRONICS LABORATORY CENTER
San Diego, California

Under Purchase Order N00953-68-M-2988

Publication 456-01-1-896

ARINC RESEARCH CORPORATION

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER 456-01-1-896 ✓	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) DESIGN AND FABRICATION OF AUDIO AMPLIFIER UTILIZING MASTER-SLICE INTEGRATED CIRCUIT		5. TYPE OF REPORT & PERIOD COVERED
		6. PERFORMING ORG. REPORT NUMBER 456-01-1-896
7. AUTHOR(s) R.A. Mammano		8. CONTRACT OR GRANT NUMBER(s) N00953-68-M-2988 new
9. PERFORMING ORGANIZATION NAME AND ADDRESS ARINC Research Corporation ✓ 2551 Riva Road Annapolis, Maryland 21401		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS U.S. NAVY ELECTRONICS LABORATORY CENTER San Diego, California		12. REPORT DATE July 1968
		13. NUMBER OF PAGES 12
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) U.S. NAVY ELECTRONICS LABORATORY CENTER San Diego, California		15. SECURITY CLASS. (of this report) UNCLASSIFIED
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

UNCLASSIFIED/UNLIMITED

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

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UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

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(6) DESIGN AND FABRICATION OF AUDIO AMPLIFIER UTILIZING MASTER-SLICE INTEGRATED CIRCUIT

(11) Jul[redacted]68

(12) 15 p.

Prepared for

U. S. NAVY ELECTRONICS LABORATORY CENTER
San Diego, California

Under Purchase Order (15) N[redacted]953-68-M-2988

Prepared by

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(14) Publication 456-01-1-896

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CONTENTS

LIST OF ILLUSTRATIONS

1. INTRODUCTION

This report describes the design and fabrication of an audio output amplifier built with a Master-Slice integrated circuit. This work was performed by ARINC Research Corporation for the U. S. Navy Electronics Laboratory Center, San Diego, California, under Purchase Order N00953-68-M-2988.

The purpose of this program was the development of a general-purpose communication circuit that would demonstrate the utility of the Master Slice, and also serve as a means of familiarizing NELC personnel with assembly techniques associated with this technology.

For detailed information concerning the Master Slice IC, the reader should refer to ARINC Research Publications W7-425-TN001-1, April 1967; W7-426-TN001-1, August 1967; and W8-447-TN001-1, March 1968.

2. DESIGN GOALS

Design goals established for this audio amplifier circuit were as follows:

a. Operate with minimum distortion over the frequency band of 300 to 3000 hertz.

b. Utilize a specified miniature magnetic microphone.

c. Provide maximum power output consistent with component and packaging limitations.

d. Utilize a minimum number of components, particularly those that would have to be external to the Master Slice.

e. Use fabrication techniques compatible with the capability of the NELC Microelectronics Laboratory.

The above goals affected the design of the amplifier in two major ways. First, magnetic microphones are characteristically low-output devices, and the particular one specified for this application is no exception. To obtain useful power at the output requires approximately 60 db of voltage gain. Since this is too much for a single amplifier stage, a preamplifier also had to be provided.

A second major design decision concerned the requirement for maximum power output consistent with the Master Slice components. The original design goal for the Master Slice was to obtain maximum frequency response; but in so doing, two problems were encountered in applying the circuit to an audio application:

a. A high resistivity process was used to minimize parasitic capacity, but this resulted in higher saturation resistance, which limited the current capabilities of the power transistors to approximately 100 milliamps.

b. The high frequency response of the components gives the circuit a strong tendency to oscillate unless specific steps are taken to limit the bandwidth.

While the latter problem may be solved by the addition of an external capacitor for frequency stabilization, the loss in transistor efficiency at currents greater than 100 milliamperes requires a compromise between load resistance, supply voltage, and power handling capability. The result is that for an output power of 1/2 watt, the load resistance must be greater than 40 ohms and the supply voltage above 20 volts. Lower values of load resistance may be accommodated, but at reduced power levels.

3. CIRCUIT DESIGN

The schematic diagram for the resultant audio amplifier design is shown in Figure 1. This circuit consists of a preamplifier stage (Q1 and Q2), a differential voltage amplifier (Q3 and Q4), and the output current amplifier (Q5 to Q9).

The preamplifier is biased to provide a fixed gain of approximately 30 db from Q2. Q1 is a diode-connected transistor providing a stable bias point for Q2. Since Q1-Q2 and R2-R4 are closely matched, the current through both transistors is identical; and by making R3 less than R1, a linear operating point is established for Q2. Capacitor C1 is used for stability to limit the high frequency gain.

The differential voltage amplifier provides for another 30 db of gain and the voltage offset necessary to drive the push-pull output stages. The differential configuration gives both a stable operating point and a convenient means of inserting a variable amount of feedback for gain control.

Current amplification is provided by transistors Q5 through Q9, which operate as complementary emitter-followers. The use of a lateral PNP transistor for Q7 gives Q8 and Q9 the voltage characteristics of a PNP transistor with a current gain similar to the NPN combination of Q5 and Q6. The primary load current flows alternately through Q6 and Q9, with Q5 and Q8 providing additional current gain for low standby current and high operating efficiency.

High frequency stability for the output stage is provided by R12 and C5, which bypass the inductive component of the speaker voice coil. Capacitor C4, with a single battery supply, keeps direct current out of the speaker voice coil, but could be eliminated by the use of a balanced power supply.

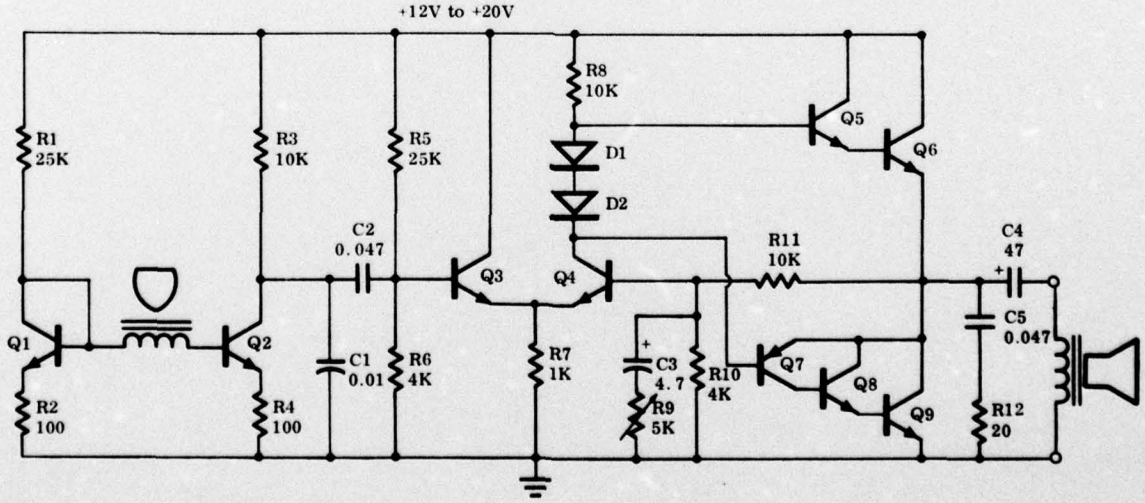


Figure 1. Complete Audio Amplifier Schematic

4. CIRCUIT FABRICATION

Because of the relative complexity of the circuit, it could not all be built on a single Master Slice chip. Two chips, however, will provide all the resistors, diodes, and transistors necessary to complete the amplifier, leaving only five capacitors and a volume control external to the circuit. Three of these five capacitors could be utilized in chip form for additional miniaturization.

The allocation of components to the Master Slice chips was as depicted in Figure 2. The preamplifier and lower half of the output stage are included in one chip, while the differential amplifier and the output-stage upper half are on the other. With this allocation, internal power dissipation is divided, providing approximately equal chip temperature. An additional advantage of this allocation is that there are only two direct interconnections between the chips. The other interconnections can be made at the package lead terminations.

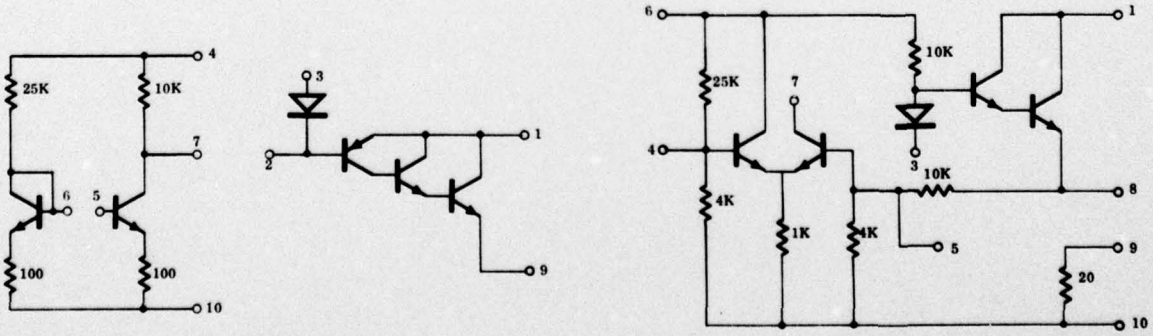
The component interconnections to be made on each Master Slice chip are shown in Figures 3 and 4. Figure 5 illustrates the total package wiring. These wires and jumpers are incorporated with a wire bonding machine in the following order:

a. The jumpers between adjacent pads are made with individual wire bonds, with the wire pulled away from the bond.

b. The interconnection wires on each individual chip are added, with the usual order being to start with the shorter lengths.

c. Interconnections between chips and from the chips to the package lead terminations are made last.

Photographs of a completed pair of Master Slice chips appear as Figure 6.



A. Preamplifier and Lower Power

B. Differential Amplifier and Upper Power

Figure 2. Allocation of Components to Master Slice Chips

Figure 3. Component Interconnections on Master Slice for Preamplifier and Lower Power Unit

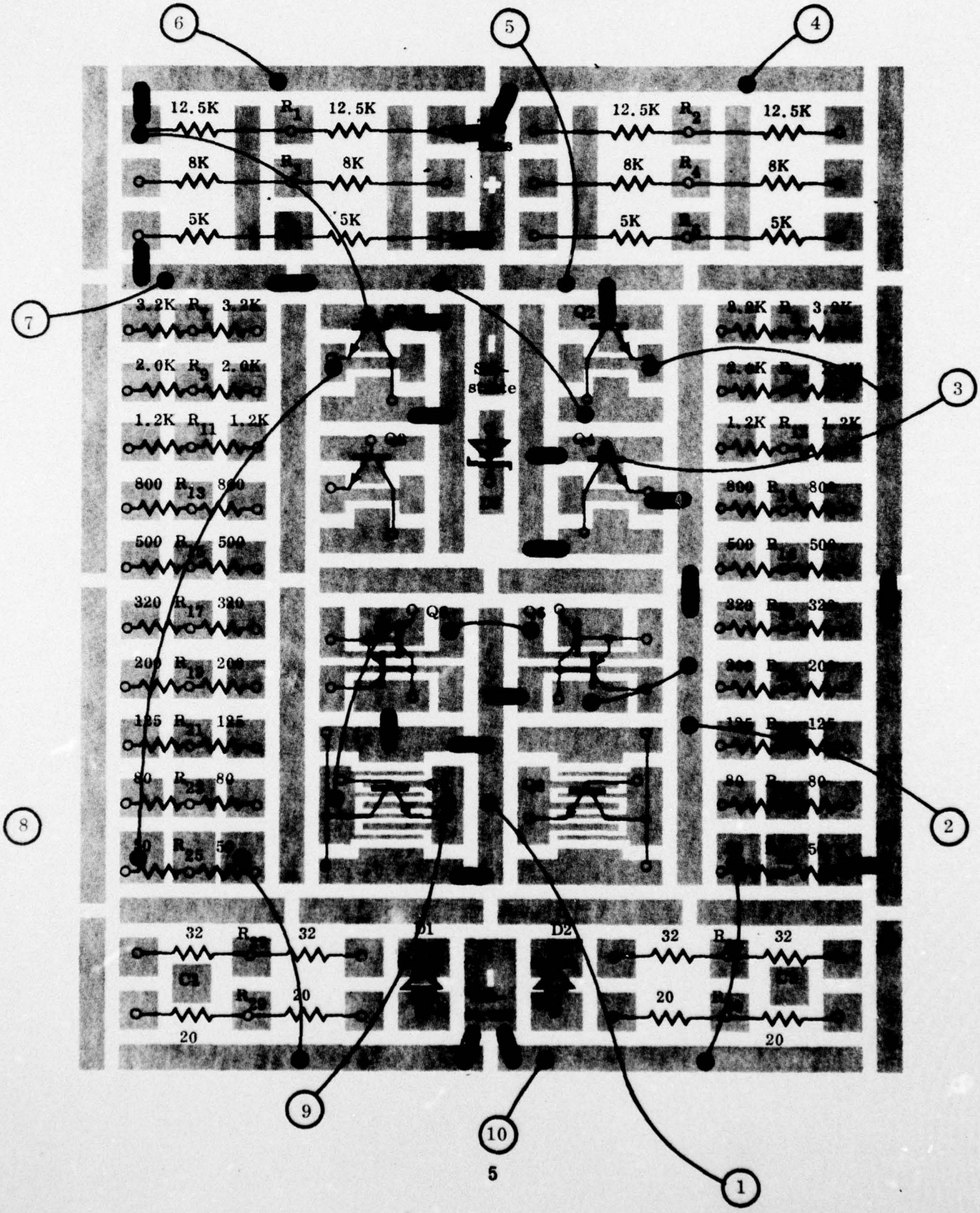
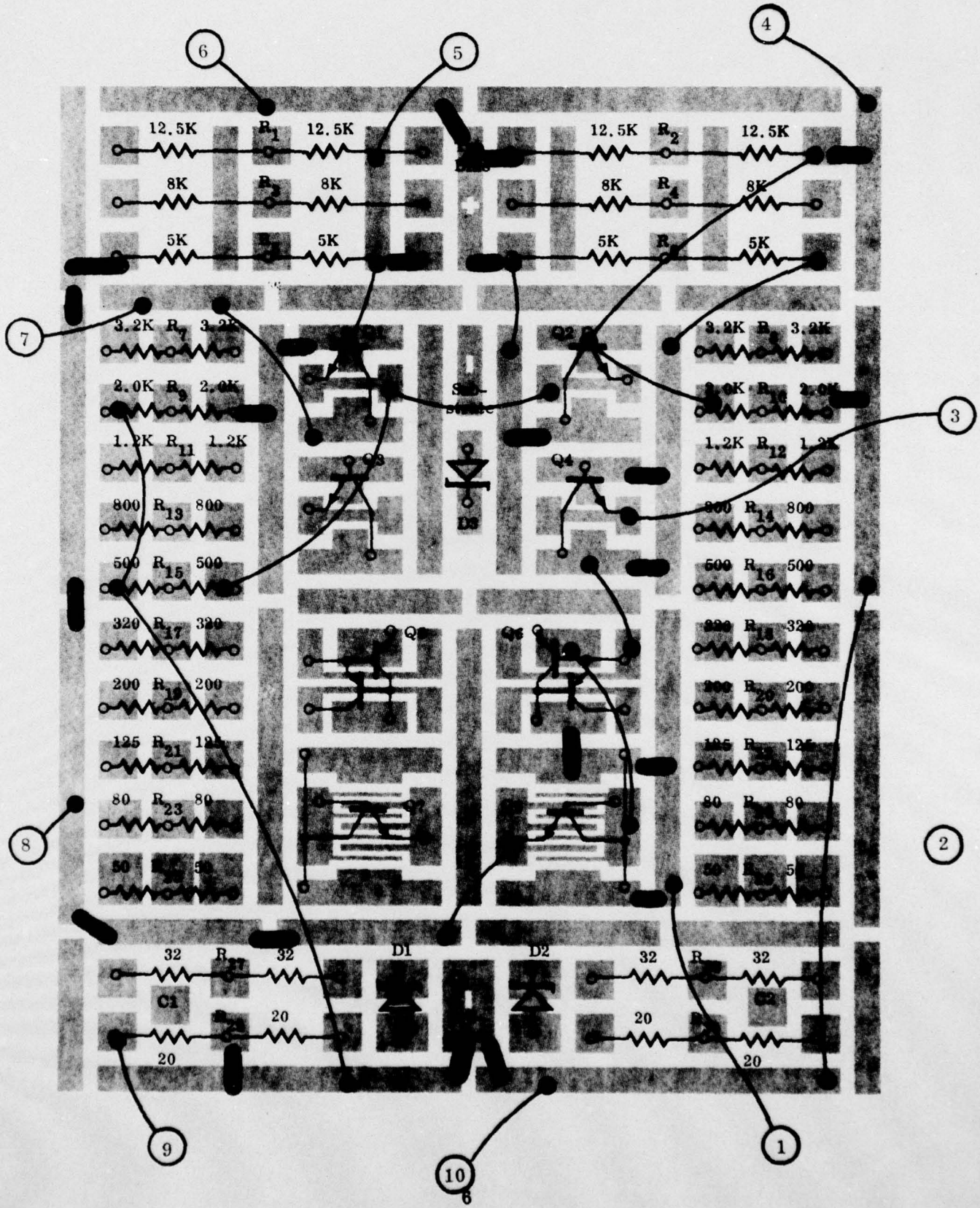


Figure 4. Component Interconnections on Master Slice for Differential Amplifier and Upper Power Unit



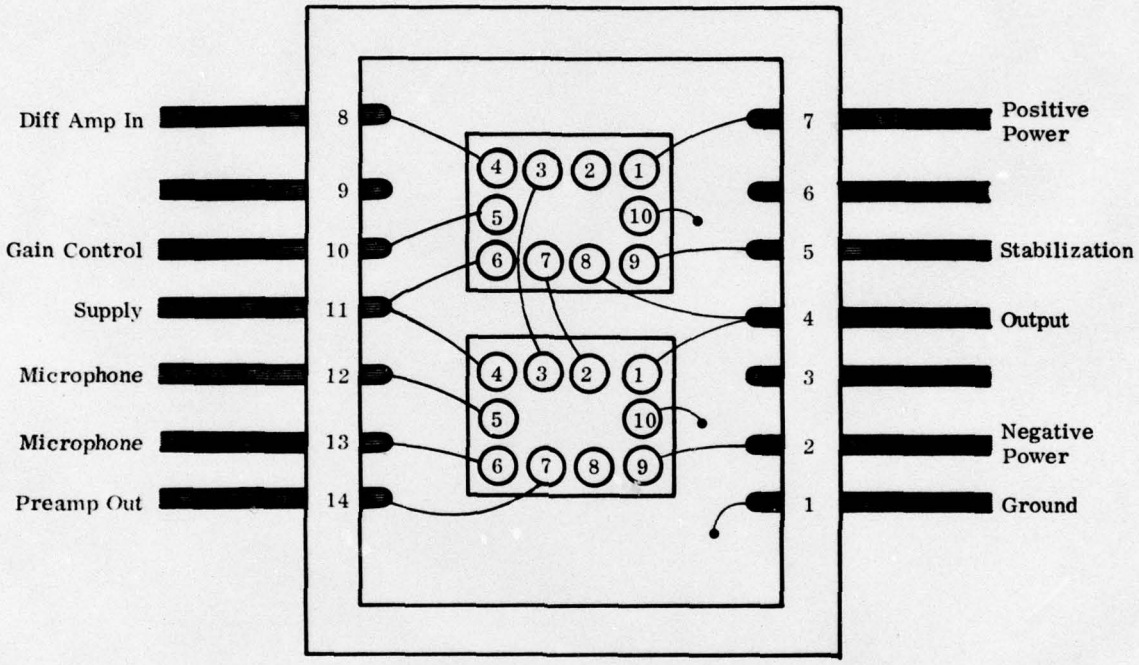
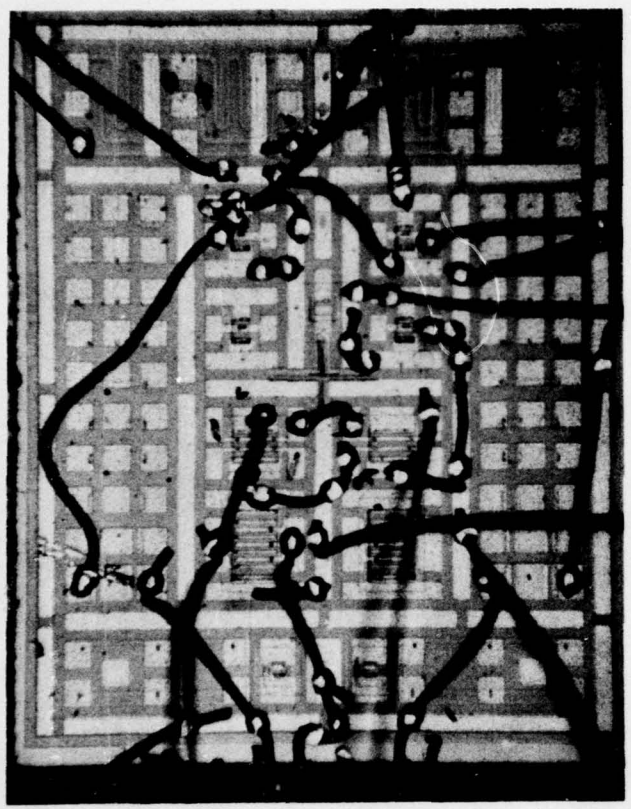
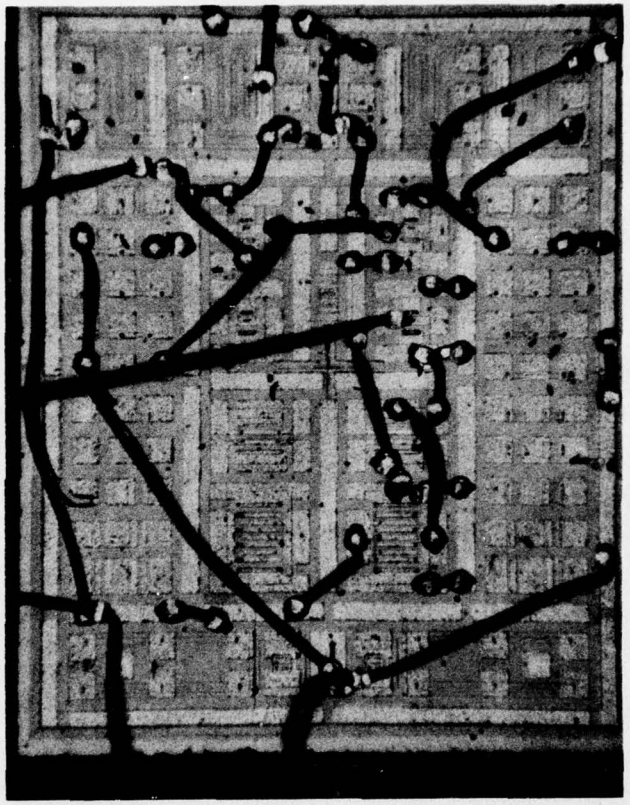


Figure 5. Package Wiring for 14-Pin Flat Pack



Preamplifier



Differential Amplifier

Figure 6. Photographs of a Completed Pair of Audio Amplifier Chips

5. CIRCUIT TESTING

The completed audio amplifier can be evaluated in the test circuit shown in Figure 7, with the following precautions:

a. The power supply should initially be current-limited to 20 milliamperes to prevent burning out a shorted device that may be repairable.

b. The power supply impedance should be low and the leads short. If the circuit still oscillates, it may be necessary to place a capacitor (1 to 10 microfarad) from pin 11 to pin 1.

c. As with any high-gain circuit, efforts should be taken to minimize stray capacity and inductance and to keep the input and output lines isolated.

To evaluate the performance of the amplifier, the procedure outlined below should be followed:

a. Insert the device into the test fixture with the power supply off, signal generator off, R_L disconnected, and R_C equal to 5000 ohms.

b. With the power supply current-limited to 20 milliamperes, turn the power on and increase the voltage to 20 volts. If the current is more than 10 milliamperes, the circuit is defective.

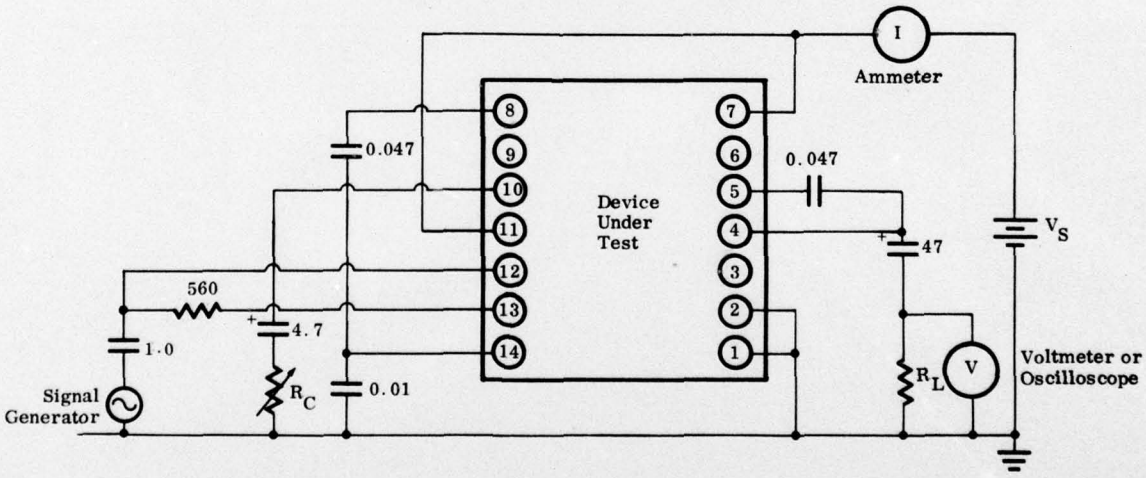


Figure 7. Audio Amplifier Test Circuit

c. Ensure that the circuit is not oscillating and then measure the dc voltage at the package pins. Approximate values (±20%) are listed below:

Pin	Volts	Pin	Volts
1	0	8	2.8
2	0	9	0
3	0	10	2.8
4	10	11	20.0
5	0	12	0.7
6	0	13	0.7
7	20	14	14.0

d. Connect the signal generator and set the frequency to 1000 hertz and amplitude to 5 millivolts rms. Check the output for low distortion. The amplitude of the output should be 350 ± 50 millivolts rms.

e. Reduce the value of R_C to 200 ohms. The output should still have low distortion, and the amplitude should now be 2.5 ± 0.5 volts rms.

f. Increase the value of power supply current-limiting to 200 milliamperes and connect a load resistor, R_L, of 16 ohms. Check to see that the circuit is still free of oscillations. The output will now have some crossover distortion. The amplitude should now be 0.7 ± 0.2 volts rms.

g. Check for constant output amplitude (±3 db) as input frequency is varied from 300 to 3000 hertz.

h. Set the frequency back to 1000 hertz and increase the amplitude to 50 millivolts rms. (NOTE: Do not leave the amplitude long at this level--excessive internal temperature rise will result.) The output should be evenly clipped top and bottom, with an amplitude of 8 ± 2 volts peak-to-peak. Reduce the input amplitude.

i. Turn off the power and remove the device from the test fixture.

6. CONCLUSIONS

While the audio amplifier circuit in this form has demonstrated the capability and versatility of the Master Slice integrated circuit, additional improvements in the circuit packaging and assembly procedures are still possible. As a first step, through utilization of a larger package with an interconnecting substrate pattern, four of the five capacitors may be included within the package. Three of these would be in chip form and the other would be a microminiature solid tantalum unit.

A second extension, and an extremely important step if more than a dozen or so circuits are to be fabricated, is the design of a special metallization mask to provide component interconnections at the wafer level. This will eliminate the major part of the labor, with a corresponding (and significant) reduction in circuit costs.

Following this approach, the Master Slice concept can provide: 1) a rapid means of verifying a tentative design, 2) relatively inexpensive prototype devices, and 3) early assurances that a production design will meet all requirements.