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During the first year of the program we assembled measurement apparatus and established a technique, based on drain current transients, in determining trap activation energies on GaAs FET's using a modification of deep level transient spectroscopy (DLTS).

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During the final year, we used transient capacitance DLTS techniques by utilizing special FET structures (fat FET's) and specially-doped test wafers. A hole trap (at 0.45 eV due to copper) was identified in p-GaAs and an electron trap at 0.34 eV in an n-GaAs IMPATT diode was detected. A technique was devised for identifying trap energy levels from a single DLTS temperature sweep. Surface traps, whose signature differs qualitatively from bulk trap signatures, were discovered in FET wafers. An FET structure which was grown and fabricated into recessed gate devices minimized the effect of traps, as was demonstrated by measuring pulsed and DC I-V characteristics.

FOREWORD

In light of the increasing importance of microwave semiconductor devices, Raytheon Company, Research Division has undertaken a study of electrical traps in microwave materials under the auspices of the Air Force Office of Scientific Research. This report concentrates on the progress achieved during the third and final year of the program.

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This report has been given an internal number of S-2333.

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1.0 INTRODUCTION

This final report on a three-year study of electrical traps in GaAs and their effects on microwave devices will concentrate on the experiments and analysis carried out during the final year of this project. Many of the important results of these earlier studies are discussed in interim reports,[1-2] including (1) the development of a novel deep level transient spectroscopy (DLTS) method based on current transients instead of capacitance transients, which had the advantage of being directly applicable to operating FET's,[2] (2) the development of an important new method for increasing mobility in FET's and other thin semiconductor films, and (3) the measurement of the transient changes from the DC I-V characteristics of FET's caused by pulsing the gate or the drain voltages.[1-2]

1.1 Electron and Hole Traps in IMPATT Diodes and FET's

The importance of trapping centers in semiconductor materials has been recognized for many years,[5-6] but the developing art of growing high-quality VPE GaAs with controlled doping levels for IMPATT diodes and FET's has made it more important than ever to understand the role of electron and hole traps. By determining the energy levels of the important traps, the chemical impurities which caused them can be identified, which is an aid in modifying the growth techniques in order to reduce the density of impurities and lattice defects in GaAs. The physical location of these traps gave information which was useful in devising structures for semiconductor devices which would minimize their effects upon performance. For FET's, structures can be fabricated which isolate traps from the substrate by means of buffer layers and isolate traps on the surface by means of a recessed gate.

Because of the evident importance of traps and surface charge to the operation of FET's, our effort was concentrated upon these devices. However, experiments were also carried out to measure trap densities near the doping spike of a Read IMPATT diode and to measure hole traps in p-GaAs.

At the present time the characterizations of p-GaAs have a particular importance because of the emerging technology for double-drift IMPATT diodes in GaAs.

The occurrence of traps in FET's causes the parameters of these devices to become time and bias dependent, and also to become light-sensitive. Fluctuations in the trap occupancy causes corresponding fluctuations in the source-gate capacitance. Although the traps investigated during this contract have fluctuations with Fourier components concentrated in the 10-to-100 kHz range, the resulting noise in the active component of an oscillator circuit is likely to be upconverted to produce FM noise in the microwave range.

1.2 Summary of Research Findings

In the earlier phase of this contract, a novel DLTS technique using current transients was used to detect traps and measure their energy levels directly upon FET's. However, the complex interactions in the three-terminal device made it difficult to interpret these measurements. Therefore, a DLTS system, similar to Lang's system,[7] was constructed for pulsed capacitance measurements. The basis of Lang's methods is derived in Sec. 2, and our equipment is described and a circuit diagram shown. Two new formulas which provide a convenient approximation for adapting the basic technique to semiconductors with nonuniform doping are also derived.

The equipment was first applied to Schottky barrier and n^+pp^+ diodes. Although the standard Lang technique requires at least two temperature sweeps to calculate the trap cross section and energy level, a calculation is described in Sec. 3 which determines these parameters and generates a number of secondary data points from a single curve, provided the base line of the DLTS curve can be determined. In our measurements we were attempting to detect the traps which existed in the best device-grade GaAs without intentionally introducing extraneous impurites, so that we were usually attempting to measure low trap densities. In a Read IMPATT diode, a trap density of 7×10^{12} cm^{-3} was detected in the drift region close to the Read spike.

The energy level of this trap was 0.34 eV below the conduction band, which was close to values for a previously measured trap level.[8] We were among the first experimenters to take measurements in p-GaAs, and, in the n^+pp^+ diode, we detected a trap 0.45 eV above that valence band which had been detected earlier as a minority carrier trap in n-material[9,10] and attributed to a copper impurity.

Applying Lang's method to GaAs grown on semi-insulating substrates required growing special low-doped test wafers and the fabrication of fat FET's. An electron trap 0.85 eV below the conduction band was detected which coincides with a previously detected trap attributed to oxygen contamination.[8] In addition, an anomalous signal was detected which was qualitatively different from previously detected signals from bulk traps. In addition to characteristics described further in Sec. 4, the new signature was distinguished from bulk traps because it not only produced peaks which had the opposite sign from the bulk trap signatures, but it also gave a strong signal for a "reverse" pulse under conditions in which bulk traps produce no response to such a pulse. This signature appears to be caused by surface states at the interface between the GaAs and the metallic gate.

Measurements were also made on normal FET wafers with active layer doping on the order of 1×10^{17} cm^{-3}, as described in Sec. 5. A theoretical model of the surface states is put forward in Sec. 6. As a by-product of this model, some quantitative calculations are given to illustrate Cowley and Sze's model[11,12] which describes the Fermi level pinning at a Schottky barrier. These calculations determine a built-in potential which does not vary significantly from 0.85 V for different metals and for different reverse biases, so that they are consistent with experimental measurements.

Section 7 gives detailed description of a growth method and a fabrication technique for producing FET's with a minimum effect due to traps. These FET's are distinguished by a buffer layer which prevents impurities such as chromium from diffusing into the thin active layer and to the surface. These FET's are fabricated with a recessed gate which keeps the surface

area between gate and drain, which may have surface states and an associated depletion layer, remote from the conducting channel.

In Sec. 8, I-V measurements on FET's are described which are taken both in a steady state and immediately after pulsing the gate or the drain. For an unbuffered device, there is a large difference between the pulsed drain curves and the DC curves. A computer model of a FET with transients due to bulk traps is described along with results that show that the measured effects are too large to be explained by bulk traps and are therefore undoubtedly due to surface states. These transient changes are found to be greatly reduced on devices grown with a buffer layer and almost completely eliminated when an n^+ contact layer is present beneath the gate and drain. A consistent study of the noise characteristics of these devices and their relationship to the bulk and surface traps described in this report would produce information which might lead to even further improvement of these low-noise devices.

2.0 DETECTION OF TRAPS BY THE PULSED CAPACITANCE METHOD

In this section, we describe the pulsed capacitance method derived by Lang and the behavior of traps in the semiconductor material. One of the objectives will be to introduce some conventions and nomenclature which are needed in this report. For completeness we will repeat some of the arguments given elsewhere, and in particular in Lang's original paper. We will discuss our experimental setup, and give a few formulas and interpretations which have not previously been published. In particular, we will derive approximate formulas for trap density which prove useful for semiconductors with large changes in doping level, such as occur in buffered FET's.

2.1 Review of the DLTS Technique

The basic experimental procedure is to pulse a Schottky barrier or p-n junction to a voltage V_p for a time T_p, where T_p is generally long enough for any trap transients to settle down. Next, the bias is suddenly changed to V_B and the capacitance is measured after times t_1 and t_2. Our experiments have always used reverse biases, so that we will use the convention that reverse bias V_p and V_B are considered positive.

After the voltage is suddenly changed to V_B, the capacitance can be written as

$$C(t) = C_B - \Delta C\, f(t) \quad , \tag{1}$$

where $f(t) = 1$ for $t = 0$ and $f(t) \to 0$ as $t \to \infty$. In fact, $f(t)$ can almost always be taken as

$$f(t) = e^{-t/\tau} \quad , \tag{2}$$

where the trap decay time τ is a function of temperature.

The DLTS technique measures the sampled values of $C(t_2) - C(t_1)$ (the negative of Lang's convention) where boxcar integrators are used to

obtain averaged values over many pulses while the temperature is slowly swept from about 90°K to 475°K. In this range the temperature limits are close to the boiling point of N_2 and the melting point of the diode solder.

For bulk traps, ΔC is positive and we use what Lang calls a majority carrier pulse with $V_p < V_B$, which we shall call a set pulse. When $V_B < V_p$, we refer to the pulse as a reverse pulse. No response is observed from a bulk trap after a reverse pulse, although during this contract, we have also detected surface traps which respond to reverse pulses and have a negative ΔC.

The behavior of the signature $C(t_2) - C(t_1)$ can be understood from the diagram in Fig. 1. At low temperature τ is large and the capacitance does not have time to change in time t_2, so the signal is weak. However, at high temperatures, the transient is over before time t_1. Thus, the maximum response will come at a temperature where τ is between t_1 and t_2.

To make this specific, assume f(t) is exponential as in Eq. (2), so that

$$C(t_2) - C(t_1) = S(t_1, t_2 \tau) \Delta C \quad , \tag{3}$$

where

$$S = e^{-t_1/\tau} - e^{-t_2/\tau} \quad . \tag{4}$$

It is convenient to run experiments with $x = t_2/t_1$ fixed for a series of measurements. At the temperature T_{max} where the signature is maximum

$$\tau_m = \tau (T_{max}) = (x-1)\, t_1/\ell n\, x \quad , \tag{5}$$

so that each temperature gives one data pair (τ_{max}, T_{max}) and

$$\Delta C = [\, C(t_2) - C(t_1) \,]_{max} / S_{max} \quad , \tag{6}$$

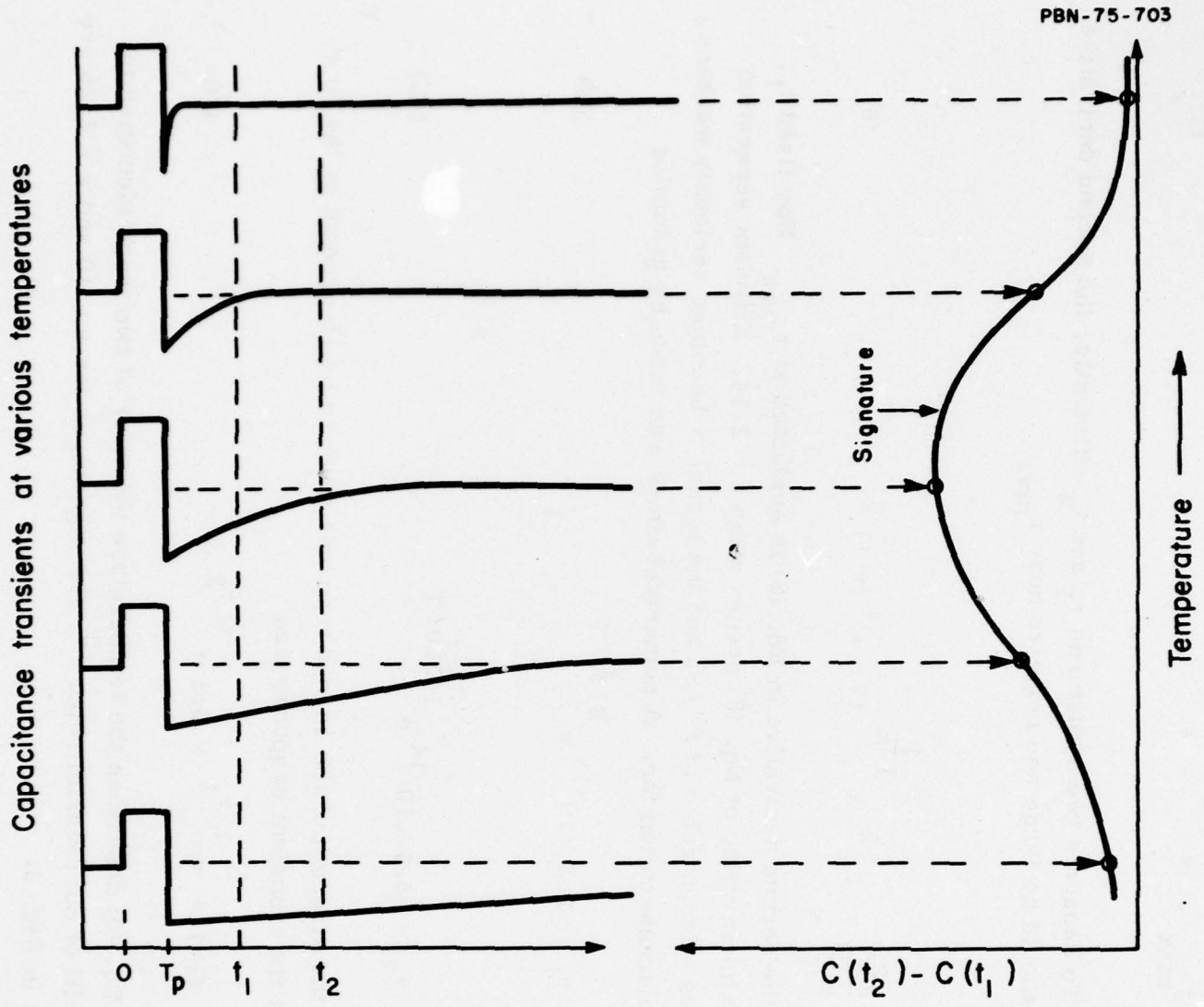

Figure 1 Schematic Diagram of the DLTS Signature $C(t_2) - C(t_1)$ from a Typical Bulk Trap.

where

$$S_{max} = x^{\frac{1}{1-x}} - x^{\frac{x}{1-x}} , \qquad (7)$$

To separate two signatures τ_1 and τ_2 efficiently, the second derivative of $S(\tau)$ should be large and negative near τ_{max}.

Now

$$\frac{\partial^2 S}{\partial \tau^2} = t_1^{-2} \; x^{\frac{1}{1-x}} \; (\ell n \; x)^4 \; (x-1)^{-3} , \qquad (8)$$

where the second derivative in Eq. (8) is evaluated at τ_{max}. For fixed t_1, the maximum value of Eq. (8) occurs when $x = 2.14$. Efficient separation requires a large value of S''/S, but the signal S becomes seriously weakened if x is decreased too far. A numerical check was made by assuming

$$\tau_1 = 2.3 \times 10^{-13} \; e^{8250/T} , \qquad (9a)$$

and

$$\tau_2 = 5.7 \times 10^{-14} \; e^{10320/T} , \qquad (9b)$$

while the strength of the second trap was taken to be 10 percent of the first, so that the transient response was

$$G(t) = e^{-t/\tau_1} + 0.1 \; e^{-t/\tau_2} . \qquad (10)$$

Here Eq. (9) describes the temperature behavior of two traps identified in Table III of our interim report.[2] The signatures for $x = 10$ and $x = 2.25$ are shown in Fig. 2.

For $x = 10$, the peak response for trap 2 should occur at the location of the arrow at $T = 414°K$, but it is completely swamped by the signal from

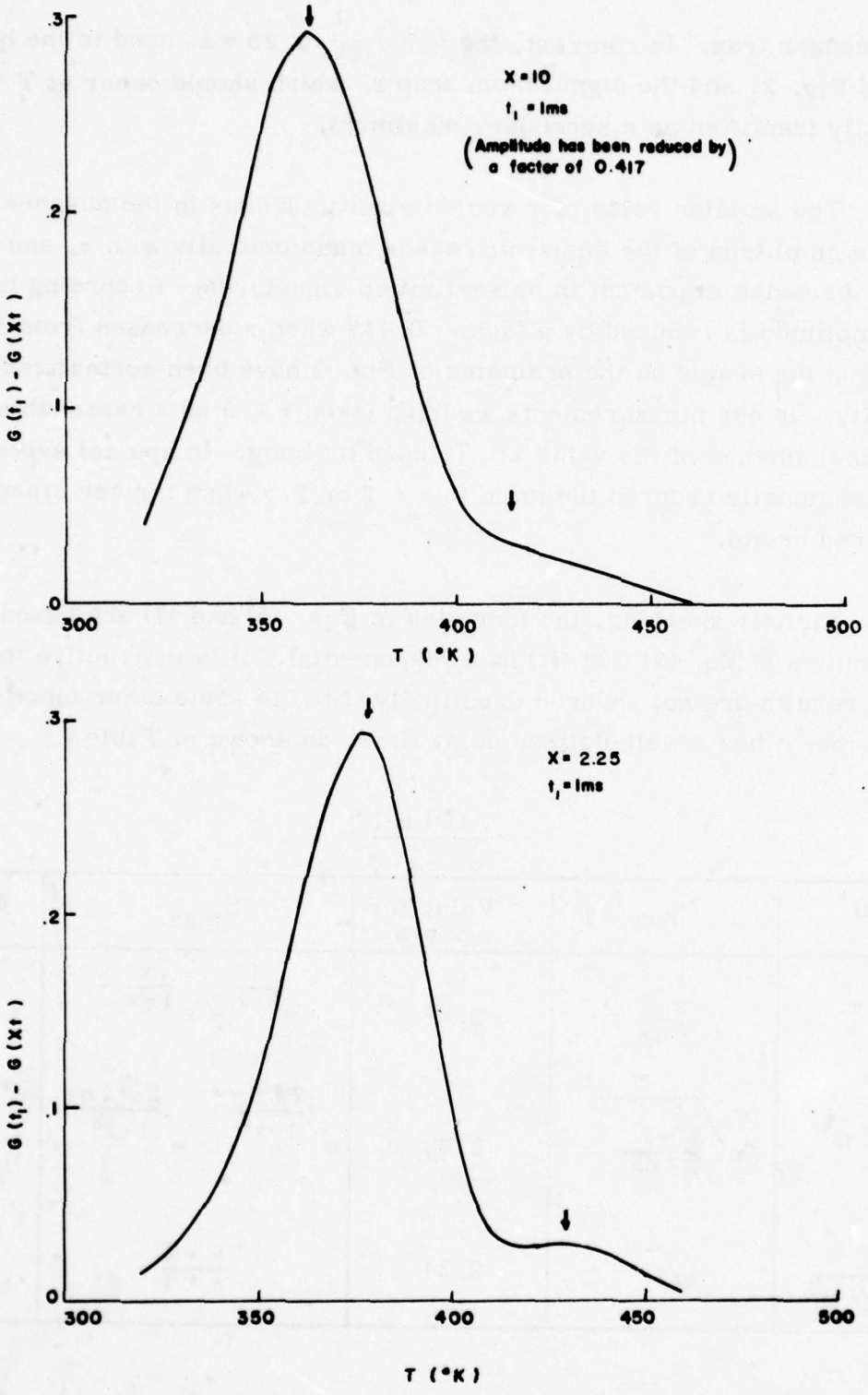

Figure 2 DLTS Response versus Temperature for τ_1 and τ_2 using different Values for x.

the stronger trap. In contrast, the value x = 2.25 was used in the bottom half of Fig. 2, and the signal from trap 2, which should occur at T = 430°K, is easily identified as a secondary maximum.

The smaller value of x would be advantageous in the absence of noise, but the amplitude of the signal increases monotomically with x, and this factor becomes important in noise-limited signatures. According to Eq. (7), the amplitude is reduced by a factor 0.417 when x decreases from 10 to 2.25 and the scales on the ordinates of Fig. 2 have been normalized to this quantity. In our measurements we have taken x = 5 as a reasonable compromise, instead of the value x = 10 used by Lang. In special experiments we occasionally reduced the ratio to x = 2 or 2.5 when further discrimination appeared useful.

Strictly speaking, the formulas in Eqs. (5) and (7) are based on the assumption of Eq. (2) that f(t) is an exponential. It is instructive to see that these results are not changed drastically if f(t) is some other function, provided that it has a well-defined delay time, as shown in Table I.

TABLE I

f(t)	τ_{max} / t_1	Value for x = 5	S_{max}	Value for x = 5
$e^{-t/\tau}$	$\frac{x-1}{\ell n x}$	2.49	$x^{\frac{1}{1-x}} - x^{\frac{x}{1-x}}$	.535
$e^{-(t/\tau)^2}$	$\sqrt{\frac{x^2-1}{2\ell n x}}$	2.73	$e^{\frac{2\ell n x}{1-x^2}} - e^{\frac{2x^2 \ell n x}{1-x^2}}$	.839
$\frac{1}{1+(t/\tau)^2}$	$\sqrt{x}$	2.24	$\frac{x-1}{x+1}$	.667

2.2 Transients in Trap Occupancy

If f is the fraction of deep-level states which are occupied

$$\frac{\partial f}{\partial \tau} = c_n n + e_p - (e_n + e_p + n c_n + p c_p) f \quad , \tag{11}$$

where e_n and e_p are the emission rates for holes and electrons, n is the free electron density and c_n, the electron capture rate, equals $v_{th}\,\sigma_n$, where σ_n is the cross-section and v_{th} is the thermal velocity, proportional to $T^{1/2}$. Electron traps are defined as traps for which $e_n \gg e_p$ and $c_n \gg c_p$, and, in the derivations of Sec. 2, we will assume that these relationships hold and also that the GaAs is an n-semiconductor so that the electron traps are majority carrier traps. The analysis of hole traps in p-material is completely analogous.

In equilibrium, the detailed balance condition requires the rate at which electrons are captured from the conduction band to equal the rate at which trapped electrons are emitted, i.e., $n_o c_n (1-f) = f_o e_n$ must hold, where $n_o = n_c \exp((E_f - E_c)/kT)$ and $f_o = (1 + g \exp((E_t - E_f)/kT)^{-1}$ are equilibrium values, and n_c is the effective density of states in the conduction band. It follows that

$$e_n = v_n \sigma N_c g \exp((E_t - E_c)/kT) \quad . \tag{12}$$

Since σ may have the form $\sigma_\infty \exp(-E_A/kT)$, i.e., the cross-section may have an activation energy, and since $E_t - E_c$ is found experimentally to be a linear function of temperature, these are some subtleties in this formula. Nevertheless, as shown in Ref. 8, e_n can be written as

$$e_n = \gamma_n \sigma_{na} T^2 \exp - (E_{na}/kT) \quad , \tag{13}$$

where σ_{na} and E_{na}, respectively, are an effective cross section and an effective "energy" below the conduction band. These parameters identify a particular trap level by its transient behavior, and in this report we will

understand cross section and energy below the conduction band in this sense. In Eq. (13), γ_n is a constant equal to 2.28×10^{20} cm^{-2} sec^{-1} $°K^{-2}$ for GaAs. A similar equation holds for hole traps where E_{pa} is an energy above the valence band and the constant is $\gamma_p = 1.7 \times 10^{21}$ cm^{-2} s^{-1} $°K^{-2}$.

In the depletion layer where n is small, the solution of Eq. (11) is

$$f = e^{-t/\tau} \quad , \tag{14}$$

where the trap is assumed full, i.e., f = 1, at t = 0 and

$$\tau \cong e_n^{-1} = A\,(300/T^2)\exp(E_{na}/kT) \quad , \tag{15}$$

where $A = 4.9 \times 10^{-26}/\sigma_{na}$.

The behavior of a Schottky diode during a DLTS pulse can now be seen schematically in Fig. 3. During the set pulse, the electrons are pulled into the boundary of the depletion layer and the traps are filled beyond the point $x = x_p - \lambda$, where λ is the small distance from the edge of the depletion layer to the point where the trap energy crosses the Fermi level. After the time t_p, the depletion layer jumps out to x(t), which is beyond the steady-state position x_B because traps between $x_p - \lambda_p$ and $x_B - \lambda_B$ remain filled for a time with an occupancy factor satisfying Eq. (14) and therefore the measured capacitance satisfies Eq. (1), under the assumption that the trap density N_T is small compared to the doping density N_D.

We are now in a position to check if the time behavior of the transient capacitance is consistent with the exponential decay of Eq. (14) with the decay time given by Eq. (15). Figure 4 shows an experimental curve taken on an n^+pp^+ diode, which will be discussed further in the next section. From four DLTS temperature sweeps, we obtained a least-squares fit to Eq. (15) with $A = 3.24 \times 10^{-14}$ and $E_{na} = 0.52$ eV. The straight line was drawn at the apparent baseline, and the height to the maximum value for signature, at T = 294 °K, was measured as Z. The rest of the curve was

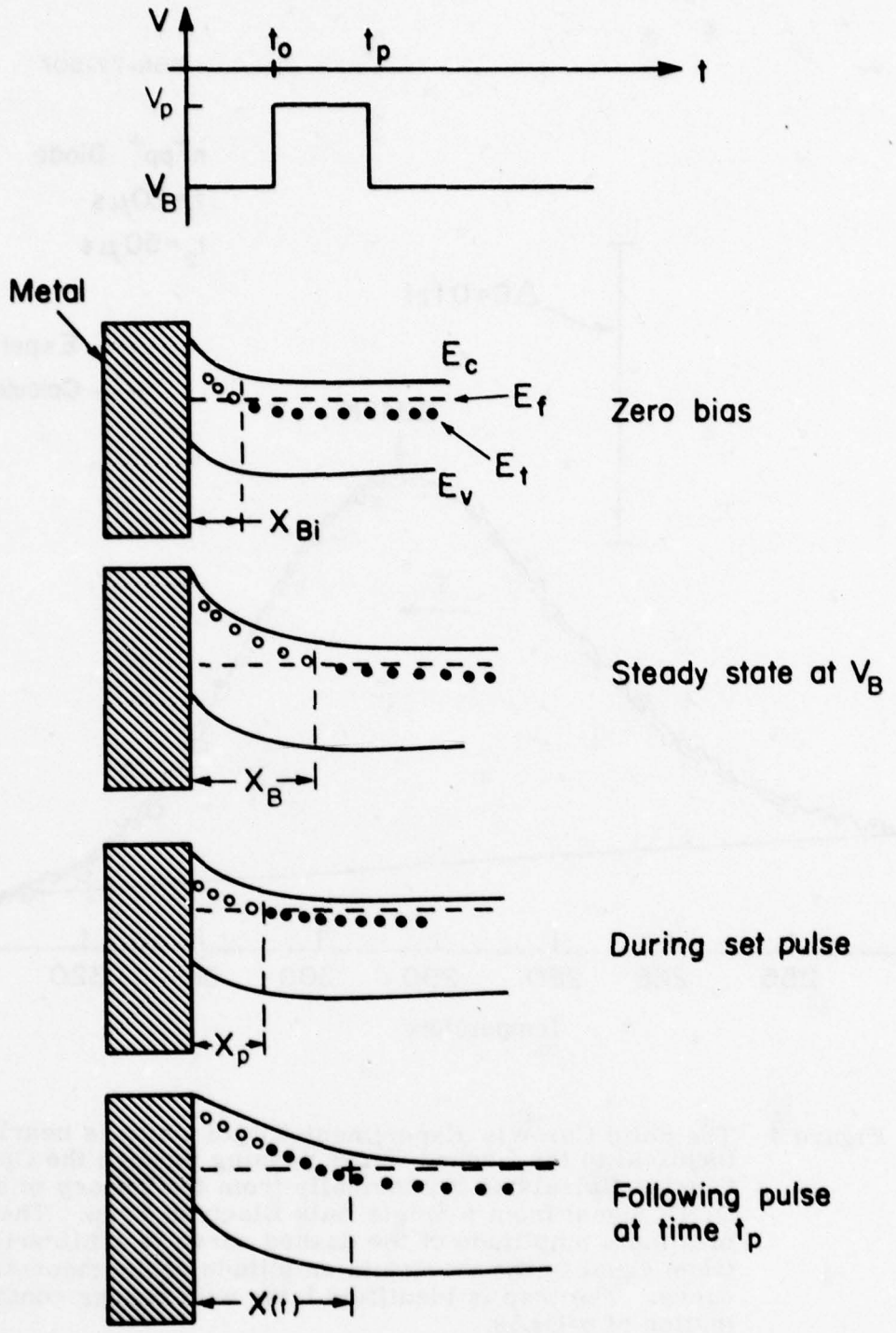

Figure 3 Schematic Diagram of the Movement of the Depletion Layer and the Trap Occupancy during a DLTS "Set" Pulse.

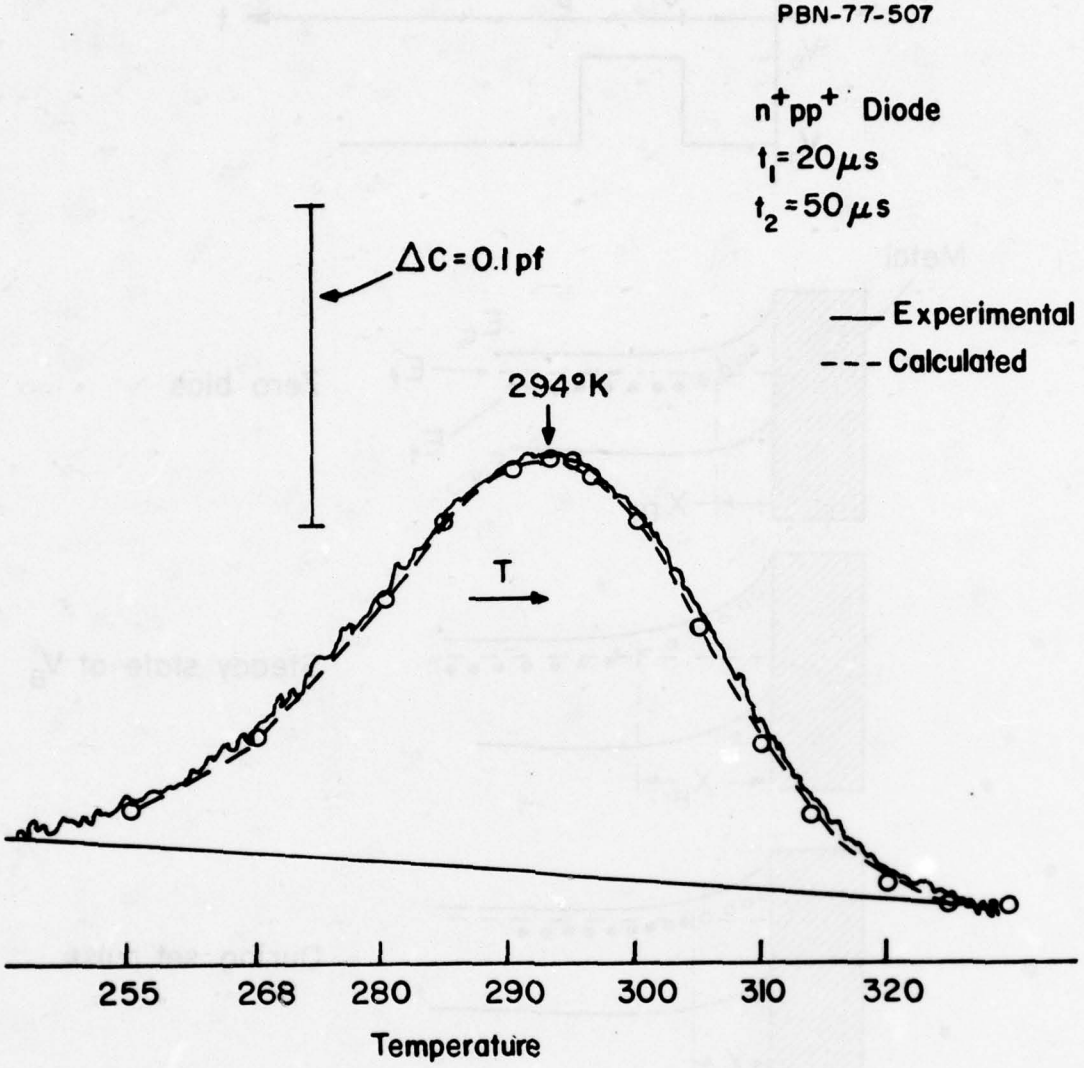

Figure 4 The Solid Curve is Experimental Data which is nearly Identical to the Dashed Curve passing through the Open Circles Calculated Numerically from the Theory of a DLTS Signal from a Single Bulk Electron Trap. The maximum amplitude of the dashed curve is arbitrarily taken equal to the maximum amplitude of the theoretical curve. The trap is identified later with copper contamination of p-GaAs.

now calculated as $Z\, S(t_1, t_2, T)/ S_{max}$ and indicated by the open circles the figure, where $S_{max} = 0.326$ is found from Eq. (7) with $x = 2.5$, and S is determined from Eqs. (4) and (15) using the values for A and E_{na}, and the experimental times $t_1 = 20$ and $t_2 = 50$. The dashed curve connecting the open circles agrees closely with the experimental curve, which gives a direct verification of the correctness of the theoretical assumption leading to Eqs. (13) and (1), at least for this particular trap.

A distribution of trap states which are uniformly distributed over a range of energy ΔE is of considerable interest because such a distribution of surface states has sometimes been suggested as a source of $1/f$ noise. The DLTS spectra in Fig. 5 were calculated with the aid of a computer program under the assumption that a uniform distribution of trap states centered at 0.58 eV existed. The decay periods, as a function of energy level, were taken as $\tau = 5.49 \times 10^{-13} (300/T)^2 \exp E/kT$ so that the response was given by

$$G = \frac{1}{\Delta E} \int_{0.58-1/2\,\Delta E}^{0.58+1/2\,\Delta E} S(t_1, t_2, \tau(E))\, dE \quad .$$

As shown in Fig. 5, the maximum amplitude for $\Delta E = 0.17$ eV is less than one-half of the maximum response for a single trap state. The signatures are much broader with a distribution of states than with a single state, but the maxima are at almost the same temperature as for a single state. When the range of ΔE is extended to 0.52 eV, the signature is flat over a large range of temperatures with no distinguished maxima, as shown by the bottom curve in Fig. 5, and the amplitude is essentially the same for $t_1 = 10\,\mu$sec and for $t_1 = 80\,\mu$sec.

2.3 Profiles of the Trap Density

Many wafers that we have investigated are nonuniformly doped with buffer regions with doping orders of magnitude below the active layer. The

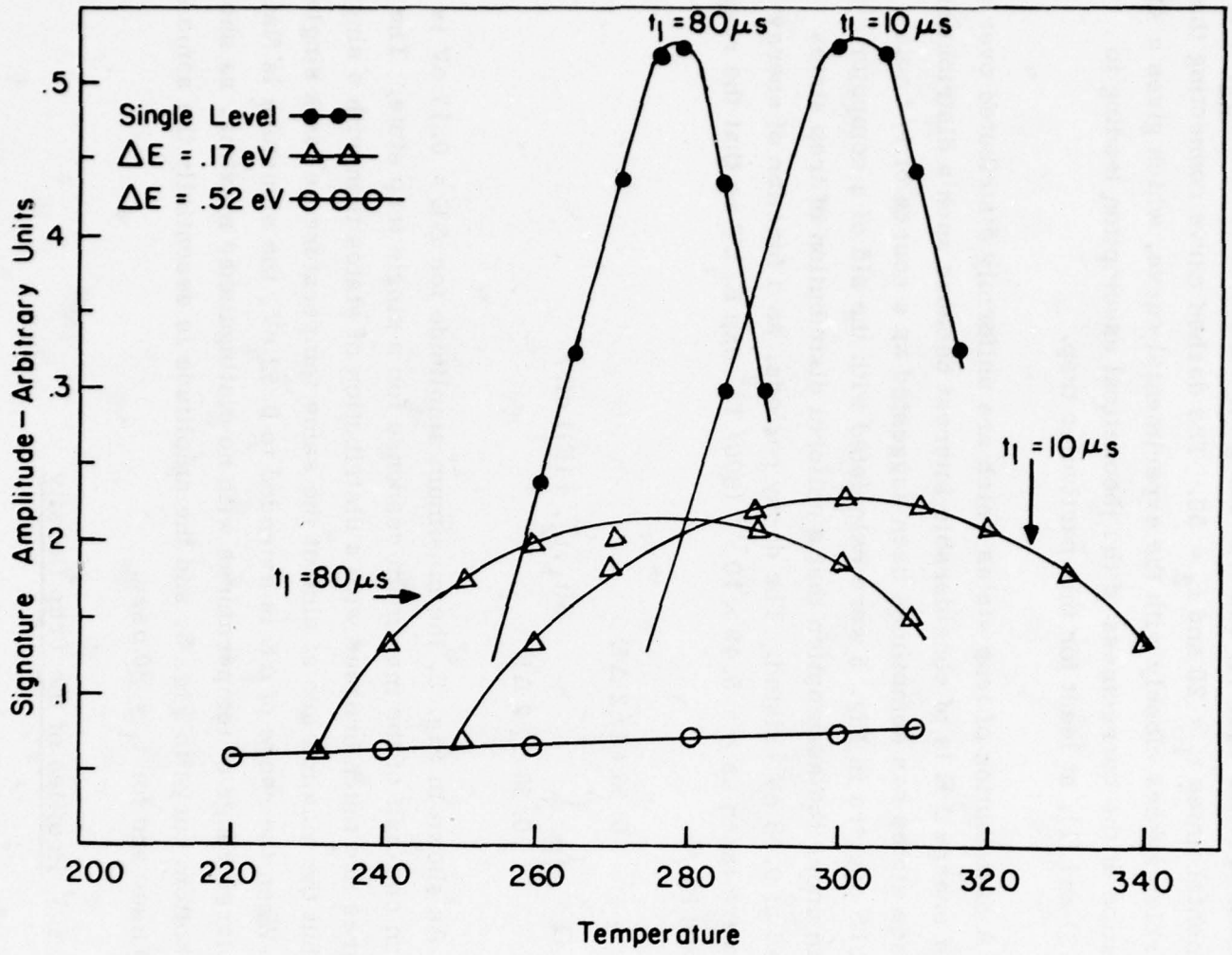

Figure 5 Comparison of DLTS Signatures from a Single Trap Level with Signatures from a Distribution of Traps Distributed Uniformly over an Energy Range ΔE and Centered at 0.58 eV. The ratio t_2/t_1 is 5 for all curves.

situation during a "set" pulse is shown in Fig. 6, where the depletion layer is at x_p during T_p. The trap level crosses the Fermi level at $x_p - \lambda_p$, so that

$$V_p + V_{BI} = \frac{q}{\epsilon}\left[\int_0^{x_p-\lambda_p} xN\,dx + \int_{x_p-\lambda_p}^{x_p} xN(1-\delta)dx\right] , \qquad (16)$$

where $N = N_d + N_T$ is the sum of the donor states plus the trap states and $N_T = \delta N$.

Now let the voltage change to V_B so that the depletion layer jumps out to $x_B + \Delta x$. We will take account of the variation in N(x), but we will assume that the fraction of trap states δ remains constant. Then, before the trap states have had a chance to empty, the total charge outside $x_p - \lambda_p$ remains constant, so that

$$V_B - V_p = (q/\epsilon)(1-\delta)\int_{x_p}^{x_B+\Delta x} xNdx , \qquad (17)$$

but after the traps have emptied and the depletion layer moves back to x_B,

$$V_B - V_p = (q/\epsilon)\left[\delta\int_{x_p-\lambda_p}^{x_p} xNdx + \int_{x_p}^{x_B-\lambda_B} xNdx + (1-\delta)\int_{x_B-\lambda_B}^{x_B} xNdx\right] . \qquad (18)$$

Substituting Eq. (17) into Eq. (18) yields

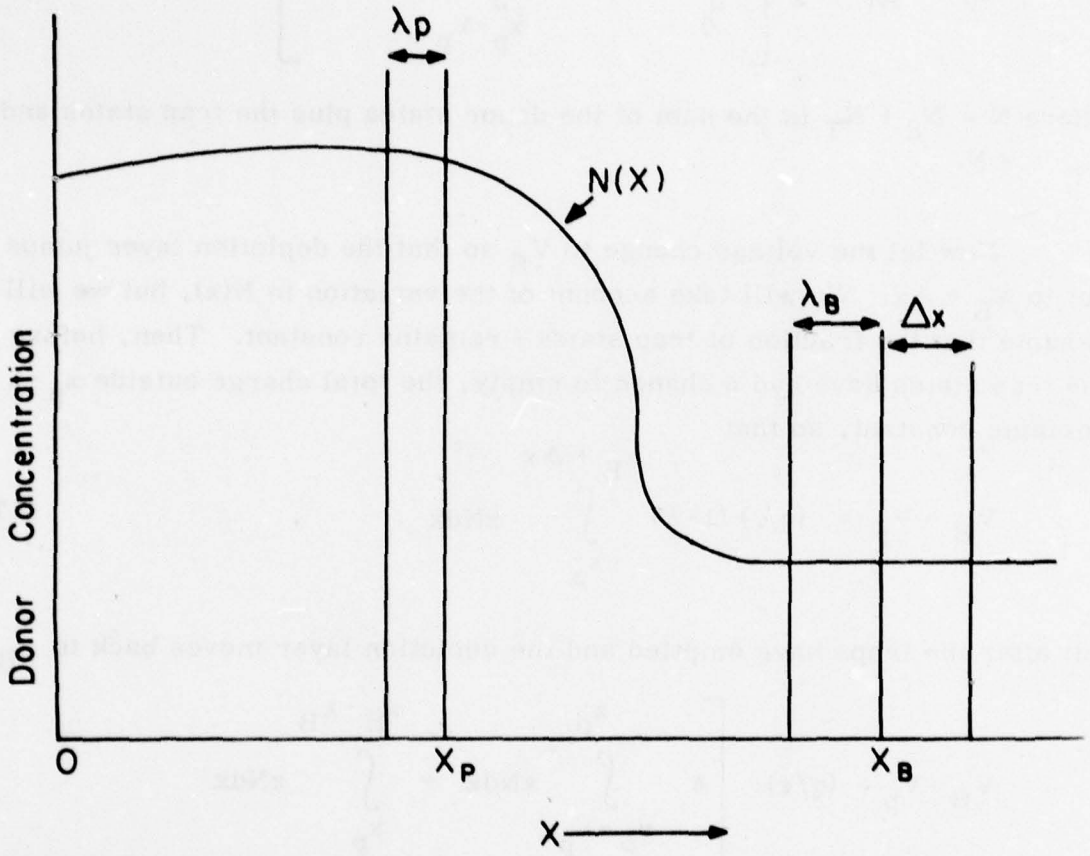

Figure 6 Schematic Diagram of Depletion Layer Positions during a Set Pulse. When the reverse bias switches from V_p to V_B, the depletion layer moves from x_p to $x_B + \Delta x$ and then slowly settles back to the equilibrium position at x_B.

$$\frac{\delta}{1-\delta}\left(\frac{\epsilon}{q}\right)(V_B - V_p) = \int_{x_B}^{x_B+\Delta_x} xN\,dx$$

$$+ \delta \int_{x_B-\lambda_B}^{x_B} xN\,dx - \delta \int_{x_p-\lambda_p}^{x_p} xN\,dx \quad . \tag{19}$$

where the integrals are all taken over a small interval so that the function N can be taken outside the integral sign. The last two integrals then become

$$\sqrt{\frac{2\epsilon V_T}{q(1-\delta)}}\ \delta \left[x_B\sqrt{N(x_B)} - x_p\sqrt{N(x_p)}\right] ,$$

which can usually be neglected. Here $q V_T = E_c - E_T$, where E_T is the trap energy level and $\lambda_B = \sqrt{\frac{2\epsilon V_T}{qN(x_B)}}$. Neglecting the last two integrals in Eq. (19), it becomes

$$\frac{\delta}{1-\delta} = \frac{qN(x_B)}{\epsilon(V_B - V_p)}\left[x_B\Delta_x + (\Delta_x)^2/2\right] . \tag{20}$$

Expressing x_B and Δ_x in terms of C_B and ΔC, and assuming $\delta \ll 1$ and $\Delta C \ll C$ gives

$$\delta = \frac{\epsilon q N(x_B) A^2}{V_B - V_p}\ \frac{\Delta C}{C_B^3} \tag{21}$$

Equation (21) is the basic equation for our profiling. In the case where N, as well as δ, is essentially constant between x_p and x_B, we can derive the equation

$$\delta = \frac{\overline{N}_T}{N_D} = \frac{2\,(V_B+V_{BI})\,\Delta C}{C_B\left[V_B-V_p-2\sqrt{V_T}\left(\sqrt{V_B+V_{BI}}-\sqrt{V_p+V_{BI}}\right)\right]} \quad , \qquad (22)$$

which often proves to be useful, because A does not have to be determined.

If V_B is large compared with V_{BI} and V_p, Eq. (22) simplifies to

$$\delta = 2\,\Delta C / C_B \quad , \qquad (23)$$

which corresponds to Lang's[7] Eq. (3). Elsewhere,[14] Lang has suggested an empirical variation of Eq. (23) which is 50 percent larger.

It should be noted that ΔC has been defined as the absolute magnitude of the capacitance deviation at time zero, as indicated in Eq. (1). The DLTS temperature sweep measures $C(t_2) - C(t_1)$ as a function of temperature. For any DLTS temperature sweep, the maximum value of $C(t_2) - C(t_1)$, which is measured experimentally with the calibrated DLTS equipment, determines ΔC from the equation

$$\left[C\,(t_2) - C\,(t_1)\right]_{max} = \Delta C\; S_{max} = 0.535\,\Delta C \quad , \qquad (24)$$

where the numerical value is for the particular case where $x = t_2/t_1 = 5$.

Strictly speaking, the time behavior of the capacitance decay is not an exponential function of time, even when the trap occupancy function decays exponentially. However, if Δx in Fig. 3 is small compared to $x_B - x_p$ in a set pulse and if $N_T \ll N_D$, the function f(t) in Eq. (1) is the same as the trap occupancy function f(t) in Eq. (14).

2.4 Design of the DLTS Equipment

The basic circuit for the capacitance measurement is shown in Fig. 7. In this circuit, C_D is the capacitance of the device to be measured,

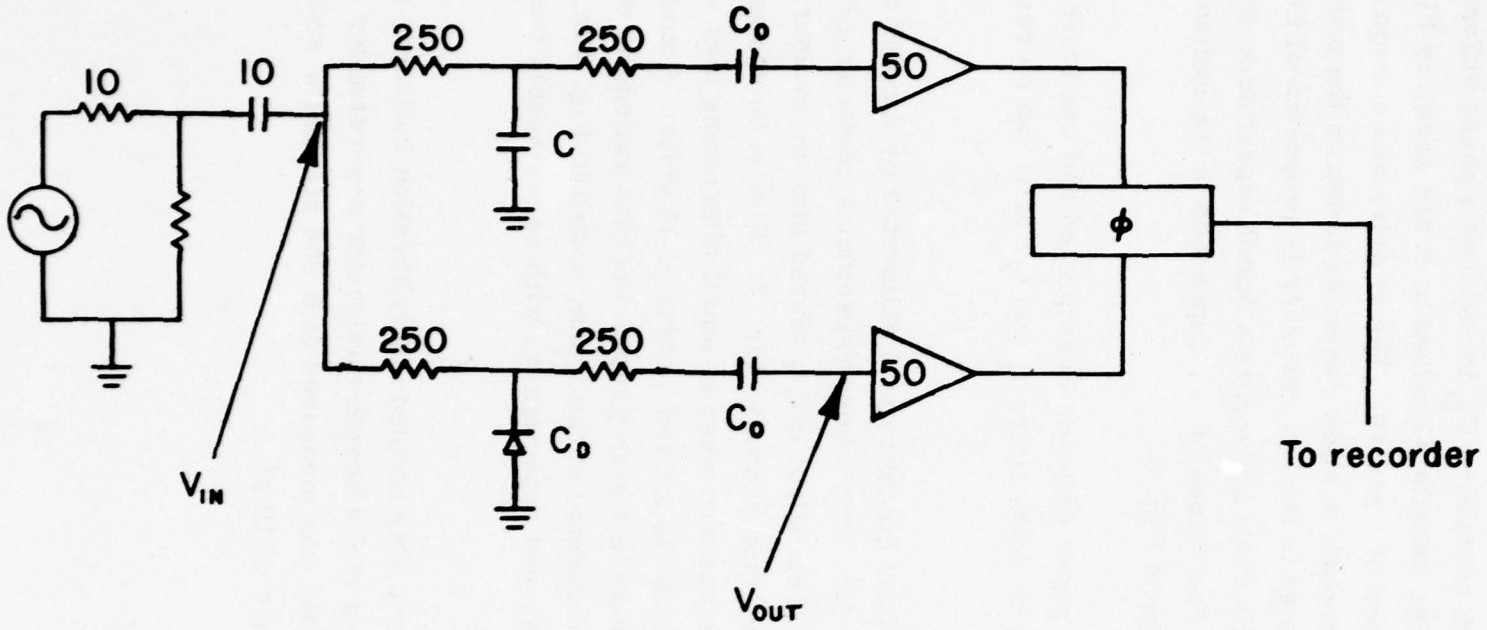

Figure 7 Diagram of the Circuit for Measuring C_D, the Device Capacitance.

and C is a comparison capacitance of a magnitude which reduces the phase difference of the two branches of the circuit to a value near zero.

The circuit branch containing C_D introduces a phase difference θ between V_{in} and V_{out}. The calculated values of θ are shown in Fig. 8 for blocking capacitance values of 1 and 10. The rf drive has a frequency of 50 MHz, which is large enough to allow response times on the order of 1 μsec. The voltage change to the x-y recorder is proportional to $\Delta\theta = \chi \Delta C_D / C_D$ when the diode undergoes a small capacitance change from C_D to $C_D + \Delta C_D$. The values of χ, expressed in the radians, were also calculated and plotted in Fig. 8.

The output of the phase detector is amplified and can be read through two boxcar integrators with delay times t_1 and t_2, or it can be read directly on an oscilloscope.

The sensitivity of the circuitry was calibrated by varying the reverse bias on a typical device, No. 930, whose capacitance curve as a function of bias, C(V), was known. The output is introduced into the measuring arm of the phase-sensitive detector shown in Fig. 7. Figure 9b shows the alternating capacitance measured when a small alternating bias voltage, shown in Fig. 9a, was added to a fixed dc bias of 35 volts. A measurement of the capacitance response to a step jump in the bias voltage is shown in Fig. 10b. The amplified version of the trace, shown in Fig. 10c, shows a fast response in the measured capacitance, with no noticeable transient behavior.

Both the pulsed and step methods of calibration indicated a sensitivity of 0.4 pf/ volt at the input of the boxcar-integrator x-y-recorder combination. A noise-limited sensitivity was measured at 0.004 pf/ cm for small variations about a device capacitance of 10 pf.

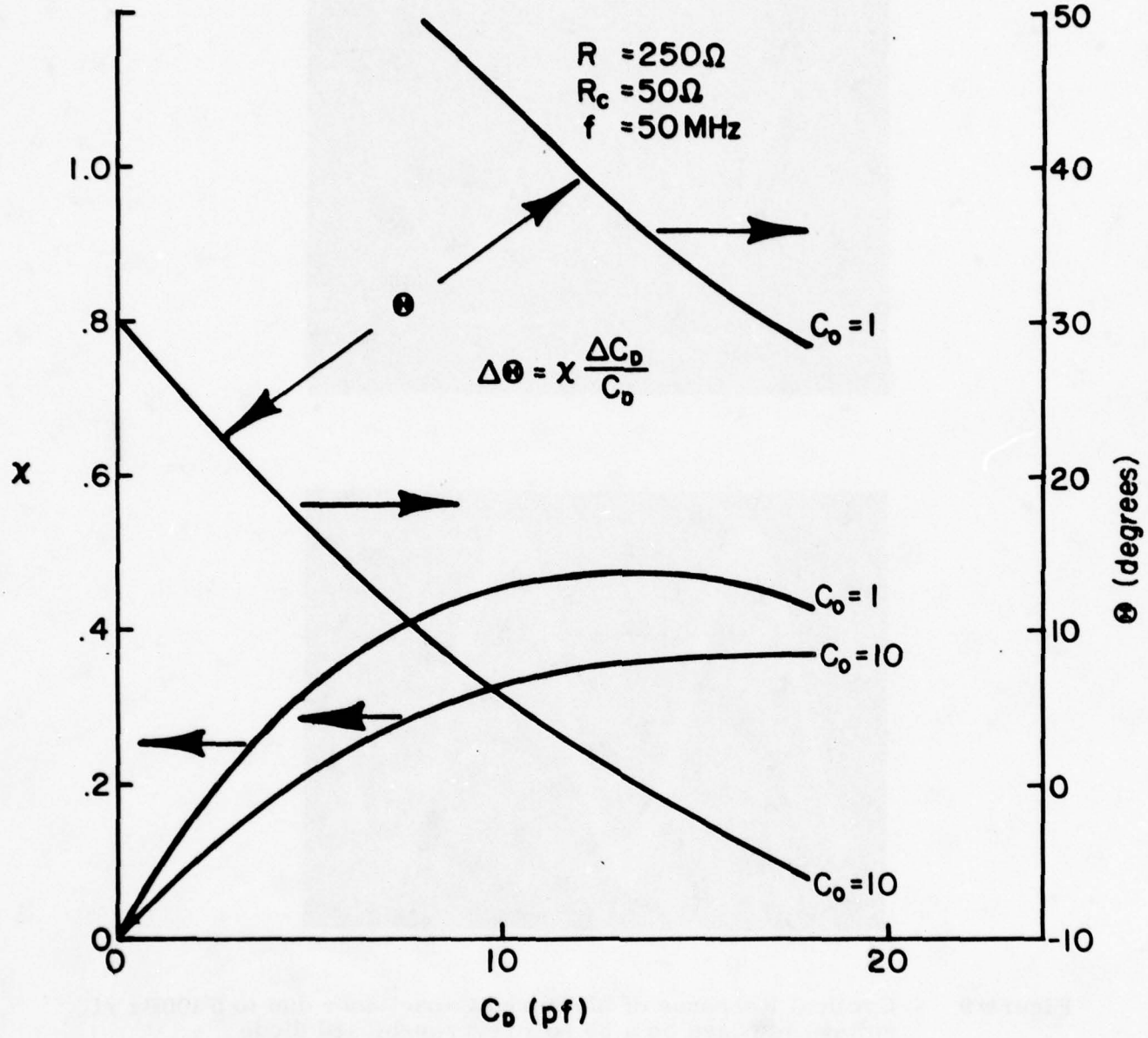

Figure 8 Plot of θ, the Phase Change (in degrees) Induced by the Device Capacitance C_D and the differential phase change (in radians) caused by a fractional change $\Delta C_D / C_D$ in the device capacitance.

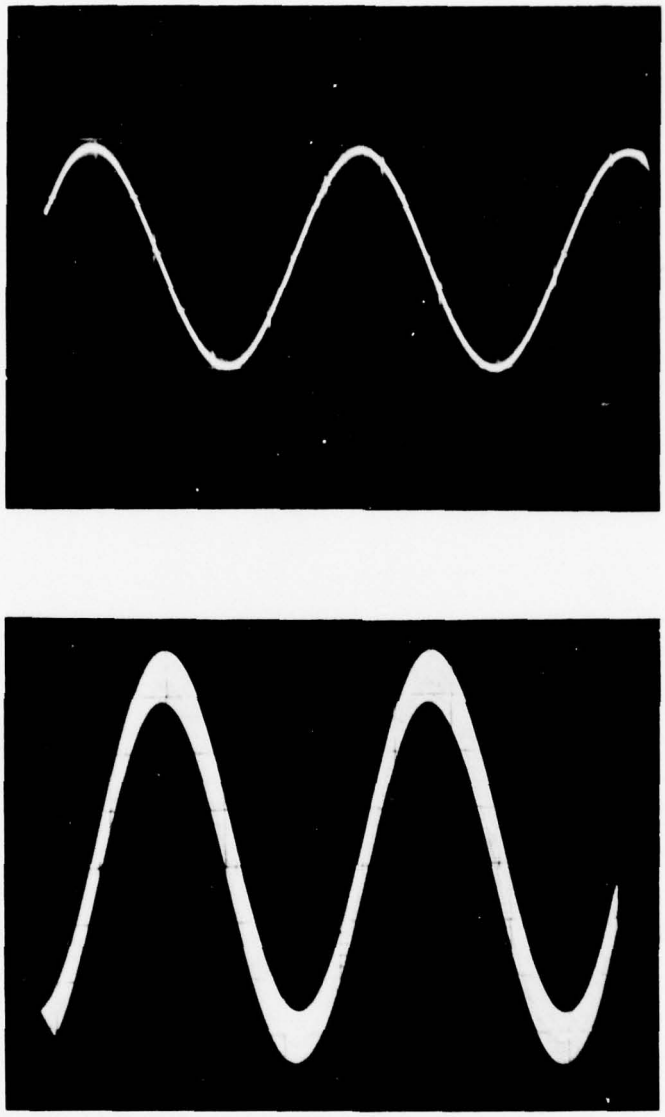

Figure 9 Cyclical Response of Measured Capacitance due to a 100Hz rf voltage imposed on a 35 volt reverse-biased diode

a) 2-volt p-p input voltage

b) capacitance signal recovered from phase detector prior to processing (0.04 pf/ div.)

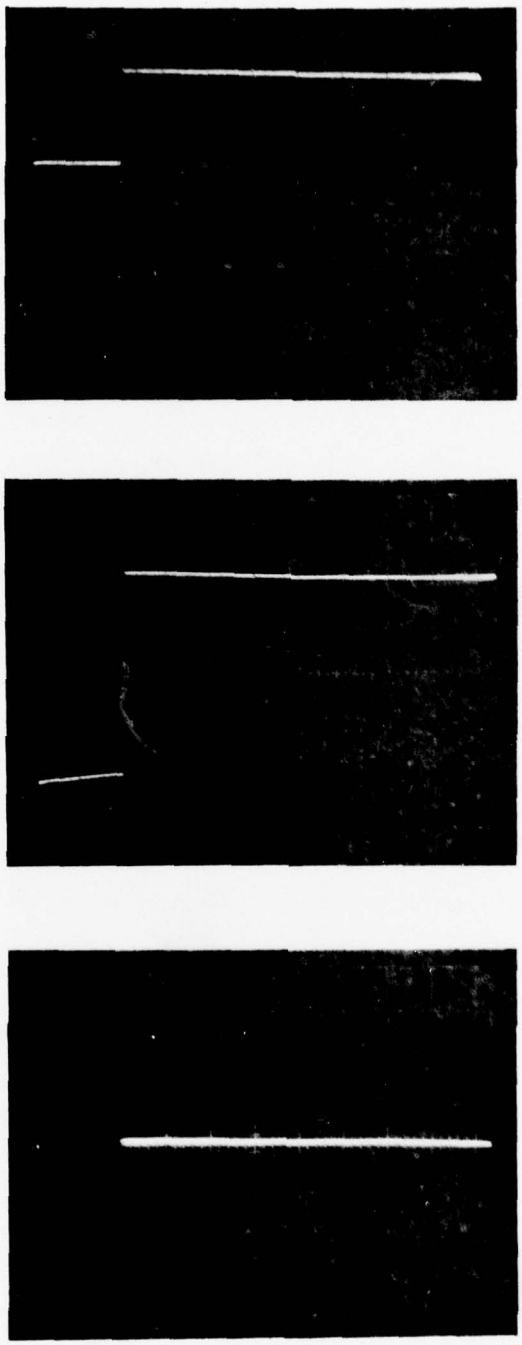

Figure 10 Pulsed Response from Reverse-Biased Diode

a) DC pulse to device (5 volts/ div).

b) capacitance change of 1.5 pf recovered from phase detector

c) amplified portion of above trace in the region of steady-state bias (35 volts).

3.0 DETECTION OF TRAPS IN N- AND P-GaAs GROWN ON CONDUCTING SUBSTRATES

A number of attempts were made to measure traps on GaAs epitaxy grown on n^{++} conducting substrates. None of these samples had been deliberately contaminated with chemical impurities to produce trap states. On the contrary, the material had been grown by techniques designed to produce high-quality IMPATT diodes. In these experiments we looked at material grown on Te-doped substrates. We suspected, and have verified by the lack of detectable trap levels in most of these experiments, that Te-doped GaAs is relatively free of undesired impurities. The semi-insulating substrates used for FET material growth appear to contain higher impurity levels.

The measurements on Te-doped substrates provide added confidence that the intrinsic vapor growth process does not provide significant densities of traps. The most likely conditions for producing traps in VPE are when sudden changes are made in the growth conditions such as occur when doping rates are drastically increased so as to produce a Read spike. A level of traps below the 10^{13} cm^{-3} level was, in fact, detected near the Read spike of C-band diode No. 904 as described below. A much larger density of traps was found in an $n^{+}pp^{+}$ wafer.

3.1 The Concept of Secondary Data Points from DLTS Curves

Bulk traps are analyzed by assuming their decay period satisfies an equation such as

$$\tau = A\,(300/T)^2 \exp\,(E_{na}/kT) \quad . \tag{25}$$

From each temperature sweep in the DLTS method, one data point is obtained, i.e., the temperature at the peak of the curve corresponds to a decay period $\tau_m = (t_2 - t_1)/\ell n\,(t_2/t_1)$, where t_1 and t_2 are DLTS measurement times. To determine A and E_{na} experimentally in Eq. (25) will require at least two curves, and more if a least-squares fit is desired.

Here we want to describe how a number of secondary data points can be obtained from a single DLTS sweep if a base line can be determined, so that we can measure the temperatures at which the signal equals α times the peak signal, where α is some number between 0 and 1. We now determine mathematically the value $\tau = \tau_A$ at the point where the signal is proportional to α times the maximum signal. This value of τ_A satisfies

$$S(\tau_A) = e^{-t_1/\tau_A} - e^{-xt_1/\tau_A} = \alpha S_{max} ,$$

where $S_{max} = x^{\frac{1}{1-x}} - x^{\frac{x}{1-x}}$.

A solution to this equation can be found such that τ_A/τ_m is a function of α and $x = t_2/t_1$. The numerical values of these solutions are given in Table II for $x = 2.5$ and $x = 5$, two values of x that we have used in our experiments.

TABLE II

DECAY PERIODS FOR SECONDARY DATA POINTS

α	$x = 2.5$	$x = 5$
	τ_A/τ_m	τ_A/τ_m
.25	10.1285	10.7672
.50	4.4270	4.6690
.75	2.4302	2.5325
.9	1.6665	1.7147
1.0	1.0	1.0
.9	.64053	.61392
.75	.49254	.45538
.5	.35143	.30634
.25	.24596	.20003

The successive values of α in Table II correspond to increasing temperatures.

3.2 Traps Near the Read Spike of a C-Band IMPATT Diode

As an example of the use of Table II, we consider the four DLTS curves in Fig. 11 which were measured in diode No. 904, a C-band Read IMPATT diode grown on a Te-doped substrate. Curves 1 and 4 each have six secondary data points marked on them for $\alpha = 0.5$, 0.75, and 0.9, where each value occurs on both the high and low temperature side of the peak. For example, in curve 1 the peak value occurs at 244°K where $\tau_m = 199$ nsec since $x = 5$ and $t_1 = 80\ \mu$sec, so that the pair of values constitute a principal DLTS data point. The first secondary point marked on curve 1, for $\alpha = 0.5$, occurs at T = 222°K where, from Table II, $\tau_A = 199\ \mu\text{sec} \times 4.669 = 928\ \mu$sec. In this manner, from the points marked on curves 1 and 4 we obtain 12 secondary data points and 4 primary data points from the peaks of the two curves. These points are listed in Table III and are marked on the lower curve in Fig. 12 (except for the two highest temperature secondary points on curve 4, which fall below the bottom of the Fig. 1). A least-squares fit to these 16 points, assuming τ satisfies the usual exponential equation (Eq. (15), gave the straight line in Fig. 12, with

$$E_{na} = 0.34 \text{ eV}$$

and

$$A = 1.2 \times 10^{-11} \text{ ,} \qquad (26)$$

where the root mean square error in this fit was 10 percent. The secondary points in Fig. 12 appear to be as accurate as the primary points, and they extend the range of our measurements considerably. The value of A corresponds to a cross section $\sigma_{na} = 4 \times 10^{-15}$ cm^2. These values for E_{na} and σ_{na} are reasonably close to two electron traps reported in the literature: one at 0.30 eV with a cross section of 7.2×10^{-15} cm^2 is labeled ELT in

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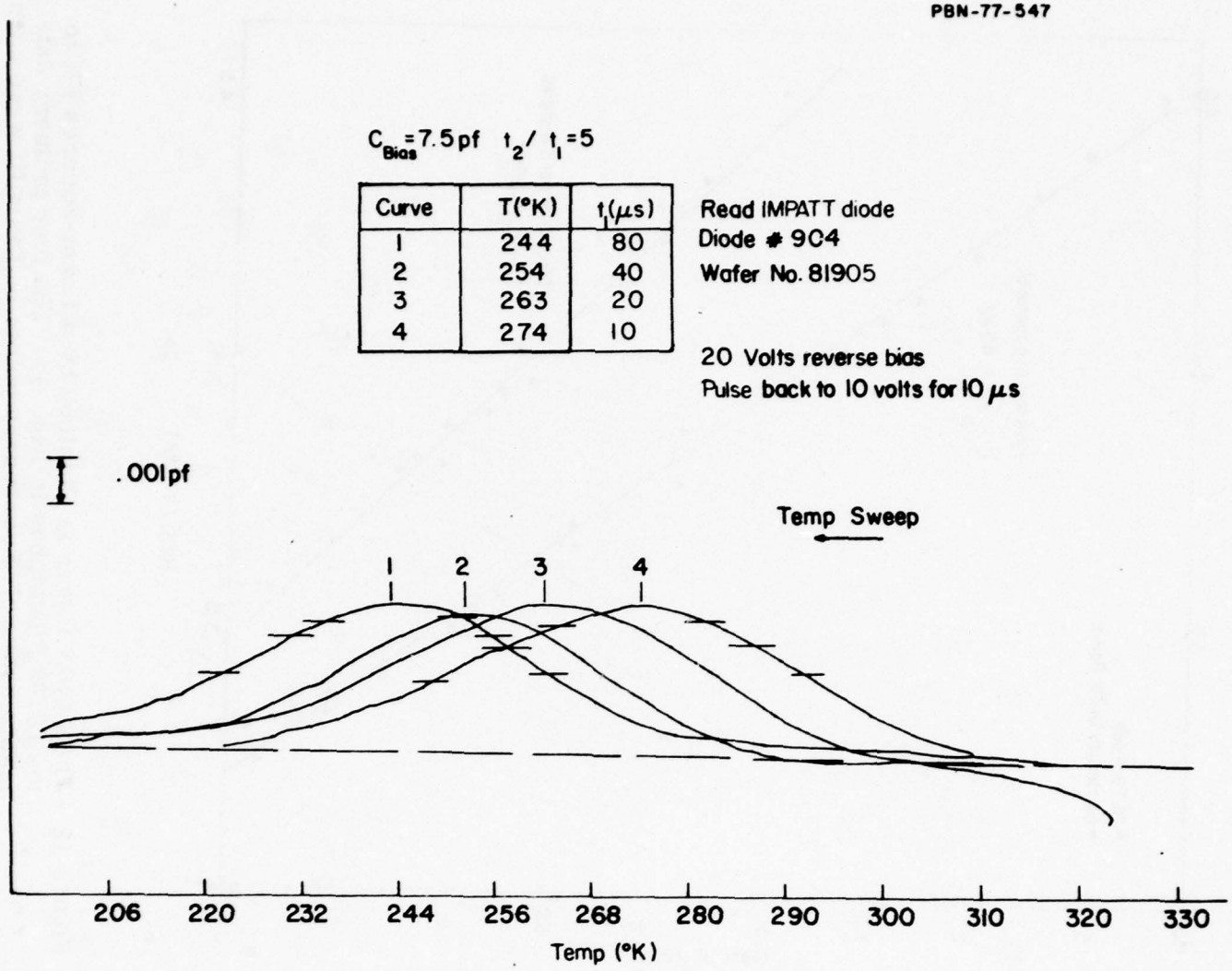


Figure 11 Four DLTS Temperature Sweeps used to Obtain the Activation Energy of an Electron Trap near the Doping Spike in a C-Band IMPATT Diode.

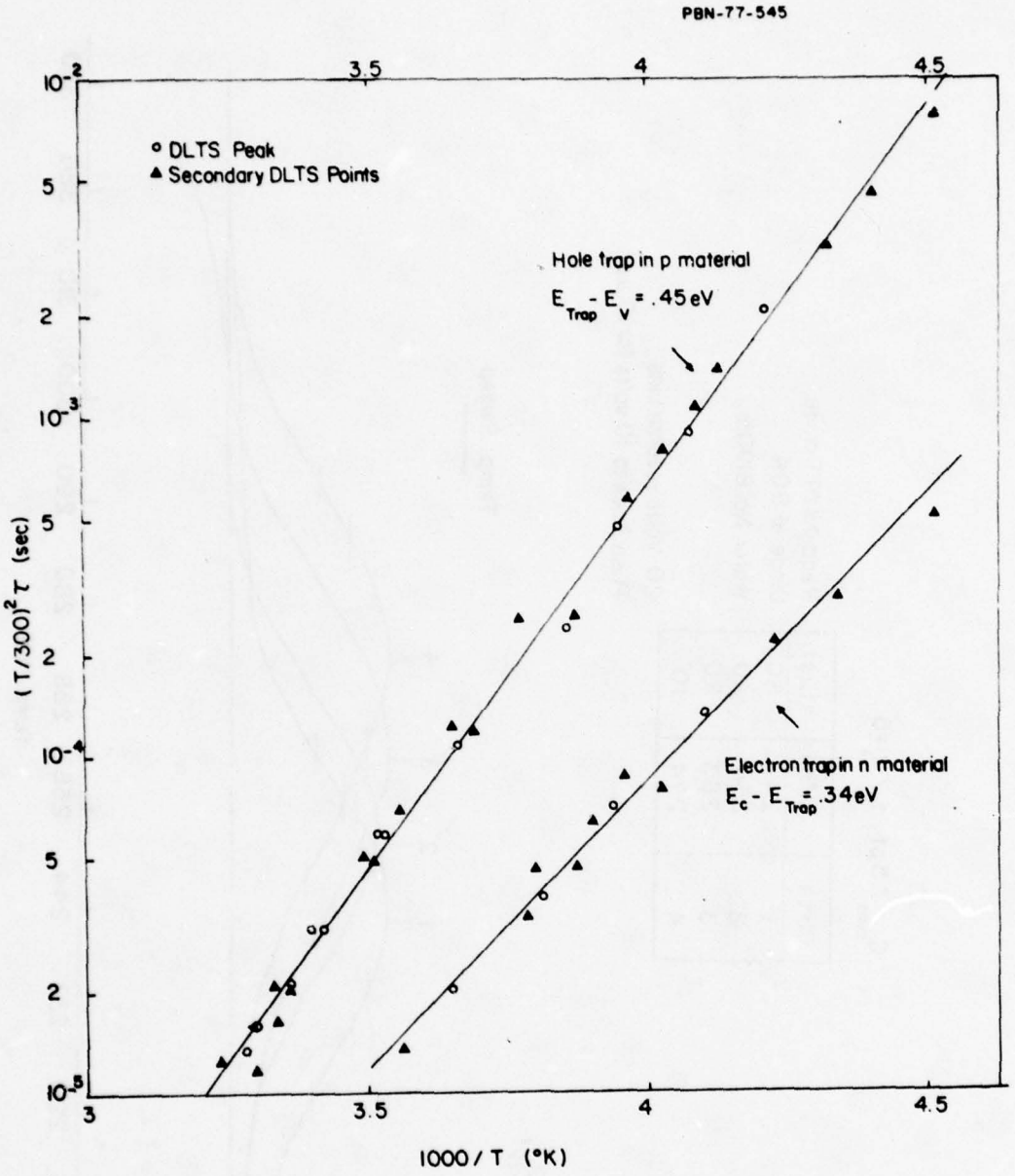


Figure 12 The Lower Curve is Obtained by a Least-Squares Fit to the DLTS Signatures in Fig. 11. The four primary data points and twelve secondary points in Table III were used. The upper straight line, corresponding to a hole trap in p material, was obtained by a least-squares fit to 40 data points, either primary or secondary data points obtained from the curves in Fig. 14. Several points used in the least-squares fit fell below the bottom of the graph, such as a primary data point for the hole trap which corresponded to T = 318°K and τ = 6.6 μs.

Ref. 8, while the other, with an activation energy of 0.36 eV and a cross section of 5.9×10^{-13} cm^2, is labeled T_1 by Wada, et al.[15]

TABLE III

DATA POINTS FOR ELECTRON TRAP IN C-BAND DIODE

Temperature °K	Decay Period (μs)	Curve No.	Percent Error*	Primary Data Point
293	7.6	4	-12	
287	11.3	4	- 8	
281	15.3	4	- 9	
274	25	4	-.2	Yes
264	43	4	- 6	
258	63	4	- 7	
248	116	4	-15	
263	61	1	19	
257	91	1	16	
252	122	1	18	
244	199	1	8	Yes
237	341	1	4	
231	504	1	- 4	
222	928	1	-20	
254	99	2	7	Yes
263	50	3	- 2	Yes

* Relative to least-squares analytical formula.

For the curves in Fig. 10, the set pulse had $V_B = 20$ and $V_p = 10$, which results in moving the depletion region over the Read spike and into the drift region. At the point x_B, the shallow donor density is 2×10^{15} cm^{-3}. The trap density indicated by Fig. 11 is only $7 \times 10^{12} cm^{-3}$, which is low enough so that it should not affect the performance of the diode.

3.3 Traps in an n^+pp^+ Diode

Few experiments have been carried out on p-GaAs except those of Hasegawa and Majerfeld[16], who measured slow decay periods on the order of seconds, while we have measured periods as short as ten microseconds. In our experiments, large trapping densities were detected in an n^+pp^+ diode. This diode had the n^+ contact deposited on the p-GaAs by silicon ion implantation at two different energies: implantation at 200 keV produced a surface density of 8×10^{13} cm^{-2}, while an additional surface density of $1.3 \times 10^{14} cm^{-2}$ was implanted at 400 keV. If these impurities are due to diffusion out of the p^+ substrate, it illustrates the wisdom of growing double-drift diodes on n^+ substrates.

Figure 13 shows C and C^{-2} as a function of bias voltage as measured experimentally from the n^+pp^+ device, which consists of four 10-mil mesas, so that the effective area is 2×10^{-3} cm^2. The steady-state acceptor doping as a function of distance from the junction was calculated, as shown in the insert. A selection of the numerical data printed out by the computer program profile is shown in Table IV, including Q, the total space charge per unit area uncovered by the depletion zone for a reverse bias V_B. With the aid of this data, we know the steady-state capacitance C_B and x_B, the depth to which we are probing for an applied reverse bias V_B.

TABLE IV

STEADY STATE DISTRIBUTIONS IN THE N^+PP^+ DIODE

V_B (volts)	C_B (pf)	x_B (μm)	N_A (cm^{-3})	Q (C/cm^2)
0	16.8	1.33	1.8×10^{15}	-1.5×10^{-8}
1.05	13.6	1.65	1.4×10^{15}	-2.3×10^{-8}
4.01	10.1	2.21	2.1×10^{15}	-4.0×10^{-8}
20.4	6.4	3.52	4.2×10^{15}	-1.0×10^{-7}
51.5	5.2	4.35	1.1×10^{16}	-1.9×10^{-7}

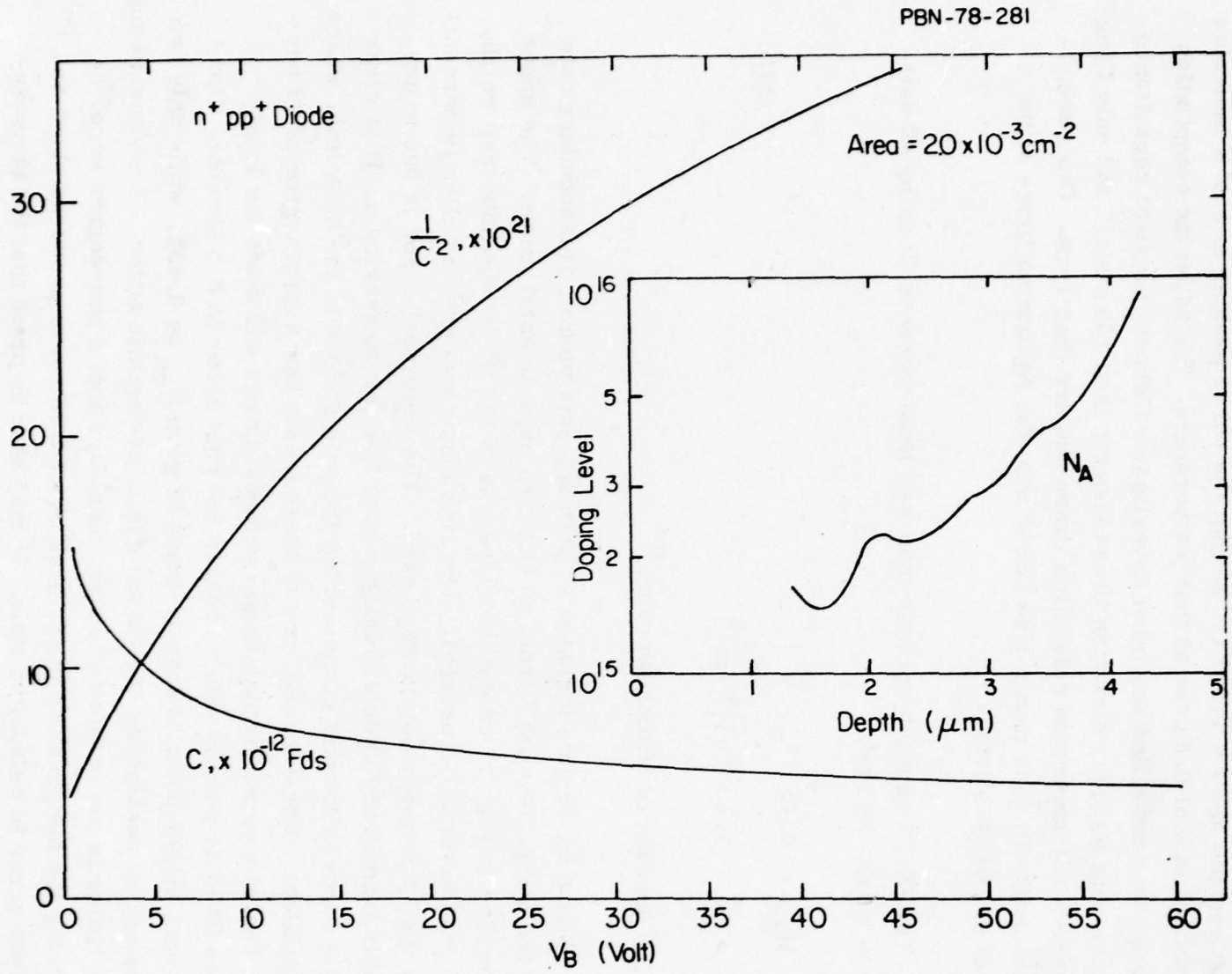


Figure 13 Experimentally Measured Curves for C and $1/C^2$ as a Function of Reverse Bias for the n^+pp^+ Diode used in these Experiments. The insert shows the acceptor doping density as a function of depth calculated by a numerical method from the C(V) curve using an area of $2.0 \times 10^{-3} cm^2$ for the total device area.

Nine DLTS curves are shown in Fig. 14. Since $x = 2.5$, the relaxation periods are $\tau = 1.637\ t_1$, so that the curve peaking at 318°K indicates a relaxation time of 6.6 μsec at that temperature. Based on the compilation in Ref. 8, we cannot find any other investigators whose transient capacitance measurements include relaxation times shorter than 100 μsec,[8] and only Lang has consistently measured relaxation times shorter than 1 ms. Our secondary data points include times even faster than the relaxation times at the peaks of the DLTS sweeps.

The DLTS data for the hole trap was least-squares fit using 40 data points to obtain the result

$$E_{pa} = 0.45\ \text{eV}$$
$$\sigma_{pa} = 1.4 \times 10^{-14}\ \text{cm}^{-2} \qquad (27)$$

using the notation of Mitonneau et al.[9]

These DLTS data included 17 primary data points, 16 secondary data points from Fig. 14, and 7 from an unshown experimental curve. The upper straight line in Fig. 12 shows the closeness of the fit for the hole trap which has an rms error of 13 percent. The rms error was even smaller (9 percent) if only the 17 primary points were used. The additional error is due to unavoidable inaccuracy in determining a base line for measuring α. It is clear that this error is largest in measuring the points close to the base line, where α is smallest. For example, one of these points had a large error of 37 percent. Therefore, we eliminated six external points and made the least-squares fit to 34 points, which reduced the rms error to 8.5 percent. However, both the 40-point and the 34-point fit gave E_{pa} as 0.452, while only two figures can be considered significant due to systematic error. The consistency of this fitting is impressive when one considers that a one-degree error in measuring the temperature at the peak of a DLTS curve produces about an 8 percent error in relaxation time. It may also be noted that the temperature scale at the bottom of Fig. 14 is nonlinear below 280°K due to the thermocouple response into the x-y recorder.

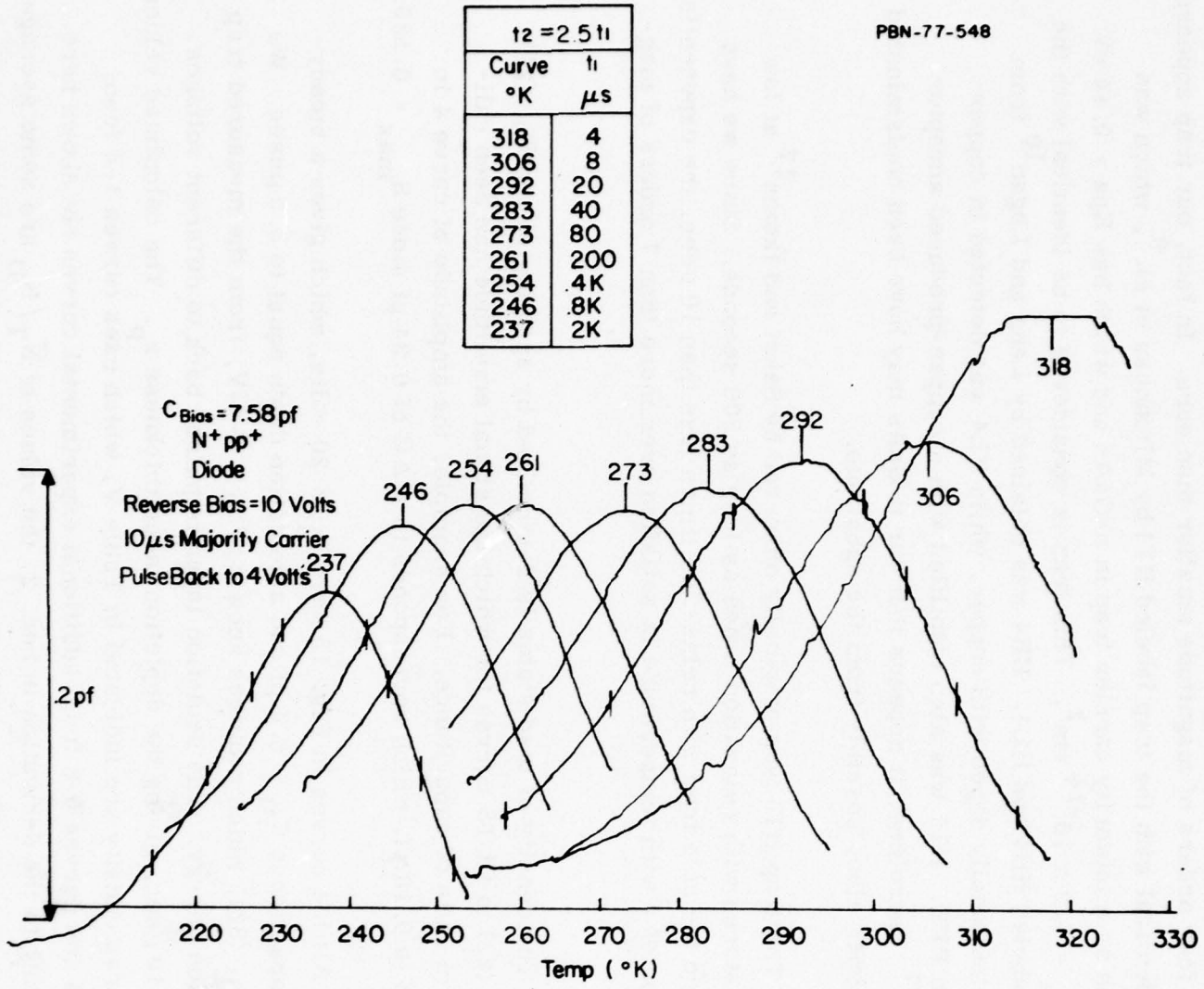


Figure 14 Nine DLTS Curves taken on p-GaAs which has a Hole Trap 0.45 eV above the Valence Band. The curves are labeled by the temperature at maximum amplitude: 8 secondary data points are marked on each of the curves labeled 237 and 292. The curve at 318°K exceeded the scale on the x-y recorder because of a high baseline probably caused by t_1 becoming comparable to the 1 μs time to switch from V_p to V_B.

Hasegama and Majerfeld detected a hole trap in p material which had an activation energy 0.44 eV above the valence band. However, this must be a different trap because its cross section is only 5×10^{-18} cm^2, which is almost four orders of magnitude smaller than ours. In fact, our trap appears to be identical with the trap labeled HT1 by Mitonneau et al.[9], which was detected as a minority carrier trap in n-GaAs and which has Epa = 0.44 eV and $\sigma_{pa} = 1.2 \times 10^{-14}$ cm^2. This trap is considered to be identical with the traps labeled HB4 and HL4. HB4 was obtained by Lang and Logan[10] from LPE intentionally doped with copper, while HL4 was detected in copper-diffused BPE. HT1 was also identified with a copper-produced acceptor level.[17] Therefore, it appears that our p-GaAs may have been contaminated with copper also, possibly from the substrate.

The trap HT1 was originally observed by Sakai and Ikoma[17] at low temperatures with relaxation times as long as 300 seconds. Since we have observed the hole trap with relaxation times less than 10 μsec, the exponential behavior of τ with temperature is satisfied over more than 7 orders of magnitude.

The density of trap states is determined by applying either Eq. (21) or Eq. (22) to DLTS curves for which the signal amplitude has been calibrated in units of capacitance. For example, the amplitude of curve 4 in Fig. 15 is 0.18 pf, which corresponds to a ΔC of 0.34 pf since $S_{max} = 0.535$.

All the curves in Fig. 15 have $V_B = 20$ volts, which gives a steady-state capacitance $C_B = 6.4$ pf and a depletion depth equal to 3.5 μnsec. We used Eq. (22), which requires knowing $V_T = 0.45V$, from the measured trap activation energy. The depletion layer is pulsed back to different voltages V_p for 10 μsec, giving the depletion layer thickness x_p. The calculated values of the trap density are indicated in Table V, which uses curves 1-4 from Fig. 15 and curves 5-8 from additional experimental curves not shown here. According to the derivation in Sec. 2, the values of $\overline{N}_T / N_D$ are some average value between x_p and x_B. The results indicate that N_T is a roughly constant fraction of the acceptor doping varying from about 8×10^{14} cm^{-3} to about 4×10^{14} as the depth changes from 3.3 to 2.2 μnsec.

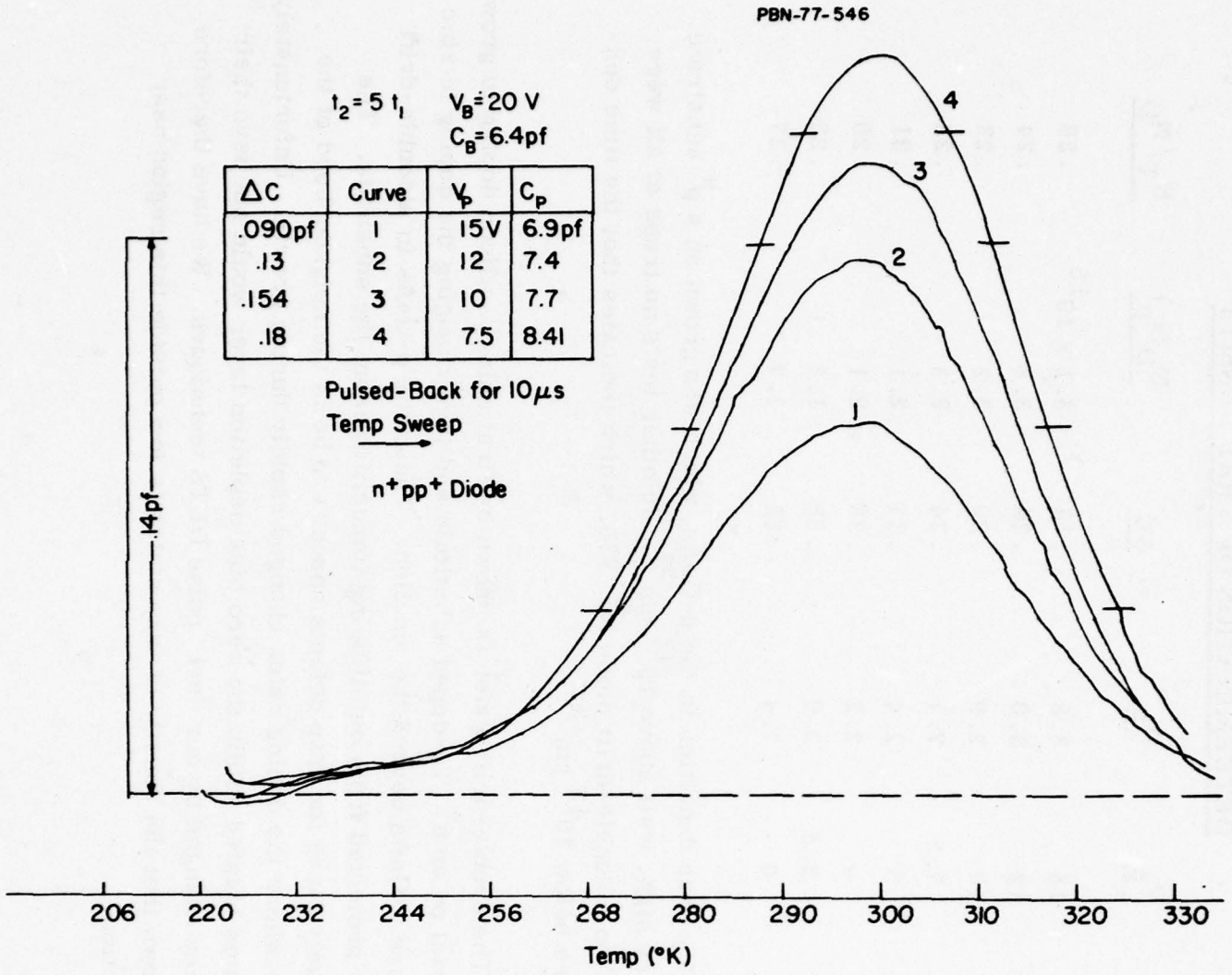


Figure 15 Curves used to find the Ratio of Trap Density to Shallow Acceptor Density and other Results in Table V. The secondary data points marked on curve 4 show that the signal is from the same hole trap detected in Fig. 14 with $V_T = 0.45$V.

TABLE V

DETERMINATION OF TRAP DENSITY

Curve	V_p	x_p	ΔC	$N_D(x_p)$	N_T/N_D
1	15	3.3	.17	3.1×10^{15}	.26
2	12	3.0	.24	3.6	.24
3	10	2.9	.29	3.2	.23
4	7.5	2.7	.34	2.3	.22
5	5	2.4	.37	2.1	.21
6	4	2.2	.39	2.1	.20
7	2.5	2.0	.58	1.8	.28
8	0	1.4	.62	1.7	.27

The trap densities in the p-GaAs, which was grown on a p^+ substrate, were very high, well above 10^{14} cm^{-3}. In other tests no traps at all were detected on a double-drift diode No. 935, which indicates that the time densities are below 10^{13} cm^{-3}.

The double-drift wafer is grown by first using a silicon doping to grow n-material on an n^+ Te-doped substitute and then changing the doping to zinc to produce p-GaAs beyond the junction. Thus, the p-GaAs in a double-drift diode is protected from outdiffusing impurities from the substrate. The most likely place for trap defects appears to be in the neighborhood of the junction where the doping rates changed rapidly during growth. Unfortunately, trap states located within the zero bias depletion layer would not have their occupancy changed by our "set" pulse DLTS techniques. We have therefore only shown that the density of trap states is low outside this region near the junction.

4.0 DETECTION OF BULK AND SURFACE TRAPS ON LOW-DOPED FET "TEST" WAFERS

During these experiments we detected a new type of DLTS signature which is qualitatively different from the signatures that have been detected for bulk traps. We will refer to these traps as surface traps because their behavior is consistent with the concept of surface traps in all of the characteristics which have been observed. Surface traps are particularly important for FET's because they are thin-layered devices in which the important interactions take place close to the surface.

4.1 Description of Fat FET's and Test Wafers

DLTS measurements on FET wafers are taken by means of special structures called fat FET's shown in Fig. 16.

During the measurements, the source and the gate are grounded. For a semi-insulating substrate these contacts take the same role as a back contact would play for capacitance measurements on a diode grown on a conducting substrate. The gate length has been increased from about 1 μm to 10 mils, which increases the capacitance to a value which can be conveniently measured. In addition, the large gate area minimizes the importance of surface charge which may exist between the gate and drain in comparison to the importance of surface states which may occur on the interface directly below the gate metallization.

Normal FET structures have an active layer doping of $N_D \approx 10^{17} cm^{-3}$. As can be seen from Eq. (22), the transient capacitance is proportional to N_T/N_D, making it difficult to detect a given trap density. Therefore, special test wafers were made up with $N_D \approx 2 \times 10^{15}$ cm^{-3} and h $\approx$ 4 μm, which will be described in this section. Measurements made directly on normal FET wafers with active layers h $\approx$ 0.3 μm and $N_D \approx 10^{17}$ cm^{-3} will be described in the next section.

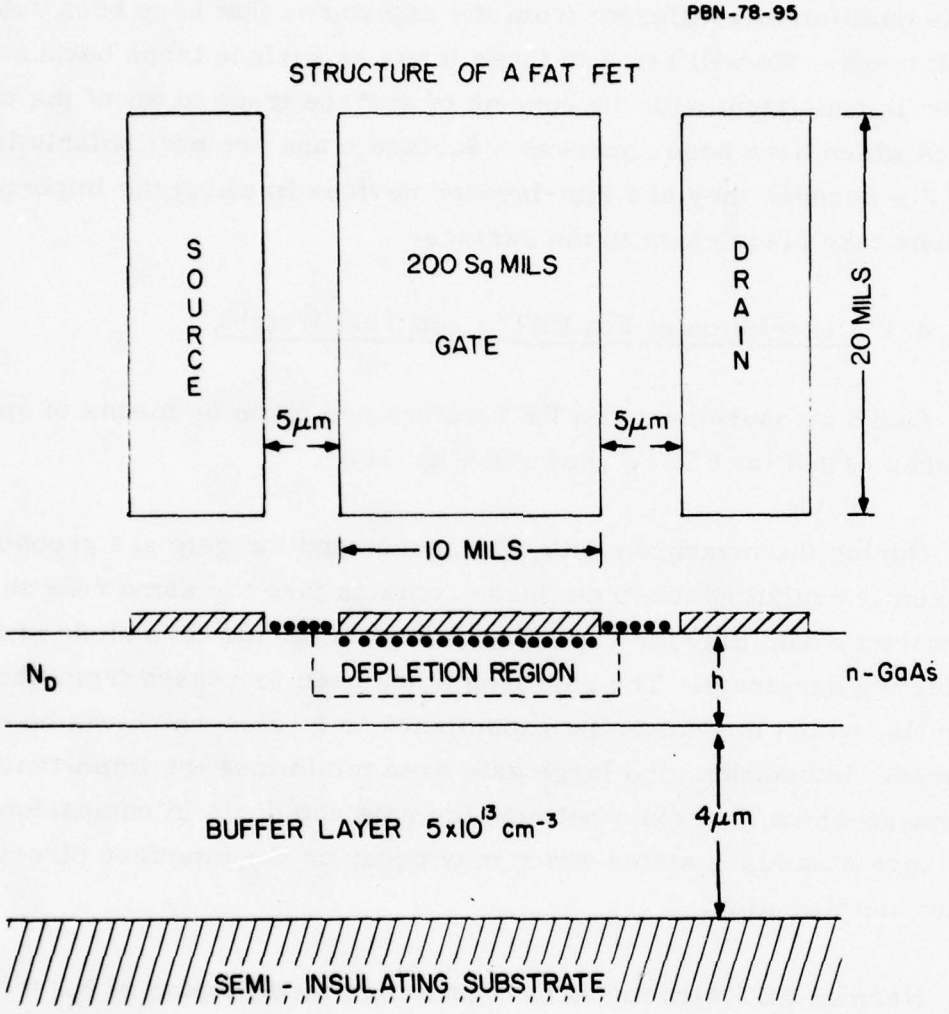


Figure 16 Structure of a Fat FET. The top view shows the dimensions of source gate and drain contacts. The side view shows a buffer layer between the semi-insulating substrate and the active layer.

Two of the low-doped test structures were investigated. Wafer No. 72507, whose profile as calculated from C(V) data taken on the fat FET* is given in Table VI, had an active layer with h = 3.9 μm and an active layer doping of about 1.8×10^{15}. A second fat FET was made from Wafer No. 72506, which had a similar doping profile but also had carbon-backing on the substrate during the growth process. We had reason to think that this might reduce the impurities in the epitaxial layers, since acceptor out-diffusion from the substrate or into the vapor stream had been shown to reduce mobility and even to change the n buffer layer near the substrate into p-material. It had been shown that growing epitaxial films on substrates with their backs covered by ≈ 200 Å of evaporated carbon had increased the mobility by as much as 50 percent. However, although both bulk and surface traps were detected on the two test structures, their intensities were similar, so that the carbon-backing technique was not very effective in reducing the measured trap levels, although it may produce more uniform doping levels in the buffer.

TABLE VI

(Wafer #72507)

V	C	Q	W	N_D
volts	pf	$C/cm^2 \times 10^{-8}$	μm	$1/cm^3 \times 10^{15}$
0	24.5	2.5	.58	---
1	16.2	4.0	.88	2.3
2	11.8	5.1	1.2	2.0
4	8.65	6.7	1.7	1.9
10	5.44	9.8	2.6	2.2
15	4.22	11.6	3.4	1.5
18	3.55	12.5	4.0	.54
20	2.85	13.1	5.0	.18
21.5	2.08	13.4	6.9	.05

* A value of 2.2 pf was subtracted from the capacitance measured on the device to account for parallel parasitic capacitance. The gate area of the fat FET was 200 mil.^{2}

4.2 DLTS Signatures from Surface and Bulk Traps Measured on the Test Wafers

The first measurements, taken on fat FET No. 19 from wafer No. 72507, produced the five curves shown in Fig. 17, which are perfect examples of a bulk trap signature. In fact, a least-squares fit to the five curves gave an rms error of only 0.7 percent (an agreement which must be partly fortuitous since it is more accurate than our measurement). This least-squares fit gave an activation energy $E_{na} = 0.85$ eV and a cross section of 1.6×10^{-13} cm^2. These parameters are similar to those of trap ET1 in Ref. 8, which were 0.85 eV and 6.5×10^{-13} cm^2. Our curves cover a range of relaxation times from 400 to 6500 μsec, while Sakai and Ikoma[17] measured ET1 over a range from 2 to 1000 sec. This trap level is often identified with oxygen contamination[8] substituting for an arsenic site.

These measurements were taken with the pulse length $T_p = 10\ \mu$sec. The voltages were $V_p = 0$ and $V_B = 4$, which, according to Table VI, corresponds to the depletion edge sweeping out from 0.6 to 1.7 μm.

The next measurements were taken with $T_p = 100\ \mu$sec, $V_p = 0$, and $V_B = 20$ V, so that the depletion layer swept out into the buffer layer where $x = 5\ \mu$m and the doping level has dropped to 1.8×10^{14} cm^{-3}. These experiments produced the nine curves in Fig. 18, which not only exhibit the positive peaks due to the bulk trap at 0.85 eV but also show negative peaks at lower temperatures, which we shall associate with surface traps.

The next experiment was designed to demonstrate that a long pulse-back time T_p is required in order to detect surface states. The results in Fig. 19 were obtained by superimposing DLTS sweeps with T_p varying from 10 μsec to 200 μsec, while τ_m ($= (t_2 - t_1)/\ell n\, t_2/t_1$) was about 50 μsec. There is no apparent change in the amplitude of the bulk trap signal as we expect from theory since the bulk traps should be filled in a short time ($1/nc_n$) after the free carriers sweep into the zero bias depletion edge. However, little or no surface trap signature can be detected for $T_p = 10\ \mu$sec;

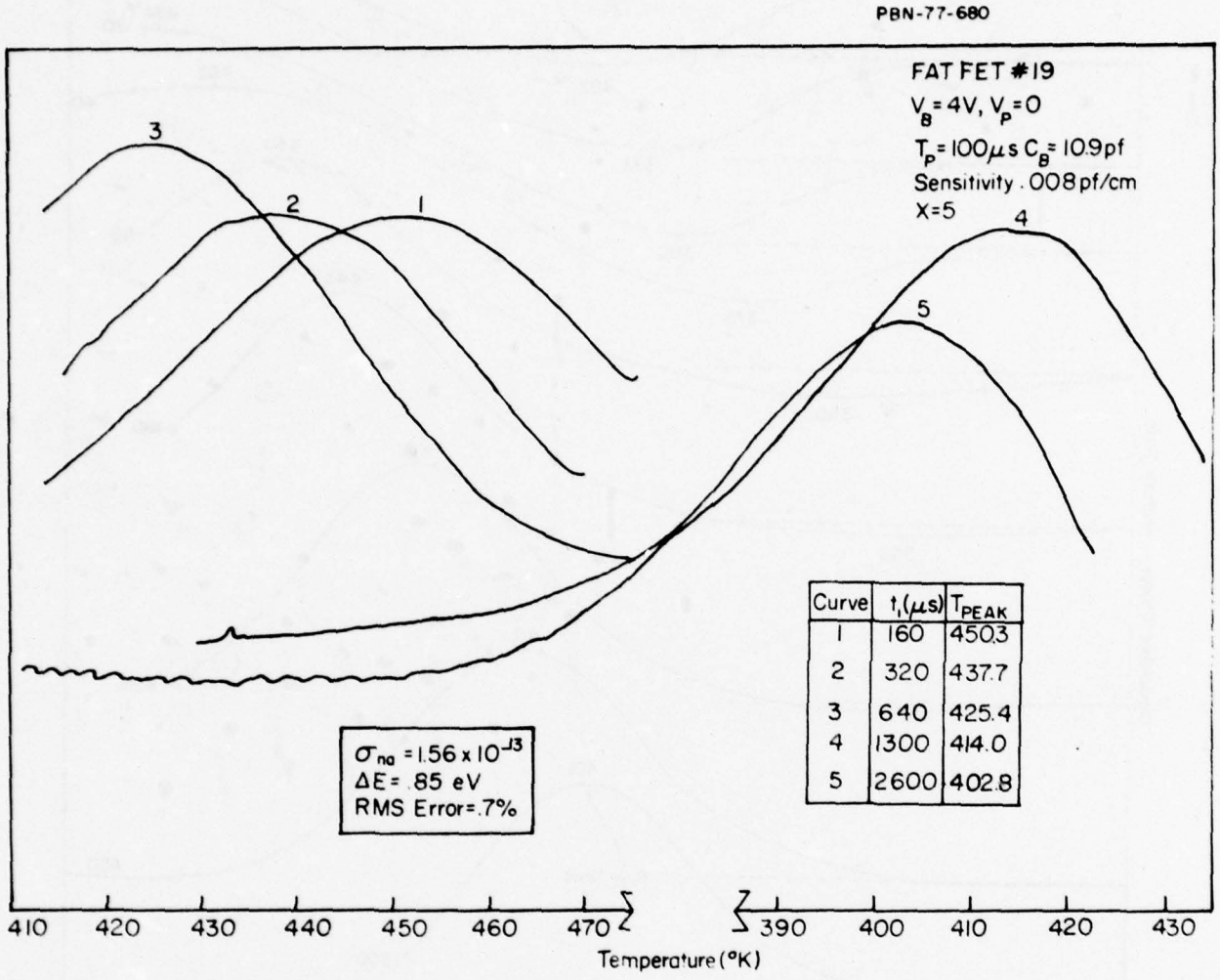


Figure 17 DLTS Curves for an Electron Bulk Trap at 0.85 eV, which has been observed by other investigators. Curves 4 and 5 are measured relative to the right-hand temperature scale which has lower temperatures than the left-hand scale which is drawn relative to curves 1-3.

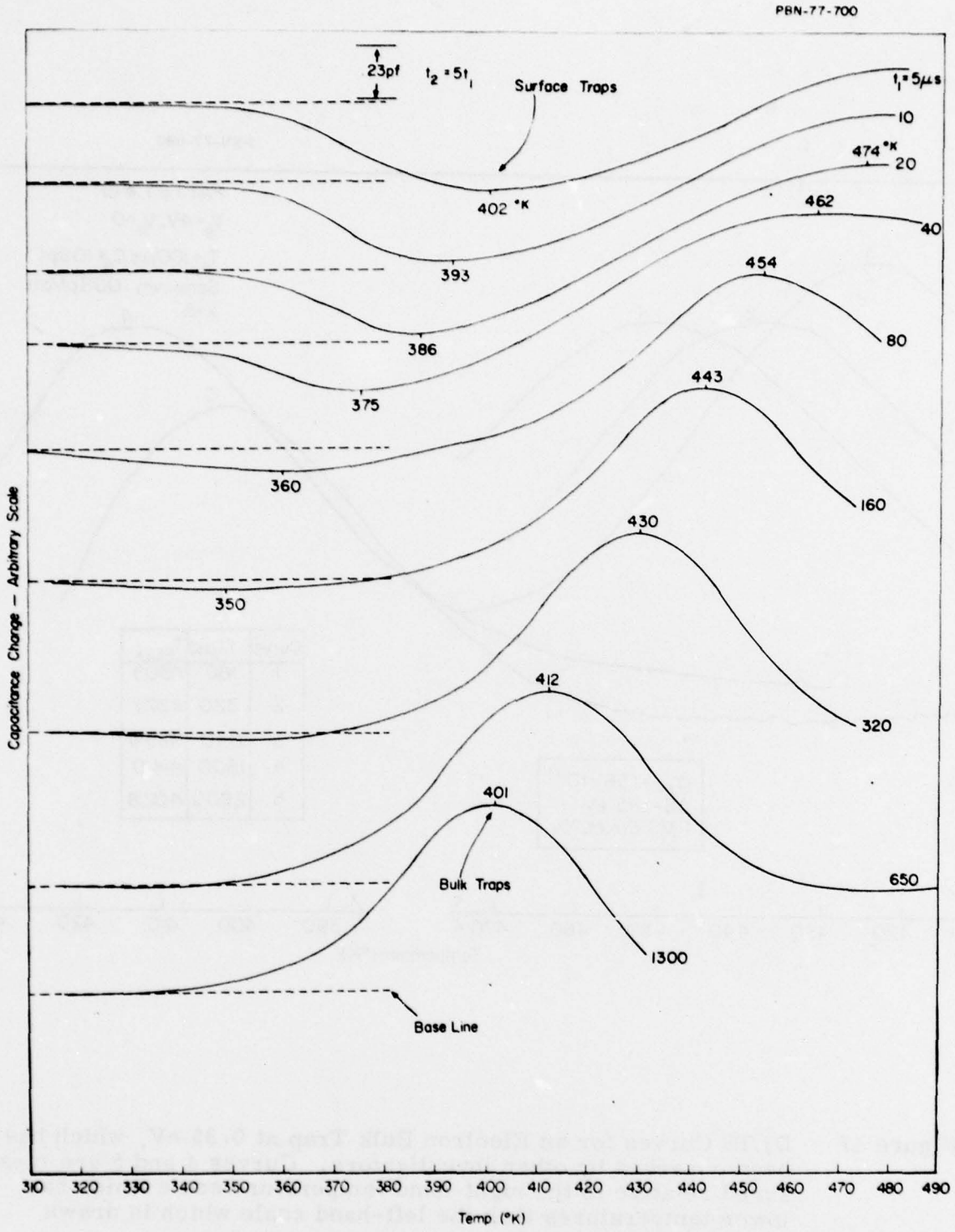


Figure 18 DLTS Curves for Values of the Boxcar Times t_i Ranging from 5 to 1300 μs. A positive peak corresponding to the oxygen bulk trap appears at the high temperature end of curves 3-9. Negative peaks, which we associate with surface states, appear at lower temperatures and can be distinguished on the first six curves.

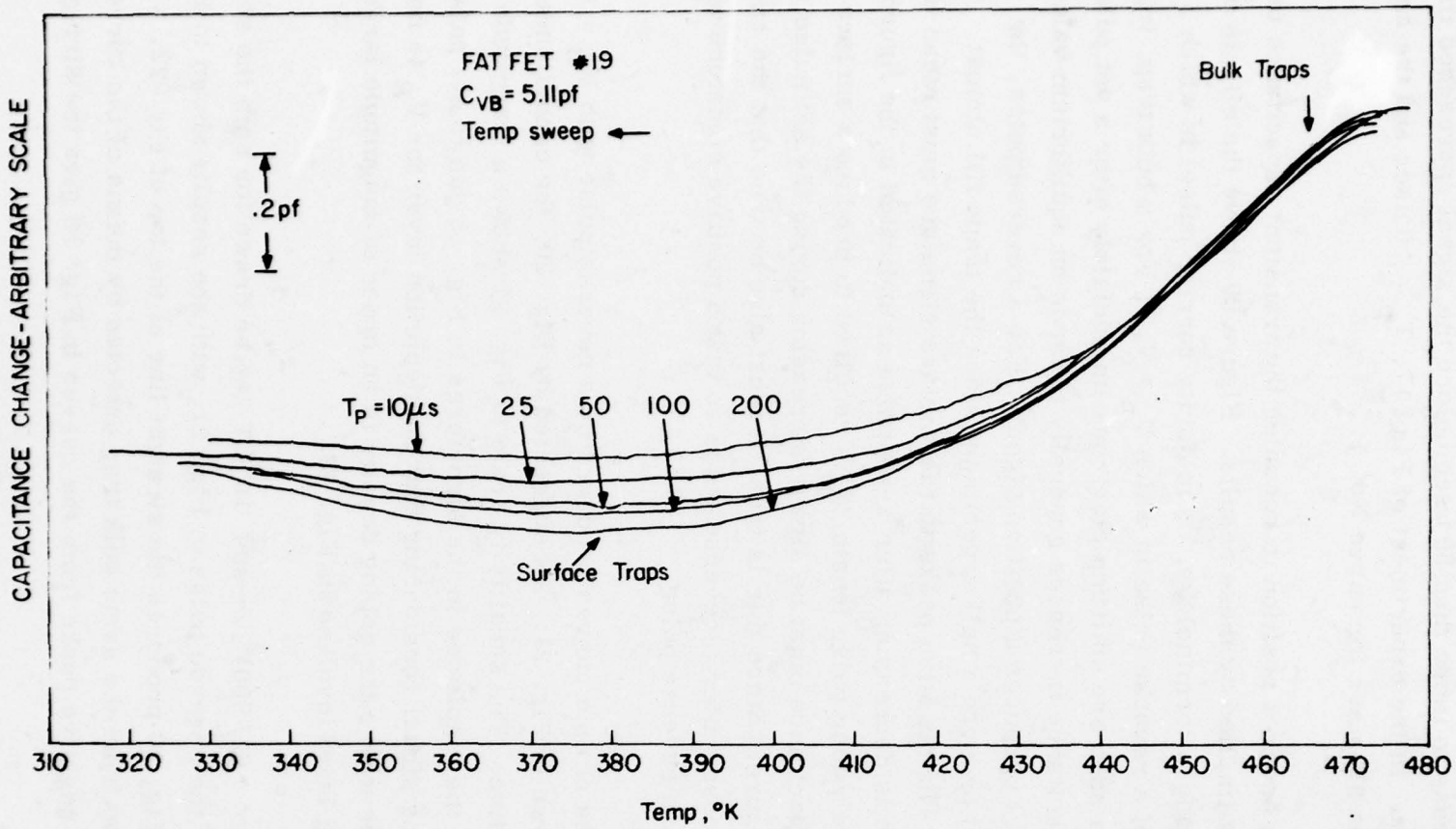


Figure 19 DLTS Temperature Sweeps on Wafer No. 72507, in which both bulk and surface trap are present, with different pulse-back times T_p. The bulk trap signature is independent of T_p but the amplitude of the negative peaks increases with T_p because the time required to empty surface traps exceeds about 50 μs.

T_p had to increase to more than 50 μsec before the signal approached its maximum value. In the experiment of Fig. 17, T_p = 10 μsec and the smallest value of τ_m was 398 μsec for curve No. 1.

Now we are in a position to consider the transient capacitance behavior which is implied by these results. Figure 20 shows the effects of a set pulse (in Lang's terminology,[7] a majority carrier pulse) in which $V_B > V_p$ and of a reverse pulse in which $V_p > V_B$. For a bulk trap, traps in the depletion zone are emitting electrons immediately after a set pulse, so that the capacitance increases gradually towards an equilibrium value and $C(t_2) - C(t_1)$ produces a positive signal. For a reverse pulse, the bulk trap would produce a null experiment since the traps fill almost immediately. The negative peaks in the surface signature must mean that the capacitance is decreasing after a set pulse as indicated in the figure. Since a relatively long pulse length T_p is required to produce a surface signature, the capacitance must be slowly increasing during the set pulse as shown in the figure. Since this is true, it must also be true that the capacitance increases after a reverse pulse so that a positive signature would be produced by a reverse pulse.

A series of nine curves produced by a reverse pulse with V_B = 0 and V_p = 20 is shown in Fig. 21. As suggested by Fig. 20, the capacitance change is positive. The sensitivity scale in Fig. 21 shows a magnitude of ΔC comparable to the amplitude in the signatures in Fig. 18 due to set pulses. This is a strong signal considering that the depletion layer for V_B is now in the active layer where the doping density is an order of magnitude larger than the doping level involved in Fig. 18.

A plot of $\tau (T/300)^2$ versus $10^3/T$ can be drawn for both the set pulse in Fig. 18 and the reverse pulse in Fig. 21, with the results shown in Fig. 22. The peaks in Fig. 18 produced the straight line at the top of Fig. 22, which is due to emission from the same bulk trap detected by means of the curves in Fig. 17. The negative peaks from the curves in Fig. 18 give the straight line

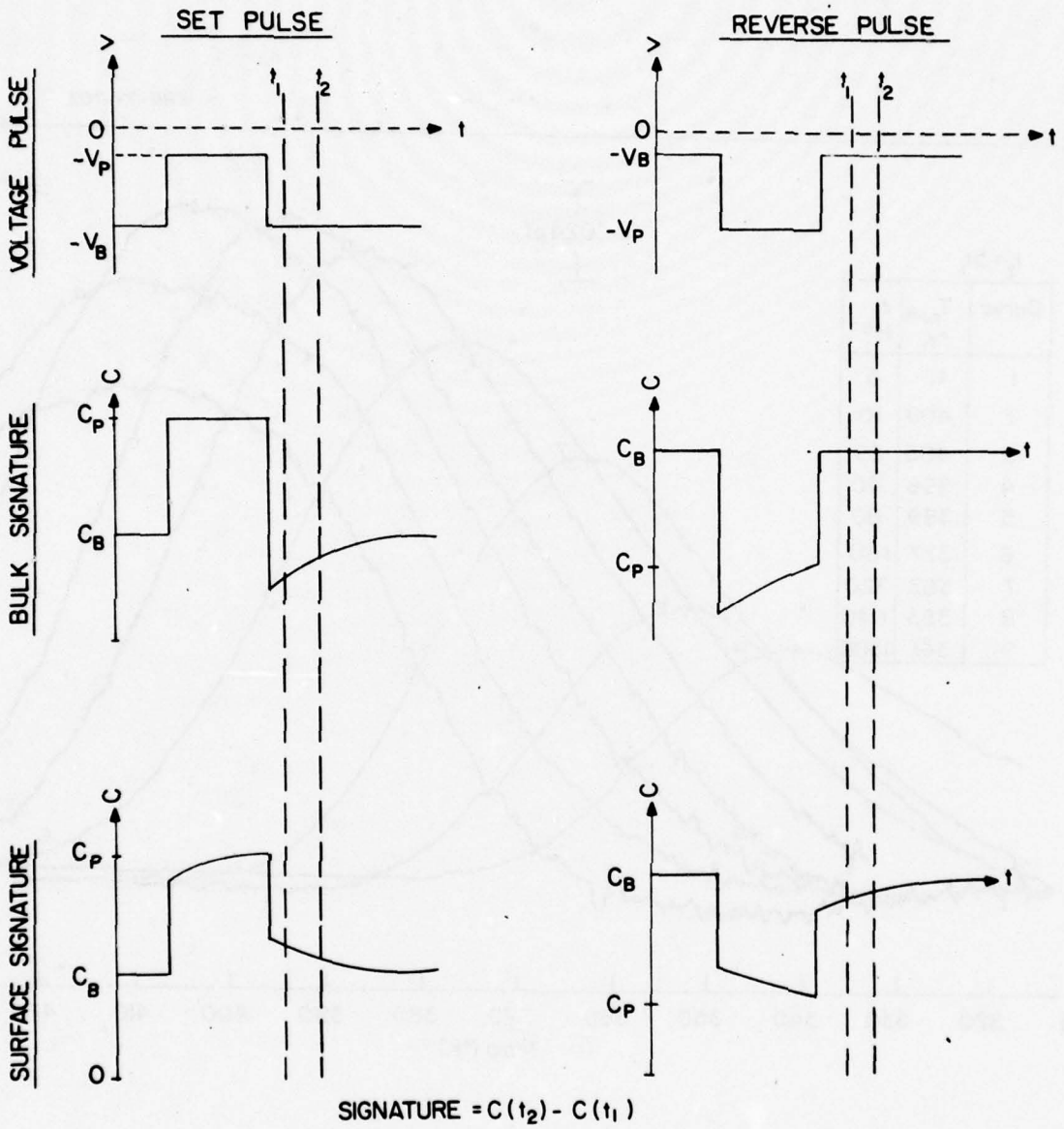


Figure 20 Schematic Diagram of the Transient Capacitance Produced by a bulk trap and by a surface signature when two types of pulses are applied to a Schottky barrier. The bulk trap produces a positive DLTS peak for a "set" pulse and no signature for a "reverse" pulse. The surface signatures produce negative peaks for a "set" pulse and positive peaks for a "reverse" pulse. The DLTS boxcar times are t_1 and t_2.

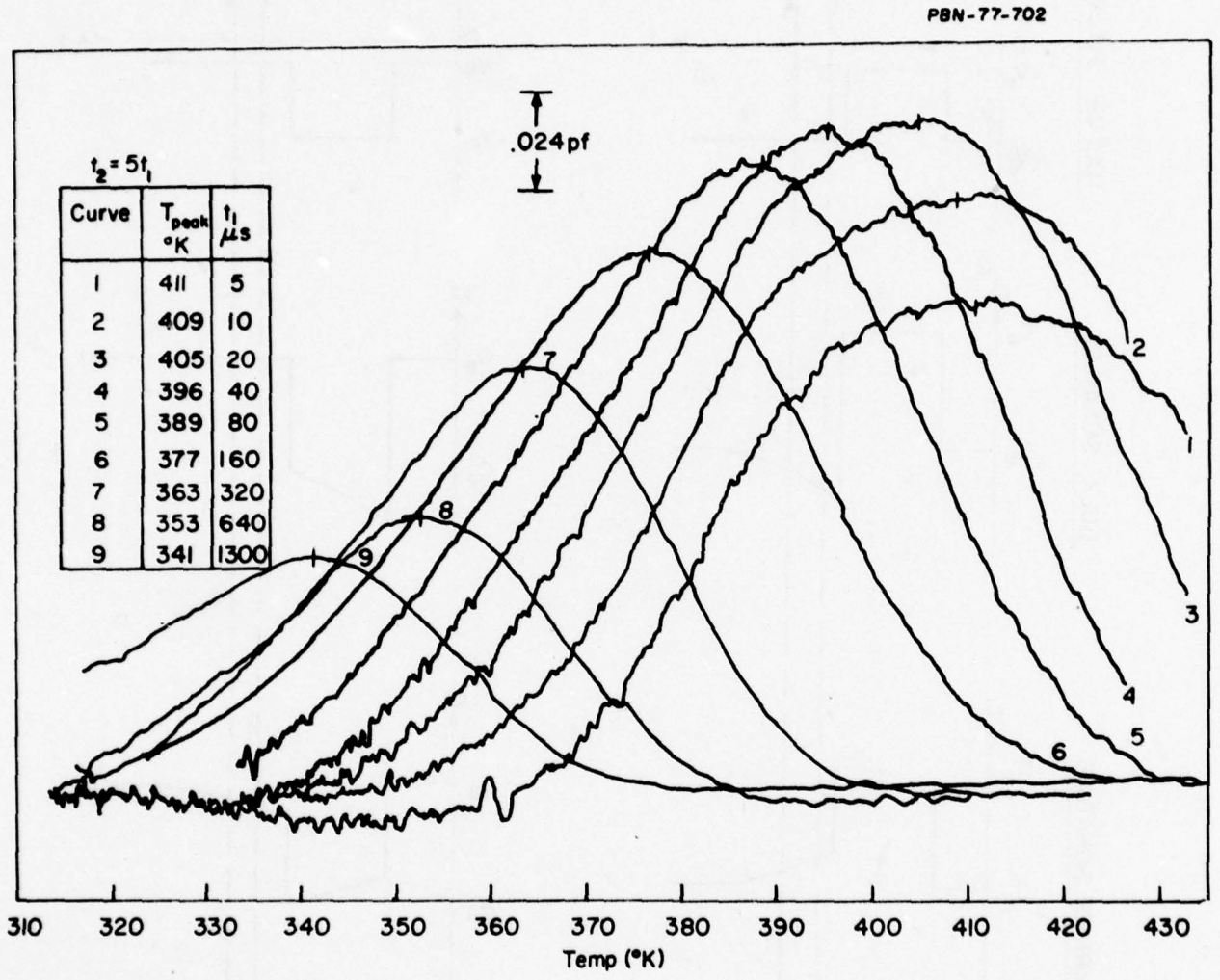


Figure 21 DLTS Curves From Surface States for a Reverse Pulse with $V_B = 0$ and $V_p = 20$ when the pulse length T_p is 100 μs.

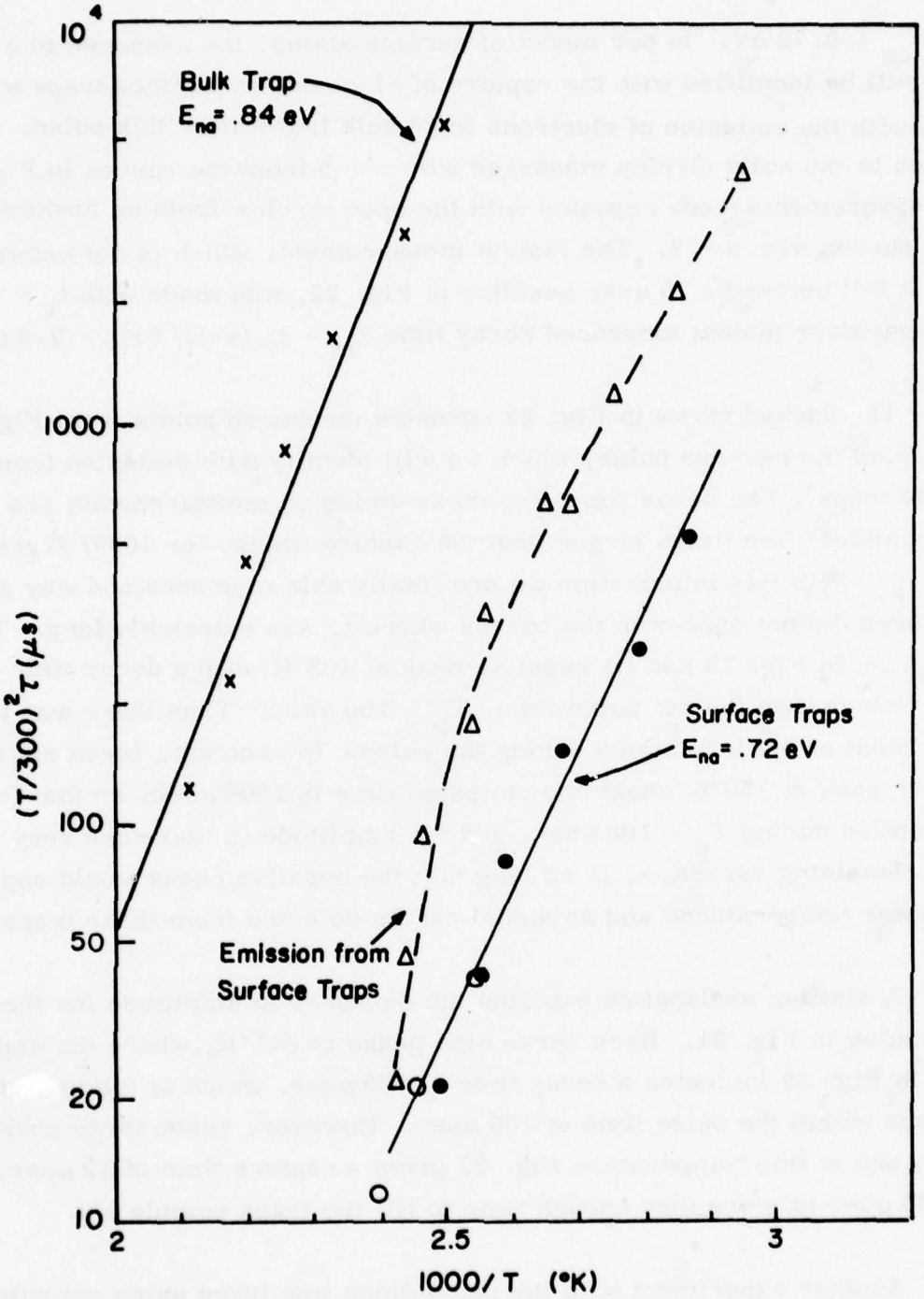


Figure 22 Plots of $(T/300)^2\tau$ versus 1000/ T. The upper straight line is a least squares fit for a bulk electron trap. The lower straight line with E_{na} = 0.72 eV is due to capture of electrons by surface states after the set pulses in Fig. 18. The dashed curve connects points calculated from the reverse pulse data in Fig. 21 which are caused by emission from surface traps.

with E_{na} = 0.72 eV. In our model of surface states, the response to a set pulse will be identified with the capture of electrons by surface traps which contrasts with the emission of electrons from bulk traps after this pulse. In addition to the solid circles measured with x = 5 from the curves in Fig. 18, the measurements were repeated with the open circles from an unshown set of curves with x = 2. The fastest measurement, which is not shown since it fell below the 10 μsec baseline in Fig. 22, was made with t_1 = 2 μsec which gave our fastest measured decay time $\tau_m = t_1 (x-1)/\ell n\, x$ = 2.9 μsec.

The dashed curve in Fig. 22 connects measured points from Fig. 21, i.e., from the reverse pulse, which we will identify with emission from the surface traps. The decay times for these emission measurements are approximately five times larger than the capture times, for 1000/ T greater than 2.6. With this information we are finally able to understand why surface signatures did not appear in the curves where t_1 was extremely long. The first curve in Fig. 18 had its negative peak at 402°K with a decay time of 60 μsec, which is less than the set pulse time, T_p = 100 μsec. Thus there was time to empty most of the trap states during the pulse. In contrast, curve six has a negative peak at 350°K where the emission time is 1500 μsec, so that few traps are emptied during T_p = 100 μsec, and the amplitude is therefore very small. In the remaining curves, t_1 is so long that the negative peaks would appear at still lower temperatures and no signal can be detected from these traps.

A similar explanation explains the decrease in amplitude for the reverse pulse in Fig. 21. Here curve nine peaks at 341°K, where the capture curve in Fig. 22 indicates a decay time of 700 μsec, which is too long to fill the traps within the pulse time of 100 μsec. However, curve three peaks at 405°K, and at this temperature Fig. 22 gives a capture time of 12 μsec, so that 100 μsec is more than enough time to fill the traps completely.

Another experiment with the same diode was taken using set pulse in which V_B = 21.5 V, but V_p took on the values 0, 5, 10, 15 and 20 volts. The curves, recorded with t_1 = 40 μsec and t_2 = 200 μsec, are shown in Fig. 23.

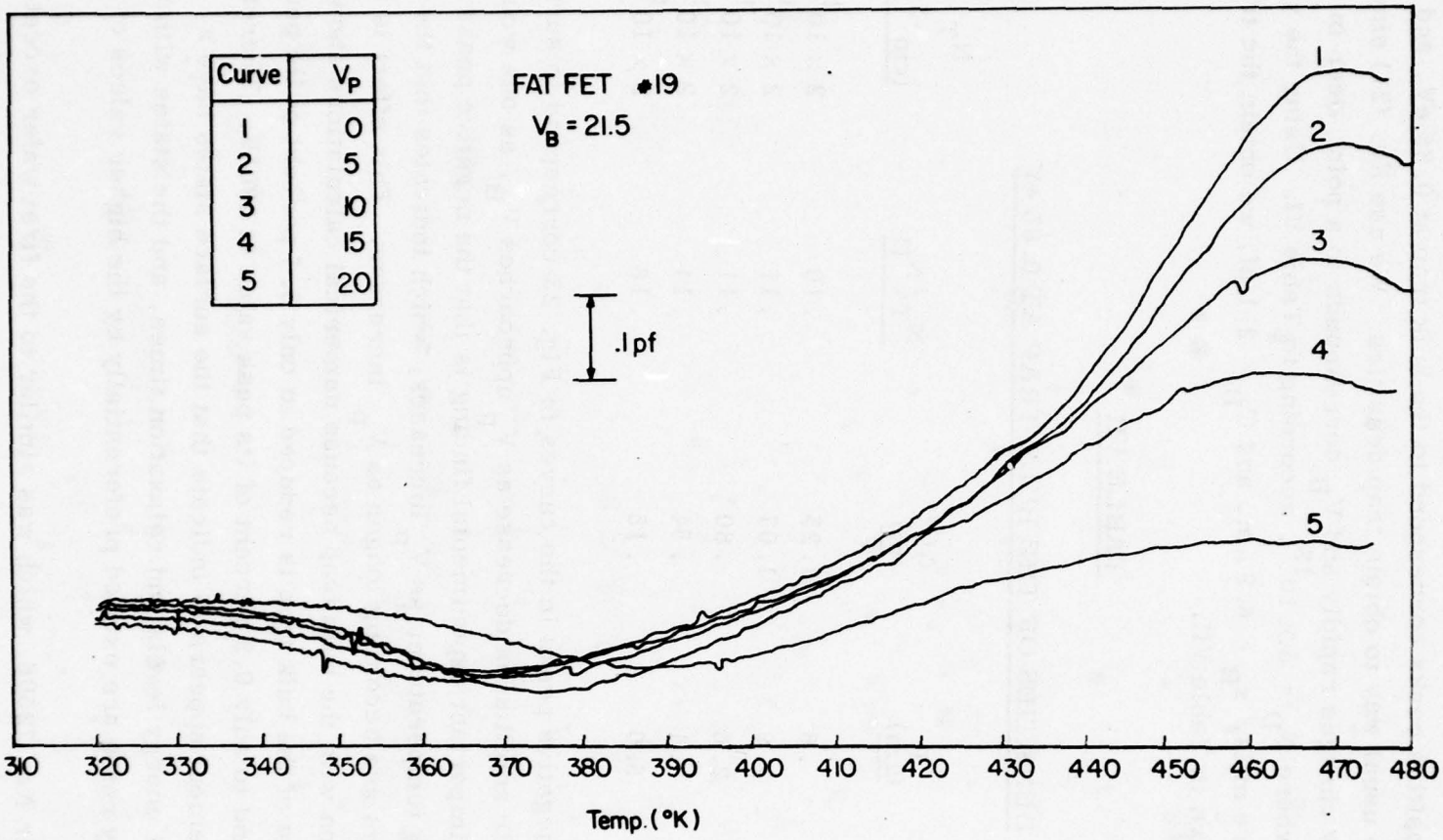


Figure 23 DLTS Temperature Sweeps for Various Values of V_p with V_B = 21.5V, t_1 = 40 μ s and x = 5 with T_p = 100 μ s. The positive peaks, corresponding to bulk traps, occur at the same temperature on each curve. The location of the negative peaks occurs at increasing temperatures as V_p increases.

The positive peaks correspond to the bulk trap at 0.85 eV, and can be used in the usual way to obtain trap densities. We use Eq. (21) since the doping density changes rapidly and V_B corresponds to a point deep in the buffer layer where $N_D = 5 \times 10^{13}$, according to Table VI. Using the values A = 200 square mils, $x_B = 6.9\,\mu m$, and $C_B = 2.1$ pf, we obtain the trap densities shown in Table VII.

TABLE VII

DENSITIES OF THE BULK TRAP AT 0.85 eV

V_p (volts)	x_p (μm)	ΔC (pf)	N_T/N_D	N_T (cm^{-3})
0	.6	1.25	.10	2×10^{14}
5	1.9	1.07	.11	2×10^{14}
10	2.6	.80	.11	2×10^{14}
15	3.4	.54	.14	2×10^{14}
20	5.0	.15	.16	2×10^{13}

The negative peaks in the curves in Fig. 23 correspond to surface states. Their amplitudes decrease as V_p approaches V_B, as one would expect. An important experimental finding is that the negative peaks occur at increasing temperatures as V_p increases, which indicates that the relaxation times are becoming longer as V_p increases. This effect is not due to competition with the bulk trap because numerical calculations showed that the amplitude of the bulk trap is reduced to only 3.4 percent of its peak value at 400 °K, and to only 0.8 percent of its peak value at 380°K. Therefore, this measurement appears to indicate that the surface states have a continuum of energy levels and relaxation times, and the states with the slower decay rates are excited preferentially by the higher values of V_p.

Wafer No. 72506, which was similar to the first wafer except that it was grown with a carbon-backed substitute, was also measured to the DLTS equipment. It had been hoped that the 200 Å carbon backing would

reduce the density of trap states but the measurements did indicate that there was little difference between the two wafers. Exact comparisons are difficult because both surface and bulk signatures are both much bigger when the depletion layer edge is at a low doping density and small changes in the C(V) curve can lead to an error in the calculated density in the low-doped buffer region. The relaxation times for both bulk and surface traps were nearly the same for both wafers, as indicated in Fig. 24.

4.3 Relationship of Anomalous Signatures to Surface States

In principle, the transient capacitance could be affected either by charge states at the interface under the gate or by mobile charge between gate and drain. In fact, the charge between gate and drain is undoubtedly important in operating FET's, but, for fat FET's, the gate length has been increased from 1 μ m to 10 mils, so that the 5 μ m between gate-and-source or gate-and-drain is much less important, as can be seen from Fig. 16. If we assume that the maximum likely effect of mobile surface charge on a capacitance measurement is to increase the effective gate length by 5 μm, then ΔC would not exceed about two percent of C_B. In fact, the surface effects increase C_B in Fig. 18 by about 14 percent. It is true that this large percentage change is a consequence of the depletion layer ending in the low-doped buffer zone where C_B is sensitive to small changes. However, this fact and our observation that ΔC is smaller when the depletion layer corresponding to V_B ends in a high-doped region suggest that the transient capacitance cannot be due to an effective increase in the gate area due to surface charges between the gate and the source-drain electrodes. Therefore we will consider whether surface states at the interface between the gate and the bulk GaAs can cause our transient capacitance.

A preliminary model is suggested by Fig. 25, where the dashed curve in Fig. 25a indicates schematically the density of surface states D(E) and the darkened area indicates that these states are filled up to Fermi level of the metal. If f is the Fermi occupation function, the negative surface charge for n-GaAs is

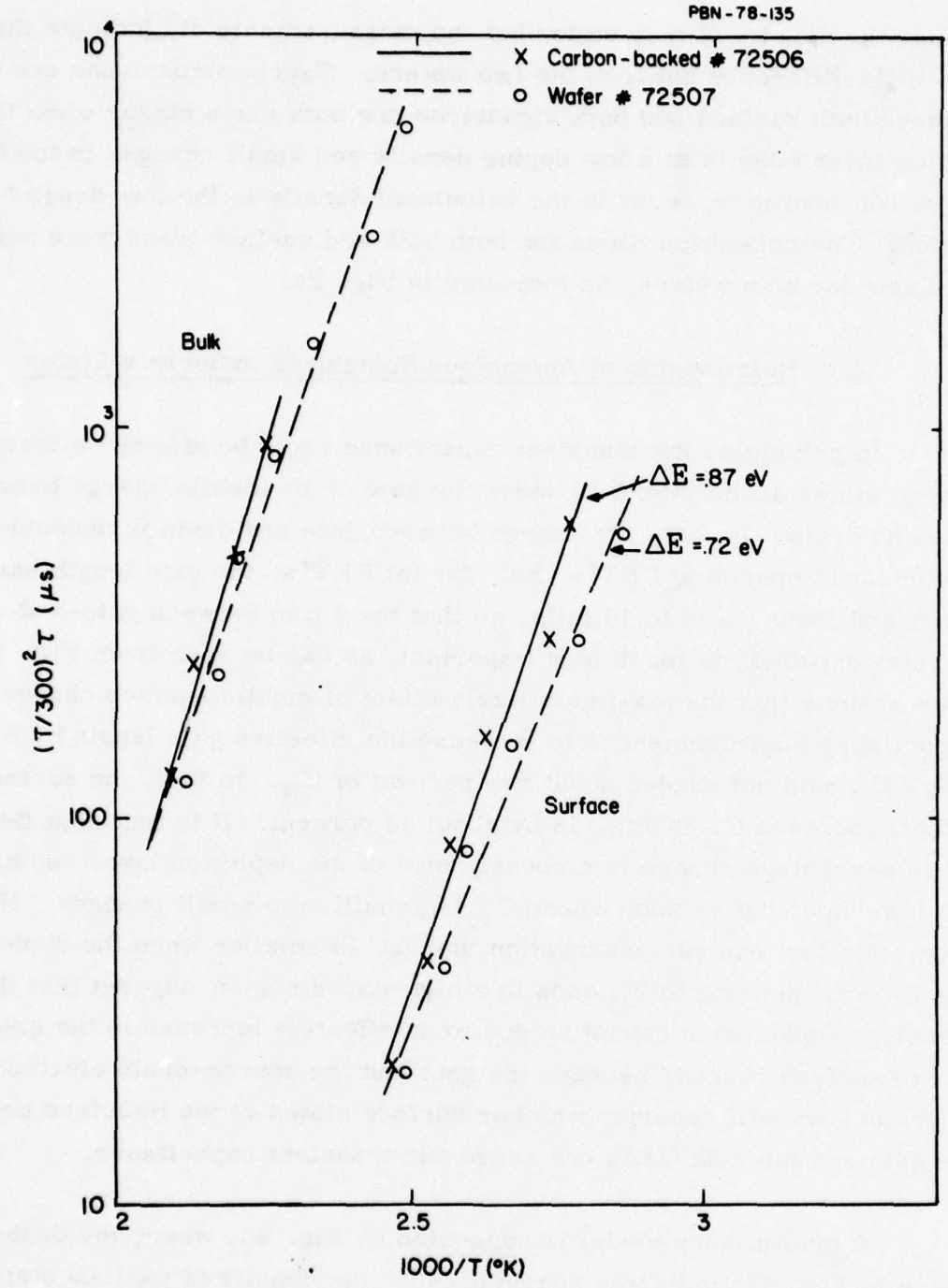


Figure 24 A Comparison of the Relaxation Times for Surface and Bulk Traps for the Test Wafer without a Carbon-Backed Substrate, No. 72507, and a Similar Carbon-Backed Wafer No. 72506. The upper bulk signature corresponds to the bulk trap at 0.85 eV which is associated with oxygen. Points were taken over a more limited range for the latter wafer which explains the slight difference in slope for the bulk trap.

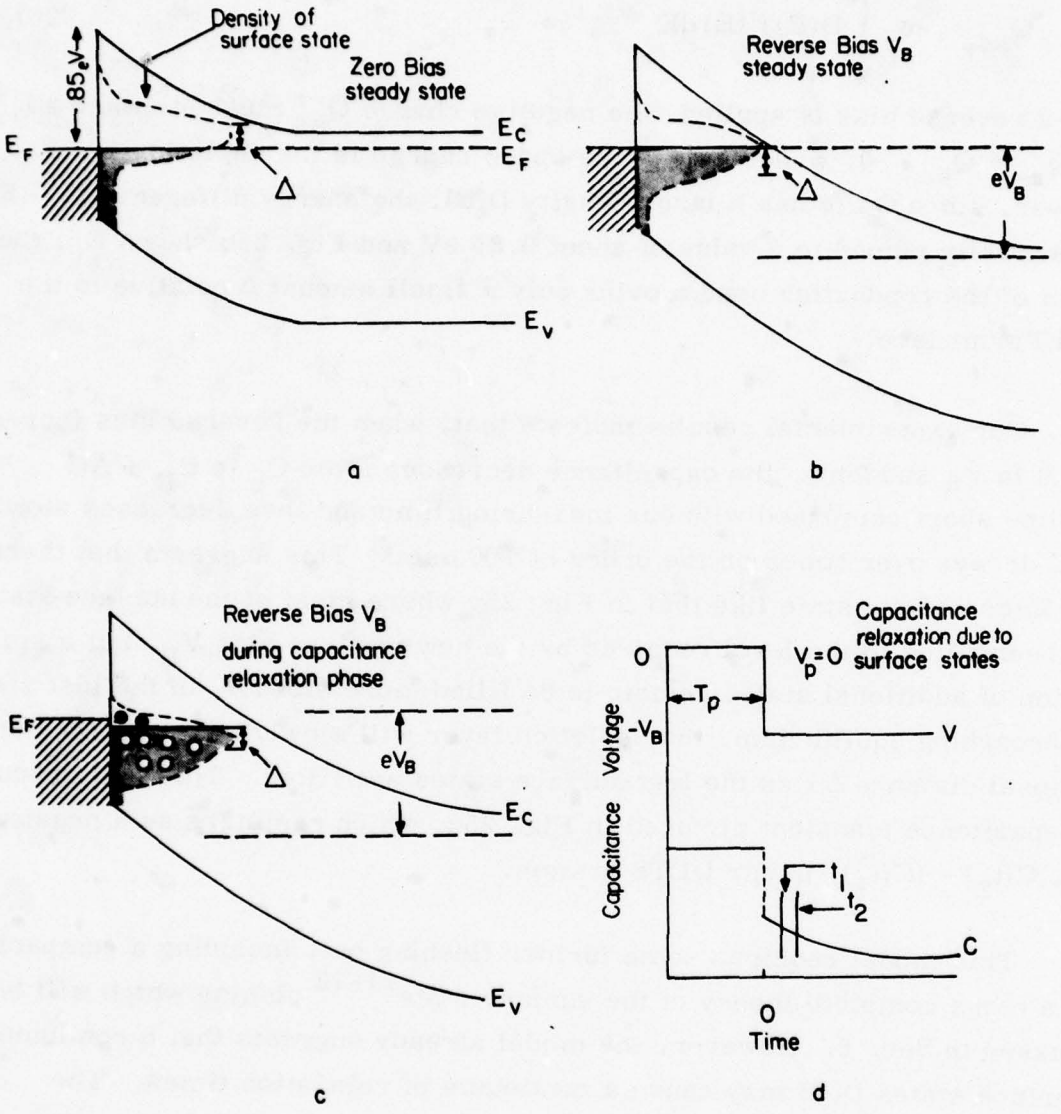


Figure 25 Energy Bands for Schottky Barriers with a Large Density of Surface States. (a) The zero bias equilibrium state has the Fermi level pinned by the high density of surface states so that the built-in potential is about .85V regardless of the barrier metal; (b) the equilibrium state for a reverse bias, V_B, has more surface states filled with electrons; (c) approximate conditions immediately after a jump from 0 to V_B while surface states are still being filled; (d) capacitance response to the situation in (c) showing the asymptotic approach to equilibrium.

$$Q_{ss} = -e \int D(E) f(E)\, dE \quad . \tag{28}$$

When a reverse bias is applied, the negative charge Q_{ss} must increase so that $Q_{ss} + Q_{sc} = 0$, where Q_{sc} is the space charge in the depletion layer. However, since GaAs has a large density D(E), the energy difference $E_c - E_f$ is essentially pinned to a value of about 0.85 eV and Fig. 25b shows E_c, the bottom of the conduction band moving only a small amount Δ relative to the metal Fermi level.

Our experimental results indicate that, when the reverse bias increases from 0 to V_B suddenly, the capacitance decreases from C_p to $C_B + \Delta C$ in a time short compared with our measuring time and then decreases slowly as ΔC decays over times on the order of 100 μsec. This suggests that there is an intermediate state like that in Fig. 25c where most of the surface states have been filled to the level required by the new reverse bias V_B, but a small fraction of additional states remain to be filled more slowly. In the last stages of approaching equilibrium, the depletion layer will slowly be moving out an additional distance Δx as the last surface states are filled. This will produce the capacitance transient pictured in Fig. 25d, which registers as a negative peak, $C(t_2) - (C(t_1)$, in our DLTS system.

This model requires some further fleshing out, including a comparison with a more complete theory of the surface state[11-12] pinning which will be discussed in Sec. 6. However, the model already suggests that a continuum of surface states D(E) may cause a continuum of relaxation times. The variation in relaxation times with voltages V_p, which appeared in the measurements of Fig. 23, may be a result of filling D(E) to different energy levels. Since Q_{sc} increases as the square root of the doping level N_D, an increase in doping level would require more states to be filled to give a larger negative charge Q_{ss} and therefore a larger signal. A short pulse time T_p might cause certain traps to be filled preferentially. Similarly, since the surface state density changes with the type of metal in the Schottky barrier, different transients and relaxation times may occur with different gate metallizations.

5.0 DETECTION OF SURFACE TRAPS IN NORMAL FET WAFERS

When DLTS measurements were applied to fat FET's on normal FET wafers with an active layer doping around $10^{17} cm^{-3}$, the bulk traps were difficult to detect because of the small ratio of trap density to doping density. However, surface traps were detected, as is indicated dramatically by the oscilloscope traces in Figs. 26 and 27, from measurements on the buffered wafer No. 82137.

In these pictures, the voltages are kept at 3 V for varying periods of times and then pulsed to 2 V with a switching time of less than 1 μsec. The capacitance transients are consistent with the schematic diagram in Fig. 20. The transients are noticeably slower when the voltage is switched from 3 to 2 V than they are when the voltage switches from 2 V to 3 V, as might be anticipated considering Fig. 22.

The upper pictures in Fig. 26 illustrate that 5 μsec is too short a time to allow the capacitance to reach its steady state value of 11.25 pfs, although the capture rate of bulk traps is so fast that the capture would appear instantaneous on these time scales. Therefore these traces are due to surface traps. In the pictures, the switching of the voltage from 2 to 3 V is not instantaneous but requires a fraction of a microsecond. (Both capacitance and voltage traces move downward as their values increase in these pictures.)

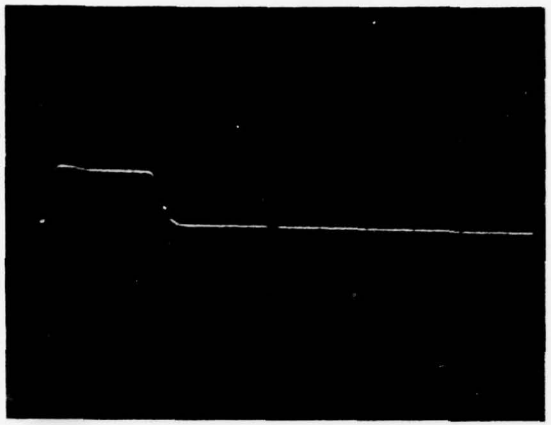
After the voltage switches to 3 V, the capacitance decays until it reaches its steady state value. Again, this is different from the behavior of a bulk trap which would cause the capacitance to overshoot its steady state value to some value less than 9.9 pfs and then slowly increase back to the steady state value as the trapped electrons within the depletion layer are released.

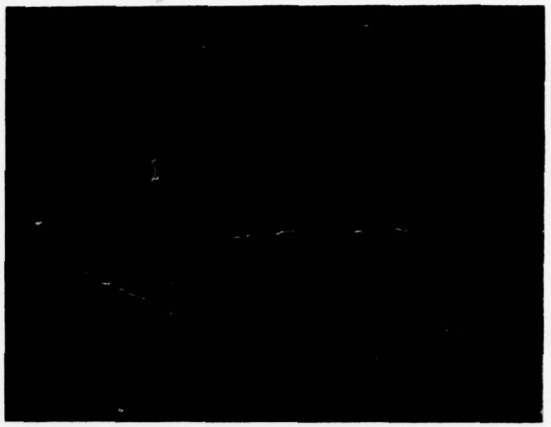
The remainder of the pictures in Figs. 26 and 27 show the results of increasing T_p, the length of the set pulse, from 5 μsec to 50 μsec to 500 μsec to 3 nsec, while simultaneously increasing the scale of the time

D.C. Pulse-Back: 3 to 2 Volts

Capacitance Pulse

5 μs Pulse
2 μs/ Div.
60 Hz Rate





50 μs Pulse
10 μs/ Div.
60 Hz Rate

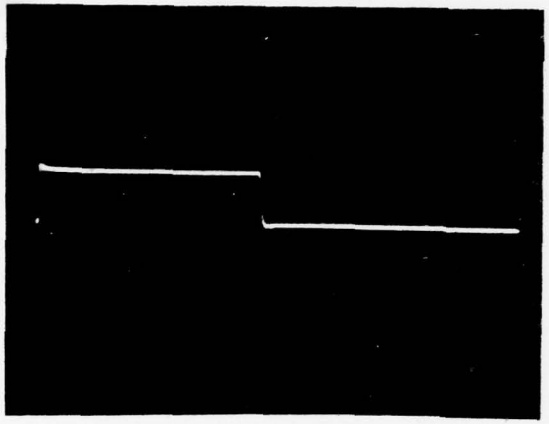
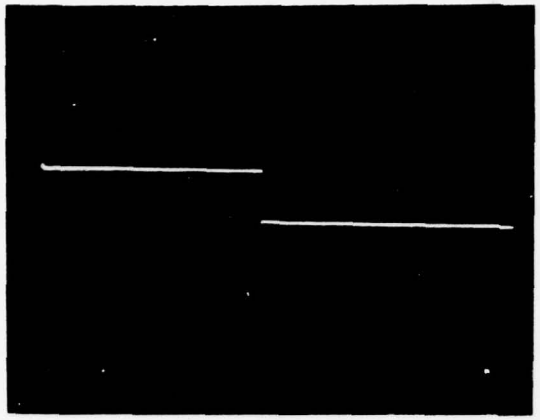


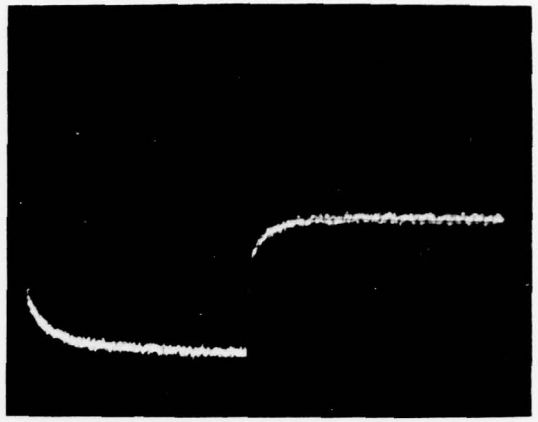
Figure 26 A Series of Oscilloscope Traces Showing the Transient Capacitance Responses when the Reverse Bias Voltage is Pulsed from 2 V to 3 V on a Fat FET, Wafer No. 82137. In the steady state these bias voltages produce capacitances of 11.25 pf and 9.9 pfs. In the top picture, the bias is held at 2 V for 5 μs and then switched to 3 V with a switching time of less than 1 μs. The capacitance does not reach steady state in 5 μs. In the bottom pictures the bias is held at 2 V for 10 μs.

D.C. Pulse-Back: 3 to 2 Volts

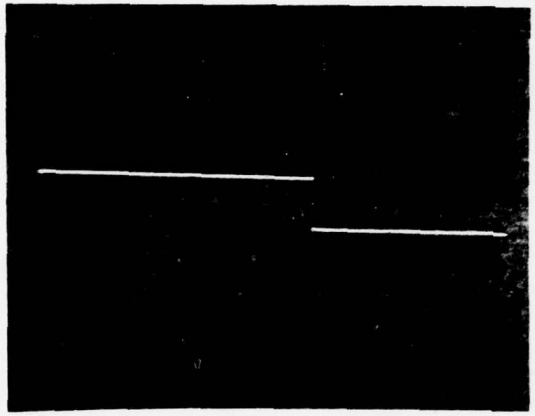
Capacitance Pulse

500 μs Pulse
100 μs/ Div.
60 Hz Rate





3 μs Pulse
500 μs/ Div.
60 Hz Rate



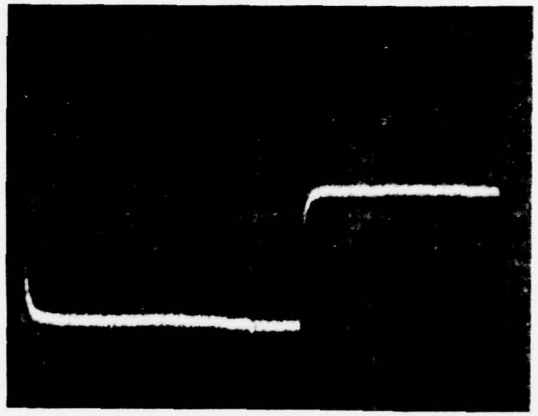


Figure 27 The Sequence of Fig. 26 is Continued, Increasing the Time during which the bias is held at 2 V to 500 μs in the Top Pictures and to 3 ms in the Bottom Pictures. The voltage switches discontinuously on these scales but the decay time is on the order of 50 μs after the bias switches from 3 to 2 V, and on the order of 30 μs after the bias switches back to 3 V.

trace on the oscilloscope. A visual estimate suggests that the e-folding time of the transient is about 50 μsec after switching to 2 V and about 30 μsec for a 3V bias.

5.1 Measurements on a Buffered Fat FET

A series of DLTS measurements were made on fat FET No. 12, fabricated from wafer No. 72449. The fat FET was similar to the sketch in Fig. 16 and had a gate area of 200 square mils, an active layer doping of $N_D = 1.1 \times 10^{17} cm^{-3}$, a thickness $h \simeq 0.29\ \mu m$, and a buffer layer thickness of 3.85 μm. The doping level as a function of x and V, as calculated from the C(V) plot measured directly on the device, is shown in Table VIII, along with the total space charge per unit area as a function of depth.

TABLE VIII

(Wafer # 72449)

V	C	Q	W	N_D
volts	pf	$C/cm^2 \times 10^{-8}$	μm	$1/cm^3 \times 10^{17}$
0	137	15.0	.10	1.1
.2	123	17.1	.12	1.1
.4	114	18.9	.13	1.2
1.0	94.3	23.7	.15	1.2
2.0	76.7	30.3	.19	1.2
3.0	65.9	35.8	.22	1.0
4.0	57.4	40.5	.25	.82
5.0	48.1	44.6	.30	.33

The DLTS curves in Fig. 28 show temperature sweeps with negative peaks for the four boxcar times t_1 = 10, 20, 40, and 80 μsec, with x = 5. Since T_p was only 80 μsec, the signal amplitude becomes smaller as t_1 is increased, as would be expected if the filling time is longer than t_1 at the temperature corresponding to the negative peak.

As with the test wafers discussed in Sec. 4, we use a reverse pulse to check the emission times for the surface states. The results show the strong signatures in Fig. 29 with the positive peaks that are typical of the surface state response to a reverse pulse. The emission times and capture times are both plotted in Fig. 30. The capture times fall along a single straight line in the same way that bulk traps do, but the emission times appear to satisfy a different relationship. The emission times, as they were obtained from the curves of Fig. 29, are listed in Table IX along with the temperature of the peaks of the curves.

TABLE IX

EMISSION TIMES FROM THE REVERSE PULSE

Curve	T_{max}, °K	τ, μsec	$(T/300)^2 \tau$, μsec
1	295	50	48
2	283	99	89
3	272	199	163
4	257	398	292
5	235	795	489
6	213	1590	800

Figure 31 shows a temperature sweep for t_1:t_2 = 10:50 μ sec over the entire temperature range from 90° to 475°K, covering most of the range between liquid nitrogen temperature to the temperature at which the solder on the device begins to melt. The valley at 308°K is the surface signature discussed above. In addition, there appears to be a slow surface trap which

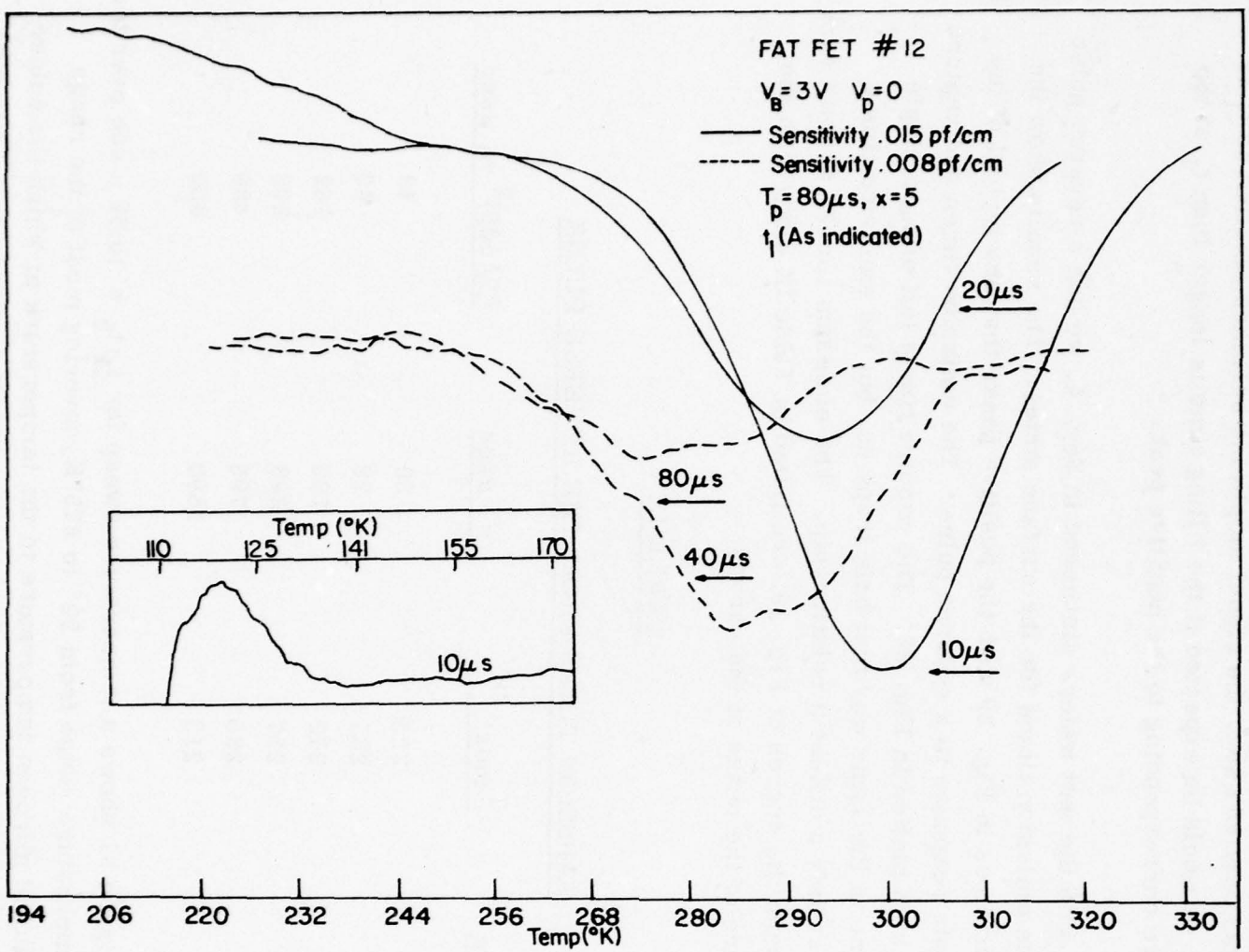


Figure 28 Surface Traps detected by DLTS Temperature Sweeps on a Normal FET. The insert, detected with the boxcar time t_1 set to 10 μs, shows a positive DLTS peak near 119°K, which corresponds to a bulk trap with an energy level 0.12 ± 0.03 eV below the conduction band.

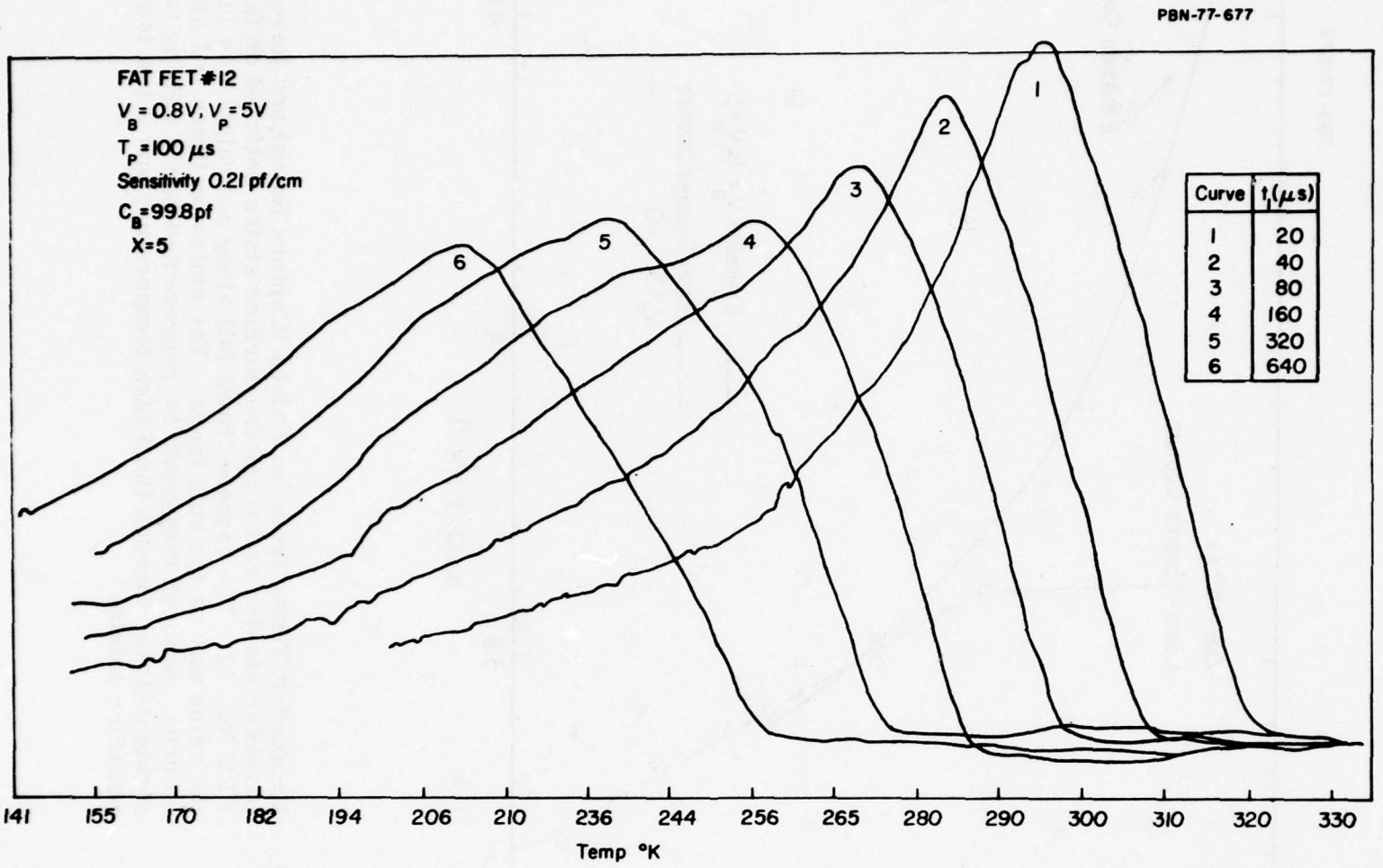


Figure 29 DLTS Signatures After a Reverse Pulse is Applied to Wafer No. 72449. There is no response from bulk traps to this type of pulse.

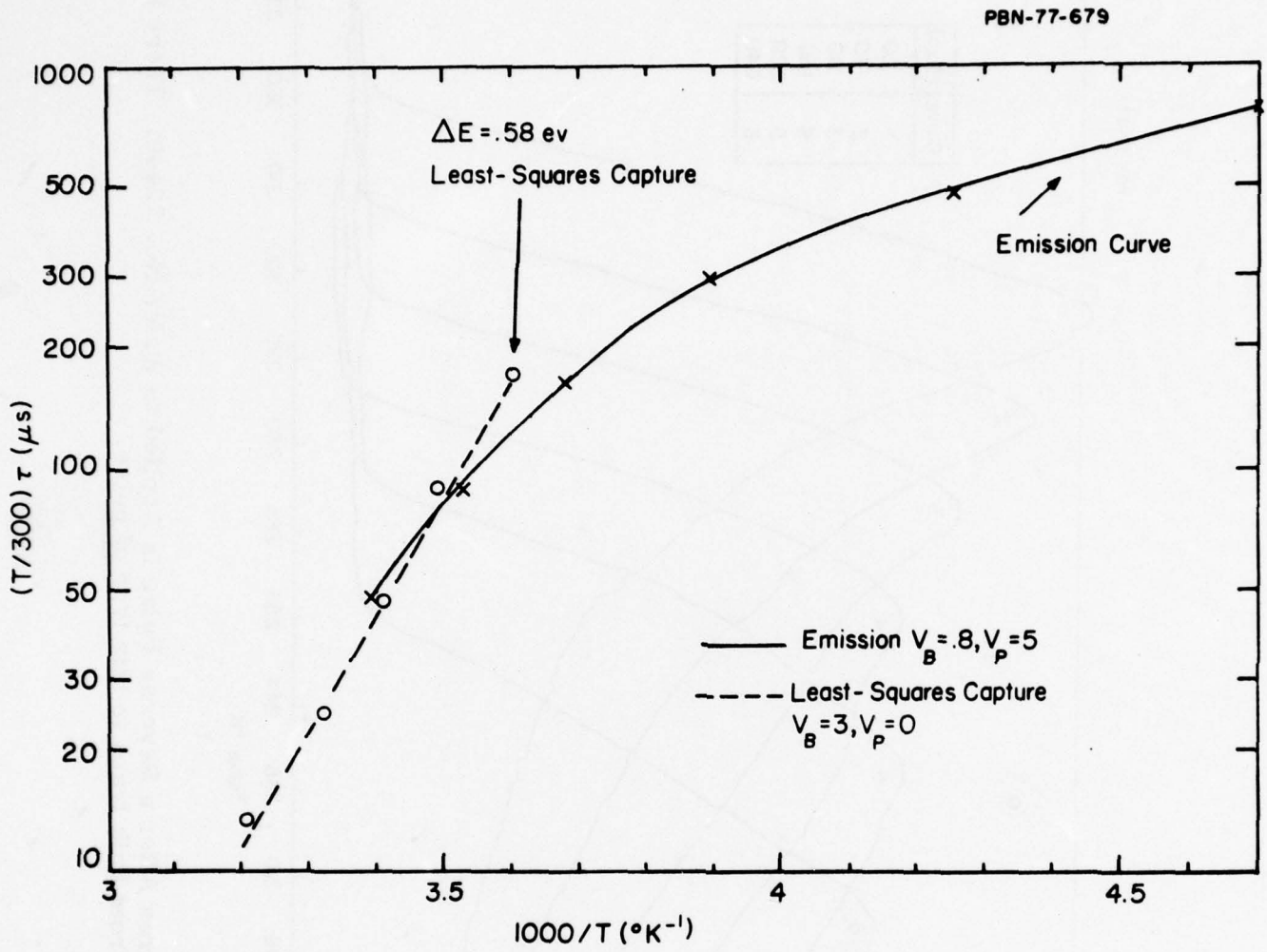


Figure 30 Relaxation Times from Set Pulses (Capture Rates) and Reverse pulses (emission rates) for the surface states detected on fat FET No. 12. The capture times fall along a straight line in the same way as for bulk traps. The emission times fall along a curve, although they could be represented fairly well by two straight lines, through the 3 high temperature and 3 low temperature points.

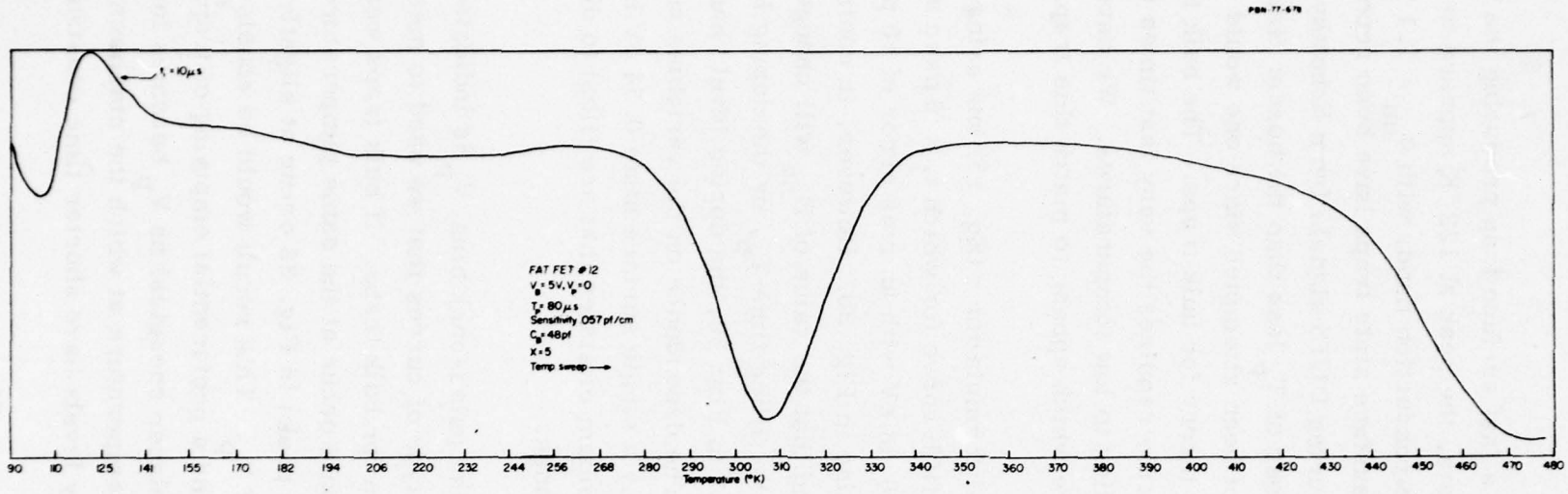


Figure 31 DLTS Sweep for a Temperature Sweep from 90° to 475°K. A peak from a bulk electron trap appears at 122°K. Valleys appear at 103°K, 308°K and 476°K.

produces a valley at 476°K and a fast surface trap producing the minimum at 103°K. Using other DLTS data, the peak at 122 °K appears to be a bulk electron trap 0.12 eV below the conduction band, with $\sigma_{na} = 1.1 \times 10^{-15}$. To our knowledge, none of the surface state traps have been reported previously by experimenters measuring DLTS signals from Schottky barriers, probably because they used values of T_p less than the boxcar times, or because reverse pulses have not been attempted since one would expect a null experiment on the basis of theory for bulk traps. The bulk trap at 122°K is very fast since it not only requires the very fast times of which our system is capable but also cooling to low temperatures. We have not found any traps listed in the literature which appear to match this trap.

On the basis of the usual formula for τ (Eq. 15) and using the four curves in Fig. 28 along with a fifth curve for which $t_1 = 5\,\mu$sec and $T_m = 312$°K, we obtain $E_{na} = 0.58$ eV with an rms error of 10 percent, producing the dashed straight line in Fig. 30. However, in contrast to the bulk trap results, we have found that the value of E_{na} will change when either the bias voltages such as V_p, the filling time T_p, or the doping level N_D changes. In going from Fig. 21 to Fig. 30, the doping level changes from about 2×10^{15} to 1.1×10^{17}. The dependence on the variables suggests that the signatures are not caused by a single surface state 0.58 eV below the conduction band, but by a continuum of states that are filled to different levels as these parameters change.

The effect of changing the pulse-back bias V_p is indicated in Fig. 32. These are the same type of curves that we used to measure trap density as a function of position for bulk traps. If bulk traps were causing these signatures, the peaks would occur at the same temperature for each curve. However, the negative peaks in Fig. 32 occur at slightly different temperatures for each value of V_p. This result would be consistent with a continuum of surface states, and a preferential emptying of traps with shorter decay times (and presumably higher energies) as V_p becomes larger. The direction of the change of the temperature at which the maximum occurs suggests that the higher energy levels have shorter time constants, as one

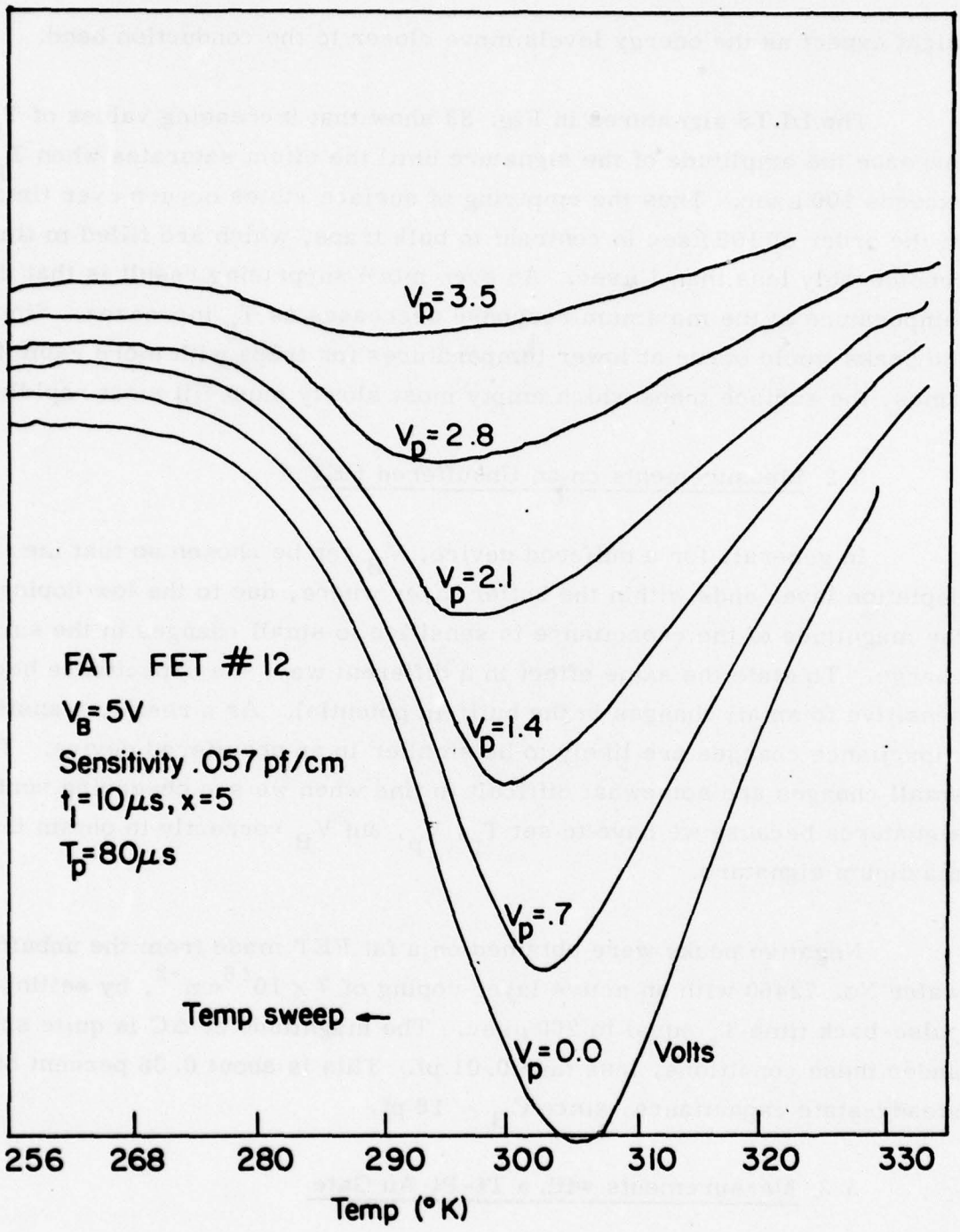


Figure 32 DLTS Signals after the Voltage is Pulsed back to Different Values of V_p with V_B fixed at 5 Volts. As the pulse-back voltage V_p approaches zero bias, more surface states are emptied as the signal amplitude increases. As V_p decreases, the maximum response occurs at higher temperatures indicating a different time constant.

might expect as the energy levels move closer to the conduction band.

The DLTS signatures in Fig. 33 show that increasing values of T_p increase the amplitude of the signature until the effect saturates when T_p exceeds 100 μsec. Thus the emptying of surface states occurs over times on the order of 100 μsec in contrast to bulk traps, which are filled in times considerably less than 1 μsec. An even more surprising result is that the temperature of the maximum response decreases as T_p increases. Since the peaks would occur at lower temperatures for traps with more rapid filling times, the surface traps which empty most slowly must fill most rapidly.

5.2 Measurements on an Unbuffered FET

In general, for a buffered device, V_B can be chosen so that the depletion layer ends within the buffer layer where, due to the low doping, the magnitude of the capacitance is sensitive to small changes in the surface charge. To state the same effect in a different way, the capacitance becomes sensitive to small changes in the built-in potential. As a result, transient capacitance changes are likely to be smaller in an unbuffered device. These small changes are somewhat difficult to find when we are observing surface signatures because we have to set T_p, V_p, anf V_B correctly to obtain the maximum signature.

Negative peaks were obtained on a fat FET made from the unbuffered wafer No. 72460 with an active layer doping of $7 \times 10^{16} cm^{-3}$, by setting the pulse-back time T_p equal to 200 μsec. The magnitude of ΔC is quite small under these conditions, less than 0.01 pf. This is about 0.06 percent of the steady-state capacitance, since C_B = 16 pf,

5.3 Measurements with a Ti-Pt-Au Gate

All previous measurements were made with gates consisting of 400 Å of chromium in contact with the GaAs, followed by 4000 Å of gold. The theory discussed in the next section suggests that the magnitude of these capacitance transients depended on the work function, ϕ_m, of the gate metal,

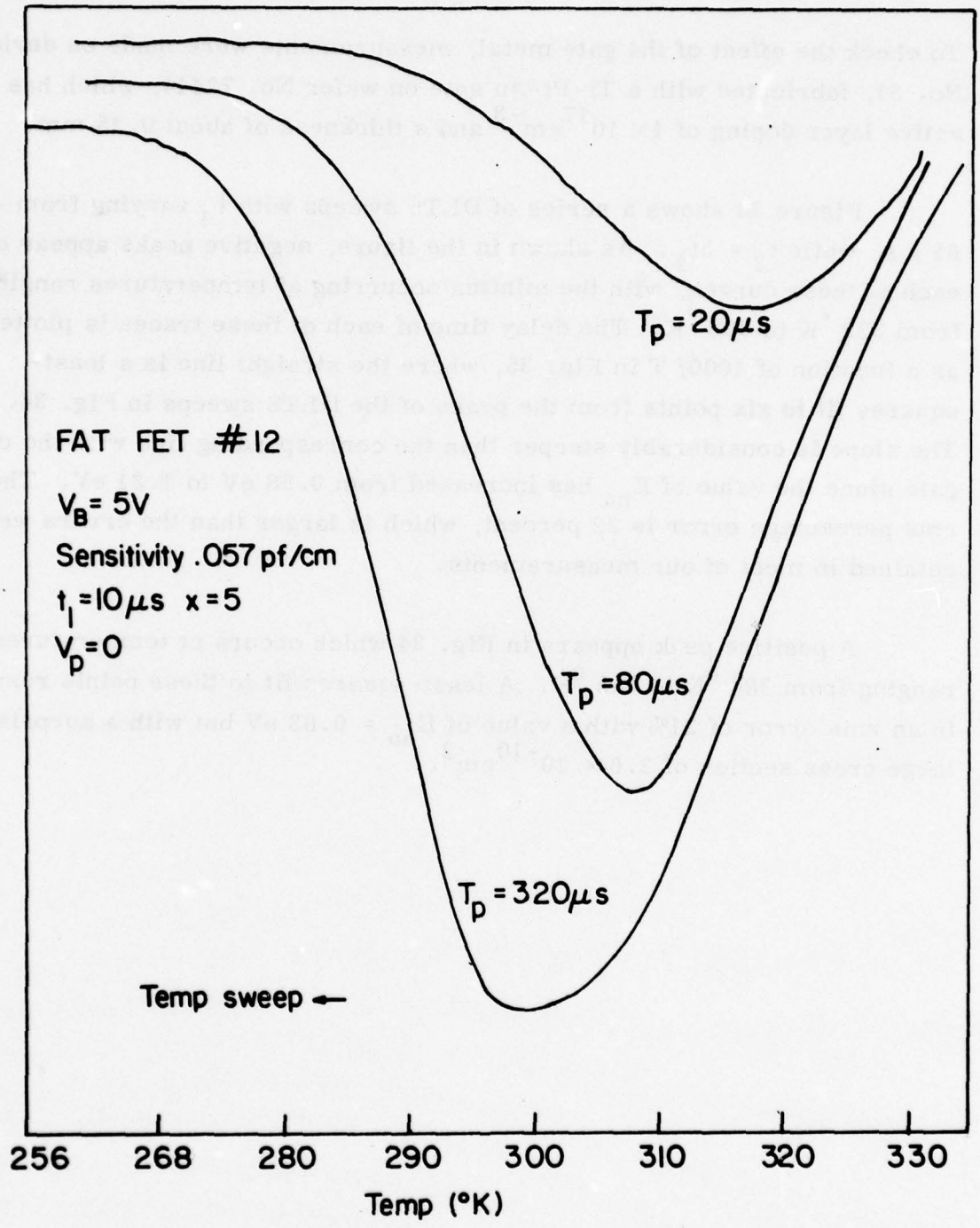


Figure 33 The Effect of increasing T_p in a Set Pulse. The surface states are slow to empty since they require about one hundred microseconds to reach full amplitude. There is a decrease in temperature of the peak response as T_p increases, suggesting that the trap states which are slowest to fill are the most rapid to empty.

To check the effect of the gate metal, measurements were made on device No. 31, fabricated with a Ti-Pt-Au gate on wafer No. 72444, which has an active layer doping of $1 \times 10^{17} cm^{-3}$ and a thickness of about 0.25 mm.

Figure 34 shows a series of DLTS sweeps with t_1 varying from 4 to 65 μ s, while $t_2 = 5t_1$. As shown in the figure, negative peaks appear on each of these curves, with the minima occurring at temperatures ranging from 322 °K to 306 °K. The delay time of each of these traces is plotted as a function of 1000/ T in Fig. 35, where the straight line is a least-squares fit to six points from the peaks of the DLTS sweeps in Fig. 34. The slope is considerably steeper than the corresponding line with the chrome gate since the value of E_{na} has increased from 0.58 eV to 1.31 eV. The rms percentage error is 22 percent, which is larger than the errors we have obtained in most of our measurements.

A positive peak appears in Fig. 34 which occurs at temperatures ranging from 384 °K to 345 °K. A least-squares fit to these points results in an rms error of 21% with a value of $E_{na} = 0.83$ eV but with a surprisingly large cross section of $2.6 \times 10^{-10} cm^2$.

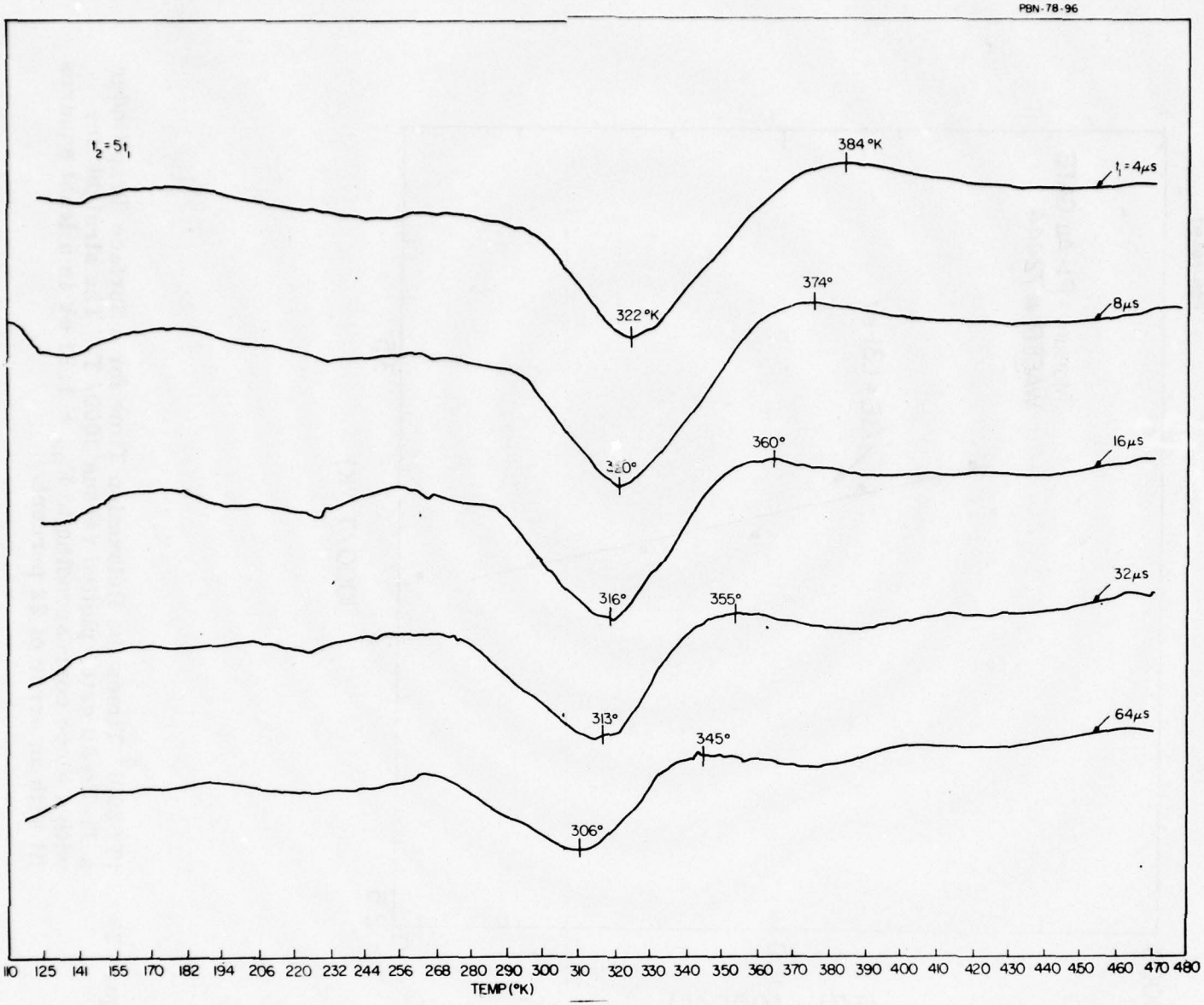


Figure 34 Five DLTS Temperature Sweeps are shown for a Ti-Pt-Au Gate on Wafer No. 72444 with the Specified Values for t_1 and t_2. The temperature of the negative peaks from surface traps and the positive peaks from a bulk trap are listed. Here T_p = 200 μs, V_B = 4V and V_p = 0.

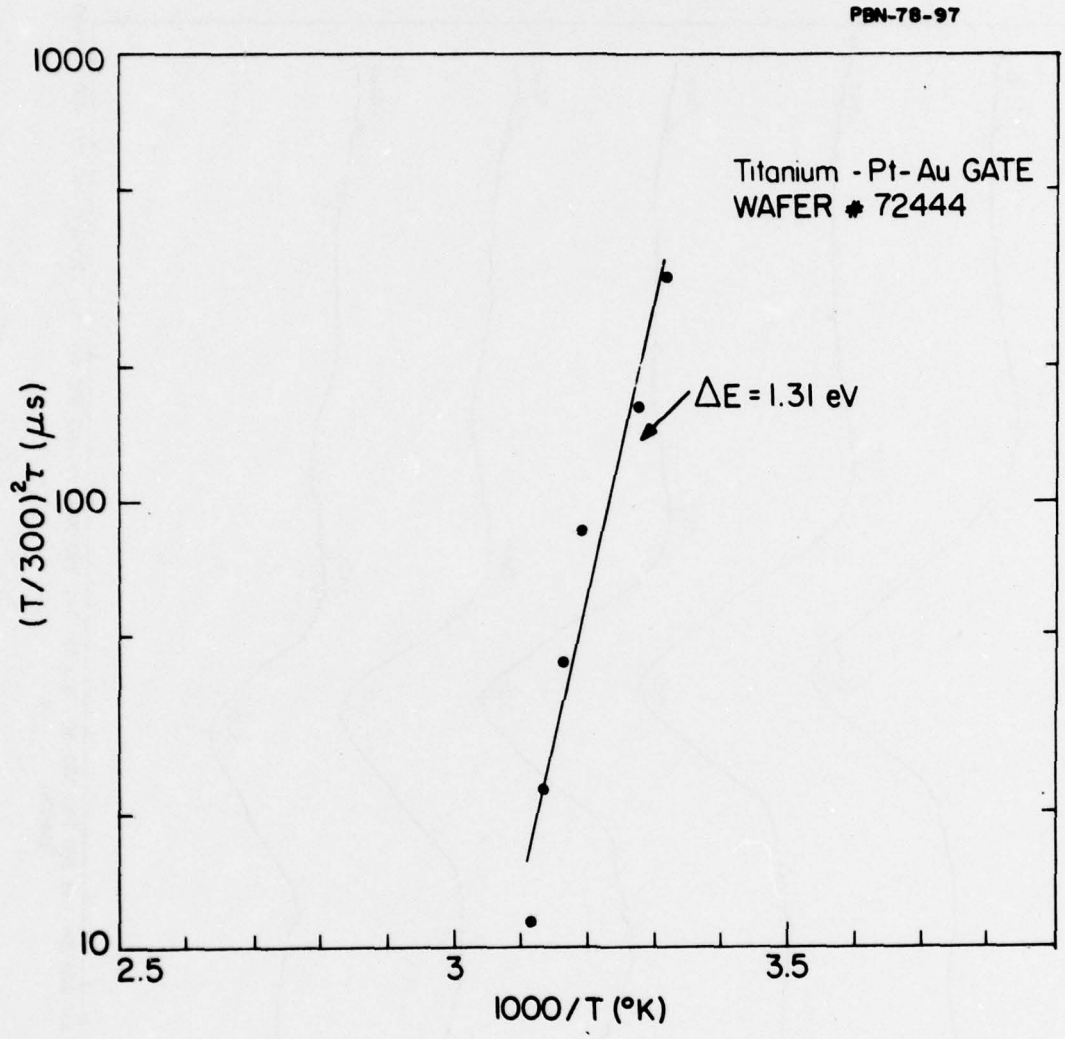


Figure 35 $(T/300)^2$ Times the Relaxation Time for a Surface Trap Under a Ti-Pt-Au gate, plotted versus 1000/ T. The straight line with a slope corresponding to E_{na} = 1.31 eV is a least squares fit with an error of 22 percent.

6.0 THEORETICAL MODEL OF THE SURFACE STATES

In this section we will relate the transient capacitance charge to the change in the occupation of surface states at the GaAs-gate interface. This model is closely related to a model of Cowley and Sze[11, 12] which explains why the built-in voltage is almost independent of the work function of the metal used as a Schottby barrier on a semiconductor with a high density of surface states, such as GaAs.

A schematic diagram of the semiconductor, shown in Fig. 36, includes both bulk electron traps in the interior of the semiconductor and surface states at the interface. The interface is pictured as a thin oxide or insulating layer separating surface states in the semiconductor, with charge Q_{SS}, from a charge, Q_M, at the metal surface. The insulating layer has a thickness δ across which a potential drop Δ is produced.

When the reverse bias applied to the semiconductor changes, the positive space charge in the depletion layer Q_{SC} changes in the usual way. To maintain charge neutrality Q_{SS} and Q_M must change also, which alters the balance of forces in the interfacial layer. Even in the limit of zero bias, to which Cowley and Sze restricted themselves, the charge densities Q_M and Q_{SS} have not been evaluated numerically in the published paper,[11] so we will discuss the zero bias case first.

6.1 The Interfacial Layer for Zero Bias

Cowley and Sze introduce five equations. The first results from charge neutrality:

$$Q_M + Q_{SS} + Q_{SC} = 0. \tag{29}$$

The space charge per unit area in the depletion layer, which we will calculate only for the case where the doping density N_D is uniform, is given by

$$Q_{SC} = \sqrt{2\epsilon q N_D \left(\phi_{Bn} - V_N - k\,T/q \right)} \tag{30}$$

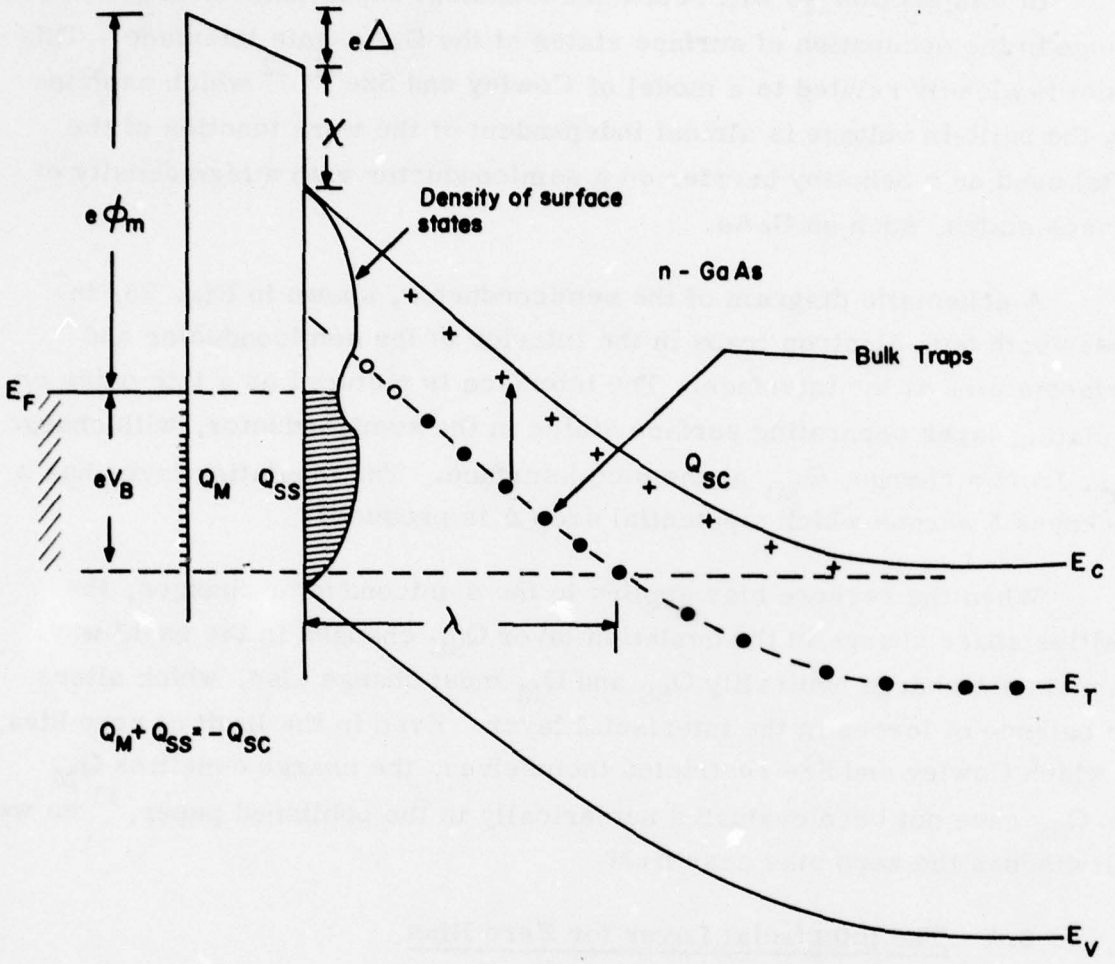


Figure 36 Schematic Diagram of Electron Trapping in the Surface States and in the bulk of the semiconductor. E_F is the Fermi level in the metal and V_B is an applied reverse bias. E_T is the bulk trap energy, λ is the distance to the point where the bulk trap level crosses the Fermi level, χ is the electron affinity, ϕ_m is the metal work function and Δ is the potential drop across the interfacial layer.

The barrier height is

$$\phi_{Bn} = \phi_m - \chi - \Delta. \tag{31}$$

From Gauss' law, the voltage drop across the insulator is

$$\Delta = -Q_M (\delta / \epsilon_i) \tag{32}$$

The surface state charge, given by the fact that all states below the Fermi level are filled, is

$$Q_{SS} = -q D_s (E_{gap} - q\phi_o - q\phi_{Bn}). \tag{33}$$

Here we have neglected the image force lowering of the barrier voltage, since it is not only small but immaterial to the built-in voltage. Both V_n, the voltage difference between the Fermi level and the bottom of the conductor band, and kT/q are on the order of 0.02 and could be neglected for our purposes. D_s is the density of quantum states per unit area in units of m^{-2} joule $^{-1}$, taken as a constant equal to its value at the neutral point $q\phi_o$ in the energy spectrum of the surface states. ϕ_m is the work function of the gate metal and χ is the electron affinity. The results are not very sensitive to the values of D_s or δ/ϵ_i where δ is the thickness of the insulating layer and ϵ_i is the effective dielectric constant of the insulating layer.

There are 5 unknowns in the 5 equations of Figs. (29) to (33). We have found two useful schemes of elimination. In the first we eliminate ϕ_{Bn} Q_{SC}, Q_M, and Q_{SS} to obtain the equation

$$\Delta = \left(-k_1 + \sqrt{k_2 - 2\epsilon q N_D \Delta} \right) / k_3 \tag{34}$$

where the k's have known values given by

$$k_1 = q D_s (E_{gap} - q(\phi_o + \phi_m - \chi)),$$

$$k_2 = 2\epsilon q N_D (\phi_m - \chi - V_n - kT/q),$$

and

$$k_3 = \epsilon_i/\delta + q^2 D_s.$$

Equation (34) has been written in a form particularly useful for an iterative solution since the effect of the term involving Δ on the right-hand side is small.

Another useful form is obtained by eliminating Δ and ϕ_{Bn} to obtain the following equations for the charge densities:

$$Q_M = -(Q_{SS} + Q_{SC}), \tag{35}$$

$$Q_{SC} = \sqrt{2 \epsilon q N_D (\phi_m - \chi - V_n - kT/q + Q_M \delta/\epsilon_i)}, \tag{36}$$

and

$$Q_{SS} = -q D_s (E_{gap} - q(\phi_m - \chi + \phi_o) - q \delta Q_M/\epsilon_i). \tag{37}$$

In solving these equations, we used the parameters given by Sze for GaAs as listed in Table X.

TABLE X

INTERFACE PARAMETERS FOR GaAs

ϵ_s fd-cm-1	δ/ϵ_i (cm^2 fd^{-1})	E_{gap}/q (Volts)	ϕ_o (Volts)	D_s (cm^{-2} eV^{-1})	χ (Volts)
1.1×10^{-12}	6.6×10^5	1.43	0.53	12.5×10^{-13}	4.07

The solution of these equations is plotted in Fig. 37 as a function of $\phi_m - \chi$, for $N_D = 1.1 \times 10^{17}$/cc. First, we note that the barrier voltage is nearly constant, increasing from 0.87 to 0.93V over the entire range of work functions which is in agreement with experiment.

Most of our experiments used chromium gates, and the chromium work function is about 4.60, which falls at 0.53 on the abscissa of Fig. 37. Here we note that Q_M is more than twice the space charge Q_{SC}, and therefore the electric field in the insulating layer is much stronger and in the opposite direction from the field in the semiconductor. The total interfacial charge, Q_M and Q_{SS}, is always positive, of course. We have followed Cowley and Sze's notation [11-12] in letting Δ be positive when it represents a decrease in voltage in going from metal to semiconductor, but for most metals this convention makes Δ negative since Q_M is positive.

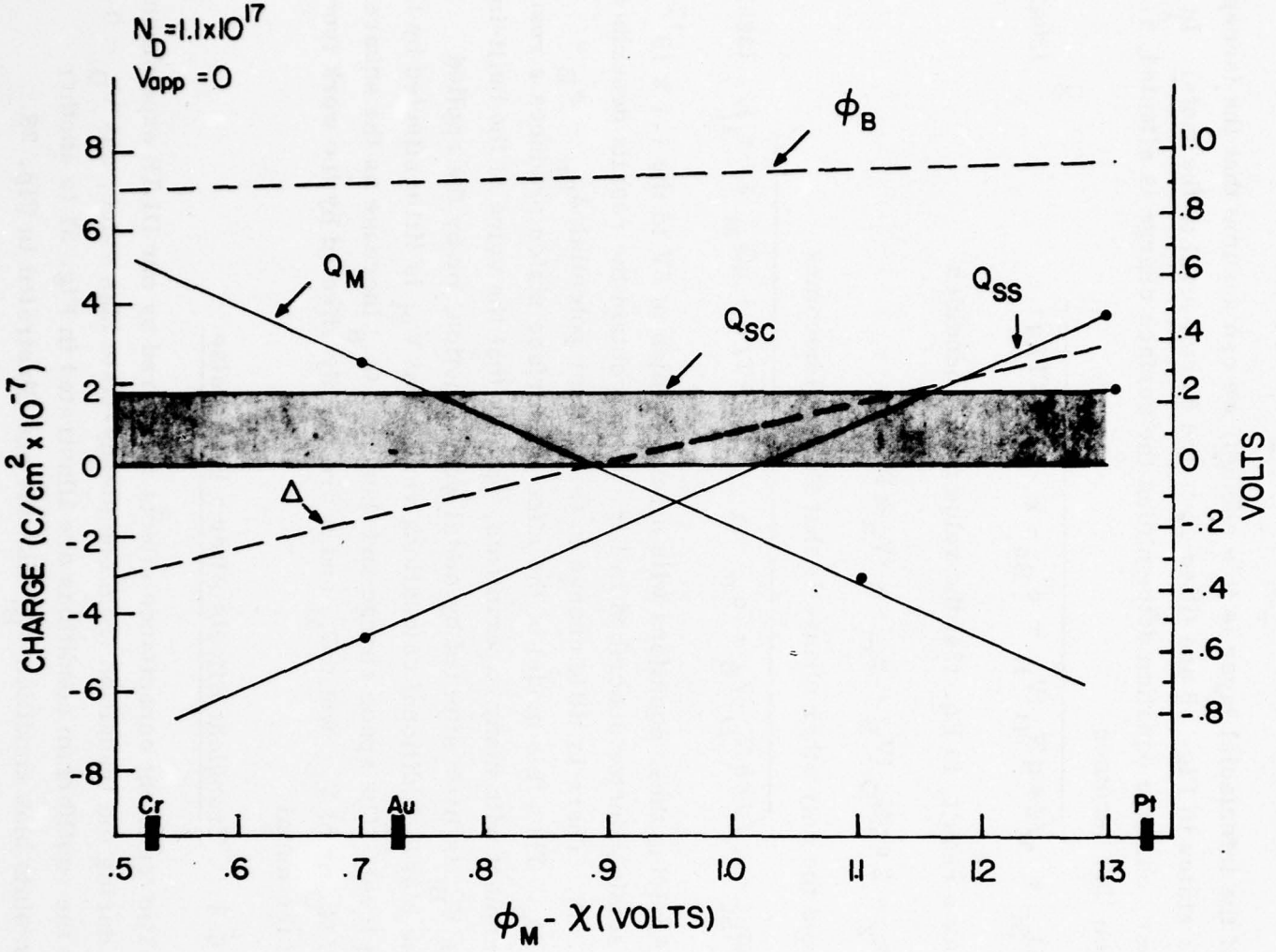


Figure 37 Values of the Charge Densities Q_{SC}, Q_M and Q_{SS} (solid lines) and Barrier Voltage ϕ_B and Interface Voltage Δ (dashed lines) as a Function of $\phi_m - \chi$ for Zero Applied Voltage with $N_D = 1.1 \times 10^{17}$/ cc, Corresponding to a Typical FET.

6.2 The Interfacial Layer with an Applied Bias

If the interfacial layer is thin enough, we can assume that the (acceptor) surface states in Fig. 36 are filled up to the Fermi level of the metal. In that case, only the equation determining the surface charge is affected, i.e., Equation (30) becomes

$$Q_{SC} = \sqrt{2 \epsilon q N_D (V_B + \phi_{Bn} - \chi - V_n - kT/q)}. \qquad (30a)$$

As a result, in Eq. (34) the value for k_2 becomes

$$k_2 = 2 \epsilon q N_D (V_B + \phi_m - \chi - V_n - kT/q)$$

and the only other change is that Eq. (36) becomes

$$Q_{SC} = \sqrt{2 \epsilon q N_D (V_B + \phi_m - \chi - V_n - kT/q + qQ_M \delta / \epsilon_i)}. \qquad (36a)$$

Applying these equations with a reverse bias of 5V to the 1.1×10^{17}/cc doped semiconductor described in Fig. 37, we obtain the results described in Fig. 38. There is little change in the barrier potential $\phi_{Bn} = \phi_B = V_{BI} + V_n$. Thus this model of the effect of surface states produces a result in agreement with many experiments, namely that the value of the built-in voltage V_{BI} is little affected by metal work function, or by the applied reverse bias. Additional calcuations verify that V_{BI} is little affected by the doping level. The space charge and therefore Q_{SS} increase as the square root of N_D or of V_B, while Q_M and Δ are mainly affected by the work function of the metal.

6.3 Transient Effects After a Bias Pulse

The transient capacitance effects measured by our DLTS experiment occur during the transition from one steady-state bias value, say $V_D = 0$ where the equilibrium conditions are illustrated in Fig. 37 to another steady-state bias condition V_B, like the one illustrated in Fig. 38.

After switching from 0 to V_B, the negative charge Q_{SS} in surface states increases to counteract the increased positive space charge in the

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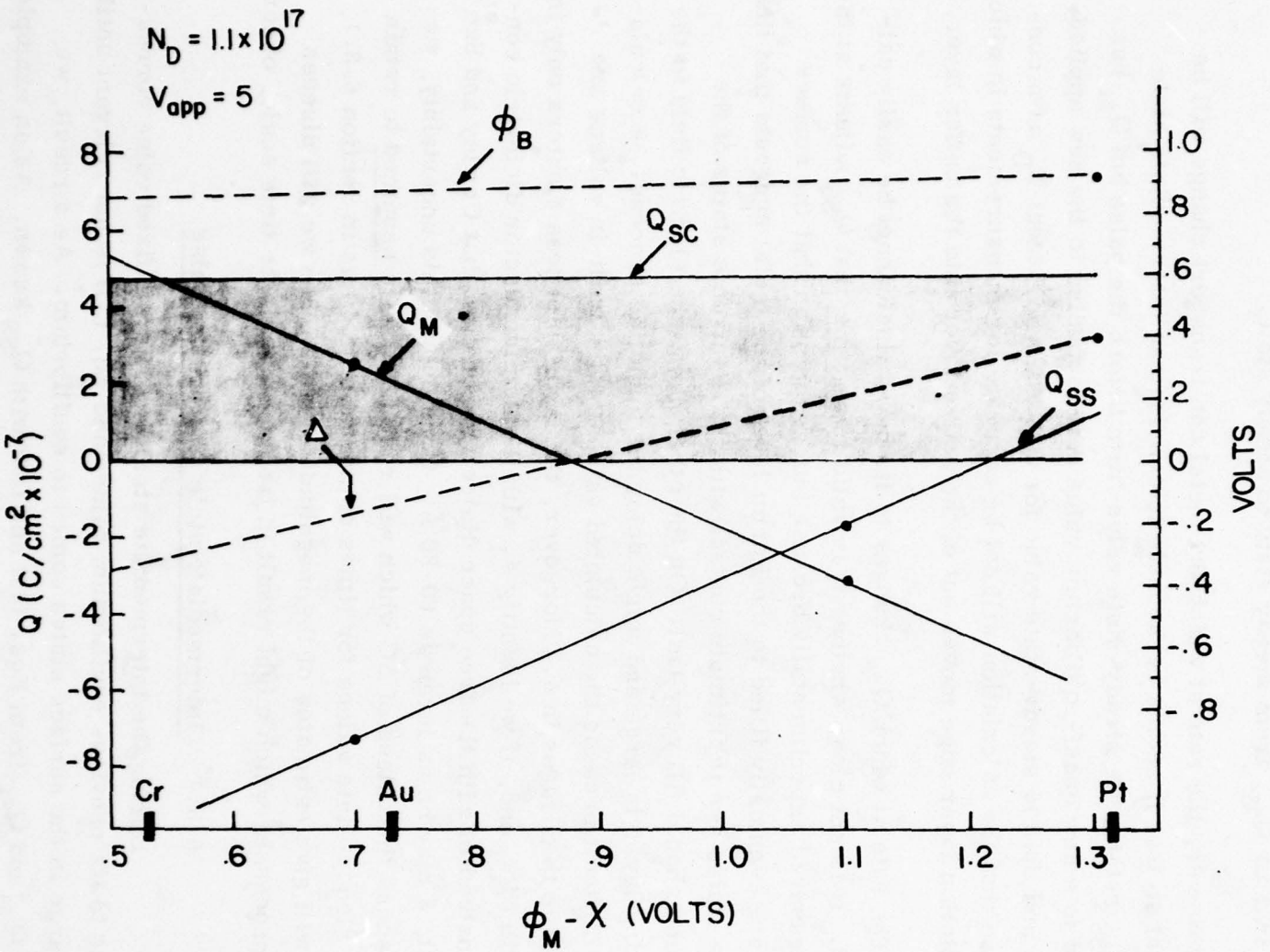

Figure 38 The Effect of Applying a 5 Volt Reverse Bias to the Metal Semiconductor Surface in Fig. 37.

expanded depletion layer. Since there is little change in V_{BI}, there is little change in Δ or Q_M, from steady state to steady state.

However, the rate at which the metal can transport change will be very fast so that it seems reasonable to consider an intermediate state when Q_{SS} retains its steady-state value from before the pulse but Q_M has changed to a new quasi-equilibrium value corresponding to the new applied voltage and the old steady-state value for Q_{SS}. We will treat N_D as a constant, so that the calculation will not be accurate for measurements in which the depletion layer edge moves out of the active layer into the buffer layer.

The rate at which Q_{SS} changes to its new value cannot be easily calculated. It is not clear whether it is valid to <u>assume</u> that Q_{SS} adjusts at the rate measured experimentally because our assumption that the surface states are eventually filled to the Fermi level of the metal suggests that the surface states are in intimate contact with the electronic states of the metal and should fill very fast. On the other hand, the electric field in the insulating layer is large and might delay the tunneling process. A calculation is difficult because the calculated values of the built-in voltage are insensitive to changes in δ. Moreover, the layer thickness δ enters only in the ratio δ/ϵ_i and, if we identify ϵ_i with the semiconductor dielectric constant instead of with the free space dielectric constant that Cowley and Sze[11] suggest, δ may be as large as 60-80 Å. Considering this uncertainty, we will discuss the values of ΔC which will result if Q_{SS} is <u>assumed</u> to retain its old steady-state values for times comparable to 10 μs in Section 6.3.1, which will give estimates of the magnitude of ΔC. Then we will discuss other processes which might result in transients with the time scales observed.

6.3.1 Intermediate state after a bias pulse

During the intermediate state Q_{SS} has the fixed value corresponding to its previous equilibrium value, and Eq. (33) is not relevant until the charge in the surface states comes to equilibrium. As a result, we obtain Q_M and Q_{SC} from Eqs. (35) and (36) with Q_{SS} known. As an example of the calculated results, we show in Table XI the intermediate state after the bias has switched from 0 to 5V, where the steady states are illustrated in Figs. 37 and 38.

TABLE XI

CHARACTERISTICS OF STEADY STATE AND INTERMEDIATE STATE

Quantity	Initial State	Inter-Mediate State	Final State
Bias Voltage (volts)	0	5	5
Δ (volts)	-.33	-.14	-.32
Capacitance (pf)	141	53.7	52.9
$E_F - q\phi_o$ (eV)	.034	.226	.048
Q_M (cm^{-2})	3.2×10^{12}	1.4×10^{12}	3.0×10^{12}
Q_{SS} (cm^{-2})	-4.3×10^{12}	-4.3×10^{12}	-6.0×10^{12}
V_{BI} (volts)	.85	.65	.83

The capacitance drop from the intermediate state to the final state is calculated as -0.8 pf in Table XI. The measured capacitance drop, estimated from Fig. 32, is ΔC = 1.2 pf. One may expect a somewhat larger capacitance experimentally because Table VIII shows that 5V put the edge of the depletion zone part way into the buffer layer, where $N_D = 3.3 \times 10^{16}$/ cc. As indicated by Table XI, the decrease in capacitance is accompanied by a transient increase in V_{BI} from 0.65 to 0.83V. Several other measurements are summarized in Table XII, including the assumed value of N_D in the calculation of the intermediate state.

TABLE XII

EXPERIMENTAL AND MEASURED TRANSIENT CAPACITANCE

Wafer No.	N_D (cm^{-3})	V_P (volts)	V_B (volts)	ΔC (calculated)	ΔC (measured)
72449	1.1×10^{17}	0	5	-.8pf	-1.2pf
72449	1.1×10^{17}	.7	5	-.7	-1.0
72449	1.1×10^{17}	1.4	5	-.5	-.7
72449	1.1×10^{17}	2.1	5	-.4	-.5
72449	1.1×10^{17}	2.8	5	-.3	-.2
72449	1.1×10^{17}	3.5	5	-.2	-.1
72449	1.1×10^{17}	0	3	-1.1	-.3
72449	1.1×10^{17}	5	.8	+4.0	+6.4
72449	1.1×10^{17}	4	.8	3.2	5.2
72449	1.1×10^{17}	3	.8	2.4	4.1
72507	1.8×10^{15}	0	4	-.016	<-.008
72507	1.8×10^{15}	0	20	-.005	-.64
72507	1.8×10^{15}	20	0	.61	.34

The agreement between measured and calculated results is generally very good. The only large discrepancy is for wafer No. 72507 when $V_P = 0$ and $V_B = 20$. Part of the discrepancy is due to the fact that the depletion edge for $V_B = 20$ is in the buffer layer where the doping is reduced to 1.8×10^{14}/ cc according to Table VI, which tends to increase the measured transient capacitance.

6.3.2 Possible transient effects

Although the transient capacitances calculated in Table XII agree reasonably well in direction and magnitude with the experimental results, it is not clear whether it is reasonable to assume that the surface states require 10 - 100 μs to reach equilibrium. In this section we want to

suggest that the high electric field at the surface of the semiconductor and the interfacial layer might cause transient effects of the order observed. A surface charge about on the order of 5×10^{-7} C/ cm^2, such as shown in Fig. 38, can cause fields on the order of 4×10^5 V/ cm, which might easily cause changes in the density of states D_s or neutral energy $q\phi_o$ or cause motion of mobile charge within the interfacial layer which could change the effective value of the dielectric constant ϵ_i.

The effect of a change in the density of states D_s can be seen from Fig. 39, where we have plotted the potential drop Δ as a function of (D_s / D_s^o), where D_s^o is the most likely value, taken from Table X. From Table XI, a change in Δ of 0.18 is enough to explain the transient capacitance for $N_D = 1.1 \times 10^{17}$ / cc. A smaller change in Δ occurs for lower doping densities. From Fig. 39, a change of the order of -0.1 volts would occur if D_s increased by a factor of 3 under the influence of the increased electric field indicated by the space charge shown in Fig. 38, which would have the right sign and magnitude to explain the observed transient capacitance.

Another method in which the balance of charges could slowly change is by means of the slow diffusion of mobile charges existing within the insulating layer. In this case the time scale would be δ^2 / D, where D is a diffusion constant which may have an activation energy to give it the exponential behavior found experimentally in Figs. 30 and 35.

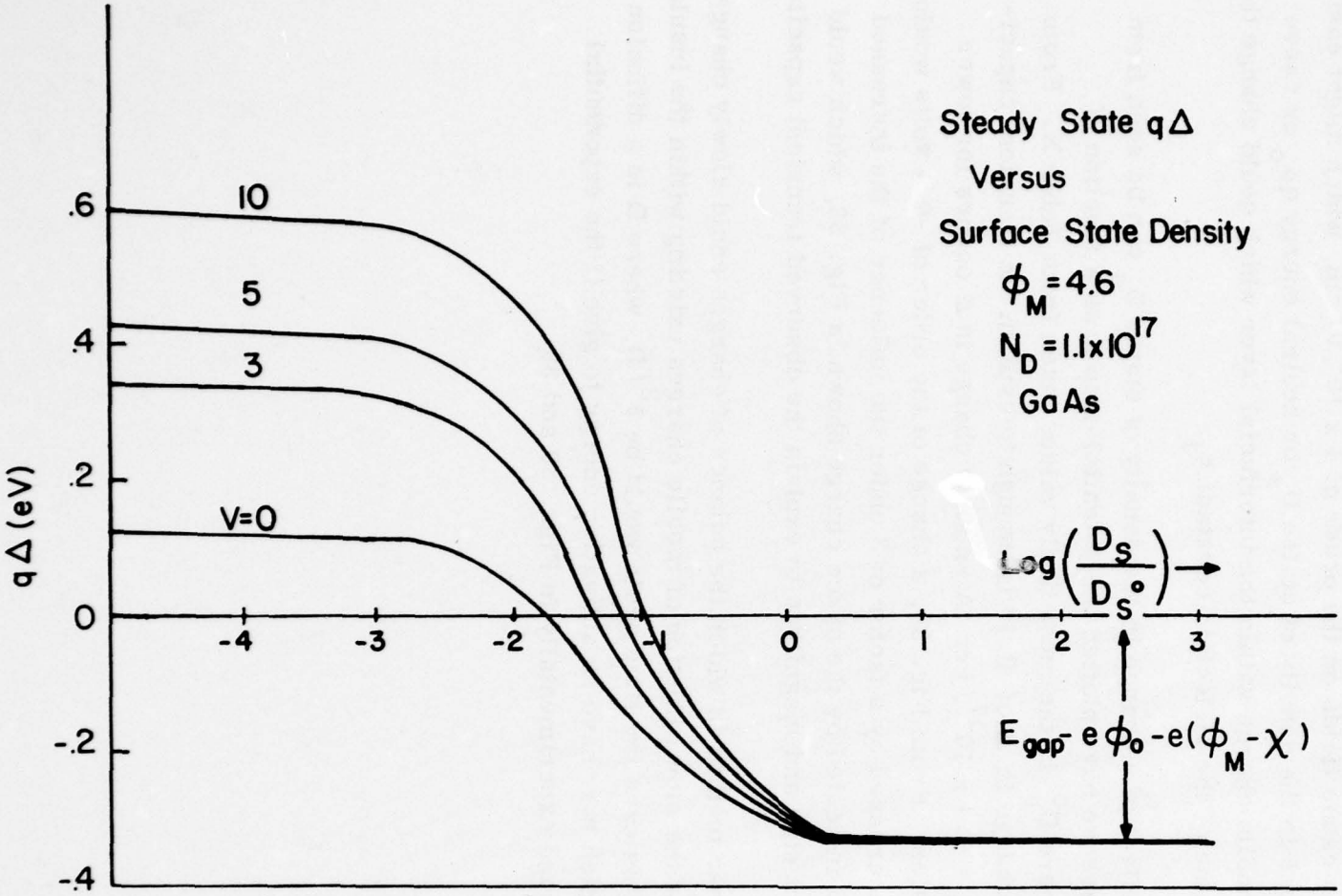

Figure 39 The Voltage Drop Δ, across the Insulating Layer as a Function of log (D_S / D_S^o) where D_S^o is Sze's value for the quantum density of states. Near $D_S = D_S^o$ the curve approaches its asymptotic value for large D_S, where the barrier height is pinned near $E_{gap}/8 - \phi_o = .9V$. For small values of D_s, $\Delta = \delta / \epsilon_i Q_{sc}$ where Q_{sc} is the space charge.

7.0 GROWTH AND FABRICATION METHODS FOR MINIMIZING TRAP EFFECTS ON FET'S

Historically, FET performance has been adversely affected by both bulk traps introduced into the channel by outdiffusion from the semi-insulating substrate and by the effects of surface states. Unfortunately, neither of these effects can be completely eliminated. The technology for the growth of bulk semi-insulating GaAs has not advanced to the state where it is possible to make outdiffusion negligible. Attempts to apply dielectric coverings (passivation) to the channel surface have generally been unsuccessful.

Since the problems could not be eliminated, FET designers have emphasized solutions which circumvent the problem. Solution 1 is the buffer layer, which moves the conducting channel to a position remote from the substrate, as illustrated in Fig. 40, and thereby reduces the number of bulk traps. This increases the channel mobility. Solution 2, also shown in Fig. 40, is the recessed gate in which the surface charge between gate-and-drain and between gate-and-source is moved away from the channel. This surface charge has important effects in device operation, although its effect was minimized in our DLTS measurement by the geometry of the fat FET. These surface states are generally negatively charged and can modulate the gate depletion capacitance as the gate-drain bias is varied. The extended deplation layer can increase the source-drain resistance, especially at low gate biases.

The doping profile for a wafer designed to be fabricated into a low-noise FET with a recessed gate is shown in Fig. 41. One of the problems associated with growing the buffer layer is that outdiffusion of acceptors from the substrate partially compensate for the doping density of donors, which is determined by the $AsCl_3$ mole fraction in the VPE reactor system. We use this compensation to our advantage by growing a thin buffer layer ($\approx$ 2 mm) and letting the acceptors drive the doping level down to the low 10^{13}/ cc range.

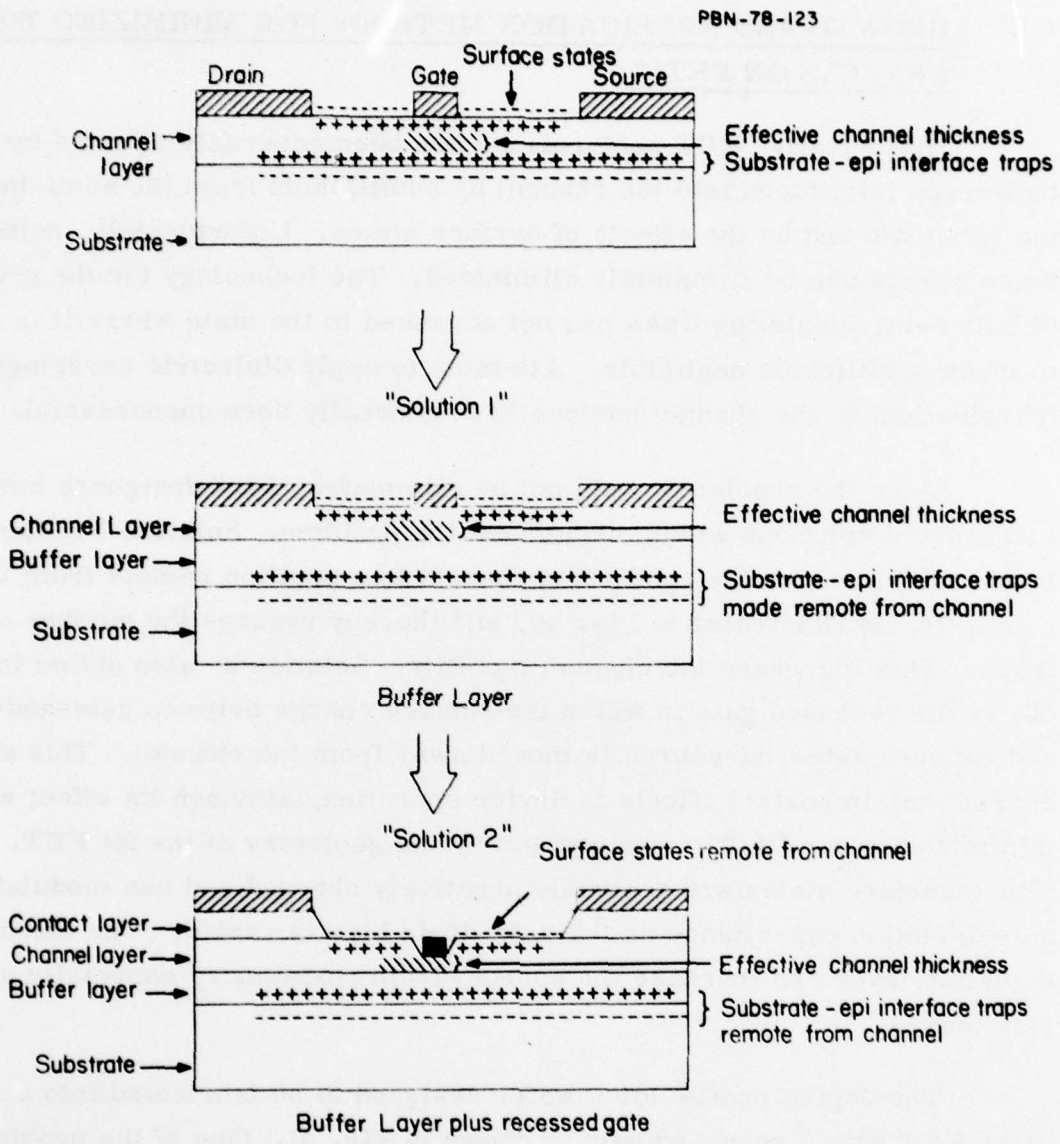

Figure 40 Chronological Sequence of Changes in Device Technology to Minimize Effects of Traps.

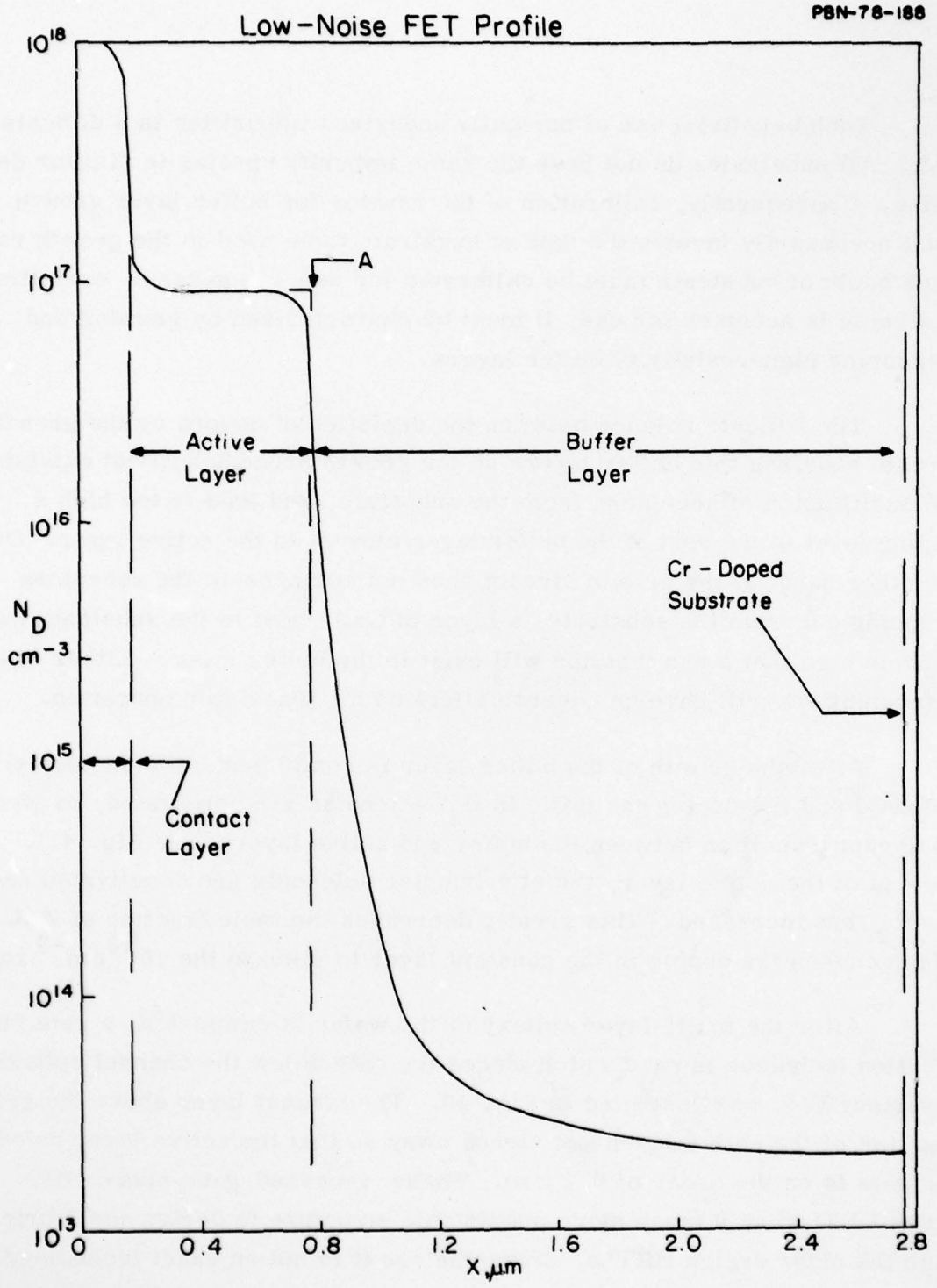

Figure 41 Doping Profile of a Low-Noise FET showing a Low-Doped Buffer Layer separating the Active Layer from the Substrate. An n^+ contact layer is grown near the surface.

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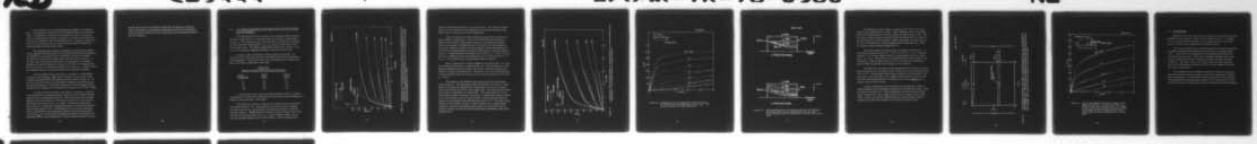

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Such beneficial use of normally undesired impurities is a c
task. All substrates do not have the same impurity species in sin
sities. Consequently, calibration of the reactor for buffer layer g
must necessarily involve the type of substrate to be used in the gr
Each boule of substrate must be calibrated for use. In general, e
new boule is accepted for use, it must be characterized by growin
measuring high-resistivity buffer layers.

The delicate balance between the depletion of donors by the
stream requires thin buffer layers so the growth process will not
the outdiffusion of acceptors from the substrate, and lead to too hi
doping level in the part of the buffer layer closest to the active lay
the other hand, if the growth stream does not compensate the acce
diffusing out from the substrate, a layer of GaAs next to the subst
become p so that a p-n junction will exist in the buffer layer. Eit
two conditions will have an adverse effect on the transistor operat

After the growth of the buffer layer is completed, an etch
solenoid and the doping gas (SiH_4 in H_2) solenoids are activitated,
an abrupt transition between the buffer and active layers (see Fig.
the end of the active layer, the etch bubbler solenoids are deactiv
the H_2 flow increased. This greatly decreases the mole fraction
which causes the doping in the constant layer to jump to the 10^{18} c

After the multi-layer epitaxy of the wafer is completed, a
rication technique is used which places the gate below the channel
layer surface, as illustrated in Fig. 40. The contact layer above
and part of the active layer are etched away so that the active laye
the gate is on the order of 0.2 μ m. These recessed-gate-plus-b
layer FET's are a much more predictable structure to design an
than the older design FET's. Nevertheless it is not an exact tec
This is exemplified by the experimental evidence from numerous
tories that I_{dss} for a given pinch-off voltage is influenced by the
deposition process, the process used to etch the channel and gate

and the type of post-etch cleaning to which the FET surface is subjected. In the next section we will present experimental results for recessed gate wafers in which a buffer layer and a contact layer are successively added to the FET structure.

8.0 I-V CURVES MEASURED ON RECESSED GATE FET'S BY PULSED AND CW METHODS

FET characteristics were evaluated using equipment which measures the source-drain current as a function of the gate voltage V_g and the drain voltage V_d. The voltages can be kept steady or the current can be measured at a fixed time after pulsing either V_g or V_d from some fixed value to the measurement value. The pulsed measurements indicate the presence or absence of the transient emptying and filling of bulk and surface traps.

In order to make comparisons between different structures, we evaluated FET's which were buffered and unbuffered and which were grown with and without n^+ contact layers (see Fig. 40) connecting the channel to the source and drain as indicated in Table XIII.

TABLE XIII

DEVICES TESTED FOR I-V CHARACTERISTICS

Device Designation	Buffer Layer	Contact Layer
A	No	No
AB	Yes	No
AC	No	Yes
ABC	Yes	Yes

A large number of I-V curves was taken with these devices, of which we will show a selected few to illustrate the device improvement resulting from adding a buffer zone and a contact layer.

The solid curves in Fig. 42 show the DC characteristics measured on the unbuffered device A(2). The dashed curves show the result of pulsing the drain from 0 to V_d, and measuring the drain current 100 μ s after the drain is turned on. Pulsing the device causes a current increase on the order of 4 mA near the knee of the curves, i.e., near the drain voltage, where velocity saturation begins to occur in the channel. These transients were

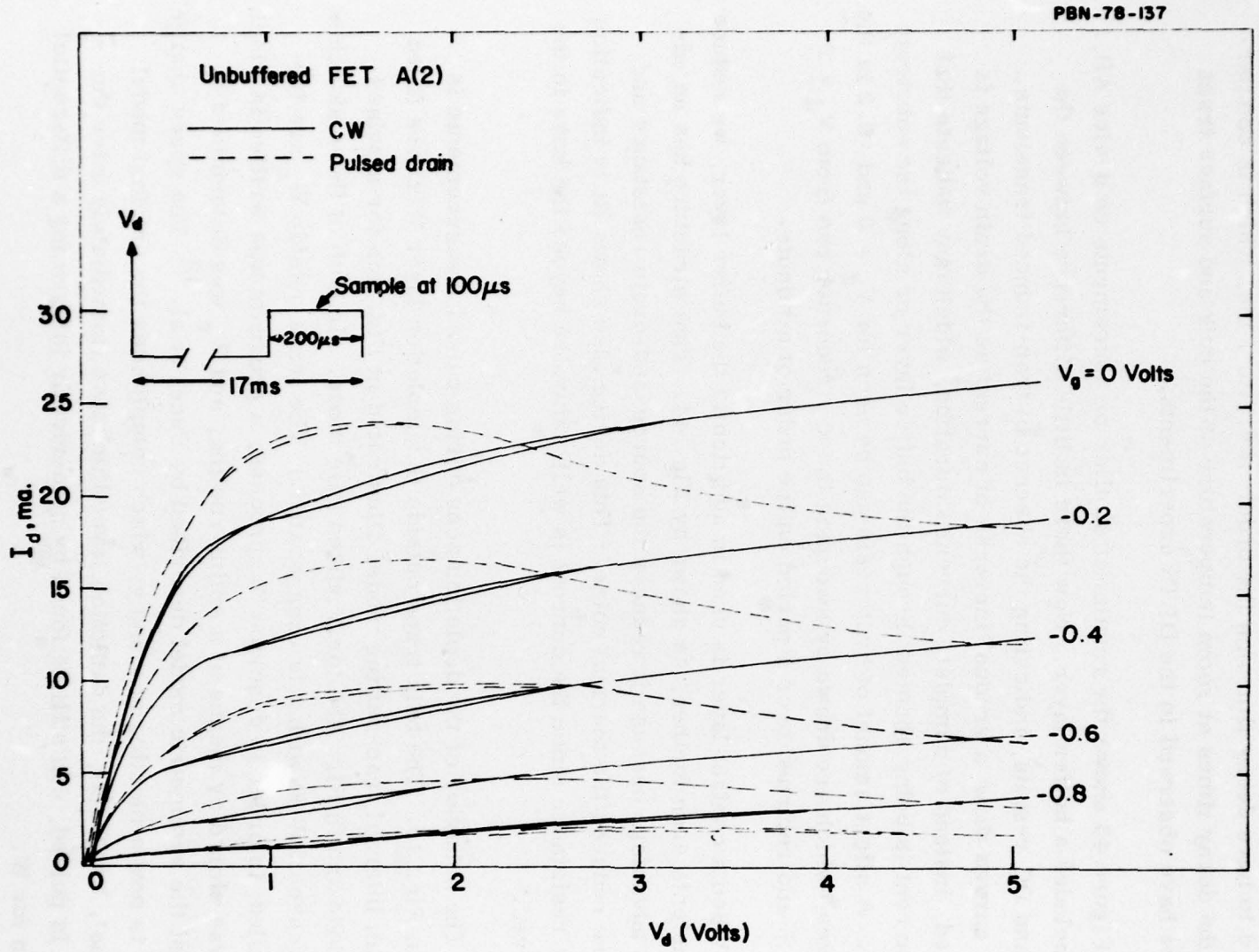


Figure 42 Comparison of DC and Pulsed Drain Characteristics for an Unbuffered Wafer with a Recessed Gate. The kinks which appeared on DC curves taken earlier in this program have disappeared but large transient effects are still found, persisting for periods lasting from 0.2 to 1 ms.

observed to have decay times on the order of 0.2 to 1 ms, which is comparable to the decay times at room temperature of the bulk and surface traps which we have observed in the DLTS experiments.

Figure 43 shows the results of similar measurements on device AB, which includes a buffer layer. Now there is little difference between the pulsed and DC results, indicating the absence of trap-induced transients. The DC curves show a gradual increase of current as the drain voltage is increased, instead of complete current saturation, which may indicate that some current is being shunted through the buffer layer or along the substrate surface. A slight amount of hysteresis can be seen for $V_g = 0$ and -0.2 in the DC curves, which are drawn by sweeping the x-y recorder pen from $V_d = 0$ to $V_d = 5$ and returned over a period on the order of a minute.

When a contact layer is used in addition to the buffer layer, we reduce the transients even further, as shown by Fig. 44. This structure has an additional advantage because it reduces the source-and-drain resistance and therefore reduces the thermal noise. This device also shows little indication of shunt resistance since the current is well saturated beyond the knee in the I-V curves.

The behavior of the depletion zone during pulsed measurements is shown in Fig. 45. The bulk traps outside the depletion layer W(x) are filled during an internal trap-setting mode, illustrated in Fig. 45a for a pulsed drain mode and in Fig. 45b for a pulsed gate mode. (In both of these sketches, the increase of W(x) with x is exaggerated.) The traps outside W_o are initially filled; in order to describe the process, a program was written in which $W_o(x)$ was stored by means of a spline routine, and W_o was determined by means of the symmetric model described by Pucel et al.[18] The space charge density is now a function of x and y, which complicates the original model somewhat, but $W_1(x)$, the depletion layer thickness immediately after the voltage is pulsed, can still be found by numerically integrating a differential equation for W.

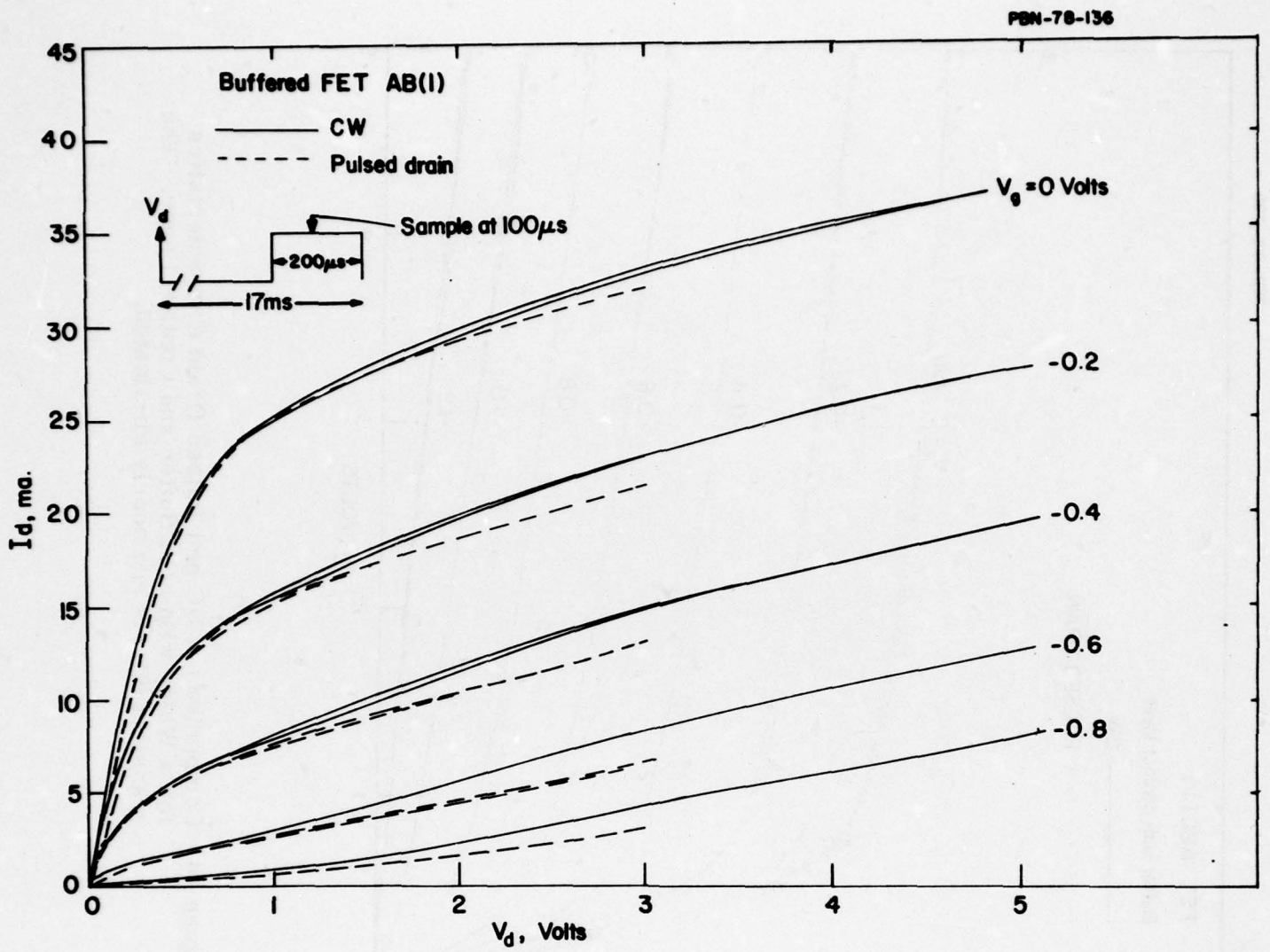


Figure 43 Comparison of DC and Pulsed Drain I-V Characteristics for a Buffered Wafer with a recessed gate. The transient effects are greatly reduced.

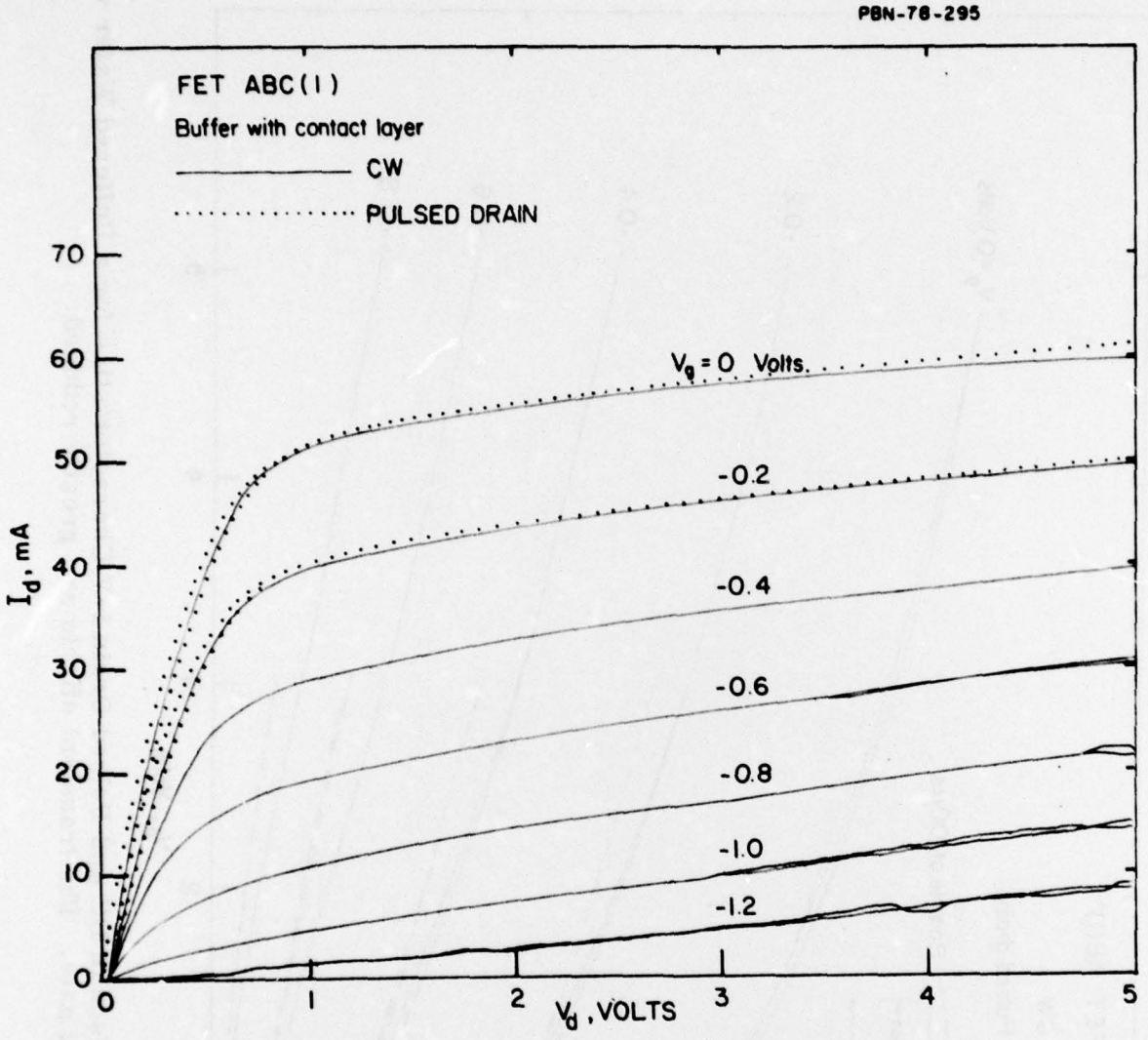
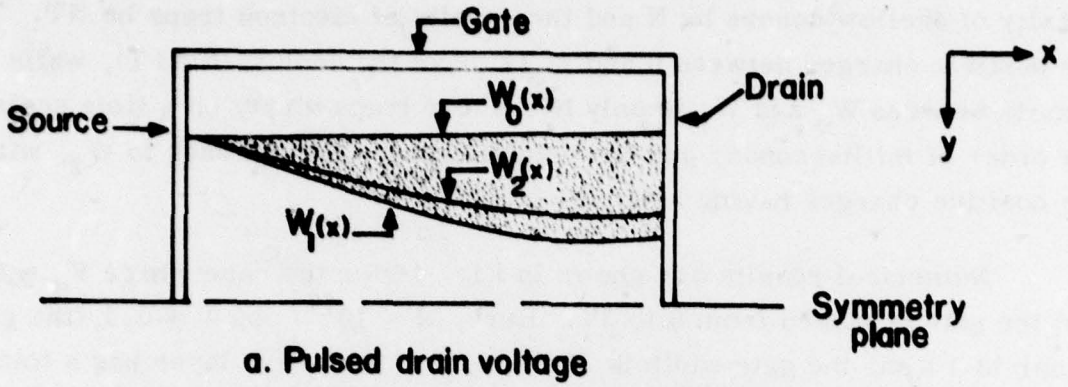
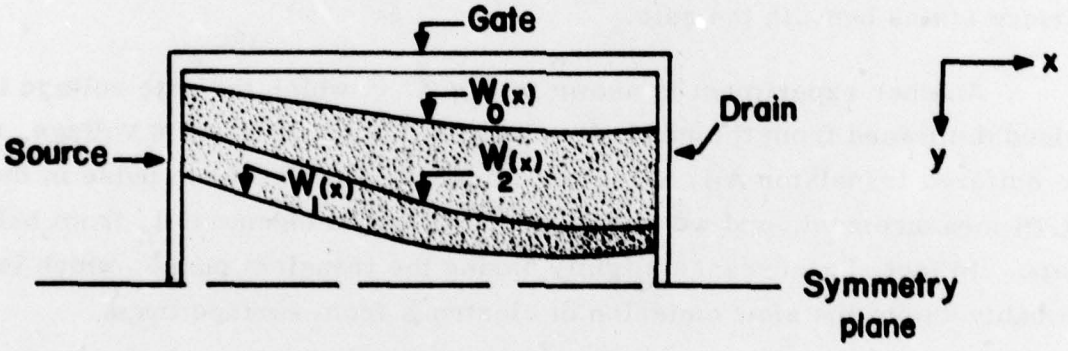


Figure 44 Comparison of DC and Pulsed Drain Characteristics for a Wafer with both Buffer and Contact Layer. The transient effects are nearly eliminated.



a. Pulsed drain voltage



b. Pulsed gate voltage

Figure 45 Schematic Diagram of a Depletion Layer in a FET During a trap setting pulse ($W_0(x)$), immediately after the pulse ($W_1(x)$) and after the FET has had time to reach a new steady state.

Immediately after the voltages are pulsed to new values, the traps between $W_o(x)$ and $W_1(x)$ will be filled. More explicitly, let the active layer density of shallow donors be N and the density of electron traps be NT. Then the positive charges between 0 and $W_o(x)$ have the density N(1+T), while the density between W_o and W_1 is only N. These traps empty on a time scale on the order of milliseconds, and the depletion layer settles back to W_2, with the positive charges having a density N(1+ T).

Numerical results are shown in Fig. 46 for the case where V_d = 5V and the gate is pulsed from 0 to 3V. Here, N = 10^{17}/ cc, T = 0.1, the gate length is 1 μ m, the gate width is 300 μ m, and the active layer has a thickness a = 0.3 μ m. The thickness of the depletion layer does not change very much with x, which is typical of these FET's, but may seem surprising to someone with a qualitative understanding of FET operation.

For bulk traps, the drain current should increase during the transient phase as shown by the calculation of Fig. 46 where the current increases from 42.4 to 47.6. Measurements with the gate pulsed from 0 showed little effect and, in fact, the current decreased slightly, which would be consistent with the DLTS results which showed the depletion layer moving outward due to surface states beneath the gate.

Another experiment is shown in Fig.47 in which the gate voltage is pulsed downward from the pinchoff voltage to the recorded gate voltage, using the buffered transistor AB. This is equivalent to the reverse pulse in the DLTS measurement, and we would expect to see no change in I_d from bulk traps. In fact, I_d increases slightly during the transient phase, which is probably due to the slow emission of electrons from surface traps.

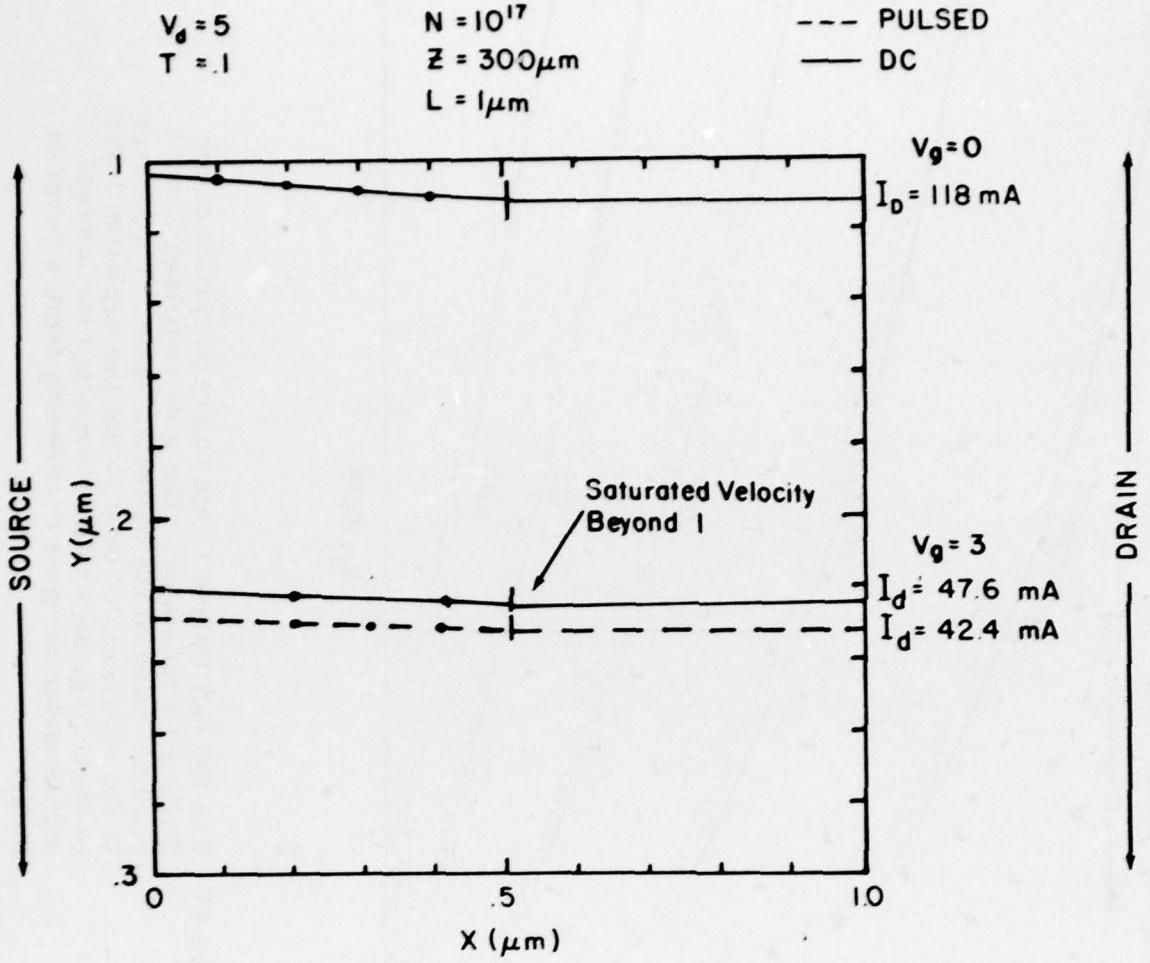


Figure 46 The Calculated Positions of the Edge of the Depletion Layer for $V_g = 0$, Immediately after pulsing V_y to 3 volts and after reaching the depletion layer has fallen back to its new steady state. In each case the channel has reached saturated velocity beyond the / marks. The values of Y from the gate to 0.1 μm are not shown.

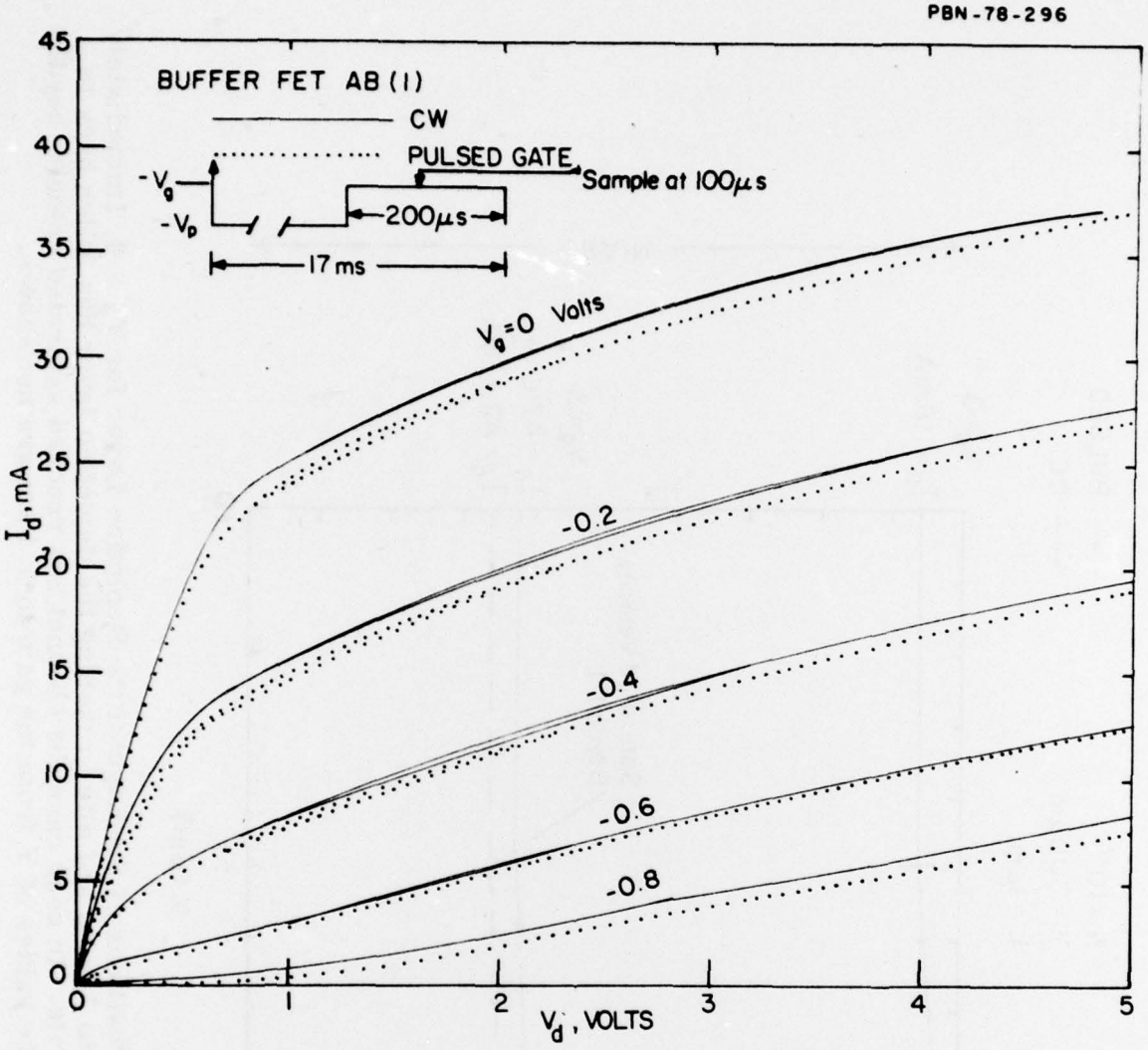


Figure 47 The DC and Pulsed Drain Characteristics of the Buffered Transistor. The gate is pulsed from pinchoff value to the indicated value. The change in the characteristics indicate the depletion layer is shrinking, as would be expected for surface states under the gate recovering from a reverse pulse.

9.0 CONCLUSIONS

During the last year of this contract, DLTS measurements detected and identified electron traps in n-GaAs and hole traps in p-GaAs. A technique was developed by which the energy level of the trap and its cross section could be obtained from a single DLTS temperature sweep.

A new type of signature due to surface traps was discovered and shown to produce stronger DLTS signatures than bulk traps in normally-doped FET's. These surface trap signatures were qualitatively different from bulk traps in several ways. They may be expected to produce noise whose frequency will be upconverted to produce FM noise affecting microwave oscillators. The noise effects of the surface traps may have important effects on the microwave operation of FET's but noise studies are beyond the scope of this contract.

FET designs have been modified to include the growth of multi-layer epitaxy with buffer layers and contact layers and the fabrication of devices with recessed gates. Pulsed and DC measurements taken on these devices demonstrated that major transient variations in FET parameters over the scales on the order of milliseconds have been eliminated by these techniques.

10. PERSONNEL

The principal investigators of this program over the past year were Dr. Lowell Holway and Dr. Michael Adlerstein. Epitaxial semiconductor growth was directed by Dr. Alan Swanson. The fabrication of fat FET's was directed by Dr. James Vorhaus and the fabrication of the recessed gate FET's was directed by Dr. B. S. Hewitt. The electronic design and the DLTS experimental measurements were carried out by Mr. Jack Curtis.

Overall technical guidance and consultation was provided by Mr. Robert Bierig, the manager of the Research Division Semiconductor Laboratory.

11.0 PUBLICATIONS, PRESENTATIONS AND REPORTS

A chronological listing is given below of the publications, presentations and reports which were generated from Contract No. F44620-75-C-0063 or which are planned.

1. "Electrical Traps in Microwave Materials," Interim Scientific Report for the period March 1, 1975 - February 29, 1976, prepared by Michael Adlerstein and Charles Krumm.

2. M. G. Adlerstein and C. F. Krumm, "Electrical Traps in GaAs Microwave FET's," Workshop on Compound Semiconductors and Microwave Devices, San Diego, California, March 11, 1976.

3. R. A. Pucel and C. F. Krumm, "Measured Drift Mobility in n-type GaAs epi Layers," Workshop on Compound Semiconductors and Microwave Devices, San Diego, California, March 11, 1976.

4. J. Thompson, S. R. Steele and R. Bierig, "Effect of Substrate Upon High Resistivity Buffers for Field Effect Transistors," Workshop on Compound Semiconductor Materials and Devices, San Diego, California, March 11, 1976.

5. R. A. Pucel and C. Krumm, "Simple Method of Measuring Drift Mobility Profiles in Thin Semiconductor Films," Electronics Letters 12 10, p. 240, 1976.

6. M. G. Adlerstein, "Electrical Traps in Microwave FETs," Electronics Letters 12 12, p. 297, June 1976.

7. Robert A. Pucel, "A Mobility Profilometer for Semiconductor Films. Raytheon Patent Disclosure No. 31385, dated October 5, 1976.

8. M. G. Adlerstein, "Trapping Phenomena in GaAs Microwave FET's," AFOSR/ NE Advisory Group Workshop on Gallium Arsenide Materials for Microwave Devices, 14 October 1976, Arlington, Va.

9. "Electrical Traps in Microwave Materials," Interim Scientific Report for the period March 1, 1976 - February 28, 1977, prepared by Michael Adlerstein and Lowell Holway.

10. L. H. Holway, Jr., M. G. Adlerstein and J. Curtis, "Electronic Trap Studies on GaAs FET Wafers," Workshop on Compound Semiconductor Microwave Materials and Devices, San Francisco, California, February 13, 1978.

11. L. H. Holway, Jr., M. G. Adlerstein and J. Curtis, "Surface State Transients in GaAs FET's," (tentative title of publication to be based on Sections 4 and 6 of this report).

12. "Electrical Traps in Microwave Materials," Final Report, prepared by Lowell Holway and Michael Adlerstein, April, 1978.

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3. M. G. Adlerstein, "Electrical Traps in Microwave FET's," Electronics Letters 12, 297-298 (1976).

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