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(6) DEVELOPMENT OF A 10 KVA POWER CONDITIONER UNIT, AIRCRAFT, 115/200 VOLT, 3-PHASE, 400 HZ.

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This paper discusses the development of parallelable power conditioning units capable of operating from 200 V line-to-line, 3-phase, 400 Hz ac or 270 V dc input power to produce a 10 kVA regulated, low-distortion 115/200 Vac, 3-phase, 400 Hz output.

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PREFACE

The work reported herein was performed by DECC (Delta Electronic Control Corporation) under contract to the United States Navy, Naval Air Development Center (Contract N62269-76-C-0076). The Contracting Officer's representative was Mr. Howard Ireland.

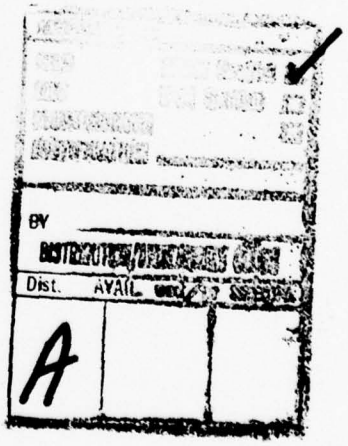

TABLE OF CONTENTS

1.0 INTRODUCTION

1.1 SCOPE

This report discusses the development of a 3-phase, 4-wire, 115/200 volt, 400 Hz Power Conditioner Unit (PCU) for aircraft use.

1.2 DESIGN OBJECTIVES

The primary objective was to design a small, light-weight, 3-phase power conditioner unit (PCU) such that sensitive loads will not be affected in their operation by power source transfers between PCUs when two or more PCUs are operated in parallel. Specific objectives are summarized in Table 1-1.

TABLE 1-1

PARAMETER	REQUIREMENT
Input	270 Vdc or 200 Vac, 3-wire, 3-phase 60 - 400 Hz
Output	115/200 Vac, 3-phase, 4-wire, 400 Hz ± 1 Hz
Rating	10 kVA
Load Power Factor	.75 (lagging) to 1.0
Efficiency	85% minimum
Overload Capacity	150% for 2 minutes 200% for 5 seconds
Short circuit current	300% for 5 seconds
Voltage Regulation	See Figure 1-1
Voltage Modulation	1.2 maximum
Frequency Modulation	± 0.5 maximum
Crest Factor	1.41 ± .07
Total Harmonic	4.5% maximum
Phase Displacement	120° ± 1.5° Balanced load 120° ± 3.0° Unbalanced load

TABLE 1-1 (cont'd)

PARAMETER	REQUIREMENT
Control	On-Off/Reset - Test
Protection	Overvoltage Undervoltage Underfrequency Overfrequency Overcurrent
Weight	50 pounds, max.
Size	10" x 10" x 20" excluding mounting & connectors
MTBF	10,000 hours
Temperature/Altitude	See Figure 1-2
Environmental Humidty	Mil-E-81910 (AS)
Salt Fog	(Procedure I)
Fungus	(Procedure I)
Sand & Dust	
Shock	
Vibration	(Fig. 514-2, curve H)
Acceleration	

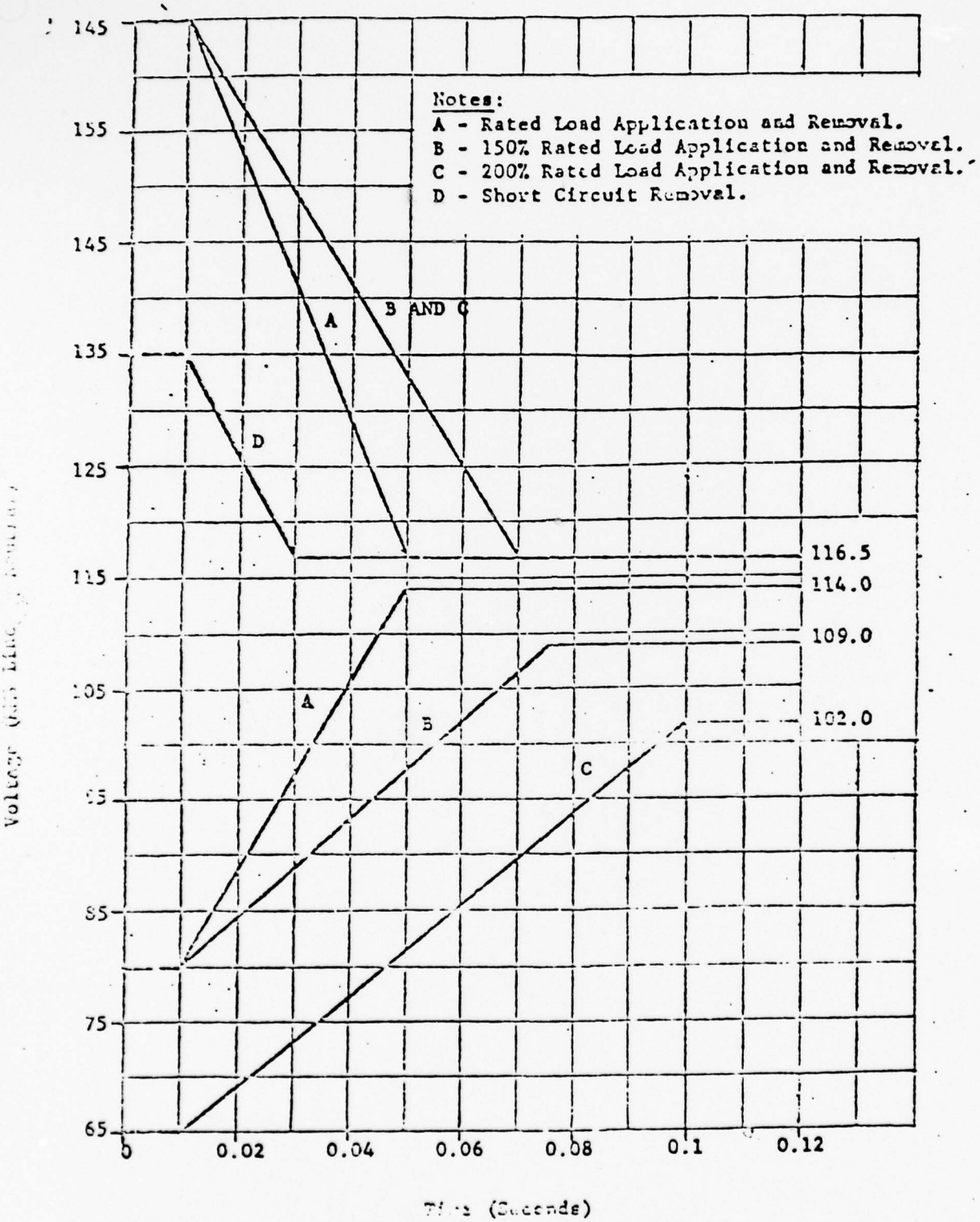

FIGURE 1-1 VOLTAGE TRANSIENT LIMITS

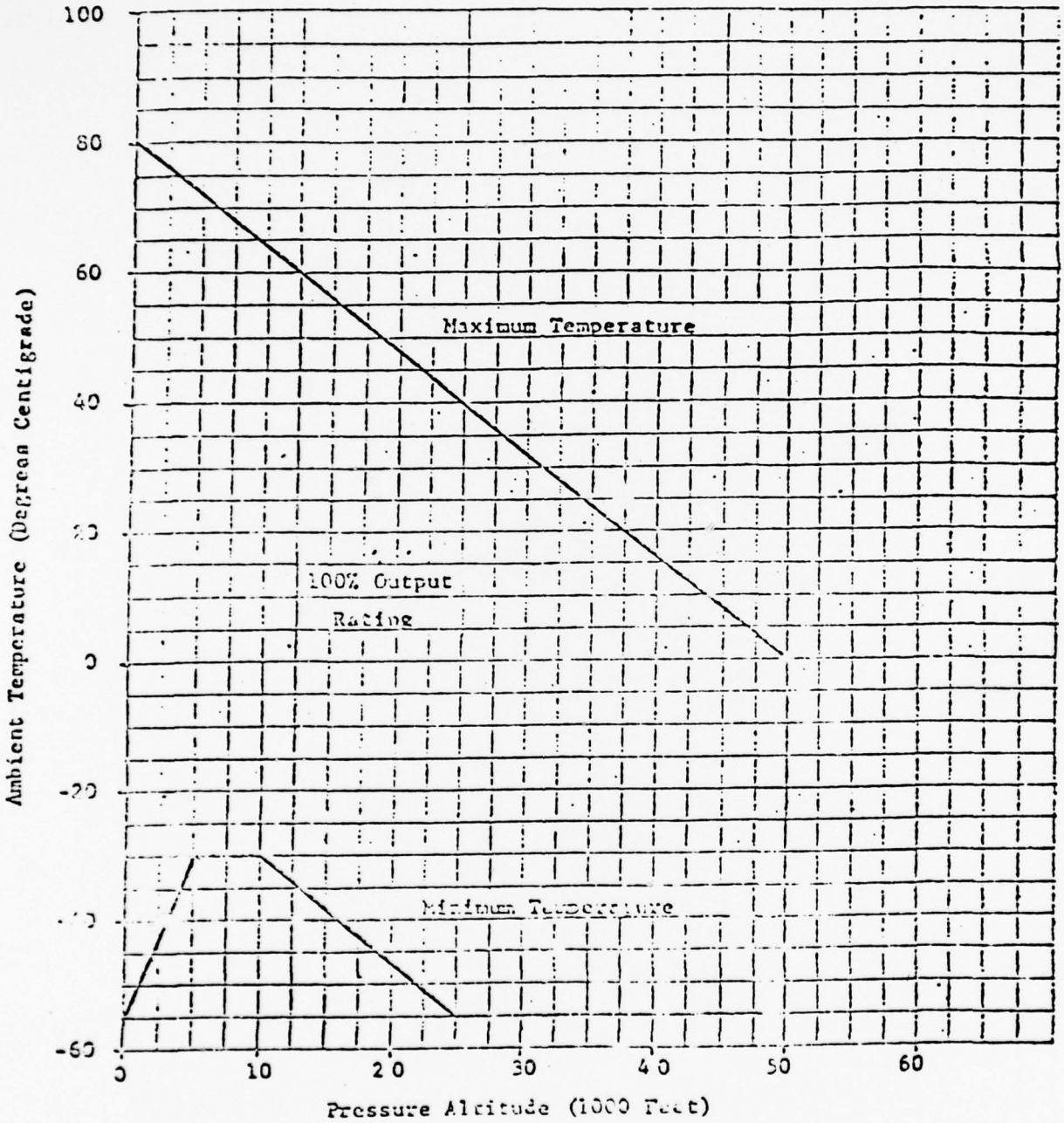

FIGURE 4-2- TEMPERATURE ALTITUDE REQUIREMENT

2.0 INVESTIGATION

2.1 BACKGROUND AND DESIGN APPROACH

The simplest type of low-frequency inverter consists of semiconductor devices switched on and off to produce a square wave of the desired frequency. To produce a sinusoidal output, filters must be used to remove the unwanted harmonics from the square wave. The amplitude of the square wave and consequently the amplitude of the output is proportional to the voltage of the dc power source. Therefore control of the output amplitude is dependent on control of the dc source. The output frequency is determined either by control of the properties of magnetics incorporated in the output stage or by the use of a low-level drive oscillator. Unfortunately, for low-frequency sinusoidal output the filters required are large, heavy, and inefficient. In addition, since the output amplitude is proportional to the dc source voltage, control of the output amplitude requires additional power circuitry to control the dc source voltage. A variation in this technique involves controlling the output amplitude by use of pulse-width-modulation techniques to produce a quasi-square-wave control signal to the output stage.

An improvement of the first technique can be made by making a more sine-like wave form. This is usually done by combining the outputs of several square- or rectangular-wave inverter stages operating at the output frequency or harmonics of the output frequency to produce a stepped wave-form. This approach greatly reduces the demands upon the output filter. Whereas this approach is used almost exclusively in fixed-frequency high-power inverters, the complexity of combining several inverter stages seems unwarranted in this application.

A third approach is to switch the output semiconductors (transistors) at a frequency which is a large multiple of the desired output frequency while employing pulse-duration-modulation techniques to synthesize the sinusoidal output waveform.

With this modulation technique, the extraneous frequency components can be made such that only high frequency (switching frequency) filtering is required. This minimizes the size and weight of the output filter.

Pulse-duration-modulation makes possible both amplitude and frequency control since the filtered output is

proportional to a low-level input signal which is readily generated and controlled. Thus, the circuitry is divided into a low-level signal source (containing all necessary amplitude and frequency control functions), followed by a relatively simple, very efficient, power amplifier.

This method requires fast power transistors in the output stage, however. Additionally, these transistors must withstand the high supply voltage utilized in the PCU.

2.2 BASIC DESIGN DECISIONS

Pulse-duration-modulation was selected as the best approach for meeting the design objectives. The following factors were dominant in reaching this decision:

1. Efficiency
2. Size and weight
3. Control provided over output parameters.

The third factor above is important because parallel operation of two or more inverters requires that the outputs be precisely controlled as to relative frequency, phase and amplitude. Furthermore, it is desirable that the control be provided using the lowest possible number of interconnections between units.

The signal source selected for the PCU is a digital-to-analog converter. This circuit provides a low distortion output which can easily be synchronized with other units and whose amplitude can be sufficiently regulated by means of dc voltage and current feedback loops to permit direct parallel connection of PCU's without external load balancing transformers. The only necessary interconnections between units, therefore, are low-level synchronizing signals for control of the output phase and frequency.

The major problems in the output stage then become:

1. Providing sufficient voltage rating to all components to withstand the 441 volt peak transient supply voltage.
2. Providing sufficient current capability to handle the 300% short circuit current requirement.

3. Providing sufficient switching speed to keep the losses within acceptable limits.

4. Providing adequate filtering without introducing excessive phase shift.

3.0 TECHNICAL DESCRIPTION

3.1 OVERALL DESIGN

A simplified schematic diagram of the actual inverter circuitry used in the PCU is shown in Figure 3-1. Each phase is essentially an independent circuit driven by a common crystal controlled clock and synchronizing circuit. The sine wave generator contains a digital-to-analog converter for each phase to develop the required modulating voltages. The modulating voltages are applied to pulse duration modulators which, in turn, control multi-transistor output switches capable of handling the required power. The basic switching frequency is 14.4 kHz. The un-regulated 270 Vdc input voltage (or rectified ac) is applied across the bridge-configured output switching stages. Three-state modulation is utilized to minimize the output filter requirements and to provide more effective control of the output.

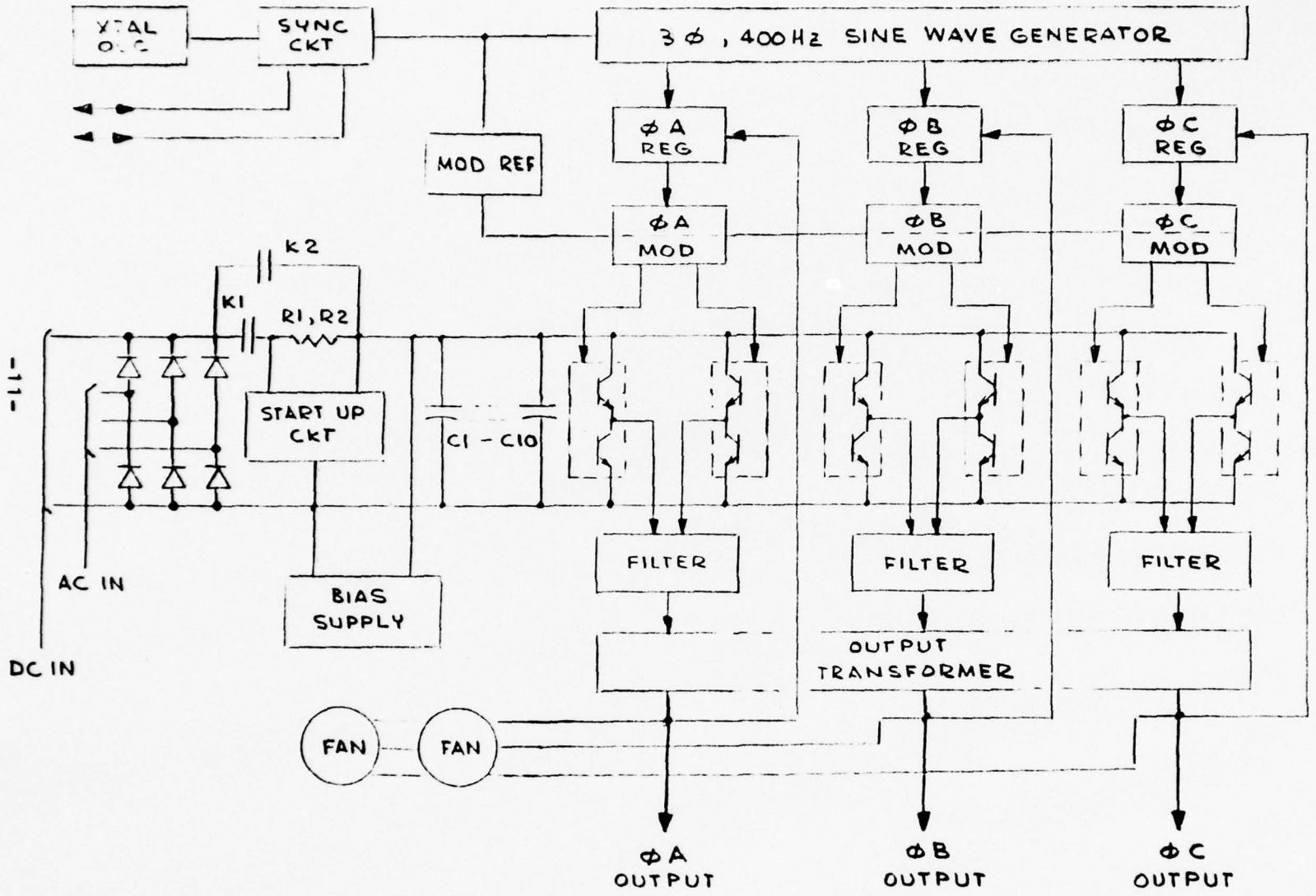
XTAL O.C.
SYNC CKT
3 Φ , 400 Hz SINE WAVE GENERATOR
MOD REF
Φ A REG
Φ B REG
Φ C REG
Φ A MOD
Φ B MOD
Φ C MOD
K2
K1
R1, R2
START UP CKT
C1 - C10
FILTER
FILTER
FILTER
AC IN
DC IN
BIAS SUPPLY
OUTPUT TRANSFORMER
FAN
FAN
Φ A OUTPUT
Φ B OUTPUT
Φ C OUTPUT

FIGURE 3-1

SDT 13305 transistors (Solitron Devices, Inc.) were selected for the output stage as having the required speed, current and voltage ratings.

Fault protection circuits are provided to protect against over and underfrequency, over and undervoltage, overcurrent, overtemperature, improper phasing and extraneous frequency components in the output. In the event of a malfunction, the output bus contactor (not supplied) control voltage is removed to take the PCU off-line. Also, the internal circuitry is de-energized. A "test" mode is provided, however, which allows check-out of the PCU off-line.

Parallel operation is accomplished by means of two synchronizing circuits common to all units plus remote sensing of the output bus voltage. One synchronizing signal establishes a common clock frequency for all units while the second insures that they are always in phase. The PCU having the highest clock frequency automatically becomes the "master" for the system. Feedback circuits within each PCU modify the individual unit output voltages in relation to the bus voltage to provide proper load sharing.

Primary power for the unit may be supplied directly from a 270 Vdc source or the internal rectifier may be used to obtain the necessary dc from a 200 Vac, (line-line) three phase source. When initially turned on, relay K1 (Figure 3-1) closes to charge input filter C1-C10 capacitors through current limiting resistors R1 and R2. As the capacitors charge, the voltage drop across R1, R2 approaches zero allowing the charging current detector to operate relay K2. K2 shorts out the resistor and connects the filter capacitors directly to the source. The circuit allows K1 to remain operated for only a limited period of time, however, unless K2 closes. Therefore, any fault within the unit which results in a continued large inrush current will cause the unit to turn off. Normally, of course, K2 will operate and full power will be available to the circuits within the PCU.

The bias supply provides all of the low level voltages needed for the internal operation

of the unit. The supply consists of a switching regulator which reduces the input voltage to 120 Vdc. This regulated voltage is, in turn, applied to an inverter circuit to provide a source of high frequency ac power that is readily transformed to the required voltages and rectified. The high frequency source permits use of small transformers having minimum capacitive coupling between windings.

3.2 SIGNAL GENERATING CIRCUITS

As noted previously, each of the phases is independent of the others except for a common reference voltage supply and the synchronizing circuits. Therefore, the discussion will be limited to the operation of a single phase with the understanding that the others are identical.

The "digital" circuit for each phase is shown in Figure 3-2. Each PCU contains a single 460.8 kHz crystal controlled oscillator and

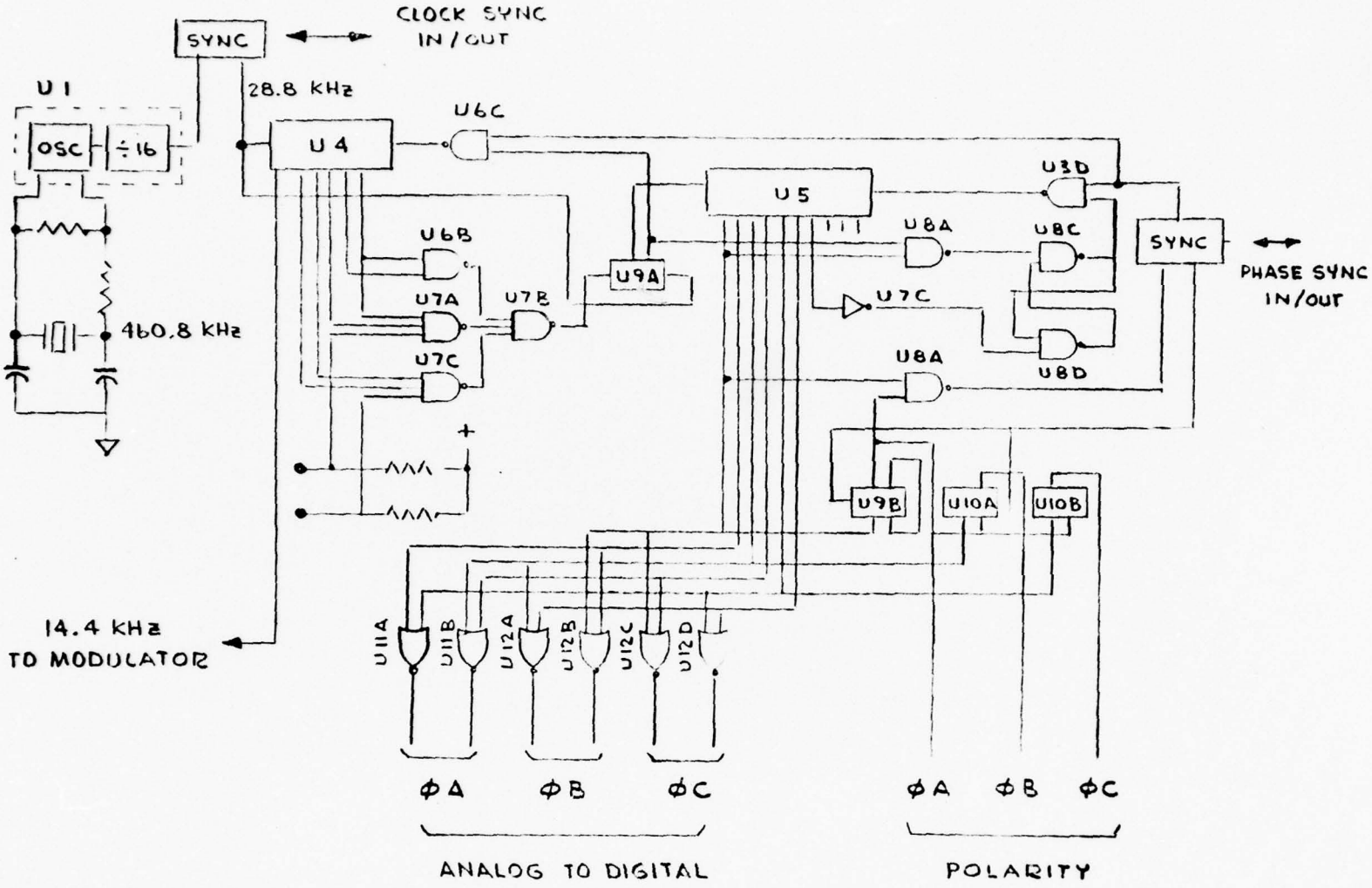
SYNC
CLOCK SYNC
IN/OUT
U1
OSC
÷16
28.8 KHz
U4
U6C
U5
U3D
U6B
U9A
U8A
U8C
SYNC
PHASE SYNC
IN/OUT
U7A
U7B
U7C
460.8 KHz
U7C
U8D
U8A
+
U9B
U10A
U10B
14.4 KHz
TO MODULATOR
U11A
U11B
U12A
U12B
U12C
U12D
ΦA
ΦB
ΦC
ΦA
ΦB
ΦC
ANALOG TO DIGITAL
POLARITY

FIGURE 3-2

divide-by-sixteen counter circuit (U1) driving a "clock sync" circuit, which allows parallel operation of two or more PCU's by insuring that all units operate at precisely the same frequency. The clock sync circuits are all inter-connected by a common bus. Since synchronizing crystal controlled oscillators is awkward, in reality each synchronizing circuit uses logic gates and a re-triggerable monostable multivibrator to select one of the available clock frequencies as the "master" clock frequency. The first PCU to generate a pulse on the bus inhibits the circuits of all other PCU clock sync circuits and thereby becomes the master.

The actual "clock signal" for the digital circuits is derived from a unijunction transistor oscillator. The UJT oscillator normally runs at a frequency slightly below 28,800 Hz, but is made to operate at 28,800 Hz by the selected "master" circuit. The UJT oscillator insures that there are no significant discontinuities in the clock signal in the event the master clock sync

signal is interrupted and another unit becomes the master.

The output of the UJT oscillator is a pulse which is applied to the input of binary counter U4 to generate a 14,400 Hz square wave which is integrated to form the triangular waveform required by the pulse-duration modulator. The 14,400 Hz signal is further divided by the counter and decoder logic to 4800 Hz. (Additional logic is provided for adaptation of the circuit to 50 Hz and 60 Hz output frequencies). The 4800 Hz signal is applied to the divide-by-six counter/decoder, U5. The decoder output is a sequence of six pulses which drive the three digital-to-analog converters. Each converter operates by switching appropriately weighted currents into a summing network so as to form the absolute value of a sine function. See Figure 3-3. The positive and negative half cycles are then determined by switching the gain of the next amplifier, AR7, from "plus one" to "minus one" at each alternate half cycle of

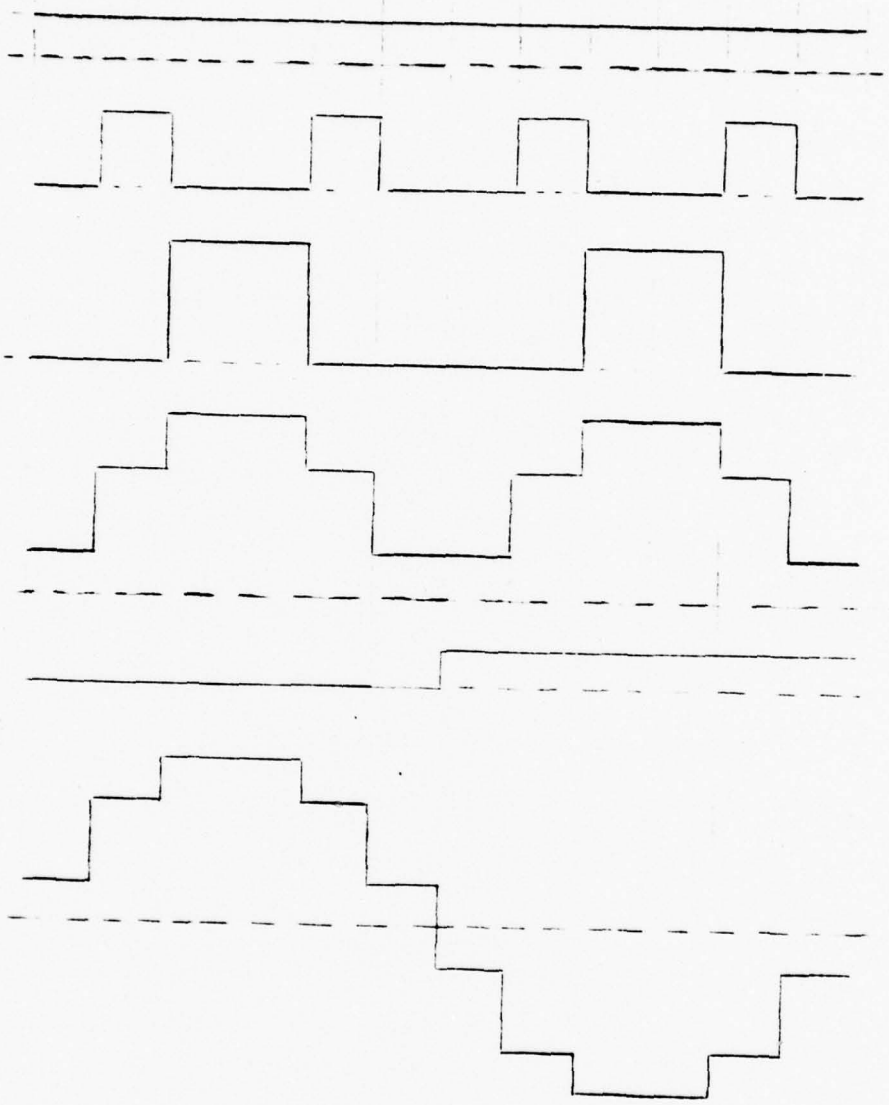

FIGURE 3-3

the output frequency. An additional "phase sync" signal is supplied between parallel operated PCU's to insure correct phasing of the units.

3.3 REGULATOR CIRCUITS

The amplitude of the PCU output is determined by the amplitude of the sinewave generator output which is, in turn, a function of the reference voltage and various current and voltage feedback paths. These circuits are shown in Figure 3-4.

There are three feedback loops which serve to determine the output voltage of each of the phases. With the output contactor open, only the inner loop consisting of transformer T1, rectifiers CR1 and CR2, filter R7 and C6, and amplifier AR6 (together with the reference voltage) determine the open circuit output voltage. Transistor Q8 effectively short-circuits amplifier AR4; therefore, the output of AR4 is fixed at a voltage equal to that of AR3. As there is no output

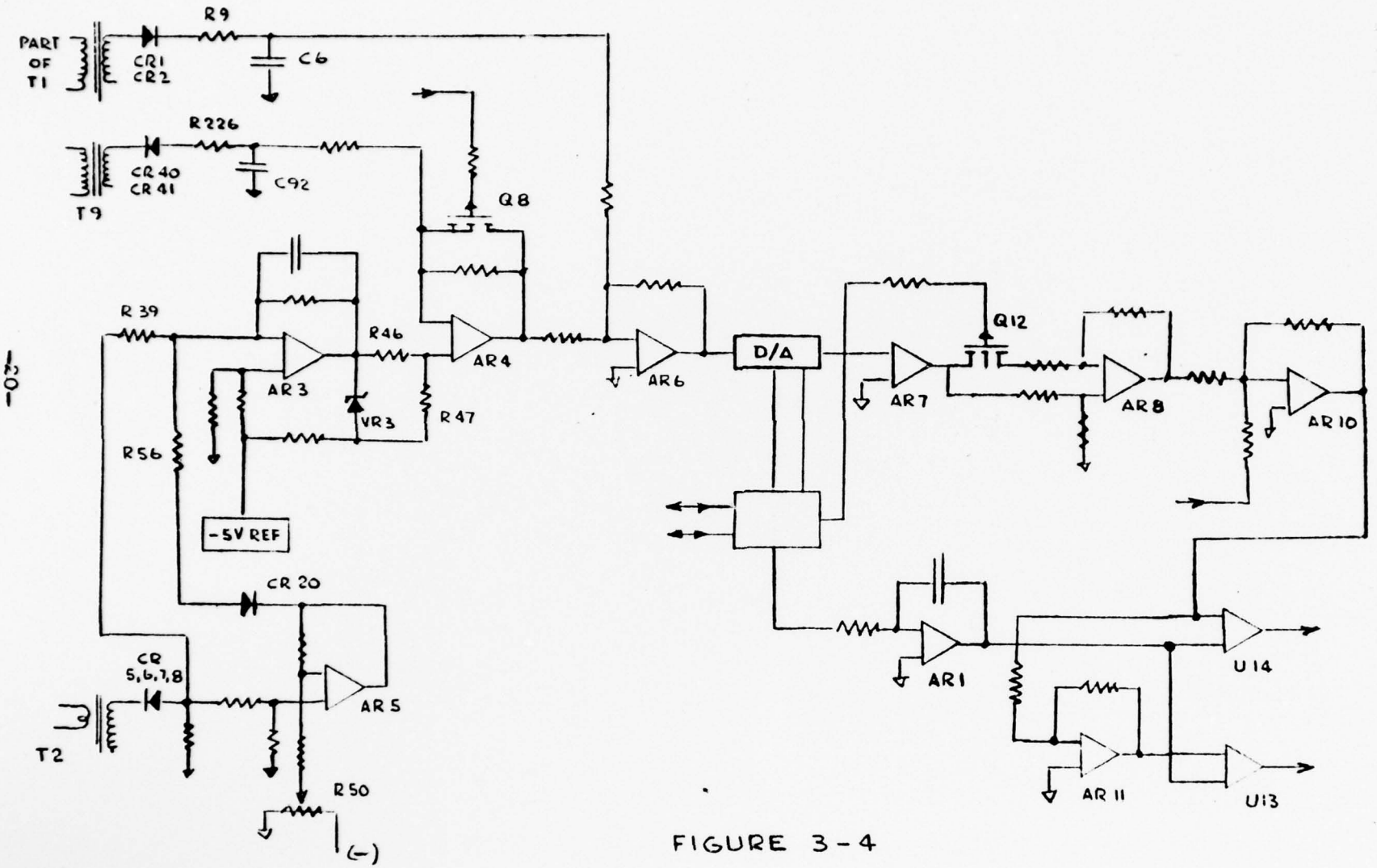
PART OF T1
CR1
CR2
R9
C6
R226
CR40
CR41
C92
T9
Q8
R39
R46
AR4
AR3
VR3
R47
AR6
D/A
Q12
AR7
AR8
AR10
R56
-5V REF
CR 20
CR 5,6,7,8
AR5
T2
R50
(-)
AR1
U14
AR11
U13

FIGURE 3-4

current with the contactor open, the output of AR3 is determined solely by the reference voltage.

When the output contactor is closed, the short is removed from AR4 and the outer loop then operates normally. Additional circuitry consisting of transformer T9, rectifiers CR40 and 41, filter R226 and C92 and amplifier AR4 are active in determining the output voltage. When load current is taken from the PCU, transformer T2, rectifiers CR5, CR6, CR7 and CR8 and amplifier AR3 serve to modify the reference voltage as required to insure current sharing with normal loads among parallel units and current limiting with abnormal loads.

3.4 FAULT DETECTION CIRCUITS

The fault detection circuits (shown in Figure 3-5) continually monitor the PCU for overcurrent, over and undervoltage, over and underfrequency, extraneous frequency components, improper phasing of parallel units,

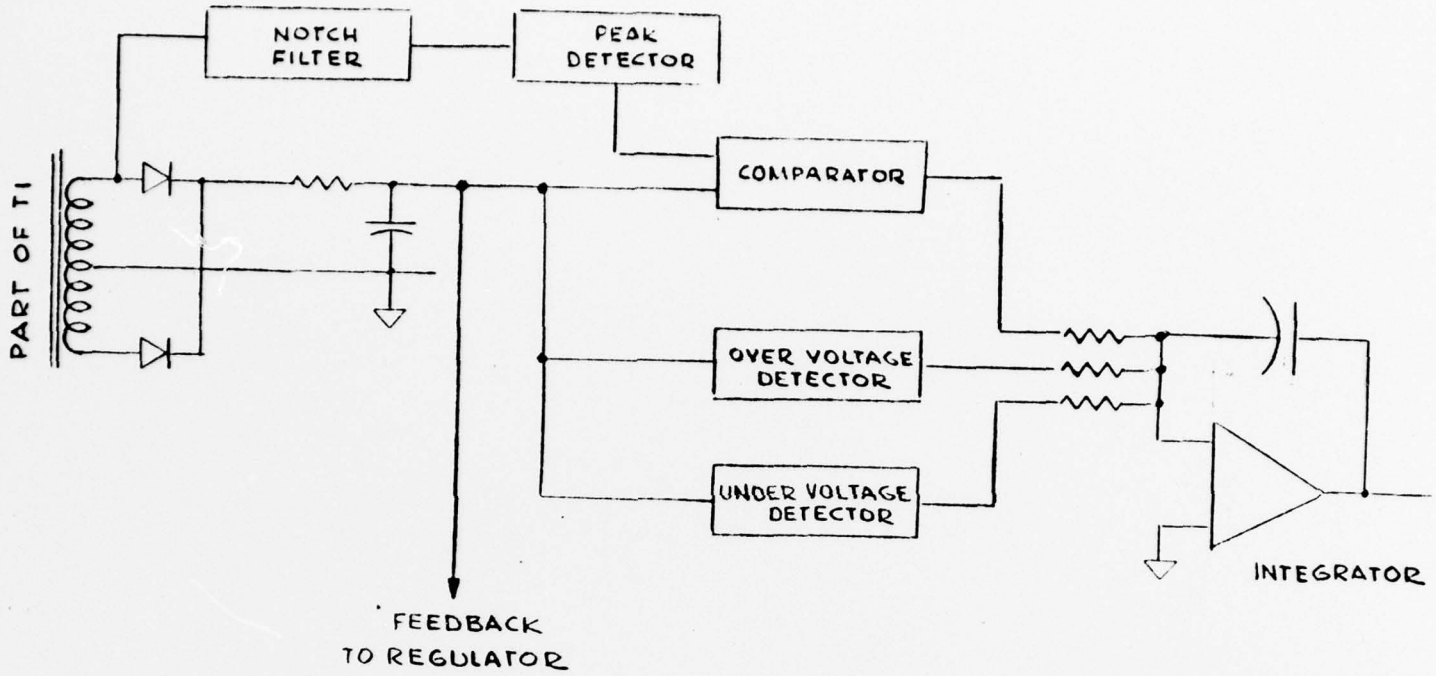
NOTCH FILTER
PEAK DETECTOR
COMPARATOR
PART OF T1
OVER VOLTAGE DETECTOR
UNDER VOLTAGE DETECTOR
INTEGRATOR
FEEDBACK TO REGULATOR

FIGURE 3-5

overtemperature and loss of input power. In general, detection of a fault will cause the unit to remove the output switch drive signals, open the output contactor and remove power from the internal circuits. For trouble shooting purposes, however, the unit will operate in the test mode so long as no attempt is made to go to the "ON" mode.

A signal from the feedback winding of the output transformer is applied to a band reject filter centered at 400 Hz. If the output deviates from 400 Hz or if there are extraneous frequencies in the output, there will then be an output from the filter. This output is detected and applied to the input of a voltage comparator. The other input to the comparator is a dc voltage proportional to the PCU output. A fault condition is signaled by the comparator when the output from the filter is excessive relative to the PCU output.

The dc voltage proportional to output voltage is also applied to the over and undervoltage detection circuits which serve to compare the output voltage to a fixed reference. The undervoltage signal is a step change in logic level, as is the frequency signal discussed above. However, the overvoltage signal varies as a function of the amount of overvoltage and therefore can be used to vary the interval during which the condition is allowed to persist as a function of the amount of excess voltage.

To achieve the required time delays for the various error conditions, each of the fault signals is applied to a separate input of an integrator circuit. Each input incorporates a resistance value such that the resulting slope of the output waveform will allow the output voltage to reach a preset voltage in the required time interval. The preset voltage is detected by means of another comparator which signals the need to shut down the unit.

3.5 SYSTEM CONNECTION

The system connections are shown in Figure 3-6.

4.0 RESULTS

4.1 TEST RESULTS

With minor circuit refinements, the PCU is capable of providing the required electrical performance. The efficiency was measured at approximately 92%. Distortion and regulation were within the required limits.

4.2 DEVELOPMENT PROBLEMS

The major development problem was finding acceptable small, light-weight components which would withstand the extreme range of input voltage and provide the required output performance. This problem was only partially solved with the result that the completed unit exceeds the target volume by 50% and the target weight by 140%. Further optimization of the design would

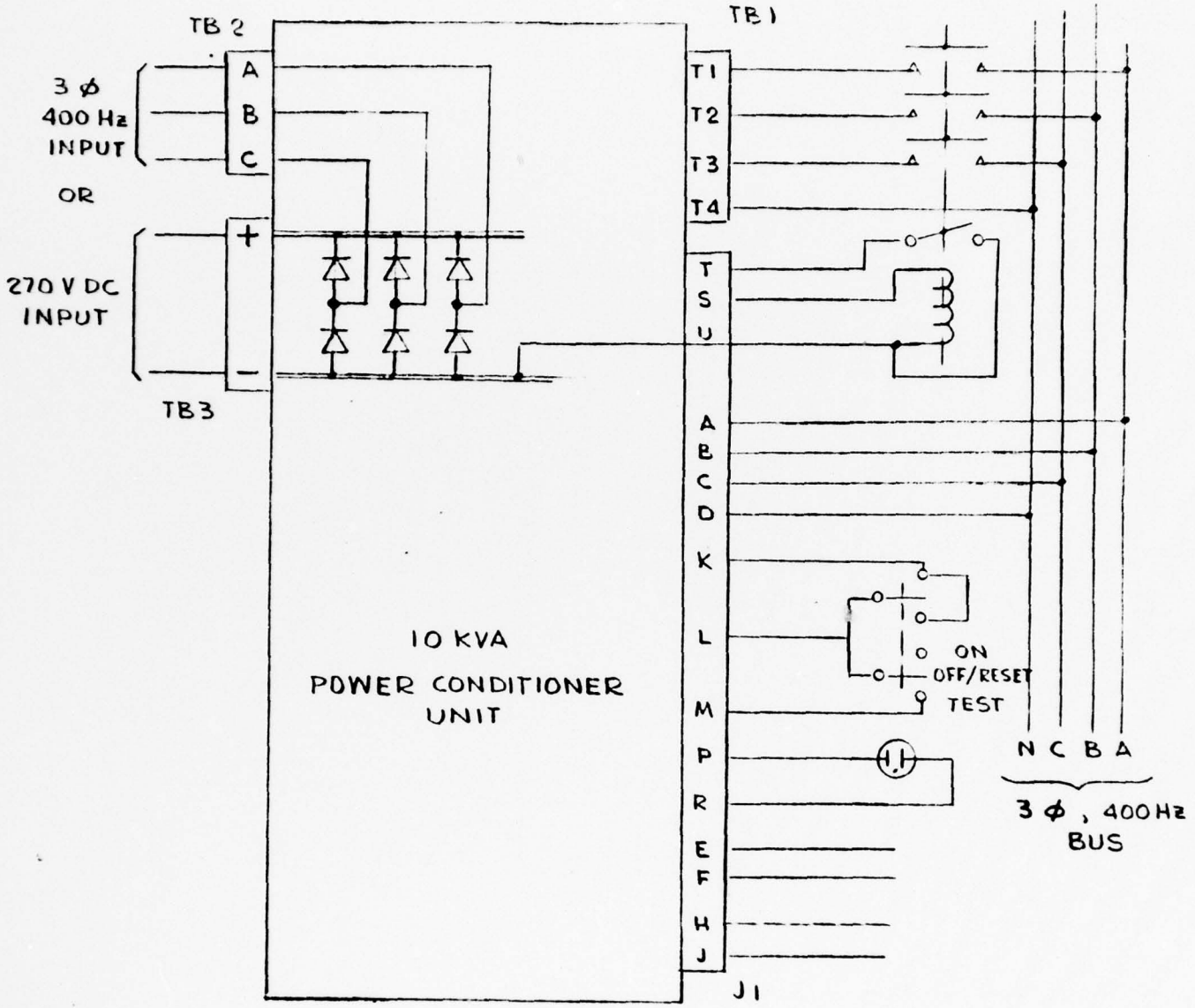
TB 2
3 ϕ
400 Hz
INPUT
OR
270 V DC
INPUT
A
B
C
+
−
TB3
TB 1
T1
T2
T3
T4
T
S
U
A
B
C
D
K
L
M
P
R
E
F
H
J
J1
10 KVA
POWER CONDITIONER
UNIT
ON
OFF/RESET
TEST
H.I
N C B A
3 ϕ , 400 Hz
BUS

FIGURE 3-6

likely produce some improvement in these figures. It should be noted, however, that the maximum input voltage to the unit can reach 441 Vdc and the peak output current from each phase can go as high as 123 amperes. Since the power output is $\frac{1}{2}$ (E_p x I_p), the switches must, in essence, be capable of a theoretical output of 27,100 watts per phase, or a total output power of 81,300 watts.

The allowable range of input voltage also effects the input filter. The input filter capacitors must provide the following functions, while withstanding the peak input voltage:

1) Reduction of ripple voltage on the internal dc bus when the unit is operated from rectified ac input power.

2) Energy storage necessary to maintain operation during input transient dips.

3) By-pass of the high frequency ripple current generated by the pulse width modulated inverter.

MIL-STD-704 requires equipment to operate normally during a 0.05 second duration loss of input power. To accomplish this, the energy stored would be

$$\frac{10{,}000 \text{ watts}}{.92} \times .05 \text{ sec} = 543 \text{ joules}$$

assuming an efficiency of 92%. If one further assumes a bus voltage of 170 Vdc is sufficient for full output voltage and that the capacitors were initially charged 270 Vdc, one can write the following:

$$\tfrac{1}{2}(270)^2C - \tfrac{1}{2}(170)^2C = 543$$

from which one readily obtains C = 24,700 mfd.

However, it was possible to include only 14,400 mfd within the existing package. This value does meet the needs of functions 1) and 3), however. Normally, of course, two PCU's will be operated in parallel from separate sources so as to avoid this interruption.

The output transformer represents another area in which performance had to be compromised somewhat to minimize the package size. The transformer turns ratio is 6:5. This is sufficient to maintain full output voltage with input voltages as low as 210 Vdc (86 Vac). Ideally, the unit would have provided full output voltage with input voltages as low as 60 Vac. This would have required using a transformer turns ratio of approximately 5:6. Use of the latter ratio would require that the transistors switch 44% more current, however, and would reduce the output filter impedance by 52%. The result would be a larger, less efficient unit. In addition, the ripple current through the input filter capacitors would increase, placing a greater stress on the capacitors.

Other developmental problem areas included the design of the dc current balance circuit and the internal protective circuitry. The dc current balance circuit was incorporated into the design to insure that no significant

dc current would be present in the output transformer. The approach taken was to compare the voltages across two shunts in each of the output bridge circuits by means of differential amplifiers. Unfortunately, the circuit layout is such that the desired voltages are masked by other, extraneous voltages which make the circuit more harmful than helpful. The circuit was eventually disconnected entirely following a failure which resulted in considerable damage to several switch plates.

The switch plates were damaged by failure of the internal protective circuitry to operate as much as by the faulty operation of the balance circuit. Fault protection is given considerable emphasis in the specification; however, this protection primarily relates to the protection of equipment connected to the PCU. Protection of the unit itself was expected to be provided by a circuit successfully used by DECC in other equipment. The circuit is intended to sense an overcurrent

condition by determining that the output switch transistors did not reach saturation voltage within a specific interval after application of the base drive pulse. It turns out, however, that with the available drive current the transistors used in the PCU will support a destructively large collector current while saturated thus negating the circuit function.

The basic problem is that of measuring a relatively small dc current in the presence of a very large ac current.

5.0 CONCLUSIONS AND RECOMMENDATIONS

5.1 POSSIBLE DIRECTIONS

While the prototype PCU's are believed capable of meeting most of the performance specifications, the units did not meet either the size or weight requirements. To meet these requirements the unit would require development of custom hybrid and/or large scale integrated (LSI) circuits. In addition, the

large volume required for cooling fins and air flow may dictate the need for an alternative method of cooling. The system requirements, together with the cost of meeting the requirements, should be carefully reviewed prior to undertaking further development activity.

5.2 IMPROVEMENTS TO THE PROTOTYPE

Assuming that the size and weight of the prototype package are found acceptable, there are several possible improvements which should be considered.

5.2.1 DC Balance

An effective circuit should be incorporated into the design to insure that no dc current flows in the output transformer, saturating the core. The existing circuit might suffice if the physical layout were improved, or possibly an entirely different approach is needed. The basic problem is that of measuring a relatively small dc current in the presence of a very large ac current.

5.2.2 Peak Current Limiter

There is presently no direct measure of the peak current through the inverter switch transistors in order to cause limiting to occur at a safe value. Such a circuit should be added to the existing design. The current transformers might be more appropriately located in the primary side of the output transformer rather than the secondary side.

5.2.3 Adjustable Resistors

There are far too many adjustable resistors incorporated into the design. Wherever possible, these should be replaced with fixed resistors.

5.2.4 Test Points

The prototype is devoid of test points. These must be incorporated into future models, particularily if the adjustable resistors are replaced with select-in-test fixed resistors.

5.2.5 Test Equipment

Test equipment and alignment procedures should be developed for testing the various sub-assemblies in an efficient manner.

5.2.6 Design Review

The prototype PCU's should be thoroughly reviewed and tested to reveal other areas requiring changes prior to undertaking a second generation design.