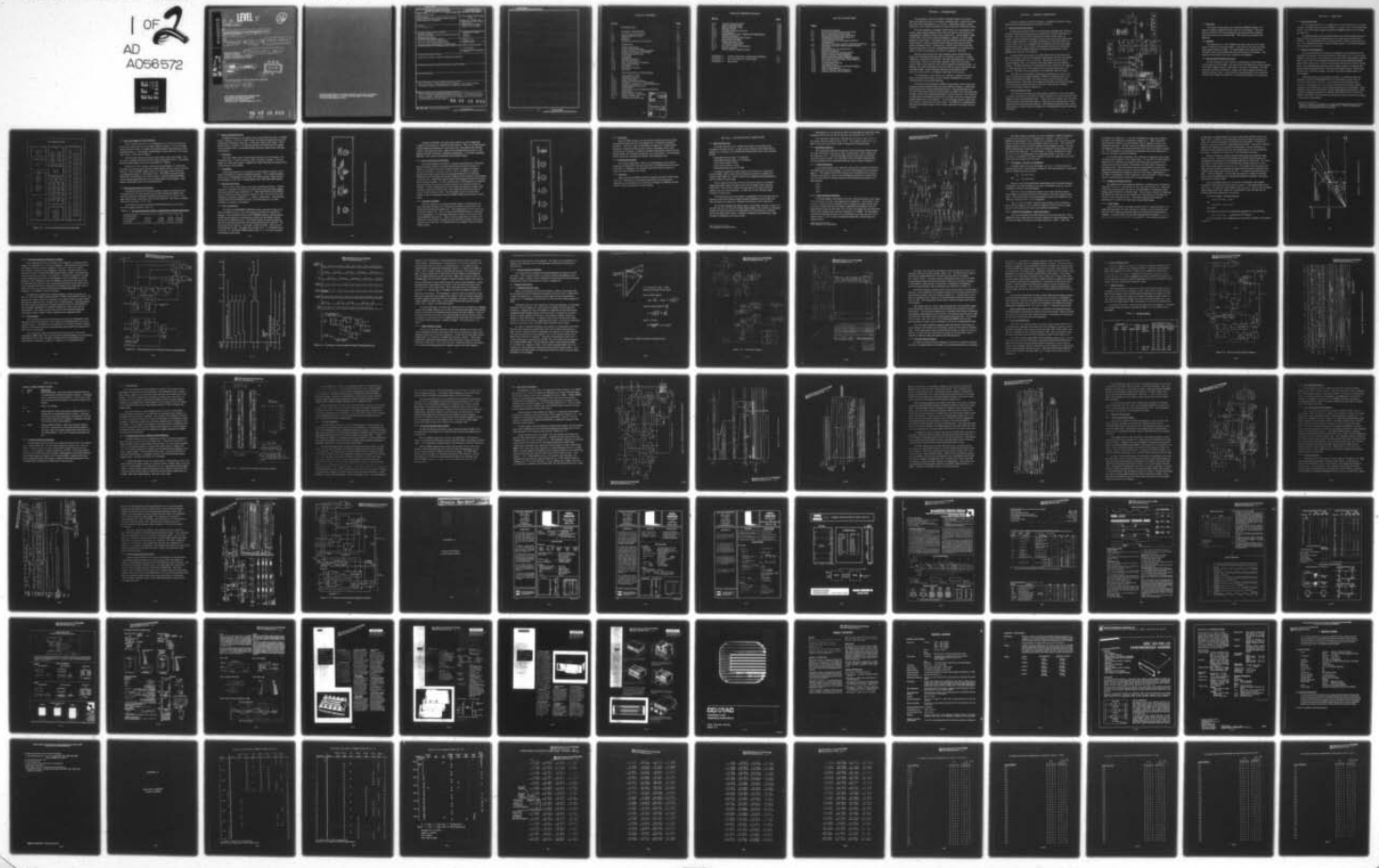
AD-A056 572 RAYTHEON CO WAYLAND MASS EQUIPMENT DIV F/G 17/9
SCAN CONVERTER AND REFRESH MEMORY WITH REMOTE TERMINAL.(U)
JAN 76 J H TURNER F19628-75-C-0156
UNCLASSIFIED ER76-4065 AFGL-TR-76-0175 NL

1 OF 2
AD
A056572



AD A056572

LEVEL II

16

18 AFGL-TR-76-0175

19

6 SCAN CONVERTER AND REFRESH MEMORY WITH REMOTE TERMINAL,

10 J. H. Turner, Jr

Raytheon Company
Equipment Division
Advanced Development Laboratory
Wayland, Massachusetts 01778

12 101 p.

14 ER76-4065

15 F19628-75-C-0156

AD No.
DDC FILE COPY

9 Final Report.
15 Apr[redacted]—10 Dec[redacted]75,

Jan[redacted]76

11

DDC
RECEIVED
JUL 19 1978
E

Approved for public release; distribution unlimited

16 6672 17 06

AIR FORCE GEOPHYSICS LABORATORY
AIR FORCE SYSTEMS COMMAND
UNITED STATE AIR FORCE
HANSCOM AFB, MASSACHUSETTS 01731

78 07 13 013
388 201

Qualified requestors may obtain additional copies from the Defense Documentation Center. All others should apply to the National Technical Information Service.

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER AFGL-TR-76-0175	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) SCAN CONVERTER AND REFRESH MEMORY WITH REMOTE TERMINAL		5. TYPE OF REPORT & PERIOD COVERED Final 75 Apr. 15 - 75 Dec. 10
		6. PERFORMING ORG. REPORT NUMBER ER76-4065
7. AUTHOR(s) J. H. Turner, Jr.		8. CONTRACT OR GRANT NUMBER(s) F19628-75-C-0156
9. PERFORMING ORGANIZATION NAME AND ADDRESS Raytheon Company Equipment Division, Advanced Development Lab Boston Post Road Wayland, MA 01778		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62101F 66720601
11. CONTROLLING OFFICE NAME AND ADDRESS Air Force Geophysics Laboratory Hanscom AFB, Massachusetts 01731 Contract Monitor/Kenneth M. Glover/LYW		12. REPORT DATE January 1976 13. NUMBER OF PAGES
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Scan conversion, meteorological radar display, color contour display, contouring, display refresh memory, image data transmission.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This document is an equipment information report describing a Scan Converter and Refresh Memory with Remote Terminal. The system performs storage, display, and transmission of color-coded contours of processed meteorological radar video data.

78 07 13 013

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

TABLE OF CONTENTS

Section		Page
1.	INTRODUCTION	1-1
2.	GENERAL DESCRIPTION	2-1
2.1	Scan Conversion Processor	2-1
2.2	Memory Interface Units	2-1
2.3	Memories	2-3
2.4	Displays	2-3
2.5	Remote Refresh Memory Receiver	2-3
3.	OPERATION	3-1
3.1	Display Adjustment	3-1
3.2	Contour Threshold Entry	3-1
3.3	Mode and Range Cell Width Selection	3-3
3.4	Scaling and Location of the Origin	3-3
3.5	Marker Spacing Selection	3-4
3.6	Time Code	3-4
3.7	Crosshatch	3-4
3.8	Multiple Data Source	3-4
3.9	Data Transmission	3-4
3.10	Data Transmission Test Modes	3-7
3.11	Reception of Images	3-7
3.12	Test Mode	3-8
3.13	Interlaced Scan Mode	3-8
3.14	Data Save	3-8
4.	DETAILED CIRCUIT DESCRIPTION	4-1
4.1	Angle Interface Unit	4-1
4.2	Coordinate Converter	4-2
4.2.1	Angle Parameters	4-2
4.2.2	Fixed Constant Multipliers	4-2
4.2.3	PPI Mode - True 12 x 12 Multipliers	4-4
4.2.4	Address Accumulators - Card 2 and Card 3	4-4
4.2.5	Range and Altitude Markers	4-5
4.2.6	CAPPI Mode	4-5
4.2.7	Coordinate Converter/Integrator Interface	4-8
4.2.8	Synchronizer	4-8
4.2.9	Angle Interface Timing	4-12
4.2.10	Earth Curvature Correction	4-13
4.3	Display Control Unit	4-13
4.3.1	Timing and Control Logic	4-13

ACCESSION for
NTIS White Section
DDC Buff Section
UNANNOUNCED
JUSTIFICATION
BY
DISTRIBUTION/AVAILABILITY CODES
Dist. AVAIL. and/or SPECIAL
A

TABLE OF CONTENTS (Continued)

Section		Page
4.3.2	Ancillary Data Formatter	4-17
4.4	Video Distribution Unit	4-18
4.5	Memory Interface Units	4-19
4.5.1	Memory Cycles	4-19
4.5.2	Parallel-To-Serial Converter	4-22
4.5.3	Color Encoder	4-23
4.5.4	Modify/Restore Logic, Register and Multiplexers	4-23
4.5.5	Contour Generator	4-25
4.5.6	Write Data and Read Data Busses	4-26
4.6	Serial Data Formatter	4-27
4.7	Display Receiver Unit	4-33
4.7.1	Timing and Control Logic	4-33
4.7.2	Test Pattern Generator	4-35
4.7.3	Receiver Counters and Registers	4-35
4.7.4	Serial Correlator	4-35
4.8	Remote Memory Interface Units	4-37
APPENDIX A	Product Information on Sub-System Modules	A-1
APPENDIX B	Read-Only-Memory Truth Tables	B-1
APPENDIX C	Memoranda	C-1

LIST OF ILLUSTRATIONS

Figure		Page
2-1	SCRM Block Diagram	2-2
3-1	Scan Conversion Processor Front Panel	3-2
3-2	Data Transmission Control Panel	3-5
3-3	Remote Refresh Memory Control Panel	3-7
4-1	Coordinate Converter Block Diagram	4-3
4-2	CAPPI Address Selection	4-7
4-3	Timing Interface for Coordinate Converter and Integrator	4-9
4-4	Integrator Coordinate Converter Timing Waveforms	4-10
4-5	Coordinate Converter Memory Buffer Timing Waveforms	4-11
4-6	Earth Curvature Correction Term	4-14
4-7	DCU Block Diagram	4-15
4-8	Display Format and Timing Diagram	4-16
4-9	Memory Interface Block Diagram	4-20
4-10	Memory Interface Timing Diagram	4-21
4-11	Color Encoder Switches and Block Diagram	4-24
4-12	SDF (Serial Data Formatter) Block Diagram	4-28
4-13	Serial Data Format	4-29
4-14	Transmit Mode Timing	4-30
4-15	Test Mode Timing	4-32
4-16	DRU (Display Receiver Unit) Block Diagram	4-34
4-17	DRU Timing Diagram	4-36
4-18	Serial Correlator and Waveforms	4-38
4-19	Memory Interface Block Diagram	4-39

SECTION 1. INTRODUCTION

This equipment converts the polar-coordinate outputs of a weather radar and signal processor to cartesian-coordinate form, contours the video, then stores the resulting data in any of four independent image-oriented memories, each of which refreshes one raster-scan color television monitor.

The most significant advantage of this system over conventional monochrome radar-image-storage devices lies in the ability of the operator to unambiguously recognize sixteen color-coded levels. Stored images of RHI or PPI radar scans can be retained indefinitely, updated, or erased independently of each other. Front-panel controls determine distance scaling, origin location, range and altitude marker spacing and range cell width. Contour threshold colors - 0 (black) thru 15 (red)--and levels (0 thru 99) having been set up on an array of thumbwheel switches can be entered into either or both of the displays in the form of a legend or color key.

Memory requirements have been limited to about 328,000 bits per display by performing operations such as coordinate conversion, scaling, translation, introduction of markers, and video contouring prior to storage of the image. Each of the memories contains a 248 x 255 array with a four-bit code to represent the color and/or intensity of individual points. In addition, the contour threshold colors and levels as well as parameters such as antenna angle, marker spacing, and time are presented within a 248 x 70 ancillary data area along the right edge of each picture.

The image data in any memory are accessed, combined with appropriate synchronization codes, and are serially transmitted to a remote refresh memory upon manual initiation.

The Remote Refresh Memory (RRM) accepts binary serial image data having a certain specified format and synchronization scheme, as generated by the Master Scan Converter/Refresh Memory. Upon establishing word and line synchronism with the incoming signal, the RRM stores the image data in either or both of its independent display-refresh memories. Each memory is continuously sequentially accessed and its output converted to analog video signals which drive a color display. The stored image remains visible until it is erased or written over by a new image. The RRM has a comprehensive self-test mode which quickly verifies proper operation of virtually all of its circuitry.

SECTION 2. GENERAL DESCRIPTION

The block diagram presented in Figure 2-1 should be referred to while reading the following description of the scan converter.

2.1 Scan Conversion Processor

Front panel controls related to scan-converter operation are located on the Scan Conversion Processor and are connected to various cards within it as shown. The Scan Conversion Processor accepts synchro inputs for antenna azimuth and elevation angles as well as video and timing signals from a radar signal processor. The input information is converted in real time from its polar form to a rectangular form suitable for entry into the image-oriented memories. The processor also generates all memory addresses, timing, and control signals needed by the memory-interface units, plus alphanumeric data and color patches.

Located within the processor is a SDF (Serial Data Formatter) which generates memory addresses sequentially upon manual initiation and accepts the corresponding data from any memory. Interleaved with appropriate synchronization codes, the resultant serial data output drives an external modem. The SDF operates in bit synchronism with a clock from the modem; at a 2400 kHz clock rate, the transmission of one image takes about 2.67 minutes. The SDF also has capability for two different self-test modes.

The SDF also accomplishes multiplexing of alphanumeric data to and from an alphanumeric keyboard display. Whenever a display image is not being transmitted by the SDF, the modem input is made available to the keyboard display. The modem data output is dedicated to the keyboard display thus allowing the remote operator to "converse" with the data originator even during display image transmission.

2.2 Memory Interface Units

Each Memory Interface Unit (MIU) performs parallel to serial and digital to analog conversions on its memory output to generate red, green and blue video signals for the corresponding display. These units also execute code conversion and contouring on the incoming video as a function of color patches and contour levels stored in the associated memory. Intermediate storage and logic in each MIU enables it to alter data in its memory as commanded by the Scan Conversion Processor.

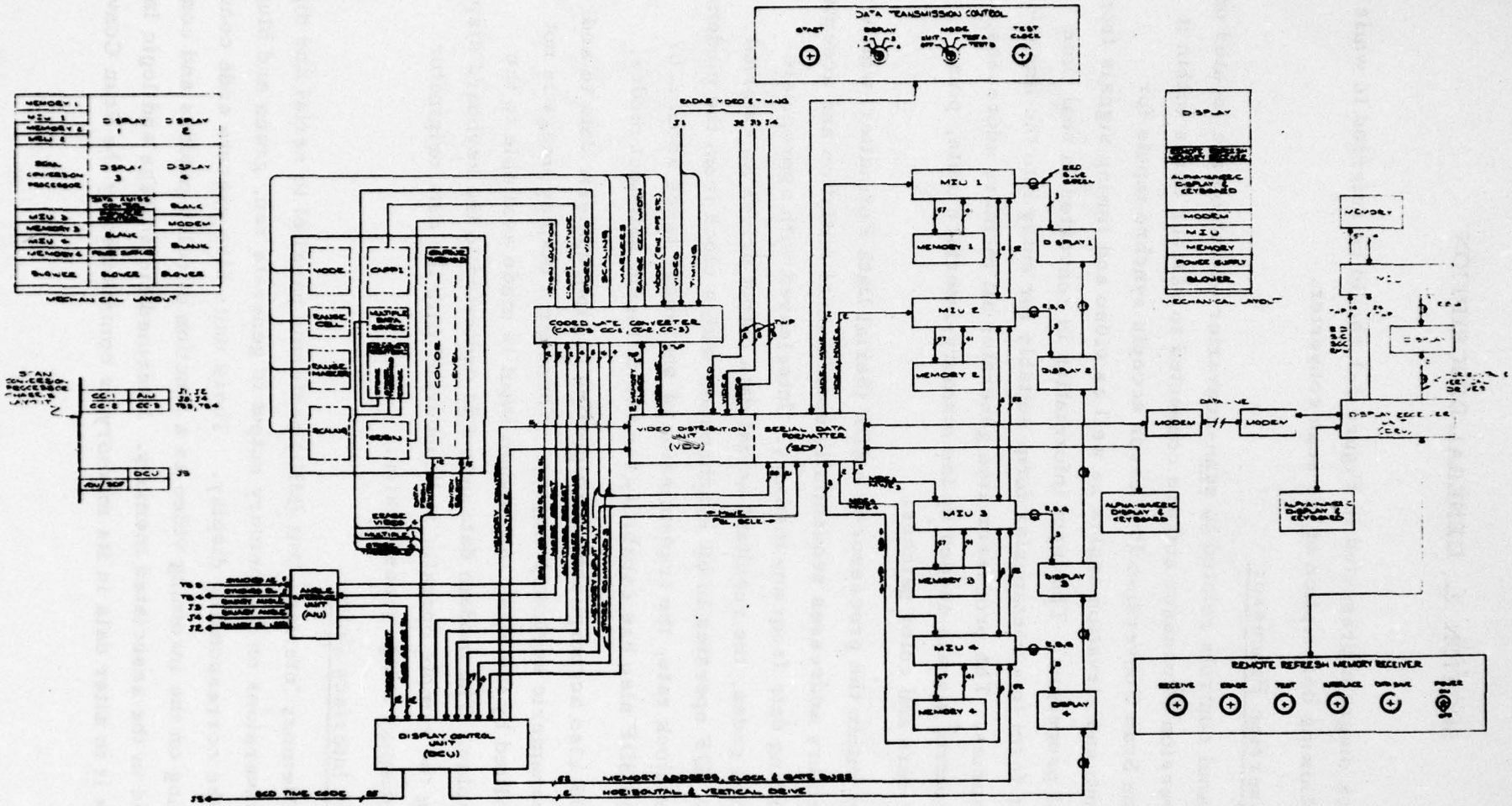


Figure 2-1. SCRM Block Diagram

2.3 Memories

The image storage media are conventional AMPEX magnetic core memory systems having 8192 40-bit words for each display. They have split cycle times of 750 nanoseconds and self-contained power supplies which also power each associated MIU. Data sheets are included in the Appendix.

2.4 Displays

The displays are 19-inch CONRAC delta-gun color units of the type used as monitors in television studies. Each unit has red, green and blue video inputs driven by its MIU. All of the displays are synchronized by the same H and V drive pulses from the Scan Conversion Processor. Data sheets for the monitors have been included in the Appendix.

2.5 Remote Refresh Memory Receiver

On the front panel of this drawer are mounted all controls needed for normal operation of the RRM. The only circuit card within the receiver drawer is the DRU (Display Receiver Unit) which is the heart of the RRM. The DRU generates all memory addresses, timing, and control signals needed by the memory interface units. It also detects the synchronization codes within the incoming data signal and generates a simulated data signal for test purposes.

SECTION 3. OPERATION

3.1 Display Adjustment

Each monitor should have its VIDEO switch in the 0 dB position for normal viewing. The MONO position may be helpful, in certain cases, for distinguishing colors. The OFF position might be useful as a standby mode in lieu of turning the power off.

The BRIGHTNESS control should be used to set the black background level (observe the area around the alphanumerics) to a point near the threshold of visibility. The CONTRAST control can then be used to obtain the desired intensity. The illuminated number at the top of each monitor is red when information is being stored in its memory.

3.2 Contour Threshold Entry

The contour threshold switches are arranged in the same pattern on the front panel of the Scan Conversion Processor (see Figure 3-1) as on the actual displays. Any of the 15 color-selectors can be set to any color between 0 (black) and 15 (red).* The 14 level-switches should be set up in ascending magnitude order from bottom to top. An area of the display will take on a color of a given patch if the corresponding signal processor output is equal to or greater than the level below the patch and less than the level above the patch. Should these levels be set to the same number, the color in the patch between them will never appear.

Having set up the contour threshold switches, the operator need only depress the STORE THRESHOLDS button for each display in which this set of contour thresholds is desired. The previous set of thresholds in that memory is then replaced by the new set without affecting the other display information which had been entered using the previous set of thresholds. (This situation, where the thresholds do not match the displayed information, can be avoided by pushing the appropriate ERASE VIDEO button before entering new contour thresholds.) All subsequent incoming video will be contoured according to the new set of thresholds.

---

*Color 15, however, is reserved for range and altitude markers and has the property of not allowing itself to be written over. Patterns appearing in this color can only be removed by erasure.

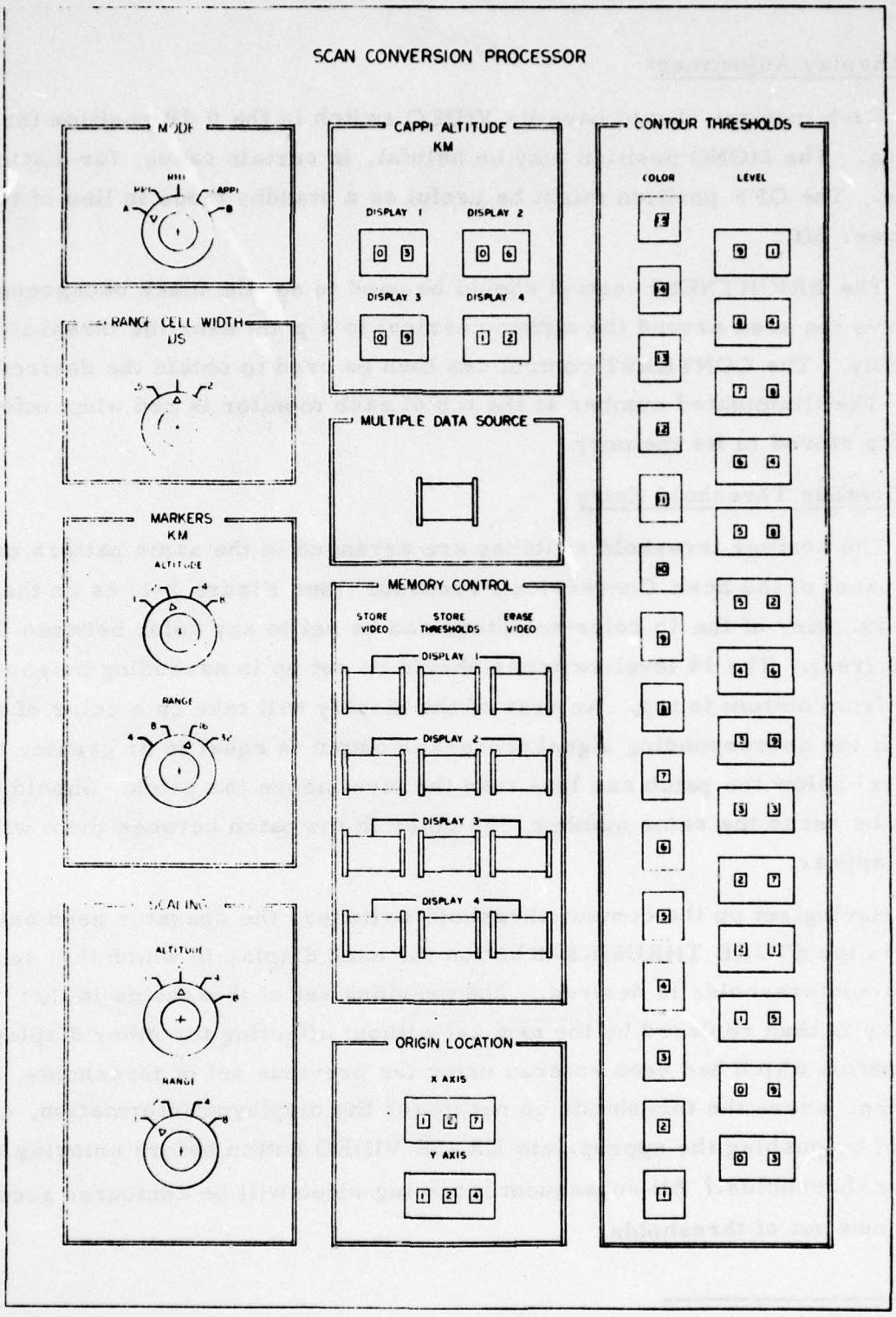


Figure 3-1. Scan Conversion Processor Front Panel

3.3 Mode and Range Cell Width Selection

These controls must be set to correspond with the radar scan sequence and the operating conditions of the radar signal processor. In the RHI (Range Height Indicator) mode, the display will present ground range along the X axis and height along Y. The antenna azimuth angle is shown after AZ, in the lower right corner, to the nearest degree.

The PPI (Plan Position Indicator) mode yields a plan-view display, with the Y-axis running North-South and the X-axis running East-West. The antenna elevation angle appears after EL to the nearest 0.1 degree.

Either RHI or PPI formats can be set up in any display or combination of displays by depressing the desired STORE VIDEO switches, which are active when lit. When a STORE VIDEO switch is on, the large number above the corresponding display is illuminated in red. The CAPPI (constant altitude PPI) mode, also permits use of either display, with the CAPPI ALTITUDE switch settings appearing after AL at the lower right of each display. Each display represents a PPI at the altitude selected.

3.4 Scaling and Location of the Origin

The ORIGIN LOCATION switches provide a means of locating the point corresponding to the radar antenna at any position within the display area. The units employed correspond to display elements at (X, Y); (0, 0) is in the upper right corner, while (249, 247) is in the lower left. The center, normally used for PPI formats, is (127, 124).

ALTITUDE (RHI only) and RANGE SCALING switches can be used to vary the scaling as listed in Table 3-1.

Table 3-1. Full Scale Range and Altitude vs Scale Switch Positions (RHI Mode)

SWITCH POS:	1	2	4	8
ALTITUDE:	128 KM	64 KM	32 KM	16 KM
RANGE:	256 KM	128 KM	64 KM	32 KM

3.5 Marker Spacing Selection

MARKER switches are provided to select ALTITUDE (RHI only) or RANGE marker spacing. In PPI or CAPPI modes, the selected range marker spacing is indicated in kilometers after RM = at the lower right of the display. When the RHI mode is employed, the selected markers are indicated in the display in the following format: M (altitude marker spacing); (range marker spacing) in kilometers.

3.6 Time Code

The lower right corner of each display contains time information in the following format: T (day of the year); (hour of the day); (minute). The time readout of a particular display is updated only while information is being stored in the memory of that display.

3.7 Crosshatch

Mode switch position B is provided as a test position in which a crosshatch is developed for monitor alignment purposes. The crosshatch appears in the color corresponding to full-scale video (the top patch), while the background appears in the color corresponding to zero video (the bottom patch).

3.8 Multiple Data Source

There are four video inputs to the scan conversion processor. Timing signals for coordinate conversion are derived from radar and range triggers associated with the input connected to J1. When MULTIPLE DATA SOURCE has been selected, the video signals at inputs J1, J14, J13 and J12 are made available for storage on displays 1, 2, 3 and 4, respectively. In the absence of MULTIPLE DATA SOURCE selection, the video input on J1 is made available for storage on all displays.

3.9 Data Transmission

The DATA TRANSMISSION CONTROL panel is pictured in Figure 3-2. When the MODE switch is in its OFF position, the other two controls are disabled. With the MODE switch in the TRANSMIT position, depressing the START button initiates the transmission of data from the display memory selected by the SOURCE switch. The START button will light immediately and will remain illuminated until the transmission has been completed. The transmission time duration, in seconds, is given by 386/f, where f is the clock frequency in kHz. The light will not come in if: 1) the MODE switch is at OFF, 2) any STORE VIDEO switch is ON, or 3) no clock is present at the Modem Clock Input.

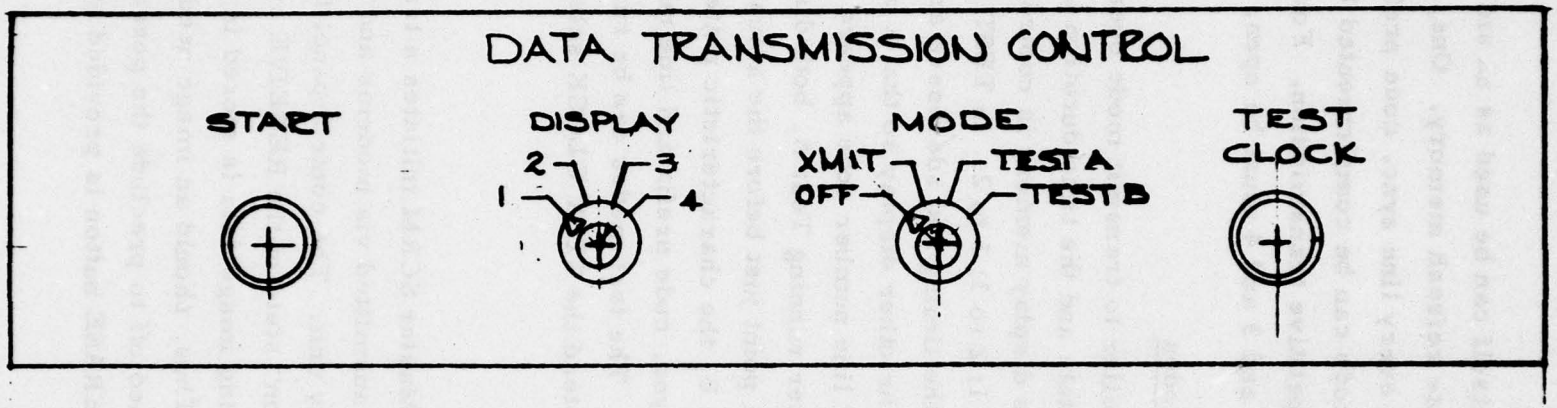


Figure 3-2. Data Transmission Control Panel

A switch on the SDF card itself can be used as an aid in diagnosing troubles in the data link or remote refresh memory. One, two or three errors can be purposely introduced into every line sync. code prefix with switches 1 and 2. The entire line sync. code can be complemented by switch 3, and switch 4 permits continuous, repetitive transmission. For normal operation, switches 1 and 2 must be closed and 3 and 4 must be open.

3.10 Data Transmission Test Modes

Test mode operation is similar to transmit mode operation, except that the serial output is held to one state and the time duration is doubled. In TEST A, the image in the source display memory is copied into another memory as follows: 1 to 4; 4 to 1; 2 to 3; 3 to 2. In TEST B, a similar process takes place except that the timing and addresses are scrambled between the source display and the other display so that a pattern corresponding to the line sync. code prefix and line number code appears instead of the image from the source display. If, after running Test A, both displays are identical, then serial data are correct at a point just before the actual line driver in the SDF. If, after running Test B, the characteristic pattern (compare with a photo) is observed, then the sync. code prefix and line number code are correct at the line driver input. The test modes can be run without the modem clock by substituting instead the TEST CLOCK selected on the control panel.

3.11 Reception of Images

When the operator of the Master SCRM initiates a transmission, the data describing an image are transmitted via modems and data line to the Remote Refresh Memory display unit. The control panel for the remote unit is shown in Figure 3-3. The "on" state of the RECEIVE switch is indicated by its illumination. The incoming image data is stored in the memory only if the RECEIVE switch is on. Thus, should an image need to be saved, the RECEIVE switch should be turned off to preclude the possibility of its being written-over by new data. An ERASE button is provided to clear the entire display image.

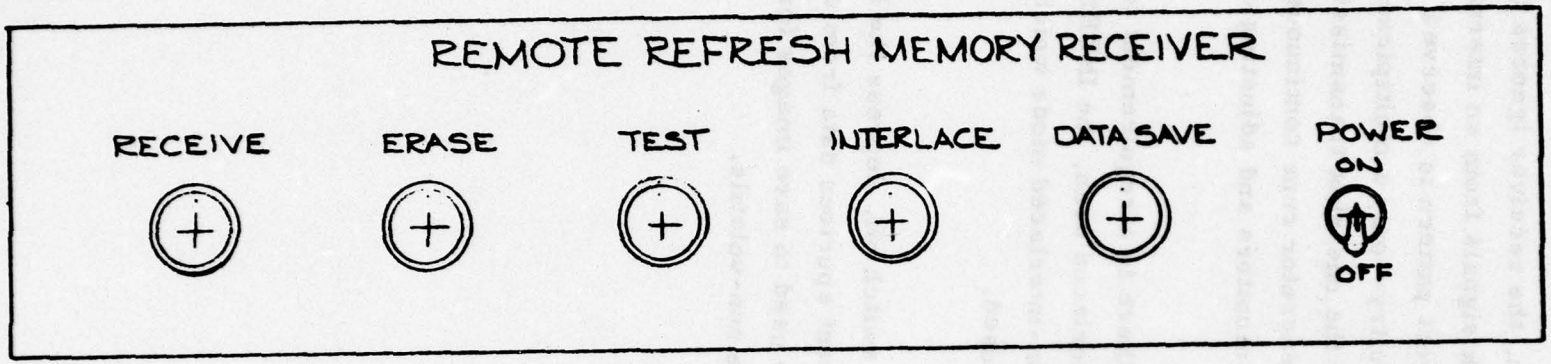


Figure 3-3. Remote Refresh Memory Control Panel

3.12 Test Mode

When the TEST switch is on, the receiver ignores the normal inputs and instead accepts data and clock signals from an internal test pattern generator. This test, if the correct pattern is observed, verifies proper operation of almost all RRM circuitry--only a multiplexer and the line receivers are not tested. Unlike the one-shot transmission of data from the Master SCRM, the test pattern generator runs continuously. The test pattern is also useful for converging the monitors and adjusting colors.

3.13 Interlaced Scan Mode

If, in future applications, there is a requirement to drive a device requiring a standard 525-line interlaced scan, the INTERLACE switch must be turned on. Otherwise, the non-interlaced mode which is better for jitter-free close viewing can be used.

3.14 Data Save

While turning the POWER switch off, depress the DATA SAVE button next to it. This action will prevent spurious data from entering the memories at turn-off and can be used to save images for indefinite periods of time, since the memories are non-volatile.

SECTION 4. DETAILED CIRCUIT DESCRIPTION

4.1 Angle Interface Unit

The Angle Interface Unit, located in the upper-rear position of the coordinate converter drawer, accepts synchro azimuth and elevation data in standard R_1, R_2 and S_1, S_2, S_3 format and converts these data to the following outputs:

Scaled BCD azimuth angle, 1° resolution
Scaled BCD elevation angle 0.1° resolution
Sine/cosine azimuth 13 bits
Sine/cosine elevation 13 bits
Elevation greater than 12.65° flag

Azimuth and elevation synchro inputs are converted to 14-bit binary numbers (MSB = 180°) in Data Device Corporation synchro-to-digital converters model ESDC-6*. These converters are inhibited during sampling by the S/D inhibit command input.

Binary angle data are next converted to sine and cosine in an Interface Engineering sine/cosine controller model 109 and angle-to-sine converter model 108*. The controller adapts the angle-to-sine converter to full four quadrant sine and cosine operation. A logic zero on the controller input terminal 23 selects sine.

The sine/cosine converter channel is multiplexed once each PRF interval. between azimuth and elevation inputs through multiplexers A16 through A18. This technique was employed to optimize the efficiency of the converters.

An Interface Engineering binary angle to scaled BCD converter, model 107,* provides the drive for the CRT antenna angle display. This converter is switched between azimuth and elevation by multiplexers A11 through A14, controlled by the front panel mode switch. Azimuth is displayed in the RHI mode; while elevation is displayed in all other modes.

*See Appendix for Data Sheets.

Multiplexers A3, A4 and A5 line shift the scaled BCD four lines down when displaying elevation to provide the increase in resolution from 1^{o} to 0.1^{o}.

The magnitude comparators, A20 and A25, generate a logic one when the antenna elevation angle exceeds 12.65^{o}. This output is used by the coordinate converter in the CAPPI mode to initiate the 2^{o} elevation step.

4.2 Coordinate Converter

The Coordinate Converter derives the cartesian memory address from the radar parameters of elevation angle, azimuth angle, radar trigger and the range gate clock. The azimuth angle and elevation angle are sampled once every radar period to form the basis of the coordinate transformation. The block diagram of the Coordinate Converter unit is shown in Figure 4-1.

4.2.1 Angle Parameters

In the angle interface unit, there are two synchro-to-digital converters; one dedicated to the azimuth angle, θ, and the other dedicated to the elevation angle, ϕ. The outputs of each S/D converter are multiplexed into a sin/cos converter such that by control of the multiplexer and function switch of the sin/cos converter, the following functions can be obtained and stored in a D type register:

$\sin \phi$
$\cos \phi$
$\sin \theta$
$\cos \theta$

4.2.2 Fixed Constant Multipliers

In the RHI display, the altitude is R $\sin \phi$, and the projection of the range is R $\cos \phi$ where R is the range expressed in kilometers. Card number 1 has two 12 x 12 fixed constant multipliers which multiply the single function input by a fixed constant such that the output is expressed in kilometers with the binary point 12 bits from the LSB. For a 2 μsec unit range cell, the conversion factor (radar distance) built into the multipliers is .2998046. All subsequent calculations following the fixed constant multipliers are done directly in kilometers which is a very useful simplification especially in determining the range markers.

---

*See Appendix for Data Sheets

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

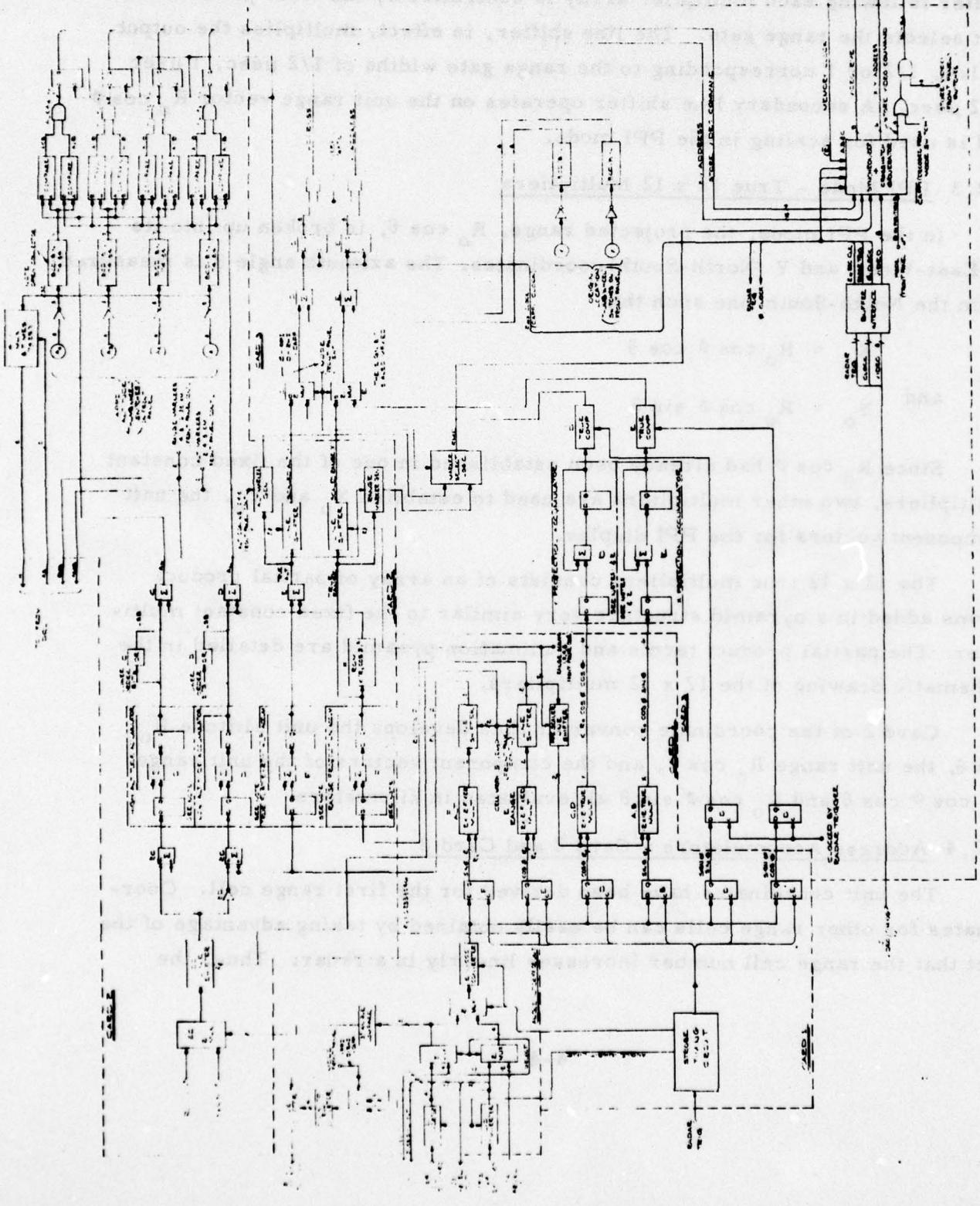


Figure 4-1, Coordinate Converter
Block Diagram

The fixed constant multipliers are each composed of adders arranged in an array such that the input is multiplied by a constant. Groups of 4-bit adders are pyramided to form a subset of 4-bit numbers with all the carry-outs fed into the carry-inputs of the next higher order 4-bit array. The schematic diagram shows the array in detail and also in block diagram format. The line shifter following each multiplier array is controlled by the front panel switch that selects the range gate. The line shifter, in effect, multiplies the output by 1/4, 1/2 or 1 corresponding to the range gate widths of 1/2 μsec, 1 μsec or 2 μsec. A secondary line shifter operates on the unit range vector $R_o \cos \phi$ and is used for scaling in the PPI mode.

4.2.3 PPI Mode - True 12 x 12 Multipliers

In the PPI mode, the projected range, $R_o \cos \theta$, is broken up into its X (East-West) and Y (North-South) coordinates. The azimuth angle θ is measured from the North-South line such that

$$X_o = R_o \cos \phi \cos \theta$$

and

$$Y_o = R_o \cos \phi \sin \theta$$

Since $R_o \cos \phi$ had already been established in one of the fixed constant multipliers, two other multipliers are used to establish X_o and Y_o, the unit component vectors for the PPI display.

The 12 x 12 true multipliers consists of an array of partial product terms added in a pyramid structure very similar to the fixed constant multiplier. The partial product terms and summation pyramid are detailed in the schematic drawing of the 12 x 12 multipliers.

Card 2 of the coordinate converter thus develops the unit altitude $R_o \sin \theta$, the unit range $R_o \cos \phi$, and the component vectors of the unit range $R_o \cos \phi \cos \theta$ and $R_o \cos \phi \sin \theta$ all evaluated in kilometers.

4.2.4 Address Accumulators - Card 2 and Card 3

The unit coordinates have been derived for the first range cell. Coordinates for other range cells can be easily obtained by taking advantage of the fact that the range cell number increases linearly in a radar. Thus, the

coordinates for range cell j + 1 are the coordinates for range cell j added to the value of the respective coordinates of range cell 1. This accumulator type structure is shown in the block diagram and is repeated 6 times in the coordinate converter. The unit vectors are loaded into each accumulator at the beginning of each radar period and at the same time the old data is cleared out. The accumulator is clocked by the range gate clock of the integrator to form the cartesian coordinate addresses.

For the RHI mode of operation, the Y address corresponds to the scaled altitude and the X address is the scaled range. For the PPI or CAPPI mode of operation, the Y address corresponds to the North-South component of the range vector and the X address corresponds to the East-West component of the range vector. The mode switch controls the multiplexer to select the appropriate coordinates as shown in the block diagram. After the multiplexer, constants controlled by thumbwheel switches can be added independently to the X and Y coordinates to affect translation in both directions. A hard limiter circuit is used to prevent overflow and erroneous addresses.

4.2.5 Range and Altitude Markers

The outputs of both the range and altitude accumulators are in kilometers (see para. 4.2.2) i.e., the 13th bit is 1 KM, the 14th is 2 KM, etc. Detection of the clock cycle at which time the bit corresponding to a preselected range changes state is used as the marker pulse. The circuitry consists of comparing the selected bit with the same bit delayed one clock period in an exclusive or circuit to form the marker pulse. The marker pulse goes through the synchronizer to produce the range mark enable (RME) signal.

4.2.6 CAPPI Mode

In the CAPPI mode, the antenna sweeps 360°, or a segment thereof, at a single elevation angle and upon reaching its starting or terminal position (for less than 360° sweep) the elevation angle is incremented and the process is repeated. A typical CAPPI will use the following elevation angles, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 14, 16, 18 and 20°. This volume scan permits

the operator to crudely establish a map of a prescribed altitude or many altitudes, since, in general, each radar beam will pass through all possible altitudes. By carefully selecting and storing the incoming data, it is possible to develop a constant altitude PPI map at any given altitude. Because the elevation angle of the antenna is incremented in small steps, a map at precisely the desired elevation would provide very few sample points; it is the established procedure to sample the elevation at or near the desired elevation.

Figure 4-2 shows a constant altitude intersecting three different angle vectors or rays. The solid lines represent the CAPPI elevation angles and the dotted lines represent elevation angles between the CAPPI rays. For elevation angle ϕj, information is recorded when the altitude reached by the altitude vector associated with the ray at $\phi j + 1/2$ is equal to the preselected altitude, similarly the data recording is stopped when the altitude reached by the altitude vector associated with the ray at $\phi j - 1/2$ equals the preselected altitude. From the diagram, it can be seen that there are no gaps in obtaining all the altitude information for a preselected altitude as the beam increments discretely in elevation angle.

In the coordinate converter, the altitude is developed in the altitude accumulator from the unit altitude vector $R_o \sin\phi$. A unit high altitude vector $R_o \sin(\phi + 1/2)$ and a unit low altitude vector $R_o \sin(\phi - 1/2)$ are also developed and introduced into their respective accumulators to form the high and low altitude addresses respectively, A_H and A_L.

For small angles, the approximations

$$\sin(\phi + 1^\circ) \approx \sin\phi + \sin 1^\circ$$

and

$$\sin(\phi - 1^\circ) \approx \sin\phi - \sin 1^\circ$$

were used.

The selection criteria for a preselected altitude A_j is the following:

$$A_L \leq A_j \leq A_H \quad ; \text{ store data in } j^{th} \text{ memory}$$

For each altitude, two comparators are used and are shown in the diagram of card 2.

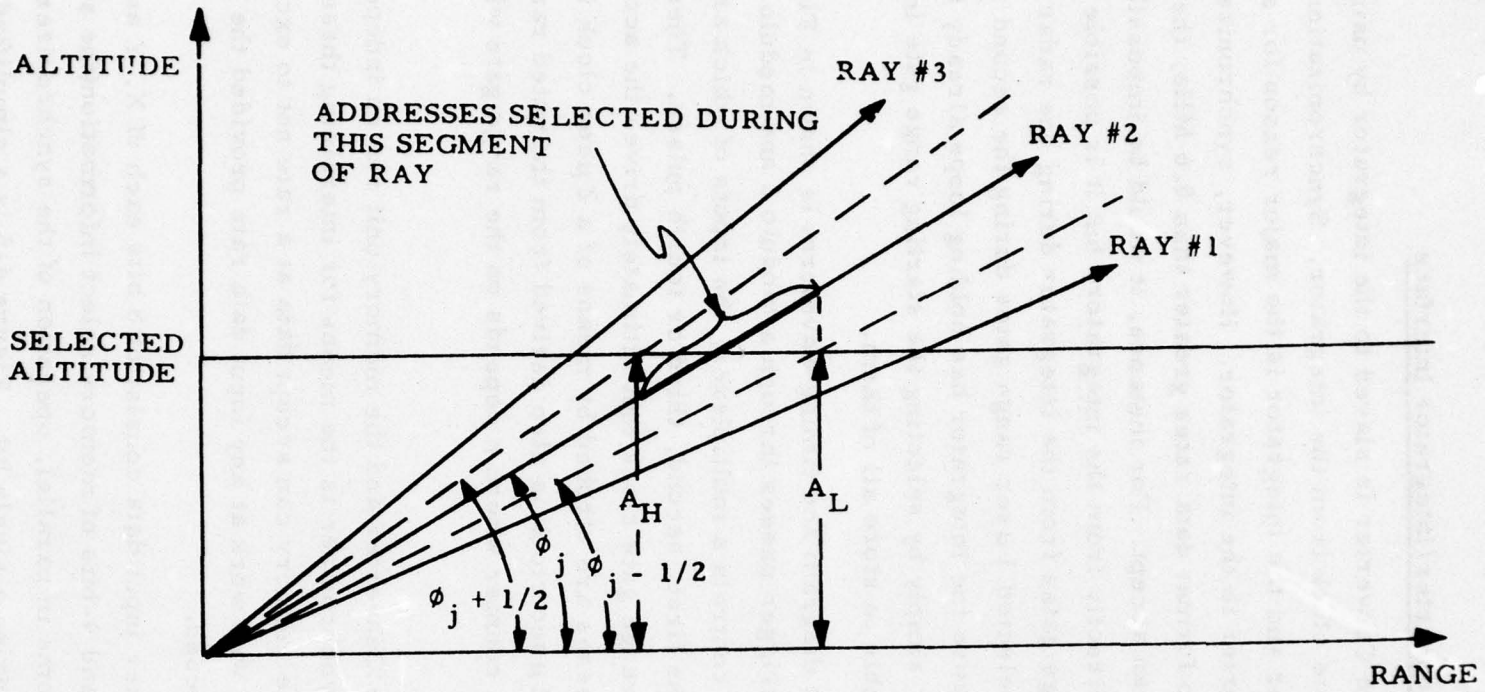


Figure 4-2. CAPPI Address Selection

4.2.7 Coordinate Converter/Integrator Interface

The Coordinate Converter is slaved to the integrator by using the radar trigger and range gate clock from the integrator. Synchronization between the Coordinate Converter and the integrator is the major reason for slaving the coordinate converter to the integrator. However, synchronization is not sufficient in order to format data rates greater than 0.6 MHz, the fastest data rate the memories can accept. For instance, it would be impossible to accept 1 μsec range gates directly from the integrator, but it is possible to receive alternate 1 μsec range gates from the integrator during one radar period and the previously non-selected 1 μsec range gates during the second radar period. This is possible because the integrator has holding loops already built into its output circuitry and, simply by selecting the starting range gate in a sequence, it is possible to store all of them.

A simple block diagram and timing waveform is shown in Figures 4-3 and 4-4. The radar trigger passes through a modulo 2 and modulo 4 counter. The output of the counter controls a multiplexer, the inputs of which are gate pulses that start on either the first, second, third or fourth pulses. These gate pulses are used to gate the range gate clock that ultimately drives the accumulators. The coordinate addresses are strobed by means of a 2 μsec clock into the synchronizer. The 2 μsec clock is also derived from the gated range gate clock and a modulo n counter where n depends on the range gate width.

4.2.8 Synchronizer

The Coordinate Converter and the memory unit run on independent clocking signals and the synchronizer is the means for interfacing these two asynchronous systems. The memory can accept data at a rate not to exceed 0.6 MHz, and the synchronizer will work at any input data rate provided the maximum 0.6 MHz rate is not exceeded.

The synchronizer input data consist of 8 bits each of X, Y and video information, RME, and 4-bits of memory select information(the store commands). Since these 29 bits come in parallel, operation of the synchronizer can be understood by considering a single bit. Figure 4-5 is a simplified block

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

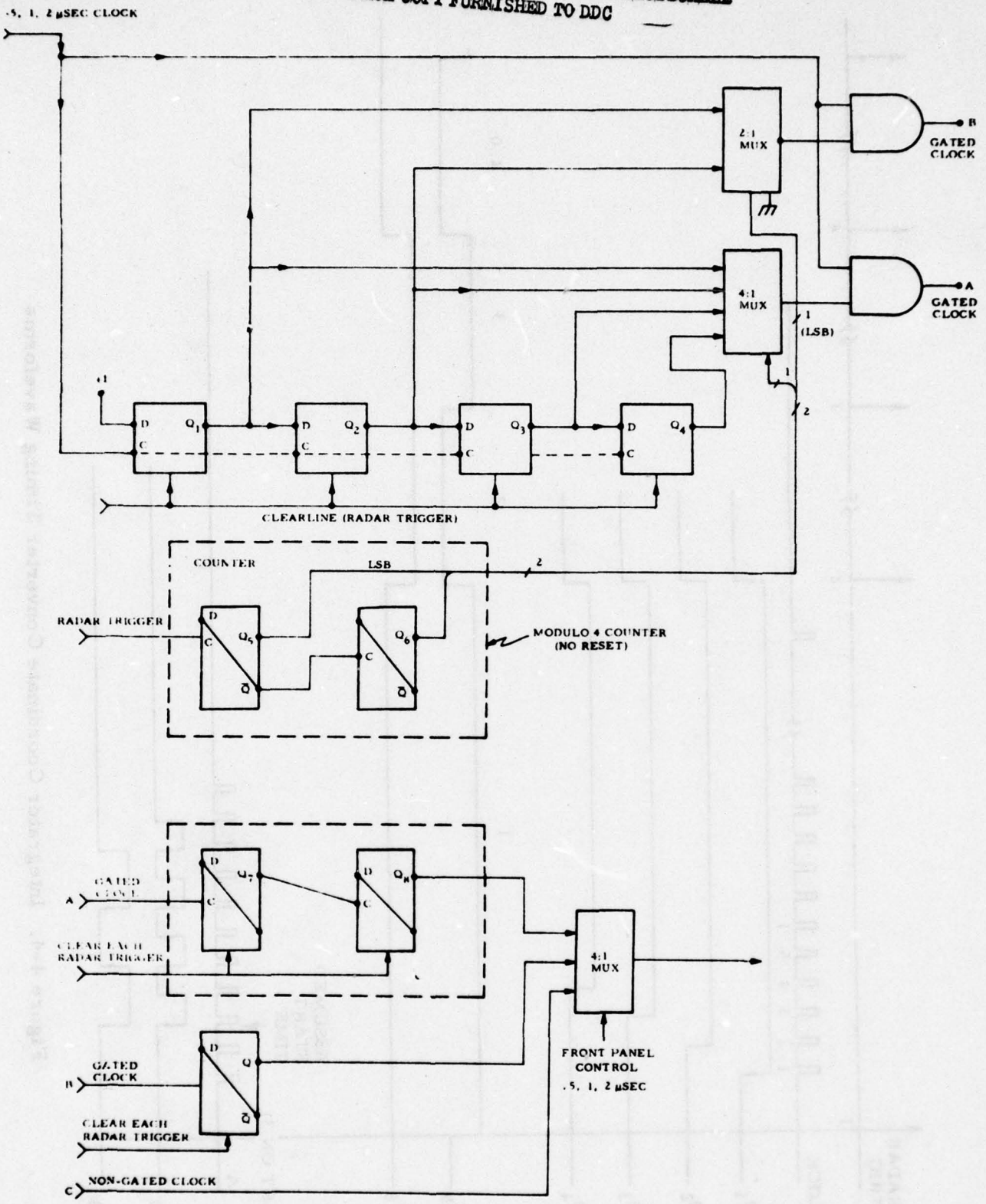


Figure 4-3. Timing Interface for Coordinate Converter and Integrator

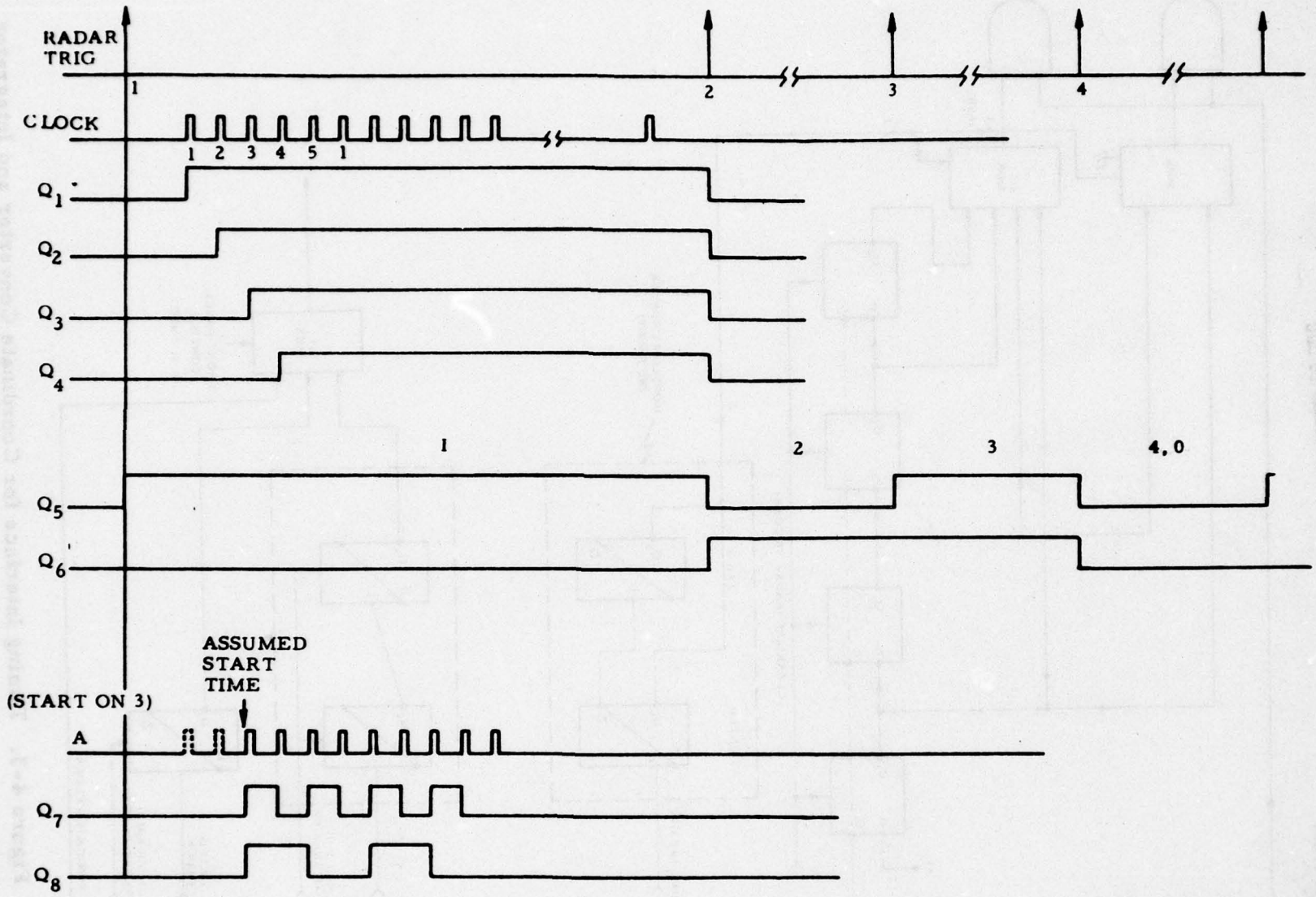


Figure 4-4. Integrator Coordinate Converter Timing Waveforms

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

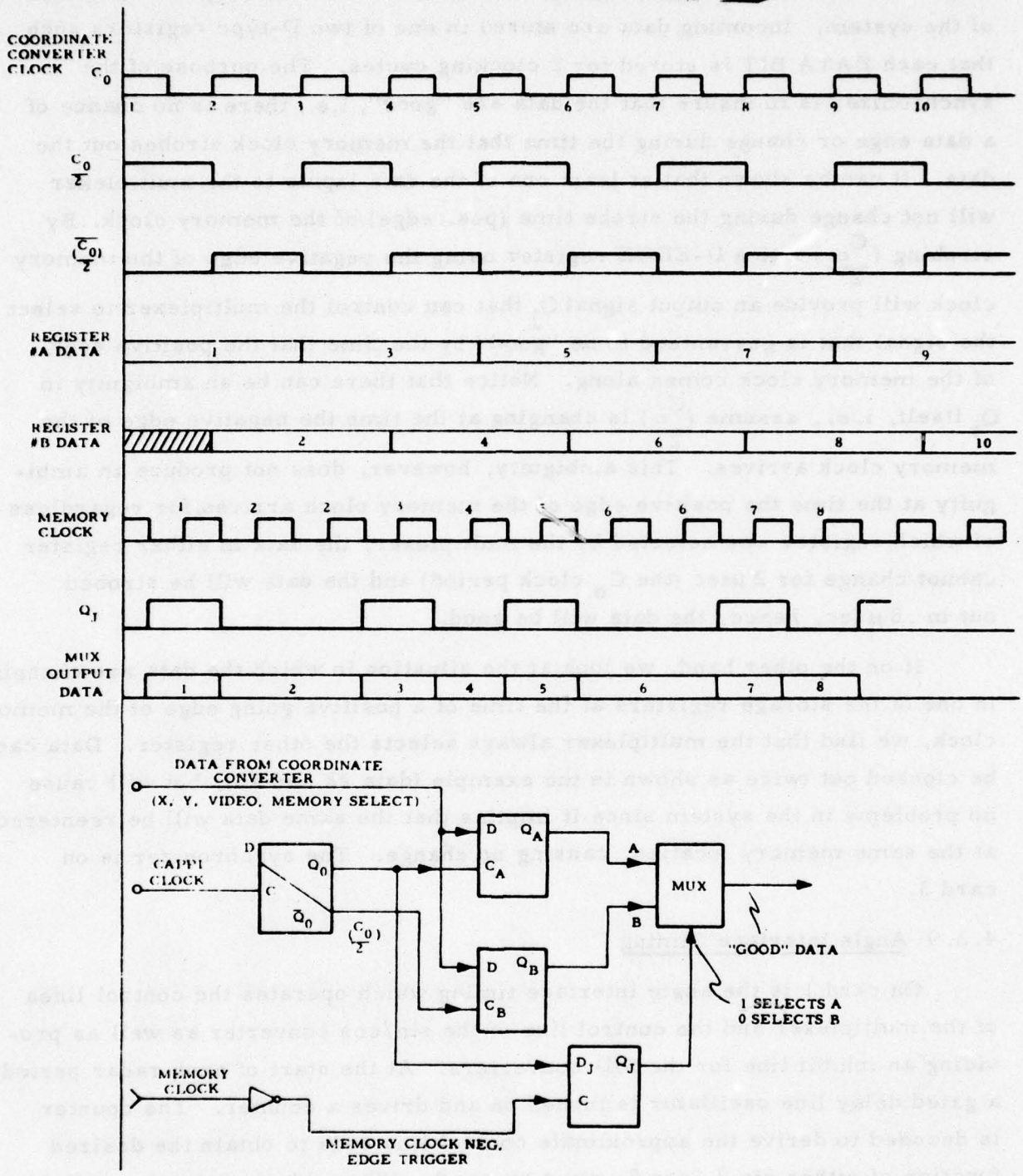


Figure 4-5. Coordinate Converter Memory Buffer Timing Waveforms

diagram of the synchronizer and the timing waveforms showing the operation of the system. Incoming data are stored in one of two D-type registers such that each DATA BIT is stored for 2 clocking cycles. The purpose of the synchronizer is to insure that the data are "good", i.e., there is no chance of a data edge or change during the time that the memory clock strobes out the data. It can be shown that at least one of the data inputs to the multiplexer will not change during the strobe time (pos. edge) of the memory clock. By strobing ($\frac{C_o}{2}$) into a D-EDGE register using the negative edge of the memory clock will provide an output signal Q_j that can control the multiplexer to select the signal that is guaranteed to be "good" by the time that the positive edge of the memory clock comes along. Notice that there can be an ambiguity in Q_j itself, i.e., assume ($\frac{C_o}{2}$) is changing at the time the negative edge of the memory clock arrives. This ambiguity, however, does not produce an ambiguity at the time the positive edge of the memory clock arrives, for regardless of which register was selected by the multiplexer, the data in either register cannot change for 2 μsec (the C_o clock period) and the data will be strobed out in .8 μsec, hence, the data will be good.

If on the other hand, we look at the situation in which the data are changing in one of the storage registers at the time of a positive going edge of the memory clock, we find that the multiplexer always selects the other register. Data can be clocked out twice as shown in the example (data #2 and #6), but will cause no problems in the system since it implies that the same data will be reentered at the same memory location, causing no change. The synchronizer is on card 3.

4.2.9 Angle Interface Timing

On card 1 is the angle interface timing which operates the control lines of the multiplexer and the control line of the sin/cos converter as well as providing an inhibit line for the S/D converters. At the start of each radar period, a gated delay line oscillator is turned on and drives a counter. The counter is decoded to derive the approximate control line code to obtain the desired function of either sin θ, cos θ, sin ϕ or cos ϕ. When this function is available, it is strobed into the appropriate D-register shown in the block diagram.

This is done only once every radar period. The input to the coordinate accumulators are those unit vectors that have been determined on the previous radar period.

4.2.10 Earth Curvature Correction

A correction term is added to the altitude address to correct for earth curvature. This correction term is a positive function that depends on the flat earth range. A ROM is used to obtain the correction factor from the range. A derivation of the correction term is shown in Figure 4-6.

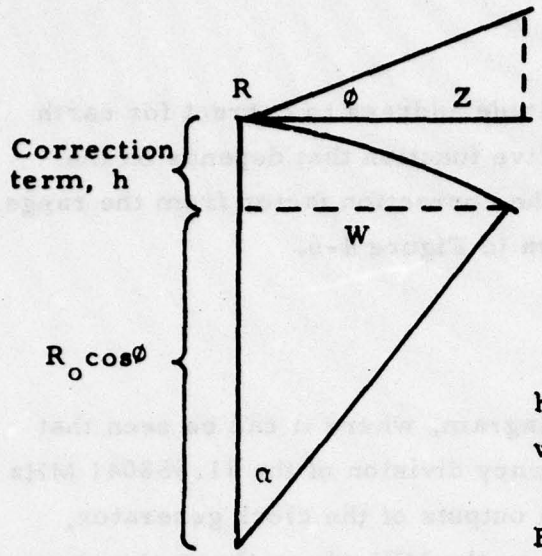
4.3 Display Control Unit

4.3.1 Timing and Control Logic

Figure 4-7 presents the DCU block diagram, where it can be seen that all timing waveforms are obtained by frequency division of the 11.958041 MHz crystal controlled clock. Discussion of the outputs of the clock generator, except for R, is postponed until the section on the MIU where these signals are used.

The square-wave R, with a period of 1.6725 microseconds, is illustrated along the X axis of Figure 4-8, which shows the display format along with waveforms. Along the X-axis, the display is organized into ten-point blocks designated DXBO through DXB31; each period of R corresponds to one block. Since each point requires four-bits for color/intensity coding, 40 bits are needed to specify each block. A memory with 40-bit words has been chosen so that one word in the memory represents each block, 32 words at consecutive addresses describe a line, and 8192 words contain the entire image.

In order to refresh the display, each memory is sequentially read while the CRT beam scans out a raster; this read cycle is always done while R is high, when the memory address multiplexer (see Figure 4-7) routes DXB and DY from the synchronous scan counters to the 13-bit memory address buss which drives all MIU's in parallel. During the remaining half cycle of R, if a store command is received from the SDF, data are written into the memory at an address (IXB, IYB). IYB is simply the input Y address from the SDF, IY, clocked into a register by PSL. In the code conversion ROM, IX is converted into a code consisting of IXB (block select) and XP (point select). As is described in the MIU section, XP determines which one of the ten points within the block is to be changed.



$h = R_o - R_o \cos\alpha = R_o(1 - \cos\alpha)$
where R_o is radius of the earth.

But for small angles,

$$\cos\alpha = 1 - \frac{\alpha^2}{2} \ldots \text{ hence, } h = R_o\left(\frac{\alpha^2}{2}\right)$$

Also for small angles $\alpha \approx \frac{W}{R_o}$

$$h = R_o\left(\frac{W}{R_o}\right)^2 \quad \frac{1}{2} = \frac{W^2}{2R_o}$$

But $W = R\cos\phi$

$$h \approx \frac{(R\cos\phi)^2}{2R_o} = K(R\cos\phi)^2$$

Figure 4-6. Earth Curvature Correction Term

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

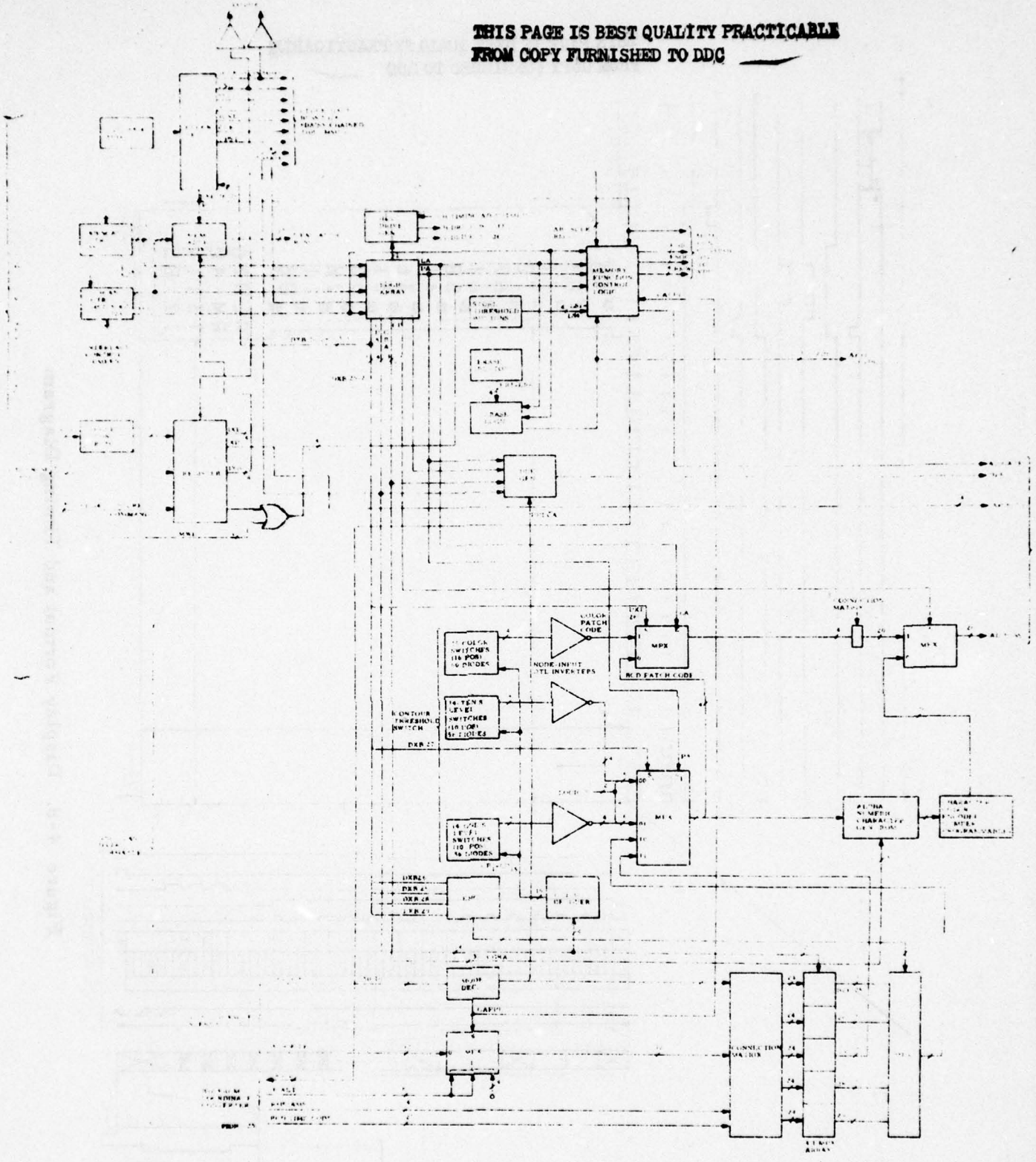


Figure 4-7. DCU Block Diagram

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

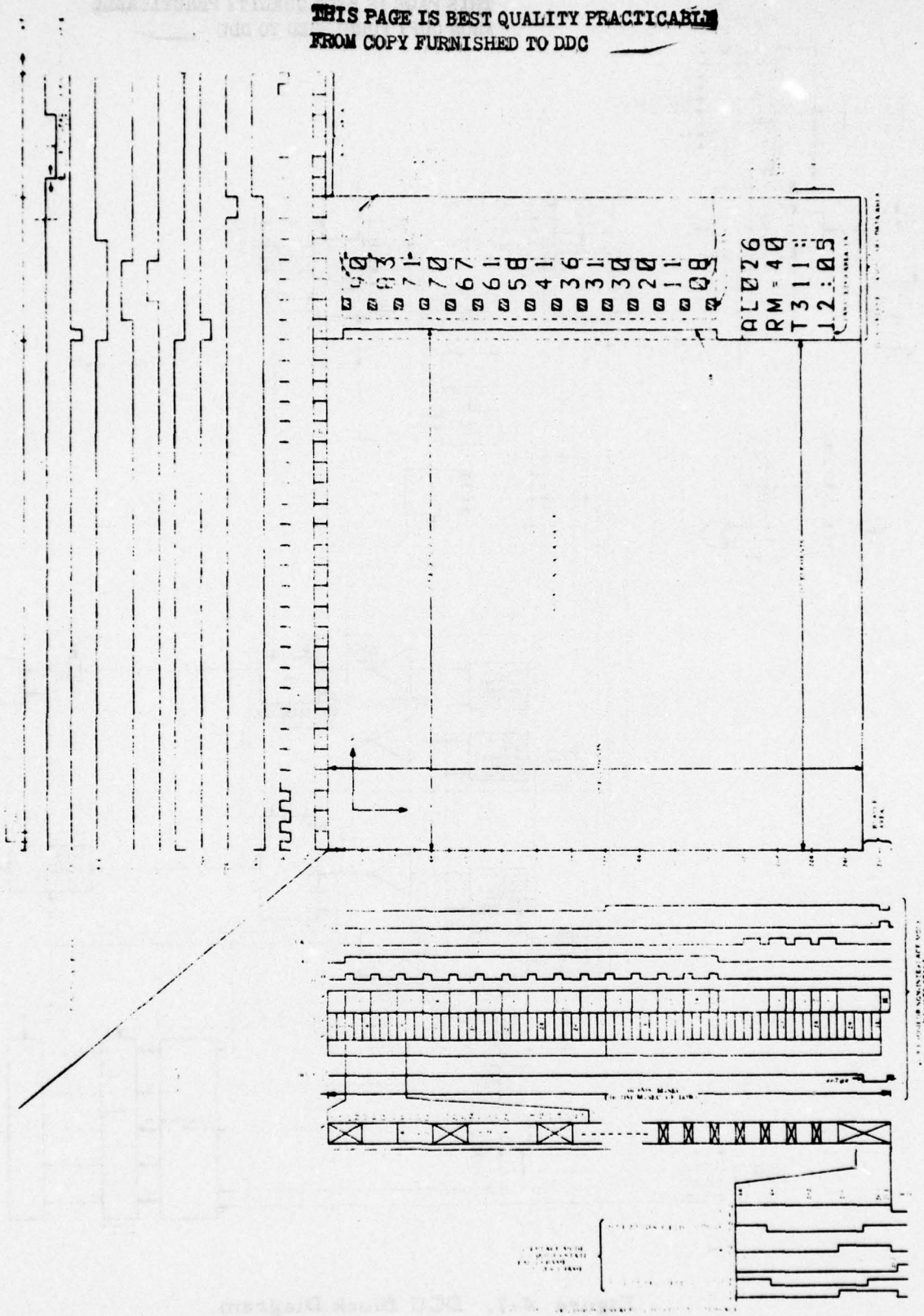


Figure 4-8. Display Format and Timing Diagram

The logic array generates waveforms, shown in Figure 4-8, which are functions of the scan counter outputs, DXB or DY. Waveforms which need to be functions of both DXB and DY are derived from them; for example: PA = PA(X) · PA(Y). The logic array is implemented with two 32 x 8 PROM (Programmable Read Only Memories) and a collection of decoders and gates. A truth table for these PROM, C16 and D20, is tabulated in the appendix, while the addressing and output waveforms are illustrated in Figure 4-8.

Interlaced scanning, possibly useful to fill interline gaps for photographic purposes, can be enabled by removing the jumper-carrier which grounds C27-9. The waveforms which result are shown in Figure 4-8. Timing of the H-drive pulse is adjustable over a range of ± 3 microseconds by means of the potentiometer in F28. This adjustment can be used to center the image in the raster of the display.

The memory function control logic generates SIC, SOC and RMW signals (to be discussed in the MIU section) which initiate various types of cycles in the memory. The AD GATE enables entry of ancillary data (contour thresholds, color patches and parameters) into the MIU. The memory function control logic also contains a four-state counter which advances once per field. The outputs of this counter, AS, select one of the CAPPI ALTITUDES from the front panel switches for entry into the parameter area of the corresponding display.

The erase logic generates properly timed ZID signals which cause all zeroes (black) to be written into the memory, except for the contour threshold area. The decimal point required in the elevation angle is located in point two, whereas all other ancillary data falls into points five through nine; hence, it requires a separate signal developed by the DPE generator.

4.3.2 Ancillary Data Formatter

In order to minimize wiring complexity of the array of contour threshold switches, encoding diodes are mounted on the switches themselves as indicated

in Figure 4-7. One switch at a time is selected by CPI through CPI5 (CPA decoded, see Figure 4-8) as the display raster is scanned. The color switch outputs are applied to the AD BUSS (a 20-bit buss through which ancillary data can enter points five through nine of any block in memory) when the CRT scan is located in the color patch areas. Similarly stored above each number in the legend area is a patch containing a BCD code for that number. The contour generator to be described in the MIU section makes use of these codes which are not visible on the display because a MASK waveform is applied to the MIU. The numbers themselves are generated in a row-select five-by-seven alpha-numeric character generator ROM which outputs five bits in parallel to a character color encoder. This encoder generates a jumper-programmable four-bit code, now set up as green (0111) or black (0000) for each of the five points.

The ancillary data (angle, altitude, marker spacing and time) are entered into the character generator at the proper time by an array of multiplexers. The mode lines, from the front panel mode switch via the angle interface unit, drive a mode decoder which controls the multiplexers and applies the proper alphanumeric identifiers; AZ, EL, AL, M, RM, or T which are hard wired.

Signals appearing on the AD BUSS or on DPE are not displayed directly, even though they are synchronous with the raster scan format. Rather, the data are stored in the memory when appropriate store commands are issued. Only the memory contents themselves are displayed.

4.4 Video Distribution Unit

The VDU card consists simply of an array of line drivers which serves to distribute the eight-bit video signal from the coordinate converter to all of the MIU in parallel. The memory control lines SIC, SOC, RMW, RME, and ZID for each MIU are also routed through the VDU, while the memory clock, $\overline{R}$, passes through on its way to the coordinate converter (see Figure 2-1).

The video inputs for MULTIPLE DATA SOURCE (inputs on J12, J13 and J14) come directly to the VDU where, when MULTIPLE DATA SOURCE has been selected, they are synchronized with the appropriate memory timing signals and coordinate converter generated memory addresses for distribution to the assigned display refresh memory. When MULTIPLE DATA SOURCE has not been selected, the video input on J1 is routed to all display refresh memories.

4.5 Memory Interface Units

The block diagram in Figure 2-1 contains two Memory Interface Units (MIU) which are identical rack-mounted drawers. Address, clock, and gate busses are supplied to the MIU in a daisy-chain configuration where each unit taps off of a twisted-pair cable which is resistively terminated only at the last MIU (No. 2). A block diagram of one MIU is presented in Figure 4-9; the detailed descriptions of various components within it are contained in paragraphs following a discussion of memory cycles.

4.5.1 Memory Cycles

The timing diagram in Figure 4-10 shows all significant waveforms for examples of the four types of memory cycles. Each cycle occupies one-half period of the square wave R (shown in both timing diagrams, Figure 4-8 and 4-10), and is initiated by manual or automatic commands listed in Table 4-1. The state of R determines whether the raster-scan address DXB, DY or the code-converted input address IXB, IYB appears on the memory address buss.

As listed in the table, each of the four types of cycles happens in response to commands when the raster scan address DXB, DY is in certain areas of the display.

Table 4-1. Memory Cycles

	Commands					Type of Memory Cycle When DXB, DY is in each Area of Display (see Fig. 4-8):			
R	Video Store	Legend Store	Erase	Parameter Store	Memory Address Buss	DA	LA	PA	Retrace
1	X	0	X	X	DXB, DY	RR	RR	RR	∅
1	X	1	X	X	"	RR	RW	RR	∅
1	X	X	0	X	"	RR	RR	RR	∅
1	X	X	1	X	"	RW	RR	RW	∅
1	X	X	X	0	"	RR	RR	RR	∅
1	X	X	X	1	"	RR	RR	RW	∅
0	0	X	X	X	IXB, IYB	RR	RR	RR	RR
0	1	X	X	X	IXB, IYB	RMW	RMW	RMW	RMW

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

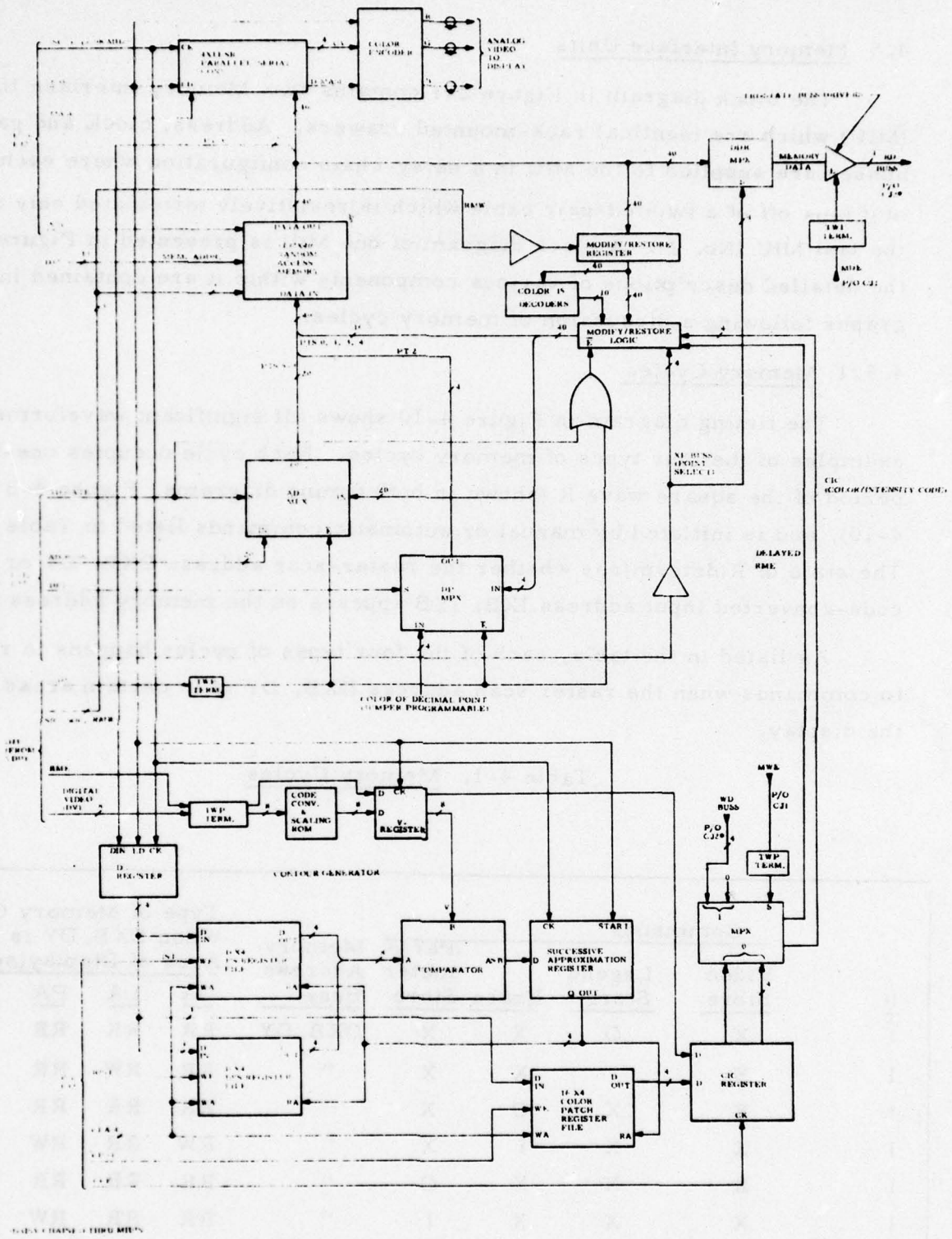


Figure 4-9. Memory Interface Block Diagram

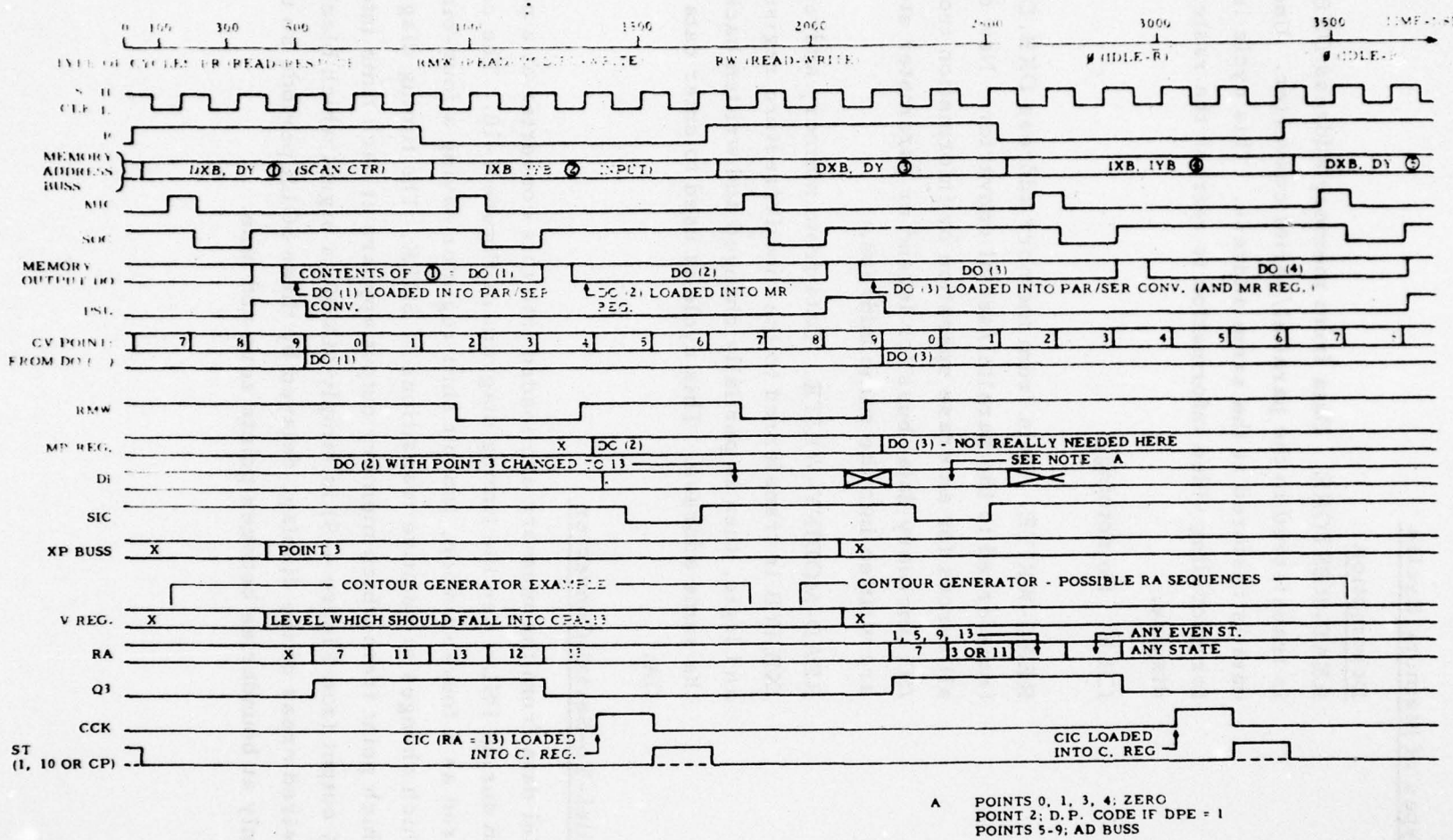


Figure 4-10. Memory Interface Timing Diagram

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

Table 4-1 (Cont)

Listing of Types of Memory Cycles

R	Cycle	Description
1	RR	READ-RESTORE. Data from memory address DXB, DY is transferred to the parallel/serial converter. Unchanged data is restored at the same address. This cycle is used for providing video information to refresh the raster-scan display.
1 or O	Ø	IDLE. Do nothing.
1	RW	READ-WRITE. Data from memory address DXB, DY are transferred to the parallel/serial converter. New data, all zeroes for an erase operation or information from the AD (ancillary data) buss for legend or parameter storage, are written into the same address.
O	RMW	READ-MODIFY-WRITE. Data from memory address IXB, IYB is transferred to the modify/restore register and logic, then is partially changed and written back into the same address. This cycle is used to enter data into DA.

4.5.2 Parallel-To-Serial Converter

Parallel data from the memory are loaded into this converter at a positive edge of SCLK during PSL - see the timing diagram in Figure 4-10. The converter is wired as a four-bit-wide, ten-bit shift register having a four-bit output CV which changes at positive transitions of SCLK. The timing diagram describes which point from which memory output appears at each time interval. The D MASK output (see Figure 4-9) is simply MASK, a signal which blacks out the undesired areas of the display, delayed by three SCLK periods so that it changes only at boundaries between points zero and nine.

4.5.3 Color Encoder

The color encoder (see block diagram in Figure 4-11) accepts the four-bit output of the parallel-to-serial converter, and if DMASK is false, outputs three analog voltages to drive the red, green and blue video inputs on the color monitor. The three identical D/A converters only have three bits each, but nevertheless it is possible to generate 512 different color/intensity outputs. Voltages at each output take on eight different levels ranging from zero (black) to one volt (full intensity); the output loading must be 75 ohms through video coaxial cable.

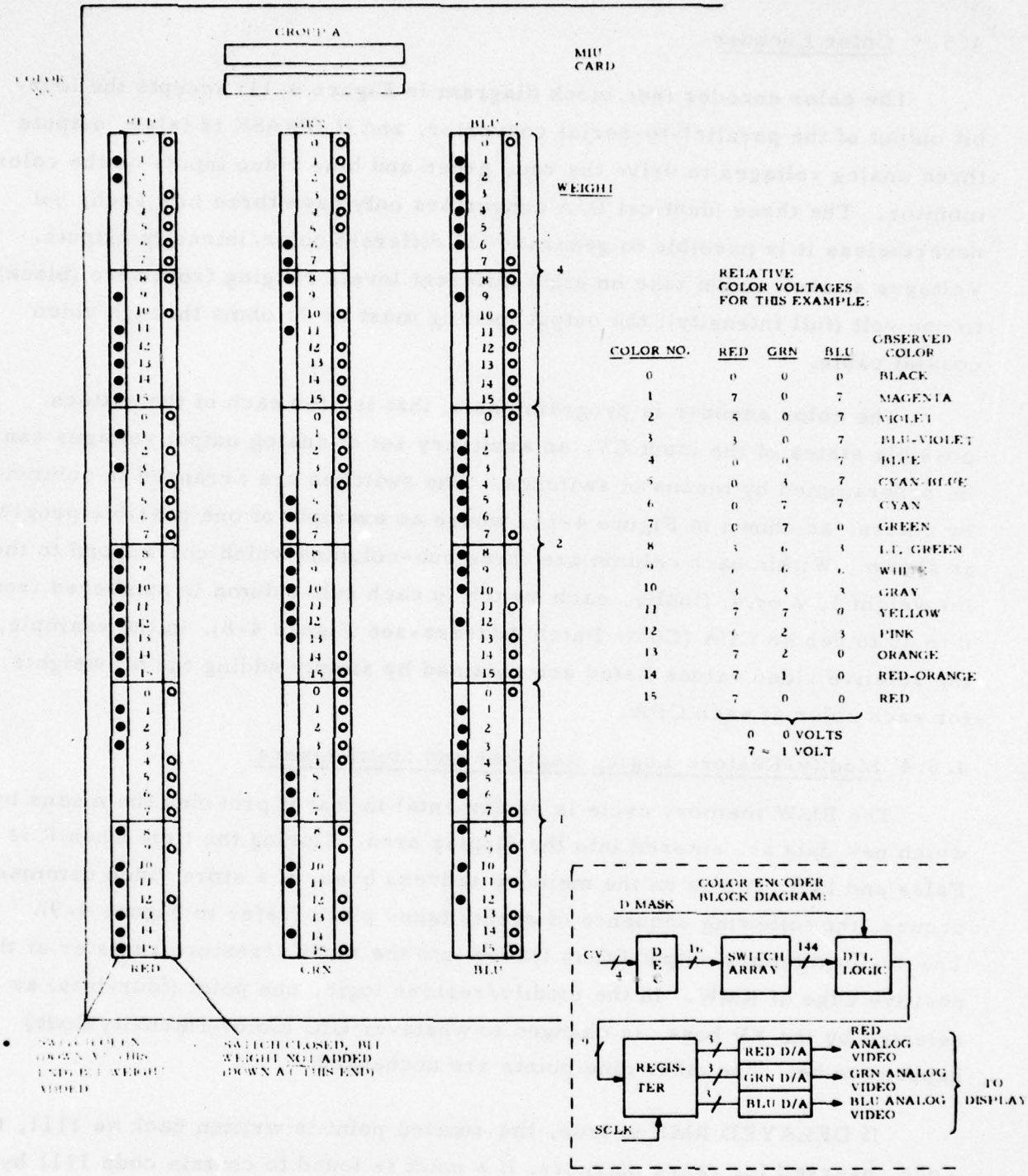
The color encoder is programmable; that is, for each of the sixteen possible states of the input CV, an arbitrary set of analog output voltages can be programmed by means of switches. The switches are arranged in columns by colors, as shown in Figure 4-11, where an example of one possible program is shown. Within each column are three sub-columns which correspond to the bit weight 1, 2 or 4; finally, each switch in each sub-column is numbered from 0 to 15 to denote CPA (Color Patch Address-see Figure 4-8). In the example, the relative video values listed are obtained by simply adding the bit weights for each color at each CPA.

4.5.4 Modify/Restore Logic, Register and Multiplexers

The RMW memory cycle is fundamental in that it provides the means by which new data are entered into the display area. During the time when R is False and IXB, IYB is on the memory address buss, if a store video command occurs, the following sequence of events takes place (refer to Figure 4-9). The 40-bit memory output DO is loaded into the modify/restore register at the positive edge of RMW. In the modify/restore logic, one point (four-bits) as selected by the XP buss, is changed to whatever CIC (Color-Intensity Code) happens to be. The other nine points are unchanged.

If DELAYED RME is true, the selected point is written back as 1111, the code reserved for range markers. If a point is found to contain code 1111 by the COLOR 15 DECODERS, it is written back as 1111. Since these events happen when R is False, the AD and DP multiplexers are switched so that all 40 bits from the modify/restore logic go right back into the memory where they are written, still at the same address, when SIC comes along.

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC



RELATIVE COLOR VOLTAGES FOR THIS EXAMPLE:

COLOR NO.	RED	GRN	BLU	OBSERVED COLOR
0	0	0	0	BLACK
1	7	0	7	MAGENTA
2	5	0	7	VIOLET
3	3	0	7	BLU-VIOLET
4	0	0	7	BLUE
5	0	3	7	CYAN-BLUE
6	0	7	7	CYAN
7	0	7	0	GREEN
8	3	6	3	LT. GREEN
9	6	6	6	WHITE
10	3	3	3	GRAY
11	7	7	0	YELLOW
12	6	2	3	PINK
13	7	2	0	ORANGE
14	7	1	0	RED-ORANGE
15	7	0	0	RED

0 = 0 VOLTS
7 ≈ 1 VOLT

Figure 4-11. Color Encoder Switches and Block Diagram

As is evident from Table 4-1, the intervals when R is False have been reserved for RMW cycles, no matter where the raster scan counters happen to be. Thus, a new input data point can be accepted once every period of R (1.6725 μsec). During the same period, ten adjacent points are output to the color encoder. This ten-to-one difference in data rates results from the memory organization employed and the fact that the input addresses are in random order, while the output addresses are in sequential order.

When ancillary data or zeroes for erase are being written into the memory in RW cycles, points two and five through nine can be changed simultaneously by means of the DP and AD multiplexers. Ancillary data enters through the 20-bit AD multiplexer when AD GATE is true, while DPE causes a 4-bit jumper-programmable code for the color of the decimal point to be applied to point two. ZID zeroes all 40 bits during erase.

4.5.5 Contour Generator

The lower half of Figure 4-9 is the contour generator which accepts one 8-bit video word and RME every period of R and presents a corresponding four-bit CIC (Color/Intensity Code) and delayed RME as its output. Contour thresholds, both colors and levels, are read from the memory when the raster scan is in the appropriate patch (see Figure 4-8) and are stored in register files -- small, fast memories capable of simultaneous reading and writing at different addresses. Data from the register files is used in a successive approximation algorithm to determine which CIC to assign to a given video input.

The incoming digital video is both scaled and converted to BCD in a ROM made up of two 256 x 4 PROM, D9 and D10 for which truth tables are included in the appendix. The ROM output is clocked by PSL into the V register where it remains available to drive the comparator during the remainder of the period of R. The example at the bottom of Figure 4-10 shows a digital video input which has a value such that it should be assigned the color which has been entered into CPA 13. The successive approximation register state RA always begins as seven whereupon the contents of the 1's and 10's register files at read address RA = 7 are compared with V. The decision made in the comparator determines that the next state for RA should be 11 (the other alternative is three), and the process continues to repeat in this manner until four decisions, corresponding to 16 bits, have been made. The final answer of RA = 13 then addresses

the Color Patch Register File which provides a four-bit code to be loaded into the CIC register by CCK. The second contour generator cycle at the lower right of Figure 4-10 shows all possible states of RA for each step.

The time interval after CCK is reserved for writing data into the three register files, as commanded by the three write strobe signals 1 ST, 10 ST and CPST. The write address applied to the register files is CPA, and the appropriate write strobe signal is gated-on when the raster scan is in the proper patch. Although each patch contains a five-by-four array of identically coded points, only one is needed to be written into the register files. Point eight has been arbitrarily chosen and is thus loaded into the D register (Figure 4-9) at PSL so that it can be entered into the proper register file when the corresponding write strobe signal occurs. Four write strobes appear during each field for every write address of the register files.

4.5.6 Write Data and Read Data Busses

The WD and RD four-bit busses, daisy-chained through the MIU as are the other busses (see Figure 2-1), permit direct access to any image point in the memory.

When the MWE control line is active, the multiplexer at the bottom of Figure 4-9 connects the WD buss directly to the CIC inputs of the Modify/Restore Logic. The Range Marker Enable signal is simultaneously rendered inoperative.

When the MDE control line is active, the tri-state driver at the top of Figure 4-9 drives the RD buss with a four-bit code corresponding to one of the ten points currently available at the memory output. The DDR multiplexer selects this point as a function of the state of the XP Buss. The RD buss differs from all others in that signals flow away from the MIU; more than one MDE control line cannot be active simultaneously lest the buss drivers perish.

4.6 Serial Data Formatter

A multiplexer, illustrated in the upper left corner of Figure 4-12, selects the X and Y scan converter outputs for application to the DCU address inputs IX, IY when either or both store commands are active (MBA = LOGIC ZERO). In this case the ninth (most significant) X bit is forced to zero and store commands are disabled for X = 255 since radar data must not appear in the ancillary data area which begins at X = 255 (see Figure 4-8). When all store commands are inactive, MBA is true and the DCU address inputs are driven by the transmit address counters TX and TY.

The serial data format appears in Figure 4-13 along with certain SDF waveforms included to show the operation of the counters in Figure 4-12. The counters are synchronous with the modem clock MCK. Interface with the memory, having faster clocks SCLK and PSL, is affected by separate read and write synchronizers.

The bit counter operates differently between the transmit and test modes, but its least significant two bits TD always define the bit number (0-3) of the point specified by the transmit point and line counters TX, TY.

In the transmit mode--see Figure 4-14--the counter has modulo four and the write synchronizer is disabled. Consider the time when TX has just changed from X_1-1 to X_1 in Figure 4-14. The expanded-time-scale waveforms show how the read synchronizer subsequently generates an MDG pulse at the earliest possible time consistent with the memory timing. Recall that MDE is the control line which activates a tri-state RD-buss driver in an MIU. MDG is simply applied to the MDE line for whichever MIU has been selected as the source by the source switch which drives the Test/Select logic. (see Figure 4-12). While MDG is active, the four-bit color/intensity code obtained from the memory address defined by X_1, Y (the present states of counters TX, TY) is on the RD buss. At the trailing edge of MDG, this word is clocked into a register and becomes SRD, the read synchronizer data output.

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

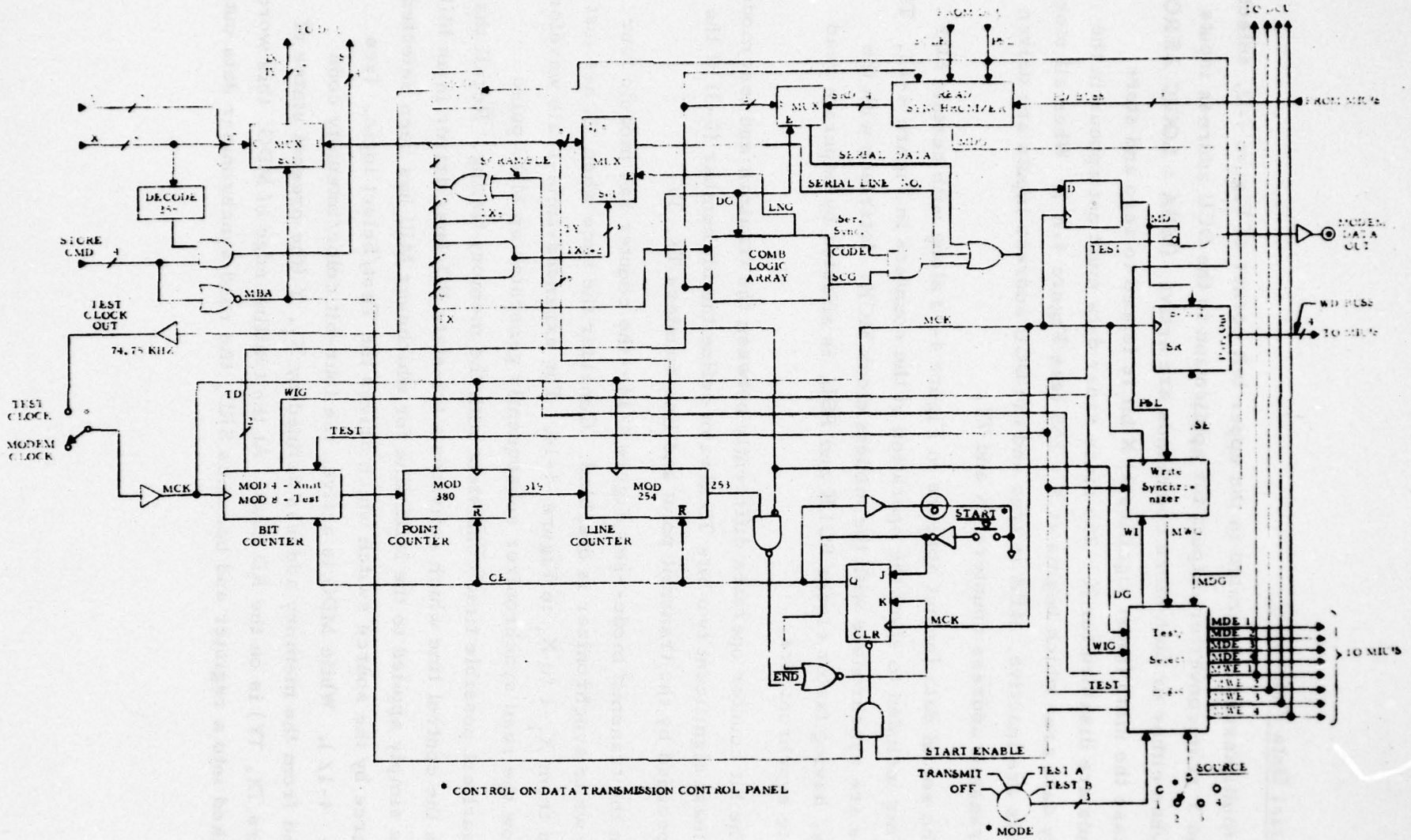


Figure 4-12. SDF (Serial Data Formatter) Block Diagram

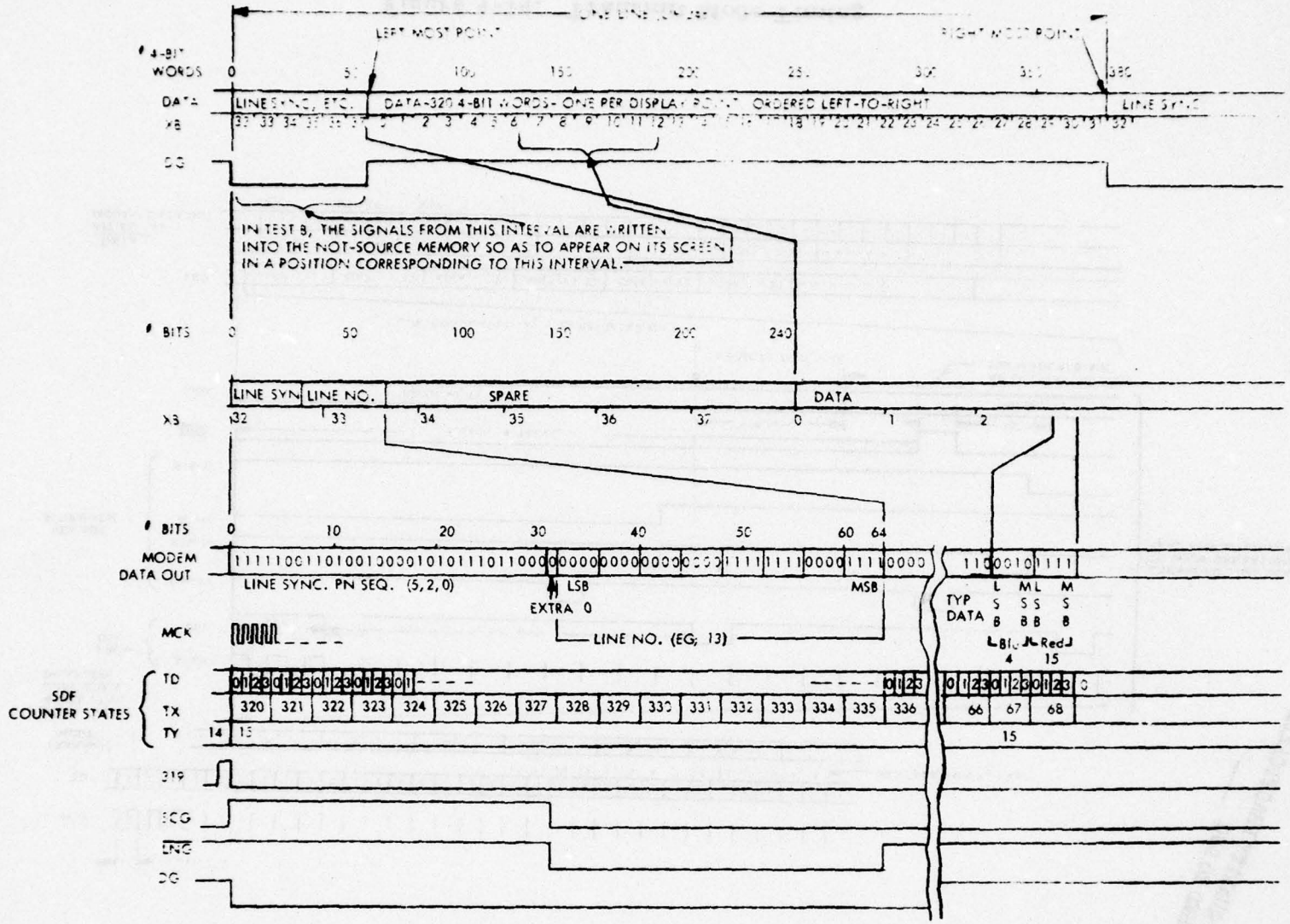


Figure 4-13. Serial Data Format

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

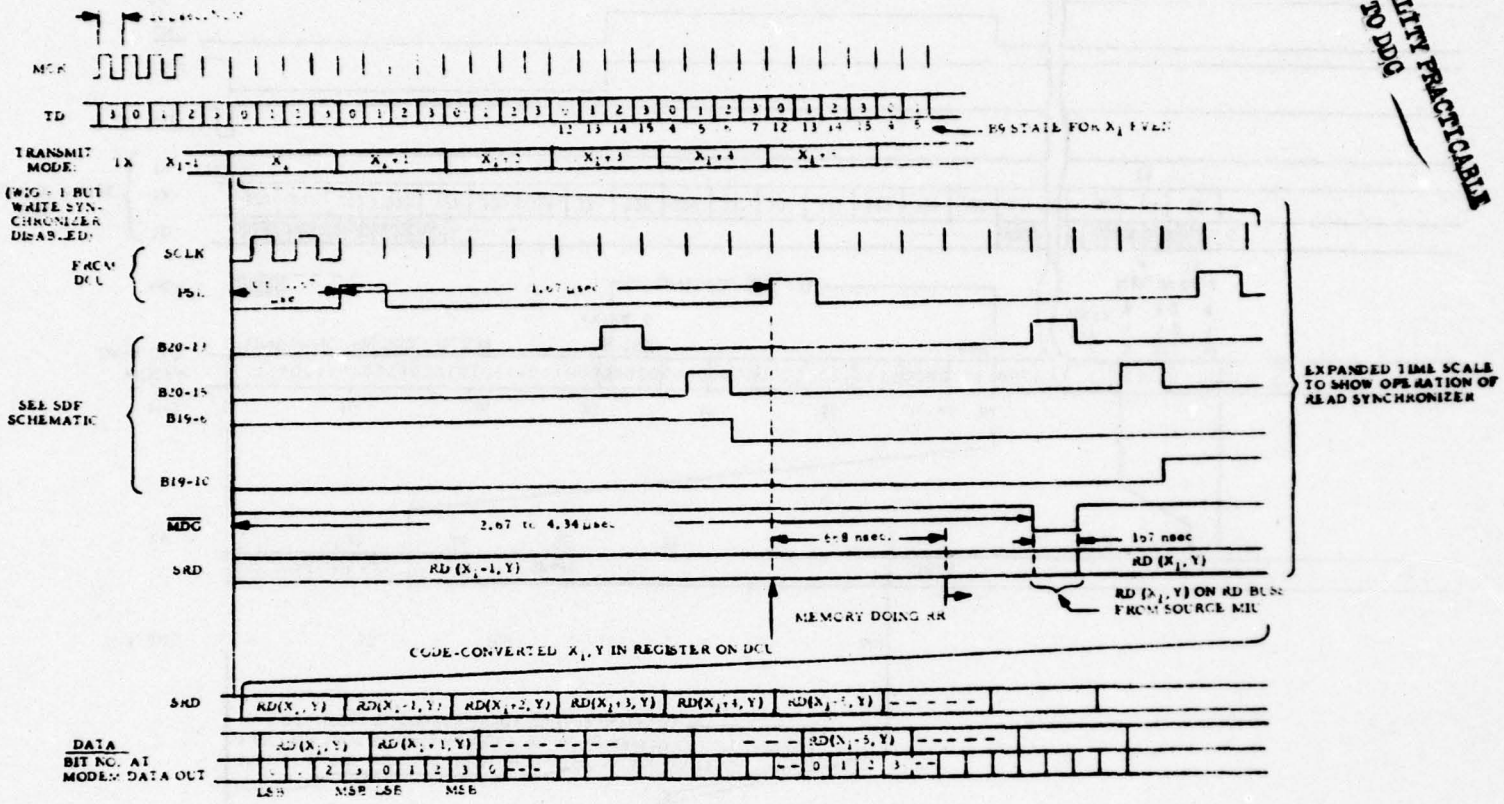


Figure 4-14. Transmit Mode Timing

SRD is serialized by a multiplexer, enabled only during the data gate DG (Figure 4-13), with its select inputs driven by TD. The resulting serial data is or'd with serial sync. code and line number signals, each gated on during its appropriate time, and the entire serial data stream is re-clocked by MCK to become MD which drives the Modem through a line driver which level-converts to the Standard RS 232 interface signal level.

The preceding paragraph also applies when either test mode is selected, except that the Modem Data Output is disabled and the bit counter has modulo eight. The WIG signal shown in Figure 4-15 initiates a write operation in which a four-bit word, having been obtained from the source memory and serialized as described above, is shifted into a parallel output register which drives the WD buss. This four-bit word is subsequently written into a not-source memory at the same address, since TX and TY haven't changed yet. The expanded-time-scale waveforms of Figure 4-15 show how MWG is developed from the WI pulse by the write synchronizer. The test/select logic (Figure 4-12) directs MWG to the MWE inputs of a not-source MIU and of the DCU; the normal store command inputs of the DCU are not used in this mode.

Test Mode A causes the source memory to be copied into a not-source memory, while test mode B results in waveforms from the time when DG is False (Figure 4-13) being written into the not-source memory. Test Mode B thus requires that the WI pulse be active only when DG is false and that the X address be scrambled (TX8 complemented) when WIG is true.

The SDF counters operate only while CE is true, in which case the blue indicator of the START switch on the Data Transmission Control Panel is illuminated. When this momentary-contact switch is closed, CE is set to its true state, provided MCK exists. When TY has reached 253 and that line is complete, CE is reset, the counters are re-initialized, and the SDF is ready for another transmission cycle. If switch four of B30 on the SDF card itself is closed, the SDF counters run continuously. The counters are unconditionally held initialized whenever any STORE VIDEO switch is on (MBA = False) or the MODE switch is in its OFF position.

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

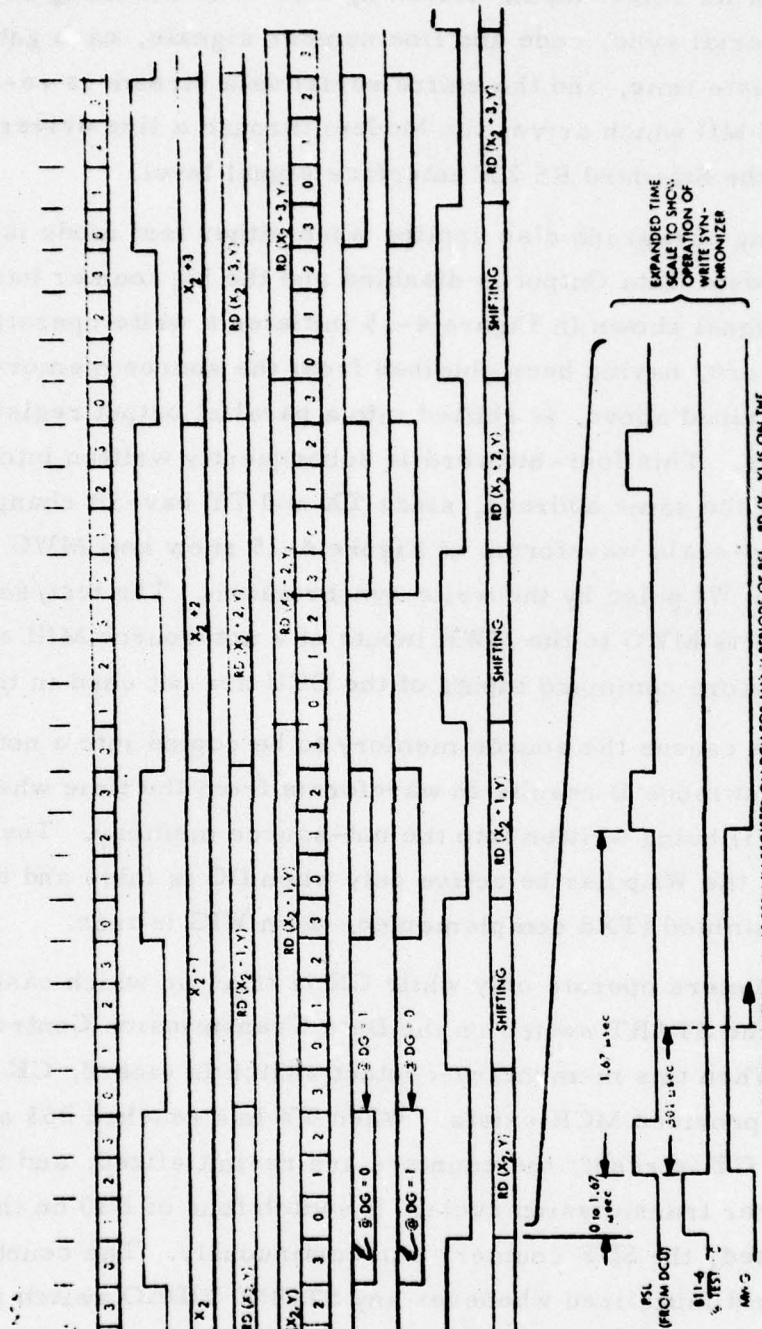


Figure 4-15. Test Mode Timing

The combinatorial logic array near the center of Figure 4-12, driven by TD and TX, generates the serial sync. code prefix and sync. code, line number, and data gates. This array includes a programmable 32 x 8 ROM having the data pattern included in the Appendix; the same ROM is also used in the Remote Refresh Memory. Switches 1, 2 and 3 of B30 on the SDF card formation as to the effect of these switches can be found on the SDF schematic.

The serial line number code is obtained by scanning the equivalent eight-bit parallel code, TY, with a one-of-eight multiplexer having select lines connected to the three least significant bits of TX. This multiplexer is enabled only during the Line Number Gate LNG.

4.7 Display Receiver Unit

4.7.1 Timing and Control Logic

Figure 4-16 presents the DRU block diagram, where it can be seen that all timing waveforms are obtained by frequency division of the 11.958041 MHz crystal-controlled clock in the timing and control circuitry below the dashed line. Discussion of the outputs of the clock generator, except for R, is postponed until the section on the MIU where these signals are used.

The square-wave R, with a period of 1.6725 microseconds, is illustrated along the X-axis of Figure 4-2, which shows the display format along with waveforms. Along the X-axis, the display is organized into ten-point blocks designated DXBO through DXB31; each period of R corresponds to one block. Since each point requires four-bits for color/intensity coding, 40 bits are needed to specify each block. A memory with 40-bit words at consecutive addresses describe a line, and 8192 words contain the entire image.

In order to refresh the display, the memory is sequentially read while the CRT beam scans out a raster; this read cycle is always done while R is high, when the memory address multiplexer (see Figure 4-16) routes DXB and DY from the synchronous scan counters to the 13-bit memory address buss. During the remaining half cycle of R, if a store command is received, data are written into the memory at an address (RXB, RYB), where RXB is a 5-bit block select code developed directly in a counter, thereby eliminating the code conversion ROM needed in the DCU of the Master SCRM. As is described in the MIU section, RXP determines which one of the ten points within the block is to be changed.

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

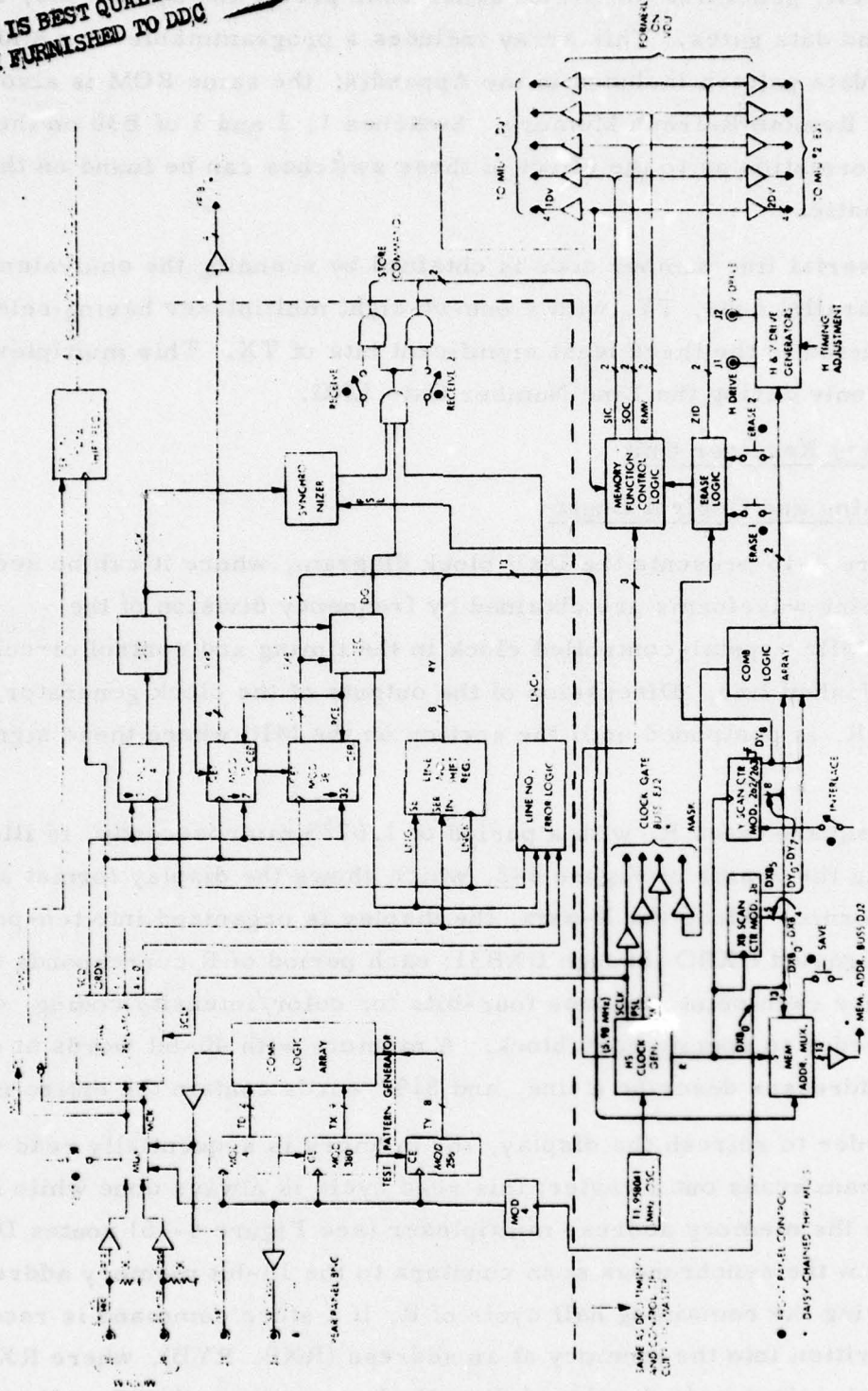


Figure 4-16. DRU (Display Receiver Unit) Block Diagram

4.7.2 Test Pattern Generator

The test pattern generator obtains its 74.75 kHz clock by dividing DXB_0 of the XB scan counter by four. The TD, TX and TY counters simulate the corresponding counters in the Master SCRM. They drive a combinatorial logic array which develops the test pattern, including sync. code and line number. This logic array uses a 32 x 8 PROM having the same pattern (see Appendix) as that used in the Master SCRM and in the serial correlator (to be described) of the DRU.

4.7.3 Receiver Counters and Registers

The serial correlator will be described in another section. But for the purposes of this section, its outputs are diagrammed in Figure 4-17 which will help to explain operation of the remaining portions of Figure 4-16. It might also be helpful to refer to Figure 4-13 of the Master SCRM final report, which describes the serial data format. The ORDY output of the correlator goes high when its other outputs are valid; it is used as a bit clock in the DRU. The serial input data delayed one clock period, DMDTA, is shifted into a 4-bit serial/parallel converter, the output of which is the color-intensity code to be stored in the memory. The RXP and RXB counters, properly initialized by SCD when the correlator finds a sync. code, develop X-addresses at which to store the color/intensity code. The command to store is issued at the proper time as determined by the synchronizer (see bottom of Figure 4-17) but only during the data gate DG. After detection of the sync. code, the line number gate LNG goes high and the line number code is shifted into its register to serve as the Y-address RY. Should there be an error in any bit of the line no. code, LNOK goes low and no store commands are issued until the next successful line.

4.7.4 Serial Correlator

A block diagram of the serial correlator appears in Figure 4-18, along with timing diagrams having two different time scales. At the negative transition of the modem clock, the correlator cycle begins with zeroing of the AB, sync. code, and line no. code counters, but not the AA counter. Concurrently, the data present at the input at this time, MDTA, is written into the RAM at an address defined by the state, say k, of counter AA. Since

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

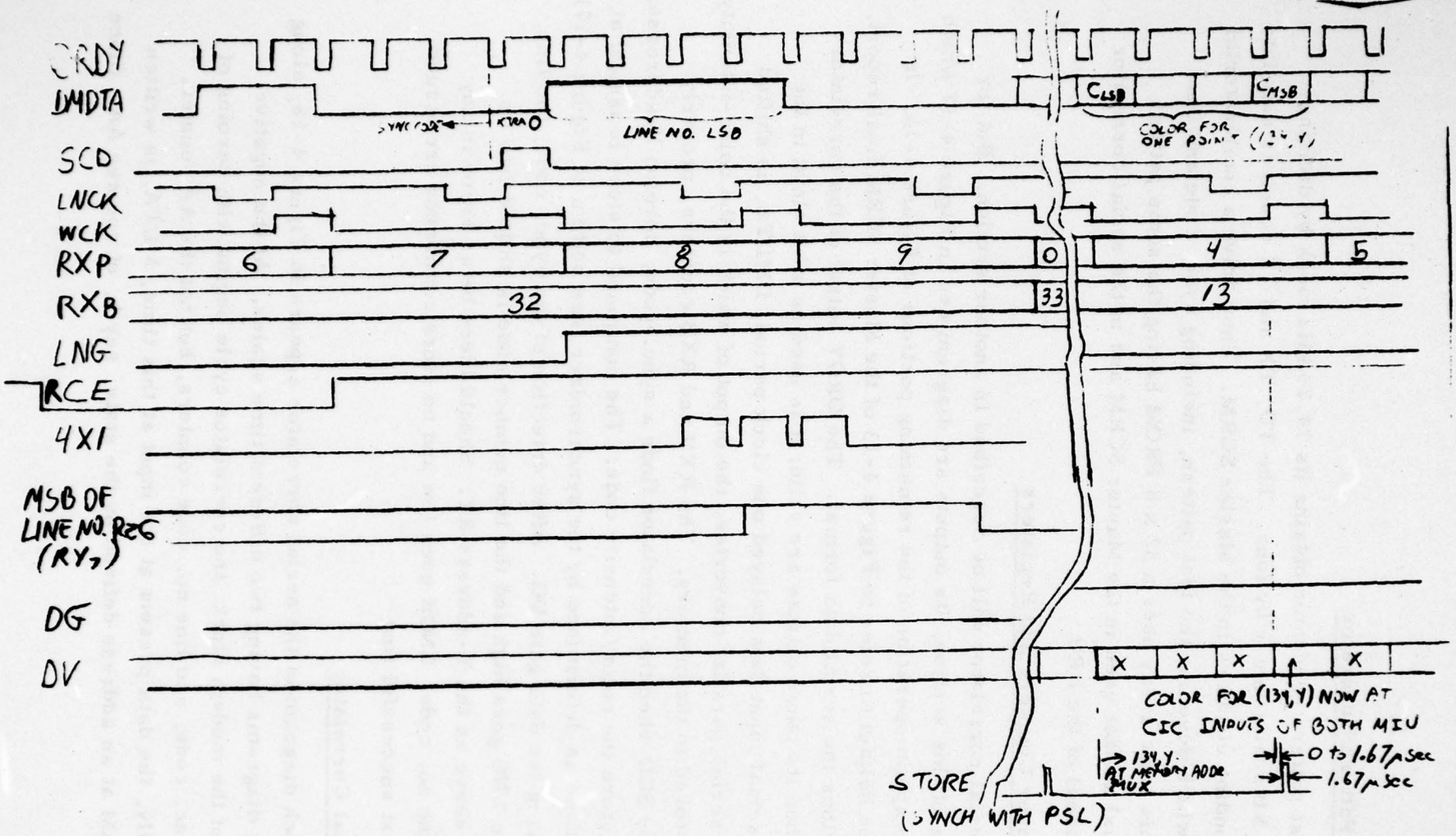


Figure 4-17. DRU Timing Diagram

this process had been going on for many previous cycles, the other RAM addresses contain bits from the earlier cycles. The correlator works by rapidly (one bit per 167.25 nsec) sequencing through these earlier data samples and comparing them with a replica (from the ROM--see Appendix) of the sequence which is being sought. Two sequences are looked for simultaneously here: the 31-bit sync. code and the four bits which make up one digit of the line number code. Because these sequences are both shorter than the 32-bit capacity of the correlator, 31-bit and 4-bit gates are needed.

The sync. code and line number code counters count the number of bits which match between the RAM output and the ROM output. The comparator logic decides whether or not to accept the code being sought. For the sync. code case, if there is one error the code is still accepted and SCD goes high. But if there are two or more errors, it is rejected. The other comparator outputs, 4 x 1 and 4 x 0, end up high if the last four bits contained 3 or 4 ones or 3 or 4 zeroes, respectively. The example at the bottom of Figure 4-18 shows operation for a case where the sync. code is not found but the last 4 bits contained 3 ones.

4.8 Remote Memory Interface Units

Another major element of the remote block diagram is the MIU which is unmodified except for deletions of certain plug-in IC's and addition of jumpers as described in drawing 911049, the RRM interconnect diagram. The ten single-wire jumpers replace gates so that these MIU's do not have the color 15 non-overwrite property of the Master SCRM MIU. The small jumper cable, described in drawing 911155, is used to bypass the contouring circuitry which is not used in the RRM MIU's. The 4-bit color/intensity code thus goes directly to the modify/restore logic (see Figure 4-19) but gets from the DRU to the MIU via four of the eight twisted pairs formerly used for digital video DV.

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

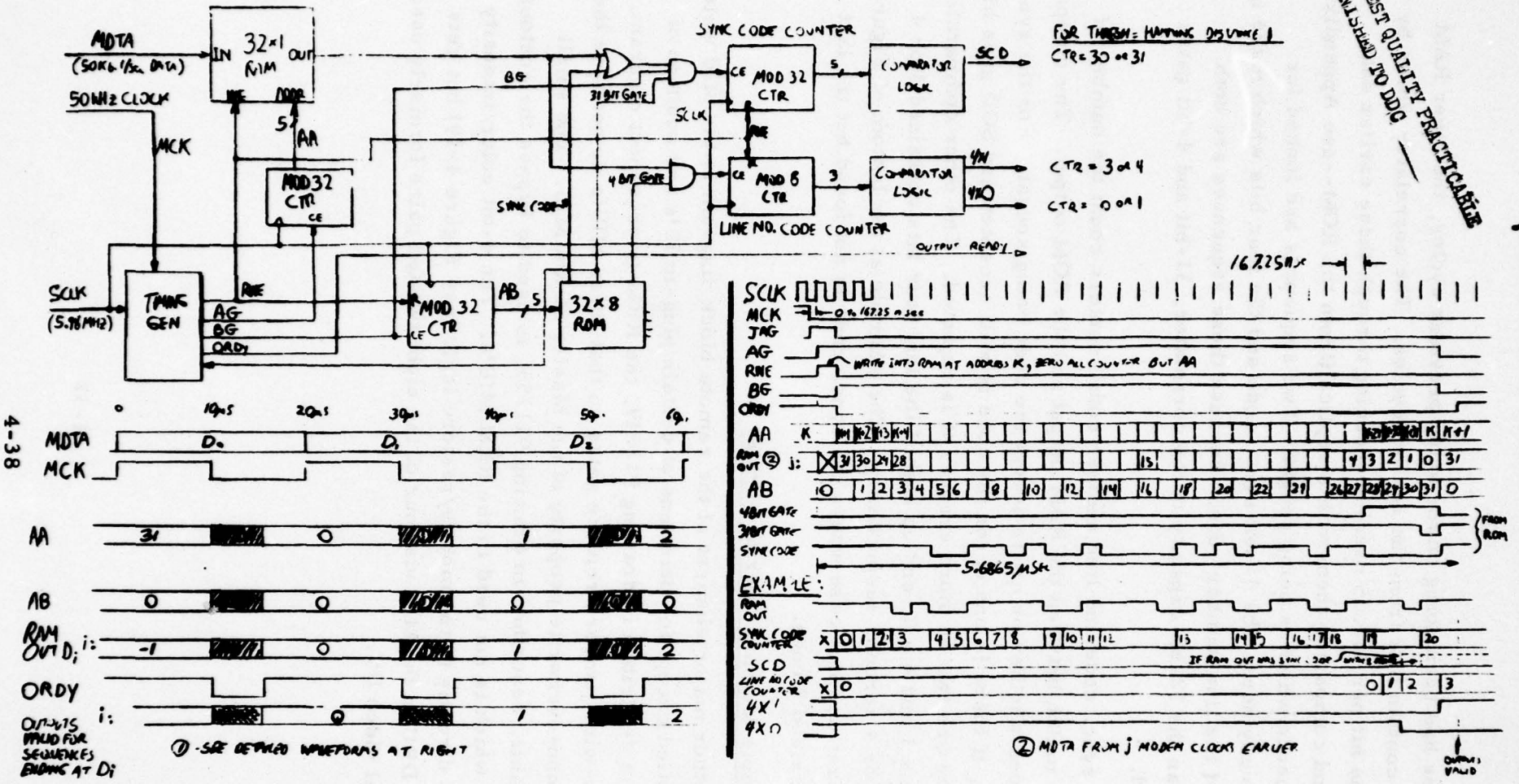


Figure 4-18. Serial Correlator and Waveforms

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

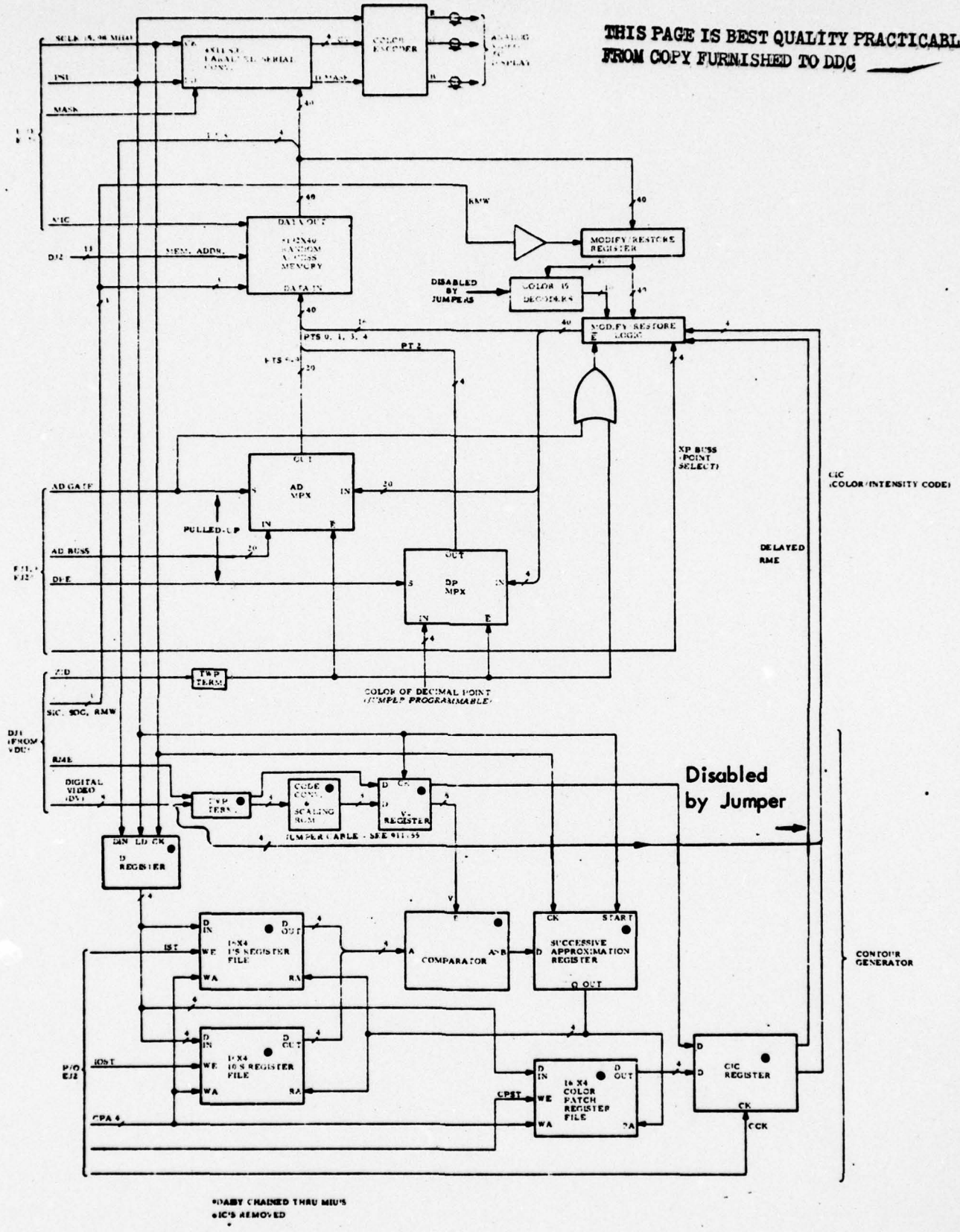


Figure 4-19. Memory Interface Block Diagram (Remote)

Preceding Page BLANK - NOT FILMED

APPENDIX A

Product Information on Sub-System Modules

INTERFACE ENGINEERING

INCORPORATED

STOUGHTON, MASSACHUSETTS



DIGITAL TRANSLATOR

BINARY ANGLE TO SCALED BCD

MODEL DD107

DESCRIPTION

The DD107 Digital Translators accept the binary digital representation of angle (MSB = 180°) and develop the angle scaled BCD equivalent. The translation is performed by normalizing the input data with a scale factor and then converting the result into BCD.

The DD107-5 is a fast, high resolution, ripple-thru translator which accepts up to 15 bits of binary angle data and provides an 18 line BCD output with a resolution of .01°.

The DD107-4 accepts a 12 bit binary input and delivers a 14 line 4 digit BCD output. This model contains an input storage register and can be operated in either continuous, data freeze, or sampling modes of operation.

Input and output logic levels are DTL/TTL compatible. Accessory 4 and 5 decimal digit panel displays with decoder-drivers are available as optional accessories.

The translators are fully encapsulated in low profile cubes. Pins are arranged in groups of 7 on .100 centers permitting direct plug-in to wirewrap planes or PC boards.

FEATURES

- ☐ FAST – 500 Nanoseconds
- ☐ PRECISE – 0.01° Resolution
- ☐ CONVENIENT – Compact and logic compatible.

APPLICATIONS

- ● INTERCOMPUTER CODE CONVERSION
- ● NUMERICAL ANGLE DISPLAYS
- ● BINARY CONTROL OF BCD SHAFT POSITIONERS

SPECIFICATIONS

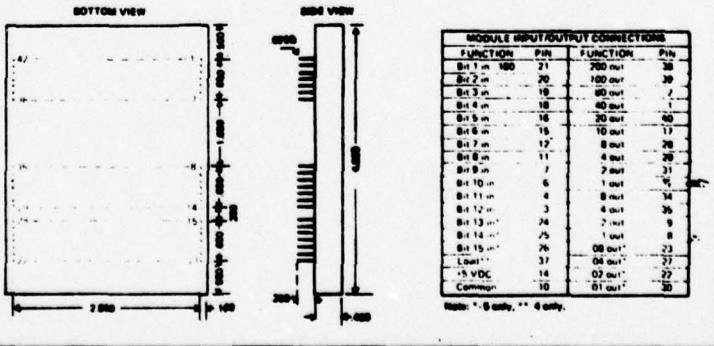
ELECTRICAL

	RESOLUTION				
MODEL	*IN*	*OUT*	*FULL SCALE*	*ACCURACY*	*STORAGE*
DD107-5	15 Bits	0.01°	359.99°	±.015°	External
DD107-4	12 Bits	0.1°	359.9°	±.055°	Internal

LOAD COMMAND (DD107-4)..... Positive True, 100 nanosec. min.
LOGIC LEVELS ..... Positive True DTL/TTL compatible
True = +2.0V to +5.5V
False = 0V to +0.8V
LOADING – Input ..... 4 Standard TTL loads max.
Output ..... 4 Standard TTL loads max.
POWER REQUIREMENTS ..... +5VDC±5% @ 750 MA

PHYSICAL

OPERATING TEMP. RANGE ..... 0° to +70°C
STORAGE TEMP RANGE ..... -54°C to +85°C
RELATIVE HUMIDITY..... 100% non-condensing
SIZE..... 3"W x 4"L x 0.4"H
PINS..... .020" round, gold plated, 0.250" long min.
WEIGHT ..... 5 ounces



MODULE INPUT/OUTPUT CONNECTIONS

FUNCTION	PIN	FUNCTION	Pin
Bit 1 in 180	21	200 out	38
Bit 2 in	20	100 out	39
Bit 3 in	19	80 out	2
Bit 4 in	18	40 out	1
Bit 5 in	16	20 out	40
Bit 6 in	15	10 out	17
Bit 7 in	12	8 out	28
Bit 8 in	11	4 out	29
Bit 9 in	7	2 out	31
Bit 10 in	6	1 out	5
Bit 11 in	4	8 out	14
Bit 12 in	3	4 out	35
Bit 13 in*	24	2 out	9
Bit 14 in*	25	1 out	8
Bit 15 in*	26	08 out*	23
Load**	37	04 out*	22
+5 VDC	14	02 out*	22
Common	10	01 out*	30

Note: * - 5 only, ** - 4 only.

INTERFACE ENGINEERING INC
396 LINDELOF AVENUE BOX 360
STOUGHTON, MASSACHUSETTS
Call (617) 344-7383

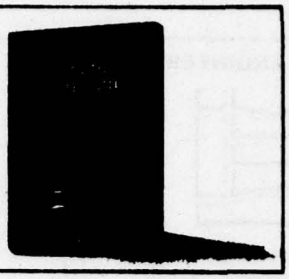
2708.'8

PRINTED IN U.S.A.

INTERFACE ENGINEERING

INCORPORATED

STOUGHTON, MASSACHUSETTS



DIGITAL TRANSLATOR

BINARY ANGLE TO BINARY SINE

MODEL DD108

DESCRIPTION

The DD108 angle translators are purely digital devices which convert a binary input angle to the corresponding sine of the angle over an input angular range of 90° or, when operated with external quadrant and complementing logic, provide 4 quadrant operation with both sine and cosine digital outputs. (Refer to Bulletin 271007).

The translators employ parallel ripple-thru memories and interpolation logic providing a translation speed limited only by propagation delays. The translation speed, faster than equivalent computer operations, permits the translator to be time shared between using hardware providing the inherent precision of digital processing without tying up a general purpose computer on costly repetitive angle translation routines. Alternatively, the translators avoid the costs and accuracy degradation inherent in analog trig function generators. Both models provide a translation precision of 16 bits. The input resolution of the DD108-A is .088° and the input resolution of the DD108-B is .011'.

Input and output logic levels are DTL/TTL compatible. The translators are packaged in compact fully encapsulated low profile cubes. Pins are arranged as in-line groups of 7 on .100 centers permitting direct plug-in to wire wrap planes or PC boards.

FEATURES

- ☐ FAST 0.75 and 1.2 μsec.
- ☐ FINE .088° and .011' steps
- ☐ PRECISE 16 bit output
- ☐ ACCURATE .005° arctan

APPLICATIONS

- SYNCHRO CONVERSION
- COORDINATE TRANSLATION
- SIGNAL PROCESSING
- RESOLVER COMPUTATION
- PATTERN GENERATORS

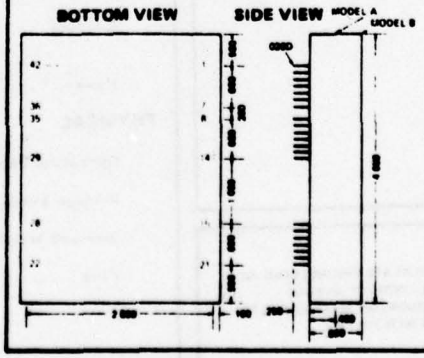
SPECIFICATIONS

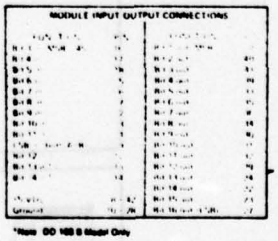
ELECTRICAL

DD 108-A INPUT		10 bit binary angle, MSB 45° LSB 088'
DD 108-B INPUT		13 bit binary angle, MSB 45° LSB 011'
DIGITAL OUTPUT		16 bit binary magnitude Sine or Cosine
ANGULAR RANGE		90° (Refer to bulletin 271007 for Sine and Cosine operation over 360° range)
TRANSLATION ACCURACY		± .015% of full scale ± .005° arc (Sin/Cos)
PROPAGATION DELAY		0.75 microseconds ..... DD 108-A 1.20 microseconds ..... DD 108-B
LOGIC		Positive true, DTL/TTL compatible True = + 2.0V to + 5.5V False = 0V to 0.8V
LOADING	Input	8 TTL loads max
	Output	2 TTL loads max
POWER	DD 108-A	+ 5 VDC ± 5% @ 600 ma
	DD 108-B	+ 5 VDC ± 5% @ 800 ma

PHYSICAL

OPERATING TEMP. RANGE	0 to 70° C
STORAGE TEMP. RANGE	- 54 to + 125° C
SIZE AND WEIGHT – DD 108-A	.3"W x 4"L x 0.4"H, 5 ounces
DD 108-B	.3"W x 4"L x 0.8"H, 10 ounces
PINS	.020" round, gold plated, .250" L min.





INTERFACE ENGINEERING INC.
386 LINDELOF AVENUE BOX 360
STOUGHTON, MASSACHUSETTS
Call (617) 344-7383

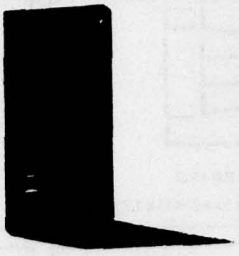
270928

PRINTED IN USA

INTERFACE ENGINEERING

INCORPORATED

STOUGHTON, MASSACHUSETTS



DIGITAL TRANSLATOR

BINARY ANGLE TO SIN/COS CONTROLLER

MODEL DD 109

DESCRIPTION

The DD109 Binary Angle to Sine and Cosine Controllers adapt the Model DD108 Binary Angle to Binary Sine translators to full four quadrant sine and cosine operation.

The controllers are purely digital devices which determine the quadrant in which the angle lies, determine the polarity of the sine and cosine outputs from the DD108, and route either the input angle or it's two's complement to the input of the DD108. Inhibit logic is provided for forbidden two's complement codes.

A single control line selects the sine or cosine output function. When the line is Low the combined output 17 bit code represents the sign and magnitude of the Sine of the input angle. When the line is High the output 17 bits represent sign and magnitude of the Cosine of the input angle.

The DD109 will accept up to 15 bits of binary angle and can be used with either the DD108A (.088° LSB) or DD108B (.011° LSB).

INTERFACE ENGINEERING INC
396 LINDELOF AVENUE
STOUGHTON, MASSACHUSETTS
Call (617) 344-7393

FEATURES

(With DD108 Angle to Sine Translator)

- ☐ FOUR QUADRANT OPERATION
- ☐ BOTH SINE AND COSINE OUTPUTS
- ☐ 12 OR 15 BIT ANGLE IN
- ☐ 17 BIT SIGN AND MAGNITUDE OUT
- ☐ ACCURACY ±0.005° ARCTAN

APPLICATIONS

- SYNCHRO CONVERSION
- SIGNAL PROCESSING
- COORDINATE TRANSLATION
- COORDINATE TRANSLATION
- PATTERN GENERATORS

SPECIFICATIONS

ELECTRICAL

Digital Input ..... 15 bit angle (MSB = 180°)

Function Select
- Sine ..... select line low (0)
- Cosine ..... select line high (1)

Digital Outputs

	Quadrant I	II	III	IV
Polarity (Direct Output)	0	1	1	0
Sine Polarity	0	0	1	1
Cosine Polarity	0	1	1	0

Angle to DD108 (MSB = 45°)

Sine Select	⊖	90°-⊖	⊖	90°-⊖
Cosine Select	90°-⊖	⊖	90°-⊖	⊖

Translation Accuracy (With DD108)
- Magnitude ..... ±.015%
- Arc Sin/Cos Ratio ..... ±.005°

Propagation Delay ..... 0.95 usec with DD108A
1.50 usec with DD108B

Logic ..... Positive true, DTL/TTL compatible
True = +2.0V to +5.5V
False = 0 to 0.8V

Loading ..... Input ..... 3 TTL loads max.
Output ..... 10 TTL loads max.

Power ..... +5 VDC ±5% @450 ma

PHYSICAL

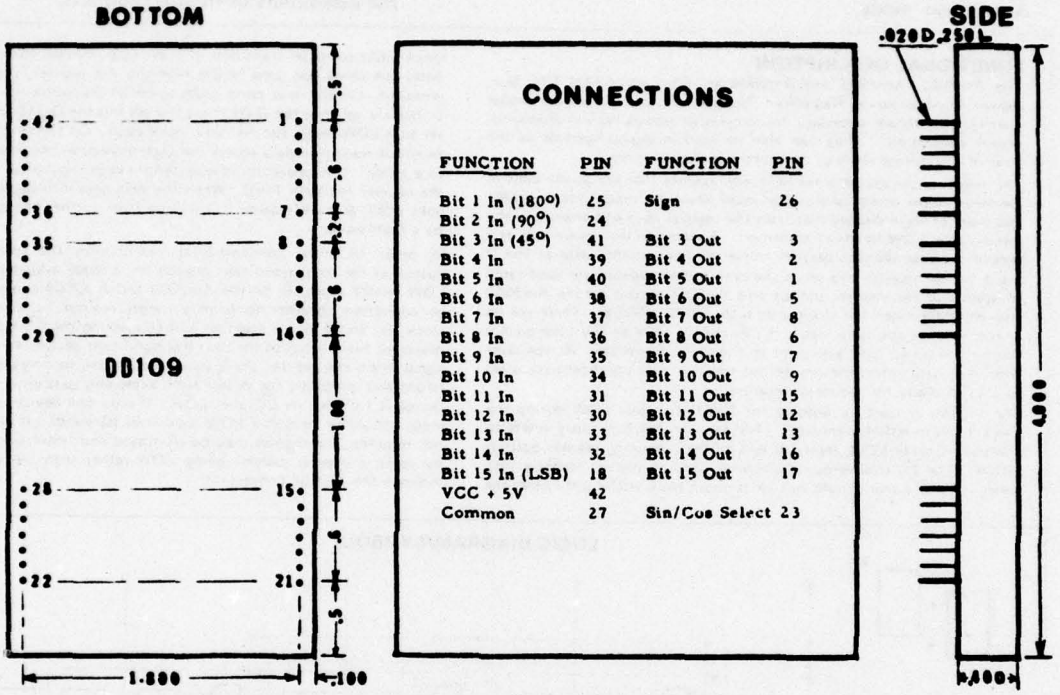
Operating Temp. Range ..... 0 to 70°C

Storage Temp. Range ..... -62 to + 125°C

Size and Weight ..... 2"W x 4"L x 0.4"H, 4 oz.

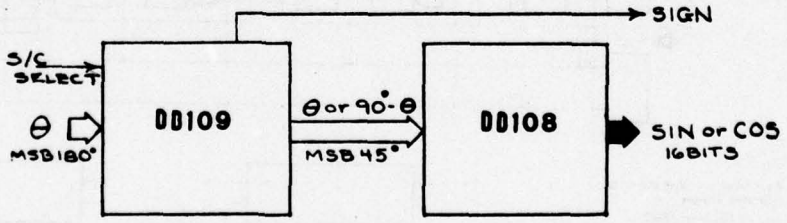
Pins ..... .020" round, gold plated
.250" L min.

INTERFACE ENGINEERING ⇨⇨ angle measurement and control



CONNECTIONS

FUNCTION	PIN	FUNCTION	PIN
Bit 1 In (180°)	25	Sign	26
Bit 2 In (90°)	24		
Bit 3 In (45°)	41	Bit 3 Out	3
Bit 4 In	39	Bit 4 Out	2
Bit 5 In	40	Bit 5 Out	1
Bit 6 In	38	Bit 6 Out	5
Bit 7 In	37	Bit 7 Out	8
Bit 8 In	36	Bit 8 Out	6
Bit 9 In	35	Bit 9 Out	7
Bit 10 In	34	Bit 10 Out	9
Bit 11 In	31	Bit 11 Out	15
Bit 12 In	30	Bit 12 Out	12
Bit 13 In	33	Bit 13 Out	13
Bit 14 In	32	Bit 14 Out	16
Bit 15 In (LSB)	18	Bit 15 Out	17
VCC + 5V	42		
Common	27	Sin/Cos Select	23



APPLICATION ASSISTANCE (617)344-7383

INTERFACE ENGINEERING INC.
300 LINDELOF AVENUE
STOUGHTON, MASS. 02072

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

AJJ

Am2502/2503/2504

Eight-Bit/Twelve-Bit Successive Approximation Registers

Advanced Micro Devices
Complex Digital Integrated Circuits

Distinctive Characteristics

- Contains all the storage and control for successive approximation A-to-D converters.
- Provision for register extension or truncation.
- Can be operated in START-STOP or continuous conversion mode.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Can be used as serial-to-parallel counter or ring counters.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

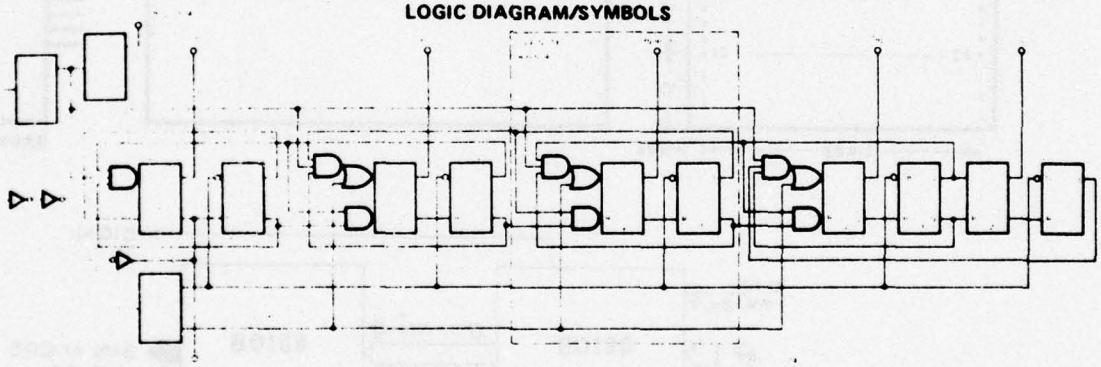
The Am2502, Am2503 and Am2504 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

The registers consist of a set of master latches that act as the control element - in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the Am2502 and Am2504 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input, it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting. After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the Am2503 and Am2504 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the Start signal resets the register, the $\overline{E}$ signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

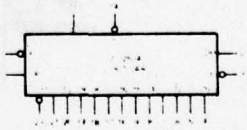
LOGIC DIAGRAM/SYMBOLS



NOTE
1. Cell logic is repeated for register stages
   Q_5 to Q_1 Am2502,3
   Q_6 to Q_1 Am2504
2. Numbers in parentheses are for Am2504



V_{CC} = Pin 16
GND = Pin 8



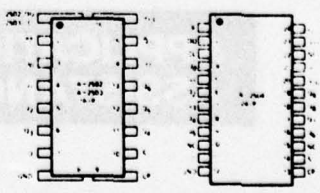
V_{CC} = Pin 16
GND = Pin 12
NC = Pins 10, 15, 22

ORDERING INFORMATION

Package Type	Temperature Range	Am2502 Order Number	Am2503 Order Number	Am2504 Order Number
Molded DIP	0°C to +75°C	AM2502PC	AM2503PC	AM2504PC
Hermetic DIP	0°C to +75°C	AM2502DC	AM2503DC	AM2504DC
Hermetic DIP	-55°C to +125°C	AM2502DM	AM2503DM	AM2504DM
Hermetic Flat Pak	55°C to +125°C	AM2502FM	AM2503FM	AM2504FM
Dice	Note	AM2502XX	AM2503XX	AM2504XX

NOTE The dice supplied will contain units which meet both 0°C to +75°C and -55°C to +125°C temperature ranges

CONNECTION DIAGRAMS
Top View



NOTE PIN 1 is marked for orientation.

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2502XC Am2503XC Am2504XC T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
Am2502XM Am2503XM Am2504XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10%

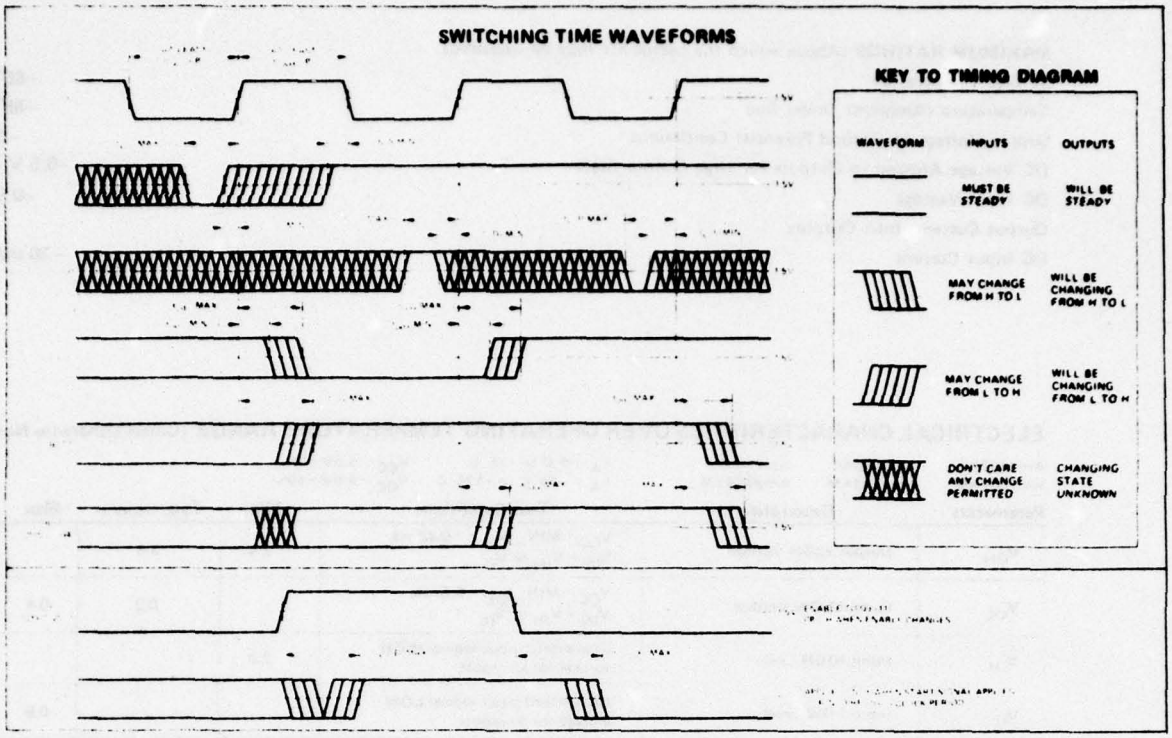
Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.48mA V_{IN} = V_{IH} or V_{IL}			2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 9.6mA V_{IN} = V_{IH} or V_{IL}				0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				6.0	40	µA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			−10	−25	−45	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am2502	XM		65	85	mA
				XC		65	95	
			Am2503	XM		60	80	mA
				XC		60	90	
			Am2504	XM		90	110	mA
				XC		90	124	

Note 1 Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2 Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

Switching Characteristics T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF

Parameters	Description		Min.	Typ.	Max.	Units
t_{pd+}	Turn Off Delay CP to Output HIGH		10	26	38	ns
t_{pd-}	Turn On Delay CP to Output LOW		10	18	28	ns
t_s(D)	Set-up Time Data Input		−10	4	8	ns
t_s(S)	Set-up Time Start Input		0	9	16	ns
t_{pd+}(E)	Turn Off Delay E to Q_7(11) HIGH	(Am2503/4) C_P = H, $\overline{S}$ = L		13	19	ns
t_{pd-}(E)	Turn On Delay E to Q_7(11) LOW			16	24	ns
t_{pwL}(CP)	Minimum LOW Clock Pulse Width			28	46	ns
t_{pwH}(CP)	Minimum HIGH Clock Pulse Width			12	20	ns
f_{max}	Maximum Clock Frequency		15	25		MHz

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC



DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output

FUNCTIONAL TERMS:

Fan-Out *The logic HIGH or LOW output drive capability in terms of Input Unit Loads.*

Input Unit Load One T^2 L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

CP The clock input of the register.

CC *The conversion complete output. This output remains HIGH during a conversion and goes LOW when a conversion is complete.*

D The serial data input of the register.

E The register enable. This input is used to expand the length of the register and when HIGH forces the $Q_7(11)$ register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (Ground).

$Q_7(11)$ The true output of the MSB of the register.

$Q_7(11)$ *The complement output of the MSB of the register.*

Q_i i = 7(11) to 0 The outputs of the register.

S The start input. If the start input is held LOW for at least a clock period the register will be reset to $Q_7(11)$ LOW and all the remaining outputs HIGH. A start pulse that is LOW for a shorter period of time can be used if it meets the set-up time requirements of the $\bar{S}$ input.

DO The serial data output. (The D input delayed one bit).

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

Negative Current *Current flowing out of the device.*

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS: (Measured at the 1.5V logic level).

t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

t_{pd-}(E) The propagation delay from the Enable signal HIGH-LOW transition to the $Q_7(11)$ output signal HIGH-LOW transition.

$t_{pd+}(\bar{E})$ The propagation delay from the Enable signal LOW-HIGH transition to $Q_7(11)$ output signal LOW-HIGH transition.

t_s(D) *Set-up time required for the logic level to be present at the* data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t_s max. and t_s min. before the clock.

$t_s(\bar{S})$ *Set-up time required for a LOW level to be present at the* $\bar{S}$ input prior to the clock transition from LOW to HIGH in order for the register to be reset, or time required for a HIGH level to be present on S before the HIGH to LOW clock transition to prevent resetting.

t_{pw}(CP) The minimum clock pulse width (LOW or HIGH) required for proper register operation.

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

AJJ

Am2502/3 TRUTH TABLE

Time	Inputs			Outputs									
t_n	D	$\overline{S}$	$\overline{E}$	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

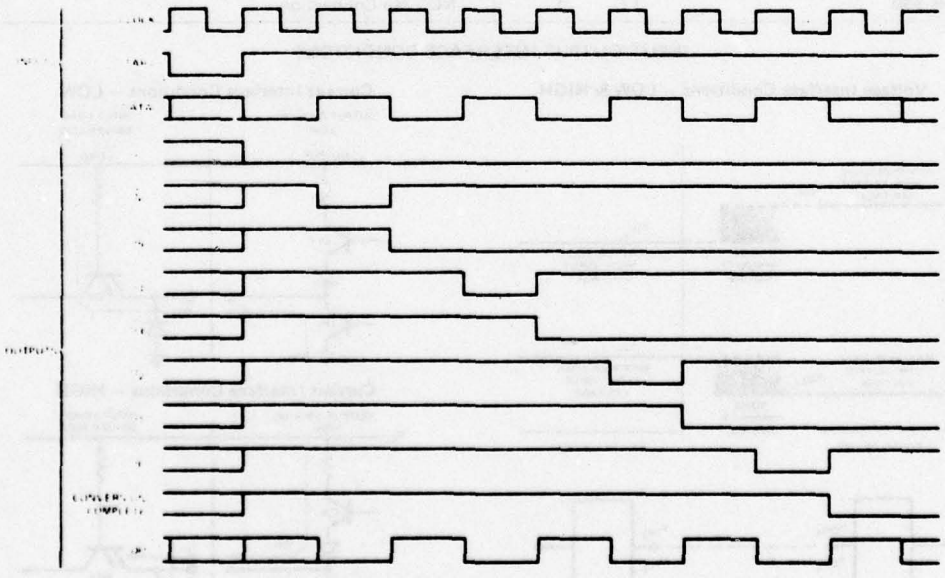
H HIGH Voltage Level
L LOW Voltage Level
X Don't Care
NC No Change

Note: Truth Table for Am2504 is extended to include 12 outputs.

USER NOTES FOR A/D CONVERSION

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of +½LSB the comparator must be biased. If current switches that require a high voltage level to turn on are used, the comparator should be biased +½LSB and if the current switches require a high logic level to turn on then the comparator must be biased −½LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion.
4. The register can be used to perform 2's complement conversion by offsetting the comparator ½ full range +½ LSB and using the complement of the MSB Q_7 (11) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

Am2502/3 TIMING CHART



Am2502/3 LOADING RULES (IN UNIT LOADS)

Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
E (2503)	1	2	2	–	–
DO (2502)	1	–	–	12	6
CC	2	–	–	12	6
Q_0	3	–	–	12	6
Q_1	4	–	–	12	6
Q_2	5	–	–	12	6
Q_3	6	–	–	12	6
D	7	2	2	–	–
GND	8	–	–	–	–
CP	9	1	1	–	–
S	10	1	2	–	–
Q_4	11	–	–	12	6
Q_5	12	–	–	12	6
Q_6	13	–	–	12	6
Q_7	14	–	–	12	6
Q_7	15	–	–	12	6
V_{CC}	16	–	–	–	–

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

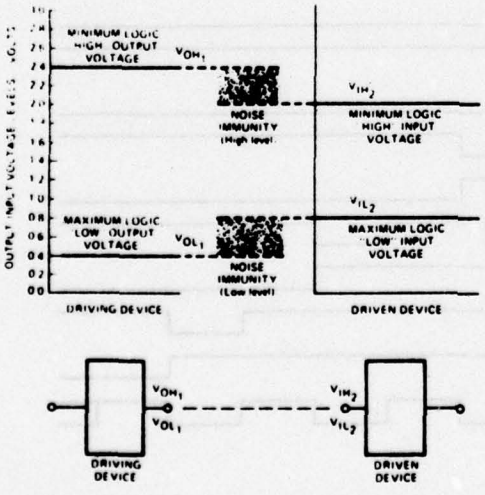
Am2504 LOADING RULES (IN UNIT LOADS)

Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
$\overline{E}$	1	2	2	–	–
DO	2	–	–	12	6
$\overline{CC}$	3	–	–	12	6
Q_0	4	–	–	12	6
Q_1	5	–	–	12	6
Q_2	6	–	–	12	6
Q_3	7	–	–	12	6
Q_4	8	–	–	12	6
Q_5	9	–	–	12	6
NC	10	–	–	–	–
D	11	2	2	–	–
GND	12	–	–	–	–
CP	13	1	1	–	–
S	14	1	2	–	–
NC	15	–	–	–	–
Q_6	16	–	–	12	6
Q_7	17	–	–	12	6
Q_8	18	–	–	12	6
Q_9	19	–	–	12	6
Q_{10}	20	–	–	12	6
Q_{11}	21	–	–	12	6
NC	22	–	–		
Q_{11}	23	–		12	6
V_{CC}	24	–	–	–	–

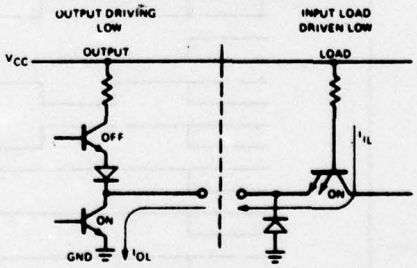
NC = No Connection

INPUT/OUTPUT INTERFACE CONDITIONS

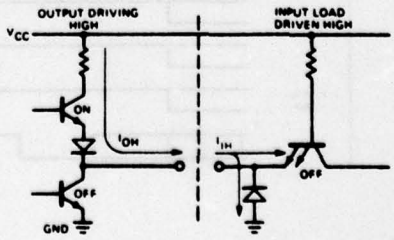
Voltage Interface Conditions – LOW & HIGH



Current Interface Conditions – LOW

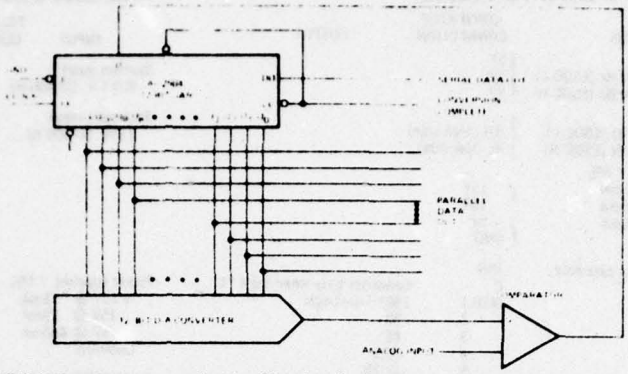


Current Interface Conditions – HIGH



THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

Am2502/3/4 APPLICATION
Continuous Conversion Analog-to-Digital Converter

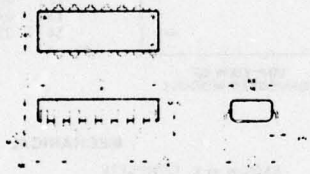


This shows how the Am2502/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed continuous conversion Analog to Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator with typical conversion rates of 100,000 conversions per second. A 10-bit continuous conversion can be performed by connecting Q_1 to Q_3 and using Q_1 as the conversion complete signal. The comparator can be the Am111 precision comparator, Am106 high-speed comparator, or Am686 very high speed comparator.

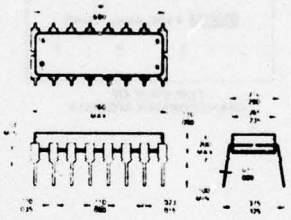
PHYSICAL DIMENSIONS

Am2502/3

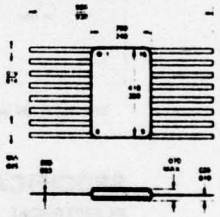
16-Pin Molded DIP



16-Pin Hermetic DIP

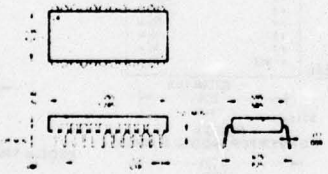


16-Pin Flat Pak

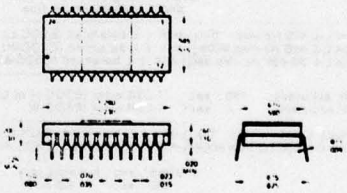


Am2504

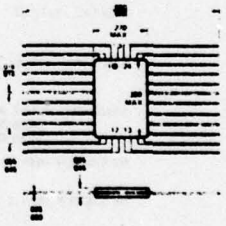
24-Pin Molded DIP



24-Pin Hermetic DIP

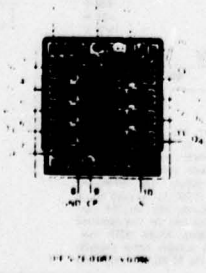


24-Pin Flat Pak

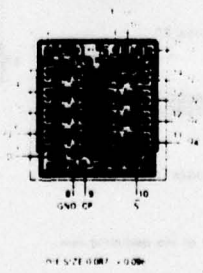


Metallization and Pad Layout

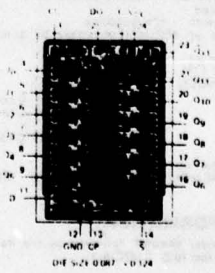
Am2502



Am2503



Am2504



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

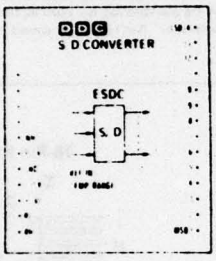
Advanced Micro Devices can not assume responsibility for use of any circuitry described other than circuitry entirely embodied in an Advanced Micro Devices product.

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

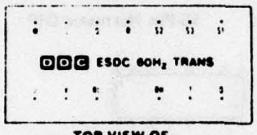
PIN DESIGNATIONS AND CONNECTIONS

Models ESDC or ERDC, H or L (400 Hz)

INPUT	CONVERTER CONNECTION	OUTPUT
Synchro input: 11.8V L-L, 400 Hz (ESDC L) or 90V L-L, 400 Hz (ESDC H)	S1, S3, S2	
Reference input: 26V, 400 Hz (ESDC L), or 115V, 400 Hz (ESDC H)	RH (high side), RL (low side)	
Power Supplies ±5%: +15V @ 55mA, −15V @ 30mA, +5V @ 280mA, Common	+15V, −15V, +5V, GND	
Logic "0" forces data hold	INH	
	C	Converter busy when logic "1"
	MSB 1	180° True Logic
	2	90
	3	45
	4	22.5
	5	11.25
	6	5.625
	7	2.813
	8	1.406
	9	0.7031
	10	0.3516
	11	0.1758
	12	0.08799
	13	0.04395
	14	0.02197



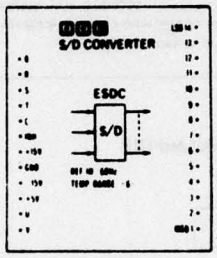
TOP VIEW OF MODULE



TOP VIEW OF TRANSFORMER MODULE

Model ESDC-6 (50-400 Hz)

INPUT	TRANSFORMER CONNECTION	CONVERTER CONNECTION	OUTPUT
Synchro input: 90V L-L, 50-400 Hz	S1, S3, S2		
Reference input: 115V, 50-400 Hz	RH (high side), RL (low side)		
	R connect to R		
	Q, Q' connect to Q		
	S connect to S		
	W (no connection)		
	T connect to T		
	V connect to V		
	U connect to U		
Power supplies ±5%: +15V @ 75mA, −15V @ 50mA, +5V @ 400mA, Common		+15V, −15V, +5V, GND	
Logic "0" forces data hold		INH	
		C	Converter busy when logic "1"
		MSB 1	180° True Logic
		2	90
		3	45
		4	22.5
		5	11.25
		6	5.625
		7	2.813
		8	1.406
		9	0.7031
		10	0.3516
		11	0.1758
		12	0.08799
		13	0.04395
		14	0.02197



TOP VIEW OF CONVERTER MODULE

SPECIFICATIONS

ELECTRICAL

PARAMETER	VALUE
ACCURACY(1)	±4 minutes ±0.9 LSB
RESOLUTION	14 Bits
CODING	natural binary 'angle'
DIGITAL OUTPUT	parallel, positive logic, DTL TTL levels, 14 angle data, 1 inhibit and 1 converter busy line
SYNCHRO INPUT(2)(3)	11.8V rms L-L 400 Hz into 10KΩ min. L-L balanced (ESDC-L) 90V rms L-L 400 Hz into 600KΩ min. L-L balanced (ESDC-H) 90V rms L-L 50-400 Hz into 4MΩ min. L-L balanced (ESDC-6)
SYNCHRO INPUT RATES(4)	0 to 360° sec., full accuracy; 180° sec² = 1 LSB error (ESDC-H or L) 0 to 180° sec., full accuracy; 6 sec² = 1 LSB error (ESDC-6)
RESOLVER INPUT(2)(3)	11.8V rms L-L 400 Hz into 10KΩ min. L-L balanced (ERDC-L) 90V rms L-L 400 Hz into 600KΩ min. L-L balanced (ERDC-H)
RESOLVER INPUT RATES(4)	0 to 360°/sec., full accuracy 180° sec², 1 LSB error
REFERENCE INPUT(2)(3)	26V at 5mA rms 400 Hz (ESDC or ERDC-L) 115V at 0.6mA rms 400 Hz (ESDC or ERDC-H) 115V at 2.5mA rms 50-400 Hz (ESDC-6)
POWER SUPPLY REQUIREMENTS(5)	+15V at 75mA, −15V at 50mA, +5V at 400mA

(1)Accuracy applies over operating temperature range, ±5% variation of power supplies and ±10°, amplitude and frequency variation.
(2)Other input voltages and frequencies available
(3)Transformer isolated
(4)Available for use with ±12V supplies
(5)14 R.P.S. available on 400 Hz converters by specifying suffix FT

ENVIRONMENTAL

TEMPERATURE RANGES

OPERATING	−55°C to +85°C (ESDC-H, L, or 6-1) 0°C to +70°C (ESDC-H, L, or 6-3)
STORAGE	−55°C to +125°C

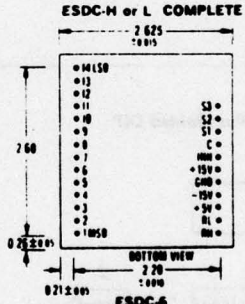
OTHER ENVIRONMENTAL:
MEETS REQUIREMENTS OF MIL-STD-202C, METHODS 204A, 106B, 107B, 101B and 105

ORDERING INFORMATION

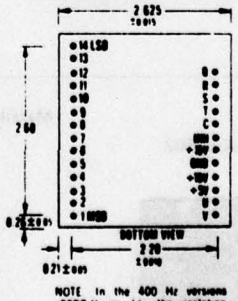
To order, specify model desired, followed by the designation of the operating temperature range required (e.g. ESDC-6-1)

MECHANICAL

ESDC-H or L COMPLETE

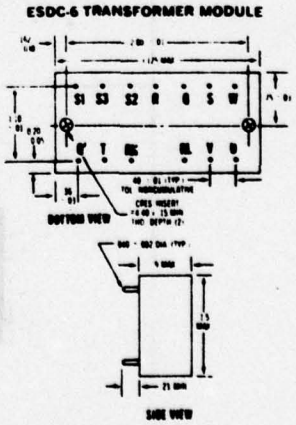


ESDC-6 CONVERTER MODULE ONLY



NOTE: In the 400 Hz versions (ESDC H or L), the isolation transformers are packaged together with the converter in a single module. The 50-60 Hz version (ESDC-6) is supplied in two modules, one for the converter and one for the isolation transformers (Model 9010 mating sock accepts either module but not the 50-60 Hz transformer module.

ESDC-6 TRANSFORMER MODULE



THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

Timing

Figure 6 shows the timing waveforms of the converters. Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a CONVERTER BUSY pulse. During the 3μs "busy" pulse, the output data is changing and should not be transferred into the computer output buffer. The converter will ignore an INHIBIT command applied during the "busy" interval until that interval is over. A simple method of interfacing to a computer is to: (a) apply the inhibit, (b) wait 5μs, (c) transfer the data, and (d) release the inhibit.

Although the computer usually will require that the data be synchronized and loaded as described above, it can be read-out asynchronously into a holding register using the trailing-edge of the "C" signal to effect the parallel transfer. This is shown in Fig. 7. In this configuration the data out of the register will change smoothly from θn to $\theta n + 1$.

Testing

Because of the high accuracy of these converters, only laboratory-grade synchro or resolver substitution boxes or standards can be used. To avoid costly test equipment, we invite you to use DDC's facilities for "source inspection," at no extra cost.

To test the unit, arrange your test equipment as shown in Figure 8. A lamp-driver or suitable readout is necessary for each of the data outputs. We recommend the circuit shown in Fig. 5C. The Synchro Standard is set to the test angles. The angles corresponding to the lights which are on are added and compared with the standard angle. Maximum observed error shall be less than ±4 minutes ±0.9 LSB over the temperature range. A table of angles versus bits is given in Fig. 9. A typical room-temperature error curve is shown in Fig. 10. Each quadrant is identical, and error has been shown for the first quadrant. Error limits are also indicated for temperature extremes.

Figure 6: Timing

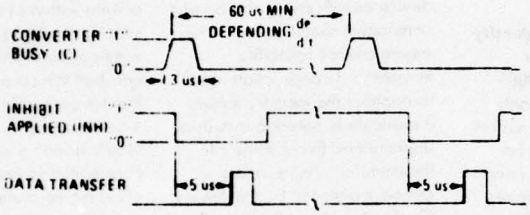


Figure 8: Test Configuration

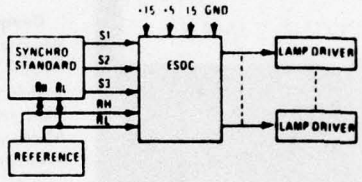


Figure 7: Asynchronous Parallel Transfer

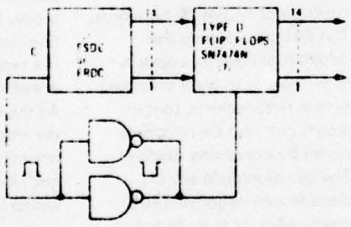
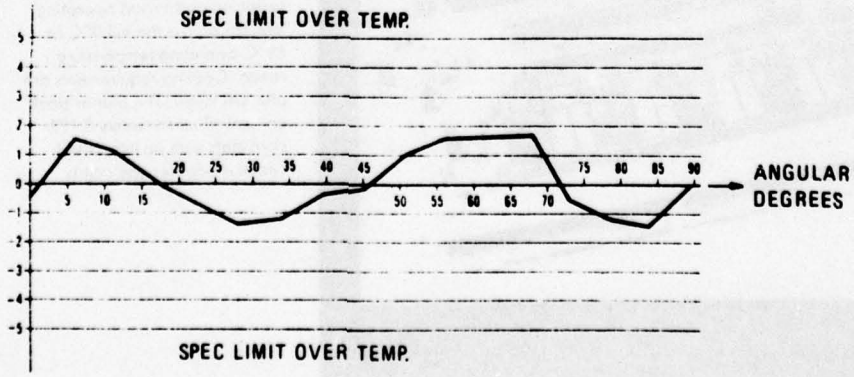


Figure 9: Angles vs. Bits

MSB	1	180
	2	90
	3	45
	4	22.5
	5	11.25
	6	5.625
	7	2.813
	8	1.406
	9	0.7031
	10	0.3516
	11	0.1758
	12	0.08799
	13	0.04395
LSB	14	0.02197

Figure 10: Typical Error, Minutes, Each Quadrant, 25°C for ESDC



2065

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

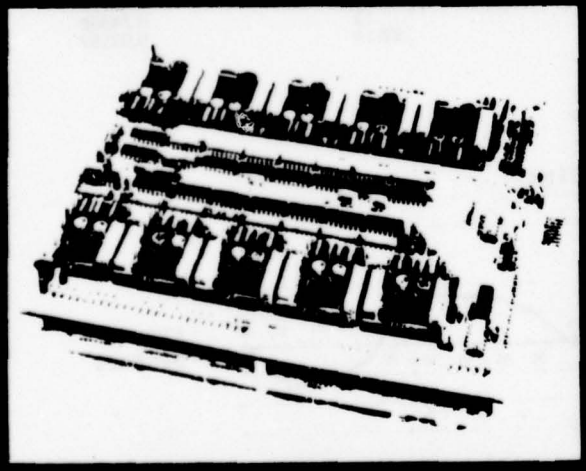
AMPEX

Ampex Computer Products Corporation
13031 West Jefferson Boulevard
Marina del Rey, California 90291

AMPEX CORE MEMORY MODULES, 250 NANOSECOND ACCESS AND 650 NANOSECOND CYCLE TIMES

Fast and compact
The Ampex 2065 core memory is faster and more compact than any other 20-bit word length memory available to the OEM. Access time = 250 ns, cycle time 650 ns. It measures only 8 inches high x 10 inches deep x 2 inches wide.

Unequaled packing density
You can store more than 160,000 bits in a single 2065 module which occupies only 170 cubic inches in your system. All circuitry is packaged on three removable printed circuit boards — data register, drive, and planar core-stack. The compact dimensions of the 2065 provide inherent packaging flexibility which is superior to that of large single board systems. As a result, you have more space available for other important system functions.



Quality assured reliability
The 2065 has more built-in reliability than any comparable OEM memory. All critical areas of the memory receive extra attention, and design simplicity is followed throughout. Conservative derating practices, device qualification, and careful component specification further ensure overall reliability. Ruggedized construction used throughout the memory makes it particularly suited to industrial applications. Every stage of the manufacturing process is closely monitored by the Ampex Quality Assurance Department in accordance with MIL-Q-9858A.

Simple interface, easily expandable
Up to eight 8K x 20 modules can be combined in parallel for a capacity of 65,536 20-bit words. This flexibility permits the addition of memory capacity in increments to meet changing system requirements. Longer words can also be accommodated by combining modules. The use of module select decode and negative-TRUE open collector outputs makes interfacing extremely simple.

Faster switching, broader margins
The 2065 uses 18-mil temperature stable cores to provide fast switching and broad operating margins across the full 0°C to 55°C operating temperature range. Cooling requirements are also simplified. The planar stack consists of up to twenty 8,192-core mats with an integrated circuit diode decode matrix.

Maximum output, less noise
Coupled noise is reduced, and a maximum output signal is provided by high density core packaging which permits shorter sense, X and Y lines. Cores are aligned in a double-herringbone pattern with a center-to-center spacing (in the sense/digit winding direction) of less than one-half the core diameter. Precise core alignment is maintained by a proprietary silastic bonding which dissipates core switching heat and minimizes temperature gradients by providing a thermal path to the substrate.
Only two voltages are required +5 and −15.

Temperature compensated
There is no need for power supply temperature compensation, since drive current sources are temperature compensated in each module.
All the interconnections within the module between circuit boards are provided. No additional low level back panel wiring is required.

Modular interchangeability
Complete module-to-module uniformity is provided by optimization of memory timing, drive currents, and threshold levels in each module. Your field support and spares requirements are greatly simplified by the ability to interchange any module within a system or between different systems. Each module is a complete memory with self contained data register and timing and control functions.

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

AMPEX
Ampex Computer Products Corporation
13031 West Jefferson Boulevard
Marina del Rey, California 90291

2065

2065 specifications

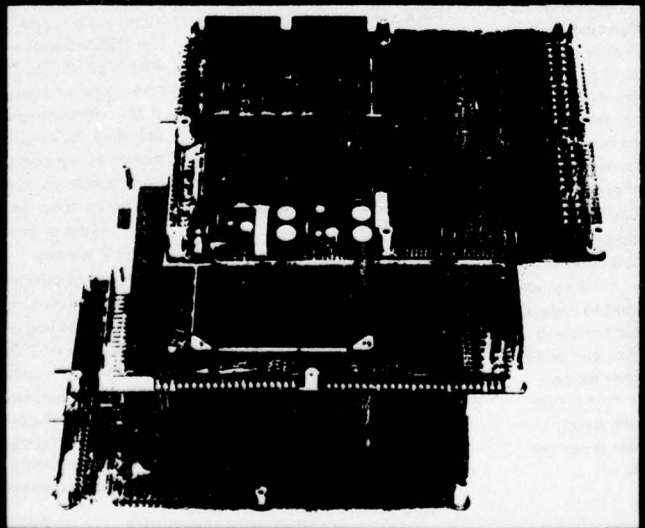
Access time	250 nanoseconds
Cycle time	650 nanoseconds
Capacity	2,048, 4,096, 8,192 words of 10, 16, 18 or 20 bits in a single module. Expandable in modules to a capacity of 65,536 words. Longer words can also be accommodated by combining modules.
Operational modes	Read-Restore Clear-Write Read-Modify-Write
Interface characteristics	TTL negative TRUE logic is used.
Standard input signal lines	Address input Data input Start input cycle (SIC) Start output cycle (SOC) Read-modify-write control Module select inputs (used to address separate modules in a multi-module system)
Standard output signals	Data output Unit available signal (memory busy) Data available signal End of cycle signal

DC power requirement

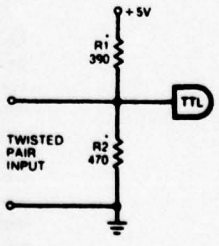
Voltage	Regulation	Current (Max)
−15 VDC	±3%	7.2 amps (20 bits)
+5 VDC	±5%	4.5 amperes source

No temperature compensation of either voltage is necessary.

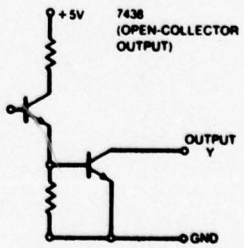
Weight	4.0 lb.
Dimensions	8.0 inches (203.2 mm) high 10.0 inches (254.0 mm) deep 2.0 inches (51 mm) wide (2.125 inches with optional metal cover)
Operating Environment	0°C to 55°C ambient temperature Up to 90% relative humidity with no condensation
Non-operating environment	−55°C to +85°C ambient temperature Up to 95% relative humidity with no condensation
Available options	Byte control (2 bytes maximum) Zone control (2 zones maximum) External logic clear (Internal logic reset to ready) External memory register reset (Output lines at high logic state) External memory register transfer (For byte or zone control) Metal extractor handle Metal covers



Typical Input Receiver

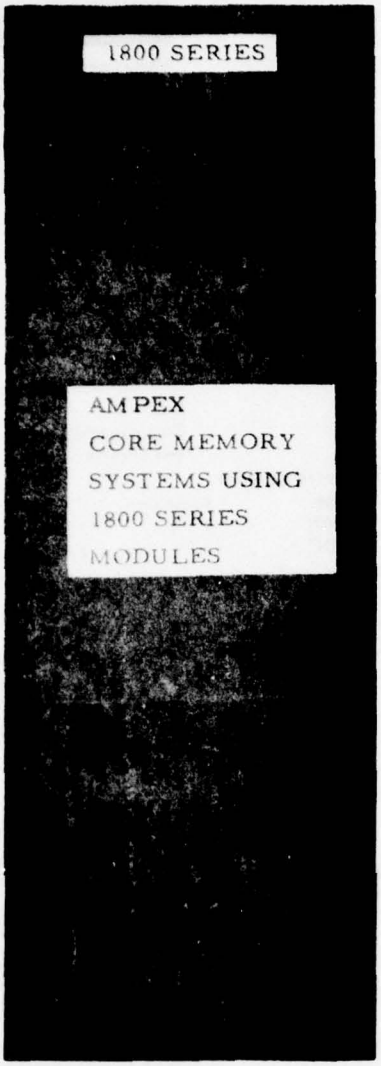


Typical Output Driver



*R1 and R2 will be as shown unless otherwise specified.

Litho in U.S.A. C-341 11/72

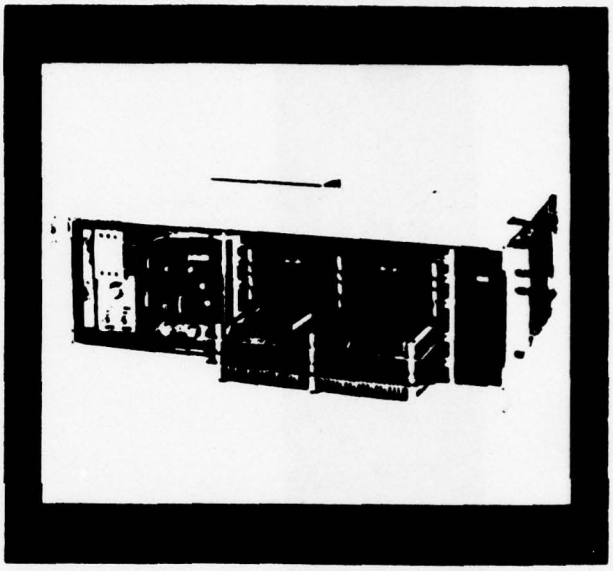


AMPEX
Ampex Computer Products Corporation
13031 West Jefferson Boulevard
Marina del Rey, California 90291
A subsidiary of Ampex Corporation

Tailored to your needs
Complete Ampex 1800 Series core memory systems are designed to provide exactly the configurations and capacities you need for specialized OEM systems – at off-the-shelf prices. There are standard configurations which accommodate from two to eight memory modules. Any desired combination of standard or special interfaces, power supplies, testers, or blowers can be specified. System capacity extends all the way to 65,536 18-bit words. Word size is completely flexible – 9, 12, 18 bits or longer if you choose. Access times are 230, 250, or 340 nanoseconds, and cycle times are 600, 650 or 850 nanoseconds, depending on the model you select. (Detailed performance and specification data on 1800 Series core memories is contained in individual Ampex product sheets on the following models: 1860, 1865, 1885, and the ruggedized 1800M Series.)

Lower design costs
You get a customized memory system – ready to plug in – for only a little more than module prices. You save even more money and time because your available design manpower can devote more effort to other portions of the system.

Higher packing density
Each of the basic 1800 Series memory configurations is carefully designed to provide maximum compactness and space-saving. You can build a complete Ampex memory system into your own system without sacrificing space required for other important system functions.



Standard or special interfaces
There are no interface problems when building the 1800 Series into your system. A standard interface is included, and space is provided in the memory card cage for any special interface you may require. If you wish, we also can supply special interface cards designed to your specification.

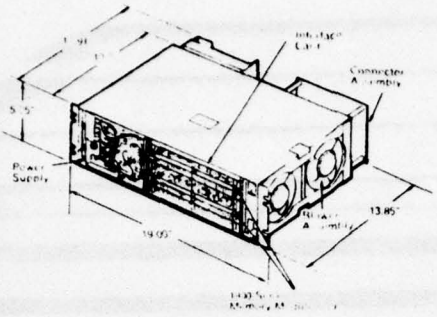
Fast, reliable, and expandable
The 1800 system is more than a fast, modular, building block memory customized to your specific requirements. It also has traditional Ampex reliability, full temperature range performance, and interchangeability.
The MTBF is 10,000 hours, with an operating range from 0°C to 55°C. For applications requiring a ruggedized memory, the 1800M Series with an extended 0°C to 70°C temperature range and resistance to shock, vibration and dust can be specified. All Ampex 1800 Series memories are completely uniform from module-to-module and can be interchanged within a single system or between different systems.

Optional subsystems
You can select as many or as few subsystems as you need. These include 115V or 220V blower assemblies, one or two 115V or 220V power supplies, and an on-line tester which can completely check-out total system operation. Standard connectors are supplied with all configurations.

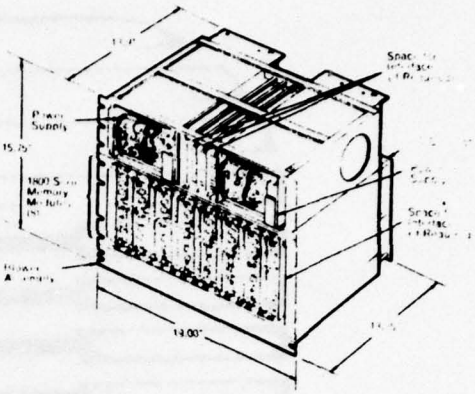
THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

AMPEX
Ampex Computer Products Corporation
13031 West Jefferson Boulevard
Marina del Rey, California 90291

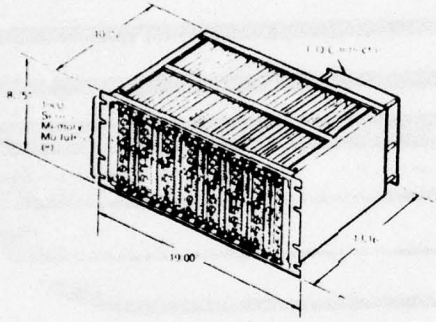
1800



Two module configuration with interface card, power supply, connector assembly, and blower assembly.

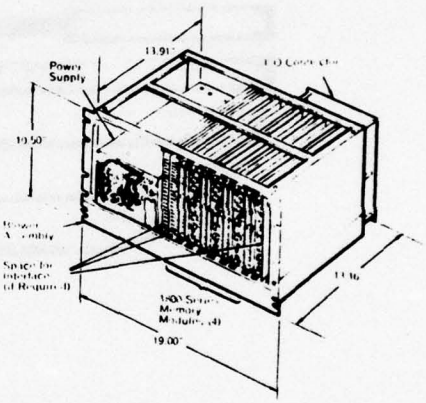


Eight module configuration with two power supplies, blower assembly, I/O connector, and space for interface.

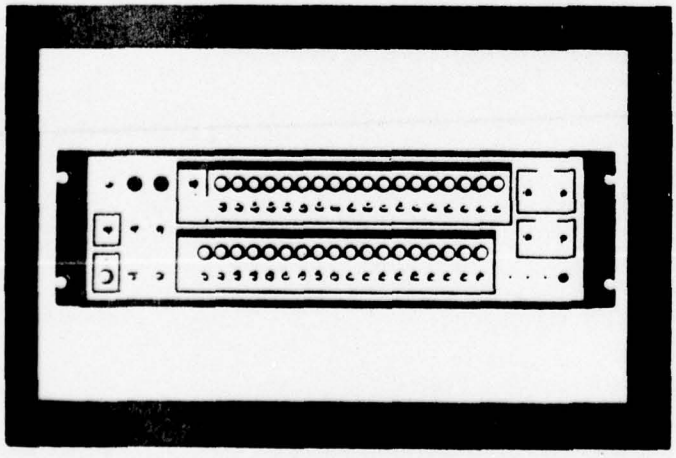


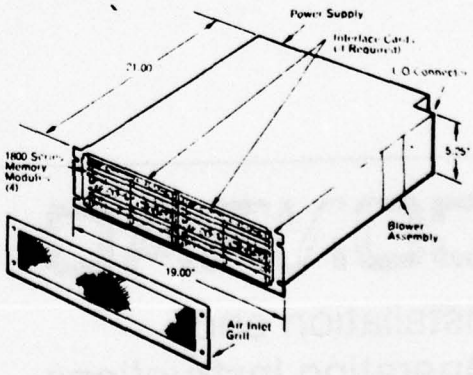
Eight module configuration with I/O connector, and space for interface.

An optional on-line tester capable of completely checking-out total system operation is available with most 1800 Series module configurations. Optional 115V or 220V power supplies also can be selected, as well as optional 115V or 220V blower assemblies. All configurations have standard connectors.



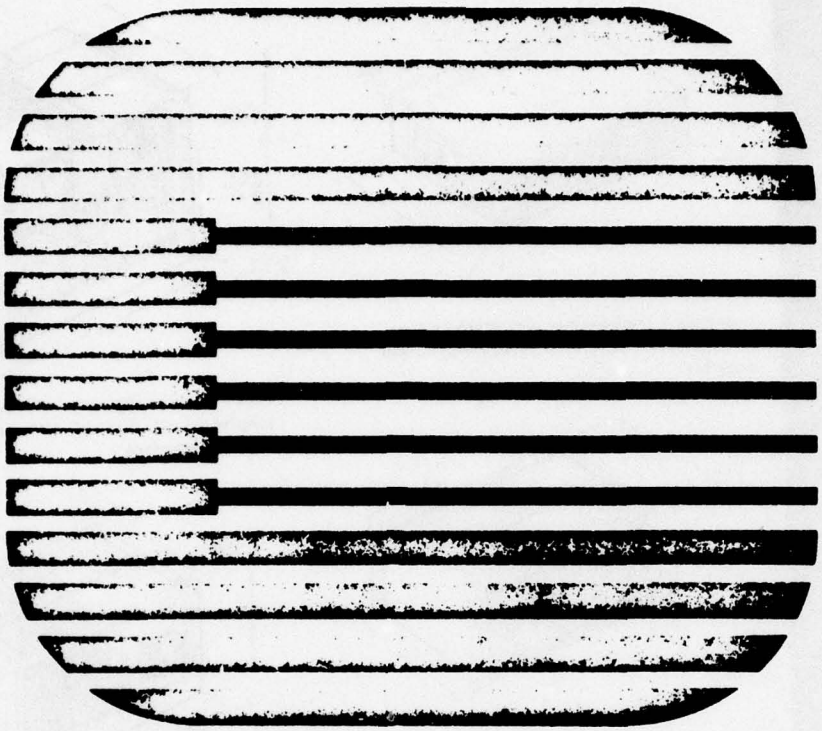
Four module configuration with power supply, blower assembly, I/O connector, and space for interface.





Four module configuration with power supply, blower assembly, I/O connector, air inlet grill, and space for interface.

Litho in U.S.A. C-330 11/72



CONRAC

Installation and Operating Instructions

Color Television Monitor
Model 5111

IB 106313-001

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

GENERAL DESCRIPTION

FEATURES

*Preset controls for contrast, brightness, and chroma

*Continuously variable aperture correction

*Negative black matrix shadow mask CRT

*Solid-state circuitry

*All setup controls from accessible pull-out drawer

*Advanced mechanical design assures structural integrity in all mounting configurations

DESCRIPTIVE INFORMATION

The advanced design of the electronic circuitry in the 5100 Series is such that the CRT itself becomes the limiting factor in performance. A keyed backporch clamp maintains true black level when operating with either composite or non-composite video. New operator conveniences include the addition of preset controls on all versions for contrast, brightness, chroma and phase.

All secondary controls and adjustments are located in a pull-out drawer below the picture tube. This location provides maximum operator convenience, prevents unauthorized tampering and gives the monitor a clean, eye-pleasing apperance.

The chassis is arrayed in "U" configuration, permitting physical separation of power supply deflection from video amplifier/decoder circuit stages. Modular circuit boards and power supplies are interconnected by a quick-disconnect wiring harness, thus simplifying maintenance procedures.

External packaging is compatible with the most up-to-date installations and employs front and back frames. Aluminum extrusions, running from front to back at each side, support full length recessed carrying handles. Sheet metal covers, above and below the extrusions, complete the package.

APPLICATION

The 5100 Series 19- and 25-inch television monitors are especially useful for group viewing in auditoriums, classrooms, lecture halls, industrial training areas, hospital paging systems, preview rooms, and other audience viewing applications. Rigid mechanical construction throughout assures structural integrity and protects all components. This is of particular importance for applications where monitors must be moved from location to location or hung from ceiling, wall or floor stand.

All units comply with U.S. Department of Health, Education and Welfare X-Radiation Safety Rules, 21 CFR, Subchapter J, applicable at time of manufacture.

PRODUCT IDENTIFICATION

First character – Identifies the Series (5)

Second character – Identifies the significant update level (1)

Third character – Identifies the option package (1 = Standard Package)

Fourth character – Identifies the color decoder standard (0 = Not Used; 1 = RGB; 2 = NTSC; 3 = PAL B; 4 = PAL M; 5 = SECAM 50; 6 = SECAM 60)

Fifth character – Identifies mechanical configuration (C = Cabinet; N = Naked, or Chassis; RS = Rack mount with slides; Y = Yoke, or Bail Mount)

Final characters – Identify the size of the CRT

TECHNICAL SUMMARY

ELECTRICAL SPECIFICATIONS

Input Power	Voltage:	100V ± 10%, 50/60Hz 120V ± 10%, 50/60Hz 220V ± 10%, 50/60Hz 240V ± 10%, 50/60Hz
	Power:	125 watts, nominal
	Power Connection:	Captive 6-foot cord with three-prong connector plug
Input Signals	Composite:	Loop-through or switchable to internal 75Ω termination. 1.0V peak-to-peak, nominal (0.35V to 2.0V) Sync is negative.
	Non-Composite:	0.7V peak-to-peak, nominal (0.25V to 1.4V). Black negative.
Video Input	Return Loss:	Greater than 40dB
Video Response	*Monochrome signal applied* ± 1dB to 5 MHz	
Differential Gain	Less than 5% for luminance of 0fL to 20fL.	
Aperture Correction	A continuously adjustable front panel control provides up to 6dB boost at 3.2MHz.	
Decoder Accuracy	Decoder error less than 1.5°.	
Linearity and Geometry	No point on raster deviates from its proper position by more than 2% of raster height.	
Convergence	On the 19-inch models, does not deviate more than .040" or 1.02mm (.051" or 1.30mm on 25" models) from picture height in a centrally located area bounded by a circle. The diameter of this circle is equal to the picture height. Elsewhere, the deviation does not exceed .080" or 2.04mm (.100" or 2.54mm on 25-inch models).	
Color Temperature	The range of RGB gain adjustments is sufficient to permit setting white color temperature to 6500°K (factory setting) or 9300°K.	
Color Temperature Accuracy	Color temperature of white does not change by more than one MPCD unit between monochrome and color input signals.	
Interlace	Better than 90%.	
Raster Size Regulation	Less than 1% change, 0% to 100% APL (Average Picture Level) at peak 20fL luminance.	
Black Level Stability	DC restorer maintains black level shift less than 1% of peak luminance from 10% to 90% APL.	
Discernible Shades of Gray	10 minimum.	
Vertical Retrace Time	1000μsec nominal.	
Horizontal Retrace Time	10μsec nominal.	
Radiation	All units comply with the U.S. Department of Health, Education and Welfare X-Radiation Safety Rules, 21 CFR, Subchapter J, applicable at time of manufacture.	
Ambient Temperature and Humidity	10° to 50°C operating temperature; 10% to 90% relative humidity; no condensation.	

MECHANICAL CONFIGURATION

Construction

The chassis, which is constructed of heavy-gauge aluminum, is arrayed in "U" configuration, permitting physical separation of power supply deflection from video amplifier/decoder circuit stages. Modular circuit boards and power supplies are interconnected by quick-disconnect wiring harnesses, simplifying maintenance procedures.

External packaging is compatible with the most up-to-date installations.

Frames

Aluminum extrusions, running from front to back at each side, form full-length recessed carrying handles. Sheet metal covers, above and below the extrusions, complete the package. These are easily removable for maintenance purposes. Conversion from cabinet to rack mounting is accomplished by removing the sheet metal covers and side extrusions and installing rack rails. The CRT is finished in black and all exposed knobs and switches are dull finish plated for minimum viewer distraction.

Weight

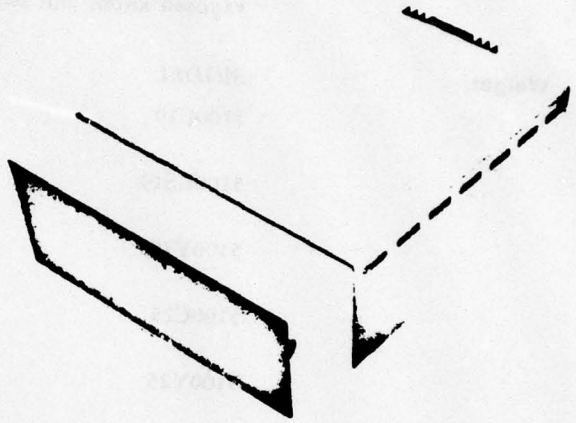
MODEL	*NET WEIGHTS*	*SHIPPING WEIGHTS*
5100C19	99 lbs. 44.9 kilos	112 lbs. 50.8 kilos
5100RS19	98 lbs. 44.5 kilos	111 lbs. 50.4 kilos
5100Y19	99 lbs. 44.9 kilos	112 lbs. 50.8 kilos
5100C25	146 lbs. 66.2 kilos	158 lbs. 71.7 kilos
5100Y25	146 lbs. 66.2 kilos	158 lbs. 71.7 kilos

General DataComm Industries, Inc.
131 DANBURY ROAD, WILTON, CONNECTICUT 06897, TELEPHONE (203) 762-0711

GDC 201-9(R) LSI SYNCHRONOUS MODEM

FEATURES:

- **LSI Technology**
- **2000 or 2400 bps Operation**
- **Remote Analoop® and Dataloop® Addressable Diagnostics for Point-to-Point and Multipoint Applications**
- **Dial or Dedicated, Two-Wire or Four-Wire Operation**
- **Stand Alone or Rack Mount**
- **Alternate Voice**
- **Secondary Channel, Forward or Reverse Operation**
- **WECO 201A or 201B Compatible**
- **Local Analoop® and Loopback Self-Test**

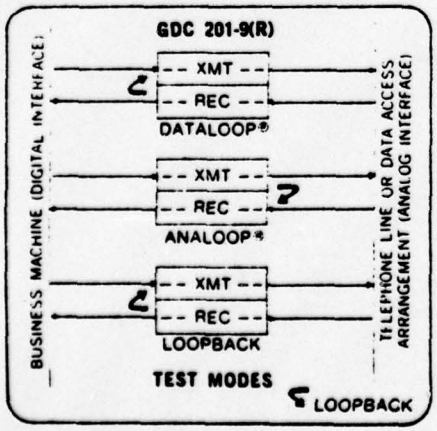


APPLICATION

The General DataComm 201-9(R) is a synchronous 2000 or 2400 bps modem designed to operate over unconditioned 2- or 4-wire type 3002 private lines or over the DDD switched network via the Manual Data Coupler CDT (1000A). The GDC 201-9(R) is fully compatible with WECO 201A (2000 bps) or 201B (2400 bps) data sets. Standard features include automatic fast sync, clear to send delay, carrier detect, external/-internal transmitter timing and MARK hold on receive data when carrier is lost.

Available for rack mounting (201-9R) at the CPU site or as a stand alone, single channel subset (201-9) for remote locations, the General DataComm 201-9 (R) LSI modem incorporates unique diagnostic functions which permit local verification of modem and system operation without the need for special tools or test equipment.

The unit is also available equipped with a diagnostic control card which permits the use of remote addressable diagnostics on a multipoint system. Simple front panel diagnostic switch controls and lighted indicators on both configurations provide complete performance assurance at your installation.



UNIQUE DIAGNOSTICS

Unsurpassed local and remote diagnostics inherent in the GDC 201-9(R) provide for rapid trouble shooting within the entire communications system. The remote Dataloop® diagnostic feature of the 201-9(R) provides remote loopback of the modem on the digital side in either point-to-point or multipoint systems. The unique Analoop® diagnostic command will loop the local or remote modem back on itself on the analog side, as well as the private line's receive side to the transmit side.

In multipoint applications an Address Generator is provided which generates a unique address associated with each remote modem. Therefore, by use of the Analoop® and Dataloop® diagnostics, each individual remote location can be analyzed with respect to terminal, modem, or private line failure. This concept of Addressable Diagnostics allows a

user to isolate faults in a matter of minutes.

In addition to the remote Addressable Diagnostic features, there are others which aid in diagnosing system problems. These include a Test Generator/Recognizer and an Alternate Voice facility. The Alternate Voice facility includes Ring Signal transmission circuitry, Ring Signal indicator, and interface for the GDC auxiliary telephone set. The auxiliary telephone set provides alternate voice capability and also monitoring capability without interfering with data transmission.

SPECIFICATIONS

Operating Modes:	Simplex or half-duplex on two-wire lines and half or full-duplex on four-wire lines; strap selectable between two-wire and four-wire operation.
Modulation:	Differential phase shift keyed 1800 Hz carrier, four phase. Transmit signal includes full bandwidth required for WECO 201 compatibility.
Operating Speeds:	2000 or 2400 bits per second, serial, synchronous on DDD or unconditioned 3002 lines.
Carrier Detect Response:	Operate Time 10 ±1 ms Release Time 8 ±1 ms
Transmit Level:	+2 to −10 dbm, adjustable via calibrated potentiometer.
Receive Level:	Nominal −10 to −40 dbm, adjustable via calibrated potentiometer. Dynamic range ±15 db around nominal.
Transmit Clock:	(strap selectable) *Internal:* 2000 or 2400 Hz ±0.01% square wave *External:* 2000 or 2400 Hz ±0.01% square wave 50 ±5% duty cycle
Receive Clock:	2000 or 2400 Hz square wave synchronized with incoming data. Receive data transition coincides with positive edges of clock.
Fast Sync:	Provides for externally imposing Fast Sync where time between messages is less than 10 ms.
Equalizer:	Statistical equalizer provides equalization of most commonly encountered telephone line amplitude and delay characteristics.
EIA RS-232B/C Compatible:	Input: SPACE (or ON) +3 to +25 V MARK (or OFF) −3 to −25 V Output: SPACE (or ON) +11 to ±1 V MARK (or OFF) −10 ±1 V
Power Supply Requirements:	AC Power: 115 V, 60 Hz 15 Watts
Operating Temp:	0 to 70°C
Storage Temp:	−20°C to 85°C
Rel. Humidity:	5% to 95%

ORDERING INFORMATION

Specify:

Configuration

List 1	2000 bps Operation
List 2	2400 bps Operation

Options

List 3	Remote Diagnostics
List 4	Single Channel Address Generator/Telephone
List 5	Rack Mount Address Generator/Telephone for up to 12 modems
List 6	Remote Telephone for Alternate Voice
List 7	Reverse Channel (75/110 baud)
List 8	Secondary Channel

For additional information, contact:
Marketing Department
General DataComm Industries, Inc.
131 Danbury Road
Wilton, Connecticut 06897
Telephone: (203) 762-0711
TWX: Wilton 710-479-3210
TWX: Montreal 610-421-3221
Telex: Brussels 846-26808

Printed in U.S.A.
© General DataComm Industries, Inc. 1973
® Registered Trademark General DataComm Industries, Inc.

9DPL5M

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

1. SPECIFICATIONS

The INFOTON VISTAR GT is a stand-alone alphanumeric display terminal for use in data entry and retrieval systems where a highly flexible interaction between man and machine is desired. The VISTAR/GT incorporates such important standard features as conversational mode, and an Infotone which operates on the bell code. Complete specifications are listed in INFOTON Document No. 02421.

1.1 BASIC SYSTEM

Power	Domestic: 100 watts, 105-130 volts; 60 Hz
	Export: 100 watts; 105-130, 210-260 volts; 50 Hz
Temperature	Operating: 0° to 50°C
	Storage: −30° to 70°C
Humidity	0% to 95% non-condensing
Dimensions	13 inches high, 19 5/8 inches wide, 23 3/4 inches deep
Weight	35 pounds
Screen Size	12 inch diagonal
Display Size	8 1/2 inches wide, 6 inches high
Characters/Line	80
Lines	24
Line Spacing	0.45 character height
Character Format	5 x 7 dot matrix
Character Spacing	0.4 character width
Character Size	0.08 x 0.19 inch *nominal*
Character Repertoire	64 ASCII
Refresh Rate	Domestic: 60 times a second
	Export: 50/60 times a second
Cursor	Non-destructive blinking underscore
Transmit Data	Character by character as entered by the keyboard.

1.2 STANDARD INTERFACE

The Asynchronous Serial Interface is a multi-purpose serial data interface which provides maximum flexibility in operator switch selectable data rates, and operation modes that can be applied to allow operation under a wide variety of serial data input and output situations. A panel at the rear of the display contains switches and connectors that allow the operator to match both the standard EIA RS232C voltage interface and the Teletype* compatible 20/60 mA current loop interface for serial communications and computer interfaces.

**Registered Trade Mark of Teletype Corporation*

The operator selectable functions include the following:

1. Eleven Receive data rates – 75, 110, 150, 300, 600, 1200, 1800, 2400, 4800, 7200, and 9600 bits per second
2. An external TTL clock input
3. Full or Half Duplex
4. Ten or eleven bit code selection (one or two stop bits)
5. Odd, Even, or Mark Parity
6. 20 or 60 mA Teletype* compatible current loop interface
7. EIA RS232C interface - Interfaces to Bell system Type 103A, 103F, 202C, 202D modems or equivalents

*Registered Trade Mark of Teletype Corporation

APPENDIX B

READ-ONLY-MEMORY TRUTH TABLES

DCU Card, D20 Harris H PROM 1-8256-5B (32 x 8)

Address			B7	PA(Y) B6	LA(Y) B5	CP B4	CPA3 B3	CPA2 B2	CPA1 B1	CPA0 B0	
0	(32				H	H	H		H	H	0
1					H		H		H	H	1
2					H		H		H	H	2
3					H	H	H	H			3
4	(36)				H		H	H			4
5					H		H	H			5
6					H	H	H	H		H	6
7					H		H	H		H	7
8	(40)				H		H	H		H	8
9					H	H	H	H	H		9
10					H		H	H	H		10
11					H		H	H	H		11
12	(44)				H	H	H	H	H	H	12
13		X									13
14		X									14
15		X									15
16	(48)			H							16
17				H							17
18		X									18
19				H						H	19
20	(52)			H						H	20
21		X									21
22				H					H		22
23				H					H		23
24	(56)	X									24
25				H					H	H	25
26				H					H	H	26
27		X									27
28	(60)	X									28
29		X									29
30		X									30
31	(63)	X									31

H ≡ High ≡ Logic One ≡ Programmed
Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

DCU Card, C16 Harris H PROM 1-8256-5B (32 x 8)

Address		B7	PA(Y) B6	LA(Y) B5	CP B4	CPA3 B3	CPA2 B2	CPA1 B1	CPA0 B0	
0	X									0
1	X									1
2				H	H				H	2
3				H					H	3
4				H					H	4
5				H	H			H		5
6				H				H		6
7				H				H		7
8				H	H			H	H	8
9				H				H	H	9
10				H				H	H	10
11				H	H		H			11
12				H			H			12
13				H			H			13
14				H	H		H		H	14
15				H			H		H	15
16				H			H		H	16
17				H	H		H	H		17
18				H			H	H		18
19				H			H	H		19
20				H	H		H	H	H	20
21				H			H	H	H	21
22				H			H	H	H	22
23				H	H	H				23
24				H		H				24
25				H		H				25
26				H	H	H			H	26
27				H		H			H	27
28				H		H			H	28
29				H	H	H		H		29
30				H		H		H		30
31				H		H		H		31

H ≡ High ≡ Logic One ≡ Programmed
Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

SDF Card, B15 Signetics 82S123 (32 x 8)

Address		01111 B7	B6	B5	WL8P B4	WL1P B3	31BG B2	4BG B1	Sync. Code B0
PT 1	LSB 0				H				H
	1								H
	2			H					H
	MSB 3				H				H
PT 2	4				H				H
	5								
	6								
	7				H				H
PT 3	8				H				H
	9								
	10								H
	11				H				
PT 4	12				H	H			
	13								H
	14								
	15	H			H	H			
PT 5	16				H				
	17								
	18								H
	19				H				
PT 6	20				H				H
	21								
	22								H
	23				H				H
PT 7	24				H				H
	25								
	26								H
	27				H				H
PT 8	28				H			H	
	29							H	
	30			H				H	
	31				H		H	H	

H ≡ High ≡ Logic One ≡ Programmed

Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

Marked "K1" for KMR

Signetics 82S123

B15 on SDF

D30, B20 on DRU

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

PROM Pattern for D9 and D10 on MIU Cards. H PROM 1-1024-5B

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

	0.0000	16.0006	32.0012	48.0019
	0000.0000	0000.0110	1000.0100	1001.1001
	1.0000	17.0007	33.0013	49.0019
	0000.0000	0000.1110	1000.1100	1001.1001
	2.0001	18.0007	34.0013	50.0020
	0000.1000	0000.1110	1000.1100	0100.0000
	3.0001	19.0007	35.0014	51.0020
	0000.1000	0000.1110	1000.0010	0100.0000
	4.0002	20.0008	36.0014	52.0020
	0000.0100	0000.0001	1000.0010	0100.0000
Decimal Output	5.0002	21.0008	37.0014	53.0021
	0000.0100	0000.0001	1000.0010	0100.1000
Decimal PROM Address	6.0002	22.0009	38.0015	54.0021
	0000.0100	0000.1001	1000.1010	0100.1000
	7.0003	23.0009	39.0015	55.0021
	0000.1100	0000.1001	1000.1010	0100.1000
$O_3O_2O_1O_0$ Outputs of D10 PROM O=Low=Program	8.0003	24.0009	40.0016	56.0022
	0000.1100	0000.1001	1000.0110	0100.0100
	9.0004	25.0010	41.0016	57.0022
	0000.0010	1000.0000	1000.0110	0100.0100
$O_3O_2O_1O_0$ Outputs of D9 PROM O=Low=Program	10.0004	26.0010	42.0016	58.0023
	0000.0010	1000.0000	1000.0110	0100.1100
	11.0004	27.0011	43.0017	59.0023
	0000.0010	1000.1000	1000.1110	0100.1100
	12.0005	28.0011	44.0017	60.0023
	0000.1010	1000.1000	1000.1110	0100.1100
	13.0005	29.0011	45.0018	61.0024
	0000.1010	1000.1000	1000.0001	0100.0010
	14.0005	30.0012	46.0018	62.0024
	0000.1010	1000.0100	1000.0001	0100.0010
	15.0006	31.0012	47.0018	63.0025
	0000.0110	1000.0100	1000.0001	0100.1010

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

64.0025	80.0031	96.0037	112.0044
0100.1010	1100.1000	1100.1110	0010.0010
65.0025	81.0032	97.0038	113.0044
0100.1010	1100.0100	1100.0001	0010.0010
66.0026	82.0032	98.0038	114.0045
0100.0110	1100.0100	1100.0001	0010.1010
67.0026	83.0032	99.0039	115.0045
0100.0110	1100.0100	1100.1001	0010.1010
68.0027	84.0033	100.0039	116.0045
0100.1110	1100.1100	1100.1001	0010.1010
69.0027	85.0033	101.0039	117.0046
0100.1110	1100.1100	1100.1001	0010.0110
70.0027	86.0034	102.0040	118.0046
0100.1110	1100.0010	0010.0000	0010.0110
71.0028	87.0034	103.0040	119.0046
0100.0001	1100.0010	0010.0000	0010.0110
72.0028	88.0034	104.0041	120.0047
0100.0001	1100.0010	0010.1000	0010.1110
73.0029	89.0035	105.0041	121.0047
0100.1001	1100.1010	0010.1000	0010.1110
74.0029	90.0035	106.0041	122.0048
0100.1001	1100.1010	0010.1000	0010.0001
75.0029	91.0036	107.0042	123.0048
0100.1001	1100.0110	0010.0100	0010.0001
76.0030	92.0036	108.0042	124.0048
1100.0000	1100.0110	0010.0100	0010.0001
77.0030	93.0036	109.0043	125.0049
1100.0000	1100.0110	0010.1100	0010.1001
78.0030	94.0037	110.0043	126.0049
1100.0000	1100.1110	0010.1100	0010.1001
79.0031	95.0037	111.0043	127.0050
1100.1000	1100.1110	0010.1100	1010.0000

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

128.0056 1010.0000	144.0056 1010.0110	160.0062 0110.0100	176.0069 0110.1001
129.0050 1010.0000	145.0057 1010.1110	161.0063 0110.1100	177.0069 0110.1001
130.0051 1010.1000	146.0057 1010.1110	162.0063 0110.1100	178.0070 1110.0000
131.0051 1010.1000	147.0057 1010.1110	163.0064 0110.0010	179.0070 1110.0000
132.0052 1010.0100	148.0058 1010.0001	164.0064 0110.0010	180.0070 1110.0000
133.0052 1010.0100	149.0058 1010.0001	165.0064 0110.0010	181.0071 1110.1000
134.0052 1010.0100	150.0059 1010.1001	166.0065 0110.1010	182.0071 1110.1000
135.0053 1010.1100	151.0059 1010.1001	167.0065 0110.1010	183.0071 1110.1000
136.0053 1010.1100	152.0059 1010.1001	168.0066 0110.0110	184.0072 1110.0100
137.0054 1010.0010	153.0060 0110.0000	169.0066 0110.0110	185.0072 1110.0100
138.0054 1010.0010	154.0060 0110.0000	170.0066 0110.0110	186.0073 1110.1100
139.0054 1010.0010	155.0061 0110.1000	171.0067 0110.1110	187.0073 1110.1100
140.0055 1010.1010	156.0061 0110.1000	172.0067 0110.1110	188.0073 1110.1100
141.0055 1010.1010	157.0061 0110.1000	173.0068 0110.0001	189.0074 1110.0010
142.0055 1010.1010	158.0062 0110.0100	174.0068 0110.0001	190.0074 1110.0010
143.0056 1010.0110	159.0062 0110.0100	175.0068 0110.0001	191.0075 1110.1010

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

[illegible]	208.0081	[illegible]	[illegible]
1110.1010	0001.1000	0001.1110	1001.0010
193.0075	209.0082	225.0088	241.0094
1110.1010	0001.0100	0001.0001	1001.0010
194.0076	210.0082	226.0088	242.0095
1110.0110	0001.0100	0001.0001	1001.1010
195.0076	211.0082	227.0089	243.0095
1110.0110	0001.0100	0001.1001	1001.1010
196.0077	212.0083	228.0089	244.0095
1110.1110	0001.1100	0001.1001	1001.1010
197.0077	213.0083	229.0089	245.0096
1110.1110	0001.1100	0001.1001	1001.0110
198.0077	214.0084	230.0090	246.0096
1110.1110	0001.0010	1001.0000	1001.0110
199.0078	215.0084	231.0090	247.0096
1110.0001	0001.0010	1001.0000	1001.0110
200.0078	216.0084	232.0091	248.0097
1110.0001	0001.0010	1001.1000	1001.1110
201.0079	217.0085	233.0091	249.0097
1110.1001	0001.1010	1001.1000	1001.1110
202.0079	218.0085	234.0091	250.0098
1110.1001	0001.1010	1001.1000	1001.0001
203.0079	219.0086	235.0092	251.0098
1110.1001	0001.0110	1001.0100	1001.0001
204.0080	220.0086	236.0092	252.0098
0001.0000	0001.0110	1001.0100	1001.0001
205.0080	221.0086	237.0093	253.0099
0001.0000	0001.0110	1001.1100	1001.1001
206.0080	222.0087	238.0093	254.0099
0001.0000	0001.1110	1001.1100	1001.1001
207.0081	223.0087	239.0093	255.0100
0001.1000	0001.1110	1001.1100	0101.0000

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

Coordinate Converter Altitude Error Correction (Card 2)

	F30				F26 LSB			
Input Address	D	C	B	A	Q	R	S	T
0-27	0	0	0	0	0	0	0	0
28-38	0	0	0	0	0	0	0	1
39-47	0	0	0	0	0	0	1	0
48-55	0	0	0	0	0	0	1	1
56-62	0	0	0	0	0	1	0	0
63-68	0	0	0	0	0	1	0	1
68-74	0	0	0	0	0	1	1	0
75-79	0	0	0	0	0	1	1	1
80	0	0	0	0	1	0	0	0
81	0	0	0	0	1	0	0	0
82	0	0	0	0	1	0	0	0
83	0	0	0	0	1	0	0	0
84	0	0	0	0	1	0	0	1
85	0	0	0	0	1	0	0	1
86	0	0	0	0	1	0	0	1
87	0	0	0	0	1	0	0	1
88	0	0	0	0	1	0	0	1
89	0	0	0	0	1	0	1	0
90	0	0	0	0	1	0	1	0
91	0	0	0	0	1	0	1	0
92	0	0	0	0	1	0	1	0
93	0	0	0	0	1	0	1	1
94	0	0	0	0	1	0	1	1
95	0	0	0	0	1	0	1	1
96	0	0	0	0	1	0	1	1
97	0	0	0	0	1	0	1	1
98	0	0	0	0	1	1	0	0
99	0	0	0	0	1	1	0	0
100	0	0	0	0	1	1	0	0
101	0	0	0	0	1	1	0	1
102	0	0	0	0	1	1	0	1

Coordinate Converter Altitude Error Correction (Card 2) (Cont)

Input Address	F30 D	C	B	A	F26 LSB Q	R	S	T
103	0	0	0	0	1	1	0	1
104	0	0	0	0	1	1	0	1
105	0	0	0	0	1	1	1	0
106	0	0	0	0	1	1	1	0
107	0	0	0	0	1	1	1	0
108	0	0	0	0	1	1	1	1
109	0	0	0	0	1	1	1	1
110	0	0	0	0	1	1	1	1
111	0	0	0	0	1	1	1	1
112	0	0	0	1	0	0	0	0
113	0	0	0	1	0	0	0	0
114	0	0	0	1	0	0	0	0
115	0	0	0	1	0	0	0	0
116	0	0	0	1	0	0	0	1
117	0	0	0	1	0	0	0	1
118	0	0	0	1	0	0	0	1
119	0	0	0	1	0	0	1	0
120	0	0	0	1	0	0	1	0
121	0	0	0	1	0	0	1	0
122	0	0	0	1	0	0	1	1
123	0	0	0	1	0	0	1	1
124	0	0	0	1	0	0	1	1
125	0	0	0	1	0	1	0	0
126	0	0	0	1	0	1	0	0
127	0	0	0	1	0	1	0	0
128	0	0	0	1	0	1	0	1
129	0	0	0	1	0	1	0	1
130	0	0	0	1	0	1	0	1
131	0	0	0	1	0	1	0	1
132	0	0	0	1	0	1	1	0
133	0	0	0	1	0	1	1	0

Coordinate Converter Altitude Error Correction (Card 2) (Cont)

Input Address	F30 D	C	B	A	F26 LSB Q	R	S	T
134	0	0	0	1	0	1	1	0
135	0	0	0	1	0	1	1	1
136	0	0	0	1	0	1	1	1
137	0	0	0	1	1	0	0	0
138	0	0	0	1	1	0	0	0
139	0	0	0	1	1	0	0	0
140	0	0	0	1	1	0	0	1
141	0	0	0	1	1	0	0	1
142	0	0	0	1	1	0	1	0
143	0	0	0	1	1	0	1	0
144	0	0	0	1	1	0	1	0
145	0	0	0	1	1	0	1	1
146	0	0	0	1	1	0	1	1
147	0	0	0	1	1	0	1	1
148	0	0	0	1	1	1	0	0
149	0	0	0	1	1	1	0	0
150	0	0	0	1	1	1	0	1
151	0	0	0	1	1	1	0	1
152	0	0	0	1	1	1	0	1
153	0	0	0	1	1	1	1	0
154	0	0	0	1	1	1	1	0
155	0	0	0	1	1	1	1	0
156	0	0	0	1	1	1	1	1
157	0	0	0	1	0	0	0	0
158	0	0	1	0	0	0	0	0
159	0	0	1	0	0	0	0	0
160	0	0	1	0	0	0	0	0
161	0	0	1	0	0	0	0	1
162	0	0	1	0	0	0	0	1
163	0	0	1	0	0	0	1	0

Coordinate Converter Altitude Error Correction (Card 2) (Cont)

	F30				F26 LSB			
Input Address	D	C	B	A	Q	R	S	T
164	0	0	1	0	0	0	1	0
165	0	0	1	0	0	0	1	0
166	0	0	1	0	0	0	1	1
167	0	0	1	0	0	0	1	1
168	0	0	1	0	0	1	0	0
169	0	0	1	0	0	1	0	0
170	0	0	1	0	0	1	0	1
171	0	0	1	0	0	1	0	1
172	0	0	1	0	0	1	0	1
173	0	0	1	0	0	1	1	0
174	0	0	1	0	0	1	1	0
175	0	0	1	0	0	1	1	1
176	0	0	1	0	0	1	1	1
177	0	0	1	0	1	0	0	0
178	0	0	1	0	1	0	0	0
179	0	0	1	0	1	0	0	1
180	0	0	1	0	1	0	0	1
181	0	0	1	0	1	0	1	0
182	0	0	1	0	1	0	1	0
183	0	0	1	0	1	0	1	0
184	0	0	1	0	1	0	1	1
185	0	0	1	0	1	0	1	1
186	0	0	1	0	1	1	0	0
187	0	0	1	0	1	1	0	0
188	0	0	1	0	1	1	0	1
189	0	0	1	0	1	1	0	1
190	0	0	1	0	1	1	1	0
191	0	0	1	0	1	1	1	0
192	0	0	1	0	1	1	1	1
193	0	0	1	0	1	1	1	1
194	0	0	1	1	0	0	0	0

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

Coordinate Converter Altitude Error Correction (Card 2) (Cont)

Input Address	F30 D	C	B	A	F26 LSB Q	R	S	T
195	0	0	1	1	0	0	0	0
196	0	0	1	1	0	0	0	1
197	0	0	1	1	0	0	0	1
198	0	0	1	1	0	0	1	0
199	0	0	1	1	0	0	1	0
200	0	0	1	1	0	0	1	1
201	0	0	1	1	0	0	1	1
202	0	0	1	1	0	1	0	0
203	0	0	1	1	0	1	0	0
204	0	0	1	1	0	1	0	1
205	0	0	1	1	0	1	0	1
206	0	0	1	1	0	1	1	0
207	0	0	1	1	0	1	1	0
208	0	0	1	1	0	1	1	1
209	0	0	1	1	0	1	1	1
210	0	0	1	1	1	0	0	0
211	0	0	1	1	1	0	0	0
212	0	0	1	1	1	0	0	1
213	0	0	1	1	1	0	1	0
214	0	0	1	1	1	0	1	0
215	0	0	1	1	1	0	1	1
216	0	0	1	1	1	0	1	1
217	0	0	1	1	1	1	0	0
218	0	0	1	1	1	1	0	0
219	0	0	1	1	1	1	0	1
220	0	0	1	1	1	1	0	1
221	0	0	1	1	1	1	1	0
222	0	0	1	1	1	1	1	1
223	0	0	1	1	1	1	1	1

AD-A056 572 RAYTHEON CO WAYLAND MASS EQUIPMENT DIV F/G 17/9
SCAN CONVERTER AND REFRESH MEMORY WITH REMOTE TERMINAL.(U)
JAN 76 J H TURNER F19628-75-C-0156
UNCLASSIFIED ER76-4065 AFGL-TR-76-0175 NL

2 OF 2
AD
A056572



END
DATE
FILMED
8-78
DDC

Coordinate Converter Altitude Error Correction (Card 2) (Cont)

Input Address	F30 D	C	B	A	F26 LSB Q	R	S	T
224	0	1	0	0	0	0	0	0
225	0	1	0	0	0	0	0	1
226	0	1	0	0	0	0	0	1
227	0	1	0	0	0	0	1	0
228	0	1	0	0	0	0	1	0
229	0	1	0	0	0	0	1	1
230	0	1	0	0	0	0	1	1
231	0	1	0	0	0	1	0	0
232	0	1	0	0	0	1	0	0
233	0	1	0	0	0	1	0	1
234	0	1	0	0	0	1	0	1
235	0	1	0	0	0	1	1	0
236	0	1	0	0	0	1	1	0
237	0	1	0	0	0	1	1	1
238	0	1	0	0	1	0	0	0
239	0	1	0	0	1	0	0	1
240	0	1	0	0	1	0	0	1
241	0	1	0	0	1	0	1	0
242	0	1	0	0	1	0	1	0
243	0	1	0	0	1	0	1	1
244	0	1	0	0	1	1	0	0
245	0	1	0	0	1	1	0	0
246	0	1	0	0	1	1	0	1
247	0	1	0	0	1	1	1	0
248	0	1	0	0	1	1	1	0
249	0	1	0	0	1	1	1	1
250	0	1	0	1	0	0	0	0
251	0	1	0	1	0	0	0	0

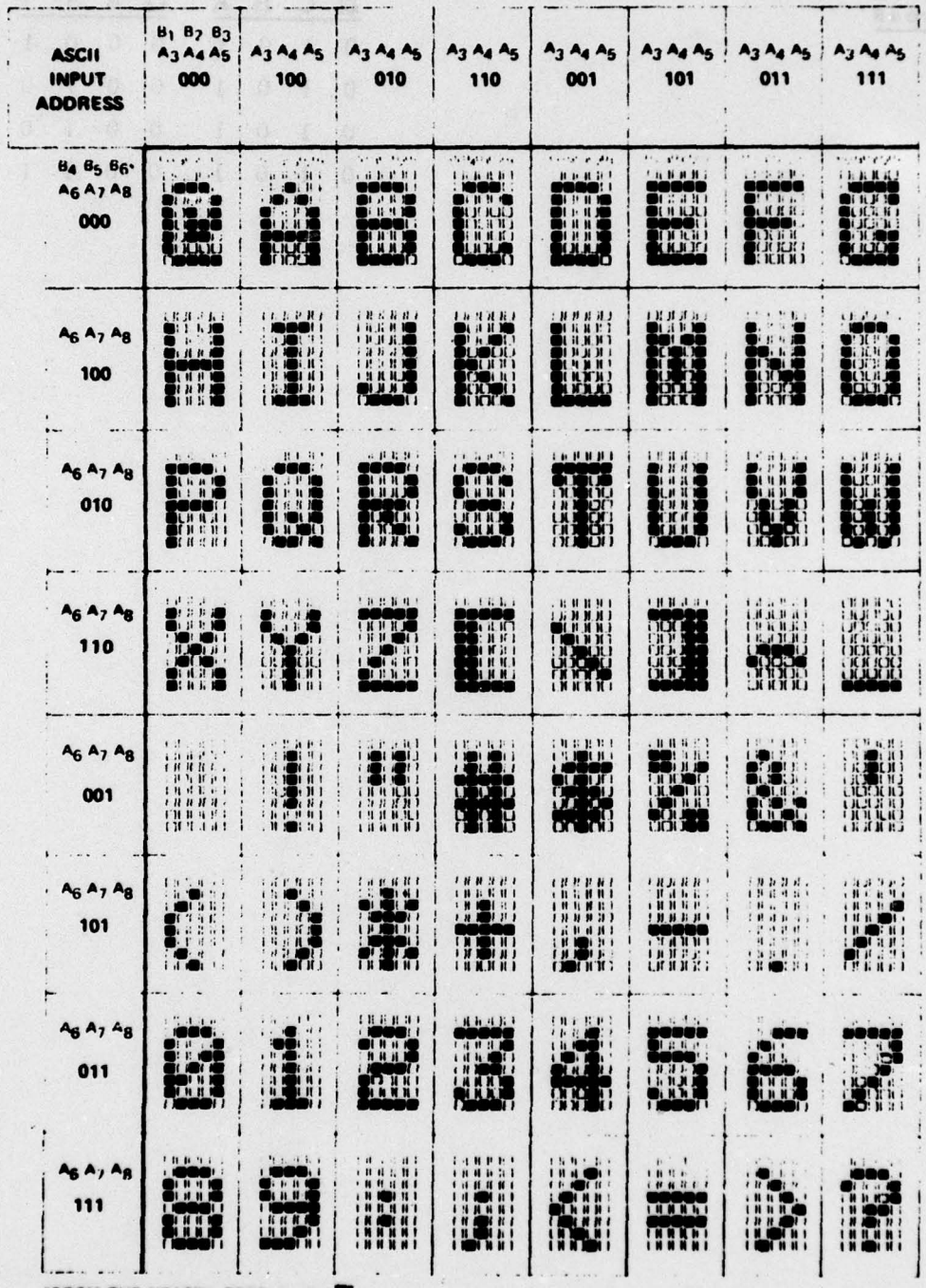
Coordinate Converter Altitude Error Correction (Card 2) (Cont)

Input Address	F30 D	C	B	A	F26 Q	R	S	T (LSB)
252	0	1	0	1	0	0	0	1
253	0	1	0	1	0	0	1	0
254	0	1	0	1	0	0	1	0
255	0	1	0	1	0	0	1	1

5 X 7 CHARACTER FONT*

MM8055

A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT



*FROM THE USASCII CODE A_8 B_7 $\overline{B_6}$

APPENDIX C

MEMORANDA

"Scan Converter Drawing List", (A.J. Jagodnik memo #AJJ-26)

RAYTHEON

FM 10-0557 (9-65) BOND

DIVISION	EQUIPMENT	Classification	Unclassified
Operation	EDL - Wayland	Contract No.	
Department	Advanced Development Laboratory	Distribution	Listed
To	J. H. Turner, Jr.	File No.	
From	A. J. Jagodnik, Jr.	Memo No.	AJJ-26
Subject	Scan Converter Drawing List	Date	4 June 1975

The fact that two slightly different scan converter refresh memory systems have been built and that both have been extensively modified in different ways has led to some confusion in the area of the applicability of drawings. The Table contained herein is intended to resolve the confusion. It contains all drawings related to the scan converters, ordered by Raytheon drawing number, and indicates the equipment to which each is applicable. Also included is information describing the size, type and form of each drawing and whether or not it references other drawings.

A. J. Jagodnik
Advanced Electronic Techniques
Wayland, Box M9, Ext. 2736

/bp

cc: G. Dennis
K. M. Glover (3)
D. L. Keefe
J. C. Murray
L. R. Novick
J. C. Westphal

SCRM DRAWINGS

Type: S - Schematic, I - Interconnection Diagram, M - Mechanical, B - Block Diag.
Form: V - Vellum, M - Mylar, S - Sepia

Dwg No.	Size	Type	Form	Abbrev. Title (Notes)		Other Dwg Ref:	Application: S/N 2 Before LWCA	S/N 1 Before KMR	LWCA (2)	KMR Master	KMR Remote
895180	B	M	V	Mtg. Brkt. Interface	(MIU Shelf)		X	X	X	X	X
895181	D	S	V	C. C. X Hatch Gen	3C		X	X	X	X	
895182	D	S	V	Test Card							
895183	D	S	V	C. C. Origin Trans. BCD/BW	3F		X	X	X	X	
895184	D	S	V	C. C. X Proj. Accum	3E		X	X	X	X	
895185	D	S	S	C. C. Hi Alt Acc	2C		X	X	X	X	
895186	D	S	S	C. C. Lo Alt Acc	2D		X	X	X	X	
SD895187	D	S	S	AIU			X	X	X	X	
895188	D	S	V	C. C. Y Proj. Accum	3D		X	X	X	X	
895189	D	M	V	Hole Layout, Rear Pnl Interface	#1 (Lower SCP)		X	X	X	3 BNC's Added	
895190	D	M	V	" " " " "	#2 (Upper SCP)		X	no J3 & J4 holes	X	no J3 & J4 holes	
895191	D	M	V	" " " " "	#3 (MIU)		X	X	X	X	X
895192	D	S	S	C. C. T. F. Earth Alt. Acc.	2E		X	X	X	X	
895193	D	S	S	C. C. R. Proj. Accum	2F		X	X	X	X	
SD895194	D	S	V	VDU			X	X	X	X	
895195	D	S	S	C. C. Alt 12 x 12 Mult.	1F		X	X	X	X	
895196	D	S	V	C. C. Range 12 x 12 Mult.	1E		X	X	X	X	
895197	E	B	V	C. C. Block Diag.			X	X	X	X	
895198	E	S	V	C. C. X 12 x 12 Mult.	1A & B		X	X	X	X	
895199	E	S	S	C. C. Y 12 x 12 Mult.	1C & D		X	X	X	X	
SD895200	E	S	S	MIU (2 sht)			X	X			(1)
SD895201	E	S	1-V 2-M	DCU (2 sht)			X	X			
895202	E	S	V	C. C. Alt Compar.	2A & B		X	X	X	X	
895203	E	S	V	C. C. Interface	3A, B&C		X	X	X	X	
895204	E	M	S	S. C. Front Panel, Hole Layout			X	X	X	X	
895205	E	M	V	S. C. Silk Screen Layout			X	X	X	X	
895718	J	I	S	Int. Diag-KMR CC		X				X	
895720	E	S	S	KMR Master SCRM F & R Panels		X				X	
895726	C	I	S	KMR Master SCRM Power Supplies						X	
897392	E	I	V	C. C. Interconnect		X	X	X	X		
897393	C	I	1-V 2-S	Scan Conv. Interconnect		X	sht 2	sht 1			
897896	B	I	V	MEM to MIU			X	X	X	X	X
897897	C	I	V	DCU & VDU to MIU (Cables)			X	X	X	X	X
897898	E	S	V	S. C. Proc. F & R Panels		X	X	X	X		
897899	E	I	V	DCU to VDU		X	X	X	X		
897900	C	I	V	S. C. Proc. DC Power Supplies			X	X	X		

SCRM DRAWINGS (Continued)

Dwg No.	Size	Type	Form	Abbrev. Title (Notes)	Other Dwg Ref:	Application: S/N 2 Before LWCA	S/N 1 Before KMR	LWCA (2)	KMR: Master	KMR: Remote
897918	B	S	V	Term for Twp Lines		X	X	X	X	X
910161	D	M	V	Hole Layout F Panel				X		
910162	D	M	S	Silk Screen F Panel				X		
910163	C	M	V	Bracket for Conn.				X		
910166	D	S	V	LWCA Control Panel				X		
910167	C	S	V	Cable Wiring LWCA Cont. Panel to DDI				X		
910168	E	S	S	DCU (2 sht)				X		
910169	J	S	S	MIU (Sections C-F; Geo. has mylar from which this was made)	X			X		(1)
910170	C	S	V	Mon. No. 5 input sel.		X		X		
910171	E	S	V	Color Encoder (MIU Same as SD895200 sht 2)				X	X	(1)
910172	C	I	V	Cable - DCU to Card 2				X		
910173	D	I	S	Cable - DDI to ULI				X		
910174	D	I	V	Cable - DDI to DCU				X		
910175	E	S	M	DDI				X		
910176	D	I	V	LWCA Scan Conv.	X			X		
911046	C	S	V	Data Trans Control Panel & Cable					X	
911047	D	S	M	SDF					X	
911048	E	S	M	DRU						X
911049	D	I	M	Remote Refresh Memory	X					X
911050	D	I	V	Cables - KMR Master	X				X	
911101	C	I	S	KMR Master SCRM	X				X	
911102	E	S	S	KMR DCU (Sht 2 same as SD895201 sht 2)					X	
911103	E	I	S	KMR DCU to VDU	X				X	
911104	J	S	S	Master KMR MIU (C-F; Geo. has mylar from which this was made)	X				X	(1)
911155	B	I	V	Remote MIU Video Jumper						X
911156	D	I	V	RRM F & R Panels						X
911157	D	M	V	Silk Screen - F. Panel Data Trans. Cntrl					X	
911158	D	M	V	Silk Screen RRMR						X
911159	D	M	S	Hole Ly F Panel RRMR						X
911160	D	M	S	Hole Ly F Panel Data Trans Cntrl					X	

(1) See 911049

(2) All LWCA drawings are not listed here; only those related to the SCRM.

Unclassified
AJJ-26
4 June 1975
Page 3 of 3