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A STRUCTURED DESIGN AUTOMATION ENVIRONMENT FOR DIGITAL SYSTEMS

W. M. vanCleemput

Technical Note No. 134

December 1977

Digital Systems Laboratory
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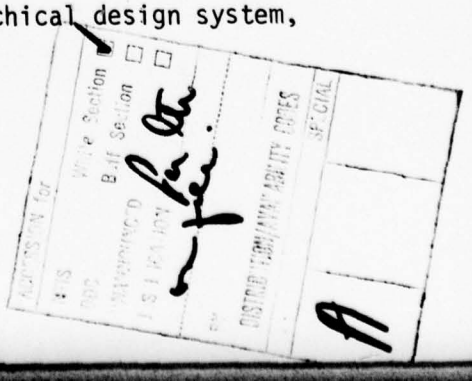
ABSTRACT

This paper describes a design automation system for digital systems that promotes a structured design approach both in logic design phase and in the physical implementation phase.

INDEX TERMS: design automation system, hierarchical design system, structured design



1. MOTIVATION

Due to explosive developments in semiconductor technology the number of equivalent logic gates that can be realized on a single chip has been rising constantly. In the near future integrated circuits containing 10,000 gates will be feasible while 50 to 100,000 gates per integrated circuit are predicted within the next decade.

As a consequence, the number of gates in a large-scale digital system has kept growing. It is quite likely that this tendency will continue for some time.

Unfortunately, the human designer has a limit in terms of what he can concentrate on at any one time. A block diagram or schematic with between ten and fifty functional blocks on it is usually quite comprehensible by a human being, while a schematic with, e.g., 1,000 logic gates on it, without any blocks of this logic being functionally designated, is most likely to be completely incomprehensible.

For this reason, the human designer often performs his design task in a hierarchical fashion. In terms of digital systems design the logic design phase is most frequently done in a top-down fashion, while the physical design phase (layout) is done in a bottom-up approach. It must be emphasized, though, that both logic design and physical design occur by combination of bottom-up and top-down approaches; this combination being very dependent on the individual performing the design task.

Very often design automation tools have imposed certain levels of abstraction within this hierarchical design process. Gate-level logic simulation and register-transfer-level design languages and simulators are an example of such predefined levels. The major problem in predefining the levels of abstraction at which a designer should perform his task is the inability to cope with technological changes. For this reason, very few of today's design automation systems can cope with microprocessors and with other LSI devices of similar complexity.

A design is characterized by two very important properties: its (intended)

behavior and its structure. In the initial phases of the design process, the behavior of a system is the most important information item about this design. However, the further a design proceeds and the more a designer defines his design, the more structural information will be added to the design information. Quite frequently structural information or limitations are a part of the initial design specification. Nevertheless, very few design automation systems have the ability to capture this type of information and to make use of it in the early stages of the design process. Software packages such as gate-level logic simulators, fault simulators, test generation programs, PC layout packages and IC layout systems all rely to a large extent on some detailed structural information about the system. However, the transformation of the initial design into this physical structure is done mainly in the designer's mind without the help of design automation programs to verify this transformation.

Whereas in the past it was feasible to look at the ultimate physical realization of a system and to perform a gate-level simulation on this design, the growing number of gates in current systems makes such an approach less and less desirable. Therefore, it has become necessary for a designer to be able to simulate his design at various levels of abstraction. In order not to loose the influence of the global system on a particular part of the system, it may be desirable to simulate a small part of the design at the gate-level while the rest of the system is simulated at a much higher level of abstraction.

A final point that motivated the development described in this paper is the fact that a large number of design automation programs currently exist although most of them are not compatible. The system described here tries to interface in a reasonable fashion to as many design packages as feasible.

2. OVERALL SYSTEM STRUCTURE

Figure 1 gives an overview of the structure of the design automation system. It should be noted that structural information is the dominant kind

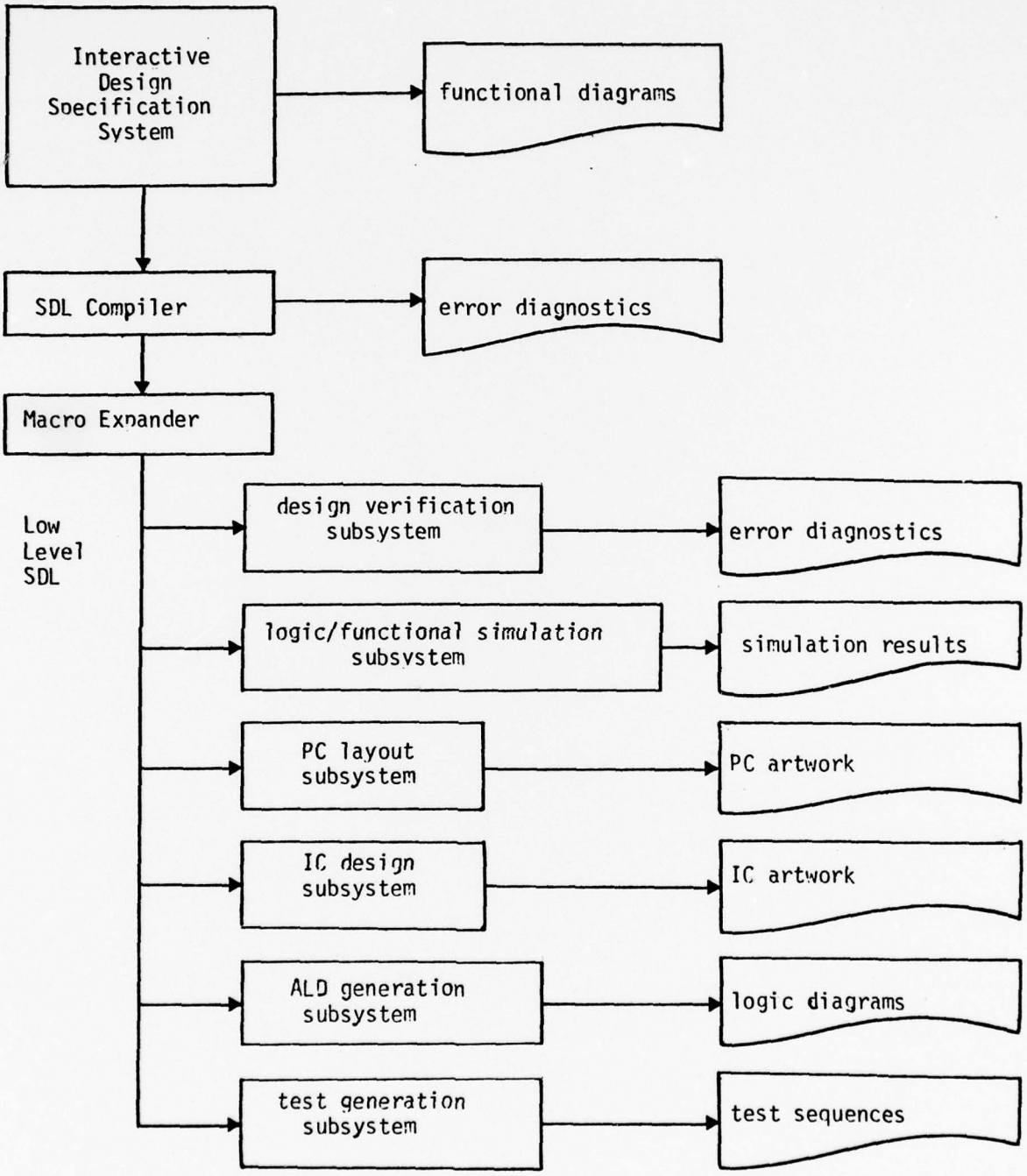


Figure 1: Overall design automation system structure

of information in this system. Behavioral information is considered as an attribute to a structural block.

In order for a designer to capture information in an interactive graphics environment, an interactive design specification subsystem [9] is available. Using this system the designer defines the structure of a system in an interactive fashion by making use of an interactive graphics terminal. The output of the design specification system is a one-dimensional structural description language called SDL [1]. This SDL description can then be compiled into an intermediate language form. The designer can make use of a hardware macro-expansion facility which will allow him to quickly expand his design to whatever level of abstraction is needed in order to perform a given task. The design process will be explained further in the next sections.

Design verification will be performed even in the initial stages of the design process. This will require a designer to provide a behavioral description for every type of block used at every level of abstraction. The types of verification currently being considered are:

1. To verify the behavior of a system at a given level against the behavior of the same system made up of components at the lower level for which a behavioral description is available.
2. To verify the consistency between the behavioral description and the structural description, e.g., when the behavioral description calls for the existence of a data path, such existence can be verified by checking the structural description.
3. To verify a design as given at one level against the expanded version of the same design at the lower level.

A number of subsystems for physical design will be implemented. These include the following: logic (gate-level) simulation, functional (register-transfer-level) simulation, PC layout, IC layout, automated logic diagram generation, and fault test generation. Each of these subsystems currently

is planned to have its own component library. Ideally, a common data base should be established. This can, however, be rather difficult if one has to modify existing software systems. These data base aspects will be further discussed in section 6.

3. LOGIC DESIGN STRATEGY

In this section we will discuss how a user would use the system in order to perform system design. A simple example is given in Figure 2, where an ALU/SHIFTER combination is defined. At the highest level of abstraction the designer would make use of the interactive design specification subsystem to draw a schematic for the highest level of the example, as shown in Figure 2a. The next step for the designer would be to specify for each type of functional block used at the highest level, a realization in terms of lower level components. For instance, for the register one could specify a realization in terms of flipflops (Figure 2b). At the next level, the fliflop is specified in terms of gates (Figure 2c), and finally, at the lowest level, for each of the gate-types one can specify its realization in terms of transistors (Figure 2d). By making use of the macroexpansion facility, the designer is able to describe his circuit at the register level, at the flipflop level, at the gate level and at the transistor level. By doing a macroexpansion to the proper level the designer can perform functional simulation at the register level, logic simulation at the gate level or circuit simulation at the transistor level.

4. DESIGN VERIFICATION

As was already mentioned in the previous section, the designer can perform a macroexpansion of his design to a lower level and then perform a simulation at that level in order to verify his design. For instance, by expanding the design down to the gate level, a gate-level logic simulation can be performed. By expanding one more level, down to the transistor level, a circuit analysis could be run in order to verify the correctness of the design. Similarly, at the original level in this example one could perform a

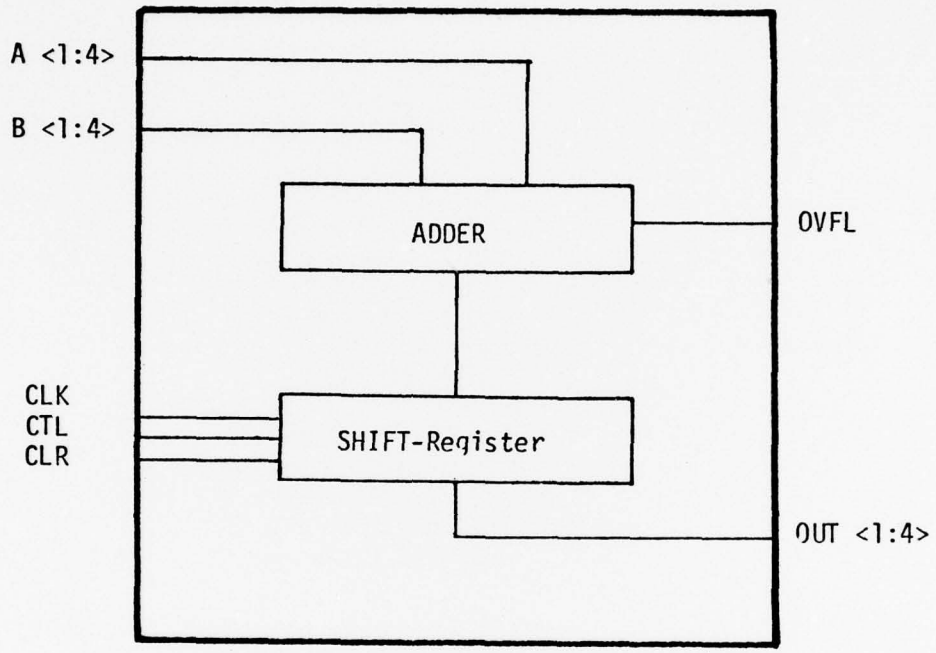


Figure 2a: 4-bit adder/shifter combination

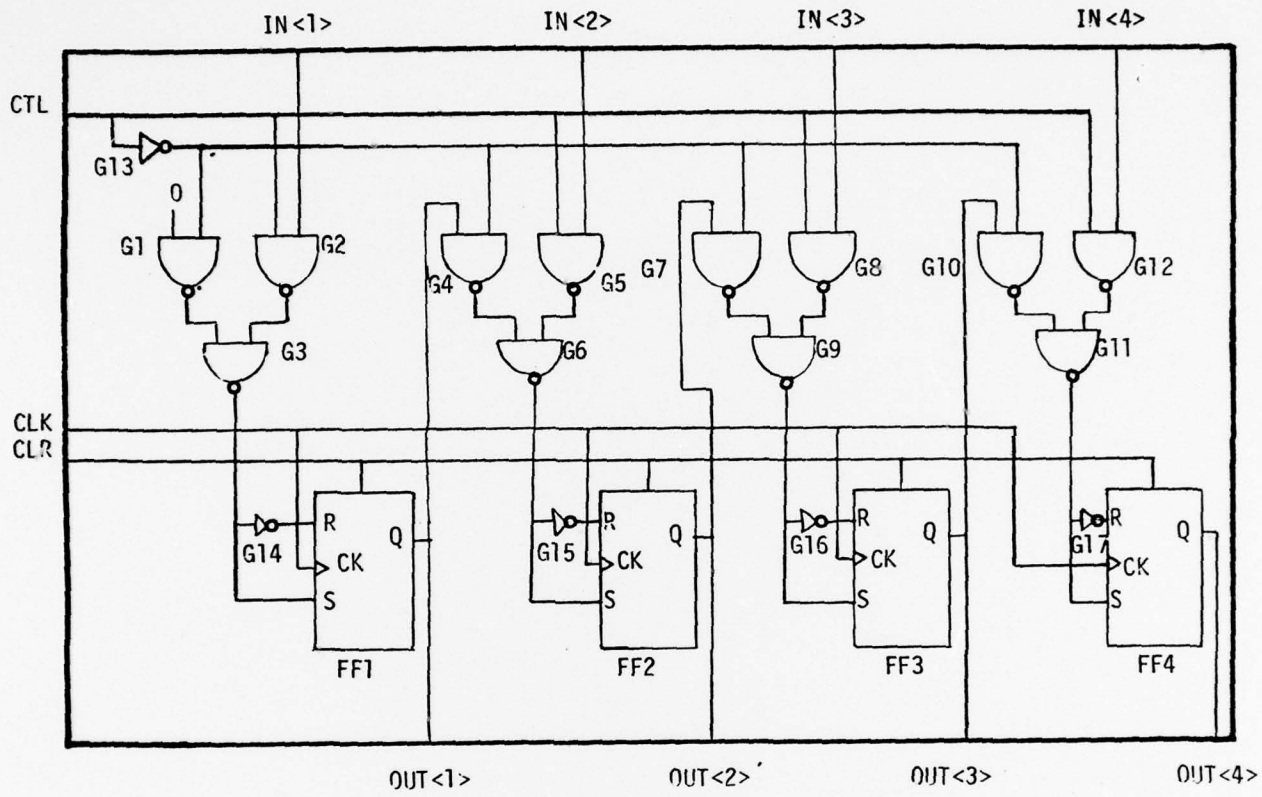


Figure 2b: 4-bit parallel input/parallel output shifter

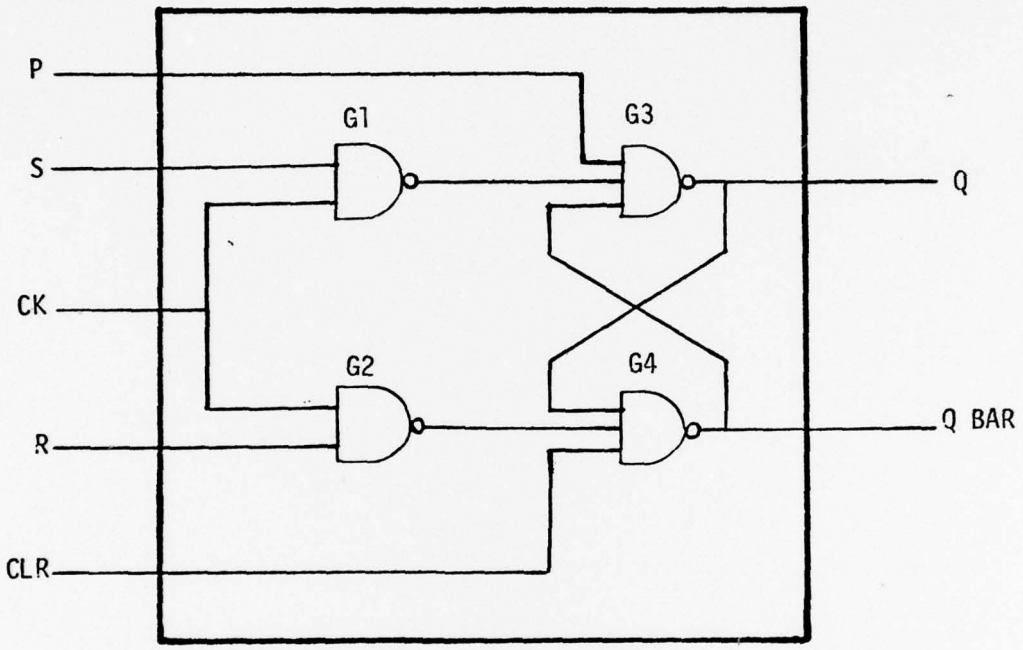


Figure 2c: Flip-flop implementation
using NAND gates

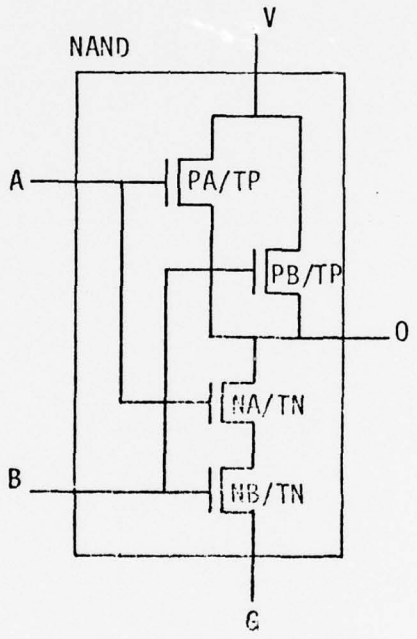


Figure 2d: CMOS implementation of
a 2-input NAND gate

register-transfer level simulation.

In a large-scale system, the emphasis at the architectural level, would be on behavioral simulation to verify performance of the system, to identify potential bottlenecks in the system, etc.

A second type of design verification that can be performed is to check the consistency of the structural information of a design at a given level (e.g., the register-transfer level) with the associated behavioral description.

A third form of design verification consists of describing the behavior of the system at a given level and also to specify the behavior of all component types used at the next lower level and then to try to prove the equivalence of both descriptions.

Finally, one may want to cross the boundaries established by the levels of abstraction by doing multi-level simulation, where a small part of the system is simulated at very great detail while the remainder of the system is simulated at a much higher level. The potential benefit of such a scheme is that one would have a clear picture of the behavior of the small part without sacrificing the influence the total system has on this part.

A register-transfer language based on DDL [10] is currently being implemented. The difference between this new implementation and most other computer design languages is that both at compile time and during the simulation, the consistency of the behavioral description is verified against the structural description.

Along the same lines, a multi-level hierarchical simulation facility based on SIMULA [11] is in the initial stages of development.

5. PHYSICAL IMPLEMENTATION SUBSYSTEM

A number of physical design subsystems are being developed. An example of a system that is currently operational is the PC design system, the structure of which is illustrated in Figure 3 [2,5]. This system supports

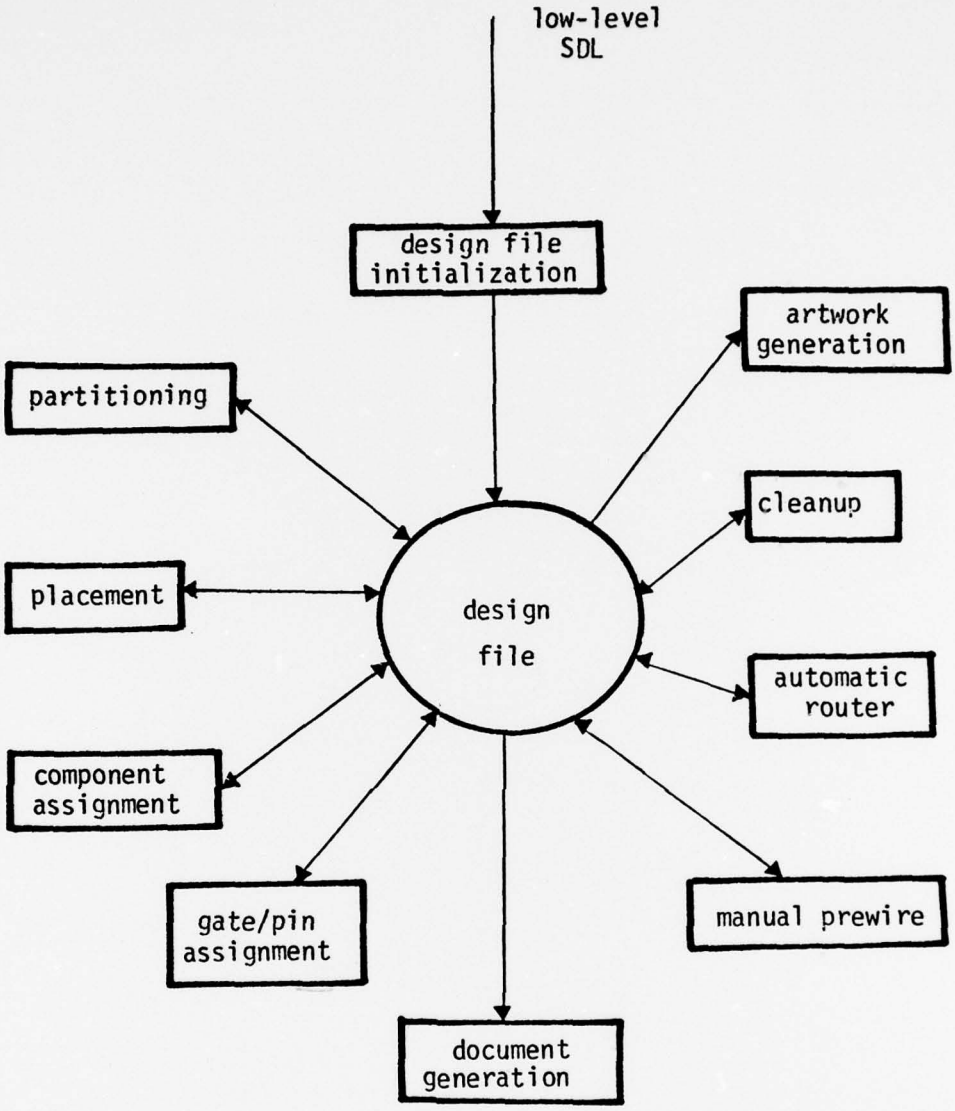


Figure 3: PC design subsystem structure

the design of two-layer boards. An extension to designing multi-layer boards is being implemented. The printed circuit board design system consists of a collection of programs to perform certain functions related to PC design. All these programs work on a common design file which contains the status of a design at any point in time.

Similarly, a subsystem for automated logic diagram generation is available. This system is based on the work reported in [3]. Within the current framework of the hierarchical system there is no longer a need for manually generating detailed logic diagrams since the hierarchical diagrams produced by the interactive design specification system provide an adequate functional specification of the system. However, for the maintenance of a system, it is necessary to have logic diagrams that reflect the physical implementation. For that reason it was decided to make use of an automated system for generating logic diagrams.

Another subsystem which is currently in its initial implementation phase is a subsystem for the layout and design of integrated circuits [4]. The structure of this system is depicted in Figure 4. Again, as in the printed circuit board design system, this subsystem is centralized around a design file that contains the status of the design. An interesting characteristic of this IC design system is the fact that it contains all the structural information provided by a designer using the design specification system. Such information provides a functional partitioning and the IC layout system will try to make as much use as possible of this type of information.

Interfaces have been written which allow a designer to perform test generation and gate-level logic simulation using the Hewlett-Packard TESTAID system [6]. Furthermore, an interface to a circuit analysis program, SPICE [7], will be implemented, thereby allowing the designer to verify a circuit at the circuit level. In a similar fashion an interface to a MOS timing simulator, MOTIS [8] will be provided.

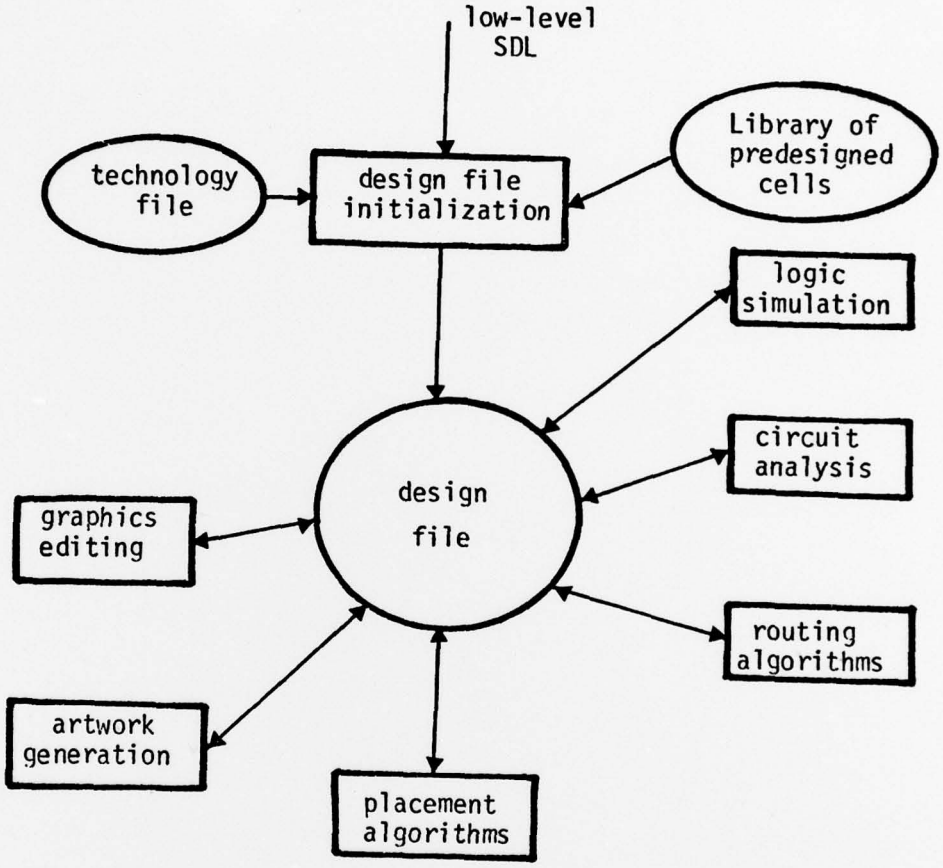


Figure 4: IC Design system structure

6. DATA BASE ENVIRONMENT

Currently, the design system consists of a collection of programs for the various functions to be performed by the designer during the design process. The link between all these subsystems currently is in the form of the Structural Design Language. However, a different kind of link exists between the various programs: the libraries used by each subsystem. For instance, a flipflop may be represented in the PC design system, where its physical characteristics are stored, in the SDL compiler subsystem, where its logical properties are stored, in the logic diagram generation system, where schematic symbols are stored, in the logic simulation subsystem where its logic model is stored, etc.

To store the information about a single component in such a diversity of locations is a rather serious problem since it makes it very difficult to check the consistency of this particular description. The obvious solution would be to store all component information and all finished designs in a central data base. This, however, would create some rather difficult problems since some of the programs used in the system such as TESTAID, MOTIS, and SPICE are not aware of such a data base and changes to the programs would be rather cumbersome. Therefore, an intermediate scheme has been devised, as illustrated in Figure 5.

Library information will be interactively entered by means of a subsystem that stores the information after verification into the central data base. Similarly, when a subsystem has completed a design, its design file can be used to update the information in the central data base by means of a design update subsystem. From the central data base, the libraries required by each of the subsystems will be produced. This will reduce the amount of access required to the data base and it will also make it possible to make use of the existing program packages without modifying them for data base access.

7. CONCLUSIONS

In the preceding paper, the underlying concepts of a design automation system currently being developed at Stanford University, were described. The major characteristics of the system are its hierarchical nature, its emphasis

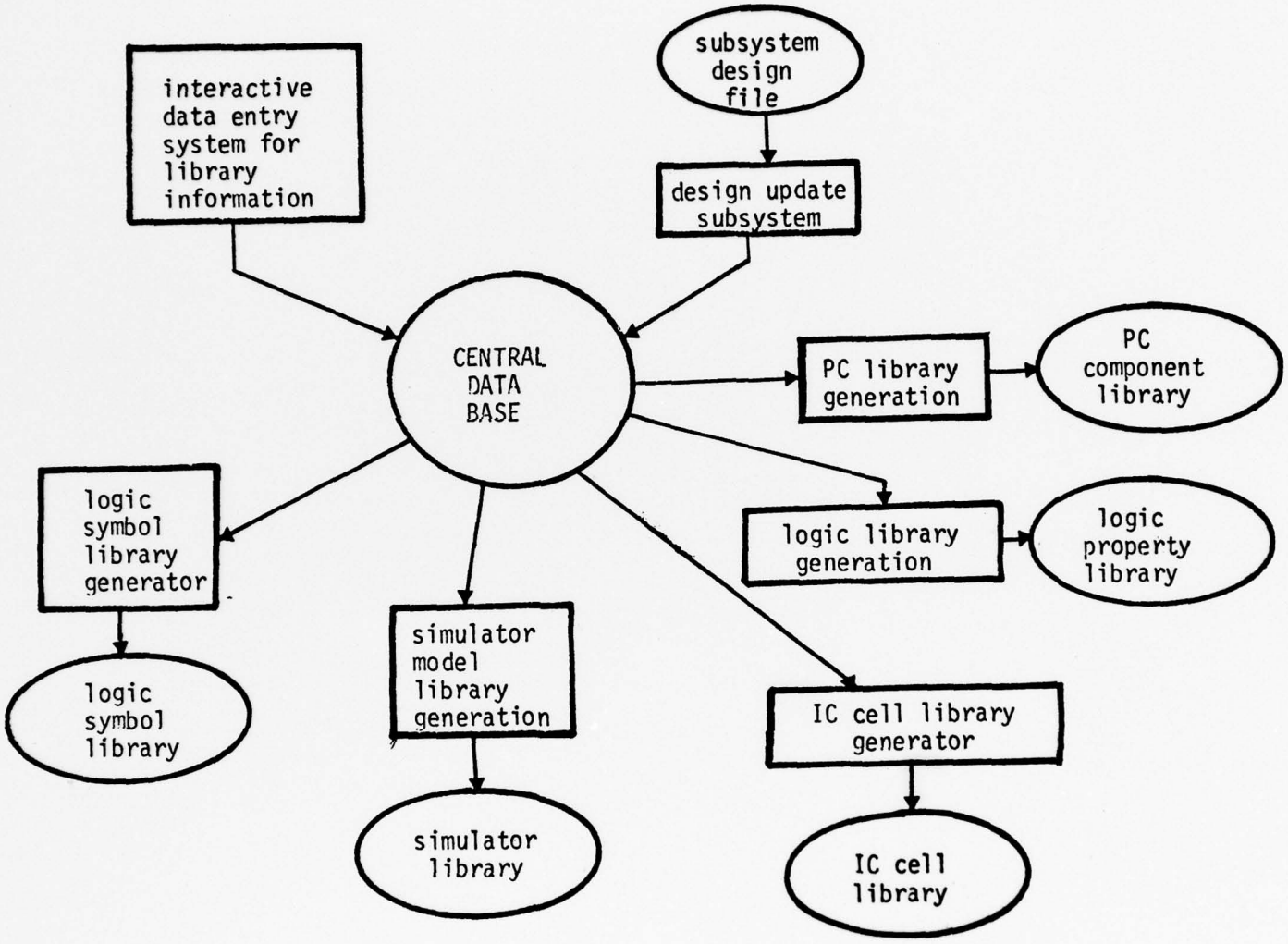


Figure 5: Data Base Organization

on structural information, and the possibility to join together a number of existing design automation software packages into a coherent system.

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