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ENCAPSULATION AND ANNEALING OF SULFUR AND SELENIUM IMPLANTED GALLIUM ARSENIDE

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes progress on a program to investigate encapsulation films used as annealing caps on ion implanted GaAs samples and to develop alternative procedures and techniques for improving the efficiency of n-type ion implants. The major (high impact) technological achievement of this research program has been the development and perfection of a chemically inert double layered encapsulation system which improves the electrical performance of ion implanted layers as well as allowing reliable annealing at temperatures up to 1100°C.

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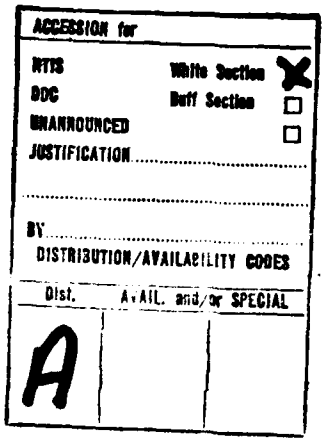

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CHAPTER I

INTRODUCTION

The objectives of this program were to provide a detailed investigation of encapsulation films used as annealing caps on ion implanted GaAs samples and to develop alternative procedures and techniques for improving the efficiency of n-type ion implants. The major (high impact) technological achievement of this research program has been the development and perfection of a chemically inert double layered encapsulation system which improves the electrical performance of ion implanted layers as well as allowing reliable annealing at temperatures up to 1100°C. The total program has included:

- Evaluation and characterization of commonly used CVD or sputter deposited SiO_2 and Si_3N_4 annealing caps used on GaAs.
- Development and testing of a low temperature (200°C) plasma deposited Si_3N_4 annealing cap.
- Investigation of the influence of residual oxygen in Si_3N_4 films on the outdiffusion of Ga from annealed and capped GaAs substrates.
- Investigation of the use of Ga_2S_3 and SiO_2/Ga_2S_3 films as annealing caps for S-implanted GaAs wafers.
- Development of a superior double layer (As)SiO_2/Si_3N_4 encapsulant for annealing ion implanted GaAs samples to 1100°C.
- Detailed microstructural characterization of defects in commercially available GaAs in the United States and Japan.
- Correlated microstructural and electrical evaluation of Al thin film caps and Au contacts on GaAs.

This report summarizes progress and results obtained during the research program. The research is described in detail in monthly reports 1 to 24, and in the journal articles and technical reports listed in the Appendix.

1.1 PROGRAM SUMMARY

During the first year of this program, we began an evaluation and experimental analysis of encapsulation procedures used for GaAs samples. We observed that none of the currently proposed techniques would satisfactorily meet all the stringent criteria required of a high temperature encapsulant for annealing ion implanted GaAs. Consequently, we decided to investigate alternative capping procedures that would allow reproducible high temperature annealing.

We began a development effort to obtain high quality plasma deposited Si_3N_4 layers. The low deposition temperature (200°C) was attractive because it would avoid the surface deterioration observed in CVD layer deposition. In addition, the process was controllable and well suited for device production procedures. Also in the first year, we began to study the use of Ga_2S_3 thin films as encapsulants for S-implanted samples.

During the second year, we completed the evaluation of Ga_2S_3 encapsulants and continued our study of Si_3N_4 caps. Further improvements in capping were obtained by using an As-doped CVD-SiO_2 layer formed on top of a plasma-deposited Si_3N_4 film. Samples encapsulated with this double layer film showed no signs of mechanical failure when annealed up to 1100°C. In addition, we detected no outdiffusion of Ga or As and no indiffusion of Si. Peak electrical activation of Se implanted samples was measured at 1×10^{19} carriers/cm^3 for samples annealed at 1100°C.

Chapter 2 discusses the results of experiments conducted on plasma deposited Si_3N_4 layers and the influence of oxygen contained within the dielectric on the outdiffusion of Ga during annealing. In Chapter 3, we discuss the improvement of Si_3N_4 caps and the development of double layered encapsulants for annealing ion implanted GaAs to temperatures of 1100°C. Chapter 4 discusses refinements of the double layered capping system and applications to other compound semiconductors. Chapter 5 reports the results obtained on thin film Ga_2S_3 and SiO_2/Ga_2S_3 systems used as annealing caps for S-implanted GaAs. Comparative experiments on S-implanted samples annealed with Si_3N_4, SiO_2, and SiO_2/Ga_2S_3 encapsulants are reported in Section 5.2.

In Chapters 6 and 7, we present the results of experiments on Al/GaAs and Au/GaAs, including both microstructural and electrical evaluations. In both cases, the metal films are routinely used as contacts on GaAs and aluminum has been proposed as a possible annealing cap at temperatures below 660°C. However, the present experiments show that interdiffusion and reactions within the Al/GaAs system limit the use of Al as a viable encapsulant.

CHAPTER 2

INFLUENCE OF OXYGEN ON THE OUTDIFFUSION OF GALLIUM IN Si_3N_4 ENCAPSULATED GaAs

A number of studies have been conducted on the properties of encapsulation layers used as annealing caps on ion implanted GaAs. Various encapsulants have included SiO_2[1-3], Si_3N_4[1-3], Al_2O_3[4], AlN[5], polysilicon[4], native Ga_2O_3[6], Al[7], Ga_2O_3/Al[8], and Ga_2S_3[9], with Si_3N_4 being the most widely used material.

Although Si_3N_4 films have been used in numerous ion implantation experiments, electrical activities and carrier profiles obtained have been shown to be dependent upon a number of parameters, including method of film deposition, stoichiometry of the nitride and type of substrate, as discussed in a recent review article.[10] The presence of oxygen is commonly observed in most Si_3N_4 annealing caps and is thought to be responsible, in part, for the poor adherence of nitride films to GaAs substrates at high anneal temperatures.[11,12] However, there have been no detailed reports on the influence of oxygen in altering the effectiveness of the cap against Ga or As outdiffusion from the substrate. The purpose of this note is to present data obtained from a number of experiments conducted on variable oxygen content plasma deposited Si_3N_4 films on GaAs.

2.1 EXPERIMENTAL PROCEDURE

Auger electron spectroscopy (AES) combined with in situ Ar-ion milling was used to determine depth profiles of the Si_3N_4/GaAs structures. The AES data were obtained by irradiating the sample with a 3-kV, 10-μA electron beam and monitoring the differential spectrum of secondary electrons with a cylindrical mirror analyzer. The ion gun provided sputtering rates of $\simeq 5$ Å min^{-1} for deposited films at an Ar pressure

of 5 x 10^{-5} Torr and ion energy of 600 eV. A standard semiquantitative formalism[13] was used to analyze the AES data.

2.2 RESULTS

In Figures 1-3, we show representative chemical depth profiles (unnormalized) obtained on samples containing variable amounts of oxygen in the form of SiO_2. Annealing in forming gas for 30 minutes at 750°C results in appreciable Ga outdiffusion in samples containing the highest oxygen concentration. The AES profiles indicate that Ga has outdiffused through the nitride to the surface of the encapsulant. Typically, such films show a darkened or nonuniform surface color in reflected light. In lower oxygen content films, the surface coloration is uniform and Ga outdiffusion is either absent or reduced to levels below the detection capabilities of the instrument. At anneal temperatures > 900°C, the high oxygen content caps generally exhibit further surface discoloration due to additional Ga outdiffusion and the initial phases of delamination can be observed.

Comparison of AES data on annealed and unannealed samples show that oxygen is incorporated during growth of the nitride films and not during subsequent annealing. In addition, there is no apparent indication that outdiffusion has occurred during deposition.

Measurements of the refractive index, n, of the nitride films show that films containing the highest oxygen concentration also exhibit the lowest refractive indices, essentially in agreement with the results of Brown et al.[14] In this early study it was shown that the refractive index of Si_3N_4 films shifted from 1.71 to 2.03 as the equivalent amount of included SiO_2 was altered from 50% to approximately zero. In the present experiments, correlation with AES data suggests that if the silicon-nitrogen ratio is maintained in film depositions, the refractive index of the nitride film will provide an indication of oxygen content and

subsequently, the relative effectiveness of the encapsulant as a barrier against Ga outdiffusion. For films containing excess nitrogen, the refractive index is also low and the concentration of voids known to be large.[10] AES profiling indicates that the outdiffusion of Ga is enhanced, similar to the case observed for stoichiometric, high oxygen content (low refractive index) Si_3N_4 films.

In all experiments we have observed no significant amounts of As within the nitride films at anneal temperatures $\leq 900^{o}C$. It is conceivable that either As outdiffusion is small, thereby escaping detection by AES profiling, or that As has outdiffused rapidly through defects in the film to the surface where it volatilized during annealing (and/or both). In either case, the present studies have consistently shown that large concentrations of oxygen within the nitride will result in increased Ga outdiffusion from the substrate.

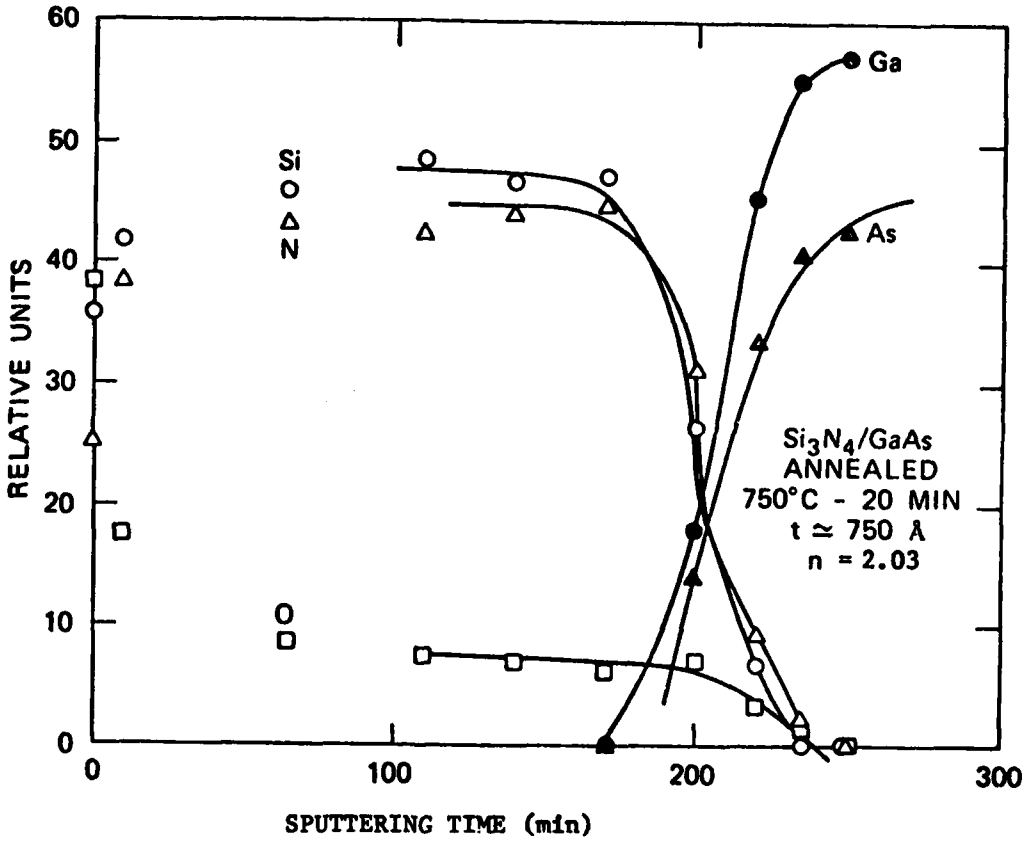

Figure 1. AES Profile (Unnormalized) of 750 Å Si_3N_4 Layer (n = 2.03) on GaAs after Annealing in Forming Gas at 750°C for 20 Minutes. No significant outdiffusion of Ga or As is observed and relative oxygen concentration in the nitride layer is low.

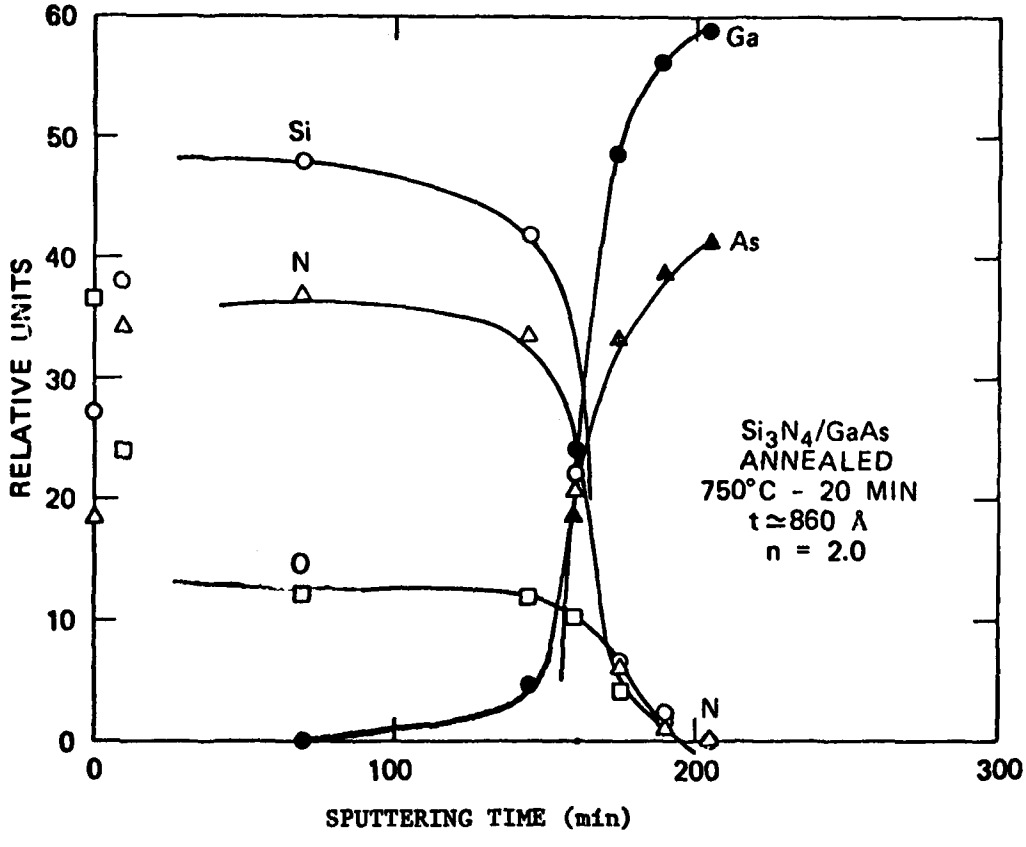

Figure 2. AES Profile (Unnormalized) of 860 Å Si_3N_4 Layer (n = 2.0) on GaAs after Annealing in Forming Gas at 750°C for 20 Minutes. Outdiffusion of Ga into the nitride film to ≃ 400 Å from the interface can be noted.

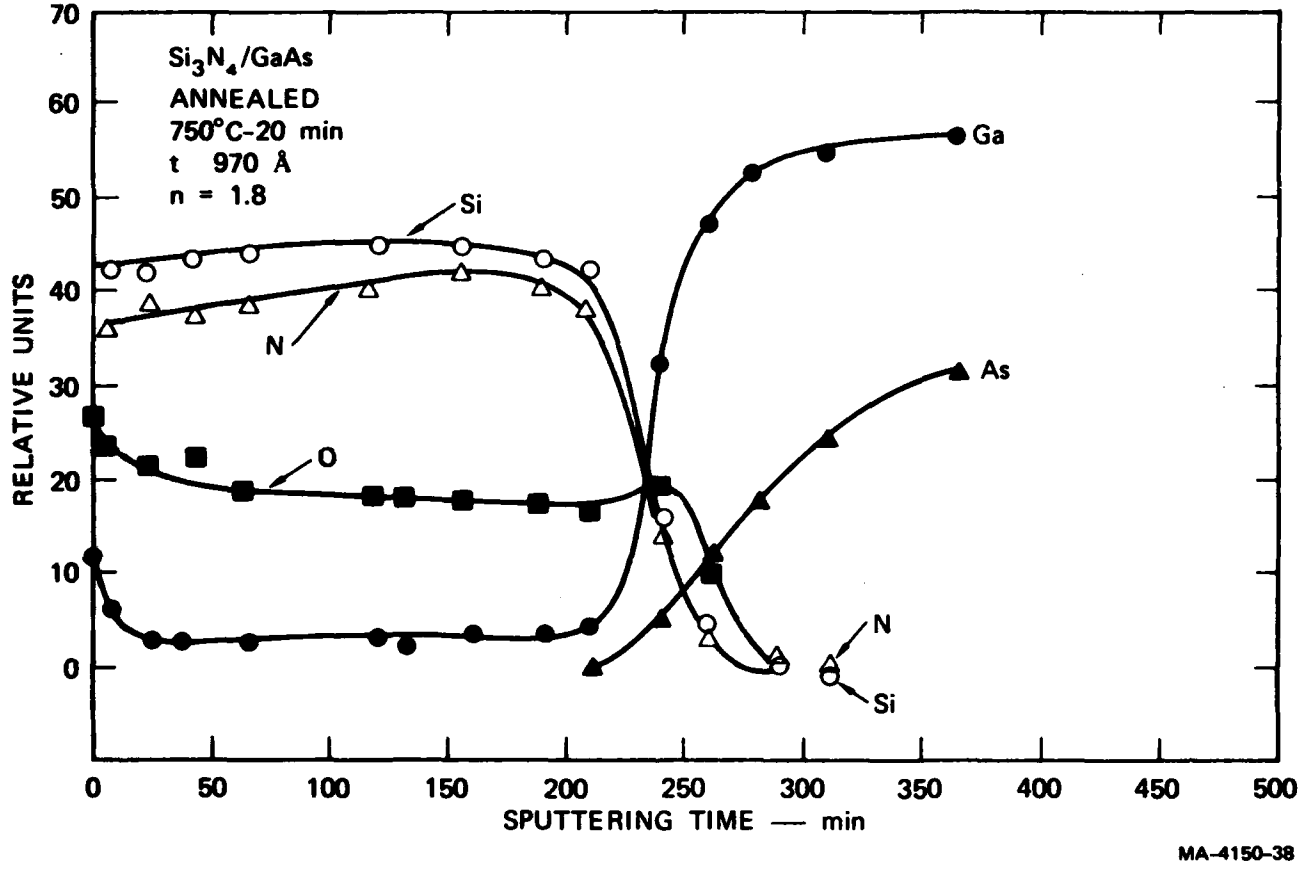

Figure 3. AES Profile of 970 Å Si_3N_4 Layer (n = 1.8) on GaAs after Annealing in Forming Gas at 750°C for 20 Minutes. The oxygen concentration is larger than observed in Figures 1 and 2 and gallium has diffused through the nitride to the surface of the film.

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CHAPTER 3

A DOUBLE LAYERED ENCAPSULANT FOR ANNEALING GaAs UP TO 1100°C

In the past few years, considerable effort has been devoted to developing new and better encapsulants for use in annealing of ion-implanted gallium arsenide and other III-V compounds.[1-3] Silicon nitride which is either sputtered, plasma deposited, or chemically deposited in the vapor phase (CVD) has been most widely used. Donnelly et al.[2] have reported reproducible annealing to GaAs up to 950°C using CVD Si_3N_4, whereas Sealy[4] has used reactively sputtered Si_3N_4 in many of his studies. Recently, Eisen et al.[5] have used reactively sputtered aluminum oxy-nitride to anneal samples up to 1000°C. However, both the sputtered silicon nitride and aluminum oxy-nitride tend to blister and pit with annoying frequency above 900°C.

We have found that high-quality plasma-deposited Si_3N_4 gives reproducible results to 900°C and has the advantage that it can be applied at 200°C which is well below the dissociation temperature of GaAs.[6] Above 900°C, however, the Si_3N_4 surface begins to show pits and blisters, making it unacceptable for use in microcircuits.

3.1 DEVELOPMENT AND ANALYSIS

In an effort to establish the cause of the pitting and surface deteroriation, a photoluminescence spectrum was taken on samples that had been ion implanted with selenium and subsequently annealed at 900°C for 4 h. The spectrum is shown in Fig. 4. The peak at 0.87 μm which is apparent in sample CS2921A1B can be attributed to an arsenic vacancy-donor complex,[7] suggesting that As outdiffusion is important in addition to the Ga dissolution that may occur in oxide-rich encapsulants.[8] In order to avoid the possibility of As outdiffusion, we therefore decided to apply an arsenic-doped SiO_2 layer on top of our plasma-deposited Si_3N_4. Donnelly et al.[2] have used a similar structure without As doping but found that it made no difference when CVD nitride was used. In contrast, we have found that samples encapsulated with our double-layer system can be successfully and reproducibly annealed at temperatures up to 1100°C.

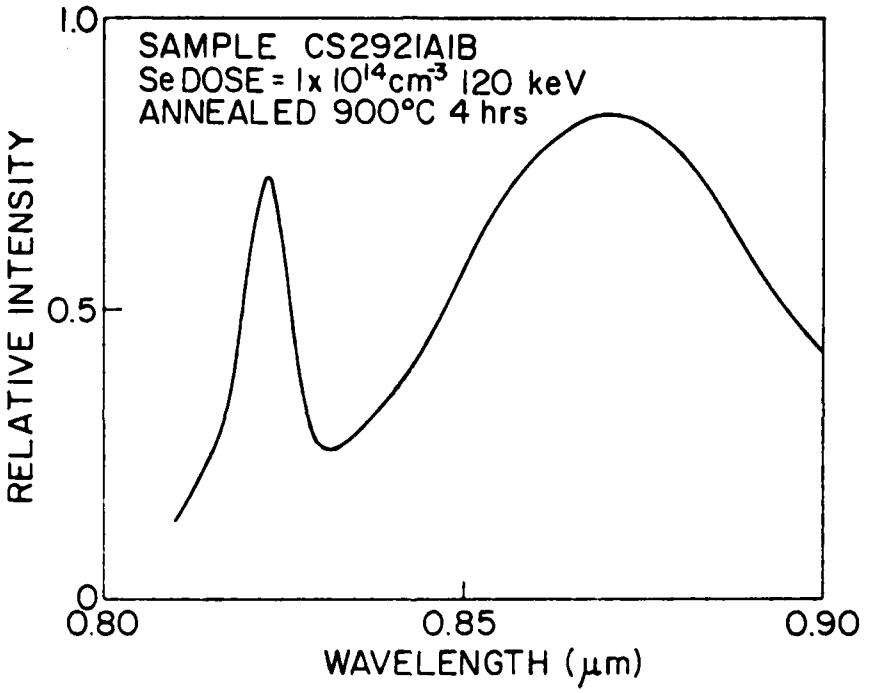

Figure 4. Photoluminescence Spectrum at Liquid Nitrogen Temperature. Sample CS2921A1B is a Se-implanted wafer annealed for 4 hours at 900°C with a plasma deposited Si_3N_4 cap.

The GaAs samples used in this experiment were all Cr-doped [100] substrates obtained from Crystal Specialties. Prior to deposition of the encapsulating layers, the samples were rinsed in TCE, acetone, methanol, and deionized water, followed by an HCl dip and another deionized water rinse.

Samples used for electrical measurements were implanted with selenium doses ranging from 10^{13} to 10^{16} ions/cm^2 at energies between 120 and 240 keV prior to the application of the Si_3N_4. During the implant all the substrates were heated to 500°C.

All substrates were coated with 1000 Å of plasma-deposited Si_3N_4 at 200°C (index of refraction measured to be 2.05) after which a 3000-Å CVD SiO_2 layer heavily doped with As (As concentration was measured by backscattering to be $\sim 2 \times 10^{20}$ cm^{-3}) was applied at 450°C.

Auger profiling analysis on unimplanted samples annealed at temperatures ranging from 900 to 1000°C indicate that some outdiffusion of Ga is present. The amount of Ga outdiffusion has been seen to vary from experiment to experiment and appears to depend on the amount of oxygen in the Si_3N_4 film.[9] If As is outdiffusing as well then it is below the sensitivity limit of our Auger system ($\sim 1 \times 10^{19}$ cm^{-3} for As). The backscattering data in Fig. 5 also supports this idea. Shown is a sample with our double-layer encapsulant deposited as described above but without As doping. The peak developing in the SiO_2 region can be attributed to this Ga outdiffusion.

Using the standard Van der Pauw technique, the electrical activity of the implanted samples was measured for various selenium doses in samples annealed up to 1100°C. All of the samples tested with the double-layered cap showed smooth featureless surfaces after anneal when examined with an SEM. Control samples with just Si_3N_4, however, showed widespread pitting above 900°C. In Fig. 6 we have plotted sheet carrier concentration

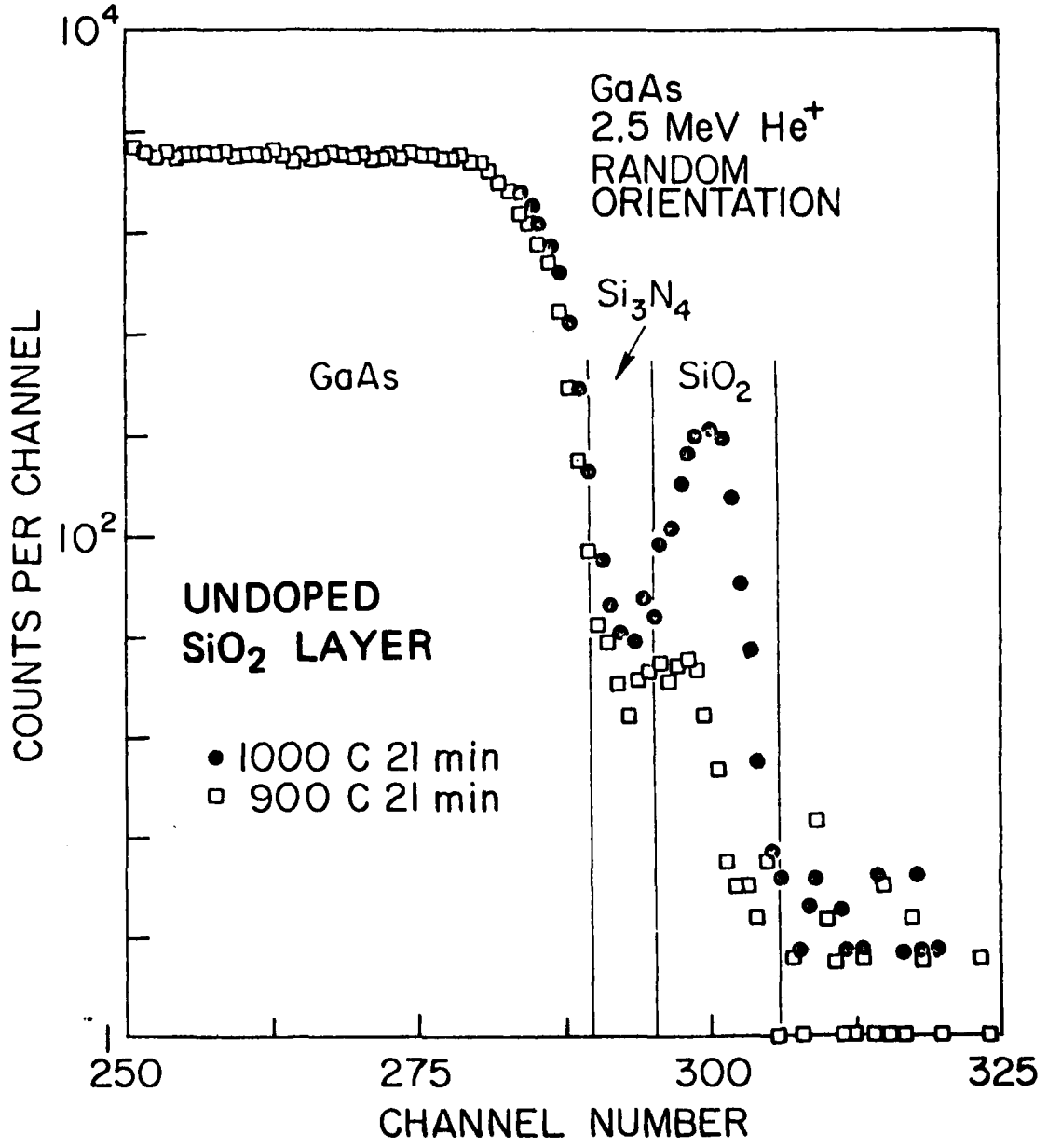

Figure 5. Backscattering Spectra for 2.5 MeV He^+ Incident on $SiO_2/Si_3N_4/GaAs$ as a Function of Anneal Temperature

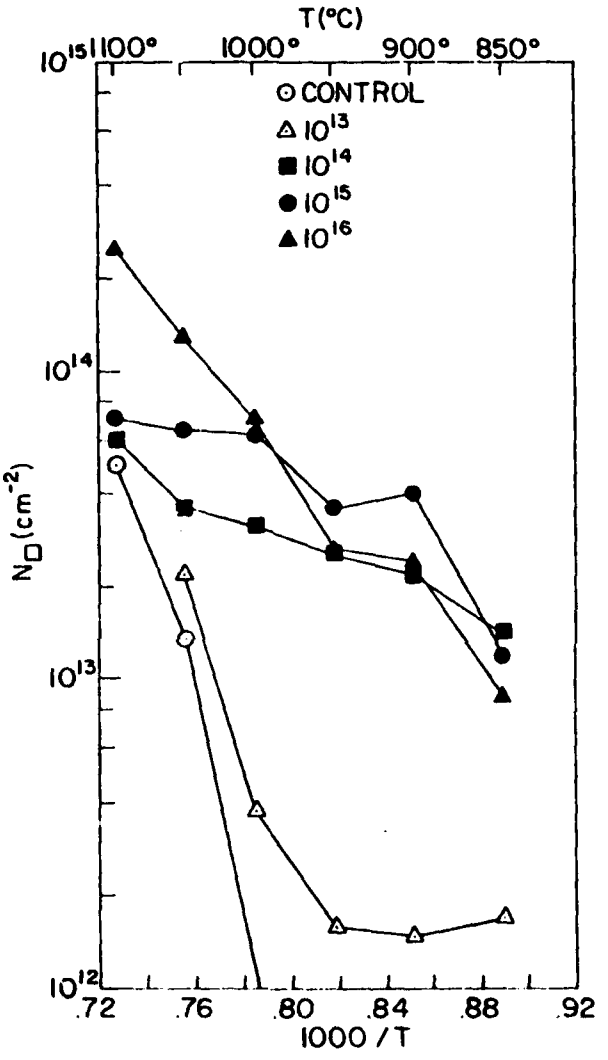

Figure 6. Sheet Carrier Concentration versus 1/T. (⊙) - no implant, (Δ) - 1 x 10^{13} cm^{-2} implant at 120 keV, (■) - 1 x 10^{14} cm^{-2} implant at 120 keV, (●) - 1 x 10^{15} cm^{-2} implant at 120 keV, (▲) - 1 x 10^{16} cm^{-2} implant at 120 keV. Above 950°C the sample with no implant has a significant carrier concentration indicative of possible Si indiffusion.

versus $1/T$ for four doses of selenium implanted at 120 keV and plotted in Fig. 7 is the corresponding sheet resistance and Hall mobility.

A significant point to note is that samples annealed above 950°C start to show increasing sheet carrier concentration. In fact, at 1050°C the 10^{13}-cm^{-2} implant shows 230% activity. We believe that these "extra donors" are due to silicon indiffusion from the Si_3N_4.

A few samples were implanted to a dose of 1×10^{13} cm^{-2} with selenium at 240 keV with either our double-layered cap or simply a Si_3N_4 cap. Chemical stripping was performed on these samples using a 160:1:1 H_2O:H_2O_2:H_2SO_4 etch calibrated at approximately 2.8 Å/sec. In Fig. 8 we see a comparison between the carrier concentration versus depth profile for a sample annealed with an As-doped SiO_2/Si_3N_4 cap and that of a sample with only a Si_3N_4 cap. A significant feature of this plot is that in the sample annealed with our double-layered system there appears to be very high electrical activity of the selenium dopant near the surface, whereas the sample with only the Si_3N_4 cap has a typical "dead layer" of about 100 Å. Disagreement of the Se profile with the LSS distribution shown in Fig. 8, may be due to anomalous diffusion of the implanted Se and will be dealt with in a later publication.

In Tables I and II we show a comparison between the samples implanted and annealed at 900°C with As-doped SiO_2/Si_3N_4 caps and those annealed at 900°C with simple a Si_3N_4 cap. Significant improvement in electrical activity can be seen.

GaAs samples have been annealed at up to 1100°C using the As-doped SiO_2-Si_3N_4 system, with no sign of pitting, flaking, or surface deterioration. Samples annealed at 900°C with this encapsulation tend to have higher electrical activity than samples with the same anneal but with only Si_3N_4 as an encapsulant. In certain situations, the two-layer encapsulant may also prevent the formation of a "dead layer".

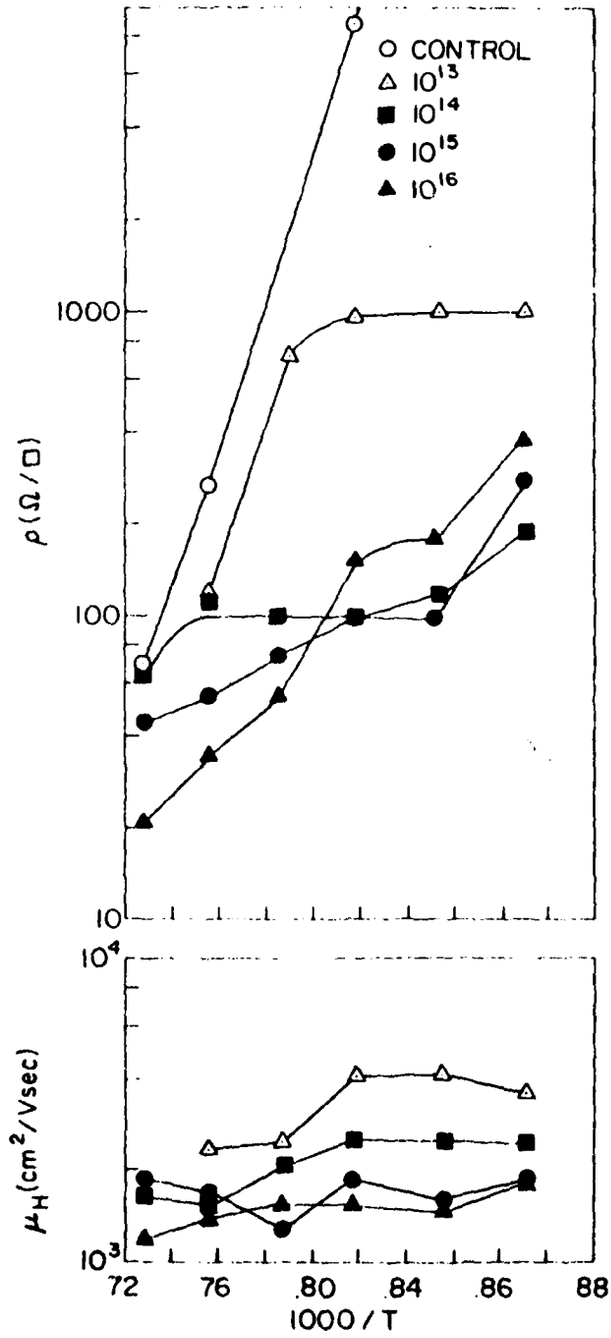

Figure 7. **Sheet Resistance and Hall Mobility as a Function of 1/T for Samples in Figure 6.**

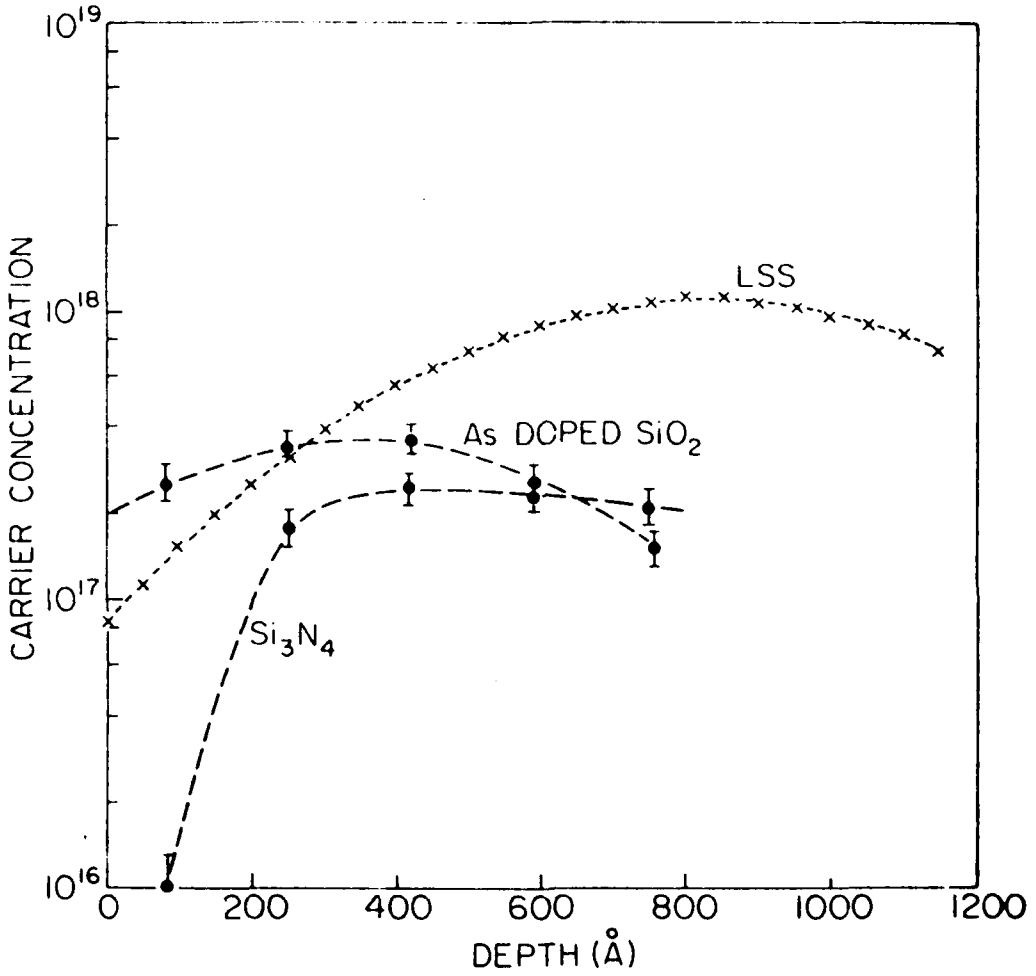

Figure 8. Carrier Concentration versus Depth Profile for Cr-Doped GaAs Implanted to a Dose of 1 x 10^{13} cm^{-2} at 240 keV Annealed with As-Doped SiO_2/Si_3N_4 and with just Si_3N_4.

A similar double layered structure using a phosphorus-doped SiO_2/Si_3N_4 encapsulation system is presently being deployed for annealing ion-implanted InP at temperatures up to 900°C.

TABLE 1. COMPARISON OF ELECTRICAL DATA FOR LOW-DOSE IMPLANTS AT 240 keV

Samples implanted at 240 keV
Substrates at 500°C

Annealed at 900°C
30 min H_2 ambient

Dose (cm^{-2})	Cap	ρ ($\Omega/\square$)	μ_H (cm^2/Vsec)	N_D (cm^{-2})
1×10^{13}	(As)SiO_2/Si_3N_4	488	5068	2.52×10^{12}
1×10^{13}	Si_3N_4	647	4992	1.93×10^{12}

TABLE 2. COMPARISON OF ELECTRICAL DATA FOR HIGH-DOSE IMPLANTS AT 120 keV.

Samples implanted at 120 keV
Substrates at 500°C

Annealed at 900°C
15 min H_2 ambient

Dose (cm^{-2})	Cap	ρ ($\Omega/\square$)	μ_H (cm^2/Vsec)	N_D (cm^{-2})
1×10^{14}	(As) SiO_2/Si_3N_4	114	2090	2.63×10^{13}
1×10^{14}	Si_3N_4	144	2222	1.95×10^{13}
1×10^{15}	(As) SiO_2/Si_3N_4	88	1940	3.68×10^{13}
1×10^{15}	Si_3N_4	131	1583	3.01×10^{13}
1×10^{16}	(As) SiO_2/Si_3N_4	107	1519	3.85×10^{13}
1×10^{16}	Si_3N_4	136	1505	3.05×10^{13}

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CHAPTER 4

MULTILAYERED ENCAPSULATION OF GaAs AND OTHER COMPOUND SEMICONDUCTORS

Encapsulation of ion-implanted GaAs has received much attention by many workers in the last few years.[1-9] The goal of these groups has been to develop an encapsulating layer which preserves the chemical and electrical properties of the starting materials.

In Table 3 are listed six of the most widely applied encapsulating films and some of their relative advantages and disadvantages. As can be seen, no single system meets all of the chosen requirements for an ideal encapsulant.

We decided to characterize the failure mechanisms for one of the above caps--plasma deposited Si_3N_4--in an effort to improve its properties. Other workers have found that an oxygen free plasma deposited silicon nitride film will not dissolve arsenic or gallium to within Auger electron analysis detection limits.[10,11] However, there still exists the possibility that arsenic may escape through pinholes or diffusion pipes during a high temperature anneal and still not be detected. In order to test this hypothesis, we encapsulated a Se ion-implanted Cr doped GaAs substrate with plasma deposited Si_3N_4 and annealed it at 900°C for 4 hours. Subsequent photoluminescence measurements yield the spectrum in Figure 4. The peak at 0.87 μm can be attributed to an arsenic vacancy-donor complex,[12] suggesting that arsenic outdiffusion through pipes or pinholes might be occurring in these samples.

In addition to the possible arsenic outdiffusion problem, we have found that high quality plasma deposited silicon nitride films tend to pit and blister with annoying frequency above 900°C. It has been shown that similar ruptures of silicon nitride on silicon occur due to the great mismatch in Young's modulus across the interface.[13] (For the case of Si_3N_4 on GaAs, the mismatch in compressibilities is even greater[14]

TABLE 3. A REVIEW OF SOME OF THE MOST WIDELY USED ENCAPSULATING LAYERS AND A FEW OF THEIR RELATIVE STRENGTHS AND WEAKNESSES.

ENCAPSULANT	EASY TO APPLY/REMOVE?	APPLIED BELOW 600°C?	DISSOLVES Ga OR As?	INDIFFUSION FROM CAP?	PEEL/PIT?
CVD Si_3N_4	YES	NO	NO	YES	YES (1000°C)
REACTIVELY SPUTTERED Si_3N_4	YES	YES	YES	?	YES (900°C)
PLASMA Si_3N_4	YES	YES	NO	NO	YES (900°C)
SiO_2	YES	YES	YES	NO	YES (1000°C)
AlN	YES	YES	NO	?	YES (1000°C)
Al	YES	YES	YES	YES	YES (700°C)

We have found that a solution to these problems is a double layered encapsulation system consisting of plasma deposited Si_3N_4 followed by chemical vapor deposited SiO_2 heavily doped with arsenic. In the subsequent sections, we shall show that this double layered cap has all the desirable traits set forth above by analyzing the outdiffusion of Ga and As, the indiffusion of Si from the Si_3N_4, the surface crystallinity, and the electrical activation of ion-implanted Se.

4.1 EXPERIMENTAL PROCEDURE

The GaAs samples used in these experiments were all [100] substrates obtained from two separate sources. The Cr doped wafers were from Crystal Specialties, while the Si doped wafers were from Laser Diodes. Prior to processing, all wafers were etched in a solution consisting of 5:1:1 H_2SO_4:H_2O_2:H_2O for 60 seconds.

Samples used for electrical measurements were then cleaned in boiling TCE, boiling acetone, boiling isopropyl alcohol, rinsed in deionized water, and dipped in 50:1 H_2O:HF followed by a final deionized water rinse. These substrates were then ion-implanted with Se doses ranging from 1×10^{13} cm^{-2} to 1×10^{16} cm^{-2} at energies between 120 and 240 keV. During implantation, the substrates were heated to 500°C.

All samples received a hot solvent cleaning similar to that described above prior to the silicon nitride plasma deposition. Between 500 and 3000 Å of nitride was deposited with a measured index of refraction between 2.03 and 2.04. Deposition rate was consistently 125 Å/min at a substrate temperature of 200°C.

Chemical vapor deposition of arsenic doped SiO_2 was performed in an Applied Materials silox reactor at a susceptor temperature of 450°C. The deposition rate was measured to be approximately 600 Å/min. Film thicknesses grown were between 0.3 and 3 μm with a measured index of refraction

of 1.47. Backscattering analysis on these oxides indicate an As concentration of about 2×10^{20} cm^{-3}.

All annealing of the encapsulated GaAs was done in flowing hydrogen.

Electrical profiling measurements used a standard Van der Pauw technique in conjunction with anodic stripping. The chemical used for the anodic oxide growth was a solution of potassium permanganate and acetone as described in Ref. 15. Front ohmic contacts consisted of alloyed indium and were protected from the anodic solution by a 20 μm coating of parylene plastic.[16]

4.2 CHARACTERISTICS OF ANNEALED (As)SiO_2/Si_3N_4 ENCAPSULATION OF GaAs

In Fig. 9 is illustrated the double layered structure used for high temperature annealing of GaAs. In this particular configuration, we have 1 μm of As doped SiO_2 on top of 1000 Å of plasma deposited Si_3N_4. Scanning electron micrographs of a samples encapsulated in this manner and annealed at 1100°C for 15 minutes showed no pitting or flaking. In the following sections, we present further evidence of the merits of this system by investigation outdiffusion of Ga and As, indiffusion of Si, and electrical properties of ion-implanted and annealed layers.

4.2.1 The Si_3N_4/GaAs Interface

In Figs. 10 and 11, we show normalized Auger profiles for films annealed at 900°C and 1050°C, respectively. No diffusion from the substrate to the encapsulant of either Ga or As can be measured to within the Auger detectability limits for these elements (1×10^{19} cm^{-3} for As and 5×10^{18} cm^{-3} for Ga). In addition, the sample annealed at 1050°C was examined using high resolution dark field and light field transmission electron microscopy (TEM) and transmission electron diffraction (TED). Substrate regions near the interface show no evidence of precipitation,

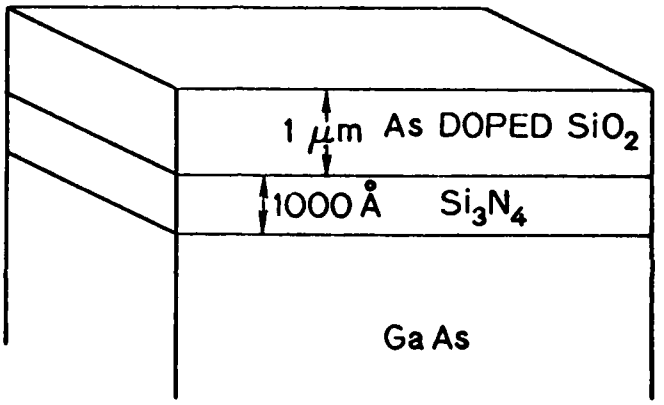

Figure 9. Schematic Representation of the Double Layered Encapsulant Typically Used for the High Temperature Annealing for Ion Implanted GaAs.

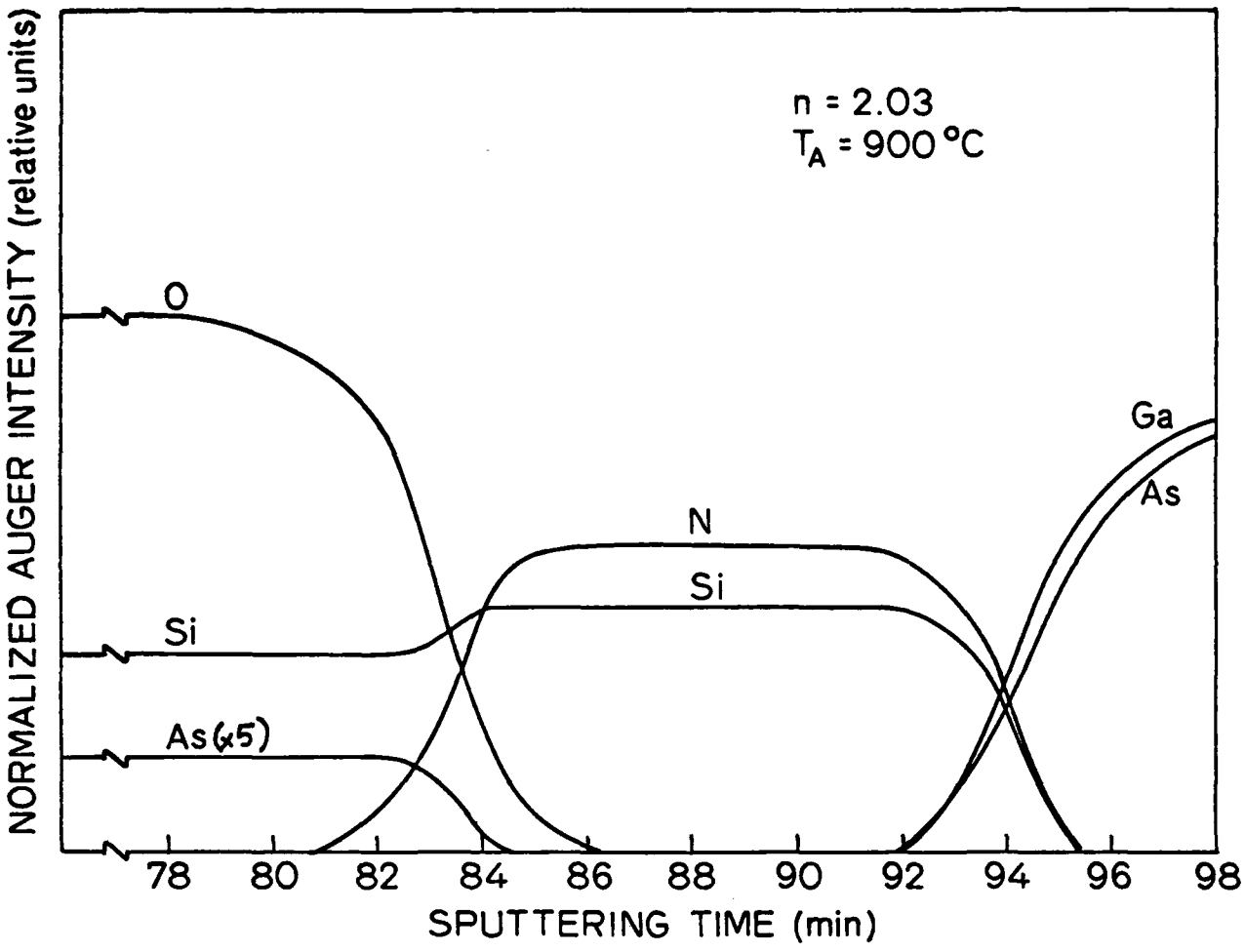

Figure 10. Auger Profile of an Encapsulating Layer Consisting of 1 μ Arsenic Doped Oxide on Top of 1000 Å Si_3N_4 After a 900°C 15 Minute Anneal.

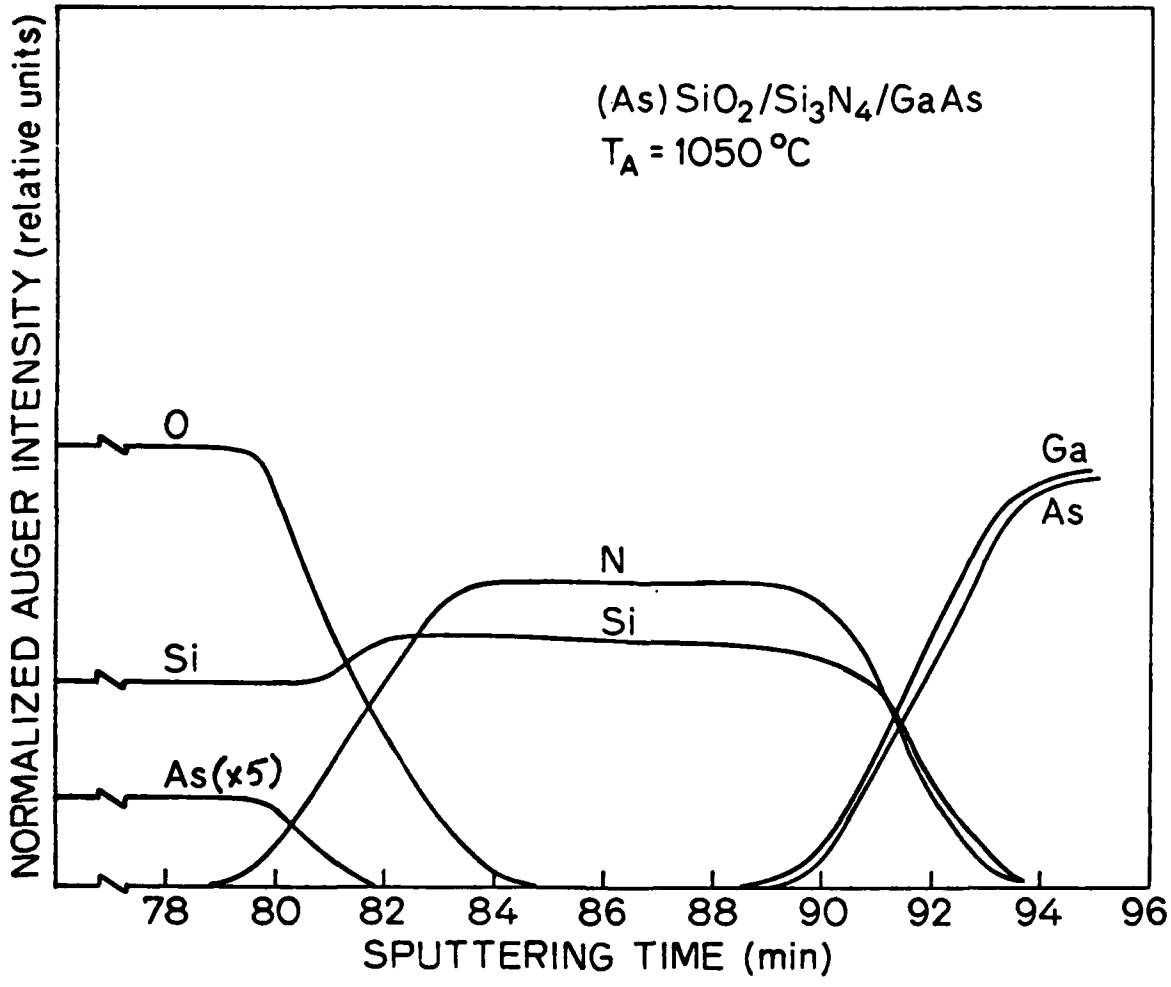

Figure 11. Auger Profile of an Encapsulating Layer Consisting of 1 μ Arsenic Doped Oxide on Top of 1000 Å Si_3N_4 After a 900°C 15 Minute Anneal. No Ga or As has outdiffused to within the Auger detectability limits.

second phase structure, or reordering as a result of the annealing. Comparison with unannealed control samples showed no perceptible increase in dislocation densities. Selected area diffraction patterns obtained in the near surface region also showed no evidence of reordering or compound formation.

Secondary ion mass spectrometry (SIMS) profiles using a Cs primary ion source[17,18] have been made on samples annealed at 1100°C for 15 minutes in order to determine whether Si indiffused from the Si_3N_4, thus doping the GaAs. With an estimated sensitivity of 1×10^{17} cm^{-3} for Si, no indiffusion was detected.

Photoluminescence measurements have been made using the 4880 Å line from an argon laser and a PbS detector on both ion-implanted and bulk Si-doped GaAs wafers with particular attention paid to the 0.87 μm Se/Si-V_{As} peak and the 1.2 μm Se/Si-V_{Ga} peak.[19] In Fig. 12 are the spectra obtained from a Si doped ($n = 1.7 \times 10^{17}$ cm^{-3}) sample before and after a 1050°C 15 minute anneal. Identical peaks near 1.2 μm are observed, indicating that Ga outdiffusion is negligible. In addition, it should be noted that the sample before anneal did not yield a detectable band-to-band or band-to-shallow-donor transition peak. This suggests that nonradiative recombination paths are dominant. In contrast, after anneal there is a strong band-to-band and band-to-shallow donor peak possibly due to thermal annealing of the nonradiative centers.

We have also compared the post anneal photoluminescence spectra obtained from identically Se ion-implanted and annealed (900°C, 15 minutes) samples. The only difference in the processing was that sample DH164189 had the double layered encapsulant of 1000 Å Si_3N_4 plus 10,000 Å (As)SiO_2, while sample SH164189 had only 1000 Å Si_3N_4. Shown in the inset of Fig. 13 are the normalized Se-V_{Ga} peaks demonstrating that the double layered encapsulation is an effective deterrent to Ga outdiffusion even when the Si_3N_4 alone is not.

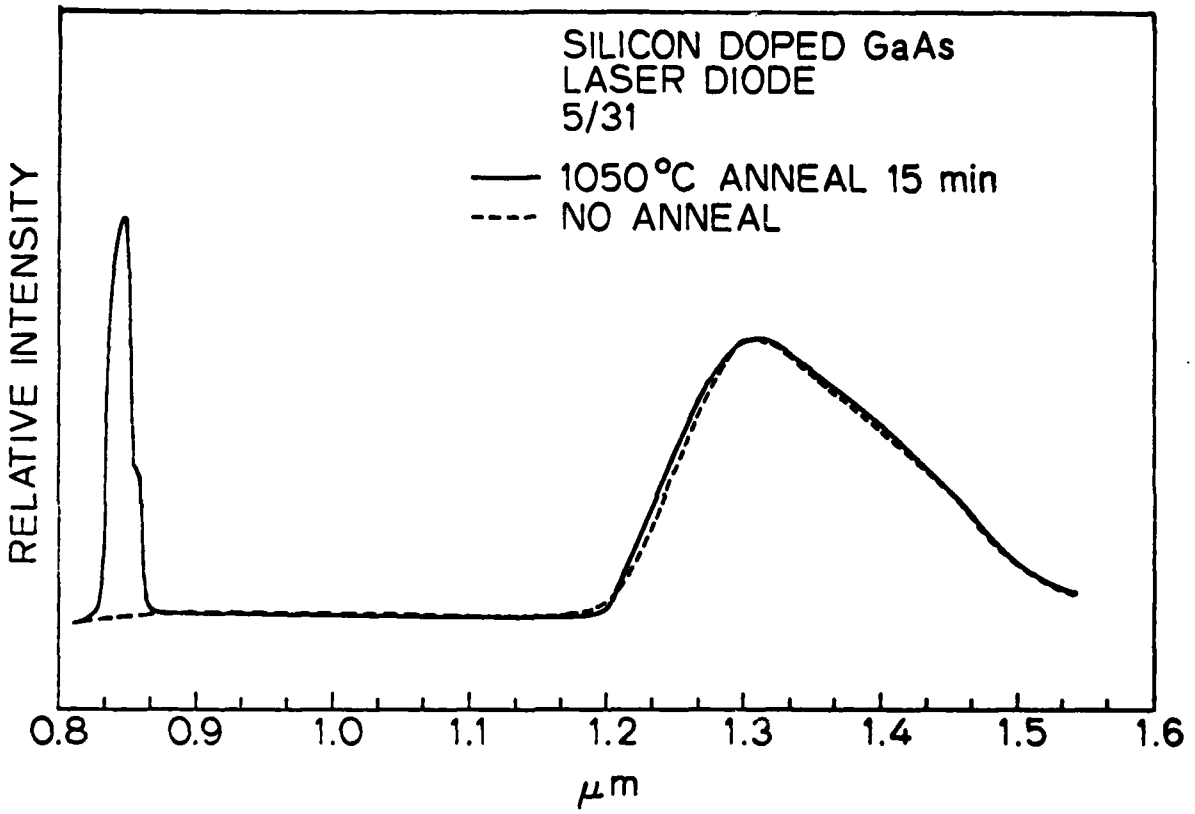

Figure 12. Photoluminescence Spectra at Liquid Nitrogen Temperatures After 1050°C Annealing. Shown is a Si doped GaAs sample before (dashed line) and after (solid line) a 1050°C 15 minute anneal. No change is detected in the Si-V_{Ga} peak appearing at 1.3 μ.

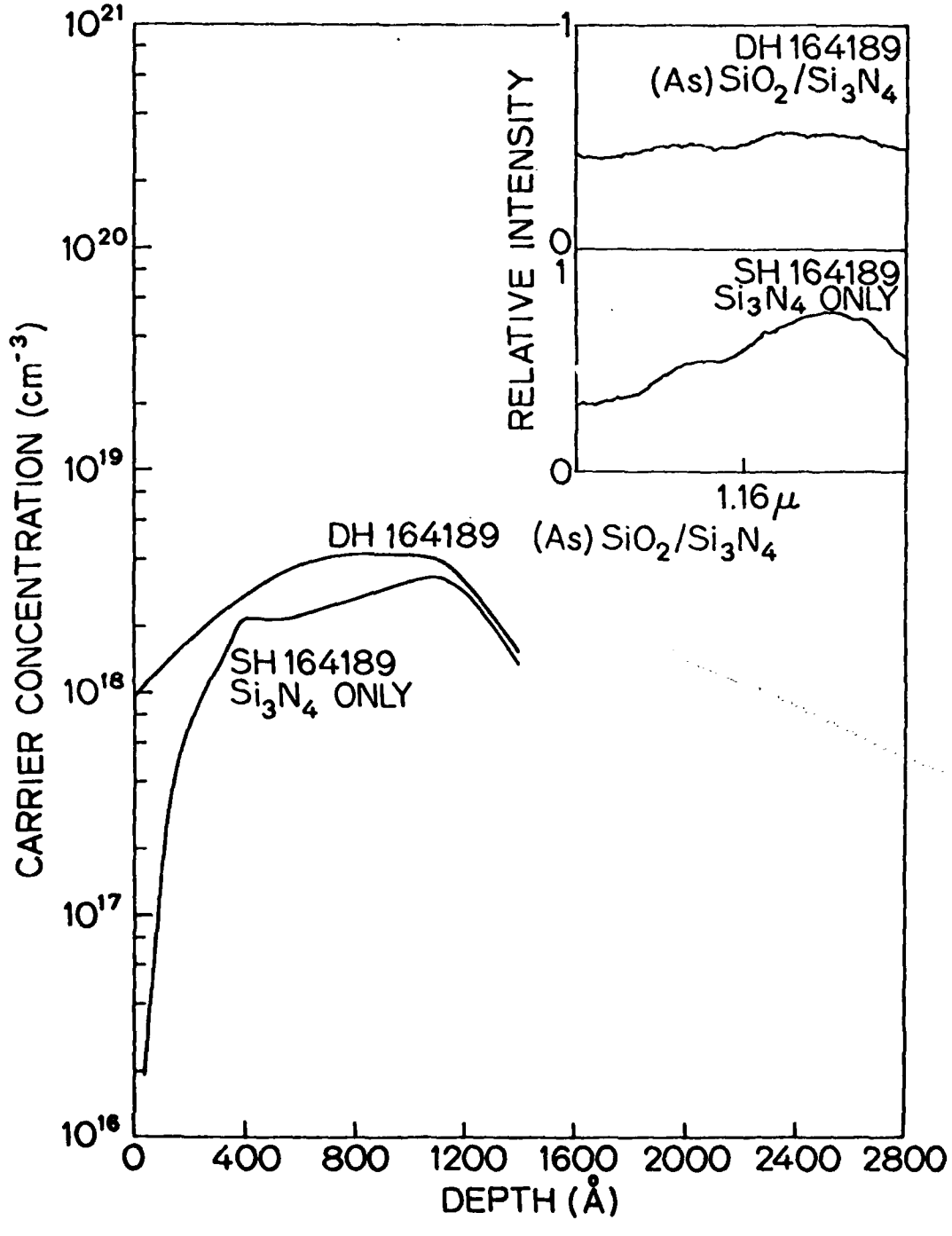

Figure 13. Carrier Concentration versus Depth Profiles for a Sample Encapsulated and Annealed with Si_3N_4 only and one Encapsulated and Annealed with the Double Layered Cap Following a 1 x 10^{16} cm^{-2} Se Implant at 120 keV. In the inset is shown the corresponding 1.2 u Se-V_{Ga} peaks for these two samples.

4.2.2 Electrical Measurements

Electrical activity of Se ion-implanted GaAs samples encapsulated with either (As)SiO_2/Si_3N_4 or Si_3N_4 only and annealed at temperatures between 850°C and 1100°C have been measured. A summary of the results obtained in a comparison between the two encapsulation systems is presented in Tables 4 and 5 for samples implanted to Se fluences between 10^{13} and 10^{16} cm^{-2} and annealed at 900°C. Those substrates annealed with the double layered cap showed consistently higher electrical activation than those annealed with Si_3N_4 only. Furthermore, in Fig. 13, we have plotted the carrier concentrations as a function of depth for the samples implanted to a Se dose of 1×10^{16} cm^{-2}. Reduced electrical activity of the Se near the surface is characteristic of those samples annealed with only Si_3N_4. It has been suggested that a reduction in electrical activity may result from additional Se-V_{Ga} pairs[20] that have been formed in the near surface region due to Ga outdiffusion into the single layered cap. This is supported by the corresponding Se-V_{Ga} photoluminescence peaks for the particular samples shown in the inset of Fig. 13.

In Fig. 14 are the carrier concentration versus depth profiles for a 10^{16} Se ions/cm^2 implant at 120 keV and annealed with the double layered cap at 850°C (squares), 950°C (open circles), 1000°C (closed circles), 1050°C (triangles), and 1100°C (crosses). Significant annealing of this implant occurs monotonically to 1100°C where a peak carrier concentration of 1×10^{19} cm^{-3} is reached. We believe that this is the highest carrier concentration ever measured for an n-type implant into GaAs.

Figures 6 and 7 summarize the annealing behavior of Se ion-implanted GaAs for doses ranging from 10^{13} to 10^{16} ions/cm^2 and for temperatures between 850°C and 1100°C. It is important to note that there are a significant number of carriers measured in the Cr-doped control samples

TABLE 4. COMPARISON OF ELECTRICAL DATA FOR 1 x 10^{13} cm^{-2} Se IMPLANTED AT 240 keV ANNEALED WITH DOUBLE LAYERED ENCAPSULANT AND ANNEALED WITH Si_3N_4.

Samples implanted at 240 keV Substrates at 500°C			Annealed at 900°C 30 min H_2 Ambient	
Dose (cm^{-2})	Cap	$\rho(\Omega/\square)$	μ_H (cm^2/Vsec)	N_D (cm^{-2})
1×10^{13}	(As)SiO_2/Si_3N_4	488	5068	2.52×10^{12}
1×10^{13}	Si_3N_4	647	4992	1.93×10^{12}

TABLE 5. COMPARISON OF ELECTRICAL DATA FOR HIGH-DOSE IMPLANTS AT 120 keV ANNEALED WITH DOUBLE LAYERED ENCAPSULANT AND ANNEALED WITH Si_3N_4 ONLY.

Samples implanted at 120 keV Substrates at 500°C			Annealed at 900°C 15 min H_2 Ambient	
Dose (cm^{-2})	Cap	$\rho(\Omega/\square)$	μ_H (cm^2/Vsec)	N_D (cm^{-2})
1×10^{14}	(As)SiO_2/Si_3N_4	114	2090	2.63×10^{13}
1×10^{14}	Si_3N_4	144	2222	1.95×10^{13}
1×10^{15}	(As)SiO_2/Si_3N_4	88	1940	3.68×10^{13}
1×10^{15}	Si_3N_4	131	1583	3.01×10^{13}
1×10^{16}	(As)SiO_2/Si_3N_4	107	1519	3.85×10^{13}
1×10^{16}	Si_3N_4	136	1505	3.05×10^{13}

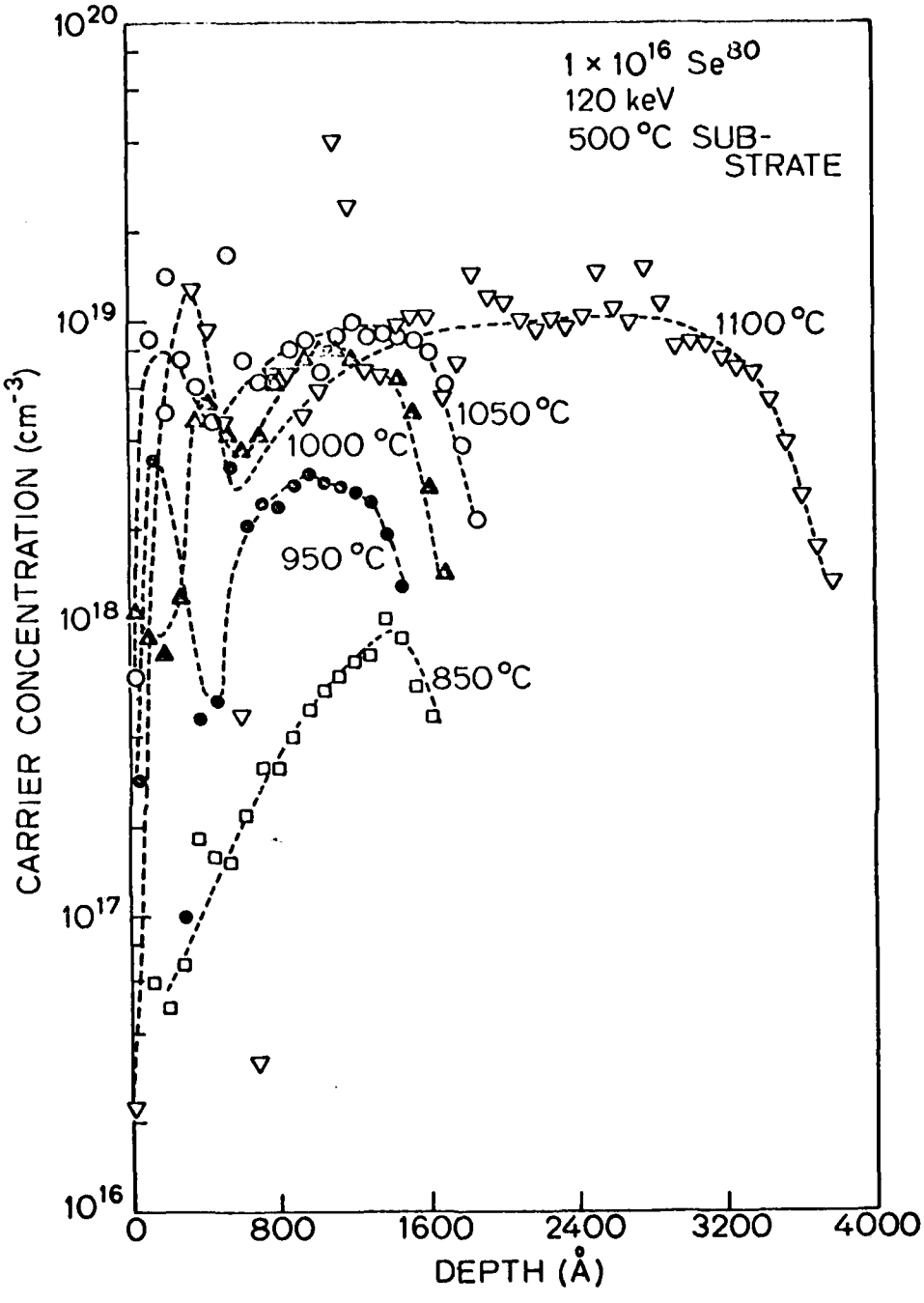

Figure 14. Carrier Concentration versus Depth Profiles for Cr-Doped Substrates Implanted to a Se Dose of 1 x 10^{16} cm^{-2} at 120 keV and Annealed with the Double Layered Cap. (□) - 850°C, (●) - 950°C, (▲) - 1000°C, (⊙) - 1050°C, (▼) - 1100°C.

for annealing temperatures above 950°C. Based on the SIMS data discussed above, however, we believe that these "extra carriers" are due to bulk substrate conversion and are not caused by Si indiffusion from the Si_3N_4.

4.3 OPTIMIZATION OF DOUBLE LAYERED ENCAPSULANTS

In order to determine the optimum ratio of doped oxide to nitride, we have annealed wafers at 1050°C and have varied both the Si_3N_4 and the (As)SiO_2 thickness. Scanning electron micrographs show that for an arsenic doped oxide to silicon nitride ratio of greater than 4-to-1, we achieve a defect free surface following annealing. This ratio is observed to be constant for Si_3N_4 thicknesses between 500 and 2000 Å. Above 2000 Å, however, no amount of arsenic doped oxide prevented widespread splitting of the dielectric layers. In conclusion, therefore, an encapsulating layer of 500 Å Si_3N_4 and 2000 Å of (As)SiO_2 might be optimum since it also will produce the least amount of interface strain due to thermal expansion mismatch.

4.4 CALCULATION OF STRAIN FOR A THIN MULTILAYERED ENCAPSULATION SYSTEM

If we assume that the mechanism for mechanical failure of encapsulants in general is that the stress in these thin layers exceeds their maximum breaking stress, then it becomes important to be able to calculate these relevant quantities.

The force required to bend a solid beam to a radius of curvature R (see Fig. 15) has been calculated[21] to be

$$F = WBt^2/6R \qquad (1)$$

B is the Young's modulus for the substrate material.

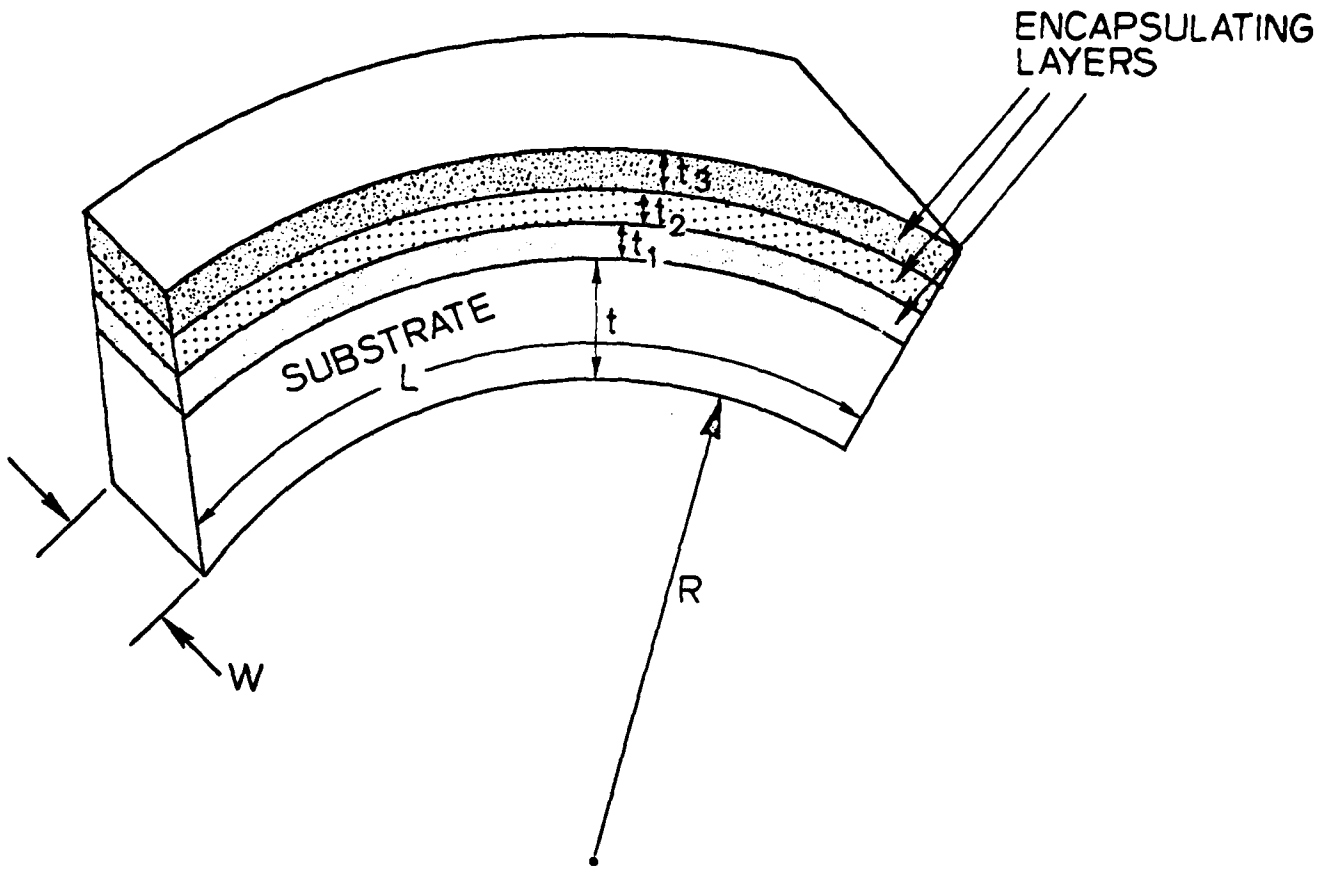

Figure 15. Schematic Representation of Sample Warpage Due to Different Expansion at the Encapsulant/Substrate Interface.

If we deposit on this beam several thin layers of different materials, each having a different coefficient of expansion, a strain will result if this system is heated to a temperature different from the deposition temperature. The force required to stretch a thin layer $\Delta x/L$ is given by

$$F = WBt \frac{\Delta x}{L} \tag{2}$$

The force required to stretch several thin layers sufficiently to make them all conform to the substrate at the annealing temperature is therefore

$$F = \frac{W}{L} (B_1 t_1 \Delta x_1 + B_2 t_2 \Delta x_2 + B_3 t_3 \Delta x_3 + \ldots) \tag{3}$$

To first order,

$$\frac{\Delta x_i}{L} = (k_i \Delta T_i - k\Delta T) \tag{4}$$

where ΔT_i is the difference between the deposition temperature and the annealing temperature for the i^{th} layer and ΔT is the difference between the deposition temperature of the 1st layer and the annealing temperature. Equating (3) and (1) gives

$$R = \frac{Bt^2}{6} \left(1/\left(B_1 t_1 (k_1 - k)\ \Delta T + B_2 t_2 (k_2 \Delta T_2 - k\Delta T) + \ldots\right)\right) \tag{5}$$

The condition for zero stress is met when $R \to \infty$, which will occur when the denominator of this equation goes to zero.

$$B_1 t_1 (k_1 - k)\ \Delta T + B_2 t_2 (k_2 \Delta T_2 - k\Delta T) + \ldots = 0 \tag{6}$$

This delineates one of the possible advantages of a multilayered encapsulant for annealing compound semiconductors: materials can be chosen such that equation (6) is a minimum, thus creating a "zero strain" encapsulant. An additional advantage of a multilayered encapsulation system is that the maximum stress for tearing of the combined layer is greater than that of each of the individual layers. In other words, even a system which <u>increases</u> the stress induced at the substrate-encapsulant interface will be an improvement if the corresponding maximum stress for tearing is increased by a greater amount.

For the arsenic doped oxide-silicon nitride encapsulation, we have calculated the two appropriate terms in equation (6) using the data of Refs. 13 and 14.

$$B_1 t_1 (k_1 - k)\,\Delta T = -6.8 \times 10^5 \text{ dynes/cm for 1000 Å } Si_3N_4 \text{ at } 1050^\circ C$$

$$B_2 t_2 (k_2 \Delta T_2 - k \Delta T) = -3.3\,\Delta\, 10^5 \text{ dynes/cm for 1 } \mu \text{ (As)}SiO_2 \text{ at } 1050^\circ C$$

Both terms contribute with the <u>same</u> sign, indicating that this double layered system has about 50% <u>greater</u> induced strain at 1050°C than the simple Si_3N_4 system. It must be noted, however, that the increased strain on the GaAs induces the same stress on the 1000 Å Si_3N_4 layer as is induced without the arsenic doped oxide. The net improvement of this encapsulation system is that it increases the effective maximum tearing stress of the combined encapsulating layer more than it increases the total stress. This suggests that a possible improvement would be to find a different second layer or possibly a third encapsulating layer that would help to compensate the stress in the cap, thus obviating the need for increasing the maximum tearing stress and possibly reducing the number of strain induced defects in the substrate.

4.5 CONCLUSIONS

A chemically inert double layered encapsulation system has been developed which improves the electrical performance of annealed ion-implanted layers as well as allows for annealing at temperatures up to 1100°C. A similar system of phosphorous doped SiO_2 on top of Si_3N_4 has also been successfully applied to the high temperature annealing of ion-implanted InP.[22] This is an indication of the possible widespread application of multilayered systems for encapsulating compound semiconductors in general.

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CHAPTER 5

THE USE OF GALLIUM SULFIDE THIN FILMS AS ENCAPSULANTS FOR SULFUR-IMPLANTED GALLIUM ARSENIDE

Ion implantation causes crystal damage which must be annealed before desirable electrical properties can be obtained. With silicon, crystal annealing is straightforward because Si does not evaporate at typical annealing temperatures. However, with GaAs the situation is more complicated, since GaAs dissociates at 660°C, an unprotected GaAs surface will become pitted through thermal decomposition at temperatures above 660°C. However, thorough annealing of implantation-produced damage requires temperatures in excess of 750°C. Hence, it is necessary to encapsulate an implanted GaAs surface prior to the annealing cycle.

Several encapsulants have been proposed (the more common being SiO_2 and Si_3N_4). While most of these encapsulants can prevent, or at least minimize, surface deterioration of GaAs and are successful in retaining implanted Se and Te within the GaAs, they usually do not prevent sulfur outdiffusion. In particular, SiO_2 prevents As evaporation but is known to dissolve both Ga and S. Si_3N_4 (with low residual oxygen content) prevents both As and Ga outdiffusion. However, we were able to detect S outdiffusion in GaAs encapsulated with Si_3N_4 using both Auger measurements and Van Der Pauw measurements.

It will be clear from this discussion that the ideal cap is one that prevents As evaporation and does not dissolve either Ga or S. A reasonable encapsulant to try for this purpose was Ga_2S_3. In fact, use of Ga_2S_3 has been suggested as a method for the diffusion doping of donor sulfur into GaAs. We, therefore, chose to investigate Ga_2S_3 as an encapsulant for sulfur-implanted GaAs.

We found that the use of Ga_2S_3 (coated with a layer of sputtered SiO_2) as an encapsulant can result in excellent surfaces after annealing, and that it also succeeds in preventing sulfur outdiffusion. Hall effect

measurements made on implanted, annealed samples indicate a high electrical conversion of the implanted sulfur. Furthermore the resulting mobilities are high (3000 $cm^2/V\text{-}S$).

Profiling of the implanted, annealed samples shows the presence of a thin highly conductive layer below the surface, with a tendency of the sulfur to diffuse towards the surface. Sulfur that has diffused into the GaAs substrate from the Ga_2S_3 encapsulant was shown to be insignificant, and can be distinguished from the implanted sulfur for doses of $10^{13}/cm^2$ or higher.

In the sections to follow we will present a discussion of techniques used in this study and a summary of results obtained using Ga_2S_3 encapsulants.

5.1 EXPERIMENTAL PROCEDURE

5.1.1 Sample Preparation

Gallium arsenide materials used in this study were boat grown samples doped with Cr to a concentration of $10^{15}/cm^3$ and high purity vaporphase epitaxial material ($\simeq$ 10 um thick) grown on semi-insulating (100) orientation GaAs substrates. Etch pit counts were obtained on a number of samples to obtain information on the dislocation content near the surface. However, to provide a more thorough characterization, transmission electron microscopy (TEM) was used to select material suitable for implantation experiments. In all cases, we found that the quality of available GaAs was often extremely variable and routine screening procedures were essential.

After cutting wafers into 5 mm $\times$ 5 mm squares the samples were carefully cleaned before additional processing. Steps in the cleaning procedure were as follows:

1) Rinse in trichloroethylene (TCE)
2) Gently scrub with cotton swab immersed in TCE
3) Rinse in acetone
4) Rinse in deionized (DI) water
5) Rinse in methanol
6) Rinse in DI water
7) Dip in HF for 10 seconds
8) Rinse in DI water
9) Dip in warm HCl
10) Rinse in DI water
11) Blow dry with N_2.

5.1.2 Ion Implantation

The machine used for ion implantation consisted of a monoenergetic (10 keV) focussed source of positive ions, a mass separator, a deflection system and a high voltage (0 to 60 KV) target.[1,2] The source pressure was commonly maintained at approximately 3×10^{-6} Torr and target chamber pressure between 10^{-6} and 10^{-7} Torr.

When S ions were desired, H_2S gas was leaked into the system through the gas inlet at a rate sufficiently slow enough to maintain a pressure of 5×10^{-6} Torr. HS+ ions were implanted rather than S+ to avoid any possible contamination by O_2+. In separate experiments solid sulfur was used as a source and H_2 gas for the discharge. The H_2 continuously reacted with S to form H_2S which was subsequently ionized to form H_2S+, HS+ and S+.

For these studies, we constructed a Faraday cup to obtain more reliable measurements of beam current within the target chamber. Construction details are shown schematically in Figure 16 and the equivalent circuit in Figure 17. Grid 1 has a smaller diameter than the cup to insure adequate collection by the unit. Grid 2 is used for collection of secondary ions and Grid 3 is employed in electron suppression. It was found that electron suppression could be neglected and a 300 V battery provided sufficient bias for collection of secondary ions.

Implantations were done on substrates maintained at a temperature of approximately 360°C. After implantation was completed, the samples were allowed to cool to a temperature of 100°C at a rate of 6°C/min.

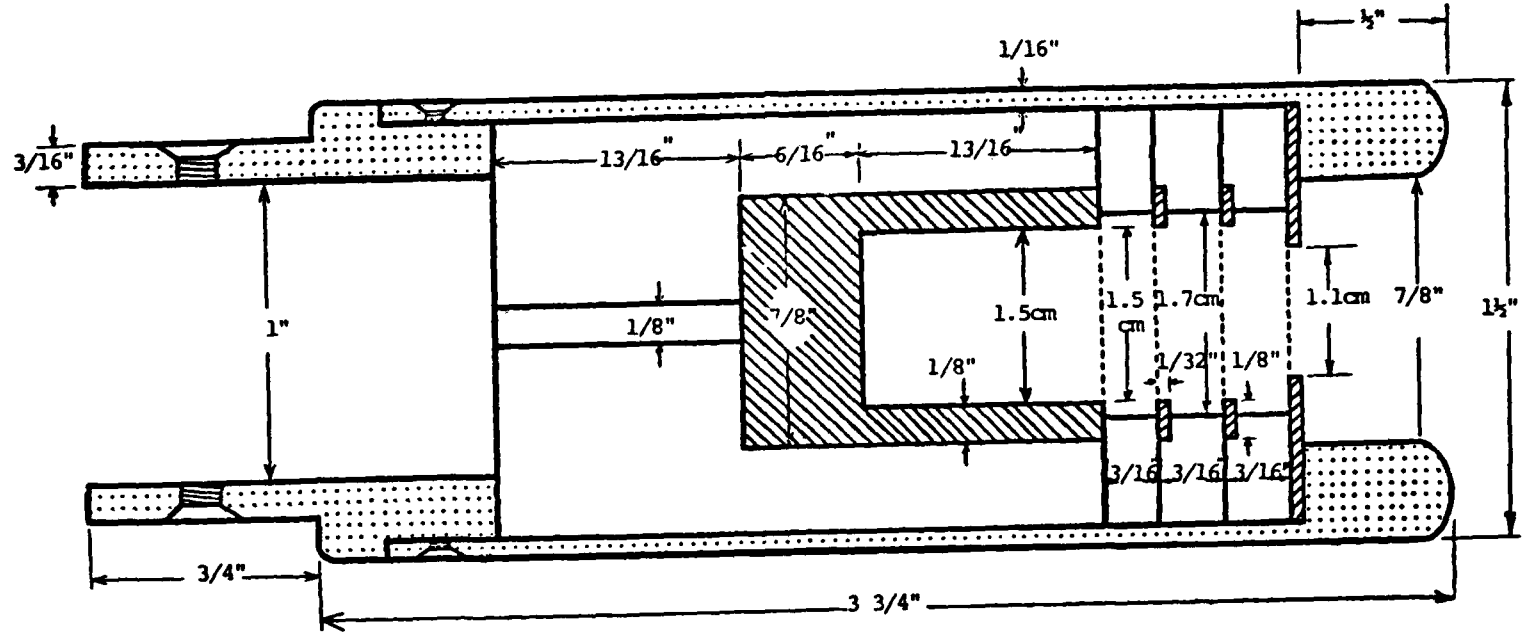

Figure 16. Faraday Cage

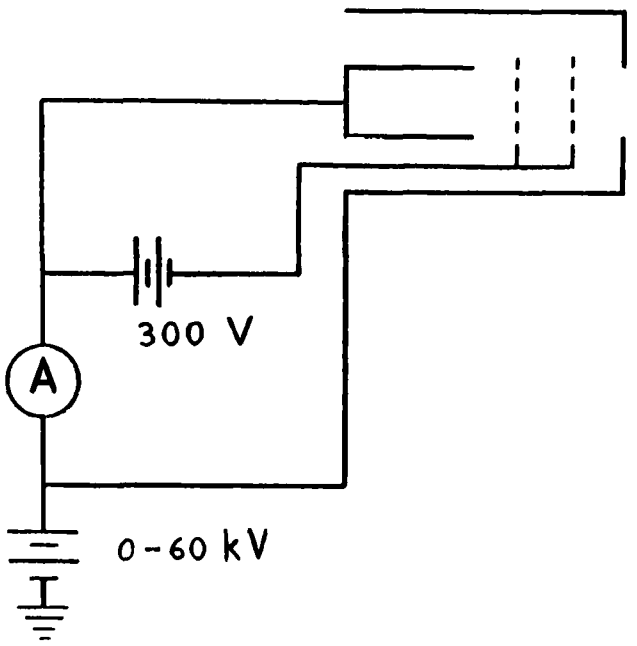

Figure 17. Electrical Schematic for Faraday Cage.

5.1.3 Encapsulation

For this study, the sample surfaces were protected during annealing by two thin films deposited on the substrate. A 6000 Å thick layer of high purity (5N) Ga_2S_3 was evaporated on the surface from a molybdenum boat, followed by deposition of a 2000 Å thick sputtered SiO_2 layer. The purpose of the SiO_2 overlayer was to prevent or reduce decomposition of the Ga_2S_3 film. Ga_2S_3 has a melting point of 1200°C, and in principle, an SiO_2 layer would not be required in the present experiments where substrate annealing temperatures are less than 900°C. However, during evaporation of the Ga_2S_3 layer it was observed that decomposition occurred, resulting in the deposition of S and Ga_2S, in addition to Ga_2S_3. Since Ga_2S decomposes at 800°C, an SiO_2 layer is required to prevent degradation of the encapsulant. To obtain lateral homogeneity and to reduce the concentration of Ga_2S within the layer, we found that an evaporation time of $\simeq$ 1 hr. for Ga_2S_3 films was optimal.

In comparative experiments, Si_3N_4 layers were formed by plasma deposition on substrates heated to temperatures of in the range 200°C to 400°C. The oxygen concentration in the Si_3N_4 films was critical in terms of preventing Ga outdiffusion and experiments showed that the amount of included oxygen should be less than 1% for annealing at temperatures in the range 800°C to 900°C and less than 0.1% for temperatures greater than 900°C. In all cases, we used low oxygen content films of refractive index $\gtrsim$ 2.00.

5.1.4 Hall Effect Measurements

Conventional Van Der Pauw geometries were used for making Hall effect measurements. The procedure used in making the required cloverleaf pattern is outlined in the following steps:

1) Spin on two coats of Shipley 1360B Resist at 5000 rpm for 30 sec.

2) Prebake for 10 minutes at 85°C

3) Align Van De Pauw mask over sample under microscope

4) Expose to ultraviolet light for 30 sec.

5) Develop in an agitated 1:1 solution of H_2O: Shipley AZ Developer for 1 min.

6) Rinse with DI water and blow dry with N_2

7) Postbake for 30 to 60 min. at 125°C.

8) Etch exposed semiconductor surface in a 1:1:160 solution of (H_2SO_4:H_2O_2:H_2O) to a depth $\simeq$ 10 times that of the implanted layer (rate $\simeq$ 200 Å/min)

9) Rinse thoroughly with DI water and blow dry.

10) Remove resist by soaking in acetone or Shipley Remover 1112

11) Rinse with TCE followed by immersion in acetone, DI water, and methanol; rinse again in DI water and blow dry with N_2.

Low resistance contacts were formed by evaporation of an 88% Au-12% Ge alloy, followed by deposition of pure Au. Alloying was done at 475°C for 4 minutes in flowing forming gas.

Resistivity and Hall effect measurements were made in the dark at room temperature. A battery powered current source was used and normally set at 100 nA. The current was monitored on a digital ammeter and voltage measurements made with a Keithley digital voltmeter. A precision magnet was used to provide a field strength of 2500 gauss.

The sheet resistivity, R_s, was calculated from the expression:

$$R_s(\Omega/\square) = 4.53 \frac{V_1 - V_2}{2I} \cdot f\left(\frac{V_1}{V_2}\right)$$

where V_1, V_2 are voltages measured on the Van Der Pauw pads, I is the current and $f\left(\frac{V_1}{V_2}\right)$ is a factor[3] defined by the ratio (V_1/V_2). Similarly, the effective mobility, μ_{eff}, and sheet carrier concentration, N_s, were calculated using the equations:

$$\mu_{eff}\ (cm^2/V\text{-}sec) = \frac{V_{H1} - V_{H2}}{2I} \Big/ (10^{-8}\ R_s \cdot B)$$

$$N(cm^{-2}) = \frac{1}{q\mu_{eff}R_s}$$

where V_{H1}, V_{H2} are Hall voltages, B is the magnetic field strength, and q is the charge on an electron.

To obtain profiles of carrier concentration and mobility as a function of depth in the substrate, it was necessary to strip uniform thin layers of material from the material without damaging the metal contacts. We found that an agitated 1:1:160 solution of H_2O_2:H_2SO_4:H_2O would not attack the contacts and provided a relatively uniform etch rate of $\simeq$ 200 Å/min. However, due to substrate variability, we found it necessary to provide an etch rate calibration for each sample profiled. For this purpose, we used a control sample subjected to the same processing and annealing conditions and simultaneously etched both the control and Van Der Pauw samples. The step height on the control sample was then measured on a Talystep instrument and the removal rate inferred for the Van Der Pauw sample.

If N_i, (μ_{eff}), and (R_s), represent respectively, the sheet carrier concentration, effect mobility and sheet resistivity at depth, d_i, and N_{i+1}, $(\mu_{eff})_{i+1}$ and $(R_s)_{i+1}$, the same terms at depth, d_{i+1}, then it can be shown that:

$$n_i = \frac{N_i - N_{i+1}}{d_{i+1} - d_i}$$

$$u_i = \frac{\frac{(\mu_{eff})_i}{(R_s)_i} - \frac{(\mu_{eff})_{i+1}}{(R_s)_{i+1}}}{\frac{1}{(R_s)_i} - \frac{1}{(R_s)_{i+1}}}$$

where n_i and μ_i are the carrier concentration and mobility at depth, $\frac{d_i + d_{i+1}}{2}$. Using these equations, we obtained profiles on implanted, annealed samples at incremental depths into the substrate.

5.2 EXPERIMENTS WITH S-IMPLANTED GaAs

For impurities implanted in GaAs to become electrically active, annealing temperatures in excess of 700°C are required. Unfortunately, at annealing temperatures exceeding 660°C, an unprotected GaAs surface deteriorates due to thermal decomposition and loss of As.[5] In the earliest studies of ion implanted GaAs, SiO_2 was typically used as the encapsulant to prevent deterioration of the semiconductor surface, although Si_3N_4 has been commonly used by investigators over the last five years.

5.2.1 Silicon Dioxide Caps

In an earlier investigation of S-implanted GaAs samples at Stanford University, Sansbury[1] used SiO_2 as an encapsulant. He implanted 70 keV S-ions ($10^{15}/cm^2$) into GaAs substrates maintained at 20°C. Carrier concentration profiles are shown in Figure 18 for implanted samples annealed at 700°C for periods between 3 and 120 minutes. In all cases, we observe that the resulting electrical activities are low (less than 0.4%). The electrical activity initially decreases as a function of annealing duration, subsequently remains approximately constant and finally decreases further. In addition, the width of the carrier concentration profile decreases and the maxima are displaced toward the surface of the GaAs. The data clearly indicate S is outdiffusing from the substrate and that SiO_2 is not an effective encapsulant for S-implanted GaAs. Furthermore, it has been shown recently that Ga dissolves readily in SiO_2, Si indiffuses at temperatures less than 900°C, and film degradation is present at higher temperatures, providing additional complications in using an SiO_2 encapsulant.

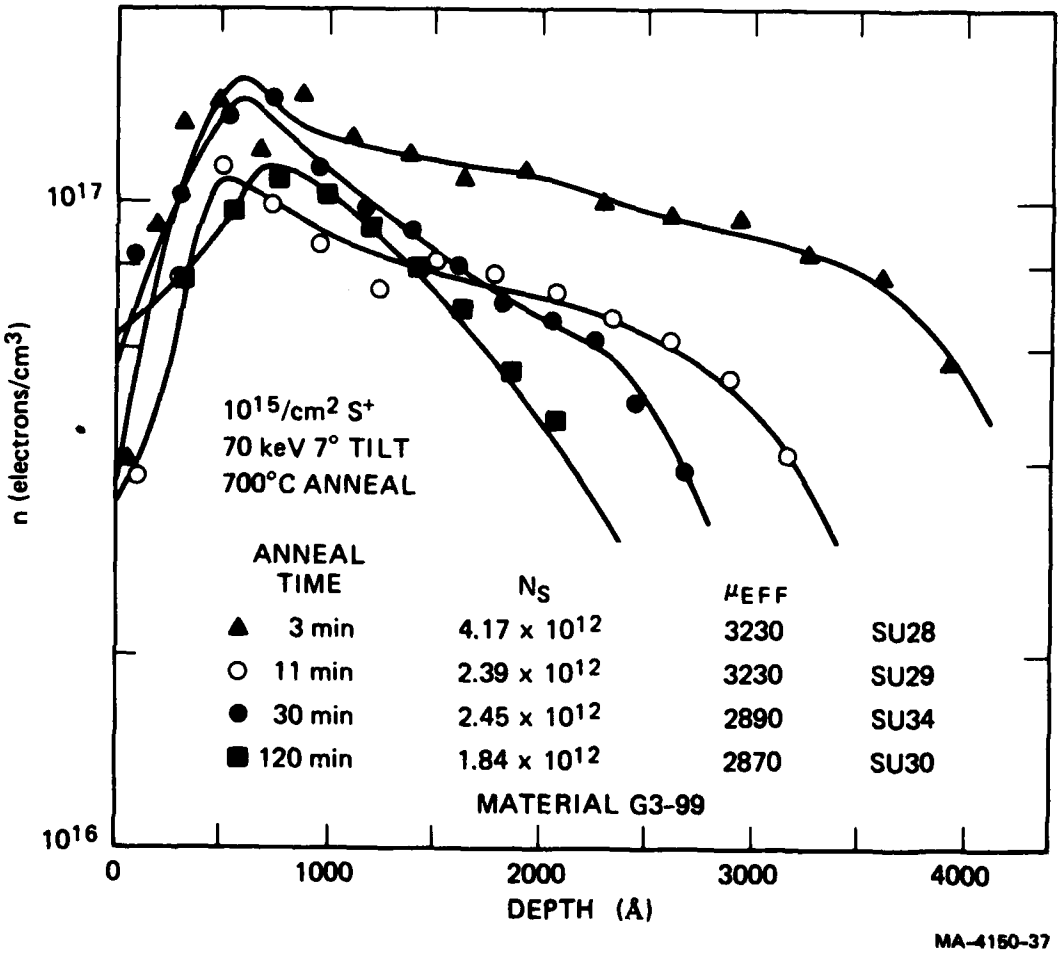

Figure 18. Carrier Concentration Profiles for S-Implanted Samples Annealed at 700°C Using an SiO_2 Encapsulant.

5.2.2 Silicon Nitride Cap

Initial investigations by researchers concentrated on the use of sputtered or CVD Si_3N_4 films where the substrate was exposed to excessively high temperatures during the deposition process. We felt that an alternative approach should be attempted using a low temperature film deposition process to avoid the problems reported in the past.

We began a development program to characterize plasma deposited Si_3N_4 films grown at substrate temperatures in the range 200 to 400°C. The most stable films were obtained at deposition temperatures of 200°C and 300°C. Our results indicated that surface cleanliness was extremely important for obtaining stability during deposition and after annealing. A thin natural (30 Å thick) gallium oxide layer would cause surface deterioration at 400°C deposition temperatures and significant surface breakdown and Ga outdiffusion through all films after annealing at temperatures less than 900°C.

The silicon-to-nitrogen ratio required very careful control to avoid the development of pinholes and microscopic defects. Of particular significance was the observed dependence of oxygen concentration on Ga outdiffusion. In comparative experiments on our films and CVD films prepared by others, Auger profiling analyses showed oxygen levels $\gtrsim 1\%$. In all cases, we observed Ga outdiffusion to the surface of the nitride film on encapsulated samples annealed up to 900°C.* To reduce Ga outdiffusion it was found that the oxygen concentration in the nitride should be less than 1% for substrate anneal temperatures $\leq$ 900°C.

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*Further development and improvement of plasma deposited Si_3N_4 and double layer, SiO_2/Si_3N_4 films is discussed in a separate paper.

To evaluate the effectiveness of low oxygen content Si_3N_4 films an annealing caps, we implanted 120 keV S-ions to a dose of $10^{13}/cm^2$ at a substrate temperature of 300°C. The samples were then encapsulated and annealed in forming gas at 900°C for ½ hour. The resulting electrical activity (Figure 19) was low (≃ 7%). At depths greater than 500 Å the electrically conducting layer was exhausted. The profile shows a high carrier concentration near the surface but drops rapidly to the background doping level of the substrate. The accumulation of carriers within the first 500 Å and the displacement of the peak carrier concentration suggests that either S is diffusing toward the surface and most of the implanted ions have become electrically inactive or S has outdiffused into the nitride cap.

To further evaluate the possibility of S outdiffusion into the Si_3N_4 cap, we did Auger profiling analyses on samples implanted to a dose of $10^{15}/cm^2$ at a substrate temperature of 325°C. The samples were then encapsulated with a 1000 Å thick Si_3N_4 layer and annealed in flowing H_2 for 15 minutes. The results repeatedly showed traces of S into the nitride at distances up to 150 Å from the interface, indicating outdiffusion of S from the substrate.

These observations were later confirmed by Eisen in a series of experiments on S-implanted GaAs. His investigations were done on 100 keV S-implanted ($10^{13}/cm^2$) samples which were capped with silicon nitride (containing oxygen) and subsequently annealed at 850°C for ½ hour. Radio-tracer techniques were used to obtain impurity profiles within the cap and substrate. The results (Fig. 20) indicated that 75% of the implanted S had diffused into the cap, 15% was within 150 Å of the surface and 10% was beyond 150 Å.

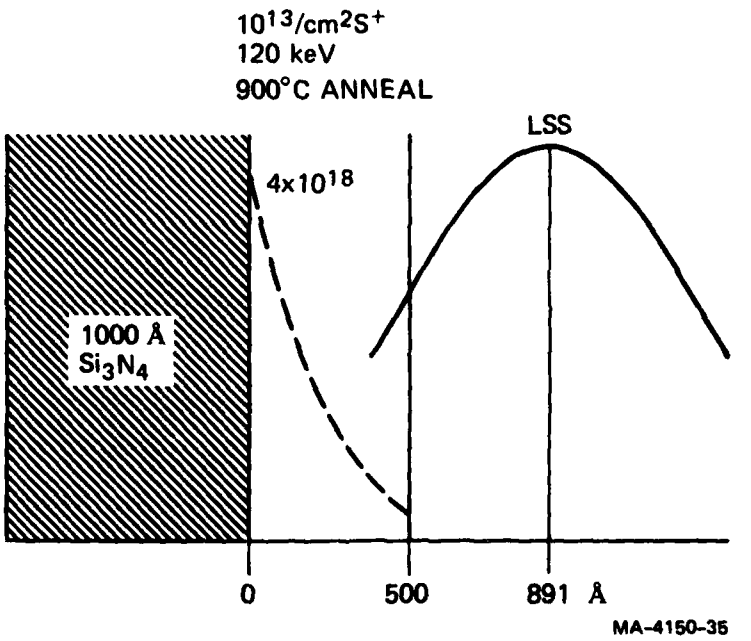

Figure 19. Carrier Concentration Profile of S-Implanted Sample Annealed at 900°C for 0.5 Hour Using Si_3N_4 Encapsulant.

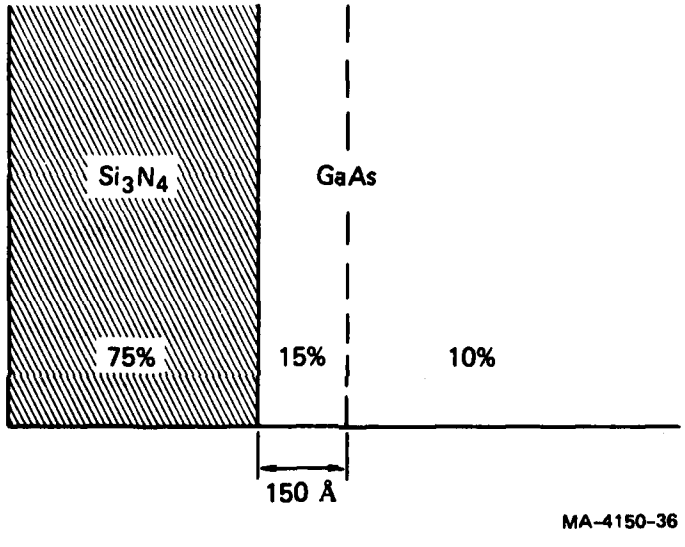

Figure 20. Schematic of Experimental Results Obtained by Eisen Showing Concentrations of S in Encapsulant and Substrate (Reference 8).

Based on our early results, which were later verified by Eisen, we conclude that the outdiffusion of S into the nitride cap is responsible for the low electrical activity.

5.2.3 Gallium Sulfide as an Encapsulant

From the previous experiments, we observed that an SiO_2 encapsulant prevents As evaporation but dissolves both Ga and S. Similarly, an Si_3N_4 encapsulant prevents As evaporation, and with low oxygen content in the nitride does not dissolve Ga, but dissolves S. The results suggest that further development and improvements are required on the nitride caps to reduce the S-outdiffusion.

Ideally, an encapsulant for S-implanted samples must prevent loss of As and not dissolve Ga or S. Since gallium sulfide contains both Ga and S, it seemed conceivable that a Ga_2S_3 cap might provide a suitable outdiffusion barrier. The annealing temperature could be made low enough to produce a small indiffusion component from the cap, but high enough to yield good electrical conversion of the implanted S.

In a previous study, Asai and Kodera[6] proposed using Ga_2S_3 as a sulfur diffusion source for GaAs. This method utilizes solid-solid redistribution and diffusion between GaAs and Ga_2S_3 below the eutectic temperature ($\simeq$ 940°C) of the quasi-binary Ga_2S_3-GaAs system.

If we assume the surface concentration of S in GaAs to be independent of time and bulk doping, and if we further assume that the diffusion coefficient is constant for a given temperature, then the resulting concentration profile of indiffused S can be described by a complementary error function with a diffusion coefficient, D, and a surface concentration, C_s. From the graph of D and C_s as a function of temperature (Figure 21), we observe that a reduction in temperature from 825°C to 750°C results in a reduction of the diffusion coefficient from $\simeq 10^{-13} cm^2/s$

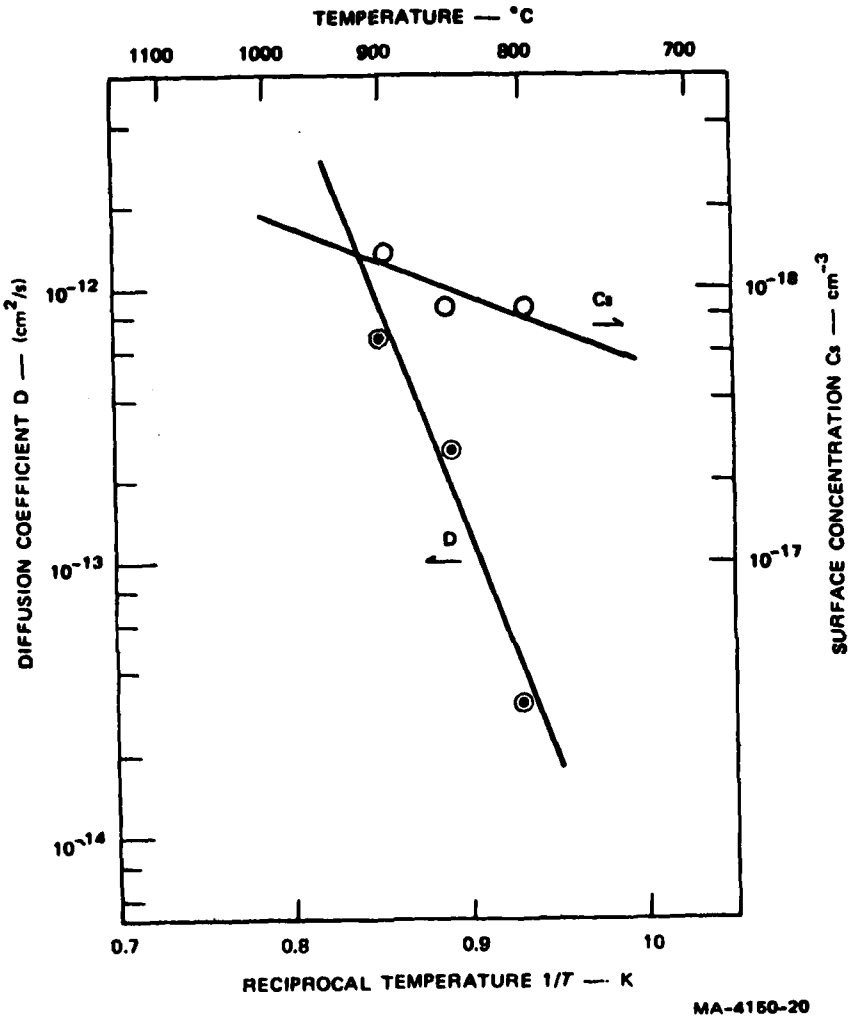

Figure 21. Diffusion Coefficient, D, and Surface Concentration, C_s, of Active Donor, S, in GaAs versus Reciprocal Temperature (Reference 6).

$\times$ to $6 \times 10^{-12} cm^2/s$, or by a factor of $\simeq 17$. Therefore, if Ga_2S_3 is used as an annealing cap for ion implanted samples and the effects of residual implantation damage do not produce a large enhancement of diffusivity, the annealing temperature can be chosen to produce little indiffusion from the cap.

In the first set of experiments we implanted 60 keV S ions into lightly doped p-type epitaxial layers on semi-insulating GaAs substrates maintained at 360°C during implantation. Similar experiments were done using S implants into semi-insulating Cr-doped GaAs. For comparative purposes and to determine the effect of damage on S diffusion from the cap, we did stoichiometric Ga + As dual ion implants to simulate the damage created by S-implantation. In all cases, the samples were encapsulated with 6000 Å of evaporated Ga_2S_3, followed by 2000 Å of sputtered SiO_2. Annealing was done at 825°C for 10 minutes in flowing H_2.

The data obtained from electrical measurements on these samples are shown in Table 6 and Figure 22. We observe that the resulting sheet resistivities are low, but the average mobility ($\simeq$ 3000 cm^2/V-sec) is high. The electrical activities are high and consistent with what would be expected from a cap that does not dissolve S when we account for the degeneracy effects[7] that arise in GaAs whenever the doping concentration exceeds $10^{17}/cm^3$. From Table 6, we observe that the data obtained on both types of samples are in relatively good agreement, except for the $10^{13}/cm^2$ dose. This difference at $10^{13}/cm^2$ could be related to variations in stoichiometry of the evaporated Ga_2S_3 layer, resulting in a sulfur rich film in one case and more indiffusion from the cap.

In Figure 22, the sheet carrier concentration profile for the stoichiometric Ga + As implanted sample is approximately the same as the non-implanted control sample. Apparently, the damage that otherwise would

TABLE 6. SUMMARY OF ELECTRICAL DATA ON S-IMPLANTED SiO_2/Ga_2S_3 CAPPED SAMPLES ANNEALED AT 825°C

Implant energy 60 keV

Implant temperature 360°C

Encapsulant 6000 Å evaporated Ga_2S_3
2000 Å sputtered SiO_2

Anneal 825°C, 10 min. flowing N_2

Run #1 Semi-insulating GaAs with lightly doped (10^{14} cm^{-3})p-type epitaxial layer

Implant	ρ	μ	N (cm^{-2})	% active
10^{12}S	1450	4900	8.8×10^{11}	88
10^{13}S	520	2000	6.0×10^{12}	60
10^{14}S	93 105	3700 3700	1.8×10^{13} 1.6×10^{13}	18 16
10^{15}S	111 102	2900 3300	1.94×10^{13} 1.87×10^{13}	1.94 1.87

Run #2 Semi-insulating Cr-doped GaAs

Implant	ρ	μ	N (cm^{-2})	% active
10^{13}S	170 184	3600 3590	1.02×10^{13} 9.4×10^{12}	102 94
10^{14}S	153 139 104	2620 2690 2480	1.6×10^{13} 1.8×10^{13} 2.2×10^{13}	16 18 22
10^{15}S	139 123	2720 3070	1.65×10^{13} 1.65×10^{13}	1.65 1.65
no implant	297	3110	$N = 6.8 \times 10^{12} cm^{-2}$	
10^{14}(Ga+As)	307	3010	$N = 6.8 \times 10^{12} cm^{-2}$	

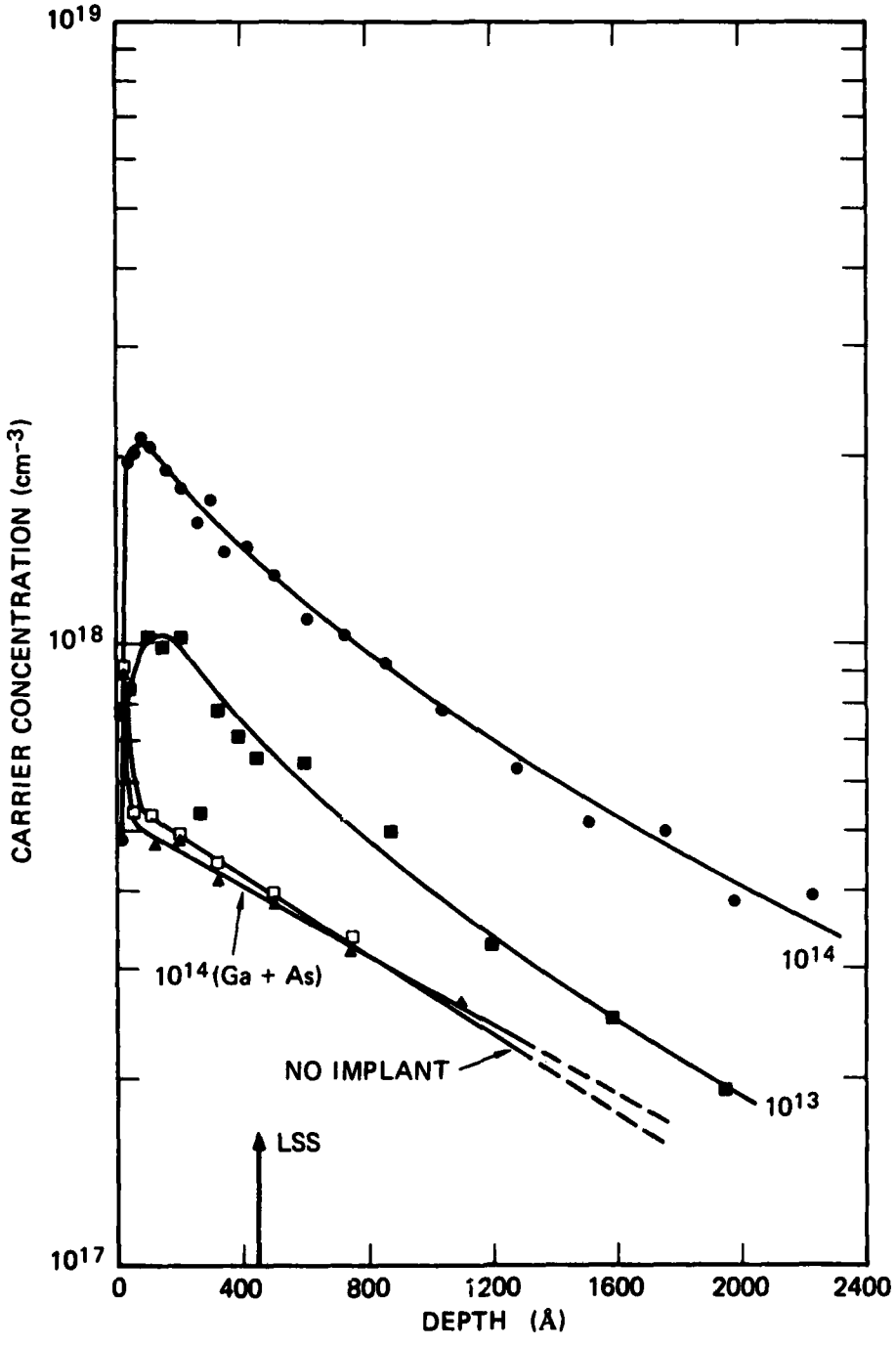

Figure 22. Carrier Concentration Profiles for Samples Annealed at 825°C for 10 Minutes.

have enhanced S diffusion from the cap has been annealed during the hot implant at 360°C. In comparison to the results obtained from samples implanted to doses of 10^{13} and $10^{14}/cm^2$, the carrier concentrations are significantly lower for the control samples. Hence, the contribution of excess carriers by indiffusing S can be identified. For both the 10^{13} and $10^{14}/cm^2$ implants, we observe a tendency for the implanted S to diffuse toward the surface, away from the predicted LSS distribution. However, the S stays within the samples as reflected in the high electrical activities recorded and some indiffused S from the cap may actually be contributing to the carrier concentration profile.

To reduce the amount of S indiffusion from the cap and to restrain the indiffusing component to a thin near surfaces regions, we implanted 60 keV S ions into lightly doped n-type epitaxial layers grown on semi-insulating GaAs substrates and annealed the capped samples in forming gas at 750°C for ½ hour. All processing conditions were identical to those used in the previous experiments, except that sputtered Ga_2S_3 was used instead of evaporated Ga_2S_3.

Electrical data obtained in these experiments is shown in Table 7 and Figure 23. Comparing the electrical activities reported in Tables 6 and 7 for samples implanted to similar dose levels, we observe that the efficiency is lower for samples annealed at 750°C, implying a reduction in the conversion of implanted S. However, in Figure 23 we observe that the amount of indiffused S from the annealed control sample is considerably less than in previous experiments. In addition, the S-diffusion profile is much narrower and confined to a region ≃ 600 Å from the surface compared to a width of ≃ 2000 Å observed previously. The indiffused S in this case appears to exert a negligible influence on the concentration profile of the implanted S.

TABLE 7. SUMMARY OF ELECTRICAL DATA ON S-IMPLANTED SiO_2/Ga_2S_3 CAPPED SAMPLED ANNEALED AT 750°C

Implant energy: 60 keV

Implant temperature: 360°C

Encapsulant: 6000 Å sputtered Ga_2S_3
2000 Å sputtered SiO_2

Annealing: 750°C, 1/2 hr, N_2

Material used: semi-insulating GaAs with a lightly doped ($10^{14}cm^{-3}$) n-type epi layer.

Implant	ρ(Ω/)	μ(cm^2/v-s)	N (cm^{-2})	% active
5 x 10^{13} S	220	2780	10^{13}	20
	380	1870	8.9 x 10^{12}	18
no implant	1900	3700	8.8 x 10^{11}	

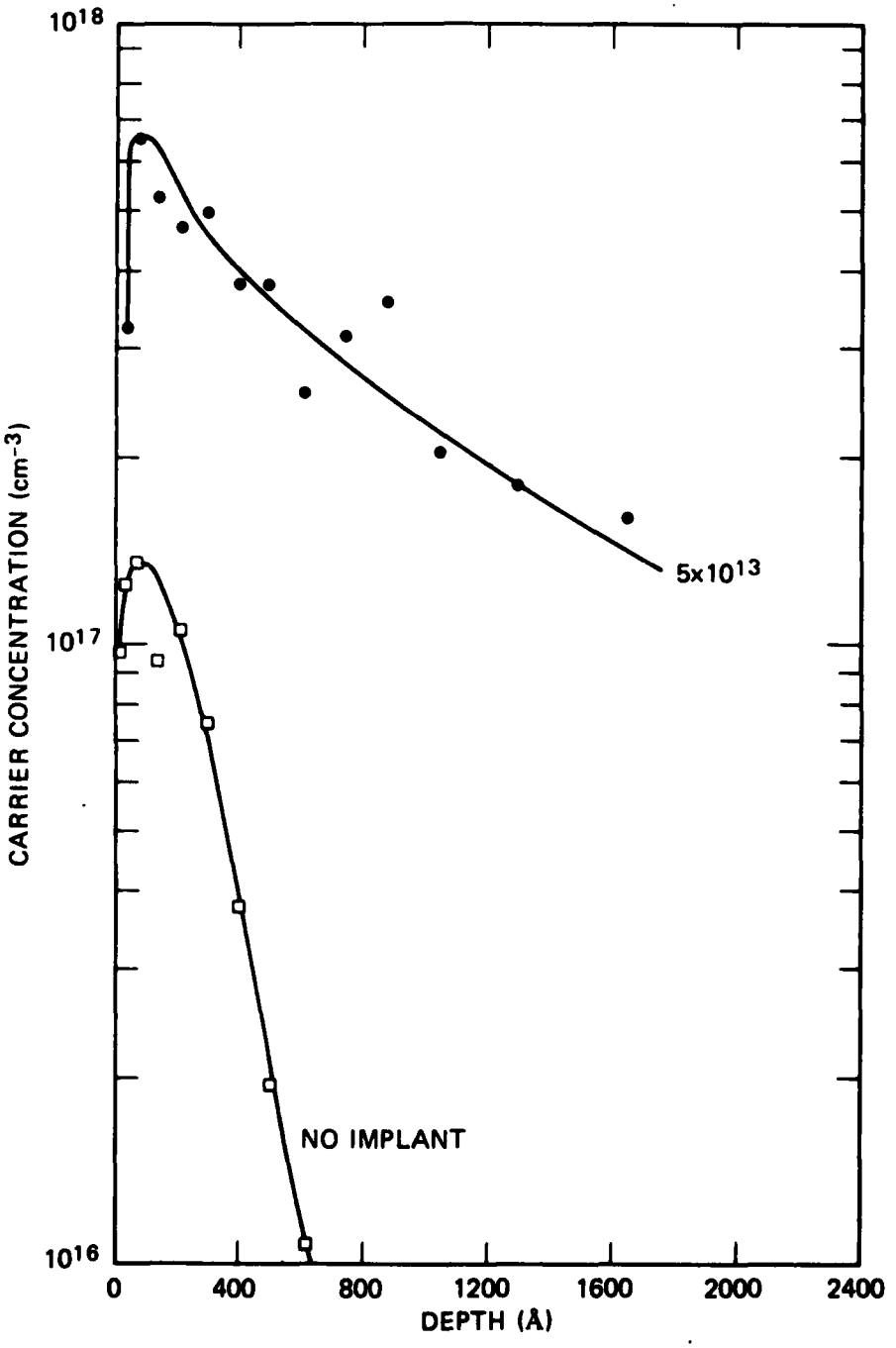

Figure 23. Carrier Concentration Profiles for Samples Annealed at 750°C for 30 Minutes.

5.3 CONCLUSIONS

In this study, we have successfully developed and characterized a two layer SiO_2/Ga_2S_3 encapsulant for annealing S-implanted GaAs samples. The results of these experiments have been compared to similar tests done on both SiO_2 and Si_3N_4 encapsulants. In general, the Ga_2S_3 caps appear stable at high temperatures and no noticeable deterioration or surface pitting was observed at temperatures up to 825°C. At these temperatures, S indiffusion from the cap is small and can be neglected for samples implanted to doses greater than $10^{13}/cm^2$. Experiments on control samples indicate that radiation damage created by the implantation of S ions has no apparent effect on enhancing indiffusion of S from the cap. The double layer SiO_2/Ga_2S_3 cap is successful in preventing S outdiffusion from the GaAs substrate, as reflected by the high electrical activities after annealing. However, electrical profiling data indicate that the implanted S tends to diffuse toward the surface, although outdiffusion is apparently absent or minimized. In all cases, Hall effect measurements indicate high average mobilities ($\simeq$ 3000 $cm^2/V\text{-sec}$) after implantation and annealing.

5.4 REFERENCES (CHAPTER 5)

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CHAPTER 6

THERMAL AGING OF Al THIN FILMS ON GaAs*

Aluminum thin films are used for the gate contact in GaAs-based Schottky-barrier field effect transistors[1] and have recently been proposed as an encapsulant for annealing radiation damage in ion-implanted GaAs.[2,3] In the first application, the Al-GaAs system need not be subjected to high temperatures, but in the second, the system must be exposed to temperatures of at least 700°C to achieve appreciable electrical activity in donor-implanted GaAs.[2,4] To be a useful encapsulant the Al layer should provide a barrier to the out-diffusion of dopant impurities and host atoms from the substrate and not significantly in-diffuse at the temperatures required for damage annealing. Given the propensity for solid-phase reactions in metal-semiconductor systems,[5] the Al-GaAs system would be unique if no significant interdiffusion or phase formation occurred at temperatures approaching the melting point of Al (660°C). This paper presents experimental results from an investigation of the electrical and structural properties of thermally aged Al thin films on GaAs.

The effect of thermal aging on the electrical and metallurgical properties of several metals, other than Al, on GaAs has been investigated. Annealing of Au films on GaAs at temperatures of 250°C and above results in the diffusion of Au into GaAs and the formation of a disordered region near the surface of the substrate.[6,7] This is accompanied by the out-diffusion of Ga through the Au film to the exposed surface, a reduction in the Schottky barrier height from 0.9 to $\sim$ 0.6 eV, and an increase in the ideality parameter from 1.0 to $\sim$ 1.2. Detailed microstructural examination of alloyed Au films on GaAs revealed several distinct damage zones within the substrate that were characterized by the presence of hexagonal AuGa, dislocation lines, and Au precipitation.[8] In the Pt-GaAs system,[7] a rapid out-diffusion of Ga into Pt at 500°C leads to the formation of a layered structure with PtGa present in the outer layer and $PtAs_2$ adjacent to the GaAs substrate; the barrier height increases from 0.84 eV in as-prepared contacts to 0.90 eV after aging at 500°C (2 h, *in vacuo*).

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*J. Vac. Sci. Technol., Vol. 13, No. 4, July/Aug. 1976.

In contrast to the above metal-GaAs systems, the W-GaAs interface is metallurgically inert up to 500°C with only a slight increase in the barrier height from 0.65 to 0.67 eV after a 500°C anneal (2 h, *in vacuo*).[7] These metal-GaAs structures illustrate both the variety of alloying behavior observable in these systems and the high sensitivity of the electrical characteristics to reactions occurring at the metal-semiconductor interface.

Several complementary experimental techniques were used to investigate thermal aging of Al thin films on GaAs. The surface topography of the annealed Al films was examined by optical and scanning electron microscopy. Electrical measurements were used to characterize thermally aged Schottky barrier contacts. Microstructural changes in the near surface region beneath the Al overlayer were analyzed by transmission electron microscopy (TEM), and chemical depth profiles of the Al-GaAs structure were obtained by combining Auger electron spectroscopy with *in situ* ion milling. The results of these studies were correlated to characterize thermally induced reactions in Al-GaAs structures.

6.1 SAMPLE PREPARATION

Samples were prepared from both epitaxially grown and bulk single-crystal GaAs. The epitaxial samples were used for electrical evaluation. The wafers consisted of a 5-μm-thick layer of *n*-type GaAs grown by vapor-phase epitaxy on (100)-oriented, Te-doped GaAs substrates. The carrier concentrations of the epitaxial layer and substrate were 4.6×10^{15} cm^{-3} and 2.0×10^{18} cm^{-3}, respectively.

Samples for microstructural and Auger analyses were prepared from both (100)-oriented and (310)-oriented bulk single-crystal GaAs. Substrates with (100) orientation were either nondegenerate *n*-type with a carrier concentration of 5×10^{16} cm^{-3} or heavy Zn-doped with a carrier concentration of 2×10^{18} cm^{-3}. The (310)-oriented material was *n*-type with a carrier concentration of 9×10^{16} cm^{-3}. Samples were prepared for TEM examination by jet-thinning from the unpolished face of the GaAs substrate, using an H_2SO_4-H_2O_2-H_2O solution.

In preparation for metallization, both epitaxial and mechanically polished bulk samples were cleaned in trichlorethylene, acetone, and propanol to remove organic contaminants. The samples were then immersed in concentrated HCl, rinsed in propanol, dried in flowing N_2, and immediately installed in a vacuum chamber. Aluminum films were deposited by evaporation from tungsten coils at a pressure of $\lesssim 2 \times 10^{-6}$ Torr (2.7×10^{-4} Pa) in a N_2-trapped diffusion-pump system. Film thickness was measured by optical interferometry. For electrical measurements, Au-Ge films were vacuum deposited onto the back surfaces of epitaxial GaAs substrates and alloyed (375°C, 1 h) to provide ohmic contacts; 0.030-in.-diam Al dots were deposited through a mask. Al was vacuum deposited on both surfaces of the GaAs substrates prepared for Auger analysis. All anneals were performed under vacuum at a pressure of $\lesssim 2 \times 10^{-6}$ Torr (2.7×10^{-4} Pa) with the samples placed in a molybdenum crucible.

6.2 RESULTS

6.2.1 Surface Topography

The surface topography of annealed Al films on GaAs was examined by optical and scanning electron microscopy. After an anneal at either 400° or 500°C for 1 h, the Al film was covered with an array of irregularly shaped erosion centers. Figure 24 shows optical micrographs of a 1250-Å film as-deposited and after an anneal at 500°C for 1 h. The erosion centers appearing in the annealed Al film are shown at higher magnification in Fig. 25. The largest of the erosion centers are nominally 7 μm in diameter, and it is estimated that the centers occupy $\lesssim$ 1% of the surface area. In Al films of the same thickness and annealed at 400°C for 1 h, the erosion centers are nominally 5 μm in diameter. Examination in a scanning electron microscope equipped with an energy dispersive x-ray analyzer revealed that the centers are crater-like depressions that expose the GaAs substrate. The erosion centers were observed in Al films deposited and annealed on both epitaxial and bulk single-crystal GaAs.

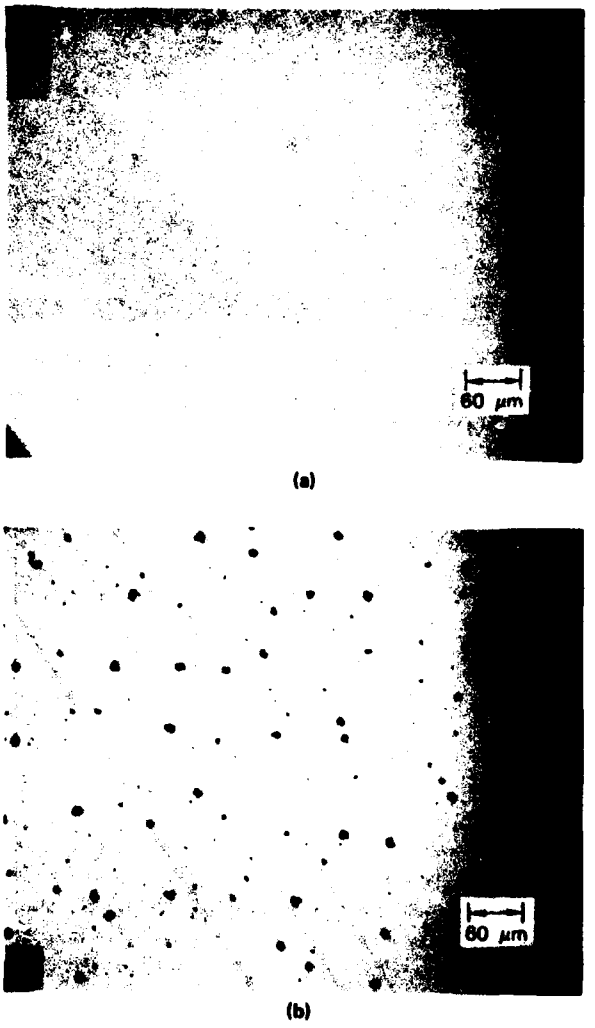

Figure 24. Optical Micrographs of a 1250-Å Al Film on Epitaxial GaAs (a) as Deposited and (b) After an Anneal at 500°C for 1 h *in vacuo*.

Figure 25. Optical Micrograph of a 1250-Å Al film on Epitaxial GaAs Shwoing the Erosion Centers Generated by a Vacuum Anneal at 500°C for 1 h.

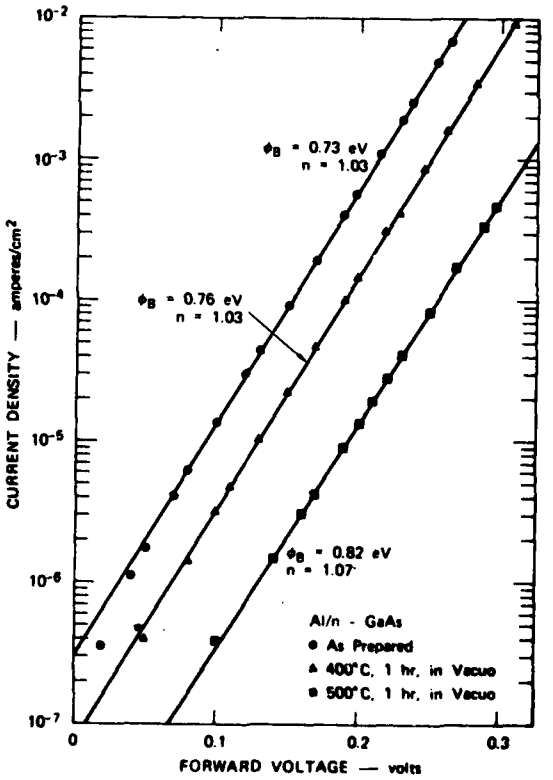

Figure 26. Dependence of Current Density on Forward Voltage for Thermally Aged Schottky Barrier Structures Consisting of Al Thin Films on *n*type GaAs.

6.2.2 Electrical Evaluation

Schottky-barrier measurements were used to detect thermally induced reactions occurring at the Al-GaAs interface. Specifically, forward current-voltage (I-V) measurements were made on Schottky-barrier contacts fabricated on epitaxial *n*-type GaAs. The characteristics for a representative set of samples are shown in Fig. 26. The current density is plotted as a function of forward voltage for an unannealed Al-GaAs contact and for contacts that were vacuum annealed at 400° and 500°C for 1 h.

The thermionic emission theory for charge transport in Schottky-barrier structures was used to analyze the data shown in Fig. 26.[9] Accordingly, the forward I-V characteristics can be described by the following equation:

$$J = 120(m^*/m)T^2\exp\left[-\phi B/kT\right] \times \{\exp\left[qVF/nkT\right] - 1\}, \qquad (1)$$

where J is the current density, m^* is the effective mass of the majority carriers, m is the free-electron mass, T is absolute temperature, ϕB is the energy barrier height, k is Boltzmann's constant, q is electronic charge, VF is the forward voltage, and n is the numerical parameter commonly termed the ideality factor. For electrons in GaAs at low electric fields, the effective mass is isotropic and $m^*/m = 0.068$.[9]

Application of Eq. (1) to the data presented in Fig 26 yields numerical values for the Schottky-barrier height, ϕB, and the ideality factor, n, for each of the I-V characteristics. The barrier height is observed to increase with anneal temperature from 0.73 eV in the as-prepared sample to 0.76 eV for the contact annealed at 400°C, and to 0.82 eV after a 500°C anneal; capacitance-voltage measurements[9] verified the observed increase in barrier height with anneal temperature. The ideality factor is approximately 1.03 for both the as-prepared contact and the contact annealed at 400°C and increases slightly to 1.07 after an anneal at 500°C.

6.2.3 Microstructural Analysis

Samples were prepared for TEM examination in the form of 3-mm-diam disks, which were jet thinned from the back face of the specimen. Figure 27 shows a representative dark-field transmission electron micrograph and selected-area diffraction pattern of a GaAs substrate from which a 1200-Å thick (as-deposited) Al film was removed after an anneal at 500°C for 2 h. Analysis of the diffraction pattern indicates the presence of Al within a near surface zone of the substrate. Dark-field electron micrographs obtained using reflections associated with Al diffraction spots show that Al is present in the form of precipitates within a zone $\lesssim$ 1000 Å from the GaAs surface. The average diameter of the precipitates is $\simeq$ 60 Å, and the apparent concentration is equal to 6×10^{15} cm^{-3}. In all cases the Al precipitation was confined to a shallow substrate zone beneath the Al-GaAs interface and was not present at depths greater than 1000 Å from the GaAs surface.

Reactions occurring at the Al-GaAs interface were investigated by depositing Al films onto prethinned GaAs substrates of (310) crystal orientation. The (310) orientation was chosen to reduce the number of diffraction spots from single-crystal GaAs that are nearly coincident with those of possible Al compounds. The Al-GaAs system was vacuum annealed at 575°C for 2 h. Selected-area transmission electron diffraction patterns were obtained with no additional surface treatment of the samples.

Figure 28 shows a representative diffraction pattern, and Table 1 compares experimentally measured "*d*" spacings with published ASTM values.[10] The analysis shows that the polycrystalline ring structure is associated with the presence of AlAs at the interface. Control experiments on unannealed Al-GaAs samples showed an absence of rings correlated with AlAs. In addition, uncoated GaAs samples subjected to similar annealing schedules have exhibited only the single-crystal spot diffraction pattern. The data then imply that the ring structure of the diffraction pattern is uniquely associated with the presence of AlAs crystallites at the interface.

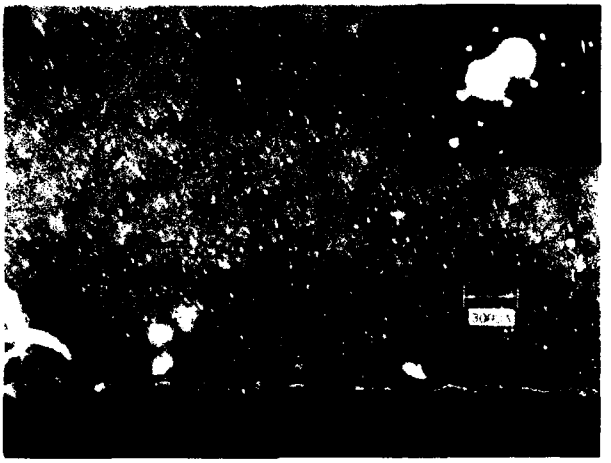

Figure 27. Dark-Field Transmission Electron Micrograph of a GaAs Substrate from which a 1200-Å thick (as deposited) Al Film was Removed after a Vacuum Anneal at 500°C for 2 h. Shown in the inset is a Selected-Area TED Pattern Obtained from the Same Substrate.

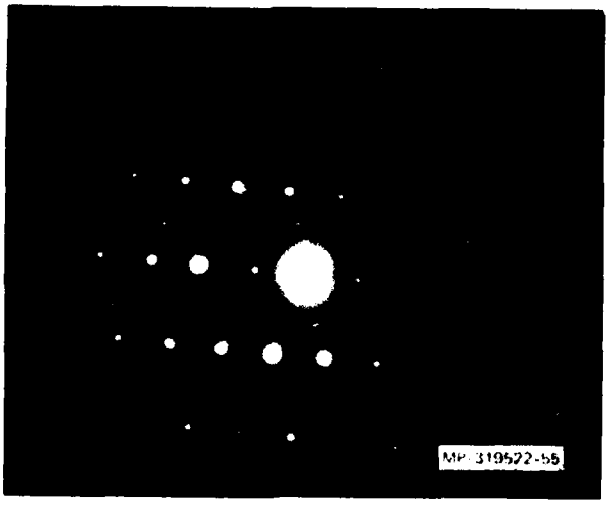

Figure 28. Selected-Area Transmission Electron Diffraction Pattern from an Al/GaAs Structure Vacuum Annealed at 575°C for 2 h.

6.2.4 Auger Analysis

Auger electron spectroscopy (AES), combined with *in situ* ion milling, was used to study thermally induced interdiffusion in the Al-GaAs system. The physical principles of AES and the application of the technique for surface chemical analysis and depth profiling are well established and will not be reviewed here.[11] In addition, the technique has been used to study interdiffusion in Au,[12] Ni/Au-Ge,[13] and Au-Pt[14] thin films on GaAs.

The Auger data were obtained by irradiating the sample surface with a 3-kV, 10-μA electron beam and monitoring the differential spectrum of the secondary electrons with a cylindrical mirror energy analyzer (Varian). The beam diameter at the surface of a sample was ∿ 50 μm. Chemical depth profiles were obtained by combining AES with *in situ* Ar-ion milling. The ion gun (Varian) provided a sputtering rate of ∿ 7 Å min^{-1} for as-deposited Al films at a static Ar pressure of 5×10^{-5} Torr (6.6×10^{-3} Pa) and ion energy of 600 eV. A standard semiquantitative formalism was used to analyze the Auger data.[11,15]

Figure 29 shows a representative chemical depth profile obtained from a 680-Å Al film on (100)-oriented, *n*-type GaAs after the sample had been vacuum annealed for 2 h at 500°C. Caution must be used in interpreting this profile in terms of thermally induced interdiffusion in the Al-GaAs structure because thermal aging results in the generation of erosion centers that expose the GaAs substrate. In Figure 29 it appears that Ga has diffused into the Al film after a 500°C anneal; in contrast, no Ga was detected in unannealed Al films. However, in samples annealed at 500°C, approximately 1% of the GaAs substrate was exposed by the formation of erosion centers. This can account for apparent trace amounts of Ga in the Al layer. The diffusion of Al into GaAs may be suggested by the tail of the Al distribution extending into the substrate; in unannealed Al films on GaAs, the interface was more abrupt. Here again, the apparent indiffusion may be associated in part with the formation of erosion centers during thermal aging.

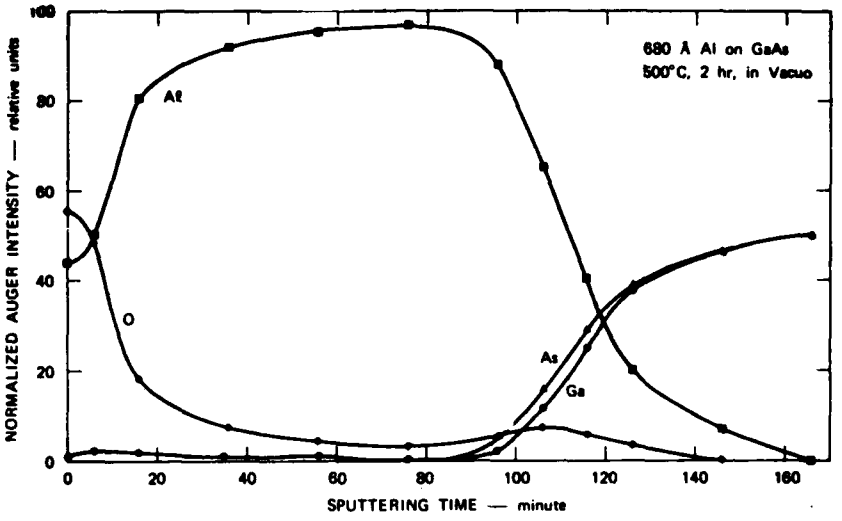

Figure 29. Chemical Depth Profile from a 680-Å Al Film on Single-Crystal GaAs. The Al/GaAs structure was vacuum annealed at 500°C for 2 h. Ar-ion milling was used to obtain the depth profile from normalized Auger intensities of elements present on the sputtered surface.

6.3 DISCUSSION AND CONCLUSIONS

The most evident structural effect of thermally aging Al thin films on GaAs is the formation of erosion centers that expose the substrate. The formation of surface pits has been observed in alloyed Au films on GaAs.[6,12] The pitting indicates a laterally nonuniform alloying process with the pits representing regions where the indiffusion of Au is extremely rapid. In contrast to the irregularly shaped craters observed here, the pits in Au films on (100)-oriented GaAs are rectangular and bounded by (111) planes in the GaAs substrate. The erosion centers in Al films on GaAs may be due to an indiffusion of Al along dislocation lines (diffusion pipes) and related to the observed formation of Al precipitates in the near surface region of the GaAs substrate.

The presence of the erosion centers must be considered in the interpretation of both the electrical and the Auger data. The current densities plotted in Figure 26 are not adjusted for the apparent reduction in contact area accompanying the formation of the erosion centers. However, since $\lesssim$ 1% of the surface area is estimated to be occupied by these craters, the correction is negligible.

In the Auger data, the erosion centers can account for apparent trace amounts of Ga in alloyed Al layers on GaAs. However, the appearance of a small Ga peak at the surface of the Al film as shown in Figure 29, with a Ga concentration above trace levels, suggests that Ga has indeed outdiffused through the Al film. This is consistent with the observation of a rapid penetration of liquid Ga along grain boundaries in bulk polycrystalline Al.[16]

The electrical properties of Schottky-barrier structures are generally sensitive to metallurgical reactions occurring at the metal-semiconductor interface. In the present study, the barrier height of as-deposited Al films on GaAs was found to be 0.73 eV, in close agreement with a previously reported value of 0.75 eV.[17] The increase in the barrier height to 0.82 eV after a vacuum anneal at 500°C (1 h, *in vacuo*) is considered to be associated with interfacial reactions other than the

formation of the erosion centers. No compounds associated with reactions between Ga and Al are known to form.[18] However, AlAs crystallites were detected in all samples examined in the present study, including specimens of (100) as well as (310) orientation. In all cases no additional compounds were detected at the interface. It can therefore be concluded that the thin interfacial layer of AlAs is uniquely correlated with the observed increase in Schottky-barrier height.

TABLE 8. TRANSMISSION ELECTRON DIFFRACTION DATA - Al/GaAs*)

Measured d (Å) values	ASTM d (Å) values GaAs	AlAs	Al
2.837 (spots)	2.832 (200)		
2.837 (ring)		2.83 (200)	
2.352 (ring)			2.388 (111)
1.999 (ring)		2.00 (220)	
1.713 (spots)	1.704 (311)		
1.416 (spots)	1.416 (400)		
1.394 (ring)		1.414 (400)	
1.290 (spots)	1.297 (331)		
1.296 (ring segment)		1.298 (331)	

*(hkl) values are given in parentheses.

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CHAPTER 7

ELECTRON MICROSCOPY STUDIES OF THE ALLOYING BEHAVIOR OF Au ON GaAs

The continued emphasis on the development of improved techniques for the fabrication of electronic devices has prompted a large number of investigations on the nature of metal-semiconductor contacts. The number of studies of metal films on silicon has been extensive and, thus far, the solid-solid reactions of over a dozen metal-silicon systems have been investigated[1-4] by ion backscattering or other complementary techniques. In contrast, the amount of information available on metal-gallium arsenide reactions has been minimal.

For the simple metal-silicon systems (i.e., Au-Si, Ag-Si) it has been shown[4,5-7] that silicon migrates through the metal layer at temperatures significantly below the eutectic temperature. In other systems (i.e., Pt-Si,[4,8] W-Si[9]) subjected to extended annealing, silicon migrates through the metal layer and reacts to form complex metal silicides. In all cases it was found that a thin oxide layer at the interface was sufficient to suppress silicon migration and the formation of compounds.

In 1971, Gyulai et al.[10] presented the results of an investigation of the alloying behavior of Au and Au-Ge layers on GaAs using ion-backscattering and current-voltage measurements. Their data indicated the formation of a heavily disordered region that increased in extent within the substrate as a function of increasing Au layer thickness and alloying time at temperatures > 500°C. Subsequently, Sinha and Poate[11] examined the effect of alloying on the electrical characteristics of GaAs Schottky diodes metallized with W, Au, and Pt. The W-GaAs interface was found to be metallurgically inert at temperatures up to 500°C, and Pt, Ga, and PtAs compounds were found in the outer layer and near the interface of the Pt-GaAs system after alloying at temperatures $\geq$ 500°C. At temperatures > 250°C they found for Au-GaAs that gallium outdiffused to the gold surface and gold diffused into the GaAs, accompanied by a reduction in Schottky barrier height.

In all previous studies of metal films on GaAs or Si there have been no detailed investigations of microstructural defects within the semiconductor substrate. It is the purpose of this note to extend the results of Gyulai et al.[10] and Sinha and Poate[11] on the Au-GaAs system and to provide depth-resolved data on alloying and microstructural modifications in the GaAs substrate.

7.1 EXPERIMENTAL

Single crystal GaAs substrates of (100) orientation were used in this study. The samples were subjected to a final bromine-methanol polish and rinsed in methanol before deposition of the Au films. Gold thin films of thicknesses in the range 400 to 4500 Å were deposited from a boat in a turbomolecular pumped system maintained at a vacuum level of $\sim 10^{-7}$ Torr. Subsequent annealing was done in the vacuum system at 550°C for periods between 20 and 75 min.

Specimens were prepared for transmission electron microscopy (TEM) examination by jet-thinning from the back face of the sample using an H_2O_2-H_2SO_4-H_2O solution. Sectioning techniques for GaAs have been described in an earlier paper by Magee and Comer.[12]

7.2 RESULTS

Examination of GaAs samples before they were alloyed indicated an apparent absence of microstructural defects. A small number of isolated dislocation lines averaging 0.25 μm in length were observed, yielding calculated dislocation densities $< 10^4/cm^2$. In all cases, no other defects were detected by TEM.

The results obtained after alloying Au films of thickness < 2500 Å on GaAs substrates at temperatures > 500°C are summarized briefly in Table 9. In the sections to follow, these data will be discussed in more detail.

TABLE 9. DATA SUMMARY

Depth Zone	Microstructural Characterization	Comments
0 to 400 Å	Irregularly distributed amorphous layer	TEM, TED, and RED data
400 to 2000 Å	AuGa (hexagonal); dislocation lines, some Au segregation	TEM, TED
2000 to 5000 Å	High dislocation density, dislocation forests, Au precipitates	no AuGa observed at depths > 2000 Å

In the near surface zone (< 400 Å in depth) the GaAs structure was highly disordered, resulting in a discontinuous amorphous layer observed in both transmission electron diffraction (TED) and reflection electron diffraction (RED) patterns. The lateral extent of the amorphous region increased as a function of increased annealing time and, after a 75 min alloying time, a semicontinuous amorphous zone was formed. Gyulai et al.[10] obtained similar evidence of a disordered structure from backscattering data but were unable to identify the nature or origin of the structure. From correlated Auger electron spectroscopy measurements we observed excess Ga and As at the surface of samples subjected to the longer annealing periods, indicating that, in addition to the high concentration of Au, changes in stoichiometry at the surface also contribute to the formation of the discontinuous amorphous regions.

Figure 30 shows a bright-field electron micrograph and selected area electron diffraction pattern obtained on an alloyed sample sectioned at approximately 500 Å from the GaAs surface. The sample was alloyed with a 4000 Å thick Au layer at a temperature of 550°C for a period of 45 min. Measurements of "*d*" spacings from electron diffraction patterns (Table 2) and subsequent comparison with established ASTM values[13] indicated that the second phase structures were hexagonal AuGa containing 21 atomic percent Ga. Typically these structures were present beneath the amorphous zone but were occasionally observed at the surface of the sample. In all cases, AuGa was generally not found at depth > 2000 Å.

Figure 30. Bright Field Electron Micrograph and Associated Selected Area Diffraction Pattern of Sectioned GaAs Sample. The particles shown are aligned along a (011) direction and have been identified (Table 1) as hexagonal AuGa.

TABLE 10. TRANSMISSION ELECTRON DIFFRACTION DATA - Au/GaAs*)

Measured *d*-values (Å)	ASTM *d*-values (Å) GaAs	(AuGa)H	*d*-values (Å)	ASTM *d*-values (Å) GaAs	(AuGa)H
5.186		(101) 5.290	1.999	(220) 1.999	
3.865		(110) 3.870	1.697	(311) 1.704	
3.254	(111) 3.260		1.591		(223) 1.611
2.824	(200) 2.832		1.461		(006) 1.457
2.486		(211) 2.430	1.307		(413) 1.306
2.308		(113) 2.320	1.215		(306) 1.220
2.160		(203) 2.199			

*) (*hkl*) values are given in parentheses.

The formation of AuGa within the substrate introduced considerable strain because of the large lattice misfit. As shown in Fig.31, dislocations are inevitably present at the edges of AuGa particles. In Fig.32, the micrograph obtained in the region below the zone of AuGa formation indicates a region of high dislocation density. This form of damage has been observed to depths > 3000 Å for samples subjected to extended alloying periods.

In addition to reacting with Ga to form AuGa, the Au segregates to form precipitates (Fig. 33), which have been identified in transmission electron micrographs and selected area diffraction patterns. The precipitates were observed in decreasing density for depths extending to $\sim$ 3000 Å in GaAs samples alloyed at 550°C for periods > 30 min. For shorter alloying times, the concentration of Au precipitates appeared to reach a maximum at depths < 2000 Å.

In contrast to the results obtained for thick Au films on GaAs, samples with thin ($\sim$ 400 Å) Au gilms annealed at 550°C for periods < 30 min exhibited precipitates only within near surface zones. Furthermore, we obtained single crystal diffraction patterns on the alloyed samples, indicating an apparent absence of highly disordered zones. For samples annealed at times > 30 min, AuGa was observed in small, irregularly distributed regions.

7.3 CONCLUSIONS

In this study we have shown that alloying Au films on GaAs produces several distinct damage zones within the substrate. The first zone includes a heavily disordered region, which increases in lateral extent as a function of initial film thickness and alloying duration. The second region is characterized by the presence of hexagonal AuGa, dislocation lines, and Au precipitation. The third zone contains a high density of dislocation lines extending to depths > 3000 Å. In samples containing thin Au films and alloyed for short periods, amorphous regions are absent and the formation of AuGa is less extensive.

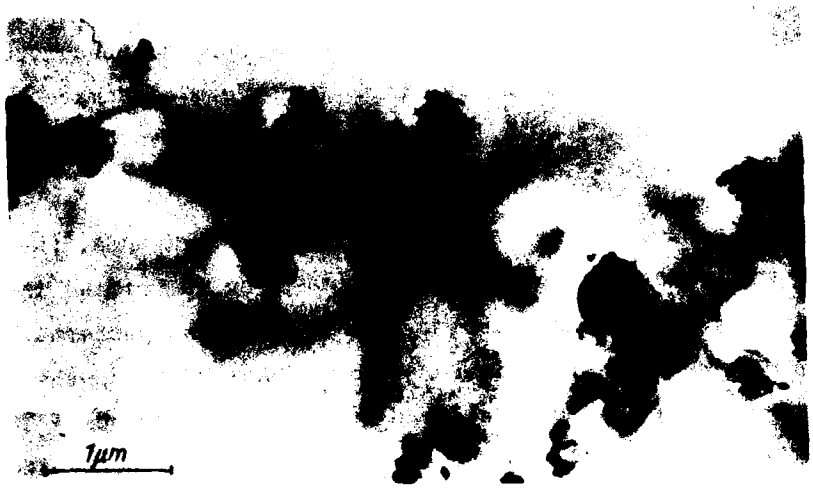

Figure 31. Bright Field Electron Micrograph Showing the Presence of Dislocations Around AuGa Particles.

Figure 32. Bright Field Electron Micrograph of Region Beneath AuGa in Sectioned Sample.

Figure 33. Bright Field Electron Micrograph Showing the Presence of Au Precipitates.

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APPENDICES

A.1 LIST OF PUBLICATIONS (WPAFB Contract F33615-75-C-1084)

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A.2 TECHNICAL REPORTS (SRI) (WPAFB Contract F33615-75-C-1084)

1. T. Magee, "Influence of Oxygen on the Outdiffusion of Gallium in Si_3N_4 Encapsulated GaAs," SRI Technical Report 4150-1 (1975).
2. T. Magee and J. Peng, "Microstructural Evaluation of Defects in Commercially Available GaAs," SRI Technical Report 4150-2 (1976).

A.3 GRADUATE THESES (STANFORD UNIVERSITY) (Research supported partially by WPAFB Contract F33615-75-C-1084)

1. E. Ammar, "Implantation and Annealing of Sulfur in Gallium Arsenide," Degree of Engineer, Electrical Engineering Department, Stanford University, March 1977.
2. A. Lidow, "Encapsulation and Annealing of Selenium Implanted Gallium Arsenide," Ph.D. Thesis, Electrical Engineering Department, Stanford University, December 1977.

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