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CHARGE-COUPLED SCANNED IR IMAGING SENSORS

RCA Laboratories

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This program was directed at fabricating infrared focal planes consisting of Schottky-barrier detectors multiplexed by charge-coupled shift registers, and demonstrating their imaging capability against 300K background radiation. Three devices were designed and fabricated: a 64-bit, three-phase line-array with transfer gaps, a 62-bit line array, and a 25x50 area array, the latter two with four-phase, → next page

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sealed-channel, overlapping-gate, double-polysilicon structure. The detectors were palladium silicide and platinum silicide on p-silicon. Fabrication involved only standard silicon-processing operations. Excellent agreement has been obtained between calculated infrared performance and experimental data. Detector uniformity better than 1%, already achieved with palladium silicide, is adequate for staring-mode thermal imagers. These sensors make possible imagers with thermal resolution on the order of tenths of a degree C, and productions costs less than present scanned systems.

PREFACE

This Final Report was prepared by RCA Laboratories, Princeton, New Jersey, under Contract No. F19628-73-C-0282 and ARPA Order No. 2444. It describes work performed from 29 June 1973 to 15 February 1977, in the Integrated Circuit Technology Center, J. S. Scott, Director, and the Process and Applied Materials Research Laboratory, H. Kressel, Director. E. S. Kohn was the principal investigator; the Project Supervisor was K. H. Zaininger. Other members of the Technical Staff who participated in the research were W. F. Kosonocky, F. V. Shallcross, M. L. Shultz, R. D. Larrabee, P. A. Levine, S. O. Graham, J. E. Carnes, J. Banfield, B. Levin, and G. Meray (Research Associate). This report includes infrared measurements made at RADC/ET by R. W. Taylor, F. D. Shepherd and S. A. Roosild. F. S. Shepherd and S. A. Roosild were the contract monitors.

The first draft of this report was submitted by the authors on 15 May 1977. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

As background information, you may wish to see the Semiannual Technical Reports prepared by RCA Laboratories, on 14 January 1974 (AFCRL-TR-74-0056); 15 July 1974 (AFCRL-TR-74-0375); 15 May 1975 (AFCRL-TR-75-0284); 14 November 1975 (RADC/ET-TR-75-0624); and September 1976 (RADC/ET-TR-76-277).

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I. INTRODUCTION

Ever since the concept of charge coupling was reported several years ago, imaging with charge-coupled devices (CDDs) has constituted an area of intense activity [1-3]. Visible imagers with full TV resolution have been demonstrated [4]. While devices with a variety of gate structures, channel types, and chip layouts have been reported, almost all of these have in common the use of silicon as the photo-absorbing material. Whether the photosensitive region is under the shift-register gates, under separate photogates, or at separate photodiodes, minority carriers photoexcited in the silicon form the charge packets to be clocked out. Since these devices have basically the spectral response and quantum efficiency associated with silicon photodiodes, they are useful as infrared imagers to wavelengths as long as 1.1 μm.

There is considerable interest in imagers sensitive to longer-wavelength infrared radiation. Imagers sensitive in the 2- to 3-μm range are useful to the military for viewing high-contrast scenes involving jet and rocket plumes, while devices responding to radiation as far out as 4.5 μm can image 300K scenes by their own thermal radiation, and are of interest for industrial and medical, as well as military, applications [5]. Infrared detector arrays which accomplish this are already in existence, and, in some cases, perform close to their theoretical limit. These imagers, known as FLIRs (Forward-Looking Infrareds), contain linear arrays of cooled infrared detectors with mechanical scanning. Their applications are restricted primarily by their high cost. A considerable amount of effort has gone into the development of Vidicon television camera tubes for use in the infrared, but the technical problems encountered are formidable. Thus, an infrared, charge-coupled imager would be a welcome device.

1. C. H. Sequin and M. F. Tompsett, *Charge Transfer Devices*, Suppl. 8 for *Advances in Electronics and Electronic Physics* (Academic Press, New York, 1975).
2. W. F. Kosonocky and J. E. Carnes, RCA Review 36, 566 (Sept. 1975).
3. W. F. Kosonocky, "CCD's--An Overview," Proc. WESCON, Sept. 1974.
4. RCA Data Sheet SID 51232, Lancaster, Pa., Jan. 1975.
5. Proc. IEEE, special issue, "Infrared Technology for Remote Sensing," Jan. 1975.

There are several approaches to the design of infrared, charge-coupled imagers. One is the fabrication of charge-coupled shift registers on materials having the desired intrinsic response [6]. Such materials include InAs, InSb, and HgCdTe. Infrared radiation would be absorbed in the wafer, generating minority carriers that would then be transported just as in silicon devices. Unfortunately, at the present time the fabrication of such devices on materials other than silicon creates severe technological problems. A second approach is the fabrication of charge-coupled shift registers on silicon wafers with separate infrared detectors prepared on the wafer. Although Schottky barriers are a natural choice, photoconductive films and heterojunction detectors present other possibilities. A third approach is the use of extrinsic silicon. Since this mode of operation requires the freeze-out of carriers, the device would have to be cooled to a temperature considerably lower than that required for most other infrared detectors. The entire chip could be frozen out as reported by Nelson [7] and the shift register run in the accumulation mode, a very different mode of operation. Alternatively, different dopants could be used for the detectors and for the shift register so that the former would be frozen out but not the latter. Such a device could be run in the "normal" depletion mode.

A prime concern in the develoment of any thermal imager is the large background radiation present in the thermal scene. A typical requirement for a thermal viewer is to make possible recognition of an object at 300.1K in a uniform 300K scene. In this case, the "signal" is the difference between the number of photons arriving from the hotter object and the number arriving from an equal solid angle of the background. This signal can be less than 1% of the background, but, in order to detect it, the sensor must read the entire background. It is this requirement of handling the entire background that taxes the target-storage and beam-density capability of standard Vidicon tubes and makes the solid-state alternative so attractive. But, regardless of the capability of the detector to handle the background without saturating, the presence of the background severely aggravates the problem of detector nonuniformity. If the detectors were to vary in sensitivity by just a few percent,

6. A. J. Steckl et al., Proc. IEEE 63, 67 (1975).
7. R. D. Nelson, Applied Physics Letters 25, 568 (1974).

the nonuniformities in the picture due to the background would overwhelm the signal with fixed-pattern noise.

Complicating the problem is the fact that most types of infrared detectors cannot be produced even as uniformly as detectors fabricated for the visible part of the spectrum. Detector nonuniformity is not a problem for visible imagers because of the high contrast usually present in the reflected visible light from normal scenes, but it is always a major consideration for thermal imagers. That is why, in FLIRs, the separate amplifiers for the 100 or more detectors in the linear array must be trimmed individually to compensate for differences in detector sensitivities. This compensation method contributes to the high cost of line scanners and is clearly impractical for an area imager.

Thus, for thermal area imagers, excellent uniformity is an essential requirement. Fortunately, the requirement for high quantum efficiency can be relaxed for area arrays. Line scanners (FLIRs) require reasonably sensitive detectors to achieve background-limited performance, but area imagers, having frame storage, can achieve the same quality of performance with detectors whose quantum efficiency is two orders of magnitude lower. Detectors with insufficient sensitivity for scanned imagers using line arrays may still be quite suitable for area arrays. Schottky-barrier detectors involving metal silicides are particularly uniform in photoresponse [8]. Our results here show that fixed-pattern noise of less than 1% is possible.

Our approach to the design of infrared-sensitive, charge-coupled imagers has been to merge these two well-known technologies, namely silicon charge-coupled shift registers and silicide Schottky-barrier detectors, both fabricated on silicon wafers. The operation requires that the majority-carrier signals from the detector be converted to minority-carrier packets for transport by the shift registers. A method proposed by RADC [9] for accomplishing this with the help of metal-oxide semiconductor field-effect transistors (MOSFETs) provided

8. F. D. Shepherd et al., "Silicon Schottky-Barrier Monolithic IR-TV Focal Planes,"*Advances in Electronics and Electron Physics*, Vol. 40B (Academic Press, New York, 1976), p. 981.
9. F. D. Shepherd and A. C. Yang, Proc. Int. Electron Device Meeting, Washington, DC, Dec. 1973, p. 310.

the impetus for this program. A different scheme, however, was designed into the first line array, a three-phase, single-metal device. Developed at RCA Laboratories, this method [10] made possible background subtraction at each detector. But experiments with the device showed that background subtraction was not needed. Indeed, superior performance was obtained with a simplified method of operation referred to here as the "Vidicon mode," in which the background-subtraction circuitry is ignored. Our second chip had its major device, a 25x50 area array, designed specifically for Vidicon-mode operation. A 62-element line array was, however, included on this chip to make experiments on other methods of operation possible.

10. B. F. Williams and W. F. Kosonocky, U.S. Patent 3,845,295, Oct. 29, 1974.

II. SCHOTTKY-BARRIER DETECTORS

A. SCHOTTKY-BARRIER DIODES

A simple Schottky-barrier device is shown in Fig. 1(a), consisting of a metal film evaporated onto a semiconductor wafer through a hole in an insulator. The device has electrical characteristics similar to those of a p-n junction, its characteristics depending upon the barrier height at the interface in much the same way that the characteristics of the p-n junction depend upon the bandgap. The barrier height itself depends upon the choice of metal, as well as the choice and polarity of the semiconductor. Its value is nearly independent of semiconductor doping and minority-carrier lifetime. A reverse-biased Schottky-barrier diode exhibits dark current both from thermally generated minority carriers in the semiconductor being collected by the metal, and from majority carriers in the metal being thermally excited over the barrier into the semiconductor. Since the barrier height in any detector of interest to us is smaller than half the bandgap of silicon, the latter process dominates. Similarly, the device can act as a photodetector by absorbing light either in the semiconductor or in the metal. In the former case, photoexcited carriers in the semiconductor are collected at the interface, and the spectral response is similar to that of a p-n junction. In the latter case, carriers are photoexcited over the barrier from the metal to the semiconductor; there they become majority carriers. The quantum efficiency in this case is relatively low, but the response extends to photon energies as low as the barrier height, a value that can be considerably smaller than the bandgap. The light to be detected by this process can be incident through either the semiconductor or the metal. If it is to be through the metal, the metal must be thin, and the uniformity of response is critically dependent upon the uniformity of the metal thickness. With light incident on the semiconductor, however, absorption takes place at the interface regardless of metal thickness, and a thick layer of metal ensures uniformity. The semiconductor need not be thinned since it is transparent in the spectral region of interest. Since the spectral yield in this mode depends almost entirely on the absorption process in the metal and transport over the barrier, the sensitivity is

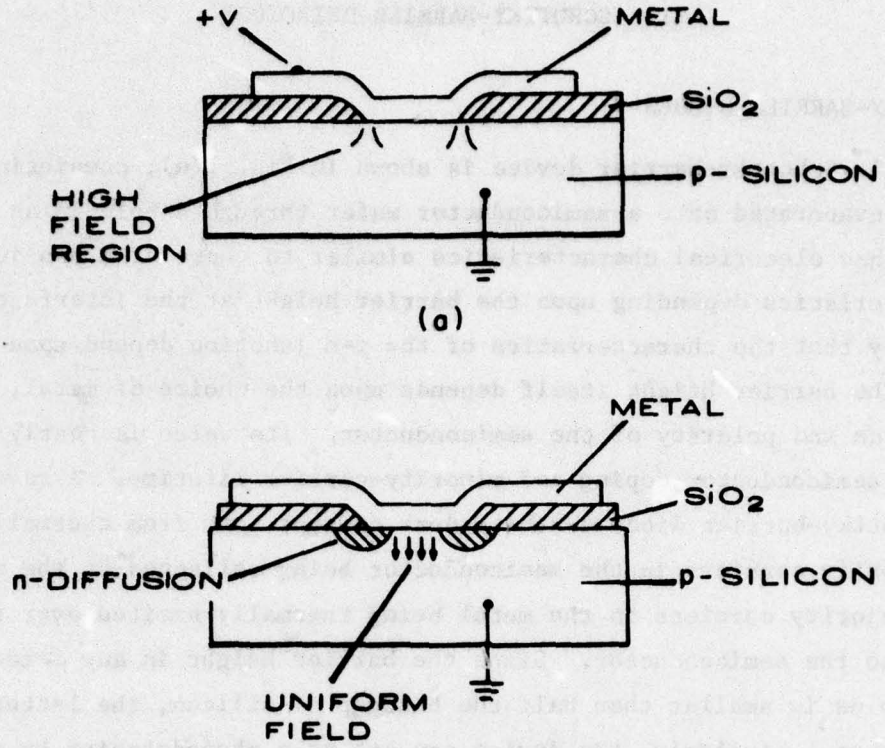


Figure 1. Schottky-barrier detectors: (a) without guard rings and (b) with guard rings.

almost independent of such parameters as semiconductor doping and minority-carrier lifetime, thus eliminating major sources of nonuniformity in semiconductor detectors. It is for this reason that an array of Schottky-barrier detectors is potentially much more uniform in response than other types of semiconductor detectors and is probably limited in uniformity by the accuracy of the photolithographic process defining the boundaries of the detectors. There is experimental evidence that this is so [8]. For these reasons, we chose to use Schottky-barrier detectors and to illuminate them through the substrate. For our detectors, we chose silicides formed with palladium or platinum on p-type silicon.

Palladium and platinum are metals that react chemically with silicon to form silicides having metallic properties. The actual Schottky barrier

is therefore between the silicon substrate and the silicide film formed beneath the original silicon surface. One advantage of this reaction is that surface oxides and other contaminants cannot influence the barrier as they could if the barrier were between silicon and a nonreacting metal. Another advantage is that the excess metal can be removed, by etching, and the device contacted with a more conventional metal such as aluminum.

B. PHOTORESPONSE

Schottky-barrier detectors operating in the internal-photoemission mode have their quantum efficiency given by [8]

$$QE(\nu) = \frac{C_1}{q} \cdot \frac{(h\nu - q\psi_{ms})^2}{h\nu} \tag{1}$$

where $h\nu$ is the photon energy, q is the charge on an electron, and ψ_{ms} is the metal-semiconductor barrier height in volts. The equation is written so as to make the constant C_1 expressed in reciprocal electron volts, as it is usually found in the literature. This equation is valid only when the photon energy is greater than the barrier height,

$$h\nu > q\psi_{ms} \tag{2}$$

and, in the case of illumination through the wafer,

$$h\nu < qE_g \tag{3}$$

where E_g is the bandgap of silicon.

Photons with energy greater than the bandgap of silicon will be absorbed in the silicon and will generate minority carriers that can be collected at the metal. This, however, is not the desired mechanism, and in any case will not be important for 300K thermal imaging.

The spectral response of the Schottky diodes was measured [11] by means of a modified Perkin-Elmer† Model 98 monochromator. In this apparatus, the output beam was split into two equal path-length beams. One illuminated the

†Made by Perkin-Elmer Corp., Norwalk, Conn.

11. R. W. Taylor, et al., "Schottky IR-CCD's," Proc. IRIS Detector Specialty Group Meeting, 22-24 March 1977, Air Force Acad., Colorado Springs, Col.

sample under test, and the second illuminated a calibrated thermocouple. By use of the ratio of the diode response to the thermocouple response, the effects of source envelope and atmospheric attenuation were eliminated from the measurement. The resulting data are then presented as a modified Fowler plot to determine both C_1 and ψ_{ms}. Typical data for a palladium silicide diode are shown in Fig. 2.

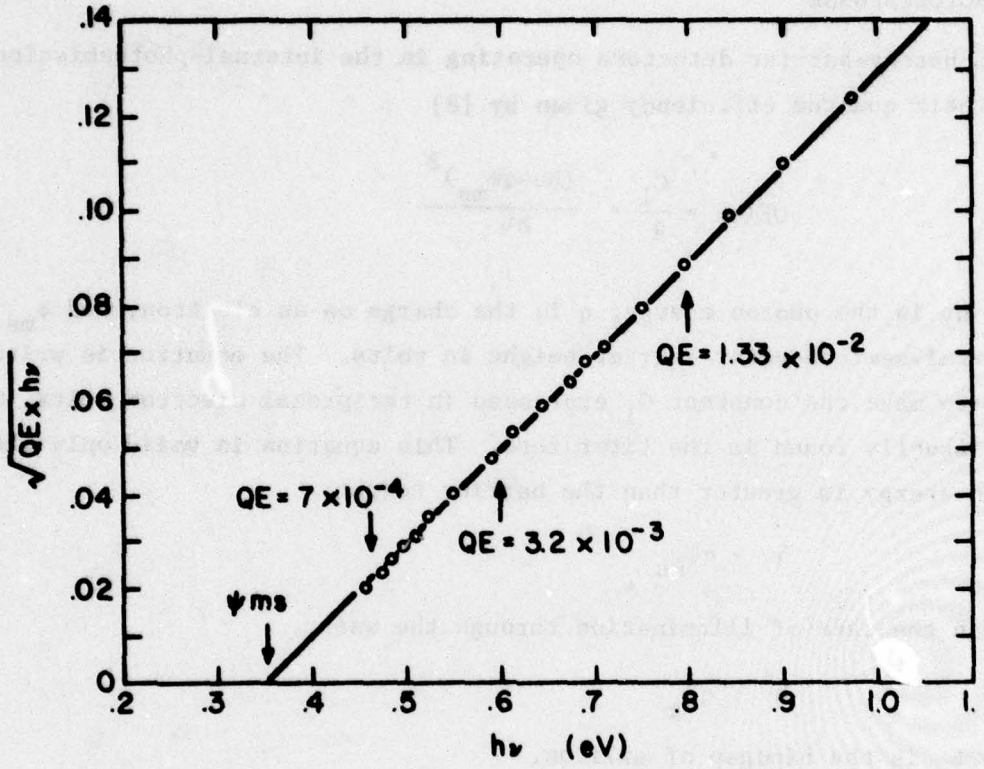


Figure 2. Spectral response of Pd_2Si Schottky diode ($h\nu$ and ψ_{ms} are expressed in electron volts).

C. SCHOTTKY-BARRIER DARK CURRENT

Dark current is of fundamental concern to us since the uniformity of response of Schottky-barrier detectors would be lost if this current were significant and variable among detectors in the array. A large dark current, even if uniform, would be intolerable because it would fill the wells. The theoretical dark current of an infrared-sensitive Schottky-barrier detector is due almost entirely to the internal thermionic emission of carriers from the metal over

the barrier into the semiconductor. The current density for this process is given by [12]

$$J = A^* T^2 \exp - \frac{q\psi_{ms}}{kT} \qquad (4)$$

where A^* is about 32 A/cm^2, ψ_{ms} is the barrier height, q is the electronic charge, k is Boltzmann's constant, and T is the detector temperature. Theoretical dark currents are compared in Table 1. With ψ_{ms} equal to 0.35 V for a palladium silicide-to-p-silicon barrier at 77K, the predicted current density is $2.4\text{x}10^{-18}$ A/cm^2; at 300K, it would be 3.8 A/cm^2. This must be compared with the charge-storage capability of the CCD. For our three-phase array, the detector area is 4.5 mil^2, while the CCD gate area is 2.5 mil^2. The capacitance of the gate oxide is 0.1 pF/mil^2 = 10^{-13} F/mil^2. Thus, the capacitance of our gate is $0.25\text{x}10^{-12}$ F. The charge that would cause the surface potential under the CCD gate oxide to change by 1 V is $0.25\text{x}10^{-12}$ F x 1 V = $0.25\text{x}10^{-12}$ C. If the frame time is 1/30 s, the dark current at the Schottky barrier needed to produce this charge is $0.25\text{x}10^{-12}$ C/(1/30) s = $7.5\text{x}10^{-12}$ A. Thus, the current corresponds to a current density at the Schottky barrier of $7.5\text{x}10^{-12}$ A/4.5 mil^2 = $7.5\text{x}10^{-12}$ A/$2.8\text{x}10^{-5}$ cm^2 = $2.7\text{x}10^{-7}$ A/cm^2. Taking a 1-V swing at the CCD interface as the maximum-tolerable dark signal, we have $0.27\text{x}10^{-6}$ A/cm^2 as the maximum-tolerable dark-current density at the Schottky barrier. Thus, it is clear that our device cannot possibly operate at room temperature; at 77K, however, the calculated dark current is below the maximum-tolerable amount by a factor of more than 10^{10}. For platinum silicide, the margin is smaller but still sizable. For the dark current to be kept this small in practice, however, care must be taken to prevent surface channeling, and in some cases, to reduce field concentration at the edges. Test devices, made early in the program, illustrated these problems. (See Semiannual Technical Report, 14 January 1974 (AFCRL-TR-74-0056).) Our CCDs, however, had channel confinement. Furthermore, the inverted surface present in p-Si acted to reduce the field concentration at the edge. Guard rings, illustrated in

12. S. Sze, *Physics of Semiconductor Devices* (Wiley-Interscience, New York, 1969).

Fig. 1(b), were designed into the second mask set, but good results were obtained with CCDs lacking that feature. Palladium silicide detectors in particular were reverse-biased to several volts without excess dark current. Results presented later show that in IR-CCDs run at temperatures high enough to cause observable dark current, the dark currents in the array were remarkably uniform. The area-array chip had several test devices for measuring detector dark current, including a storage test device. Results with this test, discussed later, show storage time on the order of 1 s, corresponding to a dark current of 16×10^{-9} A/cm^2.

TABLE 1. SCHOTTKY-BARRIER DARK CURRENT AT THREE TEMPERATURES

Temperature (K)	Current Density A/cm^2 and Number of Carriers	
	3.54-μm Pd_2Si	4.5-μm PtSi
77K	2.4×10^{-18} (<<1)	4×10^{-13} (2)
90K	5.9×10^{-15} (<<1)	2.0×10^{-10} (1049)
100K	7.5×10^{-13} (4)	8.0×10^{-9} (4.2×10^4)

These values were calculated from the Richardson equation with $A^* = 32$ A/cm^2(K)^2 for holes in silicon [13]. The numbers in parenthesis represent the number of carriers accumulated in 30 ms in a detector of area 2.8×10^{-5} cm^2.

13. J. M. Andrews and M. P. Lepselter, Solid-State Electron. 13, 1011 (1970).

III. INFRARED PERFORMANCE ANTICIPATED FROM SCHOTTKY-BARRIER ARRAYS

The response of Schottky-barrier detectors to thermal radiation has been reported by Shepherd et al. [8] and by Kohn et al. [14]. The spectral radiance emitted by a thermal radiator per frequency increment is [15]

$$L_\nu = \frac{2h}{c^2} \frac{\nu^3}{(e^{h\nu/kT} - 1)} \quad \frac{W}{(m^2)(sr)(Hz)} \tag{5}$$

The spectral *photon* radiance is then

$$L'_\nu = L_\nu / h\nu = \frac{2}{c^2} \frac{\nu^2}{\left(e^{h\nu/kT} - 1\right)} \tag{6}$$

The spectral *incidence* of photons is given by the same expression with the *background* temperature T_b in place of T. Thus, the number of carriers generated in a detector of area A in time t_s is given by

$$n_b = \int_{\nu_{ms}}^{\infty} QE(\nu)\, L'_\nu(\nu, T_b) A t_s \left(\frac{\pi}{4F^2}\right) d\nu \tag{7}$$

where $QE(\nu)$ is the spectral quantum efficiency of the detectors, and the expression in parenthesis converts from steradians to focal ratio F. For Schottky-barrier detectors, the integral is taken from the cutoff frequency, ν_{ms},

$$\nu_{ms} = \frac{q\psi_{ms}}{h} \tag{8}$$

---

14. E. S. Kohn et al., "Infrared Imaging with Monolithic, CCD-Addressed Schottky-Barrier Detector Arrays: Theoretical and Experimental Results," in Proc. Int. Conf. on the Application of Charge-Coupled Devices, San Diego, Cal., 1975.
15. RCA Electro-Optics Handbook, EOH-11 (RCA Commercial Engineering, Harrison, N.J., 1974), p. 36.

to the cutoff of silicon, but little accuracy is lost in taking it to infinity because the exponential term becomes negligible. With the approximation

$$e^{h\nu/kT_b} \gg 1 \tag{9}$$

and with the expression for the quantum efficiency of a Schottky-barrier detector

$$QE = \frac{C_1}{q} \frac{(h\nu - q\psi_{ms})^2}{h\nu} \tag{10}$$

$$n_b = \frac{\pi A t_s C_1 k^4 T_b^4}{q c^2 F^2 h^3} \left(\frac{q\psi_{ms}}{kT_b} + 3\right) \exp -\left(\frac{q\psi_{ms}}{kT_b}\right) \tag{11}$$

or

$$n_b = 2.7 \times 10^{10} A t_s C_1 T_b^4 (\mu_o + 3)\, e^{-\mu_o} \tag{12}$$

where

$$\mu_o = \frac{q\psi_{ms}}{kT_b} = \frac{11{,}609\ \psi_{ms}}{T_b} \tag{13}$$

All quantities are in mks units except C_1, the detector efficiency factor, which is reported in the literature in reciprocal electron volts. The first q in Eq.(10) accounts for this. The quantities are defined in Table 2. The values in the table are for our line array with PtSi Schottky barrier. With these values,

$$n_b = 3.8 \times 10^5 \text{ carriers} \tag{14}$$

Thus, the stored charge is

$$Q_b = q_{nb} = 1.6 \times 10^{-19} \text{ C} \times 3.8 \times 10^5 = 6.0 \times 10^{-14} \text{ C} \tag{15}$$

TABLE 2. QUANTITIES USED IN CALCULATIONS

c	Speed of light	3×10^{8} m/s
h	Planck's constant	6.626×10^{-34} J·s
k	Boltzmann's constant	1.38×10^{-23} J/K
q	Electron charge	1.602×10^{-19} C
A	Area of detector	$2.8 \times 10^{-9} m^2$
A_s	Area of gate	10^{-9} m^2
C_l	Detector QE factor	0.1 eV^{-1}
C_{fd}	Capacitance of floating diffusion	0.5×10^{-12} F
F	Focal ratio of optics	1
L_ν	Spectral radiance	$W/(m^2)(sr)(Hz)$
L'_ν	Spectral *photon* radiance	$1/(m^2)(sr)(Hz)$
n_b	Number of background carriers	
n_f	Detector nonuniformity	
n_n	Combined electrical noise	
N	Number of transfer gates	200
N_{ss}	Density of fast traps	4×10^{10} cm^{-2} eV^{-1}
t_s	Storage time	33.3×10^{-3} s
T_b	Background temperature	288K
T_d	Detector temperature	80K
ϵ	Loss per transfer	5×10^{-4}
ψ_{ms}	Schottky-barrier height	0.275 eV for PtSi:p-Si
		0.35 eV for Pd_2Si:p-Si

The output signal is

$$V_b = Q_b/C_{fd}$$

$$= \frac{6.0 \times 10^{-14}}{0.5 \times 10^{-12}} \approx 0.12 \text{ V} \tag{16}$$

The calculated 288K background photoresponse is plotted as a function of Schottky-barrier cutoff wavelength in Fig. 3. These data were calculated for a proposed higher-density array with 1-mil^2 detectors and a 0.2-pF floating diffusion, but are otherwise consistent with the previous calculation, arrived at by means of the 10% eV^{-1} curve.

The contrast (per kelvin) is given by

$$\gamma = \frac{1}{n_b}\frac{dn_b}{dT_b} = \frac{1}{T_b}\frac{\left(\frac{q\psi_{ms}}{kT_b} + 3\right)^2 + 3}{\left(\frac{q\psi_{ms}}{kT_b} + 3\right)} \tag{17}$$

The equation is plotted as a function of cutoff wavelength λ_c in Fig. 4, for a background temperature of 288K(15°C). A 288K background detected by PtSi Schottky barriers has 4.7% per K contrast. Thus, a difference of one kelvin produces a signal of about 19,000 carriers. The shot noise is on the order of 620 carriers. Other noise sources [16(a,b)] are shown in Table 3. Thus, good temperature resolution is possible, but only if the electrical noise sources are kept near the theoretical limit. The margin can be improved with a longer integration time.

The noise-equivalent temperature NEΔT is a measure of the temperature-resolving capability of the retina, and is defined as

$$NE\Delta T = n_n/\gamma n_b \tag{18}$$

16. J. E. Carnes and W. F. Kosonocky, RCA Review (a) 33, 327 (1972); (b) 33, 607 (1972).

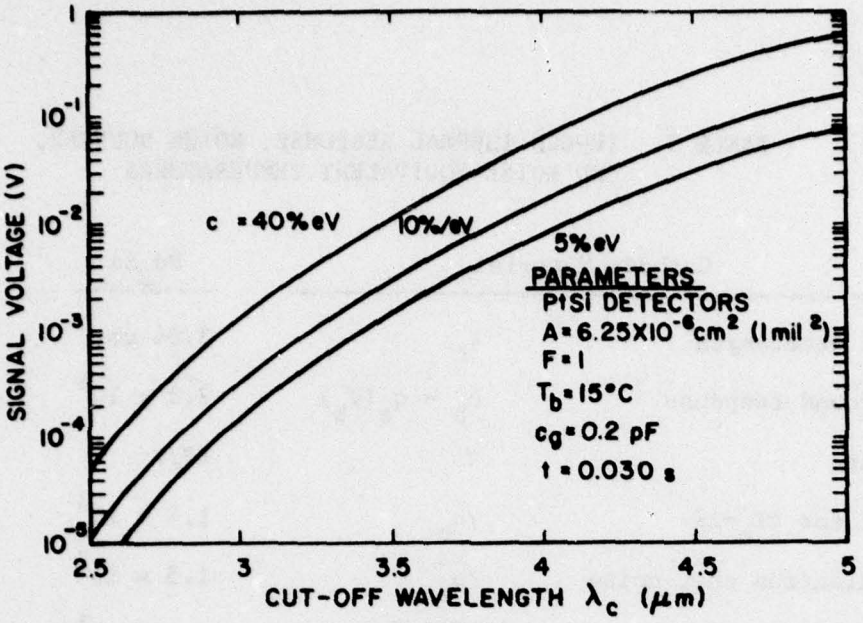


Figure 3. Background photoresponse vs cutoff wavelength.

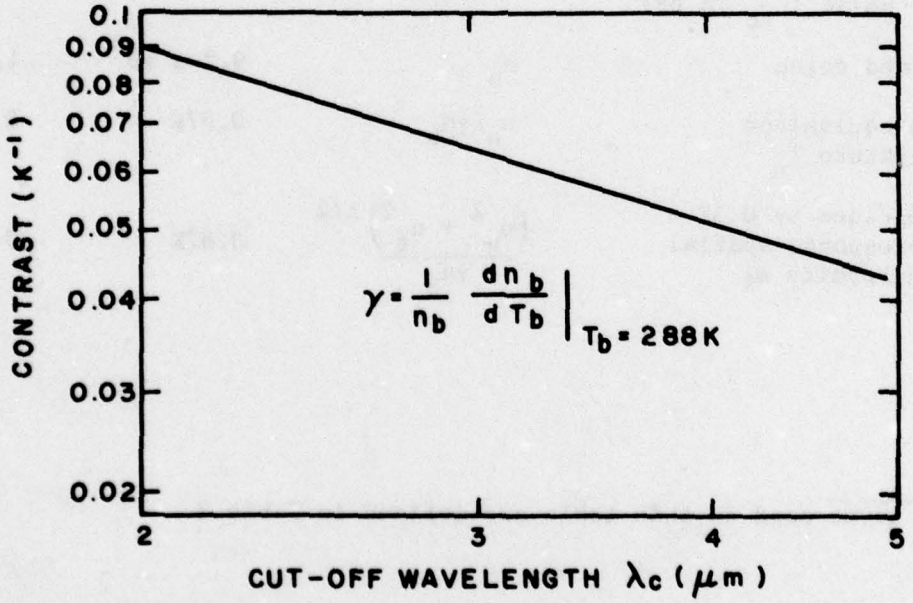


Figure 4. Schottky-retina signal contrast (per K) as a function of detector cutoff wavelength.

TABLE 3. IR-CCD THERMAL RESPONSE, NOISE SOURCES, AND NOISE-EQUIVALENT TEMPERATURES

Cathode Material		Pd_2Si	PtSi
Cutoff wavelength	λ_c	3.54 μm	4.5 μm
Background response	$n_b = q_s(T_b)$	2.3×10^4	3.8×10^5
Contrast	γ	6%/K	5%/K
Signal for ΔT_b=1K	γn_b	1.4×10^3	1.9×10^4
Photoelectron shot noise	$\sqrt{n_b}$	1.5×10^2	6.2×10^2
Background-charge incomplete-transfer noise	$\sqrt{2\varepsilon N n_b}$	6.8×10^1	2.8×10^2
Fast interstate trapping noise	$\sqrt{1.4kTNN_{ss}A_s}$	8.8×10^2	8.8×10^2
Floating-gate reset noise (C_{fd} in pF)	$200\sqrt{C_{fd}}$	1.4×10^2	1.4×10^2
Combined noise	n_n	9.2×10^2	1.1×10^3
Noise-equivalent temperature T_n	$n_n/\gamma n_b$	0.67K	0.06K
T_n degraded by 0.5% photoresponse spatial nonuniformity n_f	$\frac{\left(n_n^2 + n_f^2\right)^{1/2}}{\gamma n_b}$	0.67K	0.12K

*The terms used in this table are defined in Table 2.

This is simply the increase in background temperature required to increase the output signal by an amount equal to the rms electrical noise n_n on the signal. The calculated NEΔT of our three-phase line array is shown in Fig. 5 as a function of detector cutoff wavelength for a 288K background. Electrical noise of 2000 electrons per packet is assumed. For PtSi on p-Si, an NEΔT on the order of 0.1K is predicted. This does not take fixed-pattern noise into account.

The various signal levels and noise sources are presented in Table 3 for Pd_2Si and PtSi on p-Si detectors. Here the results of Carnes and Kosonocky [16(a,b)] were adapted to our infrared signal levels and cryogenic temperatures. Fixed-pattern noise was brought in by assuming 0.5% spatial nonuniformity as observed in our better Pd line arrays.

Examination of Table 3 shows that the dominant noise mechanism is fast interstate trapping. If we use buried-channel rather than surface-channel CCD technology, this noise mechanism would become negligible. The change in technology would result in a threefold improvement of Pd_2Si-array sensitivity, and in a background-limited performance for the PtSi arrays. Further sensitivity improvements would be obtained by reducing the floating-gate capacitance and, in the case of the PtSi array, by reducing photoresponse nonuniformities. The noise-equivalent temperatures given in Table 3 indicate expected performance at short range. At long range, atmospheric absorption would seriously degrade the Pd_2Si performance.

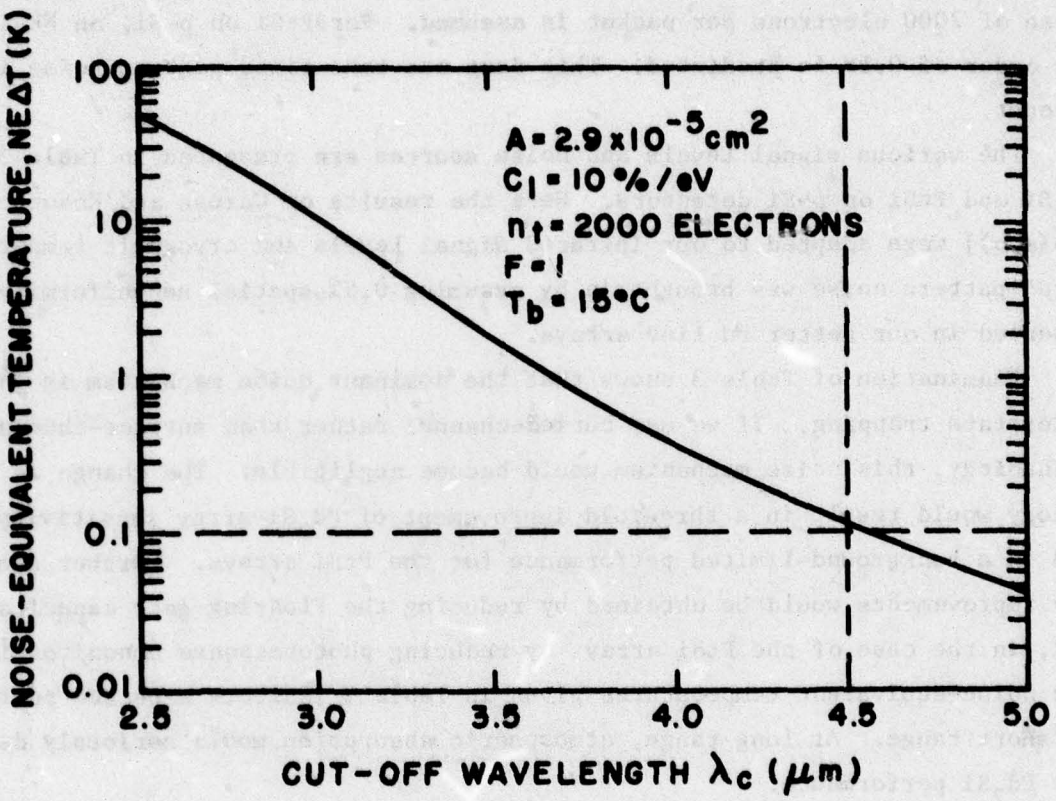


Figure 5. IR-CCD noise-equivalent temperature vs cutoff wavelength.

IV. IR-CCD DESIGN CONSIDERATIONS

A. CHARGE-COUPLED SHIFT REGISTERS

The first 64-element infrared-charge-coupled device (IR-CCD) was made with a three-phase, single-metal, CCD structure, illustrated in Fig. 6(a). At the beginning of this contract the single-metal CCD technology [1,3] represented the most expedient process for proving the feasibility of Pd_2Si and PtSi Schottky-barrier IR-CCDs. The second design (the 25x50 element array) was done with the four-phase, double-polysilicon, CCD technology illustrated in Fig. 6(b). The sealed-channel, overlapping-gate CCD represents the present state-of-the-art CCD process with stable- and high-performance operation [16]. Such surface-channel CCDs, operating with about 10% bias charge ("fat zero"), have typical transfer losses of about 10^{-4} per transfer [16(c)]. However, the overlapping-gate, buried-channel CCD can be made with a transfer loss of only about 10^{-5} even when operating without the bias charge [2]. Another important advantage of double-polysilicon CCD construction is that the additional metallization levels permit a more compact layout for the two-dimensional IR-CCD array.

Although the devices made under this contract had only surface-channel CCDs, the mask set included the option for fabricating buried-channel CCDs with surface-channel, on-chip, floating-diffusion amplifiers.

B. CCD OPERATION WITH SCHOTTKY-BARRIER DETECTORS

The operation of charge-coupled shift registers is described with reference to our three-phase, single-metal design. The structure used for coupling the Schottky-barrier detectors to the charge-coupled shift register is shown in Figs. 7 and 8. A row of Schottky-barrier metallizations is seen in the center of the chip. The center area of each metallization contacts the p-wafer forming the infrared-sensitive area. Each metallization also contacts individual charging and transfer diffusions. The transfer gate overlaps the transfer diffusions and can couple them individually to the phase-1 gates of the shift register. The phase-1 gates are wider than the other shift-register

16. (c) W. F. Kosonocky and J. E. Carnes, RCA Review 34, 164, (73).

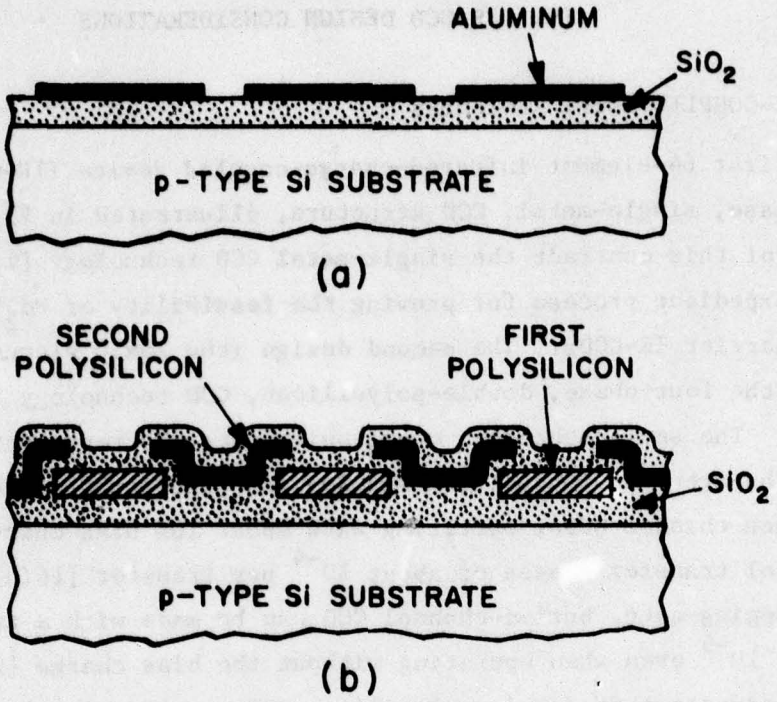


Figure 6. Two types of charge-coupled structures: (a) single-metal CCDs, and (b) sealed-channel CCDs in the form of a double-polysilicon gate structure.

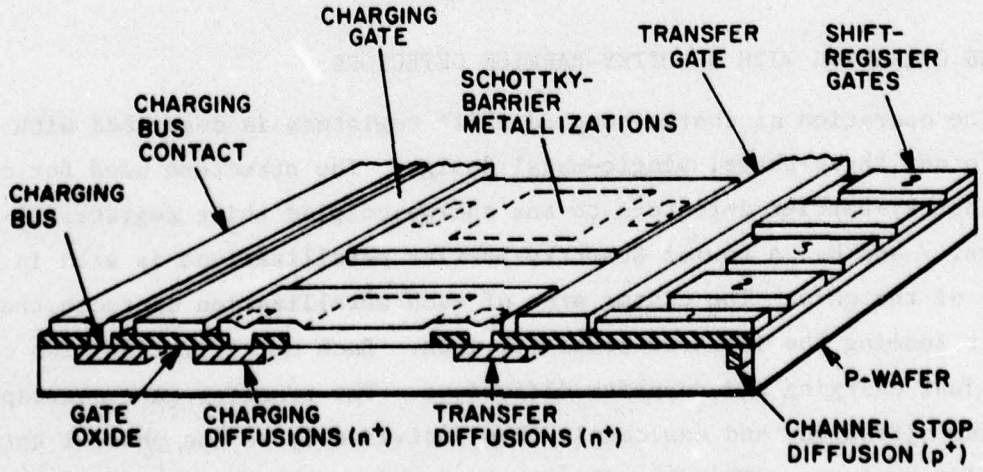


Figure 7. Structure used to couple Schottky-barrier detectors to the charge-coupled shift register.

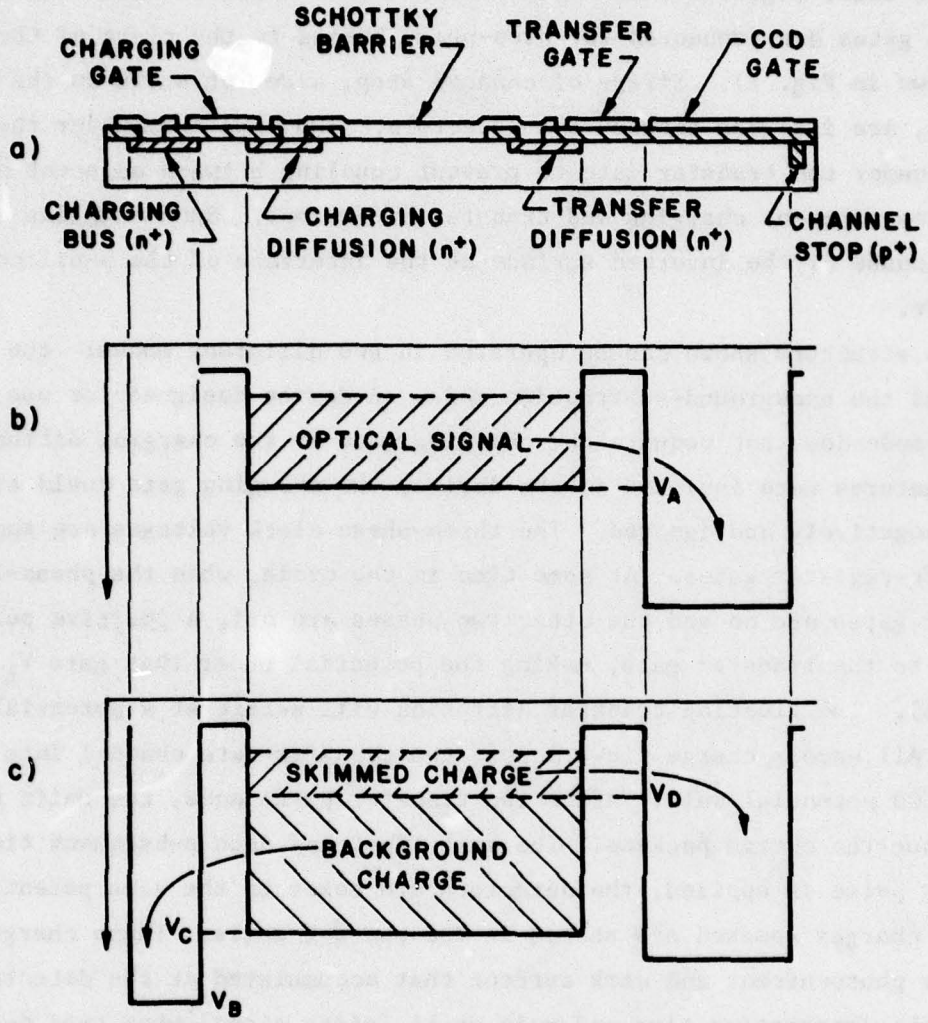


Figure 8. Electron potential-energy profile of IR-CCD during operation: (a) cross section of device; (b) potential profile during operation in the Vidicon mode; (c) potential profile during operation in the background-subtraction mode. (Some details were omitted to aid clarity.)

gates for just this reason. The charging gate on the left of the detectors overlaps the individual charging diffusions and can couple them all at once to the charging-bus diffusion. A channel-stop diffusion at the right terminates the shift-register channel, as shown in the illustration. The shift-register gates are connected to three-phase busses to the right of the channel (not shown in Fig. 7). Strips of channel stop, also not shown in the illustrations, are included between the detectors. They run from under the charging gate to under the transfer gate to prevent coupling between adjacent detectors or between adjacent charging and transfer diffusions. Such coupling could occur because of the inverted surface at the interface of the p-silicon and its oxide.

The structure shown can be operated in two different modes: the Vidicon mode, and the background-subtraction mode. A device designed for use in the Vidicon mode does not require the charging gate or the charging diffusion. If these features were included in the device, the charging gate could simply be biased negatively and ignored. The three-phase clock voltages are applied to the shift-register gates. At some time in the cycle, when the phase-1 shift-register gates are on and the other two phases are off, a positive pulse is applied to the transfer gate, making the potential under that gate V_A, as in Fig. 8(b). The floating transfer diffusion will settle at a potential equal to V_A. All excess charge flows across the transfer-gate channel into the deeper CCD potential well. After the transfer pulse ends, the shift register clocks out the charge packets. The next time, and each subsequent time, the transfer pulse is applied, the detectors are reset to the same potential, V_A, and the charges removed are stored in the phase-1 wells. These charges represent the photocurrent and dark current that accumulated at the detectors during the integration time and made up the video signal when read out. This mode of operation is somewhat different from that used in interline devices with photogates [1], where all minority carriers are removed from the detectors during the transfer time. It is more closely related to the mode of operation of a Vidicon tube, since the detectors are reset to the same potential each frame; the charge removed to do this makes up the video signal: hence, the designation, *Vidicon mode*. An imager designed for use in this mode should have detectors whose charge-storage capacity is about the same as that of a shift-register well.

During the transfer process, it is important for the phase-1 well to be large enough to hold the full detector charge without its surface potential rising above V_A. If necessary, phase-2 can be pulsed on during the transfer time to ease this requirement by sharing the transferred charge. Once the transfer pulse is over, any single well can hold the entire charge packet because there is no longer the requirement that the surface potential at the well be greater than V_A.

A major advantage of the Vidicon mode of operation is the insensitivity of this mode to variations in MOS threshold under the transfer electrode and to variations in detector capacitance. Variations in MOS threshold will cause different detectors to be set to different potentials, but each detector is set to *its* same potential each frame. The charge packet removed represents the optical signal at that detector, independent of both gate threshold and detector capacitance. Other modes do not have this immunity from processing variations. This is discussed further in Appendix A.

V. DESIGN, FABRICATION, AND CHARACTERIZATION OF THREE-PHASE, SINGLE-METALLIZATION IR-CCDs

A. LAYOUT

Our first IR-CCD was a 64x1 linear CCD with gates 0.52-mil long in the direction of charge transfer and with 0.08-mil gaps. The repetition length is thus 1.8 mil per bit, and the channel is 5.0 mil wide. The Schottky-barrier contact holes are 5.0-mil x 0.9-mil rectangles and are spaced on 1.8-mil centers along the CCD register, so that each detector can load into a phase-1 CCD gate when the transfer gate is clocked. There is a source diffusion with loading gates at one end of the shift register and a resettable floating diffusion connected to an on-chip MOS transistor at the other end. Numerous other devices are on the chip, including alignment marks, photolab marks, level numbers, devices for measuring metal resistivity, diffusion resistivity, diffusion lateral spread, channel-stop threshold, MOSFET characteristics, etc.

Figure 9 shows photomicrographs of the two ends of a completed device on a wafer containing about 50 chips. The vertical white rectangles in a row

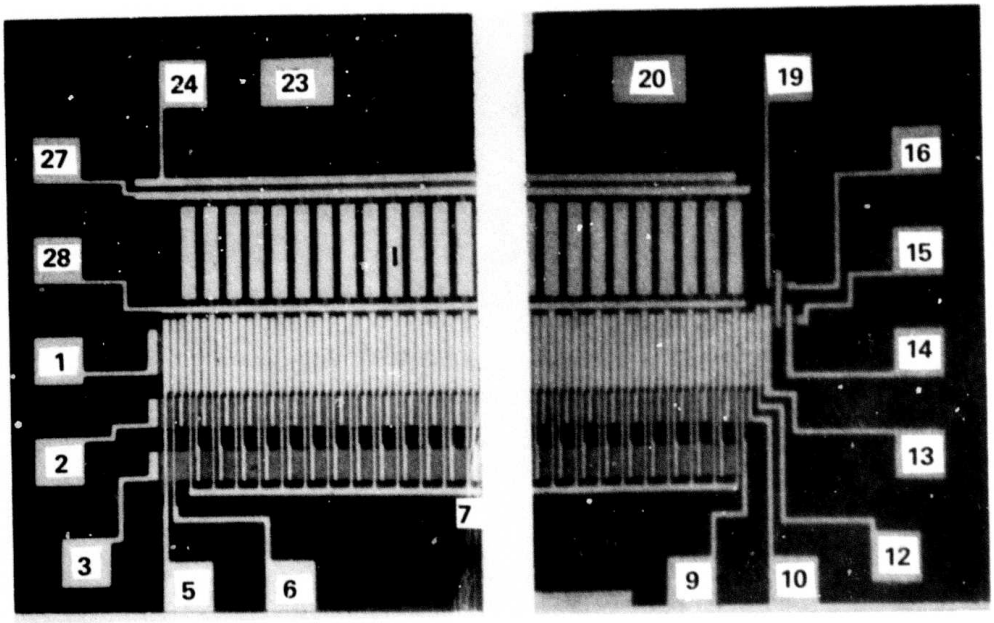


Figure 9. Photomicrographs of the two ends of the CCD chip.

along the top are the Schottky-barrier metallizations, each overlapping the contact holes to the substrate and to the setting and transfer diffusions. The charging gate (27) and the transfer gate (28) control the channels to the charging bus (contacted by 24) and the phase-1 gates (7), respectively. The bonding pad for the phase-1 busbar (7) cannot be seen because it is near the center of the CCD. Phases 2 (3 and 9) and 3 (2 and 10) are double-end connected because they require a diffused crossunder which is more resistive than a metallization. Two separate gates are provided at the beginning (5 and 6) of the shift register and at the end (12 and 13). A source diffusion (contacted by 1) is provided to permit electrical input to the shift register while a floating diffusion with a reset gate (14) and drain (15) is provided at the output. The floating diffusion is connected to an on-chip MOS transistor whose source and drain diffusions are brought out to pads 16 and 19. Contact to the substrate is made at pads 20 and 23, each of which contacts a channel-stop diffusion. The output stage is seen more clearly in the enlargement in Fig. 10. The "L"-shaped floating diffusion is seen to be connected through a contact hole to the gate of the MOS transistor. It is overlapped by the reset gate (14) which controls the channel to the drain (15).

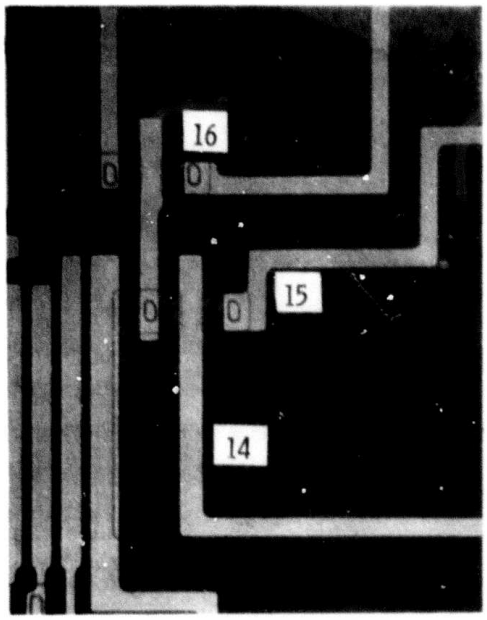


Figure 10. Output section of the CCD chip showing the reset gate (14), the channel drain (15), and the MOSFET (source at 16).

The channel-stop diffusion surrounding these elements could be seen under the microscope but does not show well in this photograph.

B. PROCESSING

For the single-level metallization-type structure with diffused channel confinement, the fabrication procedure is as follows: A p-type, $10^{15}/cm^3$ doped [100] silicon wafer is subjected to a p-type (accumulation) diffusion and an n-type (source-drain) diffusion, each defined by a thermal oxide left after a photolithographic step. The gate oxide is grown, and contact holes are opened. Palladium or platinum is then deposited. Palladium is evaporated onto the wafer in a vacuum system in which the wafer is heated to cause silicide formation. Platinum is deposited in either an E-gun evaporator system or in a magnetron-sputtering system. In either case, a separate sintering bake is required for silicide formation, as well as an anneal to remove damage. All evaporation and sputtering systems must receive special care to avoid sodium contamination; sodium would get into the oxide in ionic form and cause the device characteristics to drift. The remaining noble metal is etched off; then the wafer receives a thin evaporated film of titanium, followed by a film of aluminum. The titanium layer is required because aluminum can react with palladium or platinum silicide. The aluminum is defined photolithographically with an etch that stops at the titanium. The titanium is then etched down to the gate oxide with an etch that does not attack aluminum. Next, a protective SiO_2 layer is deposited, and holes are opened for the bonding connections. The wafers are scribed and diced, and the chips are mounted with epoxy in integrated-circuit holders with holes cut to permit rear illumination. The final step is to bond leads from the bonding pads on the chips to the holder. A summary of the fabrication procedure and mask levels is shown in Table 4. If this were a visible-sensing CCD, it would be necessary to thin the chips to permit rear illumination. This step is not necessary for us since silicon is transparent to infrared radiation beyond 1.1 μm.

C. WAFER TESTING

Several chips were tested for open circuits, short circuits, and diode characteristics. When all of these tests proved satisfactory, it was decided

TABLE 4. PROCEDURAL STEPS IN THE FABRICATION OF SINGLE-METAL, SCHOTTKY-BARRIER INFRARED CCDs

Fabrication Steps

1. Diffuse channel stop (mask 1).
2. Diffuse source and drain (mask 2).
3. Etch contact holes (mask 3).
4. Clean wafer.
5. Evaporate and drive in palladium (or platinum).
6. Remove excess palladium (or platinum).
7. Evaporate titanium and aluminum.
8. Etch pattern in aluminum (mask 4).
9. Etch titanium by use of aluminum as mask.
10. Deposit SiO_2 overcoat.
11. Etch bonding holes and scribe lines in SiO_2 (mask 5).
12. Scribe and cleave wafer.
13. Mount chip in package and bond leads.

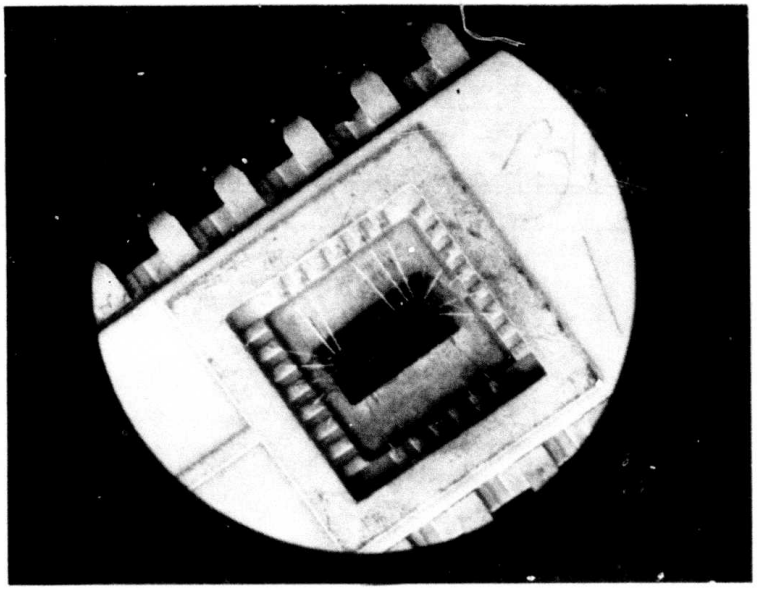
to operate the chips as CCD shift registers with electrical input directly on a probe-card station and to select chips on the basis of CCD performance. About three-fourths of the chips with no obvious visible defects operated well as shift registers. The first run included Pd wafers and Al-only wafers. Since most of the shift registers on the wafers made with palladium worked as well as the devices on wafers made with aluminum only, nothing more was done with the Al-only control wafers. Al-only control wafers were not deemed necessary in subsequent runs.

A 28-pin, gold-plated, ceramic, dual-in-line holder was selected for the chips. After the wafers were scribed and diced, tested chips were mounted

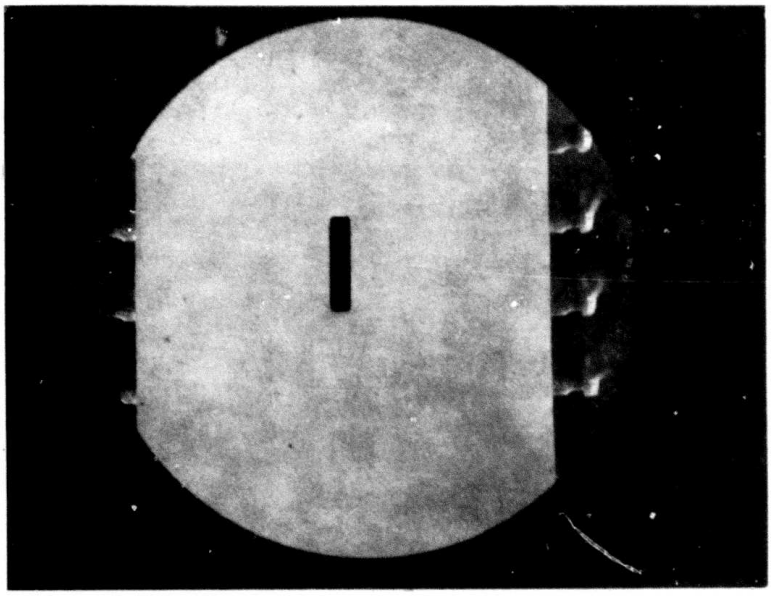
and bonded to the holders which had been previously prepared with 0.120-in. x 0.030-in. rectangular holes ultrasonically ground in the centers of the 0.200-in. square chip-mounting areas. These holes are required for rear illumination with infrared radiation. A bonded chip is shown in Fig. 11(a); the back of the package is shown in Fig. 11(b) with the same magnification. To affix the chip with the detector array directly over the hole, we viewed the chip from the top, as in Fig. 11(a), with a low-power microscope equipped with an infrared image converter in place of the eyepiece. The image converter has an S-1 photocathode that is sensitive to light transmitted by silicon. With illumination from below the holder, we could see the bright rectangular hole in the ceramic masked by the aluminum metallization pattern of the device. All bonded chips were positioned in this manner.

D. OPERATION WITH ELECTRICAL INPUT

A circuit diagram of the IR-CCD chip is shown in Fig. 12. The extra gates G_1 and G_2 were included to make possible various input schemes, notably the charge-preset input. For the measurements reported in this section, G_1 received the burst of pulses while G_2 was clocked in sequence with the line. G_3 and G_4 were provided to allow flexibility in the output circuit. For most of our measurements, G_3 was clocked in sequence with the line; G_4 received a small, positive dc bias; and the reset gate was pulsed. The substrate was biased negatively by a few volts so that the gates always keep the surface inverted. For operation with electrical input, the transfer gate receives a negative bias, isolating the shift register from the detectors. The three-phase, overlapping clock waveforms run continuously. A word-generator circuit runs in synchronism with the clocks and produces a settable number of positive pulses (such as 4) each time it counts a settable number of clock pulses (such as 128). The word is applied to G_1 and is expected at the output 64 clock periods later. Figure 13 shows such an output word with 1/10 of the leading pulse missing. Since there were 192 transfers (64x3), the average transfer loss was about 5×10^{-4} per transfer. To get this fairly good transfer efficiency with a surface-channel CCD, it is necessary to introduce a bias



(a)



(b)

Figure 11. (a) Photograph of a bonded chip. (b) Rear view of holder.

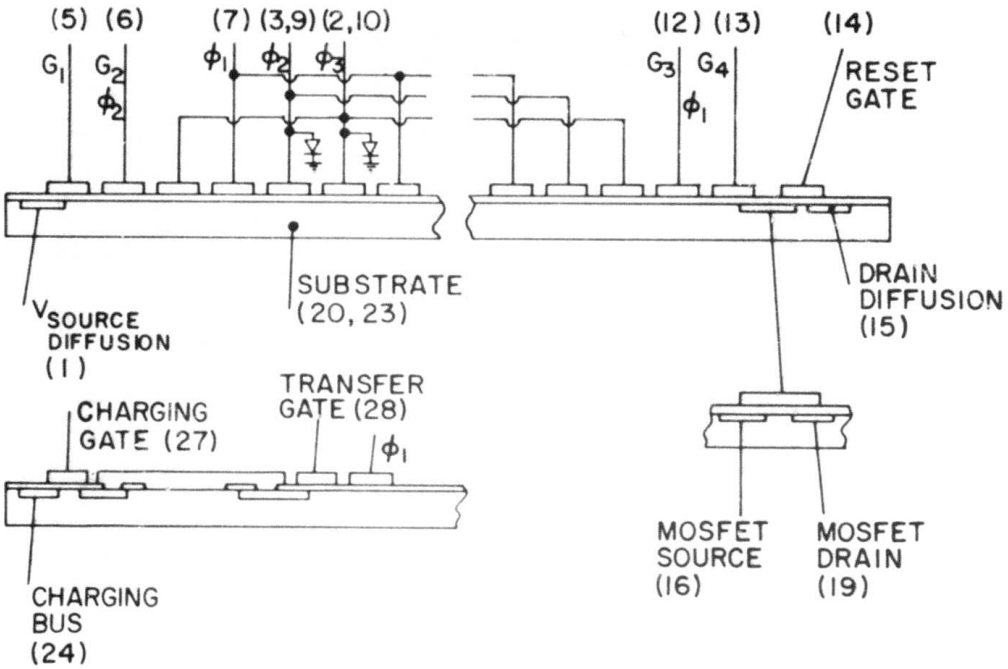


Figure 12. Circuit diagram of the three-phase IR-CCD chip.

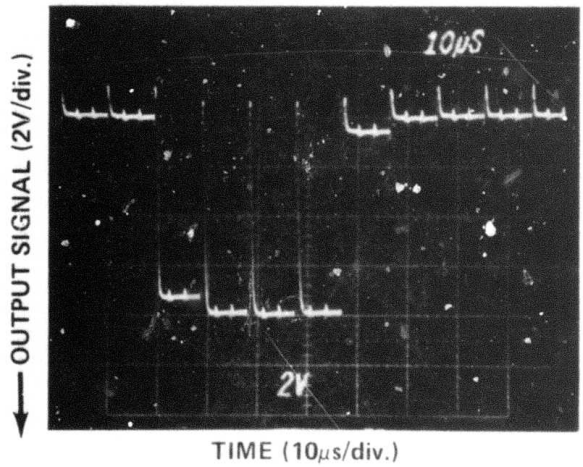


Figure 13. Output word for a 4-bit electrical input.

level or "fat zero." For our chip running at 250 kHz, the optimum bias level was experimentally determined to be 0.3 μA. The output signal is taken from the MOS transistor, whose gate follows the potential of the floating diffusion. The MOS transistor can be wired as a source-follower or as a common-source amplifier, depending on which polarity of output signal is desired.

VI. DESIGN, FABRICATION, AND ELECTRICAL OPERATION OF THE DOUBLE-POLYSILICON, AREA-ARRAY CHIP

A. DESIGN OF THE 25x50 IR-CCD

Design considerations for an area array are different from those for a line array because of the need to minimize the size of the unit cell in both dimensions. A single level of metal permits little design flexibility, as it requires diffused crossunders and their associated contact holes for any but the simplest structures. This approach wastes area. The 2D array was therefore made with overlapping gates consisting of two levels of polysilicon strapped by aluminum. Sealed-channel (gapless) structures, in general, give better transfer efficiency and better device stability. The levels of polysilicon are individually oxidized immediately after definition. Contact holes are made in both levels of polysilicon and in the gate oxide all in one step, and silicide is formed in all contact holes in one step. Barriers are thus formed where the undiffused substrate is contacted. Ohmic contacts are formed in the holes at the two levels of polysilicon and at source-drain diffusions in the substrate. An aluminum metallization and definition step straps the conductors together and completes the device.

An outline of the 2D array is shown in Fig. 14. It is an "interline" system, in which all the detectors transfer their signals into the shift registers at once in response to a pulse on the transfer gate. The column registers are then clocked down one bit, bringing the charge packets from the bottom row of detectors into the horizontal register. The latter is then clocked out, producing one horizontal line on the display. The column registers are subsequently clocked down one bit for each row of detectors. When the entire array has been read out in this manner, the transfer gate is pulsed again, loading the next frame. A natural consequence of this layout (as seen in Fig. 14) is that the detectors are spaced more closely in the vertical than in the horizontal direction. The channel width must be minimized for this reason as well as for area utilization. Wiring the clock gates for two-phase operation would simplify the gate bussing but would limit the well capacity. It would also create a conflict between the substrate doping required for efficient two-phase operation and the substrate doping required for the detectors. We must, therefore, bus out the clock gates for four-phase

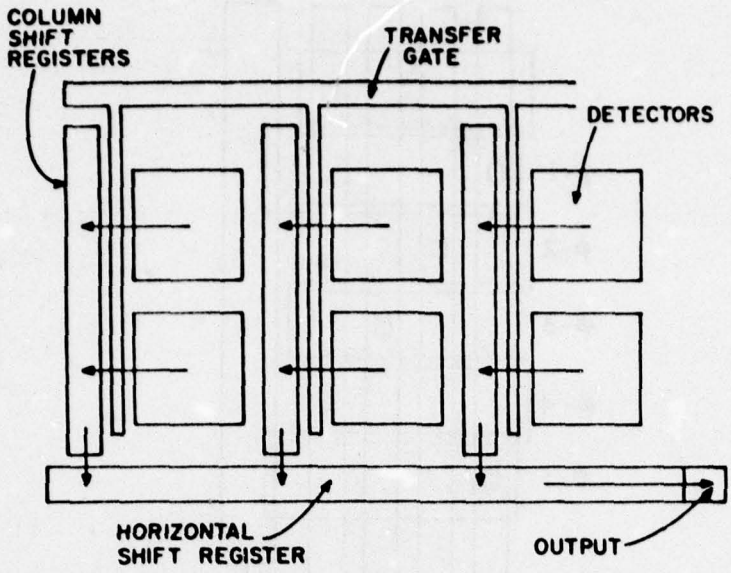


Figure 14. Interline-transfer scheme for the two-dimensional array.

operation. Connecting the gates horizontally across the chip between the detectors wastes detector area. We have worked out designs with the gates bussed vertically for each column, on each side of the channel; although such a design is a big improvement, the columns are still wider than we should like them to be. The design we adopted is unique and is outlined in Fig. 15. A scale drawing is shown in Fig. 16. The overlapping, four-phase gates for each column are defined and strapped separately by use of the two layers of polysilicon and the one layer of aluminum. The channel and transfer gates, with overlapping clock busses, are about 3 mil wide. The detector holes are about 2.5-mil square, and are spaced 3.2 mil apart vertically and 6.4 mil apart horizontally. Twenty-five percent of the repeated area is used for infrared detection. The 3.2-mil vertical bit length corresponds to gates 0.8 mil long in the direction of transfer. While these gates are relatively long, they present no problem at clock rates of a few hundred kilohertz. We could get faster performance with eight gates per detector, each 0.4 mil long, but there would not be enough room for good contact holes when strapped as in Fig. 15.

Detailed drawings of two other parts of the array are shown in Figs. 17 and 18. Figure 17 illustrates how charge is transferred from the column registers to the output register. The last two gates of the column registers are

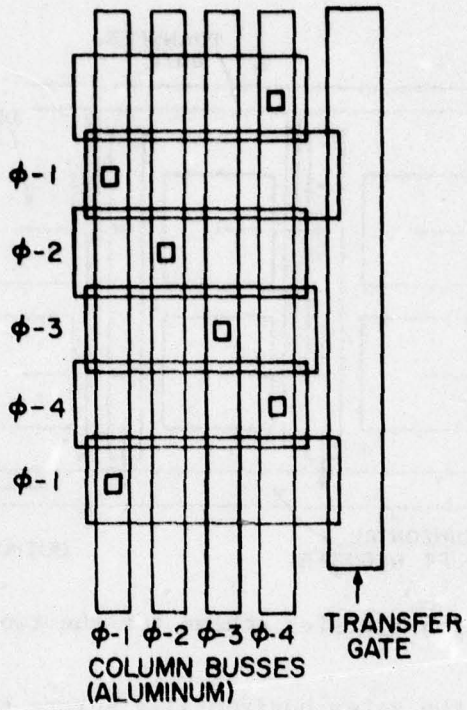


Figure 15. Connection of gates in a typical column. The column straps are themselves bussed across at the top. The transfer gate and the phase-2 and -4 gates are first-level polysilicon, while the phase-1 and -3 gates are second-level polysilicon.

bussed separately, as shown. Figure 18 illustrates the output section. The output-register channel terminates in the U-shaped, floating diffusion and the drain diffusion. Connected to the floating diffusion is the gate of an MOS transistor fabricated at the same time as the array. This array with 25x50 detectors is a square 160 mil on a side, and fits on a 230-mil square chip leaving room for the peripheral structures, a line array, and test devices. There were practical reasons for not including an input circuit to the columns in this device. Both the charging circuit for background subtraction and the input circuit for frame comparison are included in the one-dimensional IR-CCD being fabricated on the same chip. This is discussed below.

B. DESIGN OF THE 62x1 LINE ARRAY

A line-array imager consisting of 62 Schottky-barrier detectors adjacent to a four-phase, double-polysilicon shift register was designed on the same chip as the 25x50 imager and was fabricated together with it. This line

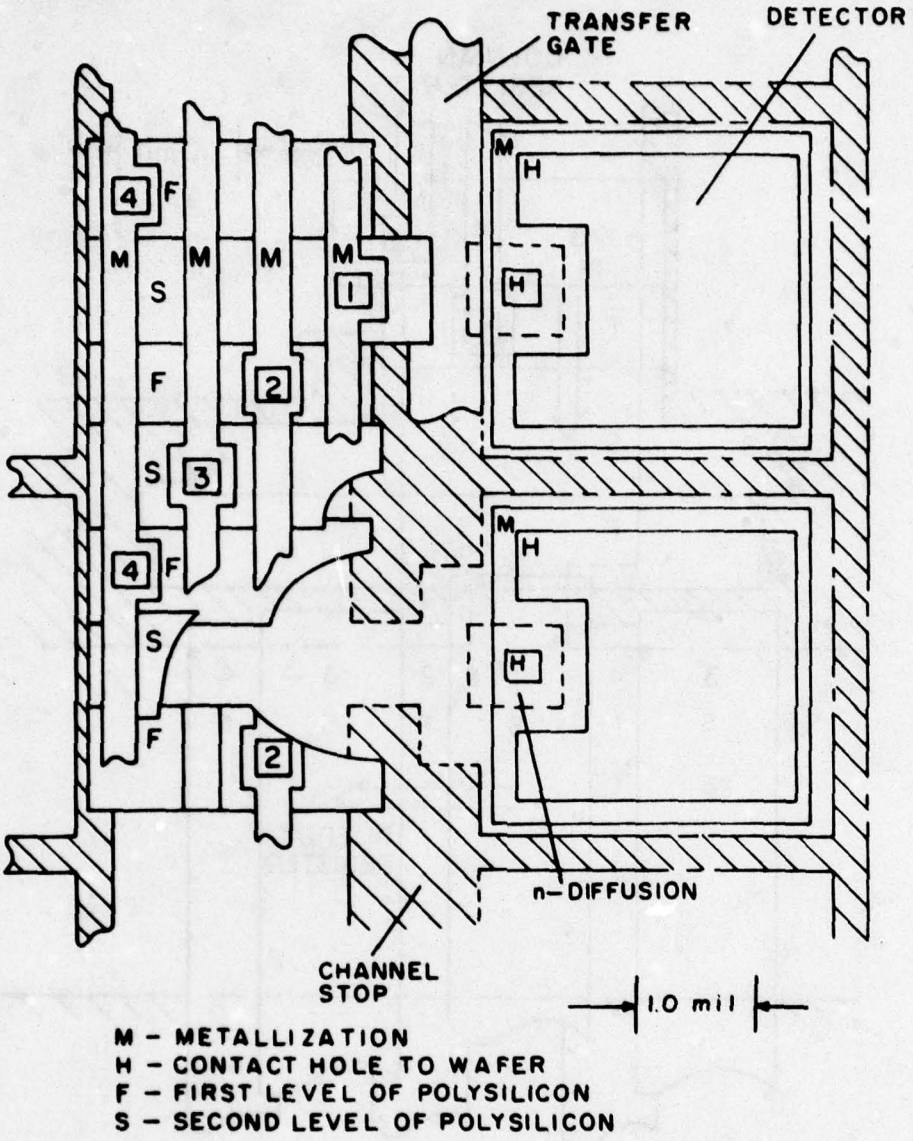


Figure 16. Scale drawing of vertical shift register adjacent to two detectors. The source-drain diffusions are shown as dashed lines, while the channel-stop diffusions are crosshatched. Hidden lines are omitted for clarity, but are shown in cutaway section. The solid polygons are labeled according to the key in the figure.

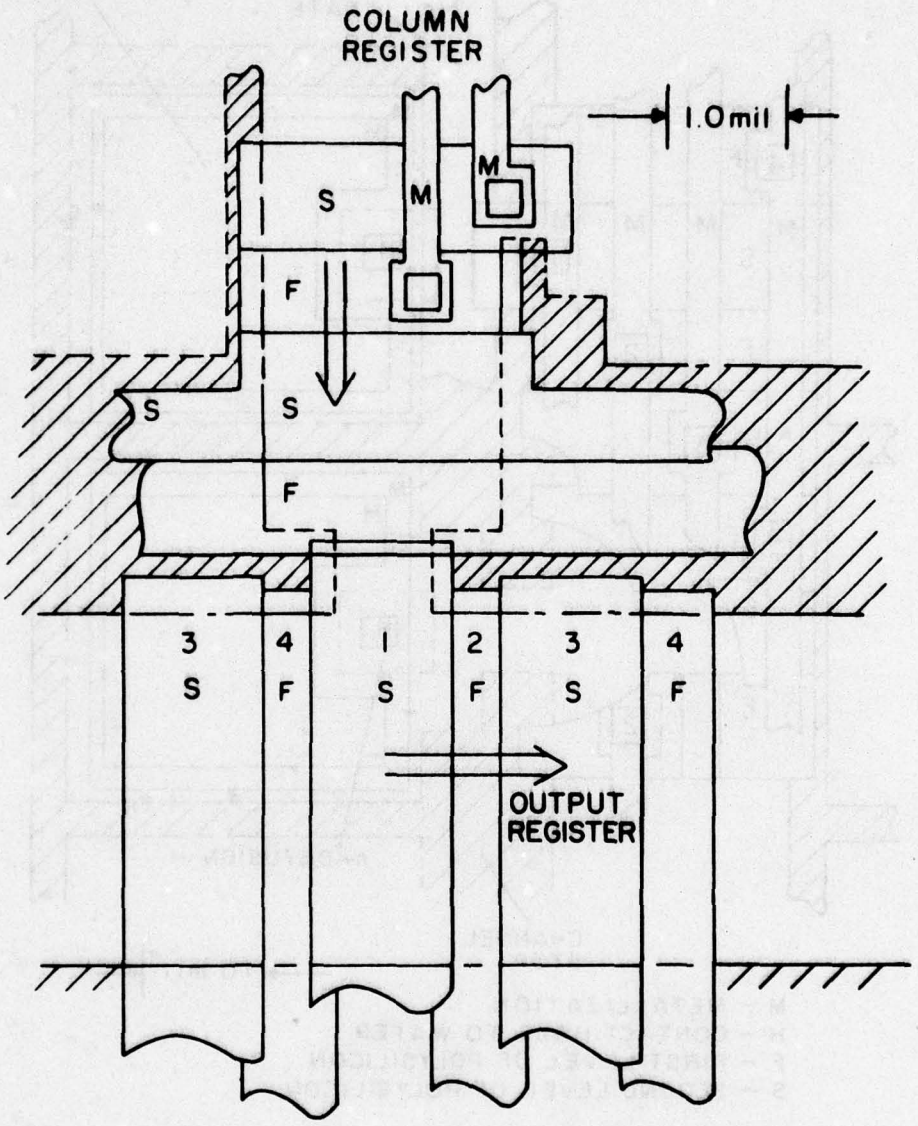


Figure 17. Scale drawing of column-register to output-register transfer structure. Hidden lines are deleted for clarity, except for the channel-stop diffusion which is crosshatched where not hidden. The solid polygons are identified as in Fig. 16. Arrows indicate the direction of charge flow.

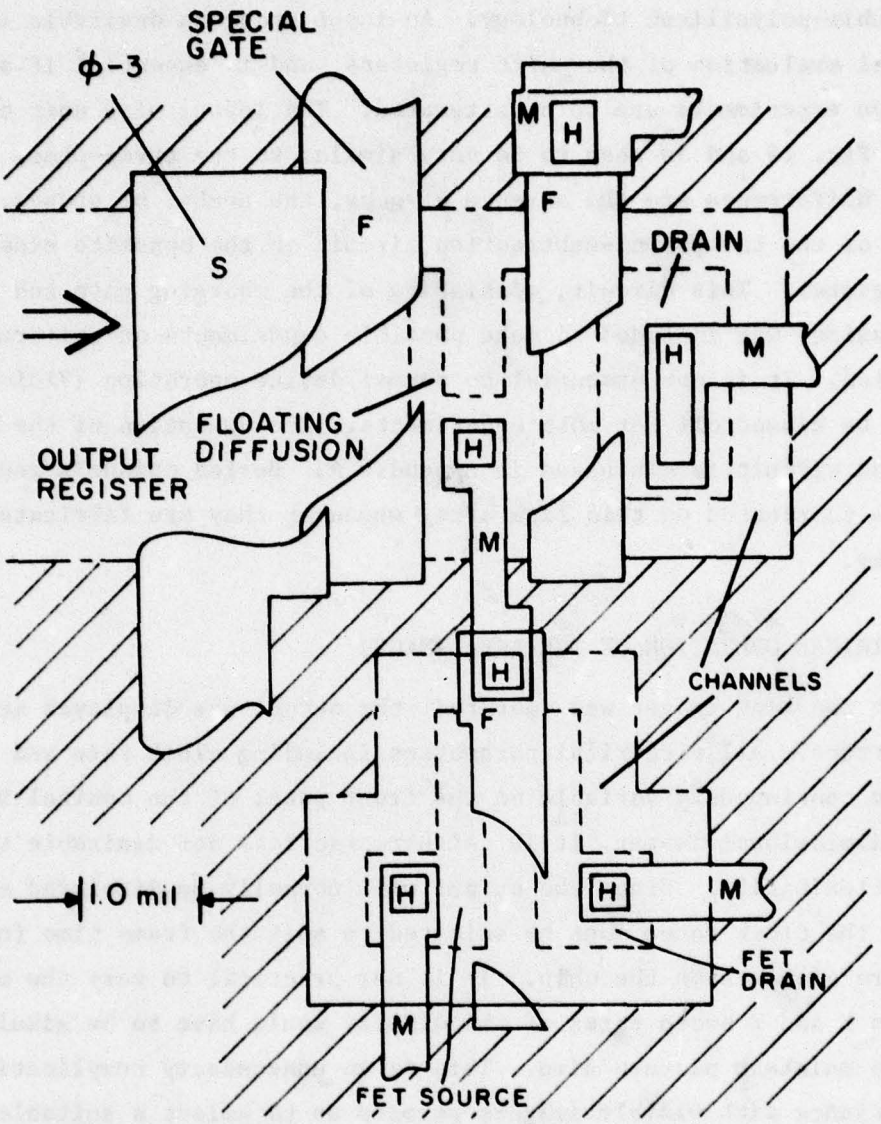


Figure 18. Scale drawing of the output section. The channel-stop diffusion is crosshatched; all hidden lines are deleted.

array was made to provide a device with an input diffusion made in the present, double-polysilicon technology. An input stage is desirable in the electrical evaluation of the shift registers, and is essential if any frame comparison experiments are to be attempted. The layout of a unit cell is shown in Fig. 19 and is seen to be very similar to the three-phase structure. The main differences are the absence of gaps, the number of phases, and the presence of the background-subtraction circuit on the opposite side of the shift register. This circuit, consisting of the charging gate and the charging diffusion, was included to make possible experiments on uniform-background subtraction. It is not essential to normal device operation (Vidicon mode) and will be biased off for most experiments. The operation of the uniform-background circuit is discussed in Appendix A. Buried channels and guard rings are fabricated on this line array whenever they are fabricated on the area array.

C. ELECTRICAL OPERATION OF THE AREA IMAGER

When the line imager was operated, the output was displayed as an oscilloscope trace. All electrical parameters including clock rate and integration time were continuously variable on the front panel of the control box. For the two-dimensional imager, it is neither practical nor desirable to build in so much flexibility. Since the output will normally be displayed as a TV picture, the clock rates must be selected to suit the frame time for the number of picture elements on the chip. It is not practical to vary the clock rate since the X and Y sweep rates of the display would have to be simultaneously varied to maintain picture size. This is an unnecessary complication, since our experience with visible imagers permits us to select a suitable format. We have chosen to run the chip (and hence, the display) at a 60-Hz frame rate. Thus, the *minimum* integration time will be 1/60 s. A longer integration time is achieved by leaving additional time between frames, but the time required to read out a frame (hence, the clock rate) is never changed. We determine the additional time by continuing to count the master clock even after a frame has been completed, and by beginning the next frame when the preset count is reached. Thus, it will be possible to set the integration time to 2^n x (1/60) s, ranging from (1/60) s to many seconds. At (1/60) s there will be no observable flicker in the display. While a standard TV monitor has a 60-Hz frame

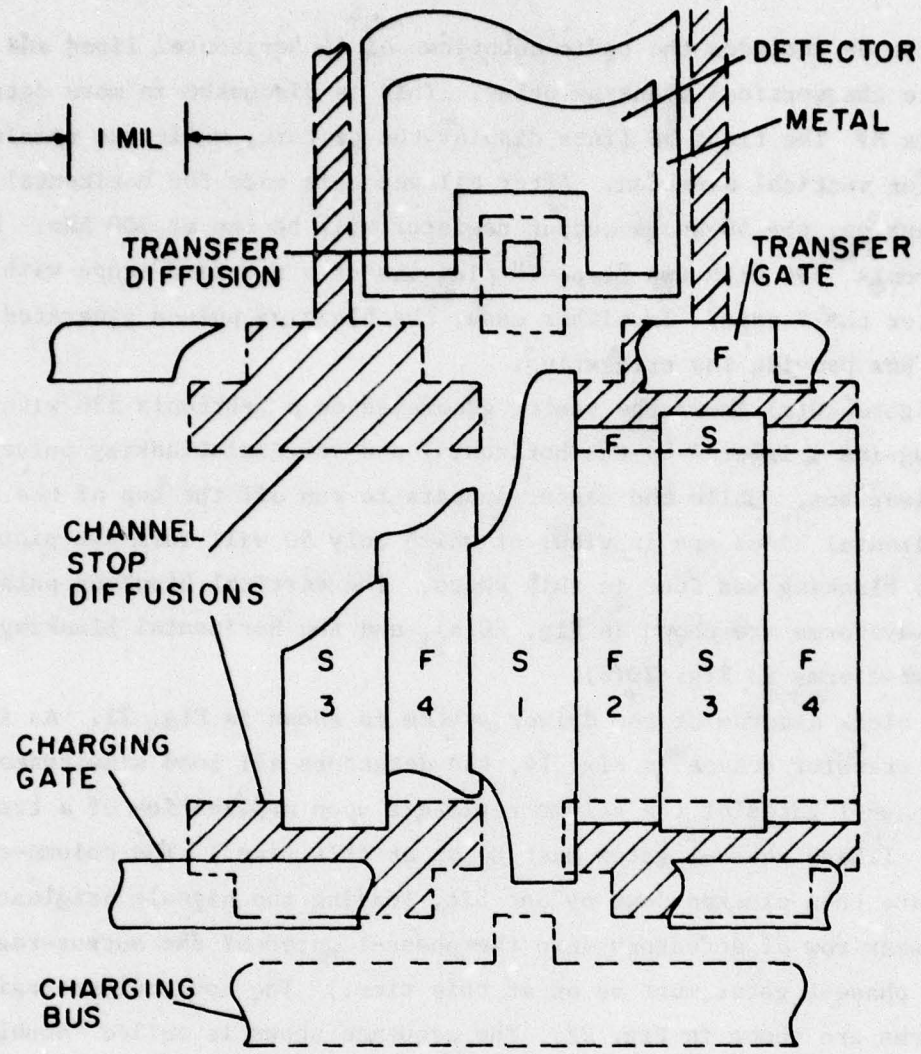


Figure 19. Scale drawing of one stage of the 1D line array. The gates are drawn broken to reveal the diffusions. The design is symmetrical about the phase-1 gate.

rate, it scans each line in 64 μs, a value not easily changed. Allowing for reasonable overscan, the 50-stage output register would be required to run at 1 MHz, a speed somewhat fast for a CCD with gates 0.8 mil long. Furthermore, the CRT beam would be on only a small fraction of the time. We prefer to make the line time LT as long as possible, namely,

$$LT = \frac{\text{minimum frame time}}{68} = \frac{(1/60)\ \text{s}}{68} = 245\ \mu\text{s}$$

where the 68 includes the basic countdown of 64 horizontal lines and 4 more to generate the vertical blanking pulse. This is discussed in more detail in Appendix B. The first 50 lines display the picture, while the remaining ones allow for vertical overscan. After allowance is made for horizontal overscan and blanking, the 50-stage output register will be run at 300 kHz. We can use a Tektronix* 536 with two "type-T" plug-ins or a standard scope with a special sweep for the Y axis. In either case, the blanking pulses generated in our driver box provide the triggering.

Figure 20(a) shows the raster generated on a Tektronix 536 with the two "T" plug-ins triggered by the horizontal and vertical blanking pulses from our driver box. While the raster appears to run off the top of the screen, 55 horizontal lines are in view, of which only 50 will form the picture. No display blanking was done in this photo. The vertical blanking pulse and sweep waveforms are shown in Fig. 20(b), and the horizontal blanking and sweep waveforms in Fig. 20(c).

A block diagram of the driver system is shown in Fig. 21. As indicated by the transfer scheme in Fig. 14, the detectors all load simultaneously into phase-1 gates of the column registers upon application of a transfer pulse. (These phase-1 gates must be on at this time.) The column-register gates are then clocked down by one bit, loading the signals originating from the lowest row of detectors into the phase-1 gates of the output-register. (These phase-1 gates must be on at this time.) The four column-register waveforms are shown in Fig. 22. The sequence shown is called "double-clocking" because two of the four gates are always on. In our case, phases 1 and 2 are normally on, except during the column-to-output-register transfer, as shown in Fig. 22. The output register is also double-clocked, as shown in Fig. 23. Output phases 1 and 2 are on when the output register is stopped, to accept the transfer from the columns. Also shown are the waveform S1, used to strobe the input diffusion for charge presetting, and the waveform required by the reset gate. Other details in these figures are discussed in Appendix B.

*Tektronix Inc., Beaverton, Oreg.

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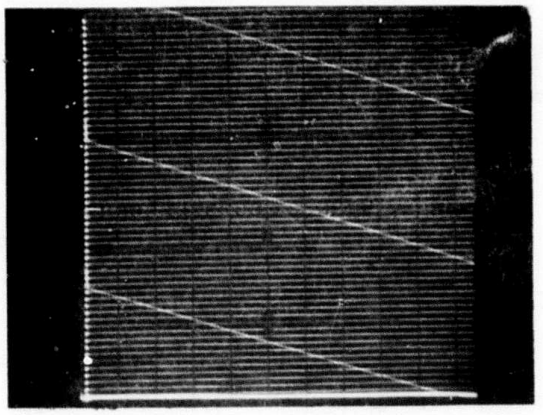
(a)



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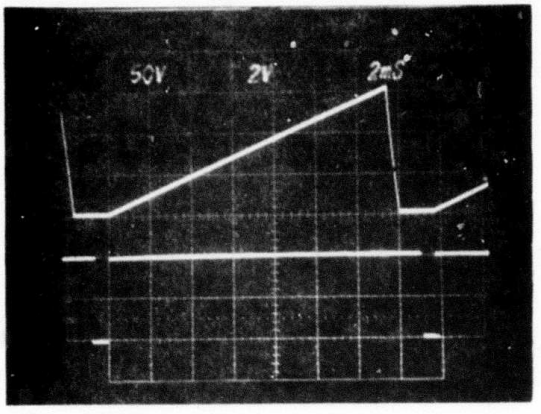

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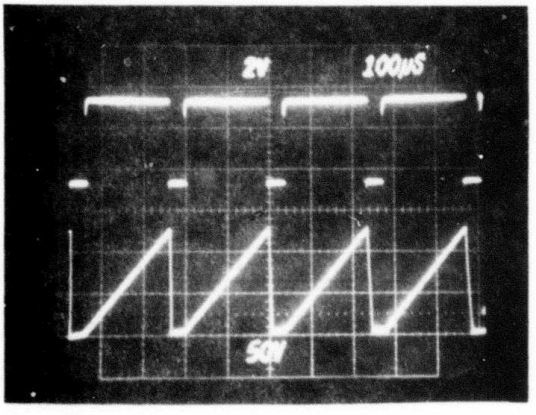

Figure 20. (a) Raster display on Tektronix 536 scope with two "type T" plug-ins, triggered by our blanking pulses and timed to be compatible with our clock rates. (b) Vertical blanking pulse from our driver box (bottom) and sweep waveform. The "type T" plug-in was set at 1 ms/div. The vernier was turned down as far as possible without a loss in triggering. (c) Horizontal blanking pulse from our driver box (top) and sweep waveform. The "type T" plug-in was set at 20 μs/div (CAL).

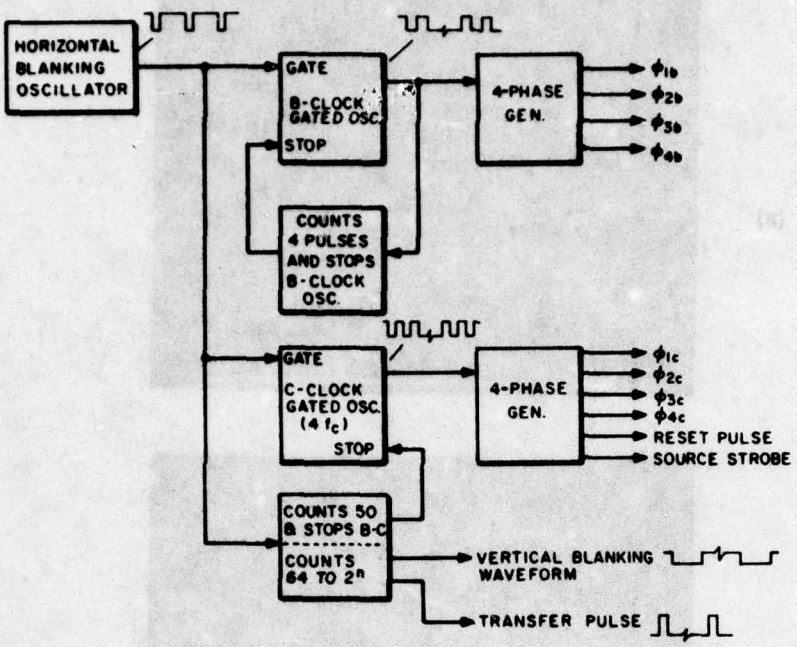

Figure 21. Block diagram of drive circuit. Subscript b refers to the column registers; subscript c, to the output register.

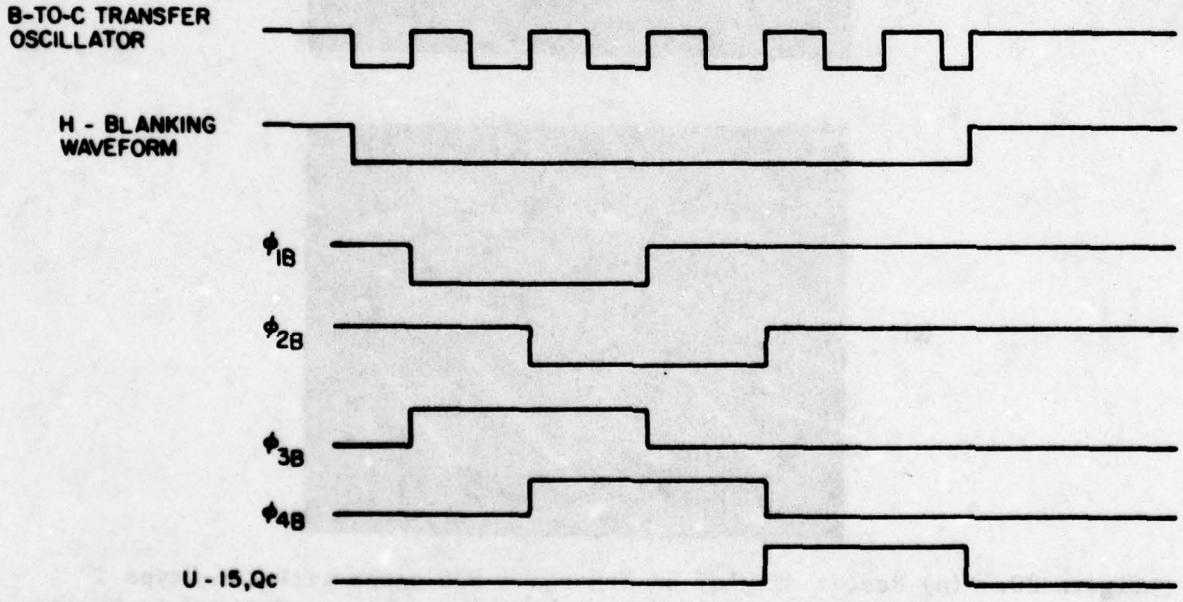

Figure 22. Column-register waveforms during column-to-output-register transfer. Subscript B refers to the column registers.

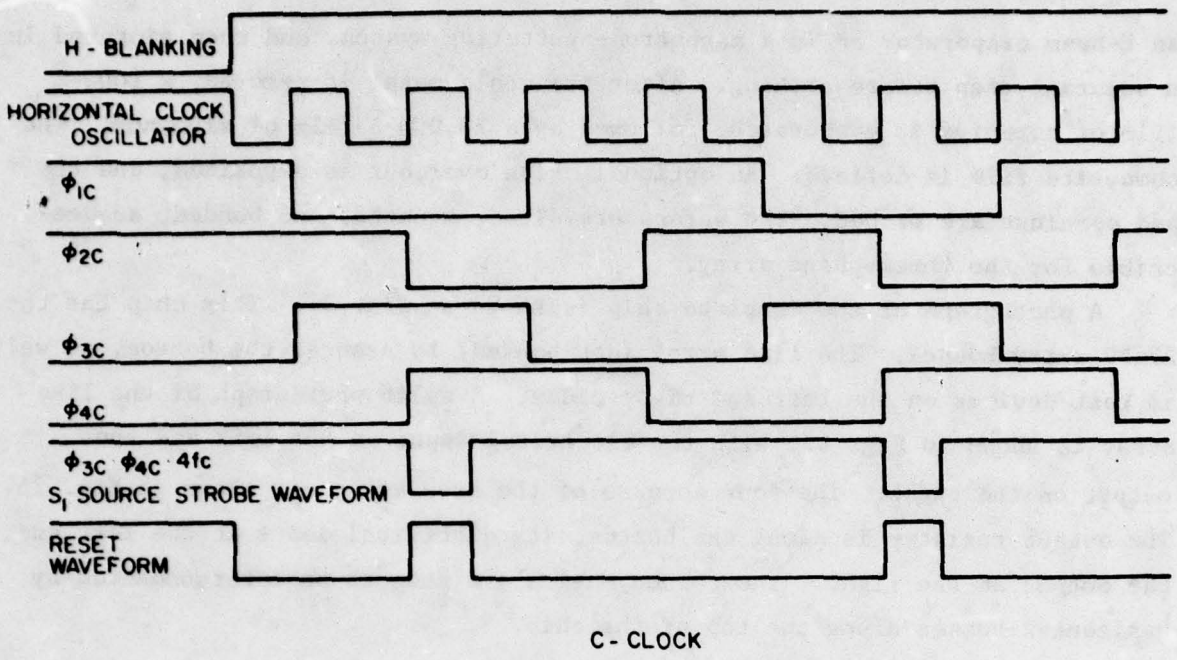

Figure 23. Output-register clock waveforms and auxiliary pulses. Subscript C refers to the output register.

D. PROCESSING OF THE DOUBLE-POLYSILICON TC-1199 CHIP

The double-polysilicon TC-1199 IR-CCD area array was processed with surface-channel shift registers. The Schottky diodes were formed by addition of the silicide-formation step to the double-polysilicon, CCD process previously developed at RCA Laboratories. In this process, six photomasks are used. A seventh is available for defining pad openings in an optional oxide overcoat. The overcoat protects the chips during handling, but is not otherwise required. Because we were concerned about the effect of the overcoat processing on the detectors, some of the wafers were completed without overcoats. In addition to the above seven masks, we have prepared, but not used, five more masks to study various processing options, including buried-channel shift registers and n-type guard rings surrounding the Schottky diodes.

The wafers were 25-50 Ω-cm, boron-doped, p-type [100] silicon, polished on both sides to a final thickness of 0.010 in. by Monsanto. The palladium or platinum silicide is formed just prior to the metallization step in the process. If palladium is selected it is evaporated in a filament evaporator, sintered in vacuum, and subsequently etched. Platinum must be deposited in

an E-beam evaporator or in a magnetron-sputtering system, and then sintered in a separate step before etching. After the noble metal is removed, a 1000-Å film of titanium is evaporated, followed by a 14,000-Å film of aluminum. The composite film is defined. An optional oxide overcoat is deposited, and the pad openings are etched. The wafers are diced, mounted, and bonded, as described for the three-phase array.

A photograph of the complete chip is shown in Fig. 24. This chip has the 25x50 array bonded. The line array (not bonded) is seen at the bottom, as well as test devices on the left and right sides. A split photograph of the line array is shown in Fig. 25, with the electrical input on the left and the output on the right. The four corners of the area array are shown in Fig. 26. The output register is along the bottom, its electrical input at the left and the output at the right. The column busses are seen to be interconnected by horizontal busses along the top of the chip.

E. SHIFT-REGISTER OPERATION

The waveforms used to operate a charge-coupled shift register were shown in Fig. 23. These are the four phases, the source strobe, and the reset waveforms. While the figure is identified with the output register in the area array, the waveforms are equally applicable to the line array. The input section of a typical shift register is sketched in Fig. 27(a); the electron-potential-energy profile, in 27(b). The charge-preset input requires dc on the two auxiliary gates G_1 and G_2, so that a pocket will form at G_2 when phase 1 is off. Just before phase 1 goes on, the source voltage is strobed low (up in Fig. 27(b)), filling the pocket at G_2. It returns to the "off" position, skimming the charge in the G_2 well at the level of V'_{G1}. (Primed quantities refer to surface potentials rather than their corresponding gate voltages.) An electrical word consisting of N bits can be inputted by increasing the voltage on G_2 for a length of time that includes N strobe pulses. The output from a line-array shift register is shown in Fig. 28. Transfer efficiency as high as 0.9999 ($\varepsilon = 10^{-4}$) per transfer has been observed in this manner with these chips.

In Fig. 27, G_2 and the first ϕ_1 gate are shown as longer than the others. This is necessary in order to input a full well because the G_2 and first ϕ_1

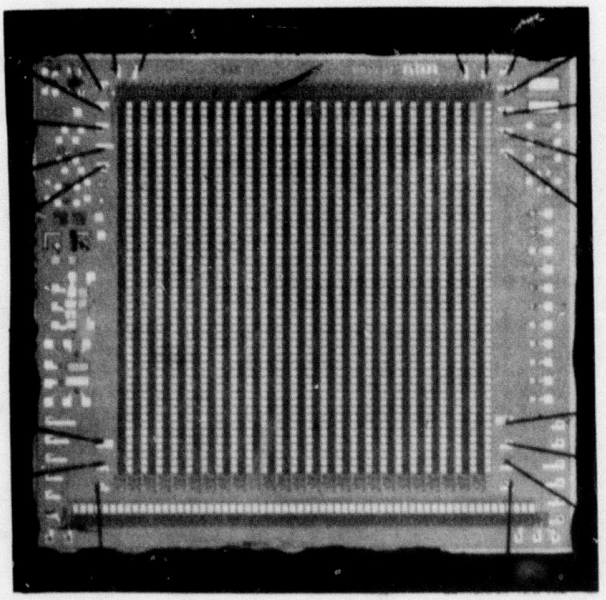

Figure 24. Photograph of full chip with 25x50 area array (center) and 62x1 line array (bottom). Magnification = 13.8X (photo reversed).

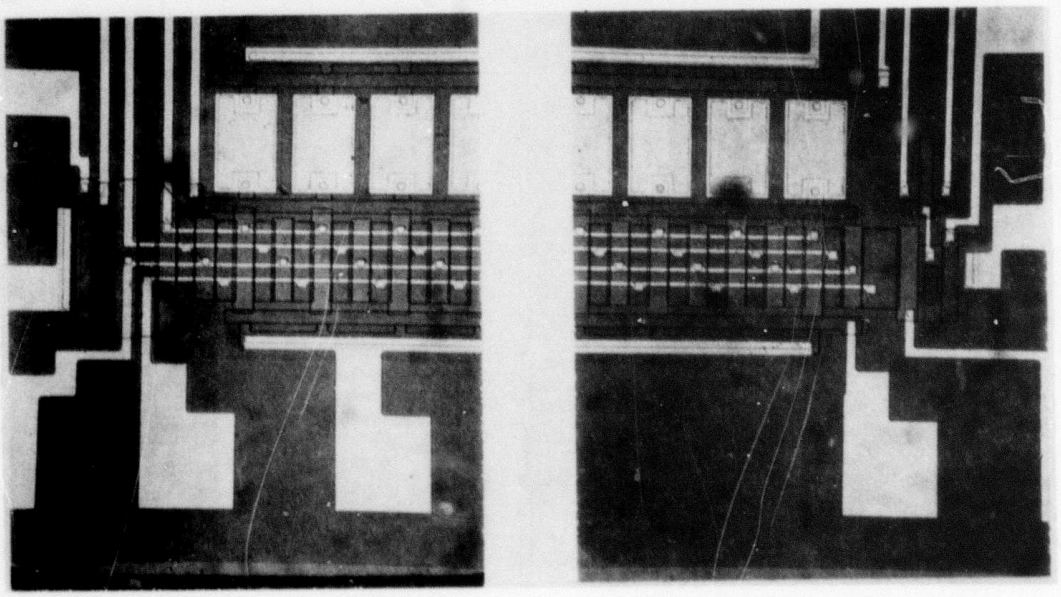

Figure 25. Photograph of ends of 62x1 line array (144X).

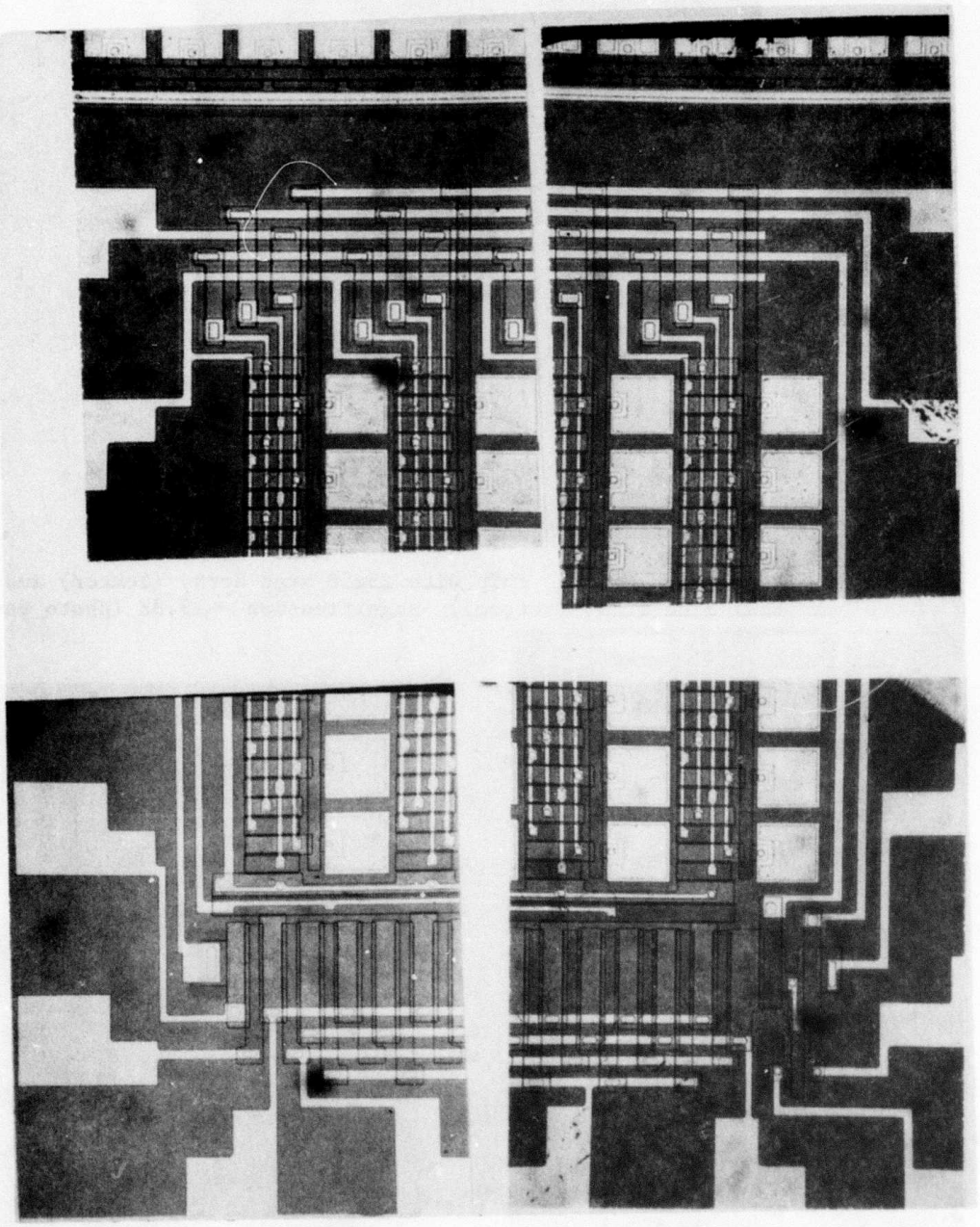

Figure 26. Photograph of four corners of the 25x50 area array.

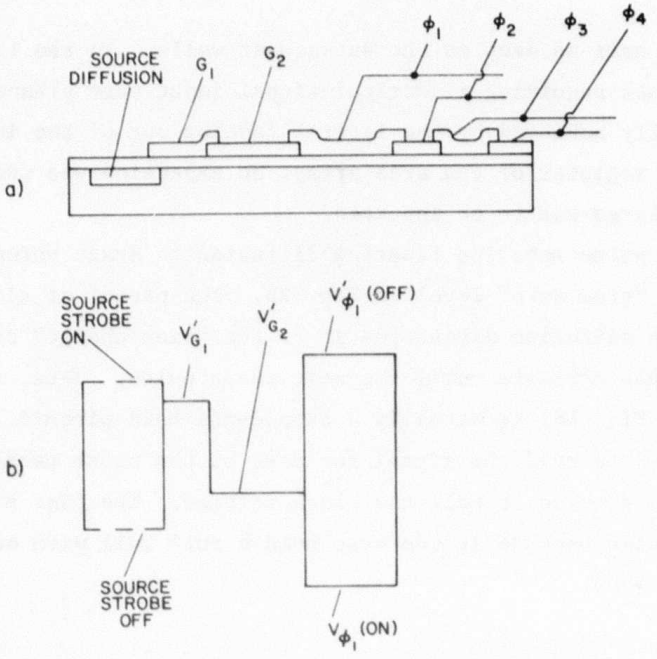

Figure 27. Charge preset input: (a) cross section of charge-coupled shift register at input and (b) corresponding potential-energy profile.

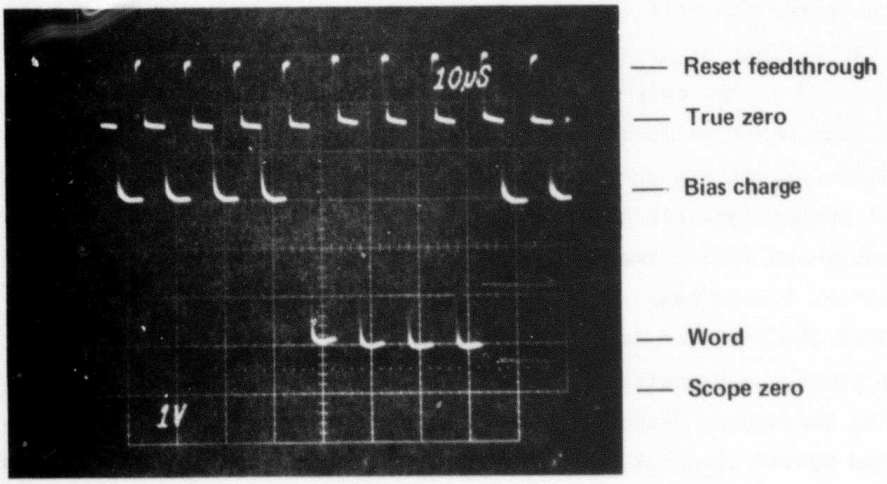

Figure 28. Four-bit word transferred through line-array shift register. The signal is sensed at the emitter-follower output.

wells are only half as deep as the subsequent wells. In the line array for which experiments requiring electrical-signal input were planned, the extra area was actually achieved by the lateral fanning out of the input section. For the output register of the area array, no expansion was needed, since only a small bias charge was to be inputted.

The reset pulse sets the floating diffusion to drain potential; this appears as the "true zero" level in Fig. 28. The packet of electrons arriving at the floating diffusion discharges it to the "bias charge" or "word" level in Fig. 28. This persists until the next reset pulse. Thus, the output circuit (shown in Fig. 18) is actually a sample-and-hold circuit. The timing could be altered to hold the signal for most of the clock period. The special gate in Fig. 18 gets dc at half the clock voltage. The last shift-register gate (ϕ-3) is wide because it too must hold a full well with only half the usual voltage swing.

F. DARK-CURRENT STORAGE TEST

The mechanisms that create dark current in Schottky-barrier diodes were discussed in a previous section. The magnitudes of the photocurrent and the CCD-well capacity are such that dark currents large enough to be troublesome to the imager can still be too small to measure with a simple DC test device. In order to test process variations for their effect on detector dark current, we included on the chip a test device that simulates the setting and integration conditions under which detectors in the arrays operate. A circuit diagram of the dark-current storage test device is shown in Fig. 29, along with the external connections for the storage test. A photograph of the test device (actually two mirror-image devices, device 1 with aluminum over the silicide and device 2 with bare silicide) is shown in Fig. 30. The maximum voltage (dc) to which the detector is to be set is applied to the coupling drain. A pulse large enough to transfer V_{SET} to the detector is applied to the reset gate G_R, and the subsequent detector voltage is observed on an oscilloscope using the on-chip MOSFET as an emitter follower. The scope trace for a detector made with magnetron-sputtered platinum sintered at 400°C is shown in Fig. 31. The detector is a rectangle 4 mil x 10 mil, and has a diffused guard ring. Fig. 31 shows a fast rate of decay followed by a storage time of about 1 s. The transfer characteristic of the emitter follower (Fig. 32) was measured statically with a

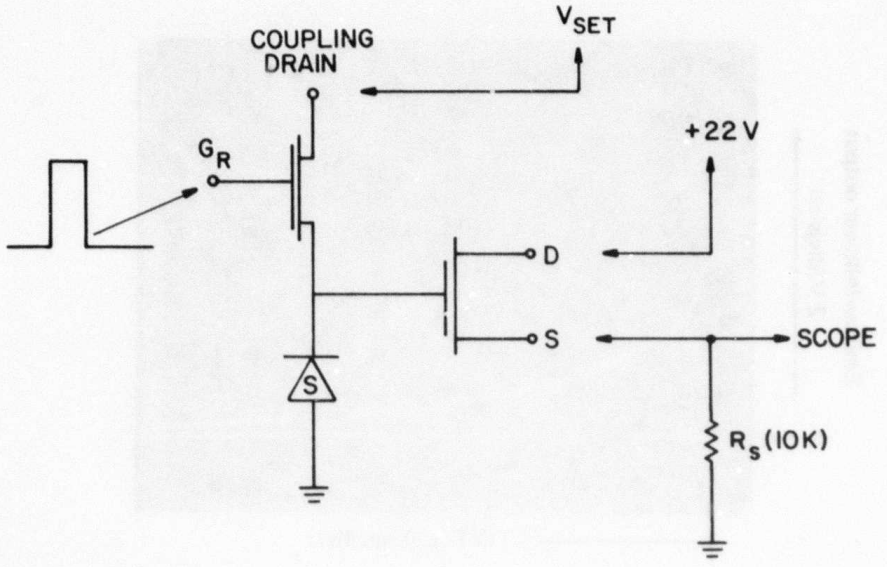

Figure 29. Circuit of dark-current test device.

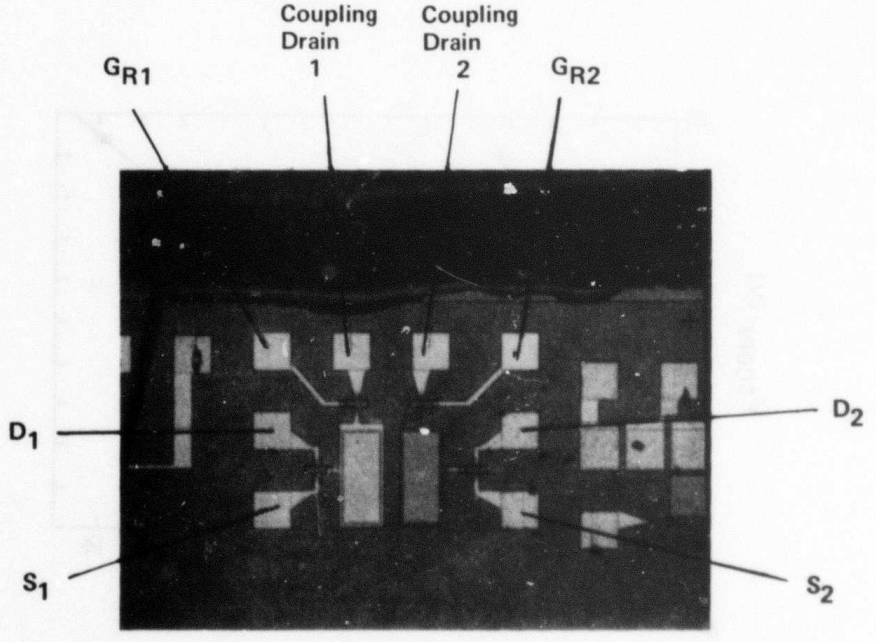

Figure 30. Photograph of dark-current storage test device. The two devices are identical mirror images except that device 1 has aluminum covering the detector.

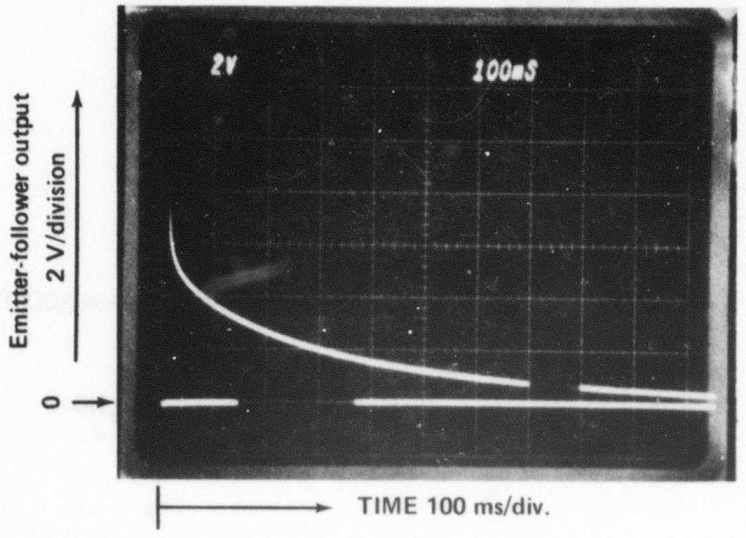

Figure 31. Decay of the voltage on a platinum silicide detector as seen through the on-chip emitter follower. The detector was made with magnetron-sputtered platinum sintered at 400°C.

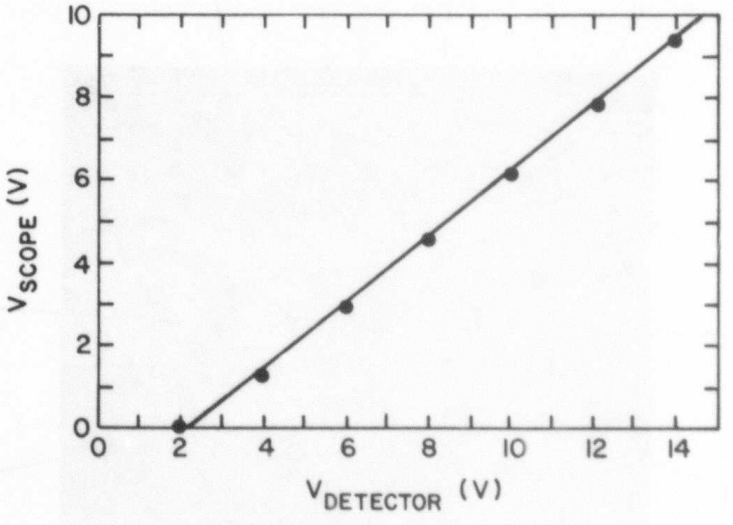

Figure 32. Measured transfer characteristic of the emitter follower in the detector-storage-test device.

large dc bias on the reset gate, so as to give us access to the detector at the coupling-drain connection. The scope voltage at which the rapid decay ends, 4.4 V, thus corresponds to about 7.5 V at the detector. The 2-V offset makes it impossible to follow the detector signal below 2 V. The data in Figs. 31 and 32 were typical of several wafers processed together. No difference was observed between devices with or without the aluminum overcoat.

The observed voltage decay rate is about 5 V/s. The voltage decay anticipated from the theoretical dark current of platinum silicide at 77K is obtained from

$$Q = CV$$

$$\frac{dV}{dt} = \frac{1}{C}\frac{dQ}{dt} = \frac{i}{C} = \frac{4 \times 10^{-13}\ A/cm^2}{3.2 \times 10^{-9}\ F/cm^2} = 1.25 \times 10^{-4}\ V/s$$

Alternatively, the observed decay rate corresponds to a dark current of

$$i_{dark} = C\frac{dV}{dt} = 3.2 \times 10^{-9}\ F/cm^2 \times 5\ V/s = 16 \times 10^{-9}\ A/cm^2$$

This number compares favorably with our estimate of 0.27×10^{-6} A/cm^2 for the maximum-tolerable dark-current density, but further improvement should be possible. Our measurement does not exclude the possibility that the discharge of the detector from 1 or 2 V to zero may take much longer than 1 s.

The switching action of the reset gate is demonstrated in the forward-biased characteristics in Fig. 33(a). Here the reset gate is switched on and off, displaying the Schottky I-V curve and the silicon-diode I-V curve, respectively, both at 77K. The reverse-biased I-V curve is shown in Fig. 33(b). Observable reverse currents (1 nA) began at 16-25 V for the various devices, all with diffused guard rings. Because of the reset transistor, the voltage actually reaching the detector saturates, as does the current. The voltage at which the transistor saturates is somewhat smaller than that applied to the reset gate. It is interesting to note that the breakdown where each curve goes vertical is the silicon-diode breakdown, with the breakdown voltage varying from 59 to 83 V for reset-gate potentials from 30 to 55 V, respectively.

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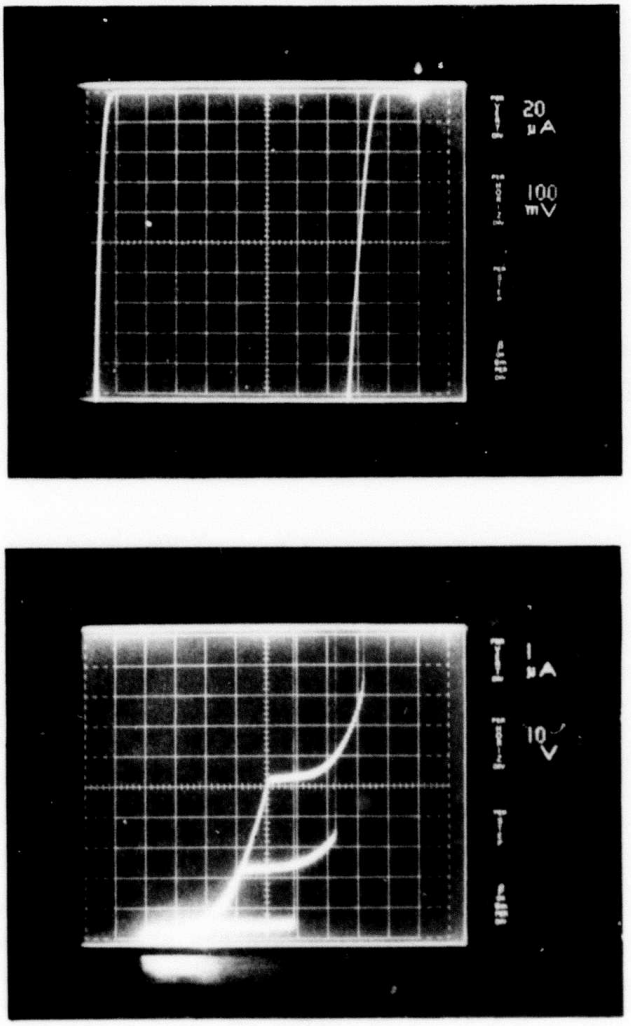

Figure 33. (a) Forward-bias characteristic of detector-storage-test device. The origin is at the top right corner of the solid grid. The Schottky-diode turn-on curve at about 150 mV is seen with a positive bias on the reset gate. The silicon-diode turn-on curve at 1.1 V is seen with a negative bias on the reset gate. (b) Reverse-bias characteristic os the detector-storage-test device at three reset gate potentials: 30, 44, and 55 V. The Schottky-diode characteristic is the curve in the lower left quadrant with its origin at the lower left corner of the solid grid.

VII. INFRARED SENSITIVITY AND IMAGING MEASUREMENTS

A. EXPERIMENTAL METHODS

Infrared imaging measurements have been discussed in the Semiannual Reports (see Preface), demonstrating sensitivity to light of wavelengths longer than 1.7 μm (see also Ref. 17). Sensitivity to thermal radiation from 300K objects was reported as well. These measurements were made with the IR-CCD immersed in liquid nitrogen in a quartz optical dewar. Imaging measurements were made with a Barnes calibrated blackbody source. Quartz windows, however, are not adequate for thermal measurements in the 3-5-μm band, and liquid nitrogen creates experimental difficulties. The more sophisticated and up-to-date infrared measurements that are reported in this section were made at Rome Air Development Center/ET, Hanscom AFB, Mass. [11, 18]. For these measurements an Air Products,* two-stage, helium refrigerator was used. The arrays were cooled in a vacuum and illuminated through a sapphire window. Operating temperatures ranged from 90 to 135K for Pd_2Si arrays and from 80 to 100K for PtSi arrays. Imaging was done with f/6.4 dual Cassegrain optics or with a 3-in., f/1, quadruplet, Ge-Si lens made by SORL.** The array was cold-shielded with a f/1.2 aperture stop. To increase detector sensitivity, CCD clocking voltages were optimized at the operating temperatures, and transfer voltages were increased to just short of Schottky-diode breakdown. Low-level signals required a 10% bias charge to avoid transfer-loss image smear. No bias was required for strong signals. Calibrated illumination was provided by a blackbody source and by an EOI† 4-bar differential target.

B. THERMAL RESPONSE AND NOISE

The thermal response of the PtSi array was measured with the differential-temperature target. Target temperature ranged from below ambient to 100°C.

---

* Air Products & Chemicals, Inc., Allentown, Pa.

** Space Optics Research Labs, a division of Optronics International, Inc., Chelmsford, Mass.

† Electro-Optical Industries, Inc., Santa Barbara, Calif.

17. E. S. Kohn, IEEE J. Solid-State Circuits SC-11(1), 139 (Feb. 1976).
18. F. D. Shepherd et al., "Ambient Thermal Response of a Monolithic Schottky IR-CCD," Proc. IRIS Thermal Imaging Specialty Group Meeting, El Toro, Cal., Feb. 1977.

Experimental results are compared with theory in Fig. 34, where excellent agreement is observed. A similar experiment with a Pd_2Si array showed poor agreement with theory because of optical absorption in a diffused layer on the backside of the substrate. PtSi arrays responded to temperatures less than 1°C above ambient with 30-ms staring time.

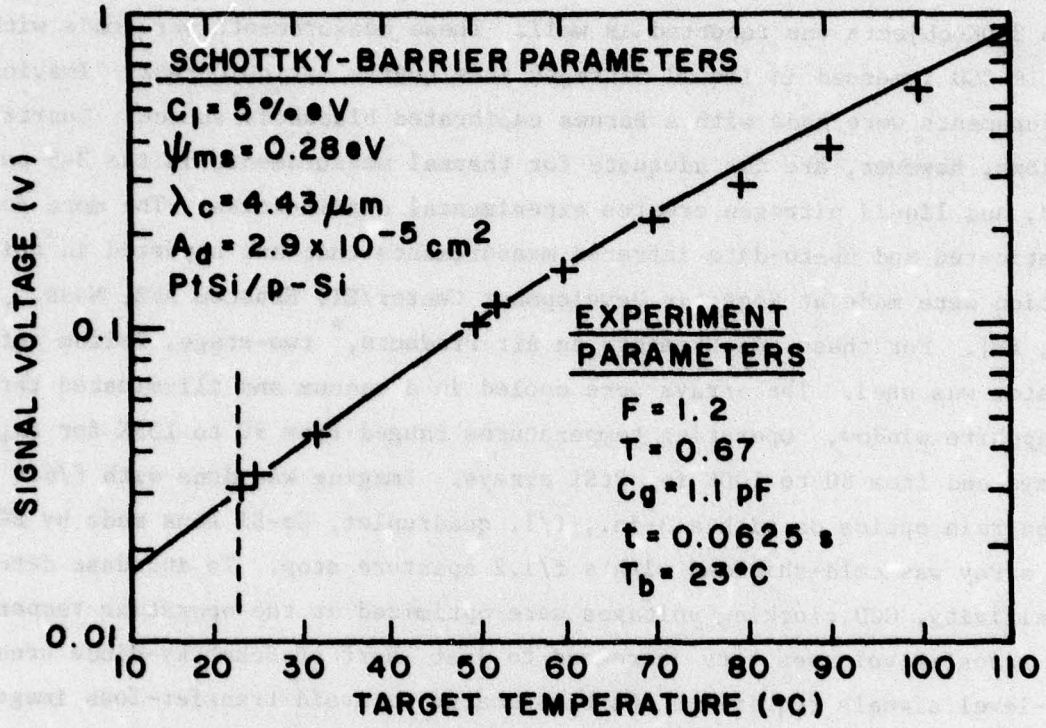

Figure 34. Thermal-transfer response of PtSi/IR-CCD. The solid line is the theoretical curve, with parameters as indicated.

Signal noise was measured with multiple-exposure photographs of the output oscilloscope traces from several detector cells. In order to determine the electron noise level, we measured the floating-gate capacitance (1.1 pF) and assumed that the observed peak-to-peak noise was six times the rms noise. The best Pd_2Si devices had rms noise levels of 1700 electrons when exposed to ambient background, or twice the value prediced in Table 3. The noise increased with signal level to the point where signal shot noise dominated the measurement. These data appear in Fig. 35.

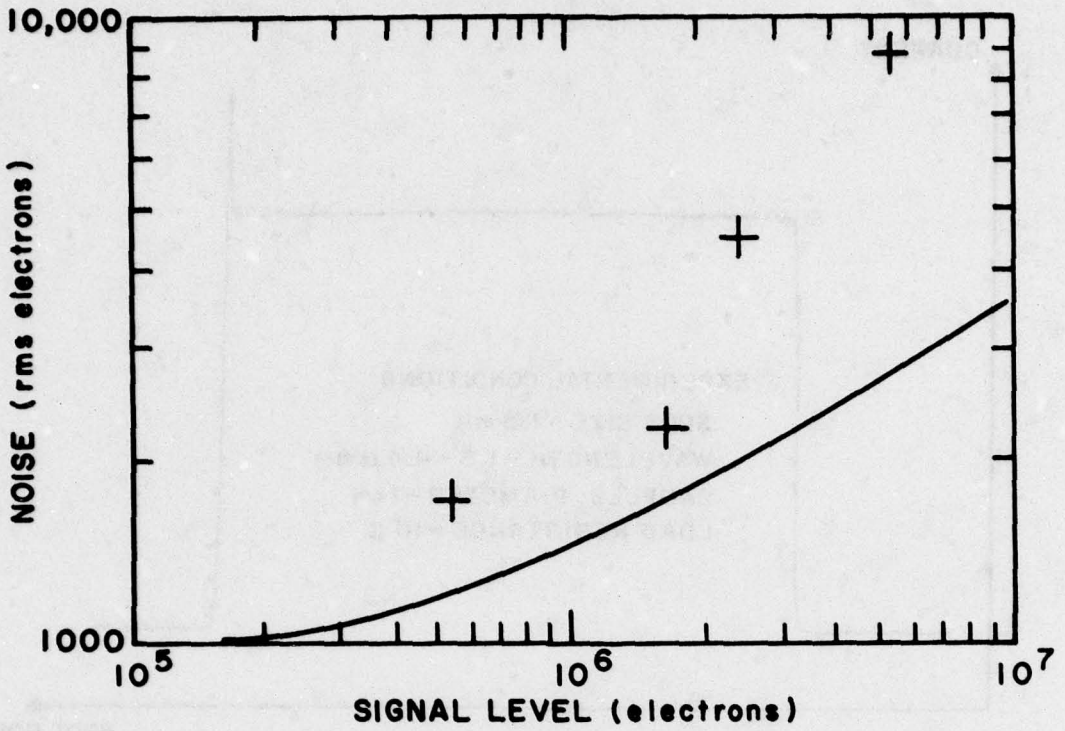

Figure 35. Noise level as a function of signal level. The solid line is calculated.

C. PHOTORESPONSE UNIFORMITY

Two methods were used to verify the uniformity of Schottky junctions and Schottky IR-CCD arrays. They were scanning within a cell, and uniform illumination of an array by a large-aperture blackbody. The spot-scanning measurement system consisted of a blackbody source with a 10-mil-pinhole aperture, a reflecting telescope with 10:1 image reduction, and a cold-stage sample holder at the image plane. The detector was translated by 2.5-μm increments in the image plane by the use of a stepping-motor drive. The sample signal was recorded on the y axis of an x-y recorder, while the x axis was driven by the reference voltage of the stepping drive. A spot scan of a 1-cm-diameter diode is given in Fig. 36. The resolution is approximately 30 μm [19]. The PtSi-electrode thickness is tapered at the edge, resulting in the enhanced

19. B. R. Capone, private communication.

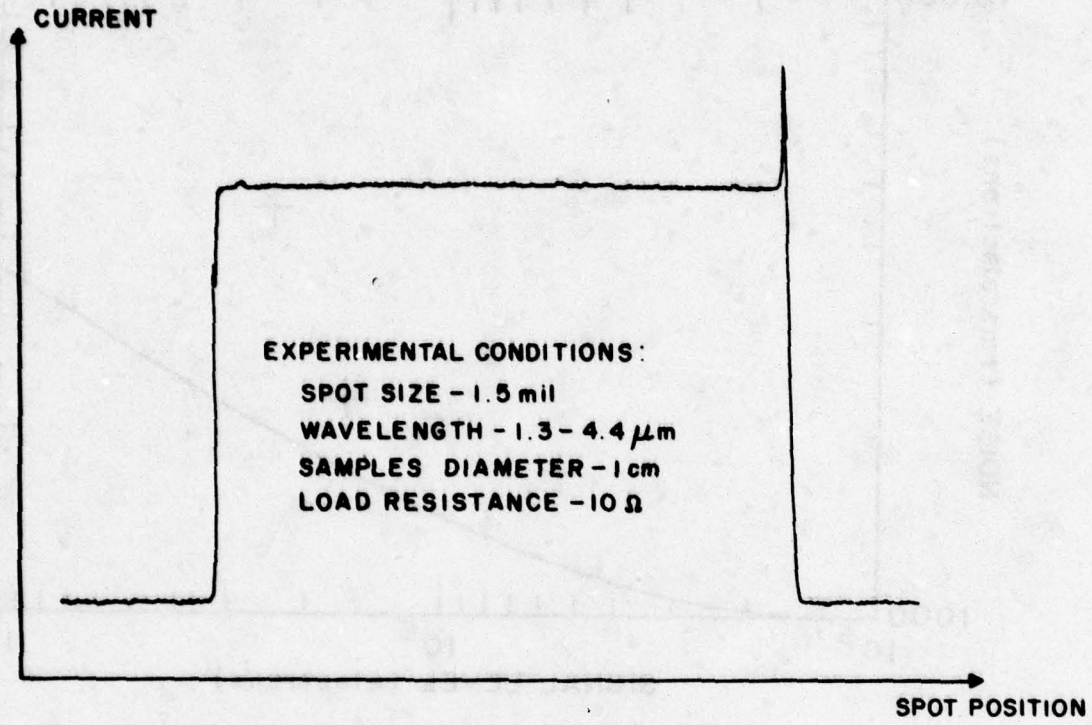

Figure 36. Photocurrent spot scan of PtSi/p-Si Schottky diode.

photoresponse seen at the right end of the figure. Fig. 37 shows the output of a Pd_2Si IR-CCD array illuminated by a 300°C blackbody. The output uniformity is 0.5% rms. One cell reads 3% below average. In Fig. 38 the blackbody source was attenuated with neutral-density filters to show that the response uniformity was independent of signal. f/6 optics and unit magnification were used for these measurements.

Fig. 39 shows the response of a Pd_2Si array to a weak signal imposed on a large, thermal-current pedestal. The operating temperature was 135K. These data indicate that there is no measurable variation of ψ_{ms} over the 64-cell array. We conclude that photoresponse uniformity in the range of 0.5% rms is possible for future systems.

D. IMAGE RESOLUTION

Figures 40(a) and (b) show the blackbody response through a series of slots of decreasing width. A PtSi array was used with f/6.4 optics. Figures 41(a) and (b) give the response for 0.025-in. and 0.0125-in. circular apertures.

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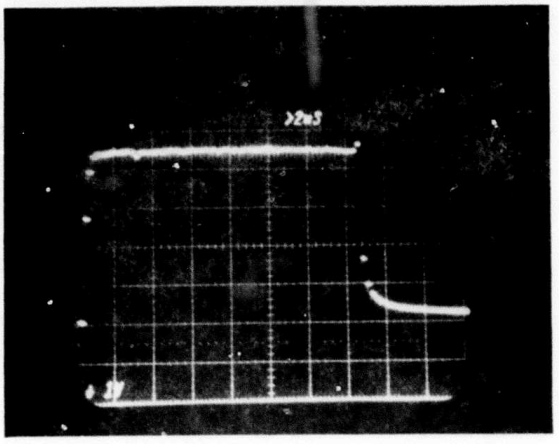


Figure 37. 64-cell Pd_2Si-array photoresponse to 300°C blackbody.

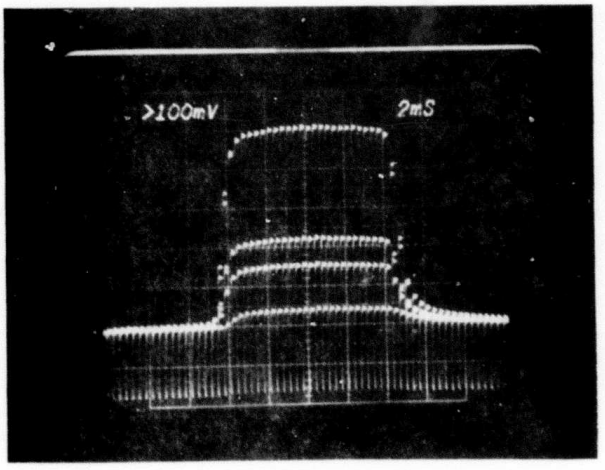


Figure 38. Pd_2Si-array blackbody response with neutral-density filters 0, 0.3, 0.5, and 1.0 density.

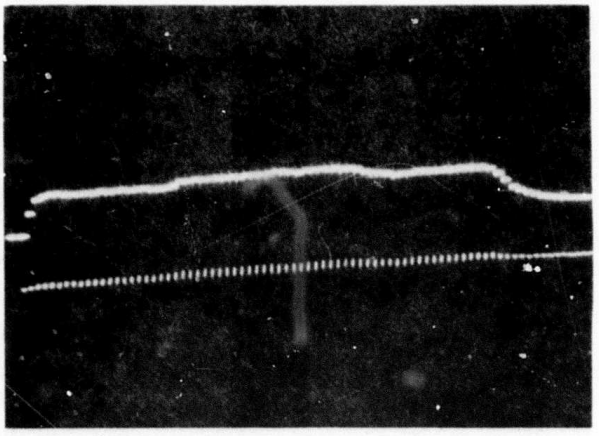
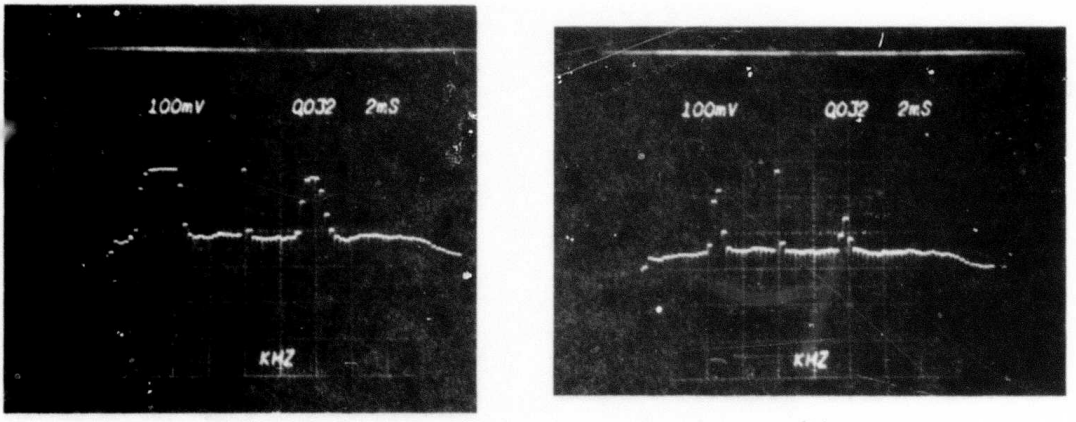
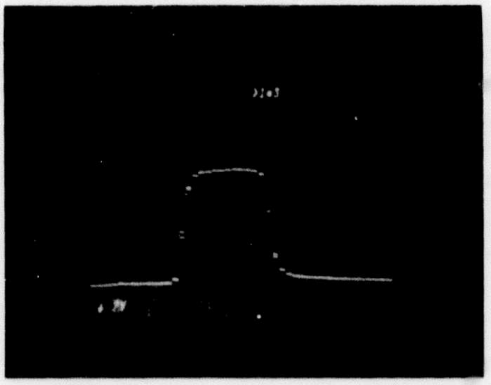


Figure 39. Pd_2Si-array operating at 135K with small signal on a thermal-emission pedestal.

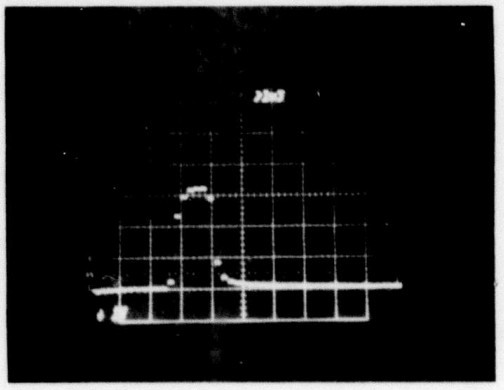


(a) (b)

Figure 40. (a) and (b). Slot mask photoresponse at 1:1 magnification. From left to right slot widths are 0.016, 0.008, 0.004, and 0.002 in.



(a)



(b)

Figure 41. Pd_2Si-array response to (a) 0.025-in. and (b) 0.0125-in. blackbody apertures.

The detectors were 0.9 mil wide on 1.8-mil centers. Transfer-inefficiency image blur is apparent on the trailing edge. Figures 42(a) and (b) give the PtSi-array response to 4-bar resolution mask. These data were taken with f/1.2 optics and 0.07 magnification. Figure 42(b) is at the Nyquist limit imposed by the detector spacing (11.1 lp/mm). It is apparent that substantial improvement in resolution is possible by a reduction in cell size and by the use of buried-channel readout. The limits to resolution would be determined by trade-offs between cell size, uniformity, and focal-plane area coverage.

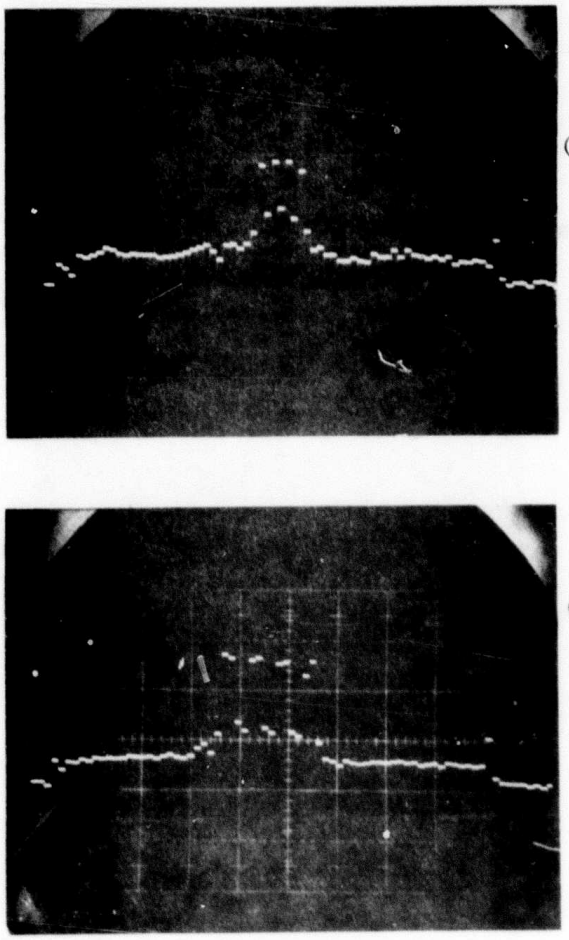


Figure 42. Four-bar resolution-mask response.

E. DISCUSSION OF RESULTS

Analysis of the PtSi-array thermal-response data as well as the characteristics of the measurement apparatus revealed several factors that limited sensitivity. The key limitation was diode breakdown which resulted in both fixed-pattern noise and a 30% loss in usable quantum efficiency. We expect to improve the breakdown voltage by further process improvements. Other factors that could be improved include optics transmission, speed, and magnification. From our experimental data we find that better diode processing and more efficient optics would result in noise-equivalent temperatures in the 0.1-0.13°C

range. Suppression of clock noise and the use of buried-channel readout would give further sensitivity gains. Visible silicon sensors have been developed with 23-μm cell size [20]. Schottky Vidicon tubes operating between wavelengths of 1.1 and 2 μm and having 12-μm-square sensing elements spaced 16 μm on center have shown Nyquist-limited resolution and 0.5% photoresponse uniformity [19]. These data indicate the possibility of future Schottky IR-CCDs with cell sizes of 25 μm, provided that the fraction of focal area used for multiplexing can be minimized. Present devices have detector cells with a 2.9×10^{-5}-cm^2 area; an imager with 25-μm cell size would have a fourfold signal reduction. On the other hand, reduction of the output-gate capacitance and the use of buried-channel technology should lead to a background-limited, rms noise level of 300 electrons. The 25-μm-cell focal plane would have a noise-equivalent temperature of 0.08°C, provided the uniformity is improved to 0.3% rms.

Time-delay-integration (TDI) operation relaxes the need for extreme uniformity and opens the way for the use of higher-efficiency Schottky-electrode materials. Cohen et al. [21] have demonstrated C_1 values in the 25% eV^{-1} range using 60-Å thick Au electrodes. These data indicate that a TDI camera could have a fourfold increase in responsivity and a twofold increase in signal-to-noise ratio.

20. G. A. Antcliffe et al., "A Backside Illuminated 400x400 Charge-Coupled Device Imager," IEEE Trans. Electron Devices ED-29(11), 1225-1232 (Nov. 1976).
21. J. Cohen, J. Vilms, and R. J. Archer, "Investigation of Semiconductor Schottky Barriers for Optical Detection and Cathodic Emission," Final Report No. AFCRL-68-0651, prepared for Air Force Cambridge Research Laboratories under Contract No. F19628-68-C-0090, Dec. 1968.

VIII. CONCLUSIONS

Infrared-imaging measurements on Schottky-barrier IR-CCDs were presented which showed excellent agreement with theory and demonstrated that the technology exists for staring-mode, IR-image sensors with excellent uniformity. The technology is standard silicon technology. Cooling requirements are modest, as 90K is sufficient and dissipation is minimal. Staring-mode operation simplifies the mechanical and optical design, suggesting costs that compare favorably with existing IR scanners. The sensors are, however, not limited to staring-mode operation. Modification to only the driving circuitry makes scanned operation with time delay and integration possible. In either case, the sensor is inherently immune to blooming and smear. Calculations indicate that with buried-channel CCDs reading out 1-mil^2 PtSi detectors, thermal resolution of 0.1K at 300K background can be achieved at standard TV-frame rates. The experimental data obtained on platinum silicide indicate that achievement of the required uniformity of 0.5% presents no fundamental problem.

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17. E. S. Kohn, IEEE J. Solid-State Circuits SC-11(1), 139 (Feb. 1976).
18. F. D. Shepherd et al., "Ambient Thermal Response of a Monolithic Schottky IR-CCD," Proc. IRIS Thermal Imaging Specialty Group Meeting, El Toro, Cal., Feb. 1977.
19. B. R. Capone, private communication.
20. G. A. Antcliffe et al., "A Backside Illuminated 400x400 Charge-Coupled Device Imager," IEEE Trans. Electron Devices ED-29(11), 1225-1232 (Nov. 1976).

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21. J. Cohen, J. Vilms, and R. J. Archer, "Investigation of Semiconductor Schottky Barriers for Optical Detection and Cathodic Emission," Final Report No. AFCRL-68-0651, prepared for Air Force Cambridge Research Laboratories under Contract No. F19628-68-C-0090, Dec. 1968.

APPENDIX A

THE BACKGROUND-SUBTRACTION MODE

It has been shown that the contrast in thermal scenes is low; 300K scenes viewed with PtSi detectors on p-Si have contrast on the order of 5% per kelvin. The bulk of the signal is a fixed amount in each detector, but the shift register must carry it all out to read the small, information-containing part. It is the purpose of the background-subtraction mode to remove a large, fixed amount of charge from each detector before the signals are loaded into the shift register. If the shift register had only the high-contrast, information-bearing signal to handle, its dynamic range would be better utilized. While it has been shown both theoretically and experimentally that for our IR-CCDs the shift-register capacity was more than sufficient to handle the thermal signal, it was nevertheless decided to use these IR-CCDs to evaluate background subtraction as a separate experiment. The original idea is illustrated in Fig. 8 and was explained in detail in Semiannual Report, 14 January 1974 (AFCRL-TR-74-0056). The experimental results were discussed in Semiannual Report No. 3, 15 May 1975 (AFCRL-TR-75-0284), where it was shown that the background-subtraction method introduced severe nonuniformities. A major cause of this nonuniformity is the variation in MOS pinch-off voltage. Uniformity is good in the Vidicon mode because a single gate (the transfer gate) is used to charge the detectors and simultaneously to read out the integrated signal. In the background-subtraction mode, as previously described and performed, two gates, the charging gate and the transfer gate, perform these functions separately; the difference between their pinch-off voltages contributes to the fixed-pattern noise on the video signal. To eliminate this source of nonuniformity, an improved background-subtraction scheme was conceived, in which the same gate is used to transfer the background charge and the signal charge out of the detector. The layout is shown in Fig. 19. There, the charging circuit is shown on the side of the shift register, opposite from the detectors. Operation of this circuit is shown in Fig. 43. Once per frame, while the phase-1 gates are on, the charging gate is pulsed on, making the surface under it go to V_A. The transfer gate is pulsed simultaneously, establishing the charging level by driving its surface to V_C. The charge thus drained away can be much larger than the well capacity, since the phase-1 gates are used as transmission

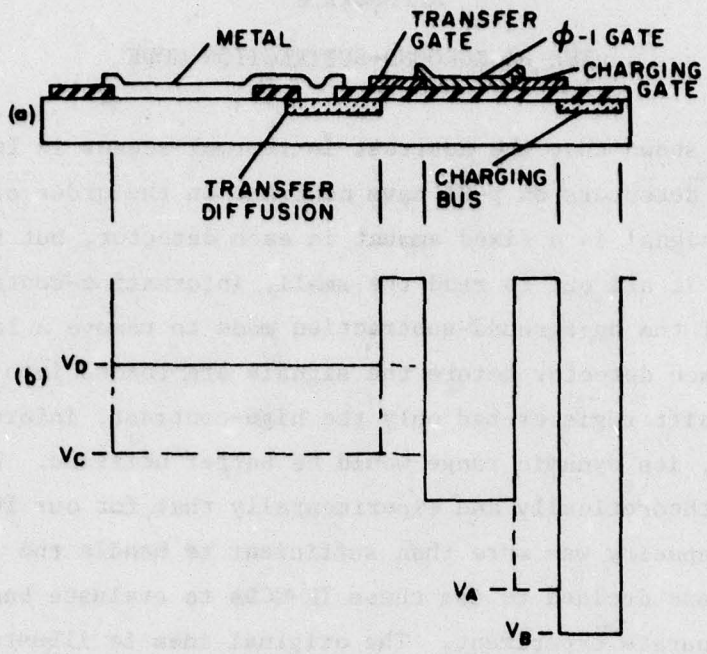


Figure 43. (a) Cross-sectional view of one-dimensional IR-CCD with new background-subtraction scheme. (b) Energy-level diagram aligned with (a). Some details were omitted for clarity. The solid lines show the phase-1 gate ON, and the transfer and charging gates OFF.

channels, not storage wells. After the integration time the transfer gate is pulsed to a smaller value, making the surface under it V_D. The smaller signals thus skimmed are accumulated under the phase-1 gates and clocked out in the usual manner. It is desirable to recharge the detectors immediately after skimming so that they can integrate the optical signal while the transferred scene is being read out. Obviously the detectors cannot be recharged while the signal charges are stored under the phase-1 gates, but these charges can be clocked to the phase-3 wells for temporary safekeeping while the phase-1 gates are used as transmission channels. This would be impossible in a charge-coupled shift register having fewer than four phases.

This layout was used for the four-phase line array on the double-polysilicon chip. To operate this line array in the Vidicon mode, it is necessary only to bias off the charging gate.

APPENDIX B

CIRCUITRY FOR THE 25x50 ARRAY

The method we chose for operating the 25x50 array was described in Section VI. The complete circuit is shown in Fig. 44. The master clock in our circuit is a 555 timer (U1 in Fig. 44), run as an asymmetric astable timer. It provides horizontal blanking pulses, shown in Figs. 22 and 23 as being low during blanking. The B-to-C transfer occurs during the short blanking time (Fig. 22). A 74124 start-stop oscillator (U10) runs during the horizontal-blanking time and drives flip-flops U11 and U12, which decode the four B-phases. A 7493 counter (U15) counts the oscillator pulses, and blocks them after the first four. The C-register runs during the long "on" time of horizontal-blanking pulse, as in Fig. 23. Another 74S124 start-stop oscillator (U2) runs during this "on" time, driving flip-flops U3 and U4, which decode the four C-phases. A 16-bit binary counter (U21, U22, U23, and U24) counts the number of horizontal-blanking pulses and stops the B-to-C transfers at a count of 50, with the help of NAND gate U29. It continues to count to the selected value ranging from 64 to 32768. When this count is reached, counter U25 counts four more horizontal lines, providing the vertical-blanking pulse. The transfer pulse is triggered and completed during this time, as shown in Fig. 45. It is worth noting that the C-clock is not counted; it is not necessary to count it, as any extra transfers of the C-register carry no detector signals and are dark on the display. Counting would, however, result in noise pickup on the display.

The function of each gate in Fig. 44 is described in Table 5. The on-chip circuitry for the area array and the pin connection are shown in Fig. 46.

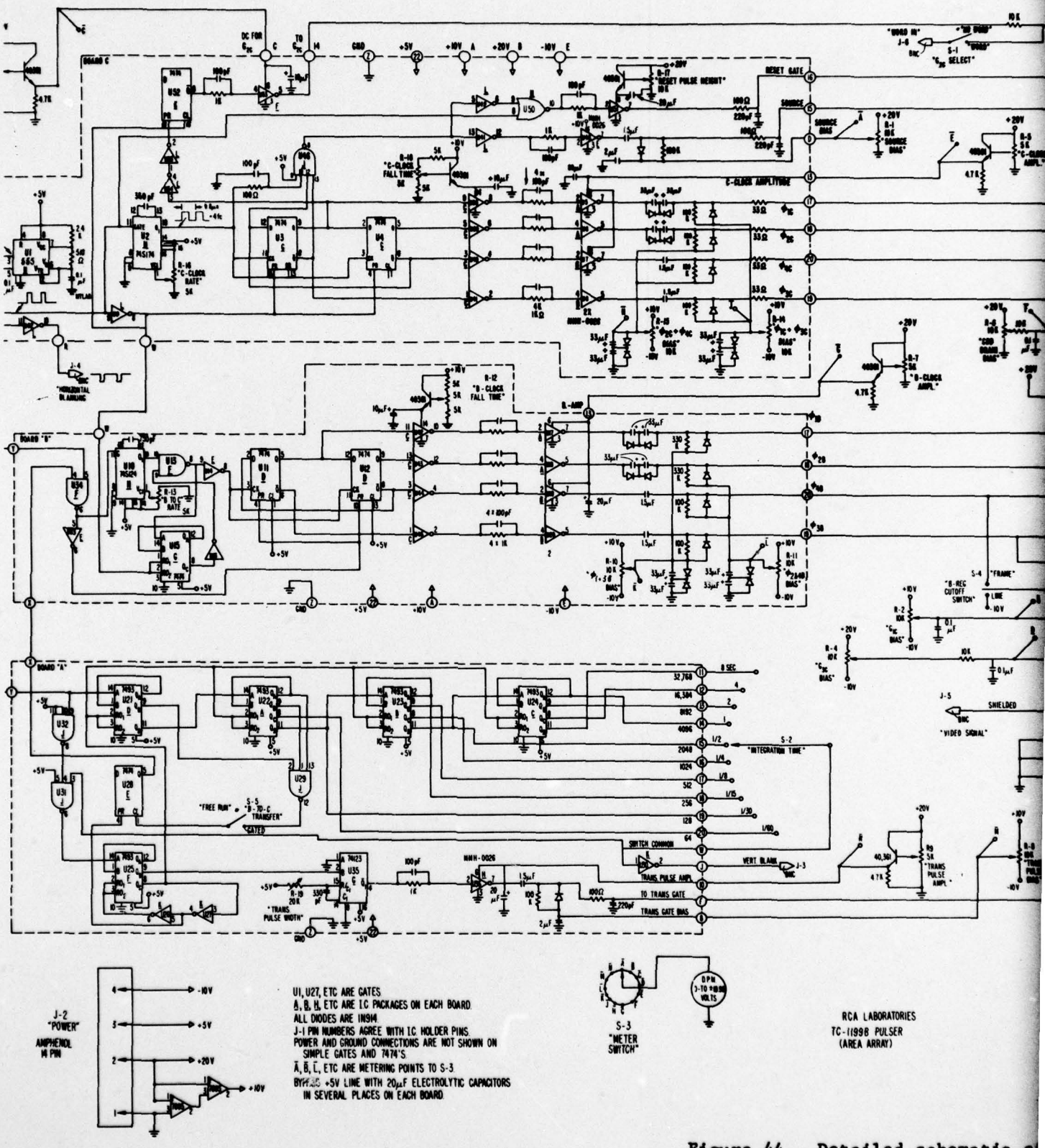
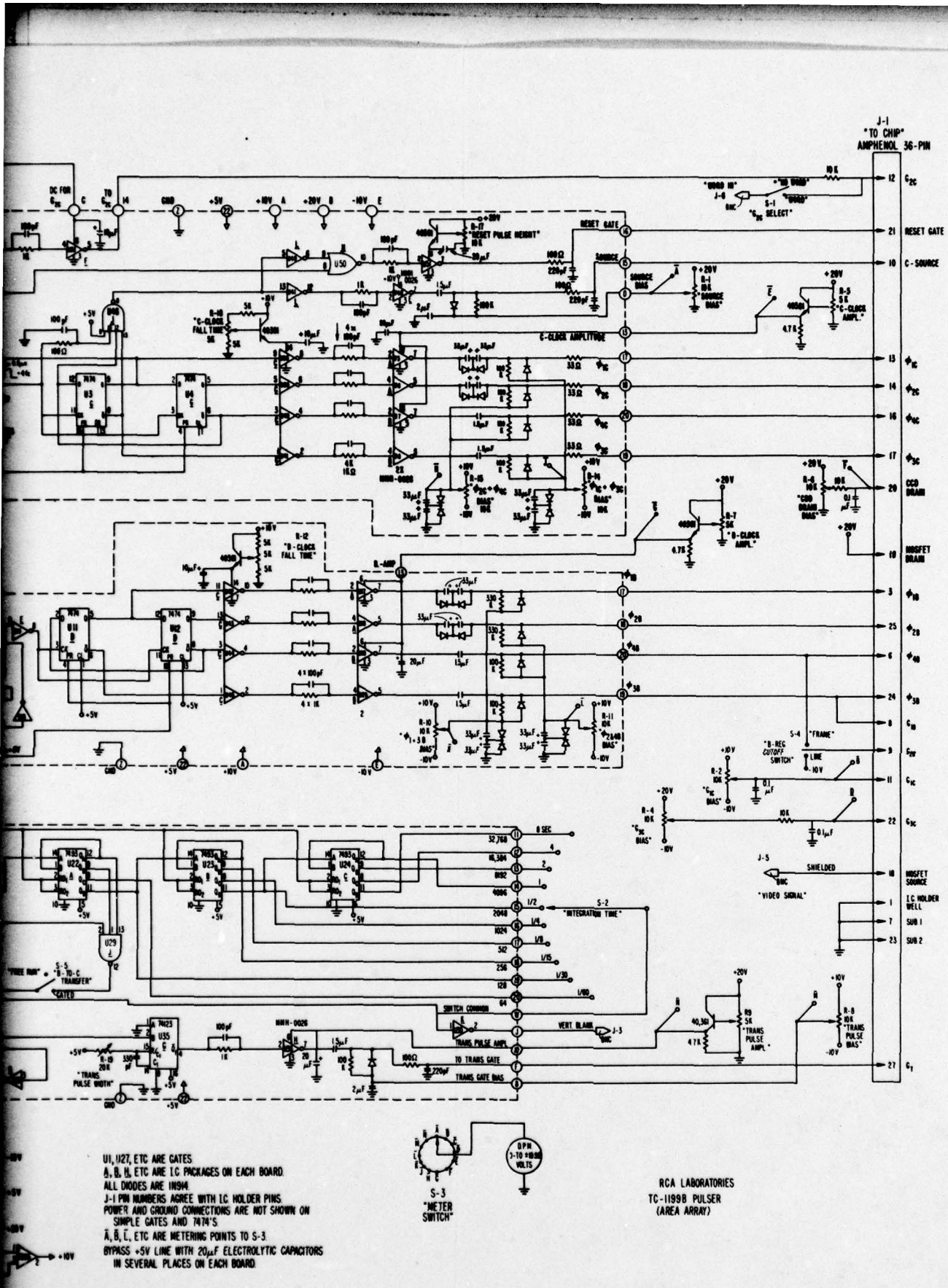


Figure 44. Detailed schematic o
circuit for the 25x5
array.



U1, U27, ETC ARE GATES.
A, B, H, ETC ARE I.C. PACKAGES ON EACH BOARD.
ALL DIODES ARE 1N914.
J-1 PIN NUMBERS AGREE WITH I.C. HOLDER PINS.
POWER AND GROUND CONNECTIONS ARE NOT SHOWN ON SIMPLE GATES AND 7474'S.
$\bar{A}$, $\bar{B}$, $\bar{L}$, ETC ARE METERING POINTS TO S-3.
BYPASS +5V LINE WITH 20 μF ELECTROLYTIC CAPACITORS IN SEVERAL PLACES ON EACH BOARD.

Figure 44. Detailed schematic of drive circuit for the 25x50 area array.

2

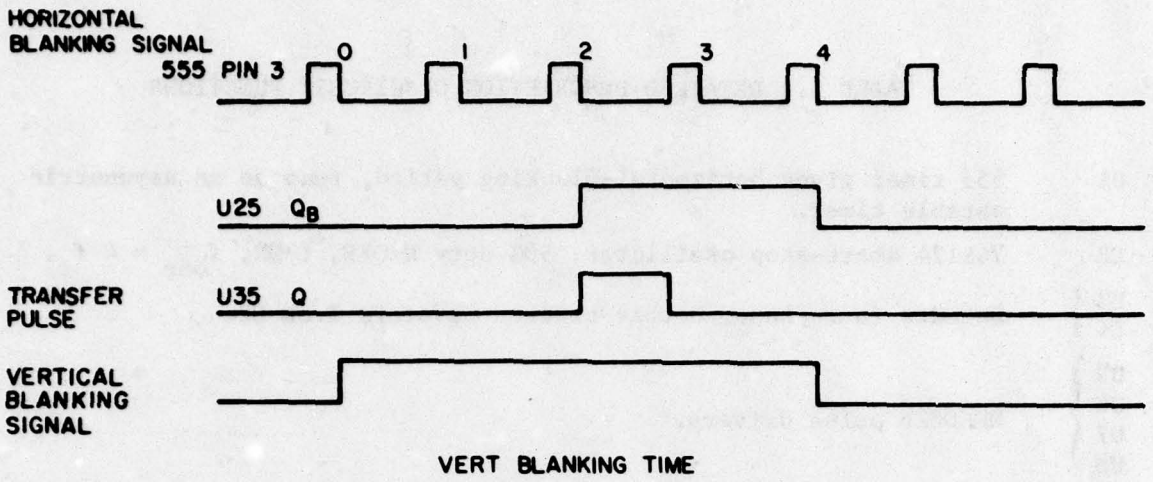


Figure 45. Position of the transfer pulse during the vertical blanking time.

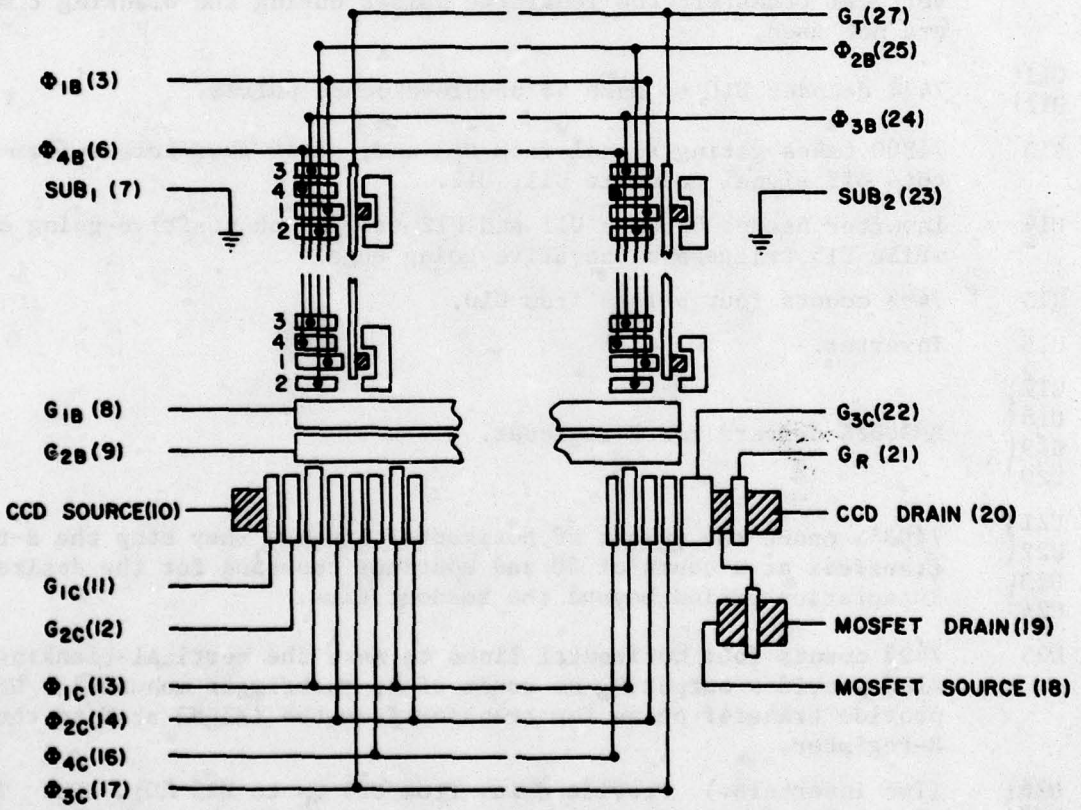


Figure 46. Wiring diagram of TC-1199 area array. The pin numbers are in parentheses. Source-drain diffusions are cross-hatched where exposed. The drawing is not to scale, and gate overlaps are not shown.

TABLE 5. DETAILED DESCRIPTION OF CIRCUIT FUNCTIONS

U1	555 timer gives horizontal-blanking period, runs as an asymmetric astable timer.
U2	74S124 start-stop oscillator, 50% duty H→OFF, L→ON, $f_{osc} = 4\ f_c$.
U3, U4	Decodes four-phase, double-clocked waveform from U2.
U5, U6, U7, U8	MMH0026 pulse drivers.
U9	Inverts waveform from U1 to driver U3 and U4 into state so that during the horizontal-blanking time ϕ_{1C}→H, ϕ_{2C}→H, ϕ_{3C}→L, ϕ_{4C}→L.
U10	74S124 gated on during the horizontal-blanking time. The first four pulses are used to produce the double-clocked 4ϕ waveform for the vertical transfer; the remaining pulses during the blanking time are not used.
U11, U12	7474 decodes U10 to make 4ϕ double-clocked pulses.
U13	74S00 takes gating signal from U15 and, after four pulses from U10, cuts off signal going to U11, U12.
U14	Inverter needed because U11 and U12 trigger on positive-going edge, while U15 triggers on negative-going edge.
U15	7493 counts four pulses from U10.
U16	Inverter.
U17, U18, U19, U20	MMH0026 drivers for B-register.
U21, U22, U23, U24	7493's count the number of horizontal lines. They stop the B-to-C transfers at a count of 50 and continue counting for the desired integration period beyond the readout time.
U25	7493 counts four horizontal lines to make the vertical-blanking time. Also provides output Q_B on count of 2, to trigger monostable U35 to provide transfer pulse for transfer from the imaged area to the B-register.
U26, U27	(Two inverters.) Provide delay from U25 Q_C to U25 RO_1, RO_2. This widens the reset pulse to be sure it can reset the five TTL loads. U27 also inverts the reset pulse for PR on U28 because the 7474 requires a low level to preset.
U28	7474 used as a latch. At the beginning of the field after the transfer from detectors, U28 is preset to Q high. This allows the B-to-C

TABLE 5. (Continued)

transfer to be normally generated. After 50 lines U28 is cleared, and Q is low. This prevents the oscillator U10 from running and producing any more B-to-C transfers.

U29 — 7420 provides the logic to decode the count of 50 to clear latch U28.

U30 — Inverter provides vertical-blanking signal.

U31 — 7400 gates on signal to U25 at start of vertical-blanking time.

U32 — Removes inversion of U31. This means U25 counts the trailing edge of the horizontal-blanking pulse.

U33 — Inverter, removes inversion of gate U34. This is so that U11 PR and U12 PR receive low levels during the horizontal-line time.

U34 — 7400 stops U10 and presets U11, U12 after two B-to-C transfers have been made.

U35 — This 74123 one shot is triggered on the count of 2 from U25. $\overline{Q}$ of U35 provides inverse of transfer pulse for detector to B-register transfer.

U36 — MMH0026 driver provides transfer pulse to transfer charge from detectors to B-register.

U37 — Inverter provides horizontal-blanking pulse.

U38, U39, U40, U41 — Inverters for C-clock. All +5-V supplies are connected together to the fall-time control. As the voltage is reduced, the drive to U5, U6, U7, and U8 is reduced, causing the fall time to increase.

U42, U43, U44, U45 — As above, but for B-clock.

U46 — 7420 logic to make S1 strobe. U46 output goes low when 4 f_c, ϕ_{3C}, and ϕ_{4C} are all high.

U47 — Inverter to compensate for inversion of driver U48.

U48 — MMH0026 S-1 strobe driver.

U49 — Inverter gives the reset gate an inverse of S1. It also buffers the reset logic from the input of U48.

U50 — 7402 output goes low at normal reset period or during horizontal-blanking time.

U51 — MMH0026 reset-gate driver.

U52 — 7474 latch is cleared by the horizontal-blanking pulse and then preset by the first low level on ϕ_{1C}. This provides a signal to keep G_2 low during the time a signal is contained under ϕ_{1C} so that charge does not spill toward the source.

TABLE 5. (Continued)

U53	MMH0026 G2 driver.
U54, U55	Form a delay so that G2 stays low until charge is transferred out of ϕ_{1C} stage 1.

APPENDIX C

CIRCUITRY FOR THE FOUR-PHASE, DOUBLE-POLYSILICON LINE ARRAY

The complete circuit for operating the four-phase line array is shown in Fig. 47. Gate I is a start-stop oscillator driving type-D flip-flops E and F, which are cross-coupled to generate the four double-clocked waveforms. These waveforms are buffered by gates R and amplified by chips K and L. Auxiliary logic provides reset pulses, transfer pulses, and strobe pulses for the source diffusion. Timing for these pulse waveforms is similar to that already shown for the output register of the area array. S_1 selects between the "frame" (imaging) mode and the "word" (electrical data input) mode. A binary counter, chips B, C, and D, provides a trigger for use during electrical word testing. A 555 timer chip ("S") sets the integration time in the imaging mode, and triggers the transfer pulse just before start up of the shift register. S_3 determines whether the shift register runs or stops during the major fraction of the integration time. S_2 selects between pulsed and continuous operation of the transfer gate. External pulse generators are required for generation of the input-pulse train for electrical testing, and for operation of the improved background-subtraction circuit. The on-chip circuitry and the pin connections for the line array are shown in Fig. 48.

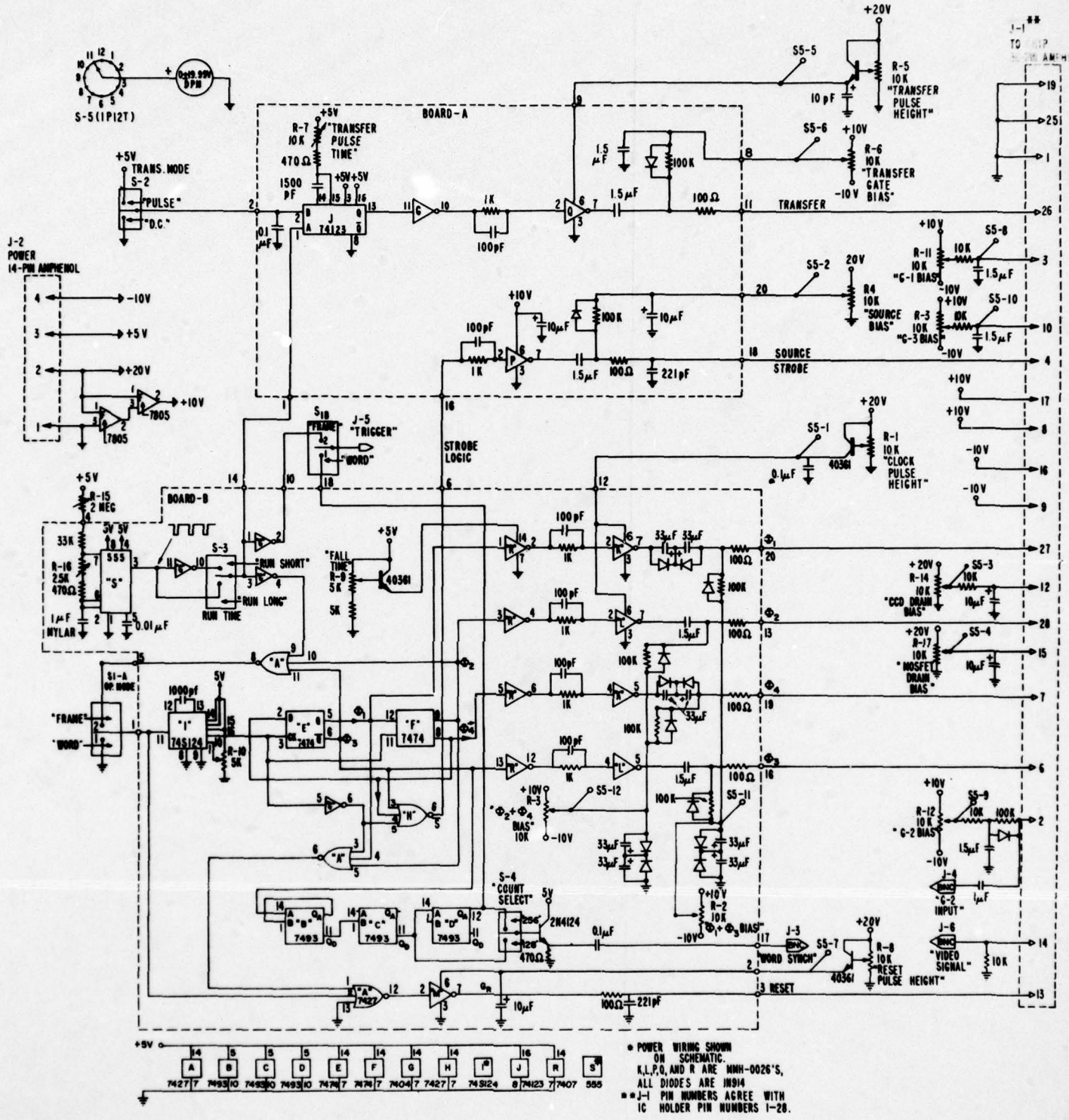


Figure 47. Detailed schematic of drive circuit for the double-polysilicon line array.

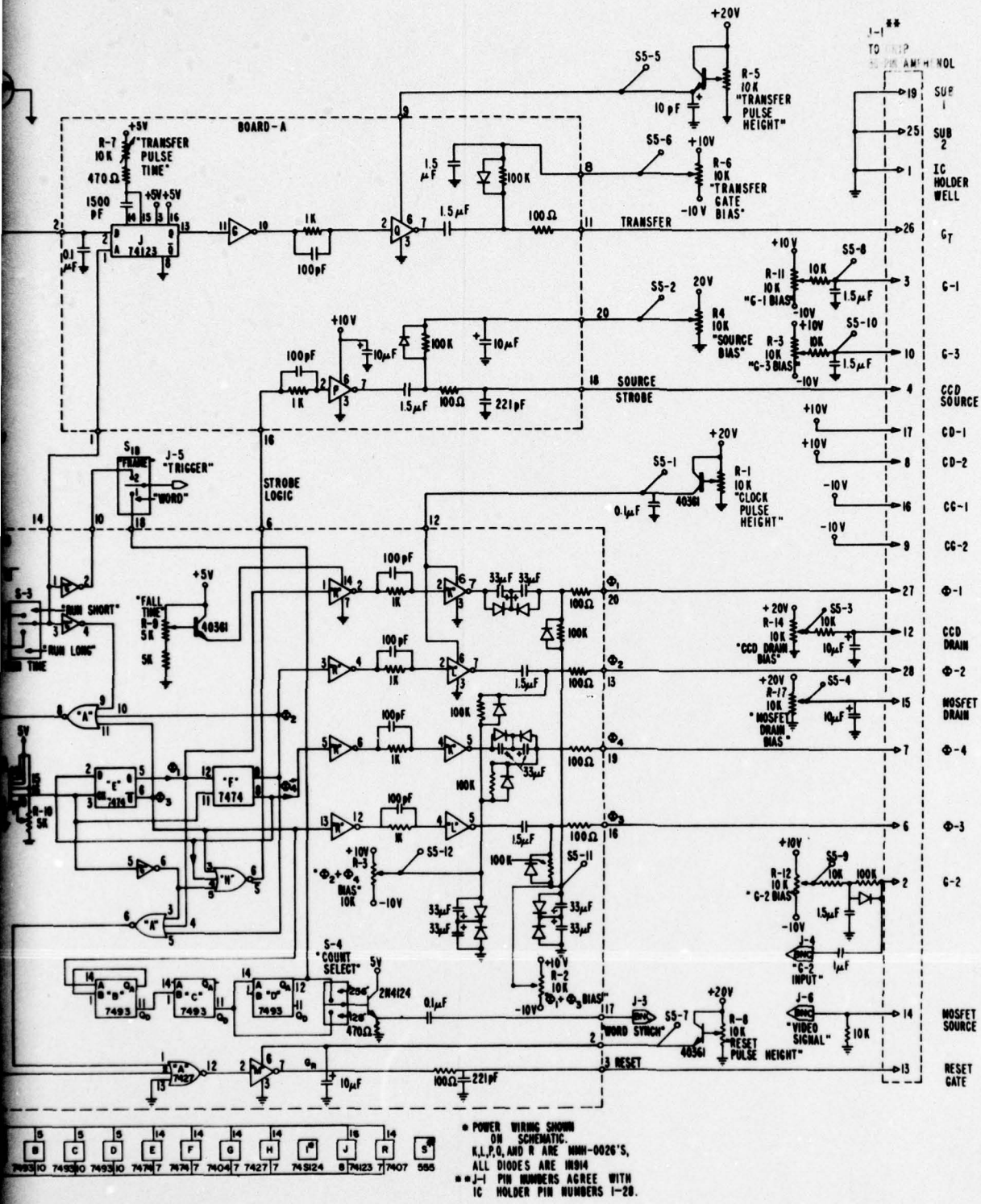


Figure 47. Detailed schematic of drive circuit for the double-polysilicon line array.

2

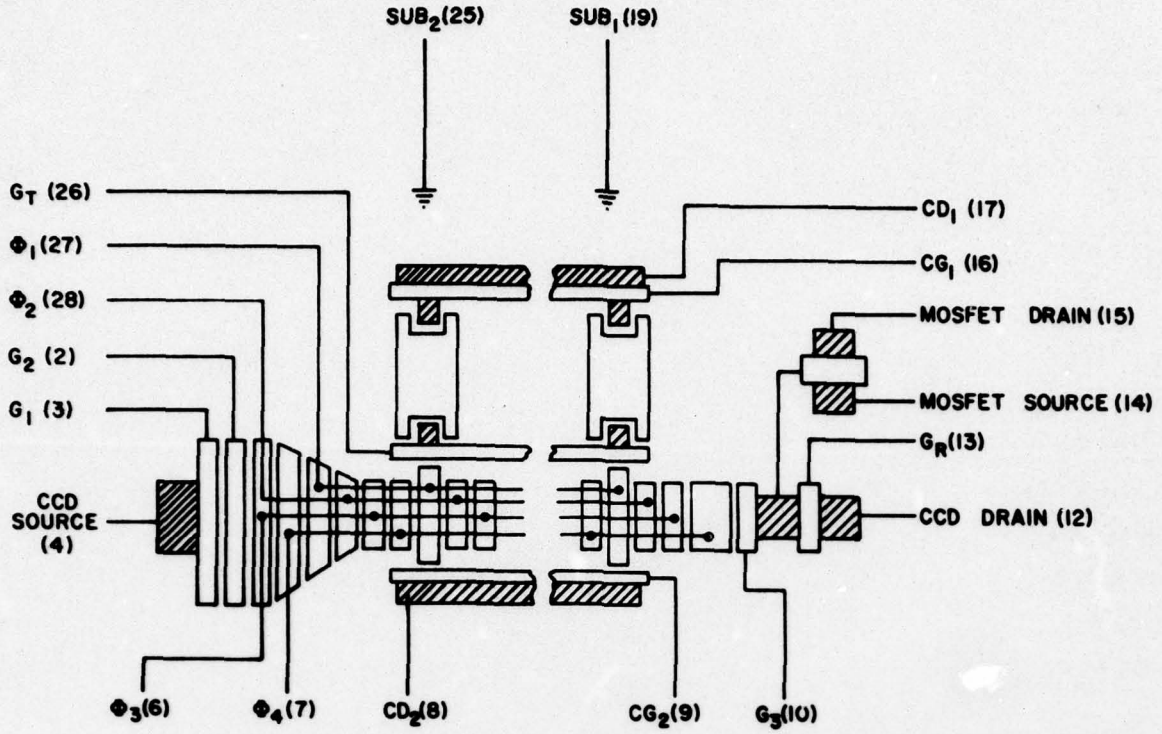


Figure 48. Wiring of TC-1199 line array. The pin numbers are in parentheses. Source-drain diffusions are crosslatched where exposed. The drawing is not to scale, and gate overlaps are not shown.