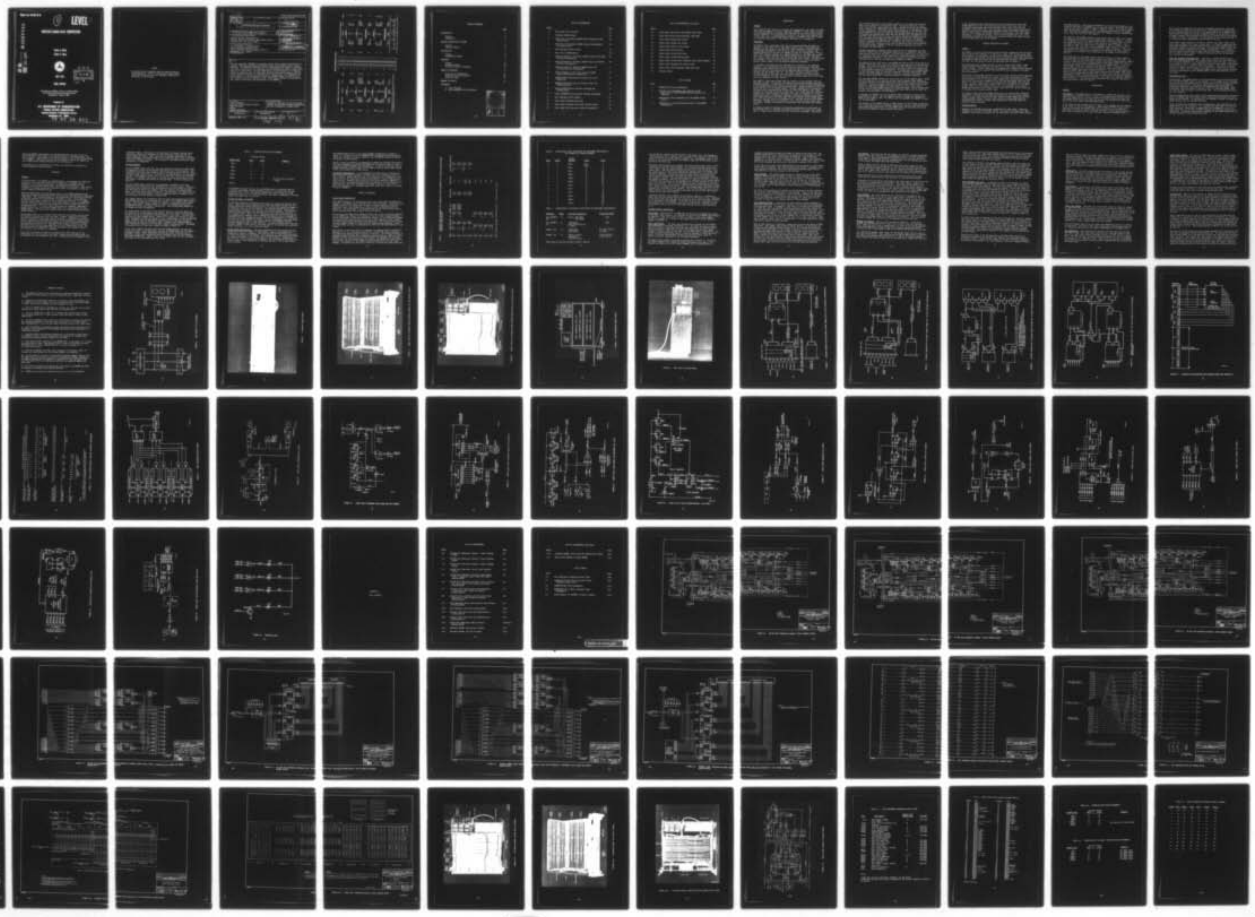
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JUL 78 E A MACK, A R MOSS

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DIGITIZED RADAR DATA COMPRESSOR

Edwin A. Mack
Arthur R. Moss

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FINAL REPORT

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Prepared for

U.S. DEPARTMENT OF TRANSPORTATION
FEDERAL AVIATION ADMINISTRATION
Systems Research & Development Service
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16. Abstract

The data compressor (DACOMP) is a special-purpose device designed specifically to increase radar data recording capabilities at air route traffic control centers (ATRCC's). The DACOMP accomplishes this by "compressing" the number of channels each radar occupies prior to recording, thereby reducing the number of tape tracks required for each radar. The three 2400 bit-per-second channels of a digitized radar are compressed onto one high-speed (9375 bit-per-second) channel. Because of the threefold reduction in recording track requirements, use of DACOMP's will enable ARTCC's to record information from an increased number of radar sites on the recorders that are available to them. This report explains the installation, use, theory of operation, and maintenance of the DACOMP.

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METRIC CONVERSION FACTORS

Approximate Conversions to Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
in	inches	*2.5	centimeters	cm
ft	feet	30	centimeters	cm
yd	yards	0.9	meters	m
mi	miles	1.6	kilometers	km
		AREA		
in^2	square inches	6.5	square centimeters	cm^2
ft^2	square feet	0.09	square meters	m^2
yd^2	square yards	0.8	square meters	m^2
mi^2	square miles	2.6	square kilometers	km^2
	acres	0.4	hectares	ha
		MASS (weight)		
oz	ounces	28	grams	g
lb	pounds	0.45	kilograms	kg
	short tons (2000 lb)	0.9	tonnes	t
		VOLUME		
tsp	teaspoons	5	milliliters	ml
Tbsp	tablespoons	15	milliliters	ml
fl oz	fluid ounces	30	milliliters	ml
c	cups	0.24	liters	l
pt	pints	0.47	liters	l
qt	quarts	0.95	liters	l
gal	gallons	3.8	liters	l
ft^3	cubic feet	0.03	cubic meters	m^3
yd^3	cubic yards	0.76	cubic meters	m^3
		TEMPERATURE (exact)		
°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

*1 in = 2.54 (exactly). For other exact conversions and more detailed tables, see NBS Misc. Publ. 286, Units of Weights and Measures, Price $2.25, SD Catalog No. C13.10:286.



Approximate Conversions from Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
mm	millimeters	0.04	inches	in
cm	centimeters	0.4	inches	in
m	meters	3.3	feet	ft
m	meters	1.1	yards	yd
km	kilometers	0.6	miles	mi
		AREA		
cm^2	square centimeters	0.16	square inches	in^2
m^2	square meters	1.2	square yards	yd^2
km^2	square kilometers	0.4	square miles	mi^2
ha	hectares (10,000 m^2)	2.5	acres	
		MASS (weight)		
g	grams	0.035	ounces	oz
kg	kilograms	2.2	pounds	lb
t	tonnes (1000 kg)	1.1	short tons	
		VOLUME		
ml	milliliters	0.03	fluid ounces	fl oz
l	liters	2.1	pints	pt
l	liters	1.06	quarts	qt
l	liters	0.26	gallons	gal
m^3	cubic meters	35	cubic feet	ft^3
m^3	cubic meters	1.3	cubic yards	yd^3
		TEMPERATURE (exact)		
°C	Celsius temperature	9/5 (then add 32)	Fahrenheit temperature	°F

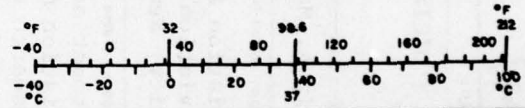


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INTRODUCTION

PURPOSE.

The purpose of this report is to explain the installation, use, theory of operation, and maintenance of the data compressor (DACOMP); a device which increases the recording capacity of digital radar recorders at air route traffic control centers (ARTCC's). By "compressing" the data on the three radar channels from a remote site into a single high-speed channel, the DACOMP effectively triples the recording capability of the recorder with which it is integrated.

BACKGROUND.

Information from a long-range radar and its associated beacon equipment is digitized at the radar site by the common digitizer (CD). These digitized messages are then routed to the ARTCC via three independent parallel channels. Each message is assigned by the CD output logic to the first channel that becomes available for use when the message is ready for transmission. Each of these three channels consists of a modem transmitter at the radar site, a telephone line or radar microwave link connecting the radar site with the ARTCC, and a modem receiver and data receiver group (DRG) at the ARTCC. The DRG routes the messages to the 9020 central computer complex (CCC), system maintenance monitor console (SMMC), and printing and monitoring equipment.

At the ARTCC, the digitized radar information is recorded at the modem-DRG interface. The recorded data are then used for various phases of National Airspace System (NAS) enroute testing, training, and maintenance. The recorders which are used for this purpose are the Ampex FR-1800, the Bell and Howell VR-3700, and the Sangamo Sabre IV. The normal recording capability of an FR-1800 recorder is two radar sites (six radar channels or 12 tape tracks). For the VR-3700 and the Sabre IV, the normal recording capability is four radar sites (12 channels or 24 tape tracks).

Most ARTCC's utilize more radars than the capacity of the recorders that are available to them. The need for increasing the available recording capability developed because of a requirement to record seven or eight radars simultaneously on two FR-1800 recorders at the Los Angeles ARTCC. NAFEC was asked to study the matter and arrive at a suitable method. Various techniques were investigated, the main effort centering around efforts to reduce the number of tape tracks required to record and play back a radar site. Two tracks (data and clock) are required for a single channel; therefore six tracks are required for a three-channel radar site. An alternate technique to reduce the number of tape tracks was to have each radar site close down one output channel on the common digitizer (CD) and send data on two channels only. This was and still is a limited technique, allowing the site information to be recorded on four, rather than six tracks. However, this method is inconsistent with the normal NAS configuration.

A promising technique consisted of pulse-width modulating the clock pulse of each channel prior to recording according to whether or not there was a logic zero or a logic one on the data line for the bit cell concerned. This method

would effectively double the recording capability by recording the clock and data for one channel on a single tape track. The actual method was fairly simple and required a small amount of logic to encode and decode the information. However, two limitations caused this technique to be abandoned in favor of data compression. First was the bit width limitation of the FR-1800. The pulse width for the logic one condition (104 microseconds) was less than the 111-microsecond minimum pulse width that the FR-1800 could accommodate at the specified tape speed and error rate. The second limitation stemmed from the fact that many of the tapes from ARTCC's would be played back at National Aviation Facilities Experimental Center (NAFEC), which has a four-DRG/CD adapter complement per 9020 simplex. Separating the clock and data lines on playback would have resulted in the need for additional DRG's and CD adapters in the 9020 systems at NAFEC in order to reproduce completely the radar environments of many ARTCC's.

The data compression technique finally used was one of compressing the three 2400-bit channels into one high-speed channel prior to recording. This technique does not modify the site data in any way and requires only two tape tracks for recording, also only one DRG channel and a single CD adapter in the CCC are required for playback. Thus, up to 12 radars could be played back simultaneously without the need for additional equipment at NAFEC.

The original output clock rate of the DACOMP was 7500 bits per second, which is slightly faster than three times the 2400 bit-per-second rate of a single radar channel. This was well within the 9 kilohertz (kHz) maximum data rate for the FR-1800 recorder at a 3.75 inch-per-second tape speed, which is the speed used to record normal uncompressed information. A disadvantage to the DACOMP method is that additional logic is required to compress a single three-channel radar. However, the 9-kHz bandwidth of the recorder was being more efficiently used, and this method generated a threefold increase in recording capability.

Two four-radar DACOMP drawers were first built for the Los Angeles ARTCC. NAFEC was then requested by the National Airspace System Program Office (NASPO) to fabricate nine more four-radar drawers for other ARTCC's equipped with FR-1800 recorders. This would enable those sites to double their radar recording capability by reducing the number of tracks needed to record a radar site. Finally, 12 six-radar DACOMP drawers were fabricated under contract GS-00S-15685 by the Electronic Engineering Company of California (EECo), sent to NAFEC for checkout, and installed at various ARTCC's.

At present, the DACOMP's at the Los Angeles ARTCC have been in operation for approximately 4 years. The last ARTCC to receive a DACOMP was Jacksonville ARTCC in the summer of 1975. All ARTCC's are now equipped with DACOMP's except for the Miami ARTCC.

The checkout of the DACOMP drawers at NAFEC resulted in the design and fabrication of special-purpose test equipment (analyzers), capable of generating simulated modem radar information for the DACOMP inputs and analyzing the output data from the DACOMP for logic problems and faults.

It was determined during the fabrication of the second group of four-radar DACOMP drawers that the 7,500 bit-per-second output clock rate could not accommodate high message densities; therefore, the output clock rate was increased to 9375 hertz (Hz). This was done without an extensive modification effort and was found to adequately accommodate heavy radar target data rates. However, this required the FR-1800 recorder to be operated at its next higher tape speed (7.5 inches per second), since the 9-kHz maximum data rate of the FR-1800 when operated at the normal 3.75 inches-per-second tape speed is below the 9.375-kHz output rate of the DACOMP.

GENERAL DESCRIPTION OF DACOMP

OVERALL.

The DACOMP is a device which funnels digitized radar transmitted over the three 2400 bit-per-second channels of a radar onto a single 9375 bit-per-second high-speed channel. By this means, the data from a radar site, which normally would occupy six recorder tracks, now occupy only two recorder tracks after compression. The DACOMP is inserted between the receiver-modem-DRG interface, and the recorder; the data paths are shown in simplified form in figure 1.

Each digitized radar message consists of four or seven 13-bit fields. Each message contains range, azimuth, and other data of each target seen by the radar or beacon. A 13-bit IDLE field is automatically inserted between messages by the CD. The CD also transmits this IDLE field over a channel if no radar data are available.

Functionally, each DACOMP consists of a pair of 91-bit serial-in shift registers for each of the three channels of a radar. The 52-bit four-field or 91-bit beacon message on one of the three radar channels will be automatically clocked into one of the two shift registers by the 2400 bit-per-second clock from the modem. The shift register holds this message until the DACOMP output channel is free, then the output logic clocks it out at a 9.375-kHz or, at some dense traffic ARTCC's, at an optional 12-kHz rate. The high-speed data from the DACOMP are recorded on one recorder track, while the 9.375- (or 12-) kHz clock is recorded onto a second recorder track.

The timing is such that the message stored in one of the two shift registers assigned to a channel will be completely shifted out onto the output channel before the other shift register for that channel becomes loaded with the next incoming target message. Internal logic uses the incoming IDLE field for synchronization, while the output logic generates its own IDLE fields for insertion between messages.

PHYSICAL ASPECTS.

Normally, the FR-1800 recorder can accommodate two radar sites. These are designated as the "ODD" and "EVEN" radars. One site is recorded on the ODD-numbered tracks which are grouped into one head stack; the other radar utilizes

the EVEN headstack. When using the DACOMP with its threefold compression, the FR-1800 is now able to accommodate up to six radar sites. These will be designated as the "ODD-1," "EVEN-1," "ODD-2", "EVEN-2," "ODD-3," and "EVEN-3" radars. Since the 28-track recorders use only the ODD-numbered tracks for the DACOMP data, these ODD and EVEN designations have been changed to letter designations, i.e., - "A," "B," "C," "D," "E," and "F."

The logic for each DACOMP consists of a wire-wrap plane or frame; these frames are physically incorporated into a DACOMP drawer, shown in figure 2. A drawer can accommodate four or six DACOMPs compressing an equivalent number of radars. The frames are stacked into two or three levels of two frames each. For a four-radar drawer, the radar sites are designated "ODD-1," "EVEN-1," "ODD-2," and "ODD-3." The four frames which accommodate these radars are located in the top and middle levels of the drawer and are shown in figure 3. For a six-radar drawer, the frames which accommodate the remaining two radars (EVEN-2 and EVEN-3) are located in the bottom level of the drawer, and are shown in figure 4.

The inside front of the DACOMP drawer contains a master oscillator assembly which supplies the crystal-controlled output clock pulses to each frame. The indicator lights on the front panel indicate when radar message data are present on each of the three input channels as well as the output channel for each of the four- or six-radar sites accommodated by the DACOMP drawer. In the six-radar DACOMP drawer, the oscillator and indicator logic is combined into a single board. A fan for cooling is also mounted on the front panel of the six-radar DACOMP drawer and is shown in figure 2. The rear of the drawer contains a +5-volt power supply, input/output connectors, and bypass relays which allow normal uncompressed recording when the drawer power is OFF. The output connectors are (BNC), and they match the recorder input cables which originally went directly to the recorder patch panel. The layout of a six-radar drawer is shown in figure 5. The various cable connections are located at the rear of the drawer and are shown in figure 6.

INSTALLATION

GENERAL.

RACK TYPES . The DACOMP drawer is installed in a standard 19-inch rack, 19 to 21 inches deep, provided locally. One of the automated radar terminal system (ARTS III) modem racks or one of the radar site modem racks may be used, but the DACOMP drawer must be the same rack in which the recorder jack panels are mounted due to the short interconnecting cables.

In all types of rack installations, the drawer slide assembly must be fastened at the front and rear of the cabinets. When using an FR-1800 recorder, the recorder patch panel and DACOMP drawer must be installed in the same rack. When using a VR-3700 or Sabre IV 28-track recorder, at least the record patch panel must be installed in the same rack that contains the DACOMP drawer.

When a radar site modem rack is used for the DACOMP installation, the large side brackets on which the final portion of the drawer slide is mounted must be moved outward slightly to allow for the greater width of the DACOMP drawer. When an ARTS III modem rack is used, outward movement of the brackets is not necessary; however, four holes must be drilled in the back side of the cabinet to anchor the back of the slides. The rear brackets of the slides may have to be inverted to mount satisfactorily in the rear of the rack.

A four-radar drawer requires 3.5 inches of vertical rack space, while a six-radar drawer occupies 5.25 inches of panel space. If there is additional heat-generating equipment in the same rack in which a four-radar DACOMP drawer is installed, forced-air cooling is required. The six-radar drawer contains its own fan; therefore, additional air cooling is unnecessary. Air is taken in from the front, blown across the logic, and exits the drawer via rear slots after cooling the power supply. Caution: Watch the ties worn by personnel when in front of the drawer!

POWER AND GROUNDING CONSIDERATIONS. Both types of DACOMP drawers require 120 volts alternating current (a.c.) single phase at not more than 150 watts; this is usually available at a convenience outlet inside the rack. The third wire (ground) of the a.c. outlet should be returned to the signal ground system rather than to the a.c. ground in the breaker panel. This is not a uniform practice in ARTCC's and may result in a.c. noise (i.e., from motors, relays, fluorescent lights, etc.) affecting the DACOMP logic. Signal ground and frame ground are tied together in all DACOMP drawers at the BNC connectors on the rear panel.

CONFIGURATION TYPES.

Operationally, the DACOMP drawers are installed between the recorder jack panel and the digital RECORD inputs of the recorder. It is assumed in the following descriptions that the DACOMP drawer is being added after the original recorder/patch panel installation. Each patch panel has been modified by NAFEC to provide the additional radar inputs to the DACOMP/recorder subsystem. This modification varies according to whether a four- or- six-radar DACOMP drawer is used, and also according to the recorder type. All interconnecting cables have been supplied.

When the DACOMP drawer power switch if OFF, deenergized relays inside the drawer bypass the DACOMP logic and provide normal recording paths between the patch panel and the recorder. No cabling has to be changed to include or remove the DACOMP function for the recorder operation.

There are three basic DACOMP/recorder configurations, each consisting of one DACOMP drawer and two recorders. It is assumed that each ARTCC will have two radar recorders. These basic configurations will accommodate up to 8 or 9 radar sites, and are used in all ARTCC's except Salt Lake City, which has 11 radar sites. A special configuration consisting of two DACOMP drawers and two VR-3700 recorders is used at Salt Lake City.

The three basic configurations are (1) one four-radar DACOMP drawer and two FR-1800 recorders, (2) one six-radar DACOMP drawer and two FR-1800 recorders, and (3) one six-radar DACOMP drawer and two 28-track recorders (VR-3700 or Sabre-IV). The special Salt Lake City configuration consists of two six-radar DACOMP drawers and two 28-track recorders (VR-3700). In each configuration, the RECORD inputs to the two recorders are to be connected in parallel after the DACOMP, but the (playback) outputs of each recorder must have their own playback patch panel. A description of each of the three basic configurations and of the Salt Lake City configuration follows.

FOUR-RADAR DACOMP DRAWER WITH FR-1800 RECORDERS. This configuration, shown in figure 7, records four radars (ODD-1, EVEN-1, ODD-2, and OLD-3) onto 8 of the 12 tracks of each FR-1800 recorder when in the DACOMP mode; the other four tracks are unused. In the normal uncompressed mode, the ODD-1 and EVEN-1 radars are recorded onto all 12 digital tracks of each recorder. (The FR-1800 recorder is a 14-track machine; two tracks are used for time-of-day and for tape servo data.) The RECORD cables, which originally went from each recorder to BNC connectors located at the rear of the recorder jack panel, are now connected to the 12 BNC output jacks (J103 through J114) located on the back of the DACOMP drawer. See example in figure 6. As seen in figure 7, the RECORD inputs of each recorder are connected in parallel. The connectors are marked as to which RECORD track the cable is to be connected. A new cable connecting the 12 BNC jacks at the rear of the recorder patch panel to connector J1 of the DACOMP drawer is shown. This cable applies the clock and data RECORD inputs for each of the three channels of the ODD-1 and EVEN-1 radars to the DACOMP drawer at connector J1. The clock and data RECORD inputs for the ODD-2 and ODD-3 radar channels are applied to the DACOMP drawer by another new cable extending from connector J4 of the recorder patch panel to connector J2 of the DACOMP drawer. This is the modification to the patch panel; the 13th through the 18th columns of jacks are brought out via J4. The cables connecting the playback jacks of each of the FR-1800 recorders to those of the recorder patch panel are not changed.

SIX-RADAR DACOMP DRAWER WITH FR-1800 RECORDERS. This configuration, shown in figure 8, records six radars onto 12 tracks of each of the two FR-1800 recorders when in the DACOMP mode. In the normal uncompressed mode, the ODD-1 and EVEN-1 radars are recorded onto all 12 tracks of each recorder.

The cabling of this configuration is identical to that of the four-radar DACOMP/FR-1800 configuration described in the previous section but with this addition. The clock and data RECORD inputs for the fifth and sixth radars (EVEN-2 and EVEN-3) are applied to the DACOMP drawer by a third new cable extending from connector J5 of the recorder patch panel to connector J3 of the DACOMP drawer. The patch panel modification brings the 13th to the last column of jacks out via J4 and J5.

SIX-RADAR DACOMP DRAWER WITH 28-TRACK RECORDERS. This configuration, shown in figure 9, can record eight or nine radars onto the 24 recording tracks of each of two Sabre IV or VR-3700 recorders when in the DACOMP mode. Six of these radars are compressed onto the 12 ODD record tracks of each recorder simultaneously through DACOMP connectors J1, J2, and J3. The remaining 12 EVEN

tracks are used to record the uncompressed data and clocks of two radars using three channels apiece (eight-radar total) or three radars using two channels apiece (nine-radar total). In the normal uncompressed mode, four radars utilizing three channels each or six radars utilizing two channels apiece can be recorded onto the 24 recording tracks of each of the two recorders simultaneously.

In the recorder patch panel, the lower 12 BNC connectors which were originally used for playback are now used to record the uncompressed data from the two or three radars onto the EVEN RECORD channels. As seen from figure 9, an entire patch panel is used to record, and each recorder now requires its own patch panel for playback. A limited number of additional patch panels for use as playback panels may be available at the Federal Aviation Administration (FAA) Depot under the following Federal Stock Number (FSN): 9274-407-7586, describe as "Kit for FR-1800 Recorder." This kit includes two 50-foot 12-coaxial cable bundles terminated with BNC fittings at each end, two identification strips, and eight patch cords. Reference: FAA Aeronautical Center Drawings DE-C-1005-1, DE-B-1005-2, DE-D-1005-3, and DE-B 1005-4.

SALT LAKE CITY CONFIGURATION. This configuration, shown in figure 10, can compress 12 radars onto the 24 recording tracks of each of two VR-3700 recorders connected in parallel. Six radars are applied to each of patch panel Nos. 1 and 2. As seen in figure 10, the odd tracks of the recorders are connected to the outputs of DACOMP 1. When DACOMP 2 is energized, the EVEN recorder tracks are connected through connector J7 of the relay box to the outputs of DACOMP 2, which consist of the compressed data from radars G through M. When DACOMP 2 is deenergized, the EVEN recorder tracks are connected through J6 of the relay box to the playback jacks of patch panel 1. These playback jacks contain the uncompressed data from radars C and D when DACOMP 1 is deenergized. When DACOMP 1 is energized, no output occurs from the playback jacks.
With both DACOMP's energized, the six radars applied to patch panel 1 (A through F) are compressed by DACOMP 1 and recorded onto the 12 ODD tracks of each VR-3700 recorder. The six radars applied to patch panel 2 (G through M) are likewise compressed by DACOMP 2, routed through connector J7 of the relay box, and recorded onto the 12 EVEN tracks of each recorder.

When only DACOMP 1 is energized, the six radars applied to patch panel 1 (A through F) are compressed by DACOMP 1 and applied to the 12 ODD tracks of the recorders.

The EVEN tracks are connected through J6 of the relay box to the playback jacks of DACOMP 1. However, since no output appears on these jacks when DACOMP 1 is energized, nothing is recorded onto the EVEN tracks.

When only DACOMP 2 is energized, the six radars applied to patch panel 2 (G through M) are compressed by DACOMP 2 and applied through connector J7 to the 12 EVEN tracks. The uncompressed data from the two radars connected to J1 of DACOMP 1 (A and B) are applied to the 12 ODD tracks. Hence, eight radars (six compressed and two uncompressed) can be recorded when only DACOMP 2 is energized.

With both DACOMP's deenergized, the uncompressed data from four of the six radars applied to patch panel 1 are applied to the 24 recording tracks. The data from two of these radars (A and B) are applied to the 12 ODD tracks through J1 of DACOMP 1. The data from the other two radars (C and D) are applied to the 12 EVEN tracks through connector J6 of the relay box.

As in figure 9, two additional patch panels are required for patching the playback signals of each recorder.

OPERATION

GENERAL.

The utilization of the DACOMP is straightforward. Its operation is completely automatic. With the drawer power switch turned OFF, the DACOMP logic is bypassed in all recording operations. The RECORD mode patching is then identical to that which existed before installation of the drawer. This applies to ARTCC's utilizing the 28-track VR-3700 or Sabre IV recorders, as well as ARTCC's using the FR-1800 recorders.

When the DACOMP power is turned ON, the relays in the DACOMP drawers become energized, thereby allowing the DACOMP logic to record information from additional radar sites. The patching schemes for the RECORD mode vary according to whether an FR-1800 recorder or a VR-3700/Sabre IV machine is used. These patching schemes are described in detail in the following two sections. It is assumed that the radar sites are using all three modem channels for data transmission, and that all three channels for each radar site will be patched over for a recording mission. If a radar site is using only two channels, these may be patched into any two of the three RECORD jacks for a radar position in the DACOMP drawer. The unused input channel may be left unused without affecting DACOMP operation.

The playback cables of all recorder types used are not affected, and the playback patching locations are still the same. However, separate patch panels are used for playback when using 28-track recorders. Furthermore, the information contained in a compressed radar will now be accessed at a single three-circuit jack representing one radar channel on the patch panel upon playback. The information content of the compressed radar consists of data and clocks, available at the tip and ring, respectively, of the three-circuit jack. The data and clocks of a compressed radar are recorded on two tracks of either the FR-1800 or VR-3700/Sabre IV recorders.

Since only one channel of a DRG is now required for each radar due to the compression, only one CD adapter per radar, instead of the original three, is now required for interfacing with the CCC. A single DRG will accommodate three

compressed radars. Adaptation of the particular CCC computer program being used may be required to compensate for the faster data input rate and the single adapter per radar. Other than this, no special requirement or equipment is necessary for playback other than an additional patch panel when using a VR-3700 or Sabre IV recorder. The CD format of the radar data has not been altered due to compression.

FR-1800 PATCHING.

With the DACOMP drawer power OFF, the data patched into the ODD or EVEN radars as designated in black on the recorder jack panel are recorded normally. The information from these radar channels will be recorded onto the tape via their respective head stacks and will be available on playback mode at the corresponding ODD or EVEN playback jacks. That is, the data and clock of the ODD radar channel, 1 for example, will appear at the tip and ring, respectively, of the ODD channel 1 playback jack during the playback mode. This is illustrated in figure 11.

With the DACOMP drawer turned ON, the information contained in the three channels of the ODD radar will be compressed into a single channel. These compressed data and clocks will then be recorded on tape on the same two tracks that were used to record the channel 1 data and clocks of the original ODD radar. This path can be seen in figure 12. Upon playback, the compressed data and clocks of the three channels of the original ODD radar now appear at the tip and ring of the ODD channel 1 playback jack.

In a similar manner, the information from any radar site patched into the three EVEN RECORD jacks will be compressed and recorded on the original EVEN channel 1 tracks. This information will appear at channel 1 of the EVEN playback jacks during playback mode. These original two radar site RECORD inputs are now designated as ODD-1, and EVEN-1, respectively. The corresponding DACOMP's in the drawer are also so designated.

The vacant jacks to the right of the playback section of the patch panel are now utilized for the additional radar inputs. The first three are designated as ODD-2, and go to the similarly-labeled DACOMP in the drawer. The next three jacks are the ODD-3 DACOMP inputs. These two new radars are recorded on those tracks previously occupied by channels 2 and 3, respectively, of the original ODD radar. Playback data are obtained by patching into the ODD radar channel 2 playback jack for the recorded ODD-2 radar. Likewise, the compressed ODD-3 radar information appears at the ODD radar channel 3 playback jack. The RECORD and playback paths of these four radars are shown in figure 12.

In the case of ARTCC's equipped with six-radar DACOMP drawers, the last six jacks to the right in the patch panel are used as DACOMP inputs for the EVEN-2 and EVEN-3 radars. Radar information patched into these locations will be recorded on those tracks originally used by channels 2 and 3 of the original EVEN radar designation. Table 1 lists the six radar inputs and the corresponding tracks for the compressed data and clocks.

TABLE 1. DACOMP/FR-1800 TRACK ASSIGNMENTS

DACOMP Frame	Recorder Tracks Data	Clock	Comments
ODD-1	11	13	
ODD-2	7	9	
ODD-3	3	5	
EVEN-1	12	14	
EVEN-2	8	10	Not used with four-radar drawer
EVEN 3	4	6	

The FR-1800 tape speed for use with the DACOMP drawer in operation must be 7.5 inches per second, thereby providing 4 hours or recording time for each 9,200-foot reel of tape. The 9375-Hz DACOMP clock rate exceeds the 9-kHz maximum data rate for a 3.75 inch-per-second tape speed; consequently, the next higher tape speed must be utilized.

VR-3700 OR SABRE IV PATCHING.

The 28-track recorders use separate patch panels for record and playback functions. These panels were intended for use with the FR-1800 recorder, so the original track and function designations on the panel back should be changed to be compatible with the 28-track machine. The six-radar DACOMP drawers were also originally designed to be used with the FR-1800 recorder. The individual DACOMP's within the drawer were designated in ODD and EVEN radar notation (i.e., ODD-1, EVEN-1, ODD-2, etc.). The radars used with the 28-track machine are alphabetically assigned, and the DACOMP designations should be changed to correspond with the configuration used. The two configurations to be discussed below are the single DACOMP/two 28-track recorder combination, which can record and play back up to eight or nine radars; and the two DACOMP/two VR-3700 recorder combination used at Salt Lake City. In either configuration, only the six-radar DACOMP is used, and the recording speed is the same as that used with normal recording, i.e., 3.75 inches per second.

SINGLE DACOMP CONFIGURATION. The single DACOMP/two 28-track recorder configurations can record up to eight or nine radars. These are alphabetically designated as radars A through H. The data from six of these radars (A,B,E,F, G, and H) are applied to the DACOMP. The compressed data and clocks from these six radars are applied to the 12 ODD tracks of the recorder. Designations C and D provide normal uncompressed recording of two three-channel (or three two-channel) radars. This information is applied directly to the 12 EVEN tracks of the recorder.

The RECORD/playback paths of the single DACOMP configuration is shown in figure 13. Actually, as in the DACOMP/FR-1800 configuration described previously, two recorders are used in parallel, and the RECORD inputs are applied in parallel to each recorder.

Figure 14 shows the patching arrangements for RECORD and playback patch panels. The track assignments for normal and DACOMP use are shown in table 2, along with patch panel and DACOMP plug designations. It will be noted that with the DACOMP turned OFF, radars A and B are recorded on the ODD tracks while radars C and D are recorded on the EVEN tracks.

TWO-DACOMP CONFIGURATION. The two-DACOMP/two-VR-3700 recorder configuration used in Salt Lake City compresses 12 radars onto the 24 available tracks of each recorder. Radars A,B,C,D,E, and F are applied to data compressor 1 (see figure 10) and the compressed clocks and data applied to the 12 ODD tracks of each recorder. Likewise, radars G,H,J,K,L, and M are applied to DACOMP 2 of figure 10, and the compressed clocks and data applied to the 12 EVEN tracks of each recorder. The track assignments are shown in table 3, while table 4 shows the combination of recording capabilities using both, either, or neither of the two DACOMP's.

THEORY OF OPERATION

BASIC CIRCUIT DESCRIPTION.

Each DACOMP consists of a wire-wrapped logic plane containing 128 integrated circuits. The DACOMP drawer contains four or six such planes. Basically, each DACOMP consists of six serial-in, serial-out storage registers, along with associated control and timing logic. This is shown in simplified form in figure 15. Also contained in the DACOMP drawer are the +5-volt power supply, the six bypass relays, and a master crystal oscillator.

Each of the three radar input channels utilize two of the six storage registers in the DACOMP logic plane. Each register (A or B) stores a single incoming search (four-field) or beacon (seven-field) message. As the digitized messages are continuously outputted from the CD, one of the registers on each channel is always accepting and checking the incoming data. The control logic of each "online" register checks for IDLE character fields between messages. These idle characters are used to synchronize the input bit and field counters of the channel.

Upon receipt of the first field of a message, the message label is checked to determine if it is a four-field (search) or a seven-field (beacon) message. The appropriate message-length flip-flop is then set. IDLE character decode is inhibited during the time that a message is being shifted in. When the entire message has been loaded into the online register (as determined by the input field counter and the message-length flip-flop), the register is taken offline and the other register of the channel becomes available for the next input message. A register-full flip-flop is then set to notify the output logic that

TABLE 2. RECORDER TRACK ASSIGNMENTS AND CONNECTOR CROSS-REFERENCES FOR SINGLE DACOMP/28-TRACK RECORDER CONFIGURATION

Radar	Record Panel Rear	In - DACOMP - Out	Normal Tracks	Comp. Tracks	Each Playback Panel Rear
A1	Record 11/13	J1 - M/P J111/J113	3/5		Record 1/13
A2	R 7/9	- H/K J107/J109	7/9	3/5	R 7/9
A3	R 3/5	- C/E J103/J105	11/13		R 3/5
B1	R 12/14	- N/R J112/J114	17/19		R 12/14
B2	R 8/10	- J/A J108/J110	21/23	7/9	R 8/10
B3	R 4/6	J1 - D/F J104/J106	25/27		R 4/6
C1	Playback 11/13		2/4		Playback 11/13
C2	P 7/9		6/8	Same	P 7/9
C3	P 3/5		10/12	Tracks	P 3/5
D1	P 12/14		16/18	As	P 12/14
D2	P 8/10		20/22	Normal	P 8/10
D3	P 4/6		24/26		P 4/6
E1	J4 - M/P	J2 - M/P			
E2	- H/K	- H/K		11/13	
E3	- C/E	- C/E			
F1	- N/R	- N/R			
F2	- J/A	- J/A		17/19	
F3	J4 - D/F	J2 - D/F			
G1	J5 - M/P	J3 - M/P			
G2	- H/K	- H/K		21/23	
G3	- C/E	- C/E			
H1	- N/R	- N/R			
H2	- J/A	- J/A		25/27	
H3	J5 - D/F	J3 - D/F			

NOTE: Pins and tracks given in Data/Clock format, i.i., 11/13 (11- Data/13 = Clock)

TABLE 3. RADAR/RECORD TRACK ASSIGNMENTS FOR TWO-DACOMP CONFIGURATION (TWO DACOMPS ON 28-TRACK RECORDER)

Radar	DACOMP	DACOMP ODD/EVEN	Signal	Track
A	1	ODD-1	Data	3
			Clock	5
B	1	ODD-2	D	7
			C	9
C	1	ODD-3	D	11
			C	13
D	1	EVEN-1	D	17
			C	19
E	1	EVEN-2	D	21
			C	23
F	1	EVEN-3	D	25
			C	27
G	2	ODD-1	D	2
			C	4
H	2	ODD-2	D	6
			C	8
J	2	ODD-3	D	10
			C	12
K	2	EVEN-1	D	16
			C	18
L	2	EVEN-2	D	20
			C	22
M	2	EVEN-3	D	24
			C	26

TABLE 4. COMBINATIONS OF RECORDING CAPABILITIES FOR TWO-DACOMP CONFIGURATION

Condition	Radar	Recording Capability	Tracks Not Used*
Both DACOMP's OOO	4:	Direct; A&B (ODD) C&D (EVEN)	None
Both DACOMP's On	12:	Compressed; A,B,C,D,E,F,G,H,J,K, L, and M	None
DACOMP 1 ON	6:	Compressed; A,B,C,D,E,F,	All even tracks not used.
DACOMP 2 ON	8:	Direct; A and B Compressed; G,H,J,K,L and M	11,13,17,19,21, 23,25, and 27

*This does not include the spare tracks 1 and 28.

the now offline register has data ready for the output line. The message is then shifted out of the register onto the single output channel at the 9375-Hz clock rate before the other register becomes full. The message (data) is outputted on one of the two lines of the channel, while the 9375-Hz clock is outputted on the other line.

The output logic consists of an output bit counter and an output field counter, polling logic, and the transfer gating. The counters determine the bit and field times of the data being handled, and also control the operations of the output logic. IDLE characters are generated from the output bit counter, and are always present on the output channel when messages are not available from the input registers. During idle character output time, the polling logic checks the six register-full flip-flops and stops its polling sequence when a full register is found. When the IDLE character field is completed, the transfer gating is enabled. The selected register is connected to the output channel, a 9375-Hz clock is applied to the register, and the data contents are shifted out to the recorder. The size of the message is also transferred to the output field counter to set its run length. When the data have been completely clocked out, a pulse is transferred back to reset the message-length flip-flops and the register-full flip-flop of that register. Then an IDLE character is put on the output channel, the transfer gating is disabled, and the polling logic begins looking for the next full register.

A crystal-controlled clock assembly in each drawer supplies a 1.5-megahertz (MHz) clock for the polling logic and 18.75 kHz for the output clock. Indicators on the front panel show when data are present on any of the three input channels or on the output of each DACOMP. If an IDLE character only is present on any input channel, the corresponding indicator will not be ON. Likewise, the output indicator will not be lit if the output channel has only IDLE characters on it.

DETAILED CIRCUIT DESCRIPTION.

INPUT LOGIC. Channel one of a DACOMP will be used in the detailed description of the input logic, however, the operation of the other two DACOMP input channels is identical. This input logic is shown in channel 1 input logic diagram XD2588-A1, appendix A. Sections of this logic described below are shown in figures 16 through 21.

INPUT CONDITIONING . The input data obtained from the modem and the 2400-Hz clock generated in the modem are bipolar; i.e., the logic one state is represented by a +6-volt condition, while the logic zero state is represented by a -6-volt condition. These bipolar inputs are reshaped and the logic levels clamped to +5 and 0 volts for the logic one and zero states, respectively. This is done by input-conditioning circuitry which is identical for data and clock inputs. The input conditioning circuitry for the data inputs, shown in figure 16, will be referenced in the following discussion.

The bipolar input (IDTA-1) is shown in waveform (a) of figure 16. The diode in clipper assembly (612) clamps the positive excursion at +5 volts. The resistor and capacitor of this clipper assembly form a low-pass filter to

eliminate high-frequency noise which might be riding on the input line. The negative excursion of the bipolar input is clipped off by the diode in integrated circuit (IC) 618-1, resulting in waveform (b). This waveform is reshaped by IC 618 (pins 1 and 2) which is a Schmidt trigger. The inverted waveform (c) is shown at 618-2. A second section of IC 618 (pins 3 and 4) adds additional reshaping and reinversion, resulting in waveform (d) at 618-4.

In the case of the clock input conditioning circuitry (figure 17), both phases from IC 618 are required. The inverted input clock (CLK-1) is applied to the shift register clock gate (64), while the normal reinverted sense (104) is delivered to the input bit counter, IC 622 and 623.

SHIFT REGISTER. The reshaped data pulses are clocked into the online shift register, which is shown in figures 18 and 19. Shift register A will be assumed to be online for the purpose of this discussion. This shift register comprises eight IC's; 621, 615, 36, 35, 34, 33, 32, and 31. IC's 621, 615, 34, and 31 store eight bits each, while IC's 36, 35, 33, and 32 accommodate 16 bits apiece. Connected serially, they constitute a storage register for the 52 or 91 bits (four or seven fields) of each valid search or beacon message from the CD.

The first 13 bit positions are brought out for decoding of the IDLE character and the first field (message label) of each message. These 13 bit positions consist of all the 8 bit positions of IC 621 and the 5 leftmost bit positions of IC 615 (figure 18). In addition, taps for the 52nd (IC 34) and the 91st (IC 31) bit positions (figure 19) are also brought out since they are the locations of first bit in a complete search or beacon message.

IDLE CHARACTER DECODE . Decoding of the IDLE character between messages is necessary to keep the bit and field counters of the channel in synchronization during message times. In register A, the first 13 bit positions are applied to a gate 614, which is expanded by diode assemblies 68 and 620 (figure 18). The IDLE character consists of 3 logic zeroes followed by 10 logic ones. Since the decode gate requires a logic one on all inputs, the first three bit positions from IC 615 (pins 5, 6, and 10 (figure 18)) are inverted by 69-8 and 69-11 and applied to pins 10 and 12 of gate expander 68. In the initial condition, the IDLE INHIBIT lines, 111 and 113, will each be in a logic one state. These lines, applied to pins 13 and 11, respectively, of the gate expander 68, enable this gate to decode the IDLE character.

When an IDLE character is detected, a logic zero occurs at the output of NAND gate 614-8. This signal, IDLE character decode (ICD-1A), is OR'ed with the B-register IDLE character decode (ICD-1B) in IC 67 to become the bit/field counter reset signal BFCR-1. This signal is applied to 67-11,12 (figure 20). The negative-going output (FCR-1) is used to reset the field counter 617. BFCR-1 is also OR'ed with the bit-13 count of the bit counter 622 and 623 (B13-1, figure 17) to reset that counter back to state zero. Thus, upon receipt of a valid IDLE character, both the bit and field counters are cleared to state zero, thereby putting the channel in bit and field synchronization with the output circuitry of the CD. This IDLE character is not used by the output logic, since the latter contains its own IDLE character generator.

BIT COUNTER. Flip-flops 623 and 622 (figure 17) comprise a divide-by-thirteen counter. They are connected in a semisynchronous mode to minimize change-of-state delays. This is accomplished by toggling the one- and two-count flip-flops (623) in synchronism with the reshaped clock, but not applying the clock to the fourth- and eight-count flip-flops (622).

State 13 (NB13-1) of the counter is decoded by gate 616-6 (figure 17) and inverted through 610-8 to become B13-1. This is then OR'ed with the bit field counter reset level (BFCR-1) through 610-6 to reset the counter back to state zero as bit counter reset (BCR-1A.) The bit counter then steps through states zero to 12, resets on count 13, and starts over as long as a clock is present.

Synchronization with the idle character is introduced through 610-4 which resets the bit counter when an IDLE character is satisfactorily decoded.

State zero of the bit counter is decoded by the other half of IC 616 (figure 20) to indicate the beginning of field times. This level, NB00-1, appears at 616-8 and is applied to field decoder 611. This level is used twice in the input operation: the first time is when the first (message label) field is occupying the first 13 positions of the register and is ready for message length decode; the second use is to generate a shift register full signal (SRFS) when all 52 or 91 bits of the message have been inputted into the register.

FIELD COUNTER. The field counter (IC 617, figure 20) is stepped by the negative-going edge of the end of field signal (EOF-1) from 622-5 of the bit counter. This negative edge is present when the bit counter is reset to zero. The field counter is a four-stage binary counter IC of which only the first three stages are used for a count of zero through seven. The field counter is reset to state zero by FCR-1 (617-13), which was produced by the IDLE character decodes. As long as the incoming data consists of IDLE characters only, the field counter is kept in state zero. When a search or beacon message appears, its first field allows the field counter to be incremented to state 1. This state is decoded by IC 611 and appears as a negative level at 611-11 when enabled at bit-time zero by NB00-1 at the 611-D input. The output of 611-11 is a signal (FLD1-1) which occurs during the first bit time of field one, when the message label is in position in the register. FLD-1 is steered by 610-11 (figure 21) to enable the two message-size flip-flops IC63.

MESSAGE SIZE DECODE. This circuitry is shown in figure 21. A four-field message is characterized by bits 2 and 3 in its label field each being set to zero. These are pins 6 and 5, respectively, of IC 615 in the storage register. A four-field message is decoded by gate 69 to produce search label decode (SLD-1A) at 69-8. This stores a "one" in the four-field length flip-flop 63-9.

In a seven-field message, bits 2 and 3 of the message label field are each at the logic one condition. This condition is decoded by NAND gate 67 to generate the beacon label decode signal BLD-1A at 67-4. BLD-1A is a negative-going level; hence, this stores a logic zero in the seven-field length flip-flop 63-5.

When a four-or seven-field length message has been decoded and its corresponding length flip-flop set, IDLE decode inhibit lines 113 or 111, respectively, will go to the logic zero state. This inhibits IDLE decode gates 68, 614, and 620 (figure 1e), thereby preventing an erroneous decoding of subsequent message data fitting an IDLE character bit pattern.

The actuation of either of the message length flip-flops (63) will select the correct output line from the shift register using gate complex 47 (figure 19). If the four-field length flip-flop has been set, line SCH-1A (63-9) will be high (logic one state) and will enable the outputting of the four-field message from the 52-bit tap of shift register IC 34-6 through pins 9 and 10 of gate 47. Similarly, if the seven-field length flip-flop has been set, line BCN-1A (63-6) goes to the logic one state, enabling the outputting of the seven-field message from the 91-bit tap of shift register IC 31-5. In either case, when the message is ready for outputting, it will be shifted out of the register to the output data line (NOD-1A) via this path (47-8).

SHIFT REGISTER FULL LOGIC. As additional fields of the message are clocked into the shift register from the modem, the field counter keeps track of the number of fields in the register. The field count decoder (IC 611 figure 20) is strobed by the bit-zero decode of the bit counter, so that each output of the decoder occurs only when the respective field is in the first 13 positions of the register, i.e., in IC 621 and the five leftmost bits of IC 615 (figure 18). When a field-four decode (611-8, figure 20) occurs, the fourth field will have been completely inputted into the first 13 bit positions of the register, while the first bit of the first field (label field) occupies bit position 52. If this is a four-field message, the entire message is now in the register. The four-field length flip-flop 63-9 (figure 21) will have been set to the logic one condition by the message label decoding logic described earlier (69-8, figure 21). This puts a high level on 62-9 (figure 19). The 4EOM-1 line goes high due to inversion of the field-four decode by 65 (figure 20) putting a high level on 62-10 (figure 19). Similarly, if this is a seven-field message, gate 62 will be enabled by the coincidence of a seven-field message label decode (BCN-1A) (63-6 to 62-12) and bit time zero of the seventh field (611-6, figure 20, inverted through 65-13, thence on 7EOM-1 to 62-13, figure 19).

In either case, when the message has been fully inputted into the shift register, gate 62 will generate a shift register full signal (SRFS-1A). This signal does two things: first, it sets shift register full flip-flop (48-10, figure 19) to tell the output logic, via SRF-1A, that shift register A of channel one is full; secondly, the shift register control flip-flop (65) is caused to toggle, thereby enabling the opposite register in the channel (B in this example) to accept the next message from the CD, and disconnecting register from the incoming clock and data. Signal SRFS-1A applied to 65-2 (figure 19) forces SRC-1A low and SRC-1B high.

Since the next field of the incoming data is the IDLE field, this is now clocked into register B and decoded as in register A to synchronize the bit and field counters. Except for the common bit and field counters, register B is identical in operation to the first register. When the B register becomes

full, the SRFS-1B signal sets shift register full flip-flop (48-4, appendix A), telling the output logic that shift register B of channel 1 is full and available for outputting. The SRFS-1B signal also retoggles the shift register control flip-flop 65. This now reconnects shift register A to the incoming data. Since the message in shift register A will have been completely clocked out by the output logic (to be described below) before shift register B becomes full, shift register A is thereby ready once more to receive the next CD message.

OUTPUT LOGIC. The output logic controls the transfer of the CD data from the six input registers of six-DACOMP drawer to the output line and supplies the 9375-Hz output clock. The output logic runs asynchronously with respect to each of the six input sections, but there is a series of control and timing signals between the two areas for the proper transfer of data. This output logic is shown in FR-1800 data compressor output logic diagram XD2588-A4, appendix A. Sections of this logic described below are shown in figures 22 through 29.

CLOCK SOURCE. The source for the several clocks used in the output logic consists of a 3 megahertz (MHz) crystal oscillator located on the front of the DACOMP drawer (figures 3 and 5). The 3-MHz output of this oscillator is then applied to a divide-by-10 counter which is followed by a divide-by 16 counter to produce an 18.75-kHz output. This 18.75-kHz output, together with a 1.5-MHz output taken off the first stage of the divide-by-10 counter, are supplied to each of the four or six individual DACOMP's contained in the drawer. Within each DACOMP, the 1.5-MHz output is used as a clock for the polling logic to be described later. The 18.75-kHz output is divided in half to provide the 9.375 kHz output clock.

OUTPUT BIT COUNTER. The output bit counter (OBC) shown in figure 22 consists of flip-flops 104A and 104B connected to form a divide-by-13 counter, corresponding to each of the 13 bits in a message field. The 18.75-kHz input to the DACOMP from the clock source is divided by flip-flop 116B to produce the 9375-Hz clock, one phase of which is used to drive the OBC. The OBC operates in a semisynchronous mode with flip-flop 104A and 104B toggling simultaneously in synchronism with the 9375-Hz clock. Flip-flops 103A and 103B are also toggled simultaneously, but in synchronism with the Q- output of 104B; hence, the OBC operates as a ripple counter between the two sections.

Gate 102A decodes state 13 of the counter and immediately resets the counter to state zero. The counter then steps consecutively between states zero and 12, thereby producing the 13 bit counts corresponding to a message field.

IDLE CHARACTERS. Gates 102B and 102C generate the IDLE field from the OBC. The logic is such that states zero, one, and two of the OBC produce a logic zero out of 102C, while states 3 through 12 produce a logic one out of gate 102C. The IDLE character or pattern therefore consists of 3 zeroes followed by 10 ones, i.e., - 000 11111 11111. This pattern is applied to the DACOMP output between each message as well as when no message data are available for the output line.

OUTPUT FIELD COUNTER. The output of 103D output bit counter, stage D (OBCD) drives the output field counter (OFC) 108. The OFC and its associated logic are shown in figure 23. The OFC is a synchronous four-stage binary counter which keeps track of the message fields on the output line. Only the first three flip-flops in the counter are utilized, thereby making it an octal counter; i.e., states zero through seven. State zero of this counter will always put an IDLE character on the output line. After the IDLE character had been outputted, the OFC goes from state zero to state one. This is decoded by 109, which is a binary-to-octal decoder. The output of 109 (NFLD-1) is at a logic zero level during field one time. If there are no data ready in the shift registers, the ASRF line will be in the logic zero state. This condition resets the OFC to state zero again via gates 115B and 115C and single-shot 114. The NFLD-0 (state zero) signal from 109 is inverted by gate 122A and delayed 700 microseconds (μs) by the Negative Output Field Counter Reset (NOFCR) output of single-shot 114 to eliminate irregularities in timing due to changes in the states of the OFC. The output of 122A (FLD-0) is used to gate the IDLE character to the output line (OUTDTA) via gates 122B and 120A.

As long as no shift register is full, this logic will repeat itself, providing an IDLE pattern on the output to the recorder each field time. The 9375-Hz clock from 116B is sent to the recorder via driver/gate 120B.

POLLING LOGIC. When the output counter is sending an IDLE character to the recorder, the polling logic portion of the output logic is continuously checking each of the six shift register full (SRF) flip-flops (48, figure 19) looking for a full shift register. The polling is done by the polling counter, comprised of flip-flops 116A, 110A, and 110B. This logic is shown in figure 24. The polling counter is driven by the 1.5-MHz clock from the master oscillator assembly. The outputs of the polling counter PCA, PCB, and PCC are applied to transfer gates 21, 118, 111, 27, and 213. Each of these gates is an octal decoder or an eight-to-one multiplexer, but functions as a transfer gate to or from the input logic. Each will be discussed individually with its related function.

Output lines SRF-1A, 1B, 2A, 2B, 3A, and 3B from the six SRF flip-flops 48 (figure 19) are applied to the full register select multiplexer 21, as shown in figure 24. One of these six lines is gated to the output depending upon the octal state of address lines A_0, A_1, and A_2, which, in turn, depends upon the logic state of the polling counter. When the polling counter is running, the logical state of each of the six SRF flip-flops is checked every 8x667 nanoseconds (ns), or 4.3 μs. The polling sequence is SRF-1A, 2A, 3A, 1B, 2B, 3B, 1A, 2A, etc.

The state of the SRF flip-flops being checked determines the state of the line POLL and its complement NPOLL from multiplexer 21. As long as the SRF flip-flop is reset (SRF-n is in the logic zero state), the line POLL will be in the logic one state. This enables the first stage of the polling counter (116A) to be toggled by the 1.5-MHz clock, advancing it to the next octal count. If the next SRF flip-flop in the polling sequence is set (SRF-n +1) is in the logic one state), the POLL line will go to the logic zero state. This will remove the enabling levels on 116A, thereby freezing the polling counter at

that octal address until the SRF flip-flop, which had been set, becomes cleared. The octal code now on the PCA, PCB, and PCC lines is applied to all the transfer gates, selecting signals to and from that particular shift register's logic.

The complement of each of the six SRF flip-flops (NSRF-1A through 3B) is applied to gate 15 of figure 24 to generate the any shift register full signal ASRD. When no shift register is full, all six inputs to gate 15 will be in the logic one state. The ASRF line will then be in the logic zero state, thereby causing the OFC to be immediately reset to the octal zero count whenever it advances to the octal one state, as explained previously.

DATA TRANSFER. When the polling logic has found a full shift register, several steps occur to transmit the four- or seven-field CD message from the shift register to the recorder. First the Negative Shift Registor Full (NSRF) line into gate 15 from the SRF flip-flop concerned will go to the logic zero state. This forces the ASRF line to the logic one state, which inhibits the resetting of the OFC upon reaching the octal one count. With OFC in state one, figure 23 shows that line NFLD-0 will be in the logic one state, while FLD-0 will be in the logic zero state. This disables transmission of the IDLE character through 122B and enables the output data line ODATA from the data transfer multiplexer 213. The path taken by the output data is shown in figure 25. The data transfer multiplexer had selected the appropriate data line NOD-n from the selected shift register when the polling counter had stopped. Now the path to the output is completed through gates 122C and 120A whenever the OFC is in any state other than zero. The first data bit of the message is now on the output line. To shift out the remaining CD data stored in the selected shift register, a 9375-Hz clock must be applied to the shift register. This clock must be delayed one bit time, since the first data bit is already on the output line. The manner in which this one-bit delay is accomplished is shown in the clock-enabling logic of figure 26 and in the timing diagram of figure 27. As seen in figure 26, the 9375-Hz clock is continuously available at the clock select gates 64 of all six input channels; however, the actual logic is shown only for channels 1A and 1B. Assume that shift register 1A is filled and ready to be outputted. The 2400-Hz input clock to shift register 1A has been shut OFF, since input data are now being loaded into shift register 1B.

The required one-bit time delay is generated by one-shot 107, inverter 101C, and gate 101B. The one-shot has a delay of nominally 60 to 80 μs and is shown as waveform "D" in figure 27. The output of gate 101B is the ENABLE signal (waveform "E" of figure 27), which is delayed from the start of field one by the amount of time imposed by the one-shot 107. This enable signal is steered by the clock enable decoder 111 to the selected shift register logic (in this case, 1A). The decoder output is inverted by gate 117, becoming, in this case, SEL-1A (waveform "G" of figure 27). This is AND'ed with the 9375-Hz clock applied to the clock-select gate 64 (waveform "F," figure 27). The output clock (waveform "H," figure 27) now starts at the second bit time, shifting the second bit of the message onto the output line.

MESSAGE SIZE CONTROL. The OFC must now know how many fields must be clocked out of the selected shift register to complete the message outputting. The message will either be four or seven fields in length. The manner in which this is done is shown in figure 28.

The state of the beacon (seven-field) message flip-flop (63, figure 21) appears at line BCN-1A. The logic level on this line is transferred via the message size transfer multiplexer 27 to control the run length of the OFC. If the beacon message flip-flop is not set, then a four-field message was received. Therefore, if the MSGSZE line from 27 is at the logic one state, a seven-field message is in the selected shift register, and the OFC will be allowed to run to its last state, state seven. It will then revert to state zero as part of its normal sequence and allow an IDLE field to be transmitted after the message. Gate 115A in figure 28 controls the run length of the OFC. When MSGSE is in the logic one state, gate 115A is inhibited, and the OFC runs as described above. When a four-field message has been inputted, MSGSZE will be in the logic zero state and the OFC will reset to the zero state immediately upon entering state five. This happens because line NFLD-5 from the OFC decoder 109 will go to the logic zero state as soon as it enters state 5. Gate 115A then operates, triggering one-shot 114 via gate 115C and resetting the OFC. The states of the OFC correspond to the message field being clocked out; i.e., state one means that message field one is on the output lines, state two means that message field two is being outputted, etc. State zero clocks out the IDLE field.

END-OF-MESSAGE RESET. After the CD message has been transmitted to the recorder, the shift register full flip-flop (48) for the selected shift register must be reset in order to allow the polling counter to resume searching for full registers. The logic for accomplishing this is shown in figure 29. When the OFC is reset upon the completion of a message output, the last flip-flop (OFCC) of the counter will make a negative transition. This transition is inverted by 101D and then differentiated by an RC network 113 to produce a positive pulse at the input to gate 101A. Gate 101A is enabled only when a full shift register has been selected; that is, when line NPOLL is in a logic one state. The resulting negative pulse (SRFR) from gate 101A is routed to the appropriate SRF flip-flop 48 via multiplexer 118. The nominal 50- to 100- ns pulse resets the SRF flip-flop as well as the two message-length flip-flops of that register. Once the SRF flip-flop is reset, the POLL line from multiplexer 21 goes to a logic one state, allowing the polling counter to resume its sequence.

INDICATOR LOGIC.

Indicator lights are provided on the front panel to tell the user that the DACOMP assembly is functioning. The logic is shown in figure 30. The two SRF flip-flop outputs from each channel are OR'ed together via gates 121A, B, or C to drive a light-emitting diode (LED). This indicates that data have been loaded into one of the two registers of that channel. The FLD-0 signal from the OFC decoder 109 is in the logic one state when the OFC is in any state other than state zero; i.e., when data are being sent to the recorder. This signal is used to drive the OUTPUT via a 2N3702 transistor. None of the LED's come on when an IDLE character is present on the input or is being outputted.

SUMMARY OF RESULTS

1. The DACOMP, because of its threefold data compression capability, reduces the number of tracks required to record information from a radar site from six to two.

2. Because of the threefold reduction in recording track requirements, use of DACOMP's will enable ARTCC's to record information from an increased number of radar sites on the recorders that are available to them.

3. Use of a DACOMP with an FR-1800-type recorder will increase the recording capability of this recorder type from two to six radar sites.

4. Use of a DACOMP with a Sabre IV or VR-3700-type recorder will increase the recording capability of these recorder types from four to eight or nine radar sites.

5. Use of two DACOMP's with a Sabre IV or VR-3700-type recorder will increase the recording capability of these recorder types from 4 to 12 radar sites. This configuration is in use at Salt Lake City ARTCC, which has 11 radar sites.

6. When the DACOMP is deenergized, normal uncompressed data recording occurs. Patching or cable changes are not necessary when going from uncompressed to compressed recording.

7. Playback cables and patching locations are not affected by installation of DACOMP's; however, separate patch panels are required for playback when using 28-track recorders such as Sabre IV or VR-3700.

8. When using FR-1800 recorders in the DACOMP mode, a tape speed of 7.5 inches per second must be used. When using VR-3700 or Sabre IV recorders, the same recording speed is used in DACOMP mode as for normal recording; i.e., 3.75 inches per second.

9. Only one CD adapter per radar site, instead of the original three, is required for interfacing with the CCC when DACOMP's are employed.

10. The CD format of the four- or seven-field digitized message reports from the radar sites has not been altered due to compression; however, adaptation of computer programs may be required to compensate for the increase in data rate from 2400 to 9375 or 12,000 Hz and also for the single CD adapter per radar site.

11. The 9.375 (or optional 12) kHz output clock rate of the DACOMP was found to adequately accommodate high message densities.

12. DACOMP's are currently in operation in all but 1 of the 20 ARTCC's.

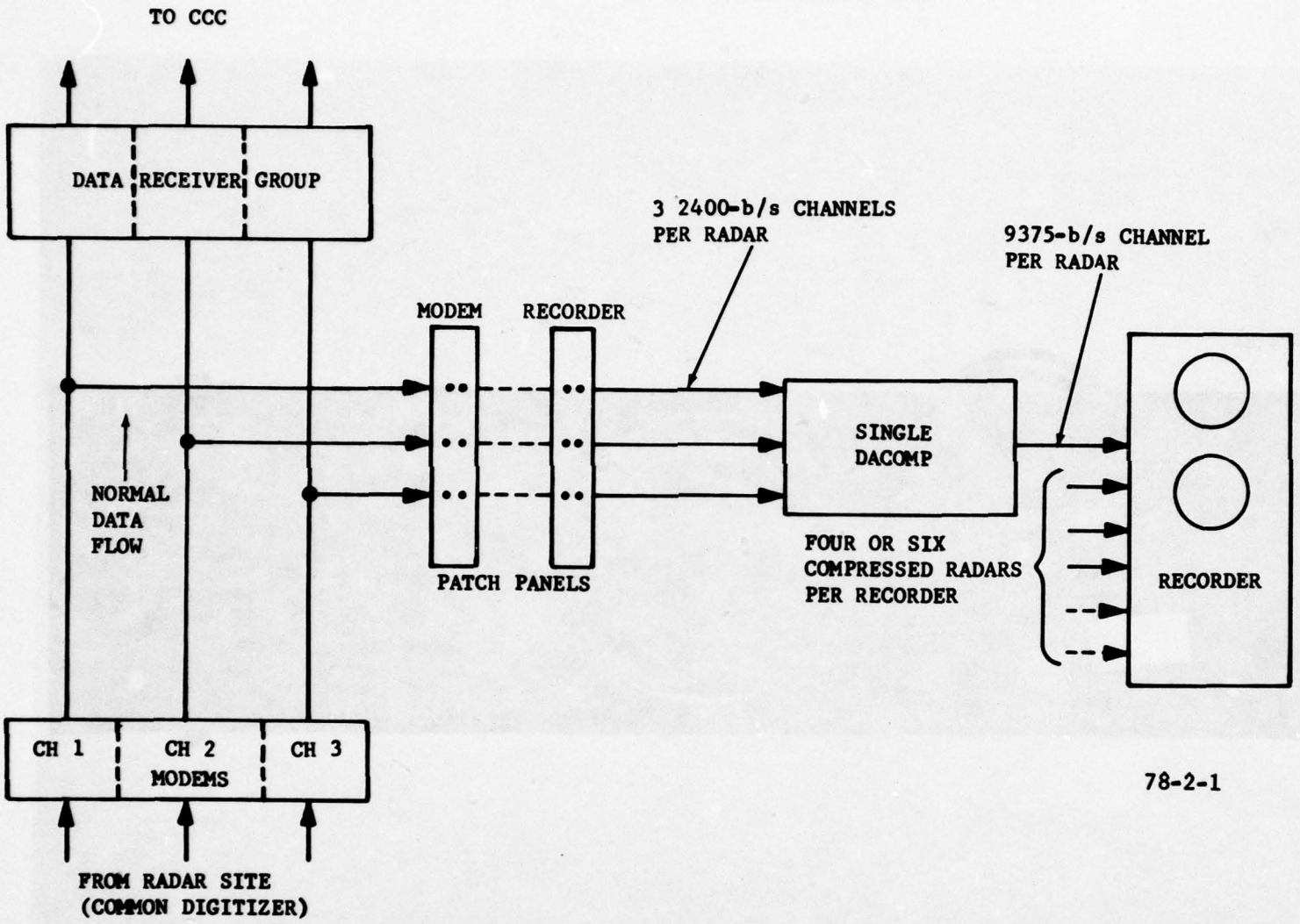


FIGURE 1. DATA PATHS--CD TO RECORDER

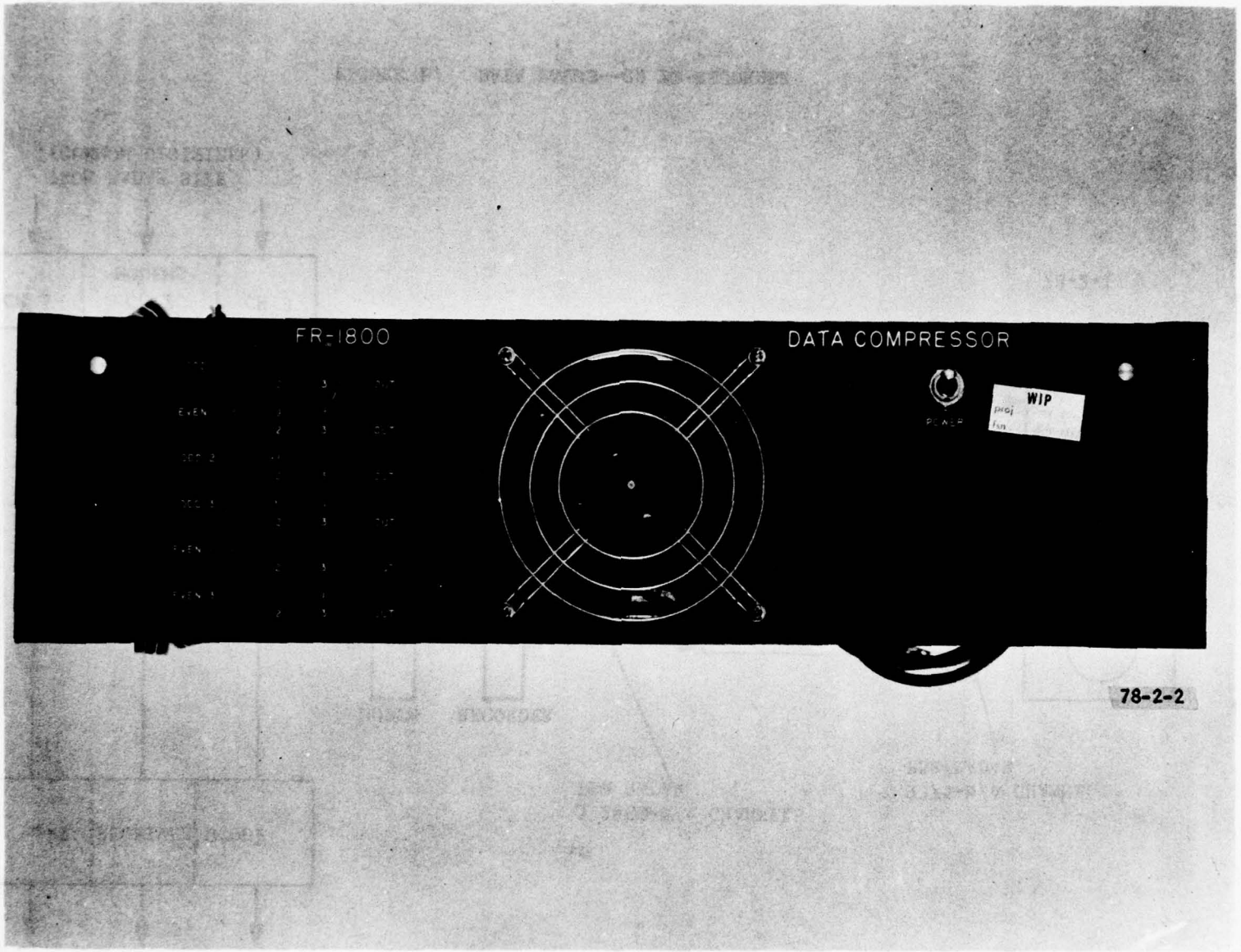


FIGURE 2. SIX-RADAR DACOMP DRAWER

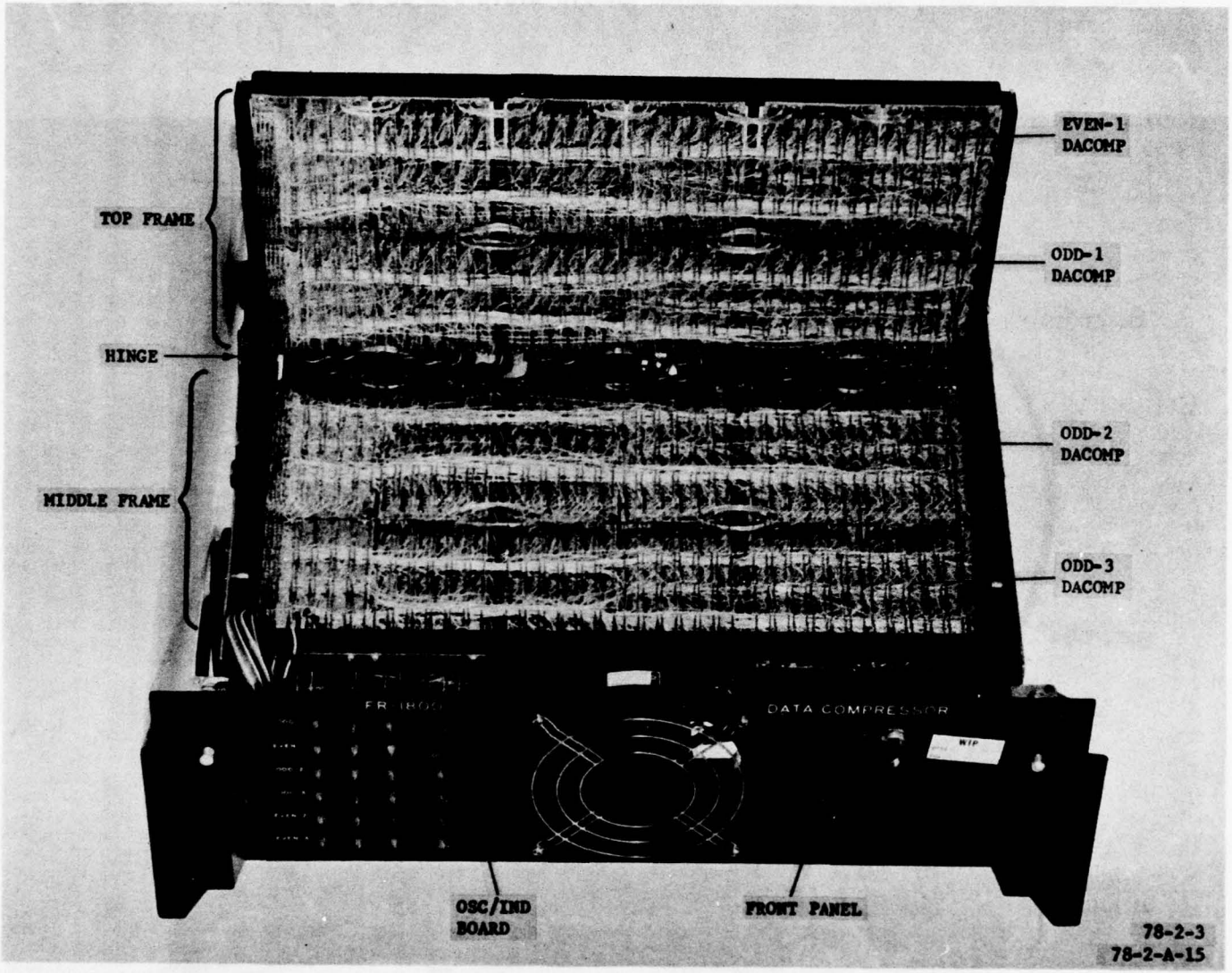


FIGURE 3. FRONT VIEW OF SIX-RADAR DACOMP DRAWER SHOWING TOP AND MIDDLE LEVELS

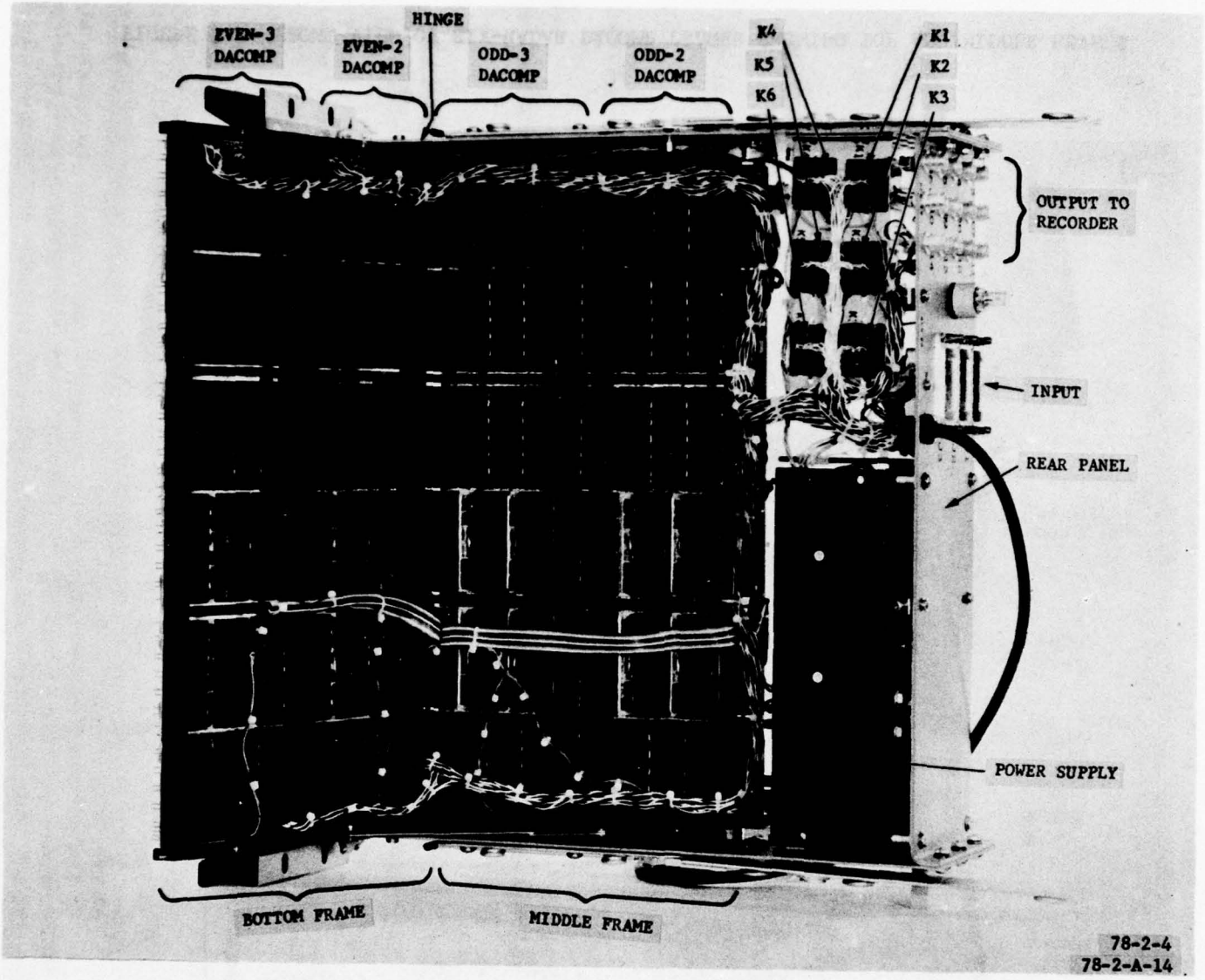


FIGURE 4. BOTTOM VIEW OF SIX-RADAR DACOMP DRAWER SHOWING MIDDLE AND BOTTOM LEVELS

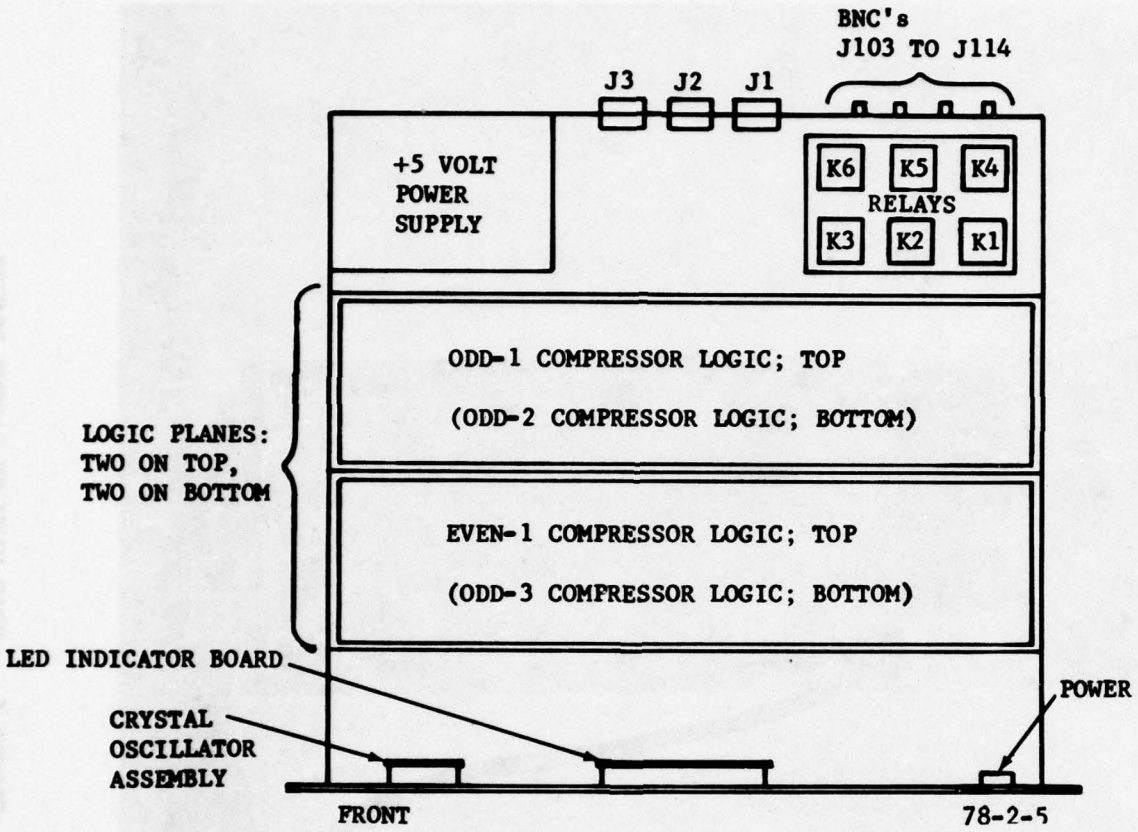


FIGURE 5. DATA COMPRESSOR DRAWER LAYOUT

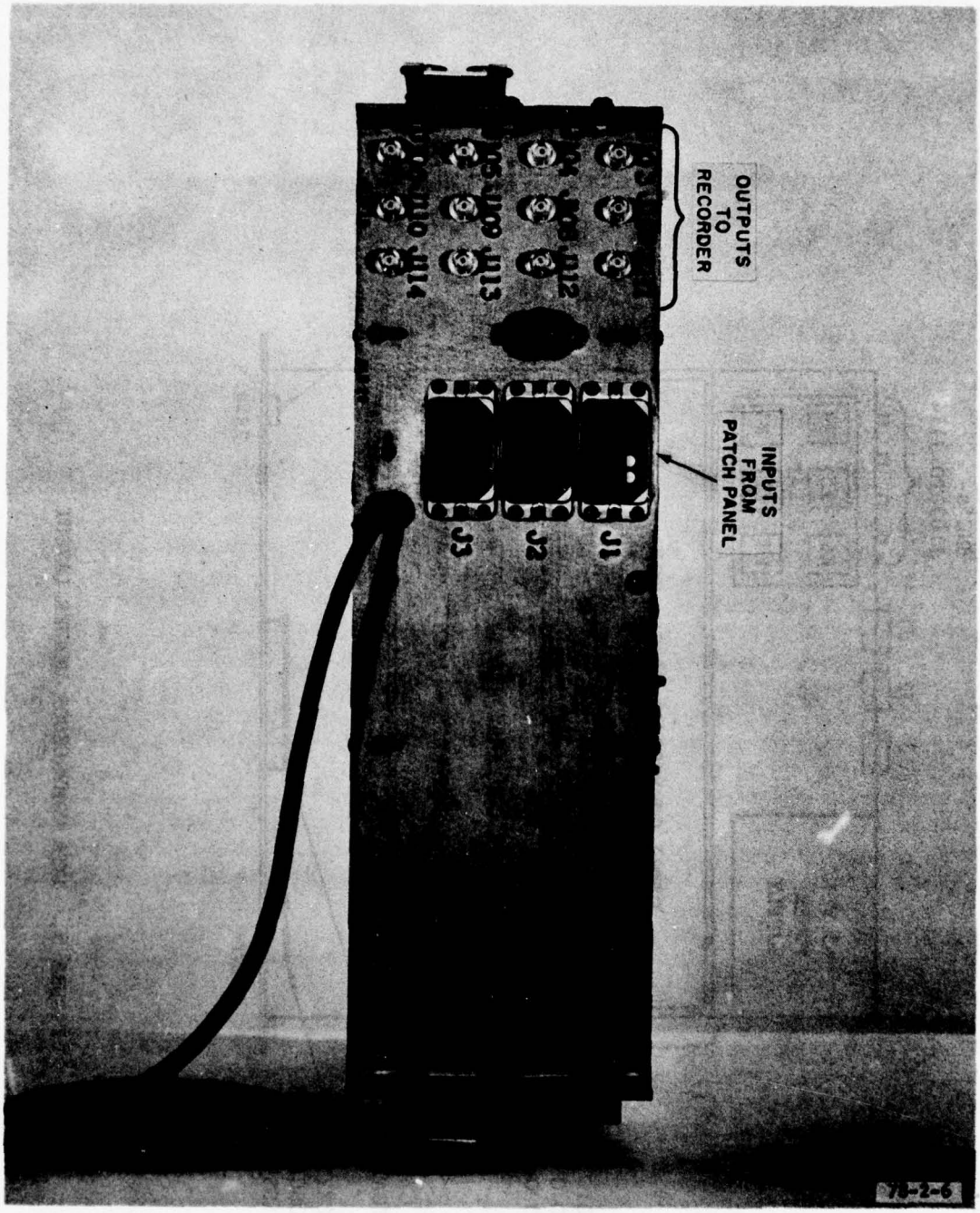


FIGURE 6. REAR VIEW OF DACOMP DRAWER

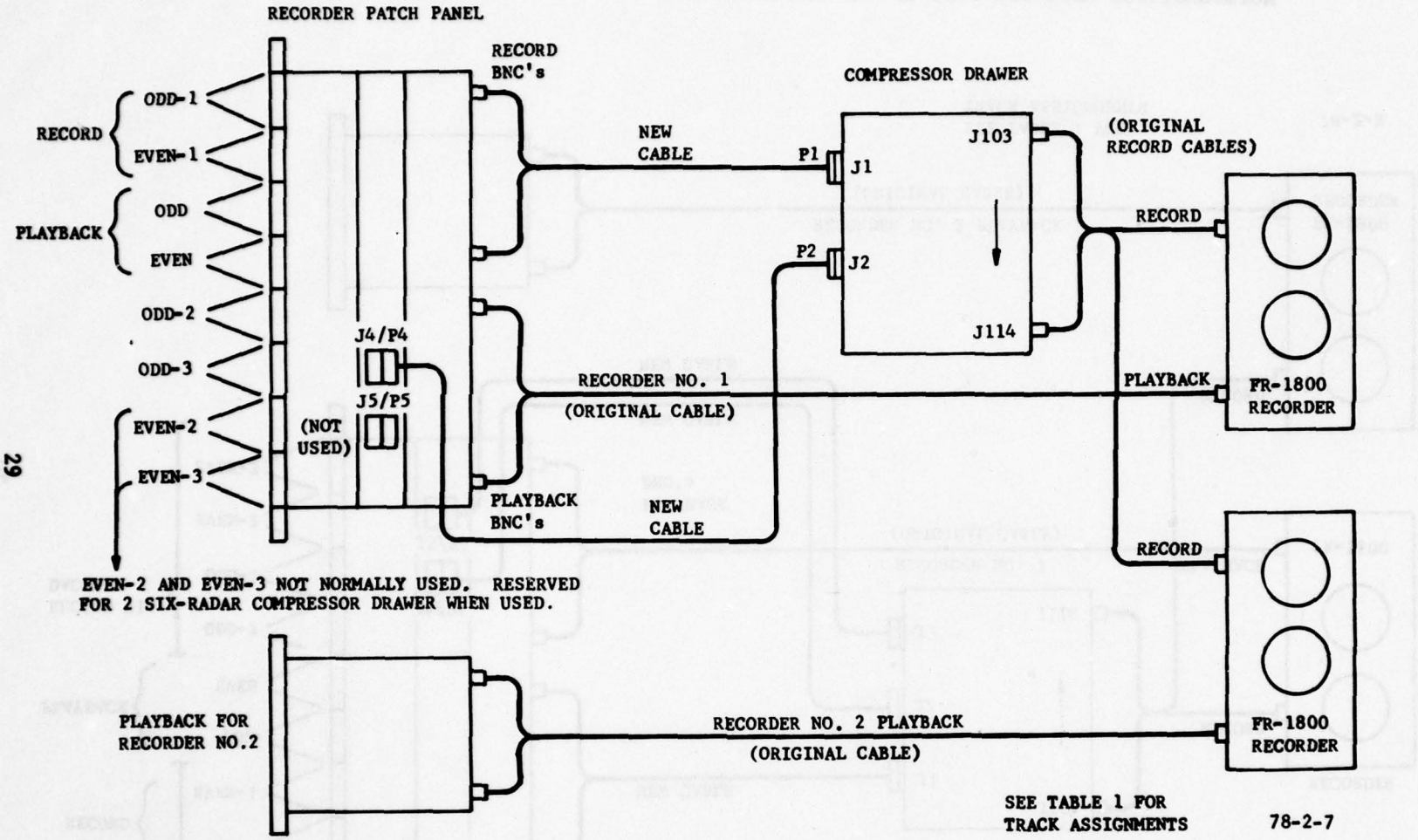


FIGURE 7. CABLING DIAGRAM FOUR FOUR-RADAR DACOMP DRAWER AND FR-1800 RECORDER CONFIGURATION

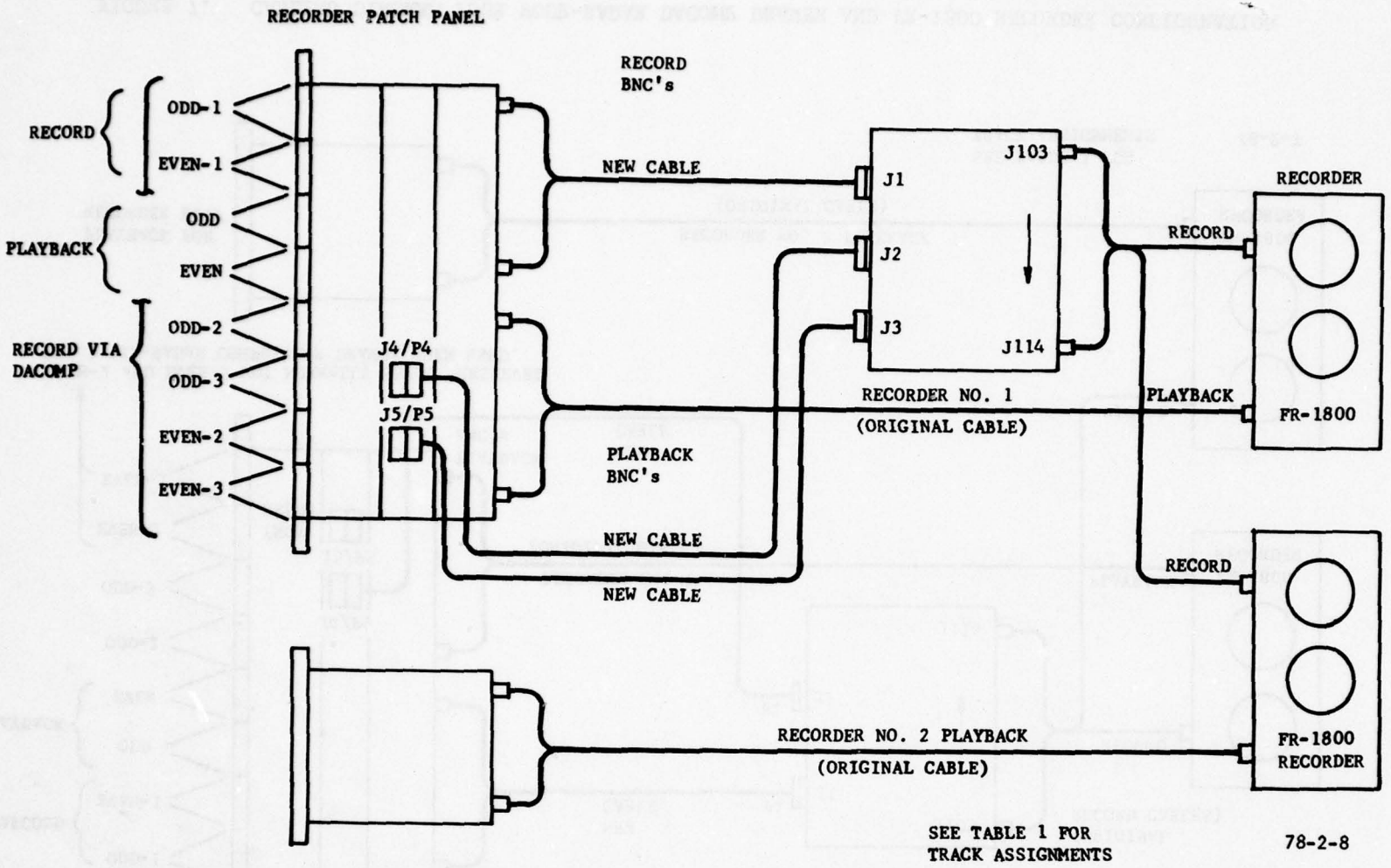


FIGURE 8. CABLING DIAGRAM FOR SIX-RADAR DACOMP DRAWER AND FR-1800 RECORDER CONFIGURATION

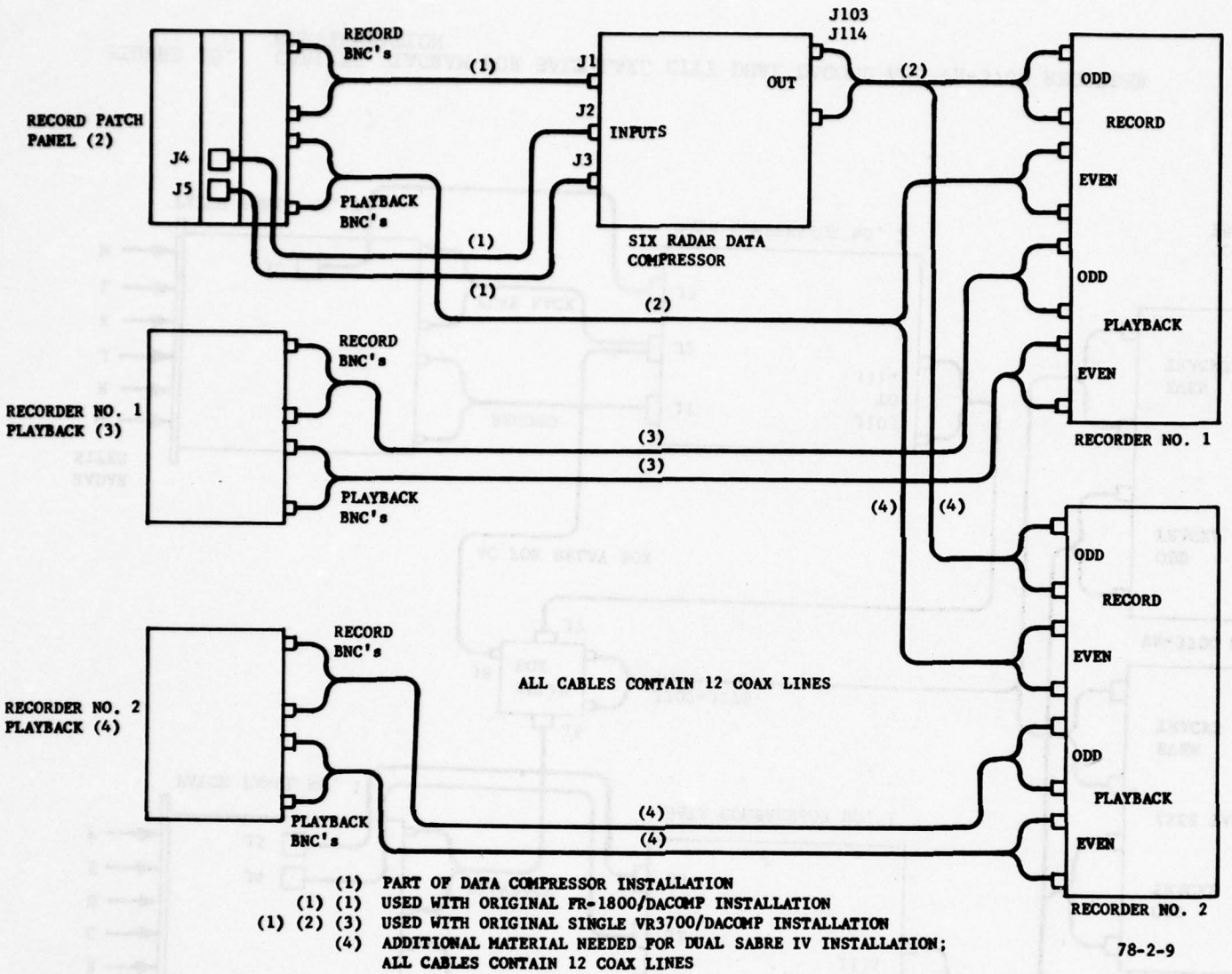


FIGURE 9. CABLING DIAGRAM FOR SIX-RADAR DACOMP DRAWER AND 28-TRACK RECORDER CONFIGURATION

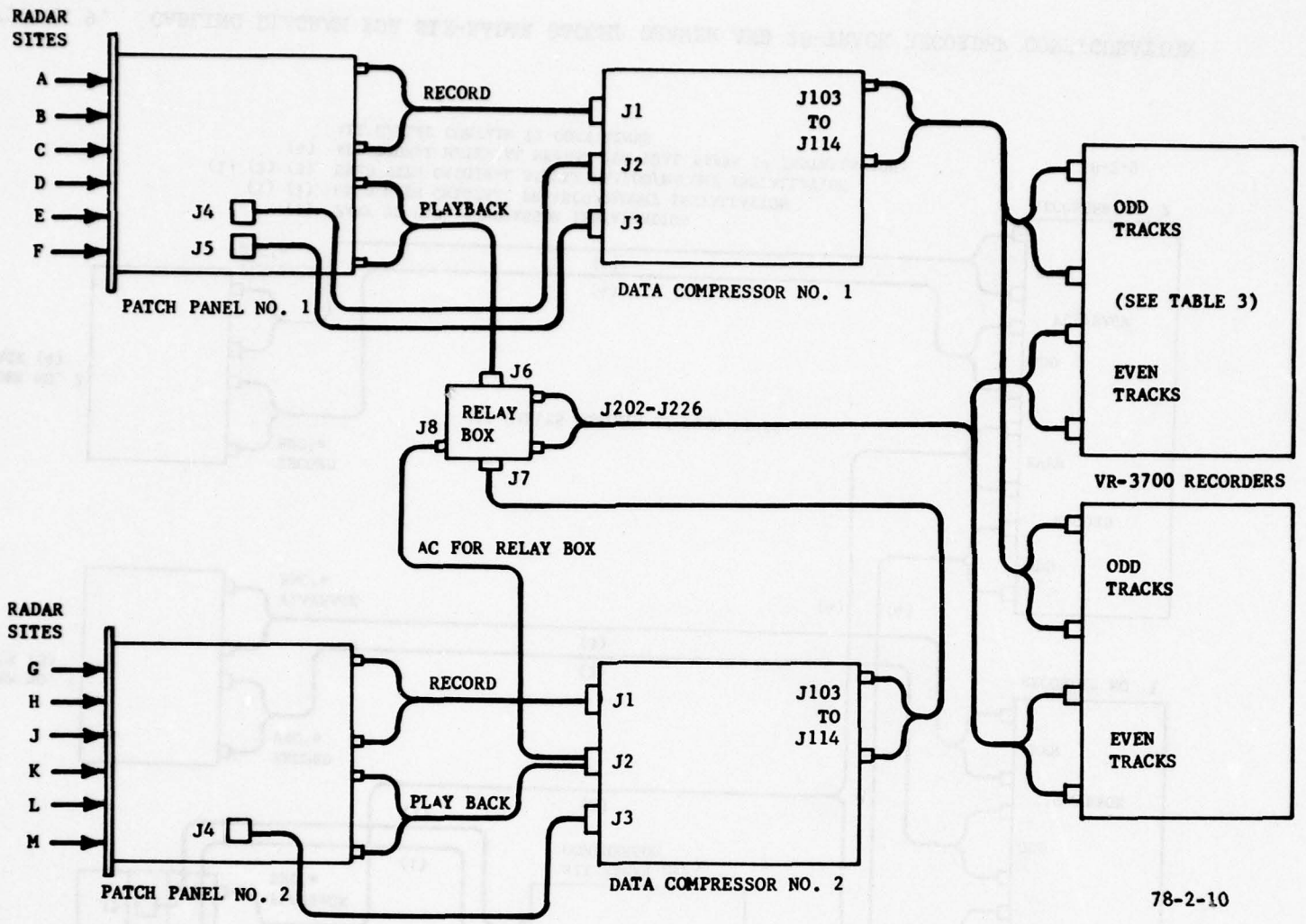


FIGURE 10. CABLING DIAGRAM FOR SALT LAKE CITY DUAL DACOMP AND VR-3700 RECORDER CONFIGURATION

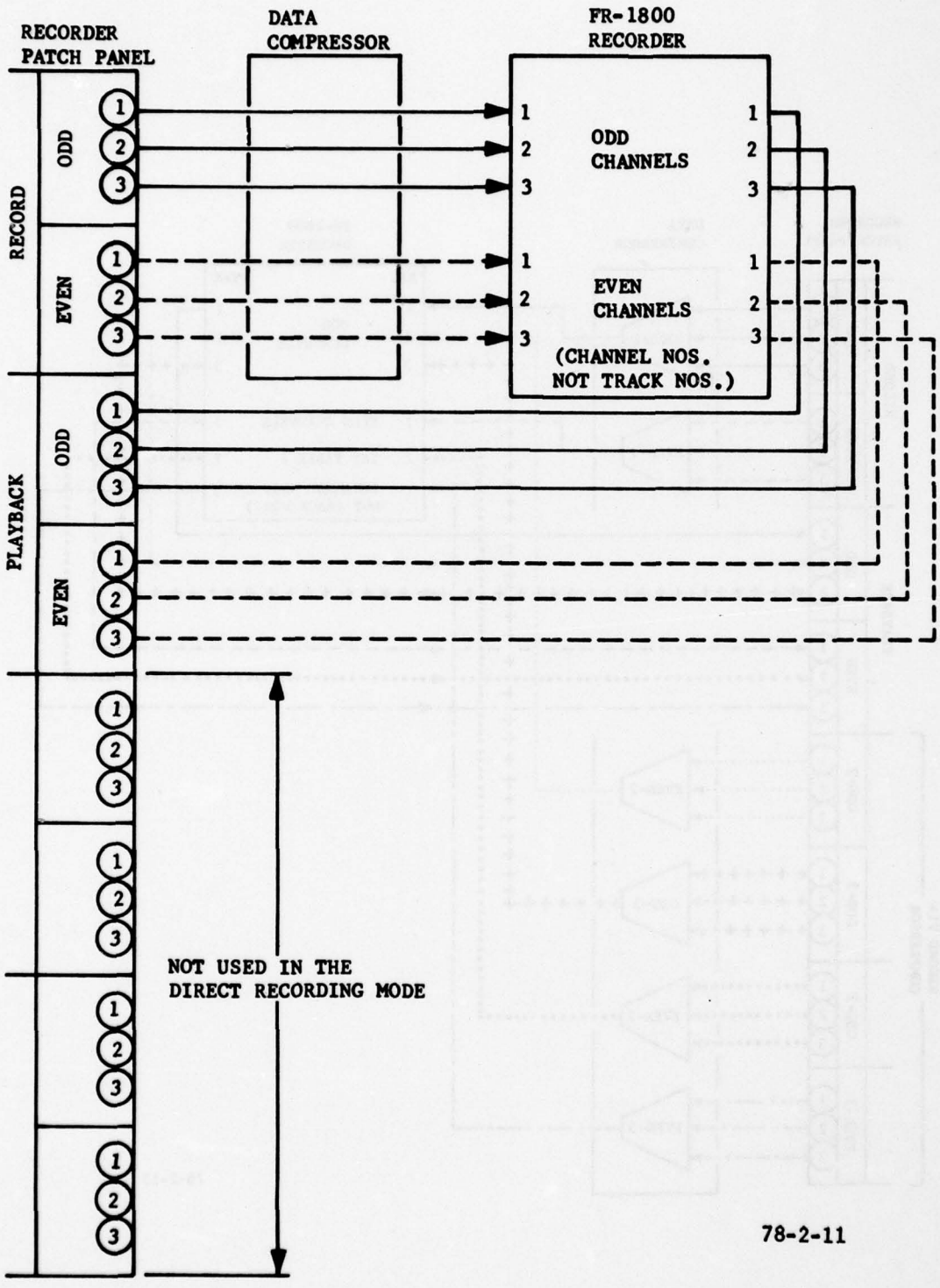


FIGURE 11. DACOMP/RF-1800 RECORDING AND PLAYBACK PATHS WITH DACOMP OFF

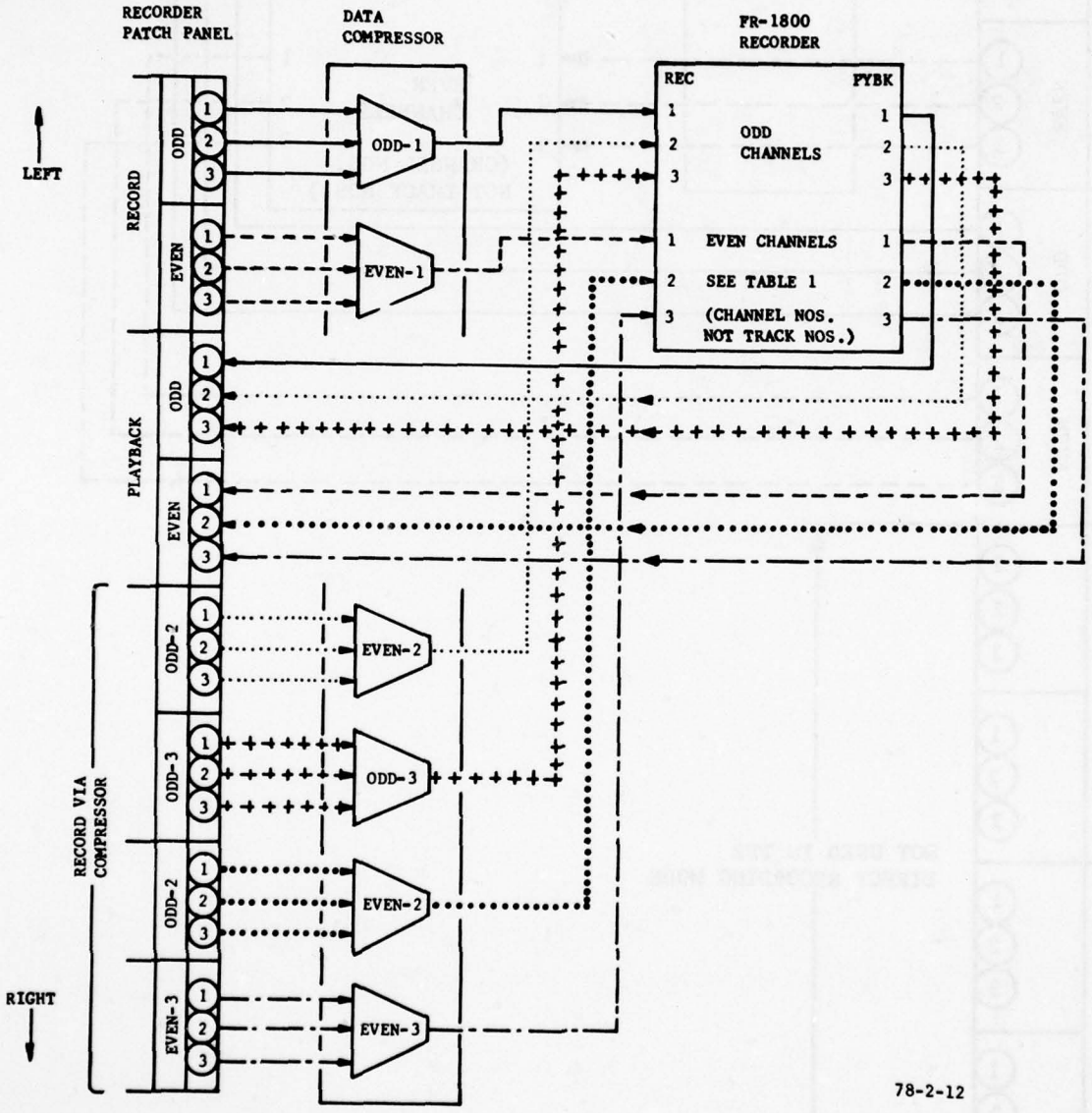


FIGURE 12. DACOMP/FR-1800 RECORDING AND PLAYBACK PATHS WITH DACOMP ENERGIZED

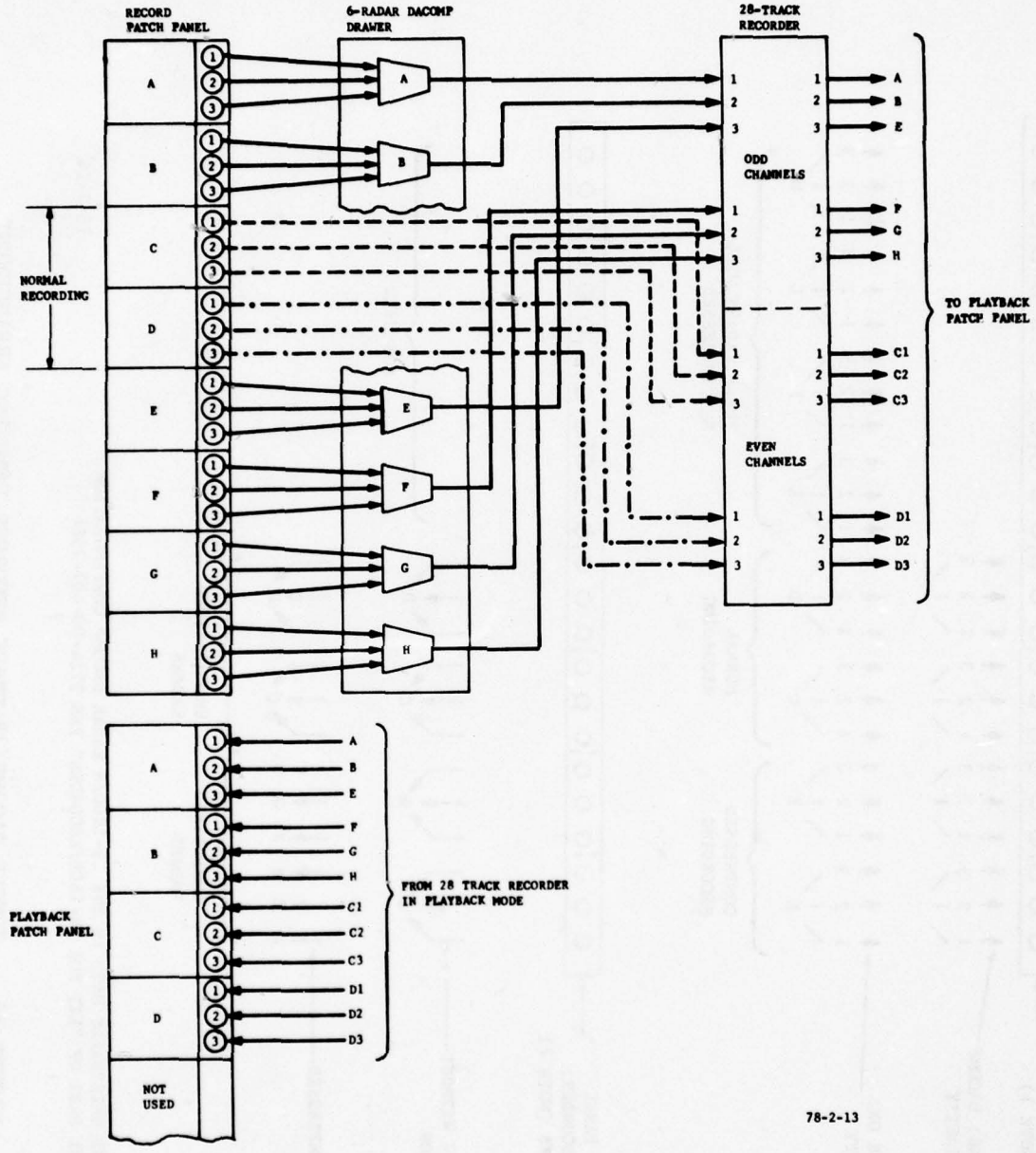
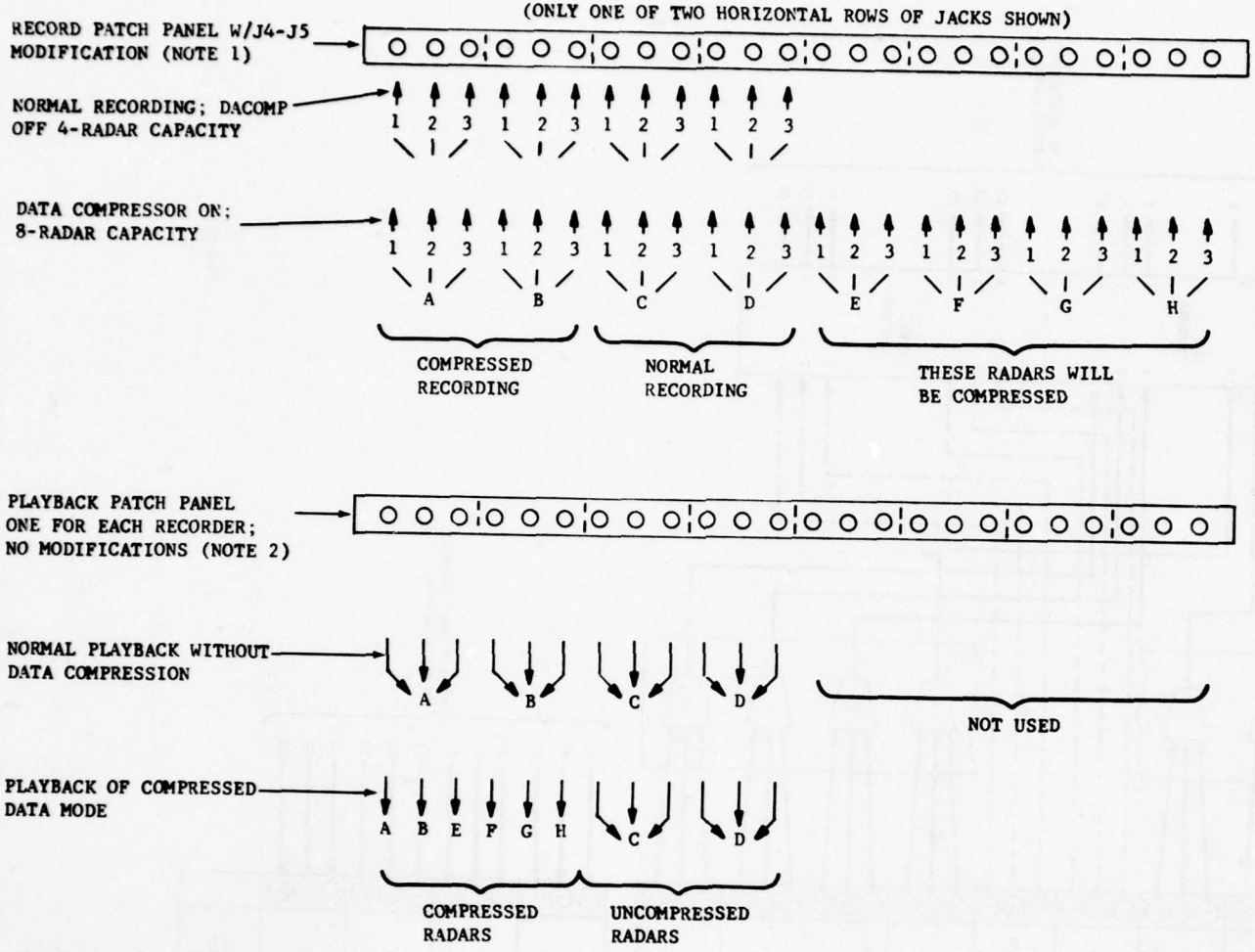


FIGURE 13. SINGLE DACOMP/28-TRACK RECORDER RECORDING AND PLAYBACK PATHS



NOTES:

1. THIS PANEL ORIGINALLY USED IN THE FR-1800/6 RADAR DACOMP CONFIGURATION
2. THIS PANEL PART OF "KIT FOR FR-1800/RECORDER" FSN 9224-00-407-7586

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FIGURE 14. SINGLE DACOMP/28-TRACK RECORDER PATCHING ARRANGEMENT

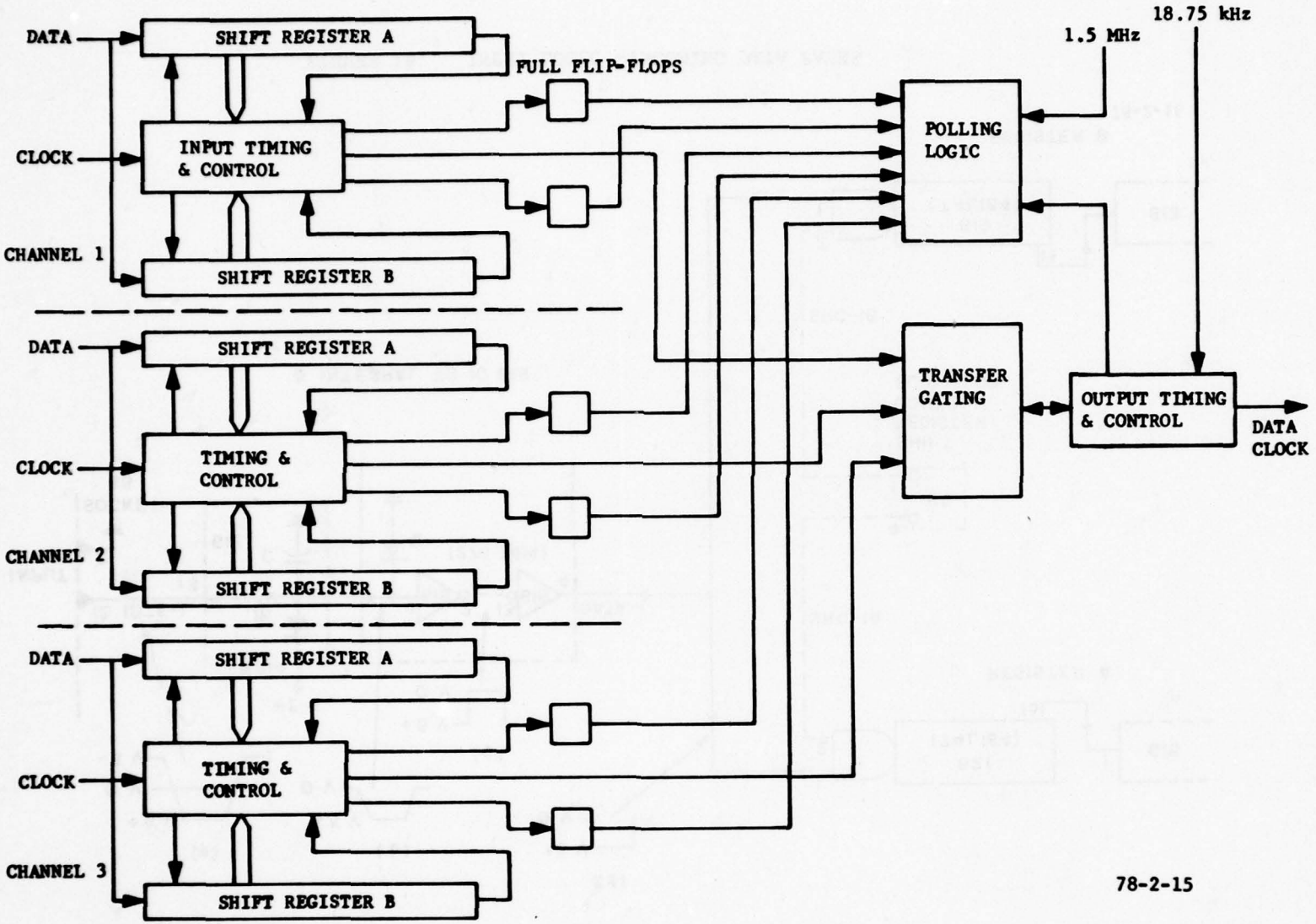


FIGURE 15. DATA COMPRESSOR BLOCK DIAGRAM

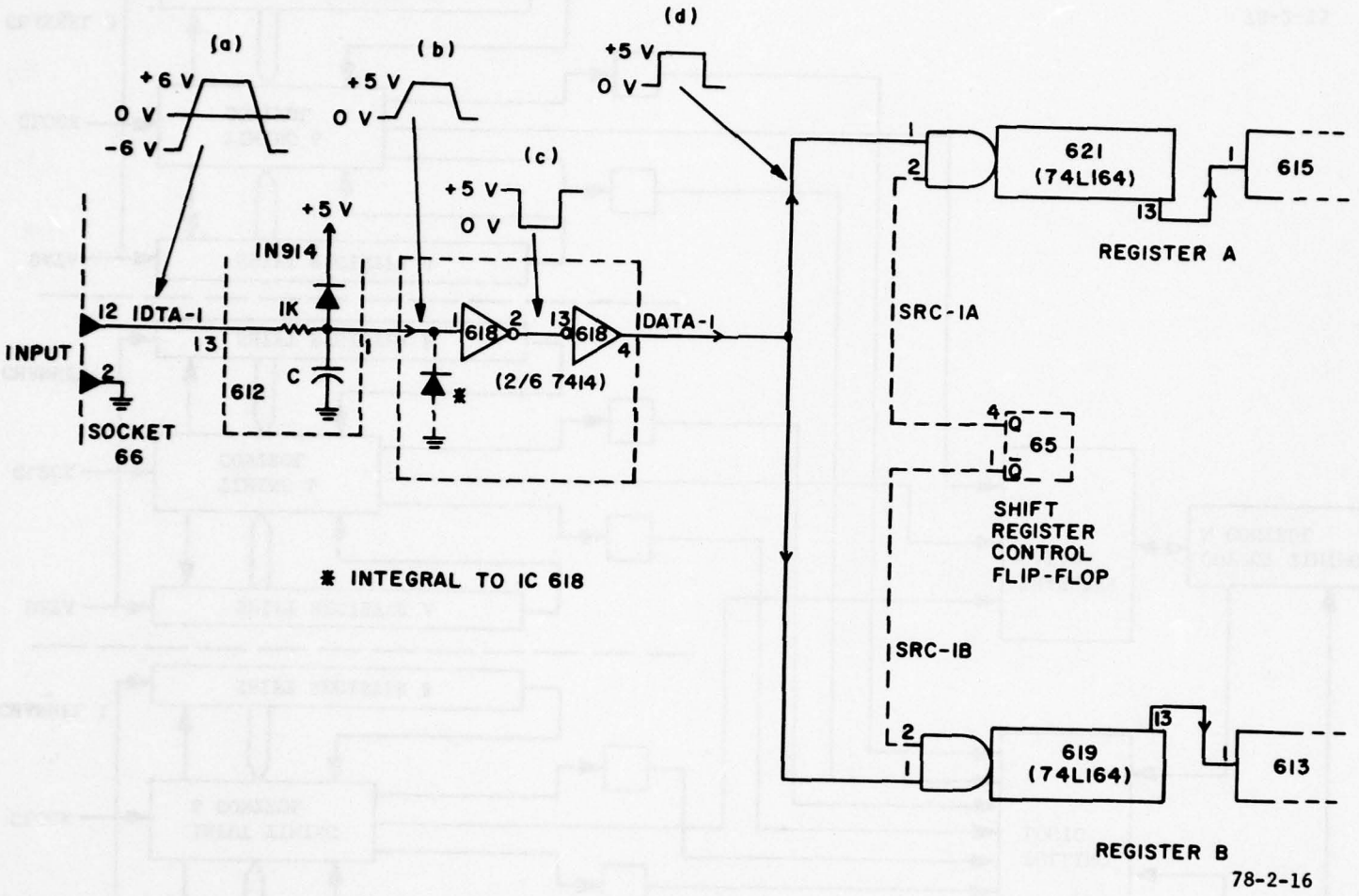


FIGURE 16. INPUT LOGIC--INCOMING DATA PATHS

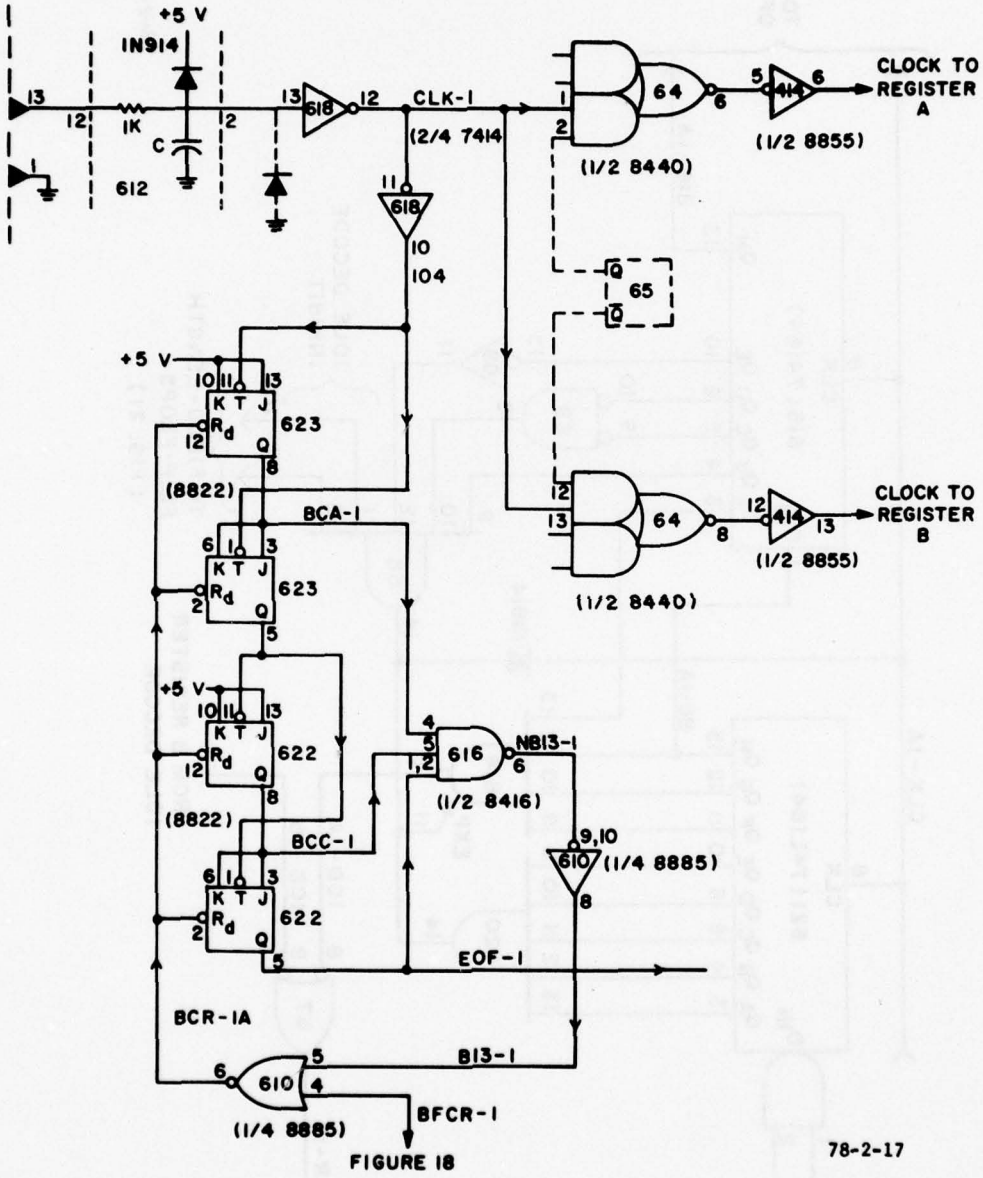


FIGURE 18

FIGURE 17. INPUT LOGIC--INCOMING CLOCK PATHS AND BIT COUNTER

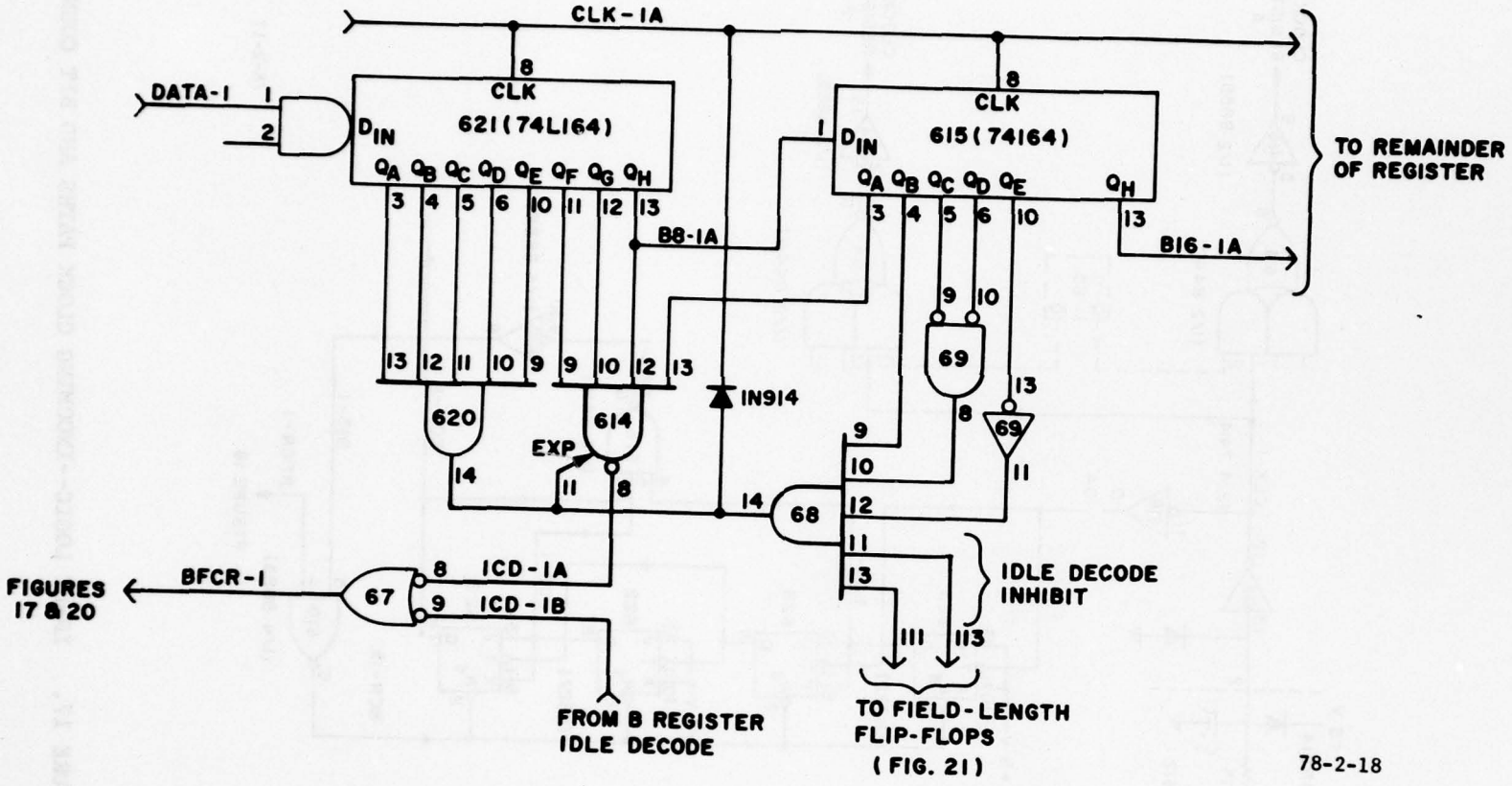


FIGURE 18. INPUT LOGIC--IDLE CHARACTER DECODE FOR REGISTER A

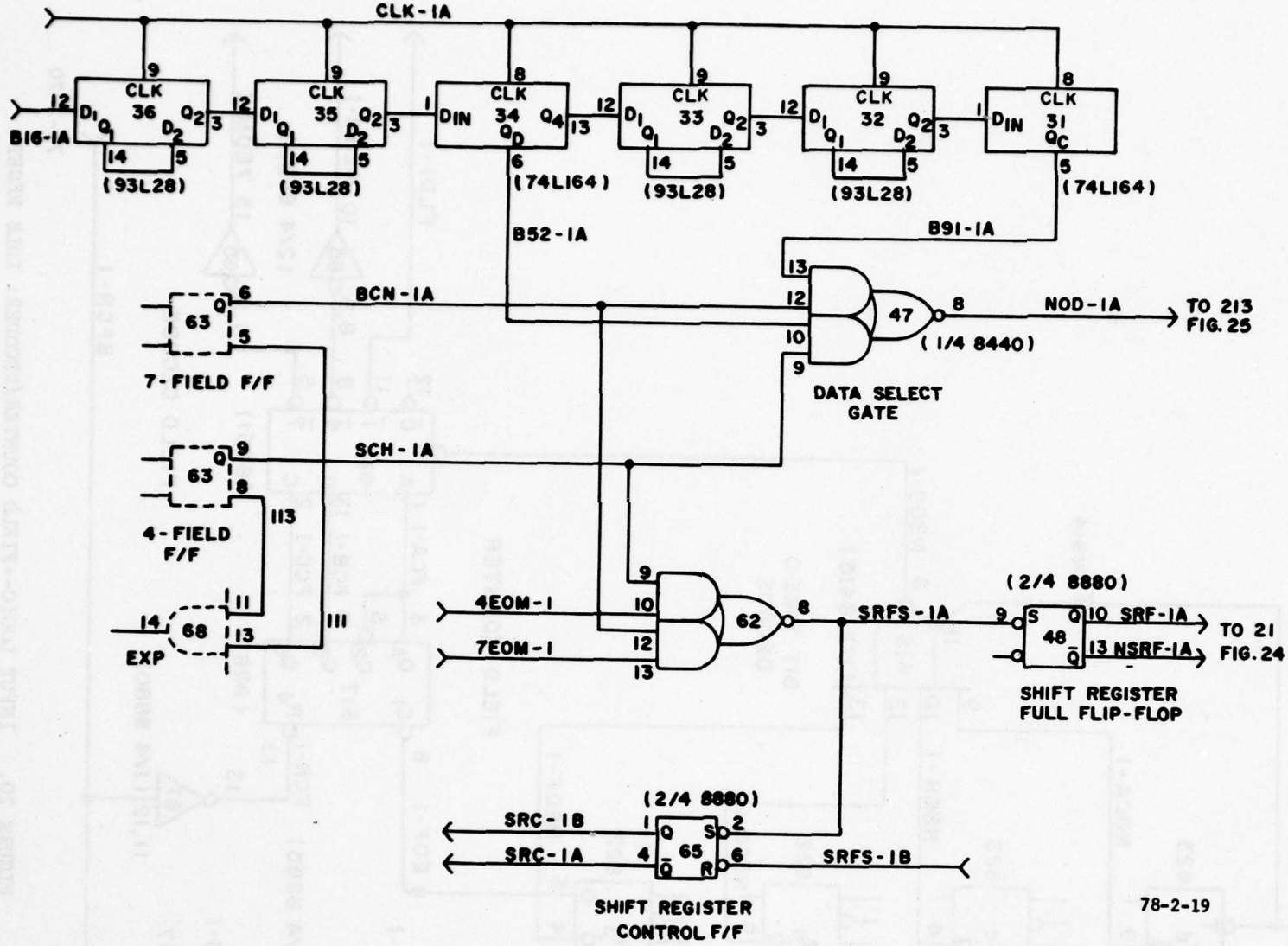


FIGURE 19. INPUT LOGIC--DATA SELECT AND REGISTER FULL LOGIC

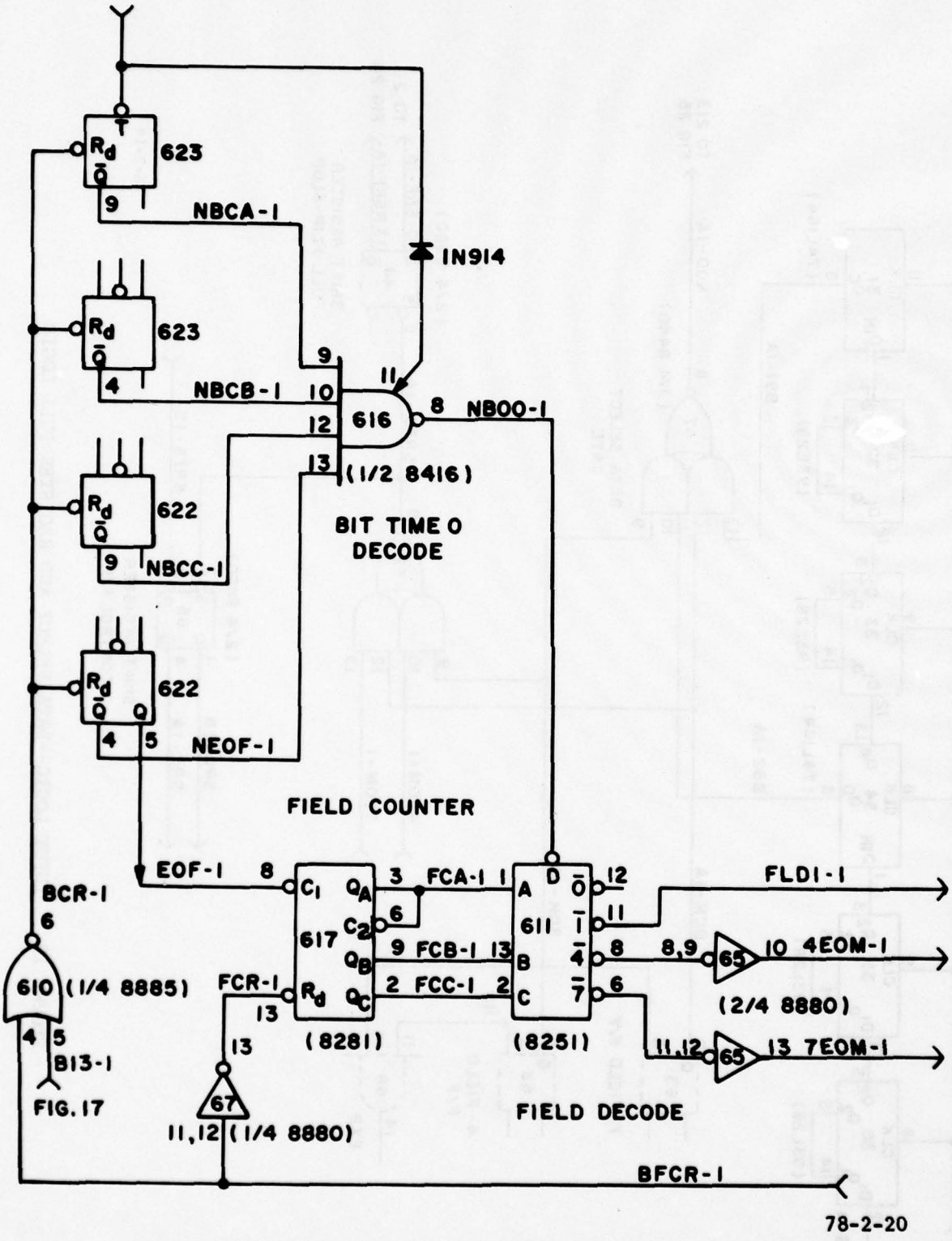


FIGURE 20. INPUT LOGIC--FIELD COUNTER/DECODER: IDLE RESET

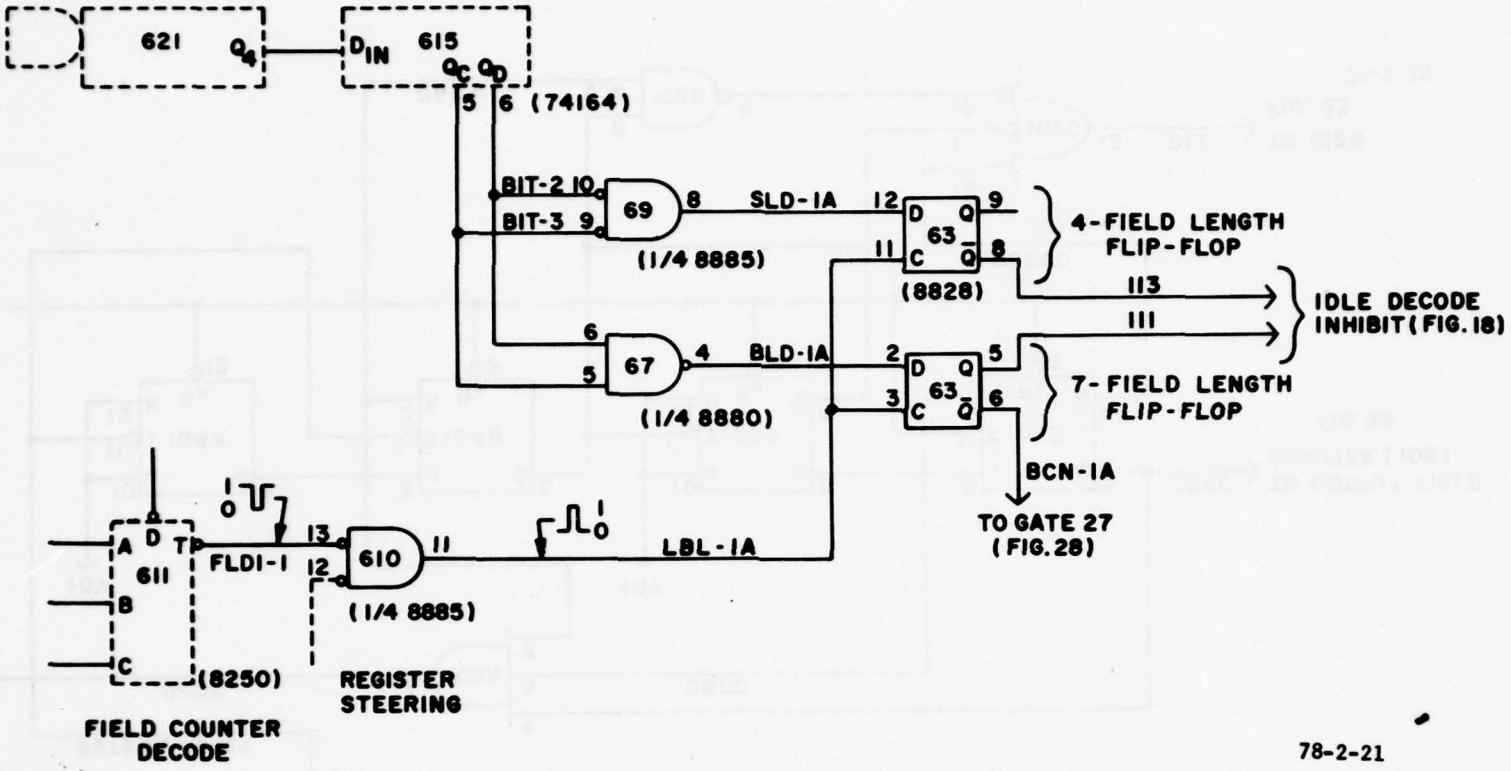


FIGURE 21. INPUT LOGIC--MESSAGE SIZE DECODE

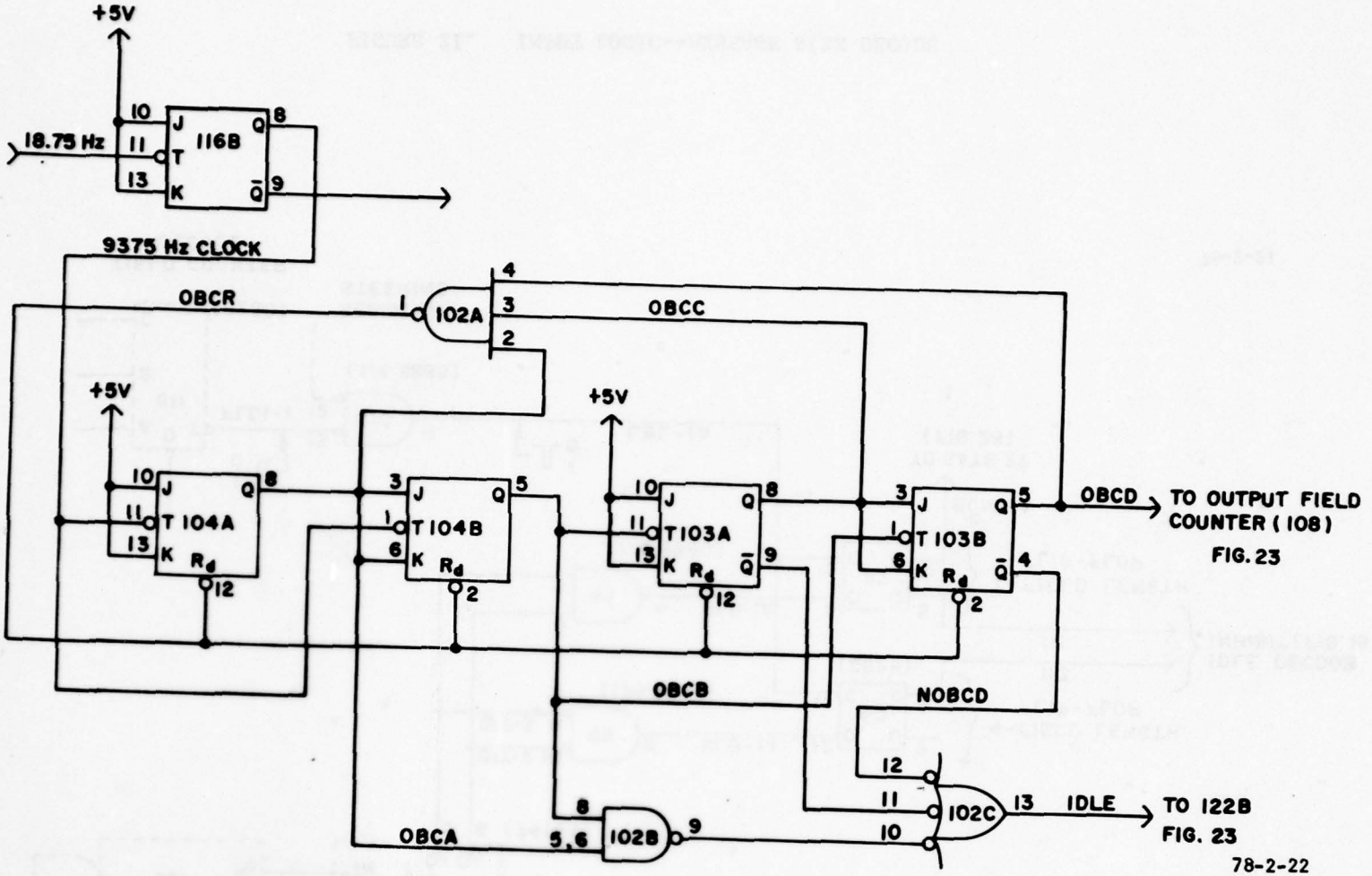


FIGURE 22. OUTPUT LOGIC--OUTPUT BIT COUNTER

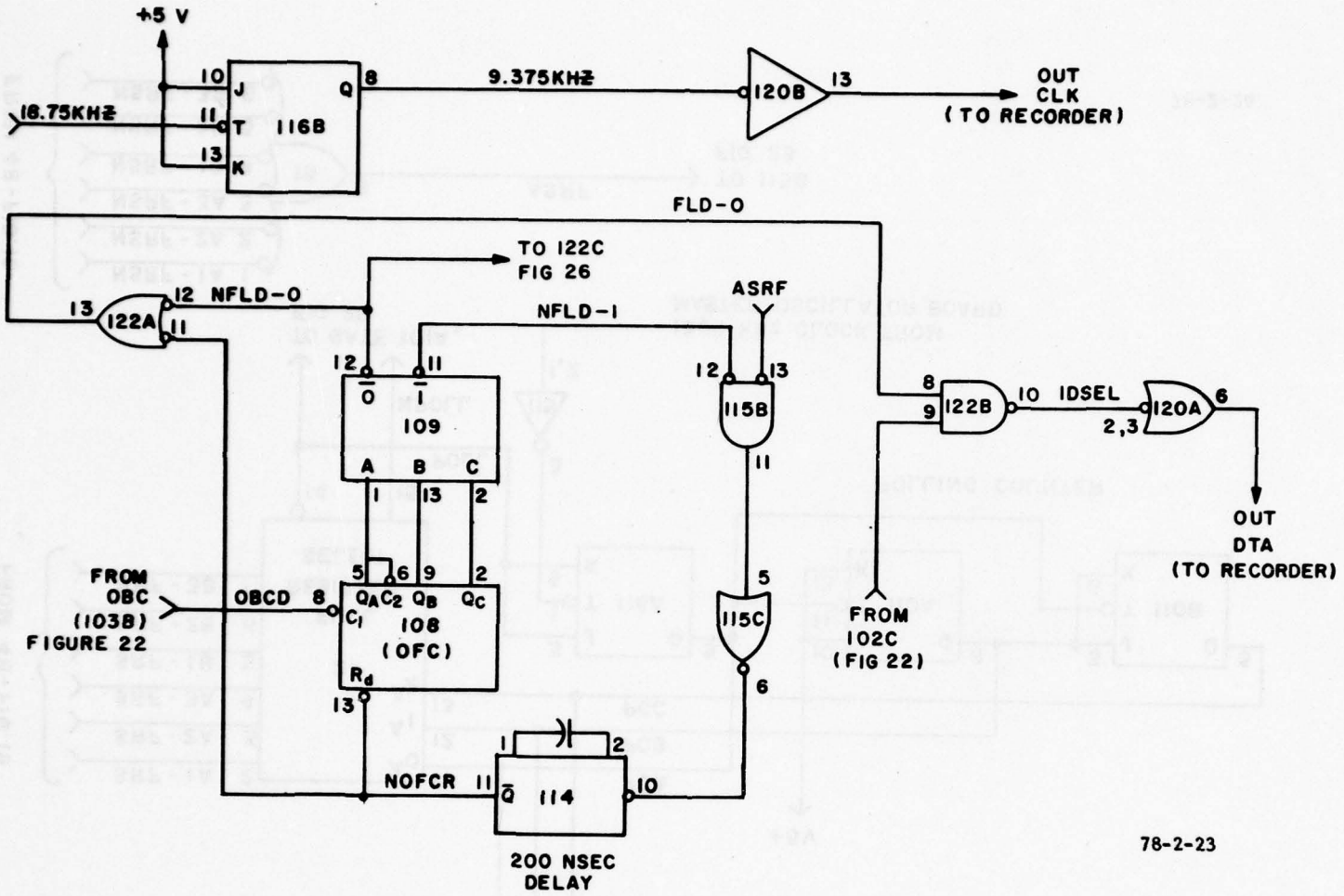


FIGURE 23. OUTPUT LOGIC--OUTPUT FIELD COUNTER

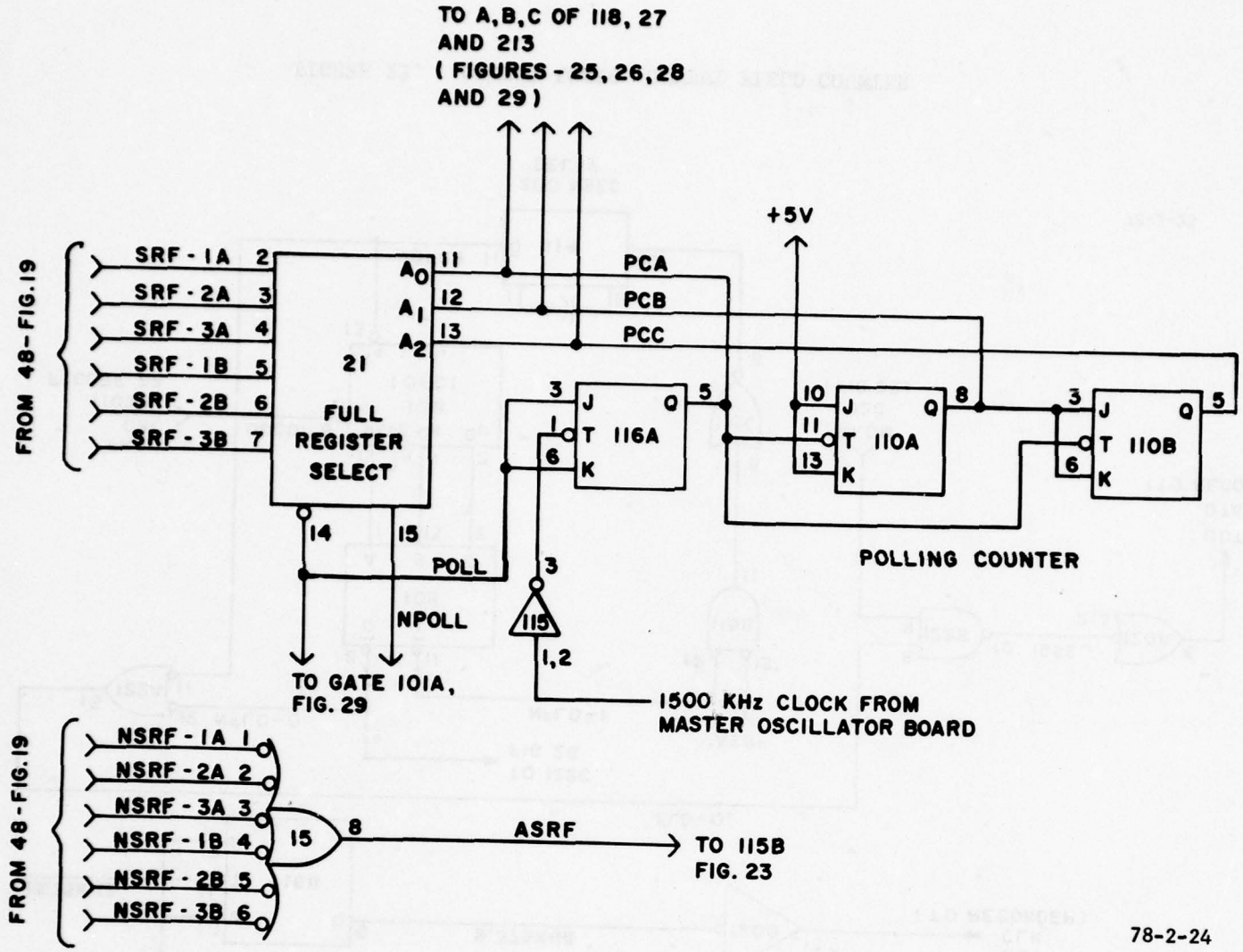


FIGURE 24. OUTPUT LOGIC--POLLING LOGIC

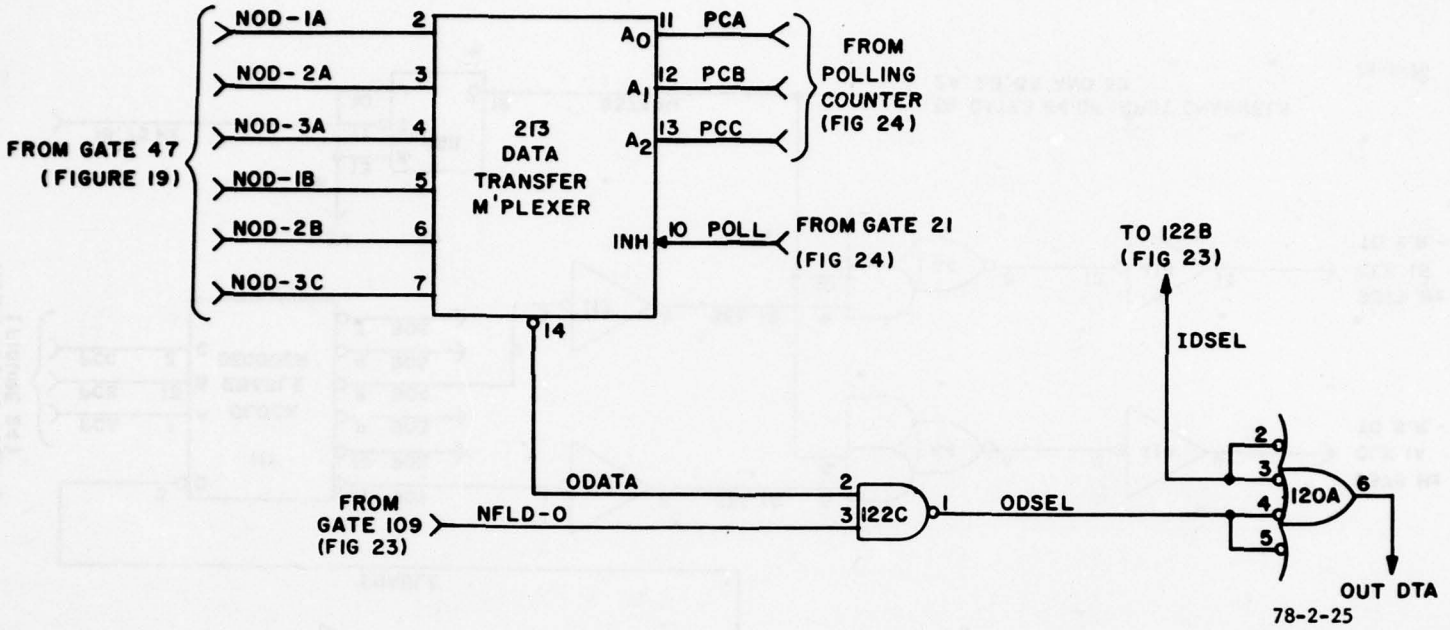


FIGURE 25. OUTPUT LOGIC--OUTPUT DATA PATHS

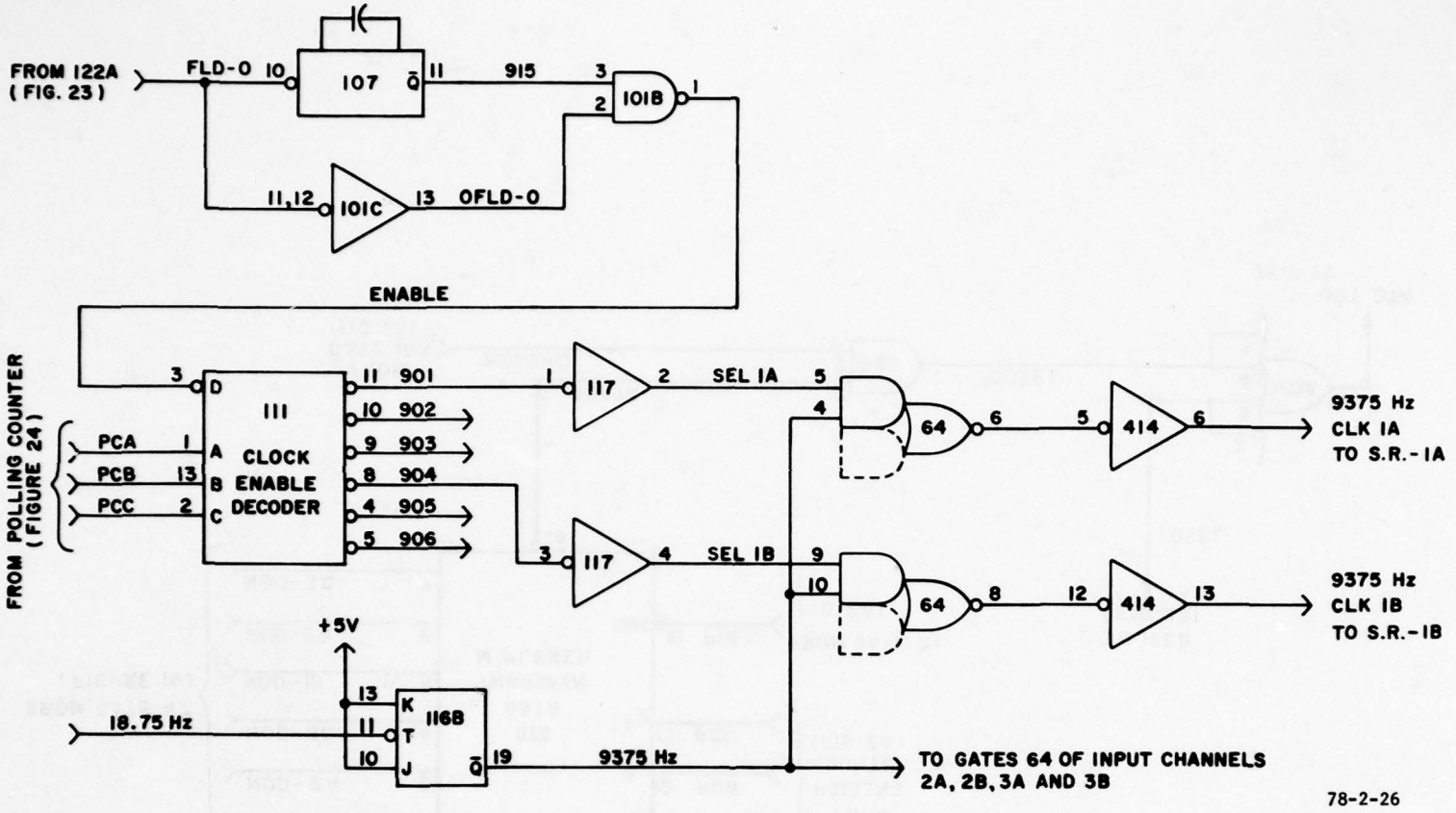


FIGURE 26. OUTPUT LOGIC--CLOCK-ENABLING LOGIC

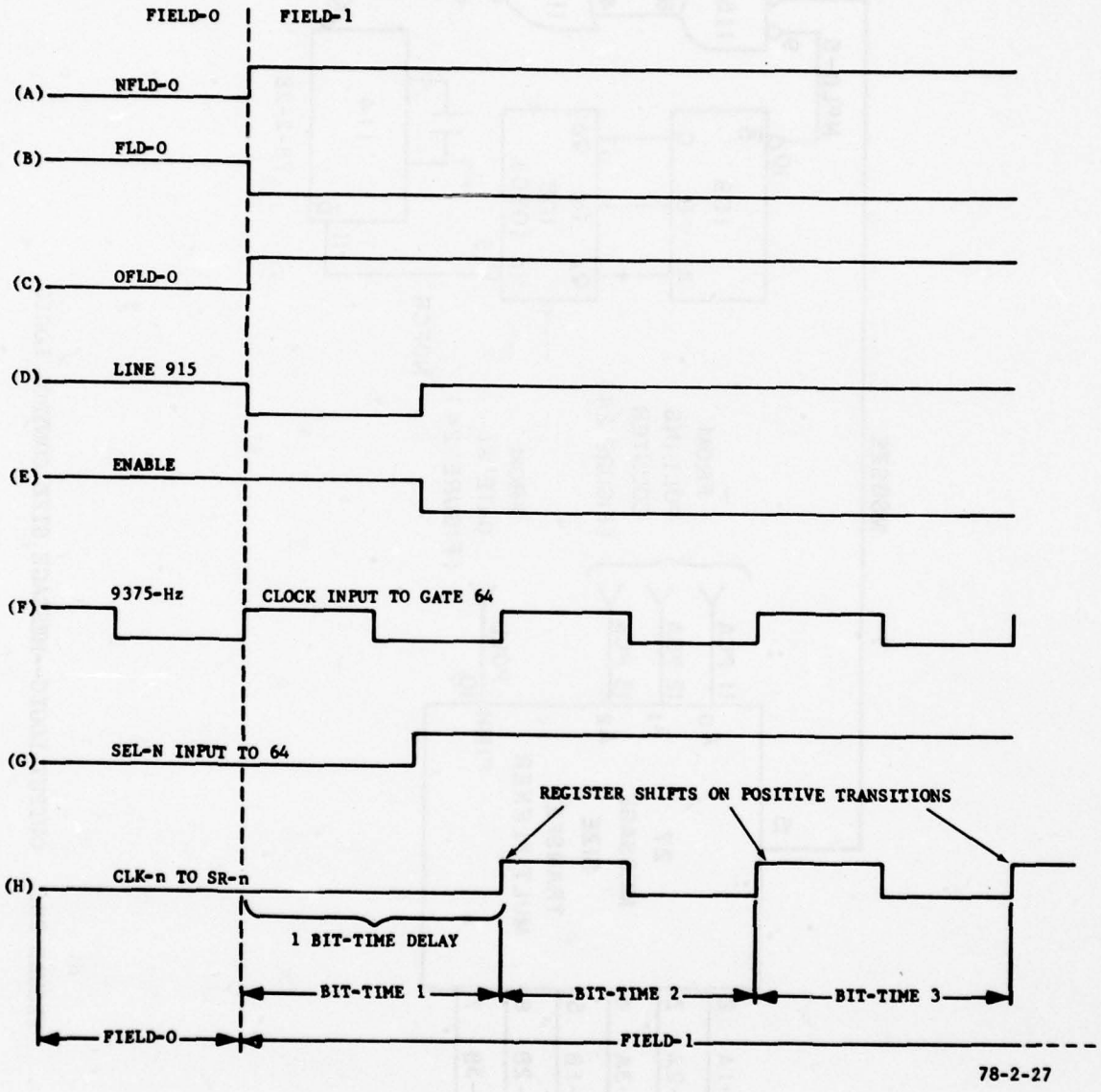
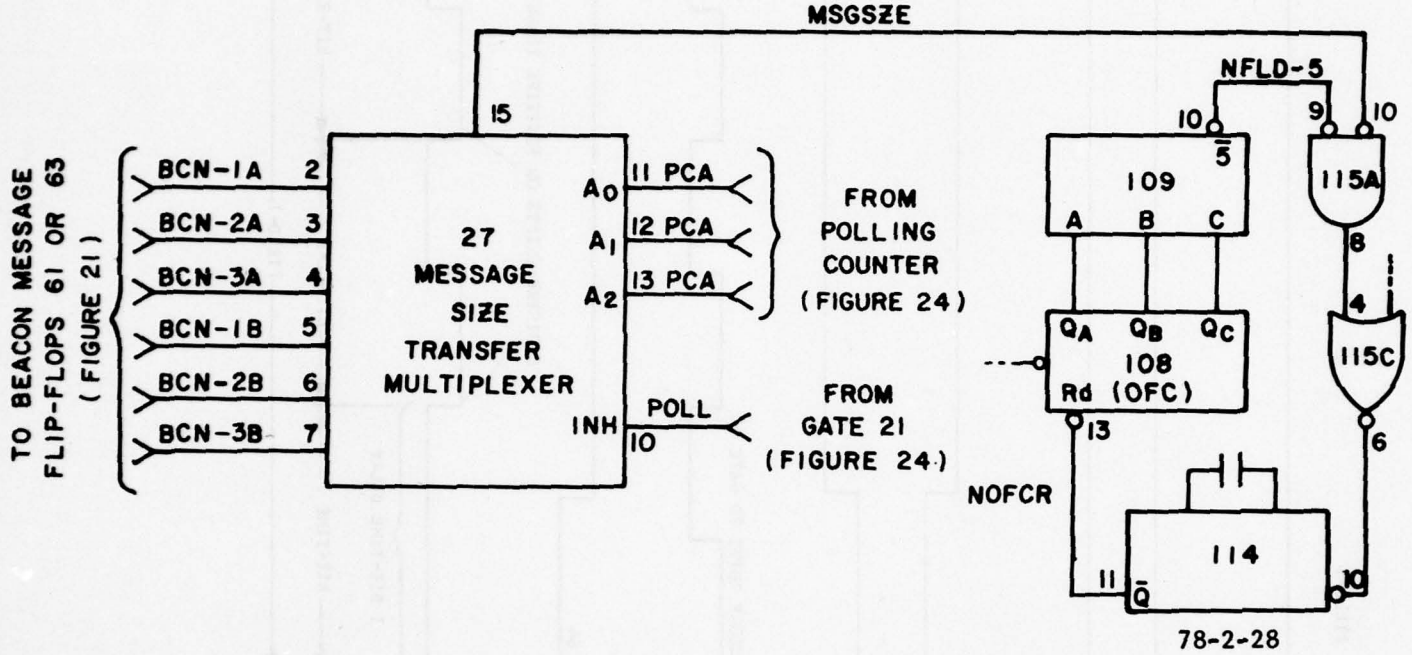


FIGURE 27. OUTPUT LOGIC--9375-Hz SHIFT REGISTER CLOCK TIMING DIAGRAM



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FIGURE 28. OUTPUT LOGIC--MESSAGE SIZE CONTROL LOGIC

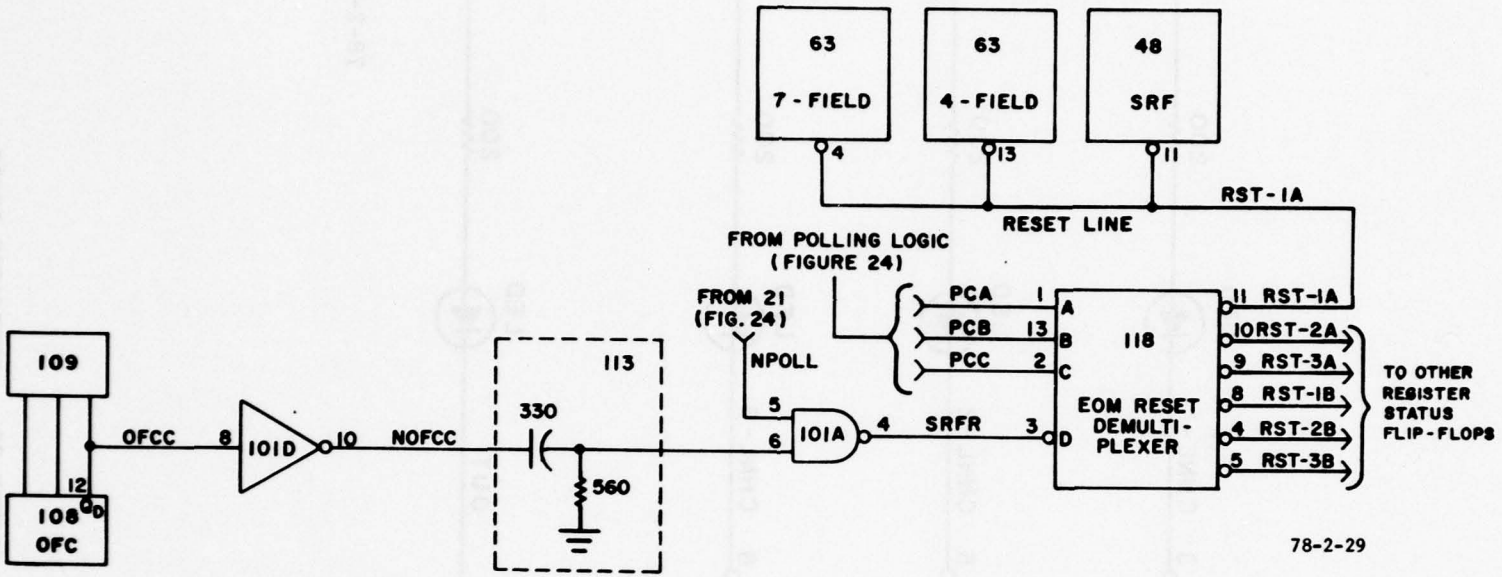


FIGURE 29. OUTPUT LOGIC--END-OF-MESSAGE (EOM) RESET LOGIC

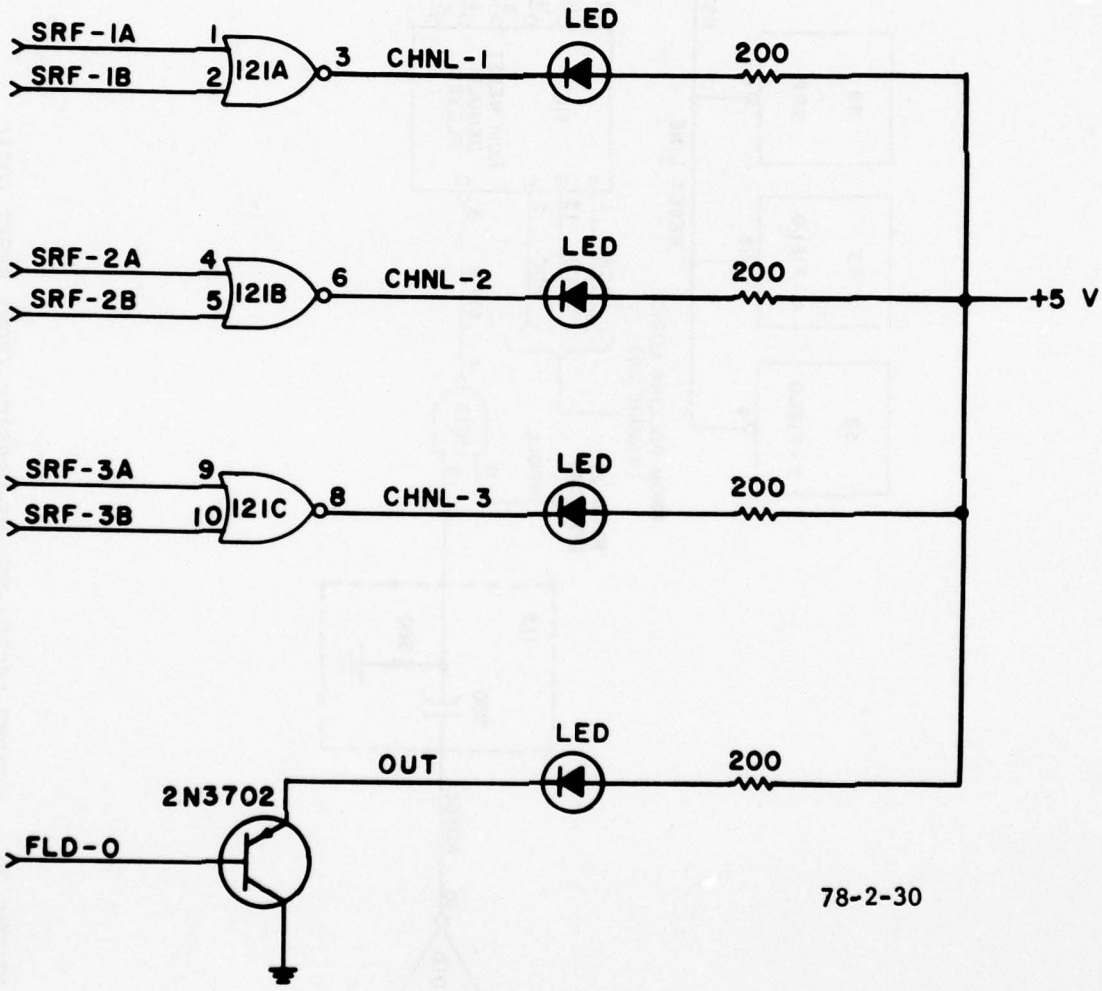


FIGURE 30. INDICATOR LOGIC

APPENDIX A

Logic Diagrams

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A-6	FR-1800 Data Compressor--Internal Clock, Indicator and Power Paths--4 Logic Frames per Drawer--Drawing XD2588	A-6
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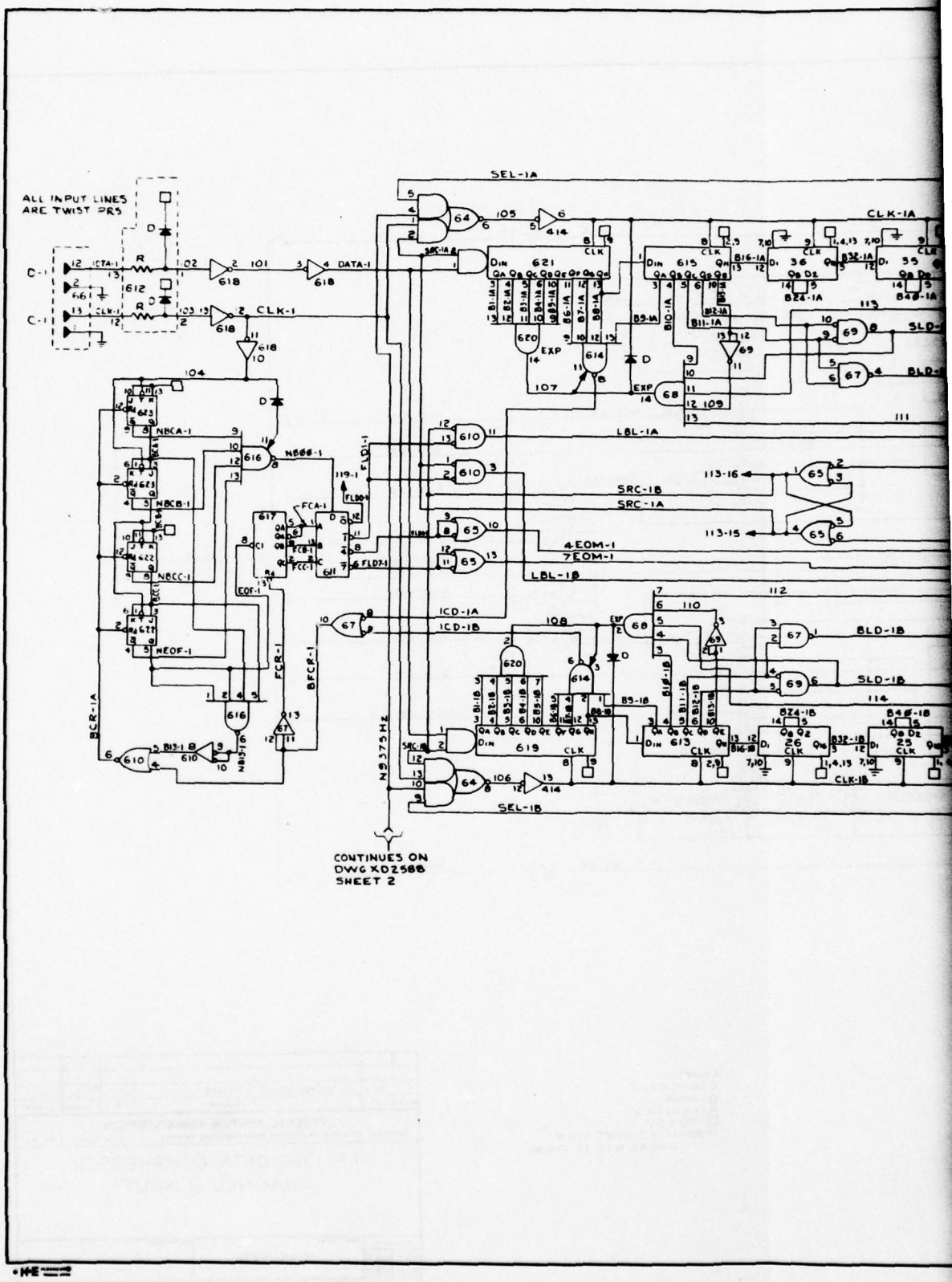
LIST OF ILLUSTRATIONS (Continued)

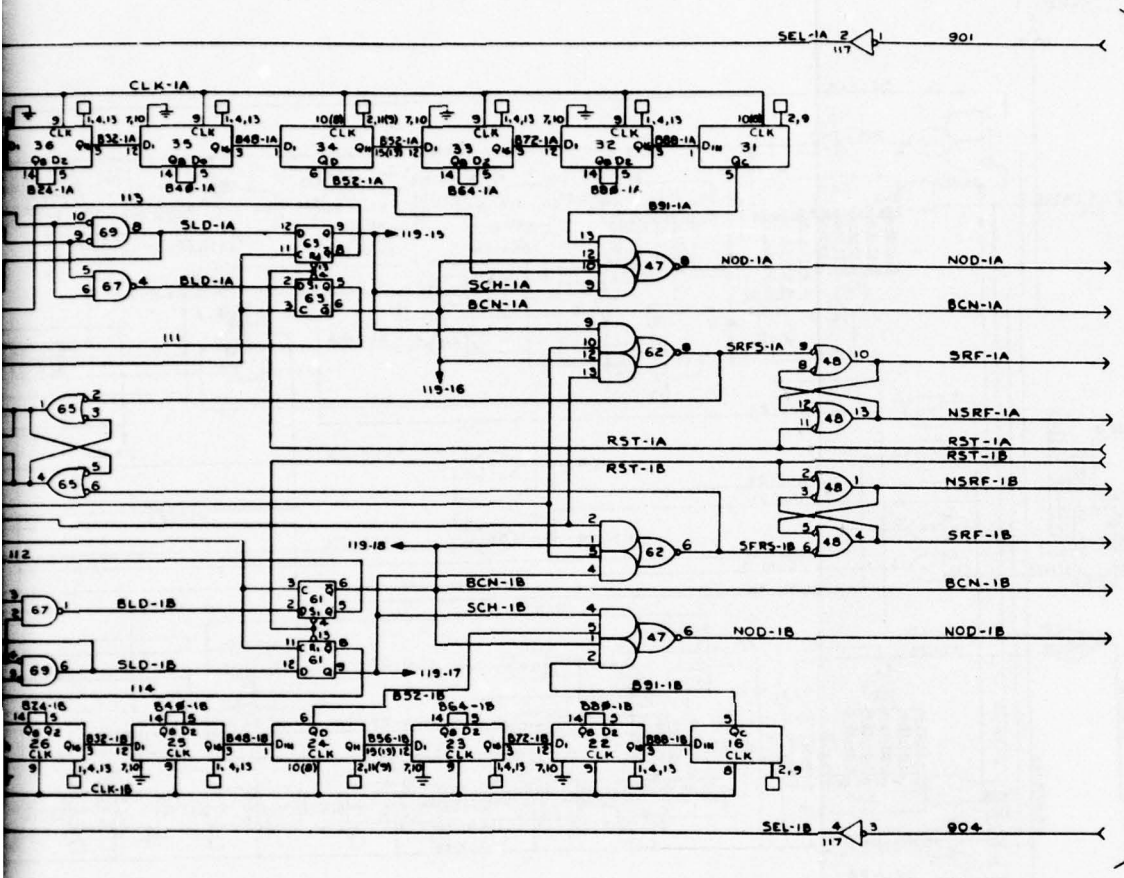
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PRECEDING PAGE BLANK-NOT FILMED


ALL INPUT LINES ARE TWIST PRS
C-1
C-1
CTA-1
CLK-1
612
661
R
R
D
D
102
101
103
618
DATA-1
CLK-1
SEL-1A
64
105
414
621
SRC-1A
CLK
DIN
615
616-1A
624-1A
632-1A
640-1A
36
35
B10-1A
B11-1A
620
EXP
614
107
68
109
69
67
SLD-
BLD-
111
LBL-1A
610
113-16
113-15
65
SRC-1B
SRC-1A
4EOM-1
7EOM-1
LBL-1B
112
110
ICD-1A
ICD-1B
108
BLD-1B
SLD-1B
114
619
613
106
SEL-1B
N9.375 MHz
104
623
NBCA-1
NBCB-1
NBCC-1
NEOF-1
622
616
617
FCA-1
FCB-1
FCC-1
EOF-1
FCR-1
BFCR-1
BCR-1A
119-1
FLD0-1
FLD7-1
NBBB-1
CONTINUES ON DWG XD2588 SHEET 2



LEGEND
C = 0.0047 μf
D = IN914
R = 1K Ω, 1/4W
□ = TO + 5V
M(N) = M IS SOCKET PIN #
WHERE N IS IC PIN #

REV LTR	DATE	DESCRIPTION	ENGRG	APPROVED
A	7/30/74	SHT. NO. CHG. FROM 6 TO 9 SHTS.	EM/GH	8/29/74

FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER — ATLANTIC CITY, N.J.

FR-1800 DATA COMPRESSOR
CHANNEL 1 INPUT

REVIEWED BY	SUBMITTED BY	APPROVED BY
KSB 8-26-74 RLH 8-28-74	ANA-522	

DRAWN BY	ISSUED BY	DATE
R.A. MACK	ANA-140	10-12-73

CHECKED BY

DRAWING NO. XD2588
SHEET 1 OF 9.

78-2-A-1

FIGURE A-1. FR-1800 DATA COMPRESSOR--CHANNEL 1 INPUT--DRAWING XD2588

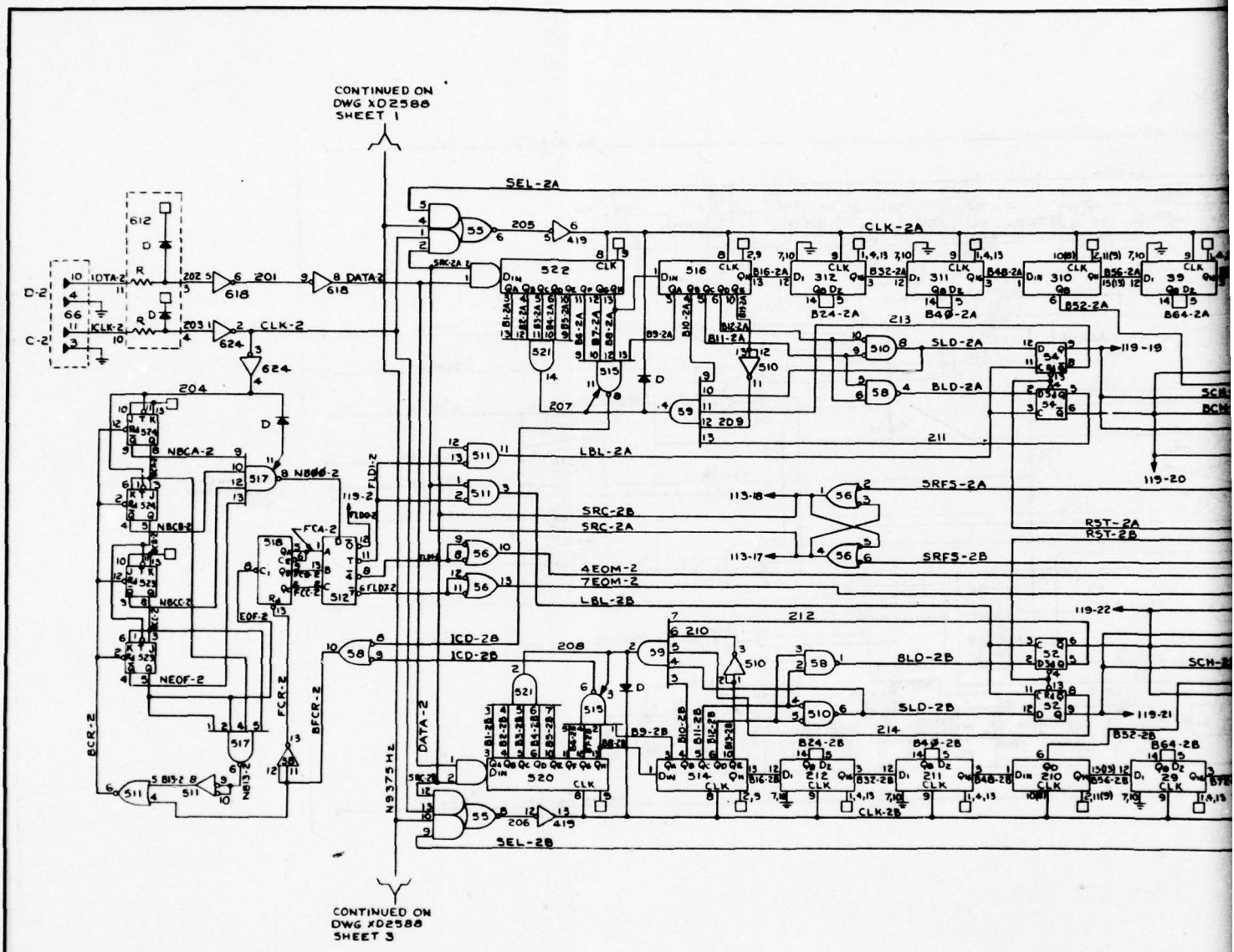
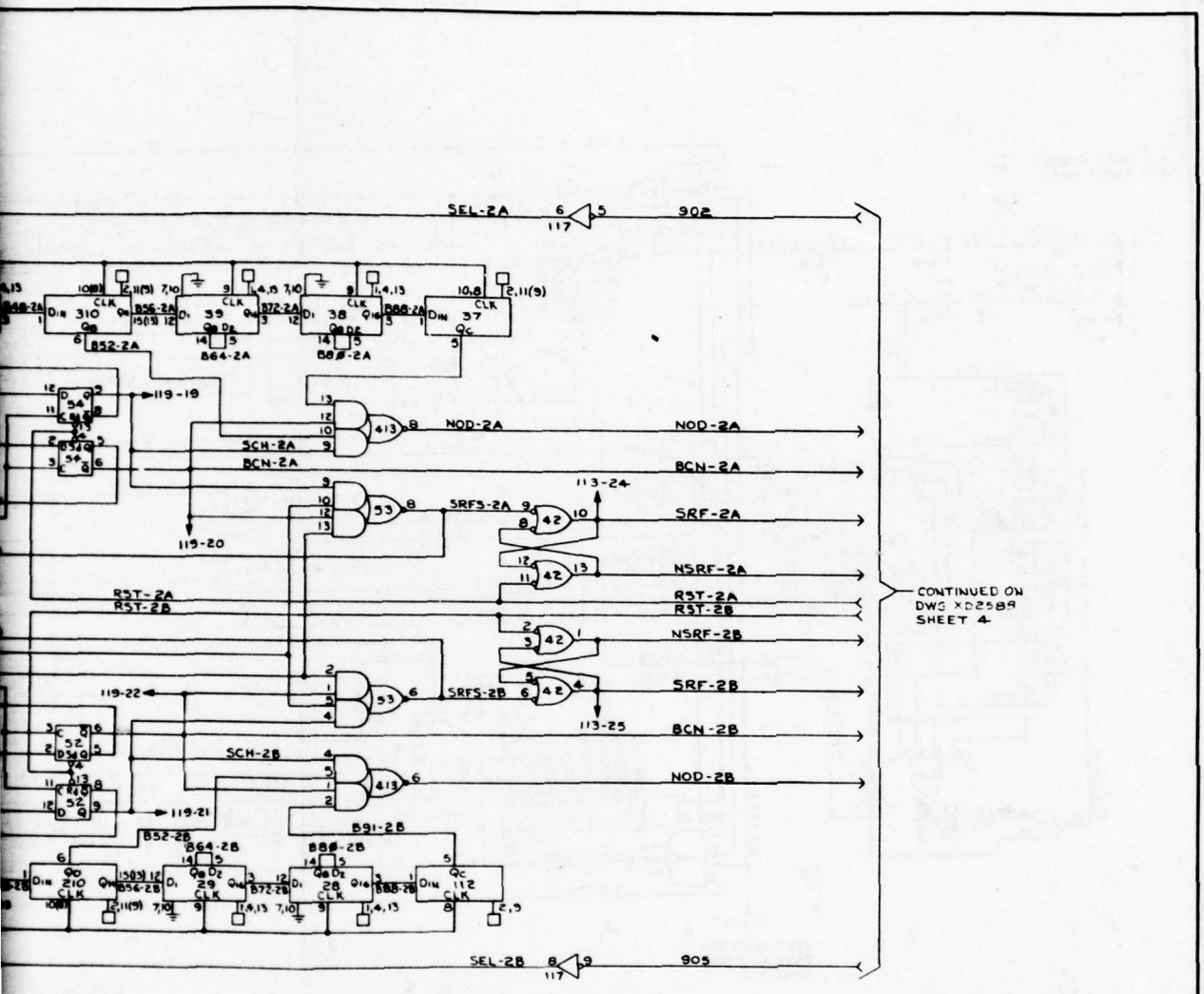


FIGURE A-2. FR-1800 DATA



LEGEND
C=0.0047μf
D=1N914
R=1KΩ, ¼W
□: TO +5V
M(N)=M IS SOCKET PIN #
WHERE N IS IC PIN #

REVISIONS	DATE	DESCRIPTION	CHECKED	APPROVED
A	7/15/75	SHT. NO. CHG. FROM 6 TO 9 SHTS.	ES/GH	8/29/74

FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER — ATLANTIC CITY, N.J.

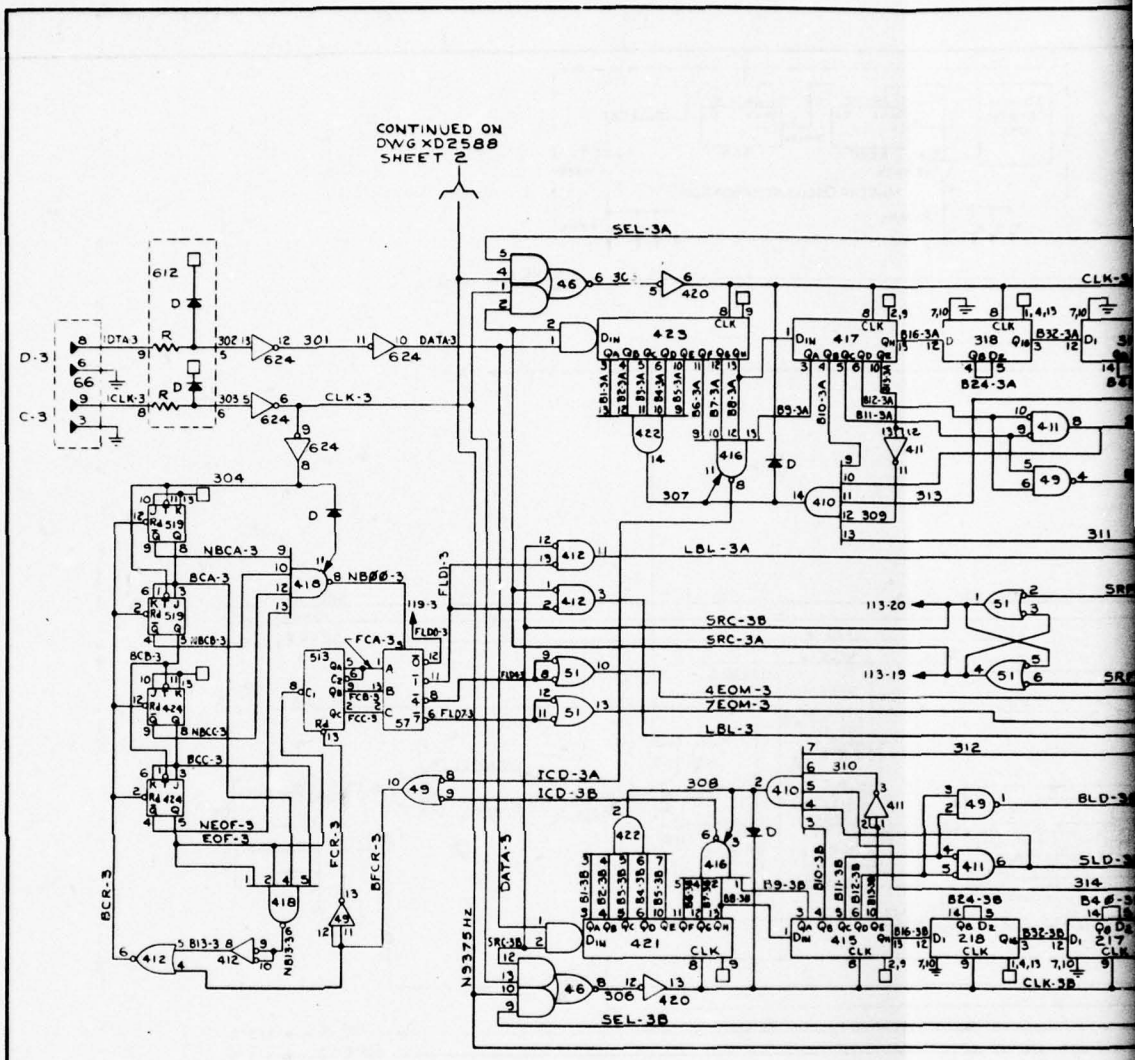
FR-1800 DATA COMPRESSOR CHANNEL 2 INPUT

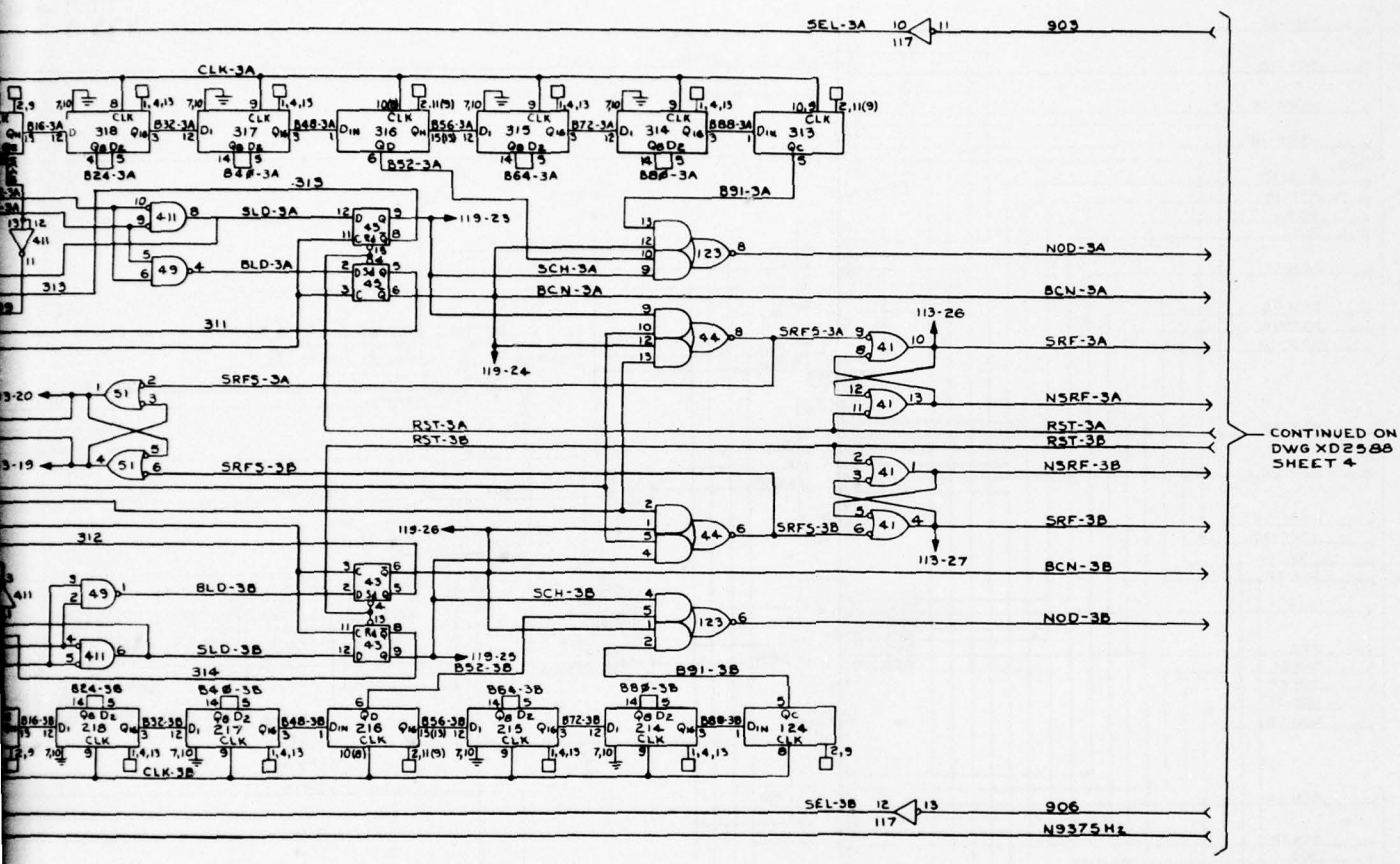
REVIEWED BY		DESIGNED BY	APPROVED BY
KSB	8-29-75	ANA-522	
RLH	8-29-75		
DRAWN BY EA MACK		ISSUED BY ANA-140	DATE 10-16-75
CHECKED BY			DRAWING NO XD2588 SHEET 2 OF 9.

2/9

78-2-A-2

A-2. FR-1800 DATA COMPRESSOR--CHANNEL 2 INPUT--DRAWING XD2588


CONTINUED ON
DWG XD2588
SHEET 2
SEL-3A
SEL-3B
CLK-3
DATA-3
D-3
C-3
612
624
420
423
417
318
218
217
415
421
416
422
410
411
412
418
419
424
513
51
49
46
304
307
308
309
310
311
312
313
314
LBL-3A
LBL-3
SRC-3B
SRC-3A
4EOM-3
7EOM-3
ICD-3A
ICD-3B
NBCA-3
BCA-3
NBCB-3
BCB-3
NBCC-3
BCC-3
NEOF-3
EOF-3
FCA-3
FCB-3
FCC-3
FLD0-3
FLD1-3
FLD2-3
FLD3-3
FCR-3
BFCR-3
BCR-3
NBØØ-3
NB13-3
DATA-S
N9375HZ
SRC-3B
CLK-3B
BLD-3
SLD-3
SRC
113-20
113-19
119-3
119-3B



LEGEND
C = 0.0047 μf
D = IN914
R = 1KΩ, 1/4 W
□ = TO + 5V
M(N) = M IS SOCKET PIN #
WHERE N IS IC PIN #

REV LTR	DATE	DESCRIPTION	DRAWN	APPROVED
A	7/30/74	SHTS. NO. CHGD. FROM 6 TO 9 SHTS.	EW/GHL	8/29/74

FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER — ATLANTIC CITY, N.J.

FR-1800 DATA COMPRESSOR CHANNL 3 INPUT

DESIGNED BY	SUBMITTED BY	APPROVED BY
KSB 10-26-73 RLH 11-28-74	ANA-522	
DRAWN BY E.A. MACK	ISSUED BY ANA-140	DATE 10-17-73
CHECKED BY		DRAWING NO. XD2588 SHEET 3 OF 9.

78-2-A-3

FIGURE A-3. FR-1800 DATA COMPRESSOR--CHANNEL 3 INPUT--DRAWING XD2588

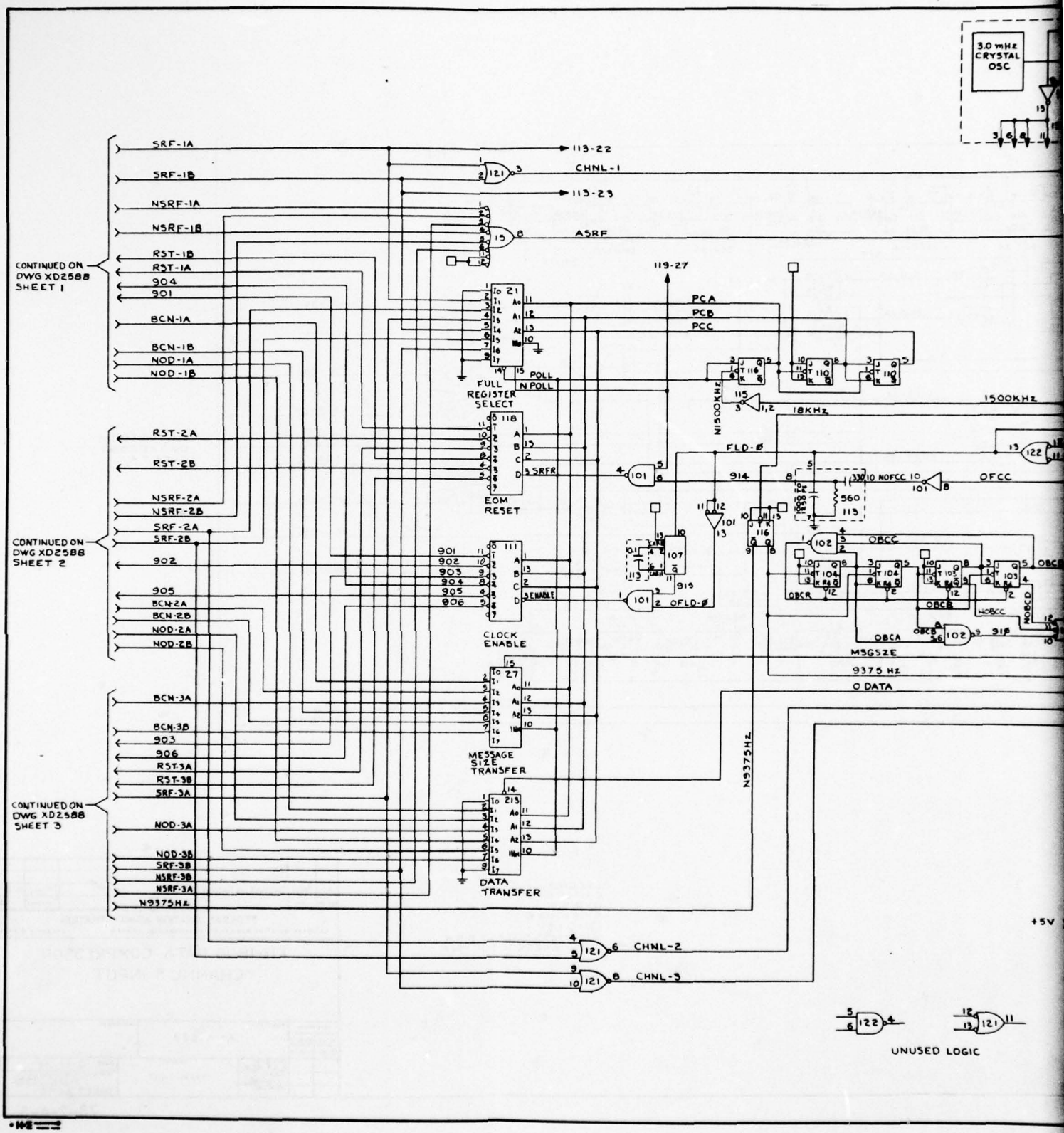
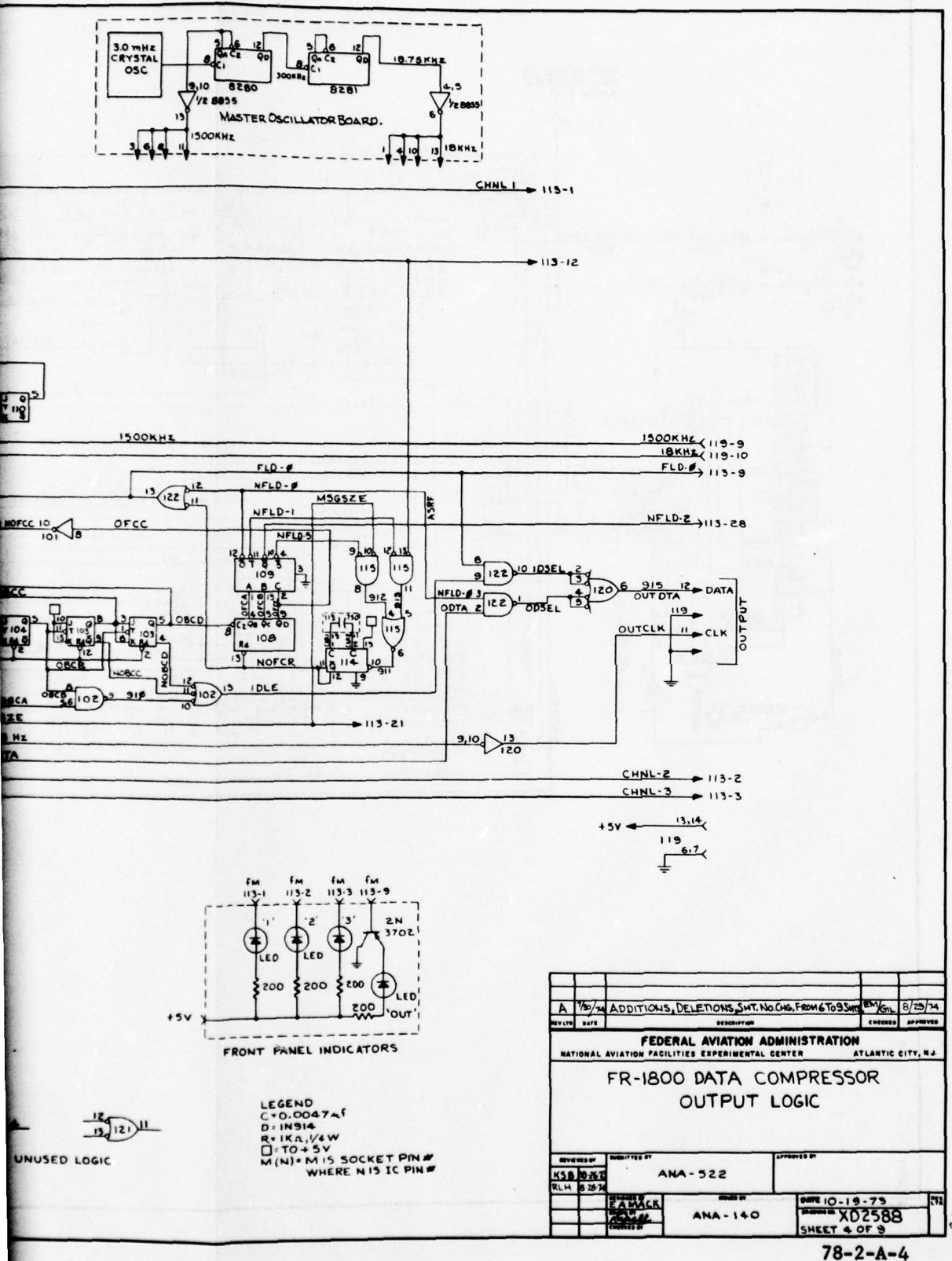


FIGURE A-4. FR-1800 DATA COM



REV LTR	DATE	DESCRIPTION	CHECKED	APPROVED
A	7/30/74	ADDITIONS, DELETIONS, SHT. NO. CHG., FROM 6 TO 9 SHTS	EM/GHL	8/29/74

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NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER — ATLANTIC CITY, N.J.

FR-1800 DATA COMPRESSOR OUTPUT LOGIC

REVIEWED BY		SUBMITTED BY	APPROVED BY
KSB	10-26-73	ANA-522	
RLH	8-28-74		
DESIGNED BY E.A.MACK		ISSUED BY ANA-140	DATE 10-19-73
CHECKED BY			DRAWING NO. XD2588
			SHEET 4 OF 9

78-2-A-4

FR-1800 DATA COMPRESSOR--OUTPUT LOGIC--DRAWING XD2588

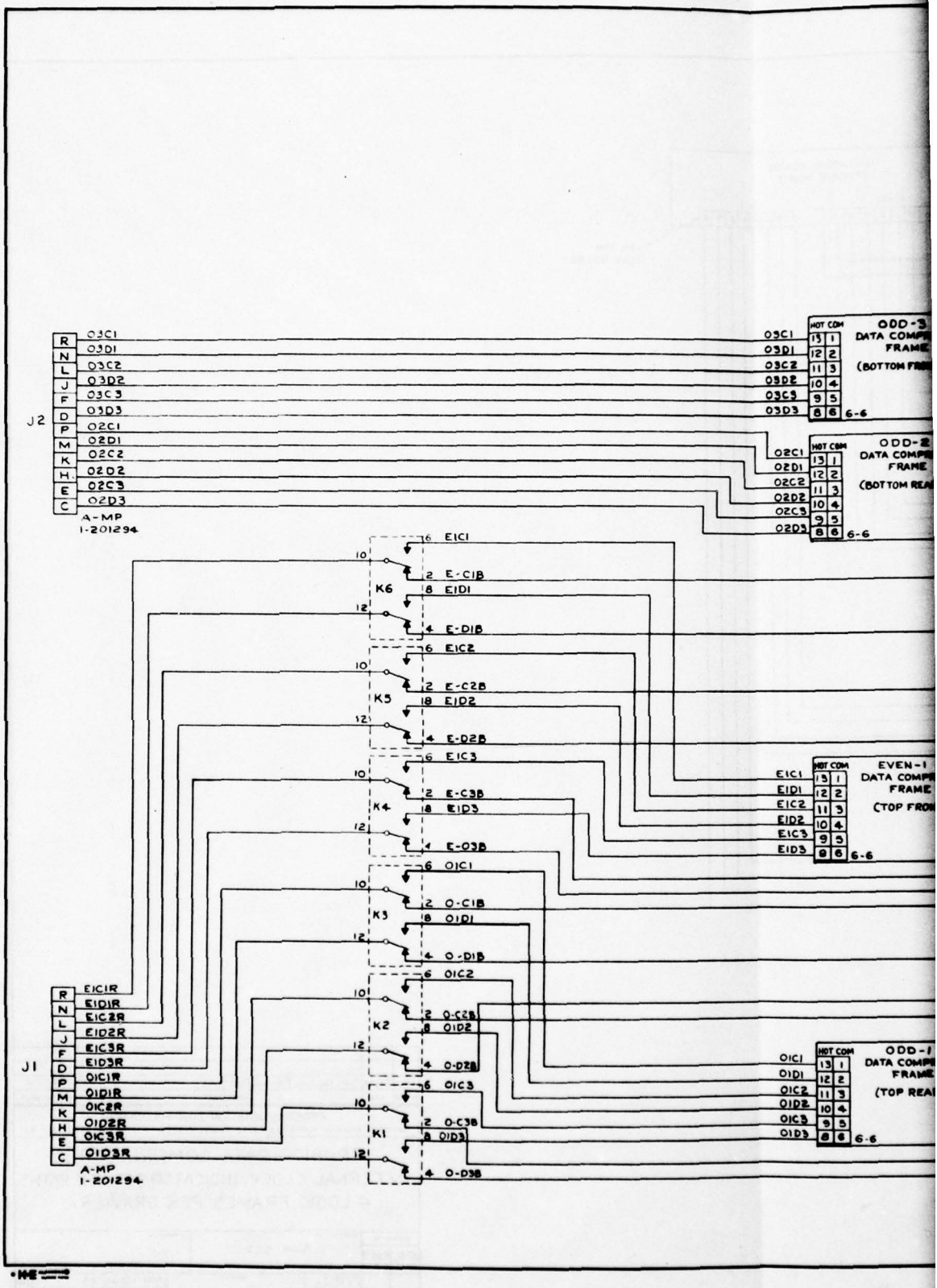
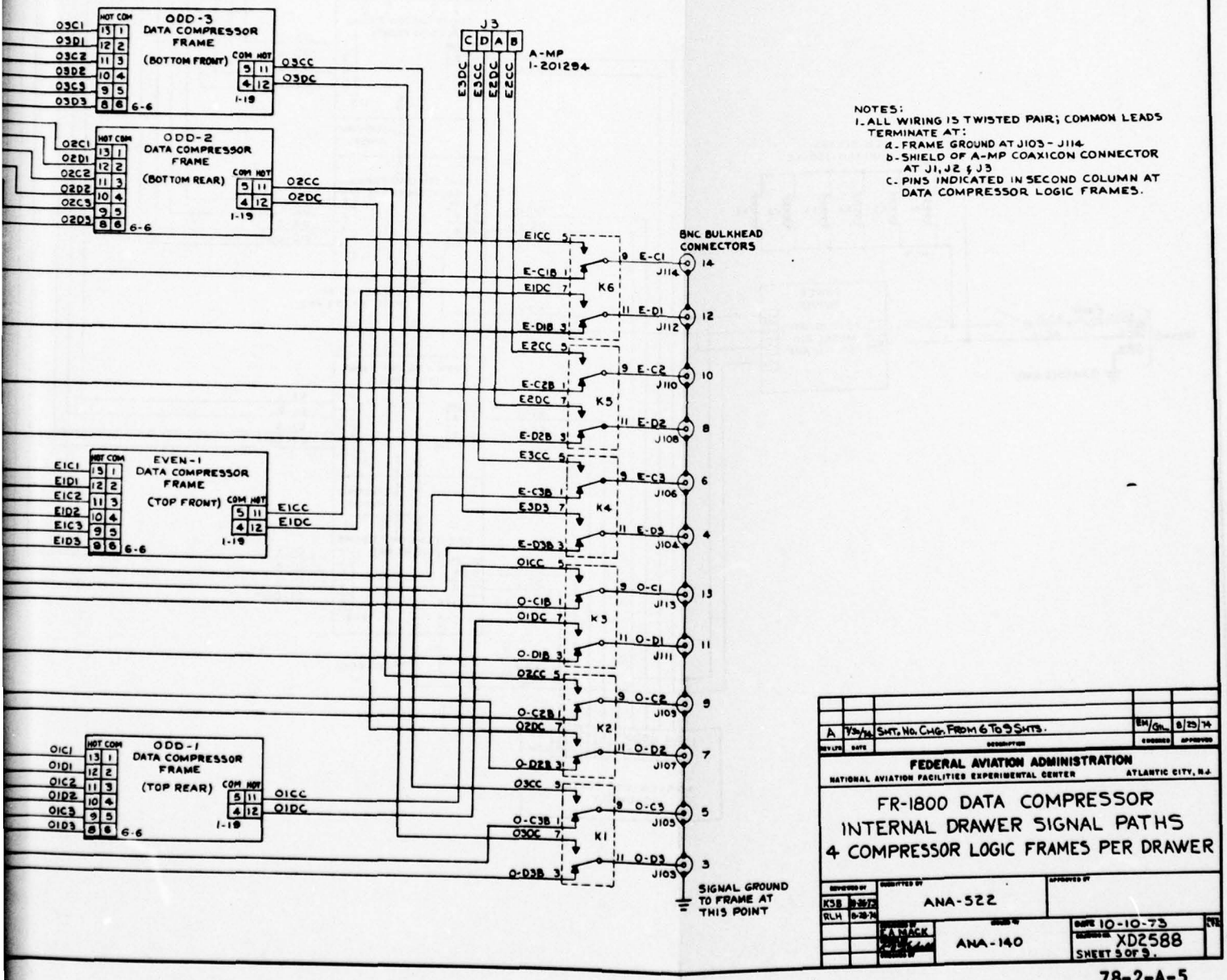


FIGURE A-5. FR-1800 DATA COMPRESSOR-
DRAWING XD2588



NOTES:
1. ALL WIRING IS TWISTED PAIR; COMMON LEADS TERMINATE AT:
   a. FRAME GROUND AT J103 - J114
   b. SHIELD OF A-MP COAXICON CONNECTOR AT J1, J2 & J3
   c. PINS INDICATED IN SECOND COLUMN AT DATA COMPRESSOR LOGIC FRAMES.

REVISIONS			
REV LTR	DATE	DESCRIPTION	ENGINEER / APPROVED
A	7/31/74	SHT. NO. CHG. FROM 6 TO 5 SHTS.	BM/GR. 8/23/74

FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER — ATLANTIC CITY, N.J.

FR-1800 DATA COMPRESSOR INTERNAL DRAWER SIGNAL PATHS 4 COMPRESSOR LOGIC FRAMES PER DRAWER

DESIGNED BY	SUBMITTED BY	APPROVED BY
KSB 8-28-73 RLH 8-28-74	ANA-522	
DRAWN BY F.A. MACK	CHECKED BY ANA-140	DATE 10-10-73
		SCALE NONE — SHEET 5 OF 5. — XD2588

78-2-A-5

DATA COMPRESSOR--INTERNAL DRAWER SIGNAL PATHS--4 COMPRESSOR LOGIC FRAMES PER DRAWER--
XD2588

A-5

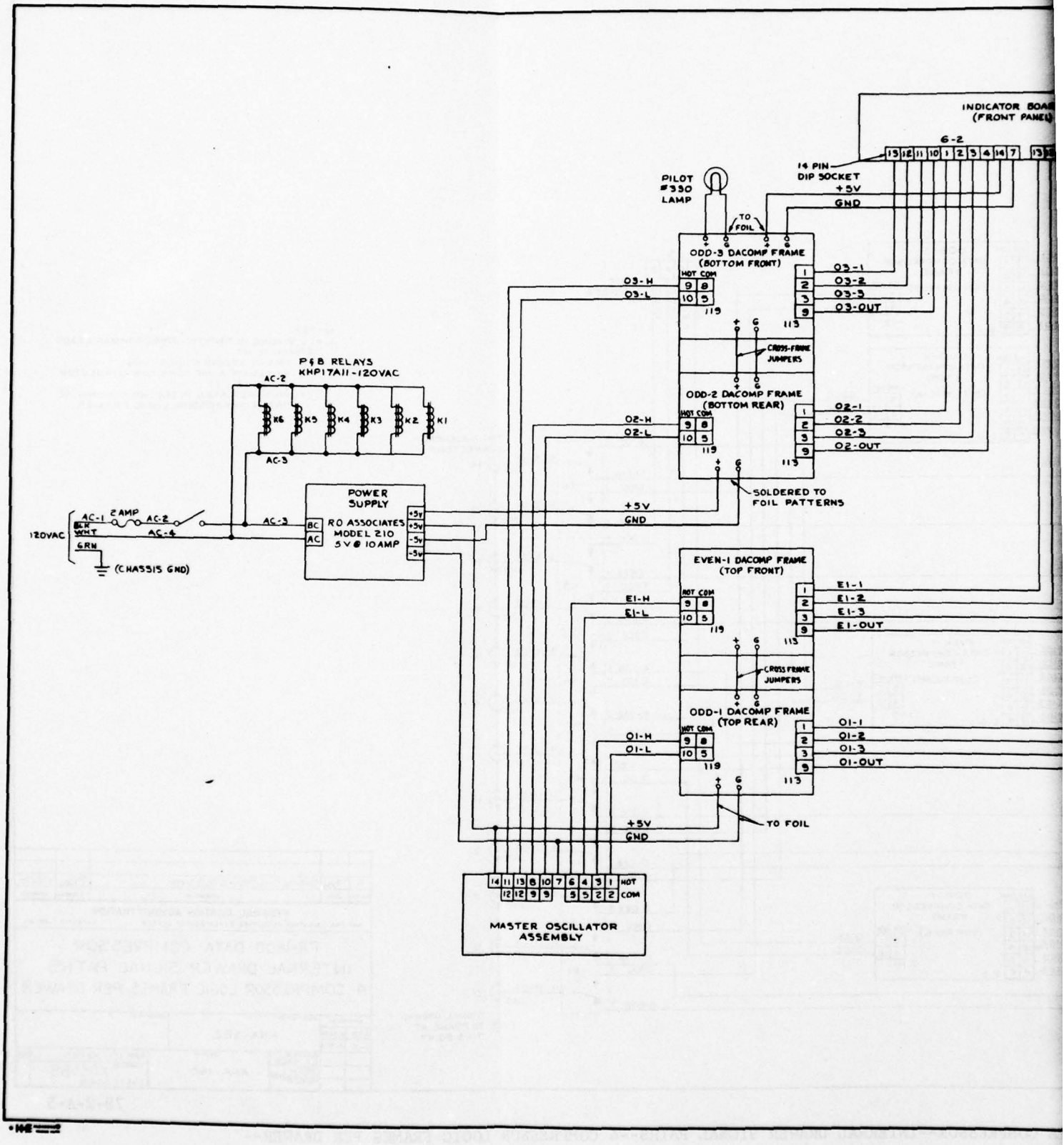
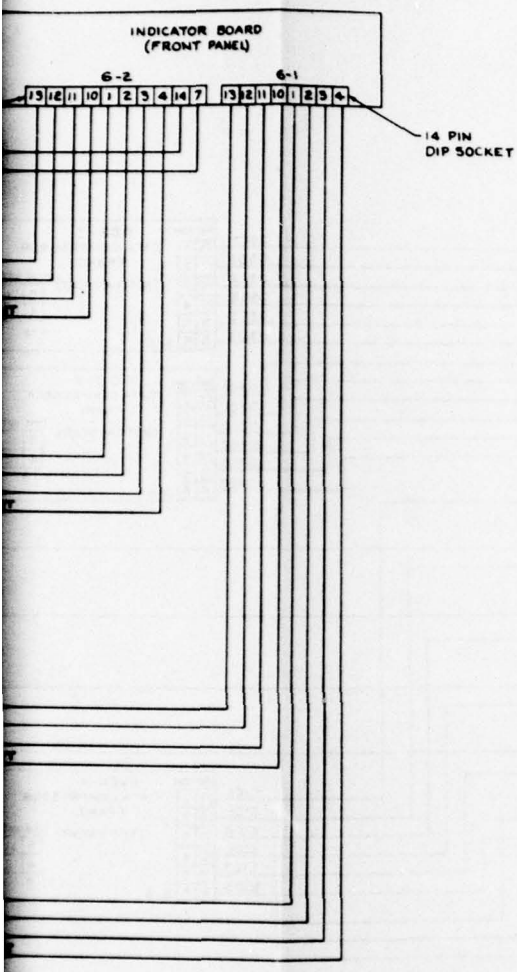


FIGURE A-6. FR-1800 DATA COMPRESSOR--INTERNAL CLOCK, INDI
DRAWING XD2588



REVISED BY	DATE	DESCRIPTION	CHECKED	APPROVED
A	7/24/74	SHT. NO. CHG. FROM 6 TO 9 SHTS.	EM/GM	8/29/74

FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER — ATLANTIC CITY, N.J.

FR-18100 DATA COMPRESSOR
INTERNAL CLOCK, INDICATOR & POWER PATHS
4 LOGIC FRAMES PER DRAWER

REVISED BY	DATE	SUBMITTED BY	APPROVED BY
KSB	9-26-74	ANA-522	
RLH	9-18-74		

APPROVED BY	ISSUED BY	DATE	SIZE
E.A. MACK	ANA-140	10-11-73	
		DRAWING NO. XD2588 SHEET 6 OF 9.	

78-2-A-6

ERNAL CLOCK, INDICATOR AND POWER PATHS--4 LOGIC FRAMES PER DRAWER--

2

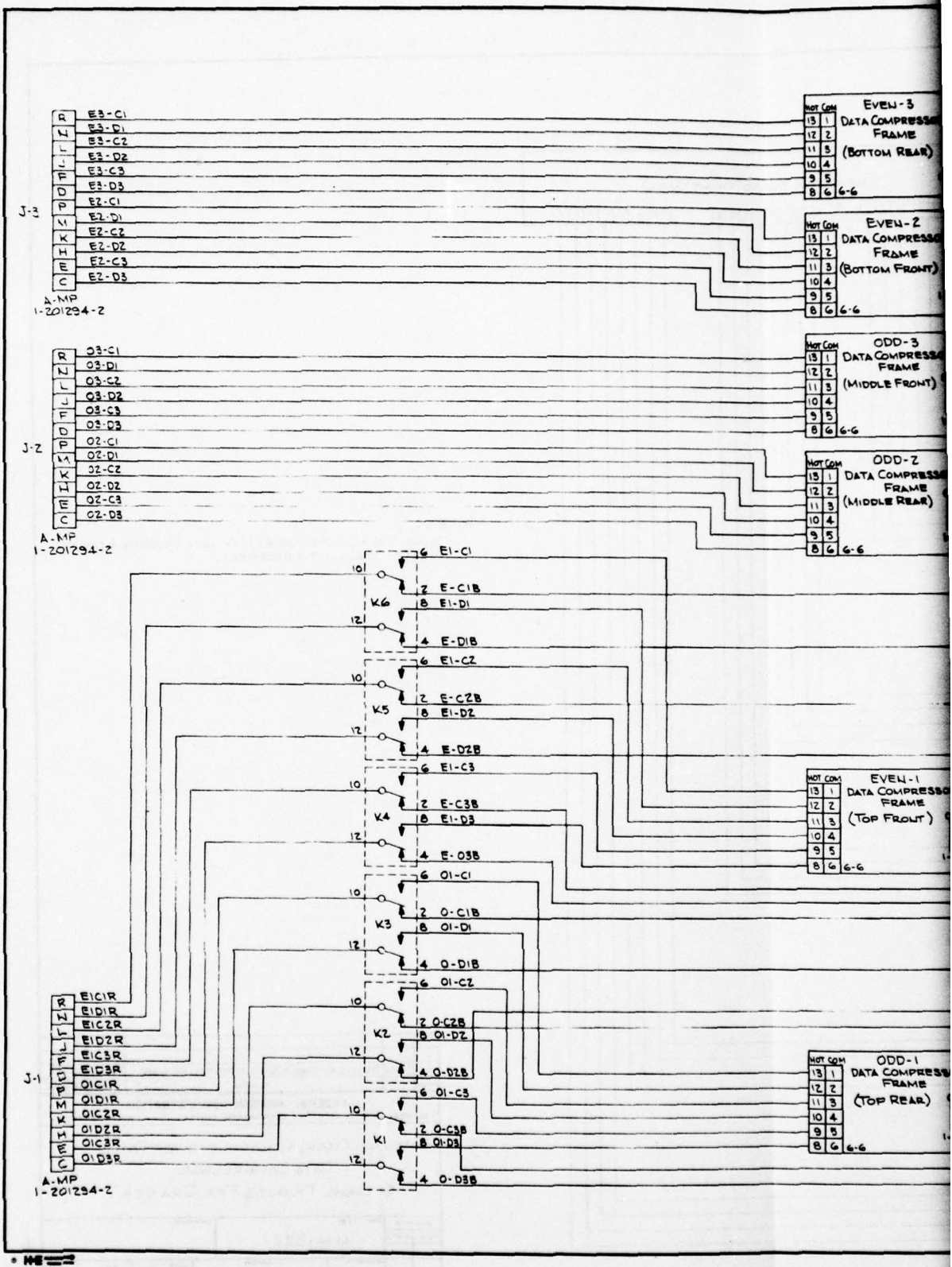
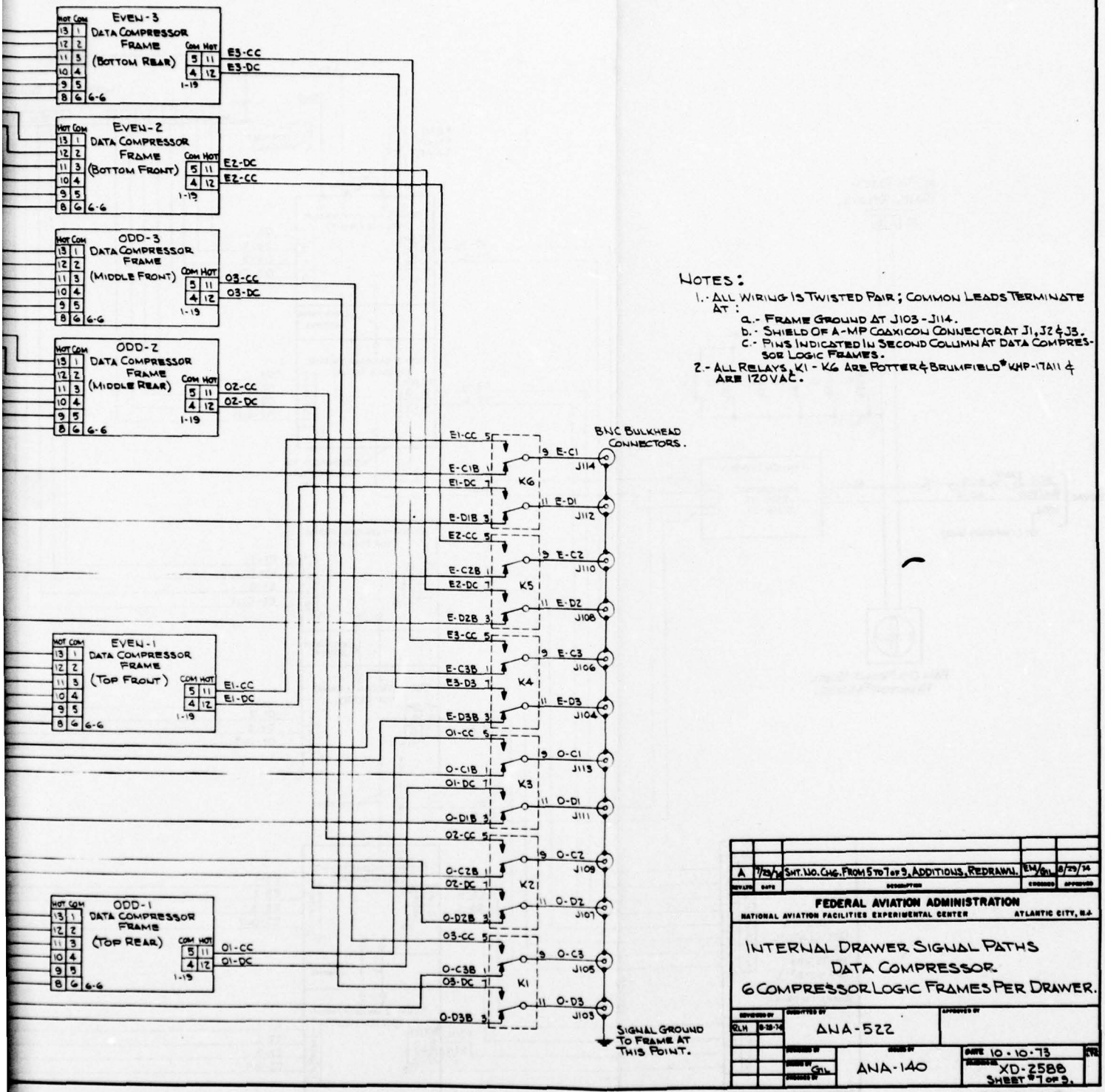


FIGURE A-7. INTERNAL DRAWER SIGNAL PATHS-DRAWING XD2588



NOTES:

1. ALL WIRING IS TWISTED PAIR; COMMON LEADS TERMINATE AT:
   a. FRAME GROUND AT J103 - J114.
   b. SHIELD OF A-MP COAXICON CONNECTOR AT J1, J2 & J3.
   c. PINS INDICATED IN SECOND COLUMN AT DATA COMPRESSOR LOGIC FRAMES.
2. ALL RELAYS, K1 - K6 ARE POTTER & BRUMFIELD* KHP-17A11 & ARE 120VAC.

REVISED BY	DATE	DESCRIPTION	CHECKED	APPROVED
A	7/29/74	SHT. NO. CHG. FROM 5 TO 7 OF 9. ADDITIONS, REDRAWN.	EM/GHL	8/29/74

FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER ATLANTIC CITY, N.J.

INTERNAL DRAWER SIGNAL PATHS
DATA COMPRESSOR
6 COMPRESSOR LOGIC FRAMES PER DRAWER.

REVISED BY	DATE	SUBMITTED BY	APPROVED BY
GLH	8-28-74	ANA-522	

DESIGNED BY	DRAWN BY	ISSUED BY	DATE
	GHL	ANA-140	10-10-73

XD-2588 SHEET #7 OF 9.

2/8

78-2-A-7

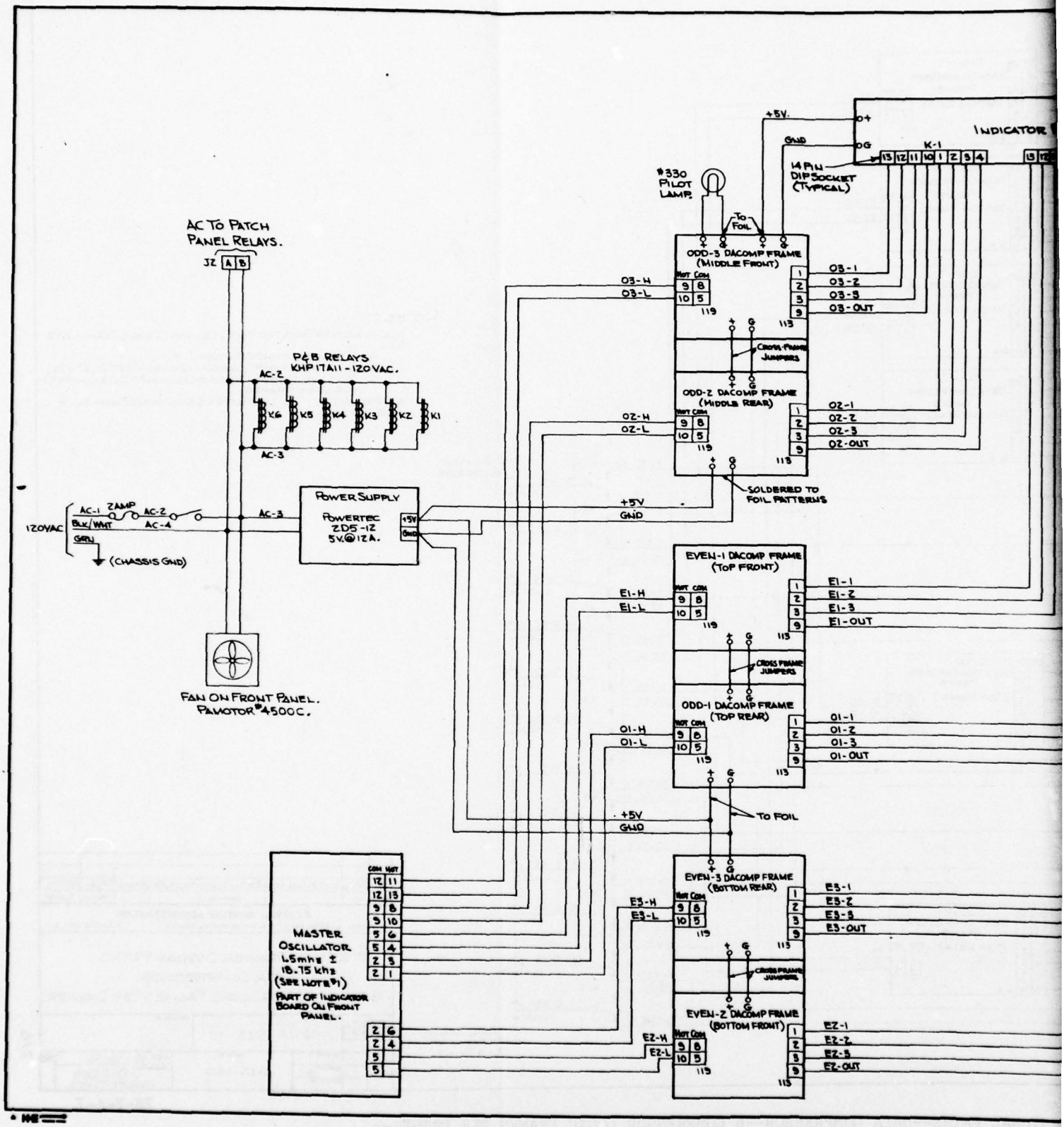
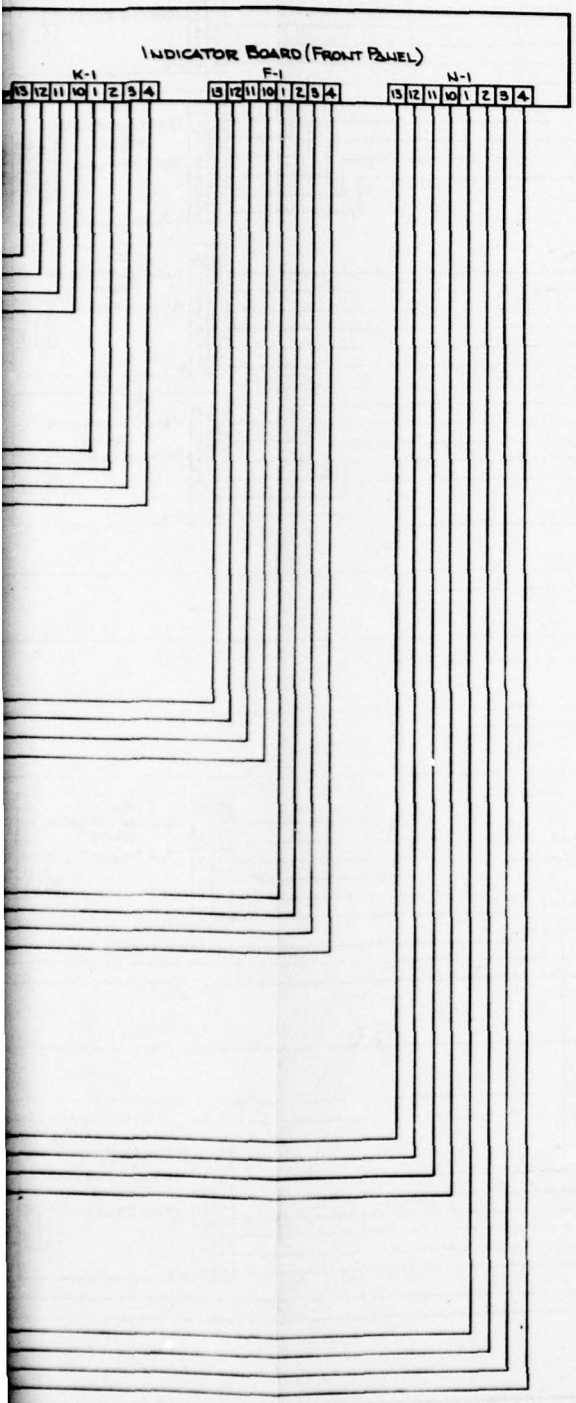


FIGURE A-8. INTERNAL CLOCK, INDICATOR AND POWER PATHS
DRAWING XD2588



NOTES:

1.- SOME DATA COMPRESSORS MAY HAVE A 1.5mhz & 24 khz MASTER OSCILLATOR ASSEMBLY.

A	7/29/74	SHT. NO. CHG. FROM 6 TO 8 OF 9, ADDITIONS, REDRAWN.	EM/GSL	8/23/74
RELEASED	DATE	DESCRIPTION	CHECKED	APPROVED

FEDERAL AVIATION ADMINISTRATION

NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER — ATLANTIC CITY, N.J.

INTERNAL CLOCK, INDICATOR & POWER PATHS
DATA COMPRESSOR
6 LOGIC FRAMES PER DRAWER.

DESIGNED BY RLH 8-23-74	DRAWN BY ANA-522	APPROVED BY	
	ISSUED BY ANA-140	DATE 10-11-73	REV.
		XD-2588 SHEET 8 OF 9.	

2/8

78-2-A-8

OR AND POWER PATHS--DATA COMPRESSOR--6 LOGIC FRAMES PER DRAWER--

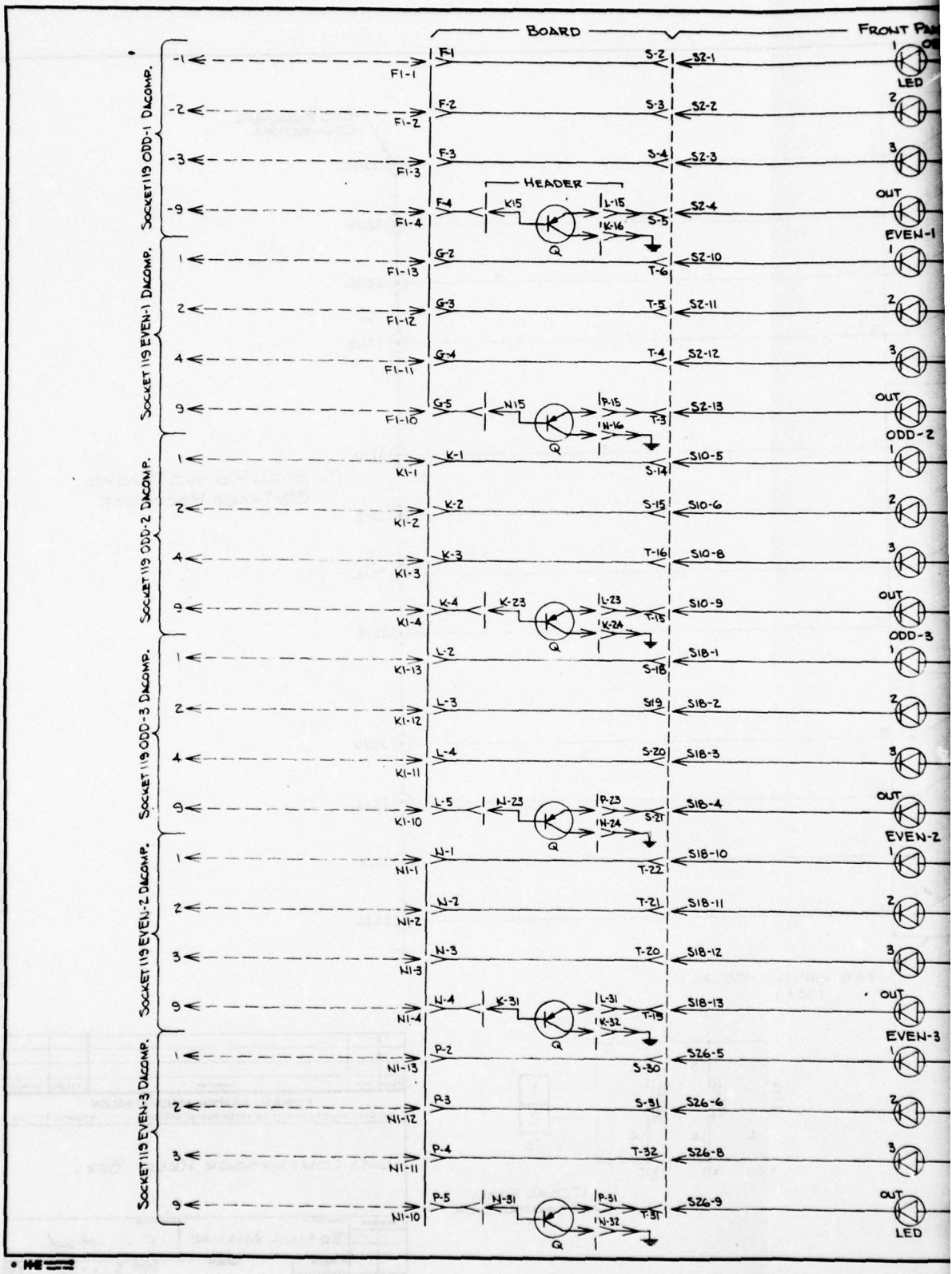
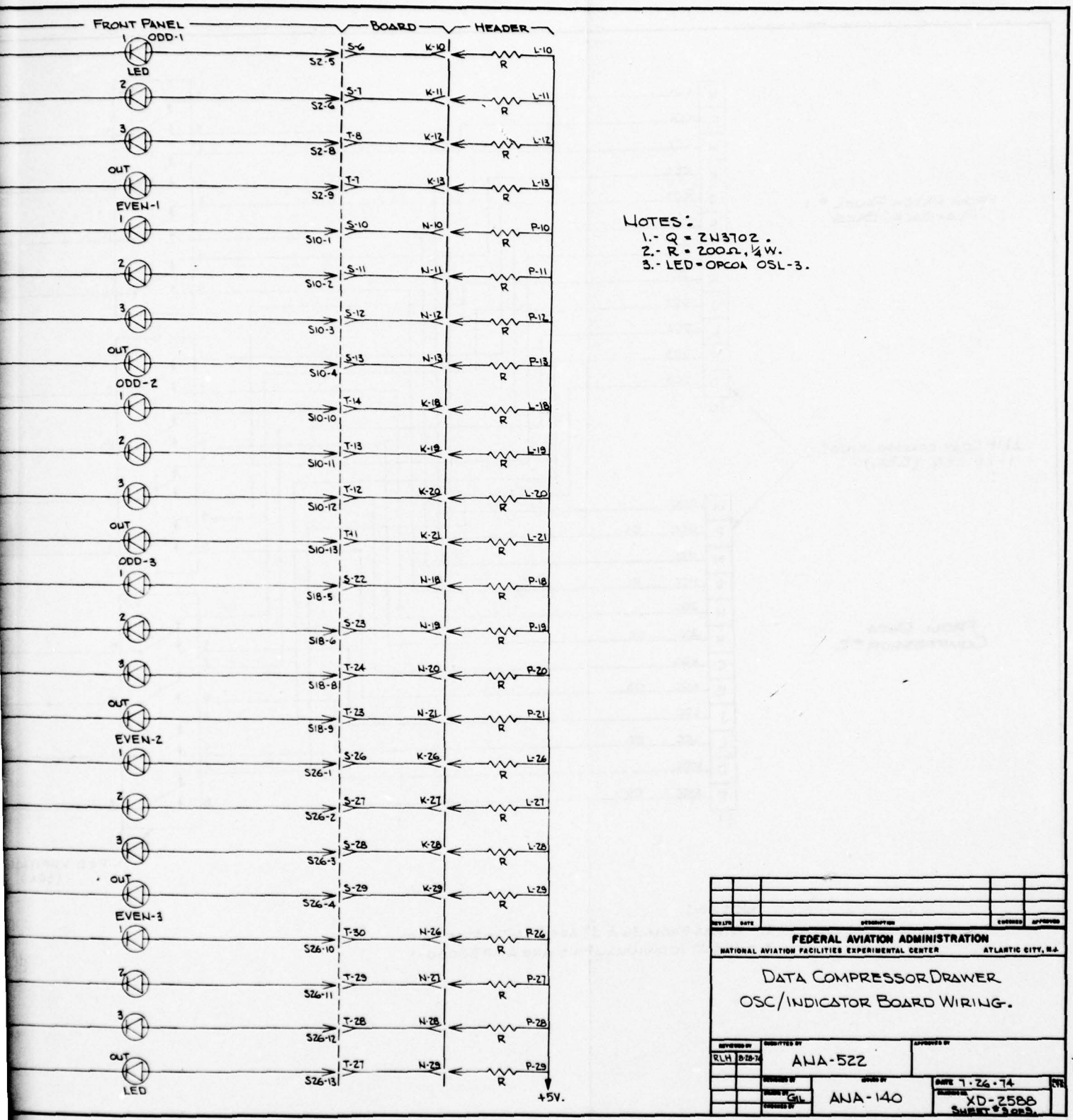


FIGURE A-9. DATA



NOTES:
1.- Q = 2N3702.
2.- R = 200Ω, ¼W.
3.- LED = OPCOA OSL-3.

REVISIONS					
REV. LTR	DATE	DESCRIPTION		DRAWN	APPROVED

FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER — ATLANTIC CITY, N.J.

DATA COMPRESSOR DRAWER
OSC/INDICATOR BOARD WIRING.

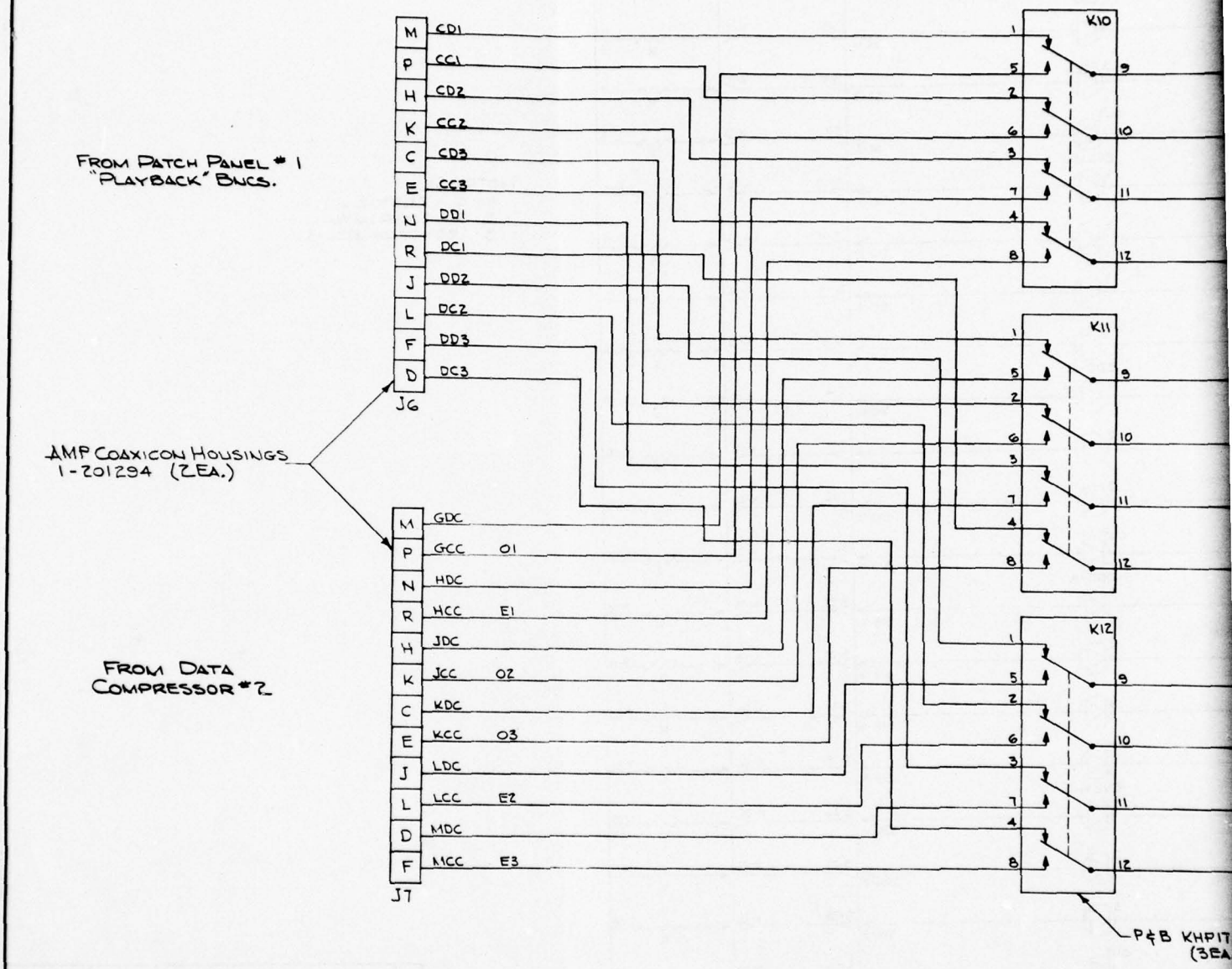
REVISED BY: RLH 8-28-74	SUBMITTED BY: ANA-522	APPROVED BY:	
DRAWN BY: GHL	ISSUED BY: ANA-140	DATE: 7-26-74	
CHECKED BY:		DRAWING NO.: XD-2588 SHEET 2 OF 3 SHTS.	

2/8

78-2-A-9

URE A-9. DATA COMPRESSOR DRAWER--OSC/INDICATOR BOARD WIRING--DRAWING XD2588

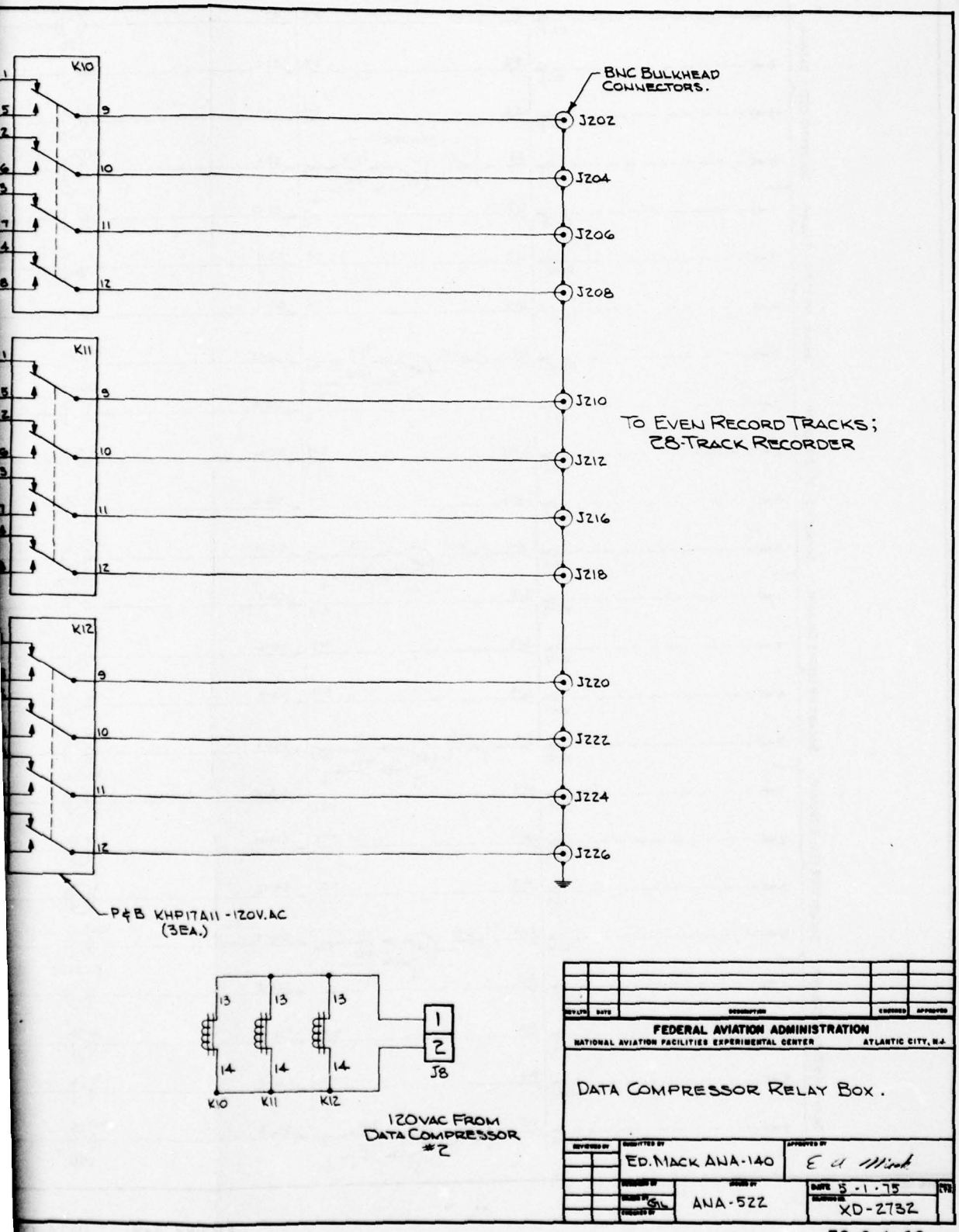
2



NOTES:

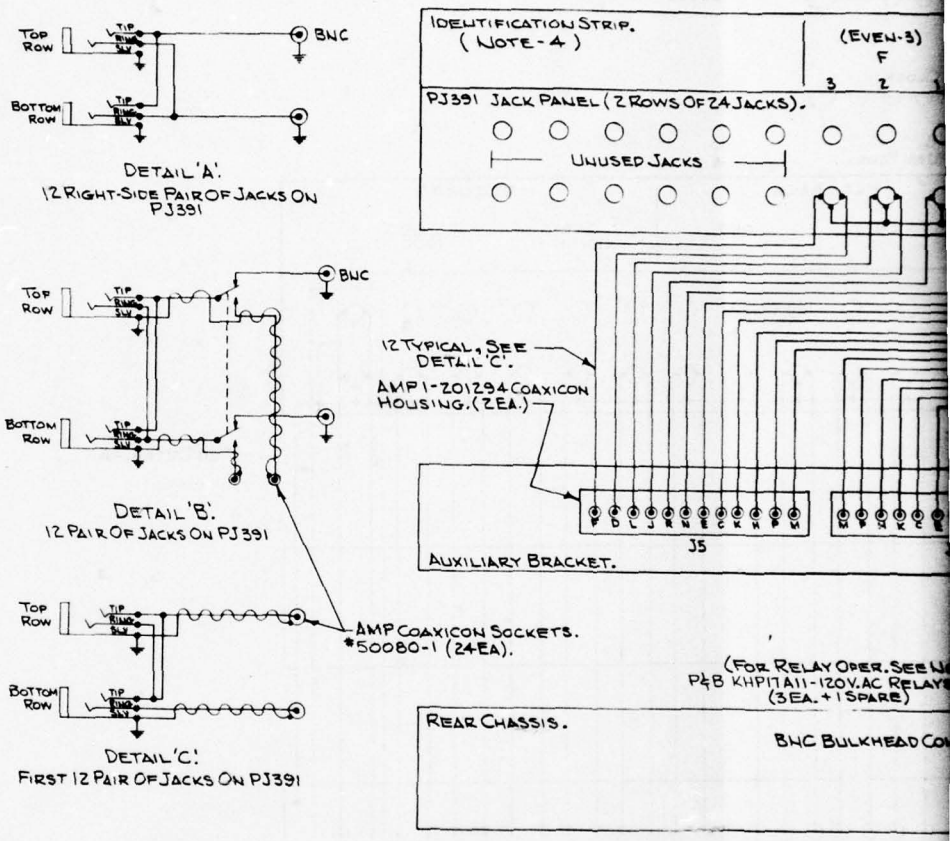
1. - WIRES FROM J6 & J7 ARE #26 TWISTED PAIRS.
2. - J6 & J7 INDIVIDUAL PINS ARE AMP 50080-1.

FIGURE A-1



78-2-A-10

FIGURE A-10. DATA COMPRESSOR RELAY BOX--DRAWING XD2732



NOTES:

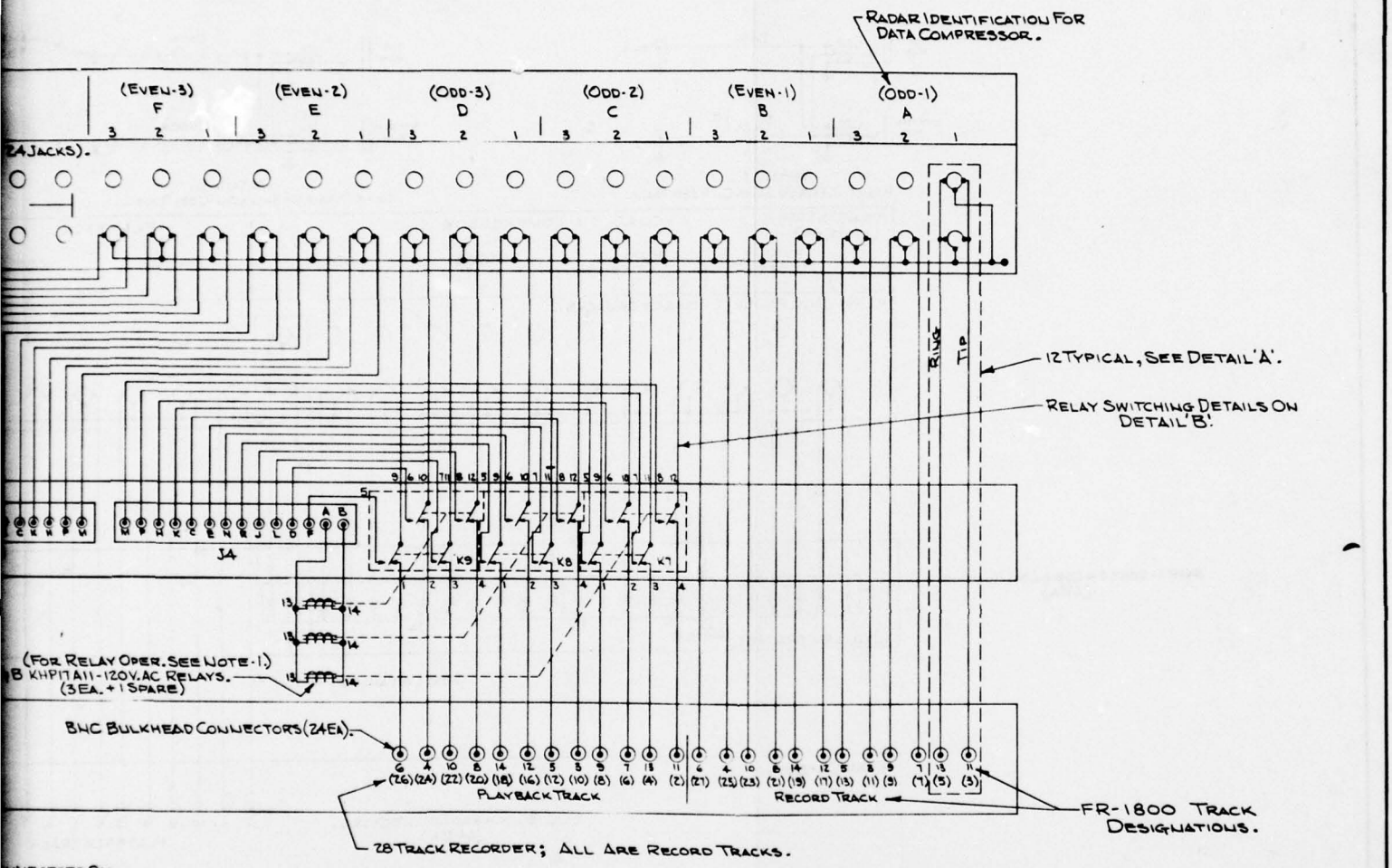
1.- WITH THE RELAYS DEENERGIZED, DATA GOES TO THE PLAYBACK BNC CONNECTORS ON THE REAR CHASSIS. WITH 120V. AC SUPPLIED FROM THE DATA COMPRESSOR THRU J4 THE RELAYS ROUTE THE SIGNALS FROM C & D RADARS TO J4.

2.- THIS PATCH PANEL IS A MODIFICATION OF THE PANEL SUPPLIED WITH THE FR-1800 INTERFACE KIT., FSN 9274-407-7586.

3.- ORIGINAL PANEL DRAWINGS - FAA DEPOT DE-C-1005-1, SHTS. 1 TO 4.

4.- I D STRIP SHOWN REVERSED FOR CLARITY.

FIGURE



TOP VIEW OF RECORDER PATCH PANEL

NNECTORS ON
SSOR THRU J4

D WITH THE

S. 1 TO 4.

REV LTR	DATE	DESCRIPTION	CHECKED	APPROVED

FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER ATLANTIC CITY, N.J.

RECORDER PATCH PANEL
W/ RELAY MODIFICATION.

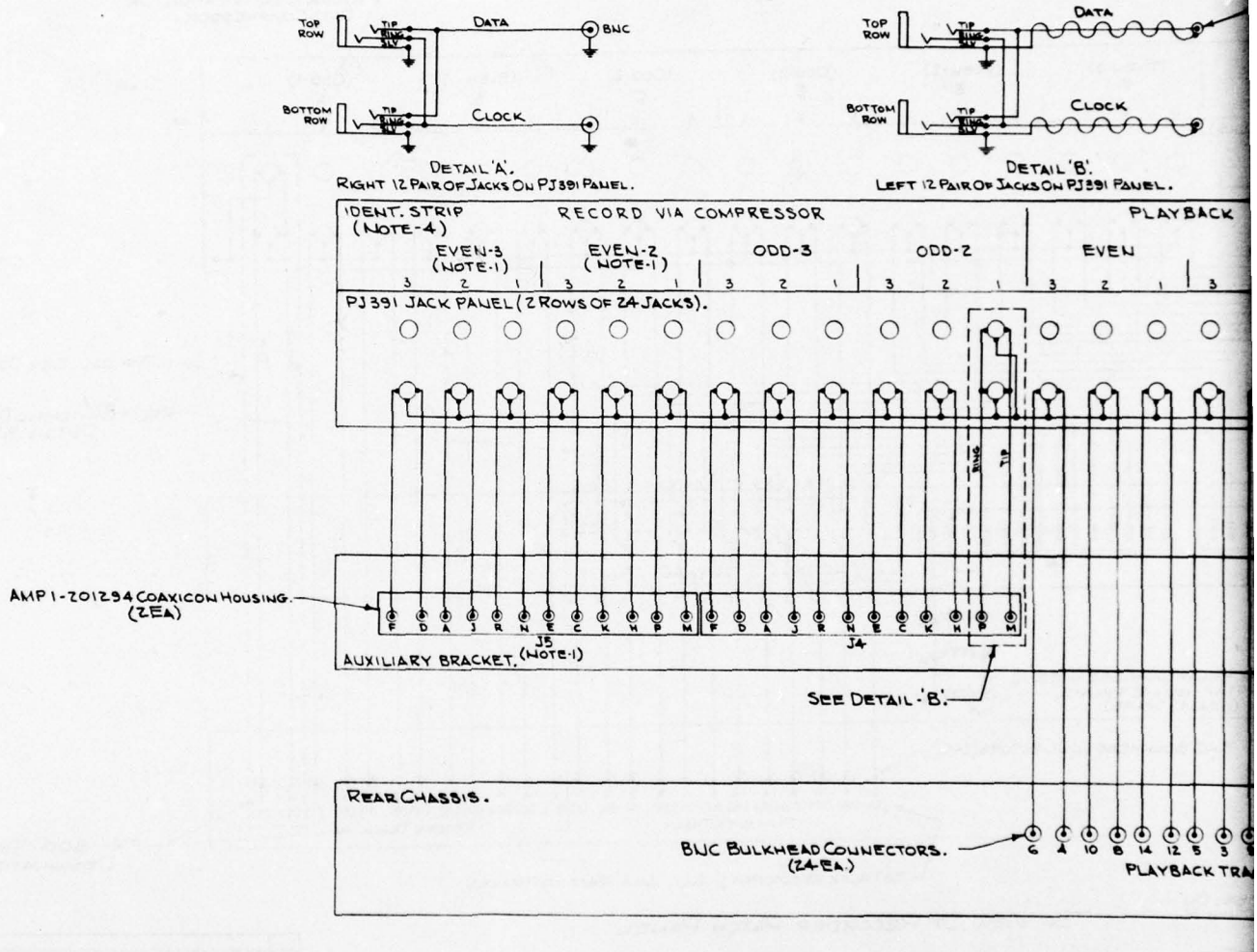
SUBMITTED BY: ED. MACK ANA-140	APPROVED BY: E. a Mack	
DESIGNED BY / DRAWN BY: ANA-522	DATE: 4-30-75	DRAWING NO.: XD-2730

2/9

78-2-A-11

FIGURE A-11. RECORDER PATCH PANEL WITH RELAY MODIFICATION--DRAWING XD2730

2



TOP VIEW OF PATCH PANEL ASSE

NOTES:

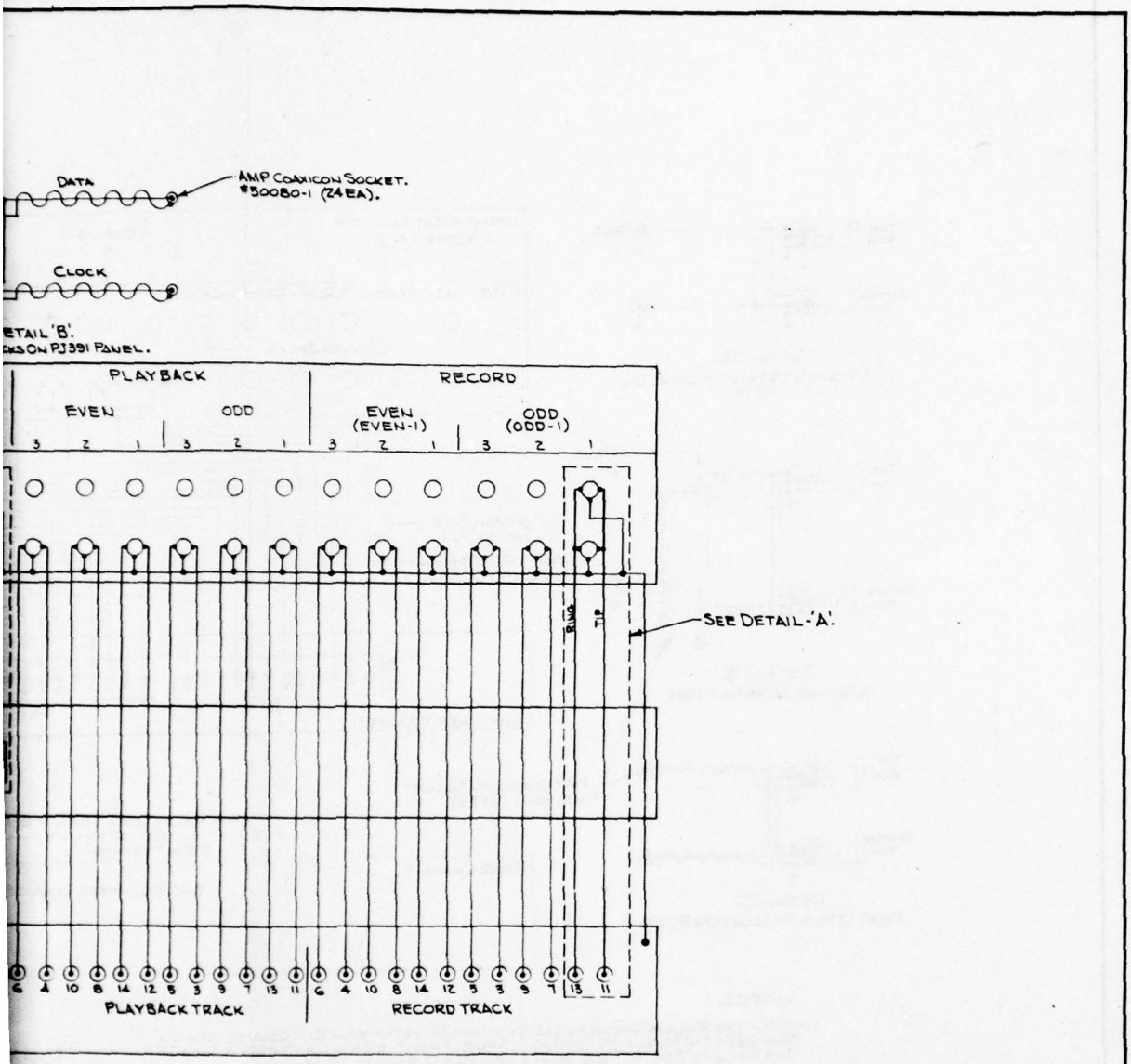
1.- WITH THE 4 RADAR DATA COMPRESSORS, J5 WILL NOT BE USED AND THE EVEN-2 & EVEN-3 DESIGNATIONS ON THE IDENTIFICATION PANEL WILL BE OMITTED.

2.- THIS PATCH PANEL IS A MODIFICATION OF THE PANEL SUPPLIED WITH THE FR-1800 INTERFACE KIT., FSN 9274-407-7586.

3.- REFERENCE DRAWINGS, FAA DEPOT DE-C-1005-1 SHTS. 1 TO 4.

4.- ID STRIP SHOWN REVERSED FOR CLARITY.

FIGURE A-12. RECORDER PATCH P



TCH PANEL ASSEMBLY

REV LTR	DATE	DESCRIPTION	CHECKED	APPROVED

FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER ATLANTIC CITY, N.J.

RECORDER PATCH PANEL, W/ J4 - J5 MODIFICATION.

REVIEWED BY	SUBMITTED BY	APPROVED BY
	ED. MACK ANA-140	C. F. [illegible]

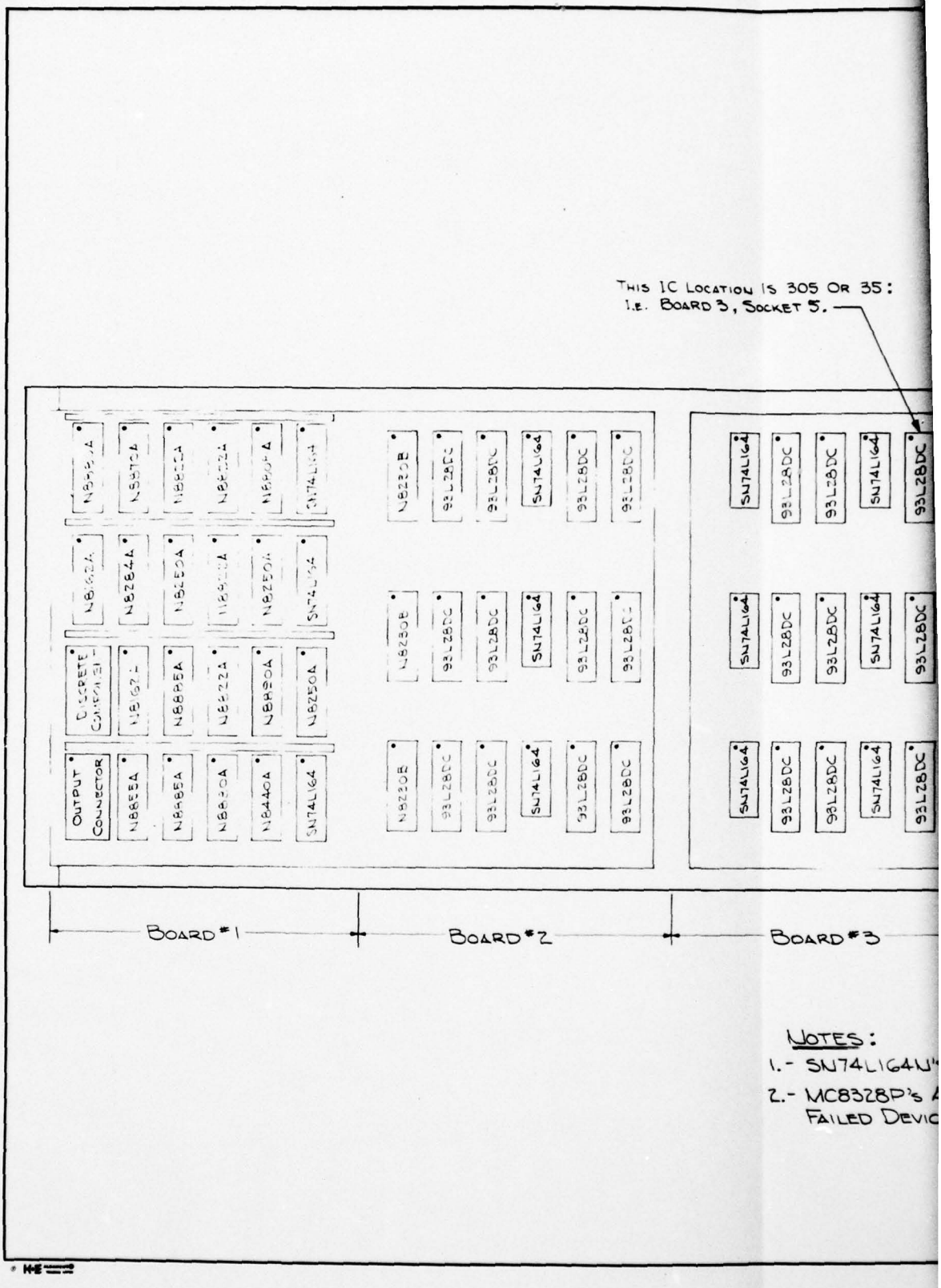
DESIGNED BY	DRAWN BY	DATE	CAGE
CHECKED BY	ANA-522	5-1-75	
		DRAWING NO. XD-2731	

2/9

78-2-A-12

RECORDER PATCH PANEL WITH J4/J5 MODIFICATION--DRAWING XD2731

2

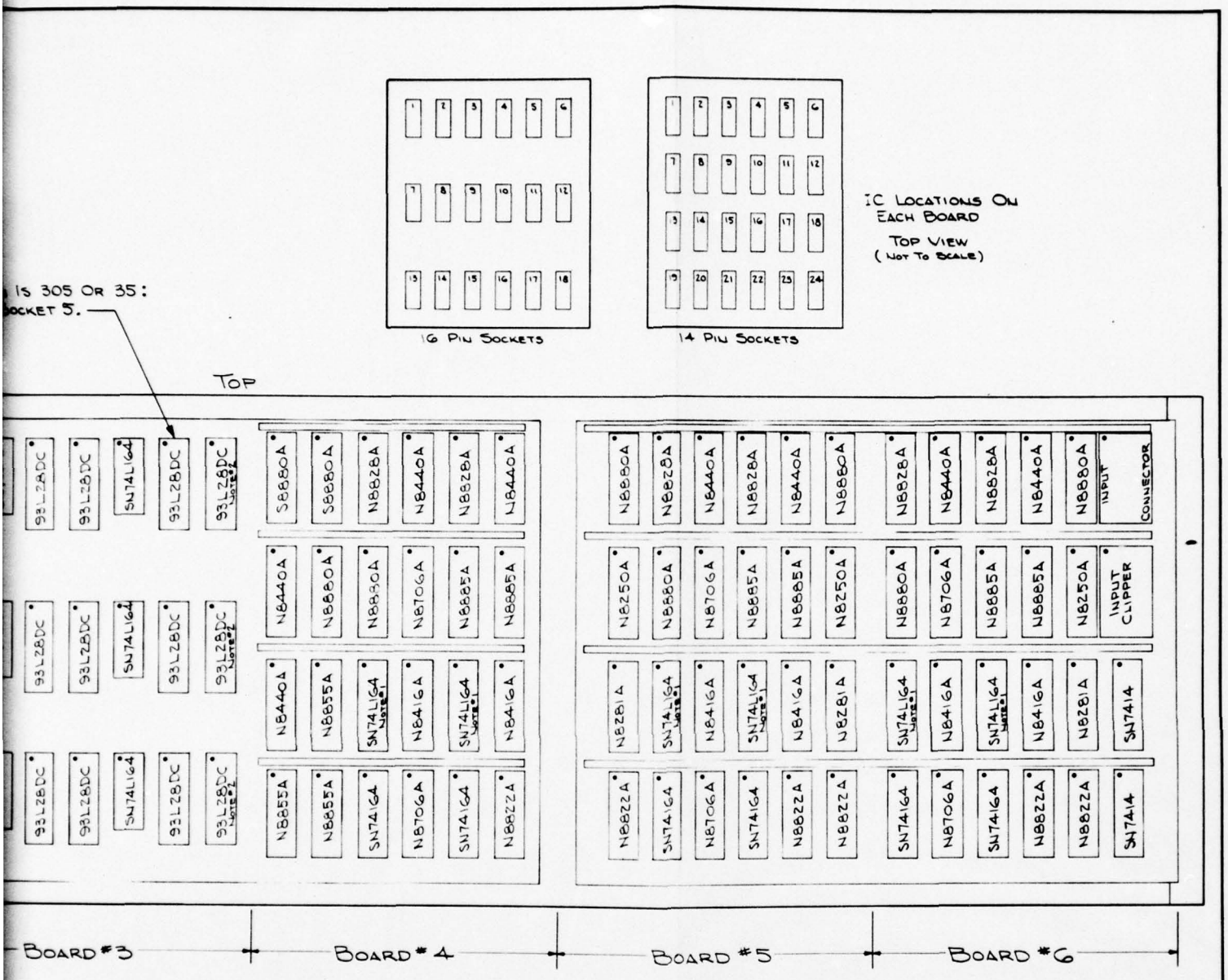


NOTES:

1.- SN74LI64N

2.- MC8328P's A
FAILED DEVIC

FIGURE



NOTES:

1.- SN74L164N's IN THESE LOCATIONS MAY BE REPLACED WITH SN74164's.

2.- MC8328P's AND 9328's MAY BE IN ALL OR SOME 93L28 LOCATIONS. FAILED DEVICES SHOULD BE REPLACED WITH 93L28's.

SCALE - 2/1.

REV LTR	DATE	DESCRIPTION	DRAWN	APPROVED
A	4/15/74	ADDED IC LOCATIONS ON BOARD	EM/GL	

FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER ATLANTIC CITY, N.J.

SINGLE DATA COMPRESSOR FRAME IC LAYOUT.

REVIEWED BY	SUBMITTED BY	APPROVED BY
E.M. 9/24/74	ANA-522	Ed Mack
DRAWN BY E. MACK; CHECKED BY GIL	ISSUED BY ANA-140	DATE 10-22-74; DRAWING NO. XD-2699

2/9

78-2-A-13

FIGURE A-13. SINGLE DATA COMPRESSOR FRAME-IC LAYOUT--DRAWING XD2699

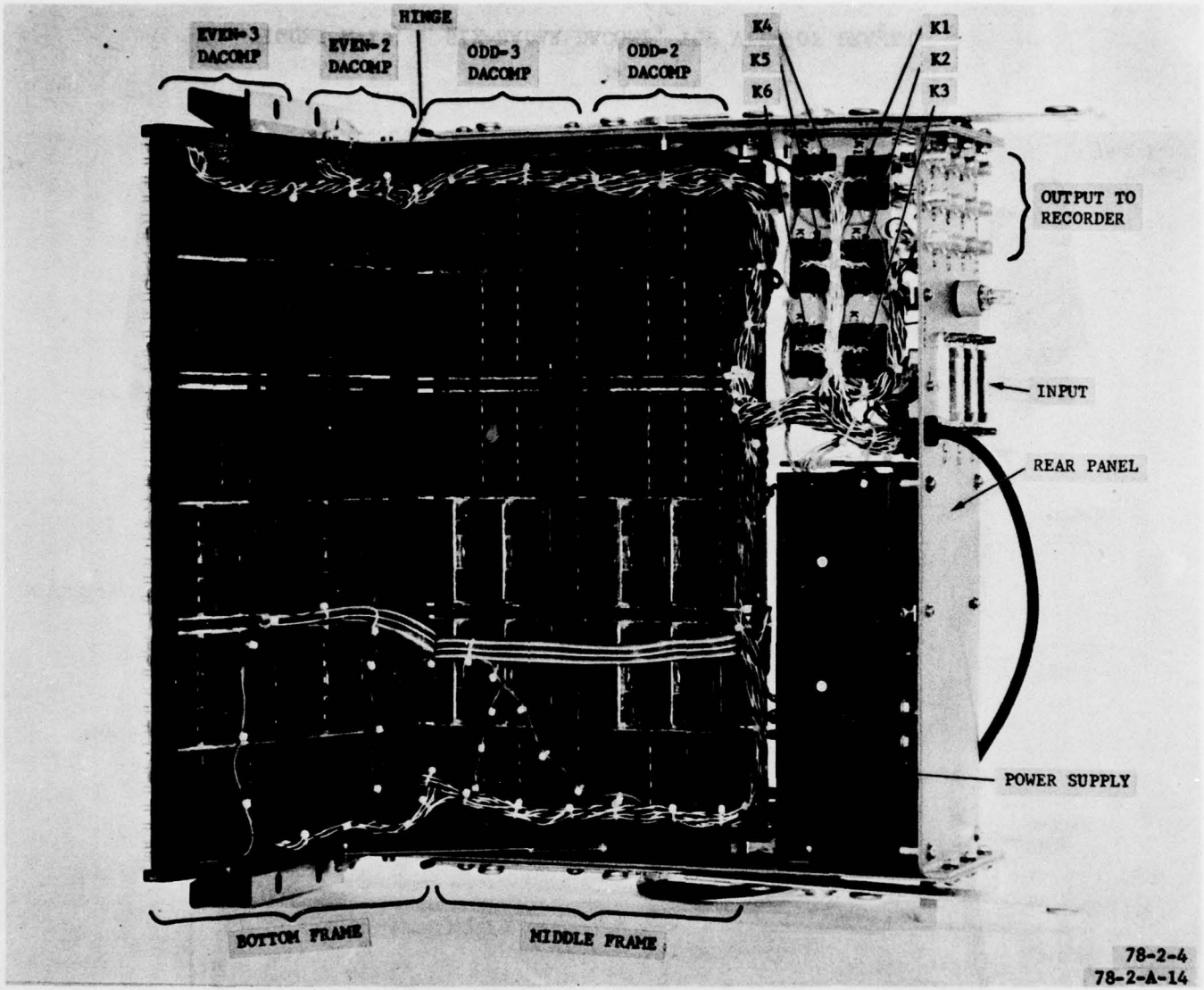


FIGURE A-14. SIX-RADAR DACOMP, BOTTOM VIEW OF DRAWER

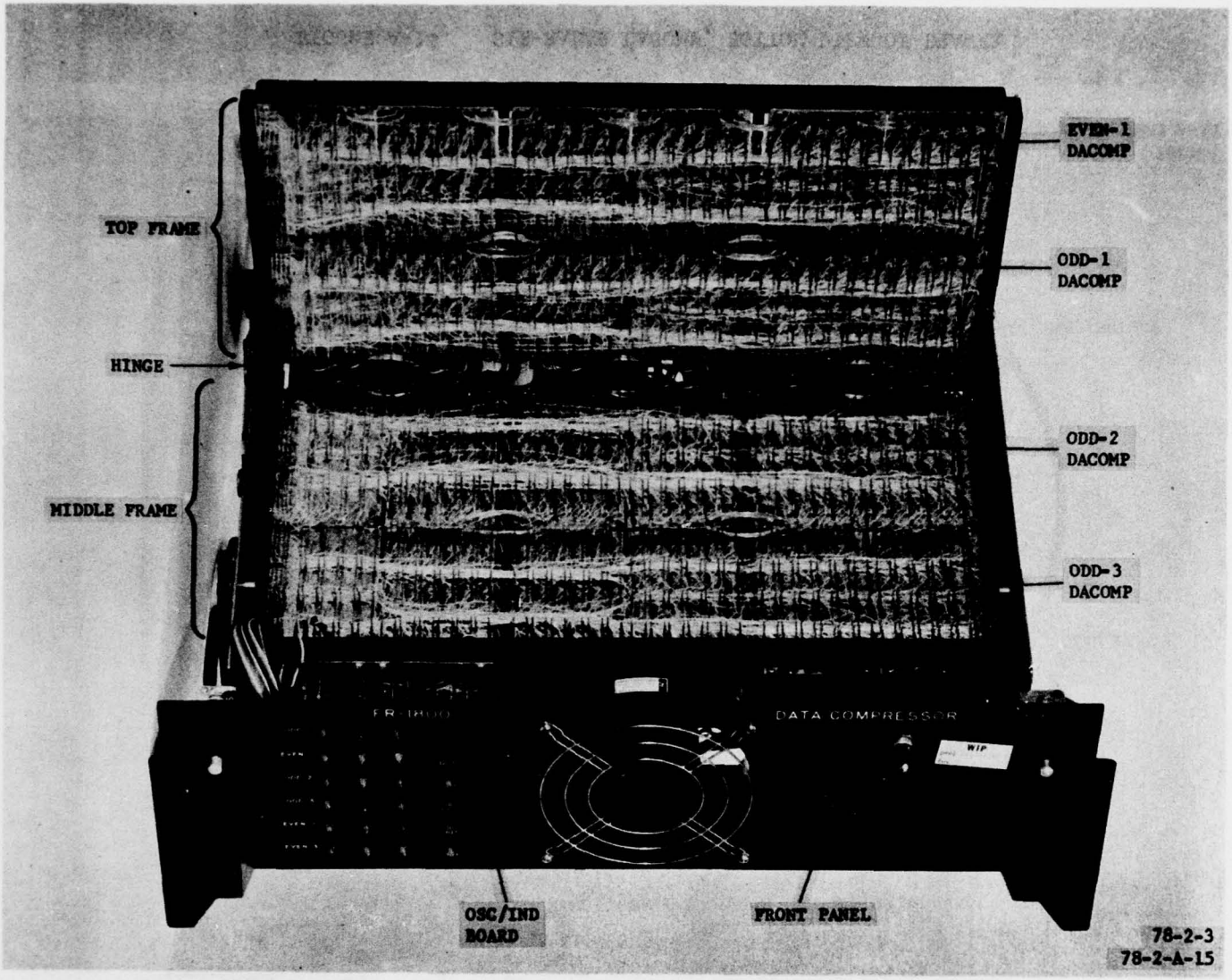


FIGURE A-15. SIX-RADAR DACOMP, TOP VIEW OF DRAWER

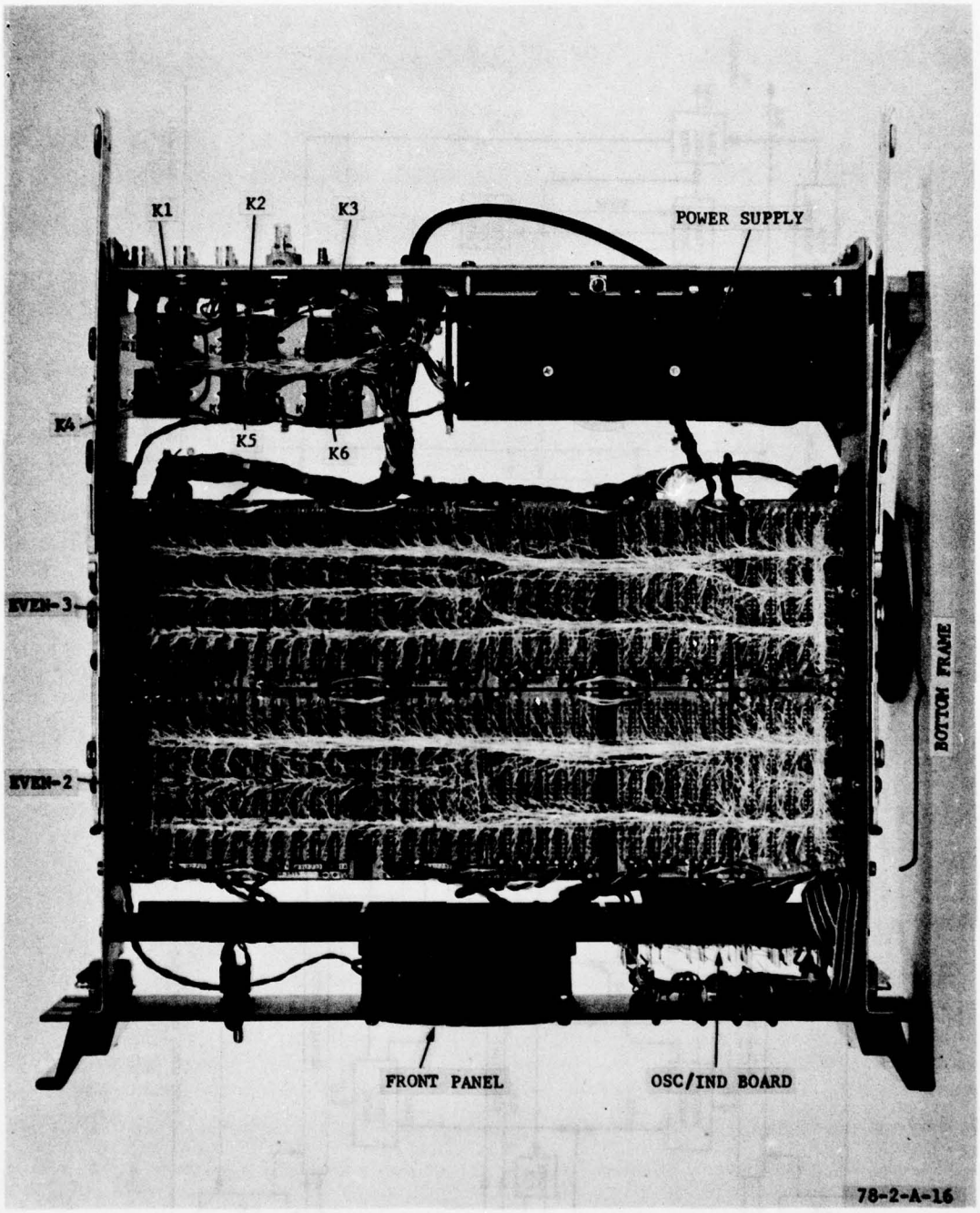


FIGURE A-16. SIX-RADAR DACOMP, BOTTOM VIEW WITH BOTTOM LEVEL CLOSED

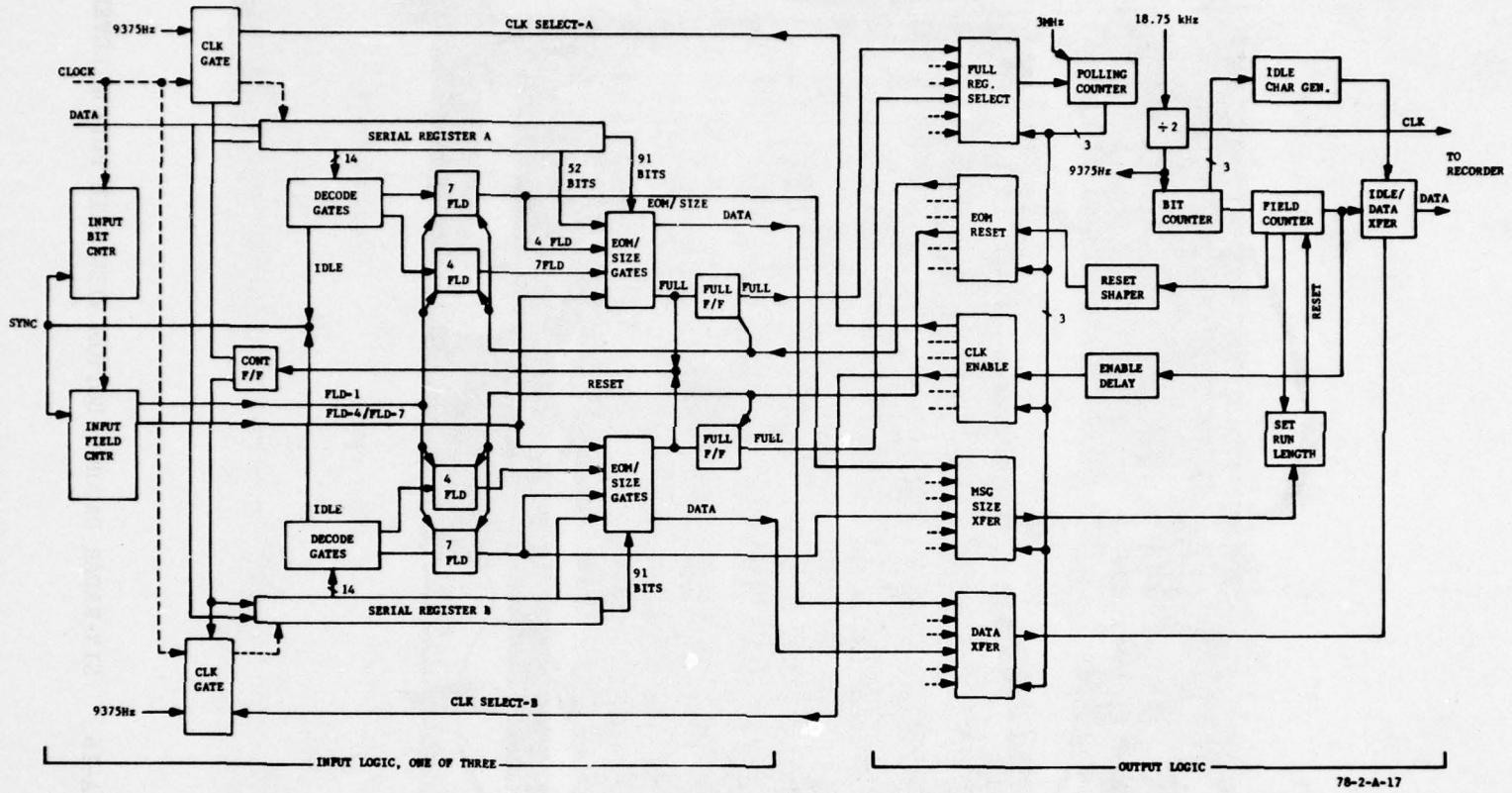


FIGURE A-17. DETAIL BLOCK DIAGRAM OF SINGLE DACOMP

TABLE A-1. DATA COMPRESSOR INTEGRATED CIRCUIT TYPES

Type	Description	Quantity per DACOMP Frame	FSN 5962
7414	Hex Schmitt Trigger	2	272-0132
	Sub: 74LS14		
74164	8-bit serial in-parallel out	24	
74L164	Register		
8162A	One-shot Multivibrator	2	104-1639
8230B	8 to 1 Multiplexer	3	478-4421
8250A	Octal Demultiplexer	6	247-9176
8280A	Decade Counter	1*	734-5394
	Sub: 74196N, 74LS196N		
8218A	4-stage Binary Counter	3 + 1*	734-5899
	Sub: 74197N, 74LS197N		
8284A	Sync Binary Counter	1	
8416A	Dual 4-in NAND Gate	6	734-5914
8440A	Dual and-or-Inv. Gate	9	734-5932
8706A	Dual 5-in Expander	6	734-6046
8808A	8-in. NAND Gate	1	734-6046
	Sub: 7430N, 74L30N, 74LS30N		927-1568
8822A	Dual J-K Flip-Flop	10	104-1660
8828A	Dual D Flip-Flop	6	734-6279
	Sub: 747N, 74LS74N		016-4287
8855A	Dual NAND Driver	4 + 1*	734-6285
8870A	Triple 3-in NAND Gate	1	734-6287
8880A	Quad 2-in NAND Gate	11	734-6288
8885A	Quad 2-in NOR Gate	8	104-1663
8890A	Hex Inverter	1	
	Sub: 7404N, 74L04N, 74LS04N		404-2559
9328	Dual 8-bit		
93L28	Serial-in Serial-out	24	
9328	Shift Register**		

Notes:

*Also used in master oscillator assembly, one per drawer.
**8328 and 9328 are used in older compressors; failed units should be replaced by 93L28's.

TABLE A-2. INTEGRATED CIRCUIT TYPE AND LOCATION TABLE REFERENCE FIGURE A-13

Location	Type	Location	Type
101	N8880A	21	N8230B
102	N8870A	22	MC8328, 93L28*
103	N8822A	23	MC8328, 93L28*
104	N8822A	24	SN74164N, 74L164*
15	N8808A, 7430, 74LS30*	25	MC8328, 93L28
16	SN74164N, 74LK64*	26	MC8328, 93L28*
107	N8162A	27	N8230B
108	N8281A, 74197, 74LS197*	28	MC8328, 93LA8*
109	N8250B	29	MC8328, 93L28*
110	N8822A	210	SN74164N, 74L164*
111	N8250B	211	MC8328, 93L28*
112	SN74164N, 74L164*	212	MC8328, 93L28*
113	Discrete Components	213	N8230B
114	N8162A	214	MC8328, 93L28*
115	N8885A	215	MC8328, 93L28*
116	N8822A	216	SN74164N, 74L164*
117	N8890A, 7474, 74L04*, 74LS04*	217	MC8328, 93L28*
118	N8250B	218	MC8328, 93L28*
119	Output Connector	41	N8880A
120	N8855A	42	N8880A
121	N8885A	43	N8828A, 7474, 74LS74*
122	N8880A	44	N8440A
123	N8440A	45	N8828A, 7474, 74LS74*
124	SN74164N, 74L164*	46	N8440A
31	SN74164N, 74L164*	47	N8440A
32	MC8328, 93L28*	48	N8880A
33	MC8328, 93L28	49	N8880A
34	SN74164N, 74L164*	410	N8706A
35	MC8328, 93L28*	411	N8885A
36	MC8328, 93L28*	412	N8885A
37	SN74164N, 74L164*	413	N8440A
38	MC8328, 93L28*	414	N8855A
39	MC8328, 93L28*	415	SN74164N, 74L164*
310	SN74164N, 74L164	416	N8416A
311	MC8328, 93L28	417	SN74164N, 74L164*
312	MC8328, 93L28*	418	N8885A
313	SN74164N, 74L164*	419	N8855A
314	MC8328, 93L28*	420	N8855A
315	MC8328, 93L28*	421	SN74164N, 74L164*
316	SN74164N, 74L164*	422	N8706A
317	MC8328, 93L28*	423	SN74164N
318	MC8328, 93L28*	424	N8822A
51	N8880A	61	N8828A, 7474, 74LS74*
52	N8828A, 7474, 74LS74*	62	N8440A
53	N8440A	63	N8828A, 7474, 74LS74*
54	N8828A, 7474, 74LS74*	64	N8440A
55	N8440A	65	N8880A
56	N8880A	66	Input Connector
57	N8250A	67	N8880A
58	N8880A	68	N8706A
59	N8706A	69	N8885A
510	N8885A	610	N8885A
511	N8885A	611	N8250A
512	N8250A	612	Input Clipper/Filter
513	N8281A, 74197, 74LS197*	613	SN74164N, 74L164*
514	SN74164N, 74L164	614	N8416A
515	N8416A	615	SN74164N, 74L164*
516	SN74164N, 74L164	616	SN74164N
517	N8416A	617	N8281A, 74197, 74LS197
518	N8281A, 74197, 74LS197*	618	SN7414N, 74LS14*
519	N8822A	619	SN74164N
520	SN74164N	620	N8706A
521	N8706A	621	SN74164N
522	SN74164N	622	N8822A
523	N8822A	623	N8822A
524	N8822A	624	SN7414N, 74LS14

*Preferred Replacements

TABLE A-3. DACOMP/FR-1800 TRACK ASSIGNMENTS

DACOMP Frame	Recorder Tracks Data	Clock	Comments
ODD-1	11	13	
ODD-2	7	9	
ODD-3	3	5	
EVEN-1	12	14	
EVEN-2	8	10	Not used with 4-radar drawer
EVEN-3	4	6	

TABLE A-4. DACOMP/VR-3700 OR SABRE 4 RECORDER TRACK ASSIGNMENTS

DACOMP Frame	Recorder Tracks Data	Clock	Comments
ODD-1	3	5	"A" Radar input
ODD-2	7	9	"C" Radar input
ODD-3	11	13	"D" Radar input
EVEN-1	17	19	"B" Radar input
EVEN-2	21	23	"E" Radar input
EVEN-3	25	27	"F" Radar input

TABLE A-5. SERIAL NUMBERS FOR DACOMP IN BATCH-3 DRAWERS

Drawer	ODD-1	EVEN-1	ODD-2	ODD-3	EVEN-2	EVEN-3
1	45	46	48	47	49	50
2	51	52	54	53	55	56
3	57	58	60	59	61	62
4	63	64	66	65	67	68
5	69	70	72	71	73	74
6	75	76	78	77	79	80
7	81	82	84	83	85	86
8	87	88	90	89	91	92
9	93	94	96	95	97	98
10	99	100	102	101	103	104
11	105	106	108	107	109	110
12	111	112	114	113	115	116

AD-A057 442 NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER ATL--ETC F/G 17/9
DIGITIZED RADAR DATA COMPRESSOR.(U)
JUL 78 E A MACK, A R MOSS

UNCLASSIFIED FAA-NA-78-2 FAA-RD-78-48 NL

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APPENDIX B

Data Compressor Test Techniques

LIST OF ILLUSTRATIONS

Figure		Page
B-1	Test Setup for Single Reader Input Channel Test	B-4
B-2	Test Setup for Testing all Three Radar Input Channels	B-5

GENERAL.

Testing of the data compressor (DACOMP) is done to verify that the device is accurately compressing each and every common digitizer (CD) message into the single high-speed channel. These techniques are used to isolate the trouble area in the DACOMP/recorder subsystem by a process of elimination of operational areas. Detailed troubleshooting is then done using the recorder manual or the DACOMP instructions. Testing of the subsystem need not be done as a periodic maintenance function, but always prior to its use on a recording mission or whenever any suspicion arises concerning the equipment reliability.

The DACOMP cannot operate with the data receiver group (DRG) directly without using the companion recorder. The DACOMP was designed to operate as a "front end" to an Ampex FR-1800, Bell & Howell VR-3700, or similar recorder. The reason for the incompatibility is that the DACOMP outputs are positive transistor-transistor logic (TTL) levels and the DRG requires bipolar signals. The recorder will accept TTL input levels and it's output levels are bipolar. Consequently, the recorder must be verified completely operational before any DACOMP testing is initiated. Section 3 below covers the recorder checkout, while section 4 concerns the DACOMP tests. The DACOMP referred to in these tests is a single compressor within the drawer capable of condensing one radar. Each drawer will contain either four or six DACOMP's. All input patching to each DACOMP is done through the recorder patch panel.

EQUIPMENT.

a. Three channels of digital CD data (one radar) and a recorder is minimum equipment configuration to satisfactorily check both the recorder and the DACOMP.

1. Data source: Three channels of live or test data from the monitor jack output of the receiver modems. These three channels need not be of the same radar, but should be verified error-free.

2. Recorder: One FR-1800 VR-3700, or similar recorder with all heads cleaned and degaussed and loaded with a degaussed scratch tape if necessary. All periodic maintenance should have been performed recently.

3. Data Receiver Group: A single channel is the minimum needed, but three channels representing (one radar) are preferred. This DRG should not be in use by the online NAS system. Several ARTCC's have DRG's installed for future radars which can be used. Optional test 4.b (3) below will need four DRG channels, all which must be accessible by the offline 9020 system.

4. Dual-channel oscilloscope. Two coaxial interconnecting cables will be needed each consisting of a 1/4-inch, two-conductor phone plug (PJ-47) on one end and a mating connector for the scope on the other. These will be used for the monitor jacks on the recorder front panel.

b. Additional Equipment

1. Offline 9020 Simplex: A CD preliminary equipment checkout (PECO) program (74B3) is utilized to check the incoming radar data for message rate and errors. Use the Quality Precheck option (/5.80000000/) an IBM 1403 printer is needed as the output device. Checking is done by comparing message totals on the line live data used for the test against those received from the DACOMP/ recorder. The totals will differ slightly for each 1-minute printout due to the time lag between record and playback heads in the recorder, but will begin to average out over several minutes. Any errors received on the live radar data should be reflected on the test data.

2. DACOMP Analyzer: A device which checks and displays the internal operation of the DACOMP to which it is connected. It also analyzes the DACOMP output for content and errors. It contains a CD data generator for the DACOMP inputs and is available at NAFEC on a limited loan basis.

TEST PROCEDURES.

a. FR-1800 Recorder Verification, Low Rate. This is a check of the record/ reproduce functions at the normal data rate of 2400 bits per second (b/s).

1. Conditions:

(a) Recorder: RECORD FORWARD modes

(b) Tape Speed: 3 - 3/4 inches per second (ips)

(c) Data Inputs: Live radar on all ODD channel inputs

(d) Input Switches: + position on all input modules (FR-1800 only)

(e) Scope: One input for clock, the other for corresponding data track as listed in table B-1. Use monitor jacks on recorder front panel.

2. Check

(a) Input and Output Levels: Logic one +5 V $\pm$1 V
Logic zero -5 V $\pm$1 V

(b) Clock phase: Positive-going edge of clock at data change time.

(c) Output pulse jitter: Scope sync on one edge of signal and deviation (jitter) of other edge measured. Jitter: 20 µs approximately.

3. Repeat above conditions and checks using live radar on all EVEN channel inputs.

TABLE B-1 CLOCK AND DATA TRACK ASSIGNMENTS

Channel	ODD		EVEN	
	Clock	Data	Clock	Data
1	13	11	14	12
2	9	7	10*	8*
3	5	3	6*	4*

*No data present if site has four DACOMP drawer in test b (1).

b. FR-1800 Recorder Verification, High Rate. This is a check of the record/reproduce operation at 9375 (b/s) using the clock and IDLE character output of the DACOMP.

1. Conditions:

(a) Recorder: RRECORD FORWARD mode

(b) Tape Speed: 7-1/2

(c) Data Input: DACOMP on without any data applied to its inputs.

(d) Input Switches: + position (FR-1800 only)

(e) Scope: as in test a (1) (e) above. Note tracks 4, 6, 8, and 10 will not have signals if site has a four-DACOMP drawer.

2. Check

(a) Input levels: Logic one +3.5 to 5 V
Logic zero 0 V to +0.5 V

(b) Output levels: Logic one +5 V $\pm$1 V
Logic zero -5 V $\pm$1 V

(c) Clock phase: positive-going edge at data change time

(d) Output pulse jitter: 10 µs approximately.

3. Additional Check: Recorder outputs patched into DRG. The following DRG channel indicators should be out: Clk. sync (alarms), IDLE-1, IDLE-2, FLDS. No targets on RAPPI for the DRG.

4. Faults: If a good IDLE cannot be obtained from the DACOMP, a problem is with its output bit and field counters. If excessive jitter is noted, a realignment of the recorder is necessary.

DACOMP CHECK.

a. Single Channel Input. Application of live data to DACOMP-under-test. One DACOMP input channel at a time.

1. Conditions

(a) Recorder: RECORD FORWARD modes

(b) Tape Speed: 7-1/2 ips

(c) Data Input: Patch a live radar channel in the channel 1 input of the DACOMP. See figure B-1.

(d) Recorder Output: DACOMP/recorder output patched into DRG channel.

2. Check (a) DRG alarms: sync, clk fail out.

(b) DRG indicators: IPE, FLDS, IDLE-1, and IDLE-2 are out.

(c) RAPPI display: no targets should fall outside of the of the antenna rotation pattern.

3. Additional Check: Address the CD adapters of the DRG being used with the offline 9020. See 2b(1) above for program. The message counts of the live channel and the channel from the DACOMP/recorder should closely match without additional errors.

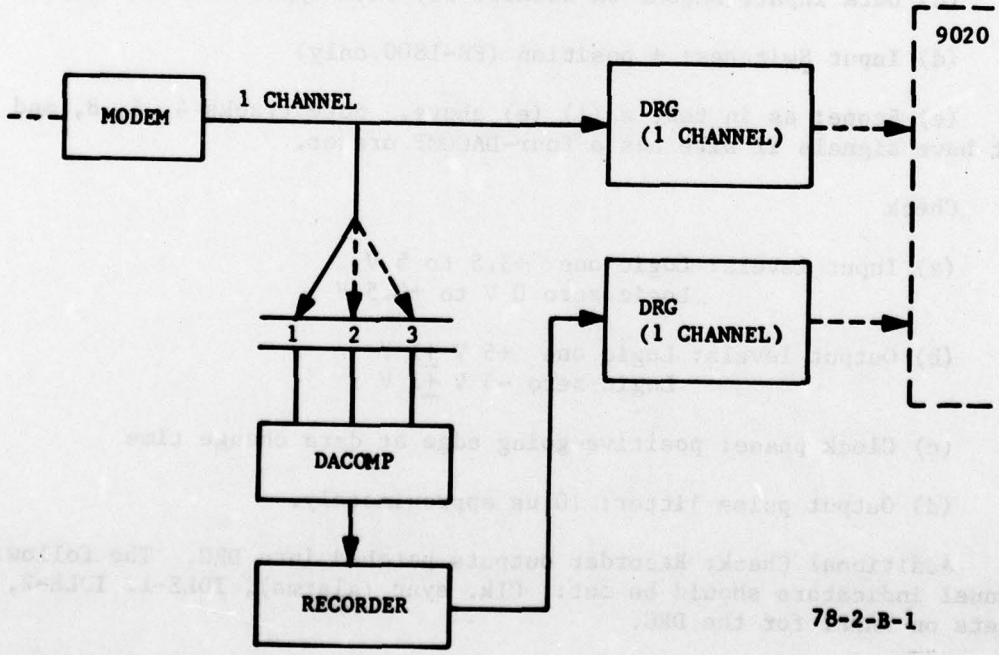


FIGURE B-1. TEST SETUP FOR SINGLE READER INPUT CHANNEL TEST

4. Repeat above conditions and checks with the live channel patched into the channel 2 input of the DACOMP unit under test. Do the same for the channel 3 input.

5. Faults. If the check points do indicate errors in the compressed data for one of DACOMP inputs, but the other two are satisfactory, then the fault has been isolated to the input logic for that channel of that DACOMP, and more detailed troubleshooting is necessary. If each of the three channels shows errors, the problem lies in the output logic of that DACOMP. In either case, detailed trouble shooting now is required, and is beyond the scope of this section.

NOTE: If random access plan position indicator (RAPPI) shows a XX symbol at due north when testing a particular DACOMP input channel, one of the shift registers has opened up in that input logic and can be quickly found by scope-checking of both register chains.

b. Full Input Check

1. Conditions: Identical to 4a(1) above except:

(a) Data Inputs: All three DACOMP inputs with live radar (figure B-2).

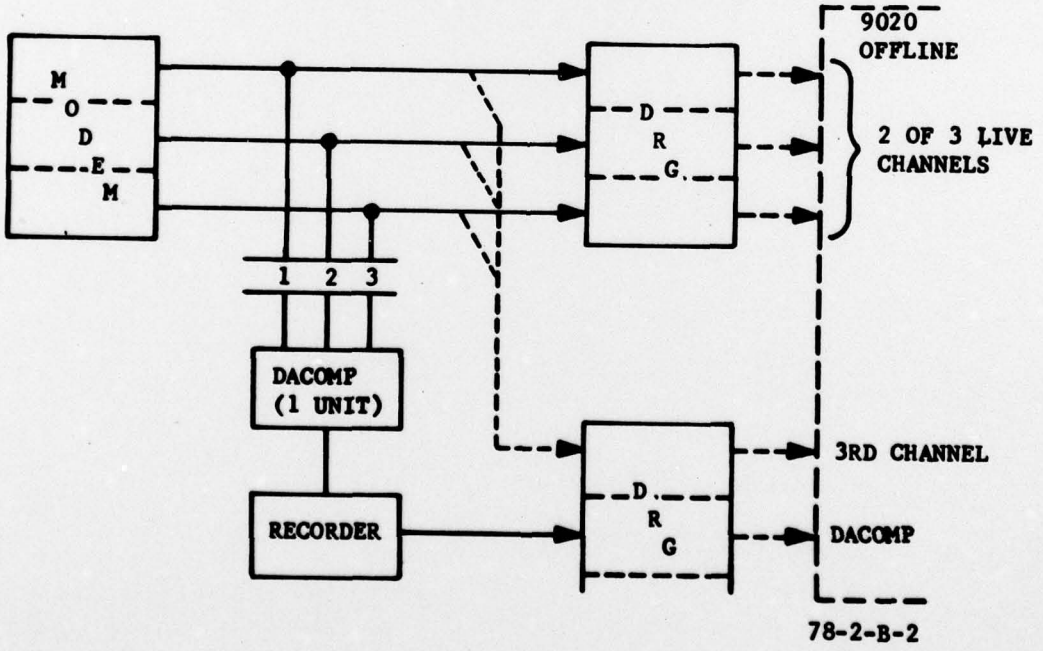


FIGURE B-2. TEST SETUP FOR TESTING ALL THREE RADAR INPUT CHANNELS

2. Check: Add in 4a(2) above.

3. Additional Check: As in 4a(3) above except all three channels of the live radar being used must be made accessible to the offline 9020. Usually two of the three channels are normally accessible in a offline Simplex and the other channel will have to be parallel patched over to an offline-accessible DRG channel. If an uncommitted DRG is available and it is cabled to the 9020, it can be utilized as the third channel input and the compressed data path.

4. Fault. If errors show up in this check and not in the previous single-channel checkout at the DACOMP, repeat test 4a again. If same results occur, the problem is probably an overload of the compresser due to extremely high target densities in the radar scan. The DACOMP output clock (9375 kHz) will have to be increased to 12 kHz. Modification to the master oscillator assembly on the front panel will have to be made locally to divide the 3-MHz oscillator signal by 125. This will provide a 24-kHz clock to the DACOMP's which is again divided by two for 12 kHz.