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DEVELOPMENT OF TECHNOLOGIES AND PROCEDURES FOR ADVANCED MICROCI--ETC(U)

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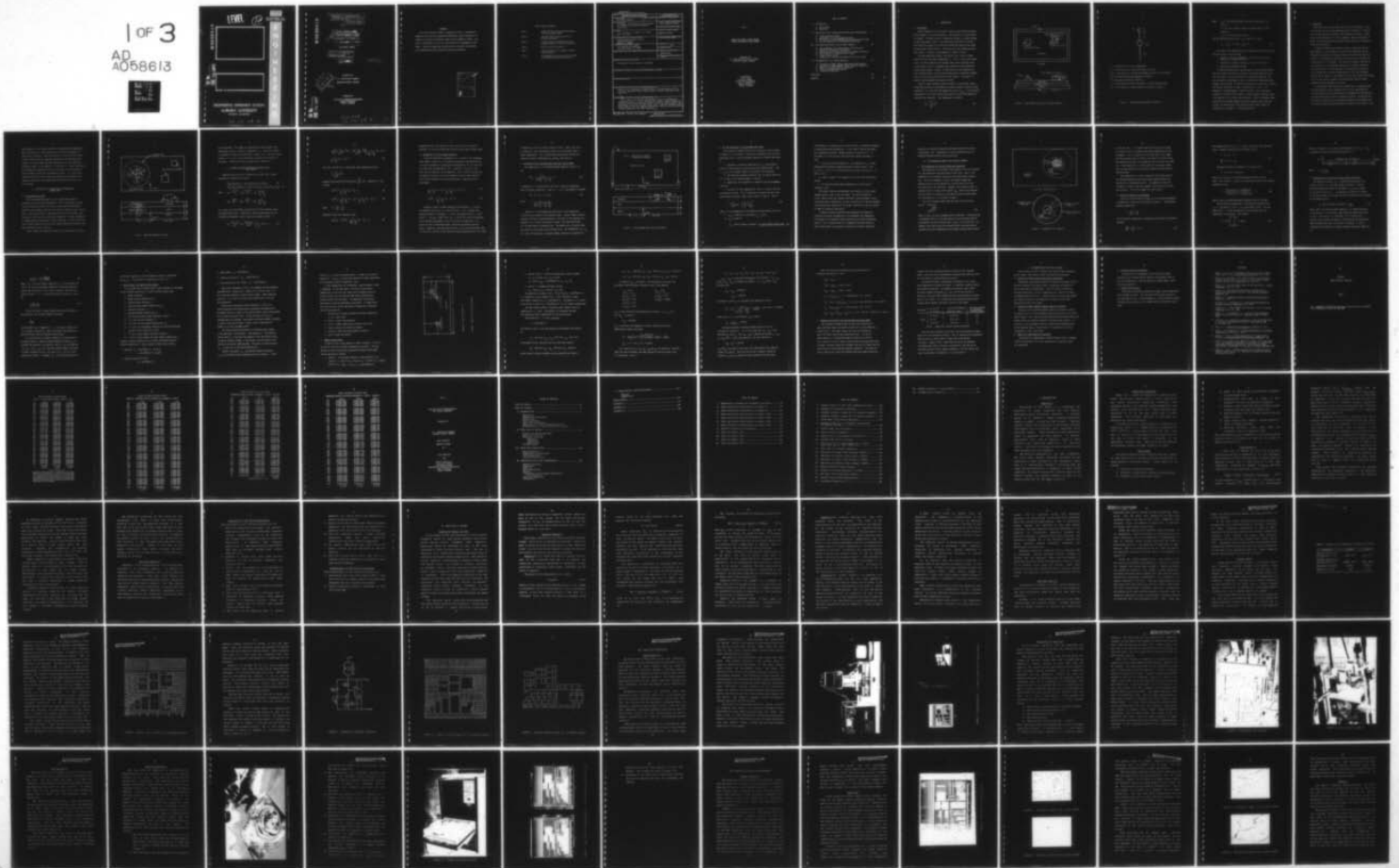
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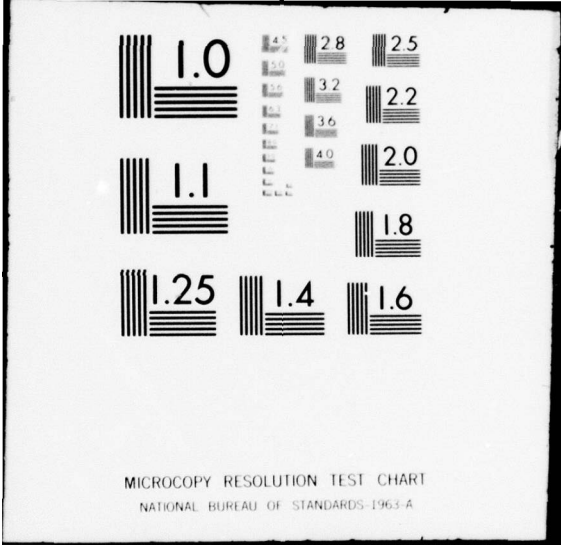
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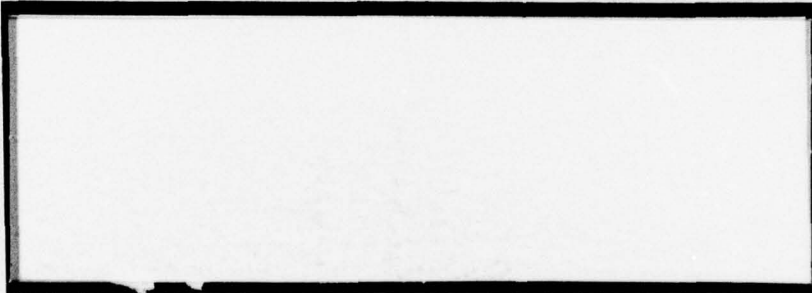
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6 Development of Technologies and Procedures for Advanced Microcircuit Prototype Fabrication.

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9 FINAL TECHNICAL REPORT.

15 Contract DAAK40-77-C-0042

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D. V./Kerns and T. D./Slagh

Co-Project Leaders

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Prepared for  
U. S. Army Missile Command  
Redstone Arsenal, Alabama

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FOREWORD

This final technical report is submitted to the U.S. Army Missile Command by the Electrical Engineering Department, Auburn University, to complete its contract obligations under contract DAAK40-77-C-0042. This report is published in six parts, each separate and independent of the others. Each part summarizes significant work related to the contract tasks completed during the period of contract performance.

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Circuit Boards and Hybrid Substrates

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20 ABSTRACT (Continue on reverse side if necessary and identify by block number) This report investigates the problems involved in implementing integrated circuits. Its six separate parts address hybrid integration, computer-aided thermal modeling, thermal simulation, thermal analysis and measurement, thick film resistor noise, noise in optical isolators, auto- mated conductor routing, computer aided design, thin-film microcircuits on flexible substrates, and logic simulation. ↙		

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Part 1

SIMPLIFIED HYBRID SYSTEM THERMAL  
MODELS FOR DEVICE LAYOUT DESIGN

Prepared for  
U.S. Army Missile R and D Command  
Redstone Arsenal, Alabama

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## I. INTRODUCTION

### A. The Problem

Hybrid integrated circuits usually contain several heat dissipating devices bonded to a ceramic substrate. The substrate is in turn bonded to a header. The whole system is completely enclosed in a metal package, of which the header is part. The primary heat flow path is from the heat generating regions of the devices through the substrate and header to the external header surface. This heat also flows through any epoxy bond regions. A typical system geometry is shown in Figure 1.

The heat generating region of the devices will rise to a higher temperature than the header temperature,  $T_c$ . This is due to two reasons. First, the device generates its own heat power which ultimately flows to the header, causing a temperature drop between the heat generating region and the header. Second, if other devices on the substrate are also dissipating heat, then the device experiences an additional temperature rise due to the proximity of the other devices. Thus there is thermal coupling between the devices involved.

Figure 2 shows a thermal resistance model for a particular device. A detailed discussion of the thermal resistance concept is given by Slagh and Ruwe [1, 2]. Note that the temperature source,  $T_{cp1_i}$  is the increased temperature of this device due to the presence of other heat generating devices on the substrate. This temperature is given by

$$T_{cp1_i} = \sum_{\substack{j=1 \\ j \neq i}}^N \theta_{ij} P_j \quad (1)$$

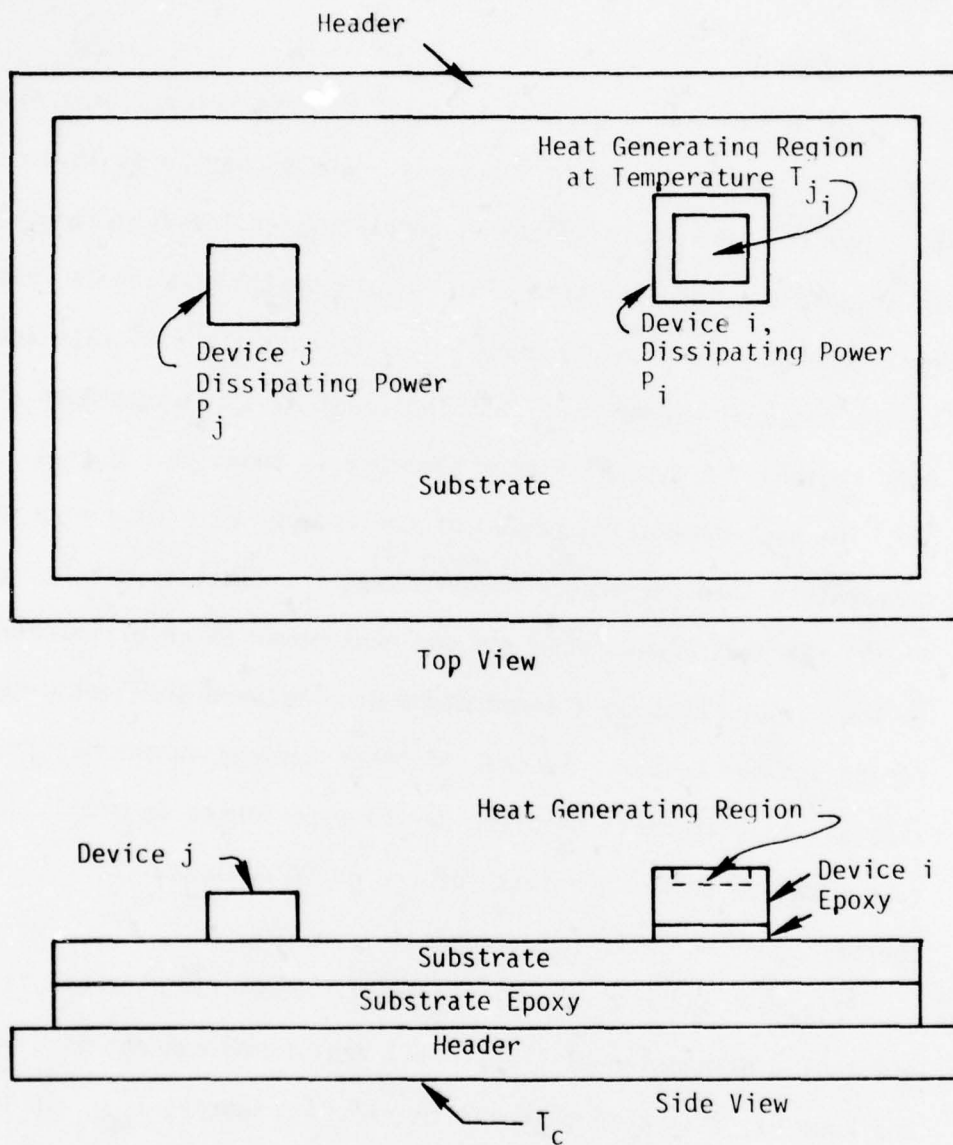
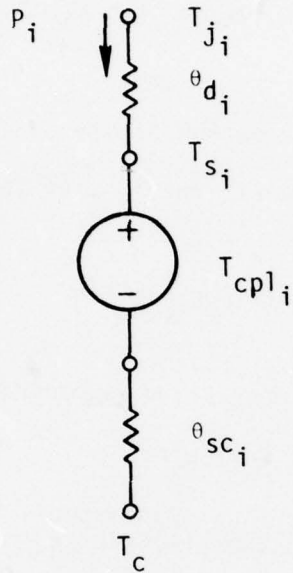


Figure 1. Basic Hybrid Structure for Thermal Analysis.



$T_c$  is the header lower surface temperature.

$T_{s_i}$  is the mid-substrate temperature under the device.

$T_{cpl_i}$  is the portion of the substrate temperature due to other devices.

$T_{j_i}$  is the heat generating temperature of device  $i$ .

$P_i$  is the power dissipation of device  $i$ .

$\theta_{d_i}$  is the thermal resistance from device  $i$  to mid-substrate layer.

$\theta_{sc_i}$  is mid-substrate to header thermal resistance for device  $i$ .

Figure 2. Thermal Resistance Model for Device  $i$ .

where  $\theta_{ij}$  is the coupling thermal resistance from device j to device i

N is the total number of heat dissipating devices on the substrate

$P_j$  is the dissipation of device j

The heat generating temperature,  $T_{j_i}$ , of device i is then

$$T_{j_i} = T_{cpl_i} + P_i (\theta_{d_i} + \theta_{sc_i}) + T_c \quad (2)$$

At excessive heat generating region temperatures devices may suffer from one or more of the following:

1. Change of electrical parameters, to the point that circuit operation is unsatisfactory [3].
2. A drastically lowered lifetime until device failure [4].
3. Immediate catastrophic failure.

It becomes important then, that the hybrid circuit design engineer and layout technician be able to predict the maximum temperatures that will be reached in the various devices on the hybrid substrate. One may use numerical techniques to solve, in effect, the three-dimensional boundary value problem. The desired information will be gained, including the thermal resistances of Figure 2 and Equations 1 and 2. This approach is disadvantageous for several reasons. First, the hybrid structure is generally quite complex. Second, boundary conditions need to be applied at all surfaces and interfaces. Third, the engineer and/or technician are probably unfamiliar with the necessary heat flow laws. Fourth, the subdividing of the system into small nodal volumes for simulation on a computer is a time consuming task.

## B. Objectives

There were two principal objectives for the investigation. First, is to develop an accurate two-dimensional heat flow model as a simplification of the previously mentioned three-dimensional problem. Second, by the further assumption of circular symmetry, thermal resistances of devices and coupling thermal resistances between devices are obtained in closed-form expressions.

For hybrid systems with alumina or beryllia substrates that are epoxy bonded to a kovar header, the system three-dimensional partial differential equation with interface boundary conditions has been simplified to a two-dimensional equation at the mid-substrate surface with insignificant loss of accuracy. This means that computer solutions by such methods as finite-difference techniques are greatly simplified. The simplification is manifested both in characterizing a particular circuit layout with a solution algorithm and in the time and memory required by the computer. Since hybrid circuit layouts invariably possess little if any physical symmetry, this method makes complex thermal problems much more adaptable to solution.

By the further simplification of assuming that a rectangular heat dissipating device on the substrate surface can be represented by a circular shaped device of the same area, the temperature distribution on the substrate has been found in closed-form solution. By applying the principle of superposition, the substrate temperature distribution can be found when many dissipating devices are present on the surface. This

method leads to a very rapid calculation of maximum device temperatures that can be made by a layout technician with the aid of mathematical tables and a calculator. While the accuracy of this simplified method is not as high as the full computer simulation of the two-dimensional problem, it is much higher than many methods, such as the "spreading resistance" model, in use today [5]. In addition, it allows determination of the additional temperature rise of a device due to the proximity of other dissipating devices on the substrate surface. It is felt that a simplified algorithm of this type could readily be incorporated into a computer aided design system where other than thermal criteria are to be considered.

## II. DERIVATION OF THE SIMPLIFIED TWO-DIMENSIONAL THERMAL MODEL

### A. Three-Dimensional Model

The three-dimensional hybrid circuit system thermal model is described in terms of nodal conductances. This is equivalent to using finite-difference equations for solution of the partial-differential equations with boundary conditions that describe conductive heat flow [2]. That is, the system volume is subdivided into very small volumes, each containing a node point at a particular temperature. Thermal conductance  $G$  between adjacent node points is easily expressed. As the size of the small volumes approach zero (with their number approaching infinity), the model approaches perfect accuracy.

Figure 3 shows the conductance layout for a surface area,  $\Delta x$  by  $\Delta y$ ,

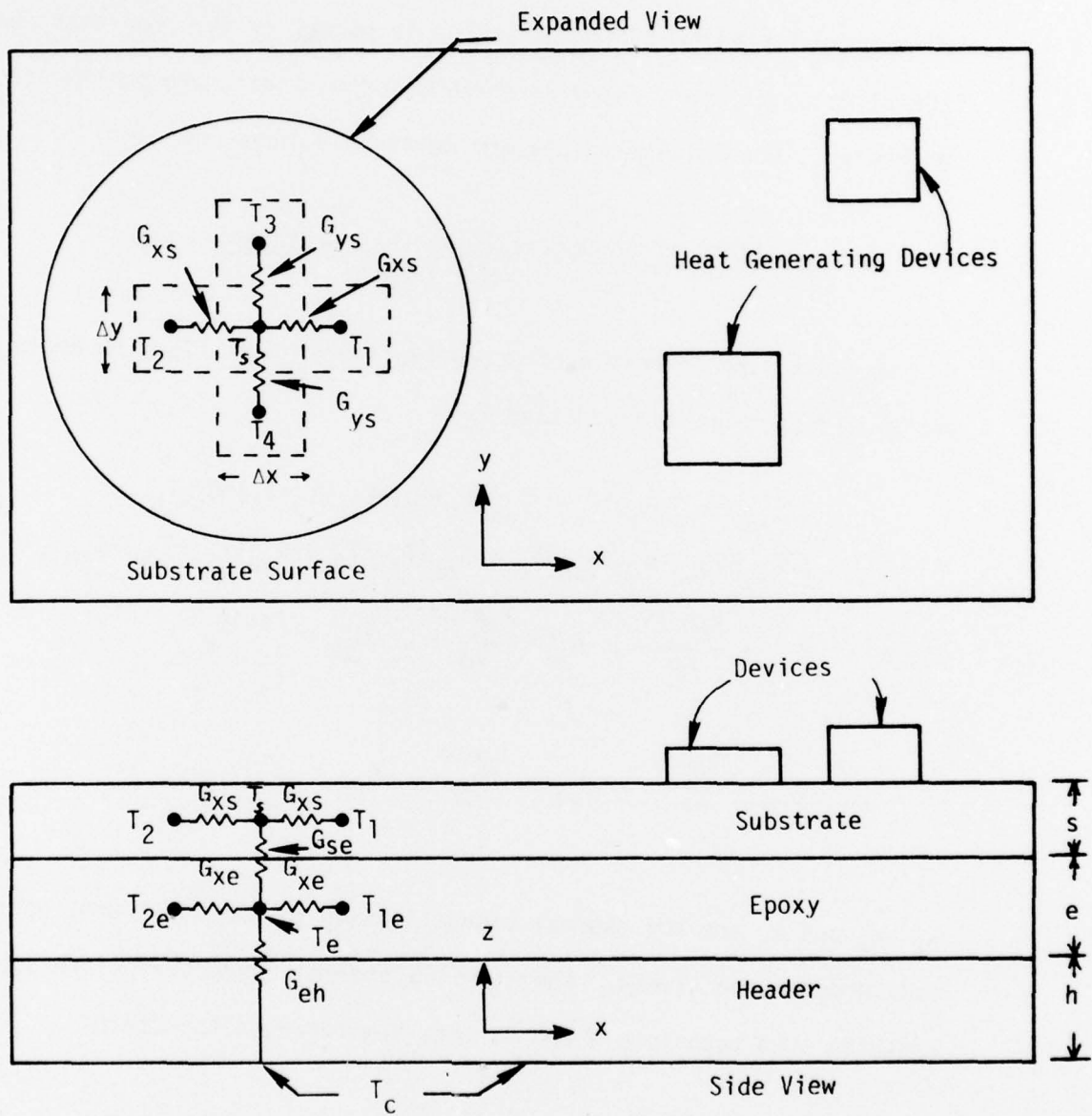


Figure 3. Node and Conductance Layout

on the substrate. Also shown are conductances extending down to the lower header surface, sinked at a temperature  $T_c$ . Since this surface is isothermal, the heat flow direction is normal to it. For this reason, lateral (i.e. in the x and y directions) conductances are omitted in the header. Conductance values are determined in general by

$$G = \frac{(\text{thermal conductivity}) \times (\text{cross-sectional area})}{\text{path length}}$$

Applying the principle of "conservation of heat flow" to nodes designated by temperatures  $T$  and  $T_e$ :

$$(2G_{xs} + 2G_{ys} + G_{se})T_s = G_{xs}(T_1 + T_2) + G_{ys}(T_3 + T_4) + G_{se}T_e \quad (3)$$

$$(2G_{xe} + 2G_{ye} + G_{se} + G_{eh})T_e = G_{xe}(T_{1e} + T_{2e}) + G_{ye}(T_{3e} + T_{4e}) + G_{se}T_s + G_{eh}T_c \quad (4)$$

where

$$G_{xs} = \frac{k_s s \Delta y}{\Delta x}, \quad G_{ys} = \frac{k_s s \Delta x}{\Delta y}, \quad G_{se} = \frac{2\Delta x \Delta y}{\frac{s}{k_s} + \frac{e}{k_e}}$$

$$G_{xe} = \frac{k_e e \Delta y}{\Delta x}, \quad G_{ye} = \frac{k_e e \Delta x}{\Delta y}, \quad G_{eh} = \frac{\Delta x \Delta y}{\frac{e}{2k_e} + \frac{h}{k_h}}$$

$k_s$ ,  $k_e$  and  $k_h$  are the thermal conductivities of the substrate, epoxy and header respectively. When the six thermal conductances are substituted into Equations 3 and 4, they are arranged to obtain

$$k_s s \frac{T_1 + T_2 - 2T_s}{(\Delta x)^2} + k_s s \frac{T_3 + T_4 - 2T_s}{(\Delta y)^2} + \frac{2}{\frac{s}{k_s} + \frac{e}{k_e}} (T_e - T_s) = 0 \quad (5)$$

$$k_e e \left[ \frac{T_{1e} + T_{2e} - 2T_e}{(\Delta x)^2} + \frac{T_{3e} + T_{4e} - 2T_e}{(\Delta y)^2} \right] + \frac{1}{\frac{e}{2k_e} + \frac{h}{k_h}} (T_c - T_e) + \frac{2}{\frac{s}{k_s} + \frac{e}{k_e}} (T_s - T_e) = 0 \quad (6)$$

The limit  $\Delta x \rightarrow 0$  and  $\Delta y \rightarrow 0$  is then taken, where expressions such as

$$\frac{T_1 + T_2 - 2T_s}{(\Delta x)^2}$$

approach the second partial derivative,  $\frac{\partial^2 T_s}{\partial x^2}$ , etc. Equations 5 and 6 become

$$k_s s \nabla^2 T_s + \frac{2}{\frac{s}{k_s} + \frac{e}{k_e}} (T_e - T_s) = 0 \quad (7)$$

$$k_e e \nabla^2 T_e + \frac{1}{\frac{e}{2k_e} + \frac{h}{k_h}} (T_c - T_e) + \frac{2}{\frac{s}{k_s} + \frac{e}{k_e}} (T_s - T_e) = 0 \quad (8)$$

where  $\nabla^2 = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}$

Equations 7 and 8 are combined to give

$$k_e e \nabla^2 T_e + k_s s \nabla^2 T_s + \frac{1}{\frac{e}{2k_e} + \frac{h}{k_h}} (T_c - T_e) = 0 \quad (9)$$

Equations 8 and 9 then become the controlling partial differential equations for the three-dimensional substrate-epoxy-header thermal model.

#### B. Assumptions for Epoxy Bonded Substrates

The point designated by temperature  $T_e$  is nearer to the isothermal lower header surface than is the point designated by the temperature  $T_s$ . It is thus reasonable to assume that the magnitude of  $\nabla^2 T_e$  is certainly no larger than the magnitude of  $\nabla^2 T_s$ . Therefore, if  $k_e e \ll k_s s$ , the first term of Equation 9 can be neglected. Also, since the second term of Equation 8 and the last term of Equation 9 are the same, then the first term of Equation 8 can also be neglected. Equations 8 and 9 then become

$$\frac{1}{\frac{e}{2k_e} + \frac{h}{k_h}} (T_c - T_e) + \frac{2}{\frac{s}{k_s} + \frac{e}{k_e}} (T_s - T_e) = 0 \quad (10)$$

$$k_s s \nabla^2 T_s + \frac{1}{\frac{e}{2k_e} + \frac{h}{k_h}} (T_c - T_e) = 0 \quad (11)$$

Consider a typical alumina substrate with thickness,  $s = 25$  mils, and thermal conductivity,  $k_s = 6 \times 10^{-4}$  W/mil-°C. This is bonded with conductive epoxy of thickness,  $e = 5$  mils, and conductivity,  $k_e = 4 \times 10^{-5}$  W/mil-°C. Thus  $k_e e = 2 \times 10^{-4}$  W/°C,  $k_s s = 1.5 \times 10^{-2}$  W/°C and the assumption of the preceding paragraph is valid. For beryllia substrates,  $k_s$  is almost an order of magnitude higher, making the assumption even more valid. Physically, this means that lateral (x and y directions) heat flow is essentially confined to the substrate only, and neglecting the first terms

of Equations 8 and 9 will lead to almost no error. What little error is present will cause conservative results to be predicted; that is higher temperatures. This is because the approximation effectively removes the lateral conductances  $G_{xe}$  and  $G_{ye}$  (see Figure 3).

C. Derivation of the Two-Dimensional Substrate Surface Model

The temperature  $T_e$  is eliminated between Equations 10 and 11 to give

$$\nabla^2 T_s - \frac{T_s - T_c}{k_s s \left( \frac{s}{2k_s} + \frac{e}{k_e} + \frac{h}{k_h} \right)} = 0 \quad (12)$$

A temperature  $T$  is now defined as the rise in substrate temperature above the header temperature. That is,  $T = T_s - T_c$ , and Equation 12 becomes

$$\nabla^2 T - \lambda^2 T = 0; \quad T = T(x, y) \quad (13)$$

where

$$\lambda = \frac{1}{\sqrt{k_s s \left( \frac{s}{2k_s} + \frac{e}{k_e} + \frac{h}{k_h} \right)}}$$

Equation 13 is two-dimensional and applies to the temperature variation at the middle of the substrate layer. Figure 4 shows a typical substrate with heat dissipating devices. The edges of the substrate are adiabatic (i.e. no heat flow normal to them). The normal derivative of  $T$  at these edges is therefore zero. The shaded area is directly below the devices in the middle of the substrate area. The temperatures  $T_{s_i}$ ,  $T_{s_j}$  etc., also of these areas, represent boundary conditions for Equation 13.

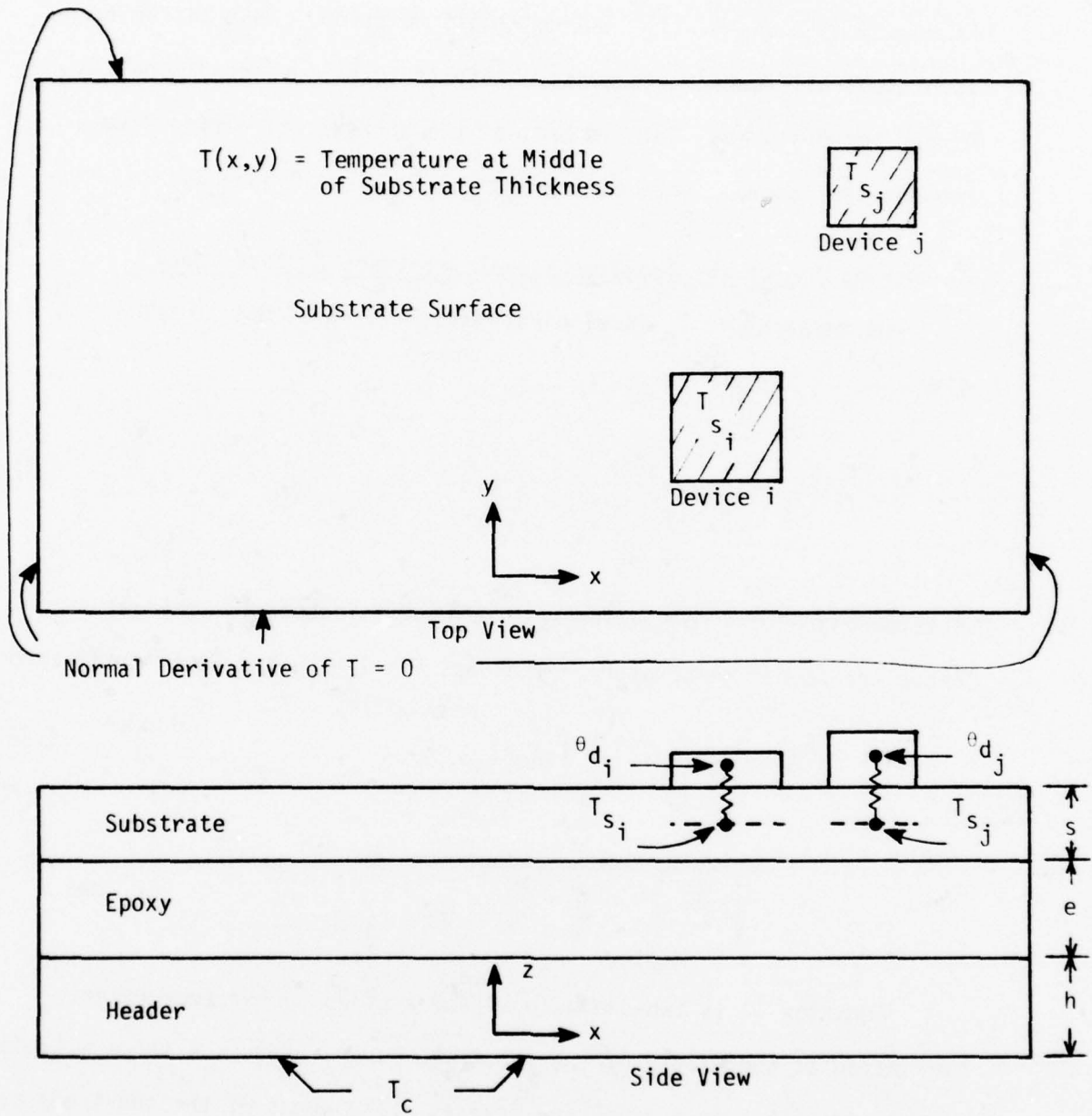


Figure 4. The Two-Dimensional Heat Flow Problem.

#### D. Use and Advantages of the Two-Dimensional Model

While numerical methods [6] are still necessary for the solution of Equation 13, the problem is simplified considerably from the three-dimensional case. A typical procedure would be as follows (see Figure 4):

1. Designate a convenient temperature for  $T_{s_i}$ , below device  $i$ . Assume all other devices are passive and do not generate heat. Then  $T = T_{s_i} - T_c$  at the shaded region in the middle of the substrate.
2. The additional boundary condition, that the normal derivative of  $T$  is zero at the substrate edges, is applied.
3. Numerically solve Equation 13, subject to the above boundary conditions.
4. Evaluate the total downward heat flow,  $P_i$  in watts, from the mid-substrate surface. This is equivalent to summing the heat flows down through incremental areas  $\Delta x \Delta y$  as shown in Figure 3. That is

$$P_i = \sum_{\text{All areas } \Delta x \Delta y} \left[ \frac{T}{\frac{1}{G_{se}} + \frac{1}{G_{eh}}} \right] \quad (14)$$

where  $T$  is the temperature at the middle of the particular area,  $\Delta x \Delta y$ .

5.  $\theta_{sc_i}$  in Equation 2 is given by  $(T_{s_i} - T_c)/P_i$
6.  $\theta_{d_i}$  is given by

$$\theta_{d_i} = \text{device thermal resistance} + \frac{s}{2k_s(\text{device base surface area})} \quad (15)$$

If the device is a transistor, IC or resistor chip, its thermal resistance is often given by the manufacturer. If not, then it can be calculated by a "spreading resistance" formula discussed in Section III C. If the device is a film resistor, then the device thermal resistance is zero.

7. From the solution obtained in 3, the temperature  $T_{s_j}$  is noted along with the substrate temperature below all other devices. Then  $\theta_{ji} = (T_{s_j} - T_c)/P_i$  is the coupling thermal resistance from device  $i$  to device  $j$ , etc.

8. Steps 1 through 7 are repeated for all other heat dissipating devices.

9. All heat generating region temperatures are then given by Equations 1 and 2.

The thermal solution outlined above can be done as a final system thermal analysis, that is quite accurate. This does not help the circuit layout technician, however, who needs a quicker method of calculating peak device temperatures, as well as guidelines for device placement. The two-dimensional problem will be further simplified in the next section in order to accomplish these goals.

It should be further noted that the temperature distribution  $T$ , given by the solution of Equation 13 also represents the temperature on the top of the substrate surface; except directly under dissipating devices. This is because there is no temperature gradient normal to this surface; which is equivalent to saying that internal conduction,

convection or radiation through the enclosed nitrogen filled space is negligible [7,8]. Temperatures of non-dissipating devices are therefore obtained directly from the solution.

### III. ONE-DIMENSIONAL MODEL USING CIRCULAR SYMMETRY

#### A. The Assumptions of Circular Devices and Substrates

Two assumptions are now made so that Equation 13 can be converted to a one-dimensional characterization of heat flow. That is, the temperature  $T$  will become a function of the radial space variable  $r$  only. The first assumption is that a rectangular shaped heat generating device can be modeled as a circular device, with the same base area on the substrate. Secondly, the substrate itself is assumed circular in shape, with a radius  $R_{o_i}$  equal to the distance from the center of the device to the nearest actual substrate edge. This configuration is illustrated in Figure 5.

The first assumption means that the radius of the circular device  $i$  is given by

$$r_{o_i} = \sqrt{\frac{a_i b_i}{\pi}} \quad (16)$$

where  $a_i$  and  $b_i$  are the rectangular device dimensions. Characterizing a rectangular device in this way should give quite accurate results provided that the device aspect ratio,  $(a_i/b_i)$ , is not too high. For example; with aspect ratios not exceeding three, the actual device periphery and the circumference of the assumed circular device differ

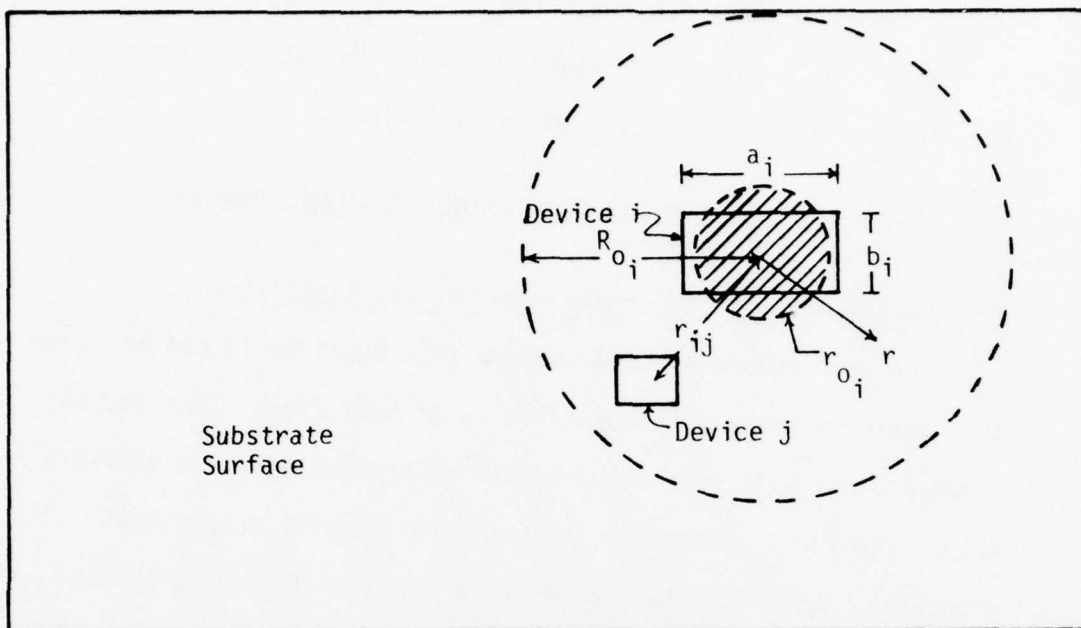


Figure 5a. Device Geometry

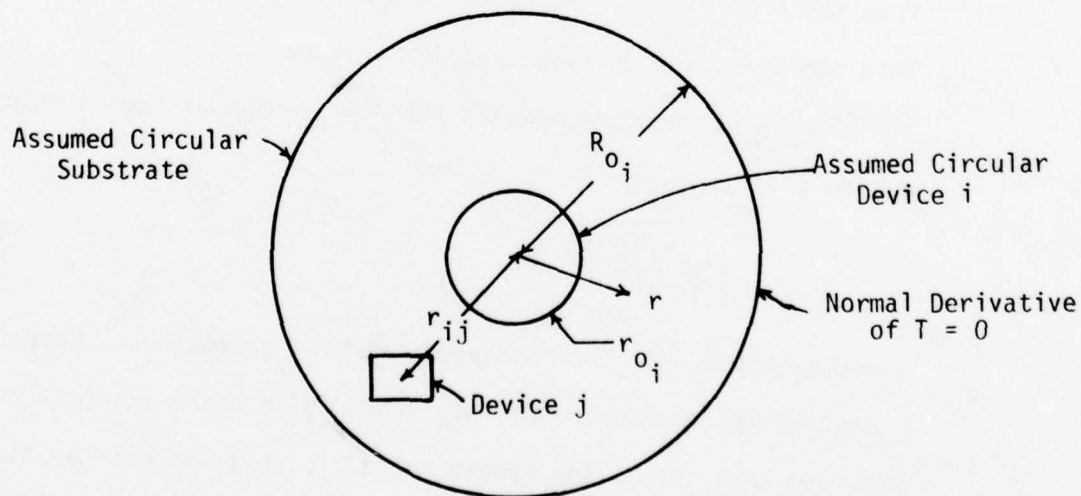


Figure 5b. Assumed Circular Symmetry

by less than 30%. It is probable that the circular device model will tend to predict a slightly lower device temperature than the rectangular. This is because the circle area that is not common with the rectangle area is closer to the center of the device than the rectangle area that is not common to the circle area (see Figure 5a.). The assumption of a circular model for rectangular shapes has also been employed by Ellison [9], though his results apply to hybrid packages.

The assumption of a circular substrate, with radius equal to the distance between the device and actual substrate edge, will obviously give conservative results. In comparison to the "45° spreading resistance" model [2], however, the results will be much more accurate. This will be shown in a later section.

#### B. Substrate Temperature Distribution

Using the circular model of Figure 5b, the substrate temperature  $T$  becomes only a function of the spatial variable  $r$ . The Laplacian operator becomes [10]

$$\nabla^2 = \frac{d^2}{dr^2} + \frac{1}{r} \frac{d}{dr}$$

and the substrate temperature is governed by the ordinary differential equation:

$$\frac{d^2 T}{dr^2} + \frac{1}{r} \frac{dT}{dr} - \lambda^2 T = 0 \quad (17)$$

This equation applies for  $r_0 \leq r \leq R_0$  for a particular heat generating device. Boundary conditions are (see Figure 4 also):

$$T = T_s \quad \text{at} \quad r = r_0$$

$$\frac{dT}{dr} = 0 \quad \text{at} \quad r = R_0$$

(18)

The general solution of Equation 17 is given by [11]:

$$T = C_1 I_0(\lambda r) + C_2 K_0(\lambda r)$$

(19)

where  $I_0(\lambda r)$  and  $K_0(\lambda r)$  are modified Bessel functions of 0th order. The constants,  $C_1$  and  $C_2$ , are evaluated by applying the boundary conditions to give:

$$T = \frac{K_1(\lambda R_0) I_0(\lambda r) + I_1(\lambda R_0) K_0(\lambda r)}{K_1(\lambda R_0) I_0(\lambda r_0) + I_1(\lambda R_0) K_0(\lambda r_0)} T_s$$

(20)

where  $I_1$  and  $K_1$  are modified Bessel functions of the first order.

The mid-substrate temperature is then given by Equation 20 for  $r_0 \leq r \leq R_0$  and by  $T_s$  for  $0 \leq r \leq r_0$  (see Figure 4 also). The heat power flow  $P$  is given by Equation 14, with the summation sign replaced by an integration. This becomes:

$$P = k_s s \lambda^2 \int_{\phi=0}^{2\pi} \int_{r=0}^{R_0} T r dr d\phi$$

(21)

When this integration is carried out the temperature  $T_r$  for  $r_0 \leq r \leq R_0$ , is obtained in terms of the device dissipation  $P$  as:

$$\frac{T}{P} = A \left\{ \frac{K_1(\lambda R_0) I_0(\lambda r) + I_1(\lambda R_0) K_0(\lambda r)}{K_1(\lambda R_0) \left[ \frac{r_0}{2} I_0(\lambda r_0) - \frac{1}{\lambda} I_1(\lambda r_0) \right] + I_1(\lambda R_0) \left[ \frac{r_0}{2} K_0(\lambda r_0) + \frac{1}{\lambda} K_1(\lambda r_0) \right]} \right\} \quad (22)$$

where  $A = \frac{1}{2\pi k_s \lambda^2 r_0}$

### C. Determination of Device and Coupling Thermal Resistances

The thermal resistance  $\theta_{sc}$  is obtained from Equation 22 by setting  $r$  equal to  $r_0$ . The total thermal resistance  $\theta$  from the device heat generating region to the header is  $\theta_{sc}$  plus  $\theta_d$ , where  $\theta_d$  is given by Equation 15.  $\theta_d$  represents the thermal resistance of the device added to the thermal resistance through half the thickness of the substrate layer.

$$\theta_d = (\text{device thermal resistance}) + \frac{s}{2k_s ab} \quad (23)$$

where  $a$  and  $b$  are the device base dimensions. As stated previously; if the device is a film resistor, then the device thermal resistance is zero. If the device is a transistor, IC or resistor chip; then the device thermal resistance is often given by the manufacturer. When the manufacturer does not give this information, it can be conservatively estimated by a simple "spreading resistance" model [2] as:

$$\frac{1}{2k_d(c-d)} \ln \left[ \frac{c}{d} \left( \frac{d+2t}{c+2t} \right) \right] \quad (24)$$

where:  $k_d$  is the chip thermal conductivity,  $t$  is the thickness and  $c, d$  ( $c > d$ ) are the rectangular dimensions of the heat generating area on top of the chip. This is not, in general, the total top area of the chip. If  $c = d$  the device thermal resistance is given by

$$\frac{t}{k_d c^2 \left[ 1 + \frac{2t}{c} \right]} \quad (25)$$

If the chip device is epoxy (rather than eutectic) bonded to the substrate, then the epoxy thermal resistance

$$\frac{v}{k_v ab}$$

must be added to  $\theta_d$  in Equation 23.  $v$  is the epoxy thickness and  $k_v$  its thermal conductivity. Both the thickness and conductivity may be different from the substrate bonding epoxy.

If a second device is placed a distance  $r_{ij}$  from the device dissipating power  $P$ , then the coupling thermal resistance  $\theta_{ji}$  is obtained from Equation 22 by setting  $r$  equal to  $r_{ij}$ ; provided that  $r_{ij} \leq R_0$ . If  $R_0 < r_{ij} \leq 4/\lambda$ , then the coupling thermal resistance is taken as Equation 22 with  $r$  set equal to  $R_0$ . This will give conservative results. If however,  $r_{ij} > 4/\lambda$  then the devices are

sufficiently separated so that the thermal coupling is negligible and  $\theta_{ij} \approx 0$ . This condition is applied even if  $R_0 > 4/\lambda$ .

#### D. Use of Results for Hybrid Circuit Layout

It is assumed that the hybrid circuit layout designer has knowledge of the following quantities or is able to readily obtain them:

1. header thickness,  $h$
2. header thermal conductivity,  $k_h$
3. substrate epoxy thickness,  $e$
4. substrate epoxy thermal conductivity,  $k_e$
5. substrate thickness,  $s$
6. substrate thermal conductivity,  $k_s$
7. all dissipating device base dimensions,  $a$  and  $b$
8. if a chip, the chip thickness,  $t$
9. if a chip, the chip thermal conductivity,  $k_d$
10. if a chip, the rectangular dimensions of the heat generating surface on top of the chip,  $c$  and  $d$
11. if chip is epoxy bonded, the epoxy thickness,  $v$
12. if chip is epoxy bonded, the epoxy thermal conductivity,  $k_v$

Values of thermal conductivities are usually obtainable from the material manufacturer. Typical values of these are as follows:

1. substrate:  $k_s = 6 \times 10^{-4} \text{ W/mil-}^\circ\text{C}$  for  $\text{Al}_2\text{O}_3$   
 $= 3.9 \times 10^{-3} \text{ W/mil-}^\circ\text{C}$  for  $\text{BeO}$
2. substrate epoxy (Ag filled):  
 $k_e = 4 \times 10^{-5} \text{ W/mil-}^\circ\text{C}$

3. Kovar header:  $k_h = 4 \times 10^{-4} \text{ W/mil-}^\circ\text{C}$
4. Silicon chip material:  $k_d = 1.9 \times 10^{-3} \text{ W/mil-}^\circ\text{C}$
5. Chip bonding epoxy (Au filled):  $k_v = 4.4 \times 10^{-5} \text{ W/mil-}^\circ\text{C}$

Epoxy layer thicknesses,  $e$  and  $v$ , are somewhat variable depending upon fabrication "squeeze out". Values of 5.5 mils for  $e$  and 1 mil for  $v$  have been measured on actual hybrid systems. Other dimensions such as  $h$ ,  $s$ ,  $a$ ,  $b$  and  $t$  are given by the manufacturer, or can be easily measured.

The chip heat generating surface dimensions,  $c$  and  $d$ , can often be obtained from specifications supplied by the manufacturer. An example would be a sketch of the surface emitter region configuration for a discrete transistor chip. If not available, this may be observed under a microscope. Occasionally the device thermal resistance is given in the specifications. Curves, such as those given by Harper [5, p1-101], are often useful.

The layout designer now decides on a tentative device layout on the substrate. He calculates  $\lambda$  from Equation 13. The effective device radius  $r_o$  is obtained from Equation 16 for each device and  $R_o$ , the device substrate radius, is the distance from the center of the device to the nearest substrate edge. The center to center distance  $r_{ij}$  is noted for all dissipating device pairs.

Thermal resistances  $\theta_{sc}$  and coupling thermal resistances  $\theta_{ji}$  are calculated by the instructions given in Section C. To the

value of  $\theta_{sc}$ , for each dissipating device, is added  $\theta_d$  as given by Equation 23. Finally, all device heat generating region temperatures are calculated by means of Equations 1 and 2.

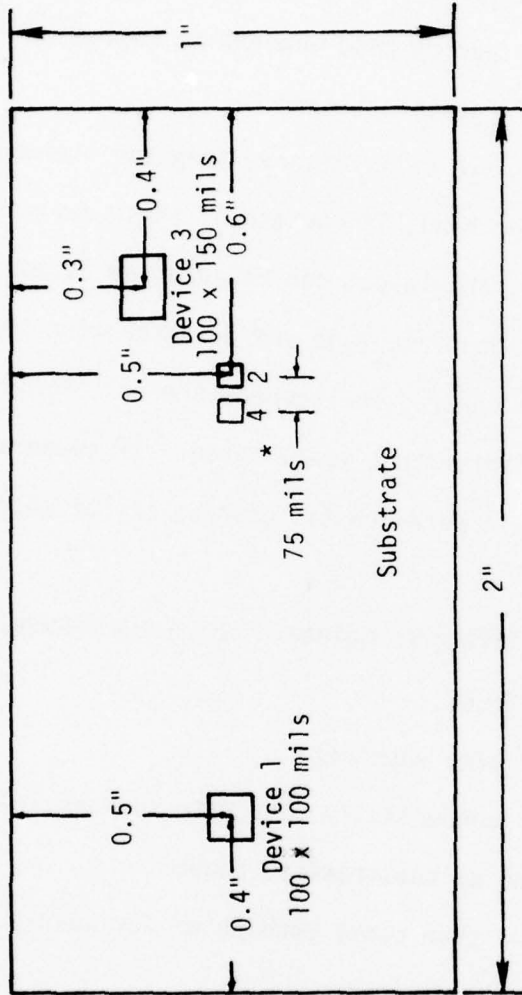
If these temperatures are satisfactory, then the thermal layout is completed. On the other hand, if certain of these device temperatures are too high, the layout can be adjusted by moving devices farther from the substrate edge and/or separating the devices farther from each other. The temperature calculations would again be made and performance reevaluated. If temperatures are still too high, certain more drastic changes may be necessary. Some of these might be:

1. External heat sinking to maintain the header temperature,  $T_c$ , at a lower level.
2. Use of a larger area substrate
3. Use of a higher conductivity substrate such as BeO.
4. Direct soldering of substrate to header
5. Eutectic, rather than epoxy bonding of devices
6. Use of larger area devices

#### E. Example Layout Design

A typical hybrid layout example is shown in Figure 6. This will be used to illustrate a thermal performance calculation. The four devices are those dissipating an appreciable amount of heat power, and are described as follows:

1. Device 1 - silicon chip transistor, epoxy bonded  $a_1 = b_1 = 100$  mils,  $c_1 = 80$  mils,  $d_1 = 40$  mils,  $t_1 = 10$  mils,  $k_d = 1.9 \times 10^{-3}$  W/mil-°C,  $P_1 = 10$ W,  $v = 1$  mil,  $k_v = 4.4 \times 10^{-5}$  W/mil-°C



\*Devices 2 and 4 are 50x50 mils

Figure 6. Hybrid Circuit Layout Example

2. Devices 2 and 4 - silicon chip transistor, eutectic bonded

$$a_2 = b_2 = 50 \text{ mils}, c_2 = d_2 = 30 \text{ mils}$$

$$t_2 = 8 \text{ mils}, K_{d_2} = 1.9 \times 10^{-3} \text{ W/mil-}^\circ\text{C}, P_2 = P_4 = 4 \text{ W}$$

3. Device 3 - screened film power resistor

$$a_3 = 150 \text{ mils}, b_3 = 100 \text{ mils}, P_3 = 12 \text{ W}$$

The substrate is alumina, with  $s = 25$  mils and  $k_s = 6 \times 10^{-4} \text{ W/mil-}^\circ\text{C}$ .

It is bonded to a kovar header by an  $e = 5$  mil thickness of epoxy, with thermal conductivity,  $k_e = 4 \times 10^{-5} \text{ W/mil-}^\circ\text{C}$ . The header is  $h = 30$  mils thick and has a value of  $k_h = 4 \times 10^{-4} \text{ W/mil-}^\circ\text{C}$ , for its thermal conductivity.

The lower header surface is externally heat sinked so that its temperature is  $T_c = 50^\circ\text{C}$ . The problem is to determine the peak heat generating region temperatures for the three devices.

From Equation 13,  $\lambda$  is first calculated:

$$\lambda = 1.74 \times 10^{-2} \text{ mils}^{-1}$$

The effective radii of the three devices are determined from Equation 16:

$$r_{o_i} = 56.4 \text{ mils}, r_{o_2} = r_{o_4} = 28.2 \text{ mils}, r_{o_3} = 69.1 \text{ mils}$$

The assumed circular substrate radii are noted from Figure 6:

$$R_{o_1} = 400 \text{ mils}, R_{o_2} = R_{o_4} = 500 \text{ mils}, R_{o_3} = 300 \text{ mils}.$$

Device center to center distances are also obtained from Figure 6:

$$r_{12} = r_{21} = 1000 \text{ mils}, r_{23} = r_{32} = 283 \text{ mils}, r_{13} = r_{31} = 1217 \text{ mils}$$

$$r_{14} = r_{41} = 925 \text{ mils}, r_{24} = r_{42} = 75 \text{ mils}, r_{34} = r_{43} = 340 \text{ mils}$$

In computing  $\theta_{sc_1}$ , for device 1, the following are obtained from the table of modified Bessel functions listed in the appendix:

$$\lambda r_{o_1} = 0.98$$

$$I_0(\lambda r_{o_1}) = 1.26$$

$$K_0(\lambda r_{o_1}) = 0.43$$

$$I_1(\lambda r_{o_1}) = 0.55$$

$$K_1(\lambda r_{o_1}) = 0.62$$

$$\lambda R_{o_1} = 6.96$$

$$I_1(\lambda R_{o_1}) = 150$$

$$K_1(\lambda R_{o_1}) = 0.00047$$

$\theta_{sc_1}$  is now calculated from Equation 22 by letting  $r = r_o = r_{o_1}$  and  $R_o = R_{o_1}$ . Its value is

$$\theta_{sc_1} = 5.64^\circ\text{C/W}$$

$\theta_{d_1}$  is calculated from Equations 23 and 24, adding also the chip bonding epoxy thermal resistance:

$$\theta_{d_1} = \frac{1}{2k_{d_1}(c_1 - d_1)} \ln \left[ \frac{c_1}{d_1} \left( \frac{d_1 + 2t_1}{c_1 + 2t_1} \right) \right] + \frac{s}{2k_s a_1 b_1} + \frac{v}{k_v a_1 b_1}$$

$$\theta_{d_1} = 1.2 + 2.08 + 2.27 = 5.55^\circ\text{C/W}$$

It is noted that  $r_{12}$ ,  $r_{23}$ ,  $r_{13}$ ,  $r_{14}$  and  $r_{34}$  all exceed  $4/\lambda = 230$  mils. Hence the coupling thermal resistance between all devices except 2 and 4 is negligible. That is:

$$\theta_{12} = \theta_{21} = \theta_{23} = \theta_{32} = \theta_{13} = \theta_{31} = \theta_{14} = \theta_{41} = \theta_{34} = \theta_{43} = 0$$

$\theta_{sc2} = \theta_{sc4}$  is calculated from Equation 22 by letting  $r = r_o = r_{o2}$  and  $R_o = R_{o2}$ .  $\theta_{sc3}$  is obtained by letting  $r = r_o = r_{o3}$  and  $R_o = R_{o3}$ . The values are

$$\theta_{sc2} = \theta_{sc4} = 10.62^\circ\text{C/W}$$

$$\theta_{sc3} = 4.54^\circ\text{C/W}$$

For devices 2 and 4,  $\theta_d$  is calculated from Equations 23 and 25.

$$\theta_{d2} = \theta_{d4} = \frac{t_2}{k_{d2} c_2^2 \left[ 1 + \frac{2t_2}{c_2} \right]} + \frac{s}{2k_s a_2 b_2} = 3.05 + 8.33 = 11.38^\circ\text{C/W}$$

Since device 3 is a film resistor,  $\theta_{d3}$  is simply

$$\theta_{d3} = \frac{s}{2k_s a_3 b_3} = 1.39^\circ\text{C/W}$$

The coupling thermal resistance between devices 2 and 4 is calculated by Equation 22. It is first noted that  $r_{24} = r_{42}$  is less than both  $R_{o2}$  and  $R_{o4}$ . Thus  $\theta_{24} = \theta_{42}$  is obtained by letting  $r_o = r_{o2}$ ,  $R_o = R_{o2}$  and  $r = r_{24}$  in that equation. The value obtained is

$$\theta_{24} = \theta_{42} = 3.14^\circ\text{C/W}$$

$\theta_{ij}$  and  $\theta_{ji}$  are equal in this case, since both devices have identical values of  $r_o$  and  $R_o$ . This will not be true in general, though the values of  $\theta_{ij}$  and  $\theta_{ji}$  should not differ radically from each other.

Finally the device heat generating region temperatures are calculated from Equations 1 and 2.

$$T_{cp1_1} = T_{cp1_3} = 0$$

$$T_{cp1_2} = \theta_{24} P_4 = 3.14 \times 4 = 12.6^\circ\text{C}$$

$$T_{cp1_4} = \theta_{42} P_2 = 3.14 \times 4 = 12.6^\circ\text{C}$$

$$T_{j_1} = P_1(\theta_{d_1} + \theta_{sc_1}) + T_c = 10(5.55 + 5.64) + 50 = 161.9^\circ\text{C}$$

$$T_{j_2} = T_{cp1_2} + P_2(\theta_{d_2} + \theta_{sc_2}) + T_c = 12.6 + 4(11.38 + 10.62) + 50 = 150.6^\circ\text{C}$$

$$T_{j_3} = P_3(\theta_{d_3} + \theta_{sc_3}) + T_c = 12(1.39 + 4.54) + 50 = 121.2^\circ\text{C}$$

$$T_{j_4} = T_{cp1_4} + P_4(\theta_{d_4} + \theta_{sc_4}) + T_c = 12.6 + 4(11.38 + 10.62) + 50 = 150.6^\circ\text{C}$$

#### F. Comparison of Results with the Spreading Resistance Model

The spreading resistance model has been used extensively to make simplified thermal resistance calculations for heat generating devices [5,12]. This model assumes that heat flow spreads out over a 45° angle from the heat generating region. Its use for hybrid devices is illustrated by Ruwe and Slage [2, pp. 45-47]. For a transistor chip as a device, the spreading resistance model gave a thermal resistance (from chip to header) that was 51% higher than the more accurate finite-difference equation computation. The reason for this is easy to see, since the spreading resistance model effectively

"removes" the layer conducting material outside the 45° spreading region. Also, the use of the spreading resistance model does not allow for calculation of coupling thermal resistance.

The simplified model, incorporated in Equation 22, also allows rapid computation of thermal resistance. In addition, coupling thermal resistances are obtained. For comparative purposes, Table 1 shows the device thermal resistance ( $\theta_{sc} + \theta_d$ ), for the four devices in Section C, along with those computed by simply the spreading resistance model [2, pp. 45-47]. It is noted that the spreading resistance model predicts device thermal resistances from 28% to 64% higher.

Device No.	$\theta_{sc} + \theta_d$ calc. in Section C	$\theta_{sc} + \theta_d$ from spreading resistance model	Percentage greater for spreading resistance model
1	11.2° C/W	18.4° C/W	64
2 and 4	22° C/W	28.9° C/W	31
3	5.93° C/W	7.58° C/W	28

Table 1. Comparison of Device Thermal Resistance.

Both the model proposed in this report and the spreading resistance model will give conservative results. That is, because of the assumptions made in each case, they predict a higher than actual thermal resistance. However, Table 1 shows that the use of the spreading resistance model leads to results so conservative, that the use of this model may well lead to thermal overdesign. For this reason, the model, incorporated in Equation 22, is to be preferred.

#### IV. RECOMMENDATIONS FOR FURTHER RESEARCH

The following are areas, related to the thermal models developed in this report, that deserve further investigation and research:

##### A. Evaluation of Model against Experimental Measurement

Experimental measurements made by the contractor and others [13,14] should be compared to the model results incorporated in Equation 22, for the same hybrid configurations. This will reveal the effect of certain uncertainties, such as in parameter values used for the model, or whether bonding voids exist. Coupling thermal resistance measurement can likewise be made in the laboratory for comparison with those obtained from model calculations.

##### B. Evaluation of Model Against Thermal Computer Simulation

Accuracy of the simplified thermal model may be further verified by comparison with a finite-difference equation simulation of particular hybrid systems. This simulation would provide highly accurate results [2]. Several test cases should be compared to evaluate model accuracy. In particular, for cases where devices are placed either extremely close to the substrate edge or to each other, this comparison will reveal limitations, if any, in the model.

##### C. Model for Soldered Beryllia Substrates

The feasibility of developing a simplified model, that is somewhat similar to Equation 22, for solder bonded beryllia substrates should be investigated.

D. Flip-Chip and Beam-Lead Devices

The feasibility of developing a simplified device thermal resistance ( $\theta_d$ ) for these devices should be investigated, with the goal of incorporating it with the substrate to header model, characterized by Equation 22.

E. Trimmed Film Resistors

These devices experience significantly higher surface temperatures than untrimmed resistors. This has been verified both analytically and experimentally [13]. The development of a simplified device thermal resistance ( $\theta_d$ ) calculation, for trimmed resistors, should be investigated.

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APPENDIX  
MODIFIED BESSEL FUNCTIONS

TABLES

From: Handbook of Mathematical Functions, National Bureau of Standards  
Applied Mathematics Series, 55, May 1968.

BESSEL FUNCTIONS OF INTEGER ORDER

Table 9.8 MODIFIED BESSEL FUNCTIONS—ORDERS 0, 1 AND 2

$x$	$e^{-x}I_0(x)$	$e^{-x}I_1(x)$	$x^{-2}I_2(x)$
0.0	1.00000 00000	0.00000 00000	0.12500 00000
0.1	0.90710 09258	0.04529 84468	0.12510 41992
0.2	0.82693 85516	0.08228 31235	0.12541 71878
0.3	0.75758 06252	0.11237 75606	0.12594 01407
0.4	0.69740 21705	0.13676 32243	0.12667 50222
0.5	0.64503 52706	0.15642 08032	0.12762 45967
0.6	0.59932 72031	0.17216 44195	0.12879 24416
0.7	0.55930 55265	0.18466 99828	0.13018 29658
0.8	0.52414 89420	0.19449 86933	0.13180 14318
0.9	0.49316 29662	0.20211 65309	0.13365 39819
1.0	0.46575 96077	0.20791 04154	0.13574 76698
1.1	0.44144 03776	0.21220 16132	0.13809 04952
1.2	0.41978 20789	0.21525 68594	0.14069 14455
1.3	0.40042 49127	0.21729 75878	0.14356 05405
1.4	0.38306 25154	0.21850 75923	0.14670 88837
1.5	0.36743 36090	0.21903 93874	0.15014 87192
1.6	0.35331 49978	0.21901 94899	0.15389 34944
1.7	0.34051 56880	0.21855 28066	0.15795 79288
1.8	0.32887 19497	0.21772 62788	0.16235 80900
1.9	0.31824 31629	0.21661 19112	0.16711 14772
2.0	0.30850 83225	0.21526 92892	0.17223 71119
2.1	0.29955 30945	0.21374 76721	0.17775 56370
2.2	0.29131 73331	0.21208 77328	0.18368 94251
2.3	0.28369 29857	0.21032 30051	0.19006 26964
2.4	0.27662 23231	0.20848 10887	0.19690 16460
2.5	0.27004 64416	0.20658 46495	0.20423 45837
2.6	0.26391 39957	0.20465 22544	0.21209 20841
2.7	0.25818 01238	0.20269 90640	0.22050 71509
2.8	0.25283 55337	0.20073 74113	0.22951 53938
2.9	0.24775 57304	0.19877 72816	0.23915 52213
3.0	0.24300 03542	0.19682 67133	0.24946 80490
3.1	0.23851 26187	0.19489 21309	0.26049 85252
3.2	0.23426 88316	0.19297 86229	0.27229 47757
3.3	0.23024 79845	0.19109 01727	0.28490 86686
3.4	0.22643 14011	0.18922 98511	0.29839 61010
3.5	0.22280 24380	0.18739 99766	0.31281 73100
3.6	0.21934 62245	0.18560 22484	0.32823 72078
3.7	0.21604 94417	0.18383 78580	0.34472 57467
3.8	0.21290 01308	0.18210 75810	0.36235 83128
3.9	0.20988 75279	0.18041 18543	0.38121 61528
4.0	0.20700 19211	0.17875 08394	0.40138 68359
4.1	0.20423 45274	0.17712 44763	0.42296 47539
4.2	0.20157 73840	0.17553 25260	0.44605 16629
4.3	0.19902 32571	0.17397 46091	0.47075 72701
4.4	0.19656 55589	0.17245 02337	0.49719 98689
4.5	0.19419 82777	0.17095 88223	0.52550 70272
4.6	0.19191 59151	0.16949 97311	0.55581 63319
4.7	0.18971 34330	0.16807 22681	0.58827 61978
4.8	0.18758 62042	0.16667 57058	0.62304 67409
4.9	0.18552 99721	0.16530 92936	0.66030 07270
5.0	0.18354 08126	0.16397 22669	0.70022 45988

$$I_{n+1}(x) = -\frac{2n}{x} I_n(x) + I_{n-1}(x)$$

Compiled from British Association for the Advancement of Science, Bessel functions, Part I. Functions of orders zero and unity, Mathematical Tables, vol. VI, Part II. Functions of positive integer order, Mathematical Tables, vol. X (Cambridge Univ. Press, Cambridge, England, 1950, 1952) and L. Fox, A short table for Bessel functions of integer orders and large arguments, Royal Society Shorter Mathematical Tables No. 3 (Cambridge Univ. Press, Cambridge, England, 1954) (with permission).

## . BESSEL FUNCTIONS OF INTEGER ORDER

Table 9.8 MODIFIED BESSEL FUNCTIONS—ORDERS 0, 1 AND 2

$x$	$e^{-x}I_0(x)$	$e^{-x}I_1(x)$	$e^{-x}I_2(x)$
5.0	0.18354 08126	0.16397 22669	0.11795 1906
5.1	0.18161 51021	0.16266 38546	0.11782 5355
5.2	0.17974 94883	0.16138 32850	0.11767 8994
5.3	0.17794 08646	0.16012 97913	0.11751 4528
5.4	0.17618 63475	0.15890 26150	0.11733 3527
5.5	0.17448 32564	0.15770 10090	0.11713 7435
5.6	0.17282 90951	0.15652 42405	0.11692 7581
5.7	0.17122 15362	0.15537 15922	0.11670 5188
5.8	0.16965 84061	0.15424 23641	0.11647 1384
5.9	0.16813 76726	0.15313 58742	0.11622 7207
6.0	0.16665 74327	0.15205 14593	0.11597 3613
6.1	0.16521 59021	0.15098 84754	0.11571 1484
6.2	0.16381 14064	0.14994 62978	0.11544 1633
6.3	0.16244 23718	0.14892 43212	0.11516 4809
6.4	0.16110 73175	0.14792 19595	0.11488 1705
6.5	0.15980 48490	0.14693 86457	0.11459 2958
6.6	0.15853 36513	0.14597 38314	0.11429 9157
6.7	0.15729 24831	0.14502 69866	0.11400 0845
6.8	0.15608 01720	0.14409 75991	0.11369 8525
6.9	0.15489 56090	0.14318 51745	0.11339 2660
7.0	0.15373 77447	0.14228 92347	0.11308 3678
7.1	0.15260 55844	0.14140 93186	0.11277 1974
7.2	0.15149 81855	0.14054 49809	0.11245 7913
7.3	0.15041 46530	0.13969 57915	0.11214 1833
7.4	0.14935 41371	0.13886 13353	0.11182 4046
7.5	0.14831 58301	0.13804 12115	0.11150 4840
7.6	0.14729 89636	0.13723 50333	0.11118 4481
7.7	0.14630 28062	0.13644 24270	0.11086 3215
7.8	0.14532 66611	0.13566 30318	0.11054 1268
7.9	0.14436 98642	0.13489 64995	0.11021 8852
8.0	0.14343 17818	0.13414 24933	0.10989 6158
8.1	0.14251 18095	0.13340 06883	0.10957 3368
8.2	0.14160 93695	0.13267 07705	0.10925 0645
8.3	0.14072 39098	0.13195 24362	0.10892 8142
8.4	0.13985 49027	0.13124 53923	0.10860 6000
8.5	0.13900 18430	0.13054 93551	0.10828 4348
8.6	0.13816 42474	0.12986 40505	0.10796 3305
8.7	0.13734 16526	0.12918 92134	0.10764 2983
8.8	0.13653 36147	0.12852 45873	0.10732 3481
8.9	0.13573 97082	0.12786 99242	0.10700 4894
9.0	0.13495 95247	0.12722 49839	0.10668 7306
9.1	0.13419 26720	0.12658 95342	0.10637 0796
9.2	0.13343 87740	0.12596 33501	0.10605 5437
9.3	0.13269 74691	0.12534 62139	0.10574 1294
9.4	0.13196 84094	0.12473 79145	0.10542 8428
9.5	0.13125 12609	0.12413 82477	0.10511 6893
9.6	0.13054 57016	0.12354 70154	0.10480 6740
9.7	0.12985 14223	0.12296 40258	0.10449 8015
9.8	0.12916 81248	0.12238 90929	0.10419 0759
9.9	0.12849 55220	0.12182 20364	0.10388 5010
10.0	0.12783 33371 [ $\binom{-6}{6}$ ]	0.12126 26814 [ $\binom{-6}{5}$ ]	0.10358 0801 [ $\binom{-6}{5}$ ]

## BESSEL FUNCTIONS OF INTEGER ORDER

## MODIFIED BESSEL FUNCTIONS—ORDERS 0, 1 AND 2 Table 9.8

$x$	$e^x K_0(x)$	$e^x K_1(x)$	$x^2 K_2(x)$
0.0	$\infty$	$\infty$	2.00000 0000
0.1	2.68232 61023	10.89018 2683	1.99503 9646
0.2	2.14075 73233	5.83338 6037	1.98049 7172
0.3	1.85262 73007	4.12515 7762	1.95711 6625
0.4	1.66268 20891	3.25867 3880	1.92580 8202
0.5	1.52410 93857	2.73100 97082	1.88754 5888
0.6	1.41673 76214	2.37392 00376	1.84330 9881
0.7	1.33012 36562	2.11501 13128	1.79405 1681
0.8	1.25820 31216	1.91793 02990	1.74067 2762
0.9	1.19716 33803	1.76238 82197	1.68401 1992
1.0	1.14446 30797	1.63615 34863	1.62483 8899
1.1	1.09833 02828	1.53140 37541	1.56385 0953
1.2	1.05748 45322	1.44289 75522	1.50167 3576
1.3	1.02097 31613	1.36698 72841	1.43886 2011
1.4	0.98806 99961	1.30105 37400	1.37590 4446
1.5	0.95821 00533	1.24316 58736	1.31322 5917
1.6	0.93094 59808	1.19186 75654	1.25119 2681
1.7	0.90591 81386	1.14603 92462	1.19011 6819
1.8	0.88283 35270	1.10480 53726	1.13026 0897
1.9	0.86145 06168	1.06747 09298	1.07184 2567
2.0	0.84156 82151	1.03347 68471	1.01503 9018
2.1	0.82301 71525	1.00236 80527	0.95999 1226
2.2	0.80565 39812	0.97377 01679	0.90680 7952
2.3	0.78935 61312	0.94737 22250	0.85556 9487
2.4	0.77401 81407	0.92291 36650	0.80633 1113
2.5	0.75954 86903	0.90017 44239	0.75912 6289
2.6	0.74586 82430	0.87896 72806	0.71396 9565
2.7	0.73290 71515	0.85913 18867	0.67085 9227
2.8	0.72060 41251	0.84053 00604	0.62977 9698
2.9	0.70890 49774	0.82304 20403	0.59070 3688
3.0	0.69776 15980	0.80656 34800	0.55359 4126
3.1	0.68713 11010	0.79100 30157	0.51840 5885
3.2	0.67697 51139	0.77628 02824	0.48508 7306
3.3	0.66725 91831	0.76232 42864	0.45358 1550
3.4	0.65795 22725	0.74907 20613	0.42382 7789
3.5	0.64902 63377	0.73646 75480	0.39576 2241
3.6	0.64045 59647	0.72446 06608	0.36931 9074
3.7	0.63221 80591	0.71300 65010	0.34443 1194
3.8	0.62429 15812	0.70206 46931	0.32103 0914
3.9	0.61665 73147	0.69159 88206	0.29905 0529
4.0	0.60929 76693	0.68157 59452	0.27842 2808
4.1	0.60219 65064	0.67196 61952	0.25908 1398
4.2	0.59533 89889	0.66274 24110	0.24096 1165
4.3	0.58871 14486	0.65387 98395	0.22399 8474
4.4	0.58230 12704	0.64535 58689	0.20813 1411
4.5	0.57609 67897	0.63714 97988	0.19329 9963
4.6	0.57008 72022	0.62924 26383	0.17944 6150
4.7	0.56426 24840	0.62161 69312	0.16651 4127
4.8	0.55861 33194	0.61425 66003	0.15445 0249
4.9	0.55313 10397	0.60714 68131	0.14320 3117
5.0	0.54780 75643	0.60027 38587	0.13272 3593

$$K_{n+1}(x) = \frac{2n}{x} K_n(x) + K_{n-1}(x)$$

$$\left[ \begin{matrix} (-3)1 \\ 11 \end{matrix} \right]$$

## BESSEL FUNCTIONS OF INTEGER ORDER

MODIFIED BESSEL FUNCTIONS—ORDERS 0, 1 AND 2 Table 9.8

$x$	$e^x K_0(x)$	$e^x K_1(x)$	$e^x K_2(x)$
5.0	0.54780 75643	0.60027 38587	0.78791 711
5.1	0.54263 53519	0.59362 50463	0.77542 949
5.2	0.53760 73540	0.58718 86062	0.76344 913
5.3	0.53271 69744	0.58095 36085	0.75194 475
5.4	0.52795 80329	0.57490 98871	0.74088 762
5.5	0.52332 47316	0.56904 79741	0.73025 127
5.6	0.51881 16252	0.56335 90393	0.72001 128
5.7	0.51441 35938	0.55783 48348	0.71014 511
5.8	0.51012 58183	0.55246 76495	0.70063 190
5.9	0.50594 37583	0.54725 02639	0.69145 232
6.0	0.50186 31309	0.54217 59104	0.68258 843
6.1	0.49787 98929	0.53723 82386	0.67402 358
6.2	0.49399 02237	0.53243 12833	0.66574 225
6.3	0.49019 05093	0.52774 94344	0.65773 001
6.4	0.48647 73291	0.52318 74101	0.64997 339
6.5	0.48284 74413	0.51874 02336	0.64245 982
6.6	0.47929 77729	0.51440 32108	0.63517 753
6.7	0.47582 54066	0.51017 19097	0.62811 553
6.8	0.47242 75723	0.50604 21421	0.62126 350
6.9	0.46910 16370	0.50200 99471	0.61461 177
7.0	0.46584 50959	0.49807 15749	0.60815 126
7.1	0.46265 55657	0.49422 34737	0.60187 345
7.2	0.45953 07756	0.49046 22755	0.59577 030
7.3	0.45646 85618	0.48678 47842	0.58983 426
7.4	0.45346 68594	0.48318 79648	0.58405 820
7.5	0.45052 36991	0.47966 89336	0.57843 541
7.6	0.44763 71996	0.47622 49486	0.57295 955
7.7	0.44480 55636	0.47285 33995	0.56762 463
7.8	0.44202 70724	0.46955 18010	0.56242 497
7.9	0.43930 00819	0.46631 77847	0.55735 522
8.0	0.43662 30185	0.46314 90928	0.55241 029
8.1	0.43399 43754	0.46004 25709	0.54758 538
8.2	0.43141 27084	0.45699 91615	0.54287 592
8.3	0.42887 66329	0.45401 37001	0.53827 757
8.4	0.42638 48214	0.45108 59089	0.53378 623
8.5	0.42393 59993	0.44821 33915	0.52939 797
8.6	0.42152 89433	0.44539 46295	0.52510 909
8.7	0.41916 24781	0.44262 79775	0.52091 604
8.8	0.41683 54743	0.43991 18594	0.51681 544
8.9	0.41454 68462	0.43724 47648	0.51280 410
9.0	0.41229 55493	0.43462 52454	0.50887 894
9.1	0.41008 05783	0.43205 19116	0.50503 704
9.2	0.40790 09662	0.42952 34301	0.50127 562
9.3	0.40575 57809	0.42703 85204	0.49759 202
9.4	0.40364 41245	0.42459 59520	0.49398 369
9.5	0.40156 51322	0.42219 45430	0.49044 819
9.6	0.39951 79693	0.41983 31565	0.48698 321
9.7	0.39750 18313	0.41751 06989	0.48358 651
9.8	0.39551 59416	0.41522 61179	0.48025 597
9.9	0.39355 95506	0.41297 84003	0.47698 953
10.0	0.39163 19344 $\left[ \begin{smallmatrix} (-5)2 \\ 6 \end{smallmatrix} \right]$	0.41076 65701 $\left[ \begin{smallmatrix} (-5)3 \\ 6 \end{smallmatrix} \right]$	0.47378 525 $\left[ \begin{smallmatrix} (-5)6 \\ 5 \end{smallmatrix} \right]$

Part 2

LOW COST THIN-FILM MICROCIRCUITS  
ON FLEXIBLE SUBSTRATES

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## I. INTRODUCTION

### Objectives

The purpose of this thesis is to investigate the properties of vacuum evaporated thin film resistors fabricated on glass and flexible substrates. A secondary purpose is to evaluate a copper on Kanthal metalization scheme as a simple, low cost thin film process. Identical resistor arrays were constructed on the flexible polyimide film (Kapton) and on borosilicate glass substrates (Pyrex microscope slides). These circuits were then studied with regard to appearance and film adhesion. In addition, measurements were made to determine values of sheet resistance and temperature coefficients of resistance (TCR's). The effect of flexing the Kapton substrate on the above parameters was also examined.

The films were deposited in a two layer arrangement. The first layer, Kanthal (described in Chapter II), was deposited to a sheet resistance of 200 ohms/square rather than to a predetermined thickness. The second layer was copper and was deposited to a thickness of about 10,000 angstroms. The copper serves as the conductor material; the Kanthal provides the resistor material as well as an adhesive underlayer for the copper conductors.

### Deposition Techniques

There are a number of techniques for depositing thin films. The ones most commonly used in circuit fabrication are vacuum evaporation, sputtering, anodization, silk screening, epitaxy, vapor plating, plasma decomposition, and electron beam decomposition [1]. Vacuum evaporation and sputtering are by far the most widely used of these techniques. The resistors described in this paper were fabricated by vacuum evaporation.

In vacuum deposition a source material is heated to its evaporation point in a chamber generally at pressures of  $10^{-5}$  to  $10^{-6}$  torr. At this level of vacuum the mean free path of the evaporated molecules is large enough that they are able to travel from source to substrate in an approximate straight line. Upon arrival at the substrate the molecules condense and begin formation of a film.

### Film Growth

The growth sequence of thin films has been the subject of many studies and is outlined in Maissel and Glang [2] as being basically a nine step process. Those steps are as follows:

1. Formation of absorbed monomers.
2. Formation of subcritical embryos of various sizes.
3. Formation of critically sized nuclei.

4. Growth of these nuclei and absorption of monomers in surrounding areas.
5. Simultaneously with step 4, there is more nucleation in areas not depleted of monomers.
6. Adjacent nuclei touch and coalesce forming islands occupying less area than the original two.
7. Absorbed monomers form on freshly exposed areas and begin nucleation.
8. Large islands grow together leaving channels or holes of exposed substrate.
9. Secondary nucleation fills these voids and eventually leads to a continuous film.

This film growth process as observed on gold films deposited inside an electron microscope is described in detail by Pashley and Stowell [3].

#### Film Properties

A thin film is defined by Fogiel [1] as one whose electrical properties are dependent on the film thickness. The resistivity of thin films can often be several orders of magnitude greater than in bulk material of the same composition. According to Chapman [4]  $\rho_{total}$ , the total resistivity of a thin metal film, is given by

$$\rho_{total} = \rho_{ideal} + \rho_{residual} + \rho_{thickness} \quad (I-1)$$

In this expression  $\rho_{ideal}$  results from scattering due to the thermal vibration of metal ions about statistically

predicted lattice sites.  $\rho_{\text{residual}}$  results from the presence of lattice defects. The third factor,  $\rho_{\text{thickness}}$ , arises from the fact that the film thickness is of the order of magnitude or less than the mean free path of electrons. When this occurs, surface scattering becomes significant. Studies of the various conduction mechanisms which determine film resistivity have been made by Bashara [5], Neugebauer and Webb [6], and Dittmer [7].

The temperature coefficient of resistance will also be different for bulk and thin film samples of the same metal. In bulk metals, the TCR is positive. This is also true for thin films that are continuous. This is because, as the film heats up, the lattice vibrations increase and lead to a corresponding increase in scattering which increases  $\rho_{\text{ideal}}$  in equation (I-1). However, in very thin films, when the structure is composed of isolated islands of metal, the means of conduction changes. Conduction is achieved by the tunneling of electrons across the isolated areas between islands. This process is enhanced by heating and consequently, the resistivity decreases. One would expect this to lead to negative TCR's and indeed this is the case [8].

Film growth and resultant properties are affected substantially by deposition parameters. Of particular importance are chamber pressure, evaporation rate, substrate temperature, and film thickness.

As mentioned previously chamber pressure for vacuum evaporation should be between  $10^{-5}$  and  $10^{-6}$  torr. Pressures in this range and below minimize collisions of the source vapor with residual gas atoms. This high vacuum environment also minimizes contamination of the forming film by residual gases since it reduces the number of these gas atoms striking the substrate. Even at these pressures there will be a certain amount of gas trapped within the film structure. Residual gas contamination is virtually eliminated in films deposited at less than  $10^{-7}$  torr but that high a vacuum is more difficult to achieve [1].

Films deposited at high rates will exhibit a structure tending toward a large number of small islands. This is because there is a limited amount of time for the nuclei on the substrate to move around and form larger islands. Additionally, films deposited at higher rates will have less gas trapped. It follows that films deposited at lower rates will have a structure consisting of larger islands and containing more gas contamination.

Substrate temperature during deposition will affect the mobility of condensed atoms on the surface. At higher temperatures the surface mobility will increase and the atoms are more free to move about and form larger islands. Conversely, low substrate temperatures limit mobility and will promote a structure consisting generally of smaller islands.

The mechanical properties of thin films can vary considerably from those of their bulk counterparts. According to Berry [9], the mechanical strength of a thin film may be as much as 200 times larger than that for well annealed bulk samples and is usually several times as great as that of severely cold worked bulk material. He suggests two possible reasons for this. First, the polycrystalline film structure is more disordered than that which can be obtained by cold working. Second, if the film is thin enough, dislocations could extend throughout the entire thickness of the film and thus be locked in place, giving no mechanism for yielding.

#### Thin Film Components

Resistors can be fabricated from a film of predictable resistance on an insulating substrate. In addition to resistors, thin film technology can be used to fabricate capacitors and inductors. Thin film active devices are currently used only in specialized applications. Because of this and the limited range of values of thin film passive components (particularly capacitors), practical thin film circuits generally require additional components to be individually attached and electrically connected to those that are deposited directly on the substrate.

Advantages of Thin Film Microcircuits

Some advantages of thin film microcircuits are [1]:

1. Thin film components do not exhibit the parasitic interactions that are seen in monolithic integrated circuits. Consequently, a one to one conversion can be made from a discrete circuit to a thin film microcircuit. In addition, high frequency capabilities of thin film circuits is much better than what is currently possible with silicon monolithic IC's.
2. Compared to silicon IC's, thin films are more practical for use in passive components and interconnections.
3. Because thin film components can be fabricated on heat conducting substrates (e.g. BeO) and can be made larger than typical monolithic IC components, they can operate at substantially high power levels.
4. Thin film circuits are more radiation resistant than are semiconductor IC's.
5. Thin film microcircuits can be fabricated from a multitude of materials allowing a more complete assortment of component parameter values and circuit types than is possible with standard silicon IC technology.
6. Thin films can be deposited upon a silicon

substrate and used to improve the capabilities of silicon integrated devices.

7. Hybrids can be made in which thin films for passive components and interconnections are deposited on a substrate after which silicon IC's are inserted.
8. Thin film components display a wider operating temperature range and lower temperature coefficients than their silicon counterparts.
9. For special applications thin film active and passive devices can be fabricated on the same substrate.
10. Thin film circuits can be flexed when put on a flexible substrate allowing the possibility of very high density packaging.

#### Disadvantages of Thin Film Microcircuits

Some disadvantages of thin film microcircuits are:

1. Reproducible thin film active devices (FET's) have been difficult to achieve, however, new fabrication techniques may soon overcome this problem.
2. Bipolar transistors cannot be fabricated in thin film technology.

## II. THIN FILM IC DESIGN

### Electrical Design and Test

In the design of thin film integrated circuits, passive components should be used wherever possible, since active silicon devices require attachment after deposition. Capacitance should be minimized as well as the total resistance to reduce the total circuit area. The use of capacitors also complicates processing and large values of resistance may require separate depositions. When possible, circuit operation should depend on component ratios rather than absolute values. It is easier to maintain tolerances on component ratios than the tolerances on their absolute values. This is especially true when temperature stability is considered. Thin film components deposited on the same substrate at the same time will have similar structures and properties; the components will therefore be "matched". Components which require external adjustment in the completed circuit should be eliminated. Also an attempt should be made to minimize both power dissipation and supply voltage.

The resulting design should then be breadboarded and thoroughly tested using discrete components. It may also be of use to perform a computer simulation of the circuit.

After the electrical design is completed a check should be made to see if the circuit can be layed out without crossovers. If not, an attempt should be made to put the circuit in a form that can be made crossover free or with a minimum number of crossovers.

#### Material Selection

Once proper operation of the circuit has been verified, thought can be given to selection of materials. Since this paper is concerned primarily with resistive and conductive arrays only the selection of materials needed for conductor and resistor fabrication will now be considered.

Resistors-In the choice of a suitable resistor material some of the properties that may be of interest are resistivity, temperature coefficient of resistance, voltage coefficient of resistance, noise voltage, stability, and the effect of humidity.

The equation for resistance is as follows:

$$R = \rho L/A \quad (II-1)$$

where  $\rho$  is the resistivity in ohm-centimeters, L is length in centimeters, and A is cross sectional area in centimeters squared. A thin film resistor is often in the form of a rectangular prism so that the area is the product of the

resistor width ( $w$ ) and film thickness ( $t$ ). Thus the equation for resistance becomes:

$$R = (\rho/t)(L/w). \quad (\text{II-2})$$

Sheet resistance ( $R_s$ ) is defined as the resistivity divided by the film thickness and is normally expressed in units of ohms per square. The aspect ratio ( $L/w$ ) is really the measure of the number of squares between the resistor contacts and thus defines the resistance once the sheet resistance is known. It is important to note that for most film materials, resistivity is not independent of film thickness but approaches bulk resistivity as film thickness increases [10].

The temperature coefficient of resistance (TCR) is a measure of how much the total resistance will change for a given change in temperature. Two values of TCR are normally given. The first is for the range from  $-55^\circ\text{C}$  to  $20^\circ\text{C}$  and the second for the range from  $20^\circ\text{C}$  to  $150^\circ\text{C}$ . This encompasses the range of interest for most conventional film circuits. The defining equation is

$$\text{TCR} = [(R_{T_2} - R_{T_1}) / (R_{T_1} \Delta T)] \times 10^6 \text{ ppm}/^\circ\text{C} \quad (\text{II-3})$$

where  $\Delta T$  is  $T_2 - T_1$  and  $T_2 > T_1$ ;  $R_{T_2}$  is the resistance at temperature  $T_2$ ; and  $R_{T_1}$  is the resistance at temperature  $T_1$ .

The voltage coefficient of resistance is given by the following.

$$VCR = [(R_{V1} - R_{V2}) / (R_{V2} \Delta V)] \times 10^6 \text{ ppm/V} \quad (\text{II-4})$$

where  $R_{V1}$  is the resistance at voltage  $V1$ ,  $R_{V2}$  is the resistance at voltage  $V2$ , and  $\Delta V$  is  $V1 - V2$ .  $V1$  is usually set for the rated voltage with  $V2$  being one tenth of this value [10]. Normally VCR will not be a major factor since it is usually in the neighborhood of 5ppm/volt which is usually smaller than the effect of self heating [9].

The noise voltage of a film resistor usually consists of two parts. The first is thermal noise which is proportional to the square root of the resistance and the temperature. It is independent of frequency and is present even if no current is applied. The other constituent of noise voltage is current noise which is proportional to the resistance and applied voltage and inversely proportional to the square root of the frequency [11].

Stability refers to the tendency of a resistor to change value with the passage of time. As a rule, thin film resistors become more stable with age so a thermal treatment to accomplish pre-aging is a good practice. This annealing can also be used to adjust the TCR.

Humidity can adversely affect certain types of resistors. Where this is a consideration protection should be afforded to guard against electrolytic corrosion.

Conductors-The conductor materials for thin film resistors serve two purposes. The first is the interconnection of the thin film components on the substrate and the second is the provision of lands for external connections. Accordingly, desirable characteristics for conductive material would be low sheet resistance, good adherence, low contact resistance, compatibility with die attach or wire bonding techniques, ability to withstand heat treatment used for resistor stabilization, and resistance to oxidation or corrosion. In addition, the conductor material should be selectively etchable so that it may be removed without affecting the resistor material. Since probably no one material can satisfy all of these requirements it is common to use a multi-layered structure. The layers are chosen such that collectively they satisfy most or all of the requirements of a good conductor.

Substrates-The primary purpose of the substrate is to act as a supporting layer for the thin film components. Ideally the substrate material should have no effect on the characteristics of the deposited film other than to assure good adhesion. Unfortunately, this is not the case so substrate properties must be considered as part of the design procedure. As with conductive materials no material can satisfy all the requirements of a good substrate so the particular application must be considered in order to make a wise choice.

A good substrate should be smooth, flat, and non-porous. Any roughness or discontinuities in the substrate will result in non-uniformities in the deposited films. Flatness is important because it provides for good pattern definition during thru-mask deposition and/or during photoresist operations. A porous material is more likely to absorb and retain water or other materials that will outgas during the deposition process.

The substrate should be strong mechanically so as to withstand the stress of processing. Other mechanical properties of importance are: thermal coefficient of expansion, thermal conductivity, resistance to thermal shock, and thermal stability.

It is important that the thermal coefficient of expansion (TCE) of the substrate be similar to that of the deposited film. If there is a severe mismatch of TCE's the film will undergo undue stress during changes in temperature. Since thin film circuits normally consist of more than one material a compromise in matching the TCE's is necessary.

High thermal conductivity is desirable especially when power dissipation is a consideration in the finished circuit. It is also important during processing to maintain good surface temperature control.

Resistance to thermal shock refers to the substrate's ability to resist damage following sudden large temperature

changes. This is important during such processing operations as wire bonding. On the other hand, processing steps that include prolonged heating, such as photoresist baking, require the substrate to have good thermal stability. The most important electrical properties of the substrate are resistivity, dielectric strength, and dielectric constant. A substrate with high resistivity and dielectric strength and a low dielectric constant will assure isolation between individual components and minimization of parasitics.

Substrate materials should be inert to chemicals used in processing. Another desirable chemical property is freedom from ion migration. When a thin film resistor is under moderate power levels the temperature rises and there is an electric field along the surface. Under these conditions alkali metal oxides may become ionized, migrate through the substrate, and react electrochemically with the film.

#### Materials Selected

As mentioned in Chapter I, in this research Kanthal was chosen for the resistor material, copper for the conductors, and both borosilicate glass and Kapton were used for substrates.

Kanthal is an alloy consisting mainly of iron (70%), chromium (22%), and aluminum (5.5%). Although generally used as heating elements in furnaces and ovens it has

previously been used to produce low TCR resistors by Dhere, et.al. [12] and Watts [13]. Besides its low TCR's they discovered that it was easy to work with, compatible with conductor films, and adherent to substrates. In addition, it allowed long filament source life.

Copper was chosen as the conductor material because it is inexpensive, readily available, it can provide very low sheet resistances, and it is solderable. A disadvantage is that it corrodes easily unless protected by a layer of passivating material. Its adherence to substrates is poor. However, when it is deposited on top of a layer of Kanthal, the adherence is found to be quite good, as discussed in Chapter IV.

Pyrex was chosen because it has a long history of use as a thin film substrate and thus can be used as a standard for judging the devices made on Kapton. Kapton was chosen as a substrate because of its unique flexing properties. Polyimide materials such as Kapton have been used for hybrid microcircuit substrates, motherboards, and structures for system packaging [14]-[16]. For many applications it has been shown that these materials can be directly substituted for more conventional substrate materials. Conventional processing can be used with the exception that the rise in substrate temperature during film deposition must be limited to less than 100°C and preferably to 50°C [16]. Size and

weight are reduced, packing density increased, and there is a cost reduction.

It has been shown that polyimides exhibit high peel strengths for thin film metallization, excellent resistance to solder processing temperatures as high as 260°C, resistance to processing chemicals and solvents, dimensional stability after etching and baking, good electrical properties, and survival under repeated hand rework cycles [16]. Polyimide films do tend to absorb more moisture than conventional substrate materials but this can be overcome by an oven bake at the appropriate time [16]. Table 1 compares some of the properties of Pyrex and of Kapton.

#### Circuit Layout

A good approach to circuit layout is to use the "paper doll" technique. Greatly enlarged scale models of the individual components can be drawn and cut out. The designer can then maneuver these individual models on a large sheet of graph paper until a suitable configuration is achieved. Sufficient room must be left between components so that conductors can be drawn within certain minimum spacing constraints. An alternate and increasingly popular technique is to use a computer aided design system.

It is a good idea for thin film resistors to occupy all the area that is available to them. This will enhance the power dissipation of the circuit and reduce errors due to dimensional inaccuracies. It follows that the substrate

TABLE 1. Comparison of Properties of Kapton and Pyrex

Property	Kapton	Pyrex
Thermal Coefficient Of Expansion - /°C	$2.0 \times 10^{-5}$	$3.25 \times 10^{-5}$
Thermal Conductivity cal-cm/(cm <sup>2</sup> sec°C)	.00037-.00045	.0021-.0030
Dielectric Constant	3.0-3.5	4.0-6.0
Specific Gravity	1.42	2.32

should be as large as possible. In practice however, if the substrate area is not limited by packaging requirements or commercial availability it will be by the effective deposition area of the vacuum system. In addition, for very large substrates the film uniformity will suffer. This is because the distance from the source to all parts of a flat substrate is not constant. The film will be thicker at the point on the substrate that is closest to the source. Consequently, as substrate size increases, the differential between the thickest and thinnest points of the film also increases. No resistor in the layout should have less than 0.5 squares between its contacts. Otherwise, there may be errors due to poor control of the distance between these contacts. Sufficient contact separation also minimizes the effects of contact resistance. In this research, rectangular resistors were used where possible. Meandering line resistors have degraded high frequency performance, increased sensitivity to ion migration, and higher susceptibility to failures under humidity and load. They do have the advantage of a high resistance value for a given area. A method for making resistance calculations for resistors of non-rectangular shapes is given by Hall [17].

The layout of the circuit constructed for this thesis is shown in Figure 1. There are 28 resistors, two IC chip bonding pads, and several isolated conductors of different widths. Resistors 1 through 8 all have the same width but

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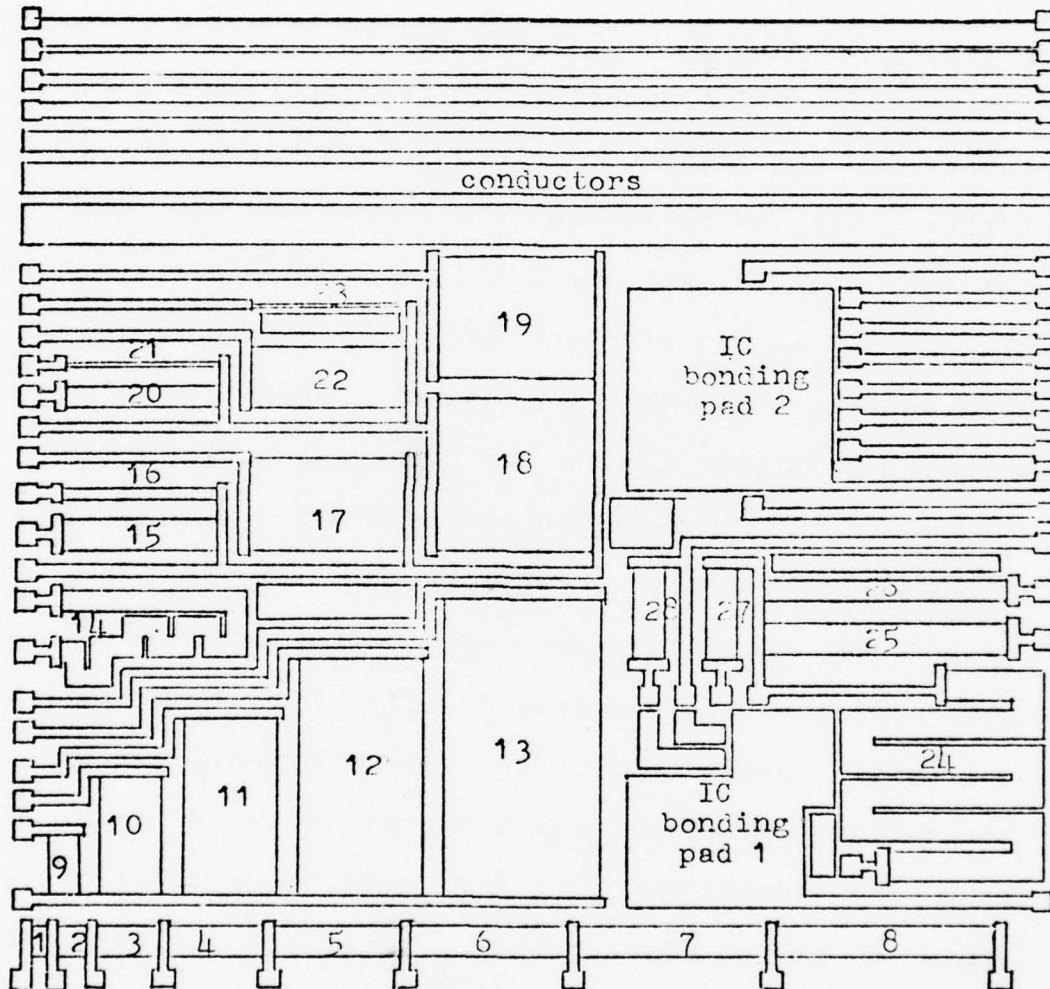


FIGURE 1. Overall layout of thin film integrated circuit

different lengths; resistors 9 through 13 have the same aspect ratio but different areas; and resistors 15 through 23 have the same length but varying widths. These resistors will serve as a test array for evaluating thin film resistors and conductors fabricated by the techniques to be described.

Resistors 24 through 28 are for use in a band gap reference circuit (See Figure 2) which can be implemented by attachment of a silicon transistor array (e.g. RCA CA3083) to one of the bonding pads. Resistor 14 can be used to detect any anomalies associated with a meandering topology resistor. The conductor array of varying line widths is utilized to assess the probability of metalization opens and the minimum line width easily reproducible.

The band gap reference circuit referred to earlier was introduced by Widlar [18], and produces a temperature stable voltage output of 1.205 volts, the band gap potential of silicon.

After the overall circuit layout is completed and checked, it should be used to make layouts for each of the individual layers of film in the circuit. The layouts for the conductor and resistor patterns needed to produce the circuit shown in Figure 1 were done with the aid of the PDP-11 computer graphics system. Use of this system is described in detail in Appendix A. The two layouts are shown in Figures 3 and 4.

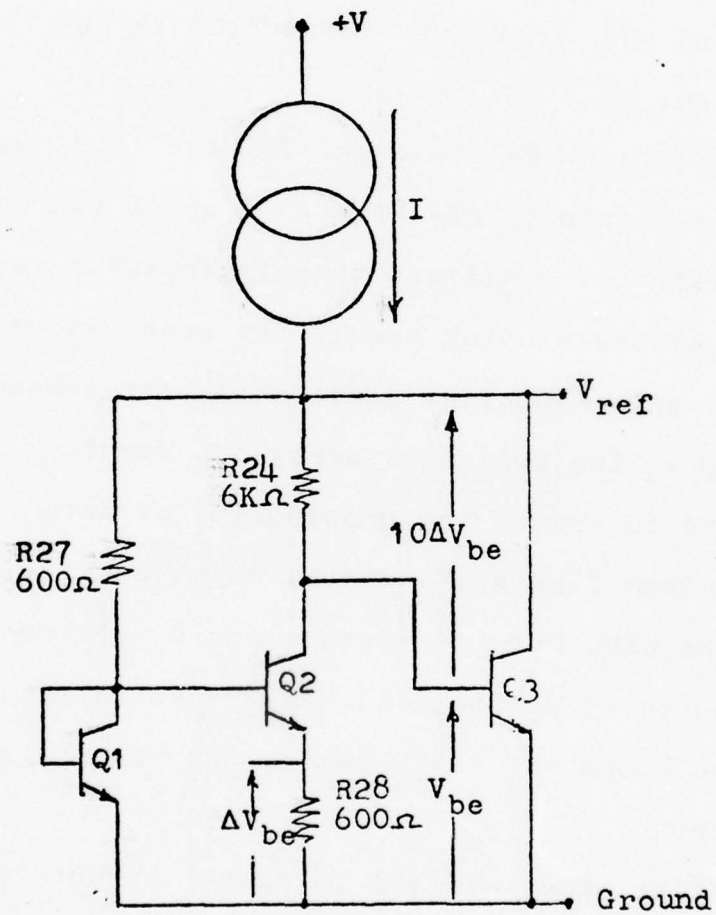


FIGURE 2. Schematic of band gap reference

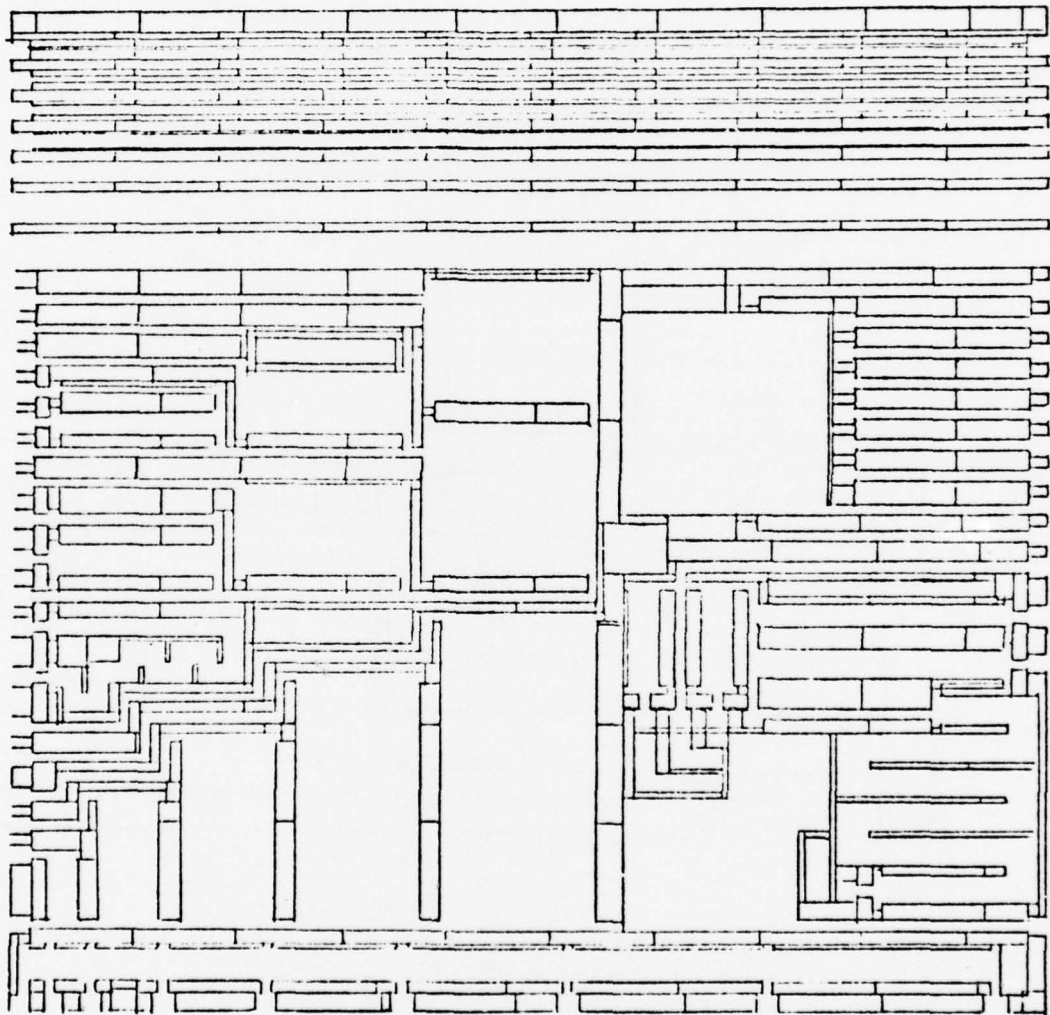


FIGURE 3. Computer graphics layout for IC conductor pattern

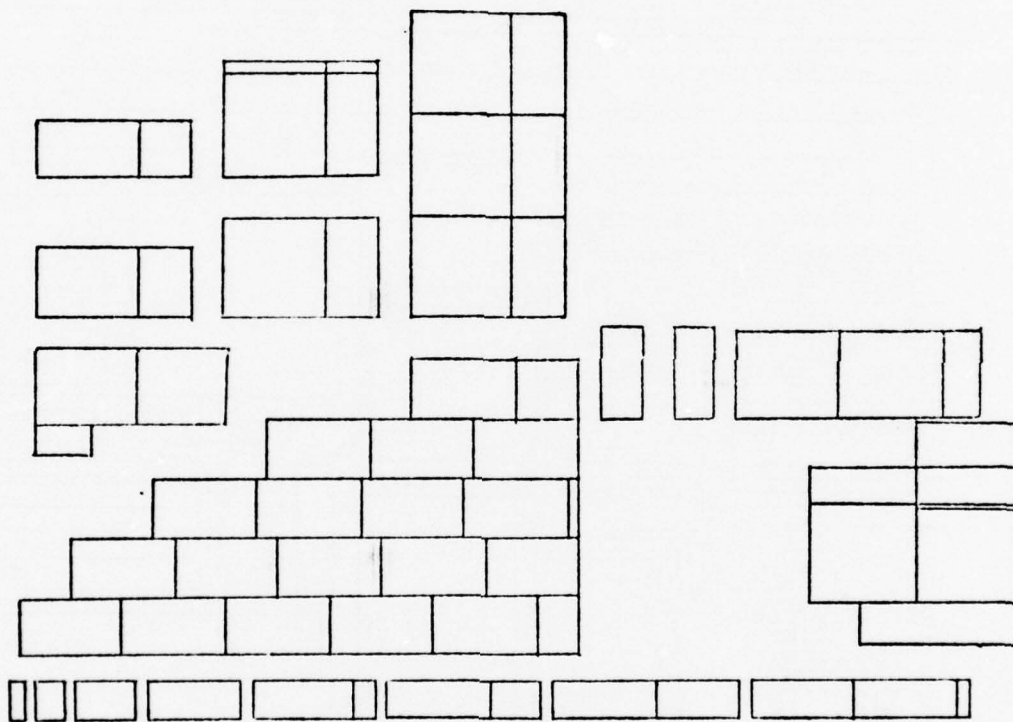


FIGURE 4. Computer graphics layout for IC resistor pattern.

### III. THIN FILM FABRICATION

#### Mask Production

The first step in fabrication is the mask production. In general there are two methods used for generation of thin film patterns. The first requires that the films be deposited on the substrate through a thin mask (usually metal) on which the pattern has been defined by holes etched all the way through (additive process). The second requires depositing the film over the whole substrate surface and then selectively etching the desired pattern (subtractive process).

Through-mask deposition is generally used when relatively large substrate areas need to be covered and where the smallest dimensions are greater than 2 mils [2]. This was not the case for the patterns discussed here. In addition, evaporation stencil masks suffer from the fact that completely connected patterns cannot be cut out of a mask without leaving the area circumscribed by such a pattern unsupported [2]. Use of through-masks was thus ruled out.

When selective etching is used it is necessary to have a photographic mask for each layer of film in the circuit. Traditionally these have been fabricated from large scale

drawings of the patterns. These drawings are photographed by special cameras and reduced to make master masks which are the size of the actual circuit. These masks are then used to make final contact masks on glass plates covered with a photosensitive emulsion.

The masks for this thesis were made using the Gyrex Model 1005 Pattern Generator. This system, shown in Figure 5, allows direct fabrication of the final contact masks without the intermediate steps. The Model 1005 consists of the electronics console, the optics housing, and the terminal assembly. The electronics console contains the microprocessor and interface electronics, paper tape reader, motor drivers, blower assemblies, power supplies, and switch panel. The optics housing contains the X-Y translation stage and motors, the aperture forming mechanism and its motors, the Xenon flash tube, high voltage power supply, and the optics. The terminal assembly contains a keyboard, display converter, and CRT display.

The process of making masks with this system consists of flashing the pattern as a series of rectangles onto a photosensitive glass plate resting on the X-Y stage. The glass plate is then developed by conventional techniques. Appendix A outlines the necessary steps for mask fabrication with this system. Figure 6 shows the two Gyrex produced masks used in this thesis.

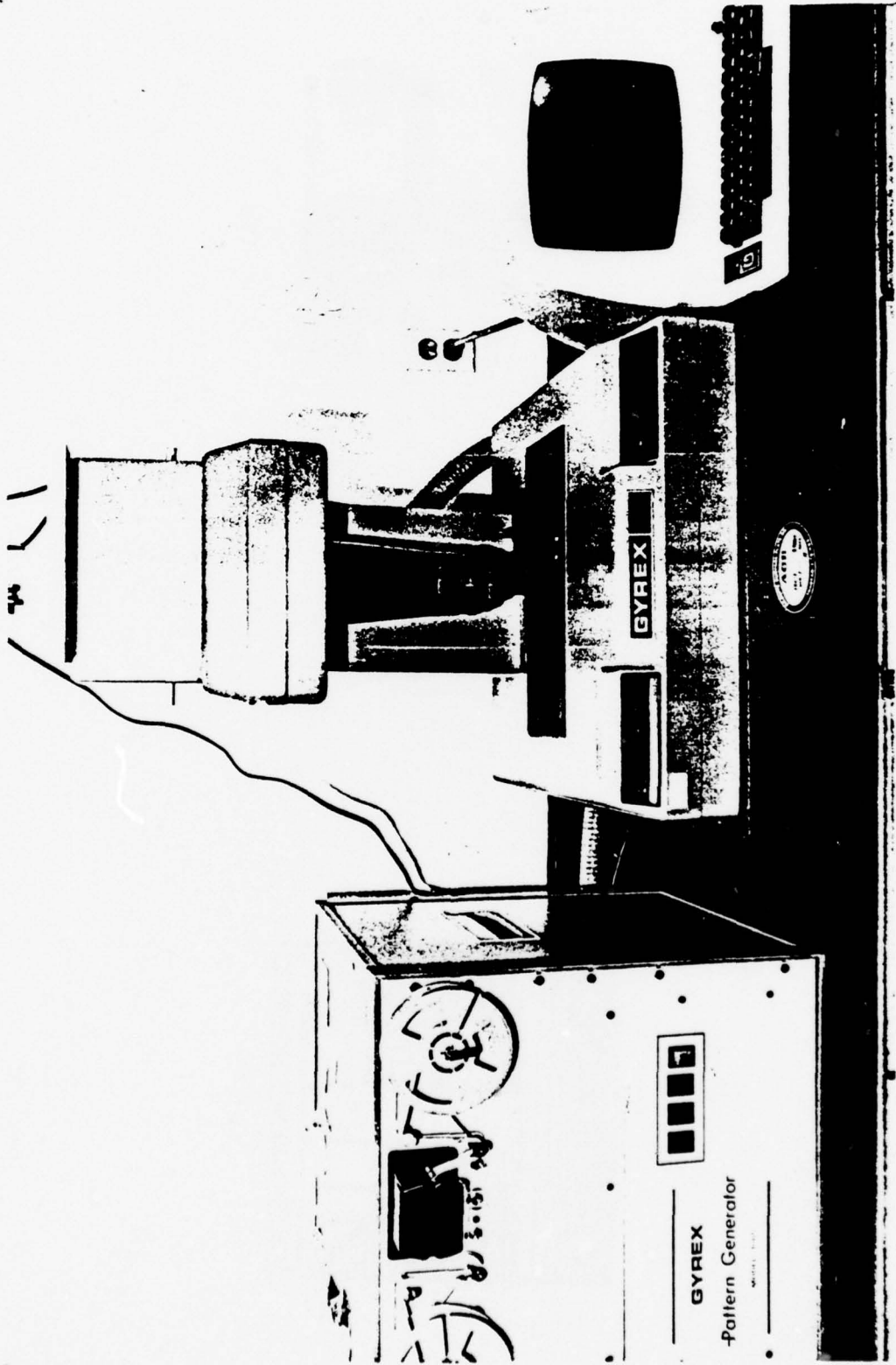
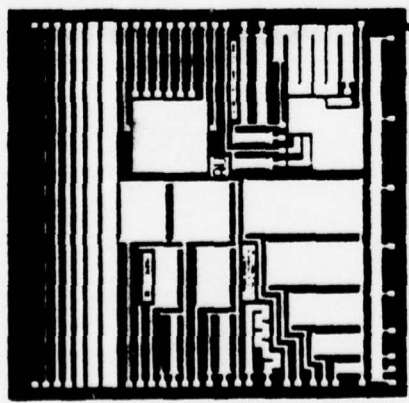


FIGURE 5. Gyrex Model 1005 pattern generator



(a)



(b)

FIGURE 6. Exposure masks for: a) conductor pattern and b) resistor pattern



### Preparation of Materials

It is of utmost importance that the substrates and source materials as well as the bell jar fixturing be clean before a film deposition is made.

The inside of the bell jar and the fixturing are cleaned by periodic wiping down with a solvent such as methanol or acetone. Because of their small size and mobility the substrates and source materials can undergo a more thorough cleaning procedure. This is especially important for the substrates. Indeed, the first few deposits were made on substrates that had undergone cleaning consisting only of an ultrasonic bath in methanol. The adhesion of the films deposited was totally unsatisfactory. When a piece of adhesive tape was applied to the films and peeled away, the films came off of the substrates with the tape. As a result a more rigorous cleaning sequence was instituted for the substrates. The steps in that sequence follow:

1. Five minute ultrasonic bath in LIQUINOX detergent.
2. Three stage de-ionized water rinse.
3. Two stage methanol rinse.
4. Nitrogen blow dry.
5. Thirty minute infrared oven bake at 150°C.

This last step should be performed just prior to the actual evaporation sequence. If the baked substrates are allowed to remain at atmospheric pressure for long they will absorb

moisture. All films that have been deposited on substrates cleaned in this manner have passed the scotch tape adhesion test. When cleaning any surfaces to be housed within the bell jar it is important to keep them free of oil and grease from the hands. For this reason dust free gloves should be worn during cleaning.

Once the cleaning is complete, the substrates can be loaded into the vacuum chamber and the various sources can be mounted. The substrates used for this study were loaded onto a custom made platform along with a glass resistance monitor of one square in size. Figure 7 shows this platform mounted in the bell jar fixturing. Charges of Kanthal and copper were loaded on the two filaments beneath the fixture hood (Figure 8). A length of about 1.75 inch of Kanthal A-1 wire was folded over and inserted into a tungsten wire basket (Mathis type B1-3X.025W). The copper used was in the form of 2 millimeter rods. Three of these (approximately 1 gram) were loaded into a tungsten wire basket (Mathis type B12B-3X.025W). In cases where substantial amounts of the source materials were left from the previous evaporation, the amounts of Kanthal and/or copper added was reduced accordingly. Size of these charges were large enough to guarantee that there would be ample material to reach desired sheet resistance and film thickness. Nomographs are available to more accurately determine the necessary charge size [9].

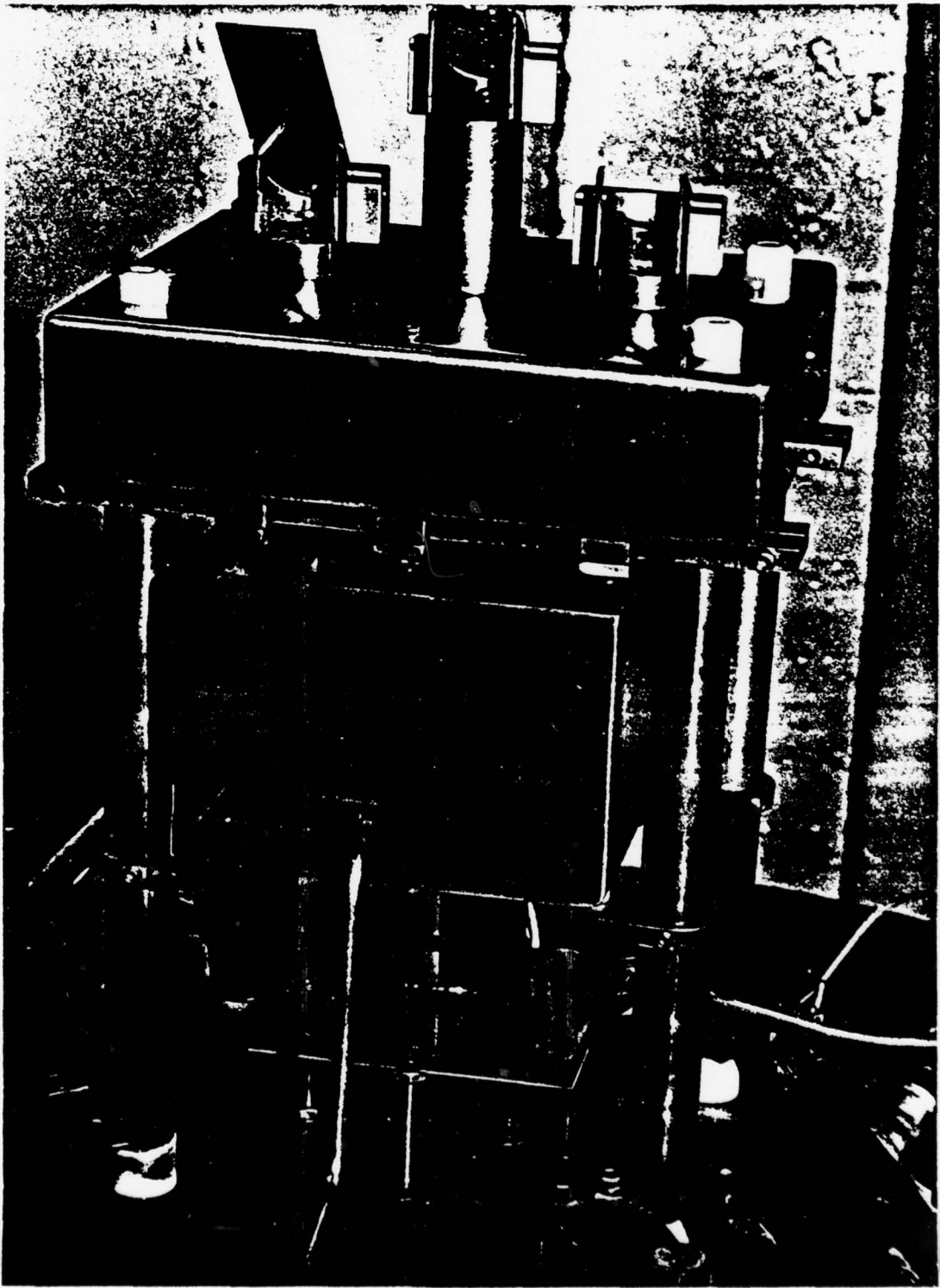


FIGURE 7. View of bell jar fixturing

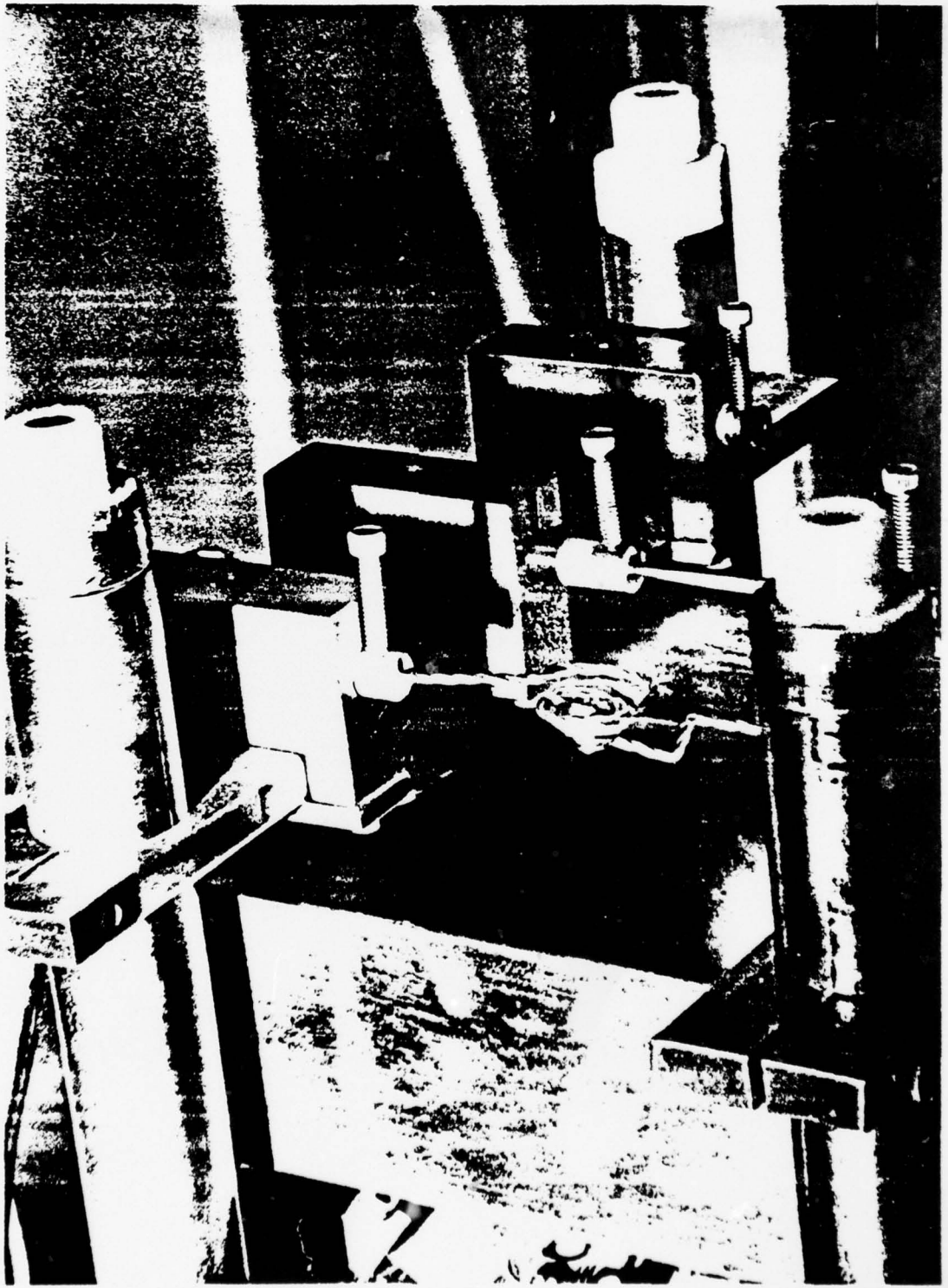


FIGURE 8. View of source filaments

### Film Deposition

When the materials are cleaned and loaded in the vacuum chamber, the next step in fabrication is the deposition of the film. The thin films were made in an NRC 3177 evaporator. This equipment was acquired as surplus property and restored by the author for this research. To deposit the films for the resistor arrays the vacuum chamber was pumped down to  $4 \times 10^{-6}$  torr via procedures listed in Appendix B.

The Kanthal was deposited first. Power supply current for the Kanthal filament was increased slowly and stabilized at 45 amps. When the current was stabilized the shutter covering the deposition window between the source and substrates was opened. The resistance monitor had been connected to an external ohmmeter by way of an electrical feedthrough. Once the meter indicated that the monitor's resistance had reached 200 ohms, the shutter was closed prohibiting further deposition.

The copper deposition was done in the same manner except that power supply current was set at 40 amps. Deposition was stopped when the copper thickness reached 10,000 angstroms according to the Kronos digital thickness monitor.

### Circuit Realization

Once the films are deposited on the substrate the desired circuit can be realized by selectively removing portions of the films. This is done by coating the film surface with a photoresist. The photoresist is exposed through photographic masks and the soluble portions of the resulting patterns are washed away in a developing sequence. This leaves "windows" in the photoresist through which the exposed films can be etched. There are two classes of photoresists; negative and positive. The negative resists become less soluble when exposed to light and produce the negative pattern of the mask. Positive resists become more soluble when exposed to light and yield a positive pattern of the mask. Negative resists are more common and cheaper but the positive resists offer the advantage of being easier to remove from the substrate. Negative photoresist was used in this thesis. The procedures used to etch the thin film resistor arrays are as follows:

1. The film coated substrates were removed from the bell jar and coated with Hunt HR-300 Negative Photoresist. The resist was spun on at 2000 RPM for 5 seconds followed by 5000 RPM at 15 seconds (Figure 9).
2. The photoresist was then exposed for 15 seconds on



FIGURE 9. Application of photoresist to substrate

the Colight M-99 (Figure 10) contact printer using the mask in Figure 6a.

3. The photoresist was developed revealing the pattern. The developing cycle consisted of 20 seconds in Hunt IC developer followed by 15 second rinses in IC thinner and isopropyl alcohol. Afterwards the substrate was blown off with nitrogen.
4. The first etch was done in ferric chloride for 5 seconds. The results are seen in Figure 11a. Occasionally the ferric chloride would remove the exposed copper but not the Kanthal underneath. When this happened a secondary etch in hydrochloric acid was used to remove the Kanthal.
5. Stripping the photoresist proved to be a problem, and numerous unsuccessful techniques were tried. Success was finally obtained by soaking the circuits in warm (80°C) Hunt Microstrip for one minute followed by a high pressure water rinse.
6. Photoresist was reapplied and exposed using the pattern in Figure 6b.
7. The pattern was developed as before but afterwards the circuit underwent a 15 minute nitrogen atmosphere bake at 65°C.
8. The final etch to form the resistors was done in concentrated nitric acid for about 3 seconds.



FIGURE 10. Colight M-99 contact printer

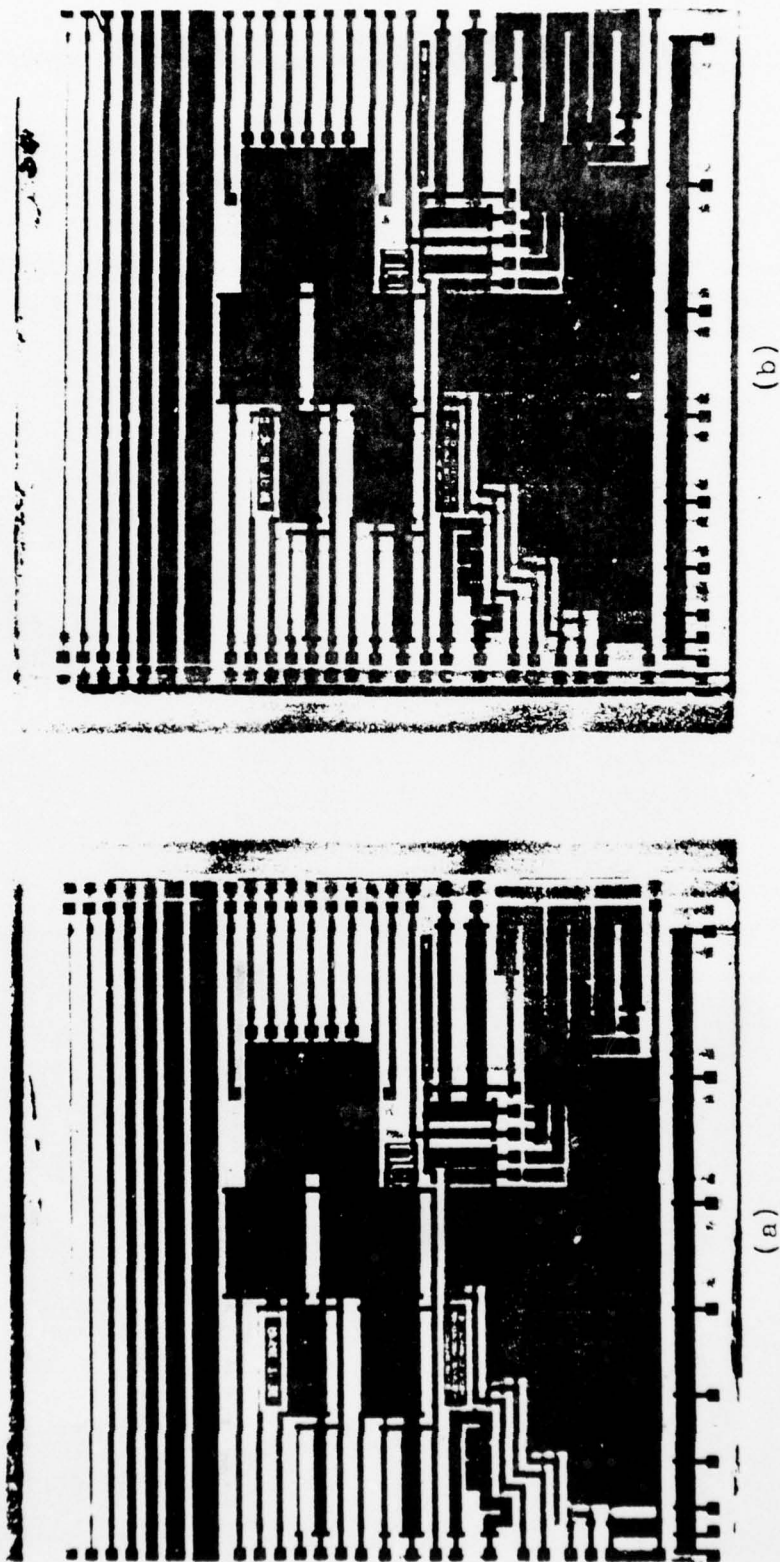


FIGURE 11. Thin film IC's on glass substrate: a) after first etch b) after final etch

Diluted acid was not used because it will etch Kanthal. The results are shown in Figure 11b.

9. Stripping of the final coat of photoresist rendered the circuit complete and ready for packaging and testing.

#### IV. CHARACTERIZATION AND MEASUREMENTS

##### Sample Selection

The processing steps described in the previous Chapter were developed over a period of several months; by carefully adjusting the steps, a photoresist process and a selective etch process were developed to yield thin film circuits which, under microscopic visual examination, appeared good. These circuits showed clear definition of the pattern, little surface contamination, sharp edge definition, and good film adhesion.

Samples of the circuits were chosen for testing from several different evaporation runs. With manual control of the evaporator filament current, however, it was very difficult to maintain identical conditions (particularly deposition rate) from one evaporation run to the next. For this reason, the samples used in comparing glass substrates to flexible substrates were all from the same run. This insured that any differences in circuit characteristics would not be due to different evaporation conditions. One glass substrate circuit from evaporation run number 6 and one from run number 8 were selected. Two each of the glass and Kapton samples were selected from evaporation run number 11 and used for comparing glass to flexible substrates. The

Kapton circuits from earlier runs were unacceptable primarily because during photoresist stripping, which required heating to 80°C, the films were severely thinned. This was ultimately corrected by reducing the time in the stripping solution to one minute. The glass samples were similar in appearance to the circuit shown in Figure 11b. The circuit in Figure 12 is typical of the Kapton samples.

#### Appearance

Visual inspection without magnification revealed the films on all samples appeared smooth and glossy. Those on Kapton were perhaps somewhat less reflective. Viewing under an optical microscope revealed that while the samples on glass looked smooth, the ones on Kapton appeared to have a grainy surface (This is confirmed in the scanning electron microscope photos discussed later). This is probably due to the smoother surface finish of the glass. If one examines a piece of Kapton that has no deposited film, it appears that the surface has many fine scratches. The presence of these scratches undoubtedly contributes to the graininess of the films on Kapton. Also, the differences in sticking coefficients of the two substrate materials may have been an important factor.

Viewing of the glass substrate circuits with a scanning electron microscope (SEM) revealed the copper films to contain small blister-like non-uniformities (See Figure 13). Except for the presence of these "blisters",

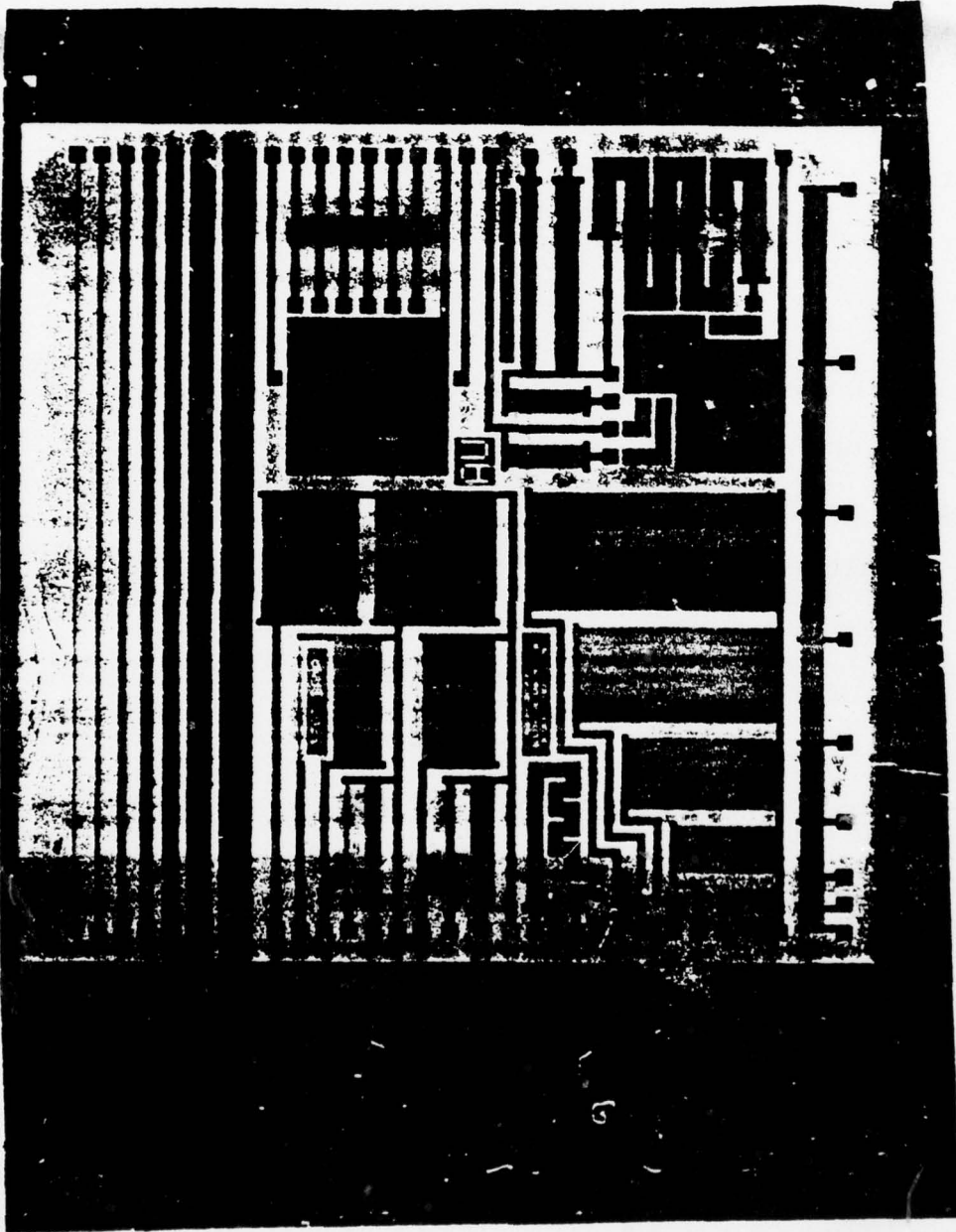


FIGURE 12. Thin film IC on Kapton substrate

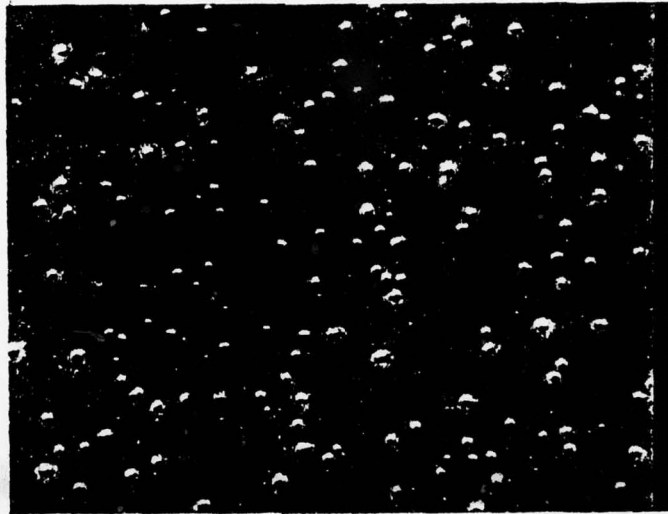


FIGURE 13. SEM photo of copper film on glass (5000X)



FIGURE 14. SEM photo of Kanthal film on glass (5000X)

the surface finish is smooth. Figure 14 is an electron microscope photo of Kanthal film on glass. The only noticeable non-uniformity is a small dust particle.

When the Kapton substrate circuits were viewed with the SEM the surface finish was quite different than the glass samples. Figure 15 is a photo of a copper film on Kapton. The "blisters" seen on the glass sample are not present but the film surface exhibits numerous irregularities. This is also evident in a photo of a Kanthal film on Kapton (Figure 16). The fact that these irregularities were not seen with the same films on glass substrates indicates that the irregularities are on the Kapton surface.

Overall line definition on the samples was reasonably good. There were isolated places on each of the circuits where small portions of photoresist had lifted causing unwanted etching of the metals. For the most part, however, this occurred in areas where the photoresist was in very thin strips such as at resistors 21 and 23 and the thinner conductors at the top (as viewed in Figure 1) part of the circuit.

Film uniformity was not always good. Numerous "pinholes" were noted in each of the samples. On some circuits, there were other areas where larger holes in the film appeared. On run number 11, there appeared to be some roughness on the body of resistor 7 on both glass substrates. This was not noticed on the Kapton samples but

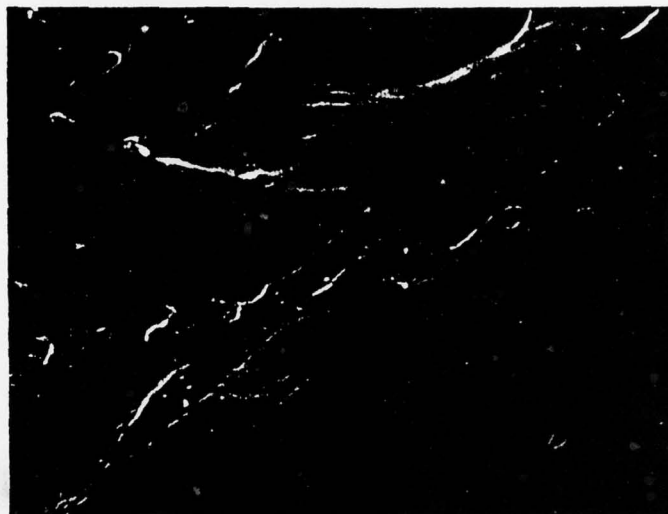


FIGURE 15. SEM photo of copper film on Kapton. (5000X)

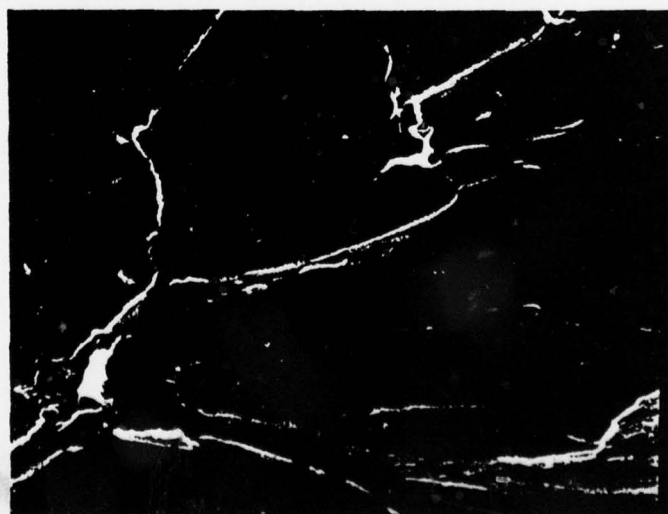


FIGURE 16. SEM photo of Kanthal film on Kapton (5000X)

with the graininess already mentioned slight roughness would be undetectable. However, when measurements were made, resistor 7 on all four substrates exhibited higher than normal resistance. This would point to a possible smear on the glass exposure mask, however, visual examination of the mask under a microscope revealed no smear.

#### Adhesion

All samples exhibited adequate adhesion. The scotch tape test, described in Chapter III, was done on each one and none of the films appeared to lift up. Although adhesion was adequate, care must be exercised during the processing of Kapton substrates. If these are left too long in the heated photoresist stripper, the films tend to become thinned as previously described.

The excellent adhesion of the copper-Kanthal system was one of the more interesting results of this work. Copper is well known for its extremely poor adhering qualities. All previous work (to this author's knowledge) involving evaporated copper films for microcircuit metalization used some special process technique for obtaining copper adhesion [14]. Usually, this was accomplished by evaporating first a resistive and good adhering material such as chromium. Before the chromium evaporation source is turned off, however, the copper source is activated so that there is some short period of time where both materials are

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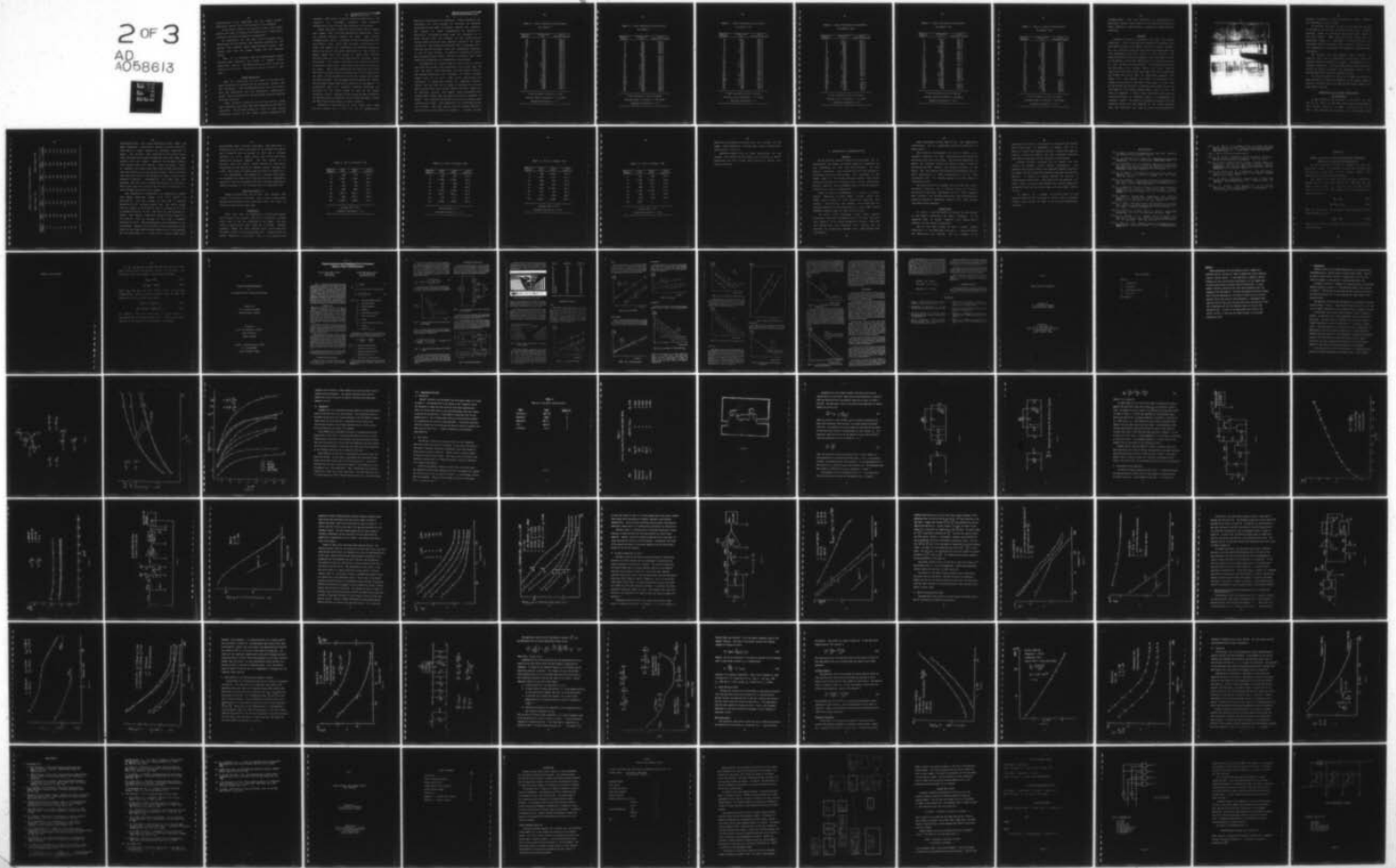
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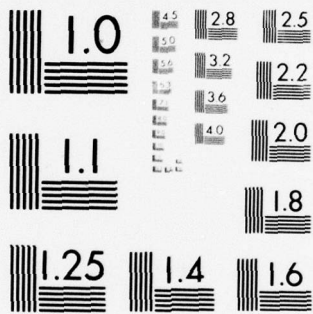
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simultaneously being deposited, and the copper becomes physically "locked" into the structure of the chromium.

It was found, however, in contrast to this, that copper adheres very well to Kanthal film without this interlocking procedure, and thus processing is simplified.

An evaporation run was made with a chromium source substituted for the Kanthal, but otherwise identical to the process that produced good copper-Kanthal circuits. The results were that the copper flaked off the chromium easily.

Thus, it is proposed that the copper-Kanthal system provides good adhesion, and allows a simple 2-step evaporation process. The actual mechanism which causes the adhesion is not known. Further work should be done in this area.

#### Sheet Resistance

When the evaporation for run number 11 was made, the sheet resistance as measured by the resistance monitor was 192 ohms/square. The corresponding values for runs 6 and 8 were 199 ohms/square and 193 ohms/square respectively. Actual sheet resistance for the processed circuits differed from this somewhat.

Sheet resistance values for the circuits done on glass were generally lower than the value measured at the time of deposition. The probable reason for this is that during processing several of the steps require heating of the

circuits. This heating tends to allow the molecules in the resistors to rearrange somewhat into preferred configurations which causes the resistance to decrease.

Sheet resistance values for the circuits done on Kapton were higher than the value measured at deposition. There are several possible reasons for this. The surface irregularities shown in Figures 15 and 16 undoubtedly have some effect. Also, since the sticking coefficients for glass and Kapton are different, and since the resistance monitor was glass, the sheet resistance of the films on Kapton might have been higher to begin with. Another possible cause has to do with the mounting problems during processing. The Kapton substrates were mounted on squares of glass for processing. The corners were held to the glass by epoxy. While this system held the substrate flat there was still a certain amount of stress put on the films during any part of the processing in which the samples were blown dry with nitrogen. Any nitrogen blowing between the Kapton and the glass caused high speed vibration of the Kapton. It is believed that this vibration possibly disturbed the structure of the films enough to lead to the higher resistance values. Thermal stress caused by heat treatments in the processing is probably not the cause as Table 1 shows the TCE of glass and Kapton are quite similar.

Resistance measurements in these tests were made directly across the resistor contacts to eliminate the

effects of interconnection resistance. Sheet resistance was calculated for each resistor by dividing the measured resistance by the number of squares between the contacts. The results of these measurements are detailed in Tables 2-7. It should be noted that all resistors on a given circuit were not included in the calculation of average sheet resistance and standard deviation of sheet resistance. Any obviously defective (open, large gap, etc.) resistor was not included. Also, the meandering resistors 14 and 24 were omitted. In addition, resistors 21 and 23 were excluded because their extreme narrowness make them especially susceptible to dimensional inaccuracies.

By comparing the results shown in Tables 2-5, it can be seen that the average sheet resistance varies less than 7% over the three runs considered, even with manual control. The standard deviations for resistors on these circuits ranged from 6.6 to 12.7. This shows good control and uniformity of deposition across the substrate surface. Tables 4-7 (all from run 11) allow a comparison of circuits made on glass with those using a Kapton flexible substrate. As described earlier, the Kapton sheet resistances were significantly higher than the same evaporation produced on glass. The standard deviations for devices on Kapton were exceptionally large. This indicates a non-uniformity across the circuit. The SEM photos show the Kapton used had a surface with a large number of randomly distributed surface

TABLE 2. Sheet Resistance Measurements  
On Sample 6

Resistor Number	Resistance ( $\Omega$ )	Sheet Resistance( $\Omega/\square$ )
1*	130	260.0
2*	235	235.0
3*	445	222.5
4*	597	199.0
5	696	174.0
6	817	163.4
7	933	155.5
8	1.05K	150.0
9*	532	265.0
10*	416	208.0
11	367	183.5
12	334	167.0
13	312	156.0
14*	4.65K	250.8
15*	1.30K	260.0
16*	3.33K	222.0
17	285	171.0
18	161	161.0
19	199	159.2
20	1.49K	198.7
21*	7.07K	235.7
22	420	168.0
23*	15.4K	256.7
24*	4.81K	160.3
25	1.19K	151.9
26	1.80K	153.2
27	460	153.3
28	464	154.7

\* not included in the following

Average sheet resistance =  $163.8\Omega/\square$

Standard deviation = 12.7

TABLE 3. Sheet Resistance Measurements  
On Sample 8

Resistor Number	Resistance ( $\Omega$ )	Sheet Resistance ( $\Omega/\square$ )
1*	121	242.0
2	175	175.0
3	336	168.0
4	489	163.0
5	631	157.8
6	778	155.6
7	924	154.0
8*	Open	-
9	334	167.0
10	346	173.0
11	338	169.0
12	330	165.0
13	323	161.5
14*	3.33K	179.6
15	826	165.2
16	2.71K	180.7
17	266	159.6
18	156	156.0
19	223	178.4
20	1.30K	173.3
21*	6.36K	212.0
22	423	169.2
23*	16.3K	271.7
24*	4.51K	150.3
25	1.23K	157.0
26	1.84K	156.6
27	468	156.0
28	469	156.3

\* not included in the following

Average sheet resistance =  $164.4\Omega/\square$

Standard deviation = 7.9

TABLE 4. Sheet Resistance Measurements  
On Sample 11GA

Resistor Number	Resistance ( $\Omega$ )	Sheet Resistance( $\Omega/\square$ )
1*	98.9	197.8
2	198	198.0
3	369	184.5
4	559	186.3
5	699	167.3
6	865	173.0
7*	1.28K	213.3
8	1.21K	172.9
9	354	177.0
10	347	173.5
11	341	170.5
12	337	168.5
13	339	169.5
14*	3.56K	192.0
15	884	176.8
16	2.84K	189.3
17	285	171.0
18	167	167.0
19	208	166.4
20	1.35K	180.0
21*	6.49K	216.3
22	428	171.2
23*	15.4K	256.7
24*	5.15K	171.7
25	1.34K	171.1
26	2.00K	169.8
27	502	167.3
28	502	167.3

\* not included in the following

Average sheet resistance =  $174.5\Omega/\square$

Standard deviation = 8.2

TABLE 5. Sheet Resistance Measurements  
On Sample 11GB

Resistor Number	Resistance ( $\Omega$ )	Sheet Resistance ( $\Omega/\square$ )
1	94.6	189.2
2	180.9	180.9
3	352	176.0
4	525	175.0
5	691	172.8
6	861	172.2
7*	1.27K	211.8
8	1.24K	176.6
9	342	171.0
10	335	167.5
11*	352	176.0
12*	363	181.5
13	331	165.5
14*	3.57K	192.6
15*	1.12K	224.0
16*	3.30K	220.0
17*	292	175.2
18	167	167.0
19	210	168.0
20*	1.53K	204.0
21*	Open	-
22	421	168.4
23*	Open	-
24*	5.28K	176.0
25	1.41K	184.9
26	2.15K	183.0
27	527	175.7
28	527	175.7

\* not included in the following

Average sheet resistance =  $174.7\Omega/\square$

Standard deviation = 6.6

TABLE 6. Sheet Resistance Measurements  
On Sample 11KA

Resistor Number	Resistance ( $\Omega$ )	Sheet Resistance ( $\Omega/\square$ )
1	125.5	251.0
2	391	391.0
3	612	306.0
4	914	304.7
5	1.228K	307.0
6	3.18K	636.0
7*	Open	-
8	1.996K	285.1
9	452	226.0
10	454	227.0
11	448	224.0
12	531	265.5
13	667	333.5
14*	Open	-
15	1.326K	265.2
16*	Open	-
17	352	211.2
18	225	225.0
19	322	257.6
20	2.03K	270.7
21*	18.02K	600.7
22	571	228.4
23*	19.2K	320.0
24*	6.65K	221.7
25*	Open	-
26	2.56K	217.9
27	810	270.0
28	709	236.3

\* not included in the following

Average sheet resistance =  $282.8\Omega/\square$

Standard deviation = 90.2

TABLE 7. Sheet Resistance Measurements  
On Sample 11KB

Resistor Number	Resistance ( $\Omega$ )	Sheet Resistance ( $\Omega/\square$ )
1	196	392.0
2	301	301.0
3	494	247.0
4	748	249.3
5	1.13K	282.5
6	1.94K	388.0
7*	3.48K	580.0
8	1.93K	275.7
9	537	268.5
10	525	262.5
11	514	257.0
12	455	227.5
13	454	227.0
14*	5.19K	280.0
15	2.16K	432.0
16	9.56K	637.3
17	355	213.0
18	215	215.0
19	307	245.6
20*	Open	-
21*	Open	-
22	536	214.4
23*	18.49K	308.2
24*	7.05K	250.0
25	1.82K	238.7
26	2.74K	233.2
27	793	264.3
28	704	234.7

\* not included in the following

Average sheet resistance =  $286.7\Omega/\square$

Standard deviation = 96.2

irregularities. Thus the variation of resistance for a particular resistor would depend on its position relative to these substrate imperfections, leading to a high standard deviation.

### Flexing

Flexing, of course, is possible only with the Kapton substrates. Also, only certain resistors are situated such that their values can be easily monitored during flexing. All the resistors used for this test had contact pads that were accessible on the left border of the circuit. The epoxy was removed from the righthand upper and lower corners of the Kapton so that the right side of the circuit was free to lift up from its glass holder. The resistor pads along the left side of the circuit (which were still anchored down) were then probed while the right side of the substrate was folded over with a pair of insulating tweezers (See Figure 17). The Kapton was flexed in this manner to a radius of curvature of less than 1 centimeter. It may seem at first that the effects of flexing would depend in part on the length of the resistor being flexed. This is not the case as Appendix C shows that the effect of flexing on percentage change in resistor values is independent of resistor length. The value of resistance measured with the substrate folded over was compared to the value measured when the substrate was flat to determine the effects of

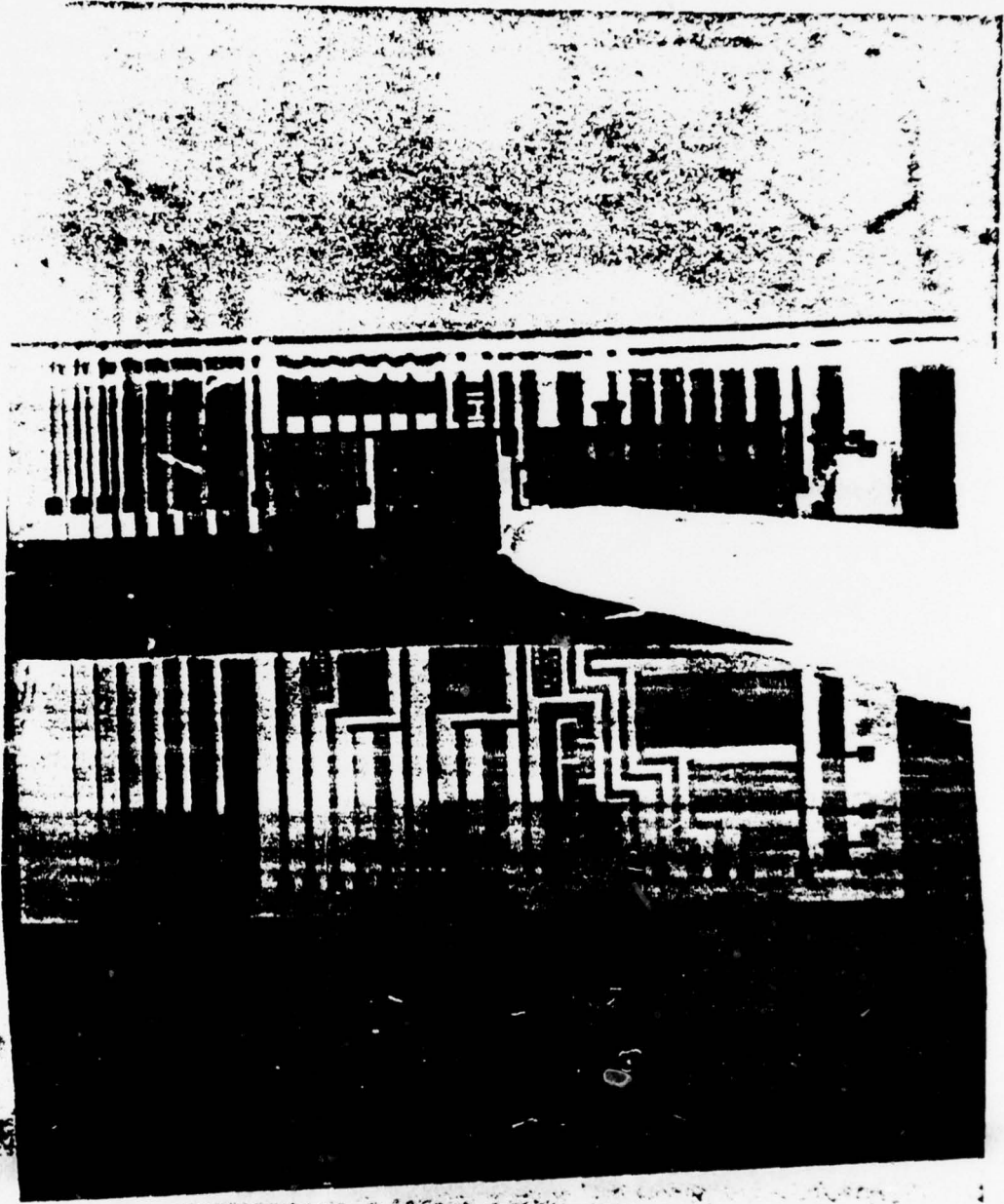


FIGURE 17. Kapton substrate under flexing

flexing. In general, effect on resistance values amounted to a decrease of 0.6% or less.

To determine how much, if any, of this decrease was due to flexing in the resistor interconnections lines, isolated conductor paths at the top of the circuits were tested in the same manner. When this was done, there was no measurable change in resistance. It follows that all the resistance changes measured in the previous flexing tests are essentially independent of changes in interconnection resistance.

The results from the flexing tests, outlined in Table 8, show that it is possible to fabricate a thin film resistor/conductor network in a planar configuration on a flexible substrate, and then subsequently fold or bend the circuit to greatly increase the packaging density while maintaining nearly constant resistor values.

It will be noted that there are a higher percentage of open resistors on Kapton as compared to the glass samples. However, resistors that were open on the Kapton samples were open before flexing.

#### Temperature and Voltage Coefficients Of Resistance

It was decided to use equation (II-3) with T1 at 25°C and T2 at 150°C to determine temperature coefficients of these samples. Because the high temperature was to be 150°C, the selected samples were given a five minute, 200°C

TABLE 8. Effect of Flexing on Resistance

Kapton Sample 11KA

Kapton Sample 11KB

Resistor Number	Kapton Sample 11KA			Kapton Sample 11KB		
	R( $\Omega$ ) flat	R( $\Omega$ ) flexed	% change	R( $\Omega$ ) flat	R( $\Omega$ ) flexed	% change
9	452	452	0.0	537	537	0.0
10	454	454	0.0	525	525	0.0
11	448	448	0.0	514	514	0.0
12	531	530	-0.2	455	455	0.0
13	667	665	-0.3	454	452	-0.4
15	1.326K	1.322K	-0.3	2.16K	2.15K	-0.5
17	352	350	-0.6	355	353	-0.6
18	225	224	-0.4	215	214	-0.5
19	322	321	-0.3	307	306	-0.3

stabilizing bake. This caused oxidation of the copper, and made subsequent connection to resistor contacts difficult. This was not a major problem on resistors deposited on glass. The pressure was increased on the contact probes until the probe tips broke through the oxide and made good contact with the copper. However, on the Kapton sample, this creates severe difficulties. Since, by design, Kapton is flexible, the sharp probe tips used to make measurements with the resistors on glass cannot be used. This is because they tend to go all the way through the Kapton circuits when pressure is applied. Consequently, new probe tips were designed and fabricated to make measurements on the Kapton. These probe tips have a blunt tip and thus are difficult to force through the oxide on the copper.

The temperature coefficients of resistance on sample 11GA (glass substrate) ranged from 41.6 ppm/°C to 58.3 ppm/°C, with an average of 48.2 and a standard deviation of 5.8. On glass sample 11GB, the TCR's ranged from 38.1 ppm/°C to 66.6 ppm/°C, with an average of 47.6 and a standard deviation of 7.8. The TCR's for the resistors on sample 11KA (Kapton substrate) ranged from 72.5 ppm/°C to 151.4 ppm/°C, with an average of 96.5 and a standard deviation of 23.6. These measurements were performed in air environment. Because of the severe oxidizing problem of the copper at the high stabilization temperature, it was decided that the measurement on the other Kapton sample (11KB) would

be performed under a stream of nitrogen. This made quite a difference as the TCR's were found to be between 30.4 ppm/°C and 71.8 ppm/°C, with an average of 46.2 and a standard deviation of 12.5. These values are in line with those measured on the glass samples. For this reason, it is believed that the poorer values recorded for 11KA were a consequence of the problem of making contact through the oxide. The results of these tests are shown in Table 9-12.

As anticipated (see Chapter II), voltage coefficients of resistance for these thin film circuits were negligible. Resistors 6 and 10 on samples 11GA and 11KB were measured at applied voltages of 2 to 20 volts with no measureable VCR.

#### Long Term Stability

Sample circuits from run 8 have been studied with respect to long term stability. Resistances on these glass samples were monitored over a two month span. No trend to drift was noted during that time.

#### Reliability

There have been no quantitative reliability studies done on any of the samples. The chief reliability problem would seem to be the oxidation of the copper. For this reason, a passivating coat would be desirable. Another possible remedy for this problem would be to treat the finished circuits in an electroless plating solution such as ATOMEX (Engelhard Industries). This solution works on the

TABLE 9. TCR's of Sample 11GA

Resistor Number	R( $\Omega$ ) 25°C	R( $\Omega$ ) 150°C	TCR (ppm/°C)
3	368	370	43.5
8	1.205K	1.212K	46.5
10	346	348	46.2
13	340	342	47.1
15	884	889	45.2
18	166.9	168.1	57.5
19	206	207.5	58.3
20	1.345K	1.352K	41.6

---

Average TCR = 48.2

Standard deviation = 5.8

---

TABLE 10. TCR's of Sample 11GB

Resistor Number	R( $\Omega$ ) 25°C	R( $\Omega$ ) 150°C	TCR (ppm/°C)
3	352	354	45.5
8	1.240K	1.247K	45.2
10	336	338	47.6
13	331	333	48.3
15	1.129K	1.135K	42.5
18	168.1	169.5	66.6
19	210	211	38.1
20	1.539K	1.548K	46.8

---

Average TCR = 47.6

Standard deviation = 7.8

---

TABLE 11. TCR's of Sample 11KA

Resistor Number	R( $\Omega$ ) 25°C	R( $\Omega$ ) 150°C	TCR (ppm/°C)
3	993	1.002K	72.5
8	3.17K	3.23K	151.4
10	492	497	81.3
13	803	813	99.6
15	1.43K	1.447K	95.1
18	424	428	75.5
19	451	456	88.7
20	2.96K	3.00K	108.1

---

Average TCR = 96.5

Standard deviation = 23.6

---

TABLE 12. TCR's of Sample 11KB

Resistor Number	R( $\Omega$ ) 25°C	R( $\Omega$ ) 150°C	TCR (ppm/°C)
3	526	528	30.4
8	2.00K	2.01K	40.0
10	548	551	43.8
13	469	472	51.2
15	2.23K	2.25K	71.8
18	222	223	36.0
19	318	320	50.3
20	Open	-	-

---

Average TCR = 46.2

Standard deviation = 12.5

---

basis of ion exchange and would leave the surface of the copper interconnections covered with a layer of gold which would inhibit corrosion.

One glass sample from an early evaporation run was treated with ATOMEX and then heated for 5 minutes at 200°C. Afterwards, the gold plated interconnections showed very little oxidation.

## V. CONCLUSIONS & RECOMMENDATIONS

### Results

One of the most positive results of this study was in establishing the copper on Kanthal system as a feasible low cost technology for thin film microcircuits. To this author's knowledge, this research was the first attempt to investigate this thin film scheme. The corrosion of the copper seems to be the only serious problem. This can be solved by treating the finished circuit with an electroless plating solution such as ATOMEX, manufactured by Engelhard Industries, as shown in Chapter IV.

There are numerous advantages of the copper on Kanthal system. Replacing precious metal conductor paths with copper would result in very significant material cost savings. Additionally, the Kanthal wire (often used for heating elements) is less expensive than most high purity elements commonly used for thin film resistors.

In prior work utilizing copper films, special processing requiring overlapping evaporations was necessary (see Chapter IV) to obtain acceptable adhesion. This work has demonstrated that excellent film adhesion can be achieved by evaporating Kanthal and copper without this overlapping.

Other advantages include ease of use, low temperature coefficients, and no measureable long term drift over a 2 month period.

This research investigated the use of Kapton as a flexible substrate for thin film microcircuits using the previously described technology. The circuits deposited on Kapton are somewhat inferior to those on glass in terms of uniformity and TCR. However, the irregular surface of the Kapton and the problems encountered with mounting, have at least contributed to these shortcomings. It is very encouraging that the flexing caused very little change in resistance values.

The data presented in Chapter IV shows that the largest resistance deviation for a circuit flexed to a radius of curvature of less than 1 centimeter is .6%. This suggests that circuits can be fabricated using this technology and folded to conform to packaging requirements, with greatly increased packing density.

#### Suggestions

As shown in the SEM photos of Chapter IV, the surface of the Kapton substrates was quite irregular. It is suggested that in further research work, Kapton with a smoother surface finish be obtained.

One of the main causes of poor circuit yield, especially in the beginning, was the difficulty with which the photoresist was removed. For this reason, it is

suggested that positive photoresist be considered for future work of this type. As mentioned in Chapter III, it is easier to remove than negative resists. Unlike the negative resists, it does not require the hot stripping solutions that were so hazardous to the circuits in this study.

Another problem, although not as severe, was the control of filament current during evaporation. The operation was totally manual and required constant vigilance to combat current surges that occurred when the sources were melting. A method is needed whereby the current is automatically controlled. This would free the operator for other tasks and would also promote more uniform deposition parameters from one run to the next, and allow some control of TCR.

In Chapter IV, a number of possible causes for the non-uniformity of the resistors on Kapton were discussed. Further work should be done to isolate the mechanism(s) involved.

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## APPENDIX C

### Effect of Resistor Length on Percentage Resistance

#### Change of Flexed Thin Film Resistors

It was previously stated in Chapter IV that the percentage change in resistance of thin film resistors due to flexing is independent of the resistor length. The following is a proof of that statement.

Two resistors are made from the same sheet resistance. Resistor  $R_A$  has width  $w$  and length  $L_A$ . Resistor  $R_B$  has width  $w$  and length  $L_B$ .  $L_B = xL_A$  and  $R_B = xR_A$ . Both resistors can be said to be composed of series increments of value  $R_n$  such that:

$$R_A = nR_n \quad (C-1)$$

$$\text{and } R_B = xnR_n. \quad (C-2)$$

When an incremental  $R_n$  is flexed uniformly end to end its value becomes  $R_{nf}$  and

$$R_{nf} = yR_n \quad (C-3)$$

where  $y$  is a constant dependent upon the radius of curvature of the flexing.

APPENDIX A and B DELETED

If  $R_A$  and  $R_B$  are oriented the same way and are flexed end to end an equal and uniform radius of curvature, the series  $R_n$ 's will all change a like amount such that

$$R_{Af} = nyR_n \quad (C-4)$$

$$\text{and } R_{Bf} = xnyR_n \quad (C-5)$$

where  $R_{Af}$  and  $R_{Bf}$  are the flexed values of  $R_A$  and  $R_B$  respectively. The ratio of the flexed value of the two resistors to the original value gives:

$$R_{Af}/R_A = nyR_n/nR_n = y \quad (C-6)$$

$$\text{and } R_{Bf}/R_B = xnyR_n/xnR_n = y. \quad (C-7)$$

It follows from this that the percentage change in resistance due to flexing depends on the radius of curvature and not on the length of the resistor being flexed.

Part 3

CHARACTERIZATION AND MODELING  
of  
LOW-FREQUENCY NOISE IN THICK-FILM RESISTORS

Prepared for  
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## Characterization and Modeling of Low-Frequency Noise in Thick-Film Resistors\*

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**Abstract** — State-of-the art hybrid thick-film resistors contain both low frequency ( $1/f$ ) and thermal noise which severely limits their application in the design of low signal level hybrid amplifiers. In this paper an experimental characterization of the noise in state-of-the-art thick-film resistors is presented and a noise model developed which is useful for both computer-aided low noise circuit design and the design of low noise resistors. The noise model developed is independent of geometrical effects and indicates that the noise performance of thick-film resistors can be specified completely in terms of a single resistor "material constant",  $K'$ . The model is shown to be in very good agreement with experimental data. Finally, areas for further work are indicated.

### INTRODUCTION

Thick-film resistors have been used for many years in hybrid microelectronic technology. An important application of this technology is the design and fabrication of linear amplifiers and systems which are capable of detecting very low signal levels. Since the ability of a system to detect low-level signals is fundamentally limited by the noise generated in the system, noise performance becomes an important design criteria. In order to design low noise hybrid circuits and systems, models must be available to predict the noise performance of the individual components of the hybrid circuit.

The purpose of this paper is to present the noise spectral response of resistors fabricated from three commonly used thick-film resistive inks manufactured by EMCA, ESL, and DuPont. Experimental results are presented to support the validity of a mathematical model which is especially suited to thick-film resistor technology.

Earlier investigations have developed models to describe the low-frequency noise characteristics of discrete resistors, and some limited work on thick-film resistors. These studies have tended to concentrate on the  $1/f$  or excess noise regions of the spectral response and assume the thermal noise to be negligible in the frequency band of interest. However, with modern thick-film resistors exhibiting noise performance superior to some discrete type resistors, both  $1/f$  and thermal noise may dominate in portions of the frequency band of interest.

It is therefore important to develop a new noise model which will simply and accurately describe thick-film resistor noise performance including both thermal and  $1/f$  noise.

### LOW-FREQUENCY NOISE MODEL

There are two types of noise found to dominate the noise spectral response of thick-film resistors; thermal noise (Ref. 1).  $e_{th}^2$ , which is given by

$$e_{th}^2 = 4kTR\Delta f \quad (1)$$

and,

excess noise or  $1/f$  noise (Ref. 2), which is given by

$$e_{ex}^2 = K \left( \frac{I_{dc}^2}{f^\alpha} \right) \Delta f R^2 \quad (2)$$

where,  $e_{th}^2$  = Mean square thermal noise voltage

$k$  = Boltzmann's Constant

$T$  = Absolute Temperature

$R$  = Resistance

$\Delta f$  = Noise Bandwidth of the system

$e_{ex}^2$  = Mean square excess noise

$K$  = Constant

$I_{dc}$  = dc current through the thick-film resistor

$f$  = Frequency

$\alpha$  = Constant ( $.5 \leq \alpha \leq 1.5$ )

The constant  $K$  in Equation (2) has been found in previous work (Ref. 3-6) to be dependent on the geometry and the material used in fabrication of the thick-film resistor as

$$K = K' \left( \frac{\rho}{\ell w t} \right) = K' \left( \frac{\rho_s}{\ell w} \right) \quad (3)$$

where,  $\ell$  = Length of the thick-film resistor

$w$  = Width of the thick-film resistor

$t$  = Thickness of the thick-film resistor

$\rho$  = Bulk resistivity (ohm · cm)

$\rho_s$  = Sheet Resistivity (ohms-per-square)

\*Parts of this work were presented at the 1976 International Microelectronics Symposium, Vancouver, B.C., Canada (Ref. 8).

The factor  $K'$  in Equation (3) is a new "material constant" which is dependent only on the firing conditions and the resulting microstructural properties of the resistor material (Ref. 3, 6). It is independent of the thick-film resistor geometry but it may exhibit some second-order dependence on  $\rho_s$  in cases where the microstructure is altered as the resistivity is changed. Using equations (1), (2), and (3) we obtain an expression for the total noise of a thick-film resistor including geometrical factors as

$$e^2_{TOT} = 4kTR\Delta f + K' \left( \frac{I_{dc}^2}{f\alpha} \right) \left( \frac{\rho_s^3 l}{w^3} \right) \Delta f \quad (4)$$

Equation (4) gives an expression for determining the entire noise spectral output of a thick-film resistor as a function of frequency. Figure 1 shows a typical plot of the thick-film

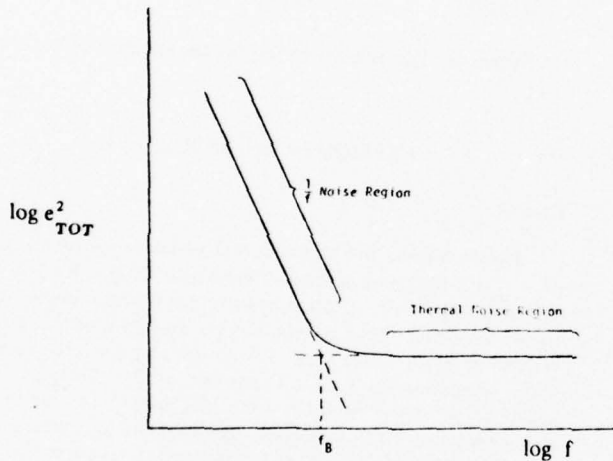


Figure 1. A typical thick-film resistor low-frequency noise spectra response.

resistor noise voltage versus frequency. The break frequency,  $f_B$ , occurs when the thermal and excess noise components are equal in magnitude. From equation (4)

$$f_B = \left( \frac{K'}{4kT} \right) \left( \frac{\rho_s^2 I_{dc}^2}{w^2} \right) = \left( \frac{K'}{4kT} \right) E^2 = (\text{constant})(E^2) \quad (5)$$

where,  $E$  = electric field across the length of the thick-film resistor.

This important relationship predicts that  $f_B$  is proportional to the square of the electric field ( $E$ ) and anything done to reduce the electric field in a thick-film resistor, for constant  $R$ , will reduce resistor noise. Equation 5 also indicates that resistor designs which increase  $E$ , at constant  $R$ , cause increased noise.

### EXPERIMENTAL PROCEDURE

Previous experimental investigations of the noise in thick-film resistors have neglected the effect of contacts or terminations on the noise performance (Ref 4, 5). In this work, contact effects are eliminated by the use of the special 4-terminal resistor test structure as shown in Figure 2. Details of the experimental method have been presented elsewhere (Ref. 7).

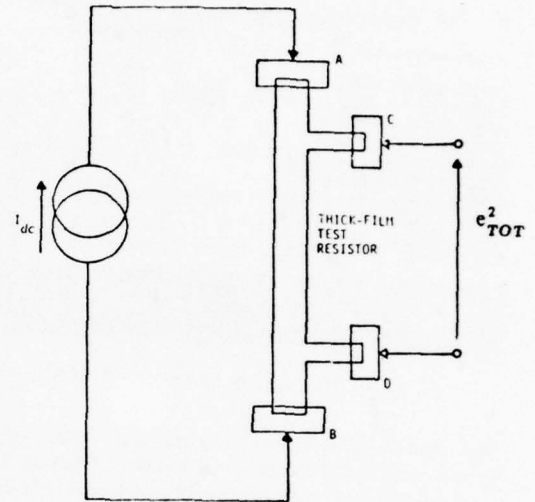


Figure 2. Circuit configuration used to exclude contact noise from measurement.

The actual circuit used in the measurement system is given in Figure 3, which uses the "comparison with a sinusoid technique" to measure equivalent input noise (Ref. 7).

For the measurement system actually used as shown in Figure 3, the experimental error is conservatively estimated to be approximately  $\pm 10$  percent. However, scatter in the data is also affected by variation of parameters external to the measurement system, such as noise pickup and variation of geometrical dimensions of the thick-film resistor, etc.

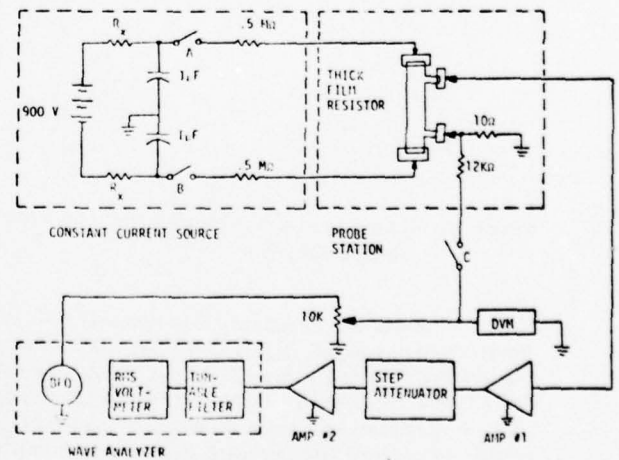


Figure 3. Actual Measurement System.

The thick-film resistor test samples were fabricated in the microelectronic laboratory of the U.S. Army Missile Research and Development Command, Huntsville, Alabama. A sample is shown pictorially in Figure 4a, and further descriptions in Figures 4b and 4c.

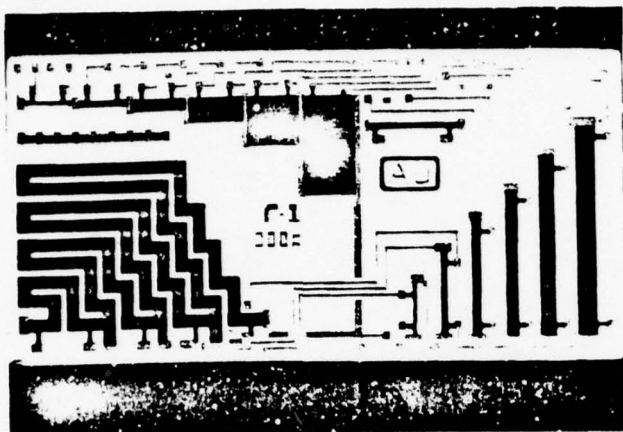


Figure 4a. Photograph of Resistor Test Sample.

The three resistive pastes used are ESL 3000 series (iridium based) with 8835-1B gold conductor, DuPont 1400 series (ruthenium based) with 8760 gold conductor, and EMCA 5000 series (ruthenium based) with Firon 212B gold conductor.

Each type ink was mixed for six nominal values of sheet resistance: 1  $\Omega$ , 10  $\Omega$ , 100  $\Omega$ , 1 k $\Omega$ , 10k $\Omega$ , and 100 k $\Omega$ . These pastes were checked with a Haake viscometer to ensure compliance with the manufacturer's specifications. Various numbers of samples were fabricated from each of the 6 resistivities for each of the 3 inks for a total of 114 samples. The samples were fired according to the manufacturer's specifications.

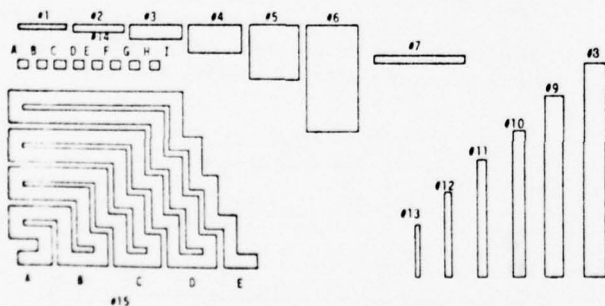


Figure 4b. System of resistor identification on a particular substrate (sample).

The geometric variations incorporated into the test resistor patterns are (see Figure 4a and 4b): 1) constant length, variable width resistors #1-6; 2) constant aspect ratio, resistors #7, #11, and 3) constant width, variable length resistors #15. In addition, two extra resistors, #7 and #14, are provided: one normal and one with extra terminations included vertically in the body of the resistor, but both having the same total number of squares and same width. This was done in order to allow some insight as to the effect of resistor contacts on the noise performance.

Resistor	Length (cm)	Width (cm)
#1	.254	.025
#2	.254	.051
#3	.254	.012
#4	.254	.203
#5	.254	.406
#6	.254	.813
#7	.610	.051
#8	1.52	.152
#9	1.27	.127
#10	1.02	.102
#11	.762	.076
#12	.508	.051
#13	.254	.025
#14 AI	.762	.051
#15 AE	13.7	.102
#15 BE	8.38	.102
#15 CE	4.27	.102
#15 DE	1.44	.102

Figure 4c. Dimensions of  $R_N$  for the resistors indicated.

## EXPERIMENTAL RESULTS

### Length

Figure 5 gives the experimental variation of excess noise,  $e_{ex}^2$ , as a function of thick-film resistor length, for the three different inks with all other resistor parameters and measurement frequency held constant. The lengths available on the resistor samples range from 1.5 cm to 13.7 cm. The nominal sheet resistance, ( $\rho_s$ ), of the samples used is 100  $\Omega/\square$ . The actual slope of the curves is given in Figure 5. As can be seen the slopes are approximately one as predicted by Equation (4). As previously stated, the experimental error in this work was estimated to be  $\pm 10$  percent (Ref. 17).

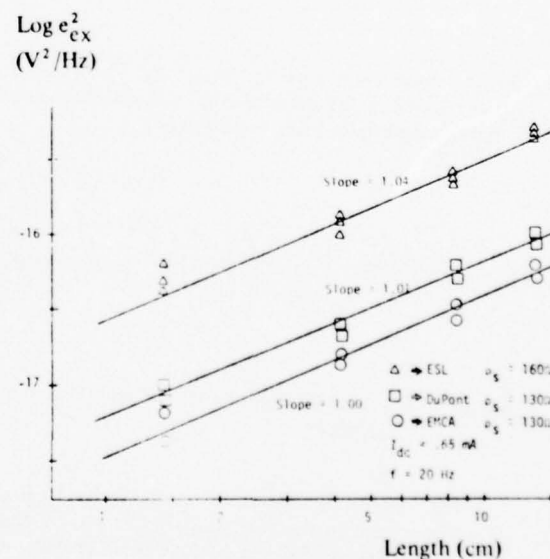


Figure 5.  $e_{ex}^2$  versus resistor length

Width

An experimental curve for  $e_{ex}^2$  versus  $(1/\text{width})^3$  is given in Figure 6. (Again, all other parameters are held constant.) From Equation (4),  $e_{ex}^2$  is expected to be inversely proportional to  $(2/\text{width})^3$ . The actual slope of the curves is presented in Figure 6. As can be seen, the slopes are approximately one, indicating agreement within experimental accuracy.

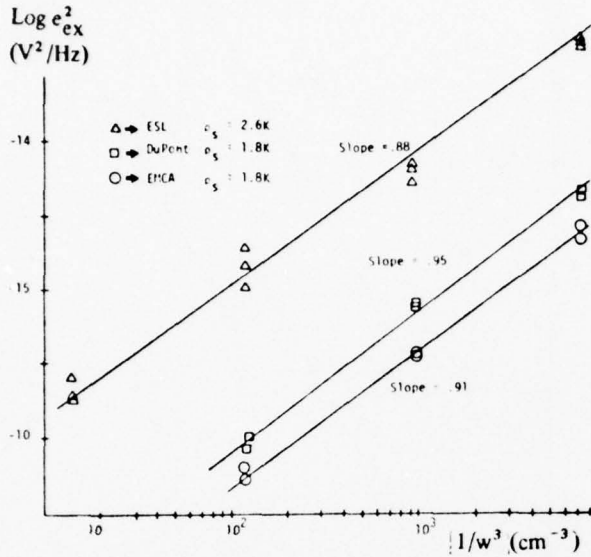


Figure 6.  $e_{ex}^2$  versus  $(1/\text{width})^3$

Sheet Resistance

Figure 7 gives some experimental plots of  $e_{ex}^2$  versus  $\rho_s$ . The slope of approximately 3 for the range of  $\rho_s$  indicated agrees with the value predicted by Equation (4). A wider range of  $\rho_s$  is not used due to limitations of the measurement

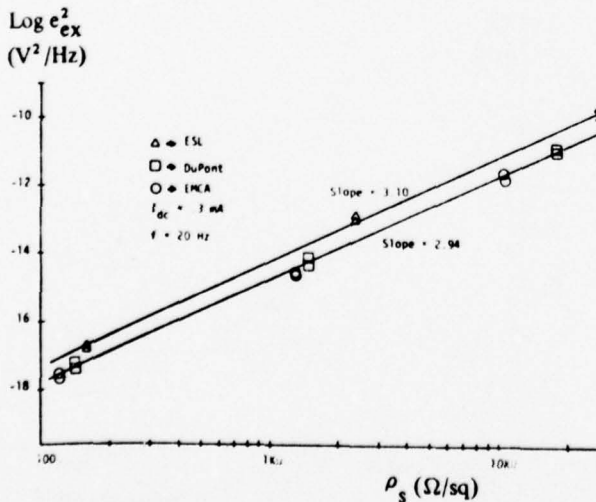


Figure 7.  $e_{ex}^2$  versus sheet resistance

dc Bias Current

An experimental plot of  $e_{ex}^2$  versus  $I_{dc}$  is given in Figure 8 for the three resistive inks with all resistor parameters (equal length, width, etc.) and frequency held constant. The slope of these curves is shown in Figure 8 and is approximately 2 as predicted by Equation (4).

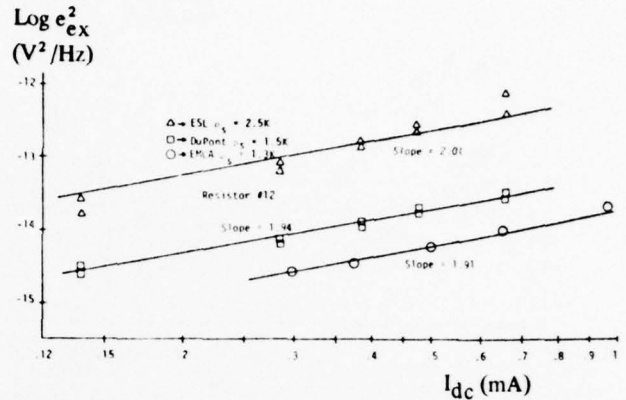


Figure 8.  $e_{ex}^2$  versus  $I_{dc}$

Spectral Plots

A family of curves of  $e_{ex}^2$  versus frequency with  $I_{dc}$  as a parameter is given in Figure 9 for an ESL sample. Similar

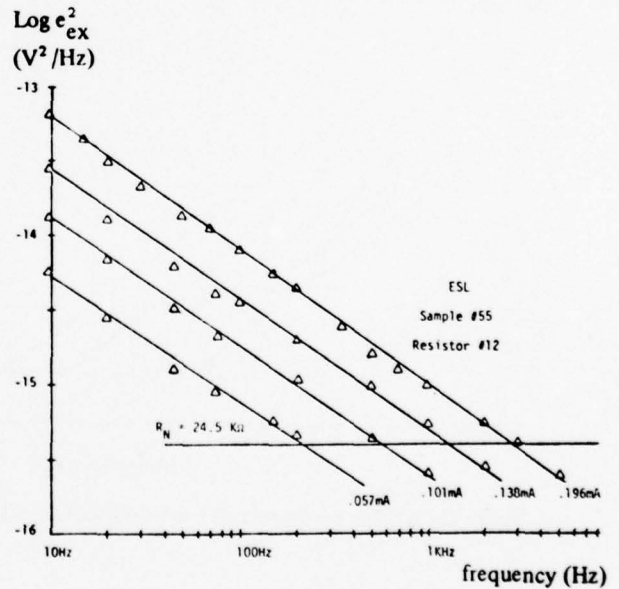


Figure 9.  $e_{ex}^2$  versus frequency for several values of  $I_{dc}$

curves are given in Figure 10 for a DuPont sample and in Figure 11 for an EMCA sample. In these Figures resistor geometry and sheet resistance were held constant. The slopes of these curves is approximately -1 which is consistent with the usual value of unity for the constant  $\alpha$  in Equation (4).

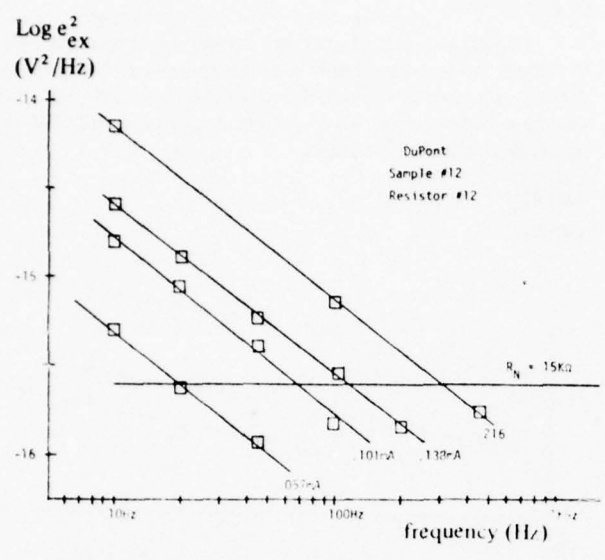


Figure 10.  $e^2_{ex}$  versus frequency for several values of  $I_{dc}$

The break frequencies,  $f_B$ , from the spectral plots of Figures 9, 10 and 11 are plotted as a function of the electric field,  $E$ , across the length of the resistor in Figure 12. Actual slopes are presented in the figure. In each case, the actual slope is close to 2 which was predicted by Equation (5).

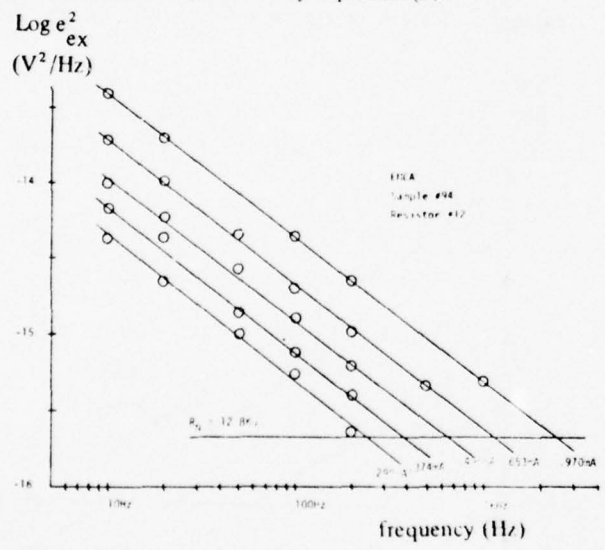


Figure 11.  $e^2_{ex}$  versus frequency for several values of  $I_{dc}$

**Temperature**

The sample was placed in an environmental chamber and data were taken at  $-35^\circ\text{C}$  and  $50^\circ\text{C}$ . The ESL (iridium based) and the EMCA (ruthenium based) resistive inks were tested in this manner. The results are shown in Figures 13 and 14. The data points for excess noise at both temperatures generally coincide on the same line, within experimental error, indicating that over this temperature range the constant  $K'$  has no apparent first order dependence on temperature. The temperature dependence of  $f_B$ , then, is due entirely to changes in the thermal noise level, as predicted by Equation (5).

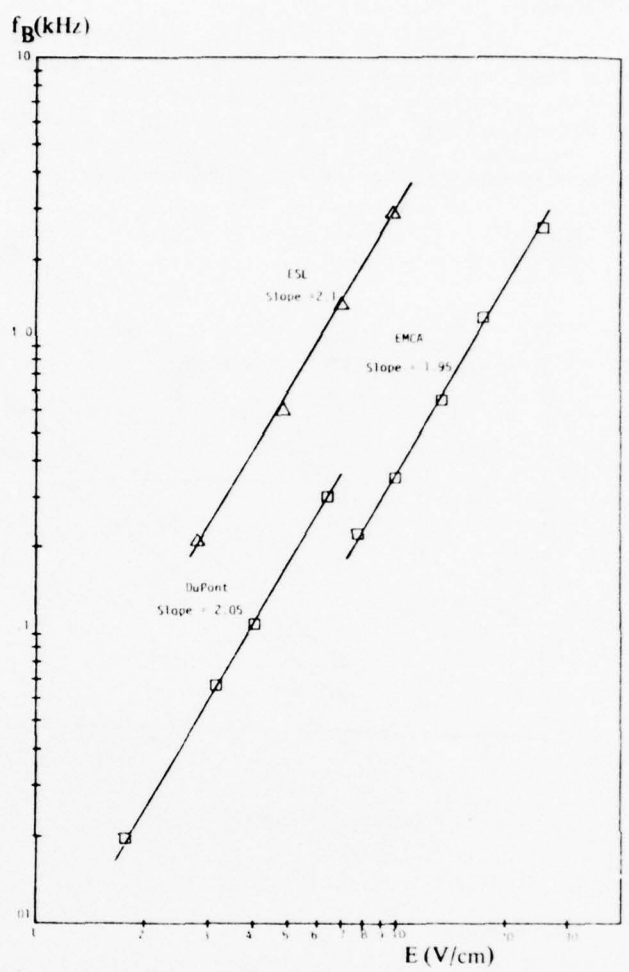


Figure 12. Break frequency versus electric field.

**Contact Effect**

Two resistors, #7 and #14, are provided to determine the effect of thick-film resistor terminations on noise performance. Resistor #14 has seven extra contacts fabricated serially

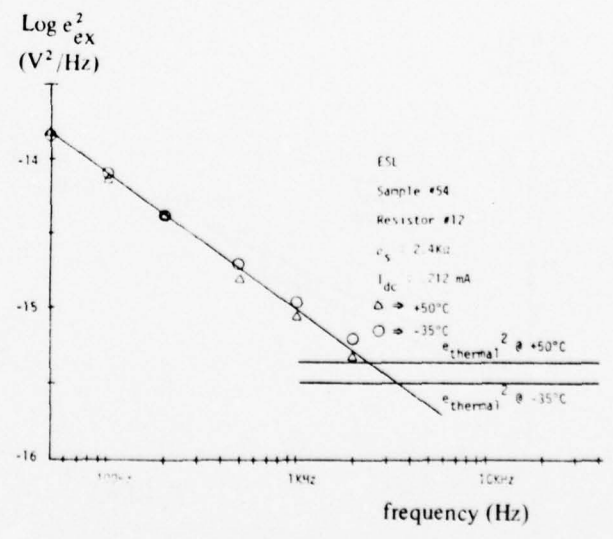


Figure 13.  $e^2_{ex}$  versus frequency for two different temperatures

in the body of the resistor, while resistor #7 is fabricated with the same number of squares of resistive material (same total aspect ratio) and same dimensions. It was found that the resistance of resistor #14 was in all cases substantially less than resistor #7, the decrease attributable to contact effects changing the resistivity of the resistor material.\* Resistor # however was found to have about (within 2 percent typically) the same resistance as #14.

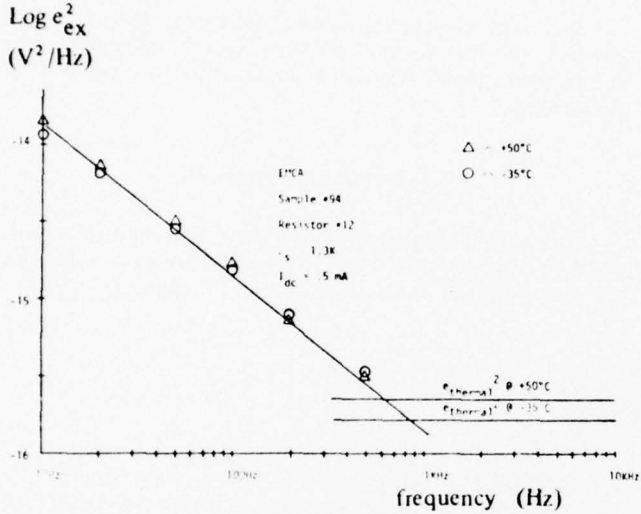


Figure 14.  $e^2_{ex}$  versus frequency for two different temperatures.

The excess noise in resistor #14 was measured and compared to resistor #12 which had the same dc resistance, but a different length. The results of this experiment for  $2.4K\Omega/\square$  ESL ink are shown in Figure 15. Within experimental error the difference in the noise in these two resistors can be attributed directly to the difference in length of the resistors. Thus, the effect of the contacts has been to the resistor and changes in the noise performance follow this sheet resistance change as predicted by Equation (4). It appears that the contacts are not adding any "new" source of excess noise to the resistor.

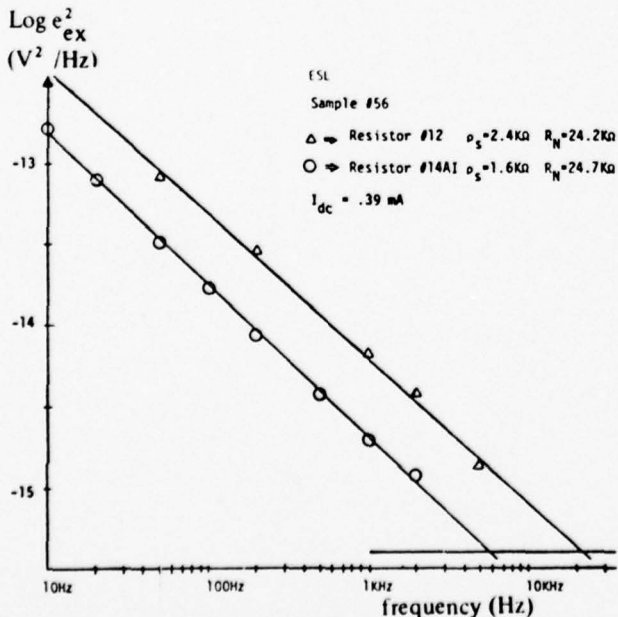


Figure 15.  $e^2_{ex}$  versus frequency for a resistor with a large number of series contacts

Excess noise has been reduced by the inclusion of extra contacts by an effective reduction in sheet resistance. At least two possible mechanisms may be responsible for this reduction. Possibly in the vicinity of a termination, contact metal is diffusing into the resistive paste during firing. This would have the effect of lowering  $\rho_s$  in this region. Since  $e^2_{ex}$  exhibits a direct dependence on  $\rho_s^3$ , any relatively small change in  $\rho_s$  results in a relatively large change in  $e^2_{ex}$ . Another possible mechanism is an increase in film thickness in the vicinity of a termination. Again, this would result in a lower average value of  $\rho_s$ . The important point is that terminations can make a large difference in the noise performance of a resistor. Experimental data taken on thick film resistors must exclude termination effects or the change in effective sheet resistance by the contacts must be incorporated if accurate comparison with models is to be made.

### CONCLUSION

A noise model Equation (4), has been verified by the experimental results of this work. The model is specifically tailored to the requirements of low-noise thick-film resistor design. It allows the computation of the entire low-frequency spectral response of a thick-film resistor.

A novel approach to noise performance optimization is suggested by Equation (5). In the past, the excess noise level of resistors in the low-frequency region of the spectrum has often been of such a magnitude that designers considered the entire noise response to be of a  $1/f$  nature. However, as can be seen in the spectral plots presented, in modern high-performance, low-frequency circuits, the thick-film resistor's noise break frequency,  $f_B$ , may fall within the low-frequency region of interest. Since the thermal noise level places a fundamental lower limit on noise level, maximum noise performance optimization is achieved when  $f_B$  is placed below the frequency band of interest.

Thick-film resistor design for low-level circuits involves meeting several design requirements. The resistance and allowable tolerance in resistance, the allowable noise level of the resistor, and the substrate area available in which to fabricate the resistor are always importance design criteria. Power dissipation, although always important, is usually negligible in the type circuit being considered. The designers task, then, is to select a specific ink, a specific geometry and sheet resistance to satisfy the design requirements.

Equation (5) gives the designer a powerful tool any parameter change which reduces the electric field in the thick-film resistor will improve the noise performance. Thus, the resistor should be as long as is possible in the space available, in order to obtain optimum noise performance.

To make a resistor of fixed resistance as long as possible require that either width or sheet resistance be varied accordingly. Long resistors require significant layout space in a circuit and the serpentine geometry is usually used. The smallest layout area will be achieved if resistor width is minimized to the minimum value possible. Finally, sheet resistance is chosen to get the desired resistance.

\*The difference in resistance was typically 66 percent (i.e. resistor #14 was 66 percent of the resistance of resistor #7) for the  $2.5 K\Omega/\square$  ESL ink. However, this number is strongly dependent on resistor geometry and ink sheet resistance.

Use of either Equation (4) or (5) requires only the determination of a single constant,  $K'$ , for a given resistive ink.  $K'$  has been shown, to a first order approximation, to be a property of the resistive material and the firing conditions and is independent of the various thick-film resistor parameters, (such as length, width, sheet resistance, etc.) over the ranges tested. From the data presented, values of  $K'$  may be computed for each of the three resistive pastes. The same values of  $K'$  are obtained whether the calculation is made using equation (4) or (5). The following values for  $K'$  were obtained:

ESL 3000:  $5 \times 10^{-19}$  mho-cm<sup>2</sup>

du Pont 1400:  $1.3 \times 10^{-19}$  mho-cm<sup>2</sup>

EMCA 5000:  $7 \times 10^{-20}$  mho-cm<sup>2</sup>

Since the constant  $K'$  serves as an index for comparison of relative noise performance, it is interesting to note that the two ruthenium based inks (DuPont and EMCA) exhibit superior noise performance over the iridium based ink (ESL).

Thick-film resistor contacts have been demonstrated to have a significant effect on noise performance for the ESL resistor/conductor ink system. Two possible mechanisms for this phenomena have been offered but not substantiated.

Since the constant  $K'$  is assumed in this study to be dependent on the firing conditions during fabrication, this dependency might also be incorporated into the model in future work.

#### ACKNOWLEDGEMENTS

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Part 4

NOISE IN OPTICAL ISOLATORS

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## Abstract

Noise measurements were performed on several commercially available optical isolators in order to examine the signal detection limits of typical devices. It was found that, in general, optical isolators are very noisy devices exhibiting all of the common types of noise usually found in bipolar junction transistors. A large number of devices exhibited burst noise which dominated their low-frequency noise performance. The noise performance of devices without burst noise was dominated by  $1/f$  noise or flicker noise at low frequencies and by shot noise at high frequencies. Experimental data indicates that in most cases the electrical noise contribution of the LED is negligible and that the dominant source of noise is the phototransistor. A model for the equivalent input noise of the optical isolator is developed and found to agree with available experimental data.

## I. Introduction

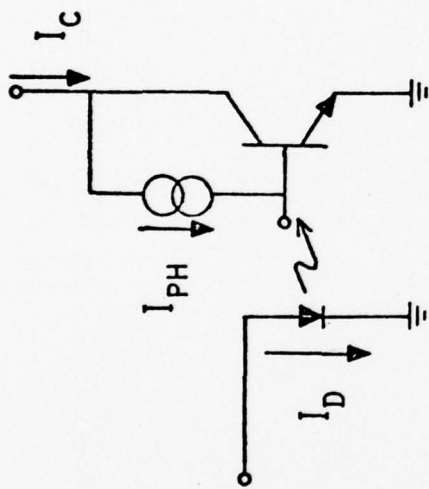
Optical isolators have found widespread use in data processing, telecommunications, process control and many other fields. They can be used as either digital devices or analog devices and are often used, for example, in the design of isolation amplifiers. [1]

An optical isolator is composed of a phototransistor or photodiode detector optically coupled to a light-emitting diode or LED as shown in Figure 1. The LED not only provides the bias current to establish the transistor Q-point but it also provides the input signal to the phototransistor.

The equations which describe the operation of the optical isolator are also shown in Figure 1. The current transfer ratios  $k'$ ,  $k$ ,  $K'$ , and  $K$  are in general dependent on LED current as shown in Figures 2a and 2b.

In low signal level applications, electrical noise is always a problem. It determines the minimum detectable signal at the input of any system. The use of optical isolators to detect small signals is limited fundamentally by the inherent noise in the optical isolator itself. The noise behavior of the optical isolator is expected to be determined by the noise inherent in both the LED and the detector. Although the noise behavior of the individual components of an optical isolator, the light-emitting diode and the photodiode or phototransistor, has been investigated previously [1,2,3,4], the noise behavior of the optical isolator has not been fully explored.

It is the purpose of this paper to examine the electrical noise inherent in several commercially available phototransistor optical



$$I_{PH} = k' I_D$$

$$I_{PH} = k(\Delta I_D)$$

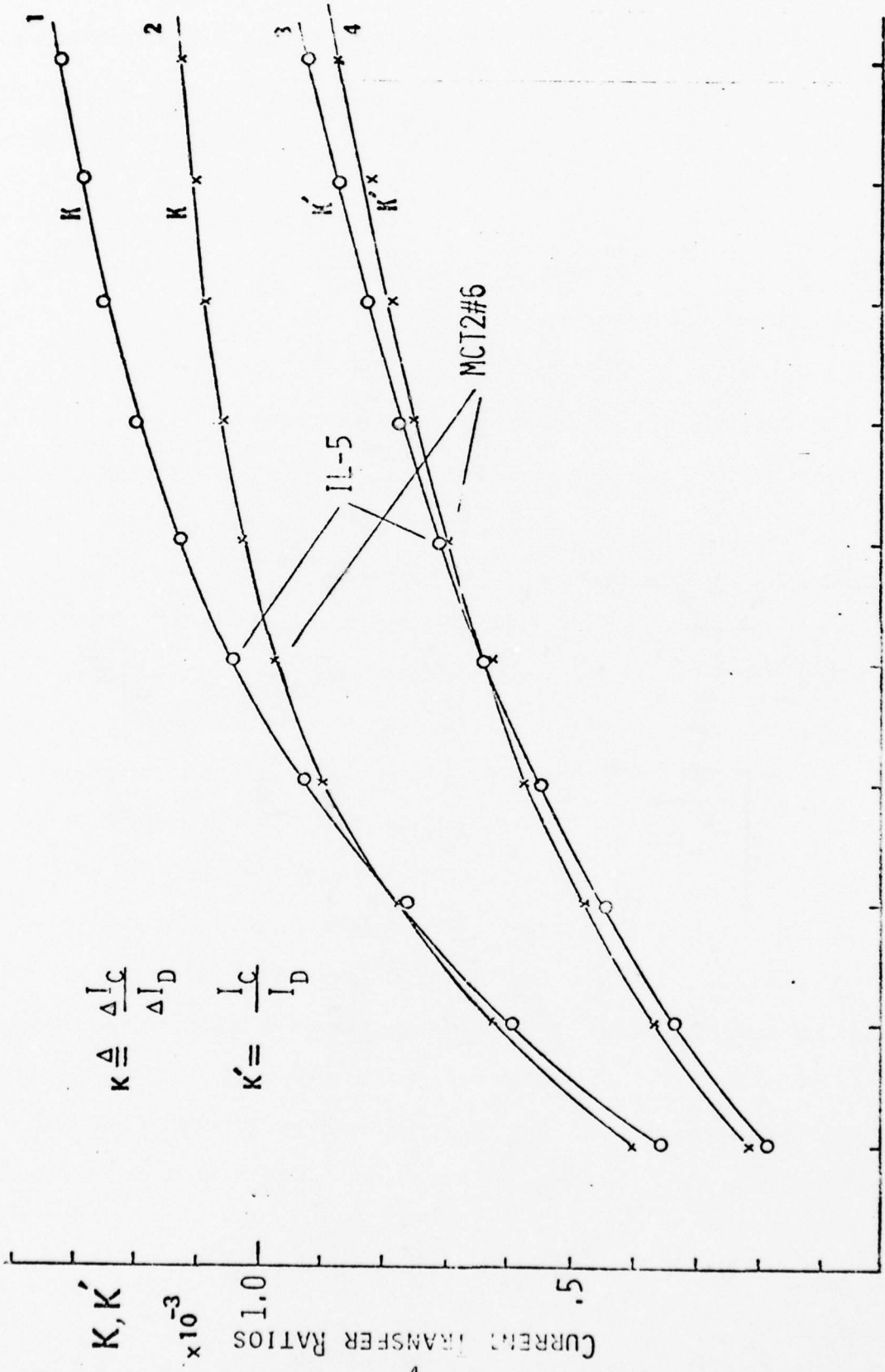
$$I_C = K' I_D$$

$$I_C = K(\Delta I_D)$$

$$I_{PH} = \left(\frac{k'}{k}\right) I_D \approx \frac{I_C}{H_{FE}}$$

$$\Delta I_{PH} = \frac{\Delta I_C}{h_{fe}}$$

Figure 1



5 10

Figure 2

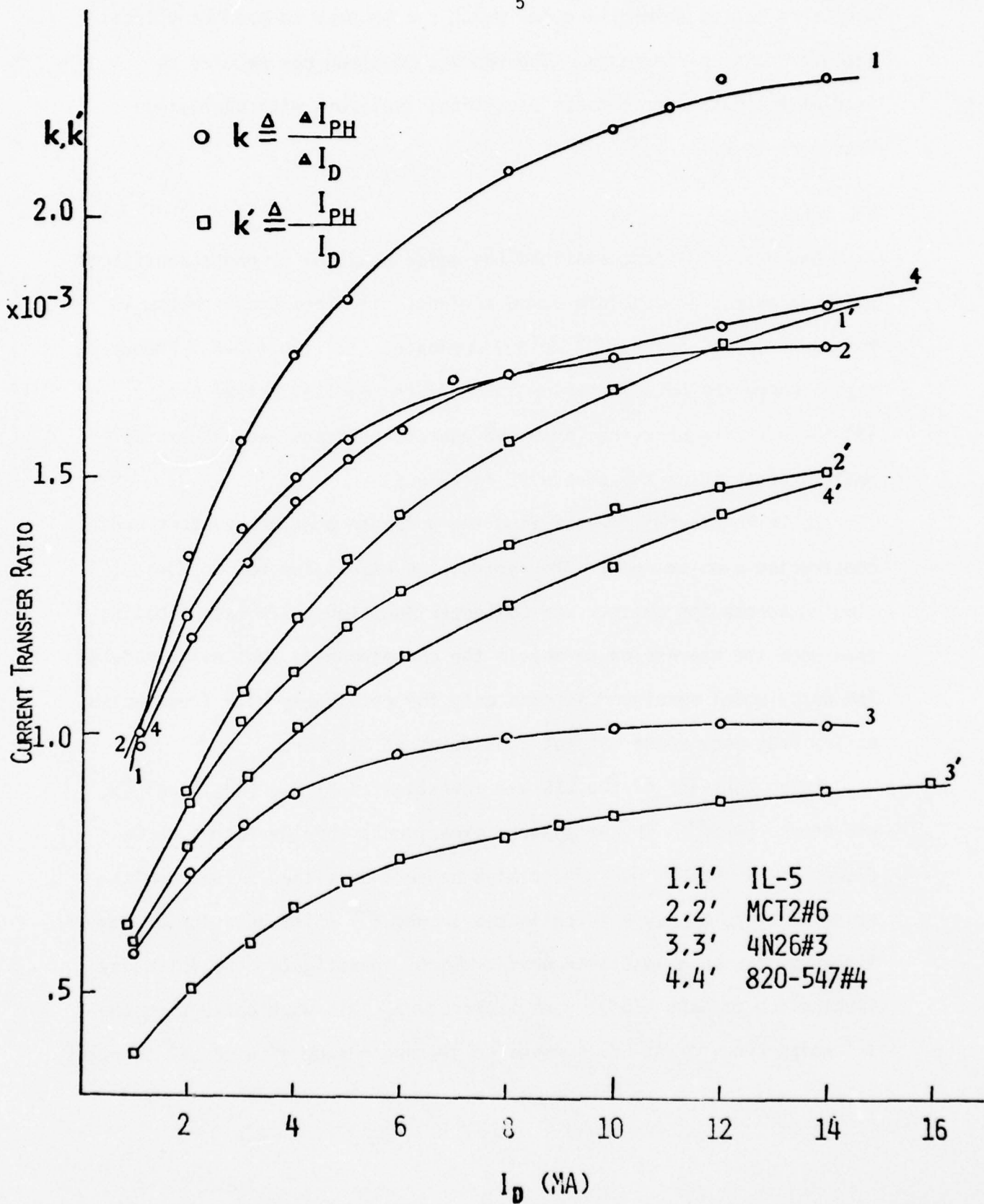


Figure 2b

isolators and to develop a model which can be used to predict optical isolator noise performance. The results obtained can be used to predict the noise performance of optical isolators with photodiode detectors as well.

## II. Background

Daughter [2] first examined the noise behavior of phototransistors which he characterized into three regions: (1) frequencies below 10 kHz where excess noise ( $f^{-\alpha}$  noise) dominates, (2) the midband frequency region where the noise behavior is dominated by shot noise, and (3) the high frequency region where phototransistors exhibit excess noise increasing as the square of frequency.

De La Moneda [3] investigated the noise in phototransistors and constructed a noise model. He derived the expression for dc current flowing across the emitter and collector junctions with base floating, then used the expression to obtain the corresponding shot noise models. The noise model developed is good only for relatively high frequencies as low frequency noise was not considered in his work.

Noise behavior of the LED was investigated by Lee [4], Conti [5] and others [6-10]. In Lee's work, experiments were performed on GaAs diodes and AL-GaAs diodes under high current densities. The results revealed that the LED's investigated showed  $f^{-\alpha}$  noise behavior at low frequencies with  $\alpha$  less than unity. Conti investigated the intensity fluctuation of GaAs LED at room temperature. His work concerning the  $f^{-\alpha}$  noise behavior of LED's revealed the dependence of  $\alpha$  on LED currents.

### III. Experimental Results

#### A. Discussion

Optical isolators were purchased from five major vendors as listed in Table I. The Monsanto MCT 2 was chosen as the "standard" device for purposes of comparison and selection from other manufacturers. Thus, all of the other devices were selected because they were quoted as being that manufacturer's replacement or equivalent part to the Monsanto MCT 2. All of these parts utilize an LED optically coupled to a phototransistor with base lead available. The devices used were selected randomly and no preference was given to optical isolators with more noise or less noise. A total of 24 devices were examined experimentally.

#### B. Burst Noise

The two most significant sources of noise at low frequencies were burst noise [11] and  $1/f$  noise [12]. A very large percentage of the optical isolators investigated exhibited significant amounts of burst noise as shown in Table II. Figure 3 shows a typical example of the burst noise signals found. This figure shows the noise in the collector current output of a Motorola optical isolator as observed on a storage oscilloscope.

In all of the optical isolators investigated, the burst noise was observed to be the same independent of bias arrangement (ie. whether the LED was used to bias the phototransistor or a conventional resistor base bias network). Thus, the burst noise originated in the phototransistor and not the LED.

TABLE 1  
OPTICAL ISOLATORS INVESTIGATED

<u>MEG.</u>	<u>TYPE</u>	<u>QUANTITY</u>
FAIRCHILD	820-547	5
MOTOROLA	4N26	5
MONSANTO	MCT-2	7
G.E.	GEH-11	5
LITRONIX	IL-5	2

Table I

TABLE 2  
OPTICAL ISOLATORS WITH SIGNIFICANT BURST NOISE

MFG.	TYPE	QUANTITY (TOTAL)	No. WITH
FAIRCHILD	820-547	5	4 (80%)
MOTOROLA	4N26	5	4 (80%)
MONSANTO	MCT-2	7	2 (29%)
G.E.	GEH-11	5	3 (60%)
LITRONIX	IL-5	2	1 (50%)

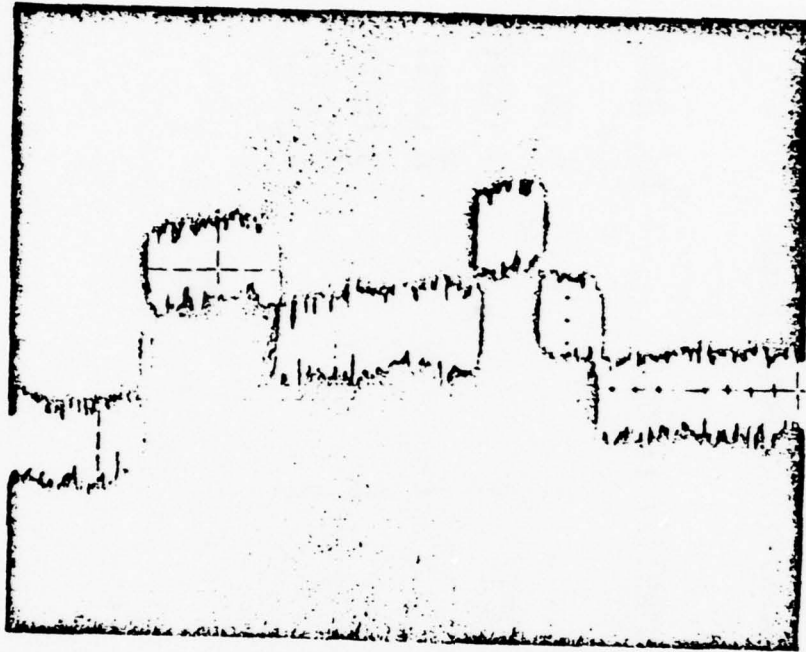


Figure 3

Accepted burst noise models predict that burst noise can be represented by an equivalent input noise current generator in parallel with the phototransistor base-emitter junction as shown in Figure 4 [12,13]. The mean-square value of the burst-noise generator is approximately [11e,11f,12,13]

$$\overline{i_{BB}^2} = AI_B \cdot \frac{df}{1 + (f/f_B)^2} \quad (1)$$

where  $I_B$  is the d.c. base current,  $f_B$  is a constant related to the burst noise frequency spectrum and  $A$  is a proportionality constant [11e,11f]. From equation (1) we see that the magnitude of the square of the burst noise current is proportional to base current,  $I_B$ . The equivalent input burst noise of the optical isolator can be derived using the equivalent circuit of Figure 5. It is:

$$\overline{i_d^2} = \frac{\overline{i_{BB}^2}}{k^2} \quad (2)$$

Thus, the equivalent input burst noise of the optical isolator is also proportional to the phototransistor base current. In an optical isolator, the phototransistor base current is set by photogeneration in the transistor c-b junction due to LED illumination. The photogenerated base current is defined to be  $I_{PH}$  as indicated in Figure 1.

From equation (2), the magnitude of the equivalent input burst noise current pulses referred to the optical isolator input is

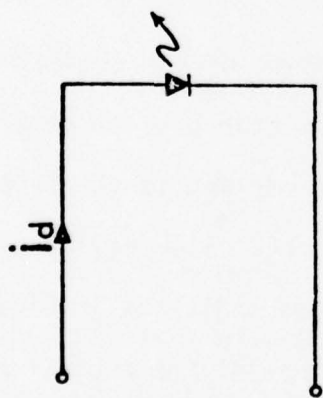
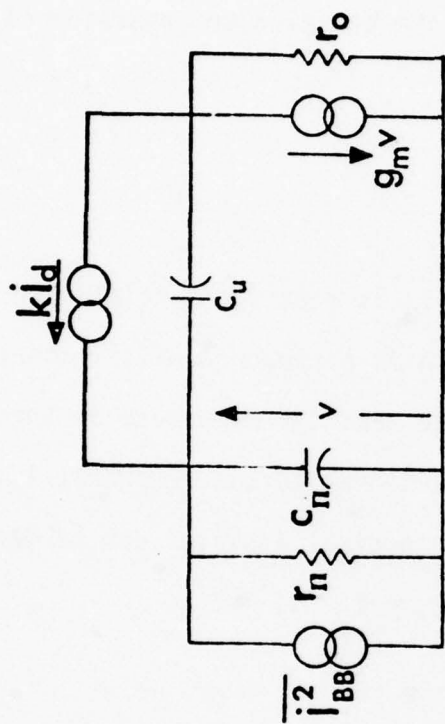
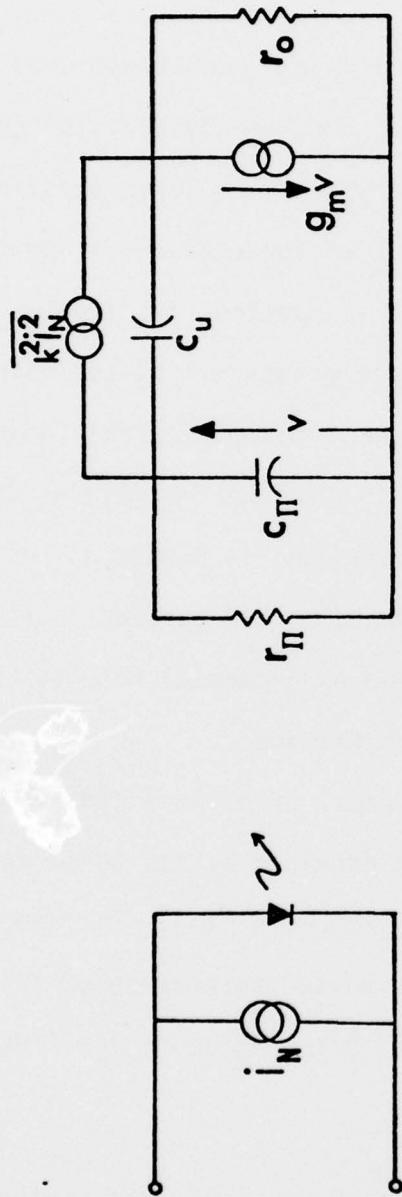


Figure 4



$\overline{i_N^2} \triangleq$  EQUIVALENT INPUT NOISE OF THE OPTICAL ISOLATOR

Figure 5

$$I_{BN}^2 = \frac{A'I_B}{k^2} \triangleq \frac{A'I_{pH}}{k^2} = \frac{A'k'I_D}{k^2} \quad (3)$$

where  $A'$  is a constant.

To check equation (3), the circuit shown in Figure 6 was used to measure the equivalent input burst noise  $I_{BN}$  to the optical isolator [14]. An example of typical results for devices with large burst noise is shown in Figure 7 in which the magnitude of the equivalent input burst noise pulses for a Fairchild 820-547 is plotted as a function of d.c. LED current,  $I_D$ . Both theoretical data points calculated using equation (3) and experimental data are shown. Calculated data points use the experimentally determined values of  $k$  and  $k'$  from Figure 2b to obtain the factor  $k'/k^2$  which has been plotted in Figure 8. As can be seen, this ratio shows a slight dependence on LED current, particularly at low LED currents. The agreement between experimental results and equation (3) was excellent for all devices examined.

Another device, Motorola 4N26 #4, typical of devices containing both large burst noise and  $1/f$  noise, was examined by its noise spectrum. The noise measurement circuit is shown in Figure 9 [14]. The experimental result is shown in Figure 10. The noise performance of this device, like many others, was dominated by burst noise at low frequencies.

### C. The Complete Noise Spectrums

For devices without conspicuous burst noise, the noise performance was characterized by flicker noise at low frequencies and shot noise at higher frequencies. Measurements of the equivalent input noise

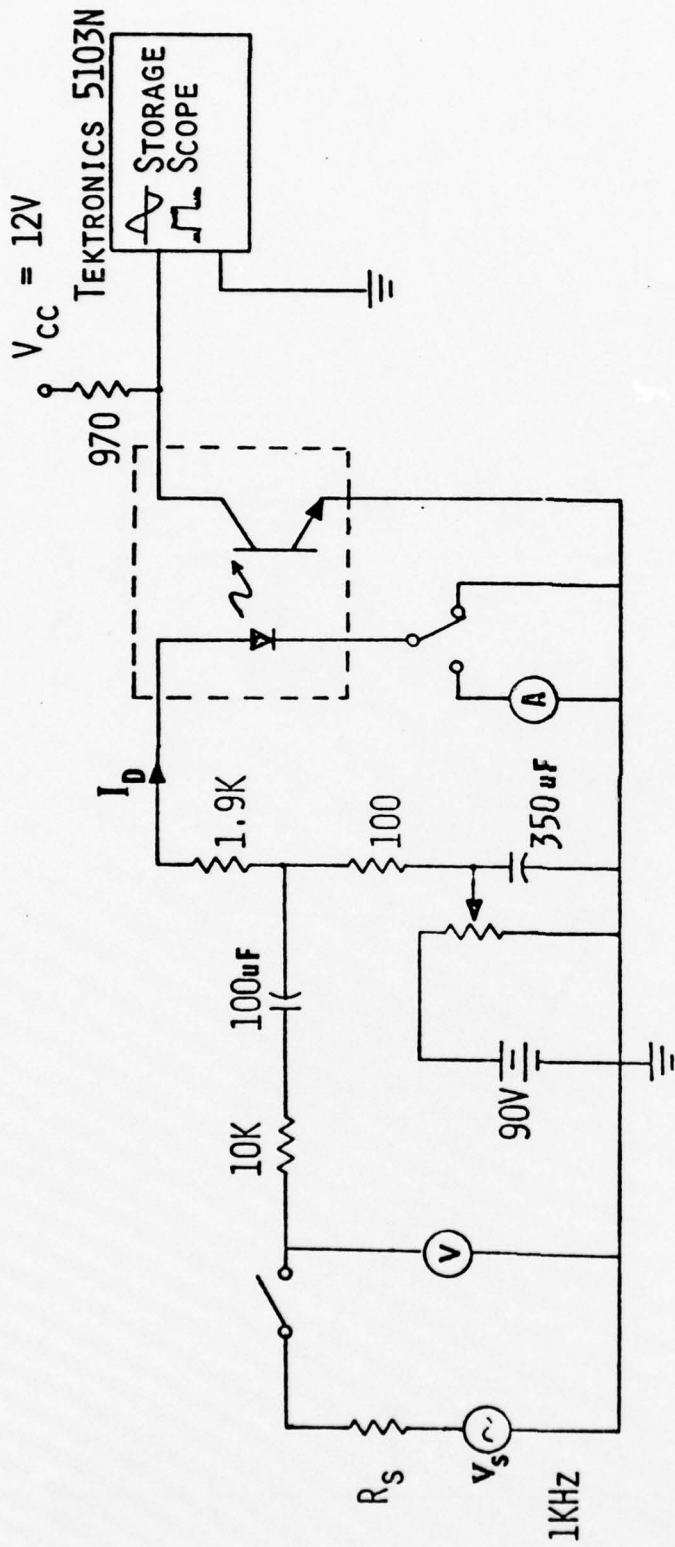
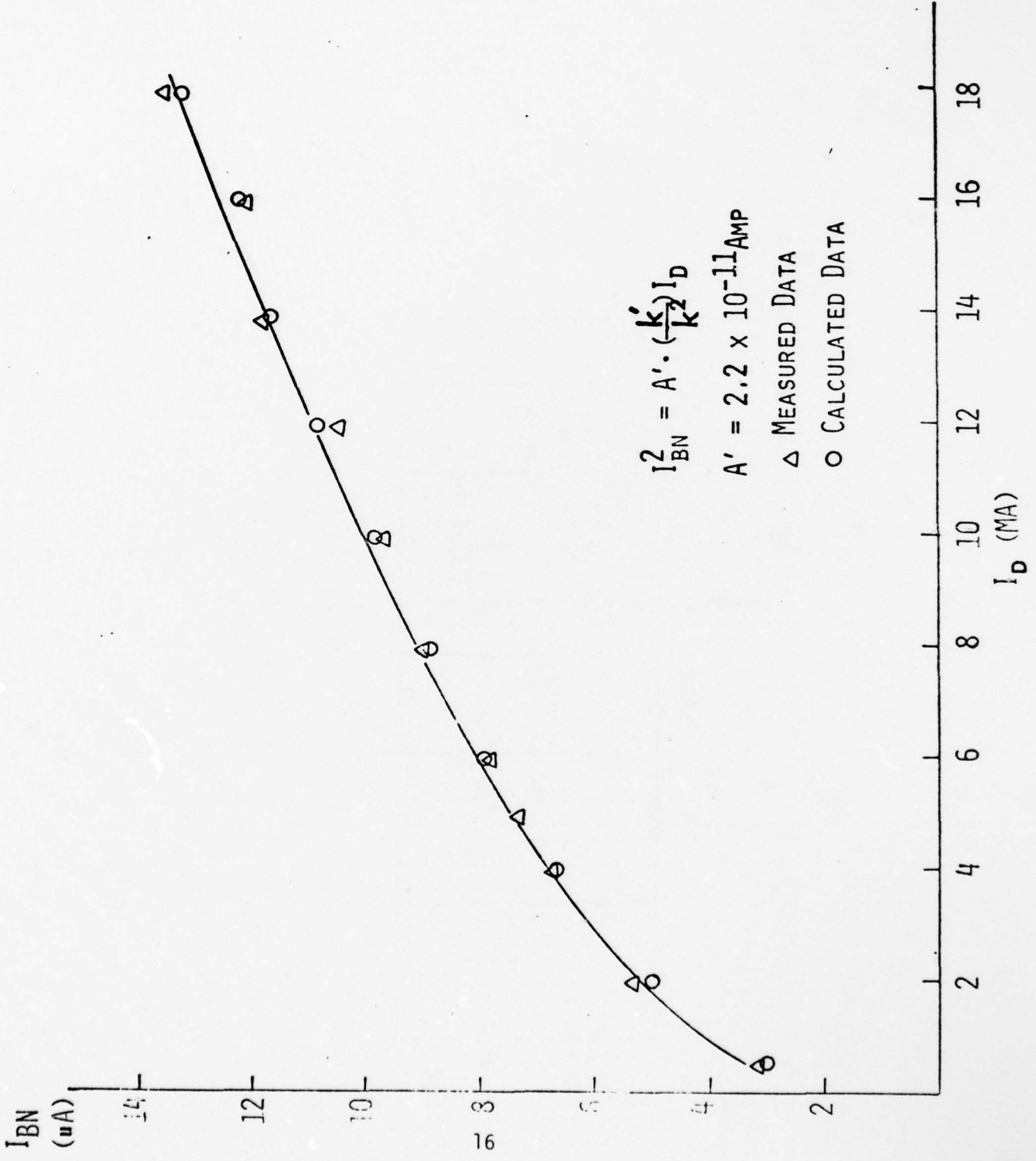


Figure 6



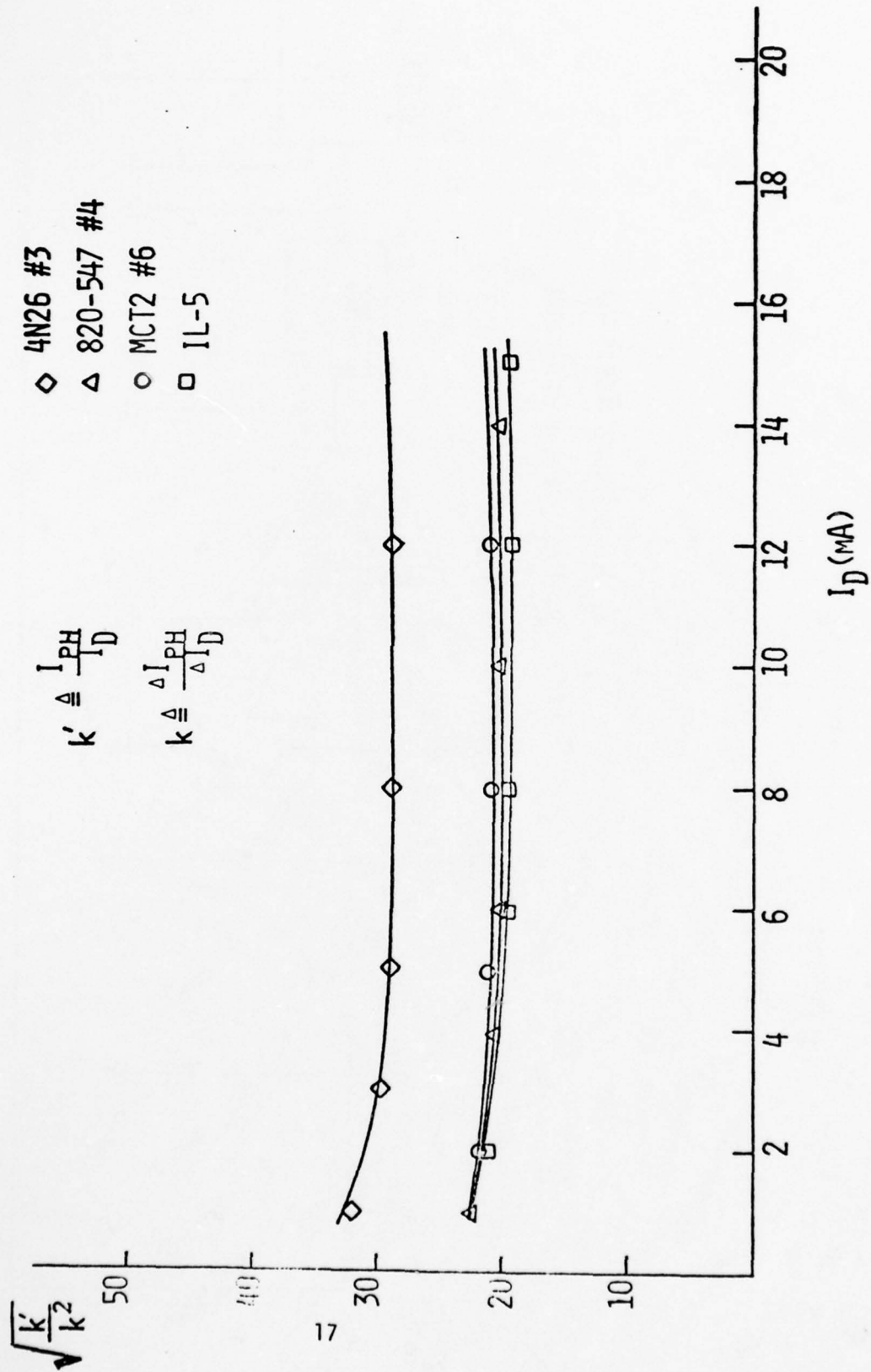


Figure 8

$R_D$  WIRE WOUND RESISTOR  
 $R_C$  METAL FILM RESISTOR

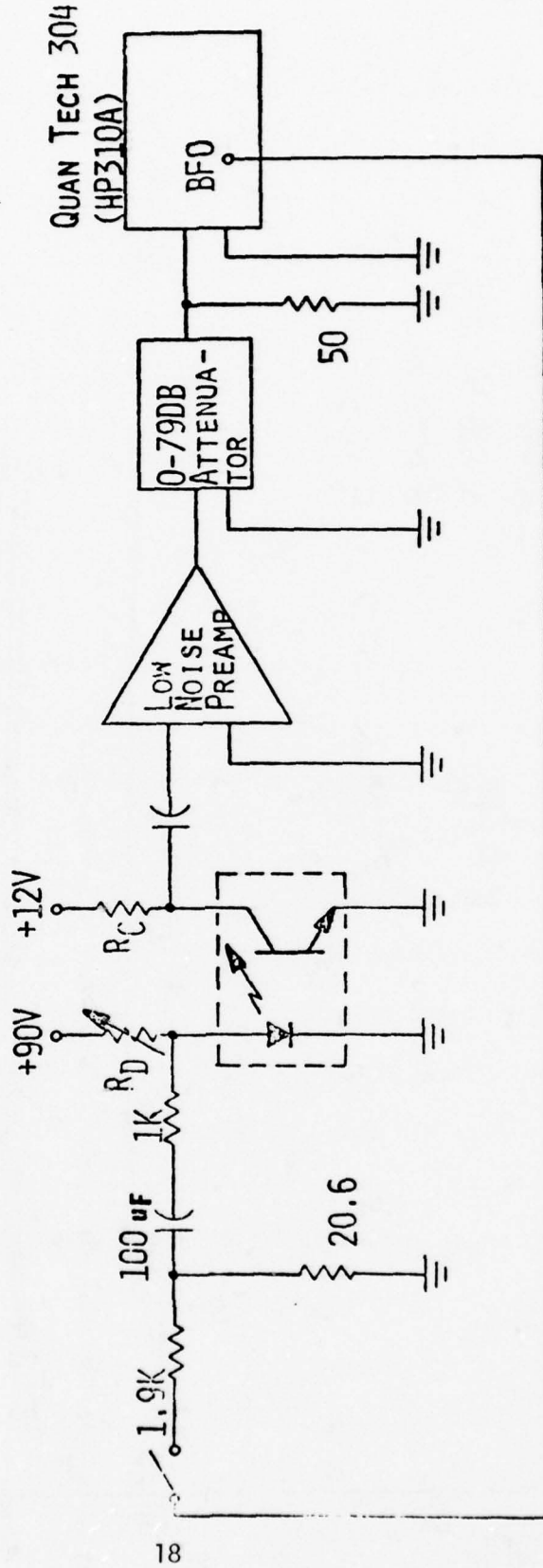


Figure 9

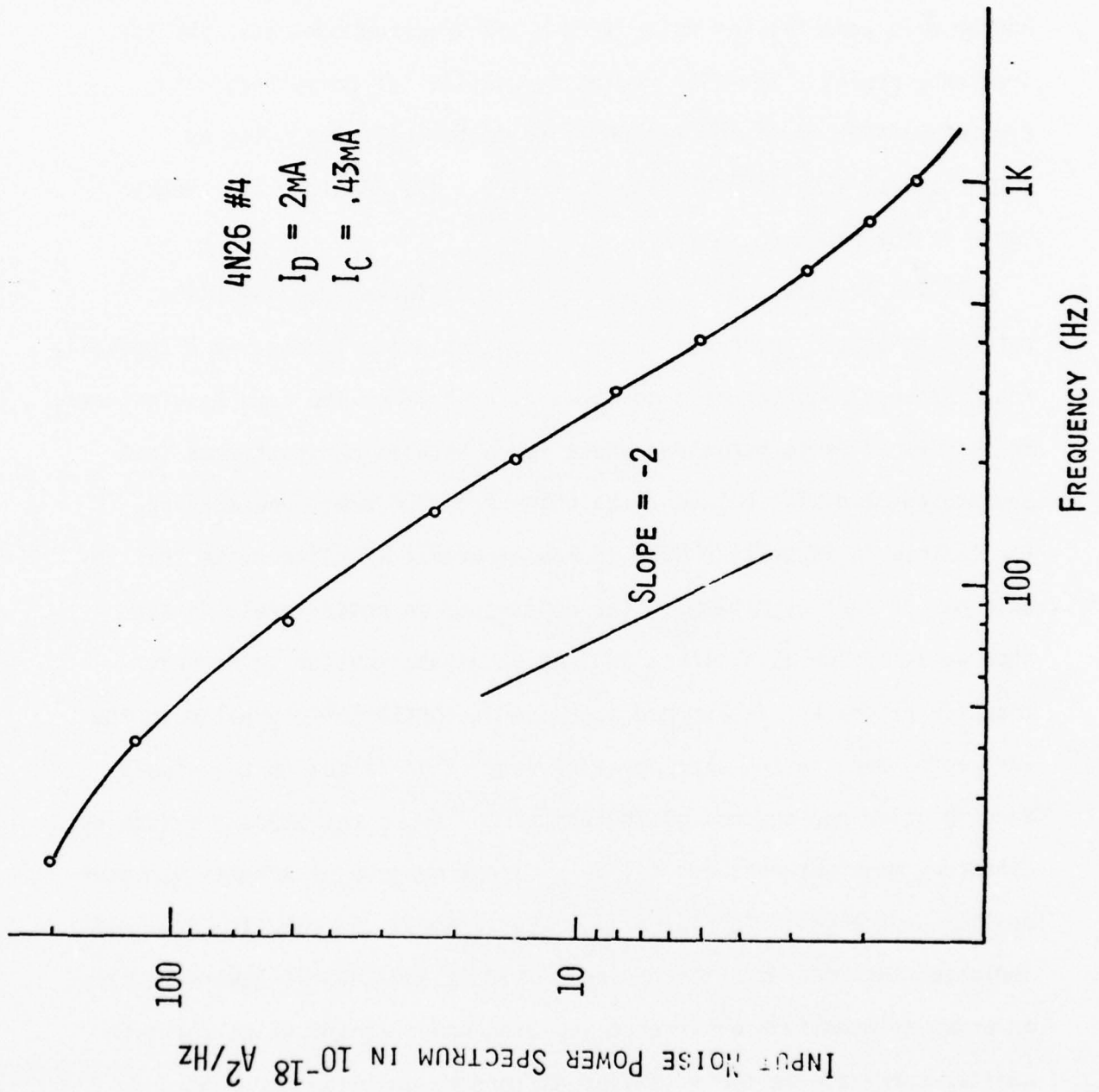


Figure 10

spectrum of several phototransistor optical isolators without large burst noise were performed using the circuit shown in Figure 9. Typical equivalent input noise spectrums are shown in Figure 11. It can be seen that flicker noise with a  $1/f$  spectrum dominates the low frequency region. The flat region beyond the  $1/f$  noise region is frequency independent and was verified to be full shot noise by comparison of experimental data to theory. (We develop this theory later in the paper.)

Figure 12 shows noise spectrums from different devices. The results presented indicate the variations in noise levels and  $k$  typically found between manufacturers and between units from the same manufacturer. In this work, large variations were found between manufacturers (not unexpected) and also between like units from the same manufacturer. For example in Figure 12, MCT2 #6 has a current transfer ratio that is only 64% of that of MCT2 #7. The difference in noise levels in the shot noise region is a direct indication of the scatter in current transfer ratio,  $k$ . The spread in noise is considerably greater in the  $1/f$  region than in the shot-noise region. This is due to the widely varying noise performance of the phototransistors and LED's provided by different manufacturers and may be a direct measure of optical isolator quality and reliability [15,16,17]. For example the data in Figure 12 indicates that two Monsanto devices, MCT2 #7 and MCT2 #6 have more than an order of magnitude difference in noise power at 100 Hz at the same emitter current. We see a similar difference in noise power between MCT2 #6 and MCT2 #7 biased at the same LED current. It is important

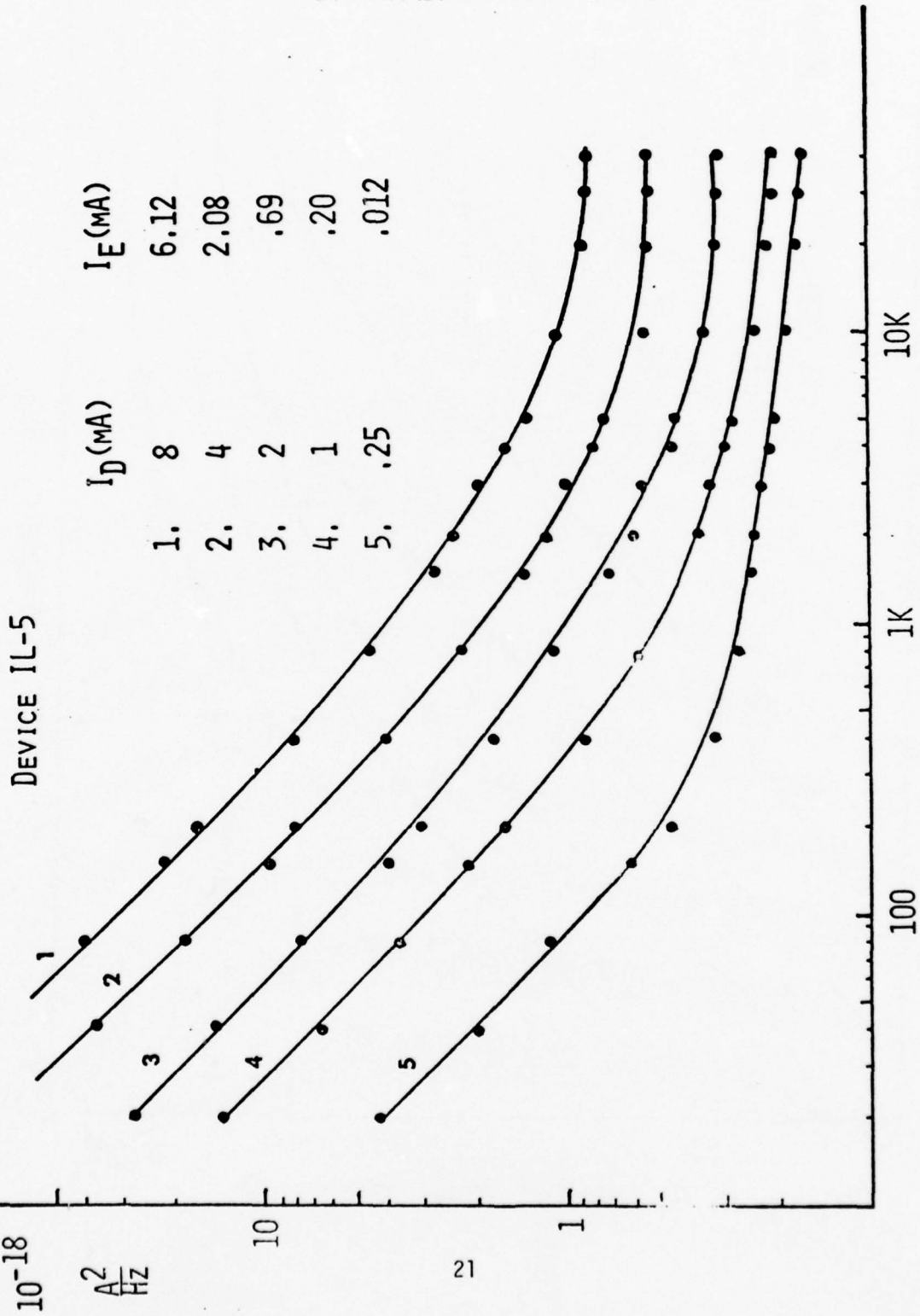


Figure 11

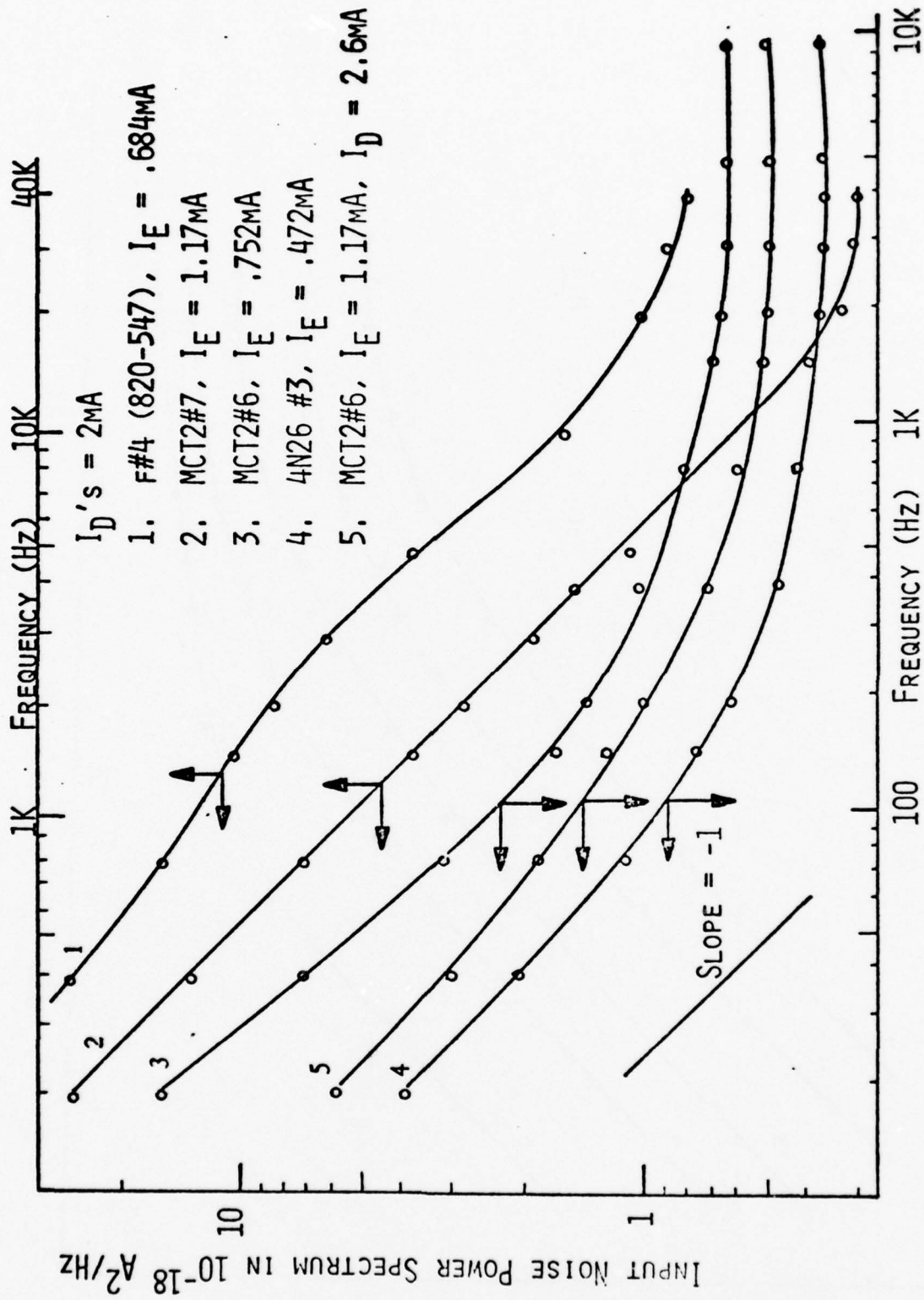


Figure 12

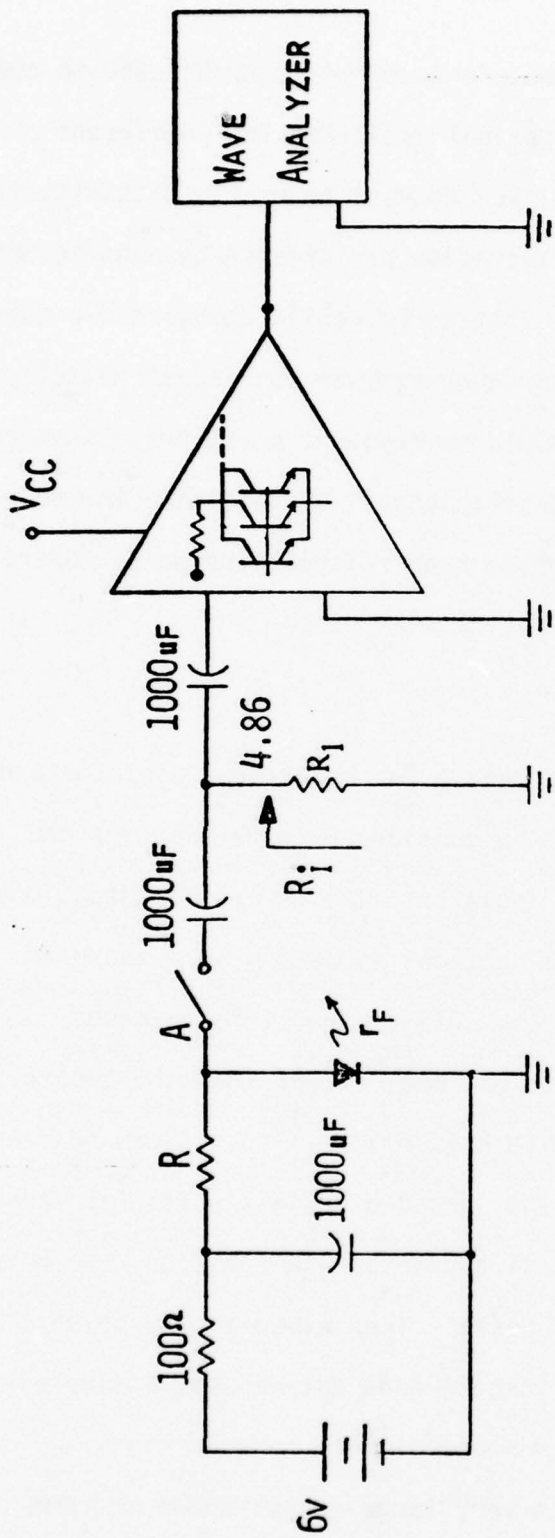
to note that Figure 12 does not contain enough data to be used to compare the average noise performance of optical isolators from different manufacturers. We do not have sufficient data to make a statistically meaningful comparison of the average noise performance by manufacturer.

Finally, Figure 12 indicates that in Fairchild device #4, a noise spectrum is obtained which has structure similar to a burst noise spectrum. However, the device showed no apparent burst noise when its noise spectrum was viewed on an oscilloscope. To determine the origin of the unusual structure in the noise spectral plot the noise contribution of the LED was examined.

#### D. Current Fluctuations of LED's

The LED is used as the input device to the optical isolator and therefore its noise behavior must be considered in determining the noise performance of the optical isolator. The current fluctuations of forward biased LED's in several optical isolators were measured with the circuit shown in Figure 13. All of the LED's examined exhibited large excess noise which was much larger than the theoretical shot noise limit ( $2qI_D$ ) as shown in Figure 14. Also, it can be seen from Figure 14 that there is a wide spread of excess noise (as large as 1:1000) for LED's with identical currents. In addition, the noise spectrum is often not simple  $1/f$  noise. (For example, the noise from the LED in unit 820-547 #4 in Figure 14 does not exhibit a simple  $1/f$  spectrum.)

Although the LED can exhibit very large excess noise in some cases, its affect on the noise performance of the optical isolator is



$$R \gg r_F \gg R_1 \approx R_i$$

Figure 13

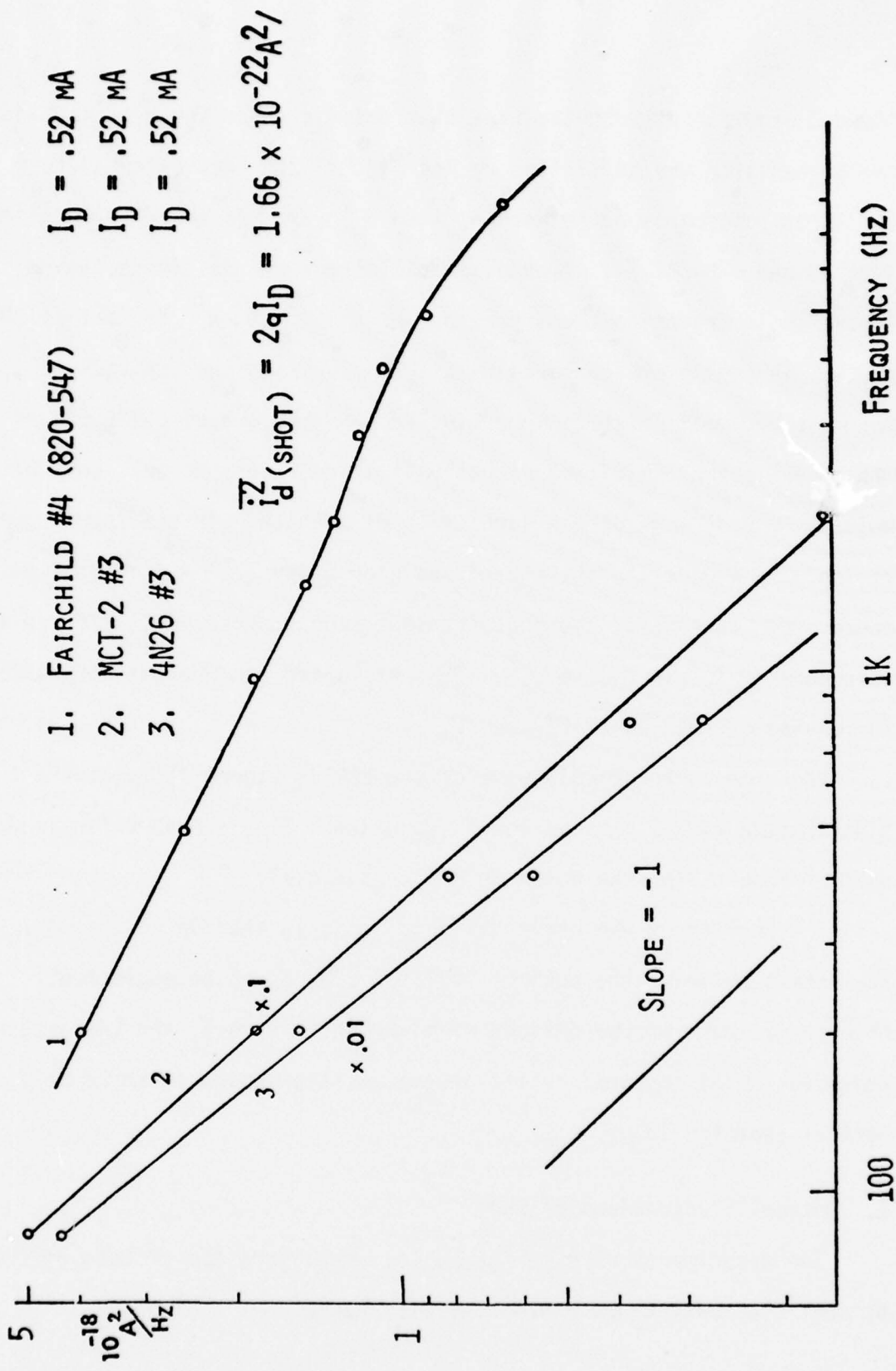


Figure 14

reduced significantly by the fact that noise sources inherent in the phototransistor are multiplied by the factor  $1/k^2$  when referred to the LED input. Comparisons between  $\overline{i_n^2}$  and  $\overline{i_d^2}$  were performed for devices 4N26 #3 and 820-547 #4. Typical results are shown in Figure 15 and Figure 16 to determine the importance of the  $\overline{i_d^2}$  term. For device 4N26 #3,  $\overline{i_d^2}$  is negligible compared with  $\overline{i_n^2}$ . This was the typical result for most optical isolators investigated. However, device 820-547 #4 was an exception exhibiting excessively large excess noise. For this unit  $\overline{i_d^2}$  and  $\overline{i_n^2}$  are of the same order of magnitude in the low frequency region. In Figure 16, the phototransistor noise ( $\overline{i_n^2} - \overline{i_d^2}$ ) is indicated. For this unit, the phototransistor noise was simple  $1/f$  and the structure in  $\overline{i_n^2}$  is due to  $\overline{i_d^2}$ . This explained the unusual structure for device 820-547 #4 in Figure 12.

The excess electrical noise of the LED in Figure 16 follows a  $f^{-\alpha}$  distribution with  $\alpha = .5$  at low frequencies. Others have determined similar results for the noise in LED's [4,5,6,7].

The results of the above analysis indicate that in some cases, the excess noise of the optical isolator LED cannot be neglected. However for most of the devices examined in this work, the LED excess noise was small compared to the phototransistor noise referred to the optical isolator input.

#### E. Optical Fluctuations of LEDs

Two experiments were performed to investigate the effects of LED optical fluctuations on phototransistor noise.

DEVICE 820-547 #4

$I_D = .52\text{mA}$

$I_C = 62\mu\text{A}$

1. INPUT NOISE SPECTRUM OF OPTICAL-ISOLATOR ( $\bar{i}$ )
2. ELECTRICAL NOISE OF LED ( $\bar{i}_D^2$ )
3.  $\bar{i}_N^2 - \bar{i}_D^2$

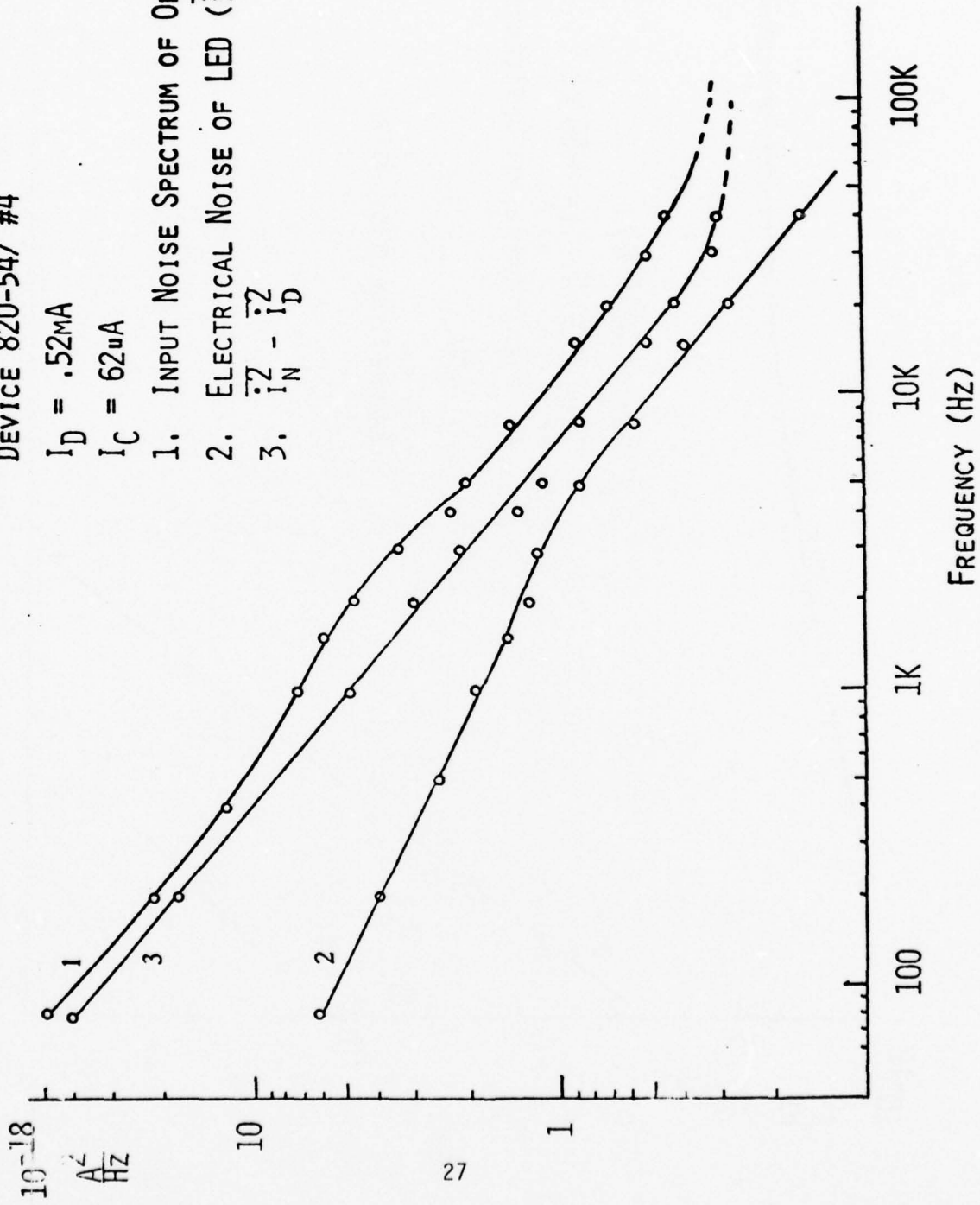
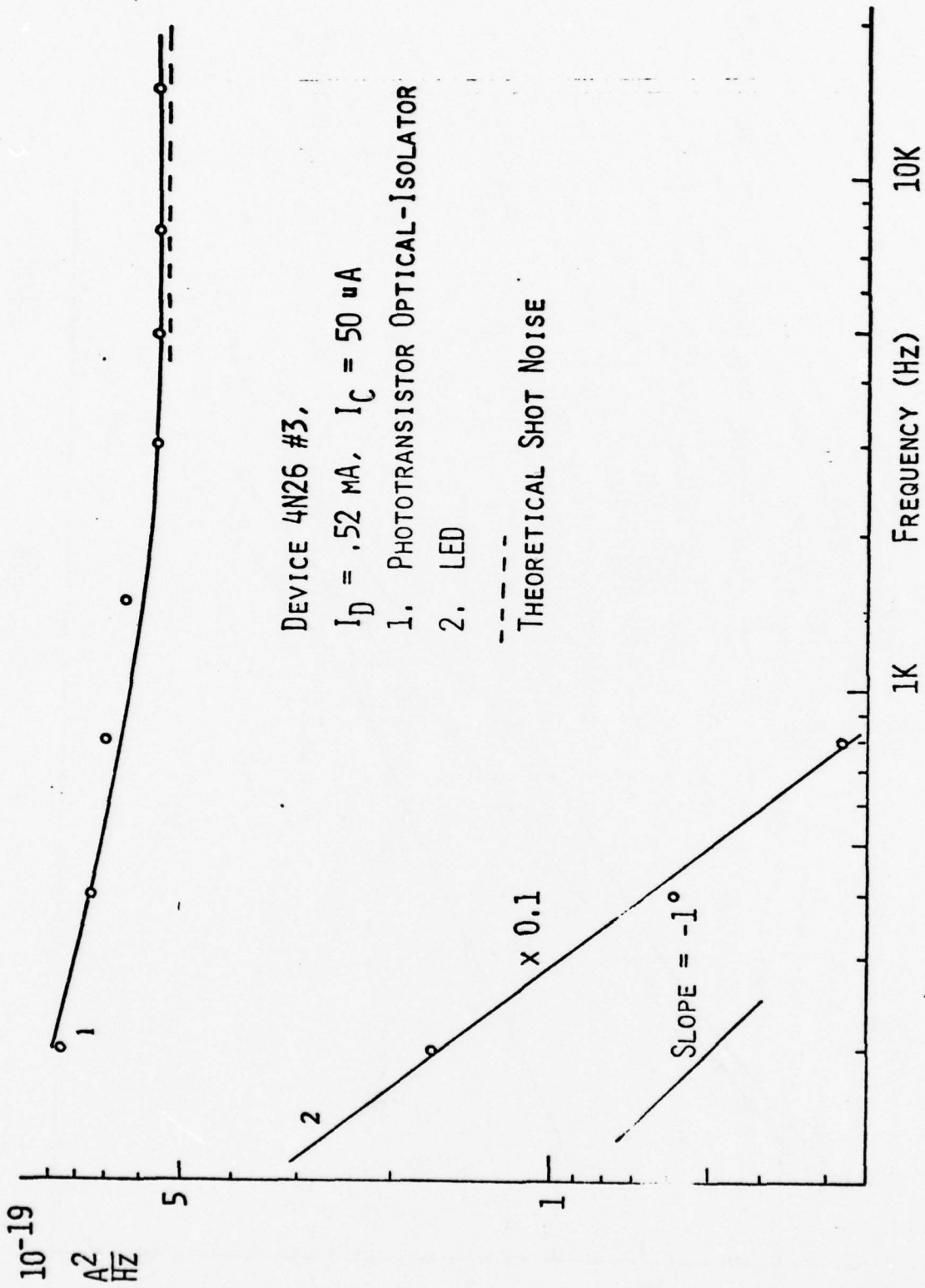


Figure 15



DEVICE 4N26 #3,

$I_D = .52 \text{ mA}$ ,  $I_C = 50 \mu\text{A}$

1. PHOTOTRANSISTOR OPTICAL-ISOLATOR
2. LED

Figure 16

In the first, the measurement system in Figure 17 was used to examine the detected noise. The measured results for devices 820-547 #4 and 4N26 #3 are shown in Figure 18. For 820-547 #4, the structure in the noise spectrum of optical fluctuation of the LED follows that of its electrical fluctuation in the low frequency region as shown in Figure 16. In both cases, the detected excess noise is significant and will contribute significantly to the phototransistor noise. The detected optical fluctuations approach the theoretical shot noise limit at higher frequencies.

In another experiment, the equivalent input noise, referred to the base, of an LED-biased phototransistor and to the base of the same transistor with resistor base bias was measured and compared. Figure 19 shows the results of two devices IL-5 and MCT2 #6. In the shot noise region, the mean square noise current of the LED biased phototransistor is twice as large as that of the resistor biased transistor as expected [3]. In the low frequency region, it is apparent that optical fluctuations of the MCT2 #6 LED are adding a significant amount of excess noise (in this case because the noise of the phototransistor is so small). However, in device IL-5 the excess noise of the LED is negligible as was the case in most of the devices examined.

#### F. Noise Performance Comparison Between the Optical Isolator and the Phototransistor

The equivalent input noise spectrums of several optical isolators and the equivalent input noise to the base of the optical isolator's phototransistors were measured and compared. In the later case, the calibrating signal was ac coupled to the base of phototransistor

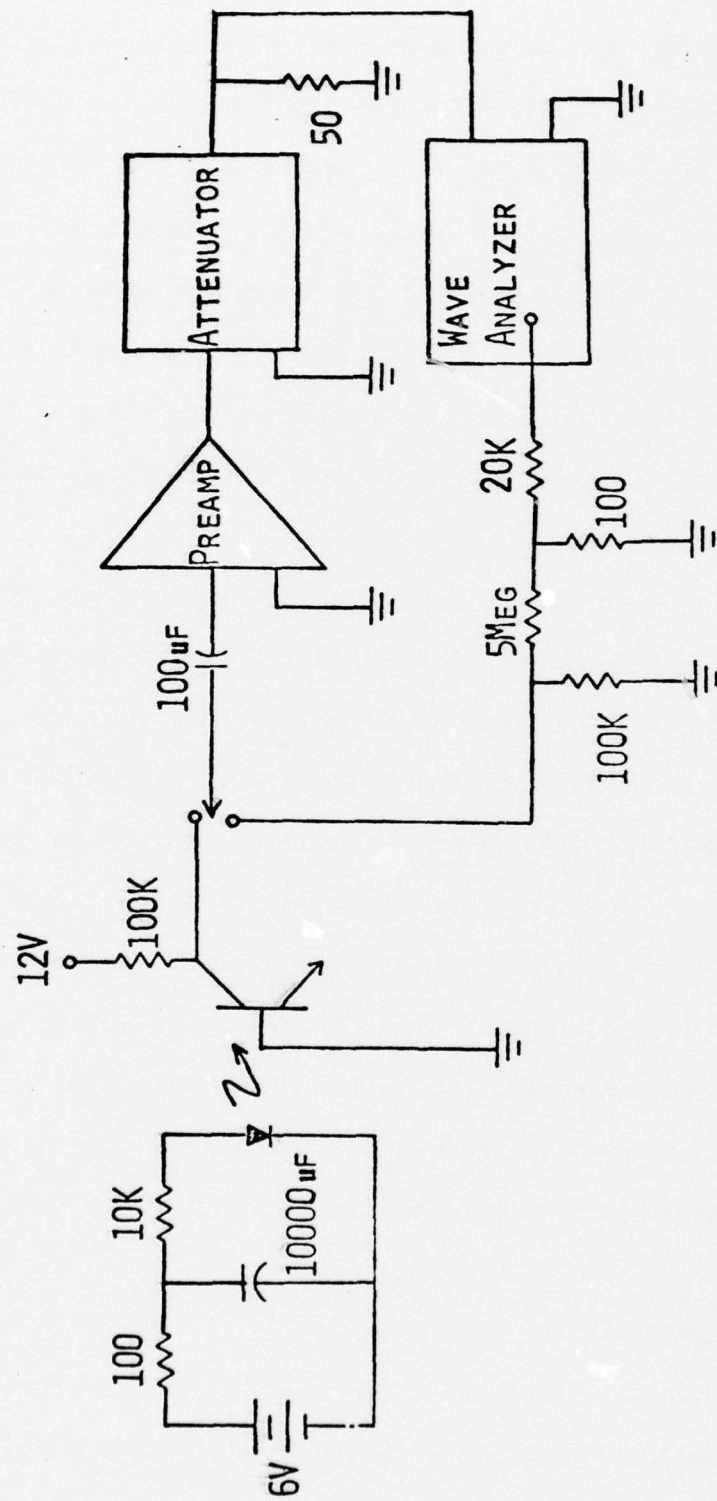


Figure 17

1. 820-547 #4      $I_D = 2.9 \text{ MA}$ ,      $I_{PH} = 2.88 \text{ uA}$   
 2. 4N26 #3      $I_D = 2.8 \text{ MA}$ ,      $I_{PH} = 1.75 \text{ uA}$

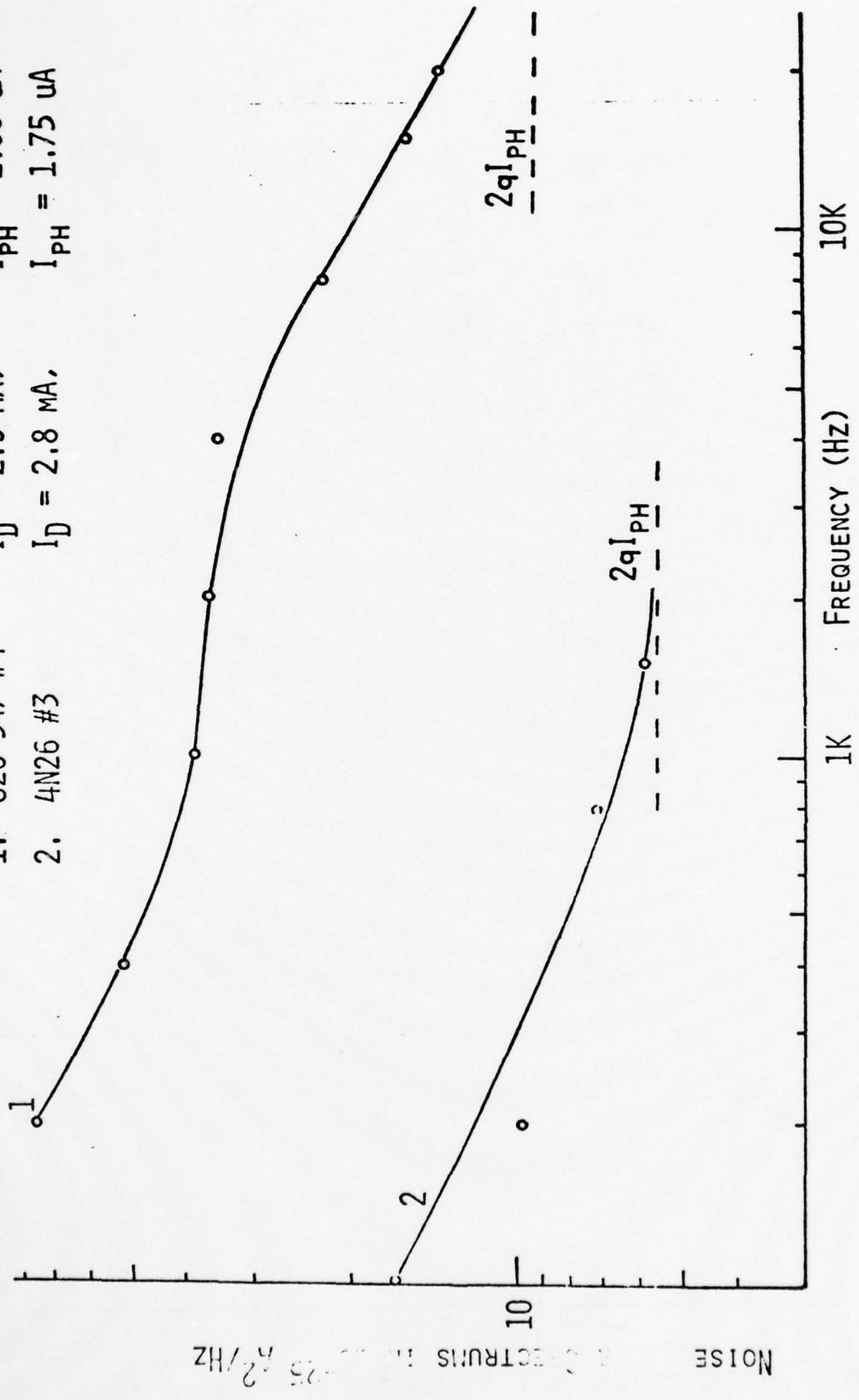


Figure 18

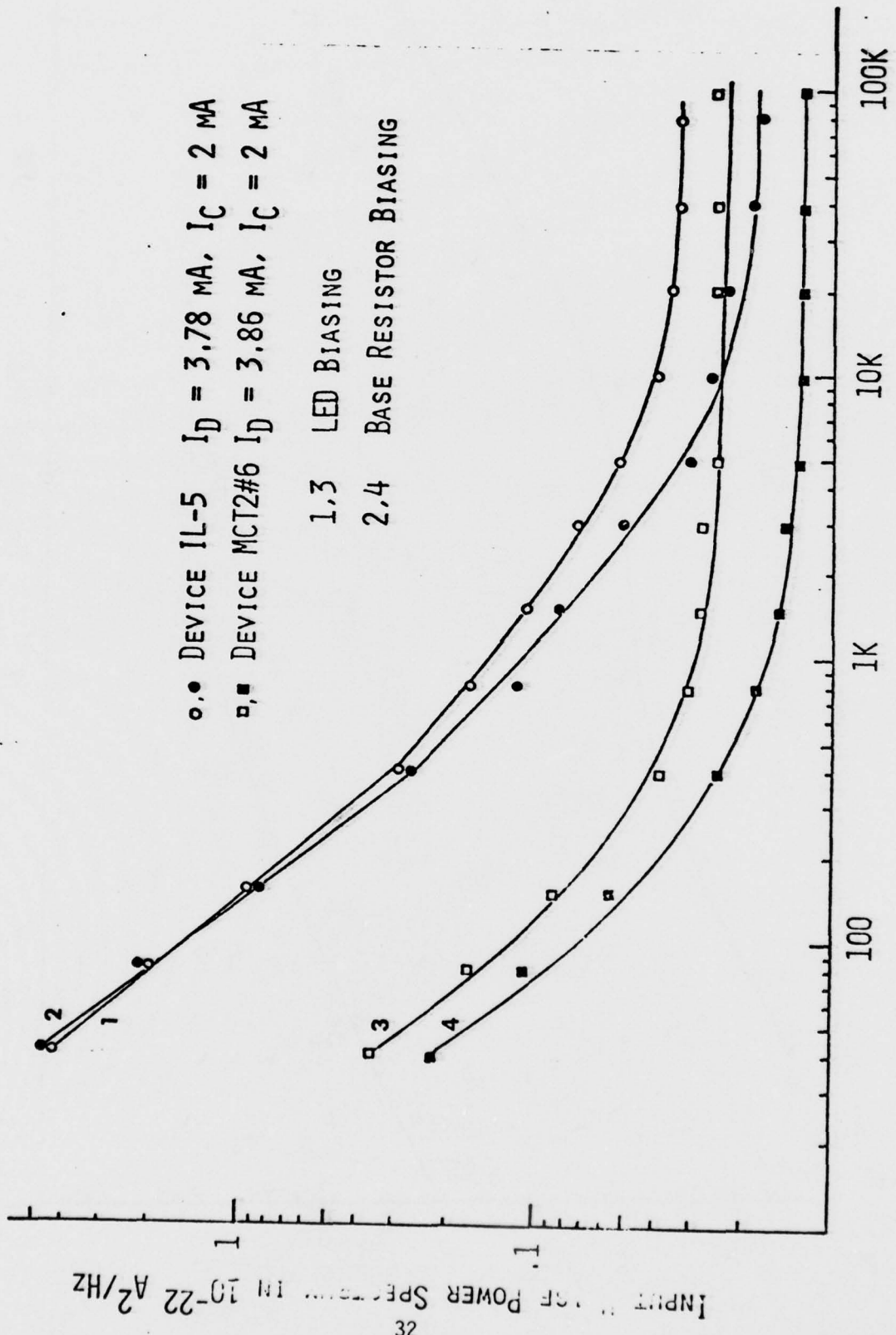


Figure 19

through a large impedance. The measured results for a typical device, IL-5, are shown in Figure 20. The equivalent input noise to the input of the optical isolator and to the base of the phototransistor differed by a factor of  $10^6$  (i.e.  $k^2$ ) over a wide range of frequencies. The results of this experiment demonstrate vividly that although the phototransistor optical isolator offers the advantage of electrical isolation between input and output, its noise performance suffers greatly from the loss of gain in the optical coupling system. Also, the results shown in Figure 20 indicate that  $k$  is independent of frequency over the frequency range examined.

#### G. Noise Model for the Phototransistor Optical Isolator

A noise model for the phototransistor optical isolator is presented in Figure 21. The right half is the electrical noise model of the phototransistor under ideal LED illumination (one which exhibits only shot noise in optical fluctuation) and the left half is the electrical noise model for the LED. In the phototransistor,  $i_{ph}^2$  and  $i_c^2$  are shot noise current generators. The contribution of flicker noise in the phototransistor is represented by two flicker noise current generators  $i_{f1}^2$  and  $i_{f2}^2$ . Burst noise in the phototransistor is represented by a current generator  $i_{bb}^2$  in the emitter-base junction. The noise current generator  $i_d^2$  accounts for the current fluctuation of the LED and usually, but not always, takes the form of flicker noise (eg. see Figure 14). All noise sources are defined in Figure 21.

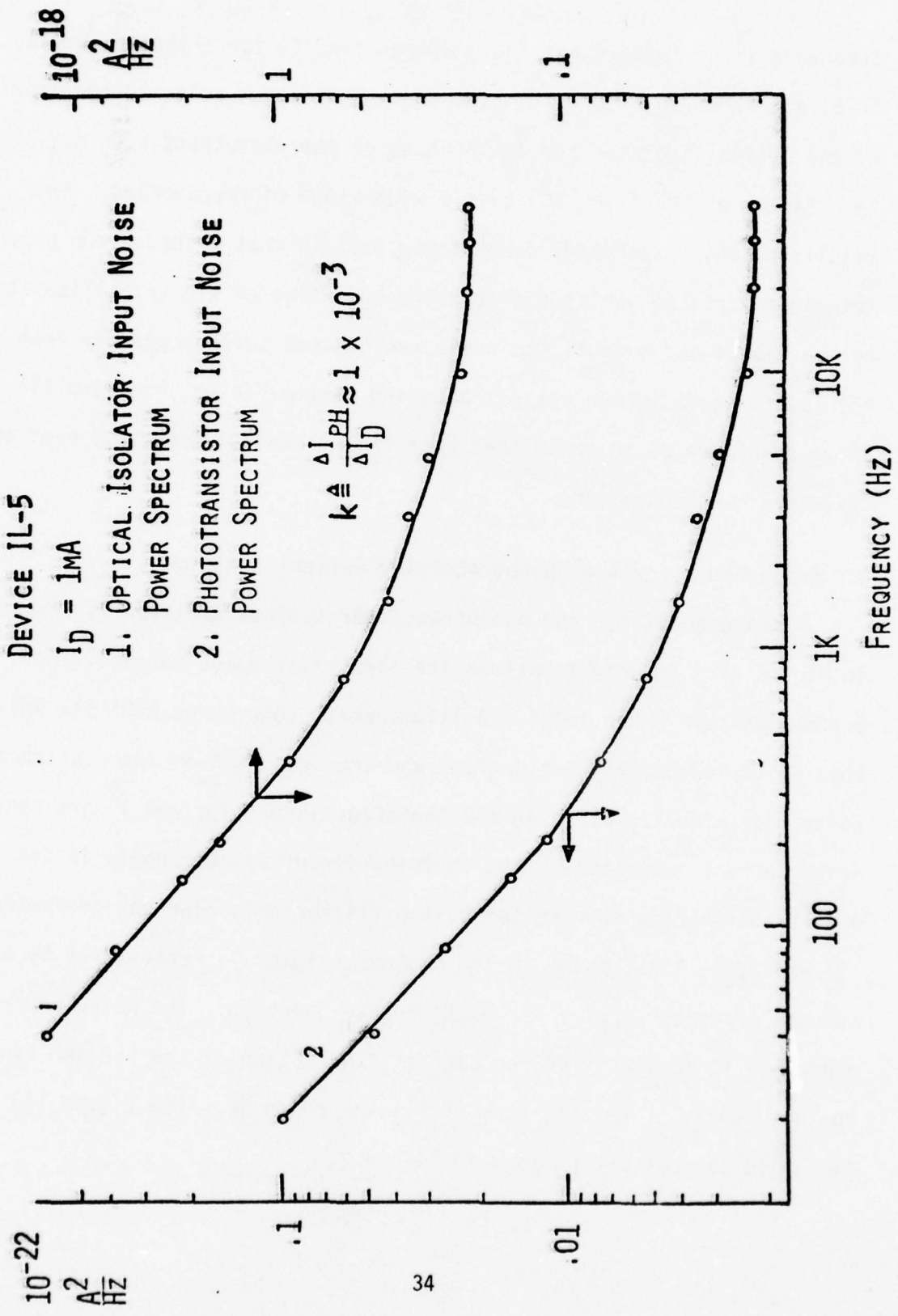
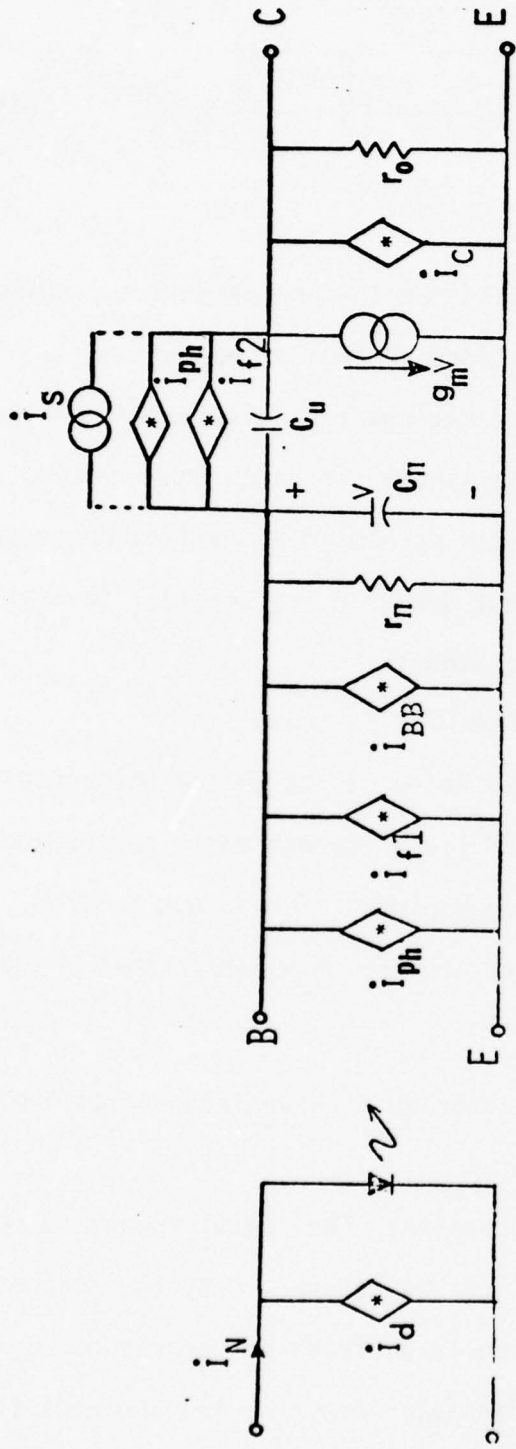


Figure 20



$$\bar{Z}_f = \bar{Z}_{f1} + \bar{Z}_{f2} = \frac{A I_{PH}^y}{f^{\alpha} \Delta f}$$

$$\bar{Z}_{BB} = \frac{A I_{PH}}{1 + (\frac{f}{f_B})^2} \Delta f$$

$$\bar{Z}_{ph} = 2q I_{PH} \Delta f$$

$$\bar{Z}_C = 2q I_C \Delta f$$

$$\bar{Z}_D \sim \frac{K}{f^{\beta}} \Delta f$$

Figure 21

The equivalent input noise of the optical isolator,  $\overline{i_n^2}$ , can be determined from the noise equivalent circuit to be:

$$\overline{i_n^2} = \frac{I_c^2}{k^2 h_{fe}^2} \left( 1 + \frac{f^2}{f_\beta^2} \right) + \frac{\overline{i_f^2} + \overline{i_{bb}^2} + 2\overline{i_{pH}^2}}{k^2} + I_d^2 \quad (14)$$

where  $2\pi f_\beta = 1/r_\pi (C_\pi + C_u)$ .

Examining the describing equations for the phototransistor noise sources we can distinguish three distinct regions of operation vs. frequency. In Figure 22 the separate regions are illustrated and the describing equations presented. This figure indicates the expected noise spectrum based on the noise model developed above (the curve is for illustrative purposes only and not drawn to any scale). Several important aspects can be seen in the figure:

- a. at low frequencies,  $1/f$  noise will dominate
- b. if burst noise or excess LED noise exists in the phototransistor, it can significantly degrade low frequency noise performance
- c. in the shot noise region the minimum noise is due to the phototransistor e-b junction shot noise which is multiplied by  $\frac{2}{k^2} \gg 1$
- d. the noise performance will degrade at high frequencies due to the frequency dependence of  $h_{fe}$ .

The last point is worth further discussion. The useful frequency range of the phototransistor optical isolator is determined by the frequency response of the phototransistor. The large feedback capacitance  $C_u$  (typically 20PF in the MCT2 phototransistor for example) enhances the

$$\dot{Z}_{IN} = \frac{\dot{Z}_C}{k h_{fe}} \left( 1 + \frac{f^2}{f_B^2} \right) + \frac{\dot{Z}_B + \dot{Z}_f + \dot{Z}_{BB} + \dot{Z}_D}{k}$$

$$\dot{Z}_{IN} \approx \frac{\dot{Z}_B}{k} + \frac{\dot{Z}_C}{h_{fe} k} \left( 1 + \frac{f^2}{f_B^2} \right)$$

NOISE INCREASE DUE  
TO TRANSISTOR GAIN  
DEGRADATION

1/f REGION

$$\dot{Z}_{IN} = \frac{K_1}{f^\alpha} + \frac{K_2}{f_B}$$

BURST NOISE OR  
EXCESS LED NOISE

$$\dot{Z}_{IN} = \frac{\dot{Z}_B}{k} \text{ SHOT NOISE}$$

$$f_c = \sqrt{2 h_{fe}} f_B$$

$\dot{Z}_{IN}$

(A<sup>2</sup>/Hz)

100

1000

10000

FREQUENCY (Hz)

Estimate 22

Miller Effect and therefore limits the useful frequency range of the optical isolator. The gain of the optical isolator will degrade rapidly at frequencies above

$$f'_\beta = \frac{g_\pi}{2\pi[(1 + g_m R_L)C_\mu + C_\pi]} \quad (15)$$

However, the noise performance of the optical isolator will not degrade until a much higher frequency  $f_c$  is reached where

$$f_c = \frac{2h_{fe}^2}{h_{FE}} \cdot f_\beta \approx 2h_{fe}f_\beta \quad (16)$$

assuming  $k$  is frequency independent. (This corner frequency is shown in Figure 22.) As a comparison for  $I_c = 1\text{mA}$ ,  $R = 1\text{k}\Omega$ ,  $h_{fe} = 400$ ,  $C_\mu = 20\text{pf}$  and  $C_\pi = 10\text{pf}$ , we have  $f'_\beta = 20\text{ KHz}$  and  $f_c = 1.4\text{ MHz}$ .

#### H. Check the Noise Model

To check the validity of the noise model as described by Equation (14), the equivalent input noise current for the phototransistor optical isolator was measured both in the low frequency region and in the shot noise region for different LED currents. The experimental data was then compared with Equation (14). Finally, the frequency dependence of the noise predicted by Equation (14) was compared to experiment results.

#### Shot Noise Region

The equivalent input noise current for devices 4N26 #3 and MCT2 #6 was measured at 20 KHz which was in the shot noise region for these

two devices. The results are shown in Figure 23. In the shot noise region Equation (14) reduces to

$$\overline{i_n^2} = \frac{4qI_{PH}}{k^2} = \frac{4q(K'I_D)}{k^2} \quad (15)$$

The calculated curves from Equation (15) are also shown in Figure 23. The experimental data and calculated data are found to be in good agreement.

#### 1/f Noise Region

The equivalent input noise current for device 4N26 #3, which was free of burst noise and excessive LED noise was measured at 40 Hz which is well within the 1/f noise region for this device. The measured result is shown in Figure 24. In the low frequency region where the flicker noise dominates, Equation (14) reduces to

$$\overline{i_n^2} = \frac{A_1(I_{PH})^\gamma}{k^2 f^\alpha} = \frac{A_1(K'I_D)^\gamma}{k^2 f^\alpha} \quad (16)$$

The constants  $A_1(1.18 \times 10^{-12})$  and  $\gamma(1.6)$  were determined by least-square-error curve fitting. The calculated data are also shown in Figure 24. Again, the experimental data and the calculated data are found to be in good agreement.

#### Frequency Dependence

In all cases it was found that equation 14 could be used to predict the frequency dependence of optical isolator noise. Figure 25 is typical of the results obtained. The experimental set-up was

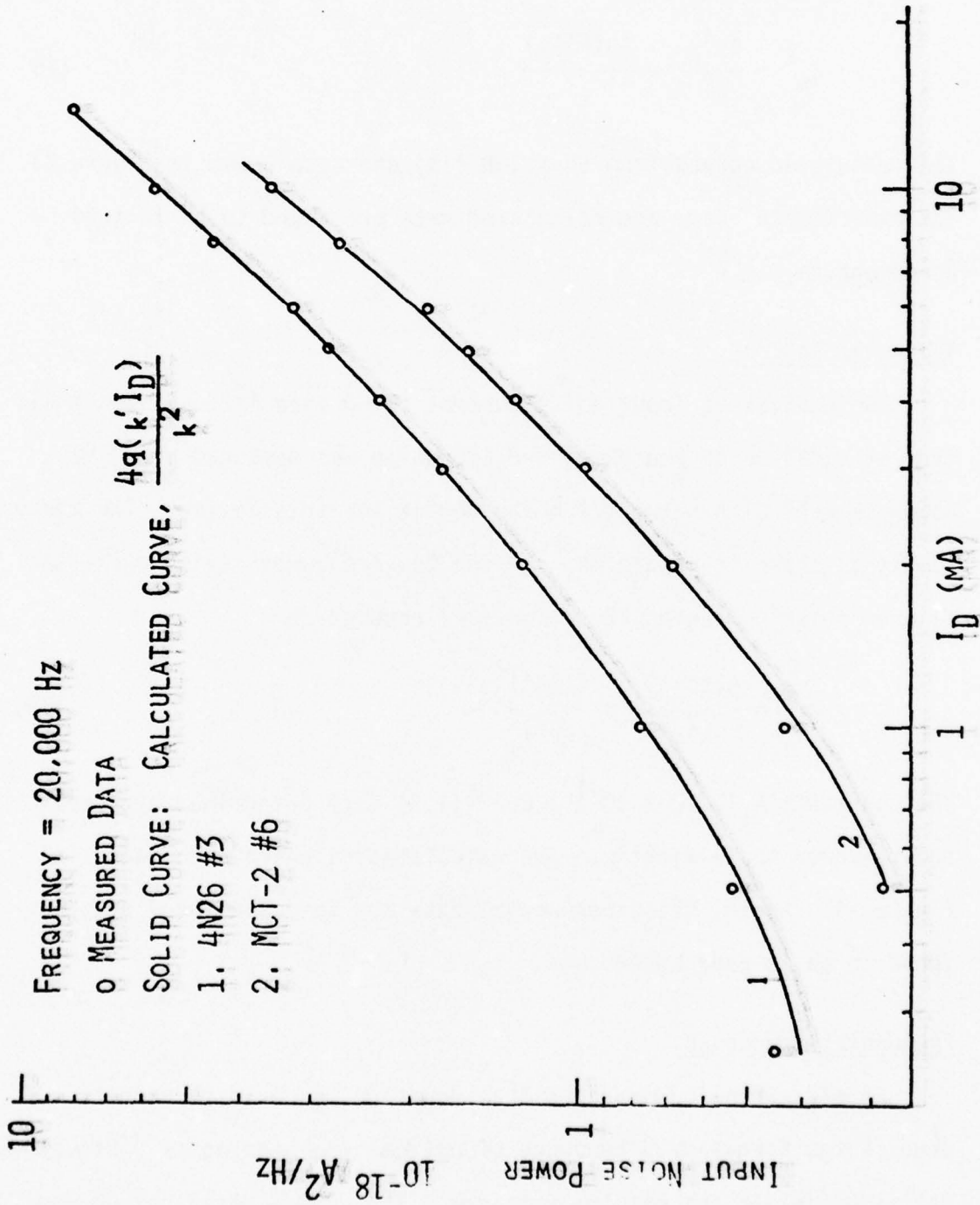


Figure 23

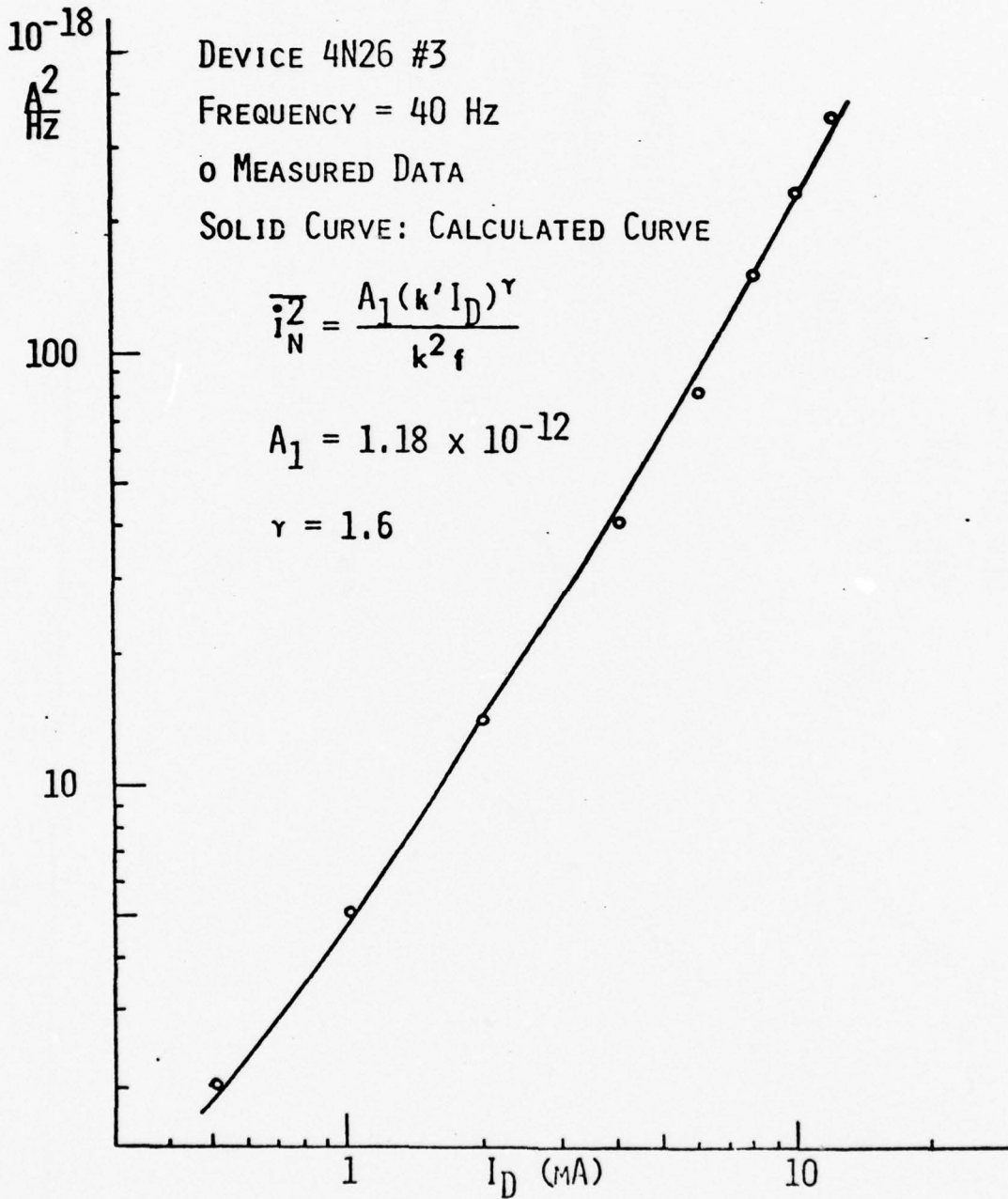


Figure 24

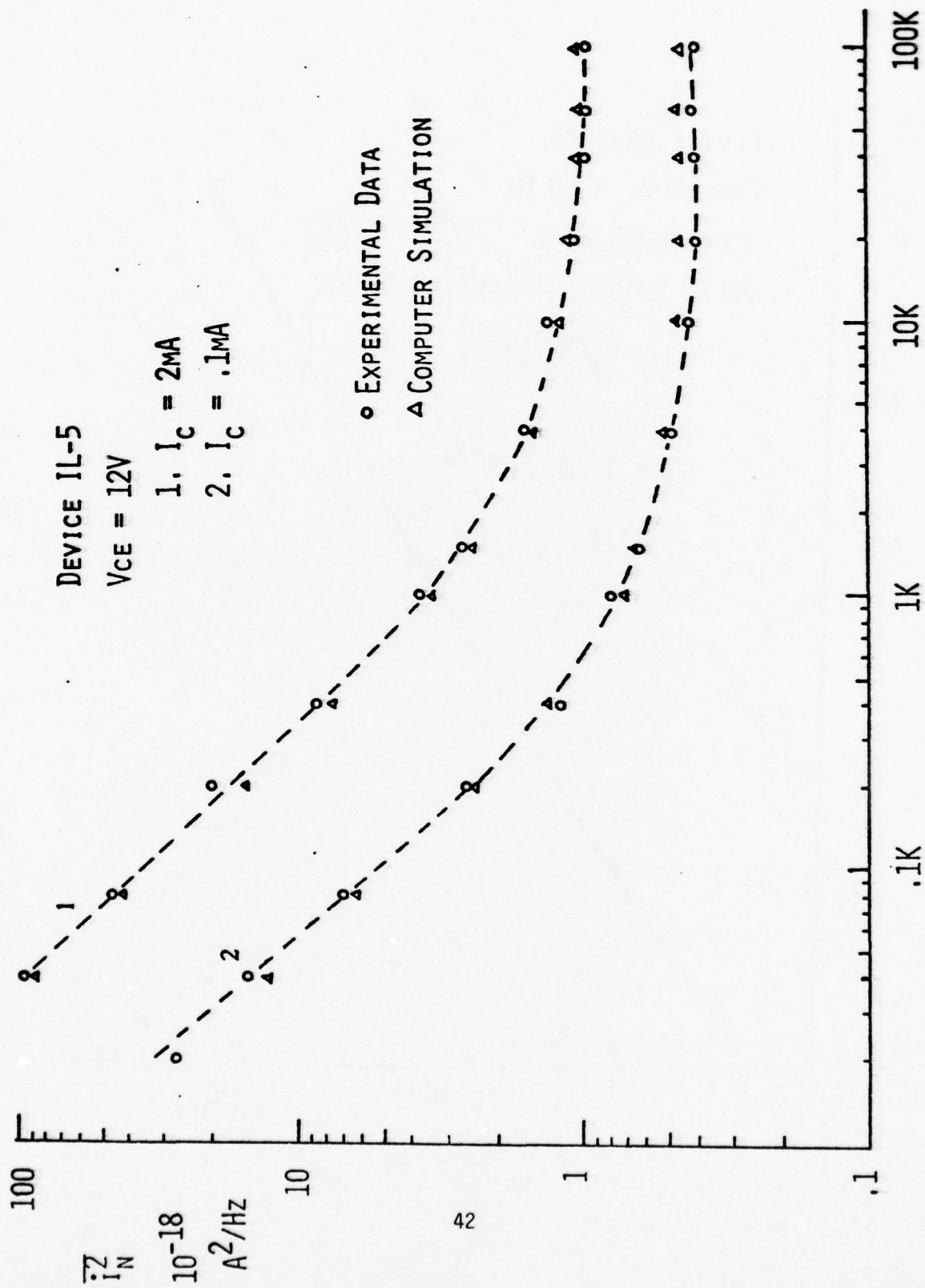


Figure 25

limited to frequencies below about 100 KHz. For this reason, we have not presented data at higher frequencies.

#### IV. Discussion

In this paper, the noise performance of several phototransistor optical isolators has been presented. A noise model for the optical isolator was developed which predicts the equivalent input noise if the necessary constants  $A_1$ ,  $A$ ,  $\gamma$ ,  $k$  and  $k'$  are available. The magnitude of the equivalent input noise of phototransistor optical isolators has been shown to be large relative to bipolar junction transistors.

Improved noise performance is obtained in a given device by operating the LED at low currents. Resistance connected to the phototransistor base should be large compared to the e-b junction dynamic resistance  $r_{\pi}$ . The best noise performance is achieved with the base terminal left floating as the effect of base resistance will be to reduce the gain of the phototransistor and therefore degrade the noise performance of the optical isolator as shown in Figure 26. Further improvements in the noise performance can only be obtained by use of optical isolators with low noise LEDs, lower noise phototransistors and better coupling between the LED and the phototransistor to maximize  $k$ .

Finally, because the phototransistors in the optical isolators examined were typically very noisy devices compared to the best low noise transistors available, the optical isolators were more noisy than necessary. Improved low noise performance can be achieved in critical circuit designs by using commercially available optical isolators with diode detectors which can drive very low noise gain stages.

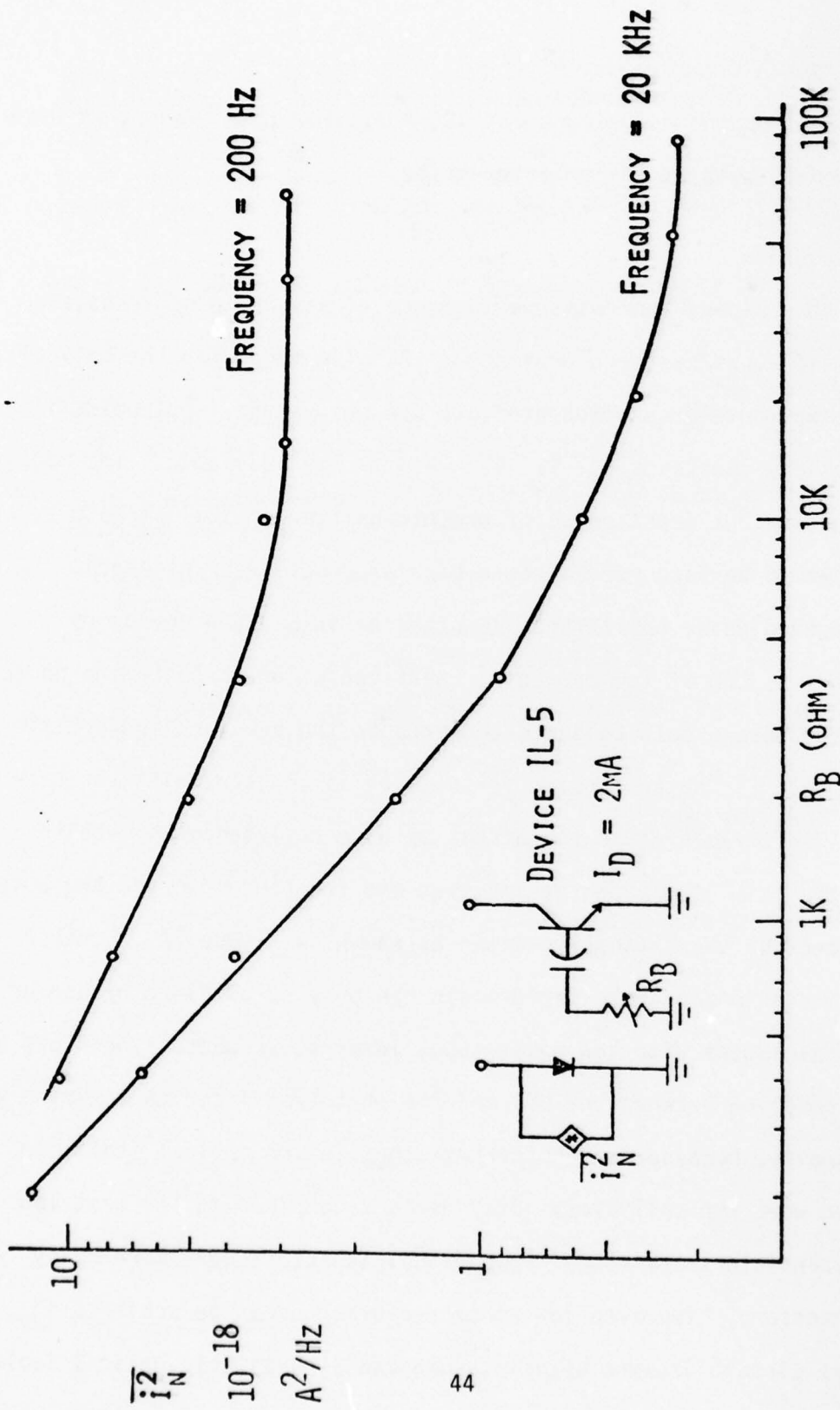


Figure 26

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Part 5

SUPPORT SOFTWARE FOR A GENERAL PURPOSE  
LOGIC SIMULATOR

Prepared for  
U.S. Army Missile Command  
Redstone Arsenal, Alabama

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## INTRODUCTION

A general purpose digital logic simulator is under development for the purpose of education and research. The simulator package was required for two reasons; to update a previously developed simulator used for educational purposes, and to provide a package more accurate in simulation and more capable in functions, for the needs of research.

The package itself is made up of a number of programs in various stages of development. The programs are written in BASIC-PLUS and are designed to run on a PDP 11/40 facility. The primary mode of user interaction with the programs is through Tektronix graphic terminals. The package provides the user with the means of inter-actively testing and debugging a combinational or sequential circuit during the specification and design stages of development. In addition, the package provides a student the means of designing a network and exploring its characteristics without having to realize his or her design in hardware.

## CONTROL PROGRAM DESCRIPTION

Linking the programs together into a cohesive unit, the controlling program CONTRL acts as the primary user interface to the simulator package. At initial sign-on, the user is presented with a high level control menu, as shown in Figure 1. The user positions the cursor block at the selected option box and types 'X' on the keyboard. The appropriate program or programs are then called in correct sequence. Upon completion of the activity selected by the user, control is returned to the coordinating program.

## Figure 1

## DIGITAL LOGIC SIMULATOR PACKAGE

TO SELECT AN OPTION, MOVE CURSOR BLOCK TO APPROPRIATE BOA AND TYPE "X".

TO MOVE CURSOR:      TYPE SPACE TO MOVE DOWN  
                          TYPE BACKSPACE TO MOVE UP

DESCRIBE NETWORK		[ ]
ENTER FAULTS		[ ]
TAG LINES FOR DISPLAY		[ ]
ENTER INPUT SEQUENCE		[ ]
SIMULATE NETWORK		[ ]
NETWORK DESCRIPTOR FILE; SAVE		[ ]
	RETRIEVE	[ ]
	DELETE	[ ]
TIMING DIAGRAM FILE; SAVE		[ ]
	RETRIEVE	[ ]
	DELETE	[ ]
EXIT		[ ]

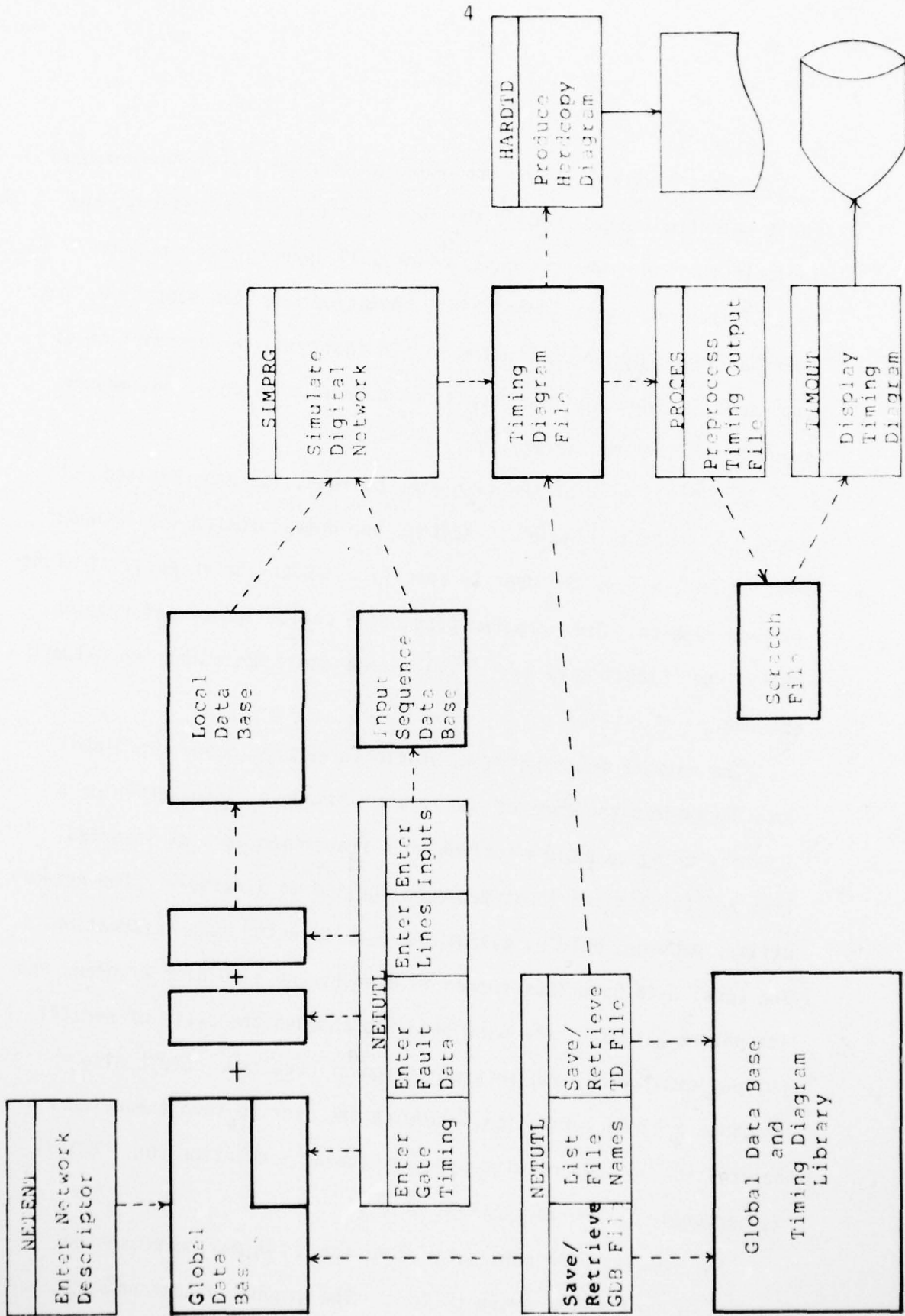
Options available allow the user to describe his or her network, fault selected lines, specify the input pattern to the network, and indicate the lines whose signal values will appear in the output file of the simulator. Once this information has been specified, the user may then simulate the network. In addition, the description of the user's network, or the results of a previous simulation, may be saved in the system library.

An overall view of the simulator package, its programs and data bases, is shown in Figure 2. NETENT, the entry program (still under development) allows the user to specify a network in an easy, straightforward fashion. This program produces a collection of information, called the "Global Data Base," which completely describes the network entered.

The network description is static in nature, hence the Global Data Base forms the core of the network "image." Information of a dynamic, changing nature include gate transition delays, inserted line faults, and the input sequence applied to a network. The network utility package, NETUTL, allows the user to enter such information. The Local Data Base thus formed is used by the simulator program, and its nature alters as the user iterates through the cycle of specification, simulation, and interpretation of results. NETUTL also provides a library function, allowing the user to save the network description, or the results of a particular simulation run. NETUTL is currently in the development stage.

The results of a particular simulation run may be presented either in hardcopy or graphics form. The graphic output package,

Figure 2



TIMOUT, displays the simulation results in the form of the ubiquitous timing diagram. This display package allows the user to select the order in which network line signals are presented, and the time window in which they are viewed. With the exception of minor interfacing details, TIMOUT and the simulator program SIMPRG as well as the preprocessing program PROCES, are all complete.

#### NETWORK INPUT PARSER

A hardware language was developed to allow the user of the simulator package to describe an arbitrary network of gates and storage elements. The user may assign names of up to six characters in length to each network line. The language format is shown in Figure 3. Gate operations upon lines are of the form:

$$\langle \text{line-name} \rangle = \langle \text{function} \rangle (\langle \text{line-name} \rangle, \langle \text{line-name} \rangle, \dots)$$

where  $\langle \text{function} \rangle$  can be AND, OR, NOT, NAND, NOR and XOR. Function names without an argument list include INPUT, CONSØ, CONST, and CLOCK. Figure 4 illustrates how a simple combinational network is described with this language.

Memory elements can also be used when describing a sequential circuit. The format for flip-flop description is:

$$\langle \text{label} \rangle : \langle \text{line-name} \rangle, \langle \text{line-name} \rangle = \langle \text{FF-type} \rangle$$

$$(\langle \text{line-name} \rangle, \langle \text{line-name} \rangle, \dots)$$

This assignment format is positional dependent. The two line-names on the left of the parentheses are the Q and  $\bar{Q}$  outputs. The flip-flop

Gate Assignment Format

<line-name> = <function>

where <function> ::= INPUT, CLOCK, CONS0, CONS1

<line-name> = <function> ( <list> )

where <function> ::= AND,OR,NOT,NAND,NOR,XOR

Flip-Flop Assignment Format

<line-name> , <line-name> = <FF-type> ( <input-list> )

where <FF-type> ::= DC, SR, JK, JKC, JKSRC

Function Format

FUNCTION <function-name> ( <output-list> ; <input-list> )

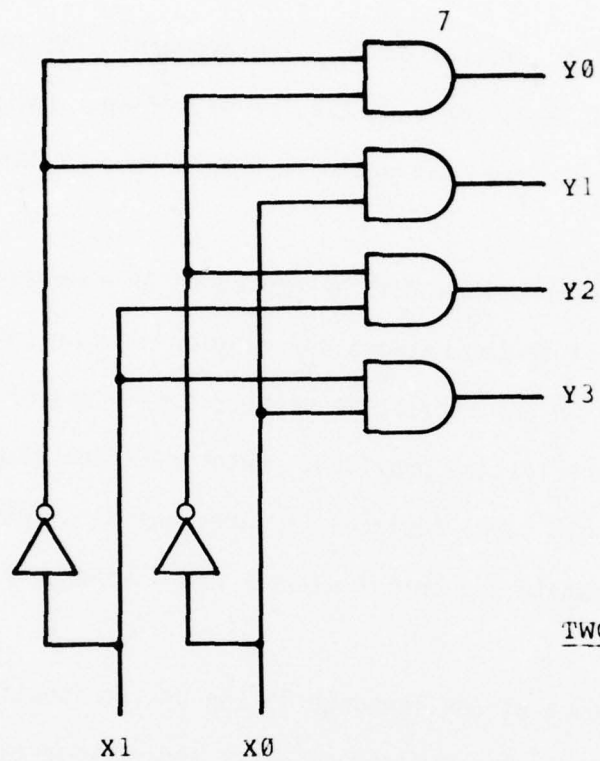
·  
·  
·  
body  
·  
·

FNEND

Usage

<output-list> = <function-name> ( <input-list> )

Figure 3



TWO BIT DECODER

CIRCUIT DESCRIPTION

$X0 = \text{INPUT}$   
 $X1 = \text{INPUT}$   
 $X0\text{BAR} = \text{NOT}(X0)$   
 $X1\text{BAR} = \text{NOT}(X1)$   
 $Y0 = \text{AND}(X0\text{BAR}, X1\text{BAR})$   
 $Y1 = \text{AND}(X0, X1\text{BAR})$   
 $Y2 = \text{AND}(X0\text{BAR}, X1)$   
 $Y3 = \text{AND}(X0, X1)$

Figure 4

types can be DC, SR, JK, JKC, or JKSR. The argument list corresponds to the order of input lines for a particular flip-flop. For example, the JKC flip-flop input line list would be J line-name, K line-name and clock line-name.

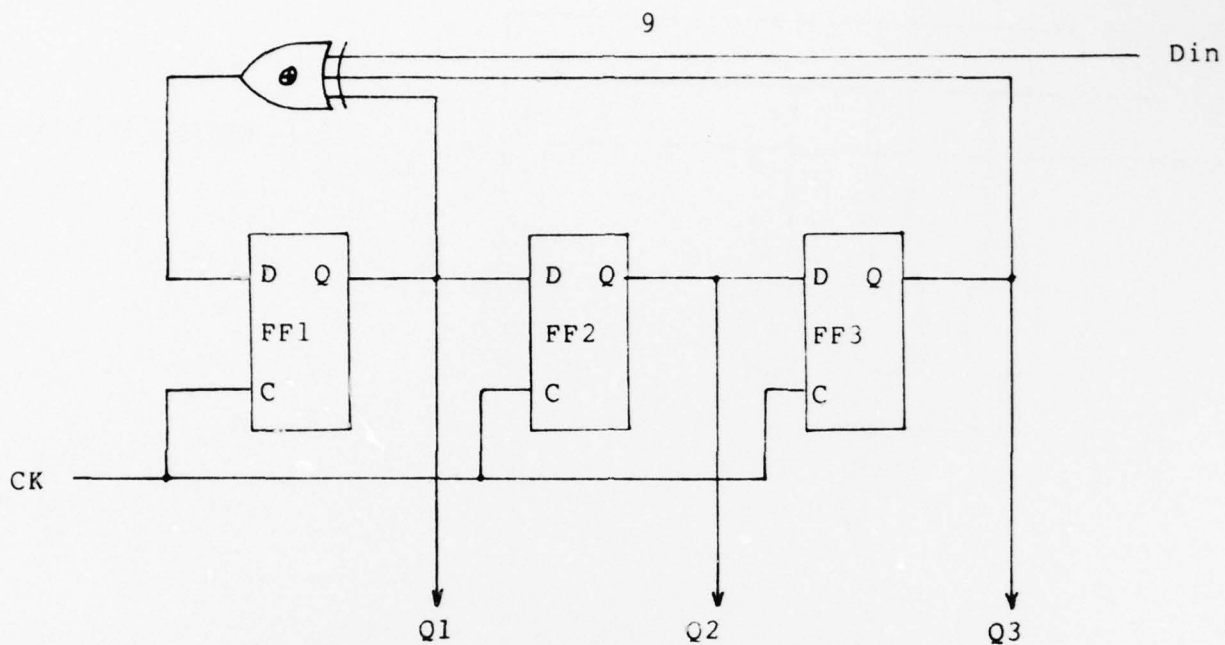
All flip-flop descriptions must be preceded by a unique identifying label. Since the network description will be entered through the keyboard in an interactive manner, some means of correcting a previous description must be provided. Entering a new flip-flop description with an old label replaces the previous description with the same label. A sample sequential network and its description is shown in Figure 5.

A powerful feature of the language is the use of function macros. The user can describe a common block of gates and storage elements once, and then use the function in other parts of the hardware description. Many useful system functions will be available, allowing the user to work with functional subunits as well as at the gate level. A functional description of a full adder and its use in a circuit description is shown in Figure 6.

The format for the FUNCTION macro is:

```
FUNCTION<FN-name>(<output-list>;<input-list>)
```

where <FN-name> is the name of the function, and each list is composed of dummy line-names preceded by '%'. The body of the macro is terminated by FEND.



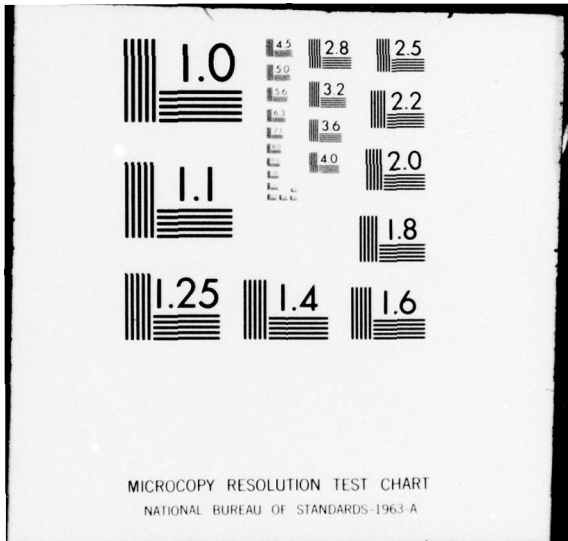
SAMPLE SEQUENTIAL NETWORK

NETWORK DESCRIPTION

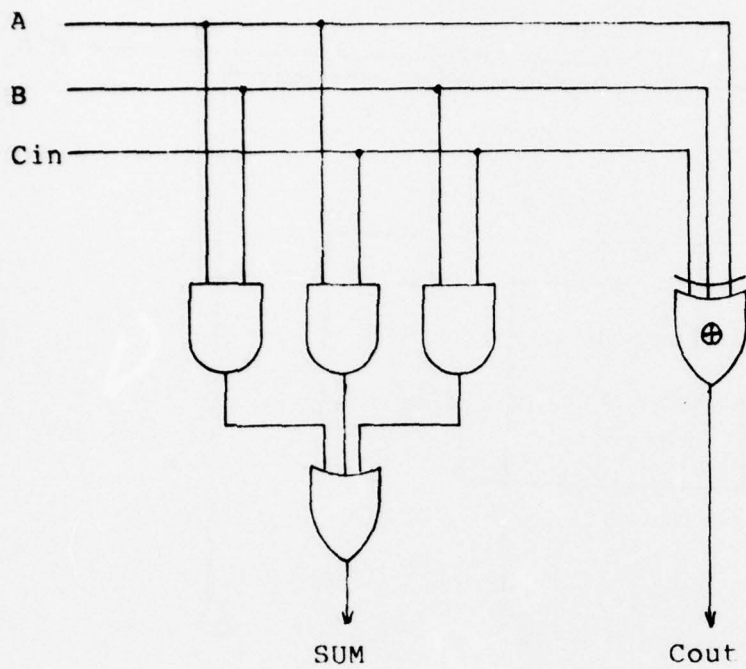
DIN=INPUT  
 CK=CLOCK  
 FF1:  $Q1, =DC(D1, CK)$   
 FF2:  $Q2, =DC(Q1, CK)$   
 FF3:  $Q3, =DC(Q2, CK)$   
 $D1=XOR(DIN, Q1, Q3)$

Figure 5





MICROCOPY RESOLUTION TEST CHART  
NATIONAL BUREAU OF STANDARDS-1963-A



FULL ADDER CIRCUIT

FUNCTION DESCRIPTION

```
FUNCTION ADDER(%SUM,%COUT;%A,%B,%CIN)
```

```
  %SUM=XOR(%A,%B,%CIN)
```

```
  %1=AND(%A,%B)
```

```
  %2=AND(%A,%CIN)
```

```
  %3=AND(%B,%CIN)
```

```
  %COUT=OR(%1,%2,%3)
```

```
FNEND
```

```
  .
```

```
  .
```

```
  .
```

```
  .
```

```
S1,C01=ADDER(A1,B1,C00)
```

```
  .
```

```
  .
```

Figure 6

## SYSTEM SUPPORT UTILITY PACKAGE

Utility functions provided can be divided into two classes; library maintenance and data base manipulation. The functions are organized into a single program which can be accessed by various processes in the simulator package.

The library functions allow the user to store and retrieve Global Data Base and Timing Diagram files in the system library. This capability greatly eases the user's workload, since a network need only be described once. The user can also save the timing diagram results of a particular simulation run for later review. Thus, the user need not proceed through the entire simulation cycle in order to reproduce results of interest.

Other functions of the utility package are concerned with the manipulation of the Global Data Base descriptor for use by the simulator. Because of disk space limitations, only the descriptor produced by the network input parser is saved.

Additional information must be appended to the descriptor before it can be processed by the simulator. The user must specify gate delay timing for each class of gate. Delays may be specified in terms of min/max delay times or as rise/fall transition times. This information is stored in the Global Data Base descriptor, since these values usually don't change.

Specific internal network lines can be tagged so that the state of these user selected lines will appear in the Timing Diagram file output of the simulator. Network I/O lines are automatically tagged. The user also enters the input sequence pattern immediately prior to simulation of the network.

As the user iterates through the simulation cycle, any of the above dynamic information can be altered. This information which is built around the descriptor core exists only for the life of the terminal session.

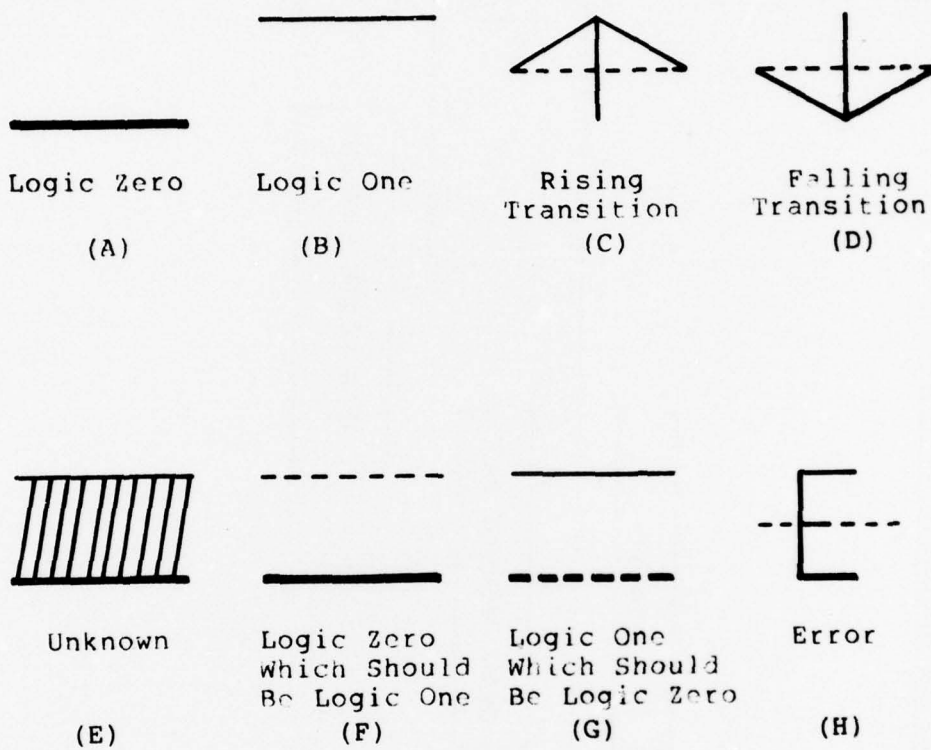
#### GRAPHIC OUTPUT PACKAGE

The graphics output package was developed to provide the user with a simple format for interpreting simulation results. The output is presented in a standard format, the timing diagram.

The output package works with logic zero, logic one, and six other signal values (see Figure 7). Gate transition delays can be depicted in one of two ways; as rise and fall transitions, or as unknown signal values. In the transition mode, an error value can be generated when a gate is presented with both rising and falling inputs. Stuck-at fault values are represented by the logic zero which should be logic one, and logic one which should be logic zero signal values. This allows the user to study the effect of propagating such an error in a parallel fault/fault-free manner.

The graphics program was developed using a top-down approach. Module hierarchy is shown in Figure 8. The main routine first calls the menu options module to request information from the user. The menu page format is shown in Figure 9.

Menu options are divided into four groups, plus a control group. The first group, a single option, allows the user to request a simulator output file other than the one associated with the current simulation run. This option is used in conjunction with the timing diagram library save and retrieve functions.



LOGIC SIGNAL VALUES

Figure 7

TIME-OUT MODULE HIERARCHY

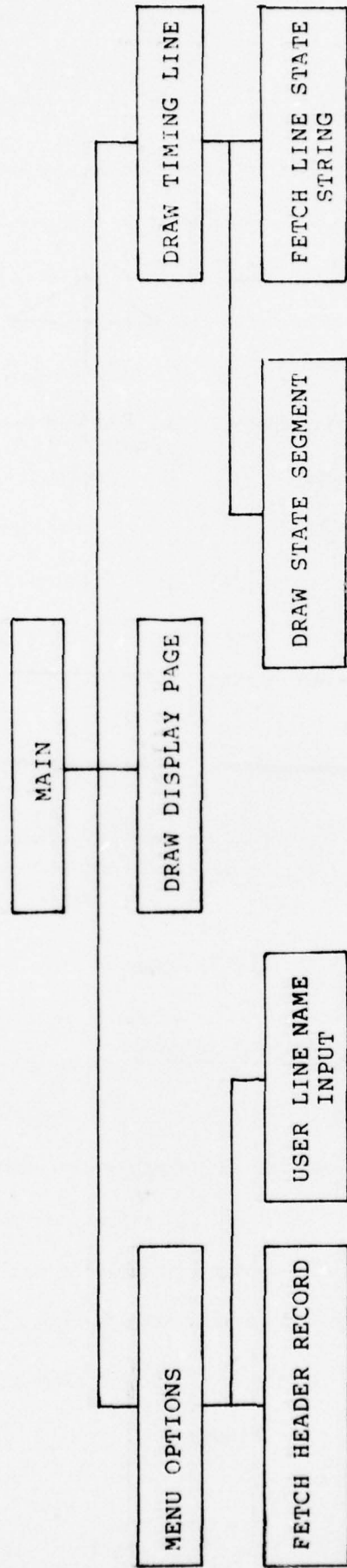


Figure 8

DISPLAY OPTIONS

OPTIONAL INPUT FILE [ ]  
 DISPLAY ALL LINES [ ]  
 I/O LINES [ ]  
 USER SELECTED [ ]

TIME WINDOW

ENTIRE SIMULATION [ ]  
 MIN & MAX TIMES [ ]  
 MIN TIME & INCREMENT [ ]

TIMING GRID

REGULAR GRID [ ]  
 NO GRID [ ]

CONTINUE [ ]  
 SPECIFY NEW OPTIONS [ ]  
 EXIT PROGRAM [ ]

Figure 9

The next group allows the user to select which lines to be displayed. All tagged network lines, network input/output lines, or a user selected subset of lines can be chosen for display.

The third group specifies the time window in which the lines will be displayed. The Entire Simulation option allows the user to view the total simulation run, and the other two options are used to display specific portions of interest. The increment value in the Min Time & Increment refers to the time difference between successive grid markers on the timing diagram display page.

The fourth group lets the user choose whether or not vertical grid markers are to be included on the timing diagram display.

Once the appropriate options are selected, the user may CONTINUE, return and MODIFY ANY OPTION or EXIT. As the user continues, any necessary information needed for the options selected is requested.

#### PROCES.BAS

The purpose of the preprocessor program, PROCES.BAS, is to transform the output file from the simulator into a file which can be used by the TIMOUT graphic output program. The simulator output file, designated Timing Diagram file in Figure 2, is an ASCII text file. The format of this file is shown in Figure 10, and the input file to the graphics program is shown in Figure 11.

The data in the Timing Diagram file contains general information on the network, and information pertaining to the simulation of the network. Among the general items passed are the number of tagged lines

## SIMULATOR OUTPUT FORMAT

(input to PROCES)

```
(# of network lines),(# of I/O lines),(time scale value)
(line #),(line #),(line #), . . . ,(line #)
(I/O line #),(I/O line #), . . . ,(I/O line #)
(header string)
(event time)
(line state),(line state), . . . ,(line state)
(event time)
(line state),(line state), . . . ,(line state)
.
.
.
(event time)
(line state),(line state), . . . (line state)
(-1)
```

NOTE: (line #) vector consists of all tagged lines, including I/O lines.  
(line state) vector is the state of all tagged lines at a given event time. There is a one-to-one correspondence between the line number vector and the line state vector.

Figure 10

INPUT DATA FILE ORGANIZATION FOR TIME-OUT (RANDOM ACCESS RECORD I/O)

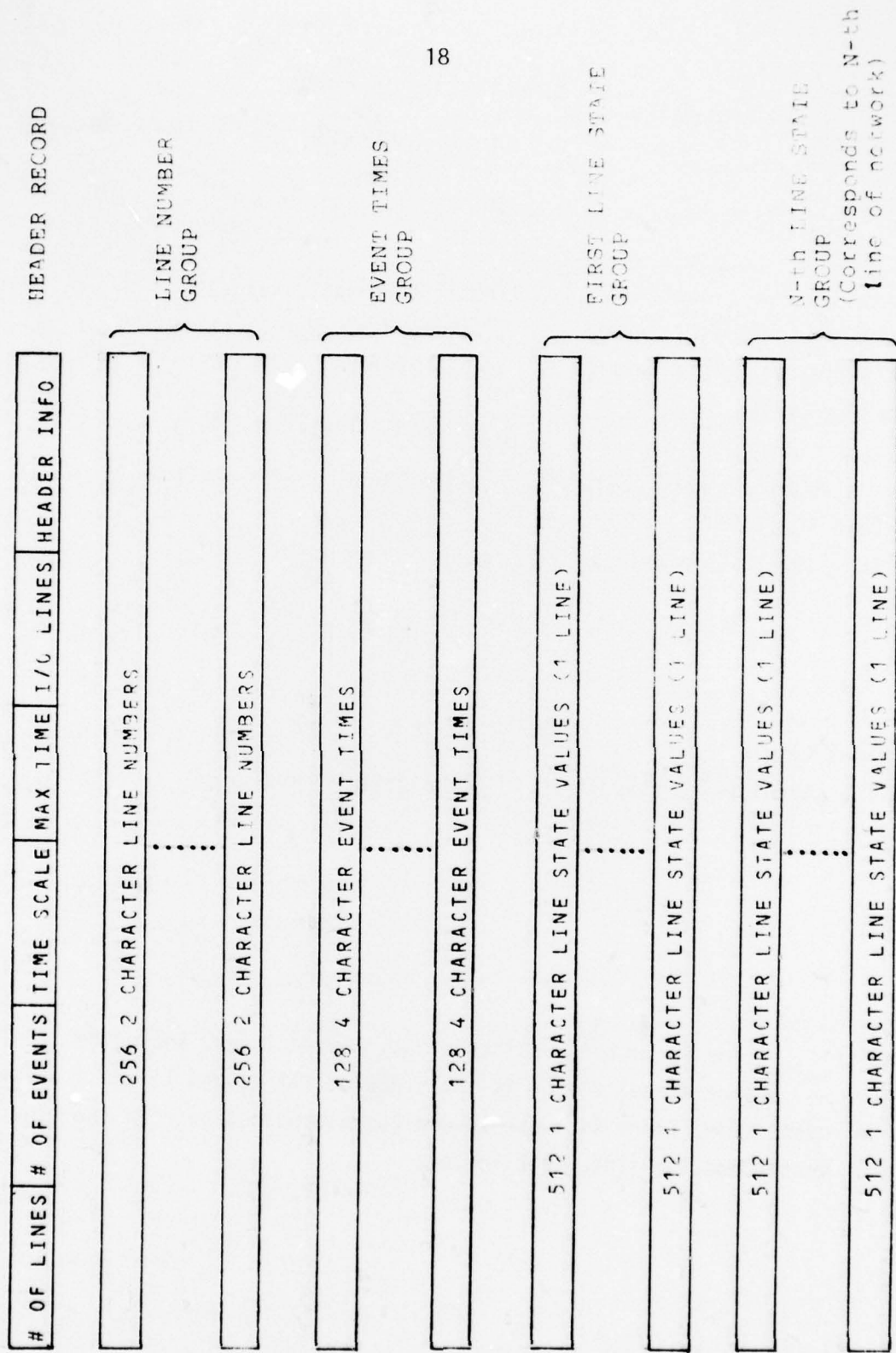


Figure 11

in the network, the number of input/output lines, a time scale value and a header string.

When a network line changes value during simulation, the simulator outputs the time of occurrence, followed by the state of each tagged line at that time. The internal representation of states in the simulator is a numeric value, while the graphic package works with alphabetic representation. A function, FNS%, is used for this simple transformation.

#### TIMOUT MODULE DETAILS

The TIMOUT graphic output package was developed in a top-down manner, with primary functions broken up into separate subroutines. The three primary subroutines are the menu options routine, the display page routine, and the timing line routine. Each main routine may call one or more subordinate routines, and the package also contains a number of functions for graphics interface with the Tektronix terminal. Subroutine and function operation is outlined in the following sections.

The main program coordinates the various subroutines in the graphics package. The code is quite short, consisting of mostly subroutine calls, conditional processing, and variable initialization.

The sequence of execution in the main program begins with initialization. The menu page subroutine is first called, and the menu options array is used for further processing. The basic timing diagram page is drawn, and the menu options array is checked to see which set of lines is to be displayed (ALL LINES, I/O LINES, USER SELECTED LINES).

The main program then displays a timing diagram. The format of a diagram is shown in Figure 16. Up to ten network lines can be displayed on the diagram. If more lines were selected than can be displayed on a single diagram, the user may CONTINUE to the next page. The user may also return to the option selection phase to alter the viewing format.

A useful option available on the timing diagram display page is TIME. Selection of this option displays a vertical cursor line. The user may position this line at a point or transition of interest and obtain the time at which the event occurred.

A scratch vector of length ten is filled with the first ten lines to be displayed. The timing line routine is called, with the line number and its position in the display passed to the routine. When finished, the mini options menu at the bottom of the display page is checked. If CONTINUE is selected, the above process is repeated with the next group of ten lines until either all lines selected have been displayed, or another option was chosen.

The user may choose to modify any of the options previously selected, in which case the main procedure repeats the sequence of menu selection, display page presentation, and timing line display. Upon exiting the graphic package, control is passed to the program responsible for coordinating the various programs in the overall simulator package.

#### MENU OPTIONS

Upon entry to the graphic package, the program first displays a menu page, as shown in Figure 9. The blinking cursor block is then

positioned to the first option block and the function FNK\$ is invoked. This function will return the character typed by the user, without echoing the character to the screen. If the user types space, the cursor is moved down to the next option block. If backspace is typed, the cursor is moved up to the next option block. Should the cursor move up or down beyond the display, the cursor wraps around to the bottom or top option block.

When the user types 'X', the option selected is entered into the menu options array and the cursor is moved down. The format of the options array is shown at the bottom of Figure 12. When the control group option 'CONTINUE' is selected, the menu options routine shows a new option page, with only the control option group in the lower right hand corner. If any option selected by the user requires additional information from the user, the data is then requested. If user selected line names was chosen, the routine for collecting this information is invoked.\* Once 'CONTINUE' is poked, the header record from the input file is fetched and disassembled. The line-number record(s) and event-times record(s) are also fetched and stored in arrays L\$ and E() respectively.

#### USER LINE NUMBER (NAME)\* INPUT

This routine requests user line number input. An asterisk is displayed, and the user then enters line numbers, separated by blanks or commas. Using the substring function available in BASIC-PLUS,

---

\*Note: The use of line names rather than line numbers is an addition not yet implemented. Implementation details are dependent on the NETENT network entry program, not yet fully developed.

MENU OPTIONS SELECTION

STEP	PROCESS	NEXT STEP (Y/N)	OUTPUTS
1	PRINT MENU AND POSITION CURSOR.	2	O%( ) -MENU OPTIONS ARRAY
2	IF USER TYPES SPACE, MOVE CURSOR DOWN.	2/3	
3	IF USER TYPES BACKSPACE, MOVE CURSOR UP.	2/4	
4	IF USER TYPES "X", ENTER SELECTION AND MOVE CURSOR DOWN.	5/2	
5	IF OPTION WAS "CONTINUE", GO TO NEXT OPTION PAGE.	8/6	
6	WAS OPTION "MODIFY ANY OPTION"?	1/7	
7	WAS OPTION "EXIT PROGRAM" ?	9/2	
8	EXIT PROCESS.	RET	
9	EXIT PROCEDURE.	END	

COMMENTS	
<u>MENU OPTIONS ARRAY</u>	
O%(1) =	0 DEFAULT FILE 1 USER SPECIFIED INPUT FILE
O%(2) =	0 DISPLAY ALL LINES 1 DISPLAY I/O LINES 2 DISPLAY USER SELECTED LINES
O%(3)	1 REGULAR GRID 2 NO GRID

Figure 12

## USER SPECIFIED LINE NAME INPUT

STEP	PROCESS	NEXT STEP (Y/N)
1	DISPLAY INSTRUCTIONS.	2
2	DISPLAY PROMPT AND RETRIEVE LINE.	3
3	IS LINE EMPTY? (Null)	5/4
4	CONVERT AND STORE LINE NAMES.	2
5	EXIT PROCESS.	RET

OUTPUT	
L2%()	USER-SPECIFIED LINE NUMBER ARRAY

Figure 13

individual line numbers are taken from the input string entered by the user, and the alphanumeric representation is converted to an integer by the function VAL. Line numbers are stored in the array L2%, with the variable N5% pointing to the last entry in the array. Line number input is terminated by typing carriage return when the prompt is displayed. See Figure 13.

#### HEADER RECORD INPUT

General information concerning the network, contained in the first record of the input data base, is fetched by this routine. Data such as the number of network line signals included in the data base and the number of simulation events are converted and stored in various program variables and arrays (see Figure 14). In addition the network line numbers and the list of event times are also fetched from their respective record(s) and stored in arrays. Previous information obtained from the header record is used to calculate the number of records used to store this data. The event-times array is later used by the timing line routine to draw the output signals requested by the user.

#### DISPLAY PAGE ROUTINE (Figure 15)

The basic timing diagram page, with or without grid markers, is drawn by this routine. Pertinent attributes of the display page, such as size, distance between timing lines, and number of timing lines per display page are assigned to variables so these characteristics can be altered to fit a particular installation. The routine draws the timing diagram page boundaries, the header string from the user and a mini

## FETCH HEADER RECORD

STEP	PROCESS	NEXT STEP (Y/N)	OUTPUT
1	FETCH FIRST RECORD.	2	N1% # OF NETWORK LINES
2	CONVERT AND STORE HEADER INFORMATION.	3	N2% # OF SIMULATION EVENTS
3	FETCH AND CONVERT LINE NUMBER RECORD(S).	4	N3% TIME SCALE FACTOR
4	FETCH AND CONVERT EVENT-TIMES RECORD(S).	RET	N4 MAX SIM. TIME
			H\$ HEADER
			L1%() I/O LINE NUMBERS
			L\$ LINE # STRING
			E() EVENT-TIMES ARRAY
			C1% NUMBER OF EVENT-TIMES RECORDS
			C2% NUMBER OF LINE-STATE RECORDS/LINE
			C3% NUMBER OF LINE-# RECORDS

COMMENTS
<u>INPUT FILE ORGANIZATION</u>
FIRST RECORD- HEADER RECORD
ONE OR MORE LINE NUMBER RECORDS (256 line #/record)
ONE OR MORE EVENT-TIMES RECORDS (128 event times/record)
ONE OR MORE LINE-STATE RECORDS FOR EACH LINE (512 states/record)

Figure 14

## DRAW DISPLAY PAGE

INPUT	STEP	PROCESS	NEXT STEP (Y/N)
O%( ) OPTIONS ARRAY	1	DRAW PAGE BOUNDARY LINES.	2
O%(4)=0 REGULAR GRID	2	PRINT OPTIONS MENU.	3
O%(4)=1 NO GRID	3	PRINT "LINE" HEADING.	4
	4	PRINT HEADER LABEL AT TOP OF DISPLAY.	5
	5	PRINT "TIME" HEADING.	6
	6	REGULAR GRID OPTION?	7/10
	7	DRAW GRID.	8
	8	CALCULATE START, END, AND INCREMENT TIMES.	9
	9	PRINT TIME VALUE FOR EVERY OTHER GRID LINE.	10
	10	EXIT PROCESS.	RET

Figure 15



options menu at the bottom of the display. If 'REGULAR GRID' option was chosen by the user, vertical timing grid markers are drawn and the time at every other marker is printed below the marker. The format of the display page is shown in Figure 16.

#### DRAW TIMING LINE (Figure 17)

The main routine passes the line to be displayed and its position on the diagram (slots 1-10). This routine then checks the line number array obtained from the input data base for a match. If not found, an error occurs and the signal value for that line is not displayed.

If found, the line state string for the requested line is fetched. The line number is printed in the appropriate location beside the timing diagram and boundary conditions are checked. If the specified start time is less than the first time in the event-times array, then the first state (initial state) of the line is drawn out to this first time, or to the specified start time, whichever is less. If both start-time and end-time are less than the first event-time, only the first state will be displayed across the timing diagram.

Once the first event-time is reached, the routine takes the first two event times in the event-time array and uses these for start- and end-point times in the state segment drawing routine. A pointer is incremented, and the second and third event times are used. This process is repeated until the endpoint event-time exceeds the specified endpoint time for the timing diagram as a whole. The last state segment is drawn from the start-time obtained from the event-time array to the endpoint time for the overall timing diagram. Should the last event-

## DRAW TIMING LINE

INPUT		STEP	PROCESS	NEXT STEP (Y/N)
L#	LINE NUMBER	1	CHECK FOR VALID LINE NUMBER.	2/12
L\$( )	LINE NAME ARRAY	2	PRINT LINE NAME IN LINE NAME COLUMN	3
T4	START TIME	3	FETCH LINE-STATE STRING.	4
T5	END TIME	4	IS START TIME LESS THAN FIRST STATE-TIME?	5/6
		5	DRAW FIRST STATE FROM START TIME TO FIRST STATE-TIME.	6
		6	FETCH STATE AND NEXT STATE-TIME.	7
		7	IS NEXT STATE-TIME GREATER THAN END TIME?	8/9
		8	DRAW STATE OUT TO END TIME.	12
		9	DRAW STATE.	10
		10	LAST STATE?	11/6
		11	DRAW STATE OUT TO END TIME.	12
		12	EXIT PROCESS.	RET

Figure 17

time be less than the timing diagram endpoint time, the last state of the specified line is drawn out to the endpoint time for the overall diagram.

#### FETCH LINE STATE STRING (Figure 18)

This routine uses an index passed by the timing line routine, plus information obtained from the header record, to obtain the record or records containing the state values for a particular line. The state values are returned in the form of a string.

Since only the line signal values for a tagged line appear in the simulator's output file, the  $i^{\text{th}}$  subgroup in the input data base does not necessarily correspond to the  $i^{\text{th}}$  line of the network. When the timing line routine checks for a match between the line number to be displayed and the line number array, it keeps track of its position in the array. If for some line number  $\ell$  and its index in the line number array,  $k$ , the line state subgroup for this line is the  $k^{\text{th}}$  subgroup in the line state records. This subgroup of records is fetched, concatenated, and excess characters eliminated. This string is then returned to the calling routine.

#### DRAW STATE SEGMENT

This routine draws a single signal state value on the screen, given the start coordinates, length, and height of the segment. Each state signal is given in alphabetic representation, as shown in Figure 19.

The routine first checks to see if a valid code has been passed, then branches to the appropriate routine. Any routine with a line segment at the zero level will draw that line segment with triple

FETCH LINE-STATE STRING

INPUT	OUTPUT
L% LINE NUMBER INDEX C1% NUMBER OF EVENT-TIMES RECORDS C2% NUMBER OF LINE-STATE RECORDS/LINE C3% NUMBER OF LINE-NUMBER RECORDS N2% NUMBER OF EVENTS	GS LINE-STATE STRING

STEP	PROCESS	NEXT STEP (Y/N)
1	DETERMINE WHICH RECORD(S) TO ACCESS.	2
2	FETCH C2% RECORDS AND CONCATENATE.	3
3	THROW AWAY EXCESS CHARACTERS.	RET

Figure 18

## DRAW STATE SEGMENT

INPUT		STEP	PROCESS	NEXT STEP (Y/N)
S\$	STATE CODE	1	CHECK FOR VALID STATE.	2/4
S1%	X-START POSITION	2	BRANCH TO APPROPRIATE SEGMENT ROUTINE.	3
S2%	Y-START POSITION	3	DRAW STATE SEGMENT.	4
S3%	LENGTH OF SEGMENT	4	EXIT PROCESS.	RET
S4%	HEIGHT OF SEGMENT			

COMMENTS	
<u>STATE CODE ASSIGNMENT</u>	
STATE "A"	LOGIC ZERO
STATE "B"	LOGIC ONE
STATE "C"	STUCK AT LOGIC ZERO
STATE "D"	STUCK AT LOGIC ONE
STATE "E"	INDETERMINATE STATE (UNKNOWN)
STATE "F"	LOW TO HIGH TRANSITION
STATE "G"	HIGH TO LOW TRANSITION
STATE "H"	ERROR

Figure 19

thickness, in order to easily distinguish between the zero and one levels for a particular timing line. Routines for additional line state values are easily added.

#### FUNCTIONS

Graphics and control functions are an important part of TIMOUT's software (see TABLE 1). Graphics functions are provided to make the software terminal-independent, as well as to ease the programmer's task. Functions provided allow the programmers to draw straight or dashed lines, vector to a given location, and alter the mode of the terminal itself.

Control functions provided perform often used mini-tasks. Among these are *obtaining the character typed by the user at the keyboard without echoing the character to the screen*, and checking the options menu at the bottom of the timing diagram display.

#### CONCLUSION

The functions of a general purpose logic simulator have been outlined in this paper. The simulator package has been designed for ease of use. The network entry program format is easily learned, and produces a very readable description of the user's network.

The library functions provided reduce the amount of repetitive work required by the user. The library allows the user to design and test a large network in terms of subsections and common modules. This approach lends itself well to group organization, where each group member is assigned a particular subsection to design and debug.

The output format of simulation results, in the form of a timing diagram, simplifies interpretation of results by presenting them in a readily understood format. The ability to specify which lines are to be displayed and the order in which they are presented, as well as the time frame in which these lines are viewed, allow detailed examination of events occurring within the network.

TABLE 1

TIMOUT FUNCTION LISTINGFunction

FNP\$(X%,Y%)	This function formats X-Y coordinate data for the Tektronix terminal.
FNQ\$(X%)	This function establishes the mode in which the user terminal operates. X%=0% Erases screen; goes into alpha mode X%=1% Puts terminal in alpha mode X%=2% Puts terminal in graphics mode X%=3% Displays user positionable crosshairs
FNO\$(X%,Y%)	Draws a solid line from the previous X-Y location to the new location specified. First vector following a mode command is not displayed.
FNS\$	Draws a solid vector from (Q1%,Q2%) to (Q3%,Q4%). These global coordinate variables are set before the function is called.
FND\$	This function draws a dashed vector from points (Q1%,Q2%) to (Q3%,Q4%).
FNW\$(X%,Y%)	This function outputs the character "X" at the specified X-Y coordinates.
FNK\$	This function disables the echo on the user terminal and returns the character typed by the user.
FNR\$	This function acquires the coordinate of the crosshairs and returns the character typed by the user. Crosshair coordinates are in X% and Y%.
FNT\$	This function allows the user to position the vertical crosshair at a point of interest on the timing diagram and prints the time at that point above the diagram. If the crosshair is positioned beyond the boundary of the diagram, the character "l" is returned.
FNM%	This function checks the mini options menu at the bottom of the display page and returns the index of the option selected. The cursor block is moved if the user types space or backspace.

## APPENDIX A - TIME-OUT USER'S GUIDE

This section gives a brief explanation of the functions of the graphic output package and the manner in which the user interfaces with it.

When first invoked, TIMEOUT presents the user with an options menu. The user must then select one option from each of the four option groups. Selection of options makes use of a movable cursor block. To move the cursor, the user types the space bar on the keyboard to move down or the backspace key to move up. To select an option, the "X" key is pressed and an "X" appears in the option block chosen. The cursor block is moved down one box by the program. If the cursor is moved up (down) beyond the first (last) option block, the cursor wraps around to the last (first) option block.

The two-bit decoder of figure 4 will be used to illustrate the use of the graphic package. The display file will be assumed to be associated with the current simulation run, hence the "OPTIONAL INPUT FILE" option will not be needed. To view the overall results, the options "DISPLAY ALL LINES," "ENTIRE SIMULATION" and "REGULAR GRID" are chosen as shown in figure A-1(a). "CONTINUE" is poked and control continues to the next option page. Since none of the options require additional data, "CONTINUE" is selected again, and the timing diagram display page is presented. Figure A-1(c) illustrates the timing diagram produced.

If the user now wishes to view an expanded portion of the diagram from time 8.0 to 12.0, the user must return to the original option page. The "MODIFY ANY OPTION" option is selected from the mini options menu at the bottom of the display page.

From the display options page, the options "DISPLAY ALL LINES," "MIN & MAX TIMES" and "REGULAR GRID" are chosen. When "CONTINUE" is poked and the next option page is displayed, the program prompts the user for additional information. Once entered, the user "CONTINUE"s to the timing diagram display. The expanded display is shown in figure A-2(c). To obtain the time at a particular transition of interest, the user selects the option "TIME." A vertical crosshair is displayed. By positioning the crosshair at a point and typing "X", the time at that point is printed above the diagram. To exit this mode, the user must position the crosshair beyond the boundaries of the timing diagram and type "X".

The user may continue this option selection-display viewing cycle, examining particular lines or combinations of lines. When finished, "EXIT PROGRAM" is selected and control is returned to the coordinating program CONTRL.

DISPLAY OPTIONS

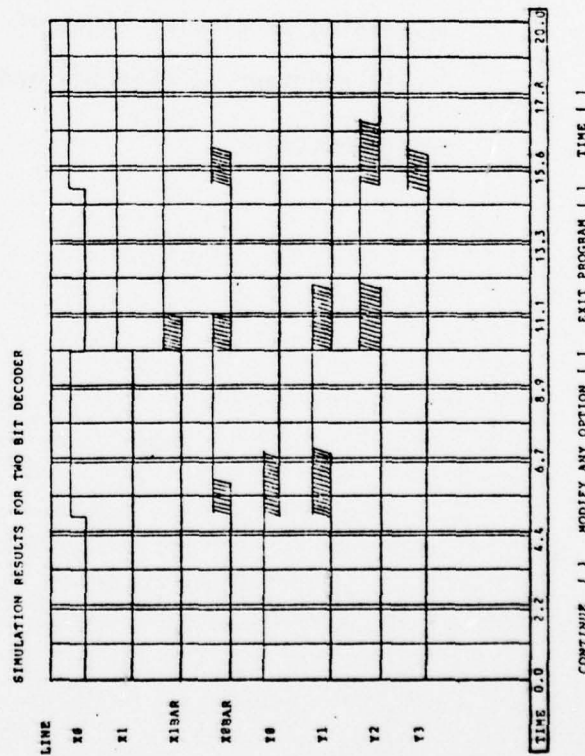
OPTIONAL INPUT FILE C J  
 DISPLAY ALL LINES [X] J  
 I/O LINES C J  
 USER SELECTED C J  
 TIME WINDOW:  
 ENTIRE SIMULATION [X] J  
 MIN & MAX TIMES C J  
 MIN TIME & INCREMENT C J  
 TIMING CPID  
 REGULAR CPID [X] J  
 NO GRID C J

CONTINUE [X] J  
 SPECIFY NEW OPTIONS [X] J  
 EXIT PROGRAM C J

(a)

CONTINUE [X] J  
 MODIFY ANY OPTION [X] J

(b)



(c)

Figure A-1

DISPLAY OPTIONS

OPTIONAL INPUT FILE C 3  
 DISPLAY ALL LINES C 3  
 I/O LINES C 3  
 USER SELECTED C 3  
 TIME WINDOW.  
 ENTIRE SIMULATION C 3  
 MIN & MAX TIMES C 3  
 MIN TIME & INCREMENT C 3  
 TIMING GRID.  
 REGULAR GRID C 3  
 NO GRID C 3

CONTINUE C 3  
 SPECIFY NEW OPTIONS C 3  
 EXIT PROGRAM C 3

(a)

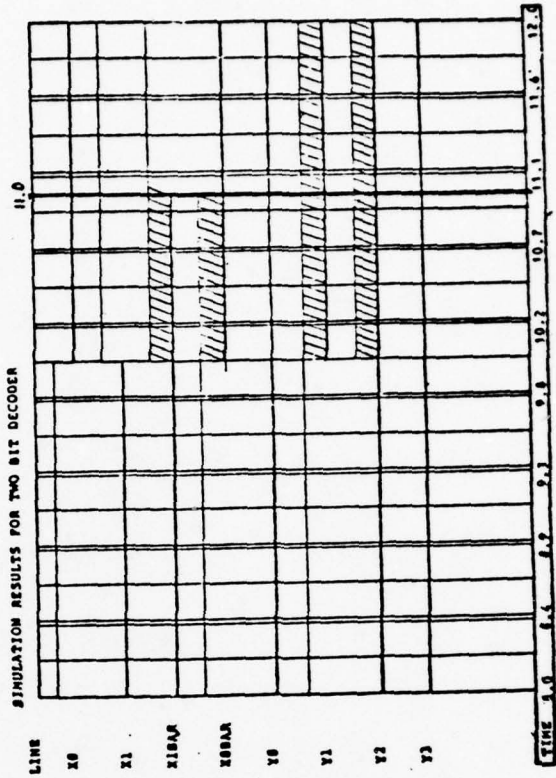
FILE-NAME IN USE IS CRT18.TMP

SPECIFY DISPLAY TIMES

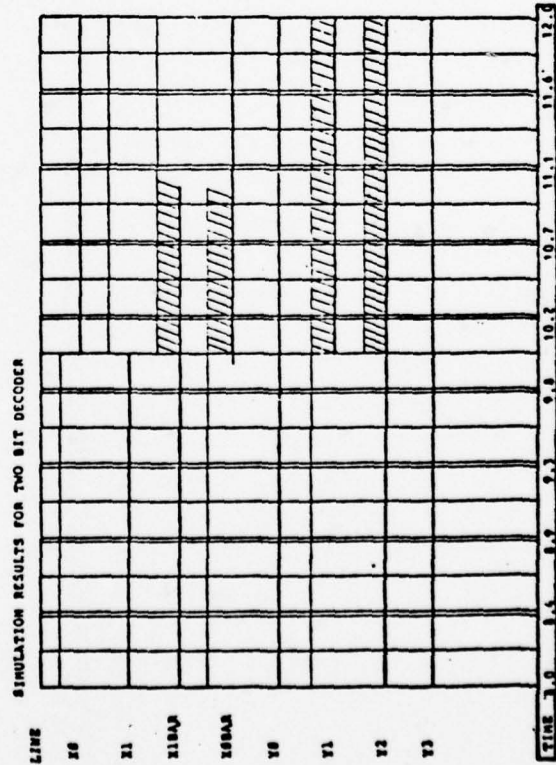
MIN VALUE = 8.0  
 MAX VALUE = 12.0

CONTINUE C 3  
 MODIFY ANY OPTION C 3

(b)



(d)



(c)

Figure A-2

APPENDIX B  
PROGRAM LISTINGS



```

1!      FILE PREPROCESSOR PROGRAM

2!      FILE :          PROCES.BAS
3!      ACCOUNT :       [10,13]
4!      VERSION 1       JULY 8, 1977
100!

!          PROGRAM DESCRIPTION

105!     THIS PROGRAM ACCEPTS AS INPUT THE ASCII FILE PRODUCED
106!     BY THE SIMULATOR PROGRAM, SIMPRG.BAS. THIS FILE IS
        THEN ALTERED TO CONFORM TO THE INPUT REQUIREMENTS OF
        THE GRAPHICS DISPLAY PROGRAM, TIMEOUT, AND PLACED IN
        ANOTHER, TEMPORARY FILE.
300!

!          I/O CHANNELS

301!     CHANNEL          USED FOR:

310!     1          INPUT FROM SIMULATOR FILE
320!     2          OUTPUT FOR TIMEOUT
400!

!          VARIABLE DEFINITIONS

401!     VARIABLE          DEFINITION

405!     L1%          # OF NETWORK LINES
406!     L2%          # OF I/O LINES
407!     H1$          TIME SCALE VALUE
408!     H$           HEADER STRING
800!

!          FUCTIONS AND SUBROUTINES

801!     !PROGRAMMER DEFINED SUBROUTINES

802!     LINE          DESCRIPTION

830!     PROGRAMMER DEFINED FUNCTIONS

831!     LINE          DESCRIPTION
840!     10100        FNS$- CONVERTS LINE STATE NUMBER REPRESETATION
        TO LETTER REPRESENTATION
900!

!          DIMENSION STATEMENTS

910     DIM S%(400%)  !LINE STATES FROM SIMULATOR (MAX 400)
920     DIM S$(400%)  !LINE STATE CHARACTER STRING FOR OUTPUT

```

```

930   DIM M$(2000)      !I/O LINE NUMBER VECTOR
940   DIM N$(4000)      !NETWORK LINE NUMBER VECTOR
950   DIM T(400)        !EVENT TIMES VECTOR
999!

!           START OF PROGRAM

1000  ON ERROR GOTO 19000
1010  L$="ABCDEFGHGH"
      !SET UP LINE # TO CHARACTER CONVERSION STRING
1020  OPEN "DUMP.TMP" FOR INPUT AS FILE #1%
      !OPEN SIMULATOR OUTPUT FILE
1030  T$=CVT$$ (NUM$ (CVT$(CHR$(0%)+LEFT(SYS(CHR$(6%)+
      CHR$(9%)+CHR$(0%)),1%))),2%)
      !UNIQUE TERMINAL ID NUMBER
1040  OPEN "CRT"+T$+".TMP" FOR OUTPUT AS FILE 2%
      !OPEN OUTPUT FILE TO CRT PROGRAM
1050  INPUT #1%,L1%,L2%,H1$
1060  MAT INPUT #1%,N%(L1%)
1065  MAT INPUT #1%,M%(L2%)
1070  INPUT #1%,H$
1080!

      INPUT EVENT TIME/LINE STATE GROUPS

2000  I%=1%
2010  INPUT #1%,T1
2020  T(I%)=T1
2030  IF T1<0 THEN 3000
2040  MAT INPUT #1%,S%(L1%)
2050!  CONVERT AND STORE LINE STATE INPUTS
2060  FOR J%=1% TO L1%
2070  S$(J%)=S$(J%)+FNS$(S%(J%))
2080  NEXT J%
2090  I%=I%+1%: GO TO 2010
3000!  OUTPUT HEADER RECORD
3010  FIELD #2%,2% AS A1$,2% AS A2$,4% AS A3$,4% AS A4$,
      400% AS A5$, 100% AS A6$
3020  LSET A1$=CVT$(L1%)           !NUMBER OF NETWORK LINES
3030  LSET A2$=CVT$(I%-1%)        !NUMBER OF EVENTS
3040  LSET A3$=LEFT(H1$,4%)       !TIME SCALE VALUE
3050  LSET A4$=CVTF$(T(I%-1%))   !MAX SIM TIME VALUE
3060  A$=""                       !CONVERT AND STORE
3070  A$=A$+CVT$(M%(K%)) FOR K%=1% TO L2%   !I/O LINE NUMBERS
3072  A$=A$+CVT$(0%)
3075  LSET A5$=A$
3080  LSET A6$=H$
3090  PUT #2%,RECORD 1%
4000!  OUTPUT LINE NUMBER RECORD(S)
4010  FIELD #2%,512% AS A1$
4020  B$=""
4030  B$=B$+CVT$(N%(K%)) FOR K%=1% TO L1%
4100  L%=0%: K%=L1%
4110  IF K%<=256% THEN 4150
4120  LSET A1$=MID(B$,L%*512%+1%,512%)
4130  PUT #2%: K%=K%-256%: L%=L%+1%
4140  IF K%>256% THEN 4120

```

```

4150 LSET A1$=MID(B$,L%*512%+1%,K%*2%)
4160 PUT #2%
4200! OUTPUT EVENT TIMES RECORD(S)
4210 K%=I%-1%: L%=0%
4220 FIELD #2%,512% AS A1$
4230 IF K%<=128% THEN 4290
4240 B$=""
4250 B$=B$+CVTF$(T(J%)) FOR J%=L%*128%+1% TO L%*128%+128%
4260 LSET A1$=B$: PUT #2%
4270 L%=L%+1%: K%=K%-128%
4280 IF K%>128% THEN 4240
4290 B$=""
4300 B$=B$+CVTF$(T(J%)) FOR J%=L%*128%+1% TO I%-1%
4310 LSET A1$=B$: PUT #2%
5000! OUTPUT LINE STATE RECORDS
5010 FIELD #2%,512% AS A1$
5020 FOR I%=1% TO L1%
5030 K%=LEN(S$(I%)): L%=0%: J%=K%
5040 IF K%<=512% THEN 5080
5050 LSET A1$=MID(S$(I%),L%*512%+1%,512%)
5060 PUT #2%: K%=K%-512%: L%=L%+1%
5070 IF K%>512% THEN 5050
5080 LSET A1$=MID(S$(I%),L%*512%+1%,J%)
5090 PUT #2%
5100 NEXT I%
5200 CLOSE 1%,2%
5210 CHAIN "TIMEOUT"
5220 GO TO 32767
10000!

```

```

! PROGRAMMER DEFINED FUNCTIONS
! AND SUBROUTINES

```

```

10100 DEF FNSS(X%)
10110 X$=""
10120 IF X%<0% OR X%>10% THEN X$="H": GO TO 10140
10130 X$=MID(L$,X%+1%,1%)
10140 FNSS=X$
10150 FNEND
19000!

```

```

! ERROR TRAP HANDLING ROUTINE

```

```

19100 PRINT ERR,ERL
!PRINT ERROR # AND LINE #
32767 END

```

1!       ! LOGIC SIMULATION DISPLAY PROGRAM

2!               FILE :            TIMOUT.BAS  
3!               ACCOUNT :         [10,13]

4!               VERSION 2         DECEMBER 7, 1976

5!               REVISION 1        DECEMBER 8, 1977

100!

!           PROGRAM DESCRIPTION

105!       ! THIS PROGRAM IS EITHER INVOKED BY THE USER  
! DIRECTLY OR BY CHAINING INTO THE PROGRAM FROM  
! THE SIMULATION PROGRAM.

300!

!           I/O CHANNELS

301!       CHANNEL 1            USER TERMINAL OUTPUT  
302!       CHANNEL 2            USER TERMINAL GRAPHICS OUTPUT  
303!       CHANNEL 3            RANDOM ACCESS INPUT DATA FILE  
800!

!           SUBROUTINES AND FUNCTIONS

801!       LINE       DESCRIPTION  
810!       11000     DISPLAY MENU AND RETRIEVE COMMANDS  
811!       13000     INPUT SIMULATION INFORMATION  
              AND EVENT-TIMES RECORDS  
812!       14000     INPUT LINE-STATE RECORDS  
813!       16000     DRAW STATE SEGMENTS  
814!       17000     RETRIEVE LINE NUMBERS FROM USER  
900!

!           DIMENSION AND DATA STATEMENTS

901       DIM O%(4%)  
          ! MENU OPTIONS ARRAY  
902       DIM R%(13%)  
          ! MENU OPTIONS ROW COORDINATES  
903       DIM C%(6%)  
          ! MENU OPTIONS COLUMN COORDINATES  
904       DIM E(1024)  
          ! EVENT-TIMES ARRAY

```

905   DIM L2%(200)
      ! USER SELECTED LINE NUMBERS
906   DIM L1%(200)
      ! I/O LINE NUMBERS (SIMULATOR SUPPLIED)
907   DIM B$(128)
      ! CHARACTER STRING ARRAY FOR EVENT-TIMES
      ! PROCESSING
910   ! Y COORDINATE DATA FOR MENU FOLLOWS:
915   DATA 636,592,570,548,460,438,416,328,306
920   DATA 152,130,108
925   ! X COORDINATE DATA FOR MENU FOLLOWS:
930   DATA 420,968,241,564,818,957
940   F0%=0%: F1%=0%: F5%=0%
950   P1=0
1000!

      !          PROGRAM START

1002  ON ERROR GOTO 19000
      ! SET ERROR TRAP
1005  READ R%(I%) FOR I%=1% TO 12%
      ! STORE ROW COORDINATES FOR MENU
1010  READ C%(I%) FOR I%=1% TO 6%
      ! STORE COLUMN COORDINATES FOR MENU
1015  T$=CVT$$ (NUM$ (CVT$(CHR$(0%)+
                LEFT(SYS(CHR$(6%)+CHR$(9%)+
                CHR$(0%)),1))),2%)
      ! STRING REPRESENTING TERMINAL NUMBER OF USER
1020  F1%=0%
1025  OPEN "KB:" FOR OUTPUT AS FILE #1%
      ! OPEN BUFFER FOR OUTPUT TO USER TERMINAL
1030  FIELD #1%, 16% AS V$
      ! SET FORMAT OF BUFFER #1
1035!

      ! DISPLAY MENU AND RETRIEVE OPTIONS

1040  GOSUB 11000
      ! MENU AND OPTIONS SUBROUTINE
1060  GO SUB 17500          !DRAW TIMING DISPLAY PAGE
1070  M%=0%: C5%=1%: C7%=1%: MAT C6%=ZER
1080  IF O%(2%)=0%
      THEN C6%(C5%-(C7%-1%)*N%)=CVT$(MID(L$,2*C5%-1%,2%))
      : GO TO 1110
1090  IF O%(2%)=1%
      THEN C6%(C5%-(C7%-1%)*N%)=L1%(C5%)
      : GO TO 1110
1100  C6%(C5%-(C7%-1%)*N%)=L2%(C5%)
1110  IF C6%(C5%-(C7%-1%)*N%)=0% THEN 1140
1120  C5%=C5%+1%
1130  IF NOT(C5%>C7%*N%) THEN 1080
      ELSE 1170
1140  C5%=C5%+1%
1150  IF C5%>C7%*N% THEN 1170
1160  C6%(C5%-(C7%-1%)*N%)=0%: GO TO 1140
1170  L%=C6%(M%+1%)

```

```

1180 IF L%=0% THEN 1230
1190 GO SUB 18000 !DRAW TIMING DIAG. FOR LINE L%
1200 M%=M%+1%
1210 IF NOT(M%=N%) THEN 1170 ! N% LINES DISPLAYED?
1220 C7%=C7%+1%: M%=0%
1230 O1%=FNM% !CHECK MINI OPTIONS MENU
1240 IF O1%=1% THEN 1040 !MODIFY ANY OPTION
1250 IF O1%=2% THEN 9000 !EXIT PROGRAM
1260 IF O1%=0% THEN
      IF L%=0% THEN 1230
      ELSE 1290 !CONTINUE
1270 A$="": A$=FNT$ !TIME OPTION
1280 IF NOT (A$="1") THEN 1270
      ELSE 1230
1290 GO SUB 17500: MAT C6%=ZER: GO TO 1080
9000!

! EXIT ROUTINE

9005 A$=FNQ$(0%)
      \SLEEP 1
      ! RESET TERMINAL TO ALPHA MODE
9010 CLOSE 1%
      ! CLOSE USER TERMINAL OUTPUT CHANNEL
9011 CLOSE 2%,3%,4%
9013 CHAIN "CONTRL"
9015 GOTO 32767
      ! END OF PROGRAM
10000!

! FUNCTION BLOCK

10005!

! FUNCTION FNP$

10010!
! THIS FUNCTION IS USED INTERNALLY TO FORMAT
! X-Y COORDINATE INFORMATION

10015 DEF FNP$(X%,Y%)=CHR$(32%+(Y%/32% AND 31%))+CHR$(96%+(Y% AND 31%))
      +CHR$(32%+(X%/32% AND 31%))+CHR$(64%+(X% AND 31%))
10020!

! FUNCTION FNO$

10025!
! THIS FUNCTION IS USED TO DRAW VECTORS AS IN
! A$=FNO$(X,Y). THE FIRST VECTOR FOLLOWING A MODE
! COMMAND ( FNQ$ ), IS NOT DISPLAYED.

10030 DEF FNO$(X%,Y%) : LSET V$=FNP$(X%,Y%) : PUT #1%,RECORD 1%,COUNT4

```

10035 FNEND  
10040!

! FUNCTION FNQ\$

10045!

! THE FUNCTION FNQ\$ IS USED TO ESTABLISH THE MODE OF THE  
! TERMINAL.

10050!

! FNQ\$(0%) ERASES THE SCREEN, GOES INTO ALPHA MODE  
! FNQ\$(1%) PUTS THE TERMINAL IN ALPHA MODE  
! FNQ\$(2%) PUTS THE TERMINAL IN GRAPHICS MODE  
! FNQ\$(3%) DISPLAYS THE CROSSHAIRS

10055 DEF FNQ\$(X%):IF X%=0% THEN LSETV\$=CHR\$(27)+CHR\$(12)  
10060 IF X%=1% THEN LSETV\$=CHR\$(27)+CHR\$(31)  
10065 IF X%=2% THEN LSETV\$=CHR\$(27)+CHR\$(29)  
10070 IF X%=3% THEN LSETV\$=CHR\$(27)+CHR\$(26)  
10075 PUT #1%,RECORD1%,COUNT2%  
10080 IF X%=0% THEN SLEEP 2  
10085 FNEND  
10090!

! FUNCTION FNR\$

10095!

! FNR\$ IS USED TO ACQUIRE THE COORDINATES OF THE CROSSHAIRS  
! FNR\$ HAS NO ARGUMENT. THE RESULT IS THE CHARACTER  
! TYPED BY THE USER. THE TERMINAL RETURNS TO ALPHA MODE.  
! THE COORDINATES OF THE CROSSHAIRS ARE IN X%,Y%

10100 DEF FNR\$  
10105 OPEN "KB:" FOR INPUT AS FILE 2%  
10110 W\$=SYS(CHR\$(3%)+CHR\$(2%))+FNQ\$(3)  
10115 FIELD #2%,10% AS U\$  
10120 X\$=""\X%=0  
10125 W\$=SYS(CHR\$(4%)+CHR\$(2%))\GET #2%,RECORD 1%  
10130 X\$=X\$+LEFT(U\$,RECOUNT)  
10135 X%=X%+RECOUNT  
10140 IF X%<5% THEN 10125  
10145 W\$=SYS(CHR\$(2%)+CHR\$(2%))\CLOSE 2%  
10150 CHANGE X\$ TO W\$  
10155 X%=32%\*((W\$(2%) AND 31%)-32%)+(W\$(3%) AND 31%)+1023%  
10160 Y%=32%\*((W\$(4%) AND 31%)-32%)+(W\$(5%) AND 31%)+1023%  
10165 FNR\$=LEFT(X\$,1%)  
10170 FNEND  
10175!

! FUNCTION FNW\$

10180!

! THIS FUNCTION OUTPUTS AN X AT THE GIVEN X-Y COORDINATES

```

10185 DEF FNWS(X%,Y%)
10190 AS=FNQS(2%)+FNO$(X%,Y%)
10195 AS=FNQS(1%)
10200 PRINT "X"
10205 FNEND
10210!

```

```

! FUNCTION FNS$

```

```

10215!
! THIS FUNCTION IS USED TO DRAW A SOLID LINE

```

```

10220 DEF FNS$
10225 AS=FNQS(2%)+FNO$(Q1%,Q2%)
! DRAW A DARK VECTOR TO START OF LINE
10230 AS=FNO$(Q3%,Q4%)
! DRAW A VISIBLE LINE
10235 FNEND
! EXIT
10240!

```

```

! FUNCTION FND$

```

```

10245!
! THIS FUNCTION IS USED TO DRAW A DASHED LINE

```

```

10250 DEF FND$
10255 AS=FNQS(2%)+FNO$(Q1%,Q2%)
! DRAW A DARK VECTOR TO THE START OF LINE
10260 Z2%=Q1%
! INITIALIZE THE POSITION POINTER Z2%
10265 Z1%=Q3%-Z2%
! CALCULATE THE DISTANCE LEFT IN THE LINE
10270 IF Z1%<8% THEN 10300
! SPACE TOO SMALL?
10275 Z2%=Z2%+4%
! SET NEW X POSITION
10280 AS=FNQS(2%)+FNO$(Z2%,Q4%)
! DRAW A DARK DASH
10285 Z2%=Z2%+4%
! SET NEW X POSITION
10290 AS=FNO$(Z2%,Q4%)
! DRAW A VISIBLE DASH
10295 GOTO 10265
! LOOP BACK AGAIN
10300 IF Z1%<=4% THEN AS=FNQS(2%)+FNO$(Q3%,Q4%)
: GOTO 10320
! IF TOO SMALL, END LINE WITH DARK DASH
10305 Z2%=Z2%+4%
! SET NEW X POSITION
10310 AS=FNQS(2%)+FNO$(Z2%,Q4%)
! DRAW A DARK DASH
10315 AS=FNO$(Q3%,Q4%)
! DRAW VISIBLE DASH
10320 FNEND

```

```

! EXIT
10330!
!
!           FUNCTION FNC$
10335! THIS FUNCTION DRAWS A ZERO-DELAY RISE TIME LINE BETWEEN
! STATES A AND B
!
10340 DEF FNC$(X%,Y%)
10345 IF NOT((Y%=1% AND X%=2%) OR (Y%=2% AND X%=1%)) THEN 10360
10350 Q1%=S1%: Q2%=S2%: Q3%=S1%: Q4%=S2%+S4%
10355 A$=FNS$
10360 FNEND
10370!
!
!           FUNCTION FNT$
!
!
10375! THIS FUNCTION ALLOWS THE USER TO POSITION THE Y CROSSHAIR
! AT ANY POINT OF INTEREST ON THE TIMING DIAGRAM AND GET THE
! TIME.
!
10380 DEF FNT$
10390 A$=FNQ$(2%)+FNQ$(3%)+FNR$+FNQ$(1%)           !GET CROSSHAIR LOCATION
10400 IF X%<P1% OR X%>P2% THEN 10435
10410 X=X%-P1%
10420 A$=FNQ$(2%)+FNO$(X%,755%)+FNQ$(1%)
10430 PRINT USING "###.#",X/T6+P1
10431 GO TO 10440
10435 FNT$="1"
10440 FNEND
10450
!
!           FUNCTION FNM%
!
!
10455 ! THIS FUNCTION CHECKS THE OPTIONS MENU AT
! THE BOTTOM OF THE DISPLAY PAGE
10460 DEF FNM%
10465 I%=3%
10470 A$=FNQ$(2%)+FNO$(C%(I%),10%)+FNQ$(1%)
10475 A$="": A$=FNK$
10480 IF A$<>" " THEN 10500
10485 I%=I%+1%
10490 IF I%=7% THEN I%=3%
10495 GO TO 10470
10500 IF A$<>CHR$(8%) THEN 10520
10505 I%=I%-1%
10510 IF I%=2% THEN I%=6%
10515 GO TO 10470
10520 IF A$<>"X" THEN 10475
10525 FNM%=I%-3%
10530 FNEND
10580!
!
!           FUNCTION FNK$
!
!
10585! THIS FUNCTION DISABLES THE ECHO ON THE USER'S TERMINAL AND
! RETURNS THE CHARACTER TYPED BY THE USER
!

```

```

10590 DEF FNK$
10595 OPEN "KB:" FOR INPUT AS FILE 2%
10600 W$=SYS(CHR$(3%)+CHR$(2%)): FIELD #2%,10% AS U$
10605 X$="": X%=0%
10610 W$=SYS(CHR$(4%)+CHR$(2%)): GET #2%,RECORD 1%
10615 X$=X$+LEFT(U$,RECOUNT)
10620 X%=X%+RECOUNT
10625 IF X%<1% THEN 10610
10630 W$=SYS(CHR$(2%)+CHR$(2%)): CLOSE 2%
10635 FNK$=X$
10640 FNEND
!1000!

```

```

! SUBROUTINE TO DISPLAY MENU AND TO RETRIEVE
! USER INSTRUCTIONS FOR DISPLAY FORMATTING.

```

```

11005 LSET V$=CHR$(155%)+CHR$(56%)
! SET 4014 BIG CHAR. MODE
11010 PUT #1%, RECORD 1%, COUNT 2%
11015 A$=FNQ$(0%)+FNQ$(1%) !ERASE SCREEN, ALPHA MODE
11020 SLEEP 1
11025 IF F1%=0% THEN O%(I%)=0% FOR I%=1% TO 4%
11030 PRINT: PRINT TAB(28);"DISPLAY OPTIONS"
11035 PRINT: PRINT: PRINT: PRINT
11040 PRINT " OPTIONAL INPUT FILE ";TAB(30);"[ ]";TAB(40);
11045 IF F1%=1% THEN PRINT "TO ""CHANGE"" OLD OPTIONS"
ELSE PRINT "TO ""SELECT"" NEW OPTIONS"

11050 PRINT
11055 PRINT " DISPLAY:";TAB(12);"ALL LINES";TAB(30);"[ ]";
11060 PRINT TAB(40);"POSITION CROSSHAIRS, TYPE X"
11065 PRINT TAB(12);"I/O LINES";TAB(30);"[ ]"
11070 PRINT TAB(12);"USER SELECTED";TAB(30);"[ ]"
11075 PRINT
11080 PRINT " TIME WINDOW:"
11085 PRINT
11090 PRINT TAB(4);"ENTIRE SIMULATION";TAB(30);"[ ]"
11095 PRINT TAB(4);"MIN & MAX TIMES";TAB(30);"[ ]"
11100 PRINT TAB(4);"MIN TIME & INCREMENT";TAB(30);"[ ]"
11105 PRINT
11110 PRINT " TIMING GRID:"
11115 PRINT
11120 PRINT TAB(4);"REGULAR GRID";TAB(30);"[ ]"
11125 PRINT TAB(4);"NO GRID";TAB(30);"[ ]"
11130 PRINT
11135 PRINT
11140 PRINT
11145 PRINT
11150 PRINT
11155 PRINT
11160 PRINT TAB(48);"CONTINUE ";TAB(69);"[ ]"
11165 PRINT TAB(48);"SPECIFY NEW OPTIONS";TAB(69);"[ ]"
11170 PRINT TAB(48);"EXIT PROGRAM";TAB(69);"[ ]"
11174 X1%=1%: Y1%=1%
11175 A$=FNQ$(2%)+FNO$(C%(X1%)+15%,R%(Y1%))+FNQ$(1%)
11180 A$="": A$=FNK$
11185 IF A$<>" " THEN 11205

```

B12

```
11190 Y1%=Y1%+1%: IF Y1%=13% THEN Y1%=1%
11195 IF Y1%>9% THEN X1%=2%
      ELSE X1%=1%
11200 GO TO 11175
11205 IF A$<>CHR$(8%) THEN 11225
11210 Y1%=Y1%-1%: IF Y1%=0% THEN Y1%=12%
11215 IF Y1%<10% THEN X1%=1%
      ELSE X1%=2%
11220 GO TO 11175
11225 IF A$<>"X" THEN 11180
11230 IF Y1%=1% THEN O%(1%)=1%: GO TO 11250
11235 IF (Y1%>9%)AND(Y1%<13%) THEN 11255
11240 IF (Y1%>1%)AND(Y1%<5%) THEN O%(2%)=Y1%-2%
11245 IF (Y1%>4%)AND(Y1%<8%) THEN O%(3%)=Y1%-5%
      ELSE O%(4%)=Y1%-8%
11250 A$=FNW$(C%(X1%)+15%,R%(Y1%)): GO TO 11190
11255 IF Y1%=10% THEN 11280
      ELSE IF Y1%=11% THEN F1%=0%: GO TO 11000
11260 GO TO 9000
11280!
      ! SECOND OPTION REQUEST PAGE
11285 A$=FNQ$(0%)+FNQ$(1%)      !ERASE SCREEN, ALPHA MODE
11290 SLEEP 1
11295 OPEN "KB:" FOR INPUT AS FILE 2%
11300 PRINT: PRINT: PRINT
11305 IF F1%=1% THEN PRINT "FILE-NAME IN USE IS ";F$
      :PRINT
      :GOTO 11340
11310 IF F2%=1% THEN CLOSE 3%
11315 IF O%(1%)=0%
      THEN F$="CRT"+T$+".TMP"
      : PRINT "DEFAULT FILENAME USED IS ";F$
      : GO TO 11330
11320 PRINT "INPUT FILE-NAME = ";
11325 INPUT #2%, F$
11330 OPEN F$ FOR INPUT AS FILE #3%
11333 GOSUB 13000
11335 PRINT
11340 IF O%(2%)<>2% THEN 11395
11345 IF (F1%<>1% OR L2%(1%)=0%) THEN
      PRINT "DISPLAY WHAT LINES ? "
      \GOTO 11365
11350 PRINT "SPECIFY NEW LINES ? ";
11355 INPUT #2%, A$
11360 IF LEFT(A$,1%)<>"Y" THEN 11390 ELSE PRINT
11365 L2%(1%)=0% FOR I%=1% TO N5%
      \N5%=0%
11370 PRINT "ENTER LINE NUMBERS SEPARATED BY COMMAS OR SPACES"
11375 PRINT "WHEN THROUGH, TYPE <CR> AFTER PROMPT."
11380 PRINT
11385 GOSUB 17000
11390 PRINT
11395 IF O%(3%)=0% THEN 11460
11400 PRINT "SPECIFY DISPLAY TIMES": PRINT
11405 PRINT " MIN VALUE = ";
11410 INPUT #2%,P1
```

```

11415 IF P1>=N4 THEN PRINT "ERROR - MAX SIM TIME= ";N4: GO TO 11405
11420 IF O%(3%)=2% THEN 11445
11425 PRINT " MAX VALUE = ";
11430 INPUT #2%,P2
11435 IF P2<P1 THEN PRINT "ERROR - MAX < MIN VALUE GIVEN":GOTO 11425
11440 GOTO 11455
11445 PRINT " TIME INCREMENT = ";
11450 INPUT #2%,P3
11455 PRINT
11460 A$=FNQ$(2%)+FNO$(0%,174%)+FNQ$(1%)
11465 PRINT
11470 PRINT TAB(48);"CONTINUE";TAB(69);"[ ]"
11475 PRINT TAB(48);"MODIFY ANY OPTION";TAB(69);"[ ]"
11480 PRINT
11482 A$=FNQ$(2%)+FNO$(C%(2%)+15%,R%(10%))+FNQ$(1%)
11484 A$="": A$=FNK$
11486 IF (A$=" ")OR(A$=CHR$(8%)) THEN
        A$=FNQ$(2%)+FNO$(C%(2%)+15%,R%(11%))+FNQ$(1%):
        GO TO 11490
11488 IF A$="X" THEN 11505 ELSE 11484
11490 A$="": A$=FNK$
11492 IF (A$=" ") OR (A$=CHR$(8%)) THEN 11482
11494 IF A$="X" THEN 11000 ELSE 11490
11505 CLOSE 2%
11510 RETURN
13000!

```

```

! SUBROUTINE TO INPUT SIMULATION INFORMATION
! AND EVENTS-TIMES RECORDS FROM DISK FILE

```

```

13010!
! INPUT SIMULATION INFORMATION (FIRST RECORD)

13015 FIELD #3%, 2% AS A1$, 2% AS A2$, 4% AS A3$, 4% AS A4$,
        400% AS A5$, 100% AS A6$
! SET FORMAT FOR SIMULATION INFORMATION
13020 N$=""
! NULL STRING
13025 GET #3%, RECORD 1%
! INPUT FIRST RECORD
13030 N1%=CVT$(A1$)
! NUMBER OF NETWORK LINES
13035 N1=N1%
13040 N2%=CVT$(A2$)
! NUMBER OF SIMULATION EVENTS
13045 N2=N2%
13055 N4=CVT$(A4$)
! MAXIMUM SIMULATION TIME VALUE
13060 L1%(I%)=CVT$(MID(A5$,I%*2%-1%,2%)) FOR I%=1% TO 200%
! CONVERT EACH CHARACTER PAIR TO A LINE NUMBER (I/O)
13065 H$=A6$+N$
! SIMULATION HEADER
13070!
! INPUT NETWORK LINE NUMBERS

13075 FIELD #3%, 512% AS B1$

```

```

! SET BUFFER FORMAT FOR LINE-NUMBER
! CHARACTER PAIRS
13080 L$=N$
! NULL THE LINE-NUMBER STRING
13085 Z=N1*2/512
! 256 LINE-NUMBER CHARACTER PAIRS PER RECORD
13090 IF Z=INT(Z) THEN C3%=INT(Z)
      ELSE C3%=INT(Z+1)
! CALCULATE NUMBER OF LINE-NUMBER RECORDS
13095 FOR I%=1% TO C3%
      ! INPUT C3% LINE-NUMBER RECORDS
13100 R1%=1%+I%
      ! DETERMINE RECORD NUMBER
13105 GET #3%, RECORD R1%
      ! INPUT LINE-NUMBER RECORD INTO BUFFER
13110 L$=L$+B1$
      ! BUILD LINE-NUMBER CHARACTER-PAIR STRING
13115 NEXT I%
13120 L$=LEFT(L$,N1%*2%)
      ! REMOVE TRASH CHARACTERS FROM STRING
13122 L$=L$+CVT$(0)
13125!
      ! INPUT EVENT-TIMES RECORDS

13130 FIELD #3%, (I%-1%)*4% AS D$, 4% AS B$(I%)
      FOR I%=1% TO 128%
      ! SET BUFFER FORMAT FOR EVENT-TIMES
13135 Z=N2/128
      ! 128 EVENT-TIMES PER RECORD
13140 IF Z=INT(Z) THEN C1%=INT(Z)
      ELSE C1%=INT(Z+1)
      ! CALCULATE NUMBER OF EVENT-TIMES RECORDS
13145 FOR I%=1% TO C1%
      ! INPUT AND CONVERT C1% EVENT-TIMES RECORDS
13150 R1%=1%+C3%+I%
      ! DETERMINE RECORD NUMBER
13155 GET #3%, RECORD R1%
      ! INPUT EVENT-TIMES RECORD INTO BUFFER
13160 FOR J%=1% TO 128%
      ! CONVERT EVENT TIMES
13165 E((I%-1%)*128%+J%)=CVT$(B$(J%))
      ! UNPACK AND STORE EVENT TIMES
13170 NEXT J%
13175 NEXT I%
13180!
      ! CALCULATE NUMBER OF LINE-STATE RECORDS

13185 C1=C1%
13190 Z=C1/4
      ! 4 EVENT-TIMES RECORDS PER LINE-STATE RECORD
13195 IF Z=INT(Z) THEN C2%=INT(Z)
      ELSE C2%=INT(Z+1)
      ! CALCULATE NUMBER OF LINE-STATE RECORDS
13200 RETURN
14000!

! SUBROUTINE TO INPUT LINE-STATE RECORDS

```

```

14005!  L% = LINE NUMBER INDEX
        C1% = NUMBER OF EVENT-TIMES RECORDS
        C2% = NUMBER OF LINE-STATE RECORDS PER LINE
        C3% = NUMBER OF LINE-NUMBER RECORDS
        N2% = NUMBER OF EVENTS
        G$ = STRING CONTAINING LINE STATES

14010  FIELD #3%, 512% AS B1$
        ! SET FORMAT OF BUFFER FOR LINE STATES
14015  G$=N$
        ! NULL THE LINE-STATE STRING
14020  FOR I%=1% TO C2%
        ! GET C2% RECORDS
14025  R1%=1%+C3%+C1%+((L%-1%)*C2%)+I%
        ! DETERMINE WHICH LINE-STATE RECORD TO ACCESS RANDOMLY
14026  R1%=R1%+1%      ! TEMPORARY FIX
14030  GET #3%, RECORD R1%
        ! INPUT LINE-STATE RECORD INTO BUFFER
14035  G$=G$+B1$
        ! BUILD LINE-STATE STRING
14040  NEXT I%
14045  G$=LEFT(G$,N2%)
        ! THROW AWAY TRASH CHARACTERS
14050  RETURN
        ! RETURN WITH LINE-STATE STRING G$
16000!

        !      SUBROUTINE TO OUTPUT STATE SEGMENTS

16005!      STATE "A" = LOGIC 0
16010!      STATE "B" = LOGIC 1
16015!      STATE "C" = LOGIC 0 THAT SHOULD BE LOGIC 1
16020!      STATE "D" = LOGIC 1 THAT SHOULD BE LOGIC 0
16025!      STATE "E" = INDETERMINANT STATE
16030!      STATE "F" = TRANSITION FROM LOGIC 0 TO LOGIC 1
16035!      STATE "G" = TRANSITION FROM LOGIC 1 TO LOGIC 0
16040!      STATE "H" = ERROR CONDITION
        !
16045!      S$ = STATE INDICATOR
        S1% = STARTING X POSITION
        S2% = STARTING Y POSITION
        S3% = LENGTH OF STATE SEGMENT
        S4% = HEIGHT OF STATE SEGMENT

16050  IF INSTR(1%,"ABCDEFGH",S$)=0% THEN 16395
        ! CHECK FOR ILLEGAL STATE
16052  F0%=F1%:F1%=0%
16055  ON INSTR(1%,"ABCDEFGH",S$) GOTO 16050,16095,16130,16180,16230,
        16235,16360,16390
        ! BRANCH TO APPROPRIATE SEGMENT ROUTINE
16060!      ! DRAW STATE "A"

```

```
16061 F1%=1%
16063 A$=FNC$(F0%,F1%)
16065 FOR I%=1% TO 3%
16068 Q1%=S1%
16071 Q2%=S2%+I%
16074 Q3%=S1%+S3%
16077 Q4%=Q2%
16080 A$=FNS$
16085 NEXT I%
16090 GOTO 16395
16095!
```

```
! DRAW STATE "B"
```

```
16097 F1%=2%
16098 A$=FNC$(F0%,F1%)
16100 Q1%=S1%
16105 Q2%=S2%+S4%
16110 Q3%=S1%+S3%
16115 Q4%=Q2%
16120 A$=FNS$
16125 GOTO 16395
16130!
```

```
! DRAW STATE "C"
```

```
16135 FOR I%=1% TO 3%
16138 Q1%=S1%
16141 Q2%=S2%+I%
16145 Q3%=S1%+S3%
16150 Q4%=Q2%
16155 A$=FNS$
16158 NEXT I%
16160 Q2%=S2%+S4%
16165 Q4%=Q2%
16170 A$=FNS$
16175 GOTO 16395
16180!
```

```
! DRAW STATE "D"
```

```
16185 FOR I%=1% TO 3%
16188 Q1%=S1%
16190 Q2%=S2%+I%
16195 Q3%=S1%+S3%
16200 Q4%=Q2%
16205 A$=FNS$
16208 NEXT I%
16210 Q2%=S2%+S4%
16215 Q4%=Q2%
16220 A$=FNS$
16225 GOTO 16395
16230!
```

```
! DRAW STATE "E"
```

```
16233 FOR I%=1% TO 3%
16235 Q1%=S1%
16240 Q2%=S2%+I%
16245 Q3%=S1%+S3%
16250 Q4%=Q2%
```

```
16255  A$=FNSS$
16258  NEXT I%
16260  Q2%=S2%+S4%
16265  Q4%=Q2%
16270  A$=FNSS$
16275  IF S3%<8% THEN 16395
16280  S4%=S1%+S3%
16285  Q1%=S1%
16290  Q2%=S2%
16295  Q4%=Q2%+H2%
16300  Q3%=Q1%+8%
16305  IF Q3%>S4% THEN 16395
16310  A$=FNSS$
16315  Q1%=Q1%+8%
16320  GOTO 16300          ! LOOP BACK AGAIN
16325!

      ! DRAW STATE "F"

16330  Q1%=S1%: Q2%=S2%+S4%/2%
16332  Q3%=S1%+S3%: Q4%=Q2%
16334  A$=FNDS$          ! DRAW DASHED LINE
16336  Q1%=S1%+S3%/2%: Q2%=S2%
16338  Q3%=Q1%: Q4%=S2%+S4%
16340  A$=FNSS$          ! DRAW ARROW STEM
16342  Q1%=S1%+S3%/2%: Q2%=S2%+S4%
16344  Q3%=S1%+S3%/4%: Q4%=S2%+3%*S4%/4%
16346  A$=FNSS$          ! DRAW ARROWHEAD
16348  Q1%=S1%+S3%/2%: Q2%=S2%+S4%
16350  Q3%=S1%+3%*S3%/4%: Q4%=S2%+3%*S4%/4%
16352  A$=FNSS$          ! DRAW ARROWHEAD
16355  GOTO 16395
16360!

      ! DRAW STATE "G"

16362  Q1%=S1%: Q2%=S2%+S4%/2%
16364  Q3%=S1%+S3%: Q4%=Q2%
16366  A$=FNDS$          ! DRAW DASHED LINE
16368  Q1%=S1%+S3%/2%: Q2%=S2%
16370  Q3%=Q1%: Q4%=S2%+S4%
16372  A$=FNSS$          ! DRAW ARROW STEM
16374  Q1%=S1%+S3%/2%: Q2%=S2%
16376  Q3%=S1%+S3%/4%: Q4%=S2%+S4%/4%
16378  A$=FNSS$          ! DRAW ARROWHEAD
16380  Q1%=S1%+S3%/2%: Q2%=S2%
16382  Q3%=S1%+3%*S3%/4%: Q4%=S2%+S4%/4%
16384  A$=FNSS$          ! DRAW ARROWHEAD
16386  GO TO 16395
16390!

      ! DRAW STATE "H"

16395!

EXIT

16400  A$=FNQ$(1%)
      ! RESET TERMINAL TO ALPHA MODE
16405  RETURN
      ! EXIT
17000!
```

```

!           SUBROUTINE TO RETRIEVE LINE NUMBERS
!           FROM THE USER TERMINAL.

17005 F3%=0% : N5%=0%
17010 FOR I%=1% WHILE F3%=0%
17015 F4%=0%
17020 PRINT "*";
17025 INPUT LINE #2%, A$
17030 IF A$=CHR$(13)+CHR$(10) OR A$=","+CHR$(13)+CHR$(10)
      THEN F3%=1%
      :GOTO 17110
17035 A$=CVT$$ (A$,156%)+ "*" ! CLEAN STRING, ADD DELIMITER
17040 J%=1%
17045 T1%=INSTR(J%,A$,"")
17050 T2%=INSTR(J%,A$," ")
17055 IF T1%=0% THEN T1%=T2%
17060 IF T2%=0% THEN T2%=T1%
17065 IF T1%=0% AND T2%=0%
      THEN K%=INSTR(J%,A$,"*")
      :F4%=1%
      :GOTO 17075
17070 IF T2%<T1%
      THEN K%=T2%
      ELSE K%=T1%
17075 D$=MID(A$,J%,K%-J%)
17080 IF D$="" THEN 17100
17085 N5%=N5%+1%
17090 IF N5%>200%
      THEN PRINT "LINE LIMIT EXCEEDED"
      :GOTO 17120
17095 L2%(N5%)=VAL(D$)
      ! STORE LINE NUMBER
17100 J%=K%+1%
17105 IF F4%=0% THEN 17045
17110 NEXT I%
17115 IF N5%=0%
      THEN 17005
17120 RETURN !RETURN FROM LINE ROUTINE
17500 !
!           SUBROUTINE TO DRAW STATE DISPLAY PAGE
17510 P1%=100% !LEFT BOUNDARY
17515 P2%=1000% !RIGHT BOUNDARY
17520 P3%=90% !BOTTOM BOUNDARY
17525 P4%=750% ! TOP BOUNDARY
17530 N%=10% ! NUMBER OF LINES/PAGE OF DISPLAY
17540 H1%=66% !DISTANCE BETWEEN LINES
17545 H2%=22% !DISTANCE BETWEEN 0 AND 1 LINES
17550 !
!           DRAW PLOT BOUNDARY LINES
17555 A$=FNQ$(0%) !ERASE SCREEN
17560 A$=FNQ$(2%)+FNO$(P1%,P3%)
17565 A$=FNO$(P2%,P3%)+FNO$(P2%,P4%)+FNO$(P1%,P4%)+FNO$(P1%,P3%)
17566 A$=FNO$(0,P3%)+FNO$(0,P3%-25%)+FNO$(1020,P3%-25)+FNO$(1020,P3%)
17567 A$=FNO$(1000%,P3%)+FNQ$(1%)
17570 !

```

```

!          PRINT OPTIONS MINI-MENU
17575  A$=FNQ$(2%)+FNO$(P1%,10%)+FNQ$(1%)
17580  PRINT "CONTINUE [ ]  MODIFY ANY OPTION [ ]  EXIT PROGRAM [ ]  ";
17581  PRINT "TIME [ ]"
17585  !
!          PRINT LINE NUMBER HEADING
17590  A$=FNQ$(2%)+FNO$(0%,P4%)+FNQ$(1%)
17595  PRINT "LINE #"
17600  !
!          PRINT TIME HEADING
17605  A$=FNQ$(2%)+FNO$(10%,P3%-20%)+FNQ$(1%)
17610  PRINT "TIME"
17612  A$=FNQ$(2%)+FNO$(10%,P3%-45%)+FNQ$(1%)
17614  PRINT A3$
17615  !
!          PRINT HEADER
17620  A$=FNQ$(2%)+FNO$(P1%,P4%+65%)+FNQ$(1%)
17630  PRINT H$
17635  !
!          DRAW TIMING GRID
!
17640  IF O%(4%)<>0% THEN 17800
17650  FOR I%=1% TO 17% STEP 2%
17652  A$=FNQ$(2%)+FNO$(P1%+I%*50%,P3%)+FNO$(P1%+I%*50%,P4%)
17654  NEXT I%
17656  FOR I%=2% TO 16% STEP 2%
17658  A$=FNQ$(2%)+FNO$(P1%+I%*50%-2%,P3%)+FNO$(P1%+I%*50%-2%,P4%)
17660  A$=FNQ$(2%)+FNO$(P1%+I%*50%+2%,P3%)+FNO$(P1%+I%*50%+2%,P4%)
17662  NEXT I%
17680  IF O%(3%)=2% THEN T5=P1+18*P3
          ELSE IF O%(3%)=1% THEN T5=P2
          ELSE T5=1.05*N4: P1=E(1%)

17690  T4=P1: T6=900/(T5-T4)
17700  T9=(T5-T4)/18
17720  FOR I%=0% TO 18% STEP 2%
17730  X=P1%+I%*50%-40%
17740  T7=T4+I%*T9
17750  A$=FNQ$(2%)+FNO$(X,P3%-20%)+FNQ$(1%)
17760  PRINT USING "####",T7
17770  NEXT I%
17800  RETURN
18000  !
!          SUBROUTINE TO DISPLAY TIMING DATA FOR A SPECIFIC LINE
!
!
18020  FOR I%=1% TO 2*N1% STEP 2%
18030  L3%=CVT$(MID(L$,I%,2%))
18040  IF L%=L3% THEN 18070
18050  NEXT I%
18060  RETURN          ! ERROR: LINE # NOT FOUND
18070  L3%=L%: L%=I%/2%
18120  M%=N%-1%-M%: Z9%=M%*H1%+P3%
18125  S2%=Z9%: S4%=H2%
18130  A$=FNQ$(2%)+FNO$(0%,Z9%)+FNQ$(1%)
18140  PRINT L3%
18150  GOSUB 14000
18160  I4=0

```

B2U

```
18170 IF T4<E(1%) THEN 18240
18180 IF NOT(T4>N4) THEN I1=T4: I9%=2%: GO TO 18330
18190 S$=MID(G$,N2%,1%)
18200 S1%=P1%
18210 S3%=900%
18220 GOSUB 16000
18230 GO TO 18480
18240 IF T5<E(1%) THEN F6%=0%: I2=T5: GO TO 18260
18250 F6%=1%: I2=E(1%)
18260 I1=T4: I3=(I2-I1)*T6
18265 S$=MID(G$,1%,1%)
18270 S1%=P1%
18280 S3%=I3
18290 I4=I4+I3
18300 GOSUB 16000
18310 IF F6%=0% THEN 18480
18320 I1=E(1%): I9%=2%
18330 IF E(I9%)>T4 THEN 18350
18340 I9%=I9%+1%: GO TO 18330
18350 I2=E(I9%): S$=MID(G$,I9%-1%,1%)
18360 I9%=I9%+1%: S1$=MID(G$,I9%-1%,1%)
18370 IF S$=S1$ THEN 18410
18380 I3=(I2-I1)*T6: S1%=P1%+I4: S3%=I3: I4=I4+I3
18390 GOSUB 16000 !DRAW STATE SEGMENT
18400 I1=I2: S$=S1$
18410 I2=E(I9%)
18420 IF I2>T5 THEN S$=MID(G$,I9%-1%,1%): GO TO 18440
18430 IF I9%=N2%+1% THEN S$=MID(G$,N2%,1%): GO TO 18440
18435 GO TO 18360
18440 I2=T5: I3=(I2-I1)*T6
18450 S3%=I3: S1%=P1%+I4
18470 GOSUB 16000
18480 L%=L3%: M%=N%-1%-M%
18490 RETURN
19000!
```

! ERROR HANDLER ROUTINE

```
19010 CLOSE 1%,2%,3%
19020 PRINT ERR,ERL
19030 GO TO 32767
32767 END
```

Part 6

AN AUTOMATIC ROUTING PROGRAM FOR  
PRINTED CIRCUIT BOARDS AND HYBRID SUBSTRATES

Prepared for  
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## I. Problem Statement

The purpose of this project is to develop a computer program that will automatically route the conductor paths required in a hybrid circuit.

The problem associated with this type program is to route the hundreds of connections present in a typical circuit with a path that avoids previously laid paths. The program should accomplish the following objectives:

- The program should route a high percentage of the connections present.
- The program should determine the shortest path that meets all designer imposed constraints with the minimum likelihood of preventing future connections.
- The program must have reasonable requirements of computer memory and execution time.

## II. Program Description

A program that meets these requirements will now be described. This program, named ARP for Automated Routing Program, will route up to 1000 connections on a maximum 256 square inch, 16 layer board. This assumes 50 mil centers between connections. No vias or feedthroughs are produced.

The program routes each layer sequentially until all connections which can be routed are routed. Obviously, since the layers are handled sequentially, the lower layers will be denser than the upper layers.

To use ARP, a wire list of the circuit must be developed. Each entry in a wire list consists of the x & y coordinates of the two terminals comprising a connection. To determine the x & y coordinates of each terminal, each layer of the chip or board must be uniformly divided into a grid, with the origin located in the lower left corner. Every terminal will then have an x & y coordinate associated with it.

Given this information, the program will first order the wire list. This operation will place those connections that will have least effect upon future connections at the top of the list. This will help insure a higher percentage of routable connections.

Before describing the routing process, the CELMAP array will be explained. This array contains all information about the state of the board. Each cell on the board maps into a cell of this array--the x & y dimensions of the board corresponding to the x & y dimensions of the array. Since the array's size is directly related to the size of the board, it is primarily responsible for the memory requirements of

the program. The array is also 3-dimensional--the third dimension consisting of two fields:

- The availability or A-field which is used to indicate whether a cell is available or not on each layer allowed. For each layer (bit #16 through bit #31 corresponds to layer 1 through layer 16) a value of 1 denotes an available cell and 0 an unavailable one.
- The sequence or S-field which is used to indicate the sequence number of an expanded cell in the routing process.

Now that the information contained within the CELMAP array is understood, the routing process will be presented step-by-step:

- 1) All A-fields must be preset according to the number of layers allowed.
- 2) Reset all A-fields for those cells that have been designated as blockades.
- 3) Reset all A-fields for all terminal cells.
- 4) Make first pass through the wire list for those connections that wish to be placed on the present layer. Jump to Step 6.
- 5) Make second pass through the wire list for all remaining connections, other than those designated for remaining layers.
- 6) Get x & y coordinates of a connection.
- 7) Determine dimensions of framing rectangle to limit cell expansion.
- 8) Clear all S-fields. Set S-field of starting cell to 1.

- 9) Initialize A-fields of both terminal cells to 1 for each layer allowed.
- 10) Add starting cell to NEWCEL list.
- 11) Determine the four neighboring cells to each cell recently added to the NEWCEL list on the previous expansion level.
- 12) Determine if each new expansion cell above can become a new frontier cell.
  - (a) Is cell unmarked?
  - (b) Is cell available on present layer?
- 13) Mark S-field of all good cells with present sequence number and add to NEWCEL list.
- 14) Unless target cell has been reached, go to Step 11 after incrementing sequence number.
- 15) Add target cell to PATH list.
- 16) Decrement sequence counter.
- 17) Determine neighboring cells to present PATH cell.
- 18) Determine if a cell above can become a PATH cell by checking if the S-field equals the present sequence counter.
- 19) Add cell to PATH list.
- 20) Unless starting cell has been reached, go to Step 16.
- 21) Output PATH list.
- 22) Reset present layer bit in A-field for each cell in the PATH list.
- 23) Clear all lists.
- 24) If through with pass 1 through wire list, go to Step 5.

25) If through with pass 2 through wire list, jump to next layer  
and go to Step 4.

26) If present layer is last layer allowed--Stop.

### III. Conclusions

ARP can be used to route the conductor paths on both printed circuit boards and hybrid chips. On a typical printed circuit board of two layers and 155 connections, it took ARP 222 seconds to route all the connections (all but 5 on the first layer).

The sequential nature of ARP makes it suited for hybrid circuits. Two popular methods of layering connections on a hybrid chip are to separate each layer of conductor with a layer of insulator or to place insulating material only at each location of overlap between adjacent layers of conductor. Since ARP treats each layer sequentially without producing any vias, each layer, in effect, is separate from any other layer. Therefore, each layer that ARP routes can be separated with a layer of insulator. The feature of being able to designate a preferred layer for a connection to be placed on gives added flexibility.

Further improvements can be made to ARP to make it easier to use. ARP is a general routing program depending upon x & y coordinate input and producing x & y coordinate output. Therefore, tailor-made inputs and outputs can be developed for any need. A net-list-to-wire-list converter would eliminate much user time in preparing a circuit to be routed. Instead of feeding x & y coordinates of each terminal to ARP, one would be able to give the position and orientation of components instead. This would, however, require a quite extensive component library.

Any form of output could easily be developed using any type of medium--from a plotter to a graphics terminal. A graphics terminal

would also lend itself to interactive routing where the placement of jumpers, the notification of areas of overlap, and the manual addition of non-routable connections may be dealt with.

USER'S GUIDE

And

PROGRAM LISTING

```
C
C
C*****
C
C
C
C
C      AAAAAAAAAA      RRRRRRRRRRR      PPPPPPPPPPP
C      AAAAAAAAAAAAAA      RRRRRRRRRRRRR      PPPPPPPPPPPPP
C      AA      AA      RR      RR      PP      PP
C      AA      AA      RR      RR      PP      PP
C      AA      AA      RR      RR      PP      PP
C      AAAAAAAAAAAAAA      RRRRRRRRRRRRR      PPPPPPPPPPPPP
C      AAAAAAAAAAAAAA      RRRRRRRRRRR      PPPPPPPPPPP
C      AA      AA      RR      RR      PP
C      AA      AA      RR      RR      PP
C      AA      AA      RR      RR      PP
C      AA      AA      RR      RR      PP
C
C
C
C
C*****
C
C
C      AUTOMATED  ROUTING  PROGRAM
C      VERSION 1      DECEMBER 1977
C      AUBURN UNIVERSITY ELECTRICAL ENGINEERING DEPARTMENT
C      DEVELOPED BY STANLEY S. KAWKA UNDER CONTRACT DAAK40-77-C-0042
C
C*****
C
```



C THIS WILL ALLOW YOU TO ACCESS THE LOAD MODULE EE251.SSK(ARP)  
 C AND EXECUTE IT. NO SOURCE LISTING WILL OCCUR-ONLY THE PROGRAM  
 C OUTPUT WILL BE GIVEN.  
 C IF THE DIMENSIONS OF THE ARRAYS ARE INCREASED THE REGION  
 C PARAMETER IN THE JOB CARD MAY NEED TO BE INCREASED ALSO.  
 C  
 C IF ANY CHANGES ARE NEEDED TO BE MADE IN THE PROGRAM THE FOLLOWING  
 C JCL IS NEEDED:

```

C //ARP JOB (EE251,EEL),'YOUR NAME',MSGLEVEL=1,REGION=192K
C /*JOBPARM LINES=10K,TIME=200
C //KILL EXEC ZAP
C //SYSIN DD *
C EE251.SSK
C //FORT EXEC FORTGCL
C //FORT.SYSIN DD *
C
C PROGRAM
C
C //LKED.SYSLMOD DD DSN=EE251.SSK(ARP),DISP=(,CATLG),
C // UNIT=DISK,SPACE=(TRK,(1,1,1)),LABEL=EXPDT=78365
C //
  
```

C THIS WILL DELETE THE OLD LOAD MODULE AND CREATE THE NEW ONE IN ITS  
 C PLACE. NOTE THAT THE EXPIRATION DATE IS DECEMBER 31, 1978.

#### BOARD SIZE VERSUS MEMORY REQUIREMENTS

C MEMORY REQUIREMENTS DEPEND PRIMARILY UPON THE CELMAP ARRAY SINCE IT  
 C REQUIRES THE MOST STORAGE.  
 C THE FOLLOWING TABLES SHOULD HELP IN DECIDING HOW MUCH MEMORY SHOULD  
 C BE REQUESTED.  
 C ASSUME 50 MIL CENTERS BETWEEN CONNECTIONS.

SIZE (SQ IN)	TYPICAL DIMENSION	DIMENSION OF CELMAP ARRAY	MEMORY
50	8*5	(160,100,2)	192K
100	10*8	(200,160,2)	384K
150	12*12	(240,240,2)	576K
200	20*10	(400,200,2)	832K
250	16*16	(320,320,2)	1024K

#### SUGGESTED ARRAY SIZES:

CELMAP	CONECT	NEWCEL	OUTCEL/PATH
160,100,2	300,6	1500,2	200,2
200,160,2	500,6	3000,2	250,2
240,240,2	1000,6	6000,2	300,2
400,200,2	1000,6	10000,2	400,2
320,320,2	1000,6	16000,2	500,2

## DATA FORMAT

THE DATA THE PROGRAM NEEDS CONSISTS OF:

1. IDENTIFICATION CARD
2. PARAMETER CARD
3. CONSTRAINT CARD
4. WIRE LIST DECK
5. BLOCKADE LIST DECK

THE IDENTIFICATION CARD IS ANY 80 CHARACTER NAME ASSOCIATED WITH THE BOARD TO BE ROUTED.

1  
ANYTHING

THE PARAMETER CARD GIVES THE DIMENSIONS (CELLULAR) OF THE BOARD TO BE ROUTED. THERE ARE NO DEFAULT VALUES.

1	3	6
0	0	0
HORIZONTAL DIMENSION=NNNN	VERTICAL DIMENSION=NNNN	LAYERS=NN

THE CONSTRAINT CARD GIVES THE VALUES FOR THE FRAME EXPANSION FACTOR AND THE LEVEL EXPANSION LIMIT. THE FRAME EXPANSION FACTOR IS AN INTEGER FROM 1-5 WHICH DETERMINES HOW MANY TIMES THE FRAME MAY EXPAND. THE LEVEL EXPANSION LIMIT IS AN INTEGER FROM 1-999 WHICH DETERMINES HOW MANY CYCLES OF CELL EXPANSION MAY BE PERFORMED. THE DEFAULT VALUES ARE 1 AND 100 RESPECTIVELY.

1	1
0	0
N	NNN

EACH CARD IN THE WIRE LIST DECK GIVES THE X&Y COORDINATES OF BOTH THE STARTING CELL AND THE ENDING CELL FOR ONE CONNECTION. IF THIS CONNECTION IS DESIRED ON A PARTICULAR LAYER, THIS PREFERENCE IS INDICATED. THE DEFAULT VALUE FOR THIS PREFERENCE IS 0 INDICATING THAT IT MAY BE ROUTED ON THE FIRST AVAILABLE LAYER. CARE MUST BE EXERCISED, HOWEVER, IN DESIGNATING A PREFERENCE FOR ANY LOWER LAYER SINCE MOST OF THE ROUTING IS DONE ON THESE LAYERS. ANY PREFERENCE FOR THE LOWER LAYERS WILL RESULT IN DECREASED EFFICIENCY. A BLANK CARD AT THE END OF THIS DECK TERMINATES THE LIST.

123456789012345  
X1 Y1 X2 Y2 L



C\*\*\*\*\*  
 C  
 C  
 C  
 C

## DECLARATION STATEMENTS

C\*\*\*\*\*  
 C  
 C

CHANGE THE FOLLOWING FOUR DIMENSION CARDS FOR ANY CHANGES IN BOARD SIZE.

DIMENSION CELMAP(160,100,2)  
 DIMENSION CONECT(300,6)  
 DIMENSION NEWCEL(1500,2)  
 DIMENSION OUTCEL(200,2),PATH(200,2)  
 DIMENSION TRACEL(4,2),PARRAY(10,2),IDENT(20)  
 EQUIVALENCE (OUTCEL,PATH)  
 INTEGER CELMAP,CONECT,OUTCEL,PATH,TRACEL,PARRAY  
 INTEGER HORDIM,VERDIM,TIMES,EXPAND  
 INTEGER STARTX,STARTY,ENDX,ENDY  
 INTEGER XLOW,XHIGH,YLOW,YHIGH  
 INTEGER XDIFF,YDIFF,XADD,YADD  
 INTEGER XBLOCK,YBLOCK  
 INTEGER TFRAME,BFRAME,LFRAME,RFRAME  
 INTEGER X,Y,P,SEQUEN,FACTOR,CONBOT,HOLD,PREF,CTEMP

C

C

C\*\*\*\*\*  
 C  
 C  
 C

## OUTPUT HEADING

C\*\*\*\*\*  
 C

WRITE(6,850)  
 WRITE(6,860)  
 WRITE(6,870)  
 WRITE(6,880)

C

C

C\*\*\*\*\*  
 C  
 C  
 C

## INPUT SECTION

C\*\*\*\*\*  
 C  
 C

READ(5,800)IDENT  
 READ(5,810)HORDIM,VERDIM,LAYERS  
 READ(5,820)TIMES,EXPAND

CHANGE THIS STATEMENT IF DIMENSIONS OF CELMAP ARRAY ARE ALTERED

IF(HORDIM.GT.160.OR.VERDIM.GT.100)GO TO 270  
 IF(LAYERS.GT.16)GO TO 680  
 IF(TIMES.LT.1)TIMES=1  
 IF(TIMES.GT.5)TIMES=5  
 IF(EXPAND.LT.1)EXPAND=100  
 WRITE(6,890)IDENT  
 WRITE(6,900)HORDIM,VERDIM,LAYERS  
 WRITE(6,910)TIMES,EXPAND

C

```

C
C *****
C
C ORDERING SECTION
C *****
C
C INPUT WIRE LIST-BLANK CARD SIGNIFIES END
C
C I=1
100 READ(5,830)(CONECT(I,J),J=1,4),CONECT(I,6)
C IF(CONECT(I,1).LE.0)GO TO 110
C I=I+1
C CHANGE THIS STATEMENT IF DIMENSIONS OF CONECT ARRAY ARE ALTERED
C IF(I.GT.300)GO TO 690
C GO TO 100
110 NUMCON=I-1
C
C INITIALIZE COLUMN 5
C
C DO 120 I=1,NUMCON
C CONECT(I,5)=0
120 CONTINUE
C
C FOR EACH WIRE LIST PAIR, DETERMINE THE NUMBER OF TERMINALS WITHIN THE
C RECTANGLE DEFINED BY THAT PAIR
C INSERT THAT NUMBER IN COLUMN 5
C
C DO 140 I=1,NUMCON
C XLOW=MINO(CONECT(I,1),CONECT(I,3))
C XHIGH=MAXO(CONECT(I,1),CONECT(I,3))
C YLOW=MINO(CONECT(I,2),CONECT(I,4))
C YHIGH=MAXO(CONECT(I,2),CONECT(I,4))
C DO 130 J=1,NUMCON
C IF(J.EQ.I)GO TO 130
C IF((CONECT(J,1).LE.XHIGH.AND.CONECT(J,1).GE.XLOW).AND.
1 (CONECT(J,2).LE.YHIGH.AND.CONECT(J,2).GE.YLOW))
2 CONECT(I,5)=CONECT(I,5)+1
C IF((CONECT(J,3).LE.XHIGH.AND.CONECT(J,3).GE.XLOW).AND.
1 (CONECT(J,4).LE.YHIGH.AND.CONECT(J,4).GE.YLOW))
2 CONECT(I,5)=CONECT(I,5)+1
130 CONTINUE
140 CONTINUE
C
C SORT THE WIRE LIST WITH RESPECT TO COLUMN 5
C (SMALLEST TO LARGEST)
C
C CONBOT=NUMCON
C NSORT=2
150 NOSWAP=0

```

```

I=1
J=2
160 IF(CONECT(I,5).LE.CONECT(J,5))GO TO 180
DO 170 M=1,6
ITEMP=CONECT(J,M)
CONECT(J,M)=CONECT(I,M)
CONECT(I,M)=ITEMP
170 CONTINUE
NOSWAP=1
180 IF(J.EQ.CONBOT)GO TO 190
I=I+1
J=J+1
GO TO 160
190 IF(NSORT.EQ.NUMCON)GO TO 200
IF(NOSWAP.EQ.0)GO TO 200
NSORT=NSORT+1
CONBOT=CONBOT-1
GO TO 150

```

```

C
C OUTPUT ORDERED WIRE LIST
C

```

```

200 WRITE(6,920)NUMCON
M=1
DO 270 I=1,NUMCON
IF(M-2)210,230,250
210 IF(CONECT(I,6).NE.0)GO TO 220
WRITE(6,930)I,(CONECT(I,J),J=1,5)
M=2
GO TO 270
220 WRITE(6,940)I,(CONECT(I,J),J=1,6)
M=2
GO TO 270
230 IF(CONECT(I,6).NE.0)GO TO 240
WRITE(6,950)I,(CONECT(I,J),J=1,5)
M=3
GO TO 270
240 WRITE(6,960)I,(CONECT(I,J),J=1,6)
M=3
GO TO 270
250 IF(CONECT(I,6).NE.0)GO TO 260
WRITE(6,970)I,(CONECT(I,J),J=1,5)
M=1
GO TO 270
260 WRITE(6,980)I,(CONECT(I,J),J=1,6)
M=1
270 CONTINUE

```

```

C
C INITIALIZE COLUMN 5
C 0-NOT ROUTED 1-ROUTED
C

```

```

DO 280 I=1,NUMCON
CONECT(I,5)=0
280 CONTINUE

```

```

C

```

```

C
C *****
C
C          AVAILABILITY   FIELD   PRESET   SECTION
C
C *****
C
C PRESET ALL A-FIELDS ACCORDING TO THE NUMBER OF LAYERS ALLOWED
C
C     DO 290 I=1,HORDIM
C     DO 290 J=1,VERDIM
C BIT #16 THROUGH BIT #31 CORRESPONDS TO LAYER 1 THROUGH LAYER 16
C 0-LAYER NOT AVAILABLE      1-LAYER AVAILABLE
C   CELMAP(I,J,1)=65536-2**(16-LAYERS)
C 290 CONTINUE
C
C     LAYER=0
C     NO=1
C     NROUTE=0
C     PREF=0
C
C INPUT INITIAL BLOCKADE COORDINATES--BLANK CARD SIGNIFIES END
C RESET ALL BLOCKADE A-FIELDS
C OUTPUT BLOCKADES
C
C 300 WRITE(6,990)
C     I=1
C 310 READ(5,840)XBLOCK,YBLOCK
C     IF(XBLOCK.LE.0)GO TO 320
C     CELMAP(XBLOCK,YBLOCK,1)=0
C     PARRAY(I,1)=XBLOCK
C     PARRAY(I,2)=YBLOCK
C     IF(I.EQ.10)GO TO 320
C     I=I+1
C     GO TO 310
C 320 IF(XBLOCK.LE.0)I=I-1
C     WRITE(6,1000)((PARRAY(J,K),K=1,2),J=1,I)
C     I=1
C     IF(XBLOCK.LE.0)GO TO 330
C     GO TO 310
C
C RESET A-FIELDS FOR ALL TERMINAL CELLS
C
C 330 DO 340 I=1,NUMCON
C     CELMAP(CONECT(I,1),CONECT(I,2),1)=0
C     CELMAP(CONECT(I,3),CONECT(I,4),1)=0
C 340 CONTINUE
C

```

```

C
C *****
C
C          ROUTING  INITIALIZATION  SECTION
C
C *****
C
C PRINT LAYER LABEL
C MAKE TWO PASSES THROUGH WIRE LIST
C PASS 1-PREF=1    PASS 2-PREF=0
C PASS 1-ROUTE THOSE PAIRS THAT ARE PREFERRED ON THE PRESENT LAYER
C PASS 2-ROUTE ALL REMAINING PAIRS (COLUMN 6=0)
C
350 NEWCON=1
    IF(PREF.NE.1)GO TO 360
    PREF=0
    GO TO 470
360 IF(NO.EQ.0)GO TO 380
370 IF(LAYER.EQ.LAYERS)GO TO 760
    LAYER=LAYER+1
    WRITE(6,1010)LAYER
    NO=0
    PREF=1
    GO TO 470
380 WRITE(6,1020)
    GO TO 370
C
C RESET A-FIELDS ON PRESENT LAYER FOR CELLS IN PATH JUST ROUTED
C
390 DO 460 I=1,P
    IF(I.EQ.1.OR.I.EQ.P)GO TO 440
    HOLD=0
    LSUB=32768
400 CELMAP(PATH(I,1),PATH(I,2),1)=CELMAP(PATH(I,1),PATH(I,2),1)-LSUB
    IF(CELMAP(PATH(I,1),PATH(I,2),1).GE.0)GO TO 420
    CELMAP(PATH(I,1),PATH(I,2),1)=CELMAP(PATH(I,1),PATH(I,2),1)+LSUB
410 LSUB=LSUB/2
    IF(LSUB.LT.1)GO TO 450
    GO TO 400
420 IF(LSUB.EQ.(2**(16-LAYER)))GO TO 430
    HOLD=HOLD+LSUB
430 GO TO 410
440 CELMAP(PATH(I,1),PATH(I,2),1)=0
    GO TO 450
450 CELMAP(PATH(I,1),PATH(I,2),1)=HOLD
460 CONTINUE
C
C GET X&Y COORDINATES OF NEXT WIRE LIST PAIR
C
470 STARTX=CONECT(NEWCON,1)
    STARTY=CONECT(NEWCON,2)
    ENDX=CONECT(NEWCON,3)
    ENDY=CONECT(NEWCON,4)

```

```
C
C IF AT END OF LIST, JUMP TO NEXT PASS OR NEXT LAYER
C IF ALREADY ROUTED, SKIP (COLUMN 5=1)
C IF PREFERRED ON ANOTHER LAYER, SKIP (COLUMN 6<>0)
C
  IF(STARTX.LE.0)GO TO 350
  NEWCON=NEWCON+1
  IF(CONECT((NEWCON-1),5).EQ.1)GO TO 470
  IF(PREF.EQ.1)GO TO 480
  IF(CONECT((NEWCON-1),6).NE.0)GO TO 470
  GO TO 490
480 IF(CONECT((NEWCON-1),6).NE.LAYER)GO TO 470
C
C DETERMINE DIMENSIONS OF FRAMING RECTANGLE
C
490 FACTOR=0
  XDIFF=IABS(STARTX-ENDX)
  YDIFF=IABS(STARTY-ENDY)
  XADD=XDIFF/10
  IF(XADD.LE.2)XADD=3
  YADD=YDIFF/10
  IF(YADD.LE.2)YADD=3
  XLOW=MINO(STARTX,ENDX)
  XHIGH=MAXO(STARTX,ENDX)
  YLOW=MINO(STARTY,ENDY)
  YHIGH=MAXO(STARTY,ENDY)
C NUMBER OF TIMES TO CONTINUE EXPANDING RECTANGLE
500 IF(FACTOR.EQ.TIMES)GO TO 730
  FACTOR=FACTOR+1
  TFRAME=YHIGH+YADD*FACTOR
  BFRAME=YLOW-YADD*FACTOR
  RFRAME=XHIGH+XADD*FACTOR
  LFRAME=XLOW-XADD*FACTOR
C
C INITIALIZE ALL SEQUENCING FIELDS TO 0
C
510 DO 520 I=1,HORDIM
  DO 520 J=1,VERDIM
  CELMAP(I,J,2)=0
520 CONTINUE
C
```

```

C
C *****
C
C ROUTING EXPANSION SECTION
C *****
C
C INITIALIZE SEQUENCE COUNTER
C
C 530 SEQUEN=2
C
C INITIALIZE AVAILABILITY AND SEQUENCING FIELDS OF TERMINAL CELLS
C
C CELMAP(STARTX,STARTY,2)=1
C CELMAP(STARTX,STARTY,1)=65535
C CELMAP(ENDX,ENDY,1)=65535
C
C NEWCEL(1,1)=STARTX
C NEWCEL(1,2)=STARTY
C LEVEL=1
C NEWBOT=2
C NEWTOP=1
C
C DETERMINE THE FOUR NEIGHBORING (N,E,S,W) CELLS TO EACH CELL ON THE
C EXPANSION FRONTIER
C
C 540 L=NEWBOT-1
C KOUNT=1
C DO 550 I=NEWTOP,L
C OUTCEL(KOUNT,1)=NEWCEL(I,1)
C OUTCEL(KOUNT,2)=NEWCEL(I,2)+1
C KOUNT=KOUNT+1
C OUTCEL(KOUNT,1)=NEWCEL(I,1)+1
C OUTCEL(KOUNT,2)=NEWCEL(I,2)
C KOUNT=KOUNT+1
C OUTCEL(KOUNT,1)=NEWCEL(I,1)
C OUTCEL(KOUNT,2)=NEWCEL(I,2)-1
C KOUNT=KOUNT+1
C OUTCEL(KOUNT,1)=NEWCEL(I,1)-1
C OUTCEL(KOUNT,2)=NEWCEL(I,2)
C KOUNT=KOUNT+1
C CHANGE THIS STATEMENT IF DIMENSIONS OF OUTCEL ARRAY ARE ALTERED
C IF(KOUNT.GT.200)GO TO 700
C 550 CONTINUE
C
C DETERMINE IF EACH EXPANSION CELL CAN BECOME A NEW FRONTIER CELL
C
C KOUNT=KOUNT-1
C NEWADD=1
C
C DO 610 I=1,KOUNT
C X=OUTCEL(I,1)
C Y=OUTCEL(I,2)

```

```

C DO COORDINATES FALL WITHIN BOARD AND FRAME?
  IF(X.LT.LFRAME.OR.X.GT.RFRAME.OR.Y.LT.BFRAME.OR.Y.GT.TFRAME)
    1 GO TO 610
  IF(X.GT.HORDIM.OR.X.LT.1.OR.Y.GT.VERDIM.OR.Y.LT.1)GO TO 610
C IS CELL UNMARKED?
  IF(CELMAP(X,Y,2).NE.0)GO TO 610
C IS CELL AVAILABLE ON PRESENT LAYER?
  CTEMP=CELMAP(X,Y,1)
  LSUB=32768
550 CTEMP=CTEMP-LSUB
  IF(CTEMP.GE.0)GO TO 580
  CTEMP=CTEMP+LSUB
570 LSUB=LSUB/2
  IF(LSUB.LT.1)GO TO 610
  GO TO 560
580 IF(LSUB.EQ.(2**(16-LAYER)))GO TO 590
  GO TO 570
C
C SET SEQUENCE FIELD IF GOOD
C
590 CELMAP(X,Y,2)=SEQUEN
C
C ADD CELL TO EXPANSION LIST
C
600 NEWCEL(NEWBOT,1)=X
  NEWCEL(NEWBOT,2)=Y
  NEWADD=NEWADD+1
  NEWBOT=NEWBOT+1
C
C GO TO RETRACING SECTION IF THROUGH
C
  IF(X.EQ.ENDX.AND.Y.EQ.ENDY)GO TO 630
CHANGE THIS STATEMENT IF DIMENSIONS OF NEWCEL ARRAY ARE ALTERED
  IF(NEWBOT.GT.1500)GO TO 710
610 CONTINUE
C
C GET READY FOR A NEW LEVEL OF EXPANSION
C
  NEWADD=NEWADD-1
  NEWTOP=NEWBOT-NEWADD
  N=NEWBOT-1
  LEVEL=LEVEL+1
C
C IF EXPANSION LIMIT REACHED INCREASE FRAME SIZE
C
  IF(LEVEL.EQ.EXPAND)GO TO 500
C
C INCREMENT SEQUENCE COUNTER
C
  SEQUEN=SEQUEN+1
620 GO TO 540
C

```

```

C
C *****
C
C          ROUTING   RETRACING   SECTION
C *****
C
C
C 630 PATH(1,1)=X
      PATH(1,2)=Y
      P=1
C
C DECREMENT SEQUENCE COUNTER
C
C 640 SEQUEN=SEQUEN-1
      IF(SEQUEN.EQ.0)GO TO 660
      LASTX=X
      LASTY=Y
C
C DETERMINE NEIGHBORING CELLS TO PRESENT PATH CELL
C
      TRACEL(1,1)=PATH(P,1)
      TRACEL(1,2)=PATH(P,2)+1
      TRACEL(2,1)=PATH(P,1)+1
      TRACEL(2,2)=PATH(P,2)
      TRACEL(3,1)=PATH(P,1)
      TRACEL(3,2)=PATH(P,2)-1
      TRACEL(4,1)=PATH(P,1)-1
      TRACEL(4,2)=PATH(P,2)
      P=P+1
CHANGE THIS STATEMENT IF DIMENSIONS OF PATH ARRAY ARE ALTERED
      IF(P.GT.200)GO TO 720
C
C DETERMINE IF NEIGHBORING CELLS CAN BECOME A NEW PATH CELL
C
      DO 650 I=1,4
      X=TRACEL(I,1)
      Y=TRACEL(I,2)
C DO COORDINATES FALL WITHIN BOARD AND FRAME?
      IF(X.GT.HORDIM.OR.X.LT.1.OR.Y.GT.VERDIM.OR.Y.LT.1)GO TO 650
      IF(X.LT.LFRAME.OR.X.GT.RFRAME.OR.Y.LT.BFRAME.OR.Y.GT.TFRAME)
1      GO TO 650
C IS S-FIELD EQUAL TO PRESENT SEQUENCE COUNTER?
      IF(CELMAP(X,Y,2).NE.SEQUEN)GO TO 650
C
C ADD CELL TO PATH
C
      PATH(P,1)=X
      PATH(P,2)=Y
C
C PRINT OUT PATH IF THROUGH
C
      IF(X.EQ.STARTX.AND.Y.EQ.STARTY)GO TO 740
      GO TO 640
650 CONTINUE
C

```

C \*\*\*\*\*

ERROR HANDLER

C \*\*\*\*\*

C RETRACING ERROR

C 660 NEWCON=NEWCON-1  
NEWCON=NEWCON+1  
GO TO 470

C GRID SIZE ERROR

C 670 WRITE(6,1040)  
GO TO 1180

C LAYER LIMIT ERROR

C 680 WRITE(6,1050)  
GO TO 1180

C WIRE LIST ERROR

C 690 WRITE(6,1060)  
GO TO 1180

C \*\*\*\*\*

MESSAGES

C \*\*\*\*\*

C EXCESSIVE DIMENSIONS MESSAGES

C 700 NEWCON=NEWCON-1  
WRITE(6,1070)NEWCON  
NEWCON=NEWCON+1  
GO TO 470

C 710 NEWCON=NEWCON-1  
WRITE(6,1080)NEWCON  
NEWCON=NEWCON+1  
GO TO 470

C 720 NEWCON=NEWCON-1  
WRITE(6,1090)NEWCON  
NEWCON=NEWCON+1  
GO TO 470

C UNABLE TO ROUTE MESSAGE

C 730 NEWCON=NEWCON-1  
WRITE(6,1100)NEWCON  
NEWCON=NEWCON+1  
GO TO 470

```
C
C  PATH OUTPUT MESSAGE
C
740 NEWCON=NEWCON-1
   WRITE(6,1110)NEWCON,STARTX,STARTY,ENDX,ENDY
   CONECT(NEWCON,5)=1
   NEWCON=NEWCON+1
   NO=1
   NROUTE=NROUTE+1
   IP=P
750 WRITE(6,1120)PATH(IP,1),PATH(IP,2)
   IP=IP-1
   IF(IP.GT.0)GO TO 750
   GO TO 390

C
C  ROUTING COMPLETED MESSAGE
C
760 WRITE(6,1130)
   L=0
   DO 780 I=1,NUMCON
   IF(CONECT(I,5).EQ.0)GO TO 770
   GO TO 780
770 WRITE(6,1140)I
   L=L+1
780 CONTINUE
   IF(L.EQ.1)GO TO 790
   WRITE(6,1150)
790 WRITE(6,1160)
   WRITE(6,1170)NROUTE,NUMCON
   GO TO 1180

C
```

```

C
C *****
C
C          FORMAT  STATEMENTS
C *****
C
C          INPUT
C
C 800 FORMAT(20A4)
C 810 FORMAT(T22, I4, T49, I4, T67, I2)
C 820 FORMAT(I1, T10, I3)
C 830 FORMAT(5I3)
C 840 FORMAT(2I3)
C
C          OUTPUT
C
C 850 FORMAT(1X, T46, 10(1HA), T61, 11(1HR), T77, 11(1HP)/
C      11X, T45, 12(1HA), T61, 12(1HR), T77, 12(1HP)/
C      21X, T45, 'AA', T55, 'AA', T61, 'RR', T71, 'RR', T77, 'PP', T87, 'PP'/
C      31X, T45, 'AA', T55, 'AA', T61, 'RR', T71, 'RR', T77, 'PP', T87, 'PP')
C 860 FORMAT(1X, T45, 'AA', T55, 'AA', T61, 'RR', T71, 'RR', T77, 'PP', T87, 'PP'/
C      11X, T45, 12(1HA), T61, 12(1HR), T77, 12(1HP)/
C      21X, T45, 12(1HA), T61, 11(1HR), T77, 11(1HP)/
C      31X, T45, 'AA', T55, 'AA', T61, 'RR', T67, 'RR', T77, 'PP')
C 870 FORMAT(1X, T45, 'AA', T55, 'AA', T61, 'RR', T68, 'RR', T77, 'PP'/
C      11X, T45, 'AA', T55, 'AA', T61, 'RR', T69, 'RR', T77, 'PP'/
C      21X, T45, 'AA', T55, 'AA', T61, 'RR', T70, 'RR', T77, 'PP'/
C      31X, T45, 'AA', T55, 'AA', T61, 'RR', T71, 'RR', T77, 'PP')
C 880 FORMAT(//1X, T13, 'AUBURN UNIVERSITY ELECTRICAL ENGINEERING DEPARTMENT
C      1NT AUTOMATED ROUTING PROGRAM          VERSION 1          DECEMBER 1977')
C 890 FORMAT(/////////'OBOARD IDENTIFICATION: ', 20A4)
C 900 FORMAT(//'OHORIZONTAL DIMENSION= ', I3, '    VERTICAL DIMENSION= ',
C      I3, '    LAYERS= ', I2)
C 910 FORMAT(//'OCONSTRAINTS: ',
C      11X, T15, 'FRAME EXPANSION FACTOR= ', I1/
C      21X, T15, 'LEVEL EXPANSION LIMIT= ', I3)
C
C 920 FORMAT('1', T45, 10(1H*), 'WIRE LIST OF ', I4, ' CONNECTIONS', 10(1H*)//
C      11X, '#CONNECTION NUMBER-COORDINATES-ORDERING CRITERIA-LAYER PREFERENCE
C      2NCE(IF ANY)')//)
C 930 FORMAT(' ', T2, '#', I4, '-', I3, ',', I3, ' TO ', I3, ',', I3, '-', I3)
C 940 FORMAT(' ', T2, '#', I4, '-', I3, ',', I3, ' TO ', I3, ',', I3, '-', I3,
C      1'-LAYER ', I2)
C 950 FORMAT('+', T45, '#', I4, '-', I3, ',', I3, ' TO ', I3, ',', I3, '-', I3)
C 960 FORMAT('+', T45, '#', I4, '-', I3, ',', I3, ' TO ', I3, ',', I3, '-', I3,
C      1'-LAYER ', I2)
C 970 FORMAT('+', T87, '#', I4, '-', I3, ',', I3, ' TO ', I3, ',', I3, '-', I3)
C 980 FORMAT('+', T87, '#', I4, '-', I3, ',', I3, ' TO ', I3, ',', I3, '-', I3,
C      1'-LAYER ', I2)
C
C 990 FORMAT('1', T50, 10(1H*), 'BLOCKADE COORDINATES', 10(1H*), /)
C 1000 FORMAT(1X, 10(I3, ',', I3, '    '))

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C
1010 FORMAT('1',T51,10(1H*),'LAYER ',I2,' ROUTES',10(1H*))
C
1020 FORMAT(////1X,T57,'NO ROUTES ON THIS LAYER')
C
1030 FORMAT('0#',I4,'*****ERROR*****RETRACTING ERROR IN FINDING PREDECES
1SOR TO CELL ',I3,',',I3/1XT22,'PROCEEDING TO NEXT WIRE LIST PAIR')
C
1040 FORMAT('1',///1X,T10,'*****ERROR*****GRID SIZE TOO SMALL'/
1'0',T10,'DIMENSIONS OF CELMAP ARRAY NEED TO BE INCREASED'/
21X,T10,'(ALSO LIMITER IN STATEMENT THAT GENERATED THIS MESSAGE)')
C
1050 FORMAT('1',///1X,T10,'*****ERROR*****LAYER LIMIT OF 16 EXCEEDED')
C
1060 FORMAT('1',///1X,T10,'*****ERROR*****WIRE LIST TOO LARGE'/
1'0',T10,'DIMENSIONS OF CONECT ARRAY NEED TO BE INCREASED'/
21X,T10,'(ALSO LIMITER IN STATEMENT THAT GENERATED THIS MESSAGE)')
C
1070 FORMAT('0#',I4,'-EXPANSION INVOLVED TOO MANY CELLS-WILL TRY TO ROU
1TE ON REMAINING LAYERS'/
21X,T8,'(OR INCREASE DIMENSIONS OF OUTCEL ARRAY AND LIMITER IN STAT
3EMENT THAT GENERATED THIS MESSAGE)')
C
1080 FORMAT('0#',I4,'-EXPANSION INVOLVED TOO MANY CELLS-WILL TRY TO ROU
1TE ON REMAINING LAYERS'/
21X,T8,'(OR INCREASE DIMENSIONS OF NEWCEL ARRAY AND LIMITER IN STAT
3EMENT THAT GENERATED THIS MESSAGE)')
C
1090 FORMAT('0#',I4,'-PATH LENGTH TOO LONG-WILL TRY TO ROUTE ON REMAINI
1NG LAYERS'/
21X,T8,'(OR INCREASE DIMENSIONS OF PATH ARRAY AND LIMITER IN STATEM
3ENT THAT GENERATED THIS MESSAGE)')
C
1100 FORMAT('0#',I4,'-UNABLE TO FIND A PATH ON THIS LAYER')
C
1110 FORMAT('0#',I4,'-THE PATH BETWEEN CELLS ',I3,',',I3,' AND ',I3,
1',',I3,' CONSISTS OF CELLS:')
1120 FORMAT(1X,I3,',',I3)
C
1130 FORMAT('1',T43,10(1H*),'LIST OF CONNECTIONS NOT ROUTED',10(1H*)//)
1140 FORMAT(' #',I4)
1150 FORMAT(1X,T57,'ALL CONNECTIONS ROUTED')
C
1160 FORMAT('1'////////1X,T49,10(1H*),'ROUTING COMPLETED',10(1H*))
1170 FORMAT(///1X,T50,I4,' OUT OF ',I4,' CONNECTIONS ROUTED')
C
C
C*****
C
C
1180 CONTINUE
WRITE(6,1190)
1190 FORMAT('1')
END

```