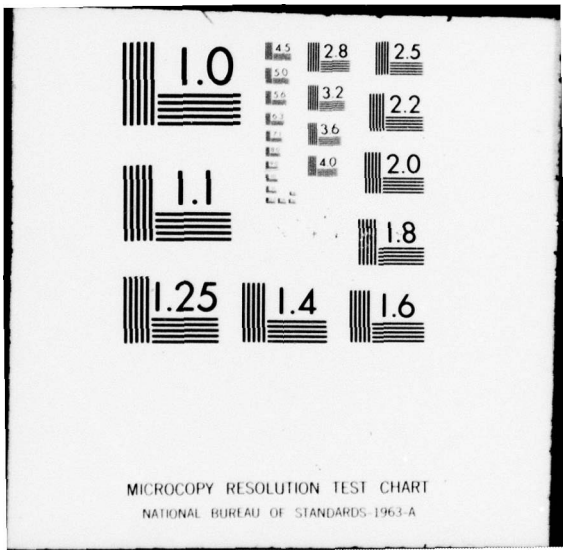
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1. INTRODUCTION

This final report covers the analysis, investigation, conclusions and recommendations of the study for the Modular Electronics Packaging program, performed by the Aerospace Electronic Systems Department, General Electric Company, Utica, New York, under Contract N00163-77-C-0295. The study was performed for the Naval Avionics Facility, Indianapolis (NAFI).

The period of performance of this program was unusually brief. As a result, the trade-off analyses and investigations are necessarily limited in depth. The technical investigations were carried forward in sufficient depth to allow the basic packaging concepts to be firmly established. Areas requiring further investigation or development have been identified.

In accordance with the contract terms, the packaging concepts were evaluated in respect to their ability to meet the requirements of MIL-E-5400. The V/STOL Type A platform was used as the driving requirement to evaluate system level considerations (e.g., installed weight, volume, etc.).

2. EXECUTIVE SUMMARY

2.1 Objectives

In considering Modular Avionics Packaging, the objective of the General Electric study program was to develop an avionics equipment packaging concept, compatible with MIL-E-5400, and applicable to multiplatform avionics requirements stretching into the 1990's.

Specific elements evaluated were: Standard Avionics Module (SAM) requirements and concepts; integrated racks and WRA requirements and concepts; and airframe interface considerations. The V/STOL Type A platform was used as the driving requirement in performing trade-off studies.

Key design objectives and constraints included the following:

- Minimizing installed avionics weight and volume,
- Mechanical simplicity,
- Significant improvement in Reliability and Maintainability,
- Eliminating single-point failure modes,
- Direct access to Weapons Replaceable Modules (WRM),
- Modules capable of being conduction-cooled,
- Significant improvement in thermal performance, and
- Improved testability at all hardware levels.

2.2 Approach

The General Electric Company has performed internally-funded V/STOL system analyses: this background, and extensive system and equipment design and production experience were applied to formulate a Modular Avionics Packaging concept, from the perspective of total systems performance optimization. Additional visibility into airframe interface considerations was provided by McDonnell-Douglas, Vought, and Lockheed. Similarly, information concerning Environmental Control Systems (ECS) was provided by five ECS manufacturers. Two companies (Airesearch and Sundstrand) performed specific trade-off studies at General Electric's request.

The V/STOL preliminary system architecture (used in the General Electric response to the V/STOL RFQ/I) was the basis for partitioning studies. Subsystems, and eventually lower-level "natural functions," were identified, independent of any constraint of module size. These natural functions were subsequently characterized in terms of power, connector pins,

and surface mounting area, based on a projection of 1982-1985 integrated-circuit technology.

The projection of integrated-circuit technical progress and achievement is admittedly conservative. The factors influencing this position were:

1) VLSI, capable of meeting military requirements, will lag commercial-grade VLSI by about two years.

2) NMOS, considered to be the leading VLSI technology, is least desirable from a radiation-hardening standpoint. NMOS is consequently less suitable for military equipment.

3) Bipolar technologies, more adaptable to radiation hardening, will not achieve the high gate-densities projected for NMOS.

4) Over-optimistic projections might not be technically fulfilled. Aircraft weight and time-on-station, equipment reliability, and ECS design could all be adversely affected by such an error.

The primary requirements for modules were found to be:

Power	-	20 watts max
Area	-	approximately 12 square inches
Connectors	-	100 pins minimum 125 pins, best estimate

These characteristics were used to investigate module configuration concepts. Various module cooling concepts were considered. Among the alternatives were:

- Conduction
- Liquid
- Heat pipes
- Heat exchanger -- internal flow-thru
- Heat exchanger -- external (fin mounted)
- Direct air cooling

Integrated Rack concepts included a variety of approaches providing intermediate and direct access to modules. Rack cooling schemes included conduction and convection methods; connector concepts considered were: conventional technology, ZIF (Zero-Insertion-Force), and LIF (Low Insertion Force) approaches.

The form factor, rack volume and ECS trade-offs associated with high-performance fighter aircraft will probably preclude the use of integrated racks on this type platform. The standard avionic module and WRA concept does however meet this need. The use of integrated racks is compatible with lower performance land and carrier-based platforms (e.g., VSTOL Type A) associated with ASW, AEW and MA missions. These platforms still offer significant performance challenges in the areas of weight and volume, but allow an added degree of flexibility in optimizing the packaging form factor.

The high performance aircraft often relies on ram air as a key element in the thermal system design. AEW, ASW and cargo/transport type aircraft allow flexibility for more innovative ECS and equipment cooling system approaches. The integrated rack concept developed for a V/STOL Type A platform is an innovative approach, incorporating the preferred MIL-STD-454E cooling concept -- direct forced-air cooling. The proposed concept circumvents contamination problems previously encountered on high performance fighter aircraft, and contributes to significantly improved avionics reliability.

2.3 Conclusions

2.3.1 Airframe

The results of this study were reviewed by both McDonnell-Douglas and Vought. The recommended concepts were found to be compatible with current and projected V/STOL Type A airframe developments.

The principal areas of concern for airframe manufacturers were:

- Number of integrated racks
- Orientation of racks in the aircraft
- Primary electrical system
- Recommended ECS approach
- Integrated rack/ECS interface

Specific conclusions relating to the airframe are:

- Airframe concepts are still sufficiently flexible to accommodate a wide range of integrated-rack approaches.
- Integrated racks should be mounted to the airframe, rather than be an integral part of it.
- Airframe use of composite materials requires extra attention to avionics EMI and EMP design and installation.

- Electrical System Baseline - 270 VDC SOSTEL system necessary to enhance power supply designs.

- Environmental Control System:

1) Freon Vapor-Cycle Central ECS for cooling electronics systems offers highest coefficient of performance (typically three times that of air-cycle).

2) Weight of air-cycle and of vapor-compression-cycle equipment approach each other if engine-bleed air is not used.

3) Air-cycle offers best cabin ECS. A liquid loop between the ECS and the integrated racks is preferable to either air or Freon loop for efficiency and reliability/maintenance.

The proposed MAP concept reduces the installed weight of candidate equipment (excluding displays, transmitter, etc.) to approximately one-third of the weight of comparable S-3A avionics (gross take-off weight reduced by over 3000 lbs.).

2.3.2 Integrated Rack and WRA

The integrated rack preliminary mechanical concept is primarily influenced by:

- Requirement for significantly improved reliability and maintainability

- Projected EMI/EMP environment

The baseline equipment concept is a structure enclosed in an aluminum shell, with EMI-gasketed doors. Modules are cooled by direct forced-air convection cooling, from a closed-loop system of filtered, dehumidified air. The rack offers direct module access, front-removable back panels, and front-mounted cabling. This approach permits:

1) Significantly reduced junction temperatures (+85°C max for V/STOL).

2) Minimized humidity and thermal-cycling-related failure modes.

3) Minimum MTTR, through mechanical simplicity.

A Zero Insertion Force (ZIF) rack concept was also developed and evaluated. ZIF concepts are more complex mechanically, with poorer conduction-cooling characteristics. A survey of 22 connector manufacturers revealed that there is no strong push for commercial usage of ZIF connectors. Without such a market, a ZIF concept is considered too high a risk to warrant further development as a NAVAIR approach. A Low Insertion Force (LIF) concept is feasible and is recommended.

Specific conclusions relating to the integrated rack are:

- The Integrated Rack approach is lighter than traditional WRA packaging (e.g., V/STOL: 454 lbs vs. 593 lbs).

- The Integrated Rack facilitates optimum subsystem partitioning.

- Subsystem back panels: wire wrap or multilayer board; technology on hand.

- Back panel producibility constraints are important to efficient subsystem definitions.

- EMI/EMP requirements are very significant factors in integrated rack material selection and design.

- Fiber optics should be used for interconnect whenever possible for weight and EMI/EMP advantages.

- Power supplies will require up to 50 percent of avionics module volume, and 40 percent of the weight.

- Power-supply packaging density requires an improvement of 2 to 3 over that generally available today (6 to 9 watts/in.^{3}).

- Direct air cooling of modules, using closed-cycle conditioned air within an integrated rack, offers best thermal performance. It is also capable of operating in a degraded mode, avoiding system single-point failure modes.

- The proposed direct-air-cooling scheme is in full compliance with applicable specifications: it is the preferred MIL-STD-454E approach.

- A liquid cold plate conduction-cooled rack offers a 40 percent volume advantage (considering the same number of racks) without a weight penalty, but the liquid cold plate conduction-cooled rack has ECS sirgle-point system failure modes.

2.3.3 Standard Avionics Modules

Alternate configurations for SAM were considered; in selecting one approach, the most significant objective is to develop a concept which is sufficiently flexible. The module chosen should accommodate the full range of anticipated requirements and technology. The concept must be thermally compatible with future Navy air platforms, as well as with existing platforms whose service life is projected well into the 1990's. It also assumes that the SAM approach will be used in the development of new avionics subsystems for retrofit into existing aircraft (e.g., P-3C). To meet the full spectrum of anticipated usage, the SAM concept adopted must be compatible with MIL-E-5400, using convection (direct forced-air) cooling, or

conduction-cooling. SAM could then meet unit, subsystem, system and aircraft ECS constraints.

With these restrictions, the current Improved - 2A (I-2A) module will not meet the projected power dissipation figures in a conduction-cooled mode. The SAM-compatible I-2B module will meet the projected power and connector-pin requirements, but its use incurs a weight penalty, and requires the use of a greater number of integrated racks. Comparison of a 3/8 ATR (HI-2A) approach and the I-2A is shown in Figure 3.4-14.

If applications of SAM could be restricted to equipment situations with direct forced-air (convection) cooling, the I-2A module offers the best weight-and-volume compromise (even though the number of racks are the same) for V/STOL. The assessment, however, ignores the potential chip-carrier packaging incompatibility, and potential Input/Output connector pin limitations.

An alternate conduction-cooling approach, using the I-2A, involves removing heat conductively from the top face of the module. This approach was not quantitatively evaluated in the study for the following reasons:

1) Loss of this cooling path when a rack door or WRA cover is removed for an indefinite period associated with maintenance is a potential reliability risk.

2) Very close tolerances required in manufacturing the module and rack (WRA), together with increased mechanical complexity, are incompatible with the MAP goals: low maintenance requirement, easy producibility, lowered development and production costs.

3) Tolerance buildup problems associated with the integrated rack frame, back panels, modules and door are, at best, difficult to control.

4) Designs which involve spring-loading the module to force it against a door or plate must supply sufficient force to overcome worst-case connector insertion forces. Meeting this requirement might will result in prohibitively high forces being needed to close the door.

Specific conclusions relating to module level are:

- Chip carriers will replace Dual In-line packages (DIP) as the packaging standard (1985).

- By 1984-1985, VLSI will not be sufficiently mature for general military requirement use. Available commercial technology, with the possible exception of memories, will not be suitable.

- Test/testability problems now being experienced with LSI may be compounded by VLSI.

- JEDEC-proposed standards for LSI chip carrier footprints, for packages with more than 84 pins (on 0.050 inch centers), or 100 pins (on 0.040 inch centers), will not fit on an Improved - 2A substrate.

- JEDEC-proposed LSI package heights may very well preclude a two-substrate module on 0.4 inch centers.

- The majority of functions should therefore be implemented with a one-substrate approach compatible with the proposed JEDEC chip-carrier standard.

- Strong DOD lobbying should be initiated to minimize the potential size penalty of the proposed chip-carrier standards.

- SAM should be designed to be either conduction- or convection-cooled (T_j = 125°C maximum, 110°C goal).

- Thermal system should be optimized for 85°C worst-case junction temperatures for reliability and controlled life-cycle costs.

- Module power dissipation capability is the driving SAM requirement (10 watts typical, up to 20 watts maximum).

- Standard Improved - 2A is thermally limited in a conduction-cooled application.

- Improved - 2B implementation has weight and volume limitations, but meets thermal and Input/Output pin requirements.

- A higher Improved - 2A (HI-2A) or 3/8 ATR yields a thermally acceptable system with minimum volume, weight, complexity and cost.

- New connector development should be considered for SAM (LIF type, 120-130 pins, 0.3 inch pitch).

2.4 Recommendations

- Further ECS trade-off studies are required by ECS specialists.

- SAM design characteristics should be refined and evaluated in FY 1978-1979.

- Integrated Rack concept refinement studies will be required in FY 1978; hardware concept evaluation in FY 1979.

- See Section 3.9 for detail MAP development planning.

- Fund power supply development activities to achieve higher power densities (e.g., 7.5 to 9.0 watts per cubic inch).

- Investigate and develop preferred connector approach.

- MAP concepts and baseline should become part of V/STOL system concept definition efforts.

3. TECHNICAL DISCUSSION

3.1 Integrated Circuit (IC) Technology Assessment

3.1.1 1985-1990 Integrated Circuit Technology Projections

3.1.1.1 Introduction

Forecasting developments in Integrated Circuit technology several years into the future is a difficult task. A forecast extending to 1990 is doubly risky. Predictions in the 1960 era, when U.S. military research and development tended to set the direction of progress, could be made with some confidence. Present-day forecasts, however, must consider the civilian/commercial influence on the marketplace as the driving force.

The environmental and electrical requirements for military equipment are markedly different (usually more severe) from those required for civilian goods. The differences may adversely affect possible military use of some of the leading commercial-developed technologies (e.g., charge-coupled devices). This report will summarize conclusions reached in a study of the probable directions of progress for each integrated-circuit technology, and will consider how developments may affect military and commerical use. The complete study is appended to this report as Appendix A.

3.1.1.2 Japanese VLSI

In considering the widely-publicized Japanese VLSI program, this report takes a conservative viewpoint. Other factors -- radiation hardness, military temperature ranges, and the lag between enthusiastic commercial announcement and qualified devices -- have moderated the estimate of Japanese goals.

3.1.1.3 Size: Smaller and Smaller

Submicron technology will certainly grow in importance for military applications. Improvements in reliability, size and performance will make a one-chip submicron system superior to 20 to 30 present LSI devices it will replace.

3.1.1.4 Special IC Technologies

Military systems, while riding on civilian market developments, and using many standard commercial devices, still have unique requirements. Combinations of extremely small size, very low power, capability to process analog data, and radiation resistance can often be met only by devices which are specifically designed for the application. Special IC technologies will be required to supplement the commercial IC products.

Of the special-performance technologies, CMOS/SOS, I^2L, and CCD are the most promising. Each is the solution to at least one problem: CMOS/SOS

operates at very low power, and has inherent radiation tolerance. I^2L can be made to perform analog and digital functions on the same chip, and seems capable of some radiation-hardening. CCD can perform analog data processing and seems suitable for high-density logic.

Special performance IC technology five to ten years hence should be paced by GaAs (gallium arsenide) devices now under development. These promise digital system frequencies around 10 gigahertz. Possible uses of the GaAs technology are SFET (Schottky Field-Effect Transistors) and TED (Transferred-Electron Devices). All of these special devices seem destined to special military use, without great commercial market impact.

3.1.2 Integrated Circuit Radiation Hardening Considerations

NMOS will probably be the leading future commercial technology. NMOS, however, will not satisfy requirements for military systems requiring radiation hardness capability. Three forms of radiation are of concern when discussing device vulnerability: neutron fluence, total dose, and transient upset.

NMOS is extremely susceptible in total dose and transient upset. NMOS gate-threshold levels are changed radically by radiation: the smaller dimensions of future devices will make them even more susceptible. RAD-hardened systems will not take advantage of NMOS VLSI development. Systems requiring radiation hardening will have to rely heavily on T^2L, I^2L and CMOS/SOS devices.

3.1.3 VLSI Device Specification and Testing

The more complex the devices (e.g., VLSI) become, the more difficult it is to generate procurement and test specifications. As devices approach minicomputer and mainframe capabilities, procurement documentation and testing will rely heavily on software programs. Much study is needed to define the problem clearly, and to develop solutions.

3.1.4 Integrated Circuit Packaging

Future LSI devices almost certainly will require more than 100 pins/package. Package manufacturers, IC manufacturers, and the manufacturers of new equipment now have renewed interest in device packaging. A summary of package advantages and disadvantages is given in Table 3.1-1.

Of the package forms available, the most likely candidate for industry-wide acceptance is the leadless chip carrier. The package is rugged, without protruding leads, uses little PWB space, has good thermal properties and is lower in cost than a DIP. Further discussion on the chip carrier is in Appendix A.

Table 3.1-1 Integrated Circuit Package Comparisons

Monolithic Die (Chip) Packaging Alternatives	Disadvantages	Advantages
Leadless chip carrier	• Solder joint stress due to board expansion • Solder-reliability, producibility repairability unknown?	Excellent packing density Durable Easy handling Pluggable Package price low
Flatpack or leaded chip carrier	• Difficult handling for, testing shipping, assembling • Not optimum size • Lead forming (for leaded CC) • Poor pluggability	Package (excluding leads) More durable than large DIP Better packing density than DIP Package price lower than DIP (large packages)
DIP	• Package size and durability (length) fragile ceramic • High cost	Pluggable
Beam tape (encapsulated) or solder bump	• Die seal • Heat removal from chip • Handling • Poor pluggability • Pin spacing	Optimum packing density

3.1.4.1 The Chip Carrier - A Future Industry Standard

Because of the noted advantages, it seems most likely that industrial/commercial devices will adopt the chip carrier as a standard.

A JEDEC panel has been formed to establish standard pin configurations for chip carriers. Two standards have been proposed: a 0.050-inch lead center, and a 0.040-inch lead center as shown in Table 3.1-2.

Table 3.1-2. Proposed Chip Carrier Lead Spacing

Commercial Standard -- 0.050 Inch Lead Spacing

No. of Pins	Size
28	0.450 inch on a side
44	0.650
52	0.750
68	0.950
84	1.150
100	1.135
124	1.165
156	2.050

Military High Density Application Standard -- 0.040 Inch Lead Spacing

No. of Pins	Size
40	0.480
48	0.560
64	0.720
80	0.880
96	1.040

LSI, coming strongly on the commercial scene, will require larger-than-reasonable packages, if manufactured as DIP. Evolving ceramic substrate technology, together with processes compatible with chip-carriers, will cause an industry trend: the chip carrier should be the industry standard by 1990. Existing blank pricing will boost the change. The chip carrier basic package is four times less expensive than an equivalent ceramic DIP.

Chip carrier device pricing in the 1985 time frame will still be slightly higher than DIP's, as suppliers attempt to recover investment cost. By 1990, the cost of a chip-carrier device will be well below the equivalent DIP.

3.1.5 Conclusions

This IC technology assessment has shown that by conservative assessment, by 1980 the commercial market can supply 65K dynamic RAMS, 16K static RAMS, and single-chip 16-bit minicomputers. By 1982, the packaging and processes will accommodate military requirements. These devices will push the upper limit of existing optical manufacturing processes.

When E-beam and X-ray processing begins commercial production, VLSI devices will begin to be available -- probably about 1985. Products such million-bit commercial-grade memories, and single-chip 32-bit minicomputers with quarter-million bit memories will emerge and be commercially available by 1987.

This conservative projection takes into account use of existing optical fabrication processes up to their physical limits, with a reasonable return on investment. Moderate phasing-in of E-beam and X-ray technologies is forecast for 1980.

A more liberal opinion, based on Japanese technological goals, would move E-beam processing up several years, with million-bit memories by 1980. This assumes uninterrupted technical progress: unknowns, in conservative opinion, will make the process considerably longer.

3.2 System Application Considerations

The Engineering Development phase of V/STOL avionics design will begin in 1985. Modular Avionics Packaging (MAP) efforts performed now for V/STOL systems must apply to the design time frame. The applicability of present MAP efforts depends heavily upon the definition of avionics functions, the validity of present definitions at the time of design, and the accuracy with which related technology developments have been forecast.

System functions for Aircraft Early Warning (AEW) and Anti-Submarine Warfare (ASW) avionics have been defined. A projection of probable 1985 technology in microelectronics has been accomplished (Section 3.1 and Appendix A). Using these studies, partitioning of the aircraft systems to the module level has been accomplished. Special care has been taken to partition into specific functions, so that this functional integrity may be transferred into new-technology hardware as it becomes available.

Physical requirements have been defined for packaging the avionics in modules which represent complete testable functions. Systems may therefore be developed using near-term technology; in 1985, the functions of the initial design may be translated into advanced technology on a one-for-one basis, without repartitioning.

Consideration has also been given to including every applicable avionics function currently needed for the AEW and ASW missions of the V/STOL. From this analysis, selection of functional modules as standards may be made, and the preliminary physical design proved.

3.2.1 System Partitioning

System partitioning efforts performed for this study started from the concept for V/STOL Avionics Systems presented in the General Electric response to V/STOL RFQ (May 1977). That preliminary system definition embodied partitioning by mission requirements. It classified avionics into three categories: (1) Core Avionics -- equipment required for all mission variants; (2) Mission Common Avionics -- those elements which are required for more than one, but not all variants; (3) Mission Unique Avionics -- those necessary for a single variant. (See Figure 3.2-1.)

The system architecture is one which allows the configuration of each mission variant to be a totally integrated avionics suite, while preserving commonality wherever subsystem and module requirements coincide. The system architecture results in "natural" functionally-bounded subsystems which are relatively independent and readily definable.

Partitioning efforts for this study addressed the two most complex variants, the ASW and the AEW systems. Each of these variants was defined as a set of "Core" avionics, plus the additional avionics required to implement the total system. In estimating subsystem and module requirements, the Flight Control avionics were included, but because of vulnerability considerations, they were assumed to be packaged in somewhat smaller

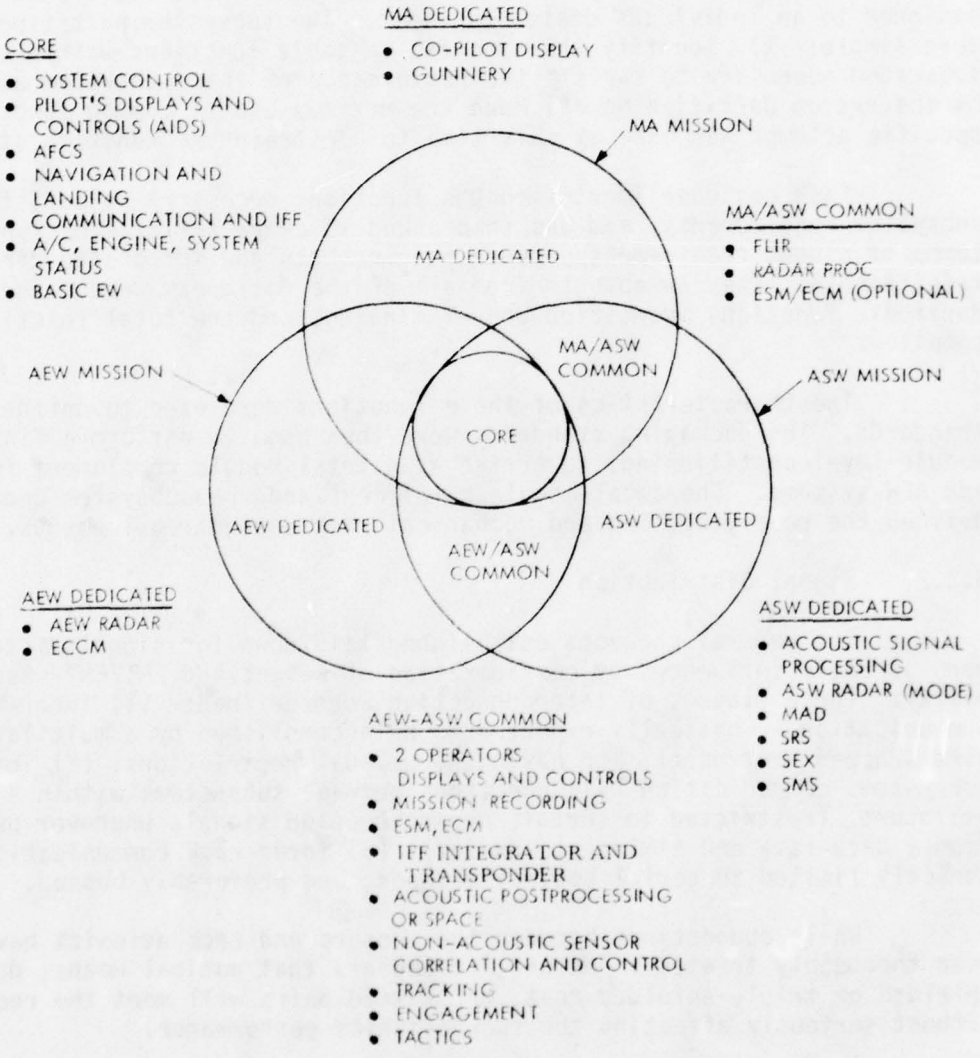


Figure 3.2-1. Common/Core Avionics Concept for V/STOL

assemblies, separate from the rest of the avionics, and perhaps protected from battle damage to some extent.

The intent was to define the total avionics system, the greatest part of which would employ standard modules, and be packaged within integrated racks. The module-and-rack design will provide ready access for maintenance purposes.

3.2.1.1 Subsystem Partitioning

The responsibility for partitioning within each subsystem was assigned to an individual design engineer. The subsystem partitioning rules were simple: 1) Identify the specific testable functions within each subsystem necessary to satisfy the performance of that subsystem as defined by the system partitioning; 2) Make the maximum use of common functions. No specific attempt was made at this time to constrain the function size.

Each designer identified the functions necessary to satisfy the subsystem requirements, and was then asked to characterize each function in terms of pinout requirements, power requirements and integrated circuit requirements. The raw outputs from all of the designers were correlated, duplicate functions identified and eliminated, and the total function list compiled.

The characteristics of these functions were used to define packaging standards. The packaging standards were then used to perform a final module-level partitioning, to arrive at a total module complement for the ASW and AEW systems. The total module complement and the subsystem groupings defined the power, cooling and mechanical rack design requirements.

3.2.2 Signal Distribution

The general concepts established laid down for signal distribution were strongly influenced by consideration of weight and EMI/EMP susceptibility. Three classes of interconnection were defined: (1) inter-module communication -- basically expected to be accomplished by a multilayer or wire-wrapped back panel, and having no unusual restrictions; (2) inter-subsystems communication -- connections between subsystems within a rack enclosure, (restricted to serial, non-dc-coupled signals whenever practical from a data-rate and timing standpoint); (3) inter-rack communications -- strictly limited to serial optical methods, and preferably bussed.

While connections between the sensors and rack avionics have not been thoroughly treated in detail, it appears that optical means, double-shielded or triple-shielded coax, or twisted pairs will meet the requirements without seriously affecting the rack avionics performance.

V/STOL EMI, EMP and weight requirements strongly indicate the value of using fiber-optic communication mechanisms in V/STOL systems.

3.2.2.1 Fiber Optics

Fiber-optics communication systems are broadly divided into two classes: (1) the fiber-optic "links" for interconnecting single information sources (transmitter) to a single terminations (receiver); (2) the fiber-optic "bus" which utilizes a common fiber-optic trunk line, by which a number of transmitter/receiver terminals can be interconnected. The fiber-optic system is further characterized by its intended use, as digital or analog. Additional subdivision includes a "full-duplex" system that provides simultaneous transmission and reception on two different busses; in contrast to a "half-duplex" system which can transmit or receive on any single bus at any time, but cannot do both simultaneously.

Multiplexing of information on a communication bus can be achieved by four distinctly different methods and their combinations:

(1) Space division multiplexing: the separation of communication channels on physically separate optical fibers (or bundles).

(2) Wavelength multiplexing: provides for multiple transmission on a single fiber by modulating optical sources (lasers or photodiodes), doped to provide optical radiation at selected wavelengths, and color-filtered optical detectors for wavelength selection.

(3) Frequency multiplexing: subdivides the very large bandwidth capability of fiber optics into a number of smaller, bandwidth-limited channels on subcarriers for transmission. Tuned bandpass receivers provide the required selectivity to discriminate against the undesired channels.

(4) Directional multiplexing: uses fiber-optic directional couplers that provide high directivity for discriminating against other optical signals operating on the same fiber, wavelength, and frequency, with negligible crosstalk, according to the direction of the optical signal.

A1. Bus Fan-Out Methods

The fan-out of the optical signals among the multiple transmitters and receivers which make up a fiber-optics bus may be accomplished by a "Tee Coupler" or a "Star Coupler," depending upon the system needs and the available interconnect loss budgets. The Tee Coupler is used where the number of system drops are small and widely separated, and relatively large insertion losses can be tolerated. (See Figure 3.2-2.) The Star Coupler has a common distribution center: because of fewer series connectors, it presents a lower overhead loss (See Figure 3.2-3).

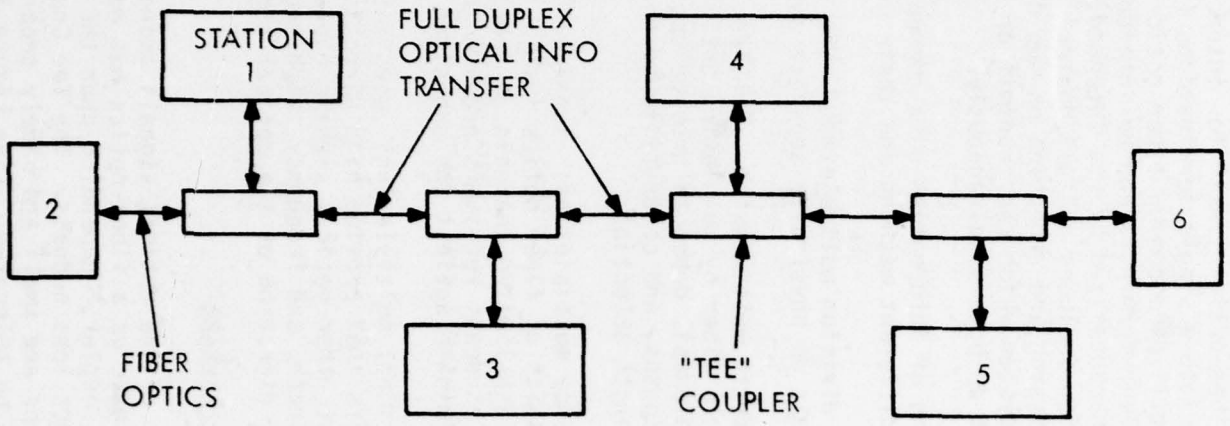


Figure 3.2-2. "Tee" System Configuration, Bus Methods

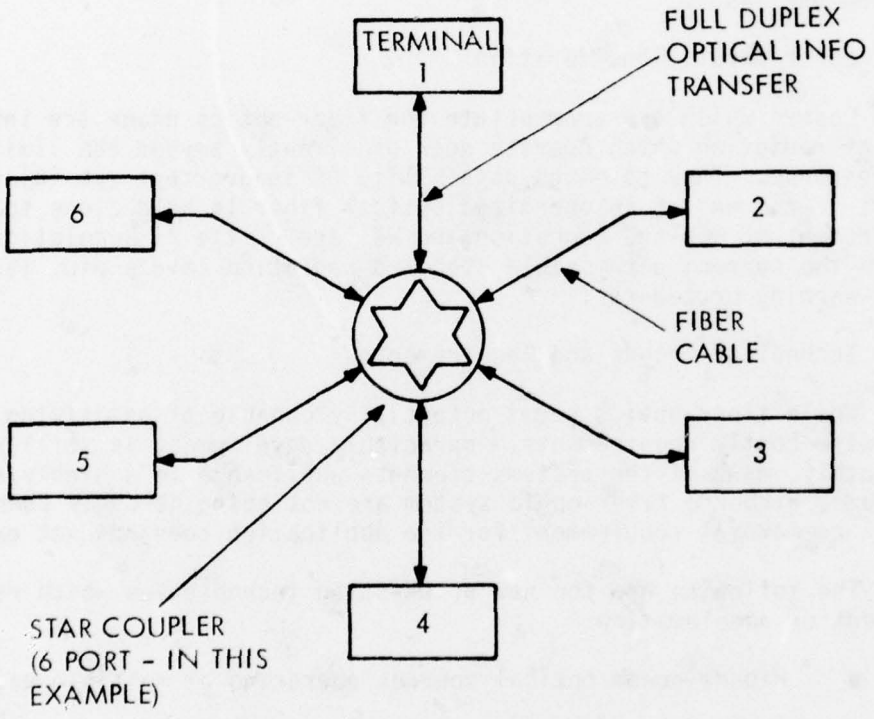


Figure 3.2-3. Star System Configuration, Bus Methods

A2. Representative System Configuration

The analog fiber-optic bus currently under consideration for the Advance Development Model of the Advanced Integrated Display System (AIDS) is shown in Figure 3.2-4. Both wavelength and frequency division multiplexing is achieved by the simultaneous use of two optical wavelengths, between 0.8 and 0.85 um, and intensity-modulating the laser sources with nine frequency-division-multiplexed signals between 125 MHz and 250 MHz. Two radio-frequency channels modulate a common laser. The optical powers of each laser are combined in a star coupler. The two rf carrier frequencies are selected so that no in-band intermodulation distortion (IMD) components are generated by the common lasers optoelectronic non-linearities. Compensation methods, such as quasi-feed forward, are necessary for IMD when active repeaters or a number of frequency-division-multiplexed (FDM) electrical signals are modulating one laser.

A3. Laser Safety Consideration

Lasers which are appropriate for fiber-optics usage are intense sources of radiation which operate near or slightly beyond the limits of visual response. They pose the possibility of inadvertent eye injury (lesions) if the end of an energized optical fiber is held close to the eye. The Department of Health, Education and Welfare, Title 21 Regulations, establish the current permissible standard radiation levels plus labeling and acoustic-warning procedures.

A4. Technology Trends and Requirements

While fiber-optics seems potentially capable of satisfying a variety of otherwise costly requirements, appreciable development is still required. Unfortunately, many of the systems elements applicable to a highly reliable, high volume, airborne fiber-optic system are not being strongly pursued, because a commercial requirement for the application does not yet exist.

The following are the new or existing technologies which require development or acceleration:

- Higher power optical sources operating at multiple wavelengths
- Cost-effective low-loss star couplers
- Cost-effective connectors
- Microelectronic FDM modules
- Increased radiation-hardened fiber-optics
- Fiber-optic back planes

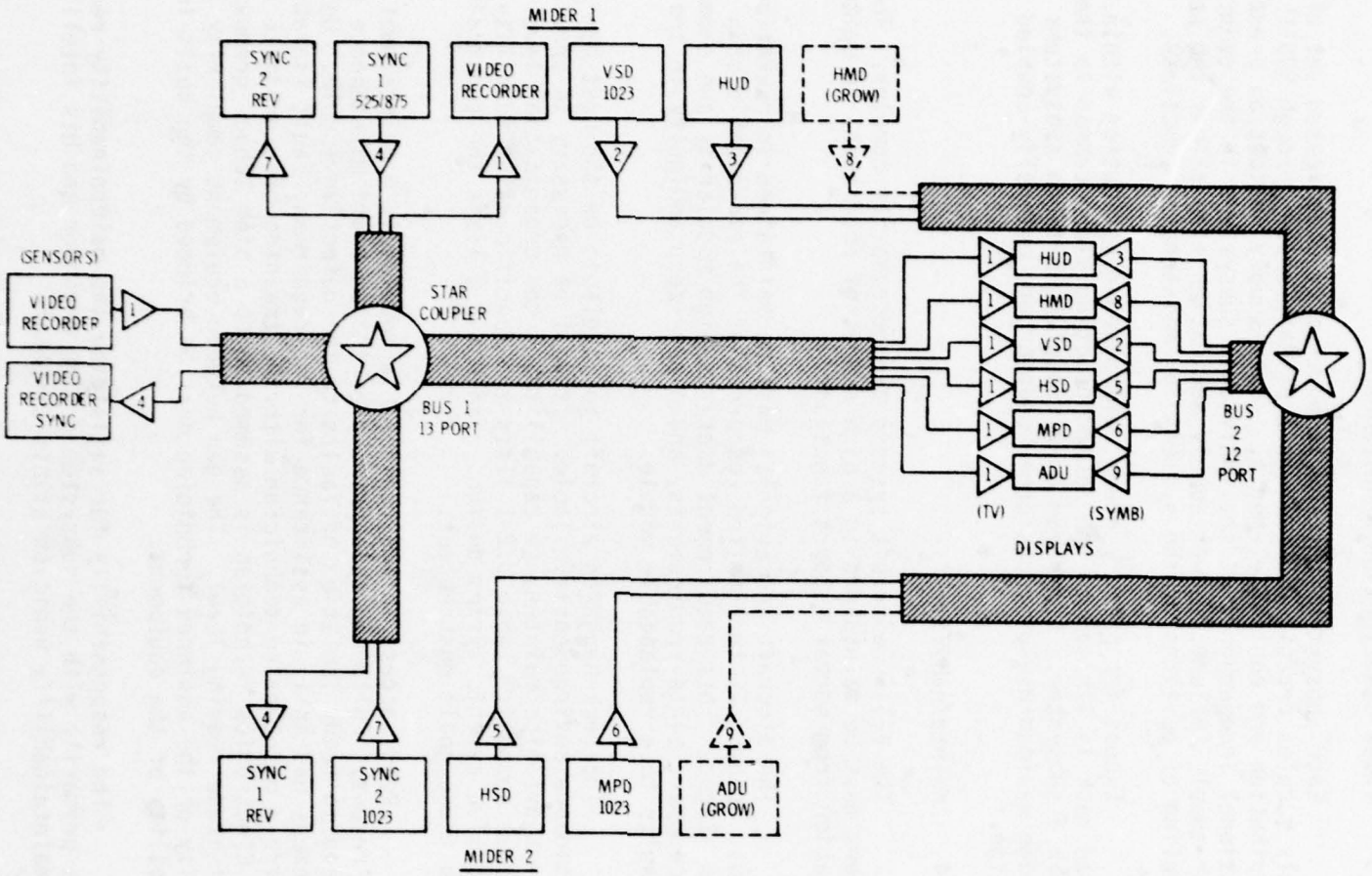


Figure 3.2-4. AIDS-ADM Fiber Optics Bus, Block Diagram

3.2.3 Power Distribution Requirements

Each subsystem function is powered by a dedicated set of power-supply modules energized by aircraft primary power through SOSTEL power distribution and control elements. Power-supply dedication preserves the functional independence of the individual subsystems in the event of a power-supply failure. Power-supply dedication also allows the selective disabling of portions of the systems for maintenance functions.

Except for primary power, all power distribution within the integrated rack is limited to the interconnecting plane common to the modules within a subsystem. A minimum of dc coupling between subsystems is achieved through maximum use of transformer-coupled and optically-coupled transmission.

3.2.4 Maintainability

The V/STOL aircraft systems are necessarily complex. These complex systems must be maintained in a high degree of readiness, in spite of unique isolation from normal support functions.

The aircraft and avionics must be maintained in operationally-ready status, using only the limited resources of the air-capable ship from which it is staged. This requirement dictates high modularity and commonality to reduce spare parts requirements, and a near-zero ambiguity in the isolation of faults to a replaceable module.

The deck-hangared aircraft is likely to be the most benign avionics maintenance environment available. It will be necessary to provide a 100 percent avionics maintenance capability at the organization level, without external support. Table 3.2-1 lists the specific maintainability goals of the V/STOL avionic system design. Table 3.2-2 lists the constraints under which those goals must be met.

Ready access to all replaceable modules is a maintainability requirement. Following this principle, the on-board maintenance concept is reduced to ready isolation of faults to the defective module. Unless the equipment had built-in assistance for the repairman, fault isolation would require a maintenance technician with the training of a graduate engineer. A Navy Electronics Technician is assumed to be a high school graduate, with an eight-grade reading level. The gap between equipment complexity and the ability of the assigned technician must be bridged by the built-in test capability of the equipment.

The responsibility for satisfying the maintainability requirements rests primarily with the subsystem design engineer and his intelligent use of the maintainability vehicles at his disposal.

The distributed nature of the system offers an inherent plus to the designer. There is very little of the system which is not accessible to one or more of the microcomputers distributed throughout. Each microcomputer can

Table 3.2-1. Maintainability Goals -- V/STOL Avionics

- Organizational Level Replacement of Lowest Level Replaceable Assembly-WRM (Weapon Replaceable Module)
- In-Flight Performance Monitor to Assess Operational Capability to Aid in Degraded Mode Selection
- Automatic Fault Isolation to One WRM in 98 percent of Failures - Simple-to-Perform Isolation
- Ready Access to Every WRM
  Reduction in MTTR and MMH
  Shorter Turnaround Time
  Greater Commonality of Modules
  Throwaway Modules
- Functional and Test Partitioning of System
  Complete Function or Subfunction on One Module

Table 3.2-2. Maintainability Constraints - V/STOL Avionics

- No Intermediate-Level Maintenance Activity
- No Carry-on Test Equipment
- No Test Points
- No Special Tools
- No Adjustment/Alignment After WRM Replacement
- No Dedicated Maintenance Station
- 150% Maximum Test Dedicated Hardware
- Maintenance by One Technician

be assigned the test responsibility for those modules under its direct control.

Full maintenance use of the distributed microcomputers is dependent upon an external test capability being designed into the interfacing modules accessible at the normal microcomputer interface.

Functional partitioning at the sub-system and module level is the key to non-ambiguous fault isolation. Coincidence of module and functional interfaces implies that individual pecularities of function implementation need not enter into the fault-isolation problem. The signals may be tested in their pure form, that is without the addition of any special test circuitry. Most single-port functions such as memories and arithmetic operators fall in this category. On the other hand, depending on its function and its placement within the systems architecture, a module may be singularly untestable without either extensive test mode circuitry built-in or by the inclusion of a special test module. Still others may be diagnosable only through deduction based on the performance of a closely-coupled group of modules.

A fault-location capability as thorough as that required for V/STOL will make use of all available methods. Table 3.2-3 compares the attributes of various methods of fault isolation.

3.2.4.1 Software Controlled Tests

The case for fault isolation and detection of fault through software controlled tests is presented below. No attempt is made here to analyze the system when the software controlled tests are used in conjunction with BITE. The case was analyzed for software fault-detection only. (See Table 3.2-4.)

In-Flight Performance Monitoring (IFPM) is fault detection and location at a higher level than that required preparatory to a repair action. The purpose of IFPM is to allow a tactical operator accurately to assess the conditions of his avionics, to the extent that any failure can be related to the loss of a particular mission function. With this assessment, the operator can determine the availability of degraded-mode operation or the possibility of selective reconfiguration to enhance the probability of mission success.

3.2.4.2 Technology Improvements Required

Extensive use of LSI devices will be absolutely necessary in order to meet the weight and volume requirements of V/STOL. LSI presents a unique BITE situation, since through proper apportioning and partitioning of chip functions, the LSI chip can possibly test itself with a minimum of outside support.

Table 3.2-3. Built-In Test Equipment (BITE), Fault Location Attributes

	BITE on Circuit Module	BITE on Separate Module
1.	Implementation	
a.	BITE is integral to module	a. BITE connected thru wiring to modules being tested.
b.	Module circuit area consumed by BITE.	b. Minimum module circuit area consumed by BITE.
c.	Test partitioning incorporated in functional partitioning.	c. Point being monitored on board can be brought out by pins. Function can be subdivided in any manner.
d.	Number of pins for controlling BITE is small.	d. May require a significant number of pins to test a particular module, but if more than one module is being tested, the number of pins utilized for BITE would be small.
e.	BITE will fault-isolate to the one module only.	e. BITE may give ambiguous indication. Is the fault in the module of interest or is it in the BITE module?
f.	Test of the module includes testing of BITE.	f. Additional test equipment is required to test that part of the module which is tied to the BITE module.
g.	Test access and results are simplified by on-module BITE.	g. Test access is complicated by remote location of BITE module.
h.	The prime equipment designer is responsible for the design of the test hardware and test logic.	h. Test responsibility may reside with another individual group.
i.	The partitioning will be greatly influenced by test partitioning.	i. Prime equipment designer not responsible to design for test.

Table 3.2-3. Built-In Test Equipment (BITE), Fault Location Attributes (Continued)

BITE on Circuit Module	BITE on Separate Module
j. Test software may be simpler because of the test partitioning.	j. Test partitioning is not required.
k. Decreased reliability	k. Increased reliability
l. Reduced ready spares requirements	l. Increased ready spares requirements (caused by ambiguity).

Table 3.2-4. Analysis of Software-Controlled Testing

Advantages	Disadvantages
1. No additional BITE hardware required.	1. Software testing provides poor fault isolation.
2. Detection is good because each instruction exercises a large amount of the equipment.	2. Faults in selected areas of the equipment preclude the test getting started.
3. Test exercises in the same manner equipment is used.	3. Expensive to generate software and difficult to maintain configuration control of software
	4. Common modules not fully utilized are not fully tested.

The BIT on the chip must provide the following:

(1) Test vector generation - A large number of vectors must be generated to adequately test the LSI chip. Efficient methods (ROM, repetitive and sequenced patterns) must be devised to generate the large number of vectors required, while minimizing the chip area consumed by the vector generator.

(2) Routing vector generator - Routing vectors must be generated and used in conjunction with the test vectors to route the test vectors through the chip for adequate test. The routing vetors must perform switching functions to open or alter feedback paths as necessary for test.

(3) Results vector monitoring - These vectors are the results of the machine operating on the test and routing vectors. The results must be read and compared at strategic locations within the chip. Comparison of results must be made with each test vector as routed through the machine. The results vectors must be generated in a manner similar to test vector generation.

3.2.4.3 Fault Isolation

Fault isolation in V/STOL avionics will be performed by automatic system diagnosis. The system will use a combination of the methods described above, provided weight and volume continue to be key system characteristics.

Recurring software develpment costs associated with the use of SAM's may be minimized by on-module BIT, which will ease the pressing connector-pin requirement. Having a module BIT capability allows flexibility in specifying technologically transparent functions.

With BIT, the circuitry required to test a function is part of the module itself and does no restrict the diagnostic interface.

The simplest module diagnostic interface -- a one-pin GO/NO GO status -- generally affords greatest flexibility in implementing a module function.

Making LSI circuitry testable is difficult: as more LSI is used in avionics, fault isolation becomes more complex. On-module test for LSI must be seriously considered. If LSI is to be successfully implemented, BIT will become a practical necessity for all maintenance levels, from module to full system.

The methods of implementing BITE and generating vectors to adequately test and fault isolate to the chip or module must be kept technically concurrent with the LSI technology. Ingenious methods for generating and inserting vectors to test LSI chips must be devised. A possible solution is to model a LSI chip in a computer simulation and test the function and the test vectors on the same simulation.

3.2.5 Reliability and Life Cycle Cost

Highly reliable systems with high operational readiness and minimum life-cycle costs are necessary to meet the Navy's future mission. It is essential that the high logistics support costs being experienced in today's fleet be reduced and translated into funding for new equipment and systems design, development and production.

In an effort to assess the reliability and life-cycle cost impact of alternate thermal design approaches, an analysis of a representative avionics subsystem (ASW-MIDER) was conducted. It is assumed that these results are sufficiently representative of the MAP packaged electronics to allow system-level generalizations.

3.2.5.1 Reliability

Significant reliability improvement is required for V/STOL and other future platforms. The MAP approach offers the capability to meet these requirements through:

- Lower junction temperatures
- Reduced interconnections
- Design standardization
- Rigorous environmental controls
- LSI

The recommended MAP concept baseline thermal design is optimized for system reliability. The use of direct-air cooling will result in average junction temperatures 10°C lower than a conduction cooled system. Additionally, the direct-air cooling approach allows for more reliable degraded mode operation in the event of battle damage or ECS failure.

The use of SAM's that are "natural functions" with on-module BIT results in a minimization of I/O pin requirements. The use of fiber-optic multiplex bussing serves to reduce the I/O pin requirements. LSI will also have a major impact on the reliability of multilayer boards (MLB's) and ceramic substrates. With a major portion of gate interconnection being performed on a monolithic chip, the number of plated-thru holes (or vias) and number of MLB (substrate) layers will be reduced.

The design standardization practices and experience on the current SEM program has shown that we can expect a SAM program to result in more reliable implementation of assembly level (WRM) circuits. This is practical because Navy design reviews of new circuit implementation approaches can be performed with a complete understanding of the design requirements of that function. Almost the opposite is true of non-standard custom electronic assemblies of today. Once a standard circuit function is designed, developed and verified, we no longer need cope with equipment unreliability and design errors associated with "reinventing" the same functions for new equipments, as we do in today's avionics.

The MAP baseline approach features significant improvements in controlling key environments which contribute to system unreliability. High junction temperatures have long been recognized as a major contributor to system failures. MAP will significantly reduce average and worst-case continuous operation junction temperatures below the 110°C goal. Temperature cycling has also been recognized as a major precipitator of equipment failure modes, such as integrated circuit wire bond opens and MLB opens. The MAP thermal design limits the excursions in temperature cycling and reduces stress and strain in critical areas. Humidity has also been a major problem in the airborne fleet. MAP integrated racks include provision to dehumidify the closed loop air used for equipment cooling. This feature minimizes failure modes precipitated by humid environment.

The high degree of LSI use anticipated as required to meet minimum weight and volume requirements for platforms such as V/STOL will greatly enhance avionics reliability. This view is based upon General Electric's microcircuit failure analysis results, which provide excellent insight into why integrated circuits fail (Figure 3.2-5). Clearly, the major reasons for integrated circuit failures have not been die-processing related. Failure-analysis results in 1976 and 1977 revealed that approximately 3 percent of the microcircuit failure mechanisms are die-processing related. (It assumes all metalization and contamination failures were so related.) If we assume that a total of 10 SSI and MSI devices were replaced by one LSI device, then the non-die processing related failure modes (70 percent of the total failures) will be reduced by an order of magnitude. Die-related failure modes will then be the major problem area (assuming LSI testability problems are resolved). However, the absolute magnitude of the system failure rate should go down significantly because of all the SSI and MSI packaging-related failures that have been reduced to those associated with only one LSI die, in one package, with many fewer total wire bonds! As to die processing related failure modes, industry price competition will force semiconductor manufacturers to produce reasonably good LSI die-processing and yields, or they will go out of business.

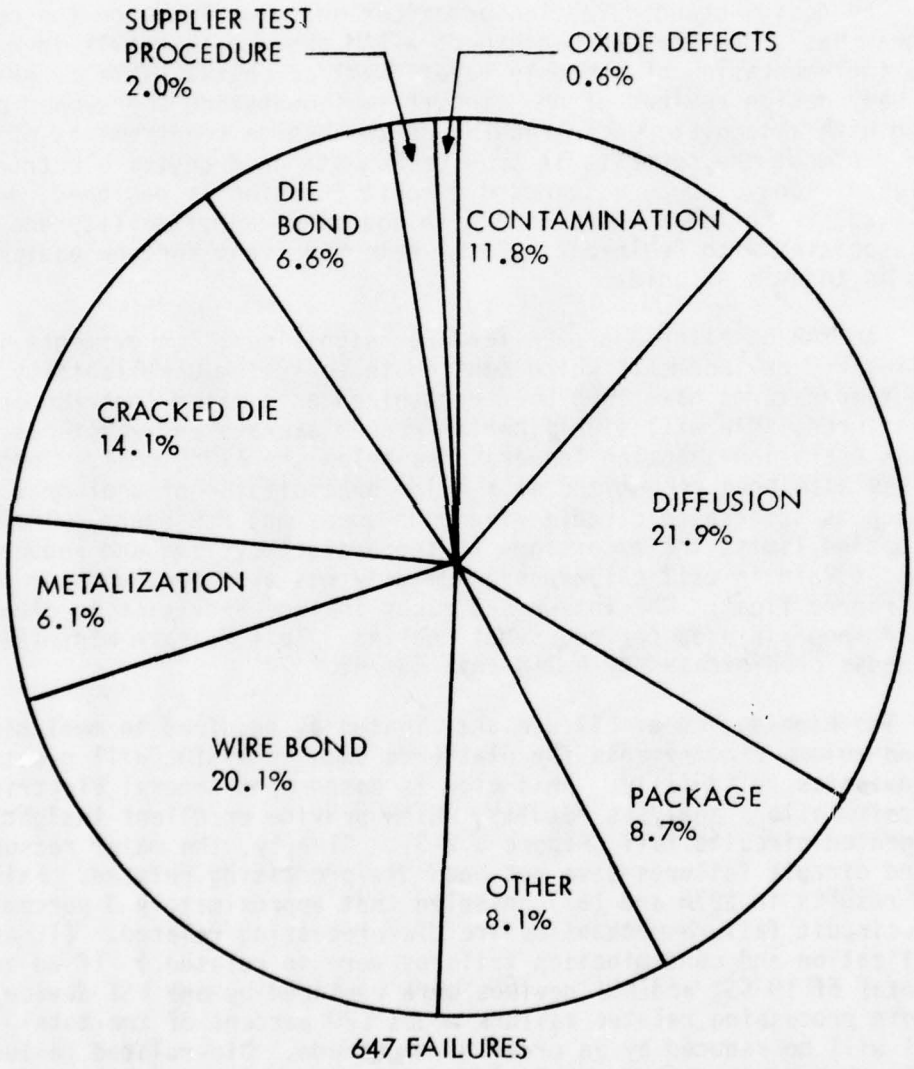


Figure 3.2-5. Microcircuit Supplier Faults Failure Mechanisms

In performing reliability analyses for equipment utilizing mid-1980's designs, there is a serious limitation due to the lack of a validated reliability model for large-scale integrated circuits. For the very high gate complexities anticipated, the current predicitive techniques yield failure rates grossly larger than good engineering judgment would deem reasonable. This lack of a good LSI reliability model is recognized by both industry and the military. Several alternate models have been proposed to cope with this problem, but none can be said to yield believable results at higher temperature ranges. In performing the reliability analyses, MIL-HDBK-217B was used as the baseline technique. Reliability failure rates were calculated and normalized for junction temperatures of 50°C (nominal condition), 65°C, 85°C, 105°C, and 125°C. (See Table 3.2-5.) Four alternative approaches to calculating the failure rates of complex LSI devices (e.g. 64K RAM's) were used.

TABLE 3.2-5. Normalized Failure Rates vs. Junction Temperature

	50°C	65°C	85°C	105°C	125°C
CASE 1	1	1.3	1.5	6.7	17.5
CASE 2	1	1.25	1.7	2.2	2.9
CASE 3	1	1.3	1.5	3.1	6.3
CASE 4	1	1.8	4.5	13.3	37.0

A1. Case 1

The failure rates of all devices except complex LSI circuits, calculated per MIL-HDBK-217B; LSI device failure rates are calculated using a General Electric derived failure rate model (G. Kasouf, "Evaluation of LSI/MSI Reliability Models" - Appendix B - to be presented at the 1978 Annual Reliability and Maintainability Symposium).

A2. Case 2

Failure rates were calculated as in Case 1, except Complex LSI failure rates at 105°C and 125°C are exponential extrapolations from the three previous temperatures.

A3. Case 3

Failure rates were calculated as in Case 1, with the exception of complex LSI devices at 105°C and 125°C. For the latter two cases, it was assumed that the LSI failure rate would follow the rule of thumb that the failure rate doubles for every 20°C rise in temperature.

A4. Case 4

Failure rates were calculated using Standard MIL-HDBK-217B formulas and factors.

To allow a relative comparison in the life-cycle cost analysis, all failure rates were normalized with respect to the subsystem failure rate at 50°C. Figure 3.2-6 depicts these normalized failure rates for each predictive approach. With the projected increased usage of complex LSI, it will be very difficult, at best, to project avionics reliability for V/STOL-type equipment. It is recommended that studies be initiated to establish viable reliability prediction models for complex LSI devices. This is essential, because at junction temperatures above 85°C, these devices drive the subsystem "predicted" reliability to an unrealistically high level using current models.

3.2.5.2 Life Cycle Cost Analysis

A representative V/STOL equipment (ASW-MIDER) was selected for Life Cycle Cost Analysis. The first step was to estimate the changes in failure rate for changes in junction temperature of the circuitry within the MIDER unit. The changes in failure rate, as described by the four cases above, were provided by Reliability Engineering as percent increases in failure rate for the various junction temperatures selected. The changes in failure rate were inserted in the MIDER input conditions into the General Electric Life Cycle Cost model.

The more important program input conditions established for LCC model are as follows:

1. Maintenance Concept - repair MIDER by R&R of Modules at organizational level.

2. Repair the failed modules at depot.

3. Duration of program - 20 years.

4. Number of Bases - 16.

5. A/C Utilization Rate - 25 hrs./month.

6. Number of MIDER Equipments - 950 distributed among aircraft at 16 bases.

7. Two depots would be used to repair the modules.

8. Appropriate data describing MIDER equipment was generated, with including cost, number of modules, MTBF, MTTR, etc. Preliminary cost information was used.

9. Appropriate data describing depots were also generated.

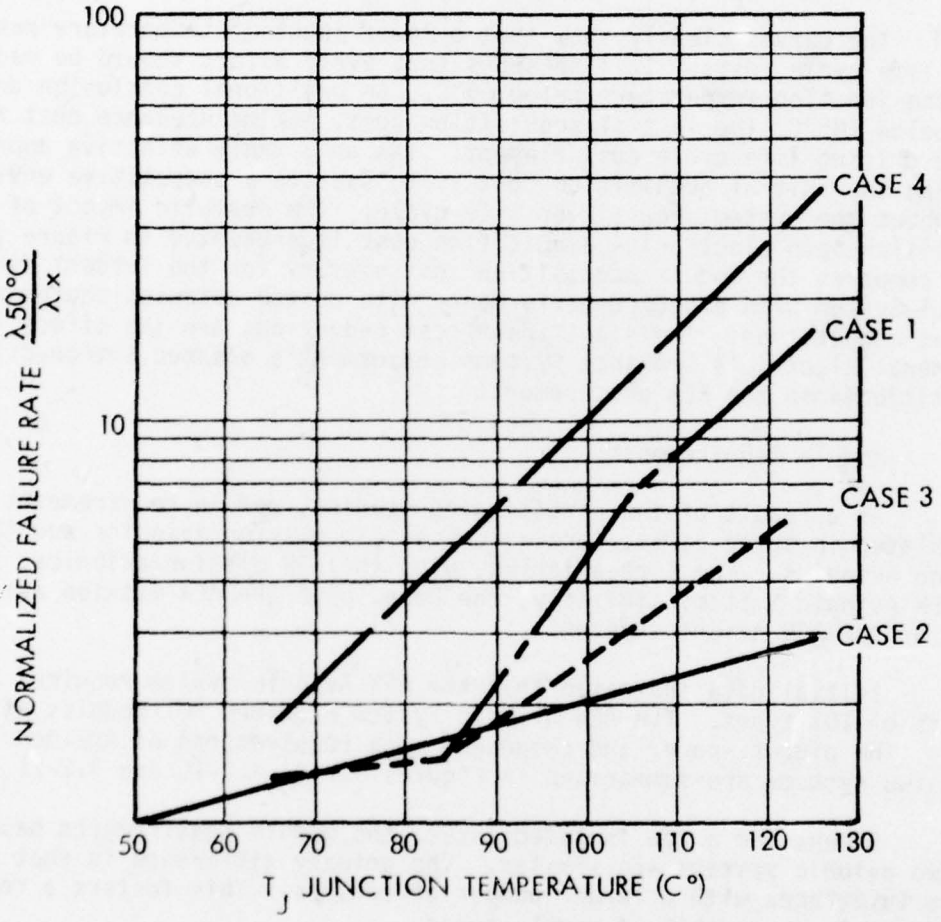


Figure 3.2-6. Normalized Failure Rates (λ) vs Junction Temperatures

The model was run first for the equipment with a junction temperature of 50°C and all other runs were normalized to the 50°C case. During each run, all the data was kept constant except the failure rate which was varied in accordance with the junction temperatures selected.

The effect of junction temperature upon life cycle cost is shown in Figure 3.2-7, with curves corresponding to the four reliability cases. Since all other variables (cost included) were kept constant, the shape of the curve is derived by the MTFB-dependent costs (spares, maintenance, inventory retention and storage, transportation, etc.). During the analysis the non-MTBF dependent items remained constant during the LCC calculations.

The curves clearly show that a lower junction temperature results in lower life cycle costs. It also shows that every effort should be made to keep the junction temperature below 85°C. An additional conclusion drawn is that below +85°C, the initial acquisition cost, not maintenance cost factors, is the driving life cycle cost element. The only truly effective approach to reducing the initial acquisition cost is to sustain a competitive environment throughout the system acquisition life cycle. The dramatic impact of competition upon electronics acquisition cost is presented in Figure 3.2-8 which compares the module acquisition cost history for the Trident Fire Control System with expected performance with custom avionics equipment without competition. The significant cost reductions are the direct result of General Electric's Ordnance Systems Department's planned introduction of competition into the SEM procurement.

3.2.6 Module Requirements

As a result of the partitioning studies, module requirements were accumulated in three parts; Core avionics, ASW mission avionics and AEW mission avionics. The Core avionics, plus the ASW mission avionics, makes up the ASW Avionic System; similarly, the Core, plus the AEW mission avionics, makes up the AEW Avionic System.

Initial data indicated that the ASW Avionic System required 735 modules of 101 types. The AEW Avionic System required 781 modules of 62 types. The pinout, power and component area requirements of the modules for those two systems are summarized in Figures 3.2-9, 3.2-10 and 3.2-11.

Except for a few isolated cases, the module requirements based on the two avionic systems are similar. The primary difference is that the ASW system interfaces with a larger number of sensors. This fosters a requirement for a larger number of module types.

Because the AEW system was better defined, it was decided further to refine the data on that system in order to achieve maximum confidence in the data upon which the module and rack packaging efforts would be based.

The "second look" at the AEW system resulted in no discernible difference in module power and circuit area requirements. There was, however, a significant increase in the pinout requirements for one commonly

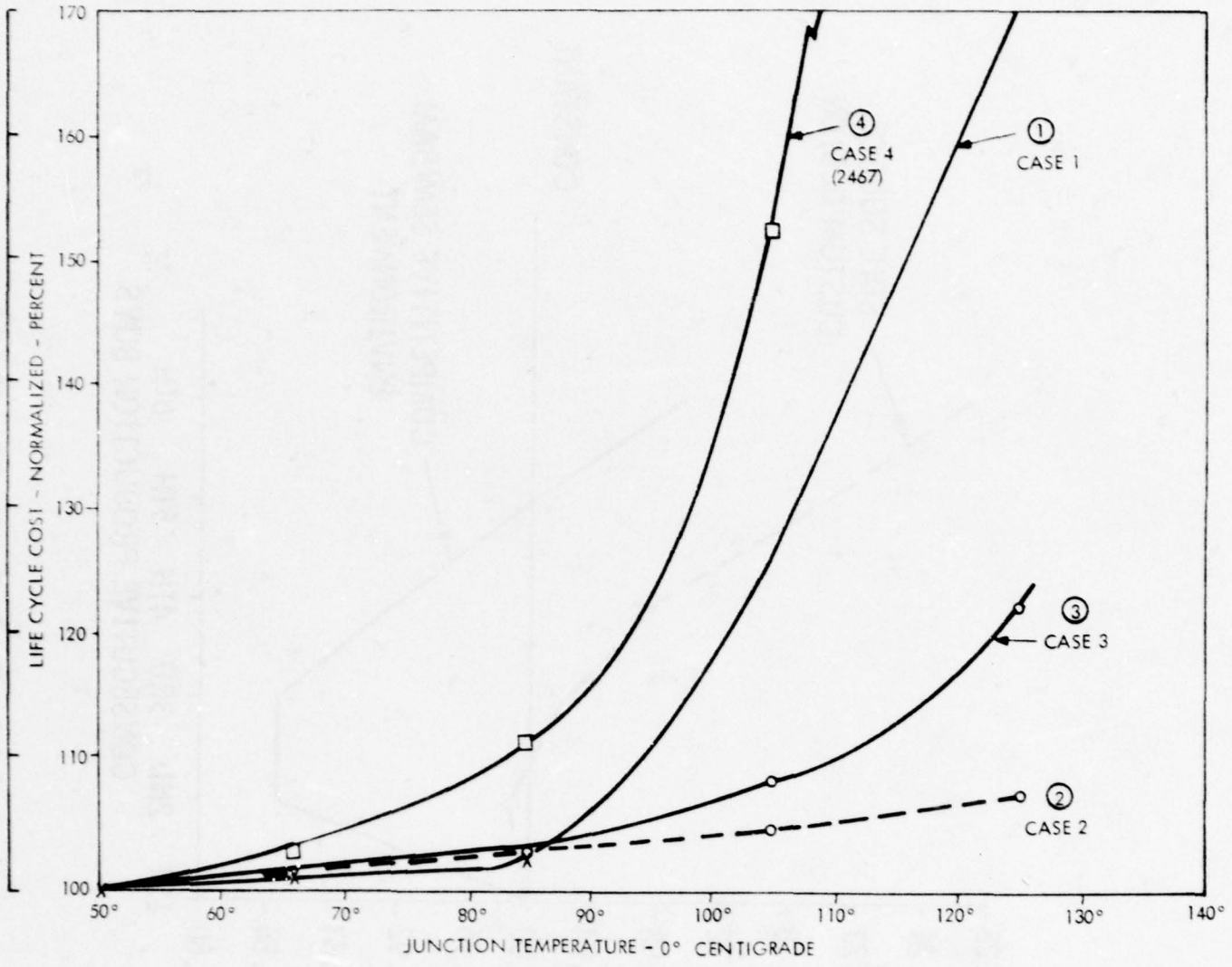


Figure 3.2-7. Normalized Life Cycle Cost vs. Junction Temperature

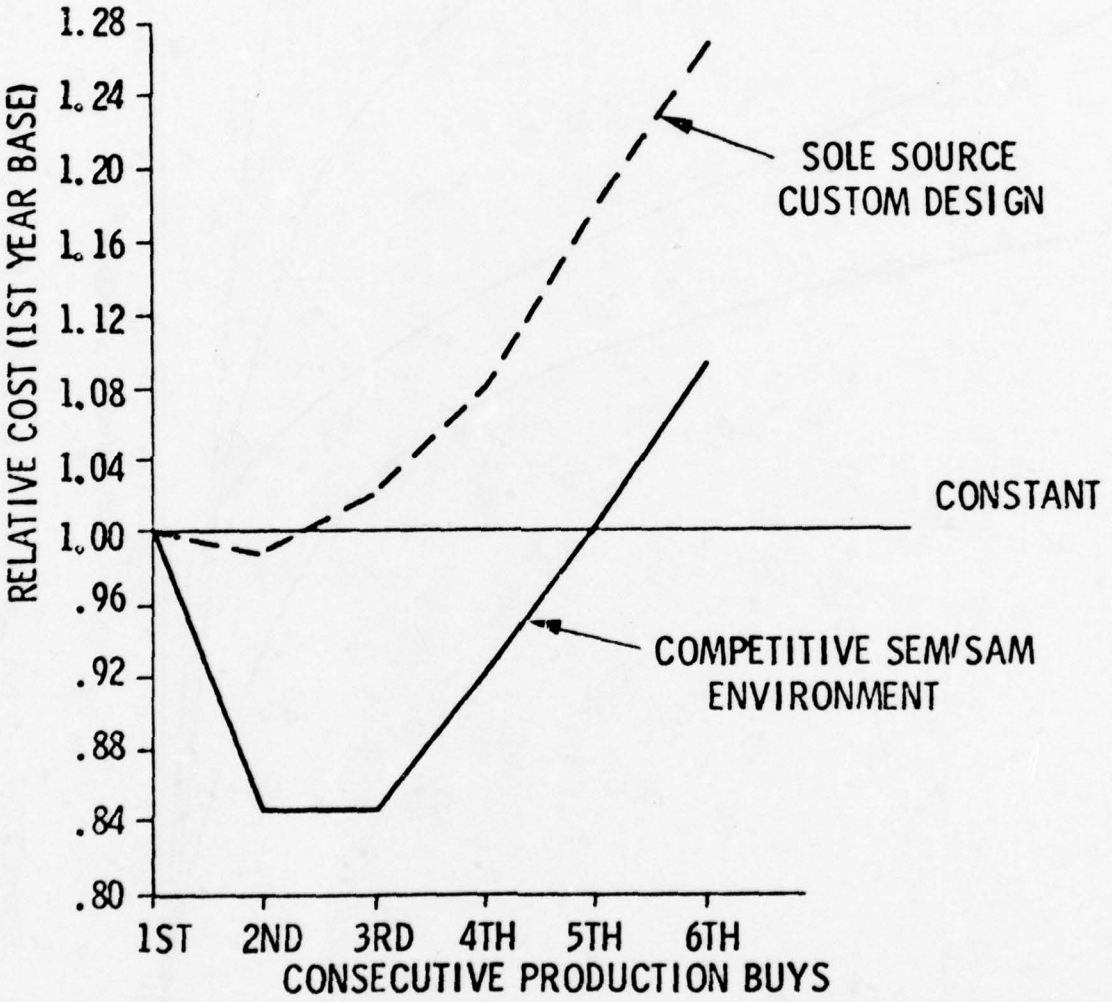


Figure 3.2-8. Module Cost History: Sole Source vs Competitive Procurement

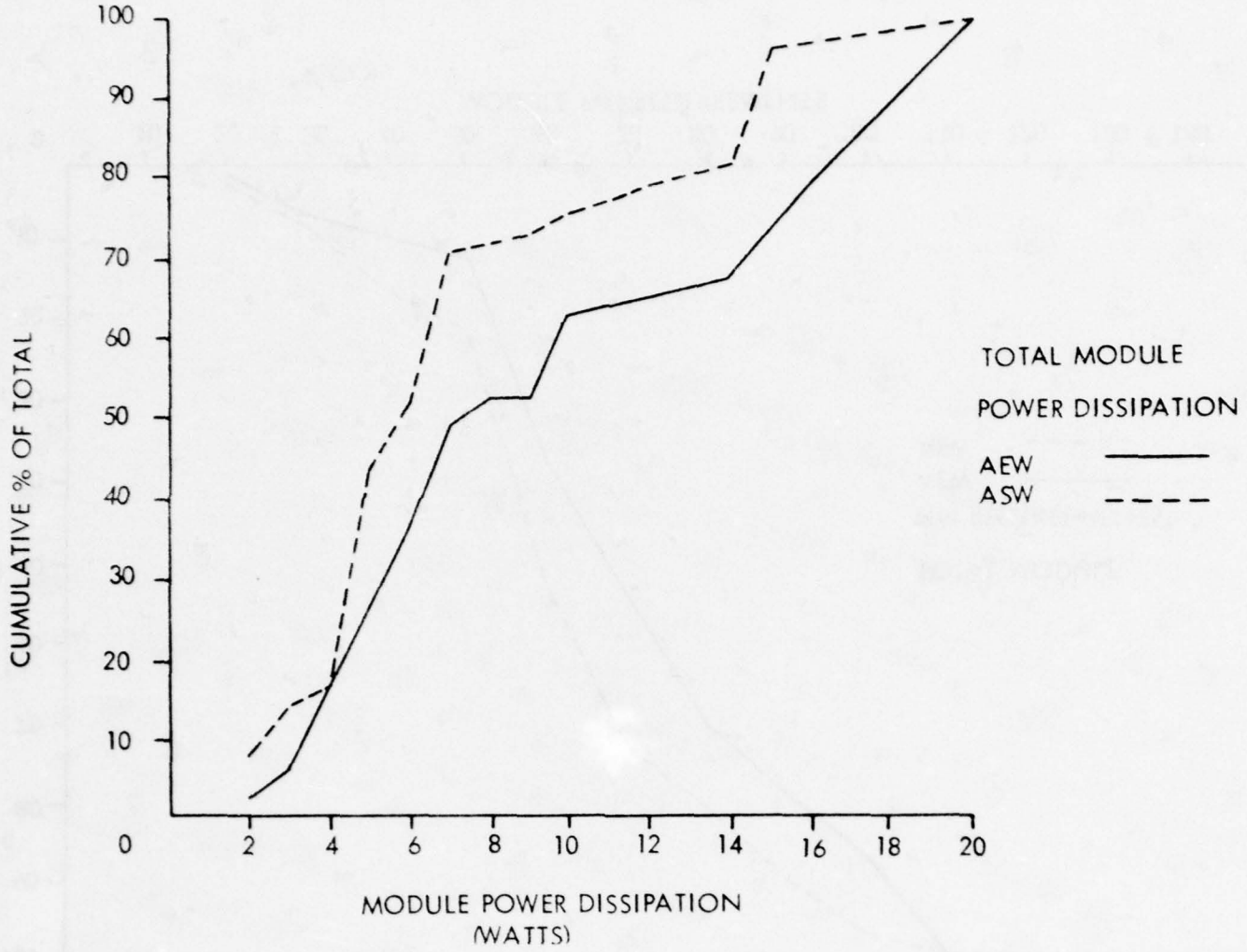


Figure 3.2-9. Total Module Power Dissipation

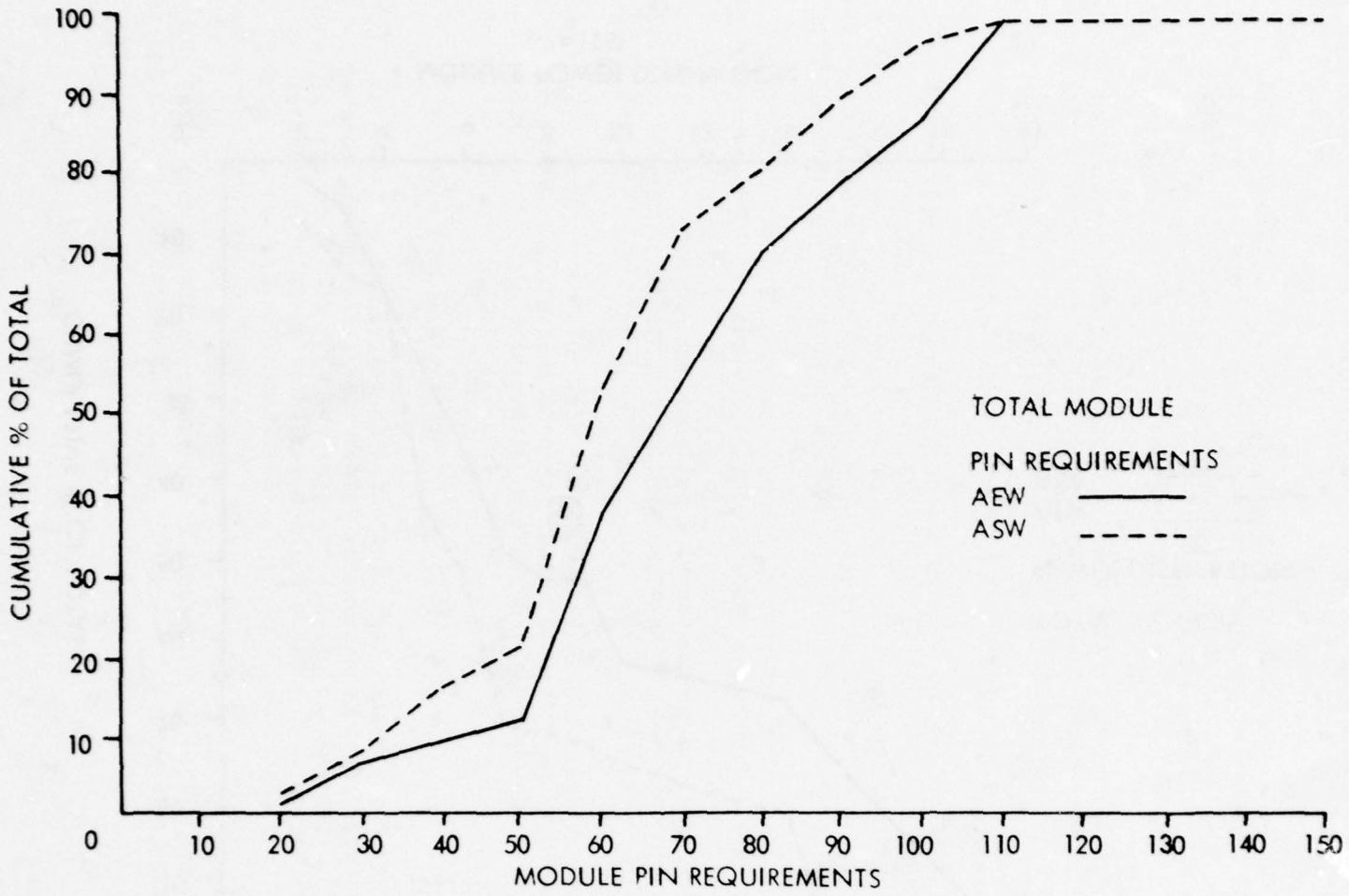


Figure 3.2-10. Total Module Pin Requirements

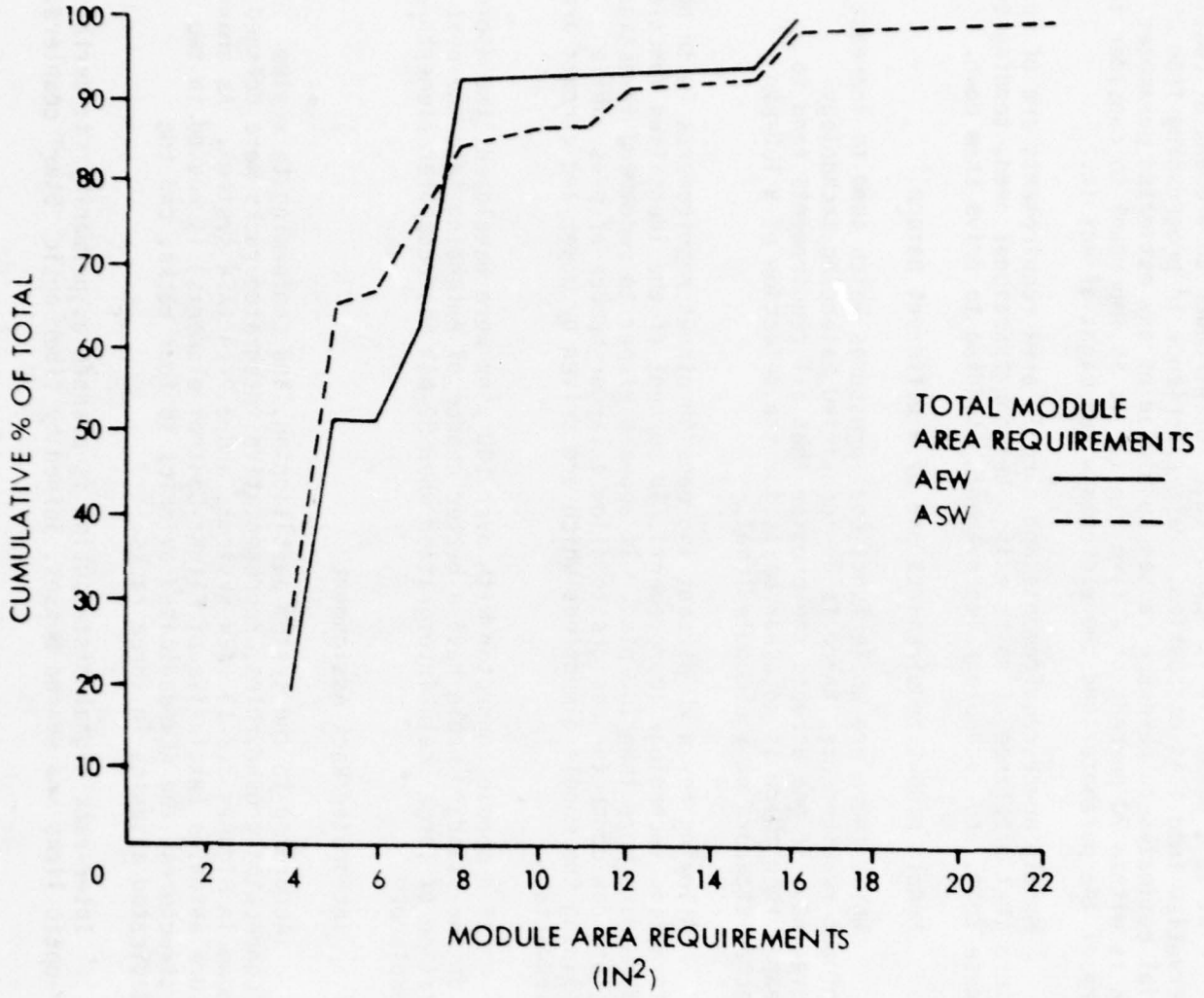


Figure 3.2-11. Total Module Area Requirements

used module. The revised pinout spread is indicated by curve A of Figure 3.2-12.

At this point, it is appropriate to introduce an element of cautious conservatism into this discussion. Past experience in progressing from initial estimates to hardware causes suspicion of any estimated parameter which is within 20 percent of a firm limit. It is important to consider the nature of the parameter and the elements which might affect it.

Module power requirements and circuit area requirements are of such a nature that a balance of sorts exists between functional need, tending to increase them, and technology improvements, tending to drive them down.

Module pinout requirements are of a different nature.

While there are ample functional pressures which tend to increase the pinout requirements, there is no identified balancing technology improvement. If one accepts the premise that all requirements tend to increase, then there is no clear basis for the selection of a 100-pin connector standard at the module level.

Allowing for a 20 percent increase in pinout requirements (with no counteracting technology improvement), 40 percent of the identified functions would require more than 100 pins. It appears proper to recommend investigation into new connector designs to allow a larger number of pins, while maintaining the module dimensions which are driven by power and circuit area requirements.

If a module connector with over 100 pins were developed, the useful life of the standard would have a better chance of extending into the next generation of large scale intergration when 32-bit microcomputer elements are commonplace.

3.2.7 Integrated Rack Assignment

According to the system partitioning, and conforming to system interconnection ground rules, representative integrated racks were defined, as shown in Figures 3.2-13 (AEW system), and 3.2-14 (ASW system). As shown, the Core avionics (exclusive of Flight-Control elements) is housed in two rack structures, the AEW-dedicated avionics in four racks, and the ASW-dedicated avionics in three racks.

Inter-rack signal distribution is planned as primarily via serial fiber-optic links and shared busses, joined by fiber optic "Star" couplers.

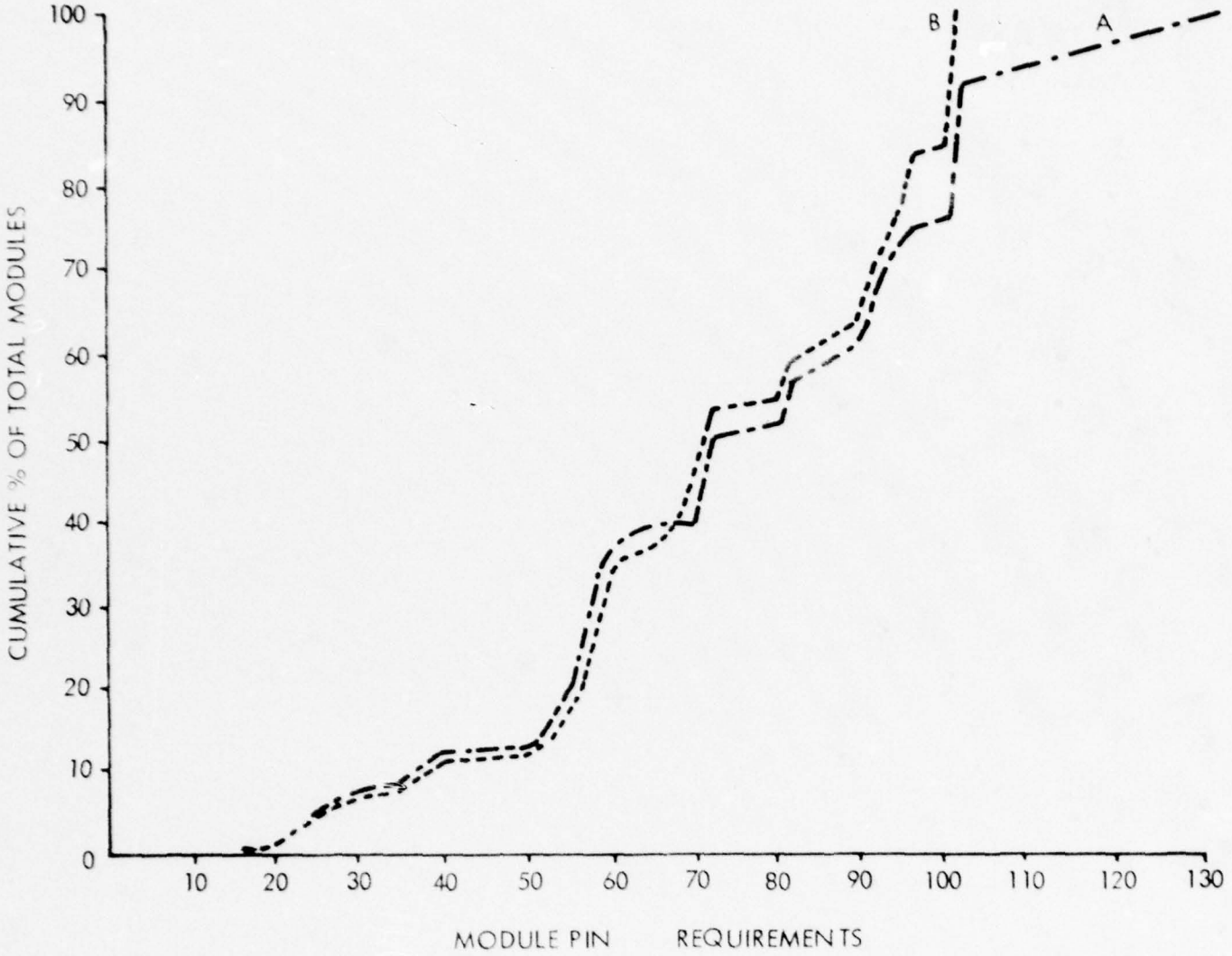
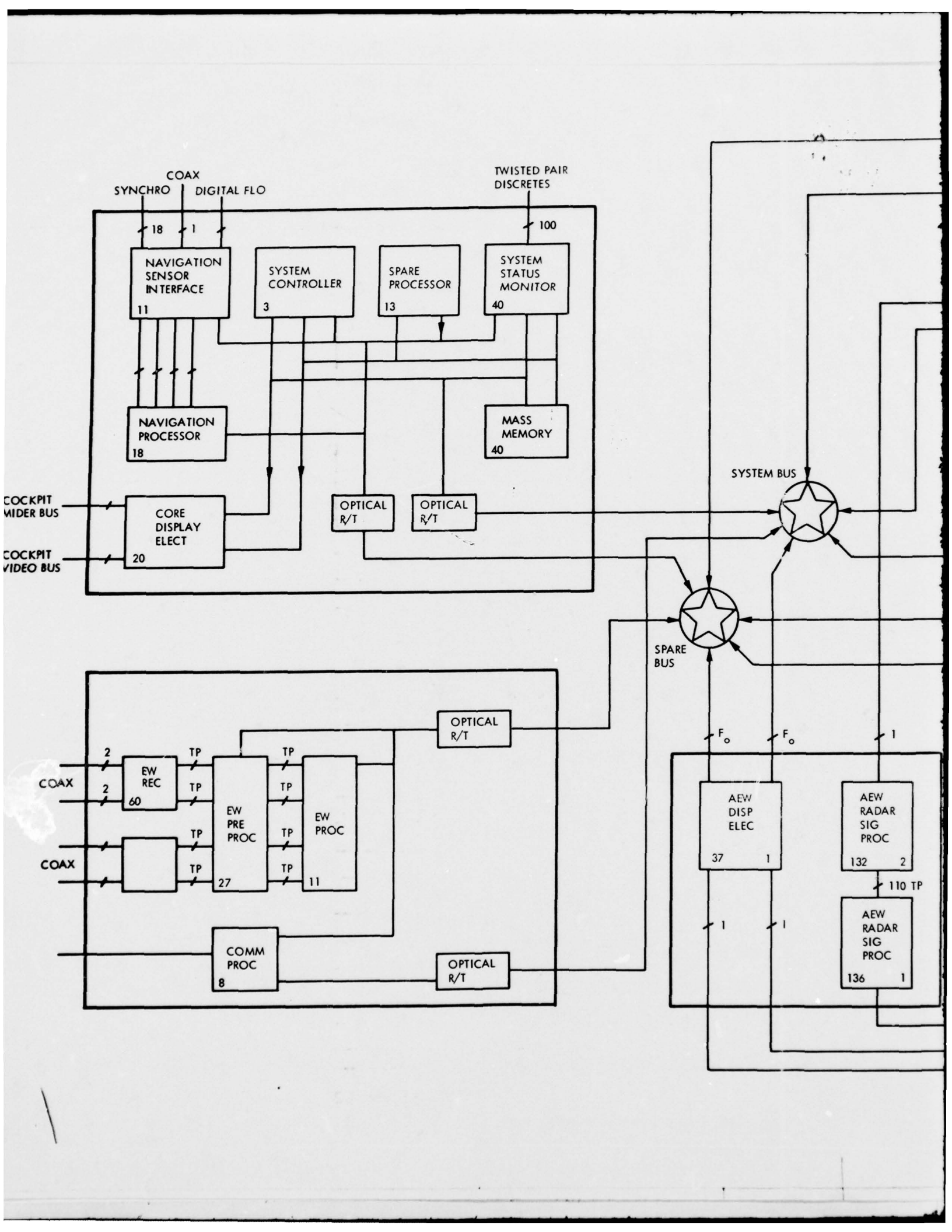


Figure 3.2-12. Total Module Pinout Requirements


COAX
SYNCHRO
DIGITAL FLO
TWISTED PAIR
DISCRETES
18
1
100
NAVIGATION SENSOR INTERFACE
11
SYSTEM CONTROLLER
3
SPARE PROCESSOR
13
SYSTEM STATUS MONITOR
40
NAVIGATION PROCESSOR
18
MASS MEMORY
40
SYSTEM BUS
COCKPIT
MIDER BUS
COCKPIT
VIDEO BUS
CORE DISPLAY ELECT
20
OPTICAL R/T
OPTICAL R/T
SPARE BUS
OPTICAL R/T
2
TP
EW REC
60
EW PRE PROC
27
EW PROC
11
COAX
COAX
COMM PROC
8
OPTICAL R/T
F_o
F_o
1
AEW DISP ELEC
37
1
AEW RADAR SIG PROC
132
2
110 TP
AEW RADAR SIG PROC
136
1

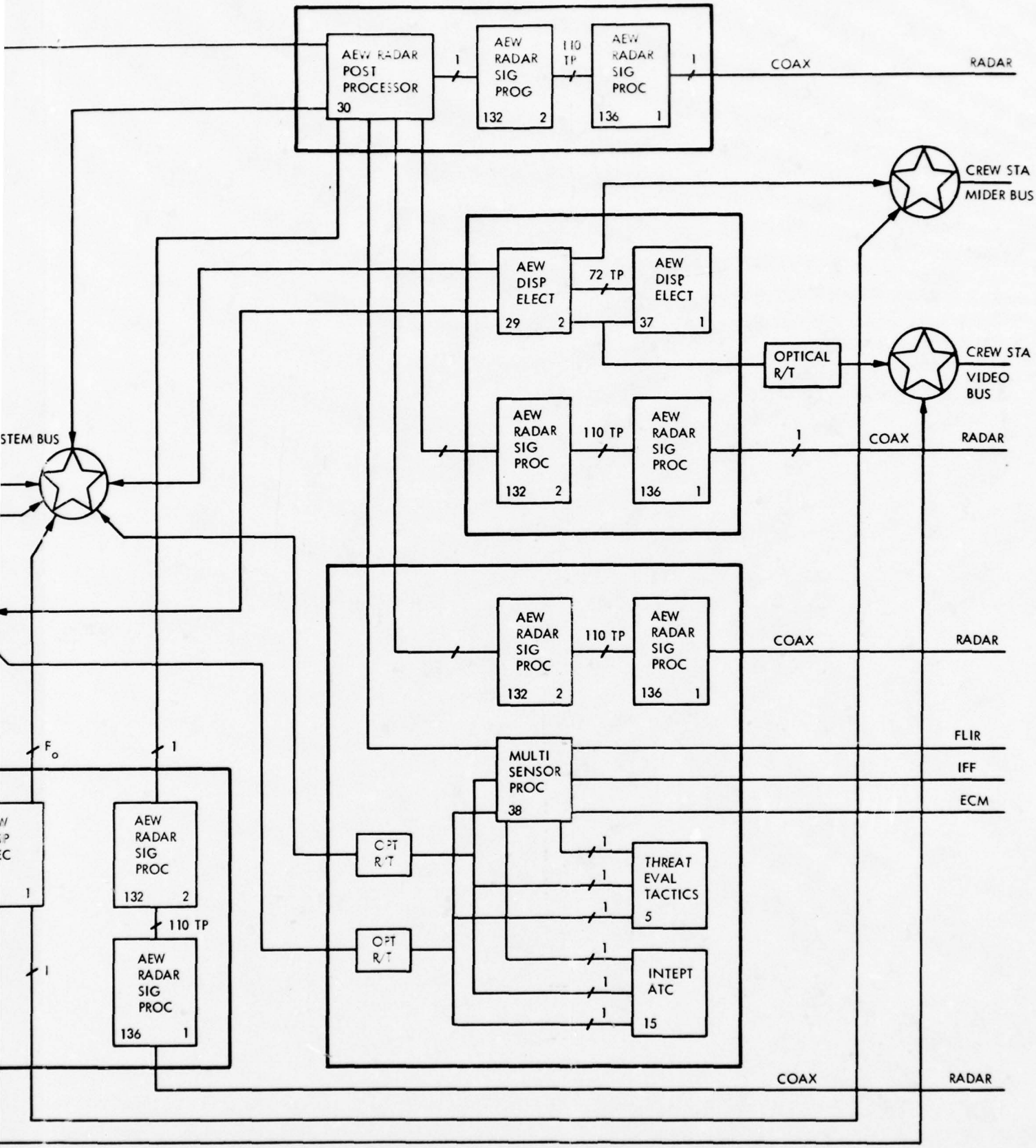
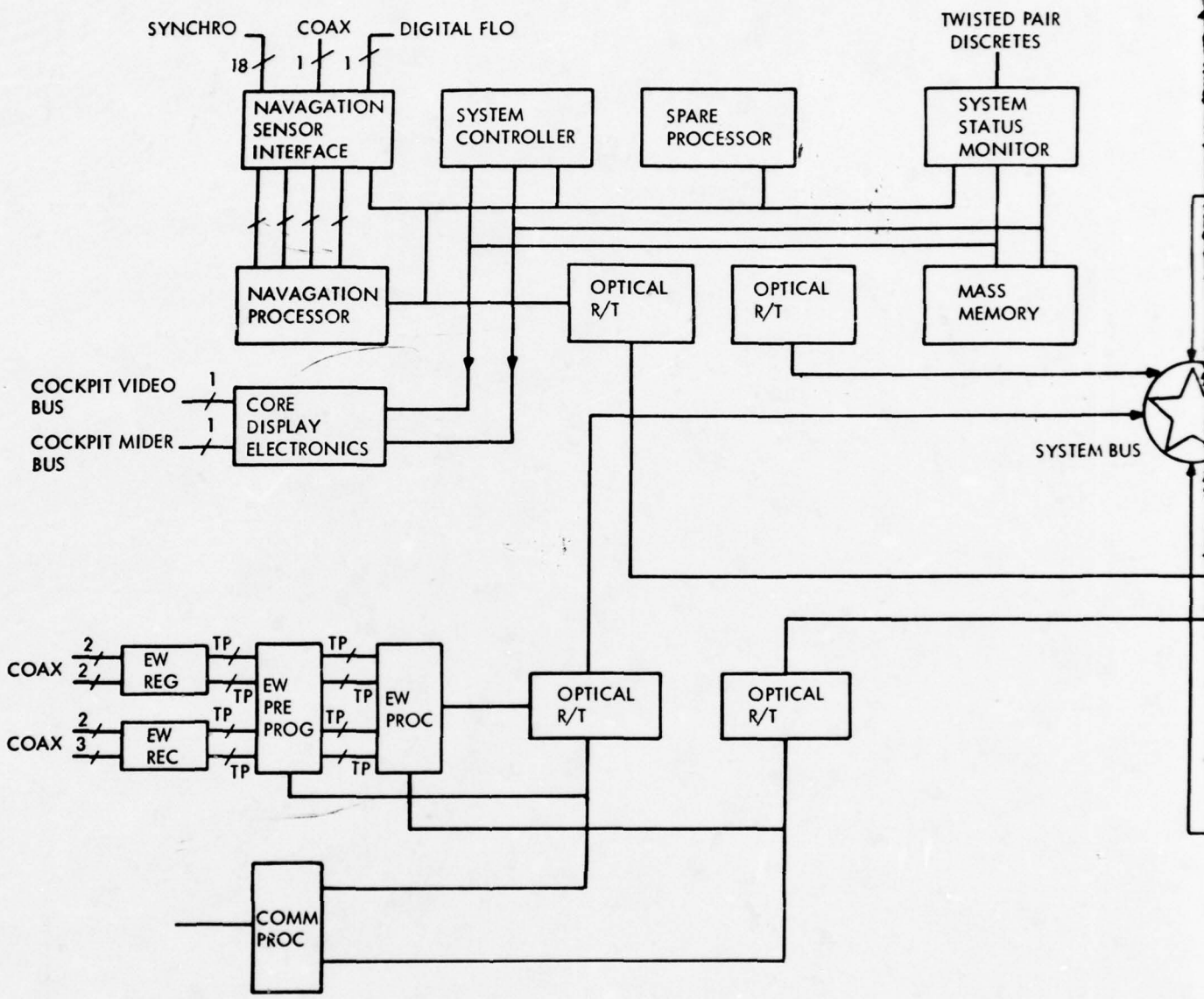


Figure 3.2-13. AEW System Partitioning, Block Diagram


SYNCHRO
COAX
DIGITAL FLO
18
1
1
TWISTED PAIR DISCRETES
NAVAGATION SENSOR INTERFACE
SYSTEM CONTROLLER
SPARE PROCESSOR
SYSTEM STATUS MONITOR
NAVAGATION PROCESSOR
OPTICAL R/T
OPTICAL R/T
MASS MEMORY
COCKPIT VIDEO BUS
COCKPIT MIDER BUS
1
1
CORE DISPLAY ELECTRONICS
SYSTEM BUS
COAX
COAX
2
2
2
3
EW REG
EW REC
TP
EW PRE PROG
EW PROC
OPTICAL R/T
OPTICAL R/T
COMM PROC

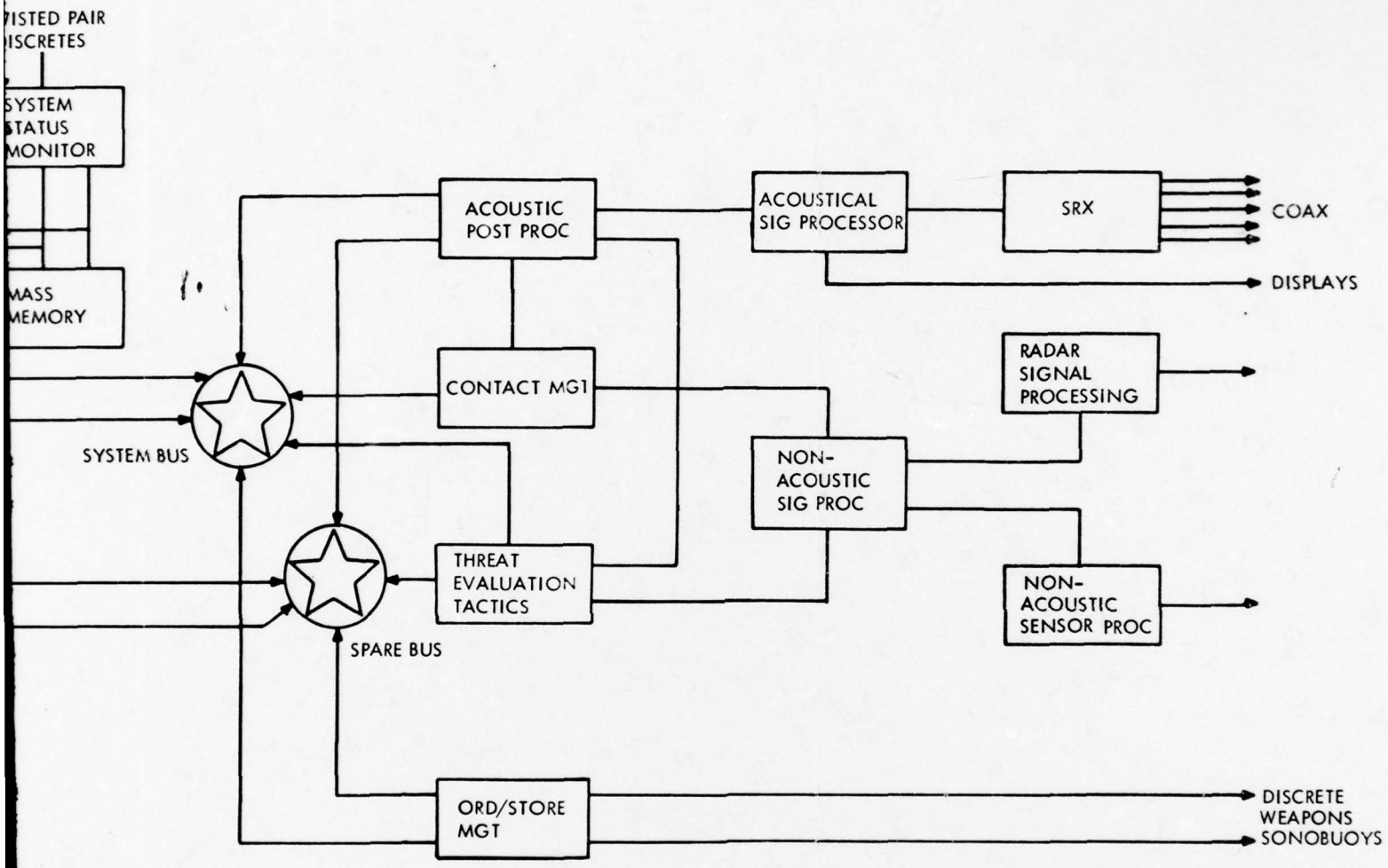


Figure 3.2-14. ASW System Partitioning, Block Diagram

3.3 Module Mechanical Concepts

3.3.1 Design

An important part of this study was to consider advanced module designs. The designs will be required for packaging circuits of the 1985 era. The modules must be reliable and efficient, to satisfy operational requirements of V/STOL and other avionic systems.

There are several overriding factors which significantly influence final module configuration. The module thermal capacity, component mounting area, and connector size can either be evolved in concert with system requirements, or, if selected haphazardly, can severely impact final system performance characteristics: weight, reliability, maintainability and life cycle cost.

The approach followed in this study involved the determination of these primary module characteristics as a result of an in-depth system investigation (Section 3.2) which was not restricted to a particular module configuration. The data system partitioning, in conjunction with integrated circuit and package technology development predictions, was used to determine primary module characteristics discussed below.

3.3.1.1 Power

Modules requiring up to 20 watts were identified. In the AEW system, approximately 30 percent of the modules have dissipation in excess of 14 watts (Figure 3.2-9). The calculated power dissipation requirements, together with a preliminary environmental control system evaluation, indicated a requirement for a module thermal design to provide a maximum coolant-to-junction thermal resistance of 3.5°C/watt (based on T_j max = +110°C). This requirement exceeded the capability of conventional conduction cooling techniques, leading to investigation of more efficient cooling methods to provide a more direct path between circuit element and coolant. These approaches involve direct air impingement, heat pipes, liquid cooling, flow-through modules, and improved conductive paths; they are described in detail in Section 3.3.2.

3.3.1.2 Component Area

Integrated circuit and package technology projections, together with the system partitioning analysis, predicted component area requirements close to the capability of the present I-2A SEM. These results (Figure 3.2-11), based on chip carrier package technology, show that the area afforded by a double-sided I-2A SEM will accommodate approximately 85 percent of the system module population. This determination is strongly dependent upon the adoption of the chip carrier (cc) as the standard package in the semiconductor industry, displacing the present dual in-line package (DIP). At present there are many positive, indications supporting this prediction, and very little opposition.

The component area requirement strongly influenced the investigation of the I-2A SEM and its derivitives as a primary candidate for this study.

3.3.1.3 Connector Pins

The selection of the connector size (pin quantity) is one of the most critical aspects of module definition. Its effect on system partitioning, built-in test, and system maintainability characteristics can be significant. Packaging density or power-dissipation limitations can usually be overcome by alternate circuit/packaging techniques (LSI and Hybrids) and by judicious placement of components with respect to the coolant.

Pin limitation problems usually result in less-than-optimum partitioning, contributing to decreased packaging density, diagnostic limitations, and increased system connection pins.

The data presented in Figure 3.2-12 indicates that the standard 100-pin connector will satisfy the requirements for only approximately 75 percent of the modules in the AEW system. (One module type used 116 times requires 102 pins.) Further, experience dictates that final pin requirements tend to increase from the initial system-partitioning estimates. Finalization of control signals, BITE requirements, and power-distribution considerations are contributing factors.

An attempt to quantify this problem is presented in Figure 3.3-1. The original AEW pin requirements curve was smoothed and another curve was established, representing an empirically derived 20 percent growth factor. A 100-pin connector then falls short of being a good choice, since it meets only about 60 percent of the module requirements on the projected growth curve.

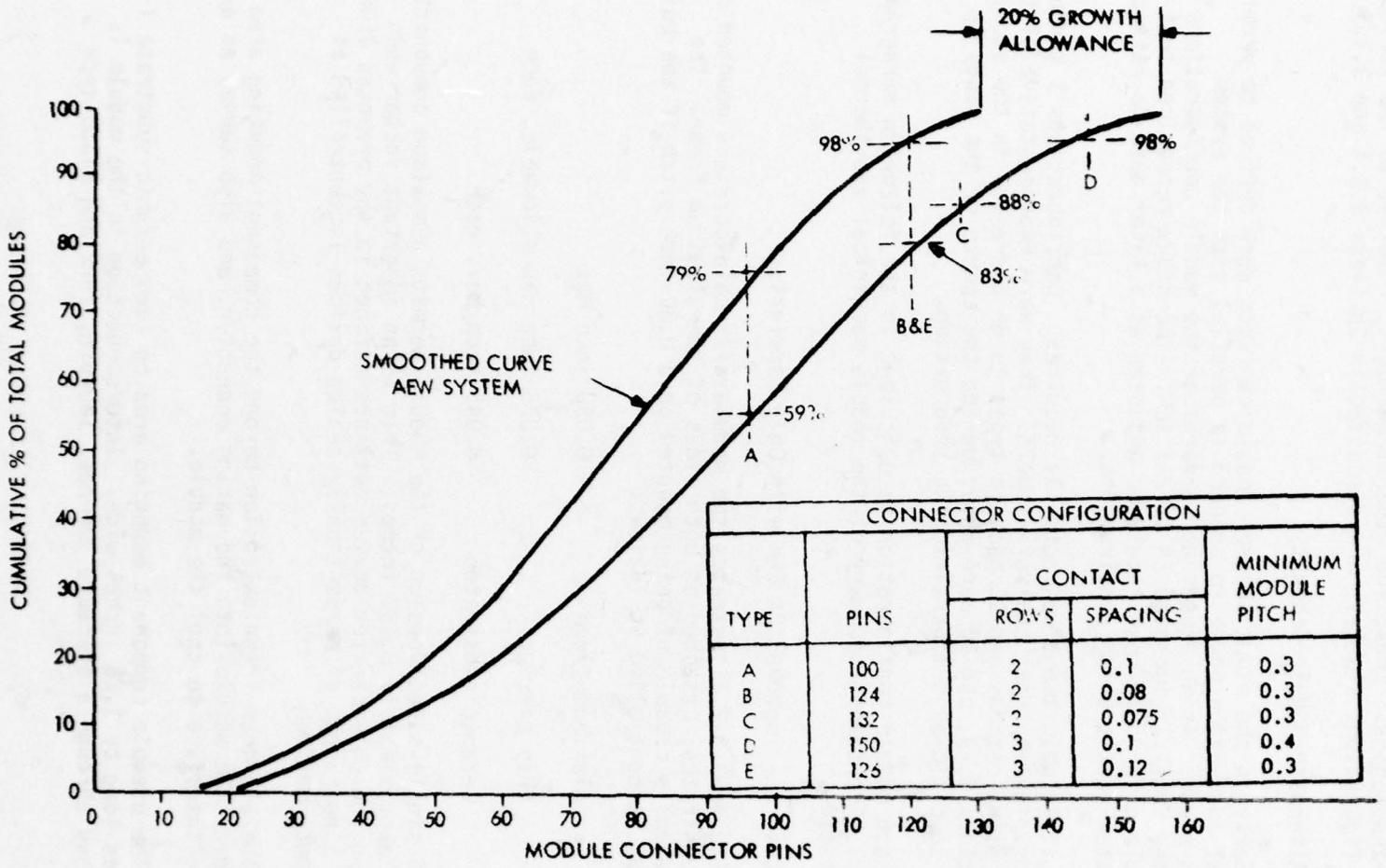
Several alternate connector configurations, summarized on Figure 3.3-1, were identified which will better satisfy the projected requirements of the standard avionics module.

A connector of approximately 125 pins appears to be a minimum choice. This size connector will cover over 80 percent of the module requirements as defined by the expanded curve. This appears to be a good choice, since it corresponds to 98 percent of the modules of the original system analysis.

Alternate connector configurations, which allow an increased pin count within the present 0.3 inch module pitch limitation, are described and evaluated in Section 3.3.3.

3.3.1.4 Other Considerations

In addition to the thermal, area, and connector constraints, several other factors were considered in evaluating various module configurations. These included module volume and weight characteristics, producibility and cost factors, reliability and maintainability impact, versatility in system



CONNECTOR CONFIGURATION

TYPE	PINS	CONTACT ROWS	CONTACT SPACING	MINIMUM MODULE PITCH
A	100	2	0.1	0.3
B	124	2	0.08	0.3
C	132	2	0.075	0.3
D	150	3	0.1	0.4
E	126	3	0.12	0.3

Figure 3.3-1. Module Pinout Requirements, V/STOL System

application, and ability to accept present and future integrated circuit and package technologies. These and other trade-offs, relative to the various module configurations studies, are discussed in Sections 3.3.4 and 3.3.5.

3.3.2 Alternate Module Concepts

Early in the study several module concepts were defined to permit the thermal evaluation phase to proceed in parallel with the system definition phase. As an expedient, several of the module configurations were based on the familiar improved 2A (I-2A) SEM. The study recognized that the basic module size would most likely be adjusted at a later date to reflect actual system partitioning requirements.

Little adjustment was actually required. Configurations 1 through 7 were the original thermal analysis models. They were representative of the various cooling methods and IC package types to be addressed in the study. Configurations 8, 9, and 10 were added during the course of the study as a result of specific system partitioning information.

Each module configuration is described in the following paragraphs. Section 3.3.4 contains a summary of the module mechanical and thermal characteristics.

3.3.2.1 Case 1 - Improved 2A SEM with Chip Carriers

Figure 3.3-2 illustrates the module with chip carriers mounted on ceramic substrates, attached on both sides of the aluminum frame. The configuration is capable of being mounted on a 0.30 inch pitch if the build-up of items is controlled as follows:

Aluminum frame	0.050 inch max
Chip carriers	0.075 inch max allowable, each
Ceramic substrates	0.045 inch max, each

A single-sided version of the module permits a maximum component height of approximately 0.190 inches. This is an important factor when considering the chip-carrier device outlines defined in the proposed JEDEC standard. The height of heremetically-sealed devices is controlled at 0.140 inches, maximum.

The aluminum frame extension beyond the component mounting area is used to guide the module into the mating connector, and also serves as a conductive interface to cool the module.

The useable component mounting area on each ceramic substrate is 5.30 inches long by 1.25 inches wide. Interconnection to the module is accomplished through a standard two-row, 100-pin, fork and blade type connector.

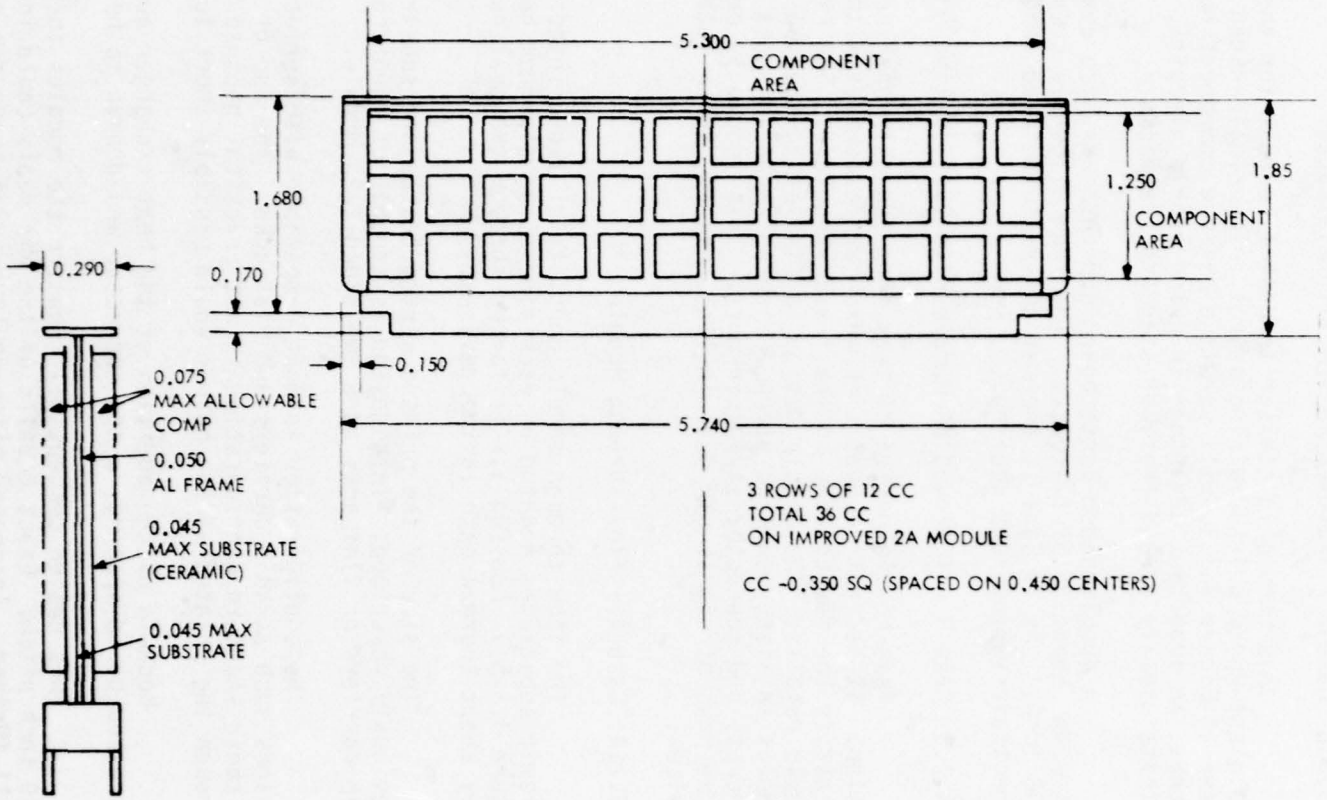


Figure 3.3-2. Improved 2A SEM with Chip Carriers (Case 1)

The thermal analysis of this module encompassed variations of components, use of one and both sides, conduction cooling with copper and aluminum heat sinks, and direct air impingement cooling.

3.3.2.2 Case 2 - Improved 2A SEM with Flatpacks

This module is similar to Case 1, except for the use of flatpacks and glass-epoxy printed wiring boards. The single-sided configuration, as shown in Figure 3.3-3, will permit a maximum component height of 0.190 inches, an important advantage in using hybrid circuits, where package heights usually exceed those of standard flatpacks.

A double-sided centerboard approach was also evaluated, allowing twice the quantity of flatpacks. (Maximum allowable component height is 0.08 inch.) As in Case 1, thermal analysis included conduction as well as direct air-impingement cooling.

3.3.2.3 Case 3 - Improved 2A Module with Dual In-line Devices

This module design differs from the chip-carrier and flatpack design. It has a true heat sink which makes contact with the device, and transmits the device heat to the frame structure. See Figure 3.3-4 for module details. The module design is similar to the two previously-discussed modules in size, mounting pitch, component-mounting area, frame guide concept, and connector style/pin outs. This module is capable of mounting three rows of six 16-pin dual in-line devices, for a total quantity of 18 devices.

3.3.2.4 Case 4 - Flow-Through Module

The flow-through module consists of two printed wiring boards or two ceramic substrates mounted on each side of an aluminum heat exchanger. (See Figure 3.3-5.) Cooling air is forced through the heat exchanger, providing a very short thermal path to the devices.

The size of the printed wiring boards and substrates are the same as previously described. This design is capable of mounting the same number of chip carriers or flatpacks as a two-sided I-2A module.

The configuration is most compatible with surface solder-attached devices such as chip carriers and flatpacks. The use of dual in-line devices in their standard configuration is not practical because lead protrusion through the printed wiring boards would possibly short to the heat exchanger.

Because of the addition of the heat exchanger and resultant increased board spacing, a new connector would have to be developed.

This design concept will require the modules to be mounted on a 0.40 inch pitch. Exact details of the air seals could increase this pitch still further. Increased pitch would provide space for a larger connector

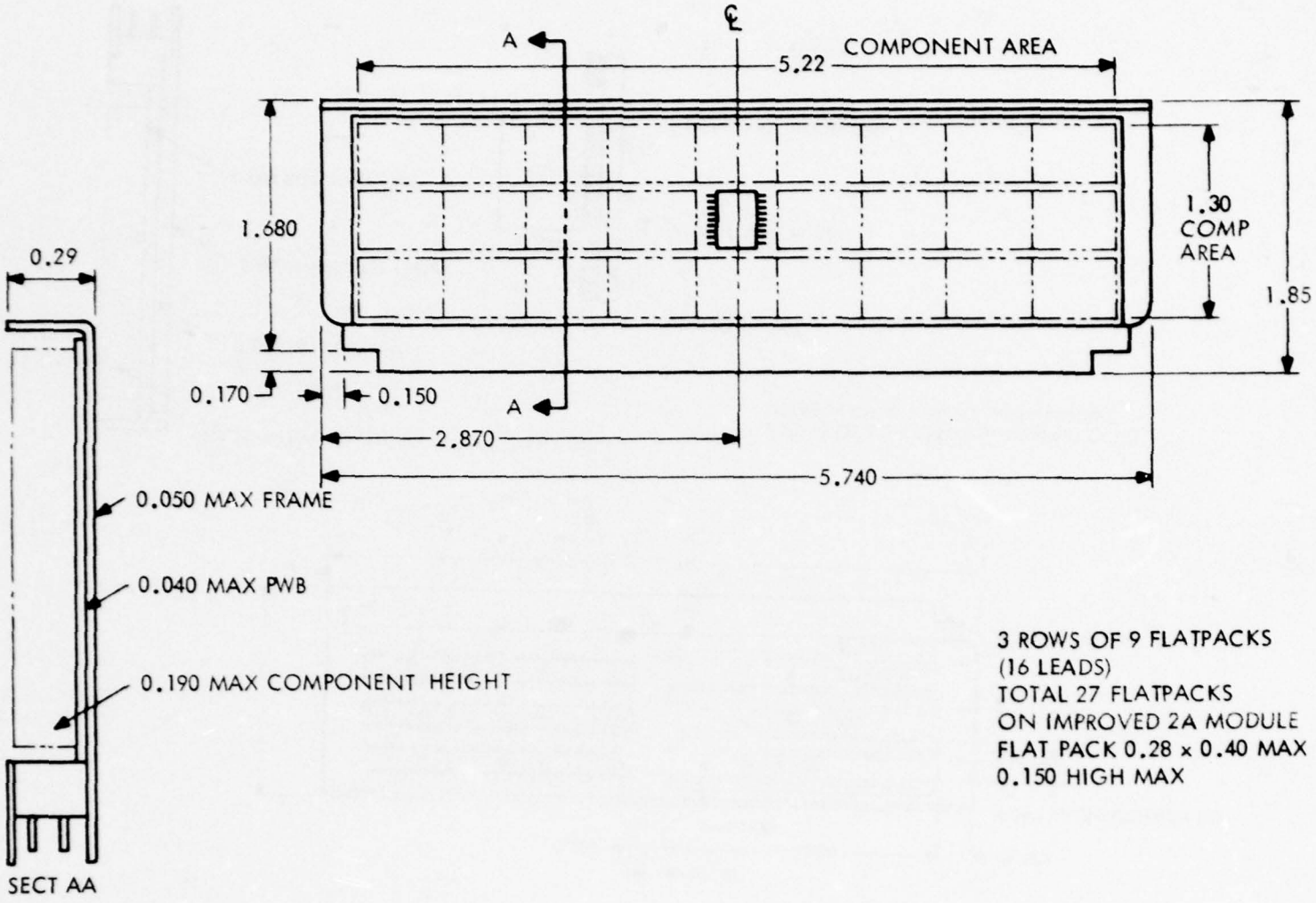


Figure 3.3-3. Improved 2A SEM with Flat Packs (Case 2)

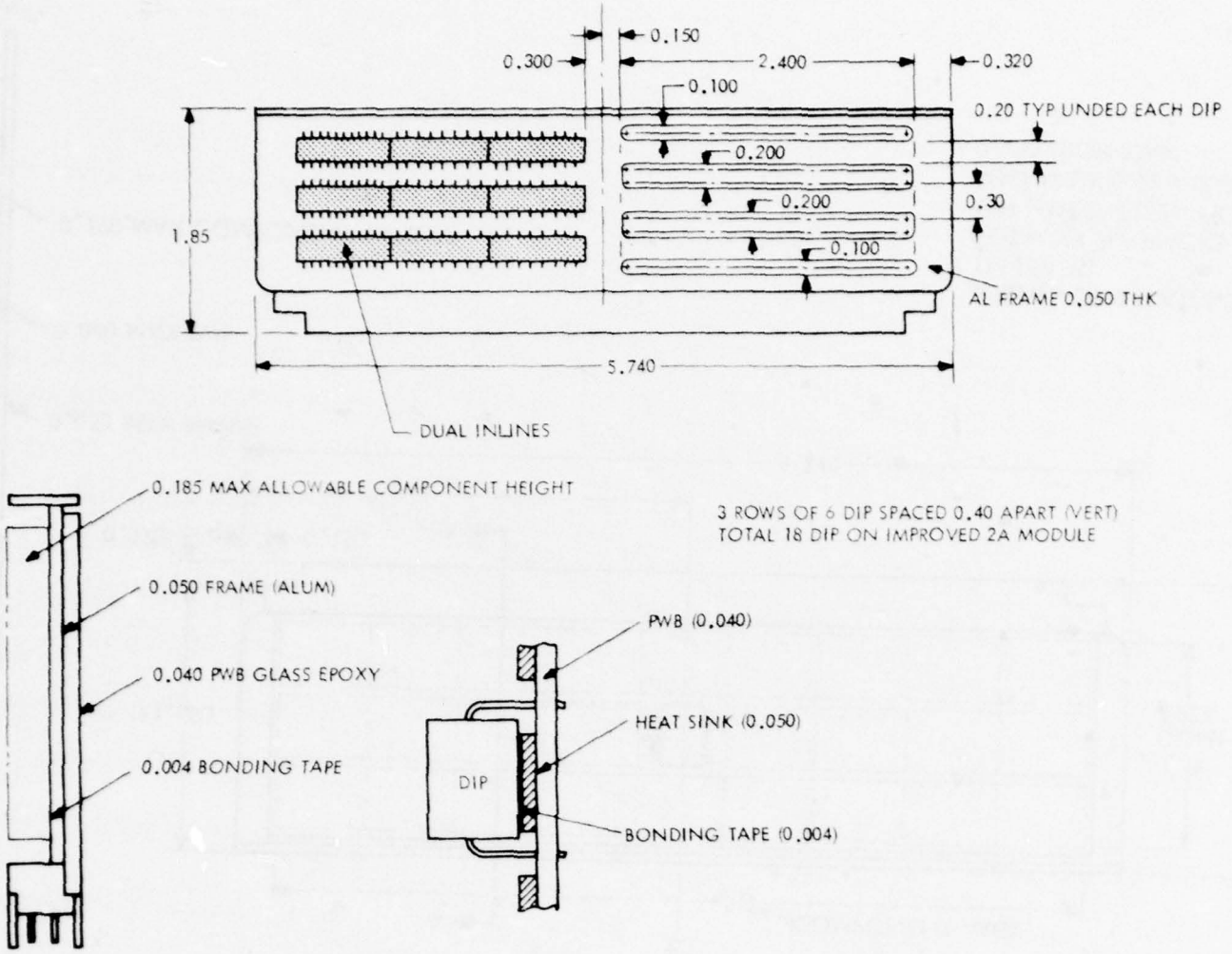


Figure 3.3-4. Improved 2A Module with Dual In-Line Devices

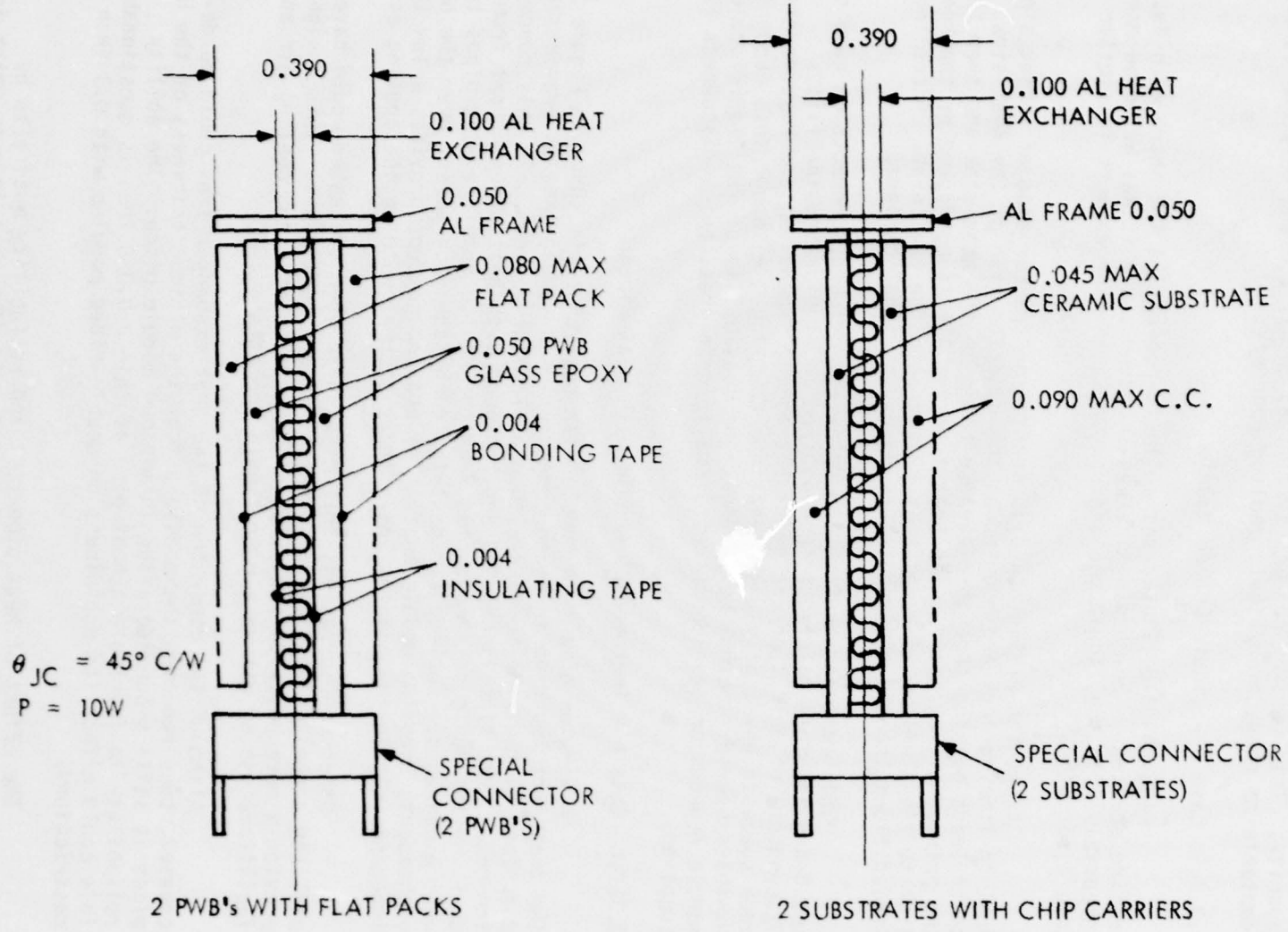


Figure 3.3-5. Flow-Through Module (Case 4)

capacity. This cooling concept is limited to air cooling only and is not adaptable to conduction/liquid cooling concepts.

3.3.2.5 Case 5 - Liquid-Cooled Module

Figure 3.3-6 illustrates a liquid-cooled 3/4 ATR board with dual in-line devices. The module size was selected since it was believed more compatible with the liquid cooling concept. In many ways it is similar to Case 3 for DIPs.

A printed wiring board is mounted on the far side of a heat sink. Dual in-line devices are mounted on the opposite side of the heat sink, with their leads passing through clearance holes in the heat sink and then into the printed wiring board. The heat from the DIP is conducted by the heat sink to the aluminum tube which is brazed onto the heat sink. A cooling liquid flows through the tube, serving as the final coolant.

This concept requires two drip-free quick-disconnects on each end of the board assembly to effect the required level of maintainability. Disconnects of this type are generally large, expensive, and require clearance space to physically disconnect the coupling. Although this concept may exhibit superior thermal peformance, the feasibility of the liquid-cooled module depends on development of a small, drip-free, quick-disconnect fluid coupling.

3.3.2.6 Case 6 - Improved 2A Module with Heat Pipes

A version of a I-2A module with heat pipes is shown in Figure 3.3-7. The component mounting area and connector used is the same as previously described on the I-2A modules with dual in-line devices. In this concept, the metal heat sink is deleted and replaced with heat pipes. Heat from the dual in-line devices is conducted from the device thru the heat pipes to the heat exchangers. Cooling air distributed by the rack passes over the heat exchangers, removing module heat. The cooling concept provides a low thermal impedance within the module, and a short thermal path to the cooling air.

Other configurations that might have been evaluated would have utilized a conductive cooling interface to the heat pipes. This design would provide a more positive isolation of the components from cooling air and also facilitate use of either air or liquid coolants.

Although the dimension of the heat exchanger fins could be decreased, thus reducing the module pitch, the minimum thickness of the heat pipes is still a consideration in minimum module pitch. The ability reliability to fabricate a heat pipe as thin a 0.050 inch is questionable. This could affect its usefulness on double-sided modules with 0.3 inch pitch restrictions.

The effect of heat pipe cost and reliability must also be considered. An attempt was made to determine the cost impact, which is reported in Section 3.3.4. The reliability of the heat pipe, whose

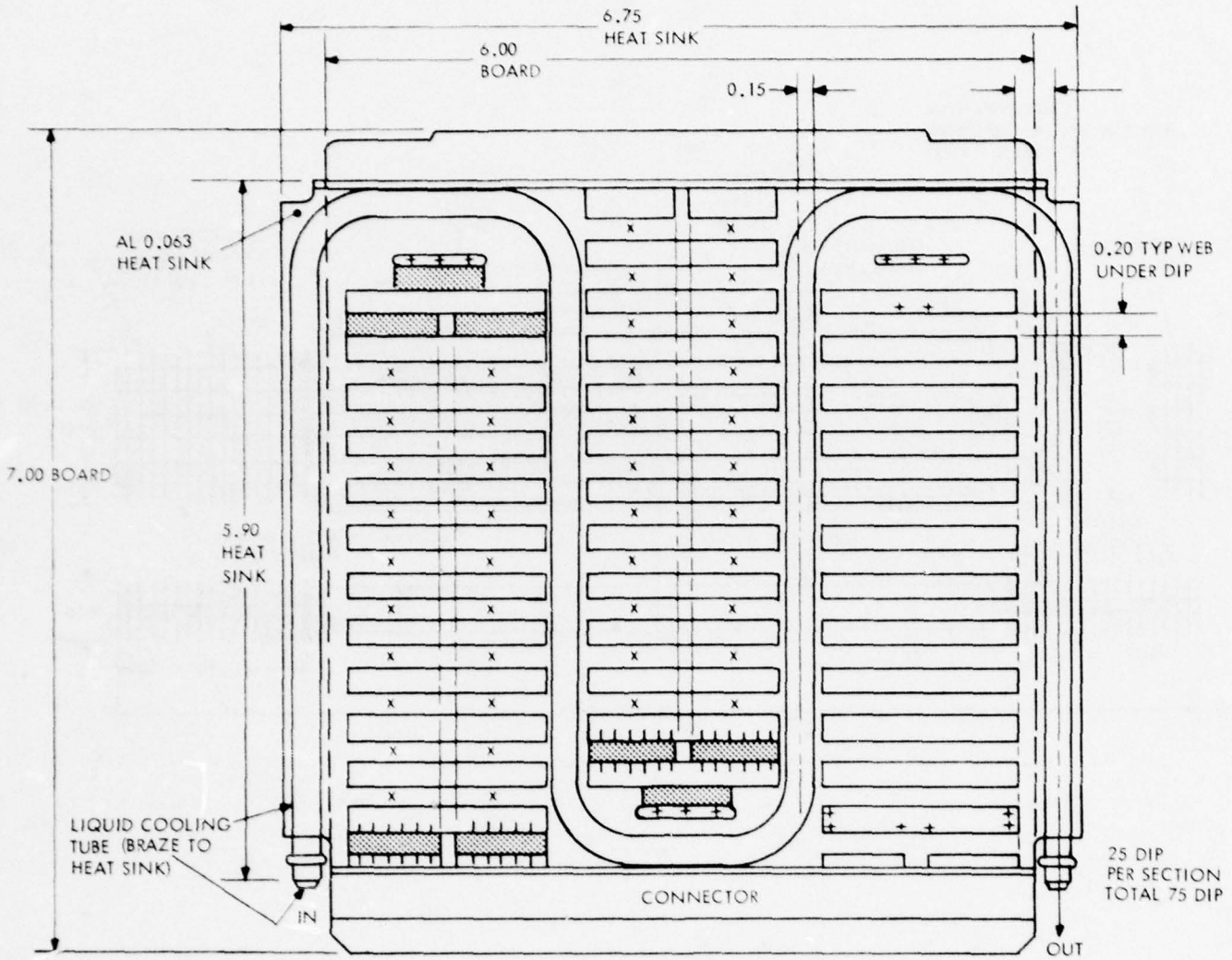


Figure 3.3-6. Liquid Cooled Module (Case 5)

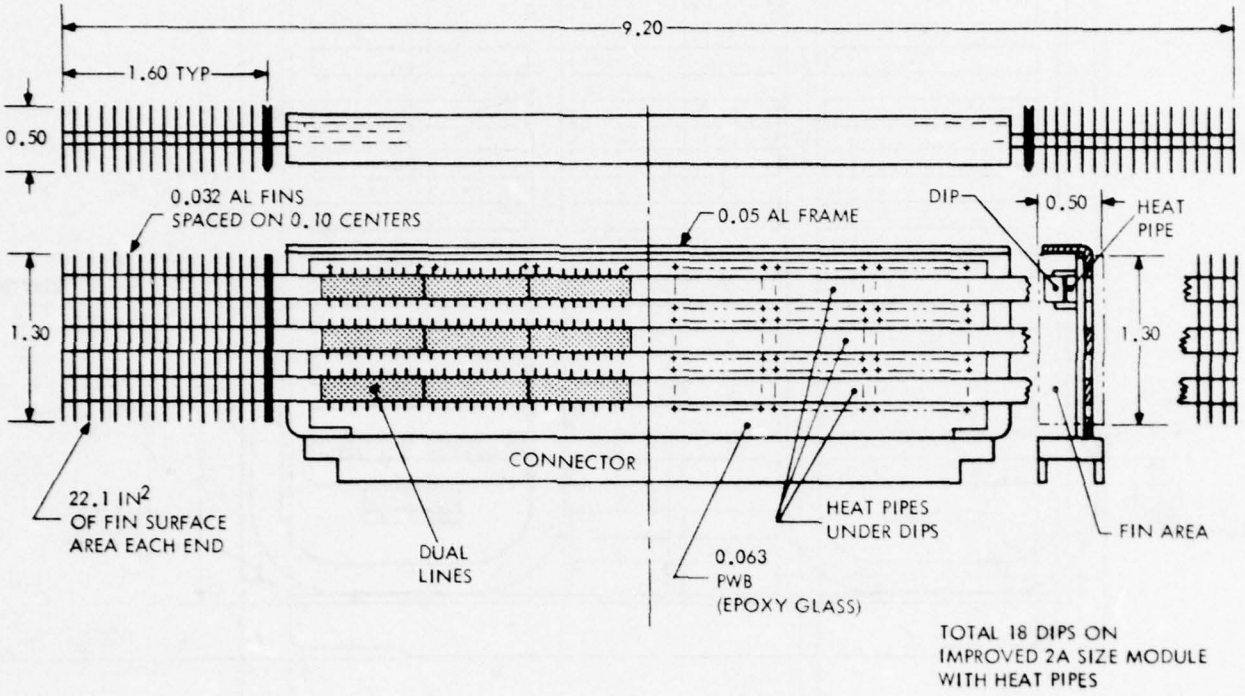


Figure 3.3-7. Improved 2A Module With Heat Pipes (Case 6)

performance can be rendered totally ineffective by a small leak, was not evaluated in this study.

3.3.2.7 Case 7 - Improved 2A Module with Fin-Mounted Heat Exchanger

The addition of a heat exchanger integral to the top surface of a standard I-2A module provides a short thermal path from the circuits to the cooling air without an intermediate mechanical interface. (See Figure 3.3-8.) The component mounting area, frame guide concept, connector and mounting pitch are exactly the same as for a standard I-2A module. Forced cooling air from the rack passes thru the heat exchanger, cooling the module. Although this configuration has the potential of increased thermal performance over the usual conduction cooling, it does not provide isolation of cooling air from the components. The mounting configuration of this design is directly interchangeable with an improved 2-A module. It is also possible to cool this module by conduction from the guide ribs in the usual manner.

The thermal performance of this module was evaluated for both the single-sided and the double-sided chip carrier configurations.

3.3.2.8 Case 8 - Increased-Height Improved 2A Module (HI-2A)

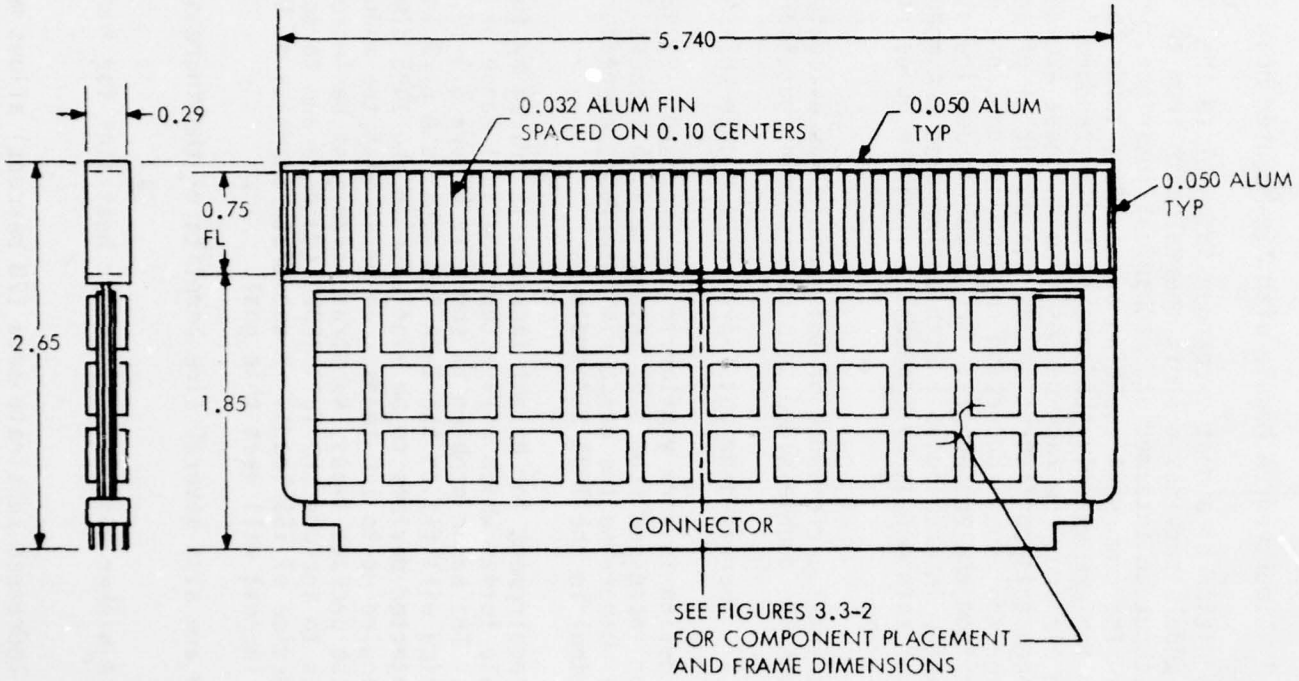
This design is very similar to the standard I-2A SEM, except the height has been increased from 1.85 inches to 2.75 inches. (See Figure 3.3-9.) Otherwise the guide-rib interface, connector, and module pitch is identical to the I-2A SEM features.

The requirement for height increase is driven by the necessity to provide a module format which will accept the full range of proposed JEDEC chip carriers. The basic problem is shown in Figure 3.3-10. The maximum size device which will fit on the I-2A SEM substrate (1.3 inches) is one with 84 leads. Projected devices to be available in the 1985 time-frame are expected to require up to 120 leads. In order that the module configuration may accept these package types, substrate size must be increased. The logical step is to include the full JEDEC standard and to accommodate the maximum size device of 156 leads. A substrate increase of 0.9 inch (1.3 inches to 2.2 inches) will meet this goal.

There are also several side benefits of the increased-height configurations:

1) A higher guide rib and wider heat sink for increased thermal performance.

2) Increased substrate area (70 percent) allows more economical module fabrication; one substrate versus the two substrates of the I-2A.



FIN AREA
$0.290 \times 0.750 = 0.2175\ IN^2$
$0.2175\ IN^2 \times 118$ FIN AREAS $= 25.66\ IN^2$

$25.66\ IN^2$ TOTAL FIN AREA

Figure 3.3-8. Improved 2A Module with Fin-Mounted Heat Exchanger (Case 7)

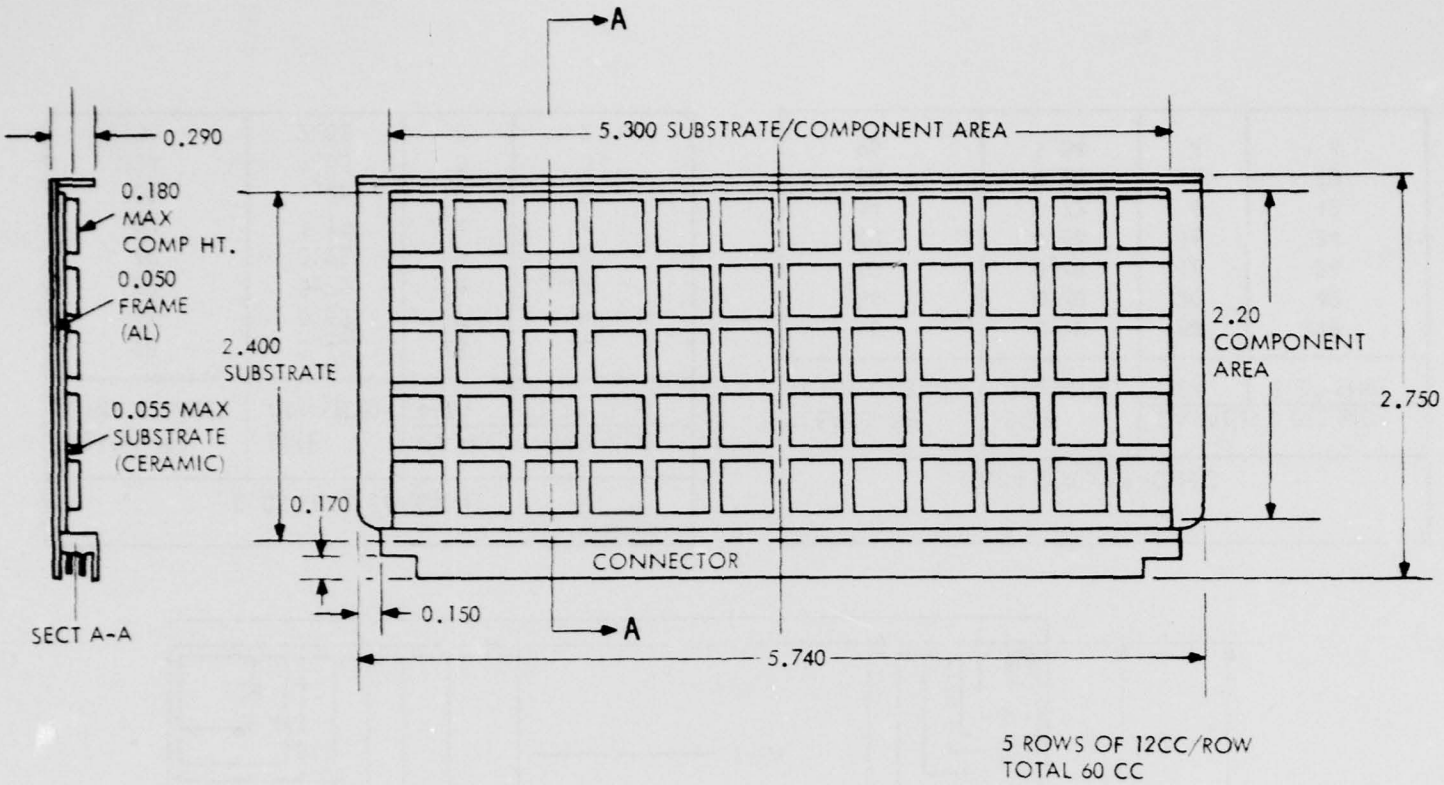
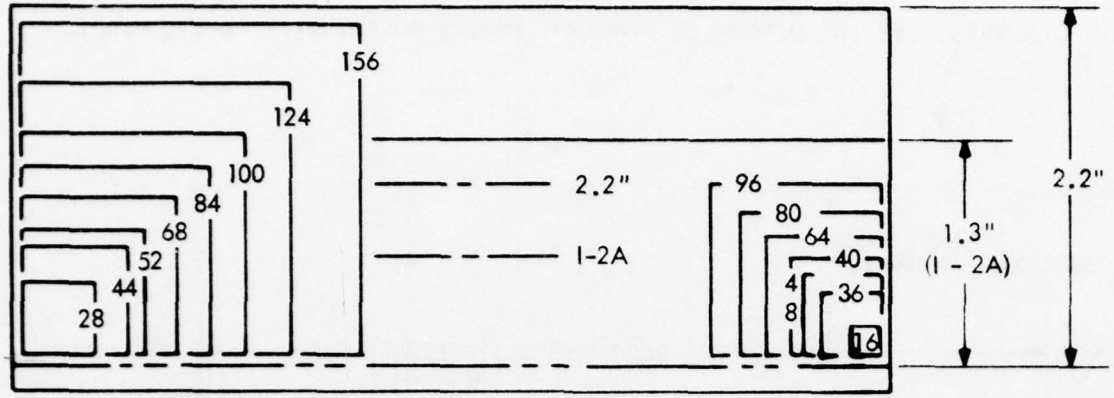


Figure 3.3-9. Increased-Height Improved 2A Module (HI-2A) (Case 8)



0.05 LEAD SPACING			
LEADS PER CHIP CARRIER	SIZE (IN/SIDE)	CAPACITY PER SIDE	
		1-2A	2.2" SUBS
28	0.45	18	36
44	0.65	7	14
52	0.75	6	12
68	0.95	5	10
84	1.15	4	4
100	1.35	0	3
124	1.65	0	3
156	2.05	0	2

0.04 LEAD SPACING			
LEADS PER CHIP CARRIER	SIZE (IN/SIDE)	CAPACITY PER SIDE	
		1-2A	2.2" SUBS
16	0.18	68	119
36	0.40	20	40
40	0.48	16	24
48	0.56	16	24
64	0.72	6	12
80	0.88	5	10
96	1.04	4	4

Figure 3.3-10. Substrate Chip Carrier Capacity

3) No requirement for crossover connections, as required in the double-substrate configuration.

(1) Improved reliability

(2) Effective substrate area not reduced by crossover area requirements. Double-sided I-2A useful area is projected to be equal to the single-sided HI-2A:

I-2A

(1.3 in. - 0.2 in.) x 2 x 5.3 in. = 11.66 sq. in.

HI-2A

2.2 in. x 5.3 in. = 11.66 sq. in.

(3) Lower cost.

(4) Single-sided configuration provides 0.18 inch allowable component height within 0.3 inch module pitch. The height of the leadless type A and B package in the JEDEC outline, dated 7/22/77, are 0.140 inch and 0.125 inch respectively, which exceeds the maximum allowable component height of the double-sided I-2A configuration.

(5) Heat-sink thickness can be increased for additional conduction-mode thermal capacity within the 0.3 inch module pitch limitation.

3.3.2.9 Case 9 - Improved - 2X (Increased-Thickness Heat Sink)

Thermal analysis revealed that the conduction path of I-2A module was insufficient to provide required cooling for the 20-watt modules identified in the system partitioning study.

The I-2X configuration (Figure 3.3-11) was developed to provide the required additional conduction thermal capacity over the standard I-2A.

Although this module requires a 0.4 inch pitch, it does allow the standard I-2A module to be used where possible in the lower power applications.

A system using the I-2X module type would most likely use a standard 0.4 inch module pitch throughout. This will have some degrading effect on packaging density.

3.3.2.10 Case 10 - Improved 2B SEM

In order to maintain complete compatibility with the present Navy SEM program, the I-2B configuration was included in the analysis. This module, shown in Figure 3.3-12, has a thermal advantage over the I-2A variants because of the dual-guide-rib interface. The greater module

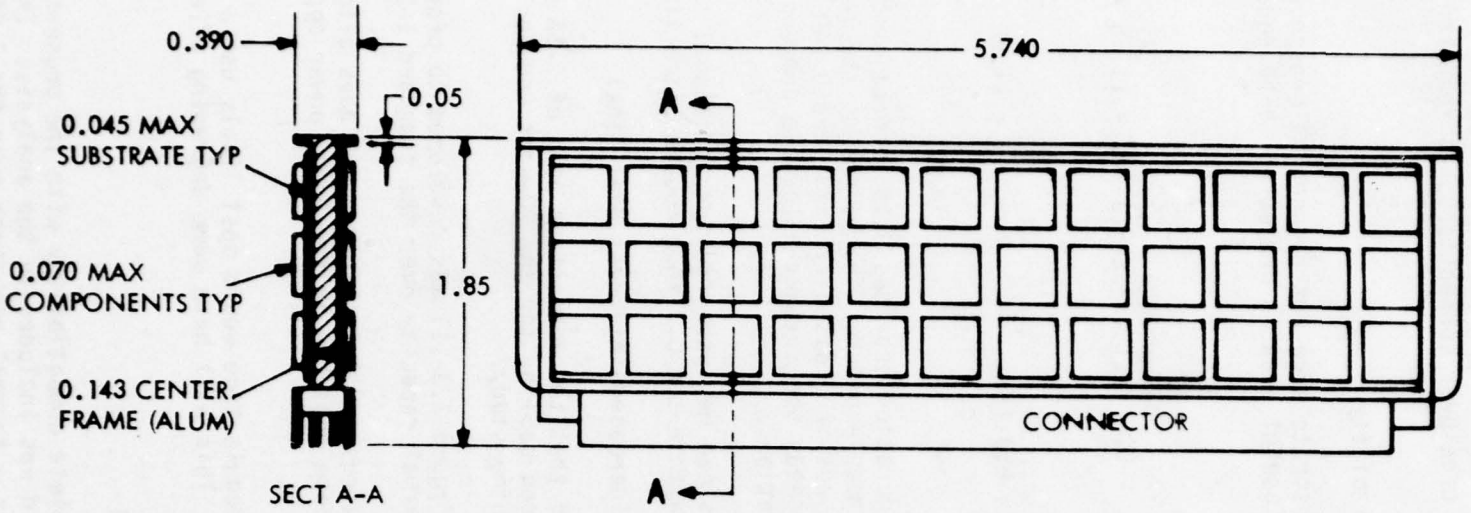


Figure 3.3-11. Improved 2X Module (0.143 Center Frame) Increased-Thickness Heat Sink: Improved 2X Module (Case 9)

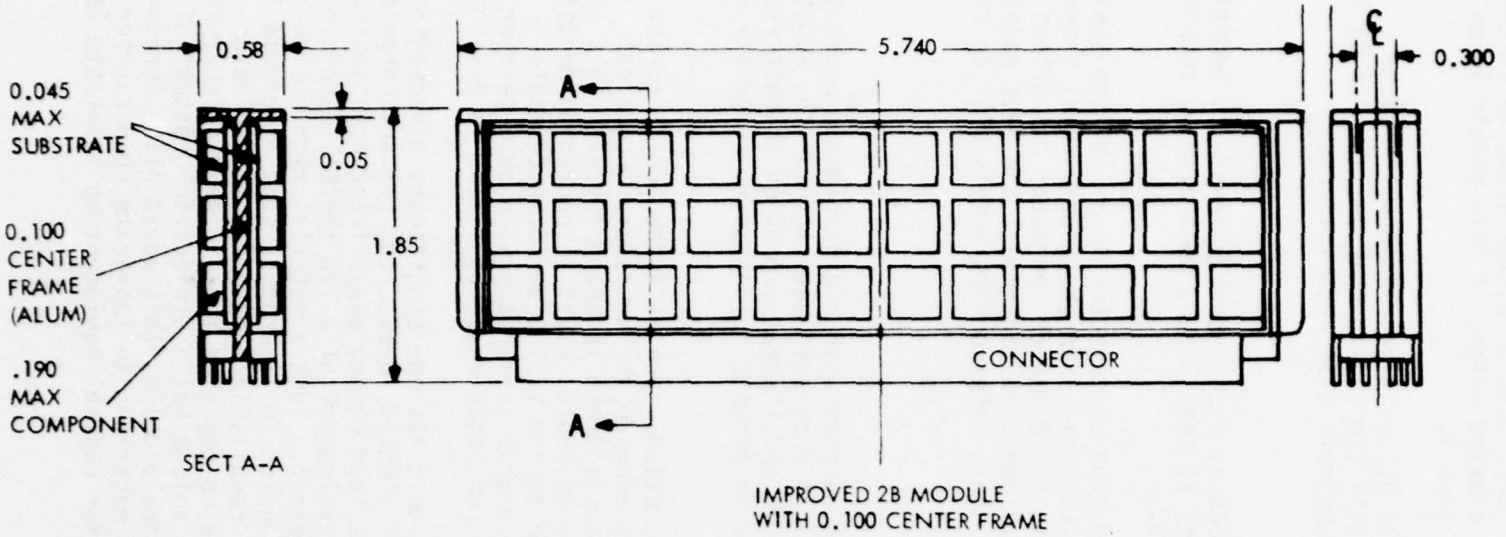


Figure 3.3-12. Improved 2B SEM With 0.100 Center Frame (Case 10)

thickness was used to advantage in providing a thicker frame to further increase thermal capacity. The estimated weight of this module is only slightly different from the I-2X, Case 9.

The greater thickness also allows higher components to be accommodated, but the module is still limited to chip carriers of 84 leads maximum because of basic module substrate size restrictions.

3.3.3 Interconnect Technology

The interconnection methods at each assembly level, in addition to satisfying the special requirements at that level, must also be compatible with the total system requirements.

The chip carrier, an important contributor to minimizing system volume and weight, places special constaints on the module-level interconnect scheme. Similarly, the requirement for a larger connector can affect the module configuration, module pitch, and also can impact the back panel interconnect technology. Each of these interconnect levels will be discussed in the following sections.

3.3.3.1 Module Substrate

The use of a ceramic chip carrier with rigid soldered connection to the substrate has dictated the use of a ceramic material for the substrate also. This ensures a close match of the thermal expansion characteristics of the chip carrier and the substrate to promote solder joint longevity under military temperature extremes.

Alternate package configuration, such as leaded chip carrier and the use of chip carrier sockets, might provide the necessary mechanical resilience to consider higher expansion rate interconnect materials such as glass epoxy. Either of these schemes would result in packaging density and reliability penalties unacceptable to the V/STOL performance goals. Therefore, the use of multilayer ceramic substrates with chip carrier will continue until a new material with suitable characteristics is developed.

The use of multilayer ceramic has one significant disadvantage. Due to the high dielectric constant of alumina (8-10), the primary ceramic used for substrates, assemblies of this type become upper-frequency limited because of capacitive loading. Development of a low thermal expansion, low dielectric constant material is needed. Such a material might be an aramid fiber reinforced epoxy. It is reported in literature that an aramid fiber and 35 percent epoxy resin matrix results in a material with a zero coefficient of expansion. It is also reported that an aramid fiber FR-5 material with a 40 percent fabric volume has a dielectric constant of 3.75. In addition to solving a performance problem, this would allow current module fabricators using glass-epoxy MLB materials to fabricate chip carrier assemblies without major outlays for capital equipment to fabricate ceramic

substrates. (This assumes that equipment and process modifications to fabricate a low expansion MLB would be minor.)

The thermal conductivity of such a material, an important attribute in the performance of conduction-cooled modules, will be lower than that of the alumina ceramic. This must be traded-off against the electrical and mechanical performance advantages. In addition to the lower dielectric constant and lower coefficient of expansion, the density of an aramid-reinforced epoxy is lower than either glass epoxy or alumina ceramic as listed below:

Alumina Ceramic	0.14	lb/in^3
Glass Epoxy	0.07	lb/in^3
Aramid Epoxy	0.05	lb/in^3

This lower density could result in a 30 to 35 percent reduction in module weight over those using alumina ceramic.

3.3.3.2 Module Connector and Back Panel Considerations

The requirement for a connector of larger than 100-pin capacity was discussed in Section 3.3.1.3. Figure 3.3-13 shows the ability of a 124-pin connector to satisfy over 80 percent of the module requirements, including a 20 percent growth factor.

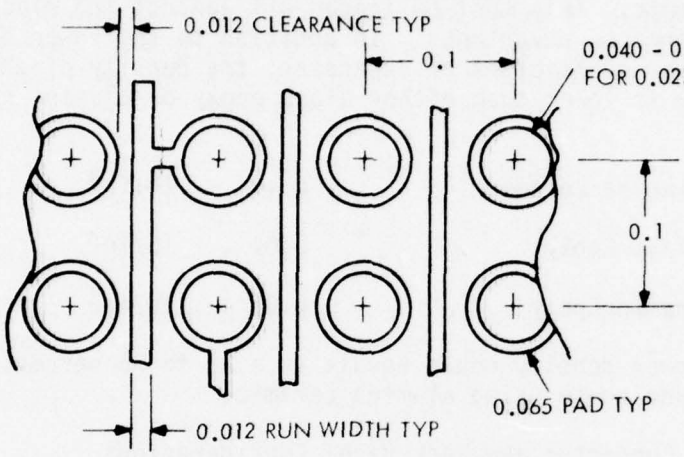
Recent developments in contact technology (Connector Assessment -- Appendix C) indicate that contact spacings less than 0.1 inch are feasible, thus facilitating development of a higher capacity connector within the present 0.3 inch module pitch. AMP and Microdot both have contacts capable of being spaced as close as 0.05 inch centers. Bendix has a similar capability in development featuring their "Brush" type contact, which has extremely low insertion force. Another low insertion force contact, "Hypertac", is available in a smaller size configuration (0.064 inch body diameter) which might be used in a staggered pattern on 0.075 inch centers.

The availability of this contact technology supports consideration of a higher capacity, low insertion force connector for the standard avionics module. The analysis in this report indicates that the failure to support the development of a larger capacity connector for the SAM will seriously limit its partitioning capability in future avionics systems.

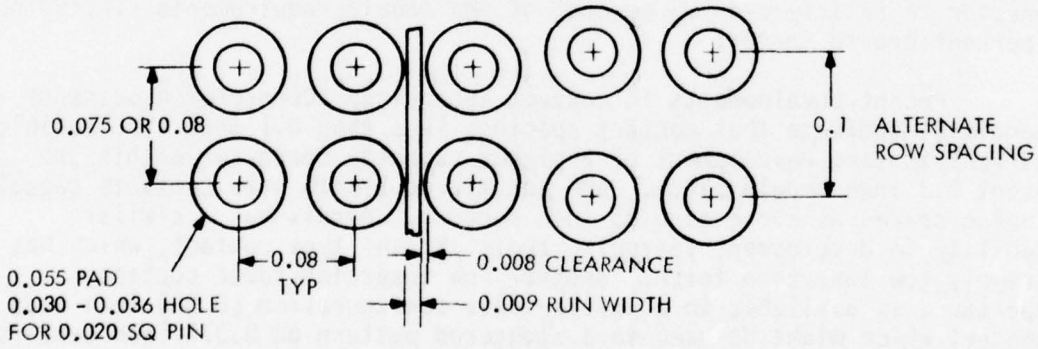
The selection of a connector configuration must address not only the module interface but should also consider the design constraints of the back-panel interconnection methods. Although other competitive interconnection methods are in use, it is expected that wire wrap* (WW) and multilayer boards (MLB) will continue to be the predominant technologies. The present

*Registered Trade Mark Gardner Denver Corp.

A. 100 PIN, 0.1 x 0.1 GRID (I-2A SEM)



B. 124 PIN, 0.08 x 0.08 GRID



C. 132 PIN, TWO ROWS ON 0.075 x 0.075 GRID SIMILAR TO "B" EXCEPT:
RUN WIDTH 0.007
CLEARANCE 0.007

D. 150 PIN, THREE ROWS ON 0.1 x 0.1 GRID ALLOWABLE MLB RUN WIDTH AND CLEARANCES SIMILAR TO "B"

Figure 3.3-13. Connector and Multi-Layer Back Panel, Design Analysis (Sheet 1 of 2)

E. 126 PIN, THREE ROWS ON 0.12 x 0.075 GRID

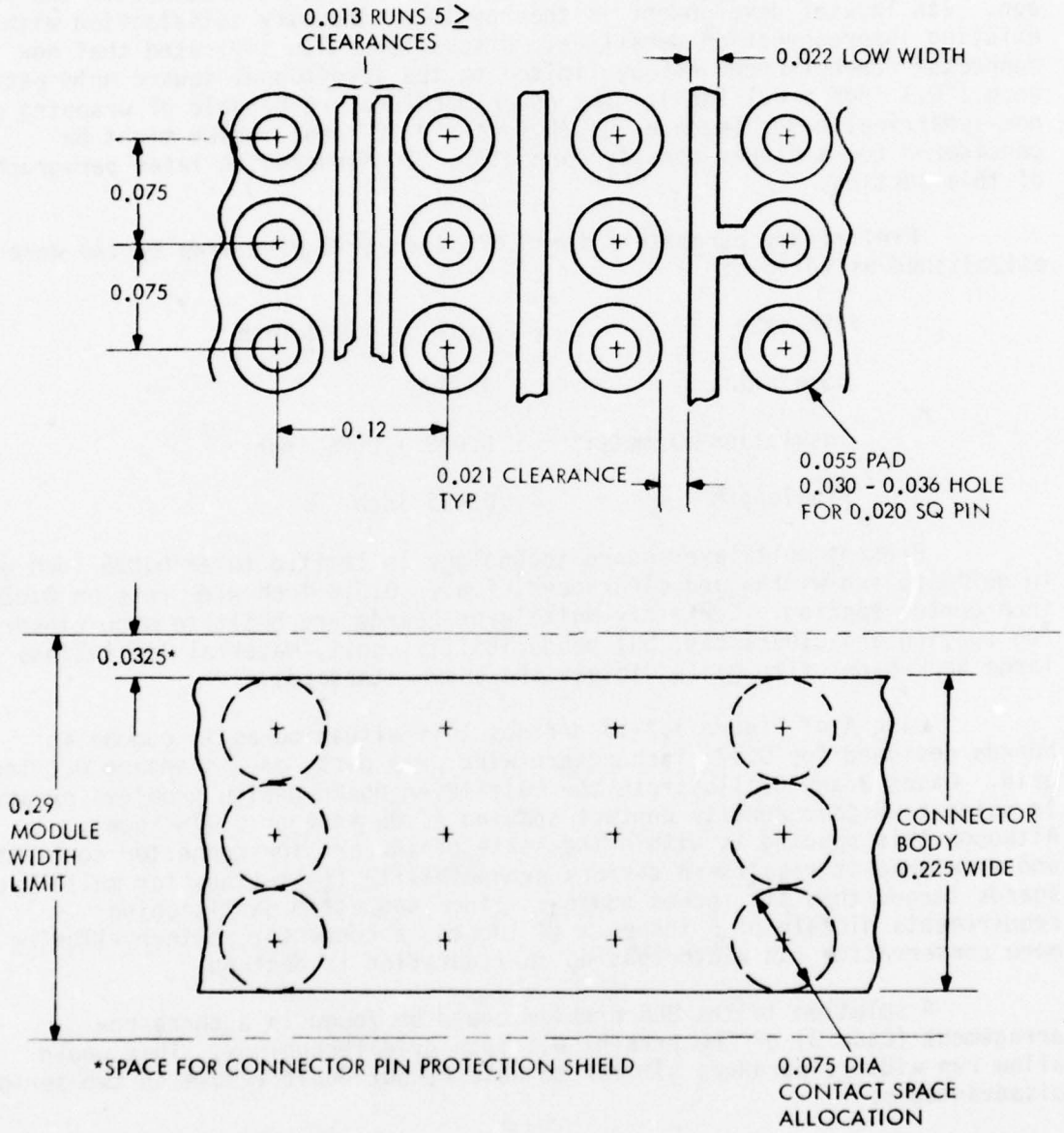


Figure 3.3-13. Connector and Multi-Layer Back Panel, Design Analysis (Sheet 2 of 2)

standards in both MLB and WW are based on a 0.1 inch grid. It is readily apparent that a higher-capacity module connector will force a change in the present grid system if the module pitch is to remain unchanged. Such an increase in density is within the present state of the art in both WW and MLB technologies.

Discussions with Gardner Denver indicate that the feasibility of automatic-machine wire wrap on 0.05 inch grid was demonstrated over two years ago. Its lack of development is the result of industry satisfaction with existing interconnection densities. Discussions also indicated that new connector concepts need not be limited to the traditional square grid pattern (e.g.: 0.1 inch x 0.1 inch). The newer machines are capable of wrapping on non-symetrical grids (such as 0.075 inch x 0.12 inch), which might be considered for a higher-density connector, as discussed in later paragraphs of this section.

Preliminary parameters for 0.075 inch grid wire wrap system were established as follows:

Pin size	0.020 x 0.020 inch
Wire size	32 AWG
Insulation diameter	0.013 ±.0005 inch
Pin length	0.425 inch

Present multilayer-board technology is limited to an 0.025 inch grid in defining run widths and clearances, i.e., .0.013 inch wide runs on 0.025 inch center spacing. Certainly multilayer boards are built to much closer run spacing and clearances, but producibility, cost, material limitations and large back-panel size goals dictate the above standards.

Case A of Figure 3.3-13 defines this situation as is common in boards designed for 0.025 inch square wire wrap pins, on a standard 0.1 inch grid. Cases B and C illustrate the multilayer board design problems created in going to higher density contact spacing (0.08 inch or 0.075 inch). Although this spacing is within the state of the art for connector contacts and wire wrap it results in serious producibility limitations for multilayer boards larger than six inches square. Since subsystem partitioning requirements dictate of 6 inches x 14 inches, a connector pattern allowing a more conservative run width/spacing configuration is desired.

A solution to the MLB problem could be found in a three-row arragement (Case D) of the present 0.1 inch grid technology. This would allow run width/clearances similar to Case A, but would result in two serious disadvantages:

1) Module pitch will increase to 0.4 inch, thus affecting system packaging density and weight.

2) Back-panel length will increase for a given system partitioning thus creating negative cost and MLB producibility factors.

Case E incorporates advantages of earlier configurations. The 0.075 inch contact spacing should allow a three row connector within the 0.3 inch module pitch. The 0.12 inch contact spacing in the row direction would allow a space for either one or two transverse runs as shown. Runs in the longitudinal direction of the connector would be limited to the area between adjacent connectors, which is not a serious limitation.

This contact arragement also ensures compatability with module substrate computer-aided design layout requirements. The three rows of contacts on 0.12 inch pitch will transpose into an in-line configuration of tabs on 0.04 inch centers at the module substrate interface. Thus a 0.01 inch common grid is compatible with the 0.04 inch tab spacing as well as the 0.04 or 0.05 inch chip carrier terminal spacing. This degree of compatibility is not characteristic of cases C and D.

3.3.3.3 Back Wiring Technology Assessment

More than 10 years ago, the multilayer printed wiring concept was developed to meet the demand for complex, very dense interconnections. These multilayer boards have filled the need extremely well as attested by the fact that in the U.S., over $250 million worth of boards are manufactured and used yearly today.

Throughout these last 10 years, the general complexity level and tooling cost of printed circuits and multilayers has steadily increased. At the same time there has been a trend towards a decrease in the number of parts produced for a given type number, particularly for digital systems. In other words, complexity, and therefore the turnaround time and cost of tooling and other front-end operations has been increasing, while the number of boards produced per tool has been decreasing. There has been no easy solution to this dilemma, since most of the tooling and manufacturing steps are incompatible with these new needs.

This situation made it possible for competitive interconnection techniques to achieve considerable penetration and give still competition to multilayer PWB technology.

These technqiues generally use insulated wires to provide required dense point-to-point interconnections. They differ in the methods of wire termination and attachment, but since all are using wire, a generic name for these technologies is discrete wiring.

The growing popularity of discrete-wiring systems is unquestionably a reaction to the printed wiring (PW) problem since these wiring systems offer the equipment designer the prospect of breaking the bottlenecks of time and artwork tooling costs which confront him when trying to get a new design into production quickly. Discrete-wiring systems offer great flexibility, simplified changes and quicker turnaround time. Unfortunately, the penalty imposed by some discrete wiring lies in its associated hardware cost for

pins, sockets, formats, and so on. Furthermore, automatic production equipment for discrete wiring is usually expensive.

A1. Multiwire

Over past years, considerable effort and expense have been incurred to advance the design and layout of wiring for multilayer boards. Digitizers and photoplotters have made some inroads into alleviating the inaccuracy and drudgery of preparing finished master patterns. But the heart of the problem, finding the most efficient (or frequently the only) path from point A to point B, for the most part, is still being done the same way it was 20 years ago. A draftsman or designer laboriously converts a schematic or point-to-point wiring list into a graphic layout for printed conductors.

Increasingly sophisticated computer routing algorithms have been developed to replace the human element in circuit-board layout. However, manual completion of unsuccessful computer routes reintroduces the human error element and the necessity for extensive checking. Finally, the frequent necessity to undo a portion of the computer routing to make manual completion possible greatly diminishes the design time saving that was originally contemplated.

The whole thrust of the multiwire approach was to minimize this problem and divorce as much as possible from manual development of required interconnections.

Multiwire interconnection systems are circuits which are formed by insulated wires "written" on an adhesive-covered insulating base. The wires are terminated or interconnected as necessary by holes which are drilled through them, exposing the wire ends. The holes are subsequently metalized to provide a plated joint between the wire end and the hole walls. These holes are also used for component insertion and the finished multi-wire board is soldered, using the same techniques as with printed circuit boards.

The finished board closely resembles a PW card and is interchangeable with one, as far as assembly procedures and packaging hardware are concerned. The assembled board can be hand-, wave- or dip-soldered. Component replacement and field change procedures are the same as those for PW boards.

General Electric is presently evaluating the suitability of multiwire for use in severe military environments. This program emphasizes the long term reliability of the interconnections under conditions of wide range temperature cycling. It is expected that the first phase of this effort will be concluded in calendar year 1977.

A2. Stitch-weld

Presently there are two versions of stitch-welding systems, differing in type of PW board used, and how welding termination is made.

The first version was originally developed by the Jet Propulsion Laboratory for aerospace applications, where quick turnaround and high reliability was required over short runs. In the past years, stitch-welding has been expanded for general commercial usage. A double-sided printed circuit board with press-fitted terminals is used as the basic vehicle. The terminals are normally gold-plated nickel or stainless steel to provide the combination of weldability and solderability required. Nickel wire for weldability is usually used, with Teflon or nylon/urethane insulation.

The wire is fed from a spool through the center of an electrode which forms one electrode of a discharge-type welding system. The other electrode contacts the opposite end of the pin from the bottom side. The insulation is broken down by mechanical pressure and heat, and a metal-fusion joint between the terminal and the pin is formed at the point of contact. A continuous run of wire is used from the start pin to the end pin of a network or string, with the joints made at all intermediate points without cutting the wire. An advantage of stitch-welding is that it can be performed on 0.050 inch centers, and wires can be removed and rewelded up to about four times.

In the second, more recent version, the stitch-welding process welds the wire to tabs on the board surface instead of to the press-fitted pins. The process begins with conventional glass epoxy, laminated on both sides with a proprietary 0.005 inch thick stainless steel. The laminate is drilled with the desired hole pattern in the same way as any conventional board. The drilled laminate is plated on the surface and in the holes with 0.001 inch to 0.002 in. of copper over a nickel flash.

Next, the plated laminate is selectively etched, first, to remove the undesired stainless steel, nickel and copper to form the 0.08-inch by 0.18-inch pads, power planes and other circuitry; and second, to remove the nickel and cooper plating from one end of the pad, to form a 0.08-inch by 0.1-inch weldable area on the pad, on both the front and back of the board. The copper-plated areas on the board are also solder-plated. Characteristically, stainless steel will not solder and remains clear for welding. Wires are now welded to the pads to form the interconnections. The strength of the stitch-wire bonds is five pounds.

A3. Solder Wrap

The Solder Wrap process was developed by United Wiring and Manufacturing in 1973 as a manual wiring process for prototype circuit boards. By late 1976, they had developed the necessary software, special hardware and automatic machines to make the Solder Wrap process competitive with the other automatic discrete wiring processors.

Basically, Solder-Wrapping consists of stringing a fine insulated wire to the solder tails or leads of sockets or pins previously inserted into a specially patterned PC board, having wiring guides between the rows of leads.

The wires are soldered to the solder tails by a probe that thermally strips away the wire insulation at the soldering point while the sockets or pins are soldered in place. The resulting loop of connections is cut at the proper places.

Automatic Solder-Wrap is the only automatic wiring process available with a complete in-line test of wiring interconnections. All Solder-Wrap machines have four lights on each wiring head that indicate failures of the parameters checked by the self-test circuitry. These lights indicate, respectively, missing pin, broken wires, stripped wires, and solder errors.

A4. Conclusions

Although the discrete wiring methods can provide schedule relief and the flexibility for making circuit changes, the multilayer backpanel will probably remain the most viable candidate for production type equipment for cost and reliability reasons. The discrete approach, however, should be taken into consideration for flyable test models, feasibility models or other small quantity equipments where delivery time can be improved or where a high degree of confidence in the circuit design is lacking.

3.3.4 Producibility Considerations

3.3.4.1 Chip carrier IC's (one or two sides on ceramic substrates).

The flow diagram shown in Figure 3.3-14 illustrates the major operations required to assemble a module with chip carrier packaged IC's on one or both module surfaces.

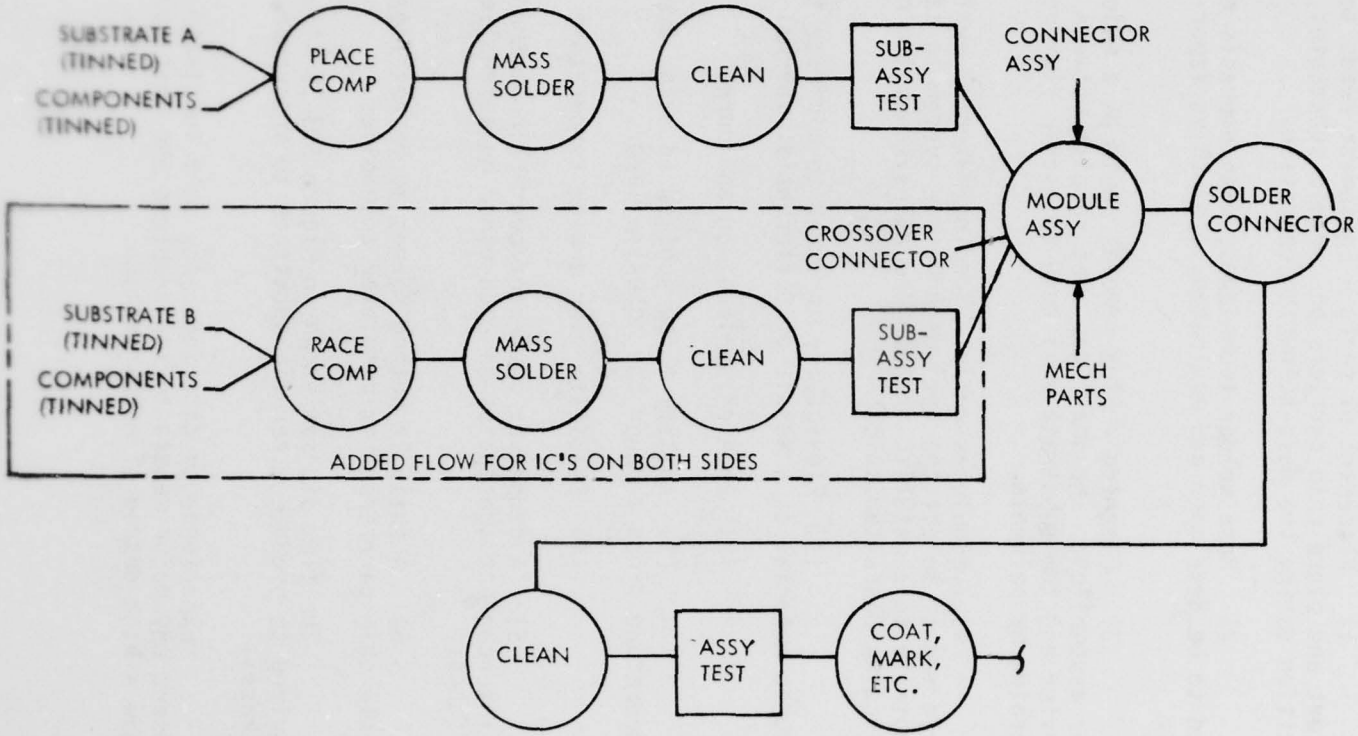


Figure 3.3-14. Simplified Flow, Assembly of Chip-Carrier IC's on Ceramic Substrates

Since chip carriers are relatively new, several areas require development. They are as follows:

1) Placement of parts - Equipment needs to be developed which will orient and place chip carriers on ceramic substrates, and insure maintaining position during the mass-soldering operation.

2) Mass solder techniques, with emphasis on a fluxless process, need to be developed and evaluated, i.e. IR vs Vapor-Phase vs Tunnel ovens, etc.

3) Cleaning - Flux removal could be a major problem on chip carrier assemblies. The small gap that results between the bottom of the chip carrier and the substrate will tend to entrap flux residues, and resist flushing by solvents.

4) Module assembly - Bonding material evaluations need to be performed to select the optimum adhesive system to attach the ceramic substrate to a metallic frame. The adhesive system needs to have the following characteristics:

(1) Flexibility in order to minimize the stresses in the ceramic material as a result of differential thermal expansion.

(2) Ease of application and cure.

(3) Ability to be applied in thin layers to minimize temperature drops through the adhesive layer.

(4) Stability over a wide temperature range.

5) A crossover connector/connection method needs to be developed to interconnect substrates to each other on assemblies that have IC's on both surfaces.

6) A suitable method neeeds to be developed to remove and replace single chip carriers from completed assemblies.

The flow diagram shown in Figure 3.3-15 illustrates the major steps required to produce a ceramic substrate to interconnect chip-carrier packages.

Experience to date indicates that substrate fabrication does not present any major manufacturing problems and that equipment exists that would allow a high degree of mechanization.

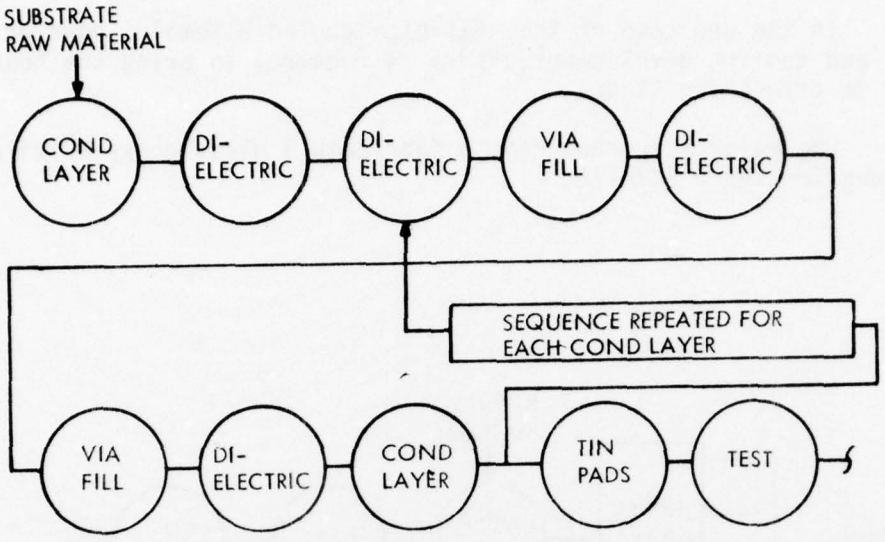


Figure 3.3-15. Simplified Flow, Substrate Fabrication for Ceramic Chip-Carrier Package Substrate

3.3.4.2 Dual Inline Package IC's - (Through Hole Mounted Glass Epoxy ELB.)

The flow diagram shown in Figure 3.3-16 illustrates the major operations needed to assemble a module with DIP IC's.

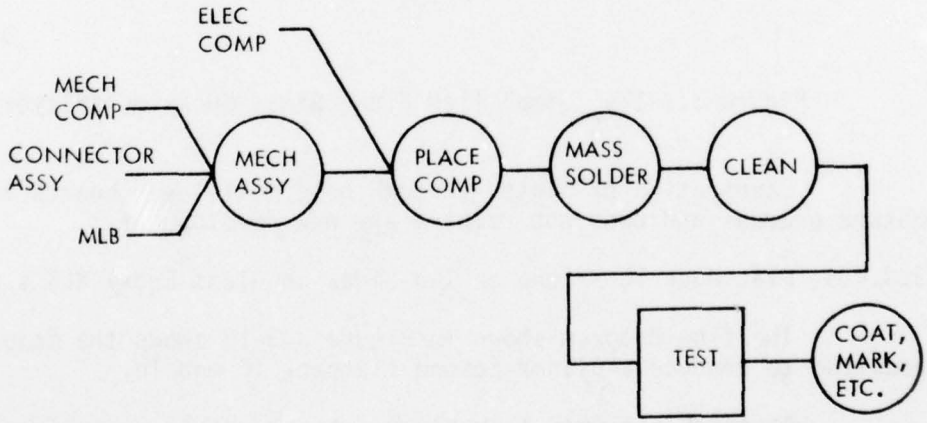


Figure 3.3-16. Simplified Flow, Assembly of Dual In-Line Packages on Substrates

Assembly of DIP's into modules using PWB/MLB is a mature process and requires no development. A large variety of equipment is available for mechanized assembly.

In the one case of the heat-pipe cooled assembly, however, some design and tooling development effort is required to bring the heat pipe design to production stage.

The major step required to fabricate a glass epoxy multilayer board are shown in Figure 3.3-17.

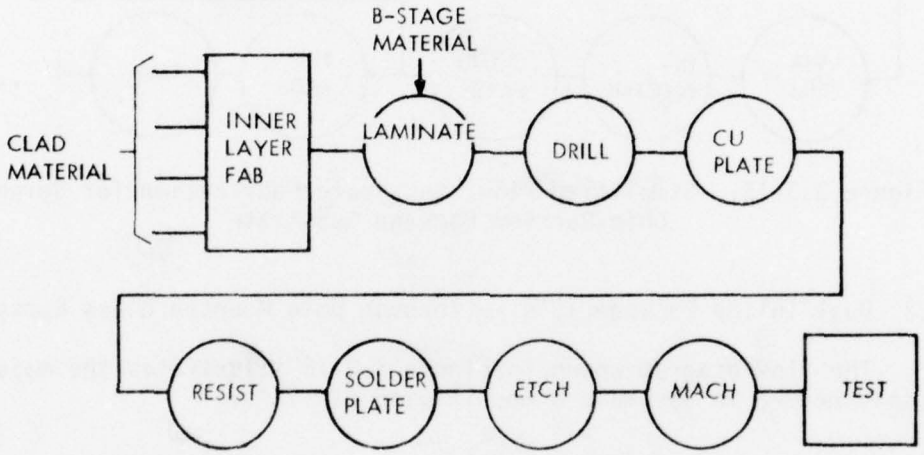


Figure 3.3-17. Simplified Flow, Glass Epoxy Multilayer Board

Fabrication of plated-through hole multilayer boards is also a mature process and does not require any new development.

3.3.4.3 Flat Pack IC's (one or Two Sides on Glass Epoxy MLB's planar joined)

The flow diagram shown in Figure 3.3-18 shows the major operators required to produce a planar-joined flatpack IC module.

Flatpack assembly to MLB's is also a mature process and would require no new development. However, it should be pointed out that mechanization for handling and planar-soldering of flat packs to glass epoxy boards essentially does not exist, and is not likely to be developed. Because of this, labor content in assemblies of this type will always be high. In addition, the cost of IC's packaged in flat packs is estimated to be three times that of an IC packaged in DIP form.

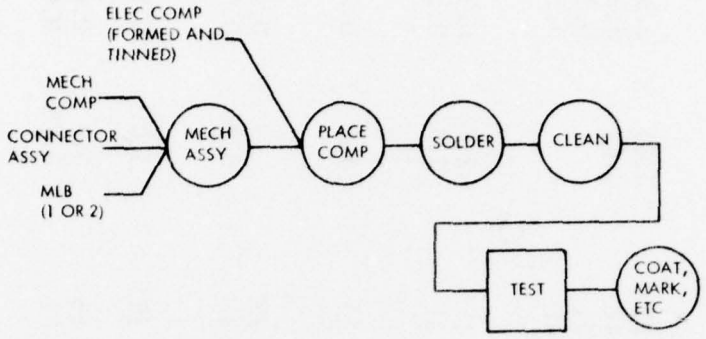


Figure 3.3-18. Simplified Flow, Assembly of Flatpacks on Planar-Joined Multilayer Board

3.3.5 Module Evaluations and Conclusions

The mechanical and thermal performance parameters of each module configuration was determined and is presented in Tables 3.3-1 and 3.3-2.

3.3.5.1 Mechanical Characteristics

Table 3.3-1 addresses the mechanical characteristics of the various modules studied. In addition to the basic characteristics such as IC capacity, weight, volume, and pitch; the packaging efficiency and cost performance of each module type was evaluated.

The packaging efficiency was rated in three ways; IC quantity relative to module volume, module weight and rack requirements.

The last value, which assumes a direct module access maintenance capability, is a rating of the amount of accessible rack face area required to accommodate a certain quantity of integrated circuits. This parameter is of great importance when addressing maintenance accessibility area requirements of aircraft installations. A higher value relates to less area required to effect the total equipment maintenance function. This parameter favors a module of minimum pitch, minimum span and maximum depth.

As one might expect, the volumetric packaging density of chip carriers , for a given module configuration, is the highest, followed by flatpacks and then DIPS. This sequence does not hold for a comparison based on weight. The packaging efficiency of flatpacks is higher than that of chip carriers; 360 vs 280 ICS/lb for the double sided I-2A SEM (Cases 1 and 2). This trend reversal is due to the additional weight of the multilayer alumina substrate of the chip carrier modules (discussed in Section 3.3.3.1).

Table 3.3-1. Module Mechanical Characteristics Summary

Case No.	Module No.	IC Capacity	Weight lb	Volume in^3	Packaging Eff. IC/in^3	Packaging Eff. IC/lb	ICs/in^2 Rack Area	Relative Cost I-2A Dips	Pitch
1	I-2A Chip Carriers								
	AL 1 Side	36	0.17	3.2	11.3	212	21	0.63	0.3
	2 Sides	72	0.25	3.2	22.5	288	42	0.61	0.3
	CU 1 Side	36	0.35	3.2	11.3	103	21		0.3
	2 Sides	72	0.43	3.2	22.5	167	42		0.3
2	I-2A Flatpacks								
	1 Side	27	0.11	3.2	8.4	245	15	2.7	0.3
	2 Sides	54	0.15	3.2	16.8	360	31	2.4	0.3
3	I-2A DIPs								
	1 Side	18	0.17	3.2	5.6	105	10	1.0	0.3
4	Flow Thru -								
	Flatpacks	54	0.15	4.3	12.6	360	23		0.4
	Chip Carriers	72	0.25	4.3	16.7	288	31	0.66	0.4
5	Liquid Cooled								
	- 3/4 ATR	75	1.2	28.3	2.6	62	18	1.0	0.6
	I-2B Equiv								
	- DIPs	18	0.3 est	6.4	2.8	60	55	1.7	0.6
	- C.C.	72	0.4	6.4	11.2	180	21	0.75	0.6
6	Heat Pipe Cooling								
	- DIPs	18	0.33	8.5	2.1	54	4	1.5	0.5
7	Fin Mounted Heat Exchanger								
	- CC 1 Side	36	0.22	4.6	7.8	164	21	0.68	0.3
	- 2 Sides	72	0.30	4.6	15.6	240	42	0.64	0.3

Table 3.3-1. Module Mechanical Characteristics Summary (Continued)

Case No.	Module No.	IC Capacity	Weight lb	Volume in^3	Packaging Eff. IC/in^3	Packaging Eff. IC/lb	ICs/in^2 Rack Area	Relative Cost I-2A Dips	Pitch
8	HI-2A CC 1 Side	60	0.25	4.7	12.8	240	35	0.57	0.3
	FP 1 Side	45	0.16	4.7	9.6	281	26	2.3	0.3
	DIPS 1 Side	30	0.26	4.7	6.4	115	1/	0.85	0.3
9	I-2X (0.142 thk heat sink) CC 2 Sides	72	0.32	4.3	16.7	225	31	0.61	0.4
10	I-2B (0.100 thk heat sink) CC 2 Sides	72	0.34	6.4	11.3	212	21	0.61	0.6

Table 3.3-2. Module Thermal Characteristics Summary

Case No.	Module Type	Thermal Resistance °C/W		Max Module Pwr +110°C Junction			Thermal Eff. Watts/Pound	
		Convection	Conduction	Convection +50°C avg Air Temp	Conduction +45°C Cold Plate	Max Pwr Conduction +71°C Cooling Air	Convection	Conduction
1	I-2A Chip Carriers							
	AL 1 Side	2.9	5.7	20.7W	11.4W	5.4W	122	67
	2 Sides	1.4	4.2	42.8W	12.5W	6.8W	171	50
	CU 1 Side	2.9	5.2	20.7W	15.5W	5.8W	59	44
	2 Sides	1.4	3.7	42.8W	17.6W	7.5W	100	41
2	I-2A Flatpacks							
	1 Side	4.5	8.2	13.3W	7.9W	4.0W	121	72
	2 Sides	2.2	6.3	27.3W	10.3W	5.0W	182	67
3	I-2A DIPs							
	1 Side	3.2	8.2	18.7W	7.9W	4.0W	110	46
4	Flow Thru -							
	Flatpacks	2.5	-	17.2W	-	-	115	115
	Chip Carriers	1.3	-	33.0W	-	-	132	132
5	Liquid Cooled							
	- 3/4 ATR	-	0.6	-	108W	-	-	90
	I-2B Equiv							
	- DIPs	-	2.5	-	26W	-	-	87
6	Heat Pipe Cooling							
	- DIPs	1.11	-	21.7W	-	-	66	66
7	Fin Mounted Heat Exchanger							
	- CC 1 Side	3.5	5.7	17.1W	11.4	5.4W	78	78
	- 2 Sides	3.0	4.2	20.0W	12.5	6.8W	67	67

Table 3.3-2. Module Thermal Characteristics Summary (Continued)

Case No.	Module Type	Thermal Resistance °C/W		Max Module Pwr +110°C Junction		Max Pwr	Thermal Eff. Watts/Pound	
		Convection	Conduction	Convection +50°C avg Air Temp	Conduction +45°C Cold Plate	Conduction +71°C Cooling Air	Convection	Conduction
8	HI-2A							
	CC 1 Side	1.7	3.3	35.3W	19.7W	9.3W	141	77.6
	FP 1 Side	2.6	4.8	227W	13.5W	6.8W	142	84
	DIPS 1 Side	1.9	4.8	31.6W	13.5W	6.8W	122	52
9	I-2X (0.142 thk heat sink)							
	CC 2 Sides	1.4	3.3	42.8W	19.7W	8.1W	134	61
10	I-2B (0.100 thk heat sink)							
	CC 2 Sides	1.4	2.8	42.8W	23.2W	11.0W	126	68

The efficiency rating based on IC quantity per unit of rack area would appear to favor the module configurations with chip-carrier type devices carried on both sides of modules, with modules on 0.3 inch pitch, i.e., Cases 1 and 7. The ability to achieve the 0.3 inch module pitch is questionable, if one considers the limited component height of this module configuration relative to chip-carrier package height requirements (discussed in Section 3.3.2.1). It is anticipated that a pitch in excess of 0.4 inches will be required to accommodate JEDEC chip carriers on both sides of an I-2A, thus reducing this rating value from 42 to approximately 31 ICs/in^2. This value is below the performance of the somewhat higher module of Case 8. The HI-2A, being a single-sided configuration, can accommodate the maximum height chip carriers without affecting the 0.3 inch module pitch.

The cost of the various module configurations was determined on a cost-per-circuit basis and then normalized relative to the common DIP I-2A module (Case 3). This data, presented in the next to the last column of Table 3.3-1, shows that:

1) More complex cooling schemes (liquid, heat pipe) impose a cost penalty because of the added mechanical complexity.

2) Flatpack configurations are prohibitively high in cost due to the cost penalty characteristic of flatpack devices (3X DIP cost).

3) Chip carrier type modules exhibit lowest cost per device. Although the projected cost of chip carrier is assumed equal to DIPs, the relative cost per chip carrier device is lower because of the greater quantity of chip carriers per module (lower mechanical overhead).

4) The effect of mechanical simplicity (one substrate) results in the HI-2A having the lowest cost per IC characteristic.

3.3.5.2 Thermal Characteristics

Table 3.3-2 lists the primary module thermal characteristics for both direct air-impingement forced convection and conduction cooling modes. The maximum allowable module power dissipations, based on +110°C maximum junction temperature, are listed for three conditions:

1) Direct air-impingement cooling at an average air temperature of +50°C. This coolant temperature was selected to prevent moisture condensation problems within the equipment.

2) Conduction cooling to a liquid cooled cold plate of +45°C. Again this temperature selection is based on moisture condensation considerations.

3) Conduction cooling to an air-cooled heat exchanger with a maximum air temperature of 71°C.

This last condition is typical of air cooled WRAs operating under MIL-E-5400 Class 1 environments. This condition was included since it is representative of what might be experienced with non-integrated rack avionics, such as flight control. This type of equipment will most likely be packaged in smaller WRAs and located in separated areas of the aircraft for redundancy vulnerability/survivability considerations. Such locations may not be readily serviced by the primary ECS, making cooling dependent upon the local environment with cooling fans to provide required air flow.

The last two columns of Table 3.3-2 provide a relative figure of merit of the thermal efficiency of the various module configurations relative to their weight. This factor is considered to be of significant importance in an avionics application where both weight and reliability (thermally related) are of prime importance.

It shall be noted, in reviewing the data of Table 3.3-2, that the convection-cooling method is significantly more effective than conduction. The ratio of thermal resistance, and consequently maximum module power dissipation, are in the range of two or three to one in favor of direct-impingement convection cooling.

Of the module types using chip carriers, the I-2A using the aluminum heat sink has the highest thermal efficiency in the convection-cooling mode (171 watts/lb). This is followed by the HI-2A (Case 8) with Case 9 a close third. This high performance of the I-2A is the result of a minimum-sized conduction path which is reflected in its relatively low conductive power-dissipation limit (12.5 W).

In the conduction-cooling mode, Case 4 and Case 5 offer the highest performance potential, but it must be pointed out that these two configurations are specifically designed for a particular coolant. They do not offer the adaptability to multiple coolant types, nor do they afford the same degree of coolant isolation as do the true conduction-cooled configurations of Cases 1, 8, 9 and 10. Of these four configurations, the HI-2A offers the greatest conduction-cooling performance. This is a result of the increased width of the thermal path in comparison to the I-2A and its derivatives. It should be noted that only Cases 8, 9, and 10 have sufficient conduction capacity (+45°C coldplate) to meet the 20-watt module requirement identified in the system partitioning study. This was of prime importance in selecting the module configurations which were evaluated in the system level tradeoff studies.

The details of the thermal analysis of the various module configurations is contained in Appendix D. Additional thermal tradeoff considerations are discussed in the remainder of this section (3.3.5).

3.3.5.3 Qualitative Evaluation

Table 3.3-3, which lists system level module application qualities, was developed as a screen in selecting those module configurations that would be evaluated in the rack-level weight, volume and thermal performance

Table 3.3-3. Module Qualitative Comparison

Configuration	Case Number 1	4	5	6	7	8	9	10
Characteristics	I-2A	Flow Thru	Liquid Cooled (DIPs)	Heat Pipes (DIPs)	Fin Heat Exchanger	HI-2A	I-2X	I-2B
Isolation of Coolant from Components	Yes	Yes	Yes	No	No	Yes	Yes	Yes
Air (or Liquid) Cooling T_j<+110°C, Q=20 watts	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Adaptable to Conduction Cooling	Yes	No	No	No	Yes	Yes	Yes	Yes
Conduction Cooling T_j<+110°C, Q=20 watts	No	N/A	N/A	N/A	No	Yes	Yes	Yes
Full Range of JEDEC Chip Carriers Acceptable	No	No	N/A	N/A	No	Yes	No	No
Minimum Module Pitch	0.3	0.4	0.6	0.5	0.3	0.3	0.4	0.6
Maintain Module Pitch with JEDEC Chip Carriers	No	No	N/A	N/A	No	Yes	No	Yes
SEM Compatibility	Yes	No	No	No	Partial	No	No	Yes

studies. Module Case 2 and Case 3 are not listed because of the emphasis on chip-carrier type package. Case 5 and Case 6, although not analyzed for chip-carrier type packages, were included to properly evaluate their unique cooling systems.

The constraints listed in Table 3.3-3 must be considered in selecting a module for a wide spectrum of system applications:

1) If a module is to be capable of being cooled with contaminated cooling air, such as ram air, positive isolation between the coolant and the components should be a basic feature of the module. This implies either a conduction-cooling capability to positive ducting of the cooling through the module.

2) To meet the system partitioning requirements and integrated-rack design goals, a module must be capable of dissipating 20 watts, while maintaining the junction temperatures at +110°C or less.

3) Conduction-cooling is considered a requirement in order to attain maximum application versatility. This feature is especially important in non-integrated rack systems, such as flight control, where the primary coolant could be contaminated air, or (because of volume considerations) cold plate cooling might be advantageous.

4) The compatibility of the module to the full size range of JEDEC chip carriers and the effect of these devices on module pitch must also be considered. This factor could limit the module in accepting future integrated circuit device technologies and/or seriously affect system packaging density.

5) Present SEM program compatibility is considered a desirable goal, but must be balanced against achieving the optimum characteristics for the standard avionics module. Partitioning characteristics (I/O pins, power dissipation, area and component compatibility) which affect avionics system weight and volume should be considered of greater importance than SEM compatibility.

Examination of Table 3.3-3 indicates that the Cases 1, 8, 9, and 10 meet the requirements of the first three items; coolant isolation, power dissipation capability of 22 watts, and adaptability to conduction cooling. The next screen, a conduction cooling thermal capacity of 20 watts, is within the capacity of the Case 8, 9 and 10 but not Case 1, the I-2A SEM. The next items, dealing with chip carrier compatibility, shows that only the HI-2A has the capability for full chip carrier compliance. On the other hand, only the I-2B and I-2A (not thermally acceptable) are compatible with the present SEM program. It should be noted that the HI-2A is acceptable to all screening characteristics except SEM compatibility.

An additional comparison of the four most likely module types to be evaluated in the system/rack level tradeoff studies is shown in Figure 3.3-19. The various module rating factors from Tables 3.3-1 and -2

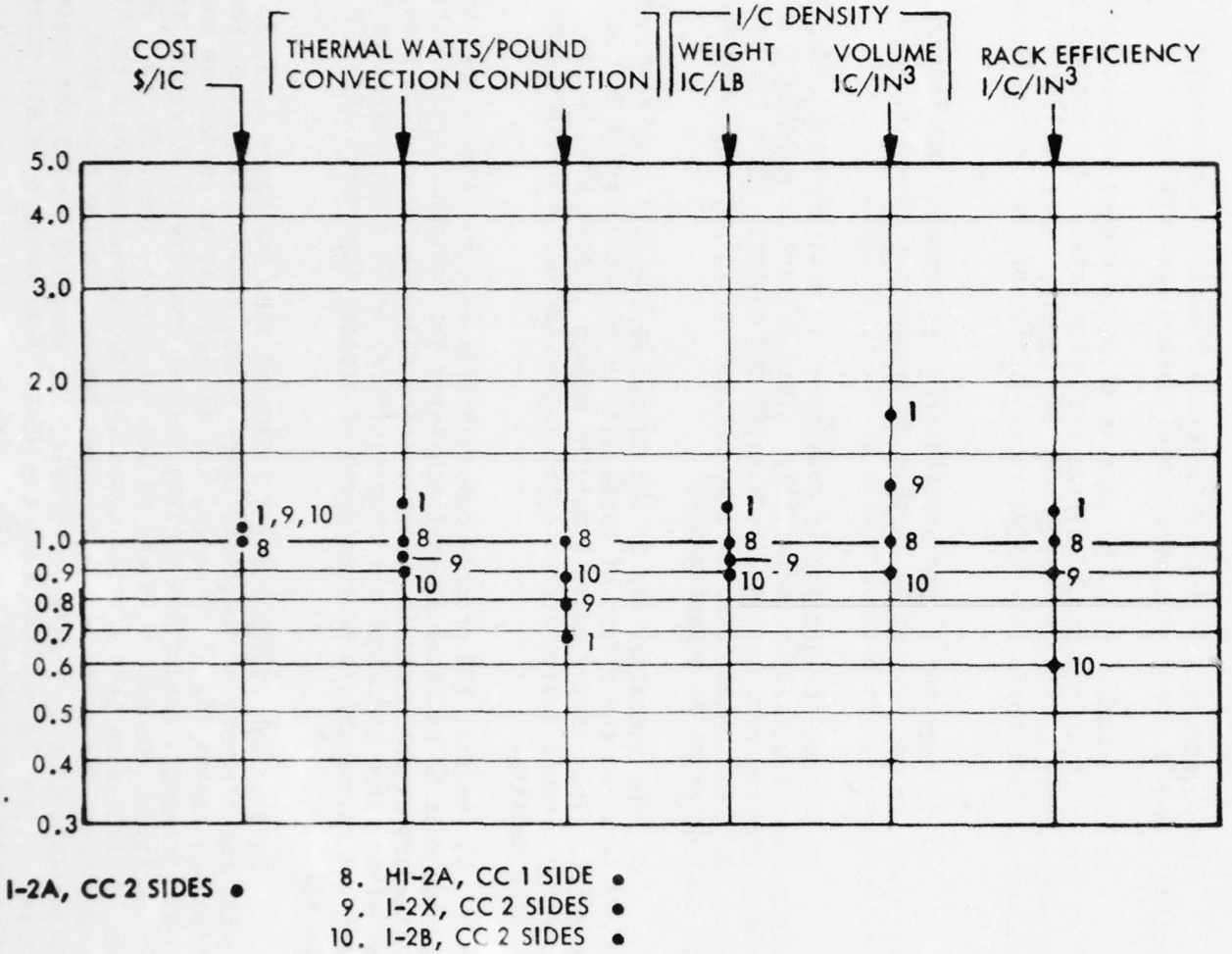


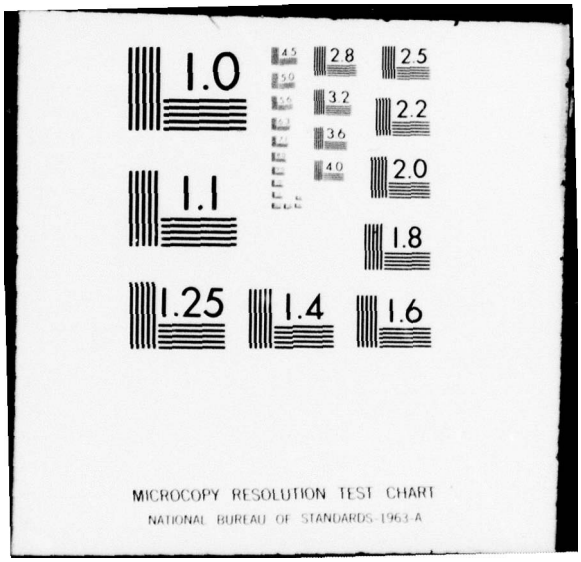
Figure 3.3-19. Relative Module Performance, Normalized to the HI-2A Module

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are shown normalized relative to the performance of the HI-2A module, Case 8. This module was used as the base because of its higher qualitive performance as analyzed in Table 3.3-3. In evaluating Figure 3.3-19, it must be remembered that the I-2A SEM, Case 1, has a conduction thermal capacity of only 12.5 watts which limits its application to that of a companion module to the I-2B SEM, Case 10. Taking this into account shows that the HI-2A has a higher performance for all factors except the volumetric packaging ($IC/in.^3$), but it is expected that in avionic installations where maintenance accessibility is important, the rack efficiency ($IC/in.^2$ of rack face area) will be the overriding consideration.

This module evaluation resulted in Cases 1, 8, 9 and 10 being selected for rack-level tradeoffs. This selection took into account the thermal performance, packaging density, device compatibility, cost and conformance to the present Navy SEM Program.

3.3.5.4 Variable-Span Modules

The flexibility of a modular packaging system can usually be increased by alternate module sizes which represent multiples or sub-multiples of the basic module size. Span increments beyond the equivalent SEM double span size were not considered for the following reasons:

1) System partitioning analysis indicated reasonable compatibility with the I-2A area limits.

2) An increased-span module has a longer conductive thermal path making effective utilization of the increased area questionable.

3) Difficulty in conduction-cooling mixed span modules.

4) Little utilization of modules in present SEM program beyond the double-span size.

A single-span module was evaluated to determine its applicability to the V/STOL AEW and Core avionics application. It was thought that the modules of low area requirements could be packaged on half-span modules (1/2 of 2A) saving overall system volume and weight. Since the thermal length would be one-half that of the larger module, it could be effectively conduction-cooled by a single guide rib interface. It was assumed that the power level would be limited to a level to achieve junction temperature limits equivalent to the larger modules. This maximum value, based on relative substrate area, was set at 5 watts for the I-1A and 8 watts for the HI-1A module sizes.

The results of this study are shown in Figure 3.3-20. The connector pin limits included both two-row and three-row types. The analysis showed that there were no module types which fell within the I-1A limits. Of the four types which fell within the area limits of the HI-1A, only one could be

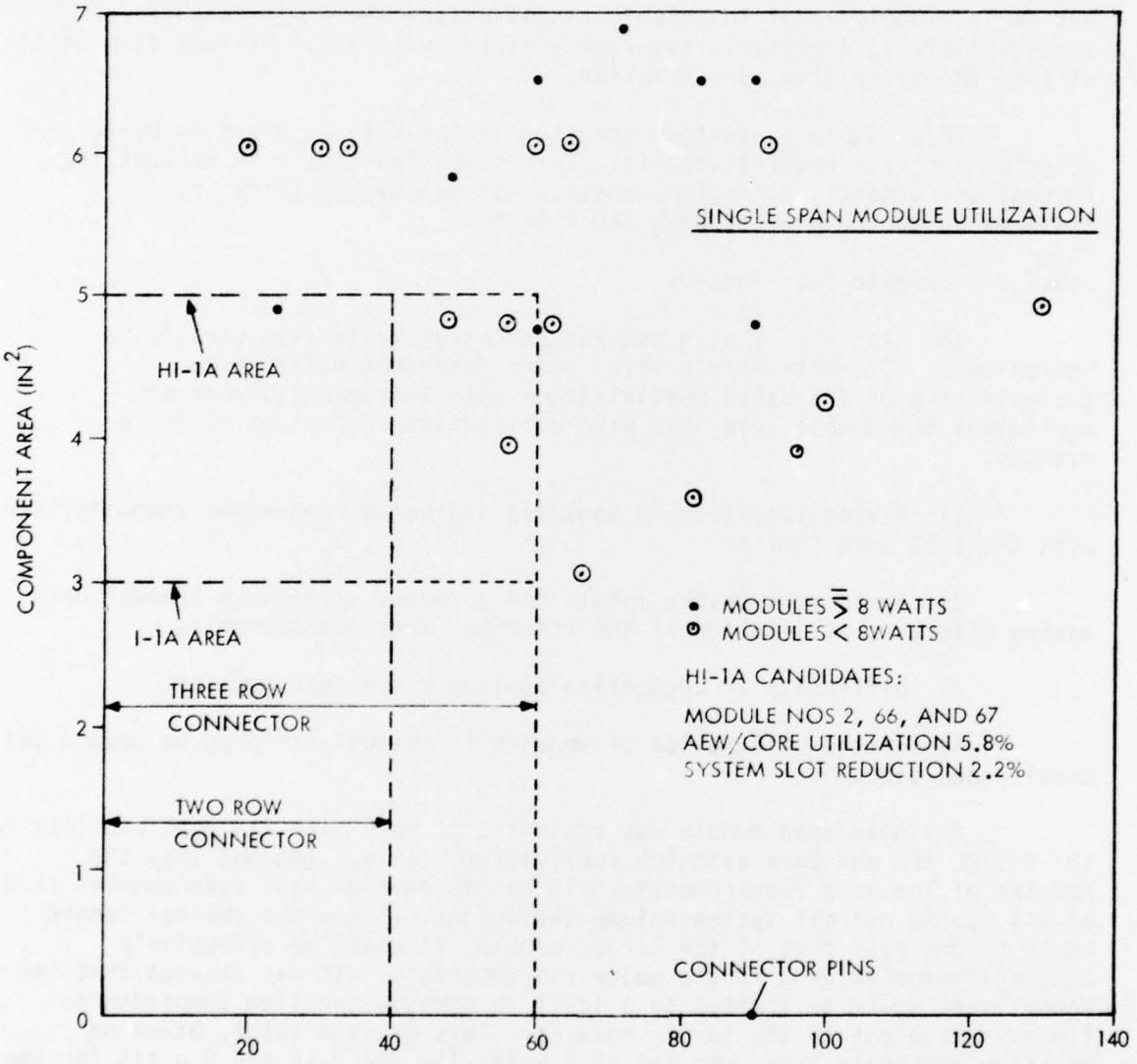


Figure 3.3-20. Single-Span Module Utilization

accommodated by a two-row connector. Unfortunately this module has a 14-watt power dissipation and cannot be cooled by a single guide rib interface.

The remaining three types, although within the power limits, would require a three-row connector. Investigation of the system utilization of these three module types revealed that they account for only 5.8 percent of the AEW/Core module complement. Further evaluation of how these single-span modules would be used in the various subsystems indicated a maximum slot saving of 2.2 percent under idealized module placement conditions.

From this analysis it was concluded that the additional complexity of two module sizes could not be justified because of the meager system level advantage.

3.3.5.5 Standard Avionic Module Conclusions

1) Full chip carrier (cc) compatibility is a requirement for the SAM. Chip carriers will replace DIPs as the standard integrated circuit package (1985).

2) SAM must be capable of being either conduction- or convection-cooled to provide maximum application versatility.

3) Power is the driving SAM requirement (20-watt capability required).

4) A larger connector is required to circumvent system partitioning restrictions (120-130 pins).

5) A higher Improved - 2A (HI-2A) module provides a thermally acceptable configuration with minimum weight, complexity and cost, and complete chip-carrier compatibility.

6) The I-2X, I-2B, and HI-2A module configurations are compatible with conduction (+45°C coldplate) cooling requirements.

7) The standard I-2A SEM is thermally unacceptable for conduction cold-plate cooling at the required power levels (20 watts).

8) The conductivity of the multilayer ceramic substrate is a significant factor in conduction-mode cooling performance, in contrast to glass epoxy multilayer boards.

9) LSI package heights (proposed JEDEC standard) preclude a two-substrate module on 0.3 or 0.4 inch centers.

10) The full range of proposed JEDEC chip carrier sizes will not fit within the I-2A substrate size limits.

11) A single substrate module configuration is more cost effective and eliminates the reliability penalty of inter-substrate connections.

12) Direct coolant to module interface results in two to three times improvement in module thermal capacity as compared to conduction-cooling. This is evidenced in direct air impingement cooling modes and in Cases 4, 5, 6, and 7 which eliminate the conductive mechanical interface losses.

13) Liquid cooling offers the potential for highest thermal performance and minimum thermal stress (Case 3 vs Case 5). The liquid interface vs maintainability consideration is the major item limiting the practical application of this technique.

14) A thermal interface to the module top-fin offers improved thermal capacity (Case 7) of the I-2A. Top fin cooling in conjunction with guide rib cooling could potentially provide sufficient thermal performance for MAP (not analyzed). A mechanical top-fin-to-heat-exchanger interface would be sensitive to tolerance and flatness limitations (0.001 inch clearance equivalent to 1°C/watt thermal resistance).

15) System partitioning analysis indicates that single-span (I-1A, etc.) modules are not an effective form factor.

16) All conduction-cooled module configurations investigated have less than 20-watt power dissipation capacity in a projected MIL-E-5400 WRA environment (+71°C exhaust temperature).

3.3.6 Module Recommendations

3.3.6.1 Connector

Develop a higher capacity connector (120-130 pin) utilizing low insertion force contact technology. This development should address:

- Maintain 0.3 inch module pitch
- Wire Wrap capability
- Multilayer board design constraints
- Connector/module substrate interface computability

3.3.6.2 Chip-Carrier Packages

Influence JEDEC chip carrier package standards to optimize their tolerances and dimensions to SAM application requirements. Of particular importance is the JEDEC maximum thickness dimension of 0.14 inches, which severely impacts the spacing of double-substrate modules. Presently-available chip-carrier packages are in the range of 0.06 inches thick.

Also of considerable importance is the resolution of the lead spacing; i.e., 0.04 inch vs 0.05 inch. It seems that early selection of one spacing is essential to the successful application of chip-carrier devices. The industry does not need another DIP/flatpack conflict.

3.3.6.3 Substrate

Develop substrate materials as alternates to multilayer ceramics. Chip carrier compatibility, lower dielectric constant for improved high frequency applications, cost, weight, and manufacturability are basic considerations. Refer to the discussion in Section 3.3.3.1.

3.3.6.4 Module

Refine the HI-2A and I-2A/2B module concepts. The conduction cooling capacity of the HI-2A and I-2B can be increased by increasing the heat sink thickness within module pitch/chip carrier thickness requirements. A preliminary estimate indicates that the 20 watt capacity can be attained for MIL-E-5400 conditions (+71°C air exhaust, +125°C T_j). Departure from the SEM standard 100 pin connector will allow other areas of optimization to be considered, such as the guide rib interface.

Chip carrier standardization results should be factored into the configuration refinement.

The final decision between the I-2A/2B type SAM and the HI-2A configuration will be most dependent on the relative importance of:

- Extension of the present SEM program to avionics.
- Weight and volume goals in future avionic systems.
- Compatibility with future LSI packaging requirements.

3.3.6.5 Liquid Cooling Interface

Scope the magnitude of the problem of developing a suitable quick-disconnect/leak-proof coupling. This is the main constraint limiting the application of liquid cooling at the module level.

3.4 Integrated Rack

The integrated rack functions as the interface between the airframe and the standard avionics module. In performing this task, it must fulfill certain basic electrical, thermal and mechanical functions, in concert with the requirements of the modules, while being compatible with the total airframe requirements.

The basic functions which must be considered include:

- Airframe installation versatility
- Thermal interface between ECS and module
- Power and signal distribution
- Maintainability - MTTR
- EMI/EMP
- Design standardization
- Field changes

3.4.1 Integrated Rack Mechanical Concept

A1. General

The integrated-rack concept for avionics equipment involves standardization of assemblies at all levels for all digital-type systems and subsystems within a given airplane. Standardization of assemblies in turn allows standardization of racks to accommodate these subsystems. Advance knowledge of SRA, WRA and cooling-system configurations, together with a particular aircraft configuration, allows the rack designer to design and locate racks in the airplane for maximum space utilization and maximum accessibility. Advance knowledge of subsystem heat loads and rack cooling system configurations also allows the ECS system designer to design his equipment.

Aside from advantages in the area of comprehensive and coherent system design, the integrated rack will provide the following advantages:

- Lighter weight
- Lower acquisition costs and life-cycle costs
- Standard maintenance procedures
- Commonality of spare parts
- Less aircraft wiring (box-to-box)

- Fewer connector or J-box interfaces (higher reliability)
- Second source possibilities
- Consistent environmental control for higher reliability

If a standard rack-packaging approach is in place before aircraft configuration has been established, then avionics space requirements can be factored into the airframe design, avoiding subsequent mismatch between airframe and avionics. The problem can be demonstrated by considering two extremes of fuselage configurations, round and rectangular. Figure 3.4-1 shows a typical pier-rack installation in a round or cylindrical fuselage section. Figure 3.4-2 shows the pier-rack installation in a rectangular fuselage section. The rectangular section obviously provides maximum space utilization for rectangular-type racks.

In addition to fuselage shape, there arise problems of headroom and aisle space. The round and rectangular fuselage sections shown are dimensioned in accordance with presently proposed designs. The headroom in the circular section is only 65 inches, making it difficult for the average-size man to replace modules. In contrast, the rectangular section provides 75 inches of headroom, not only in the center of the fuselage, but also at the outboard extremes. The headroom problem would also be of concern in the Marine Assault and VOD variations of V/STOL. The aisle-space problem is apparent in Figure 3.4-2.

Figure 3.4-3 shows a possible alternative to the pier-rack configuration for a cylindrical fuselage section. The overall rack height has been reduced by relocating the heat-exchanger unit outboard of the main rack structure.

Figure 3.4-4 shows an alternate fore-and-aft configuration for the rectangular fuselage section. The fore-and aft arrangement has alleviated the aisle space problem evident in both of the previous examples.

A2. Rack Size

Rack depth will be determined primarily by module depth and required wiring space. Figure 3.4-5 and 3.4-6 show how the rack depth of 4 inches was determined for both the air-cooled and liquid cooled racks. This depth presumes that the rack will accommodate a single layer of modules only. An alternate rack arrangement, as shown in Figure 3.4-7, will accommodate two layers of modules mounted back-to-back.

Rack height will be determined by the inside height of the fuselage. In this case, it is assumed that a 75-inch height will be available. The top of the rack is located 11 inches below the overhead to provide I/O connector clearance. This clearance is a maximum for current connectors and EMI adapters, and would probably be less for fiber-optic applications. Total rack height is 64 inches. See Figure 3.4-8.

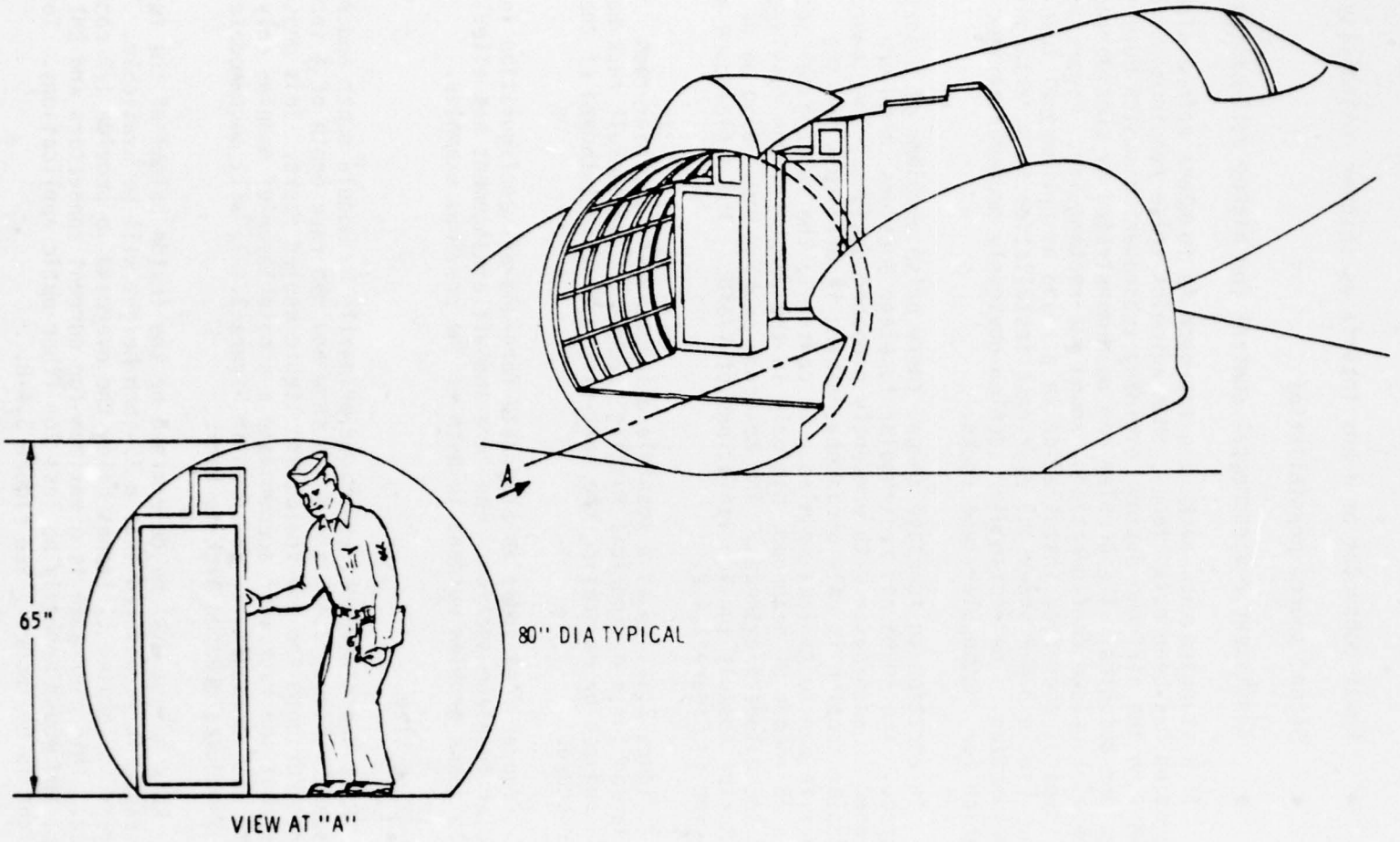


Figure 3.4-1. Typical Pier Rack Installation in a Cylindrical Fuselage

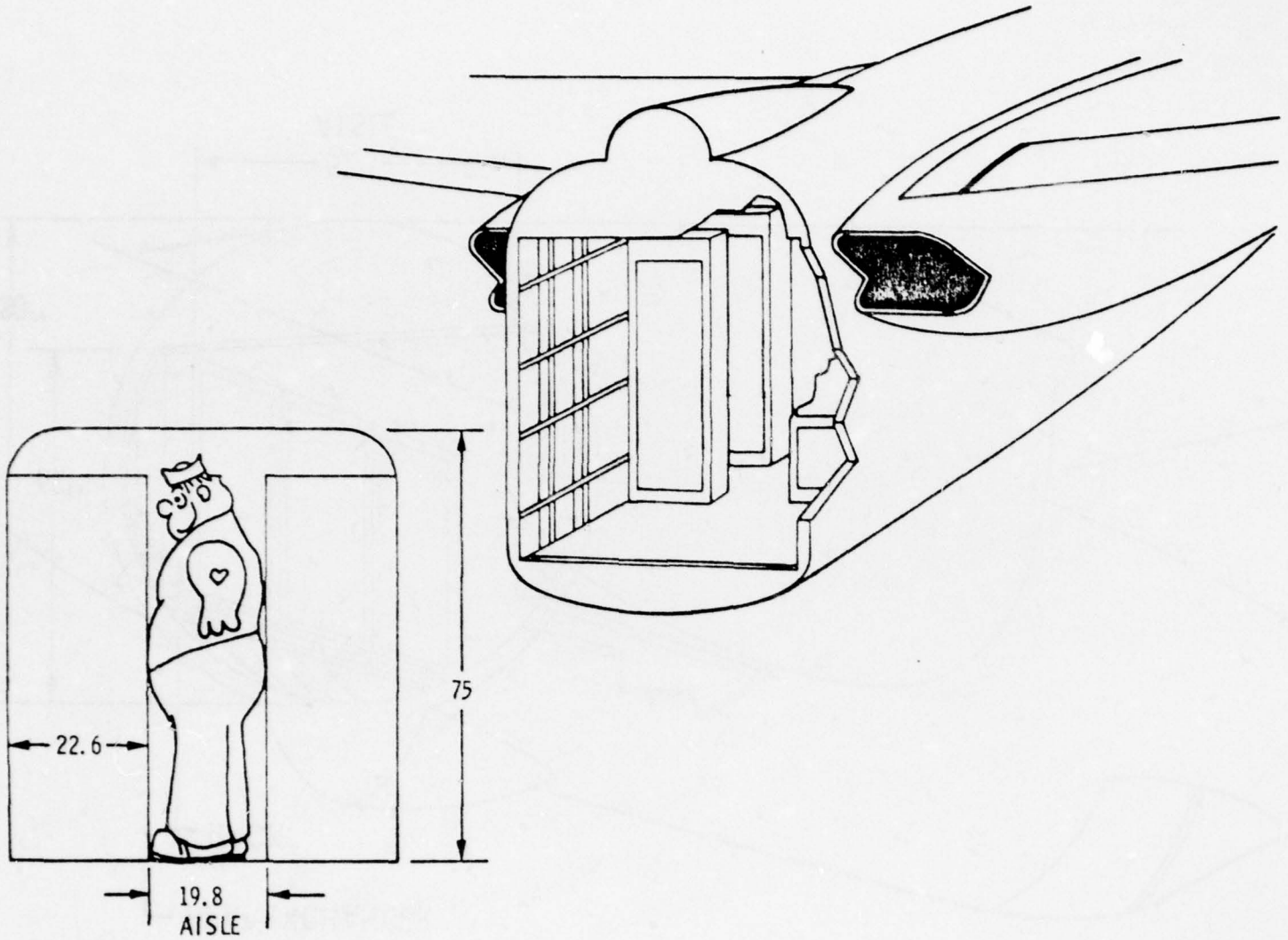


Figure 3.4-2. Pier Racks in a Rectangular Fuselage

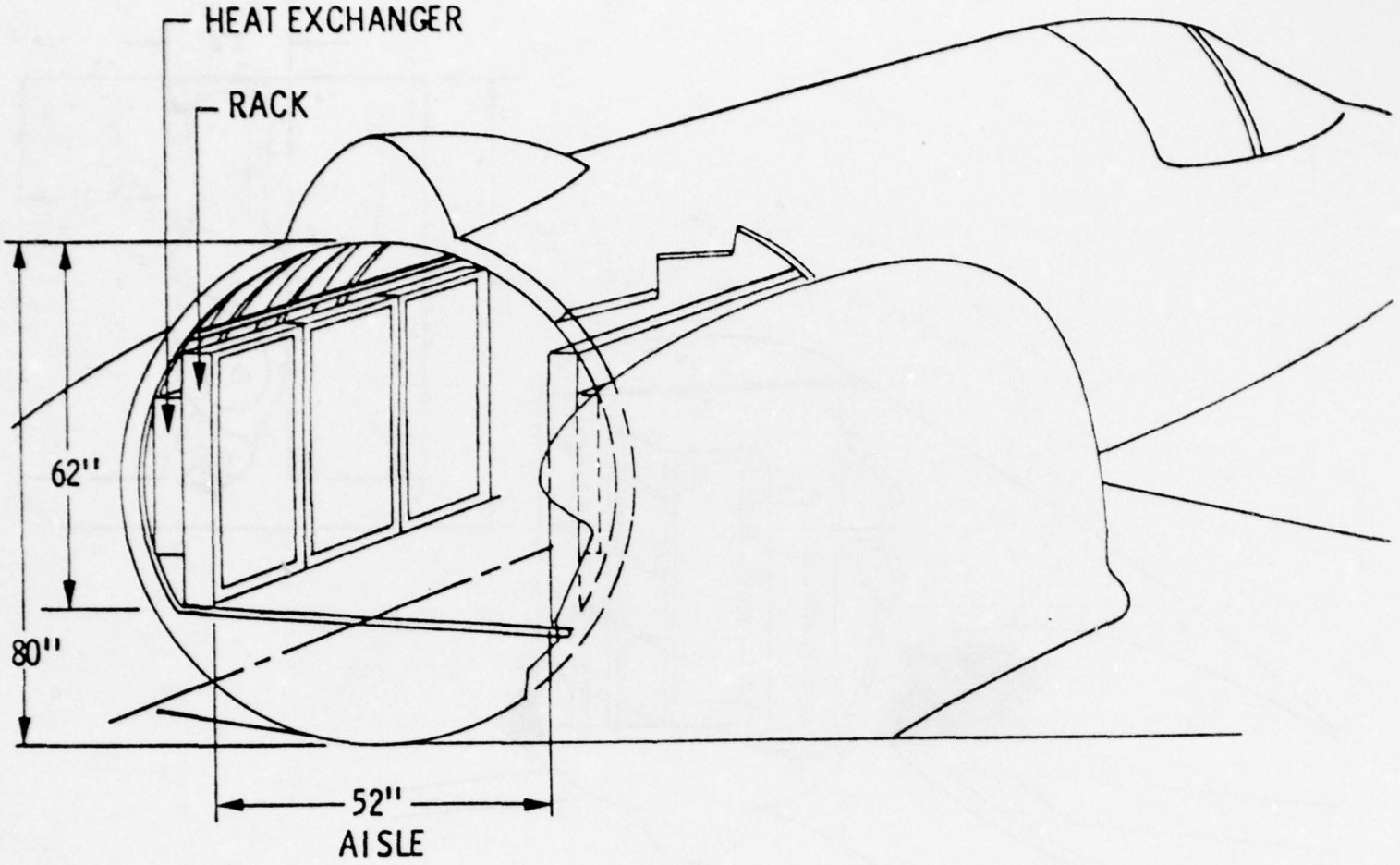


Figure 3.4-3. Fore and Aft Rack Installation in a Cylindrical Fuselage

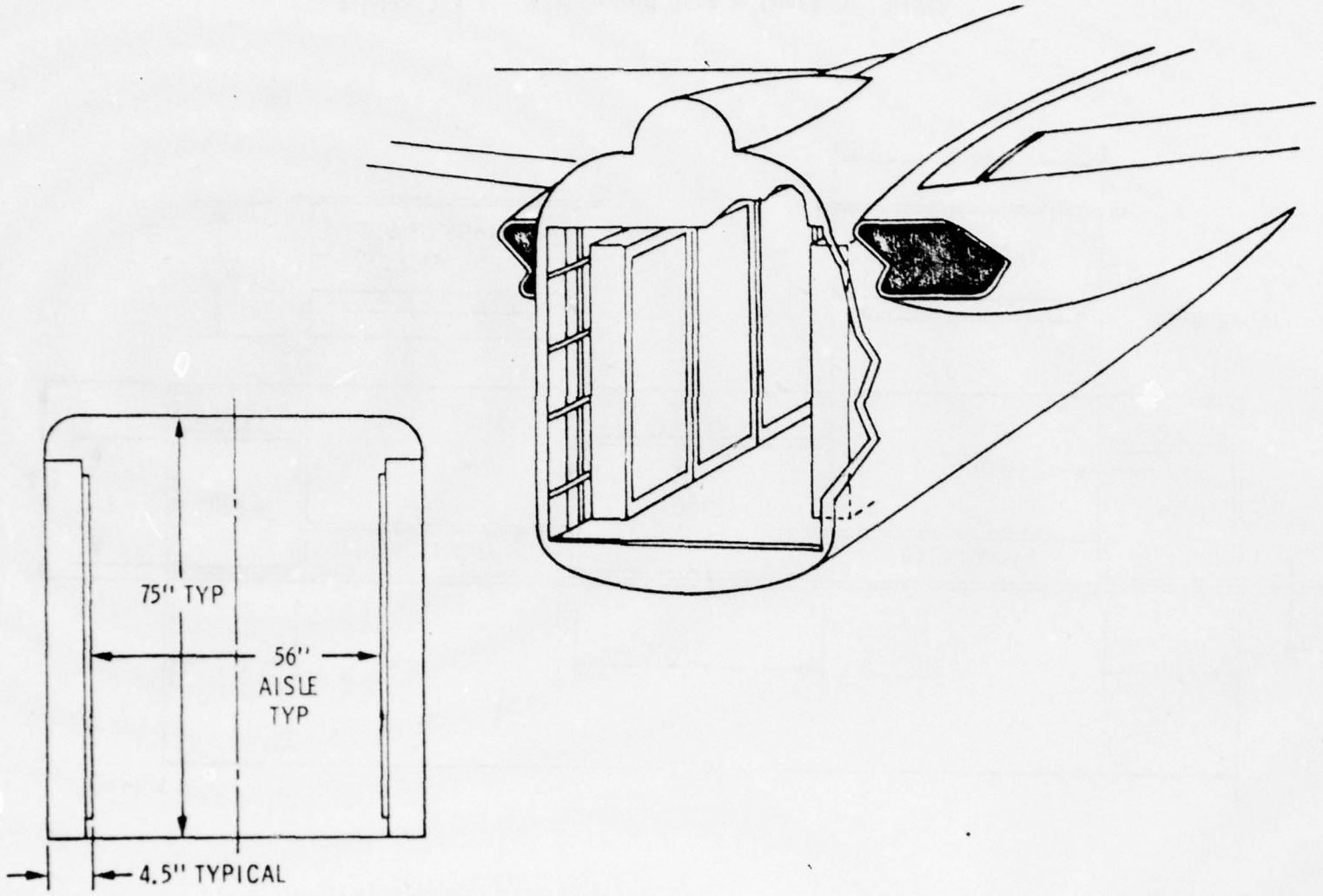


Figure 3.4-4. Typical Fore and Aft Racks in a Rectangular Fuselage

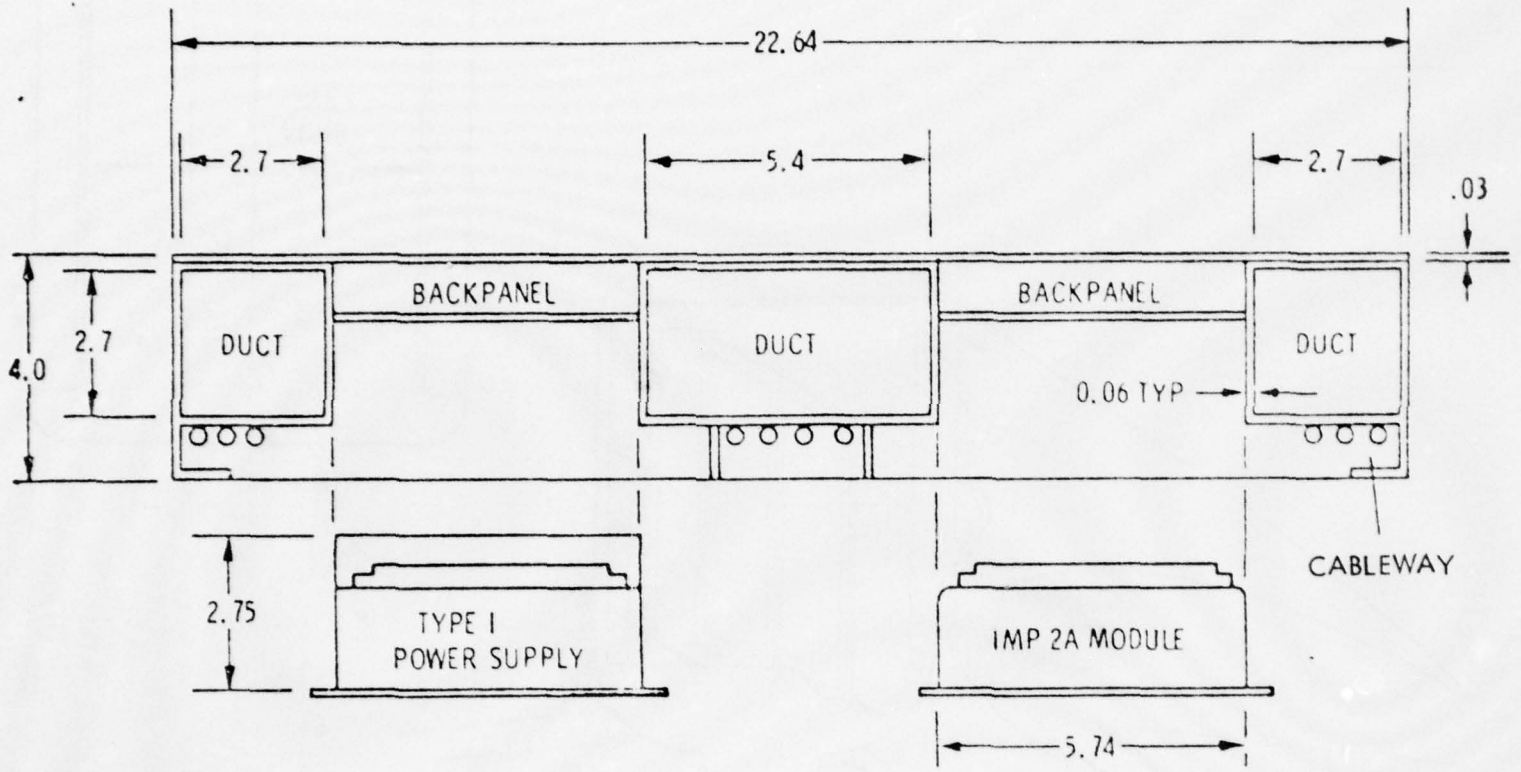


Figure 3.4-5. Air-Cooled Rack - Depth and Width
(Single Module Depth)

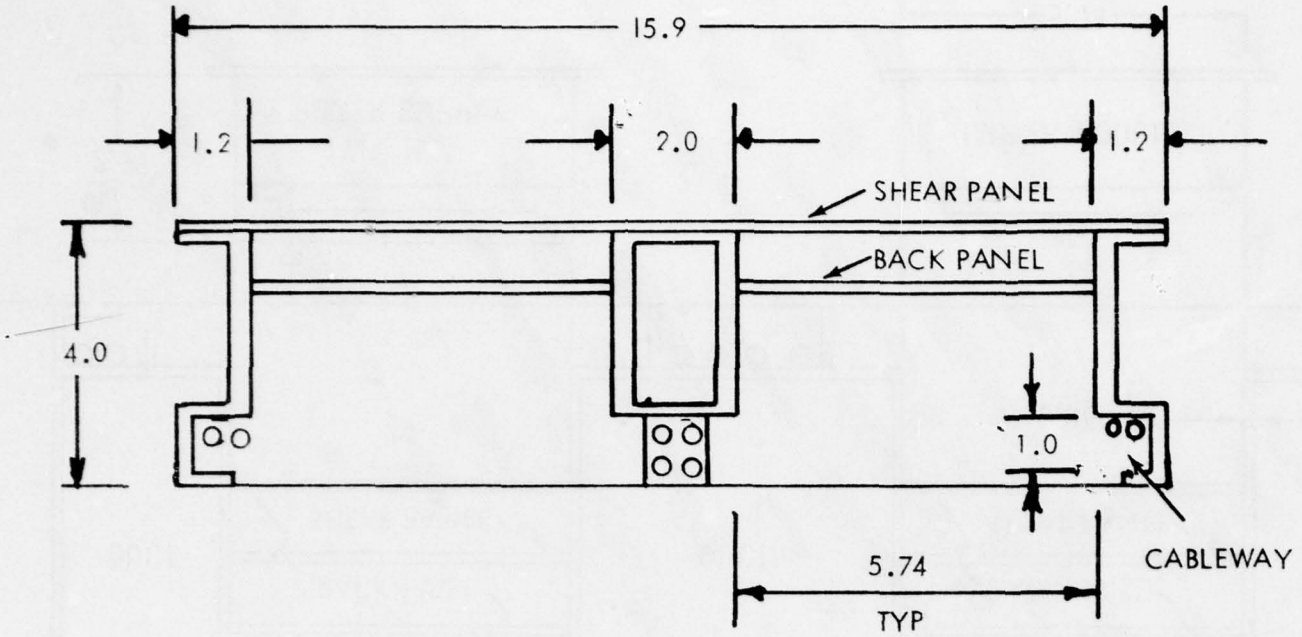


Figure 3.4-6. Liquid Cooled Rack - Depth and Width

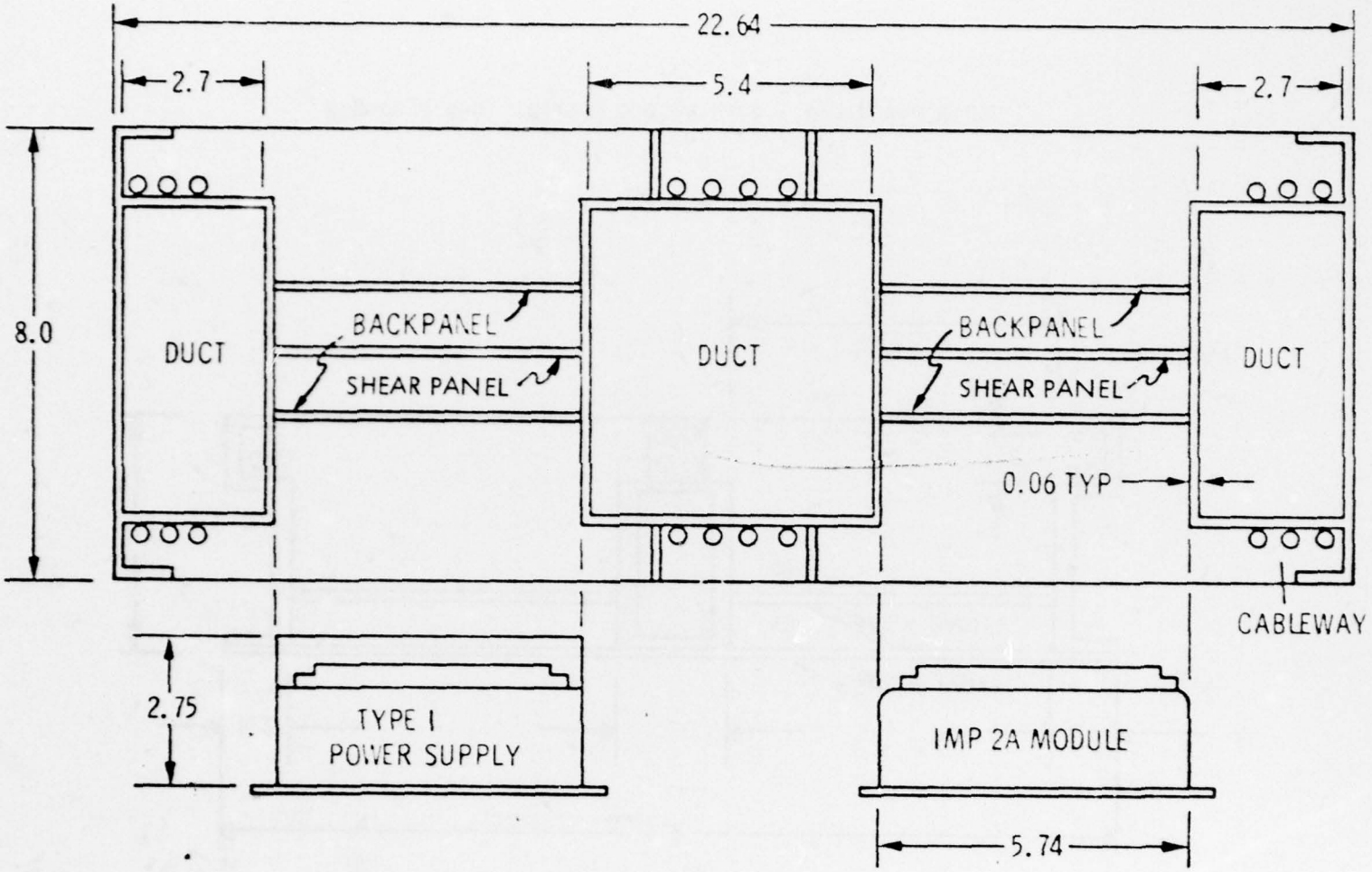


Figure 3.4-7. Air-Cooled Rack - Depth and Width
(Double Module Depth)

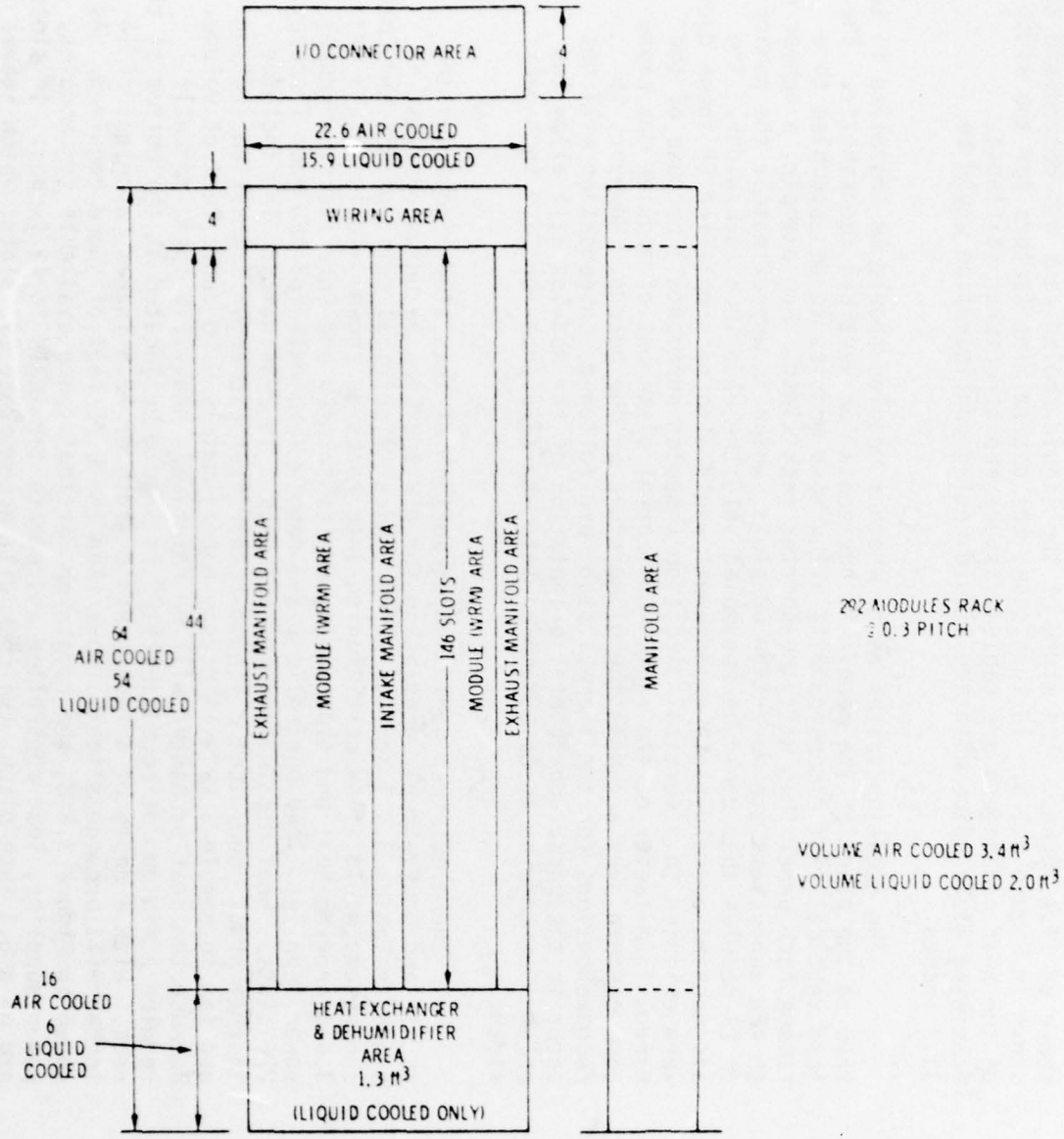


Figure 3.4-8. Pier Rack Space Allocation

A wiring area 4 inches in height will be assigned at the top of the rack and inside the rack.

The width of the pier rack is limited by the width of the airplane and required aisle space. It is assumed that the inside width of the airplane is 65 inches. Using air-duct sizes (Figure 3.4-5) recommended in the thermal study, the width of an air-cooled rack is 22.6 inches. If racks were installed on opposite sides of the aisle, this would leave an aisle space of 19.7 inches. The width of the liquid-cooled rack was determined as shown in Figure 3.4-6. In this case, the determining factors for the width of the heat exchangers are cableway space and structural stiffness. Remaining aisle space with the liquid-cooled configuration would be 33.2 inches.

The question arises as to whether modules should be installed in the rack so the plane of the module is horizontal or vertical (bookshelf). The long vertical rack dimension will allow more modules to be assembled to a common back panel than will the shorter rack width. For example, a number of th AEW subsystems use more than 60 slots, which is approximately the number of 2A modules that could be assembled into the 22.6 inch rack width. The air-ducting or cold-plate arrangement would also be simplified if these ducts were oriented in a vertical direction (modules horizontal) because of the narrow form-factor of the rack. Horizontal placement of modules may cause some concern over accumulation of moisture on the boards. However, if recommendations for the thermal study are followed, condensation will not occur in the rack. Horizontal orientation of the modules will allow two columns of modules to be assembled into the 22.6 inch- or 15.9 inch-rack width.

The electrical partitioning portion of this study indicates the module and power-supply population for AEW and Core avionics systems, as shown in Tables 3.4-1 and 3.4-2. A logical electrical split of AEW and Core subsystems would allow partitioning into racks as shown. Tables 3.4-3 and 3.4-4 provide heat and slot use summaries for AEW and Core racks. Modules, power supplies, load controllers and remote terminals for AEW rack 1 occupy 274 slots. Heat dissipation for AEW Rack 2 is 2984 watts. The included thermal study shows that a liquid-to-air heat exchanger transition section and fan to handle 3 KW will occupy approximately 0.75 cubic feet of volume. Because the heat exchanger will be relatively heavy (15 lbs), and will require a minimum of accessibility, it should be located at the bottom of the rack. With a depth of 4 inches and a width of 22.6 inches, a height of 16 inches will provide slightly more than the 0.75 feet of space required. As shown in Figure 3.4-8, the remaining vertical space available for modules, power supplies, load controller and remote terminals is 44 inches. If slots are on a 0.3 inch pitch, the rack will accommodate 292 slots, which leaves 18 spare slots in Rack 1.

Table 3.4-1. AEW Avionics Rack Summary

Module and Power Supply Population and Heat Dissipation

AEW Rack No.	Subsystem	Subsystems Per System	Module Qty	Module Slot Qty	Module Pwr Watts	Qty NAFI Type Power Supply I-1	I-2	III-1	III-2	Power Supply Heat Watts
1	AEW Sig. Processor Part 1	4	136	138	1984	8			8	496
2	AEW Sig. Processor Part 2	4	132	134	2248	8			8	562
	AEW Radar Post-Processor	1	30	36	189	1			1	47
3	AEW Intercept/ATC Tracking/Classification	1	15	18	70	1			1	60
3	Multi-sensor Processor	1	38	43	240	1			1	60
	Threat Eval. and Tactics	1	5	6	35		1			12
	AEW Display Electronics 1	1	37	41	344	1		1	1	86
4	AEW Display Electronics 2	1	29	32	275	1			1	69
	AEW Display	1	49	52	458	1	1		1	114
	Totals	15	471	500	5843	22	2	1	22	1464

1656 Fan heat (414W ea.)
5843 Module heat
1464 Power supply heat
240 Load controller and remote terminal heat
9203 Watts - Total AEW heat

9.2KW

Table 3.4-2. Core Avionics Rack Summary

Module and Power Supply Population and Heat Dissipation

Core Rack No.	Subsystem	Subsystems per System	Module Qty	Module Slot Qty	Module Pwr Watts	Qty NAFI Type Power Supply I-1	I-2	I-3	III-2	Power Supply Heat Watts
	Basic EW Data Processor	1	11	12	70		1			18
	Basic EW Preprocessor	1	27	29	59		1		1	15
1	Basic EW Radar Warning Receiver	2	60	62	308	2			2	77
	Communications Processor	1	8	10	60		1			15
	Mass Memory	1	40	42	565	1				141
	Nav. Sensor Interface	1	11	11	30		1		1	8
	Nav. Data Processor	1	18	23	131	1			1	33
2	Spare Processor	1	13	18	136	1			1	34
	Core Displays	1	20	22	143	1			1	37
	System Status Monitor	1	40	45	239	1			1	60
	System Controller	1	3	4	15			1		6
	Totals	12	251	278	1756	7	4	1	8	444

828 Fan heat (414W ea.)
1756 Module heat
444 Power supply heat
240 Load controller and remote terminal heat
3268 Total Core heat

Table 3.4-3. AEW Avionics Rack, Heat and Slot Summary

Modules (WRMS)	AEW Racks											
	Rack 1			Rack 2			Rack 3			Rack 4		
	Qty	Heat Watts	Slots	Qty	Heat Watts	Slots	Qty	Heat Watts	Slots	Qty	Heat Watts	Slots
I 2A Modules	136	1984	138	132	2248	134	88	534	103	115	1077	125
360W Type I-1 PS	8	496	112	8	562	112	3	137	42	3	269	42
125W Type I-2 PS							1		7	1		2
5W Type III-1 PS										1		2
15W Type III-2 PS	8		16	8		16	3		6	3		6
Load Controllers	4	40	4	4	40	4	4	40	4	4	40	4
Remote Terminals	2	20	2	2	20	2	2	20	2	2	20	2
Fan	2	114		2	114		2	114		2	114	
Total Slots*			272			268			164			188
Heat		2654W			2984W			845W			1520W	

*292 slots available

Table 3.4-4. Core Avionics Rack, Heat and Slot Summary

Modules (wrms)	Core Racks Rack 1 Qty	Rack 1 Heat Watts	Rack 1 Slots	Rack 2 Qty	Rack 2 Heat Watts	Rack 2 Slots
I-1A modules	106	497	113	145	259	165
360W type I-1 PS	2	25	28	5	319	70
125W type I-2 PS	3		31	1		7
50W type I-3 PS				1		8
15W type III-2 PS	3		6	5		10
Load controllers	4	40	4	4	40	4
Remote terminals	2	20	2	2	20	2
Fan	2	114		2	114	
Total Slots			174			263
Heat		7964			????	

A3. Basic Rack Design Approaches

1) Single Depth Module Rack - Front and Rear Accessibility

The most basic approach to the rack design would be a single-depth module rack with access to both sides of the rack as shown in Figure 3.4-9.

(1) Advantages

- Direct module access from the front of the rack
- Direct access to the back panel from the back of the rack
- Cables and wiring accessible for retrofit in back of rack
- Back panels rear-removable

(2) Disadvantages

- Not usable in multiple-module depth configuration (i.e. back-to-back)
- Not usable where installation prohibits rear access (i.e. fore-and-aft racks against A/C bulkhead or fuselage frames)

2) Single or Multiple Module Depth with no Rear Access

A modification of the basic approach would involve relocation of the rack wiring to the front side of the rack for accessibility, and design of a front-removable back panel.

(1) Advantages

- Single module depth racks may be installed against A/C bulkheads or frames where there is no rear access to the racks.
- Racks may be designed for back-to-back module arrangement.
- Facilitates structural design of the rack. A shear panel can be built into the rack to accommodate shear loads in a lane parallel to the back-panel plane.

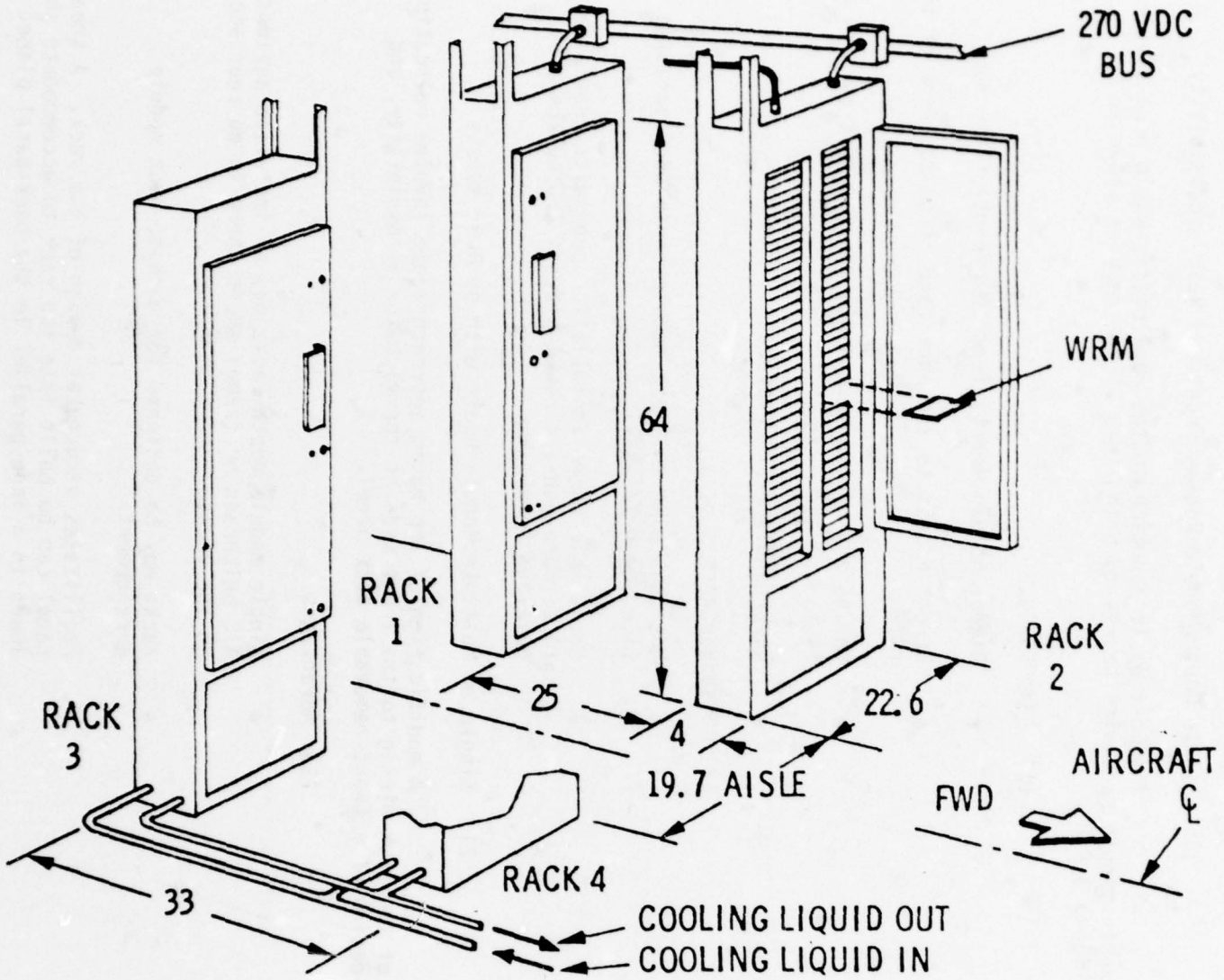


Figure 3.4-9. Typical Pier Rack Installation

(2) Disadvantages

- Complicates wiring crossovers at the front of the rack.

These two approaches were the only approaches involving standard module connectors which were studied in detail. With little present knowledge of all possible installation configurations and locations in an airplane, one or both of these approaches would seem to provide greatest versatility for installation in any aircraft location. For specific installations, an unlimited number of configurations involving WRAS on slides or hinges, with rack and panel connectors, retractable cables, flexible air ducting, etc. may be considered. These schemes generally add cost, weight and reliability penalties. They may be justified for maintainability reasons in some cases, but it is recommended that the initial approach be the simplest approach.

A4. Detailed Rack Design

1) Single Depth Module Rack-Front and Rear Accessibility

The simplest approach is to assemble modules directly into the rack with no intermediate WRA. (See Figure 3.4-9.) This would be the preferred method for conduction-cooled modules. The back panel can be either front-removable or rear-removable, and wiring between back panels would be located in the back of the rack.

2) Single or Multiple Module Depth with No Rear Access

As in the previous case, the simplest approach is to assemble modules directly into the rack with no intermediate WRA. Figure 3.4-10 shows a double module depth (back-to-back) rack with no rear access to the backpanel. In this case, the backpanel would have to be front-removable, and wiring between back panels would be on the front of the rack to allow field modifications to be made on the wiring. Front-removable backpanels and up-front wiring would also be required on fore-and-aft racks where rear access is not feasible. An advantage of this method is that a shear panel can be added to the back of the rack to take up shear forces in the direction parallel to the plane of the backpanels. (See Figures 3.4-6 and 3.4-7.)

A variation on this approach as shown in Figure 3.4-11 would involve a card cage (WRA) to contain the modules and the backpanel. The WRA would be removable from the front of the rack. In this case, air openings (for the air-cooled component approach) would be located in the card cage walls, and the manifold in the rack would have a continuous opening over the full height of the rack. The smaller Type III power supplies would mount in the card cage, and the larger Type I power supplies would mount outside the card cage, but would plug into the same back panel as its associated modules (same subsystem). Figure 3.4-12 shows a recommended WRA configuration.

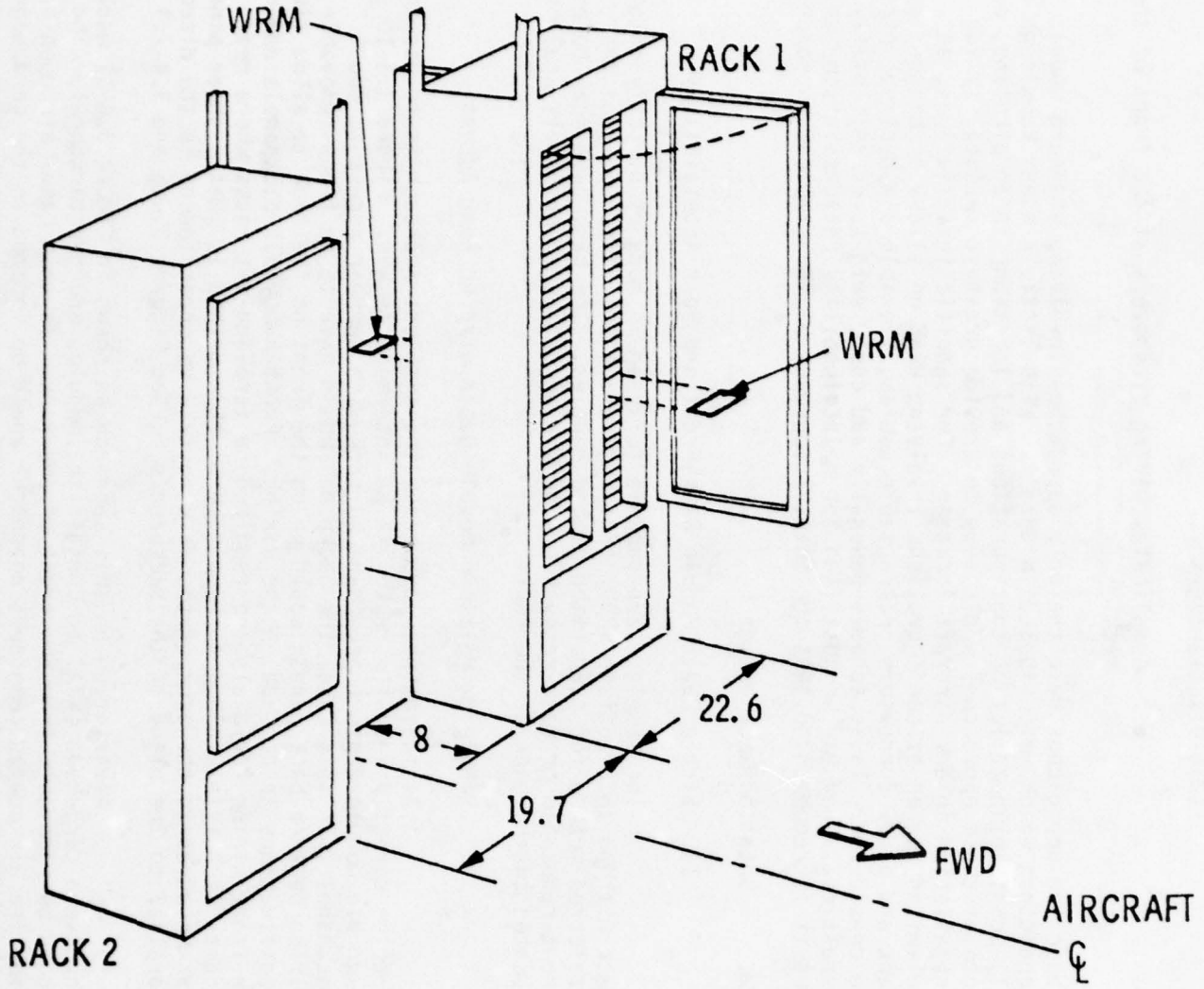


Figure 3.4-10. Direct Access to Modules (WRMs) Pier Racks - Modules Plug In Front and Rear

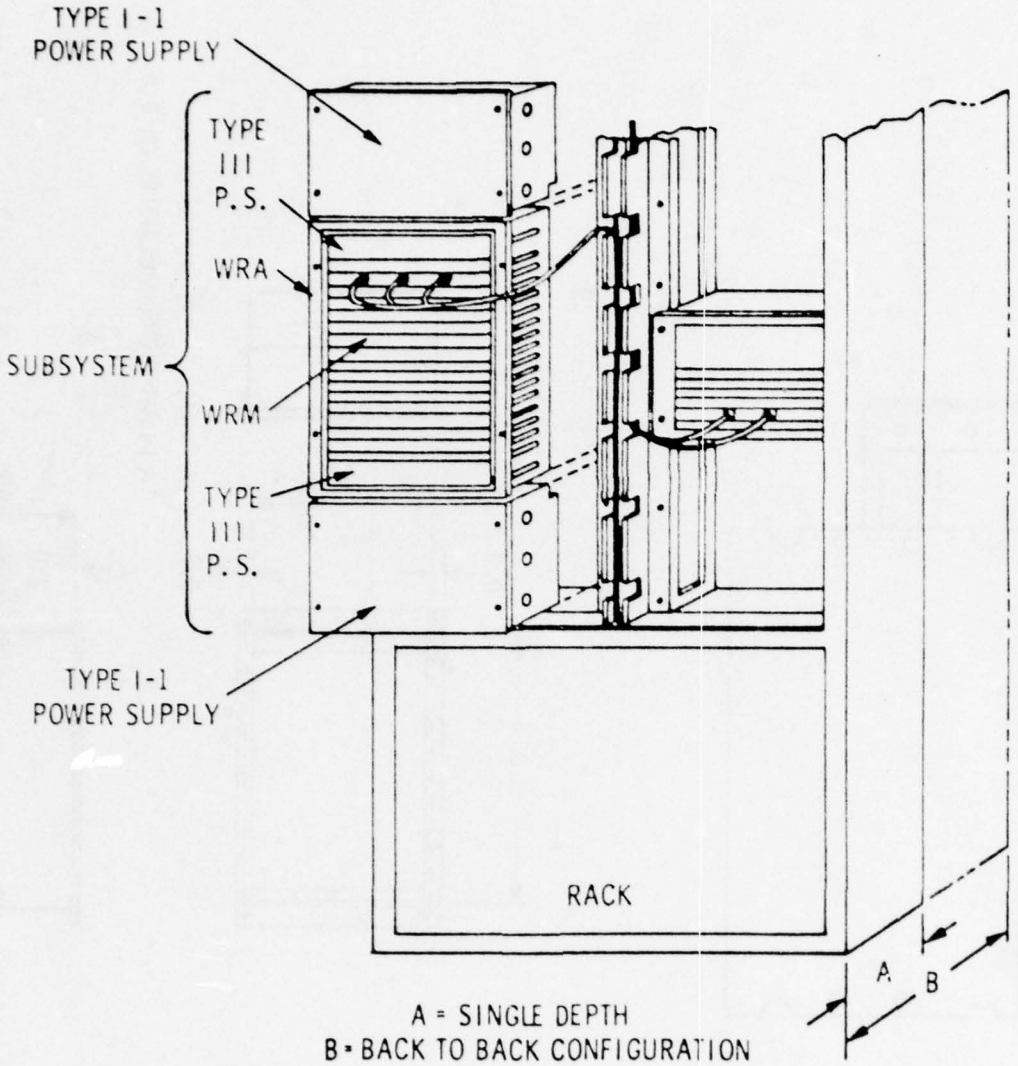
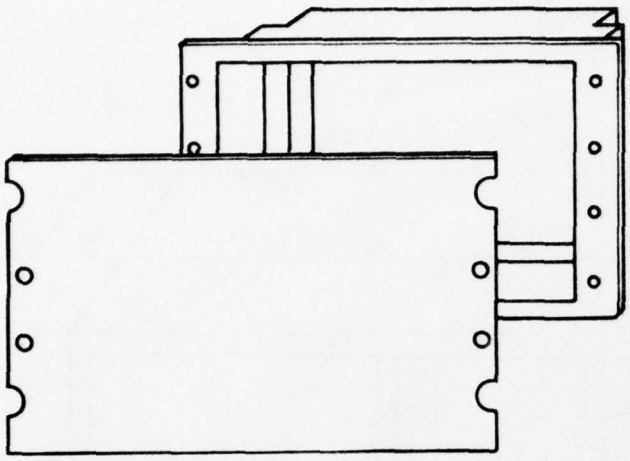


Figure 3.4-11. Rack with Front Removable WRAs and Wiring



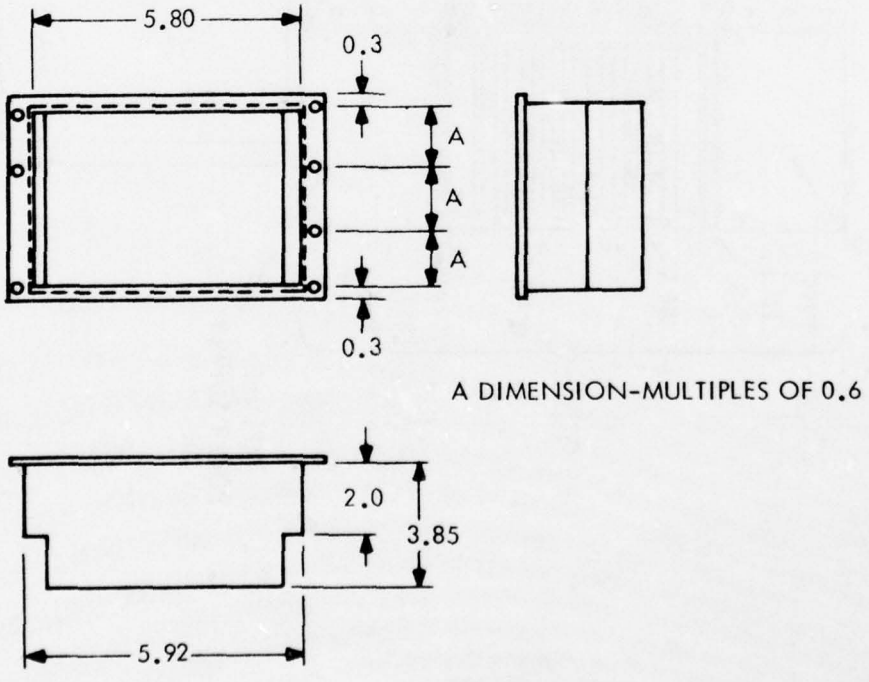


Figure 3.4-12. Integrated-Rack Compatible WRA Concept

A5. Effects of Cooling Methods on Rack Characteristics

The advantages and disadvantages of air- and liquid-cooled racks, as they affect the rack configuration, are as follows.

1) Air Cooled - Air circulated through rack and cooled in a liquid heat exchanger.

(1) Advantages

- Failure of liquid cooling supply not catastrophic
- Air impingement on components provides lowest junction temperature and highest reliability
- Allows use of separate card cages for subsystems

(2) Disadvantages

- Large volume required for plenums, ducts, heat exchanger fan(s) and transition section. See Figure 3.4-13.
- Fans generate acoustic noise

2) Liquid Cooled - Liquid circulated throughout the rack

(1) Advantages

- Because heat exchanger is not required in the rack, more space can be used for modules. Fewer or smaller racks would be required.
- No acoustic noise

(2) Disadvantages

- Loss of liquid circulation could abort the mission
- Does not lend itself to separate card cage installation

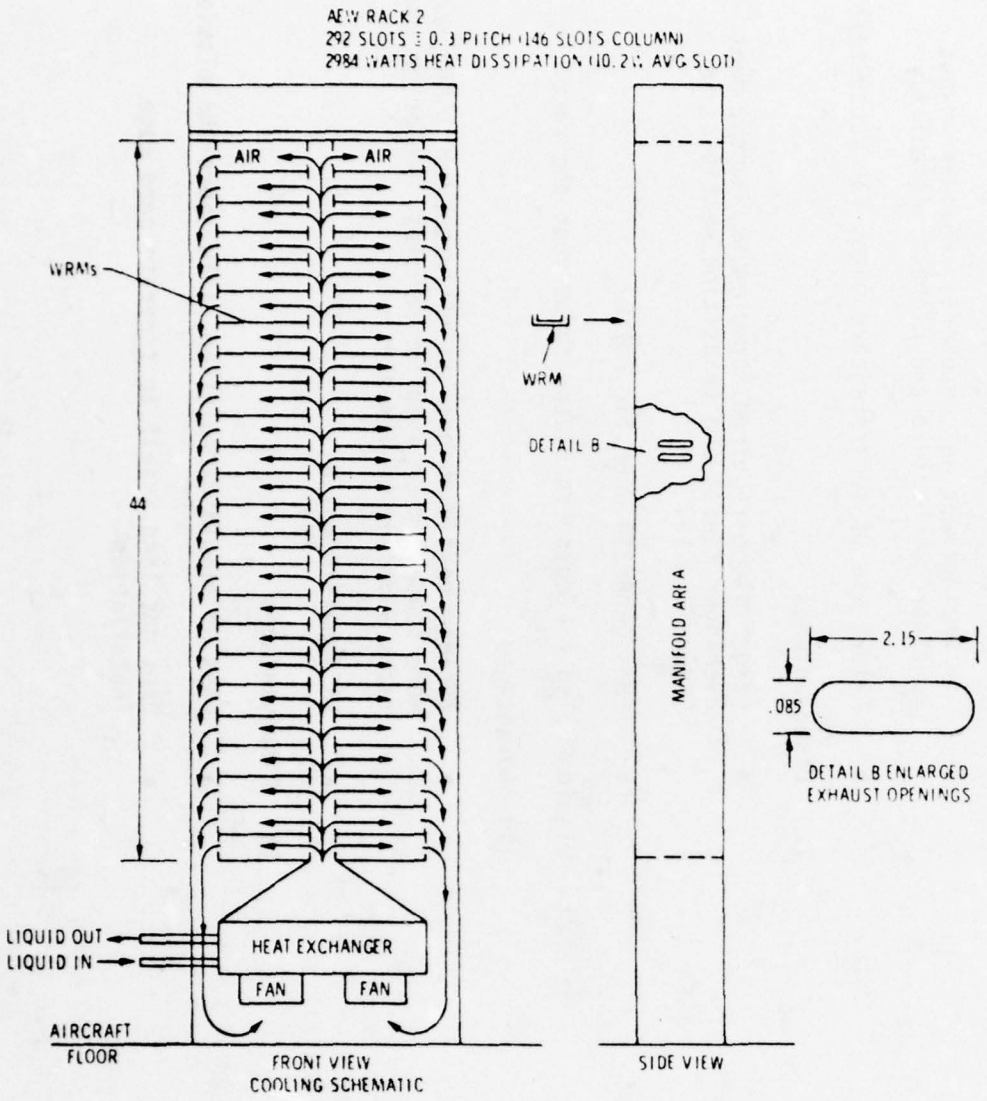


Figure 3.4-13. Cooling Schematic - Air Cooled Version

3.4.2 Integrated Rack -- Thermal Considerations

The integrated rack cooling concept was developed to provide increased electronics reliability, degraded mode of operation in the event of an ECS failure, elimination of system-level single-point failure modes, and ease of maintenance. A schematic of the preliminary cooling concept is given in Figure 3.4-13. A more detailed thermal analysis of the proposed AEW Integrated Rack is given in Appendix E.

3.4.2.1 Conformity to Military Specification: Use of Forced-Air Closed-Cycle Cooling Within Integrated Rack.

MIL-STD-454E prohibits the use of externally-supplied cooling air for direct cooling of components (MIL-STD-454E, Requirement 52 - Thermal Design paragraph 5.2), but encourages the use of forced-air cooling (Ibid., paragraph 6). The proposed forced-air cloed-cycle rack is in complete conformity with the above requirement, as:

1) Externally-supplied cooling air is not used at all.

2) A preferred cooling method, forced-air cooling using internal air, is used.

Paragraphs 5.1, 5.2, and 6 of Military Standard MIL-STD-454E, Requirement 52 - Thermal Design, state:

> 5.1 For equipment thermally designed for use with external source-supplied cooling air which may contain entrained water or other contaminants detrimental to the equipment, precautionary measures shall be taken to avoid direct impingement on internal parts and circuitry by channeling or use of heat exchangers. If this is impractical, the water and contaminant removal devices. Consistent with adequate cooling, minimum differential pressure (pressure drop) of the cooling air through the equipment heat exchanger or cold plate shall be maintained. Each separate piece of equipment being cooled shall be marked with the high and low operating temperature to which it is designed, the quantity and characteristics of air required to adequately cool the unit, and the resistance to air flow with respect to the air flow rate.
>
> 5.2 Equipment requiring externally supplied cooling air and intended for use in aircraft, shall be designed using cold plates or heat exchangers so that none of the cooling air will dome into contact with internal parts, circuitry, or connectors.

6. Other cooling methods. Other cooling methods such as liquid, evaporative coolants, and vapor cycle refrigerants shall not be used, except when natural or forced air cooling methopds are unsuitable.

The key features of a V/STOL platform integrated rack are:

1) Continuous dehumidification of the electronics

2) Restricted thermal extremes, and the reduction of induced stresses and strains

3) Direct air cooling of components by a closed-loop filtered air system

4) A simple liquid (Coolanol-20) interface with the aircraft ECS.

A1. Dehumidification of Integrated Rack

The proposed integrated rack cooling systems would permit on-ground dehumidification of the rack by the cooling and subsequent reheating of the internal air. The cooling load in the ECS would be small relative to that required for equipment cooling.

It is believed that such dehumidification of the electronic equipment within the integrated racks would have a significant impact on reliability, particularly when operating in a tropical environment.

A2. Dehumidification Requirement

Dehumidification is important because:

1) Printed circuit boards absorb 2 to 3 percent moisture. If equipment is not kept dry, when the temperature of the equipment rises, the Z axis expansion of the boards is unusually high, resulting in "cold working" of the copper in plated-through holes. This results in low-cycle fatigue.

2) Metal migration problems on the surface of PC boards cannot occur without moisture. If there is any cleanness problem on circuit boards (charged ions available), moisture will permit lead and tin to migrate across the surface of the boards. This will even occur under conformal coating.

3) Changes in impedance of printed wiring boards and changes in resistances of such devices as carbon composition resistors occur as a result of moisture adsorption/absorption.

A3. Constant Temperature Operation

During normal operation of the proposed rack cooling system, the internal cooling air temperature will be primarily influenced by the

temperature of the liquid coolant, which will be regulated to provide a constant component temperature by the ECS. The coupling of the internal cooling air through the heat exchanger is much greater than through the rack walls to the ambient as was shown above. Such a control scheme can compensate for a reduction in the internal air cooling effectiveness because of temporary loss of cabin pressurization. The reliability of the electronics may be expected to be greatly enhanced by uniform temperature operation.

A4. Emergency Operation

In the event that the ECS Coolant loop is disrupted for any reason, the temperature rise of the integrated rack above cabin temperature, assuming a combined radiative and natural convection coefficient of

$$\frac{4 \text{ BTU}}{\text{hr ft}^2 \text{ °F}} .$$

would be 46°C.

There will be an additional rise in temperature of the internal-loop air above the rack sides of about half the above. Thus during emergency operation (no ECS, or no liquid circulation between rack heat exchanger and ECS) with, for example, a 21°C cabin temperature, would result in the internal loop steady-state air temperature:

$$T_{\text{internal}} = 21°C_{\text{cabin}} + 23°C_{\text{and internal } t} + 46°C_{\text{external } t} = 90°C$$

An internal rack air temperature of 90°C would permit continued operation without damage to the electronics in the event of an ECS failure. It is true that without ventilation the cabin temperature of the aircraft would climb to higher levels. The thermal time constant for such a change would be expected to be several hours. It is probable that emergency operation of the equipment without serious damage would be possible for any single mission.

The above assumed heat transfer coefficients may prove a bit high. However, more than offsetting any under-optimism in this factor will be the high local heat-transfer coefficients over the components themselves, due to the forced-convection within the integrated rack. It is highly probable that emergency-condition component temperatures will fall under vendor-recommended maximum values.

A5. Rating of Fluids as Heat Transfer Agents (25°C or 77°F)

Selection of an ECS-to-Integrated Rack heat-transfer fluid involved both quantitative and qualitative factors.

A reasonable indication of the effectiveness of a heat-transfer fluid is measured by the rate of heat transfer divided by pumping power, all

other conditions being equal. Such a rating criterion was developed by AIRESEARCH Manufacturing Company.[1]

AIRESEARCH's equation is:

$$\Phi = \frac{\rho^2 \, C_p^{2.4} \, K^{0.6}}{\mu^{0.6}}$$

where:

ρ density lb/ft^3

Cp specific heat BTU/(lb/°F)

K conductivity BTU/(lb/°F)

μ viscosity lb/(sec/ft)

Fluid	ρ	Cp	K	μ	Φ	Relative Φ
Air	0.073	0.24	0.015	1.24×10^{-5}	1.23×10^{-2}	7×10^{-5}
Freon 22 (liquid)	74.53	0.3	0.0507	1.33×10^{-4}	1.09×10^{4}	62
FC-75	110.	0.25	0.037	9.47×10^{-5}	1.56×10^{4}	89
Coolanol 20	48.7	0.45	0.069	1.15×10^{-4}	1.62×10^{4}	93
60% Glycol - 40% water, by weight*	62.2	0.9955	0.352	$6. \times 10^{-4}$	1.75×10^{-5}	1000

*Freezing point: -34.7°C

A6. Coolant Choices

Coolanol 20 appears to be the best of the liquid coolants for a closed-loop single-phase link between the ECS and a remote integrated rack. Air cooling is seen to be very poor, compared with any of the liquid coolants.

The use of one of the Freons in a vapor-compression ECS with the evaporator in the integrated rack would prove the most efficient coolant from the standpoint of heat transferred vs pumping power due to the utilization of the heat-of-vaporization. A temperature rise of about 335°F of liquid Freon 22 absorbs the same heat as does the boiling of the same amount of liquid Freon 22.

1. Airesearch Manufacturing Company, "Design Manual for Methods of Cooling Electronic Equipment," NAVWEPS 16-1-532, page 3-116.

A Freon evaporator in the integrated rack could be coupled to an air heat exchanger to realize the very effective direct air cooling/ dehumidification discussed earlier in this report under module cooling. A second, but considerably less effective configuration (See module cooling section.) is conduction-cooled modules clamped to cold plates which are integral with the rack.

The major danger in extending Freon lines from the ECS to the racks is that the smallest of leaks would allow air to enter the vapor-compression loop, drastically raising condenser film coefficients. It is possible for atmospheric air to enter the system even though the Freon pressure is above atmospheric pressure through leaks which are of sizes comparable to the mean free path of the molecules. For this reason, a separate closed loop with a coolant such as Coolanol 20 between the remote integrated racks and the ECS would result in a more reliable system.

A7. Producibility and Cooling Considerations

Producibility considerations for each module type needs to be extended to the rack interface in order to get a more complete picture of manufacturing compexity as related to module design:

1) Conduction cooling requires that intimate contact be maintained between the module heat sink and the cold plate and, at the same time, the module must be plugged into a connector with essentially no float. These requirements require that the module rack and back plane be fabricated to close tolerances, and in addition, necessitates assembly fixturing both at the back plane and rack assembly levels to set up the necessary relationships.

2) Convection cooling does not require intimate contact at the module/rack interface. This allows the use of spring type guides for mechanical edge support which will take up some guide-to-back-plane misalignment. The same relationships as the conduction-cooled assembly still need to be maintained, but the accuracy required is reduced.

3) Liquid cooling, when carried down to the module level, adds additional complications to the rack, since a third interface is required - that is, coolant ports on the module to coolant distribution on the rack. In addition, compact fluid couplings which are easily actuated and contain the fluid when mated and unmated need to be developed.

3.4.3 System Thermal, Weight and Volume Characteristics

The approach followed to develop these system-level performance characteristics used the module- and system-level partitioning analysis information and module performance characteristics presented in Section 3.2. The analysis included the four module types selected in Section 3.3; i.e., the I-2A, HI-2A, I-2X and I-2B configurations.

3.4.3.1 Thermal

The Environmental Control System and rack thermal analysis established the rack operating temperature limits which allowed thermal performance evaluation of various module sets at the rack level. The following rack operating temperatures were used for this evaluation:

a) An average air temperature of +50°C was used for direct-impingement cooling.

b) An average cold plate temperature of +45°C was used in evaluating conduction cooling.

Another basic decision in the study addressed the limits to which the I-2A module should be used, recognizing that it is not capable of dissipating the required 20 watts in the conduction-cooling mode. The information in Section 3.3.2 was used to establish these limits:

Case 1 - System composed of all I-2A modules.

Case 2 - I-2A modules used at power levels $\leq$ 6 watts; I-2B > 6 watts. This breakpoint was based on the conduction thermal capacity limit of the I-2A module, typical of forced-convection-cooled WRA applications where the cooling air exhaust temperature is specified at +71°C.

Case 3 - I-2A modules used at power levels $\leq$ 12 watts; I-2B modules used at dissipations > 12 watts. This breakpoint represents the conduction limit of the I-2A module with +45°C cold plate cooling.

The remaining two situations evaluated were:

Case 4 - All I-2X modules

Case 5 - All HI-2A modules

Using the rack operating temperatures and the various module sets allowed a comparison of the thermal performance of each module set under direct air-impingement and cold plate conduction cooling. The results of this evaluation for the AEW system module complement is shown in Figures 3.4-14 through 3.4-17. Figure 3.4-14 shows the effectiveness of direct-impingement cooling as compared to conduction cooling as shown in the remaining graphs. The limited conduction cooling capacity of the I-2A is

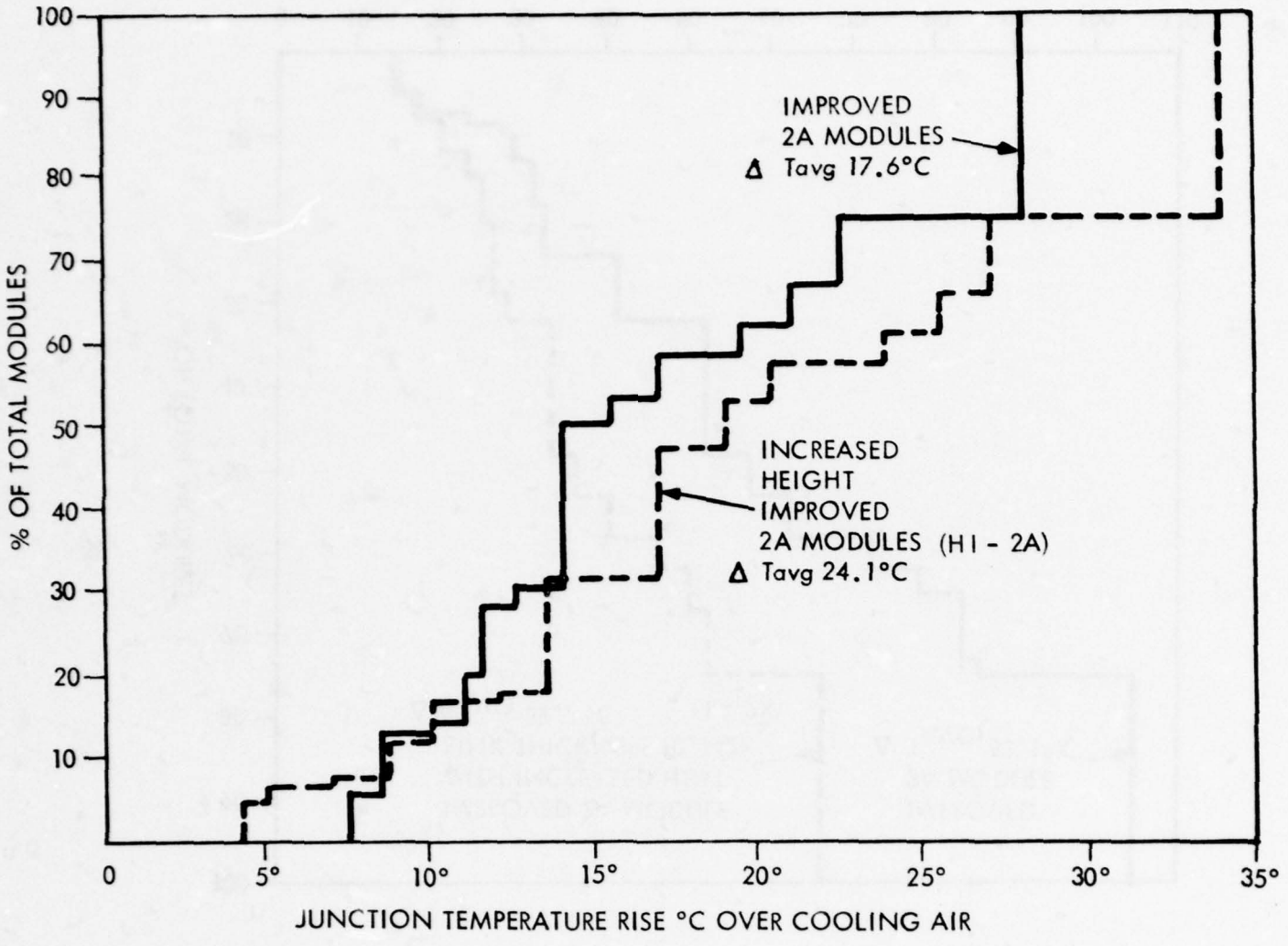


Figure 3.4-14. Direct Forced Correction Cooling for AEW, I-2A vs. HI-2A Modules

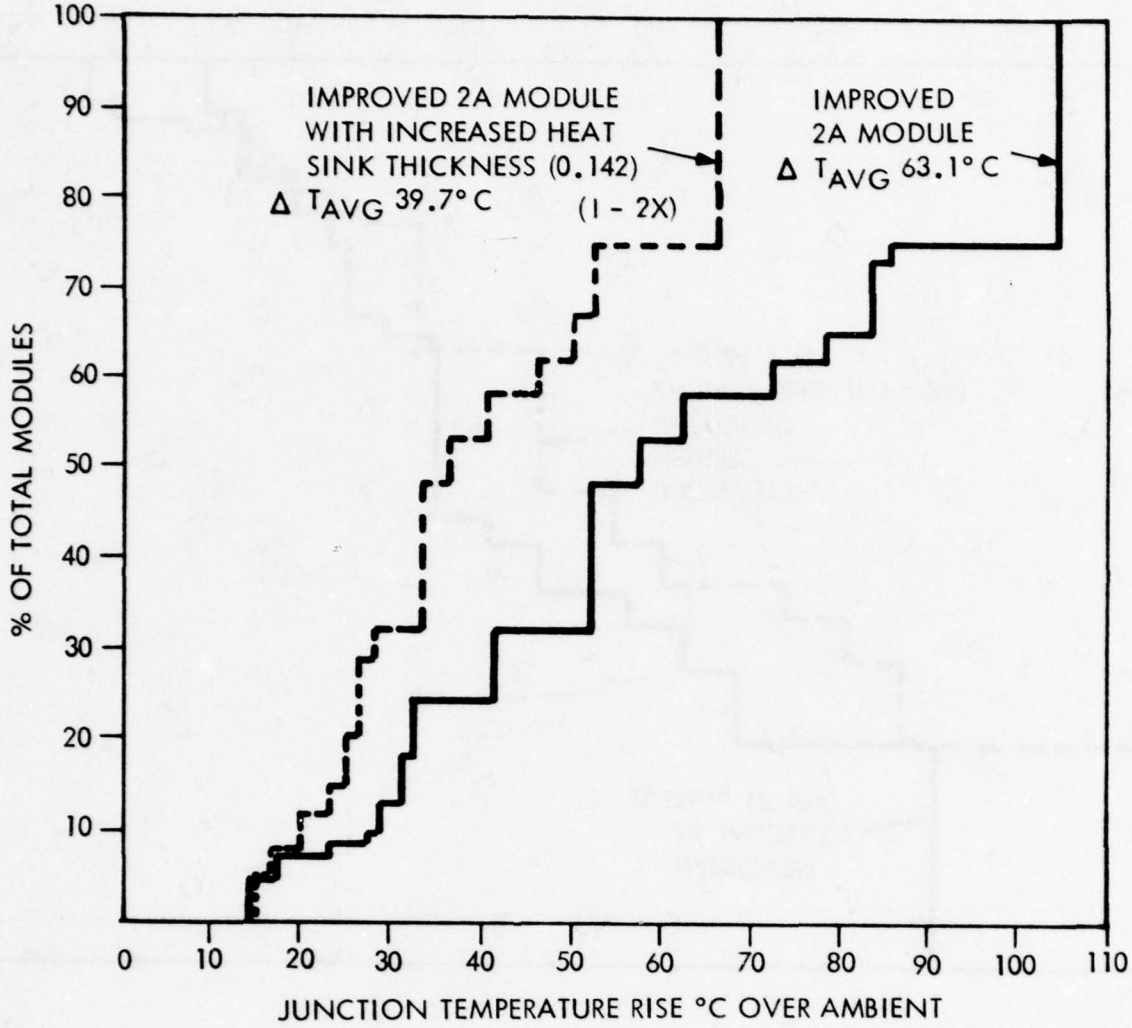


Figure 3.4-15. Conduction Cooling for AEW, I-2A with Heat Sink vs. I-2A Modules

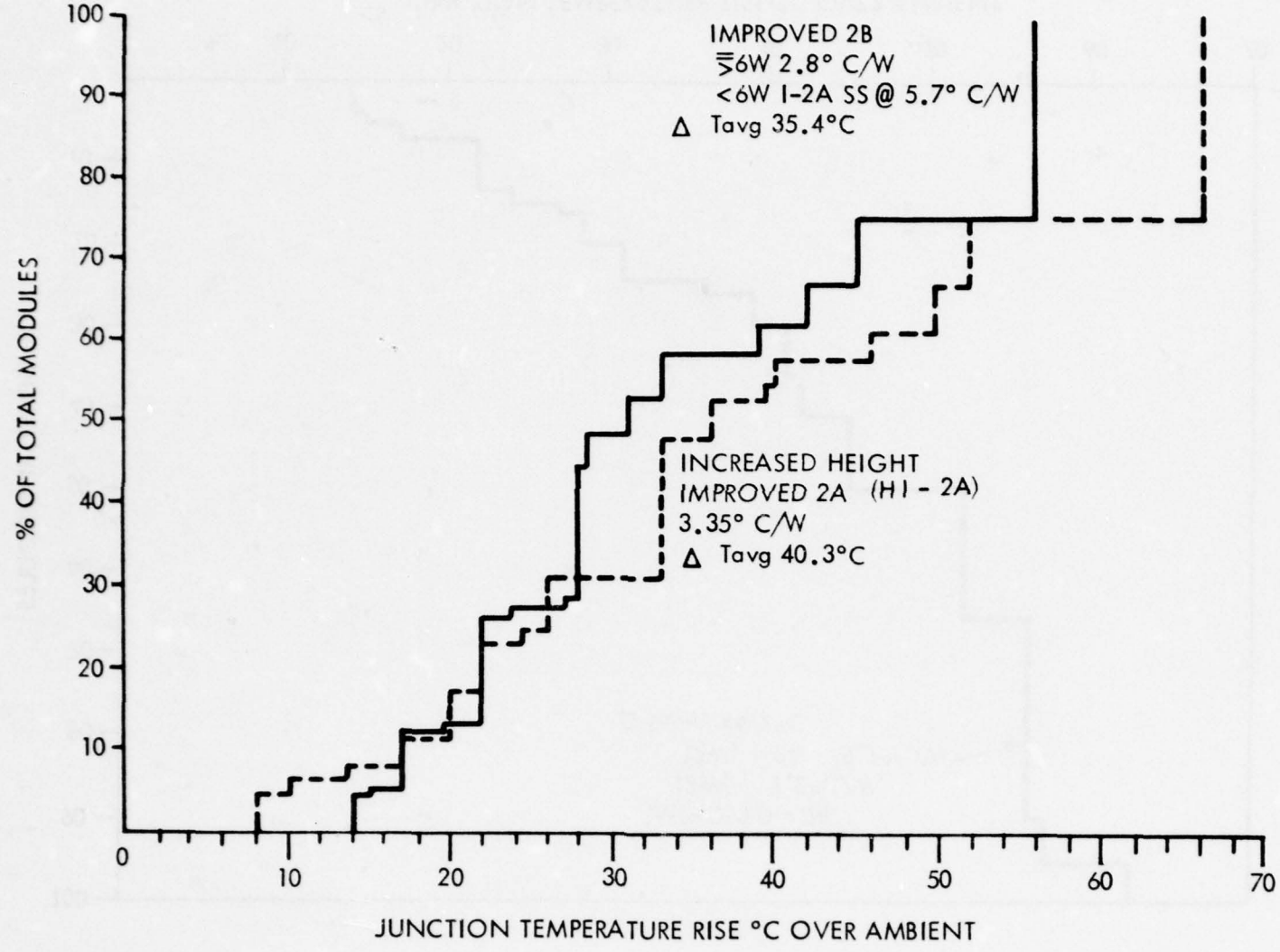


Figure 3.4-16. Conduction Cooling for AEW, I-2B vs. HI-2A Modules

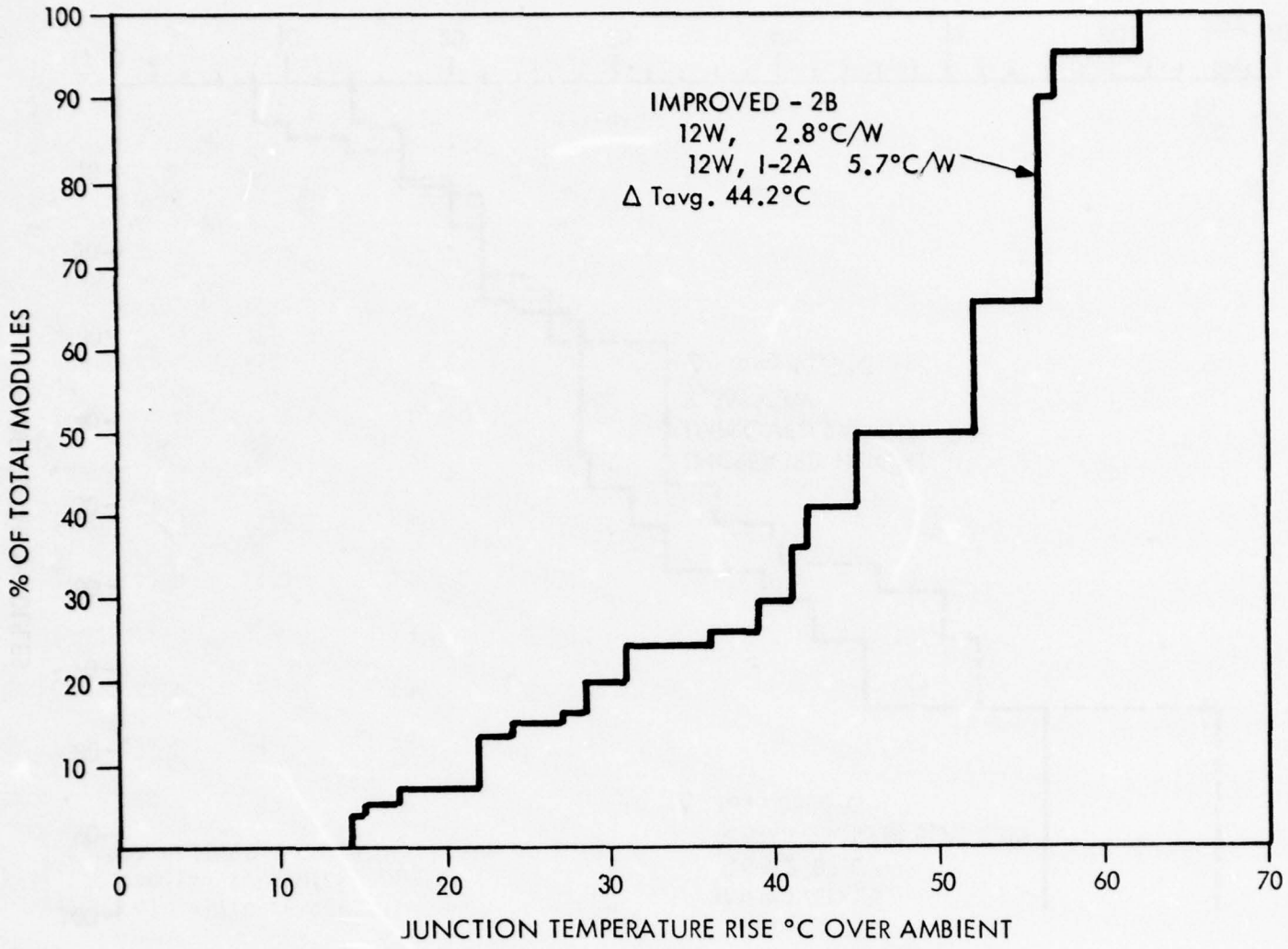


Figure 3.4-17. Conduction Cooling for AEW, I-2B Modules

shown in Figure 3.4-15. The 105°C temperature rise corresponds to a +150°C junction temperature with a +45°C cold plate temperature.

The maximum and average junction temperatures for each condition are listed in Table 3.4-5. The temperatures for the direct air cooling mode are all under +85°C. This limit was identified as the maximum permissible to achieve optimum life-cycle cost performance (Figure 3.2-7). The conduction mode temperatures are higher, although the average is close to the +85°C < cc limit.

3.4.3.2 Volume and Weight

The AEW module complement along with the weight and volume of the basic rack design was used to determine the AEW system volume and weight estimates listed in Table 3.4-5.

It should be noted that the I-2A yields the least weight and volume, but is inadequate in the conduction-cooling mode.

The HI-2A configuration meets the conduction cooling performance requirements at very slight increase in weight (<3%) over that of the I-2A. Four racks are required for both the I-2A and HI-2A implementation. The greater volume of the HI-2A system is the result of the increased rack depth to accommodate the HI-2A module.

The remaining configurations involving combinations of I-2A/I-2B modules and I-2X modules result in significant increases over the HI-2A. This is a result of the additional racks required and increased module weight.

The main advantage of the conduction-cooled (liquid cold plate) version is the significant reduction in system volume. This could be a prime decision factor in addressing the installation requirements of a high-performance aircraft.

A volume and weight evaluation of conventional WRA packaging was also performed. The WRA used in the comparison was based on the 1/2 ATR light-weight card cage unit developed by Raytheon. The size was adjusted to allow space for Wire-Wrap back panels. The results indicate an 86-pound (17%) weight penalty using the WRA approach (compared to the I-2X figures). The volume of the ATR approach lies within the range of the comparable MAP approach.

It is expected that the WRA approach would result in increased system connector requirements, and reduced reliability, because of the quantity (25) of WRAs.

Table 3.4-6 compares the performance of the HI-2A configuration to the best thermally acceptable SEM compatible system. This table indicates the relative system level penalty that must be accepted in order to achieve a SEM compatible configuration.

Table 3.4-5. Module Characteristic Summary System Level*

Characteristic		Module Type I-2A	I-2B(2) >6 watts	I-2B(3) >12 watts	I-2X	HI-2A	5/8 ATR With I-2X
Module Pitch (Inches)		0.3	0.3 & 0.6	0.3 & 0.6	0.4	0.3	0.4
Average Junction Temp.	Convection	+68°C	+68°C	+68°C	+68°C	+74°C	Not Investigated
	Conduction	+108°C	+80°C	87.8	+85°C	+85°C	
Maximum Junction Temp.	Convection	+78°C	+78°C	+78°C	+78°C	+84°C	Not Investigated
	Conduction	+149°C	+101°C	+107.4°C	+111°C	+111°C	
Quantity of Racks		4	6	5	5	4	25
Rack Utilization		77.5%	73%	76.6%	71.7%	71.4%	69%
Volume (Ft^3)	Convection	15.1	22.6	18.8	18.8	18.1	
	Conduction	8.8	13.2	11.0	11.0	10.5	16.2
Weight (Lbs)	Convection	442	557	501	507	454	593(1)
	Conduction	447	565	507	513	459	

*AEW System

Note (1) Includes estimated cable, rack and heat exchanger fan weight.
(2) +71°C cooling air (MIL-E-5400)
(3) +45°C cold plate temperature

TABLE 3.4-6. Module Tradeoff Summary V/STOL AEW System

	HI-2A (3/8 ATR)	SEM	Δ%
Racks	4	5	+25
Weight	454 lbs	501 lbs	+10
Volume	18.1 cu. ft.	18.8 cu. ft.	+4
Module Face Area	10.0 sq. ft.	13.4 sq. ft.	+34
SEM Compatible	No	Yes	-
Chip Carrier Compatibility	Yes	No	-

Table 3.4-7 shows the weight improvement that might be realized in implementing a new system using advanced circuit technology and Modular Avionic Packaging. The MAP weight estimates are based on using the HI-2A module. The results indicate a weight reduction in the range of 68 percent as compared to present S-3A avionics. It must be emphasized that this comparison addressed only that portion of the S-3A system that is applicable to MAP. This amounted to approximately 40 percent of the total system weight.

3.4.3.3 Conclusions

1) The integrated rack approach, in conjunction with advanced circuit technology, achieves a weight reduction in excess of 50 percent as compared to current production avionics.

2) The integrated rack is lighter weight than the conventional WRA approach (approximately 15 percent).

3) The integrated rack study using the HI-2A module (3/8 ATR) yielded a lighter weight system than the closest SEM compatible configuration (SEM computable is 10 percent higher).

4) Direct air cooling of modules using closed cycle conditioned air offers the best thermal performance (+85°C maximum junction temperatures vs +110°C for conduction cold plate cooling).

5) EMI/EMP is a significant driver in rack design and material selection.

6) Rack material electrical conductivity requirement precludes use of common composite materials. Development of conductivity enhancement schemes for composites is required.

7) Power supplies are up to 50 percent of the total module volume and 40 percent of the total module weight based on a 2X improvement over current technology. Increased emphasis on power supply development could achieve a 3X density improvement further reducing this penalty.

8) A liquid cold plate conduction cooled rack offers a 40 percent volume advantage without a weight penalty over direct forced convection cooling. This could be an overriding factor in crew compartment (core avionics) and high performance aircraft installations.

9) A liquid cold plate conduction cooled rack is subject to ECS single point failure modes. Redundant coolant loops with split integrated cold plates should be considered for degraded mode operation.

10) The convection cooled rack features desgraded mode operation in event of ECS coolant loop failure. Calculations indicate that the maximum junction temperatures would not exceed +125°C in this mode.

Table 3.4-7. S-3A V/STOL Avionics Weight Comparison

S-3A Avionics	
Total System Weight	4348.5 lbs.
Candidate for MAP	1980.5 lbs.
Portion Addressed in Map Study	1774.9 lbs.
MAP Study	
Core - Two Racks	215 lbs.
ASW - Three Racks	345 lbs.
	560 lbs.
68% Reduction	

11) The integrated rack can be configured for front access and maintenance allowing maximum installation versatility.

- Front removable back panel
- Front routed and accessible inter and intra rack wiring.

12) Back panel producibility constraints are important to efficient subsystem definitions. Module pitch should be minimized to allow maximum subsystem partitioning flexibility within size constraints.

13) Integrated rack approach facilities optimum subsystem partitioning. Back panel sizes and module groupings are not limited by WRA box constraints.

14) The use of fiber optics and signal multiplexing is an essential element of the integrated rack weight and maintainability objectives. The resultant reduction in interconnect complexity contributes to the practicality of front access maintenance concepts.

15) Zero insertion force connector concept would offer the advantage of efficient use of increased rack depth but at the penalty of increased mechanical complexity and module cooling method limitations. Industry survey indicates there is no strong push for commercial development and use of ZIF connectors.

3.4.4 Integrated Rack Concept with Zero-Insertion-Force (ZIF) Connector

3.4.4.1 Advantages

The use of ZIF connectors in the integrated rack concept offers many advantages over conventional connector types. A rack concept utilizing the ZIF connector has been developed for this study. It offers the following advantages.

1) Permits the use of a deep rack thereby better utilizing available space in the aircraft, without resorting to slide-out drawers or hinged fold-out door unit.

2) Permits front access to modules and motherboard.

3) Allows for hard-mounting of all cabling and internal wiring, eliminating the need for costly and less reliable wiring methods such as hinged cabling, fold-out wiring and slide-type cabling requiring excessive cable service loops.

4) Provides quick access for maintenance and replacement of entire subsystem circuitry.

3.4.4.2 Rack

The rack used in this concept is a pier type rack, 20 inches wide, 22 inches deep and 64 inches high, (See Figure 3.4-18). Input/Output connectors are located on the top surface to provide the external wiring interface to the rack. The rack structure provides five sections for avionics circuitry, one section for power supply, and one section for the heat exchanger and dehumidifier unit. Internal cabling areas are provided at the top and left side of the rack structure. An area in the back, and the area in the front of the rack are used as a plenum to circulate forced cooling air over the circuit cards (See Figure 3.4-19.).

3.4.4.3 Light-Weight Card Frames and Circuit Cards

For this study a circuit card shown in Figure 3.4-20 was designed. The useable component area is approximently twice that of a single-sided improved 2A module. Connections to the circuit card are made by edge-card contacts mating with ZIF connectors on the mother-boards. Each circuit card contains 108 edge-card contacts. The light-weight frames are used to support and position the circuit cards for proper mating into the ZIF connector (See Figure 3.4-21). The frames are capable of mounting five circuit boards, (Figure 3.4-22) or multiples of the size shown in Figure 3.4-20. Spring-loaded mounting fasteners are used to secure the circuit cards to the frames. Frames and circuit cards are front removable from racks without removing any other frames or circuit cards.

3.4.4.4 Motherboards

The motherboards consists of an aluminum plate 17 inches x 16 inches x 0.125 inches thick. Twenty-eight ZIF connectors are mounted to the mother-board. Each connector has 310 wire wrap pins.

3.4.4.5 Power Distribution Unit (PDU)

The power distribution unit is used as an interface between the interconnection wiring and the mother boards. Interconnection cabling mates with connectors on the front surface of the PDU. Internally, the connections are distributed to circuit card edge contacts, which in turn mate with the ZIF connectors on the motherboard. Special power supply voltages can also be generated within the PDU. Each PDU contain 1620 edge-card contacts which are used to interface with two mother boards, see Figure 3.4-23.

3.4.3.6 Rack Capacity

The rack contains five sections for avionics circuitry. Each section is capable of mounting 25 frame assemblies, and each frame assembly five circuit cards, for a total of 625 circuit cards per rack. This quantity of circuit cards would accommodate all circuitry required for a AEW mission on a V/STOL aircraft.

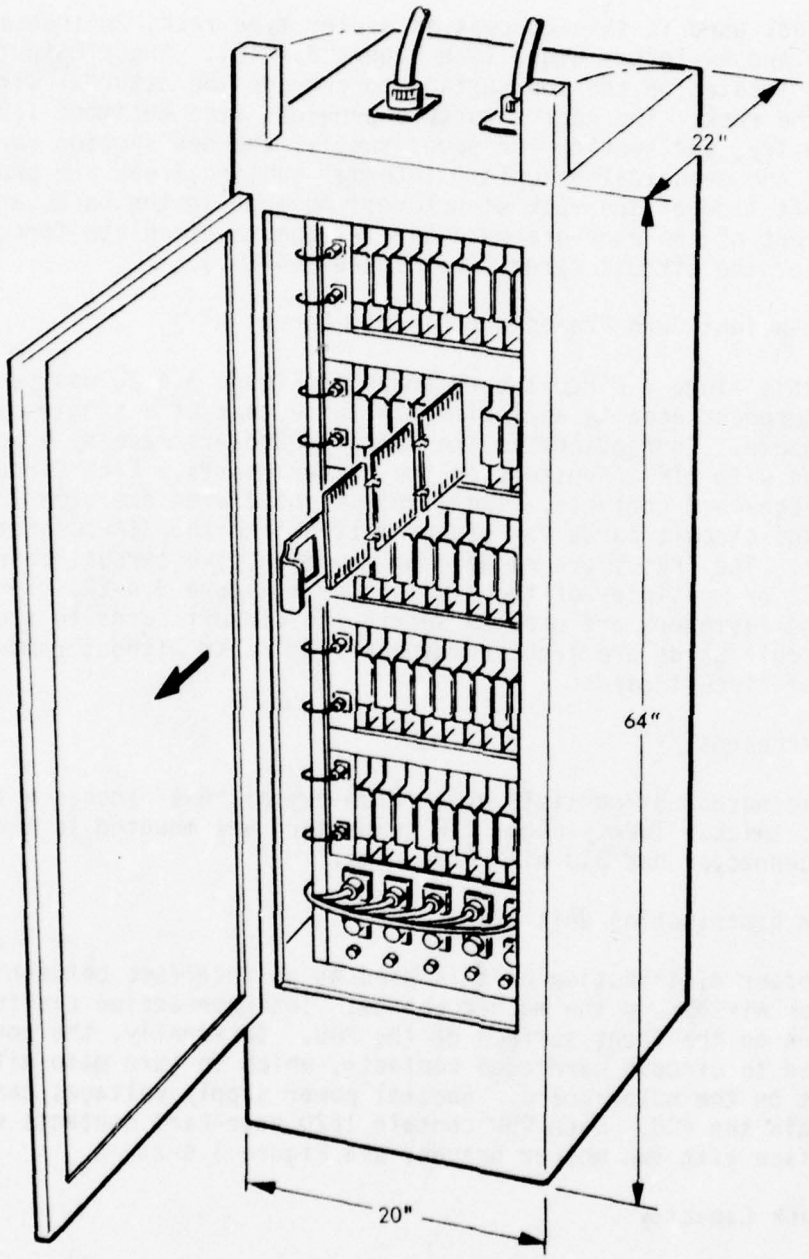


Figure 3.4-18. Integrated Rack Concept for Use with ZIF Connectors

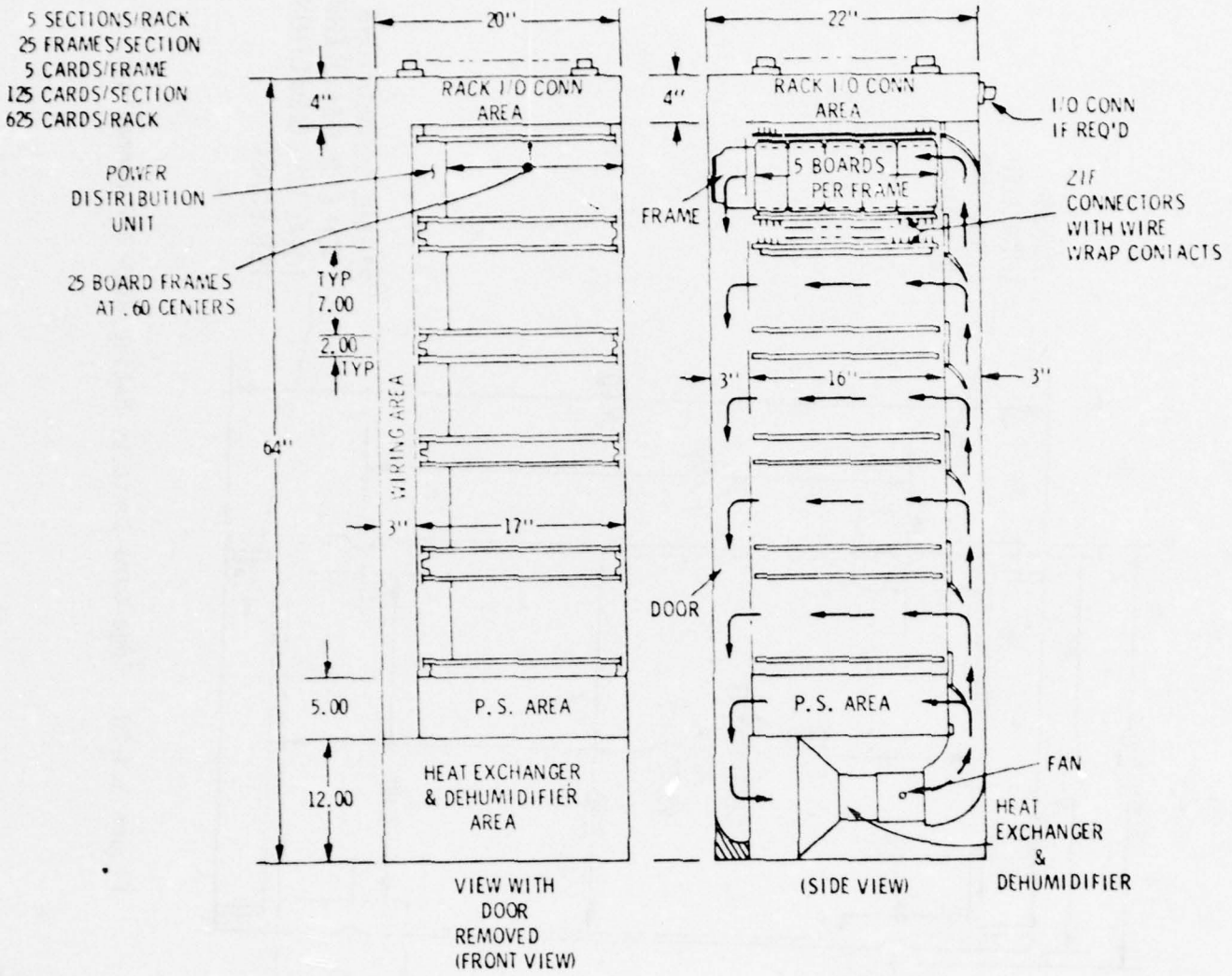


Figure 3.4-19. Integrated Rack Concept, Illustrating Cooling Method - Air over Components

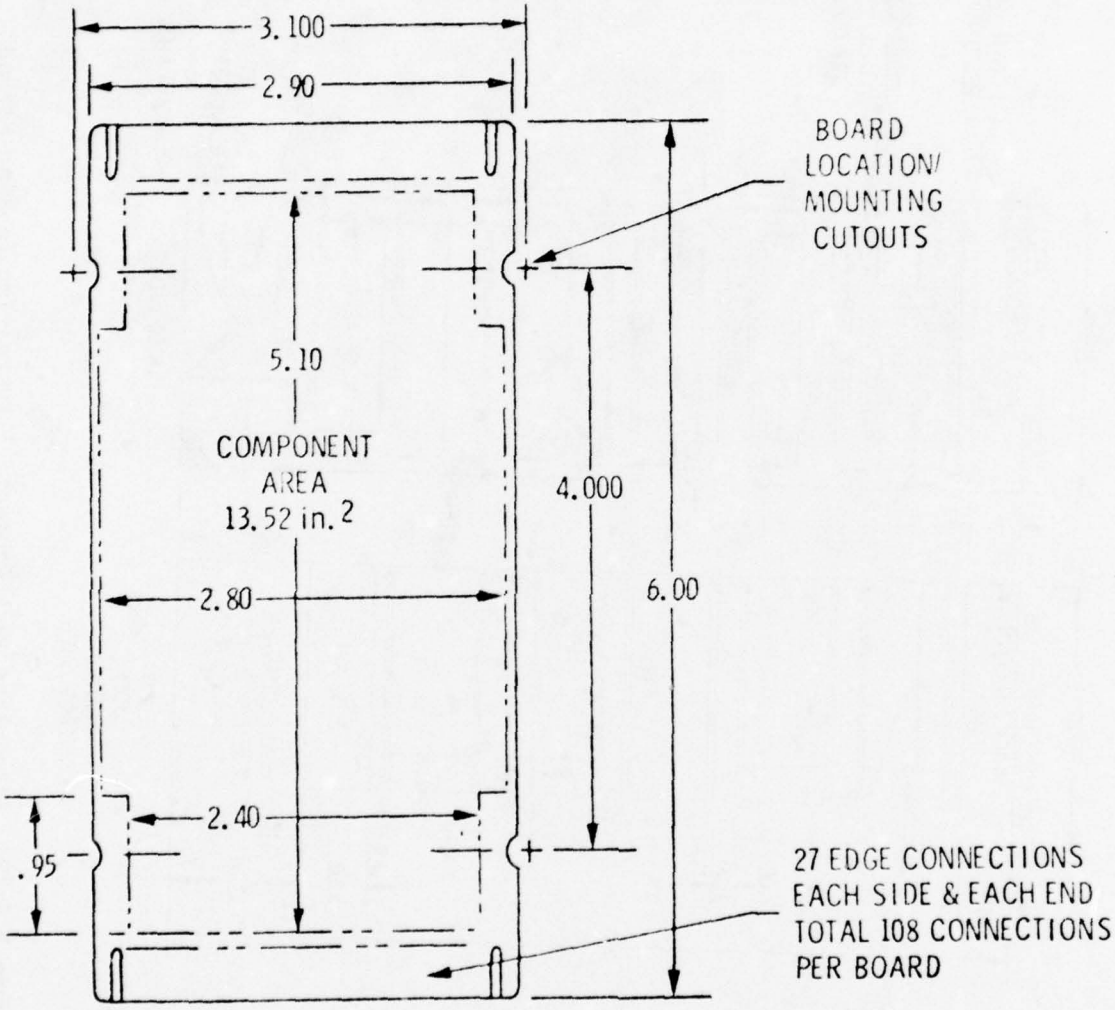


Figure 3.4-20. Edge-Card Contacts Mating with ZIF Connector

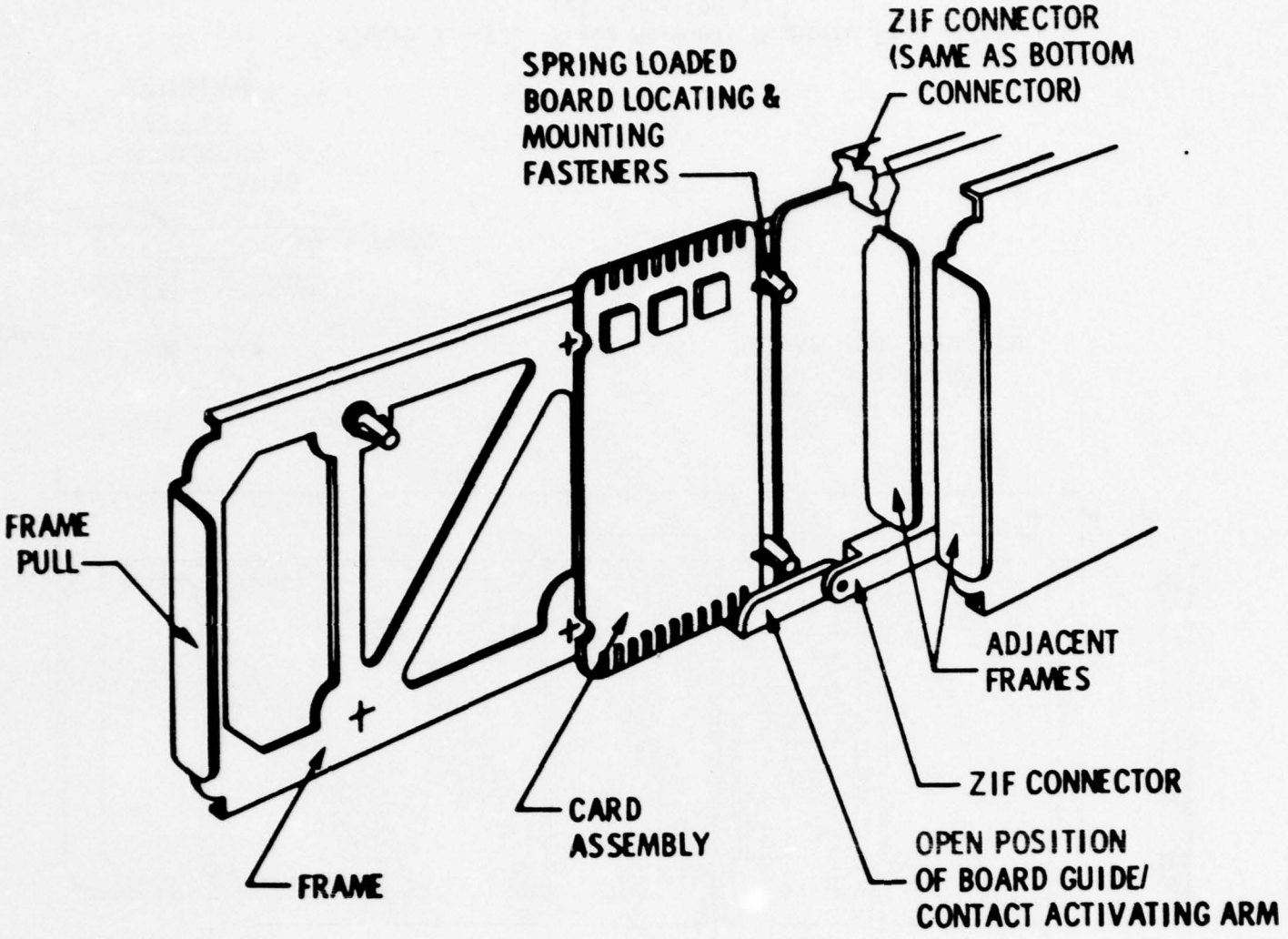


Figure 3.4-21. Assembly of Cards into Frame (ZIF Rack Concept)

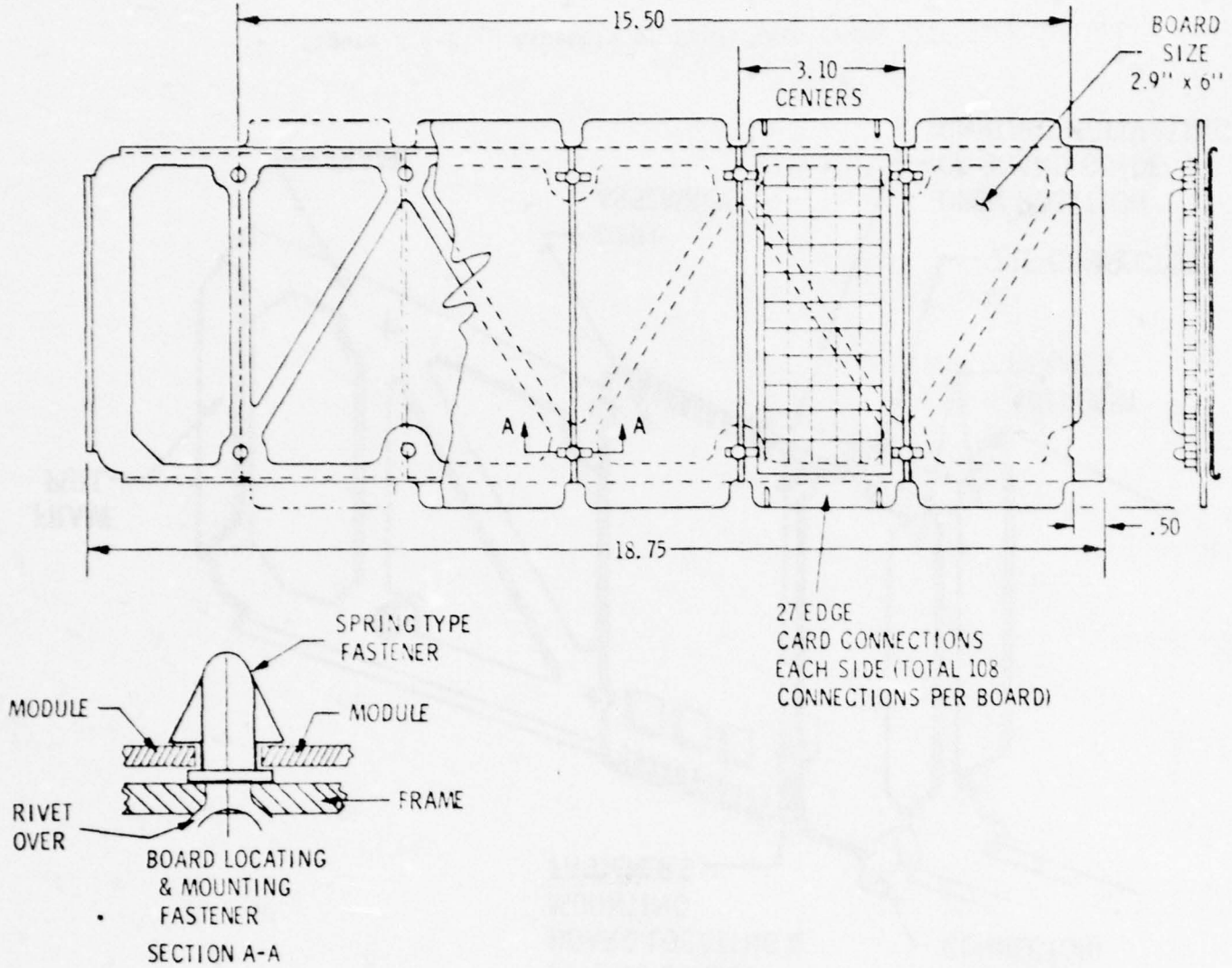
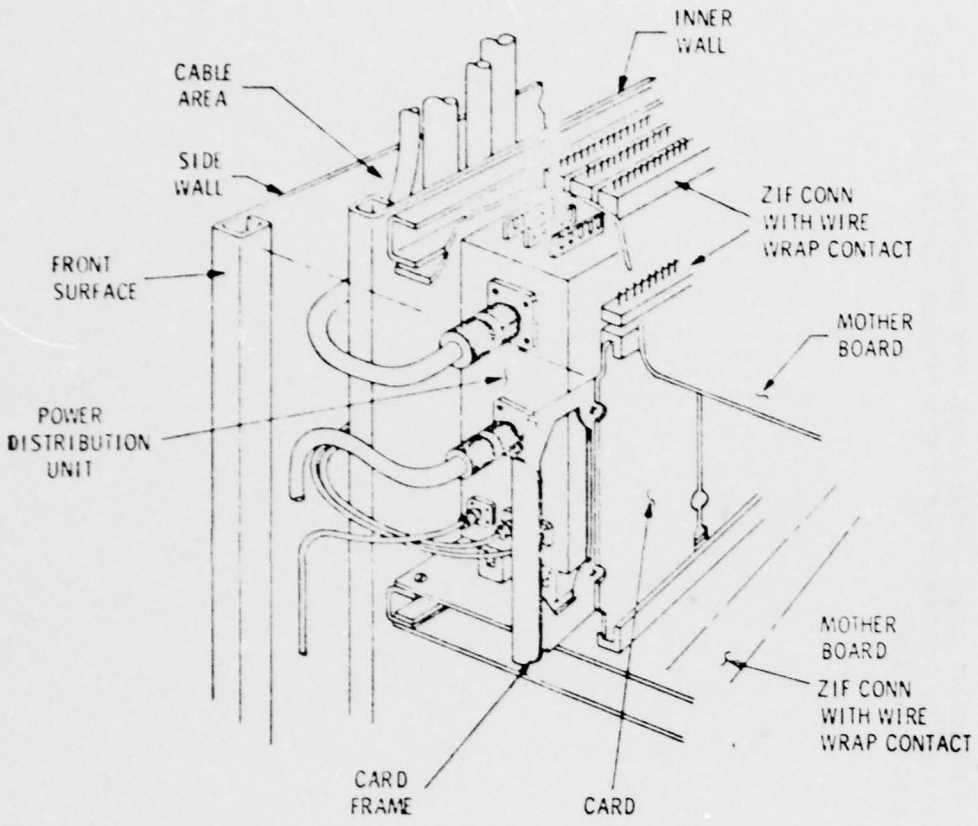


Figure 3.4-22. Frame Assembly Mounting Five Cards (ZIF Rack Concept)



- POWER & SIGNAL CABLES RUN FROM I/O AREA TOP OF RACK, BETWEEN SIDE WALL & INNER WALL, TO POWER DISTRIBUTION UNITS
- EACH SECTION OF RACK CONTAINS ONE POWER DISTRIBUTION UNIT
- POWER DISTRIBUTION UNIT HAS EDGE CARD CONTACTS ON TOP & BOTTOM SURFACES
- MAXIMUM OF 810 CONNECTIONS CAN BE MADE TO EACH MOTHER BOARD DISTRIBUTION UNIT
- INTERCONNECTIONS BETWEEN MOTHER BOARD SETS CAN BE MADE INSIDE POWER DISTRIBUTION UNIT

Figure 3.4-23. Typical Power Distribution Method, for Use in Integrated Rack with ZIF Connectors

3.4.4.7 Further Study

Areas which would require futher study and further developement to insure that this concept will meet military application are listed below.

1. Keying of circuit boards to frames to insure fool-proof interchangeability of circuit cards.

2. EMI/EMP Shielding concepts.

3. Investigation of a frame design to eliminate frame loads carried by ZIF connectors.

4. Developement of a ZIF connector with 0.10 inch contact centers and a mounting pitch of 0.60 inches.

5. Development of an efficient conduction heat-transfer method.

The ZIF rack concept advantages and disadvantages are summarized in Table 3.4-8. The reasons for recommending discontinuing further effort in concept development are also given.

Table 3.4-8. ZIF Rack Concept

ADVANTAGES

- Efficient utilization of rack face area
- Eliminate hinged and slide mounted units
- Direct access for maintenance
- Direct air cooling of module
- Variable size modules

DISADVANTAGES

- Modules not readily adaptable to conduction cooling
- Connector development required - not supported by industry requirement
- ZIF connector concept in airborne environment judged high risk

REASONS FOR DISCONTINUING CONCEPT DEVELOPMENT

- Rack depth characteristic not required for V/STOL
- Considered high risk approach - connectors and module interface
- Not comparable with conduction cooling

3.5 WRA Concept

The WRA concept would involve standardization of replaceable subassemblies to allow them to accommodate the standard module, and to insure proper fit into the standard rack. Figure 3.4-12 showed a recommended WRA or multiple-module assembly to be used with an air-cooled rack. The assembly, part of which resembles a card cage, is front-removable from the rack. The backpanel for the WRA is attached to the back side of the WRA. If the selected cooling method involves passing air over components, then slots will be provided in the WRA side walls to allow air to pass between or through modules.

The air ducts in the track would have continuous opening over the full height of the rack. If the cooling method involves conduction-cooled modules and an air-cooled heat exchanger, then the outside walls of the WRA would contain their own finned heat exchangers. In this third case, where modules are conduction-cooled to a liquid-cooled heat exchanger, the side walls of the WRA would be provided with guide ribs to effect a thermal interface with the heat exchanger in the rack. Because of the shallow depth of the modules and WRA, mechanical support would not be required in the back of the WRA is the structure is properly designed. This is a significant advantage because it eliminates the need for costly tight locating tolerances for bushings and pins. Unique modules, such as some analog types, which do not lend themselves to packaging on the standard-size module could also be packaged to fit within the WRA envelope.

The WRA would provide the following advantages:

- More effective EMI shielding between modules
- A single overall assembly for ease of handling and testing.

In order to maintain control over the fit and form factor of the WRA, all outline dimensions, mounting-hole dimensions and I/O connector locations and types should be controlled by the procuring activity.

3.6 EMI/EMP Concepts for a Modular Avionics Packaging System

3.6.1 Introduction

An investigation of electromagnetic compatiblity requirements for a V/STOL system was made to determine what concepts might be implemented in a Modular Avionics Packaging System. Where the concept employs existing technologies, guidelines are presented which should insure a packaging design compatible with system requirements. Concepts which need further development are identified.

The fundamental requirement of a system is that all associated subsystem/equipment, both airborne and ground, be designed to achieve system compatibility. Accomplishment of this objective requires consideration of many factors. Of primary concern are the electromagnetic fields which can be within the operational environment of the system, and the susceptibility level of the most sensitive device which is required to function within these fields. These two key areas of concern are investigated for the purpose of establishing a requirement baseline, from which packaging design guidelines are developed. Summary of EMP and EMI requirements are outlined in Tables 3.6-1 and 3.6-2.

3.6.2 Discussion

Device susceptibility predictions for a Modular Avionics Packaging System which would utilize an integrated rack concept are based on data contained in Integrated Circuit Electromagnetic Susceptibility Investigation (1). Levels of susceptibility versus frequency are available for several generic digital, linear and hybrid integrated circuits from 0.22 GHz to 9.1 GHz. Susceptibility below 0.22 GHz and above 9.1 GHz is projected flatly to 0.05 GHz and 40 GHz respectively. The rf level, to which the most sensitive generic type of device is susceptible, is used as a basis for generating guidelines, since all three types are likely to be used in most avionic systems. This power level of 6 microwatts is translated to an electric field intensity of 50 millivolts/meter if a device impedance of 100 ohms is assumed. A further assumption is made that the energy is coupled into a susceptibility device by an equivalent dipole, whose effective height is calculated for most efficient coupling at the most critical frequency.

Predictions are that electromagnetic field intensity levels which might be encountered within the operational environment will be similar to those defined in the DNA Handbook, Volume 3, and in the General Specification for V/STOL System Electromagnetic Compatibility Requirements.

Based on the predicted susceptibility level of 50 millivolts/meter, and a possible operational environment field intensity of 200 volts/meter, the design of an electronic system must provide for approximately 90 dB of shielding.

As much as 30 dB of shielding can be provided to electronic equipment aboard an aircraft by an aluminum skin structure alone. The

Table 3.6-1. EMP Requirements

Frequency Range	0.01 - 100 MHz
Surface Current	10.7 amps/inch

Interface Connector

(A) Pin Current -	5.34 amps peak
(B) Pin Voltage -	534 volts peak

Source generator is 534 volts and 100 ohm source impedance

$V = 500\ K\ e^{(\ Ft/Q)}\ SIN\ 2\ ft$

$K = 1.033$

$Q = 24$

Field Intensity	160,000 volt/meter

Acceptance Criteria

(A) Flight Stability Circuits - no upset - need 130 dB

(B) Mission Critical - Upset o.k.; must recover within specified period; no damage

(C) Non Mission Critical - No damage - need 70 dB

Table 3.6-2. EMI Requirements

External Environment

- Frequency Range 10 KHz - 40 GHz
- Field Intensity 2000 volt/meter max.
- Calculated Shielding Required

  80 dB 10 KHz - 200 MHz

  40 dB @ 1 - 10 GHz

  20 dB @ 10 - 40 GHz

- Calculations Based on

  (1) MCAIR Device Susceptibility Handbook

  (2) EMC Requirements, V/STOL System, general spec. for

remaining 60 dB of shielding, in this case, would be provided by the equipment rack and/or enclosure design. If a boron epoxy composite material is used as the aircraft skin, no shielding will be provided. Its use is not likely, and is not considered in this EMI/EMP concept study because of its unsuitability from the standpoint of lightning protection. Graphite epoxy has the capability of providing about 15 dB of shielding effectiveness. The ability to realize this shielding capability is directly associated with the ability to maintain electrical continuity at structure interfaces. Airframe manufacturers are developing methods, such as application of conductive spray or screen mesh on the inner surface of graphite epoxy, which would provide continuity to the airframe. The screen-mesh technique provides levels of EMI/EMP and lightning protection which approach those of aluminum.

If a conservative estimate of 15 dB shielding effectiveness is obtained from an aircraft skin structure, then an electronic equipment enclosure within the aircraft must provide an additional 75 dB shielding. The mechanical design requirements for a Modular Avionics Integrated Rack which would provide 80 dB shielding are included as an appendix. An enclosure designed to the outlined requirements is typical for avionics peculiar to a mission profile, or for avionics common to several mission profiles. Summarized shield design approach is outlined in Table 3.6-3. A susceptible condition may still exist due to interface power, control, and signal lines between Core and mission avionics. The susceptible condition can be prevented by following the Check List Of General Design Criteria (2). Ideally, all interfacing would be accomplished by the use of fiber optics. However, the application of fiber optics is limited to control and signal lines. This limitation is further extended relative to signal power level and frequency. Technology is rapidly advancing in the development of these parameters. The advantage of immunity to EMI/EMP, which fiber optics has, must be exploited due to the possibility of severe requirements as defined in V/STOL System General Specification (3).

These requirements could not be met easily without the use of fiber optics due to the prohibitive cost and weight of conventional filters and shields which would otherwise be required. Cable design approach summary is outlined in Table 3.6-4.

Primary power distribution lines can be filtered and shielded to the extent required for system compatibility by conventional means. The best shield is conduit or an integrated cableway. A separate return line must be provided and routed with each for primary power line. Low voltage conversion and regulation is ideally done as close to the load as practical. Space and power requirement partitioning among subsystems may dictate the centralization of all power-conditioning units. If secondary power must be distributed between subsystems, it should be routed with other power lines, as opposed to intermixing power lines with control or signal lines. To prevent coupling of switching, spikes or transients from one power line to another, each power line pair should be twisted, as a minmimum, and preferably have its own shield. Connectors should have an EMI backshell to insure peripheral dc bonding resistance to shields-to-ground reference of less than 2.5 milliohms.

Table 3.6-3. Shield Design Approach

- Shield against External EMI/EMP Environment
- Aircraft Composite - 10 dB
  - Graphite Epoxy
  - Metal Spray
  - Screen Mesh
- Rack - Design for 80 dB

Metal thickness	0.032 in. min.
Occasional holes	0.4 in. max. dia.
Pipe openings	L/D = 3:1
Vent openings	Screened
2 in. opening	6 mesh std/inch
2.5 in. opening	10 mesh std/inch
3 in. opening	12 mesh std/inch

  - Perforated patterns - 40% open
  - Honeycomb - welded
  - Finish - Conductive
  - Joint Overlap = 1/2" min.
  - Access Doors - Seal all around; 3 point latch
  - Bonding 2.5 Milliohms/Joint
- Total Isolation 90 dB at 200 MHz

Table 3.6-4. Cable Design Approach

- Power (270 VDC)

  Route as low Z laminated bus

  Floating from structure

  Filter at rack power input point

  Redistribute on twisted pairs

- Signal (<200 MHz, Low Power)

  External to Rack - Fiber optics, conduit or multishielded coax

  Internal - Wire wrap back plane, twisted pair, coax or fiber optics

- Control

  External to Rack - Shielded twisted pair

  Internal - Twisted pair, or shielded as required, or fiber optic

- Digital Power - 5 volt plane and chassis grounded back plane return (low Z)

- Analog Power - Voltage plane and chassis ground back plane return (low Z)

For co-located modules common to a subsystem or to different subsystem, but within a common equipment enclosure, compatibility may be preserved by baffles in the enclosure or by shields which are integral to circuit assemblies. The amount of shielding required is a function of the emission level of the offending circuit, the susceptibility threshold of the vulnerable circuit, and the path losses between the two circuits. The path loss is a function of the physical separation of the two circuits and materials which occupy the space between them. A quantitative number therefore cannot be placed on the shielding required between circuits within a common enclosure. A program should be developed which will study the required shielding for generic types of modules. Internal rack isolation guidelines summary is outlined in Table 3.6-5. Also, a short test could be run on each module at module level to determine if it is susceptible to predicted levels of EMI, and if its emissions exceed certain limits. The limits of susceptibility and emission would be as determined by the study program to be required for mission compatibility. Specification and test requirements are outlined in Tables 3.6-5 through 3.6-9 and Figure 3.6-1.

3.6.3 Conclusions

The design of an electronic system must provide approximately 90 dB of shielding as determined by susceptibility threshold and intensity of interfering signal. Boron epoxy composite cannot be used as a material in the fabrication of an integrated electronic equipment rack due to its inability to provide shielding. Graphite epoxy may be used if electrical continuity at interfaces is preserved.

Fiber optics should be used where possible because of their immunity to EMP/EMI and to the potential weight savings offered by the elimination of a need for filters. Non-fiber-optic lines should be routed through conduit or integrated cable ways with power lines being routed separately from signal lines.

Modules of high emission levels or low sensitivity provisions should be made in the rack mechanical design for the use of baffles or shields between weapon replaceable modules as needed.

An EMI-tight, self-compatible system dictates the need for good shield design practice as it applies to general criteria such as dc bonding resistance, air-vent size, seams, etc.

3.6.4 Recommendations

Continuation of development of composite materials which offer high degrees of shielding effectiveness is considered essential. Development of extended bandwidth in fiber-optics systems would open more avenues toward the design of electronics systems immune to interference. A study program should be initiated as soon as possible with the objective of determining the shield required between weapon replaceable modules, as a function of their generic type and relative location within a common enclosure. Such a program would require inputs resulting from the module hardware development and integrated

Table 3.6-5. Internal Rack Isolation

WRM TO WRM

- Rely mainly on spacing between modules
- Provide for grounded baffle plates between WRM's, if required
- Provide for totally shielded WRM's if required
- Provide capacitive decoupling at each module PIP
- Give consideration to component location by function (unit compatibility)

Structure and Low Impedance Ground Place Designed to Maximize Capacitive Isolation

Cable Routing Layout Maximizes Isolation between Power, Digital and Analog

Table 3.6-6. Specification and Test

WRM - Anticipate three Levels of Module

- Type A - Relatively Inert

  No baffling or other isolation required to adjacent modules

- Type B - Modest Emission Levels

  or susceptibility (H.V. switching, Op. Amps) - some baffling may be required

- Type C - High Level Emission

  (Modulator Pulse) or low level Susceptibility (Receiver IF) require total RF shielding

Table 3.6-7. Specification and Test

WRM Type A

Time Domain Crosstalk Test

- Emission:

  Design module to keep coupled voltages below specified limit without baffle plate

  Specified limit to be subject of further study

- Susceptibility:

  Design module to withstand emissions from adjacent module at 10 dB above specified emissions limit without baffle plate

- Test

  Use high speed time domain Go/No-Go fixture

  Method to be subject of further study

Table 3.6-8. Specification and Test

WRM Type B

Time Domain Crosstalk Test

Emissions

Same as for Type A except test fixture employs baffle plate as for actual installation

Susceptibility

Design module to withstand same level as for type A with baffle inserted

Test

Use same test fixture as for type A - provide for baffle insert

Table 3.6-9. Specification and Test

WRM Type C - Use MIL-STD-461 Modified

Unit Test - Use MIL-STD-461 Modified

- Cannot use radiation test methods - rely on WRM test
- Cannot use conduction test methods - rely on WRM test
- Can use specific test methods such as front end rejection, transmitter spurious, etc.

Rack Test - Shielding effectiveness for 80 dB AT 200 MHz

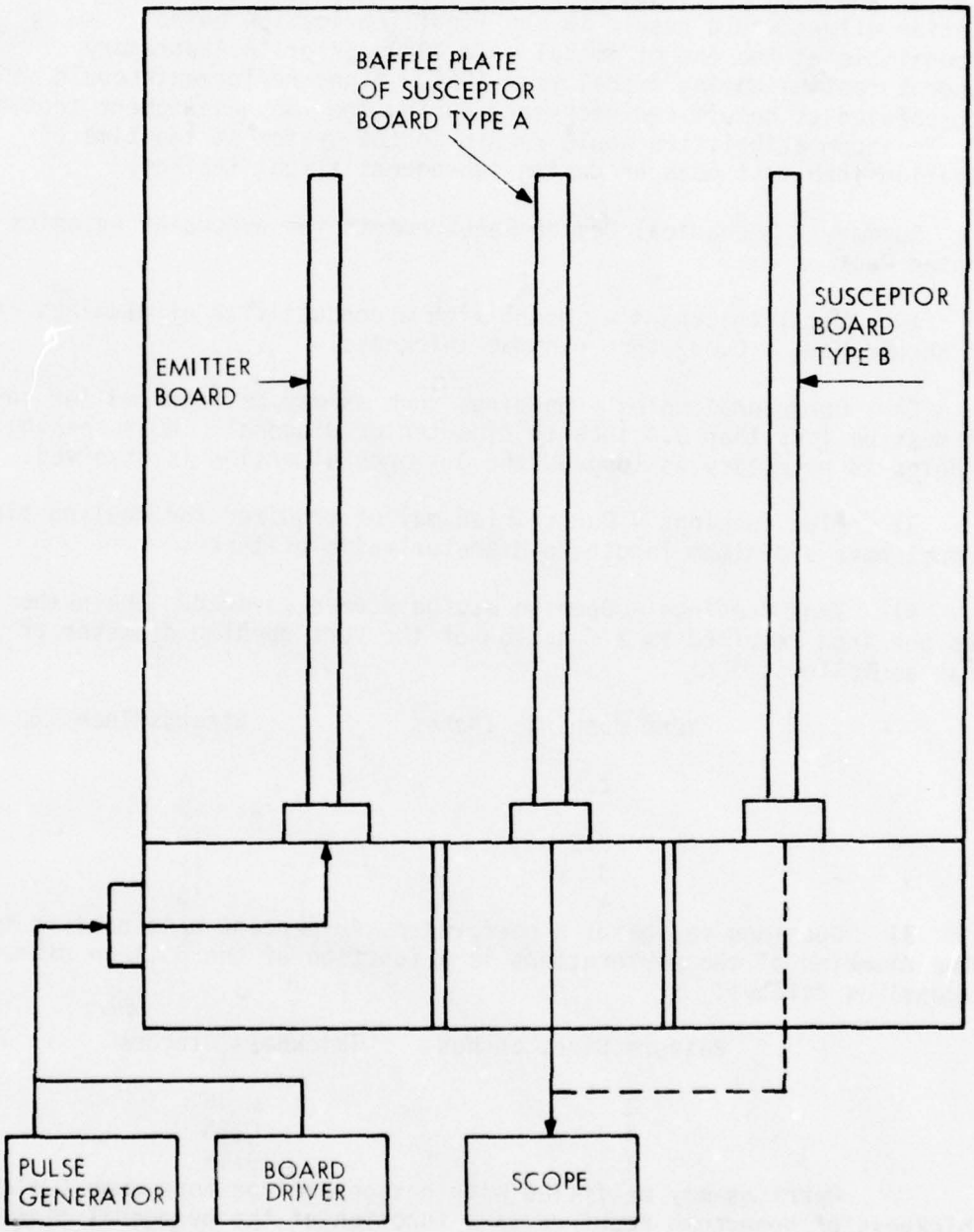


Figure 3.6-1. Crosstalk Test, Test Method Block Diagram

rack design phase, or near the end of fiscal year 1979. Outputs from the program could then be available during the integrated rack hardware fabrication and module evaluation phase. Feedback to the hardware fabrication effort would result in the final fabrication being self-compatible at the end of fiscal year 1980, prior to laboratory development testing during fiscal year 1981. Minor refinements could still be incorporated as determined necessary during the lab development testing phase. No incompatibilities would remain in the system at the time of installation into test beds or during subsequent flight testing.

3.6.5 Summary - Mechanical Design Requirements for a Modular Avionics Integrated Rack

1) Metal thickness - Metal with a conductivity of aluminum or copper should have a 0.032 inch minimum thickness.

2) Occasional holes - Openings such as may be required for corner relief must be less than 0.4 inch in diameter or diagonal. No screening over these holes is necessary as long as the 0.4 inch dimension is observed.

3) Pipe openings - Ducts which may be required for cooling air inlet must have a minimum length-to-diameter ratio of three.

4) Vent openings - Opening may be screen covered. The number of strands per inch required is a function of the vent opening diameter or diagonal as follows:

Vent Opening, Inches	Strands/Inch
1.5	4
2	6
2.5	10
3	12
4	16

3) Openings may be of a perforated, 40 percent open pattern type. Here the diameter of the perforations is a function of the pattern diameter or diagonal as follows:

Pattern Size, Inches	Thickness, Inches
2	0.35
3	0.25
4	0.15

Openings may be filled with hexagonal type honeycomb (welded). The thickness of honeycomb required is a function of the hexagonal diameter as follows:

Hex diameter, Inches	Thickness, Inches
1/8	3.8
1/4	3.4

5) Finish - Finish should be of conductive alodine, irridite oaklite, zinc chromate, etc. Do not anodize.

6) Overlap - Mating flanges should overlap by 0.5 inch minimum. If contact is by metal to metal surfaces without mesh gasketing, screw spacing should be 2 inches maximum. With the use of mesh gasketing, spacing of screws may be 6 inches. Twist lock, cam lock, or Dzus fasteners are not recommended. Flange stiffening at lap joints helps and is required for all metal thickness less than 0.060 inch.

7) Access Doors - Doors must include a bonding means such as finger stock or mesh gasket, including the hinged sides. Triple-point clamping should be provided on the un-hinged side.

Metals used for various assemblies must be compatible with the galvanic series to prevent corrosion from destroying the bonding effectiveness.

The requirements listed should ensure an EMI enclosure design which will provide 80 dB of shielding effectiveness from 10 KHz to 200 MHz and 40 dB at 1 GHz, which is adquate to meet V/STOL requirements, based on a study of its operating environment and integrated circuit electromagnetic susceptibility data.

3.7 Electrical Power Distribution and Regulation

3.7.1 Assumptions

For purposes of this study, the following elements were analyzed and evaluation as a total system concept:

1) Aircraft Electrical Subsystem - The 270 VDC SOSTEL System is assumed as a baseline. The improved quality of the power from this type of system greatly enhances the design of the avionics power supply modules and will minimize weight and volume as well as EMI-related hardware.

2) Avionics Power Supply Modules - The family of power supplies described in NAVORD drawing number AV21901 (Power Supply Modules, Standard Electronic Module (SEM) program, General Specifications for) were used as a baseline for this study.

3) Voltage and Ground Distribution Subsystem and Decoupling Networks - This is interrelated with the first two subsystems and cannot be designed independent of them.

The assumption was made that either of the aircraft's two generators would be capable of supplying 100% of power required, except for the AEW mission, where a degraded (non-simultaneous) mode of operation will be allowed, should there be a generator failure. The normal operating power of the AEW radar was assumed to be 70 KW, which would drop to 22 KW for non-simultaneous operation.

3.7.2 Aircraft Power Distribution and Control

Because of the extensive use of composite materials, the aircraft structure will not be used to return current to the generator or the regulation point of the 270 VDC system.

Power will be distributed to the integrated rack by a flat laminated bus, and will enter the rack enclosure (Figure 3.7-1) through an EMI filter box. The MAP back panel will be located near the filter box. This panel holds the load controllers and remote terminals. Normal wiring (twisted pairs) will connect the output of load controllers to the power supply modules.

3.7.3 Regulation

The subsystem or back-panel power requirements for Core avionics and AEW mission avionics are shown in Table 3.7-1 and 3.7-2, respectively. Note that (1) a very high percentage of the total power (96%) is at + 5 VDC and (2) the largest analog load is 12 watts. This division of power is a pleasant surprise, since it allows each back panel to be powered by a dedicated set of power supply modules without a large increase in the size, weight, or dissipation of the power-conditioning system. Earlier rough estimates indicated that 30 percent of the loads were analog, and that there

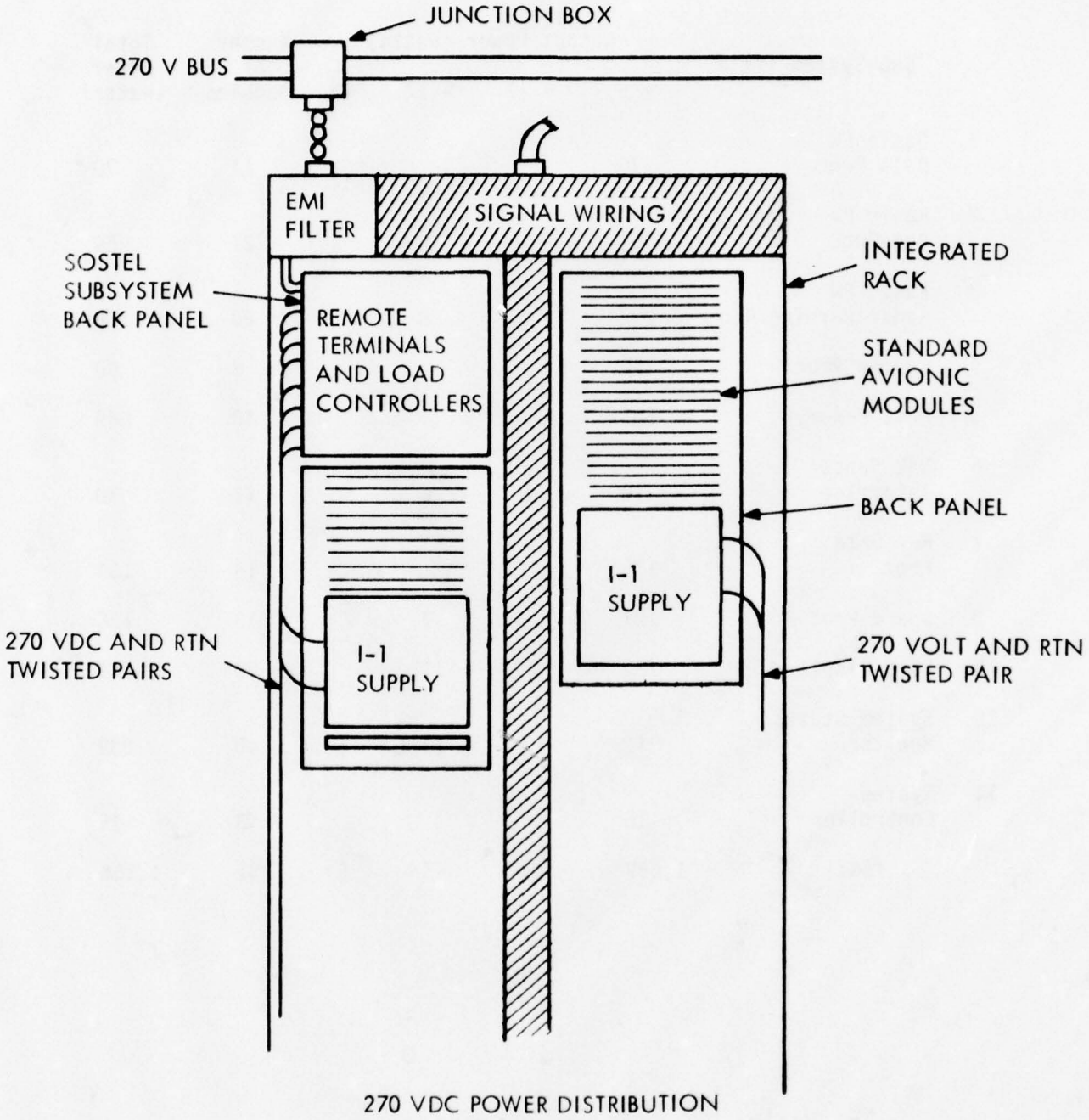


Figure 3.7-1. Integrated Rack, 270 VDC Power Distribution

Table 3.7-1. Core Avionic Subsystem

	Sub-System Title	Output Power (Watts)				Number of Modules	Total Power (Watts)
		+ 5	+ 12	- 12	V_X		
1	Basic EW Data Proc	70				11	70
2	Basic EW Pre-Proc	51		8		27	59
3	Basic EW Radar Warning Rec	292	8	8		60	308
4	Common Proc	60				8	60
5	Mass Memory	565				40	565
6	NAV Sensor Interface	19	5	6		11	30
7	NAV Data Proc	126				18	134
8	Spare Proc	127		9		13	136
9	Core Displays	132		11		20	143
10	System Status Monitor	212	12	10	5	40	239
11	System Controller	15				3	15
	Total	1,669	25	57	5	251	1,756

Table 3.7-2. AEW Mission Avionic Subsystem

	Sub-System Title	Output Power (Watts)			V^X	Number of Modules	Total Power (Watts)
		+ 5	+ 12	- 12			
1	AEW Radar Signal Proc (I)	485	5	6		34	496
2	AEW Radar Signal Proc (I)	485	5	6		34	496
3	AEW Radar Signal Proc (I)	485	5	6		34	496
4	AEW Radar Signal Proc (I)	485	5	6		34	496
5	AEW Radar Signal Proc (II)	538	12	12		33	562
6	AEW Radar Signal Proc (II)	538	12	12		33	562
7	AEW Radar Signal Proc (II)	538	12	12		33	562
8	AEW Radar Signal Proc (II)	538	12	12		33	562
9	AEW Radar Post Proc	186		3		30	289
10	AEW Intercept/ ATCE Track/Class	68		2		15	70
11	Multi-Sensor Proc	233		7		38	240
12	Threat Eval and Tactics	35				5	35
13	AEW Display	442	8	8		49	458
14	AEW Display Electronics	332		7		37	344
15	AEW Display Electronics 2	270		5		29	275
	Total	5,658	76	104		471	5,843

would be a much higher proliferation of voltages, making it difficult to be both efficient and lightweight without some centralization of the power conditioning system. It was further argued that efficiency of the power-conditioning system could not be traded off for weight without adding 24 lbs/KW (equipment and fuel penalty) for additional power generation and cooling.

Having a dedicated set of power supply modules for each subsystem minimizes the interaction of one subsystem with another, and increases flexibility, maintainability, and procurability. It also simplifies the subystem interface from a specification and wiring standpoint. It may also eliminate some of the load controllers, since the subsystem supplies can be turned on and off via logic command, allowing more subystem to share a load controller.

Table 3.7-3 lists the power supply module types described in AV21901. Table 3.7-4 lists the usage of each power supply module type. If we estimate the size and weight for the power supply modules, as shown in Table 3.7-5, the size and weight for the power supply modules is as shown in Table 3.7-6. Table 3.7-7 shows power supply weight and volume as a percent of total module (including power supply modules) weight and volume.

These percentages are roughly twice what is presently experienced in avionics equipment. The packaging and electrical efficiency of power supplies takes on much more significance in the 1980's that they have today.

Since supply voltages do not leave the back panel, the task of the power and ground distribution system is much easier. Ground and voltage planes can be used (Figure 3.7-2) to interconnect the supplies with their respective loads, completely eliminating wires from the distribution system. The tight coupling provided by the voltage and signal ground distribution planes (or strips) reduces the burden on the decoupling networks within the analog modules. In most cases, the quality of power made by the analog power supply modules will be adequate. Those modules that contain circuits highly sensitive to supply voltage variation and/or ripple should have series regulator chips internal to the module.

Cases are bound to occur where it would be desirable to use the excess capacity of a supply located on one back panel to provide a few watts of power to another location, thus reducing the number of power supplies. This option will still be available to the system designer, once compatibility has been established between (1) the modules that constitute the loads; (2) the power-distribution wiring; (3) the common power supplies. Some examples of incompatibility are:

1. The subsystem must be independently powered on and off.

2. The subsystem are redundant, and a common power supply failure would take out both subsystems.

Table 3.7-3. Primary Converters and DC to DC Converters (AV21901)

Type	Power Source	Output Voltage	Output Power
I-1	115/200 Vac 3Ø, 400 H_z	5/5.2 VDC	360 W
I-2	or 270 VDC	5/5.2 VDC	125 W
I-3	or 270 VDC	5/5.2 VDC	50 W
I-4	or 270 VDC	12/15 VDC	125 W
I-5	or 270 VDC	12/15 VDC	50 W
I-6	115/200 Vac 3Ø, 400 H_z	25/28 VDC	125 W
I-7	or 270 VDC	25/28 VDC	50 W
III-1	5 VDC	5 V	5 W
III-2	5 VDC	15 V	15 W
III-3	5 VDC	25 V	25 W

Table 3.7-4. Power Supply Usage By Type

Type	Core Avionics	AEW Mission Avionics	Total
I-1	7	22	29
I-2	4	2	6
I-3	1	-	1
I-4	-	-	-
I-5	-	-	-
I-6	-	-	-
I-7	-	-	-
III-1	-	1	1
III-2	8	22	30
III-3	-	-	-

Table 3.7-5. Projected Power Supply Module Size and Weight

Type	Output Power (Watts)	Weight (Lbs)	Size (IN^3)	Watts Per Lb	Watts Per IN^3	Eff %
I-1	360	3.0	60	120	6.0	80%
I-2	120	1.5	30	83	4.0	80%
I-3	50	1.0	20	50	2.5	80%
III-1	5	0.3	7 (Two Slots)	17	0.5	70%
III-2	15	.4	7 (Two Slots)	37	1.5	70%

Table 3.7-6. Power Supply Weight and Volume Comparison

	P.S. Modules		Circuit Modules (I-2A)	
	Weight	Volume	Weight	Volume
Core	31 Lbs.	616 IN^3	63 Lbs.	885 IN^3
AEW Mission	78 Lbs.	1541 IN^3	118 Lbs.	1590 IN^3

Assumes: Circuit Module Weight = 0.25 Lbs.
Excludes SOSTEL Modules

Table 3.7-7. Power Supply Weight and Volume Comparison

	Power Supply Module As A Percent Of Total Module Wt. and Vol.	
	Size	Weight
Core	41%	33%
AEW Mission	49%	40%

Assumes: Circuit Module Wt = 0.25 Lbs.
Excludes SOSTEL Modules

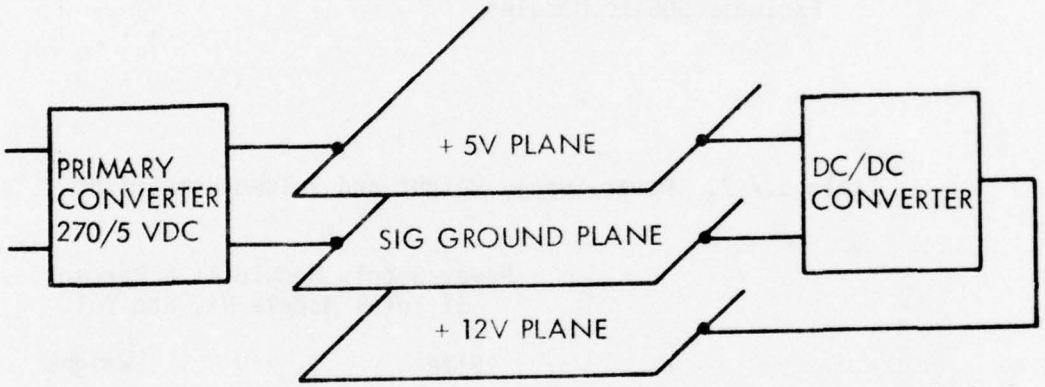


Figure 3.7-2. Back Panel Signal Ground and Voltage Distribution Diagram

3. One subsystem has a high transient load (e.g., lamps) which produce undershoots on the supply voltage greater than can be tolerated by the other subsystem.

3.7.4 MAP Recommendations

1) The SEM power supply modules described in AV21901 should be compatible with the MAP integrated rack.

2) Based on the present estimates for Core avionics and AEW mission avionics, the primary and secondary converter families shown in Table 3.7-8 (as opposed to those in AV21901) would reduce the weight, volume, and population to the levels and percentages shown in Tables 3.7-9, 3.7-10 and 3.7-11. The number of primary converter types is also reduced from seven to five. A dual converter is one that regulates on a sense winding and makes two floating outputs. The outputs can be connected in parallel to provide 100 watts at either +Eo or -E0, or in series-aiding to provide 100 watts at either +2Eo or -2Eo, or to provide 50W at +E0 and 50 watts at -Eo. The tolerance on the output voltages of a dual supply depend on the load range, and for most applications will vary between 3 and 7 percent.

3) The weight and volume of the Core and AEW mission power supply modules were based on the projected (1985) estimates shown in Table 3.7-5, which reflect less than a 2:1 improvement over what is commonly achieved today. The resources being spent on component performance, packaging, and circuit techniques for improvements to avionic power supplies too low to warrant a more optimistic projection. The major contributors to improved power supply performance are:

A1. Power Semiconductors

Progress in power transistors and rectifiers has been good, and should continue from an electrical performane, reliability, and cost standpoint. Fortunately, device technology, and requirements for military and commercial applications coincide to a large degree. Military and commercial requirements differ more in the area of device packaging. TO-3 and DO-5 cases are inefficient from a size and weight standpoint. Power hybrid techniques should be used to reduce the size and weight of the MAP supplies. Funding is essential in this area.

A2. Capacitors

In a 360N 270/5V converter, 20 percent of the component weight and volume consists of capacitors. The only high CV product capacitor which maintains a low impedance at -55°C is the solid tantalum. Over the past 20 years, solid tantalum capacitors have improved in CV product and ESR (equivalent series resistance) by only about 50 percent. Commercial supplies that do not have to operate at cold temperatures use aluminum electrolytic capacitors. An increasing demand for low voltage, high current power supplies for the computer industry resulted in commercial application of switching-type power supplies. This in turn resulted in improvements in

Table 3.7-8. Standard Power Supply Modules

Primary Converters

Type	Input Power	Output Voltage	Output Power
P-1	270 VDC	5 V	360 W
P-2	270 VDC	5 V	225 W
P-3	270 VDC	5/5.2 V	125 W
P-4	270 VDC	5/5.2 V	50 W
P-5	270 VDC	15 V Dual	100 W

Secondary Converters

Type	Input Power	Output Voltage	Output Power
S-1	+5 V	-5 V	20 W
S-2	+5 V	12 V Dual	30 W
S-3	+5 V	15 V Dual	30 W

Table 3.7-9. Core and AEW Mission Power Supply Module Comparison

	P.S. Modules		Circuit Modules (I-2A)	
	Weight	Volume	Weight	Volume
Core	27 Lbs.	526 IN^3	63 Lbs.	885 IN^3
	(31 Lbs.)	(616 IN^3)		
AEW Mission	66 Lbs. (81 Lbs.)	1303 IN^3 (1541 IN^3)	118 Lbs.	1590 IN^3

Quantities in parentheses are for AV21901 power supply family.

Table 3.7-10. Core AEW Mission Power Supply Modules vs Total Module Weight Size

	Power Supply Module In Percent Of Total Module Weight and Size	
	Size	Weight
Core	37% (41%)	31% (33%)
AEW Mission	45% (49%)	35% (40%)

Quantities in parenthesis are for AV21901 power supply family.

Table 3.7-11. Power Supply Usage

Type	Core Avionics	AEW Mission Avionics	Total
P-1	3	12	15
P-2	4	9	13
P-3	3	2	5
P-4	1	1	2
P-5	-	-	-
S-1	1	-	1
S-2	7	14	21
S-3	-	-	-

ripple current capacity, and the ESR (including cold temperatures) of aluminum electrolytic capacitors. This improved technology has not been applied to the MIL-type capacitors in M39018/1. If it were, a 200 to 300 percent improvement could be achieved in ripple current and ESR over what is presently specified in M39018/1. Some funding would probably be necessary to incorporate this improved technology into a MIL-type series.

A3. Magnetics - Low Loss

High-frequency ferrites have important commercial applications, and several companies are active in the development of this product. By 1985, ferrite material exhibiting a loss of only 0.3 W/Cm^3, operating at 3500 gauss, 40 kHz should be commercially available. This increase in flux density and operating frequency would halve the size and weight (compared to present day designs) of the magnetic components. The increase in frequency would also allow a reduction in the size and weight of filter capacitors. Whether or not amorphous alloys will be useful (such as in the case of high current output filter chokes) in 1985 avionic power supply designs is unclear: their development should be followed.

A4. Packaging

Custom integrated circuits (thick-film and thin-film) would significantly reduce the size and weight of the MAP supplies, especially the secondary converters. Monolithic circuits presently available from General Instruments (SG-152U) and Ferranti Semiconductors (ZN1066E) contain much of the control circuitry used in push-pull type converters. Unfortunately, push-pull type converters (center tapped primary or bridge) are not the most effective circuit configuration for the higher power primary converters. However, they may find application in secondary converters. A medium scale custom monolithic control circuit would improve the reliability, and lower the size, weight and production cost of the primary converters. Once the power supply circuits have been established, funds should be available to integrate those areas of the design, where improvements in size, weight, cost, and reliability could be achieved through the application of thick-film, thin-film, or monolithic-integrated circuits techniques.

4) Series regulator modules (Group IV of AV21901) should be dropped. Monolithic regulator chips are small (0.200 inch x 0.200 inch), inexpensive (approximately $5) and reliable. Modules with critical supply voltage requirements should have IC regulators internal to the module, and in close proximity to the critical circuit.

5) Primary converters should not be required to operate from three-phase, 400 Hz power. If 270 VDC is not available, rectification of AC power should be performed external to the MAP supplies. Transient suppressors should be used to limit spikes and voltage surges on the 270 VDC (or rectified three-phase, 400 Hz) bus to 350V. Using present day metal-oxide varistor (MOV) technology, a 250 ampere, 350V, 25 msec (maximum length of MIL-STD-709B surge) surge suppressor would have a volume of about 100 cu. inches. There is a large commercial application for MOV's (protecting household appliances from power line, lightning strikes up to 100,000

amperes) and advances in MOV technology will surely proceed without government funding. However, some funding for device packaging may be desirable. Limiting voltage surges to 350 volts will have a beneficial effect on the size, weight, and reliability on all of the primary converters.

6) Since primary converters can be turned on and off electronically, it may be possible in many cases to replace load controllers with fusible links. A fuse resistor, normally sized to conduct the 270 VDC current required by a 360W 270V/5V converter, could be cleared with a relatively small amount of energy, and not result in a transient that would cause other primary converters to go out of regulation.

3.8 Airframe Considerations

3.8.1 Structure Design

Design of the integrated rack will be based on expected shock and vibration inputs developed by the aircraft. Numerical input values will be specified depending on location within the airplane, in the form of the MIL-STD-810C specification. The major vibration requirement will be broad-band (5-2000 Hz) random vibration, at moderately high level. The shock requirements will be 20G operational and 40G crash safety sawtooth shock pulses of 11 millisecond duration. The basic random vibration levels in the fuselage are expected to have spectral densities of about $0.02g^2/Hz$, with values as high as $0.30g^2/Hz$ in the extreme aft end of the fuselage. These values apply between 300 Hz and 1000 Hz, with lower values resulting from a 6 db/octave roll-off below 300 Hz and 6 db/octave roll-off above 1000 Hz. Installation of equipment will reduce these values considerably at equipment resonances because of the high mechanical impedance presented by the equipment. This is recognized and partially accounted for by the weight-reduction factor permitted by MIL-STD-810 for heavy equipment. Since the MAP weights about 120 lbs., the applicable reference spectral density level in the center fuselage area will be about $0.013g^2/Hz$, resulting in an overall design vibration level of about 4 g rms.

3.8.1.1 Geometric Considerations

The basic shape of the integrated rack is a shallow rectangular box. Installed, it will be subject to loading in the three orthogonal aircraft directions. Because of the dimensions of the rack (approximately 4 in. x 22 in. x 64 in.) it becomes advantageous to devise supports in directions perpendicular to the long dimension. The support should permit the structure to act as a column when loaded in the length direction, and as a simply-supported beam in either direction perpendicular to the length. With the mass of the complete rack about 150 pounds, it is not difficult to design the load-carrying members to carry the loads as columns and beams. The areas of the rack with good load-carrying abilities are the side panels or plenums, the central module support structure, and the rear enclosure panel. When they are properly joined, the beam-column cross-section effectively becomes a channel or a form of I-beam which has good load carrying abilities.

Figure 3.8-1 is a structural schematic which is intended to show the primary load-carrying members and their interrelationship. Basically the structure is a 4-inch deep channel, 22.6 inches wide. The two shelves and the central column serve primarily, in a structural sense, to deliver internal loads to the channel. If it is supported at the base and loaded parallel to its long axis (direction A), it will react as a column, and the resonant frequency will be relatively high. If it is supported at top and bottom, against loads in the 22.6-inch direction (direction B), it will react in the manner of a simply-supported, uniformly-loaded beam, with the cross-section of a channel. The bending resonant frequency will be relatively high, but a torsional motion will be introduced because the center of gravity of the load is not properly positioned with respect to the back

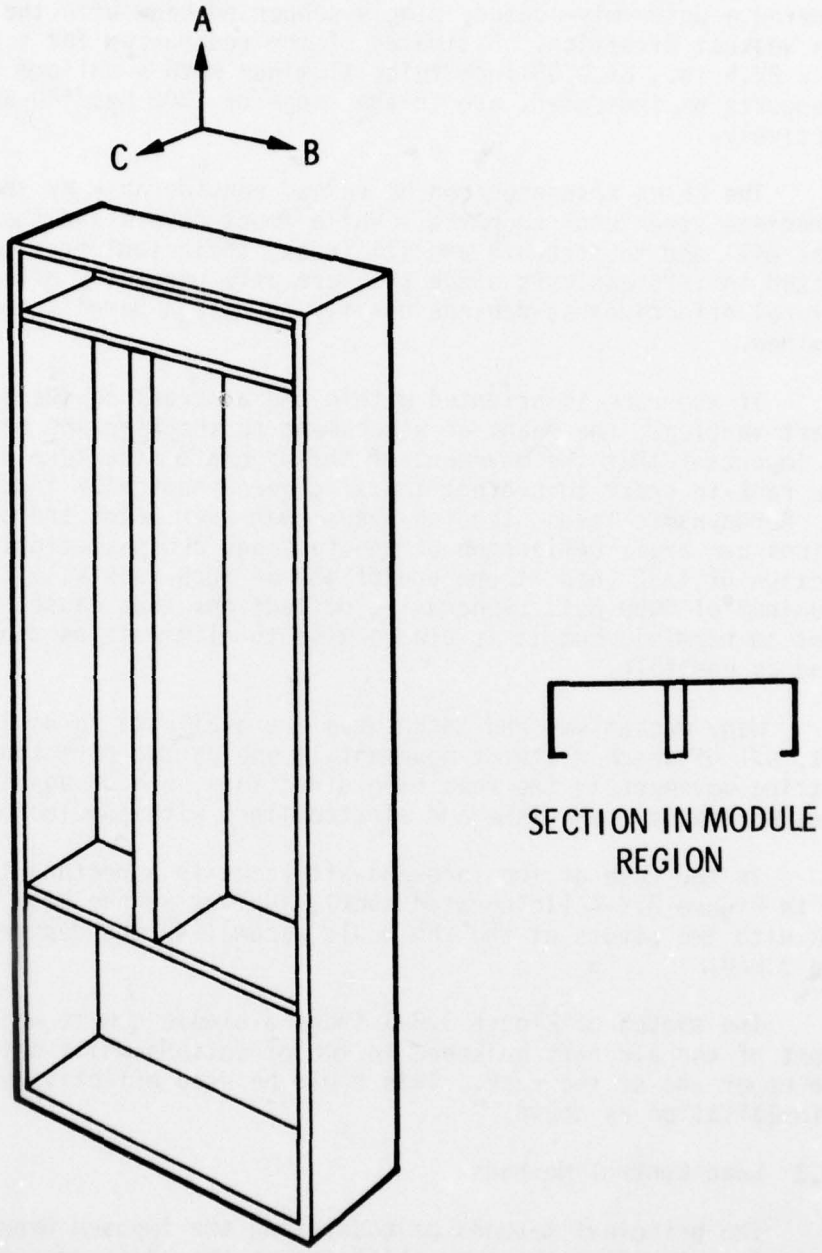


FIGURE C. STRUCTURAL SCHEMATIC

Figure 3.8-1. Integrated Rack, Structural Schematic

panel. The lowest resonant frequency, and the one of primary importance in the design, is the mode in which the rack bends in the direction of its smallest dimension (direction C). If the ends are supported, the beam can be considered a uniformly-loaded, simply-supported beam with the channel bending in its weakest direction. Estimates of the resonances for a channel section 4 in. x 22.6 in., of 0.06-inch thick aluminum with a uniform load of 150 lb., and supports as indicated, are in the range of 1300 Hz, 170 Hz and 25 Hz respectively.

The 25 Hz resonance can be raised considerably by the use of intermediate structural supports. While front covers and the installation of modules will add to strength and stiffness, their influence has been neglected in this analysis since they are only partially effective, and their structural effectiveness depends heavily on design details not yet determined.

If the rack is oriented within the aircraft so the long dimension is aircraft vertical, the means of attachment to the airplane become important. It is important that the movement of the aircraft structure not be impaired by the rack in order to prevent imposing aerodynamically induced loads on the rack. Aerodynamic loads, landing loads, maneuver loads and other airplane reactions can cause deflection of the fuselage cross-section. An axial deflection of 1/32 inch at one end of the 64-inch rack will induce a stress in aluminum of 5000 psi. Generally, deflections that cause bending stresses are not so harmful, but it is always wise to eliminate as many sources of loading as possible.

Many mechanisms and techniques are available to achieve the desired result, all of which restrict movement in one or two directions while permitting movement in the remaining directions, e.g. drag-links, flex-plates, kinematic mechanisms and slotted links with shoulder bolts.

In the case of the fore-and-aft racks in a rectangular fuselage shown in Figure 3.4-4 (Integrated Rack), a pivot at the base of the rack and a link with two pivots at the top would accomplish the desired result. See Figure 3.8-2.

The sketch of Figure 3.8-3 shows a simple scheme which allows movement of the aircraft bulkhead in two directions while maintaining support at the upper end of the rack. This could be used effectively with a pier rack installation as shown.

3.8.1.2 Load Control Methods

The principal methods of moderating the imposed dynamic loads consist of controlling the rack stiffness so the basic resonant frequencies are high, or of controlling the rack damping to reduce the resonant amplification factor. Either approach results in relatively small excursions and, hence, low stresses. Of the vibration modes considered in 3.8.1.1, the resonance which results in bending of the structure in the thin direction is the only one of concern.

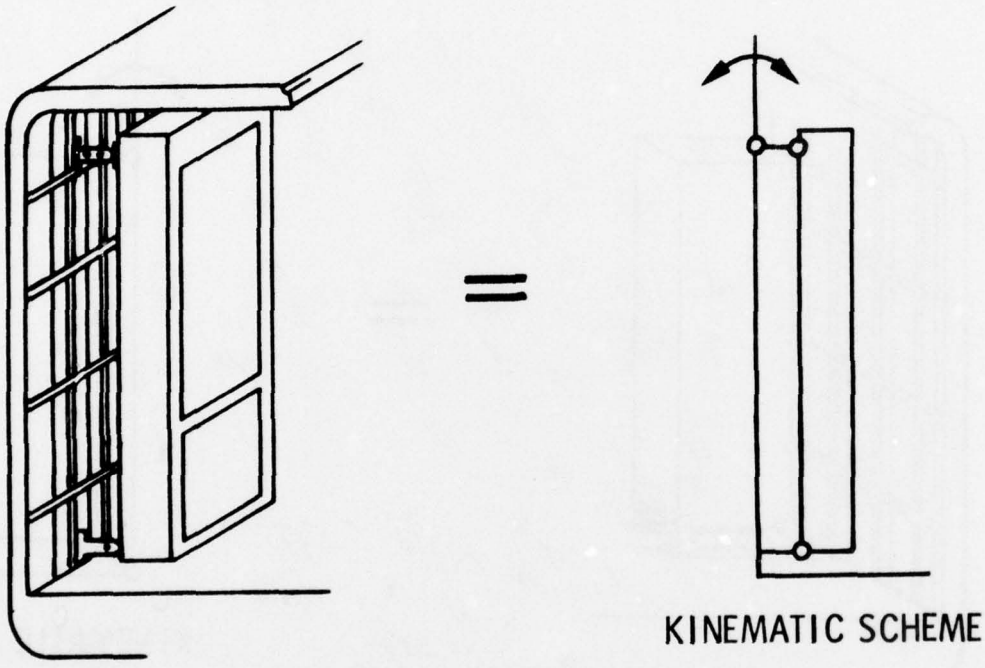


Figure 3.8-2. Mounting Scheme for Fore-and-Aft Racks in a Rectangular Fuselage

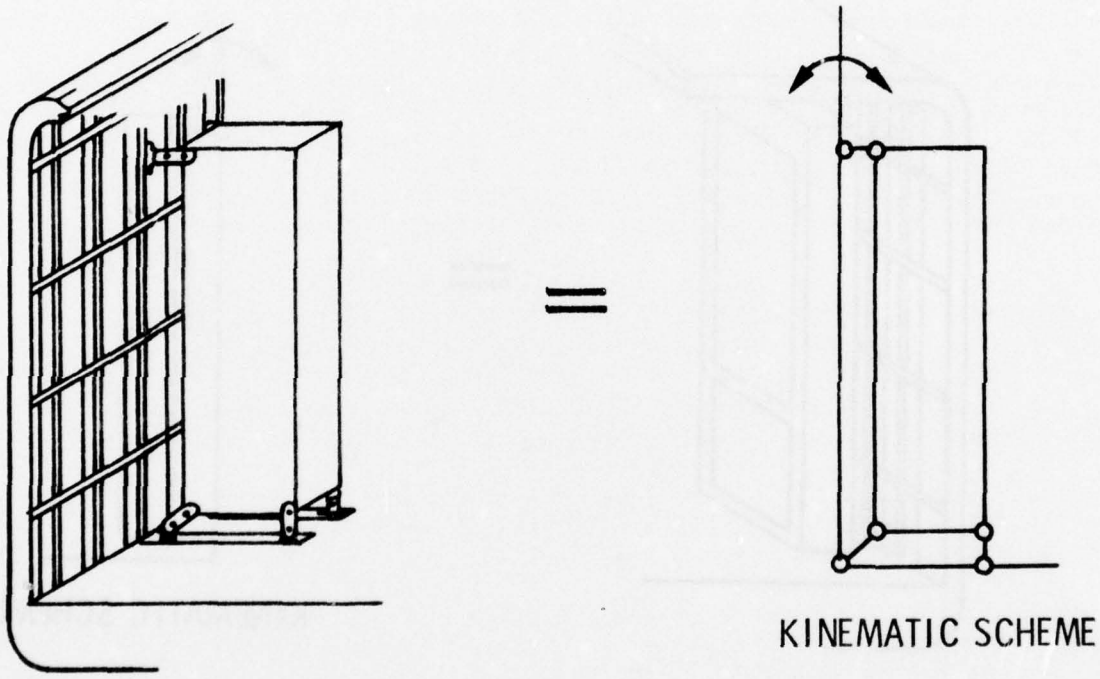


Figure 3.8-3. Mounting Scheme for Pier Racks in a Rectangular Fuselage

The reduction in displacement amplitude should result in the lightest structure. In designing for a broad-band random vibration environment, there are no definite frequency criteria because the input consists of all frequencies in nearly equal amounts. The shock environment, with 11 millisecond duration pulse, implies that lower dynamic loads result if the lowest mode resonance is not near 45 Hz.

3.8.1.3 Rack Construction

The design approach to be pursued will be to size the load-carrying structure to withstand the crash-safety shock pulse. The shock input does not become amplified if the natural frequency of the rack is outside the frequency range 35 to 110 Hz. The frequency analysis of the resulting structure must verify this assumption, but preliminary calculations satisfy the requirement.

Design of the rack will be based on prevention of permanent deformations and malperformance under the 20 g shock load and calculated vibration peak response loads which might exceed the response to a 20 g shock. Design will also provide for no ultimate failures of the structure (buckling or fracture) under the 40 g crash-safety shock load. The crash-safety condition is likely to be the ruling factor in most of the design, especially for attachment hardware and fittings.

Continuing the analysis begun in paragraph 3.8.1.1 of the much simplified channel leads to a maximum bending stress of about 75,000 psi. Better modeling of the load distribution and of the structure itself would cause reduction of the calculated stress. The short legs of the channel (the side panels of the rack) contribute most to strength and stiffness in this direction and their detailed design will determine the rack structural performance. Chief among the factors to be considered in designing the side panels is the choice of material. There are many possible candidates.

The following table lists some of the important properties of materials which might be considered:

	W, lb/in.^{3}	E, psi	F_{tu}, ksi
Aluminum alloy	0.1	10×10^6	75
Titanium alloy	0.16	18×10^6	130
Magnesium alloy	0.07	6×10^6	35
Kevlar epoxy composite	0.05	11×10^6	200
Graphite epoxy composite	0.055	19×10^6	180

Because minimum weight is one of the major goals, it appears that one of the composite materials would be most satisfactory. What the table does not show, however, is that the tensile strength normal to the lay-up of

the laminar forming the composite is very low (4,000 to 6,000 psi) and the compressive strength is about 20,000 psi in the same direction. Unless the loads acting on the member can be kept essentially uniaxial, with only small loads perpendicular to the lay up direction, the effective strength is less than for metals which do not exhibit such directional properties. In the application to the side panels, the major loads are suitably applied, but at all points of attachment to the panel the thickness must be increased to prevent local failure. Because of the many locations at which attachments must be made, the end result may be no significant weight saving at all. This possible weight saving is further negated by the requirement for EMI that there be a 0.032 inch thick aluminum or copper skin.

A composite material technique which might prove useful is the use of a layered construction of panels where aluminum sheets are bonded together with a damping material. When such a sheet is loaded so one sheet tries to slide with respect to another, a relatively large damping force is generated to oppose dynamic motion. Because of the limited depth of the side panels (only 4 inches) the use of such panels may not contribute sufficient damping to justify the slight weight increase. Another damping technique which might be useful is that introduced by B. Patel which uses platelets and damping material in a particularly effective arrangement which can be attached easily to a structure.

Forming techniques for the side panels, which depend on the final details, may help to determine the material selection. The super plastic forming of titanium alloys as reported by North American Aviation could perhaps be more satisfactory than those formed by other fabricating processes.

Consideration of the facts above leads to the initial conclusion that the best construction method would employ aluminum alloy side panels. The detail design configuration can only emerge when a clearer picture of the interior requirements is obtained. As the rack design progresses, the structural variations will be examined in detail by using stress and dynamic analysis computer programs similar in abilities to NASTRAN. This kind of analysis permits evaluation in any desired detail of the stresses, and provides a good model picture of response to vibration.

3.8.1.4 Internal Details

Many internal details necessary to successful performance of the rack must be resolved. Primary among these are the establishment of adequate load paths, so that inertia loading due to each subassembly may be delivered to the nearest rack attachment point. The central cooling-air duct will serve adequately to delivery the module loads to the rear panel for vertical loading, and to the two shelves for loading in the horizontal directions. The shelves, in turn, put load into the rear panel or into the side panels, depending upon loading direction. The side air ducts will be used to delivery module loads in all directions directly to the side and rear panels, and in some construction methods, may contribute to overall stiffness. Air flow openings and cabling runs often interfere with structural load paths. In

addition, module hold-down features need to be resolved. Retention of the modules and the use of connectors for the modules require resolution, to be sure of adequate load path for insertion forces as well as for dynamic forces exist. The resonant frequency for a module is expected to be about 450 Hz for plate type vibration.

3.8.2 Vulnerability of Modular-Racked Avionics to Gunfire

Alternative MAP concepts were assessed from the following three points of view:

1) Minimization of the size of avionics elements, separation and distribution of the elements throughout the aircraft to reduce the probability of avionics being hit by gunfire.

2) Selection of architecture, packaging, armor, and other techniques such that sustained damage to sections of the avionics does not result in extensive degradation to the whole avionics system this includes consideration of vulnerability of functions such as cooling and power systems as single point failure modes.

3) System redundancy features that will restore critical subsystem operation if projectile damage occurs.

The primary consideration is to reduce the likehood of aircraft loss due to gunfire-induced avionics failures. The loss of mission avionics functions not critical to flight, is secondary.

In general, damage to mission avionics will not result in aircraft loss, but damage to flight-critical functions such as electronic flight controls and propulsion control can cause loss. Flight critical functions must be protected by redundancy and distribution throughout the aircraft. System pervasive functions such as cooling and power distribution subsystems must be designed such that damage to non-flight critical avionics does not cause faults in the flight-critical subsystems through these pervasive functions.

Also, avionics sensors, processors and controllers where damage may abort or significantly degrade mission accomplishment must be designed and installed to minimize subsystem degradation from single fragment/projectile path damage.

While V/STOL avionics and installation have not yet been specifically defined, attention now to certain parameters will minimize the likelihood of major or total loss of avionics. Vulnerability analysis, in accordance with the techniques discussed in JTCG/AS-75-V-008, Dec. 1976, is premature, but one can make basic assumptions on major single projectile/fragment paths. According to this document, damage paths from air-to-air gunnery attacks will generally fall within a 30° cone about the aircraft longitudinal axis. Air-to-air and surface-to-air fragment damage paths, therefore, can envelop virtually the entire avionics system.

3.8.2.1 Partitioning, Physical Separation, and Distribution

Physical separation of elements to reduce the probability of a single projectile damaging essential controls therefore, should be a design goal. This goal drives avionics design to a spatially-distributed system. Use of a single integrated rack is not attractive from this point of view. Use of several integrated racks can reduce the vulnerability to gunfire and provide the weight and standardization advantages of modular integrated rack avionics. These racks should be distributed on each side of the aircraft, with redundant elements separated. In addition, providing vertical separation of critical independent elements will also limit single projectile cumulative damage effects.

In later MAP development phases, avionics installation concepts in projected aircraft designs can be evaluated using the projective path analysis identified in JTCG/AS-75-V-008 and system separation and redundancy requirements can be firmly identified.

Since the primary intended application for this design concept is V/STOL, use of armor plate (ceramic or other) was not considered because of the weight penalties incurred.

3.8.2.2 Vulnerability to Single Point Failures

A1. Cooling Systems

The number of preferred cooling systems concepts are quickly reduced when battle damage vulnerability is considered (Ref: Proposal for Modular Avionics Packaging Concept Study and Report, AESD, July 1977). The use of two-phase avionics cooling systems are immediately given low ratings in terms of vulnerability, because these systems must be sealed to contain the working fluid. Further, two-phase systems require pressure pumping, plumbing, and heat exchangers.

Air cooling concepts are much less vulnerable. Since these systems operate at low pressure and relative large volume ductwork, a single or even several projectiles, anywhere in the flow network, result in only a modest loss in cooling capacity. In the event of a significant cooling capacity loss, the equipment should still be capable of operating for a period of time at high component temperatures. Continued operation at higher temperatures will reduce equipment reliability; however, in a combat situation, the problem is not reliability, but successful accomplishment of the assigned mission, or capability to perform the mission until relieved by another aircraft.

It is recommended from a vulnerability standpoint that the "air cooled" systems be further analyzed to determine the best techniques. Any

candidate cooling system should be chosen with high priority assigned to relatively low battle damage cooling losses and weight penalties.

Since cooling capacity must be adequate to satisfy the most severe ambient conditions to be encountered, while at the same time minimizing weight requirements and system vulnerability and since adequate air mass flow can be obtained at relatively low pressure with required temperature differentials, it should be the primary avionics cooling media.

A2. Power Systems

The power conditioning systems assumed for MAP incorporate protective techniques for single point failures. If a component fails in the power conditioning equipment, and an over-voltage occurs, the over-voltage is sensed and the power supply is automatically shut off. No provisions are made for major projectile damage to many circuits. The vulnerability aspect of power system design should be considered in more detail in follow-on MAP development phases. The following general principles should be followed:

1) Redundancy of power generation and distribution system should be maintained.

2) SOSTEL should incorporate protective circuitry to shut down damaged branches automatically.

3) Protective circuitry for rack power should be provided so that damage within a rack will not get transmitted into the system.

4) Additional protective circuitry should be incorporated to minimize the impact of power supply damage on one back panel to the avionics on another back panel.

3.8.2.3 Redundancy Features

Because of vulnerability considerations flight control avionics has not been included as part of the rackable avionics. It is highly redundant and distributed throughout the aircraft. Other Core avionics which contain elements related to flight safety are packaged in redundant, separated racks. Mission avionics is conceived as packaged in several separate integrated racks in the equipment bay. Mission avionics for ASW and SEW missions, while having redundancy features, are not thought to require extensive provisions for gunfire protection because they will operate in more benign environments. Therefore, a great deal of effort to separate redundant elements of these mission avionics is not necessary. Core avionics elements, however, must exhibit a higher degree of redundancy and separation.

3.8.2.4 Summary

Table 3.8-1 summarizes the vulnerability of major avionics elements considered during the MAP study, in terms of vulnerability to gunfire.

Table 3.8-1. MAP Vulnerability Summary

MAP Concepts	Size, Separation and Distribution	Vulnerability to Single Point Failures	Redundancy	Comment
Partitioning				
Distributed system assumed	Partitioned into minimum size modules with flexibility. Separate and distribute subsystems throughout aircraft	Independence between functions a key goal for distributed system	Capability for redundancy is inherent in distributed system	System reliability with redundant feature require analysis
Rack Concepts				
Core avionics separate from mission avionics in multiple racks in cockpit area	Two or more small rack assemblies with physical separation		Redundant Core elements in physically separate racks	
Mission avionics in multiple racks in avionics bay	Rack sizes large for severe environment	Any damaged module can take out total back panel assembly. Good isolation between racks	Redundant elements not in separate racks	AEW & ASW mission avionics are not expected to be subjected to gunfire

Table 3.8-1. MAP Vulnerability Summary (Continued)

MAP Concepts	Size, Separation and Distribution	Vulnerability to Single Point Failures	Redundancy	Comment
Flight control not included in rack considerations	Small redundant elements distributed throughout aircraft	Independent from other avionics	High level of redundancy	
Module Concepts	Size and distribution for module alternatives considered are essentially the same in terms of vulnerability	Liquid cooled alternative not attractive Other alternatives roughly equal	All alternatives equally suitable	
Cooling Concepts	All systems have liquid distribution to racks	Liquid cooling concepts highly vulnerable	Requires complex approach	Techniques to reduce vulnerability of liquid systems are possible
	Direct air-inpingment has separate blowers in each rack	Direct air inpingment concept relatively good		
Power Conditioning	Power conditioners dedicated to back panel assemblies provides good separation and small-sized module	Power conditions have single failure protective good isolation between racks, moderate solution between back panels	A high level of redundancy is possible in power distribution system	This area is very amenable to improvements in SOSTEL protective circuits in each rack, protective circuits in each back panel and in redundant distribution paths

In following MAP developments, the V/STOL avionics system should be subjected to standardized aircraft vulnerability assessment methodology. Where the resultant vulnerability appears to be too high, further rearrangement should be analyzed to determine if such redistribution can provide reduced vulnerability.

3.8.3 Environmental Control System (ECS)

3.8.3.1 Introduction: The V/STOL Environmental Control Problem

The power dissipated by the AEW radar is estimated to be 59KW for the AEW version. The ECS must dispose of a large part of this heat load both in the air and on the ground when the engines are not running. It has been estimated that the ground operating time of major portions of the radar, for purposes of check-out and maintenance, will approach the air operating time.

The ECS system must also provide the usual pressurization and air conditioning of crew/passenger quarters.

The ECS will pump heat to the external ambient air, and possibly to the aircraft's fuel, during flight. See discussion in this report on using fuel as a heat sink.

3.8.3.2 Discussion

A1. Basic ECS: A Survey

GE/AESD talked with the following ECS manufacturers during the course of this study. All were extremely open and helpful.

Airesearch Mfg.

Hamilton Standard

Fairchild Stratus

The Rovac Corp.

Sundstrand Corp.

The basic ECS which must be examined for V/STOL are:

1. Air-cycle systems, particularly open cycle, using an expansion turbine as refrigerator.

2. Air-cycle positive displacement compression and expansion, "ROVAC", cycle

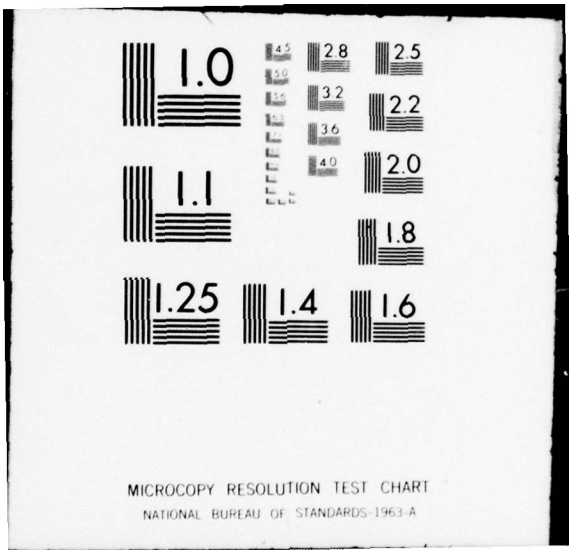
3. Freon vapor-compression cycle

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4. Simple cooling loop to ambient air and/or to fuel, with no refrigeration

5. Combinations of the above.

3.8.3.3 Discussion of Attributes of Basic Environmental Control Systems

A1. Aircycle System Attributes

1) Lightest weight of all the systems

The above statement is true if the weight of the prime compressor is not accounted for. Since for V/STOL, on-ground operation of ECS for check-out and maintenance is required, the weight of an electric motor, compressor and gear box, or that of an APU must be included. With such an inclusion, the aircycle system weight relative to ROVAC or vapor-compression systems is more nearly equal.

2) Can be used to provide direct pressurization of crew quarters.

3) Much experience with this system on military aircraft; highly reliable.

4) Open-cycle operation would appear to be advantageous due to availability of ram air at low stagnation temperatures because of subsonic speeds of V/STOL.

5) Bootstrap cycle would increase C.O.P.

6) Electric motor-driven compressor allows more efficient control than that realized with engine-driven compressor, where engine speed is not a function of ECS loading. Variable speed dc motors allow control of ECS to match loads.

7) An air-cycle, either turbine expanded or ROVAC, produces cold air which is more difficult to couple efficiently to a closed-liquid distribution loop than condensing Freon because of lower heat transfer coefficients.

8) Ram-air driven configuration for in-flight use allows for easy by-pass when outside ambient is low enough to provide direct cooling without refrigeration.

9) Use of a separate air cycle ECS for in-flight cabin pressurization/cooling a possibility, with vapor-compression system providing on-ground ECS functions and in-flight electronic cooling, when required.

10) C.O.P of air cycle turbine expander much lower than vapor-compression cycle and possibly lower than ROVAC cycle. C.O.P. is important for heavy cooling loads such as AEW radar system (estimated at 59KW).

*11) Heating and cooling available from a single unit.

*12) The refrigerant (air) unaffected by temperature extremes.

*13) Leakage not critical.

*14) Can be integrated with entire aircraft pneumatic system.

A2. Vapor-Compression Cycle Attributes

1) Easily the highest C.O.P., i.e., cooling per power expended by refrigerator. The C.O.P. of a Freon vapor-compression system is typically several times that of an air cycle (2 X to 6 X) or that of a ROVAC system.

2) Ideally suited for ground/ship board operation - needs only electrical power or mechanical drive from APU; no ram, etc.

3) Can be matched to liquid distribution loop using very compact (small-light) heat exchanger due to high boiling film coefficients of Freon, and high forced convection heat-transfer coefficients of liquid coolants.

4) Compressors are compact compared with air compressors due to higher working fluid density as well as lower required mass rate of working fluid flow. No gearbox required.

5) Much data on reliability - highly developed hardware.

6) Can operate after losing considerable Freon, but leakage of air into system shuts off refrigerating process. The running of Freon lines to integrated racks remote from ECS offers serious reliability/vulnerability drawbacks. A closed-loop liquid distribution system is considerably less vulnerable to small leaks, and would allow continued central ECS operation after damage to single distribution line. A separate closed-liquid-loop also would allow removal of the ECS from the aircraft as an operable system for maintanance replacement.

7) Adaptable to direct cold coil dehumidification of equipment cooling air within racks or cabin air. (Dehumidification - not just water separation).

A3. "ROVAC" Positive Displacement Compressor-Expander

General Electric found it difficult to assess just where "ROVAC" fits into the ECS picture. The refrigerator appears to be based on sound thermodynamic principles, but suffers from mechanical complexity with

*Points 11 through 14 above were taken directly from a Garrett-Airesearch document titled "Environmental Control Systems Military Specifications", S-99303.

cam-following sliding vanes which introduce the problems of energy losses and wear due to friction. The need to lubricate this mechanism will probably preclude the production of oil-free refrigerated air without using a heat exchanger and blower in a separate loop. The potential reliability and maintainability problems associated with this mechanically complex approach may be inconsistent with the high MTBF and operational readiness requirements of V/STOL. A schedule as to when hard facts on ROVAC should become available is summarized in a letter from Wayne R. Bomstad, P.E., Vice President-Engineering at ROVAC. The letter is Appendix F of this report.

4. Other Contributions

Two ECS manufacturers who contributed detailed written contributions to this study were Airesearch Manufacturing (Garrett) and the Sundstrand Corporation. Both should be regarded as initial feasibility calculations, and not recommendations for a design. These are presented in Appendix G and Appendix H, without any editing by General Electric.

3.8.3.4 Conclusions and Recommendations

It would appear that a Freon-vapor compression system should be the ECS for electronic cooling of integrated racks, etc. as:

1) high C.O.P. will minimize the aircraft fuel-performance penalty.

2) ideally adapted to system cooling and dehumidification during ground operation.

Further, there may be justification for a separate air-cycle system to provide pressurization and heating/cooling of crew quarters.

This determination of system configuration is worthy of a separate study by those expert in this field.

3.9 MAP Avionics Development Planning

The development and implementation of MAP standard avionic modules (SAM's) and integrated racks adds an additional element of complexity and scheduling for the initial platform implementation. Assuming that the V/STOL Type A platform is used as the driving requirement for the MAP program, the two programs' schedules must be compatible and supportive. To achieve extensive application of standard avionic modules and integrated racks to V/STOL avionics, and to allow potential V/STOL avionics vendors to comply with specifications to use these modules and racks, requires that:

1) Full specifications and documentation for the standard modules and integrated racks be available to the vendors at the time of the RFP's for V/STOL engineering development module (EDM) hardware (1985).

2) The potential vendors be provided with sufficient information, sufficiently early to accommodate the impact of using standard modules and racks into their development and manufacturing process.

3) Essential mechanical and electrical characteristics of the modules and racks be fully validated prior to the preparation of the EDM specifications.

3.9.1 MAP Standardization Plan

The following tasks for development and implementation of MAP standard avaionics modules (SAM's) and integrated racks must be coordinated with the total V/STOL development plan:

1) Development, implementation and verification of MAP mechanical and electrical concepts and standards.

2) Integration of subsystems into integrated racks.

Without proper planning and management, these tasks could induce slips into the V/STOL development schedule or cause system implementation concepts to be frozen earlier than is desirable.

The time phased plan shown in Figure 3.9-1 provides for completion of module and rack validation, and specifications preparation to allow their use in V/STOL engineering development model equipment. This plan provides a relatively firm set of essential functional SAM's that have been specified, developed (prototypes) and verified by mid-1984. This results in a firm baseline for EDM equipment specification preparation proposal activity and procurement. This approach is essential to reduce the cost and technical risks to an acceptable level for both industry and the Navy.

Successful implementation of MAP requires that the V/STOL system architecture must be designed to accommodate projected technology improvements. Careful attention to the design of a distributed system, its bus capacity and formats, and to functional partitioning can provide V/STOL

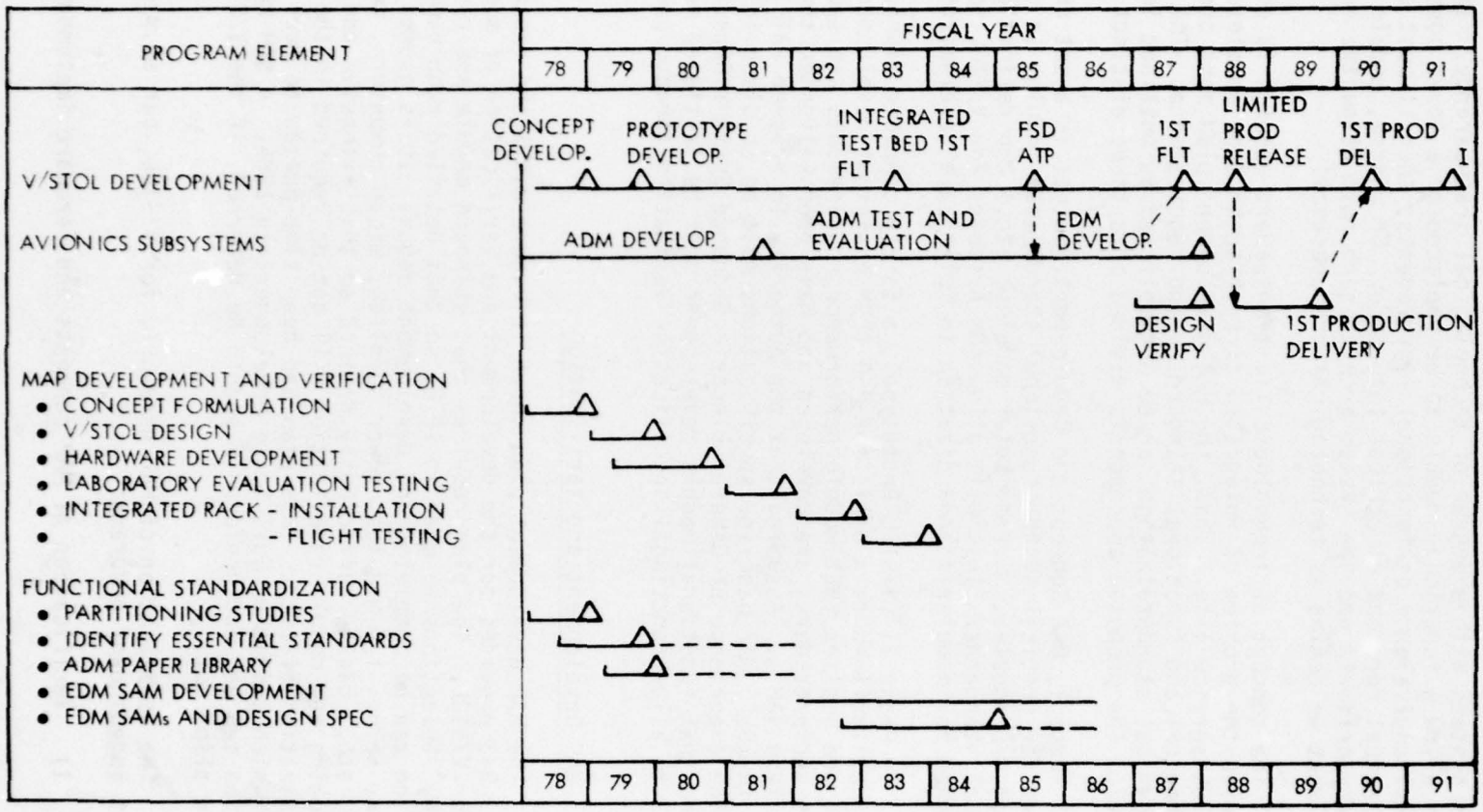


Figure 3.9-1. MAP Development and Standardization Plan

avionics systems with a degree of technological transparency. If technical advances allow a functional module to be replaced by a lower cost module with functional equivalency or functional improvements, then it must only satisfy the mechanical form and electrical interface. Of course, module repair or throw-away criteria and the system architecture must allow the replacement. That is what we define as technological transparency.

The concept of technologically transparent modules is essential in coping with the problem of integrated circuit technology obsolescence over the V/STOL service life. Thus, the MAP development plan must consider both the mechanical and functional standardization requirements. The functional and mechanical standardization can be accomplished as outlined in Figure 3.9-2. The proposed approach is divided into three distinct phases.

Phase I, MAP Concept and Development, output is a set of design standards for critical system functional standarized modules (e.g., power supplies; I/O modules, microcomputer modules, etc.) and definition of MAP mechanical standards. This will allow ADM Avionics for V/STOL to be partitioned for modular standardization in Full Scale Development (FSD).

In Phase II (V/STOL Prototype), a fairly complete library of SAM's must be well-defined as a basis for FSD (EDM equipment development). Well-defined implies that module performance requirements are specified, test fixtures and procedures are developed and have been validated through testing of prototype SAM's. Assuming that the Authority To Proceed (ATP) into FSD is granted in 1985, MAP baseline specifications must be in place in mid-to-late 1984. The experience of General Electric Ordnance Systems Department indicates that functional module development must be initiated no later than mid-1982 to allow functional specification validation through prototype SAM testing.

3.9.2 MAP Development and Verification

The MAP development plan shown in Figure 3.9-1 and expanded in Figure 3.9-3 provides for the development and verification of modules and racks for V/STOL. The plan requires that standard module and rack conceptual approach. Selections be made in 1978, so that detailed requirements definition can be completed and development begun. It is asumed that certain functions (e.g., I/O modules, power supplies, micro computers, memory modules, etc.) can be sufficiently defined so that extensive additional partitioning and module redefinition will not be required in the down-stream standardization efforts. This plan has been time-phased to meet a V/STOL program which initiates Full Scale Development in 1985. A SAM mechanical definition can be, and preferably should be deferred, if the V/STOL Program schedule slips out.

The verification of MAP hardware, for V/STOL, can be viewed as two somewhat independent programs:

1) Verification of MAP concepts and hardware implementation.

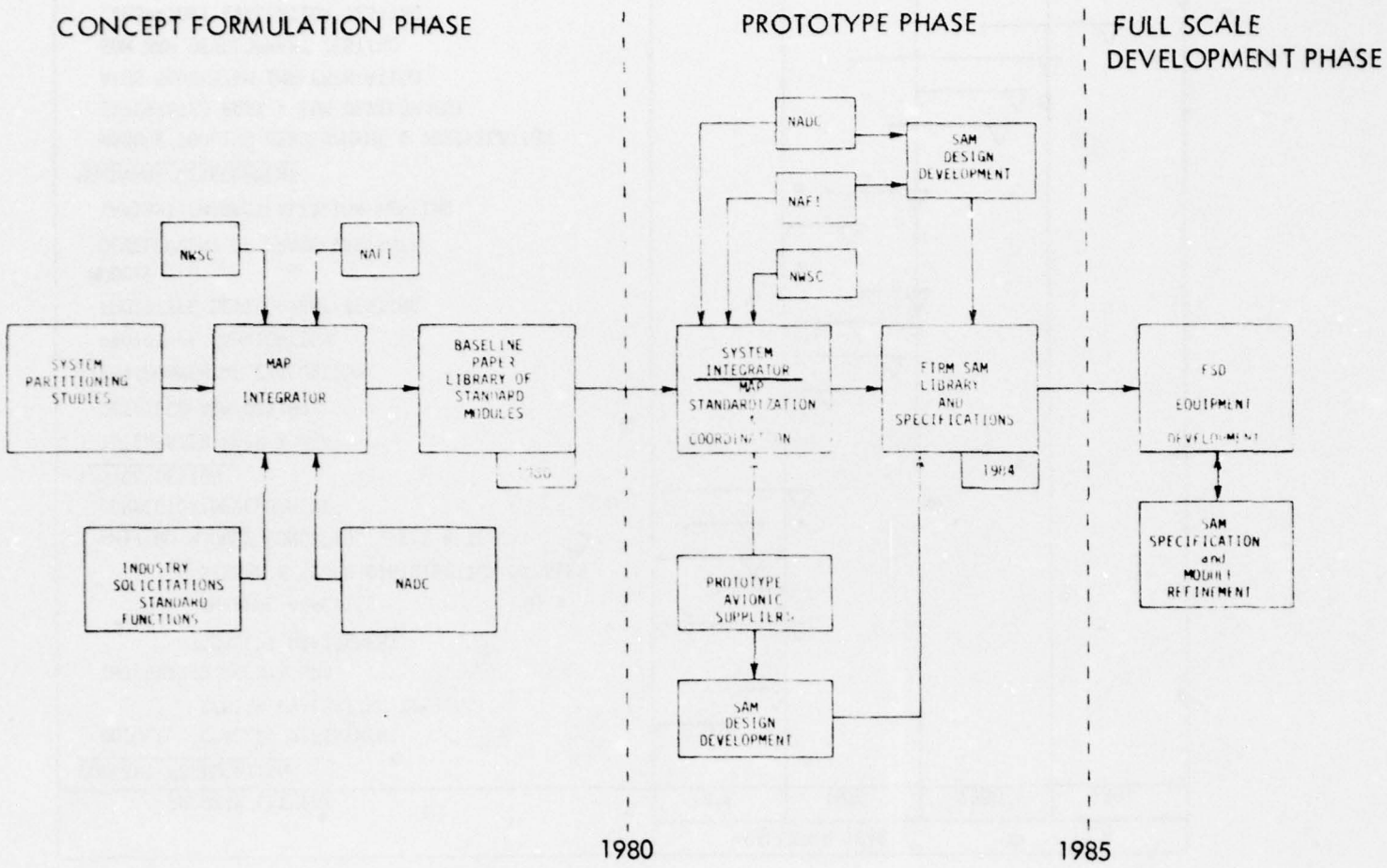


Figure 3.9-2. MAP Standardization Plan

MAP DEVELOPMENT PLAN

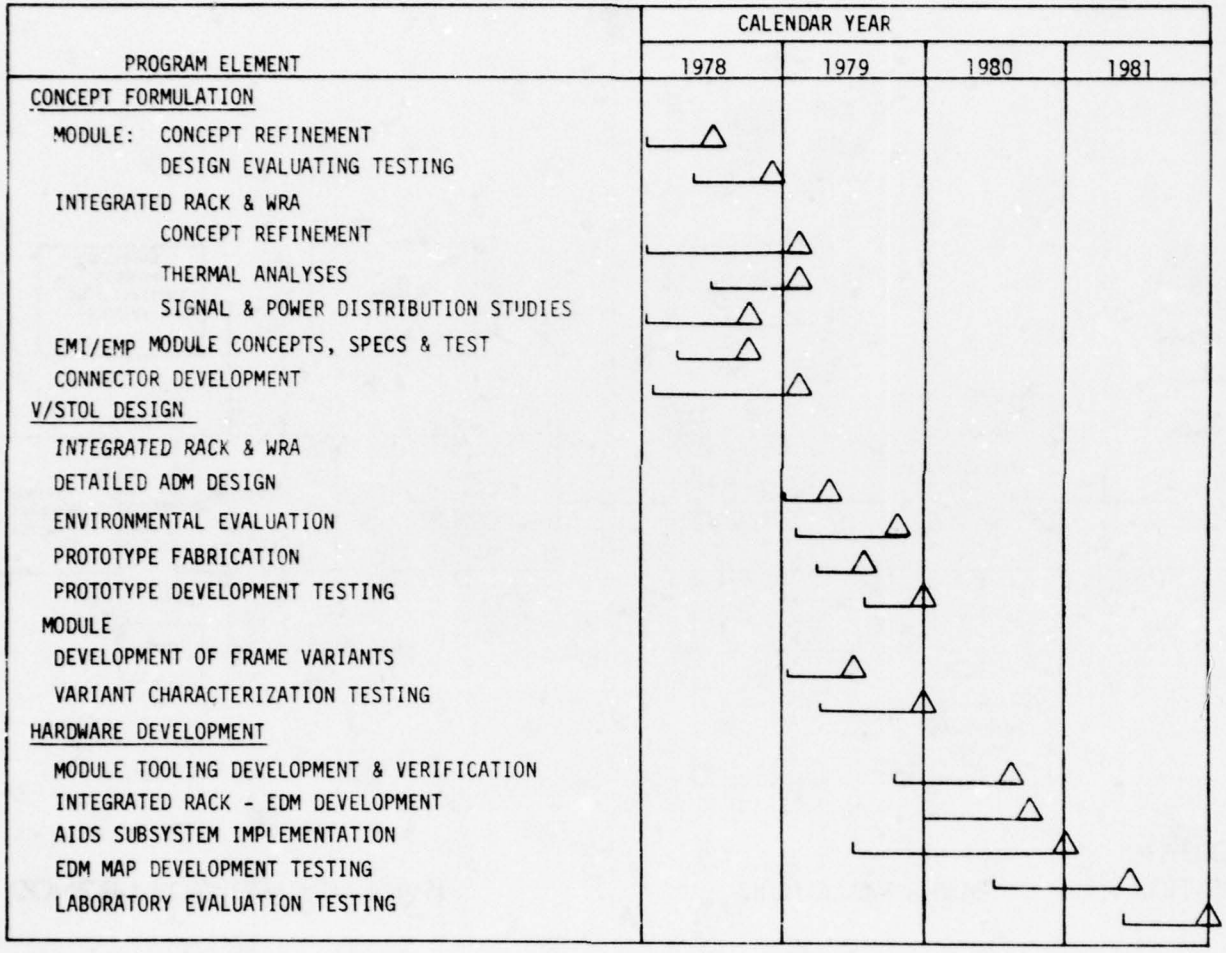


Figure 3.9-3. MAP Development Plan

2) Verification of system architecture; signal and power distribution concepts; and system and subsystem performance characteristics.

Validation of the MAP mechanical concepts including flight-testing of an integrated rack will be required as a prerequisite for DSARC II approval for Full Scale Development. A firm module mechanical definition is required prior to the development of a functional module specifications for the EDM hardware. It is recommended that selected AIDS functions be used for MAP development and validation. AIDS electronics design from the outset has been directed to using standard modules and integrated racks. This demonstration may be achieved by packaging AIDS Electronics on SAM's in a prototype integrated rack. In the early 1980 time frame, this demonstration will require industry assembly of integrated-circuit chips into chip carriers, and the possible use of hybrid techniques. This technique has been implemented on the General Electric AN/SQR-19 equipment. This approach will also allow development of a set of Core standard functional modules. Properly specified, these functions can be technologically transparent to the advanced semiconductor technology anticipated for EDM and production implementation.

The approach is considered too costly and lacks sufficient flexibility to meet the general packaging needs of the V/STOL prototype phase (ADM) Avionics System. It is also inhibited by the unavailability of 1985 projected LSI technology.

The second verification requirement is that of system architecture and avionics system/subsystem performance. The integrated technology assessment indicates that in the late 1970's and early 1980's, available LSI technology will not allow packaging densities of the order to be achievable in 1985 and beyond.

It is feasible however, to develop a prototype integrated rack that will accept a larger module (i.e., 3/4 or full ATR) which maintains a technologically transparent interface into the FSD and production phases. This will allow signal distribution, power distribution, back panel, system architecture, and subsystem performance to be validated with a representative electrically-integrated rack. Obviously, if the operational requirements change, and the module-level functional requirements are impacted, the technologically transparent requirement becomes academic.

In view of the above assessment, it is recommended that the MAP demonstration avionics be considered independent of the prototype V/STOL test-bed avionics. This will allow both concepts to be validated with maximum degree of flexibility.

3.9.3 Module and Rack Acquisition and Testing

The concepts developed during the study suggest methods of specification, procurement and acceptance testing not too dissimilar to those used in current weapon systems. At the highest level, of course, is the total weapon system, its specifications and system evaluation tests. Here

the total weapon system is tested to prove its capability to perform mission warfare tasks.

Below that level is the avionics system evaluation where the total avionics system installed in the aircraft is subjected to extensive performance tests using simulations on the ground and specifically designed flight tests. The total avionics system must be shown to pass reliability qualification tests, maintainability demonstration tests, vibration and EMI tests. This testing is normally performed by the airframe contractor or an avionics system integrator. For an avionics system that uses standard modules and integrated racks the avionics system level evaluation tests are expected to be essentially the same as those performed with traditional avionics.

Acquisition and testing of subsystems by the avionics system integrator will be somewhat different for the case of standard modules and racks. The concept developed for integrated racks includes backpanels which correspond to segments of subsystems in traditional avionics. Module, rack, and backpanel standards must be specified in the subsystem procurement specifications. This will include internal rack EMI requirements and signal interface specifications. Acceptance testing will be performed on the subsystem backpanel and electronics only in a section of an enclosed integrated rack. EMI sources and sensors will be located within the rack to demonstrate that the subsystem meets EMI requirements in all respects. Other performance measures can be evaluated in very much the same manner as is done now with traditional avionics subsystems.

Design of subsystems and procurement of modules will be very much more constrained using standard modules and racks than current design procurement vs modules may be acquired either GFE or CFE depending upon the total usage by the government. Each module must be subjected to acceptance testing including EMI testing described in Section 3.6. The subsystem back panels will be designed, fabricated and tested to demonstrate their adherence to standards and finally the entire subsystem assembled and tested as discussed above.

3.10 Conclusions and Recommendations

3.10.1 Integrated Rack Conclusions and Recommendations

1) Initiate integrated rack design refinement program for FY1978 and FY1979. This program shall address:

(1) Thermal performance:

a) Cooling path sizing and performance to meet anticipated module thermal loads

b) Direct air cooling of modules as a function of altitude

c) Variable speed D.C. fans for altitude compensation

d) Size module contaminant level and control requirements in closed air-cycle cooling

e) Dehumidification requirements and penalties

f) Integrate thermal design of rack with final SAM definition

(2) Mechanical performance and requirements:

a) Investigate and finalize module retention methods

b) Refine airframe/rack structural interface requirements

c) Address specific installation restrictions of Core vs mission avionics. Define SAM computable WRA approaches

d) Define rack structural concepts and final rack design. Integrate with airframer performance requirements (shock and vibration)

e) Establish mechanical interface specification requirements for modules, back panels card-cage unit, and rack-comparable WRAs. This specification would control the incremental modularity requirements and the interface dimensions of all rack installed hardware.

f) Define power supply mechanical requirements to insure proper thermal, mechanical, and back panel interface relationships. Investigate and define intrarack 270 VDC power distribution methods.

(3) Maintainability

a) Refine front installation concepts relating to module accessibility, back panel replacement, and inter-subsystem and rack wiring requirements.

b) Investigate and finalize fiber-optic interface requirements. Address basic considerations such as requirements for single vs. multicircuit connectors and module vs back panel fiber-optic interfaces.

2) Fabricate rack mockup and design evaluation test hardware. Design evaluation testing should be performed (early FY1980) to verify SAM, ECS, and airframe environmental compatibility to facilitate establishment of a preliminary MAP interface specification. This test program should incorporate SAM functions and verify electrical, fiber optic interconnection, and EMI-control concepts.

3) Develop an interface specification which will be the basic design and control document to allow the avionics industry to supply MAP-compatible avionics hardware.

3.10.2 Standard Avionic Module Conclusions and Recommendations

1) Full chip carrier (cc) compatibility is required for SAM. Chip carriers will replace DIP's as the standard integrated circuit package (1985).

2) SAM must be capable of being either conduction- or convection-cooled to provide maximum application versatility.

3) Power is the driving SAM requirement (20-watt capability required).

4) A larger connector is required to circumvent system partitioning restrictions (120-130 pins).

5) A higher Improved - 2A (HI-2A) module provides a thermally acceptable configuration with minimum weight, complexity and cost, and complete chip-carrier compatibility.

6) The I-2X, I-2B, and HI-2A module configurations are compatible with conduction (+45°C coldplate) cooling requirements.

7) The standard I-2A SEM is thermally unacceptable for conduction cold-plate cooling at the required power levels (20 watts).

8) The conductivity of the multilayer ceramic substrate is a significant factor in conduction-mode cooling performance, in contrast to glass epoxy multilayer boards.

9) LSI package heights (proposed JEDEC standard) preclude a two-substrate module on 0.3 or 0.4 inch centers.

10) The full range of proposed JEDEC chip carrier sizes will not fit within the I-2A substrate size limits.

11) A single substrate module configuration is more cost-effective and eliminates the reliability penalty of inter-substrate connections.

12) Direct coolant to module interface results in a two to three times improvement in module thermal capacity, as compared to conduction cooling. This is evidenced in direct air-impingement cooling modes, and in Cases 4, 5, 6, and 7 which eliminate the conductive mechanical interface losses.

13) Liquid cooling offers the potential for highest thermal performance and minimum thermal stress (Case 3 vs Case 5). The liquid interface vs maintainability consideration is the major item limiting the practical application of this technique.

14) A thermal interface to the module top fin offers improved thermal capacity (Case 7) of the I-2A. Top fin cooling in conjunction with guide rib cooling could potentially provide sufficient thermal performance for MAP (not analyzed). A mechanical top-fin-to-heat-exchanger interface would be sensitive to tolerance and flatness limitations (0.001 inch clearance equivalent to 1°C/watt thermal resistance).

15) System partitioning analysis indicates that single-span (I-1A, etc.) modules are not an effective form factor.

16) All conduction-cooled module configurations investigated have less than 20-watt power dissipation capacity in a projected MIL-E-5400 WRA environment (+71°C exhaust temperature).

3.10.3 Module Recommendations

3.10.3.1 Connector

Develop a higher capacity connector (120-130 pin), utilizing low-insertion force contact technology. This development should address:

- Maintain 0.3 inch module pitch
- Wire Wrap capability
- Multilayer board design constraints
- Connector/module substrate interface computability

3.10.3.2 Chip-Carrier Packages

Influence JEDEC chip-carrier package standards to optimize their tolerances and dimensions to SAM application requirements. Of particular importance is the JEDEC maximum thickness dimension of 0.14 inches, which severely impacts the spacing of double-substrate modules. Presently-available chip-carrier packages are in the range of 0.06 inches thick.

Also of considerable importance is the resolution of the lead spacing; i.e., 0.04 inch vs 0.05 inch. It seems that early selection of one spacing is essential to the successful application of chip-carrier devices. The industry does not need another DIP/flatpack conflict.

3.10.3.3 Substrate

Develop substrate materials as alternates to multilayer ceramics. Chip-carrier compatibility, lower dielectric constant for improved high-frequency applications, cost, weight, and manufacturability are basic considerations. Refer to the discussion in Section 3.3.3.1.

3.10.3.4 Module

Refine the HI-2A (3/8 ATR) and I-2A/2B module concepts. The conduction cooling capacity of the HI-2A and I-2B can be increased by increasing the heat-sink thickness within module pitch/chip carrier thickness requirements. A preliminary estimate indicates that the 20-watt capacity can be attained for MIL-E-5400 conditions (+71°C air exhaust, +125°C T_j). Departure from the SEM standard 100-pin connector will allow other areas of optimization to be considered, such as the guide-rib interface.

Chip-carrier standardization results should be factored into the configuration refinement.

The final decision between the I-2A/2B type SAM and the HI-2A configuration will be most dependent on the relative importance of:

- Extension of the present SEM program to avionics.
- Weight and volume goals in future avionic systems.
- Compatibility with future LSI packaging requirements.

3.10.3.5 Liquid Cooling Interface

Scope the magnitude of the problem of developing a suitable quick-disconnect - leak-proof coupling. This is the main constraint limiting the application of liquid cooling at the module level.

APPENDIX A

STUDY OF INTEGRATED CIRCUIT TECHNOLOGY

WITH PROJECTION AND FORECAST TO 1985 - 1990

APPENDIX A

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APPENDIX A

Study of Integrated-Circuit Technology with Projection and Forecast to 1985-1900

Part I. 1985-1990 Technology Projection

A.1 Intoduction

This study considers presently available Integrated Circuit devices available in the market.

It traces the development of available IC's considering device speed, size, reliability, capability, and packaging. A projection is then made, in relatively linear fashion, to the probable device capability in the 1985-1990 time frame.

Obviously some technolgies so projected will reach their physical limits, or the limits imposed by present processes.

An attempt is made to forecast the progress of newer devices and methods, following the same trends found for established technologies.

In the past, predictions of device complexity and availability were based wholly on the activities of the U.S. market. The U.S. semiconductor manufacturers have been uncontested leaders. In recent years, however, Japan has developed a technology base and marketing strategies which may challenge this leadership.

Japan has organized a "VLSI Group" -- a government sponsored cooperative effort among leading Japanese manufacturers -- to leap forward, over and beyond the U.S. computer and semiconductor industry technological position. Table A-1 gives some insight into the financial resources backing the Japanese challenge. Japanese semiconductor production comes from their major equipment firms. About half of this semiconductor production is for in-house use, with the rest going to domestic and export sales. Exports to the U.S. average 3 percent.

Table A-1. The Japanese Market - 1976 Sales
(Source: Electronics, 9 June 1977)

Company	Equipment Sales (Billions of dollars)	Semiconductor Division Dollar Volume (Millions)
*Nippon	$1.8	$357
*Toshiba	3.5	300
*Hitachi	6.5	220
*Fujitsu	1.2	112
*Mitsubishi	2.5	400
Matsushita	6.1	162

*Member, "VLSI Group"

Figure A-1 summarizes Japan's technological goals. They plan to accomplish these goals by having full-production E-beam and X-ray capabilities by 1979. Such goals give the Japanese a schedule of development which is two to three years ahead of the existing U.S. timetable. (Compare Figure A-1 with Figure A-2.)

There are diverse opinions both in Japan and in the United States as to how successful the Japanese will be. E-beam processing presents many challenges in throughput (number of wafers/minute), alignment and diffusion techniques. "Leaping" into E-beam too early could prove counter-productive.

Two approaches are developing in the United States. Texas Instruments is reacting to the Japanese challenge by moving quickly into E-beam. Intel, on the other hand, takes a more conservative approach. Intel's position is to continue improvements in optical lithography, while gradually phasing in E-beam.

The conservative viewpoint concerning developing technology is reflected in Figure A-3.

The approach is based to a great degree on the Intel opinion. Intel's technological and marketing success over the past few years makes them a credible judge of how the market will move. In addition, there is some question as to how innovative a giant conglomerate such as Japan's "VLSI Group" can be. Much of the U.S. semiconductor technolgical success has been derived from small independent companies dedicated to supplying devices to industry. "Bigness" many times results in "slowness".

	RANDOM-ACCESS MEMORY		MICROPROCESSOR		MINIMUM LINE WIDTH (MILS)
	CHIP SIZE (X 1,000 MIL^2)	BIT DENSITY (X 1,024 BIT)	CHIP SIZE (X 1,000 MIL^2)	WORD LENGTH (BITS)	
1976	32	16	52	8 & 16	0.2
1979-1980	32	64	50	16	0.07
	50	256	60	32	0.04
1981-1983	45	256	55	32	0.03
	60	1,024	65	32	0.02

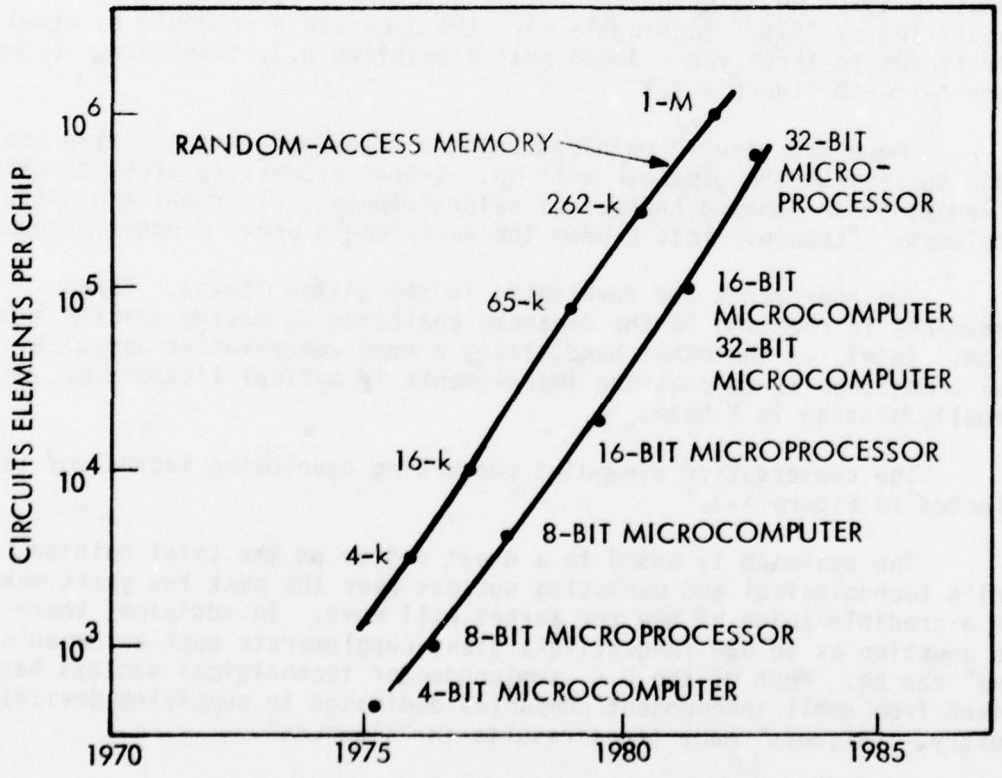


Figure A-1. Japanese VLSI Goals

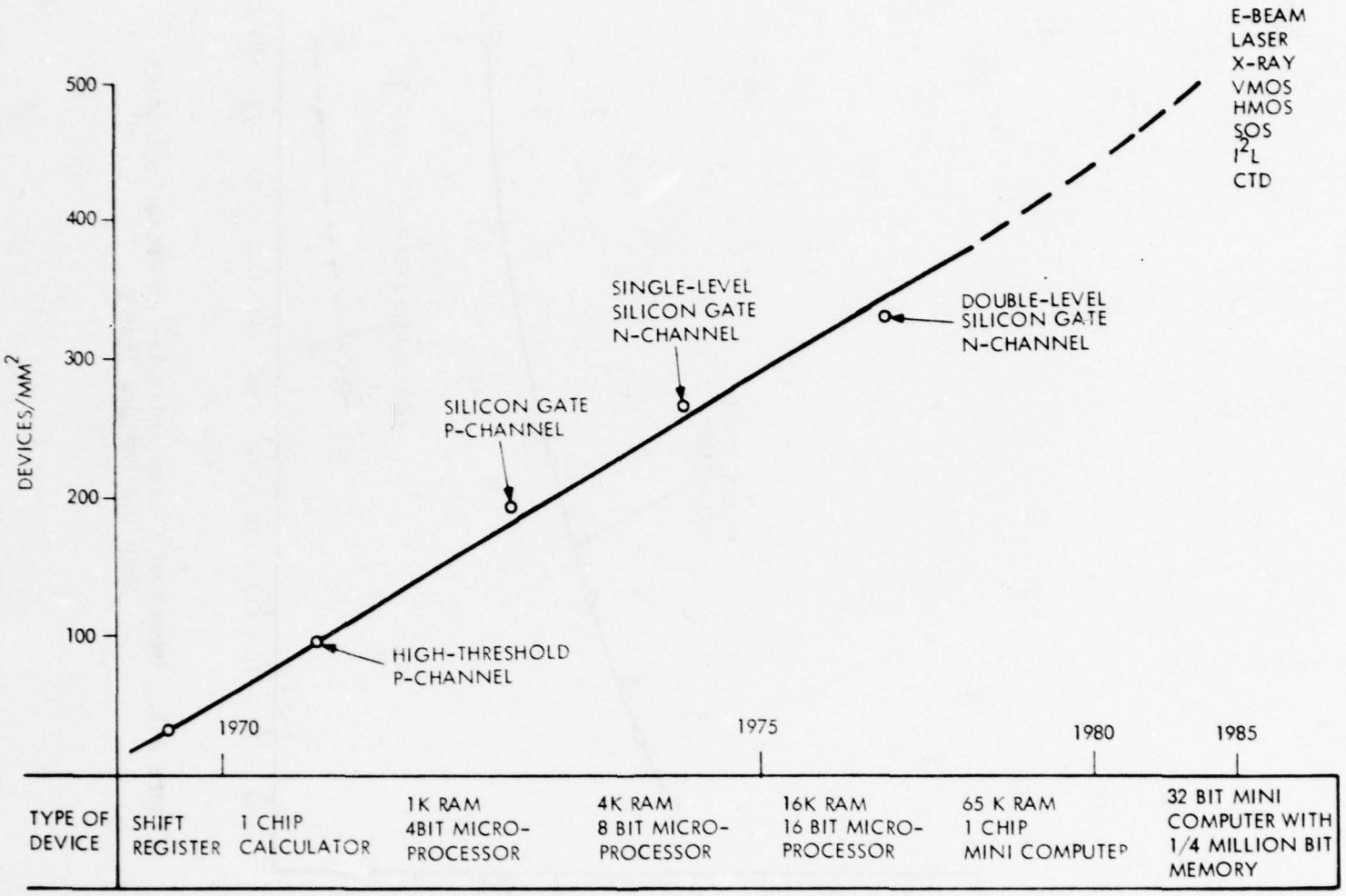


Figure A-2. United States VLSI Goals

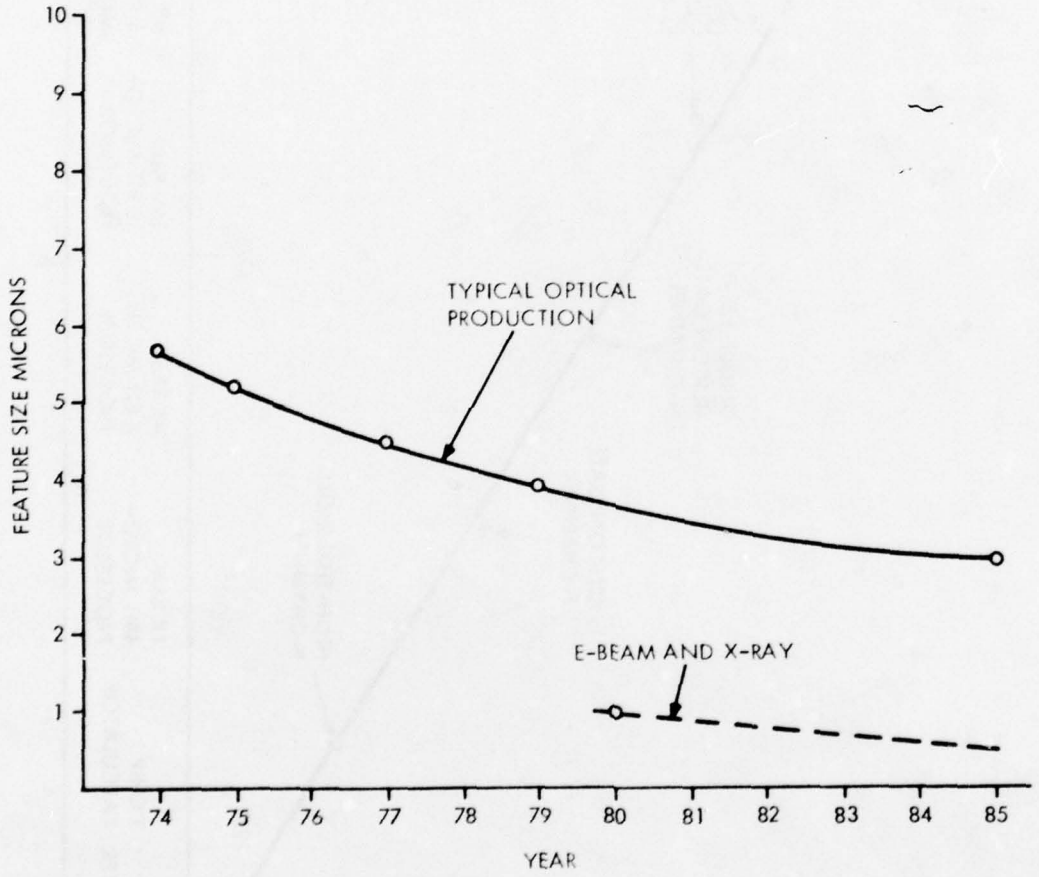


Figure A-3. Impact of E-Beam and X-Ray on Microelectronics Chip Die Feature Size

A.2 General Status of integrated Circuits

A.2.1 General

Over the last 20 years, the semiconductor industry has progressed steadily in its effort to get more capability from semiconductor technology at lower cost. Looking at the decade from 1970 to 1980, events show that every two to three years, new techniques developed in the laboratory reach the point of maturity, where they can provide new and better integrated circuits. The new technologies foster new generations of products and product families -- even whole new areas of applications.

There is no reason to believe that these trends will not continue into at least the mid 1980's. It seems time now for a step function to occur in the complexity of integrated circuits, with new or improved technologies such as HMOS (High density MOS -- Intel), VMOS (Vertical MOS -- HMI), SOS I^2L and CTD (Charge transfer devices). In addition, these technologies should be enhanced with the utilization of E-beam and X-ray masking capabilities, resulting in the appearance of VLSI (Very Large Scale Integration).

For this report, it was assumed that the technologies and fabrication improvements described will be mature in the mid 1980's and in use throughout the 1990's.

A.2.2 Wafer Processing

Over the years, the size of the wafer on which an integrated circuit is fabricated has been steadily increasing, starting from 0.75-inch diameter in the early '60's through three-inch to four-inch diameter wafer emerging in 1975. These sizes are expected to be commonplace by 1980.

This trend will certainly contine, with a five-inch wafer in use by the mid 1980's. However, because of the considerable capital investment associated with smiconductor fabrication equipment, the conversion from five-inch to six-inch wafers will not take place until the late 1980's.

A.2.3 Photolithographic Techniques

The conventional photolithographic technique presently being used by the industry is becoming less and less satisfactory from the point of product yield). Photolitho is also no longer satisfactory since die pattern dimensions are becoming comparable to the wave lengths of the ultraviolet light employed.

The conventional photolithographic process will therefore slowly be replaced by E-beam and X-ray mask techniques. (See figure A-3.) This enables the manufacture of Integrated Circuits to have superior resolution in the submicron range. The impact of the increased density that can be obtained using E-beam masking techniques is shown in Figure A-4. In terms of existing optical processes, this would be equivalent to processing on 20- to 25-inch wafers.

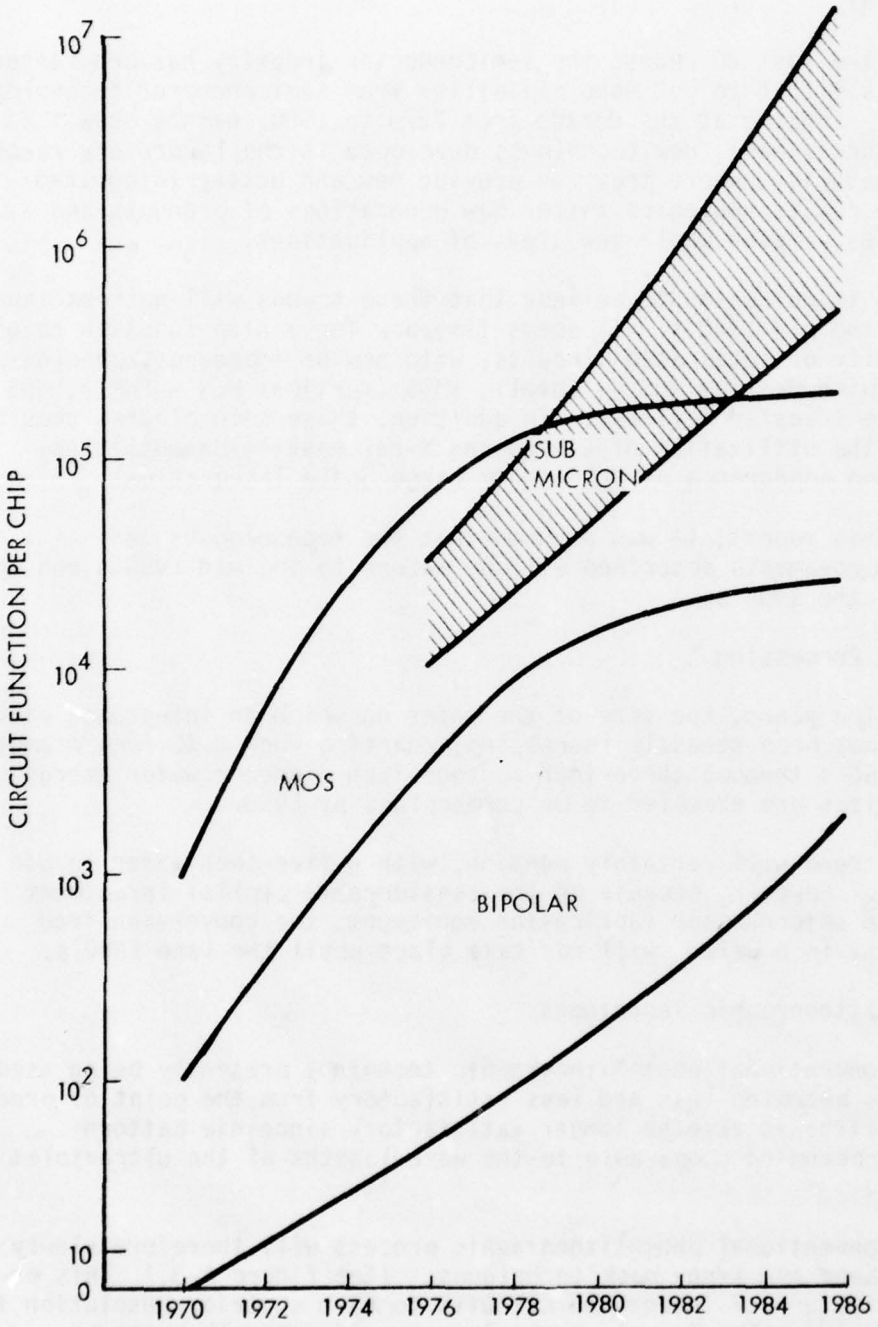


Figure A-4. Anticipated Microelectronics Circuit Density vs. Time

Submicron technology will become important in military applications, because of improvements in reliability, size and overall performance. A one-chip submicron system will be superior to the 20 to 30 present LSI devices it will replace.

One principle impact of submicron technology will be in its application to semiconductor memories. Although the first submicron production structure will be a 16K static or a 64K dynamic RAM by 1978, million-bit chips are possible by the mid 1980's.

A.2.4 Special Performance IC Technologies

While the needs of some military systems can be met with standard commercial technologies such as NMOS and T^2L, many military systems have unique requirements: extremely small size, very low power, analog data processing, or radiation tolerance. These can only be met by using integrated-circuit technologies that are tailored for these requirements.

Since the requirements are for special performance outside the standard commercial lines, and are for only a portion of the already small military IC market, commercial IC houses such as Intel, TI, Motorola, Fairchild, National, etc. do not usually respond to these needs. However, many system suppliers such as GE, Hughes, RCA, Westinghouse, TRW, etc. have vertically integrated so as to be able to produce special performance IC's. These IC's provide leverage at the system level. While the IC level itself might not be produced at a price that would be competitive in a commercial market, the IC provides the key which makes the overall system feasible.

Therefore, when projecting future military system development, we need to consider special performance - systems suppliers - IC technologies as a supplement to commercial IC's.

Currently, CMOS/SOS, I^2L, and CCD are the major contenders among the special performance IC technologies. Each is being produced or is under development by at least three companies. CMOS/SOS provides a solution to the need for either very low power consumption and/or radiation tolerance. I^2L provides the capability to perform both linear and digital functions on the same chip, and has shown the potential to be radiation hardened.

CCD provides the capability to do analog data processing (including image processing), and has been evaluated for use as a high-density logic technology.

The major special performance IC technology under development for the 1980's is GaAs (gallium arsenide). Its uses include SFET (Schottkey Field-Effect Transistors) and TED (Transferred-Electron Devices). The large advantage of GaAs is speed; the technology offers the potential for multi-gigahertz digital systems. Current activity in GaAs is at the laboratory stage. Predictions are that, by 1985, utilizing E-beam processing, devices with 100 gate density and operating in the 10-gigahertz range may be manufactured in production quantities. Such production will be

limited to special applications in the military marketplace. The devices will be produced primarily by military equipment houses, with little influence from the commercial semiconductor industry.

A.3 NMOS Technology

The MOS technology started out with a high threshold P-Channel with multiple power supply requirements. At best, these circuits could produce a simple calculator and serial-storage function. MOS then moved to N-Channel technology, with capabilities of producing a complex computer on a chip, with clock periods of less than 500 nanoseconds. Static/dynamic memory devices with less than 75 nanoseconds operating time resulted, all working on a single 5-volt power supply. This rapid growth in density and performance will continue into the mid 1980's. The introduction of new N-Channel technologies like HMOS and VMOS, along with new fabrication techniques such as E-beam or X-ray, will continue the development of MOS techniques.

However, it should be noted that in order for the HMOS to reach its full potential, the integrated circuit users must be willing to operate these devices at lower supply voltage (2- to 4-volt range). Lowering the supply voltage will increase the reliability of the device because it reduces the possibility of punch-through voltages. At the same time, lower voltage optimizes the electric field in the channel region. The increase in performance is even more striking. For RAMs and microprocessors (Figure A-5), the impact on the speed-power product alone would make it worthwhile to go from 5V to a 3V. For RAMs which operate at the saturation point of the speed-and-power curve, the lower power supply voltage reduces power dissipation by approximately 60 percent, while maintaining the speed. Reduced power dissipation becomes extremely important as the chip density goes up.

By operating microprocessors with reduced voltage, they can take full advantage of a significant speed increase for a given power dissipation. A 3-volt microprocessor chip, for example, will operate at twice the speed of a 5-volt device. The effect of supply voltage on various existing MOS processes is shown in Figure A-6. The desirability of lower operaing voltages is evident.

By the mid 1980's, a 64K static RAM, consuming less than 800 mW and operating in the 100-nanosecond range is predicted. This N-channel technology, together with new fabrication techniques, will also produce 16-32-bit microcomputer chips containing a quarter of a million bits of program memory by the mid 1980's. A form of this technology will be one of the leading technologies (if not the leading one), well into the 1990's.

A.4 PMOS Technology

PMOS devices were the building blocks for the MOS industry. PMOS devices can be found today in many older designs. However, since this report is addressing the technologies of the mid 1980's and early 1990's, it is

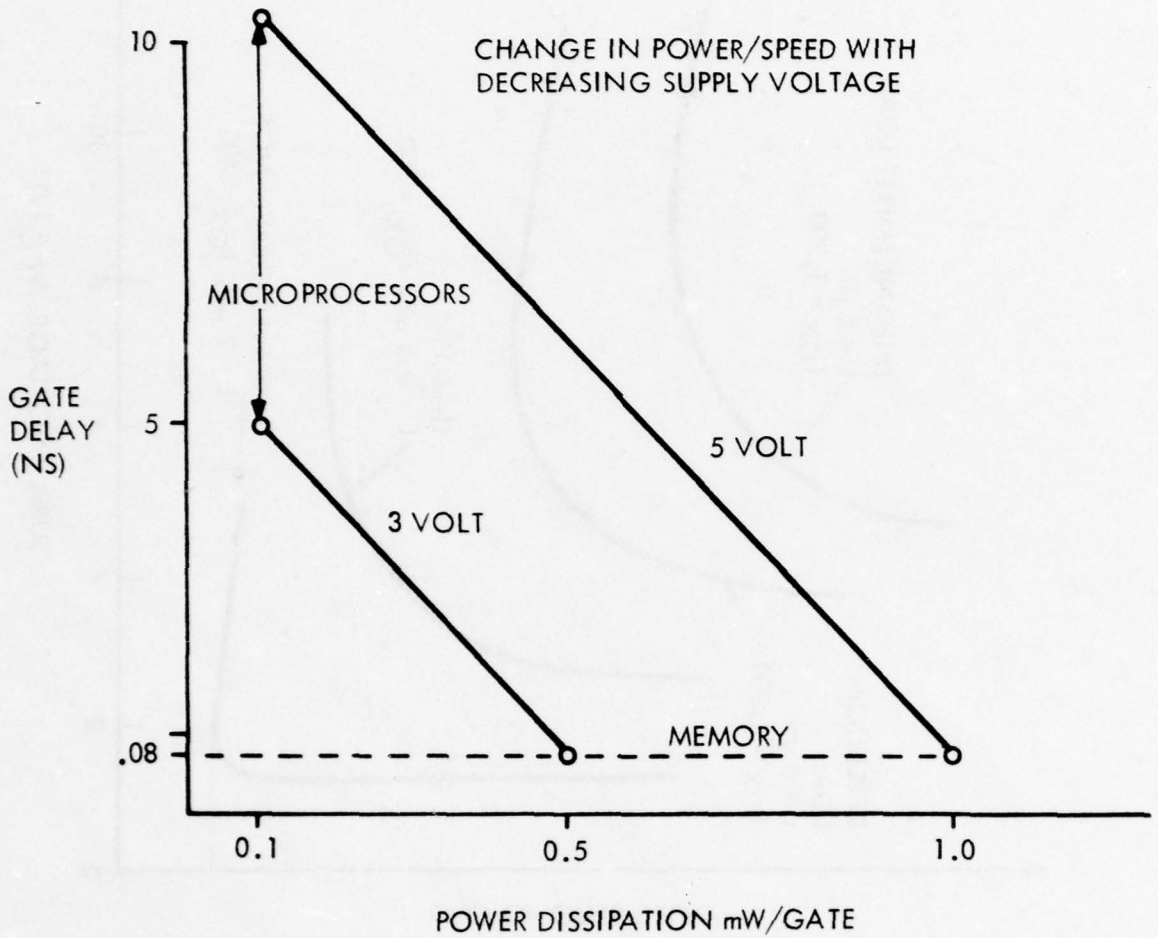


Figure A-5. Microprocessor/Memory Change in Power/Speed vs. Decreasing Power Supply Voltage

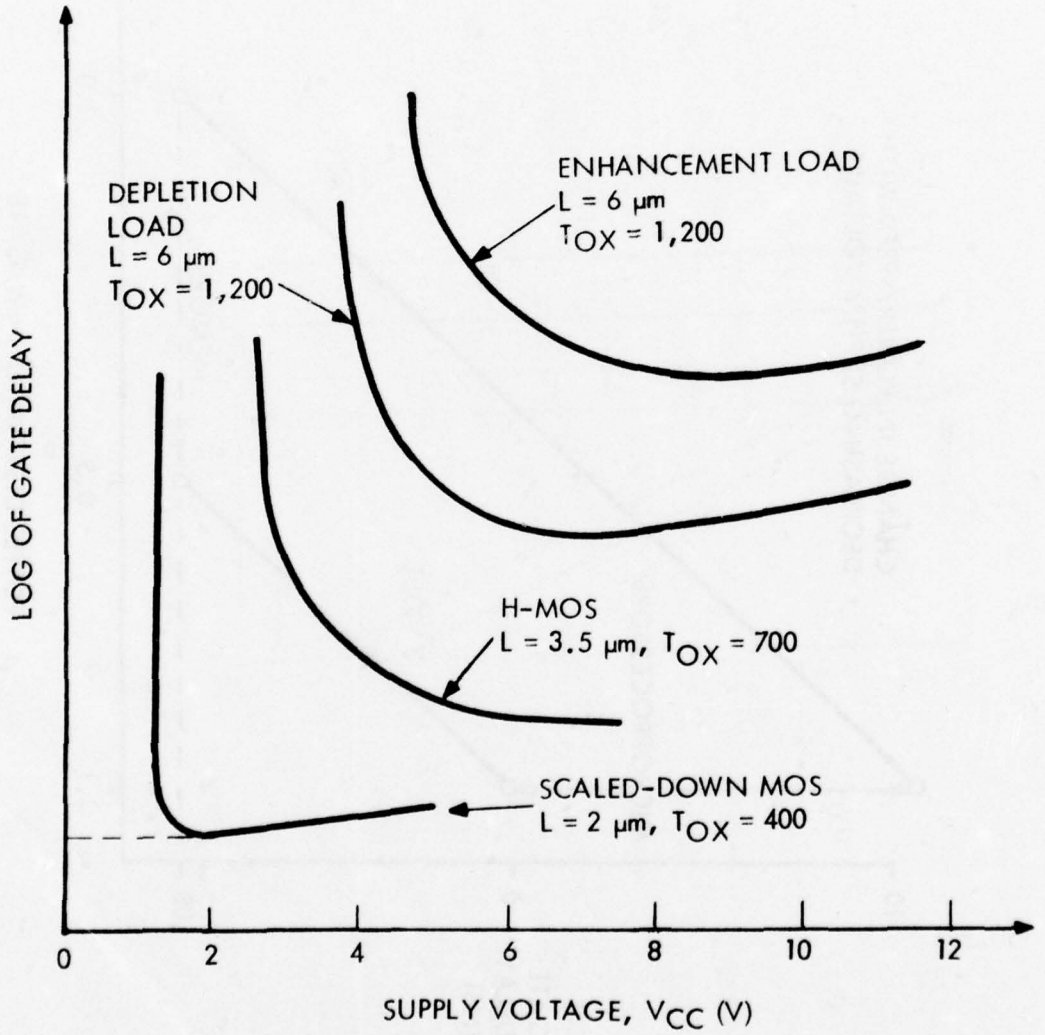


Figure A-6. MOS Process: Gate Delay vs. Supply Voltage

sufficient to say we believe that by that time period, PMOS technology will be all but extinct.

A.5 CMOS Technology

A.5.1 Description

Complementary metal oxide semiconductor (CMOS) is an offspring of the PMOS and NMOS technologies. A PMOS and an NMOS transistor are fabricated on the same substrate, in complementing pairs, to form the basic CMOS circuit. The performance features of CMOS are very appealing. They are:

Low power dissipation

High noise immunity

Wide operating voltage range (3 to 15 volts VCC)

Moderate speed

Low power is derived from the low steady state (Logic 1 or 0) leakage current of either the PMOS or NMOS transistor when in the ON state. High currents exist only during the switch from one state to another. As Figure A-7 shows, the power dissipation per gate is considerably lower than competing technologies. However, this is true only below the 5 MHz range. Beyond that point, CMOS loses its power-consumption advantage. The high noise immunity stems from the voltage threshold required to switch states. This is usually 40 percent of VCC. For 5 volts VCC, the device will be immune to noise spikes up to 2 volts. For VCC at 15 volts, noise spikes up to 6 volts would not interfere.

CMOS is clearly not cost competitive with NMOS and TTL, unless power is a concern. For example, 256x4 static RAM (ceramic, commercial temperature, 1-99 pcs.) are presently priced as follows:

CDP18225	CMOS/SOS	35 mW @ 10V	200 ns	$45
4721	CMOS	50 mW	100 ns	$63
93422	TTL	700 mW	60 ns	$25
3538F	NMOS	300 mW	350 ns	$ 9

A.5.2 CMOS on SOS

A significant improvement in the packing density of standard CMOS (sometimes referred to as bulk CMOS) is realized by utilizing a sapphire substrate (Silicon On Sapphire). SOS eliminates the need for isolation barriers between complementing pairs (the sapphire provides the barrier). The sapphire substrate results in die sizes approaching that of NMOS. Refer to Table A-2. The higher packing density also results in improved

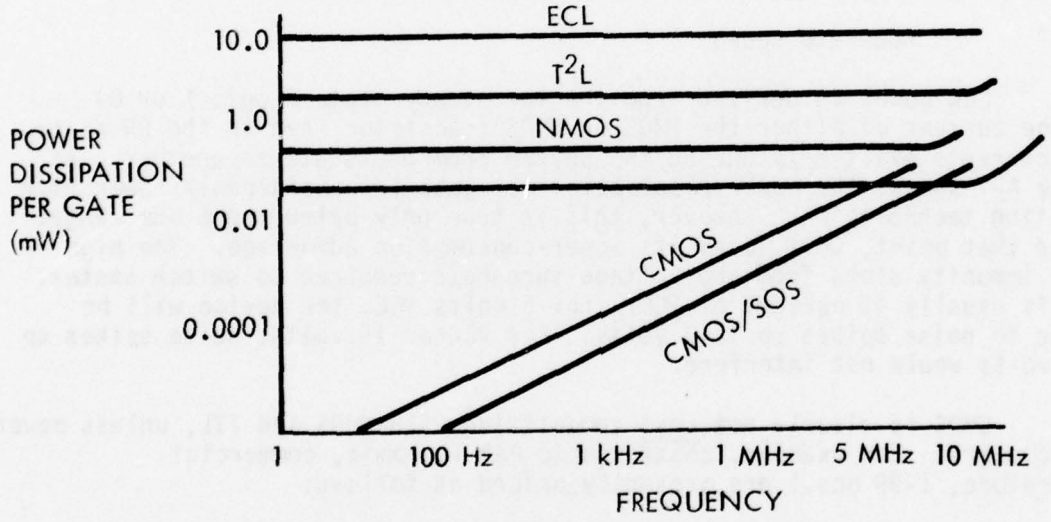


Figure A-7. Power Dissipation per Gate vs. Frequency for Various Microelectronics Technologies

speed/power performance and radiation hardening. SOS overcomes the major producibility problem of bulk CMOS (large dies, resulting in low yield and high cost).

Table A-2. Packing Density and Mask Step Comparison of Microelectronics Devices

Area/Gate (MIL^2)	NMOS 2-6	TTL 20-60	I^2L 4-6	CMOS 10-30	CMOS/SOS 8-12
Mask Steps	6	7	6	7	6
Diffusion Steps	3	4	3-4	4	5

Unforturnately, the scarcity of sapphire results in high cost for the basic substrate boule. Estimates are that a wafer of sapphire costs five times that of silicon. This higher cost cancels out the cost gain in die yield.

Over the next ten years, as sapphire becomes more readily available, costs will drop. CMOS/SOS will replace bulk CMOS. It is unlikely, however, that it will compete effectively against NMOS and bipolar logic in the high volume semiconductor market. CMOS/SOS will lay claim to that small segment of the market where power dissipation, noise immunity and radiation resistance outweigh cost considerations.

A.6 Standard Bipolar Technology

Technologies such as T^2L and ECL will continue well into the 1990's T^2L, in particular, has demonstrated the ability to remain in the market with NMOS. T^2L 4K static hi-speed RAMs (30 ns access) are available today. Although T^2L will fall behind NMOS for functional density (i.e., 16K RAM, 64K RAMS), it will hold a position in the marketplace for special high-speed processing devices and interfacing. For super-fast data proessing, devices employing ECL internally, with T^2L at the pin in/out will become popular. An example of this is TRW 16 x 16 multiply in 150 ns. (The closest MOS devices today are in the 50 us range.)

However, such devices will dissipate 3 to 5 watts of power. Special heat removing techniques will be required. Die sizes for these bipolar devices will also continue to be larger than comparable MOS and I^2L devices, resulting in higher prices.

In the 1985-1990 time frame, standard bipolar devices will hold less and less of the semiconductor market. Improvements in NMOS performance

(along with the inherent packing density advantage) will chip away at standard bipolar domains.

A.7 Charge Transfer Technology

A.7.1 Description

This category covers the Charge Coupled Device (CCD's), Surface Charge Transistor (SCT's) and Charge Image Devices (CID's). Of all these, the CCD is the most prominent due to its impact on the memory market.

CCD (Charge Coupled Device) is a MOS technology which will gain popularity over the next ten years. In CCD, charge packets representing digital data are brigaded serially through the silicon substrate. CCD memories have three to four times the bit-packing density of MOS RAMS, because CCD uses a serial-bit transfer not requiring the row and bit sense circuitry associated with MOS RAMS. Although much slower than RAMS (serial operation vs. random access), CCDs have much higher memory capacity resulting in lower cost per bit.

CCD memories will fill the cost-performance gap between high speed RAMS and disc/tape memories.

Figure A-8 compares the progress expected through 1980-1985 for CCD and other memory media. In general, CCDs are two to three years ahead of MOS RAMS in terms of memory capacity. For example, Intel announced their 16K CCD in 1975; 16K MOS RAMS appeared in 1977. Fairchild and T.I. introduced (Preliminary Data Sheets CCD 464 and TM 3064) 65K CCDs in 1977: 65K RAMS will not appear until 1980. These 16-pin devices, with typical power dissipation of 225 mW at 5 MHz, will capture a large segment of the disc/tape commercial market.

It is unlikely that CCDs will be widely accepted in military applications. The charge transfer mechanism is very sensitive to temperature. Devices presently available will operate only over the 0-50°C range, with 0 to 70°C anticipated as the upper limit.

Other applications where Charge Coupled Devices fit well is in analog delay lines. The magnitude of the charge can be made proportional to the analog signal. Delay is effected by the serial (time consuming) movement of the charge through the device. Fairchild CCD321 is an example of such a device.

A key feature of CCD is that it is very compatible with the standard MOS process allowing for optimum architectural flexibility on the same die. This has broad application in custom LSI for special applications involving analog, digital and correlation functions.

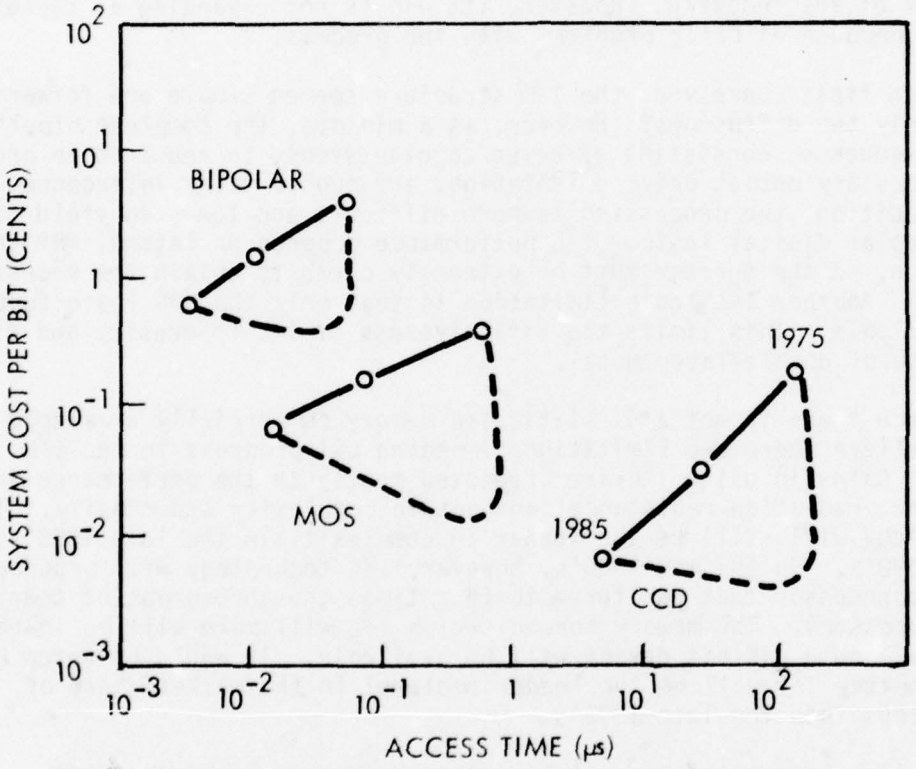


Figure A-8. Relative Cost - Performance Comparison of Microelectronics Memory Technologies

A.7.2 Conclusion

Since CD is tied very closely to the MOS process, improvements in processing realized in NMOS will naturally be implemented in CCD. Because of this, CCD will remain in step with NMOS, both from a technology advancement and producibility viewpoint. CCD will continue to remain ahead of MOS RAMS for memory density. A 1/4 million bit CCD in 1980, and a million bit CCD by 1982 for commercial applications is highly probable. Military applications, if at all ossible, will evolve five to seven years later.

A.8 Integrated Injection Logic (I^2L)

This relatively new technology, which was invented almost simultaneously in 1970 by Philips and IBM-Germany, is heavily supported by the commercial segment of the industry. However, its use is not expanding as rapidly as forecast because of basic problems with the process.

When first conceived, the I^2L structure seemed simple and forward, requiring only two diffusions. However, as a minimum, the complete bipolar processing sequence, consisting of seven to nine steps, is required to provide the necessary output drives, isolation, and double-metal interconnection. In addition, the processing is more difficult and lower in yield than standard bipolar digital logic. I^2L performance depends on lateral PNP transistor action, so the surface must be extremely clean to obtain the necessary high betas.) Another I^2L logic limitation is that only the NOR logic function is available. This limits the effectiveness of I^2L in density and dictates the use of double-layer metal.

Since there is not a 4K static I^2L memory commercially available today, we believe there are limitations impeding LSI progress in the I^2L technology. Gains in using I^2L are predicted mostly in the performance area (speed, power, radiation resistance) and not in complexity and density. The NMOS technology will still be the leader in complexity in the late 1980's, and early 1990's. In the mid 1980's, however, I^2L technology will produce a 16-bit microprocessor that has three to four times the throughput of today's I^2L microprocessors. The memory inroads which I^2L will make will be in the dynamic area, and a 64K bit device will be available. It would be noted here that the Schottky T^2L will be the leader (volume) in the market share of bipolar devices into the late 1990's.

Part II. Integrated Circuit Radiation Hardening Considerations

A.9 Military Needs

For NMOS to emerge as the leading commercial technology of the future, is not good news for systems requiring radiation hardness capability. Three forms of radiation are of concern when discussing device vulnerability:

Neutronfluence (in Neutron/Meters^2)

Total Dose (in RAD (Si))

Transient Upset (in RAD/SEC)

Figure A-9 shows the range in which the various technologies fall. In terms of Total Dose and Transient Upset, NMOS is the most susceptible. This is due primarily to the change in gate-threhold levels caused by radiation. As dimensions get smaller, devices will become even more sensitive to nuclear radiation. Therefore, systems requiring RAD/Hardening will be unable to take advantage of the VLSI explosion of the 1980's. Users requiring RAD/Hard Systems will have to rely on T^2L, I^2L, and CMOS/SOS devices. The trade-off will be system sophistication, size/weight and cost against radiation hardness.

Part III. VLSI Device Procurement Specification and Testing

A.10 Test Spectrum

The benefits derived from VLSI are not without penalty. Because of their complexity, such devices present new challenges in device specifications and testing.

The underlying problem in generating specifications is in defining device functional requirements. For example, microprocessor instruction sets a range from 40 to 100 instructions. A microprocessor is expected not only to execute all these instructions, but also to do so in any sequence. To pin down this requirement on a comprehensive basis, the procurement specification would require listing 100^{100} permutations of the instruction set, an unbearably large number.

One approach is simply to state in the procurement doeument that the device shall respond satisfactorily to all permutations of the entire instruction set. This does not define what test shall be performed prior to delivery. In effect, the scope and depth of the suppliers out-going test (on a lot-to-lot basis) is to the discretion of each device manufacturer.

This choice has the distinct disadvantage of requiring each user to expend substantial nonrecurring and recurring funds for testing, and further places the burden of insuring device adequacy on the user. This is a complete reversal of today's approach, which places the economic burden and risk management on the device manufacturer. Where a device is procured from several sources, users an suppliers alike have no common ground upon which to make judgements. As the quantitiy and complexity of devices increases, the need for standardization in specifications and testing becomes more important.

Another approach might be to define a set of test vectors which exercise a reasonable percentage of the gates within the device (85% to 95%) and verify execution of all instructions. This is somewhat of a classical approach to testing devices. However, it is also beset with difficulties. Most device manufacturers are unwilling or (because of computer-aided design) unable to supply users with detailed logic diagrams of the device. The user has no reasonable way of generating an adequate test program, except to use the supplier's program as a stepping stone.

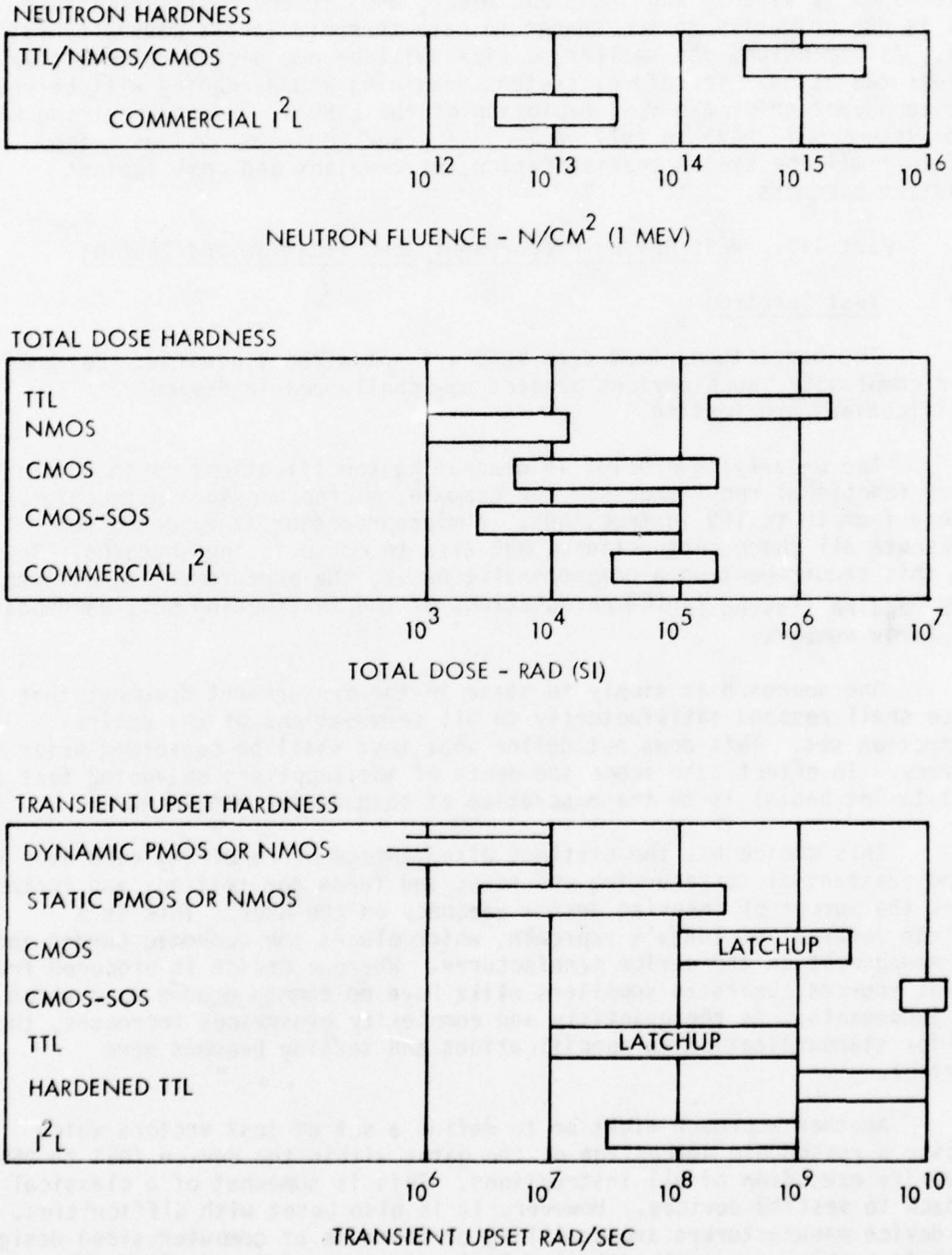


Figure A-9. Radiation Hardness Comparison of Various Microelectronics Technologies

Given that an adequate test vector program can be generated, there are logistic problems related to the actual procurement document generated. For example, the MIL-M-38519 specification sheet for the 8080A microprocessor (MIL-M-38510/420) contains 73 pages of basic electrical parameters and over 500 pages of binary test vectors (12,000 test vectors). Besides forming a very lengthy document, the test vectors are not easily incorporated on a test machine. Much effort may be required to translate such test vectors into an acceptable form for a given test machine. The task is essentially a software programming problem arising from the various computer languages used in the test equipment.

In addition, device level test vectors may not always be compatible for devices which are in face compatible at system level. Again, the 8080A and 9080A microprocessors exemplify this problem. From a systems software viewpoint, either device is usable. The system designer deals at the instruction-set or machine-cycle level. The device test deals with state conditions within a given machine cycle. For certain instructions, state level conditions for the 8080A are slightly different than for the 9080A. This is because the 9080A die is not a mask copy of the 8080A die. Device test vectors for one item do not necessarily perform an effective test for another. Since the trend in complex devices is toward non-mask second sourcing, this condition (state level vs. system level) is likely to worsen.

A.10.1 Conclusion

The more complex devices become (e.g., VLSI), the more difficult it is to generate procurement and test specifications. An important aspect of device testing is in the area of software programming and universal approaches to "software" testing of devices. As devices approach minicomputer and mainframe capabilities, procurement documentation and testing will rely heavily on software programs. Much study is needed in this area to define the problem clearly and develop solutions.

Part IV. Device Packaging

A.11 Introduction

The device package which has gained universal acceptance over the past ten years, is the DIP (Dual In Line Package) (Figure A-10). This package was developed with monolithic microelectronic devices. It became the dominant package configuration because of its rugged construction and versatility. A DIP can be plugged into a connector or reliably soldered directly into a printed wire board. The sturdy leads provided easy handling (manual and automatic) for testing, shipping, and stocking.

For a time, the flatpack (Figure A-10) challenged the supremacy of the DIP. The flatpack saved board area, a distinct advantage over the DIP. Where equipment size and weight were an overriding factor, such as in military and space applications, the flatpack was clearly better. The main

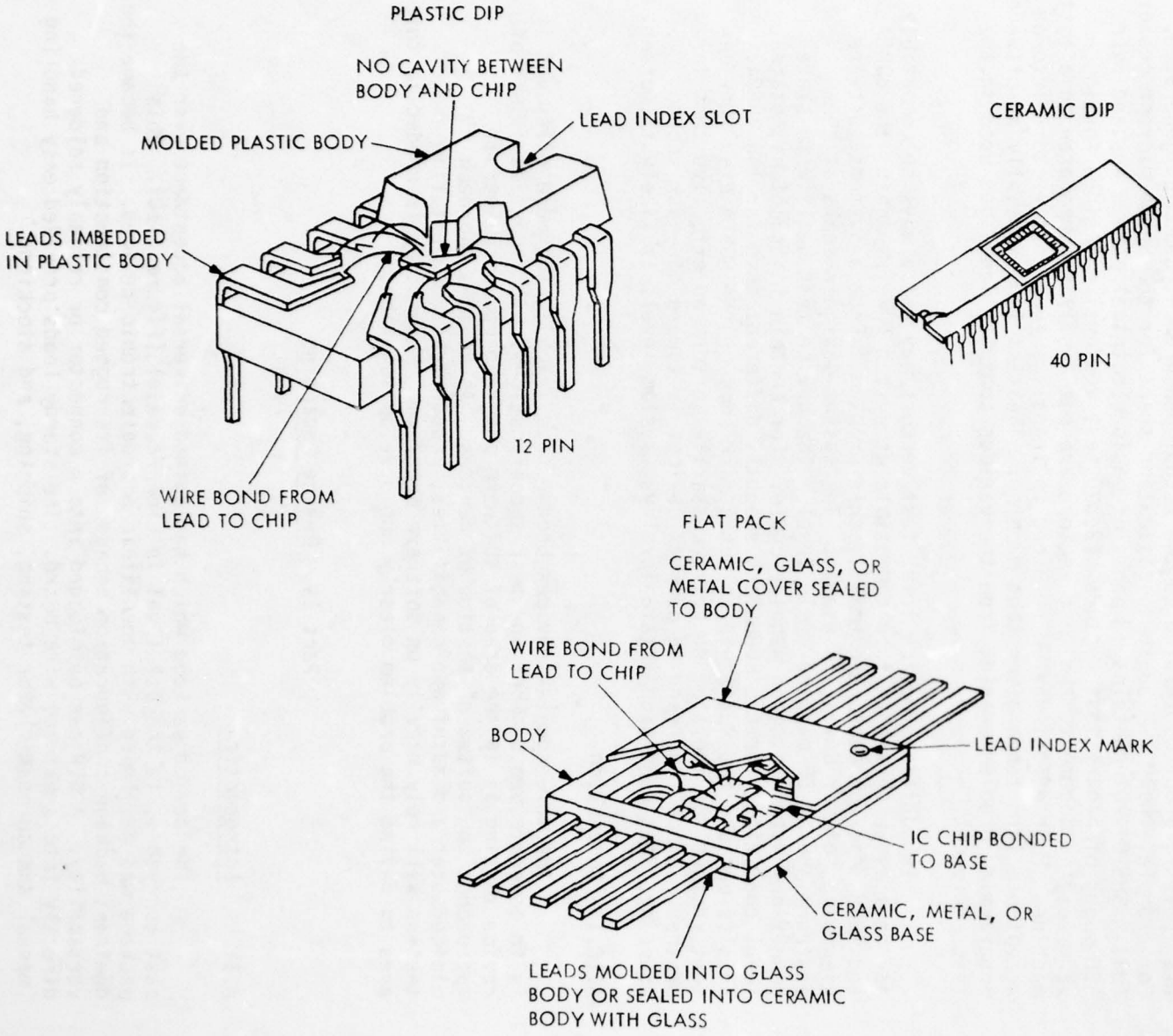


Figure A-10. Dual In-Line (DIP) Package and Flatpack Comparison

disadvantage of the flatpack was fragile leads, which caused difficulty in fabrication and handling, resulting in high assembly costs. Flatpacks cost two to three time more than a DIP.

The reduction in military and space expenditures over the past several years resulted in a considerable decrease in flatpack demand. Because of this, semiconductor manufacturers placed more and more emphasis on the DIP. This in turn encouraged utilizing DIPs for military designs. The end result was a thorough entrenchment of processes and tooling for DIPs throughout the semiconductor industry.

A.12 The LSI Push

The board area inefficiencies associated with the DIP (the die size is only about 16 percent of the package) remained at an acceptable level throughout the evolvement of SSI and MSI devices. The gradual increase in device complexity resulted in only minor increases in DIP size and lead count (14 to 24 pins). The basic package cost increased only slightly. There was little incentive to search for different packaging.

However, with the advent of LSI (microprocessors and peripherals) the number of leads has reached 40 and 64 pins, resulting in extremely large packages. A 64-pin DIP covers an area of 3 1/4 inches. Not only does this unwieldy large package waste area (a typical die is only 1/4 x 1/4 inch), but now package costs increase substantially. For example, according to Texas Instruments, package costs of their 64 pin TMS(()) and SBP9900 could be decreased by a factor of 4 to 1 by packaging in a chip carrier instead of the Dual-In-Line package -- assuming the chip carrier was a broadly accepted package.

A.12.1 LSI Pinout Considerations

LSI in itself is not the overriding reason that more and more pinouts will be required. The 16K memory devices now appearing on the market require only 16 pins. The driving force will be the trend toward placing minicomputer and eventually mainframe computer performance on a single semiconductor die.

To meet this performance, parallel processing of 16, 32, 64 or more bits will be required. The number of bits will dictate how many pinouts are needed. This will apply not only to the microprocessor but to support and peripheral devices as well. Table A-3 shows devices and pinout requirements which have evolved over the past five years. Table A-4 depicts two examples of what is expected to be developed by 1985 and be produced in volume by 1990.

TABLE A-3. DEVICE PINOUT DEVELOPMENTS

1972 -1977

Device Type	Total Pins	Data and Address Pins	Control and Bias	NC
2901 4 Bit Slice	40	24 (8 Data, 15 Address)	6	-
8 Bit Microprocessor (8080, Z80)	40	24 (8 Data, 16 Address)	16	-
8 Bit Microcomputer (8048)	40	24	16	-
16 Bit UP (Fairchild 9440)	40	16 (Data and Address Multiplexed)	24	-
16 Bit UP (TI SBP9900)	64	32 (16 Data, 16 Address)	24 (GNDS)	5
(TI TMS9900)	64	32 (16 Data, 16 Address)	26 (4 Clocks) (3 Voltages)	7
16 Bit Multiply (TRW MPY 16)	64	48 (3, 16 Bit Lines)	16 (4VCC) (5 GND)	-

TABLE A-4. PROJECTED DEVICE PINOUTS

1985 - 1990

Device Type	Total Pins	Data and Address Pins	Control and Bias
32 Bit UP	80	56 (32 Data, 24 Address)	24
32 Bit Multiply	120	96 (3, 32 Bit Lines)	24

With future LSI devices expected to have more than 100 pins, packaging has become an important consideration. Package manufacturers, semiconductor manufacturers and equipment manufacturers now have renewed interest in device packaging.

A.13 Future Packaging Concepts

Figure A-11 illustrates package schemes presently available. Which of these emerge as the standard package of the future, depends on several factors.

- Overcoming the existing inertia associated with the DIP.
- Cost
- Ruggedness in terms of handling for device testing, stocking, shipping, and assembly installation.
- Ease of solderability (oir other reliable "hardwire" connecting) to a printed wire board/substrate assembly.
- Option to insert/remove via a connector where hardwiring is undesirable.
- Thermal properties.
- Efficient use of assembly level interconnection board area.

These factors are considered in the following discussions addressing the package schemes illustrated in Figure A-11. Table A-5 summarizes these discussions.

A.13.1 Leadless Dip, (See Figure A-11(A))

The only advantage of this package over the standard DIP package is that the cost is reduced by eliminating brazing of leads and by the cost of the leads themselves. However, the inefficient use of board area and the fragility of such a package as it becomes larger, with more and more pin outs, makes it an unlikely candidate for industry standardization.

A.13.2 Beam-Tape Encapsulated, (See Figure A-11(B))

The beam tape is gaining acceptability for attaching a die to a given package, such as a DIP. The process allows for highly automated die-attach, and will no doubt be used for high-volume production to attach dies into whatever package emerges as a standard.

An alternate proposed final packaging scheme uses the beam-tape process to encapsulate the die and inner lead, leaving the exposed outer leads as the final package configuration. Thus, package costs are elminated and board area usage is optimized. In this approach, the die seal is questionable,

LEADLESS DIP

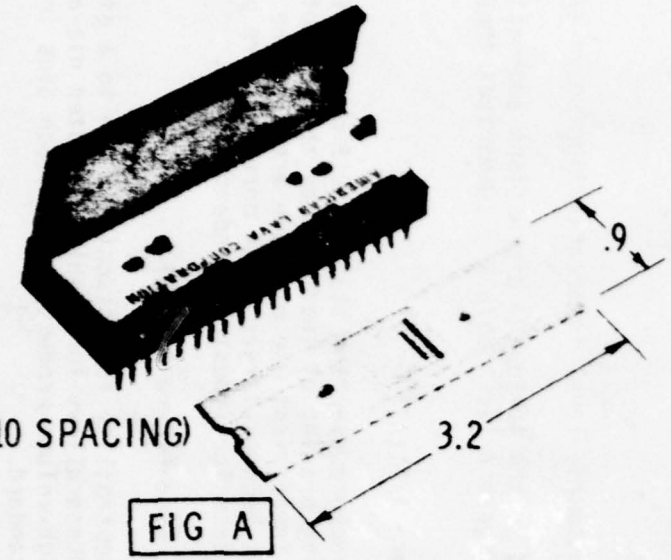
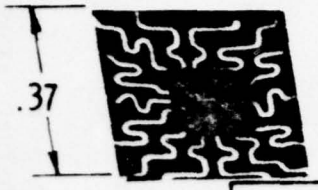


FIG A

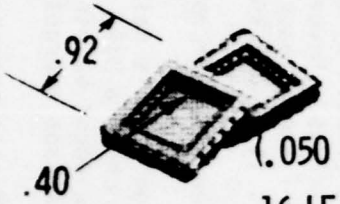
BEAM TAPE ENCAPSULATED



LEAD SPACING
.025
16 LEADS PER SIDE

FIG B

LEADLESS CHIP CARRIER



(.050 LEAD SPACING)
16 LEADS PER SIDE

FIG C

LEADED CHIP CARRIER
OR FLAT PACK (64 PIN)

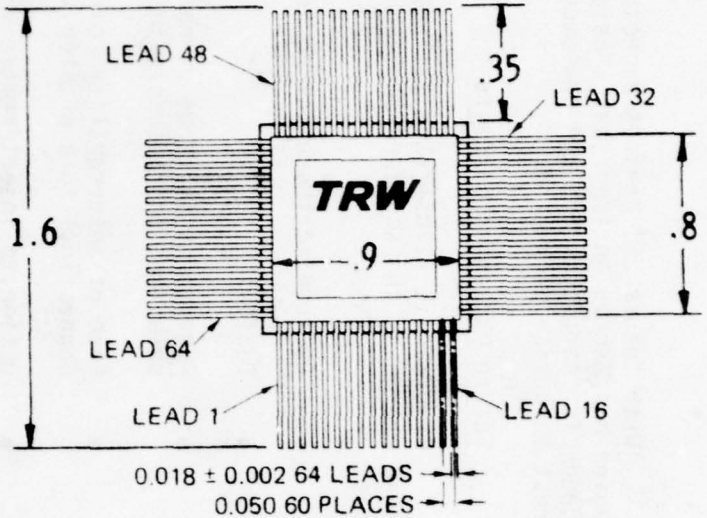


FIG D

Figure A-11. Integrated Circuit Device Packaging Schemes

Table A-5. Integrated Circuit Package Comparisons

Monolithic Die (Chip) Packaging Alternatives	Disadvantages	Advantages
Leadless chip carrier	• Solder joint stress due to board expansion	Excellent packing density Durable Easy handling
	• Solder-reliability, producibility repairability unknown?	Pluggable Package price low
Flatpack or leaded chip carrier	• Difficult handling for, testing shipping, assembling	Package (excluding leads) More durable than large DIP
	• Not optimum size	Better packing density than
	• Lead forming (for leaded CC)	DIP
	• Poor pluggability	Package price lower than DIP (large packages)
DIP	• Package size and durability (length) fragile ceramic	Pluggable
	• High cost	
Beam tape (encapsulated) or solder bump	• Die seal	Optimum packing density
	• Heat removal from chip	
	• Handling	
	• Poor pluggability	
	• Pin spacing	

although recent experiments using a polyimed-siloxane encapsulant may improve seal properties. A significant disadvantage is the poor heat transfer of the encapsulated package. A device die not being mounted directly to a ceramic substrate will severly limit the operating temperature of the device. Since the final package is not a rigid construction, handling will be difficult. The option for inserting via a connector is also unavailable.

Because of these disadvantages, it is unlikely that a beam-tape encapsulated device will emerge as the industry package standard.

A.13.3 Leadless Chip Carrier, (See Figure A-11 (A))

Of the packages discussed so far, the chip carrier appears as the most likely candidate for industry-wide acceptance. It is a rugged package (even more rugged than the DIP, since it has no leads protruding). It minimizes board area used, has good thermal properties (thermal resistivity, θ_{JC}, is about the same has an equivalent DIP) and its inherent cost is lower than a DIP.

According to a device manufacturer who has supplied over 10,000 devices in chip-carrier form, the present chip-carrier devices cost 20 percent more than their standard DIP. However, a portion of this cost may be ascribed to the special effort required to process a chip carrier in a facility geared for DIPs. As noted previously, one device supplier indicated that the price of a 64 pin chip-carrier is one quarter of the price of the DIP.

Another plus factor, for the chip carrier is its ability (like the DIP) to be made with chip connectors, allowing easy insertion and removal. The chip carrier may also be soldered into an assembly. This is an area where the carrier has difficulty competing with the DIP. The DIP can readily be soldered to existing printed wiring boards. The leadless chip carrier cannot.

Chip carriers can also be obtained with leads (leaded carrier). The basic package cost is then three times higher than the leadless. Handling and assembly are also more difficult. A leaded chip carrier is essentially a flatpack.

A.13.4 Chip Carrier: Method of Attachment

The leadless chip carrier is mounted to a motherboard by reflowing solder at the junction of the motherboard contact and the carrier contact. The solder fillet thus formed mechanically holds the package to the board.

Two problems arise when attempting to apply this method to the standard glass epoxy printed wire board now in wide use. First the different coefficients of expansion between the board material and the chip carrier (ceramic) result in serious stresses on the solder joints.

The second problem is that in order to "reflow" solder, the mother-board (and the chip carriers) must be placed in a temperature of 350°F (177°C) to 400°F (204°C). This cannot be done on glass epoxy multilayer boards because of expansion problems within the board.

Both of these problems can be overcome by mounting the carrier on a ceramic substrate. The carrier and the substrate have the same expansion rates, and no stress will be placed on the solder joints. Figure A-12 is an example of how chip carriers might be mounted on a substrate in the form of a DIP. It is unlikely, however that this type of mounting will gain wide support. The user would have to first assemble the carriers on the DIP and then assemble the DIP to a printed wire board. The preferred method would be to solder directly to a printed wire board. What might give wide support to the use of chip carriers will be the diminishing use of glass epoxy boards and the introduction of polyimide multilayer boards. These boards, expected to be available within two years, at a cost only 10 percent higher than present boards, have better thermal expansion properties in the "thickness" (Z) direction than glass epoxy. This will allow raising the board temperature up to solder reflow temperature (400°F/204°C) without stressing the board. However, expansion in the flat direction (X,Y) remains a questionable area regarding stress on the solder joints. Pactel Corp. claims chip carriers have been successfully soldered to glass layered polyimide boards. More confidence is needed in this area.

A.13.5 Reflow Solder and Chip Carriers

There is, of course , some reservation regarding the reliability of reflow solder joints. Acceptability of chip carriers is tied directly to this process. Some of the questions which need answering are:

1. Can reliable solder joints be consistently producing in high volume production?

2. How can repairs be accomplished, reflow again?

It appears some manufacturers have been successful in utilizing chip carriers and solder reflow. At least one commercial manufacturer is reported as having used over four million chip carriers with good results.

A.13.6 Thermal Density

Another problem associated with use of chip carriers is the amount of heat a typical board configuration may generate. Since carriers do allow high packing density of devices, heat removal may be a problem. For example, as cited by one manufacturer, the theoretical junction temperatures of a typical LSI configuration of 25 chip carriers, mounted on a ceramic substrate six inches by two inches, would be approximately 115°C in a still ambient air environment of 70°C.

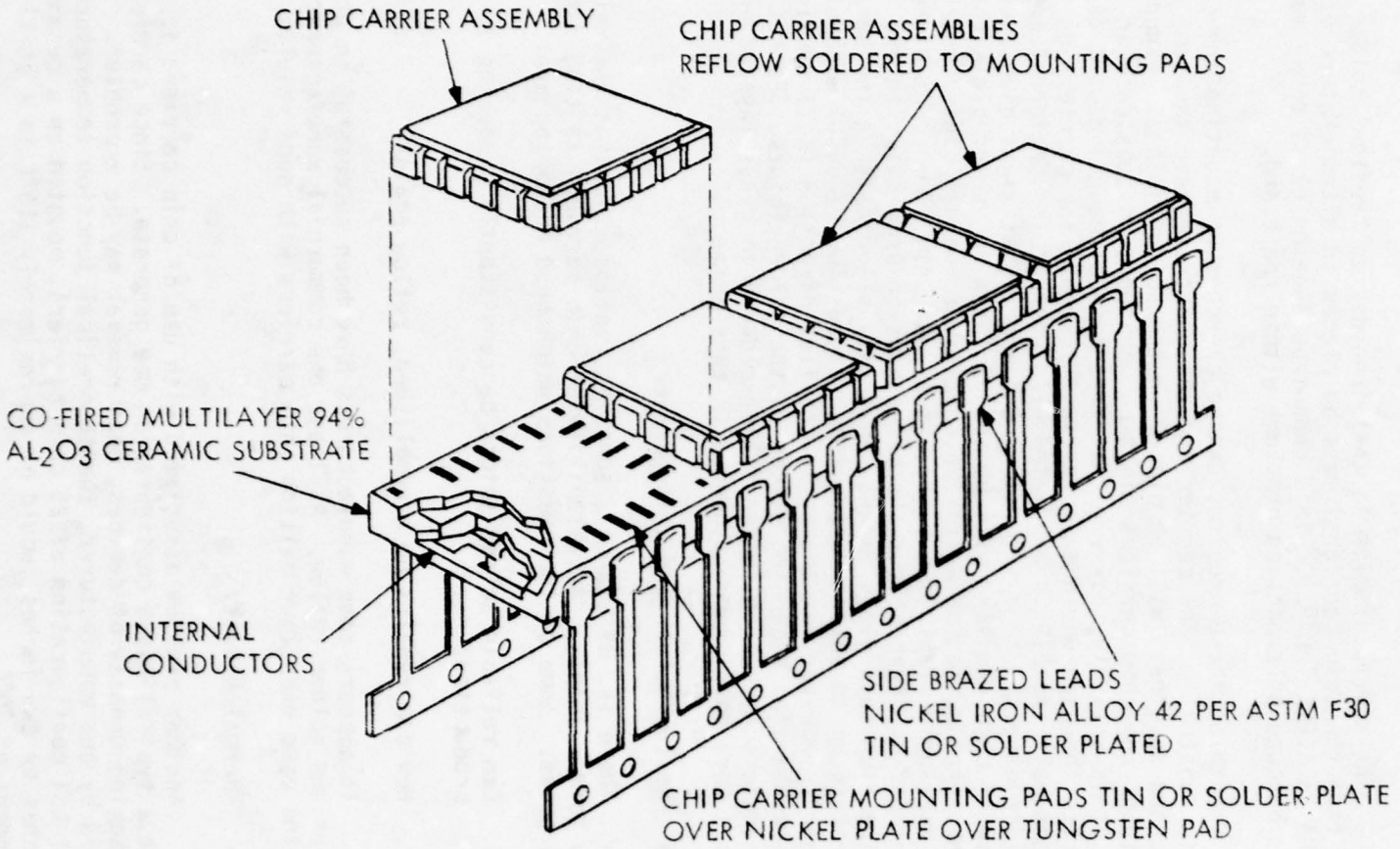


Figure A-12. Dual In-Line Motherboard (DIM) for Interconnecting from 24-Lead Chip Carriers

A.13.7 Conclusion: The Chip Carrier - The Future Industry Standard

There is no doubt that use of chip carriers is picking up momentum. Table A-6 summarizes recent activity. Of ten major device suppliers surveyed, four had delivered some product in chip-carrier form. This ranged from 500 devices up to 100,000 devices. All were special orders requiring special tooling. Most were for commercial applications. One commerical equipment manufacturer of paging radios has installed die in over four million chip carriers, filled in the cavity and mounted on a substrate with other devices.

A JEDC panel has been formed to establish standard pin configurations for chip carriers. Two standards are being proposed: A 0.050-inch lead center and 0.040-inch lead center as shown in Table A-7.

TABLE A-6. SUMMARY OF LEADLESS CHIP CARRIER ACTIVITY

- 3M and kyocera supply packages (semi alloys supplies connectors)
- Mostek over 10,000 4K dynamic RAMS, over 1,000 16K dynamic (18 pin, 0.050 lead centers)
- AMD 100,000 linear devices for telecomm
- Hughes ----- 500 in 36 lead, special order
- Motorola (equip.) ----- 4 to 5 million devices for electronic pager
- T.I. - SEM mockup (2A modules with SBP9900) Also chip carrier outline in proposed MIL-M-38510/235A
- GE/HMED E-task 20,000 devices (400 SEM modules)
- JEDEC panel

Related Activities

- Polymide boards - sanders, McDonald Douglas, Pactel/General Dynamics
- Computerized model thermal study - NAFI/GE (Elec. Labs)

TABLE A-7. PROPOSED CHIP CARRIER LEAD SPACING

Commercial Standard 0.050-Inch Lead Spacing

No. of Pins	Size
28	0.450 inch on a side
44	0.650
52	0.750
68	0.950
84	1.150
156	2.050

Military High Density Application

Standard -- 0.040 Lead Spacing

No. of Pins	Size
40	0.480
48	0.560
64	0.720
80	0.880
96	1.040

Package manufacturers have indicated problems in producing chip carriers in excess of 1.25 inch on a side. However, the progress of the JEDEC panel in delineating (and hopefully, soon approving) standard pin configuratins is supportive evidence that carriers are coming in to vogue. Although 0.040 inch spacing is being proposed as standard for military use, it is unlikely that these carriers will be readily available. The trend in the high volume commercial market is toward 0.050 inch spacing.

Further evidence that chip carriers are catching on is that device manufacturers are beginning to advertise them. Mostek indicates they have delivered 4K and some 16K dynamic RAMs in chip carriers. Texas Instruments has included a chip carrier dimension in their proposed MIL-M-38510/235A slash sheet to RADC. Mostek has also established prices on their memories in

chip carrier form. The driving force in determining when chip carriers will evolve as the industry standard is customer demand. This is, of course, a two-way street. Quotations received from vendors are sometimes so high for packages other than DIPs, that a customer necessarily ends up "demanding" the DIP. It becomes a question of who does what first. Table A-8 summarizes problems (and proposed actions) which are inhibiting the demand for chip carriers.

TABLE A-8. CHIP CARRIER PROBLEMS

- Reliability, producibility, and repairability of the solder reflow process.

  Need a rigorous feasibility study to determine environmental affects.

- Stress on solder joints due to X, Y thermal expansion of PW boards (epoxy or polymide).

  Determine severity of problem on various forms of polymide boards (copper-clad, glass-clad, etc.).

- Thermal stress on devices due to assembly packing density.

  Thermal evaluatin study with actual LSI devices mounted on ceramic and polymide boards.

- Establishment of standard sizes and pin spacing 0.050 inch lead vs. 0.040 inch pin spacing.

  Support JEDEC activities.

- Market acceptability (overcome dip inertia).

  Disseminate study results to industry.

- Capital investment to tool up for chip carrier.

  Develop market demand and provide seed money.

Tooling for a new package requires substantial investment and risk on the part of a vendor. According to one leading semiconductor supplier, bringing up a full-blown automated facility to process and test devices in chip-carrier form would require about two million dollars. Not many vendors are inclined to take that risk at this time.

However, the ever-present pressure from LSI, causing larger-than-reasonable DIP packages, and the evolving of ceramic substrate techologies and processes which are compatible with chip carriers, are clear evidence that chip carriers will begin to challenge the supremacy of DIPs by

1985. They should become the industry standard packaging by 1990. Existing blank pricing is another motivating factor. Table A-9 shows that chip carrier basic package cost is four times less than an equivalent ceramic DIP.

TABLE A-9. 3M CERAMIC PACKAGE PRICES
(100,000 QUANTITY)

	Dip	Leadless C.C.	Leaded C.C.
16 pin	$ .70	$ .21	2 1/2 X
24 pin	1.15	.55	2 1/2 X
40 pin	1.48	.73	2 1/2 X
64 pin	4.24	(approx.) 1.10 (3M not firmed up)	

Chip carrier final device pricing in the 19085 time frame will probably be slightly higher than DIPs because suppliers will be attempting to recover investment costs. By 1990, however, the cost of a chip-carrrier device will be well below the equivalent DIP.

This integrated circuit technology assessment has shown, from a conservative viewpoint, that by 1980 the commercial market will be ready to supply commercial grade 65K dynamic RAMs, 16K static RAMs, and single chip 16-bit minicomputers. By 1982, these devices will have matured such that de facto standards will have evolved for side-spread implementation in commercial, industry, and military equipment. These devices will be fabricated utilizing the upper limit of existing optical process techniques.

Through the use of mature E-beam and X-ray processing, Very Large Scale Integrated devices will begin to emerge in the mid 1980's. By 1985, the commercial market will begin to supply commercial grade million-bit memories and single-chip 32-bit minicomputers with a quarter-million bits of memory on chip. Again, from, a conservative viewpoint, these devices will reach maturity within two years (1987) and will then be widely used.

This conservative viewpoint is based on the maximum life utilization of existing optical fabrication machinery and processes, with a moderate phasing in of E-beam and X-ray technologies in 1980. A more liberal opinion based on Japan's technology goals, holds that E-beam processing will come sooner, and million-bit memories will be available in 1980. This assumes that the process will have matured enough to mass-produce such devices economically. It seems unlikely that E-beam technology will mature that rapidly. Device fabrication contains many subtle unknowns which in the past have caused failure of devices promised from the matured U.S. semiconductor industry.

The leading technology in which VLSI devices will be fabricated, will be the high density, low power, inexpensive NMOS technology. These devices will provide greater functional density, yet remain in the 500 to 800 mW power range. Other technologies such as bipolar, I^2L, CMOS/SOS will trail behind, but will find their own special applications.

The introduction of 32-bit minicomputers and associated peripherals will require new methods in procurement specifications, especially where testing of devices is defined and implemented. The trend will be toward "software" specification and test programs.

The 32-bit word length devices will drive pin-counts upward, such that today's standard DIP (Dual in-Line Package) will be replaced by the more efficient chip carrier. By 1990, 32-bit minicomputers equivalent to an IBM 360, packaged in 80-pin chip carriers, and dissipating only one-half watt of power, will be commonplace.

Part V - Recommendations

Two major areas need furher study: chip carrier assembly techniques, and VLSI procurement specifications and testing.

For chip carrier applications: (1) manufacturing feasibility studies to determine method of mounting, printed wire board compatibility, and general producibility should be initiated and completed in 1978. (2) A study to define problems and propose solutions for VLSI procurement and testing should be initiated and completed by 1980.

APPENDIX B

(Reprint)

EVALUATION OF LSI/MSI RELIABILITY MODELS

George Kasouf
and
Steven Mercurio

SI-721

A Paper Presented at

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General Electric Company
Aircraft Equipment Division
Utica, New York 13503

Evaluation of LSI/MSI Reliability Models

George Kasouf Steven Mercurio

Key Words: LSI/MSI Failure Rates, LSI/MSI Prediction, MIL-HDBK-217B, Mathematical Reliability Model, LSI/MSI Reliability.

Abstract

A reliability model, adaptable to both MOS and TTL LSI/MSI circuits, is developed. Over 24 million device operating hours of certified data, accumulated during the test-analyze-and-fix/reliability demonstration test of an airborne radar processing system and the accelerated life test of 4K MOS static RAMs, is used to evaluate the authors' reliability model and the LSI/MSI reliability models of MIL-HDBK-217B.

Introduction

To predict the reliability of an airborne radar processing system (RPS) during the early portion of the program definition phase, it was necessary to determine the failure rates of large and medium scale integrated (LSI/MSI) circuits. However, for LSI/MSI circuits, whose technology was state-of-the-art in 1972, empirical failure rates had not been established. In order to predict analytically the reliability of LSI/MSI circuits, various reliability models available at that time (early 1972) were investigated. The most useful models were described in "MOS Reliability Prediction Model" by M.F. Adams and D.M. Aaron (Ref. 1) and "Predicted Failure Rates of Yield Enhanced LSI" by W.G. Tees (Ref. 2). Both papers used mathematical techniques to obtain reliability models for integrated circuits (ICs). Tees developed a model for yield enhanced LSI circuits. Adams and Aaron developed a model for metal oxide semiconductor (MOS) circuits.

Using General Electric Aerospace Electronic Systems Department (GE/AESD) failure rate data, Tees' mathematical model and results obtained by Adams and Aaron, a LSI/MSI reliability model, adaptable to both MOS and transistor-transistor-logic (TTL) circuits, is developed. Failure rate predictions, derived using the authors' model, correlate with observed failure rate data.

Mathematical Model

The mathematical model defined by Tees for calculating the failure rates of LSI circuits is given by:

$$\lambda_{LSI} = 0.041313 + (0.000666)P + (0.000103)G \quad (1)$$

where

λ_{LSI} = LSI failure rate/10^6 hours

P = number of pins

G = number of gates

An SSI triple three-input NAND gate reference failure rate of 0.0294×10^{-6} is used to develop the weighted fractional failure rates of Eq. 1. The reference failure rate is a predicted value, using proposed MIL-HDBK-217B (April 1970); assuming an ambient temperature of 50°C operating in a space flight environment with Class A screening.

GE/AESD field data available in 1972 indicated an observed SSI failure rate given by:

$$\lambda_{SSI} = 0.0528 \times 10^{-6} \quad (2)$$

The data base for the observed SSI failure rate is 872 million device operating hours in an airborne inhabited environment with 46 confirmed failures. The SSI ICs were screened to MIL-STD-883 Class B and operated at an average 75°C junction temperature. This data base is considered a representative sample of SSI circuits used in military electronic equipment from late 1966 through 1971.

To make use of Tees' LSI weighted fractional failure rates, Tees' mathematical model is modified to reflect an airborne inhabited environment, MIL-STD-883 Class B screening, and an average 75°C junction temperature. Modification consists of replacing the predicted SSI triple three-input NAND gate reference failure rate of 0.0294×10^{-6} with the GE/AESD observed SSI failure rate of 0.058×10^{-6}.

Tees' LSI weighted fractional failure rates were derived exclusively from TTL data. However, Adams and Aaron concluded that MOS devices are 55 percent more reliable than TTL devices of equal complexity. Consequently, Tees' mathematical model is assumed applicable to both MOS and TTL LSI/MSI circuits. This assumption is further substantiated by L.C. Hamiter, Jr. in "How reliable are MOS IC's? As good as bipolars, says NASA" (Ref. 3).

Therefore, the authors' basic reliability model used for the preliminary RPS predictions for MOS and TTL LSI/MSI circuits is given by:

$$\lambda_{LSI/MSI} = 0.074185 + (0.001195)P + (0.000185)G \quad (3)$$

where $\lambda_{LSI/MSI}$ is failure rate of MOS and TTL LSI/MSI circuits for assigned pin (P) and gate (G) values, operated in an airborne inhabited environment at an average 75°C junction temperature and screened to MIL-STD-883 Class B.

MIL-HDBK-271B

A reliability prediction, obtained by the use of the LSI/MSI reliability models defined in the review copies of MIL-HDBK-217B (circulated in November 1972), yielded failure rates several orders of magnitude greater than those obtained from the authors' basic LSI/MSI reliability model developed for the RPS. Comments were submitted to RADC by GE and other LSI/MSI users expressing concern over the design restrictions imposed by the pessimistic MIL-HDBK-217B LSI/MSI models. The comments resulted in revisions that relieved some of the restrictions.

MIL-HDBK-217B (Ref. 4) was released for use in September 1974. An RPS MTBF prediction obtained using the LSI/MSI reliability models in MIL-HDBK-217B was less than the RPS MTBF prediction on which specification commitments were based. However, the MTBF observed for the RPS flight test models during Phase II of the program greatly exceeded the MTBF predicted using the MIL-HDBK-217B reliability models. This information supported the authors' basic LSI/MSI reliability model developed for the RPS. For use in the final RPS reliability prediction, the authors' basic LSI/MSI reliability model of Eq. 3 required expansion

in order to reflect LSI/MSI failure rate variation as a function of junction temperature.

Authors' Complete LSI/MSI Reliability Model

π_{T_m} vs Junction Temperature

The success of the LSI/MSI reliability model of Eq. 3 in the RPS preliminary prediction indicates that the thermal degradation penalty imposed by MIL-HDBK-217B on MOS ICs is too extreme. The thermal function defined by MIL-HDBK-217B is modified to reflect the value of unity used in the derivation of the LSI/MSI reliability model for MOS and TTL LSI/MSI circuits operated at an average 75°C junction temperature.

The thermal function of MIL-HDBK-217B (Section 2.1.5) is given by:

$$\pi_T = (0.1)\ \exp\left[K\left(\frac{1}{298} - \frac{1}{T_J + 273}\right)\right] \quad (4)$$

$$K = \begin{vmatrix} 4794 \text{ for TTL} \\ 8121 \text{ for MOS} \end{vmatrix} \quad (5)$$

The modified thermal function of MIL-HDBK-217B, which represents unity for both MOS and TTL circuitry at $T_J = 75°C$ as used in the derivation of the LSI/MSI reliability model of Eq. 3, is given by:

$$\pi_{T_m} = \exp\left[K\left(\frac{1}{348} - \frac{1}{T_J + 273}\right)\right] \quad (6)$$

$$K = \begin{vmatrix} 4794 \text{ for TTL} \\ 8121 \text{ for MOS} \end{vmatrix} \quad (7)$$

The authors' thermal degradation values π_{T_m} for junction temperatures between 25°C and 175°C are found in Table 1.

TABLE 1. π_{T_m} vs JUNCTION TEMPERATURE

T_J (°C)	π_{T_1}	π_{T_2}	T_J (°C)	π_{T_1}	π_{T_2}
25	0.10	0.02	75	1.0	1.0
27	0.11	0.02	77	1.1	1.1
29	0.12	0.03	79	1.2	1.3
31	0.14	0.04	81	1.3	1.5
33	0.15	0.05	83	1.4	1.7
35	0.17	0.05	85	1.5	1.9
37	0.18	0.06	87	1.6	2.2
39	0.20	0.07	89	1.7	2.5
41	0.23	0.08	91	1.8	2.8
43	0.25	0.09	93	2.0	3.2
45	0.27	0.11	95	2.1	3.6
47	0.30	0.13	97	2.3	4.0
49	0.33	0.15	99	2.5	4.5
51	0.36	0.18	101	2.6	5.1
53	0.39	0.21	103	2.8	5.7
55	0.43	0.24	105	3.0	6.4
57	0.48	0.28	110	3.6	8.4
59	0.52	0.32	115	4.2	11.1
61	0.56	0.38	120	4.9	15.0
63	0.61	0.43	125	5.7	19.0
65	0.67	0.50	135	7.7	31.0
67	0.72	0.58	145	10.1	50.0
69	0.79	0.66	155	13.3	78.4
71	0.86	0.76	165	17.1	122.0
73	0.93	0.87	175	22.0	183.0

π_{T_1} is applicable to bipolar digital devices, i.e., TTL and DTL

$$\pi_{T_1} = \exp\left|4794\left(\frac{1}{348} - \frac{1}{T_J + 273}\right)\right|$$

π_{T_2} is applicable to linear and MOS devices, bipolar beam lead and ECL

$$\pi_{T_2} = \exp\left|8121\left(\frac{1}{348} - \frac{1}{T_J + 273}\right)\right|$$

A comparison of the authors' thermal function of Table 1 and the MIL-HDBK-217B thermal function of Table 2.1.5-4 reveals the following:

- For TTL circuits, the authors' thermal function and the MIL-HDBK-217B thermal function are approximately equal for all values of $T_J = 25°C$ through 175°C.
- For MOS circuits, the MIL-HDBK-217B thermal degradation function is five times greater than the authors' thermal degradation function for all values of $T_J = 25°C$ through 175°C.
- The thermal degradation of MOS circuits is approximately one-half that of TTL circuits at 50°C junction temperature, correlating with the findings of Adams and Aaron.

The authors' thermal junction is plotted on semi-log paper in Figure 1.

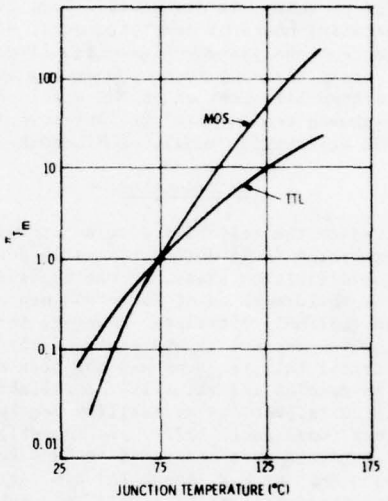


Figure 1. π_{T_m} vs Junction Temperature

Environment Factor, π_E, and Quality Factor, π_Q

The authors' basic LSI/MSI reliability model of Eq. 3 reflects an airborne inhabited environment and MIL-STD-883 Class B screening as a result of the SSI data used in the model's derivation. The environment and quality factors, given in MIL-HDBK-217B Tables 2.1.5.3 and 2.1.5.1, respectively, can be used in their original form if the weighted fractional failure rates of the authors' basic LSI/MSI reliability model are modified accordingly.

Learning Factor, π_L

The learning factor defined by MIL-HDBK-217B has the value 10 for new devices in initial production and for old devices where major changes in design or process have occurred. Otherwise, π_L is equal to one. Equipment specification encourages the use of state-of-the-art LSI/MSI circuits, but the learning factor penalizes their use. The authors have found that reliability engineering practices and process control in use today in the integrated circuit industry have deleted the requirement for π_L.

The basis for this reasoning is as follows:

- Appropriate screening will detect defects in new as well as established circuits.
- A dual 1024-bit MOS shift register (S/R) developed exclusively for use in the RPS by Hughes did not exhibit the learning factor phenomenon. There are 1130 S/Rs in each RPS system, over 26 percent of the total RPS LSI/MSI circuits.

- A 4K MOS static RAM, developed by AMD and used in a GE-designed equipment, did not exhibit a magnitude increase in failure rate, but demonstrated, during a 207,000 hour accelerated life test, a failure rate over two magnitudes less than the failure rate predicted using the LSI/MSI reliability models of MIL-HDBK-217B.
- The integrated circuit industry has regimented new IC design over the past decade. This regimentation dictates similar IC screening and process control for new as well as established product lines. The learning factor, π_L, of yesterday is now obsolete.

Therefore, the authors' complete LSI/MSI reliability model, adaptable to both MOS and TTL LSI/MSI circuits, is given by:

$$\lambda_{LSI/MSI} = \left[0.00370925 + (0.00005976)P + (0.00000925)G\right]\pi_{T_m}\pi_Q\pi_E \qquad (8)$$

where

$\lambda_{LSI/MSI}$ = LSI/MSI failure rate/10^6 hours

P = number of pins

G = number of gates

$\pi_{T_m} = \exp\left[K\left(\frac{1}{348} - \frac{1}{T_J + 273}\right)\right]$; Table 1.

$K = \begin{vmatrix} 4794 \text{ for TTL} \\ 8121 \text{ for MOS} \end{vmatrix}$

π_E from MIL-HDBK-217B Table 2.1.5.3

π_Q from MIL-HDBK-217B Table 2.1.5.1

LSI/MSI Predicted Failure Rate versus Observed Failure Rate

Certified data from an RPS system operating in a simulated airborne inhabited environment is used to calculate the observed LSI/MSI failure rate. The certified data was accumulated during the RPS 1600-hour test-analyze-and-fix program followed by a 351-hour fixed length reliability demonstration test. Analysis of the test data shows an accumulation of 3.9 and 4.6 million operating hours for LSI and MSI circuits, respectively. One LSI and no MSI failures were experienced.

The observed LSI/MSI failure rate is given by:

$$\lambda_{LSI/MSI} = \frac{1}{8.5 \times 10^6} = 0.118/10^6 \text{ hours} \qquad (9)$$

Table 2 compares the LSI/MSI observed failure rate with the predicted failure rates obtained from the authors' and MIL-HDBK-217B reliability models. The authors' and MIL-HDBK-217B predicted failure rates are derived in Appendix A.

TABLE 2. OBSERVED vs PREDICTED LSI/MSI FAILURE RATES
(Failure Rates in Failures per Million Hours)

	Confidence Level		Reliability Model	
Observed	60% Lower	60% Upper	Authors	MIL-HDBK-217B
0.118	0.026	0.352	0.188	1.530

Two points of interest are reflected by Table 2:

- The LSI/MSI observed failure rate and the authors' predicted failure rate are essentially in agreement, while the MIL-HDBK-217B predicted failure rate is an order of magnitude greater than the observed failure rate.
- The authors' predicted failure rate rests comfortably between the 60% lower and 60% upper confidence limits.

Additional Supporting Data

An accelerated life test of 100 4K MOS static RAMs, operated at an average 155°C junction temperature, provides additional data with which to compare the authors' and MIL-HDBK-217B reliability models. Three quarters of the RAMs were screened to Class B-2 and the other quarter of the RAMs was screened to Class C. Seven failures occurred during the accumulation of 207,000 device operating hours.

The observed 4K MOS static RAM failure rate is given by:

$$\lambda_{LSI/MSI} = \frac{7}{207{,}000} = 33.8/10^6 \text{ hours} \qquad (10)$$

Table 3 compares the 4K MOS static RAM observed failure rate with the predicted rates obtained from the authors' and MIL-HDBK-217B reliability models.

TABLE 3. OBSERVED vs PREDICTED 4K MOS STATIC RAM FAILURE RATES
(Failure Rates in Failures per Million Hours)

	Confidence Level		Reliability Model	
Observed	60% Lower	60% Upper	Authors	MIL-HDBK-217B
33.8	22.9	49.5	46.9	15,900

Three points of interest are reflected by Table 3:

- The LSI/MSI observed failure rate and the authors' predicted failure rate are essentially in agreement, while the MIL-HDBK-217B predicted failure rate is over two magnitudes
- The authors' predicted failure rate lies within the 60% confidence interval.
- The authors' predicted failure rate and the observed failure rate show a high degree of correlation at upper temperature limits.

RPS System Level Analysis Using MIL-HDBK-217B and the Authors' LSI/MSI Reliability Model

The complete LSI/MSI reliability model of Eq. 8 was used to predict the LSI/MSI failure rates for the RPS final reliability prediction. A final MTBF of 275 hours was predicted for the entire 19,400 part RPS system.

Selected samples of ICs from an RPS system were used to determine the RPS mean LSI/MSI failure rates. Calculation of the RPS mean LSI/MSI failure rates by selected sampling yields the desired results without resorting to detailed piece part predictions. The sample selection is based on high usage ICs shown in Tables A-1 and A-2. Table 4 compares the RPS mean LSI/MSI failure rates predicted by the authors' and MIL-HDBK-217B reliability models.

The increase in the RPS predicted failure rate, resulting from the use of the MIL-HDBK-217B LSI/MSI models instead of the authors' LSI/MSI model, is obtained as follows:

From Table 4:

$$\Delta\lambda = N\lambda_{217B} - N\lambda_{Authors} = (5151 - 667) \times 10^{-6} = 4484 \times 10^{-6} \qquad (11)$$

where $\Delta\lambda$ = increase in RPS predicted failure rate.

The impact upon the predicted RPS MTBF, as a result of the increase in the RPS predicted failure rate, is given by:

$$\text{Predicted RPS MTBF} = \frac{1}{\frac{1}{275} + \Delta\lambda} = 123 \text{ hours} \qquad (12)$$

TABLE 4. RPS MEAN LSI/MSI FAILURE RATE PREDICTIONS
Authors' Model vs MIL-HDBK-217B
(Rates Defined in Parts per Million Hours)

Device	$\lambda_{Authors}$	λ_{217B}	N	$N\lambda_{Authors}$	$N\lambda_{217B}$
LSI	0.255	2.224	1952	498	4341
MSI	0.073	0.349	2320	169	810
LSI/MSI Total				667	5151

Consequently, using the MIL-HDBK-217B LSI/MSI reliability models, instead of the authors' LSI/MSI model, decreases the RPS final reliability prediction by 55 percent.

The RPS reliability demonstration test was a 351-hour fixed-time test. No failures occurred during the test, resulting in a demonstrated MTBF of 275 hours at 72-percent confidence.

Conclusion

The authors' complete LSI/MSI reliability model predicts the observed failure rates of MOS and TTL LSI/MSI circuits more accurately than the reliability models of MIL-HDBK217B. The authors' predicted failure rates lie within the 60-percent confidence interval, while the MIL-HDBK-217B predicted failure rates are orders of magnitude greater than the observed failure rates. The circuit complexity factor and the thermal degradation factor are the quantitative differences between the authors' and MIL-HDBK-217B reliability models. The authors recommend the revision of the LSI/MSI reliability models of MIL-HDBK-217B. The revised models should be updated continuously to reflect both field and test LSI/MSI observed failure rates.

References

1. M. Adams and D. Aaron, "MOS Reliability Prediction Model," Ninth Reliability and Maintainability Conference, July 1970.

2. W.Tees, "Predicting Failure Rates of Yield Enhanced LSI," Computer Design, February 1971.

3. L.C. Hamiter, Jr., "How reliable are MOS IC's? As good as bipolars, says NASA," Electronics, June 1969.

4. MIL-HDBK-217B, Military Standardization Handbook, Reliability Prediction of Electronic Equipment, Sept. 1974.

APPENDIX A

TABLE A-1. SELECTED SAMPLES OF ICs USED TO CALCULATE RPS MEAN LSI FAILURE RATE

Part Description	Gates	Pins	N	T_J (°C)	$\lambda_{217B} \times 10^{-6}$	$\lambda_{Authors} \times 10^{-6}$	$N\lambda_{217B} \times 10^{-6}$	$N\lambda_{Authors} \times 10^{-6}$
Dual 1024-Bit MOS Shift Register	2048	14	1130	66	2.365	0.249	2672.5	280.8
1024 x 1 Bit Static MOS RAM	1125	16	283	57	2.02	0.083	571.7	23.5
1024 x 1 Bit TTL RAM	1125	16	157	72	1.67	0.267	262.2	41.9
2048 (512 x 4) Bit PROM	2048	16	50	102	2.365	1.249	118.3	62.5
1024 (256 x 4) Bit TTL PROM	1024	16	21	87	1.152	0.445	24.2	9.4
			1641				3648.9	417.95

TABLE A-2. SELECTED SAMPLES OF ICs USED TO CALCULATE RPS MEAN MSI FAILURE RATE

Part Description	Gates	Pins	N	T_J (°C)	$\lambda_{217B} \times 10^{-6}$	$\lambda_{Authors} \times 10^{-6}$	$N\lambda_{217B} \times 10^{-6}$	$N\lambda_{Authors} \times 10^{-6}$
Hex D Type F/F	38	16	386	65	0.330	0.067	127.4	25.9
Quad 2 Input MUX	19	16	178	63	0.249	0.060	44.3	10.7
4-Bit Arithmetic Logic Unit	63	24	100	75	0.445	0.105	44.5	10.5
Sync 4-Bit Binary Counter	57	16	98	72	0.430	0.094	42.1	9.1
16-Input Multiplexer	26	24	111	54	0.285	0.046	31.6	5.1
8-Bit Bidirectional S/R	87	24	64	72	0.509	0.107	32.6	6.9
64 (16 x 4) Bit	95	16	27	70	0.515	0.091	13.9	2.5
			964				336.4	70.6

$$\lambda_{LSI/MSI\ (Authors)} = \frac{417.95 + 70.6}{1641 + 964} = \frac{488.55}{2605} = 0.188/10^6 \text{ hours}$$

$$\lambda_{LSI/MSI\ (217B)} = \frac{3648.9 + 336.4}{1641 + 964} = \frac{3985.3}{2605} = 1.53/10^6 \text{ hours}$$

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APPENDIX C

INDUSTRY
LOW AND ZERO INSERTION
FORCE CONNECTORS

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SCOPE

This report assesses present industry capability and future plans for marketing Low Insertion Force or Zero Insertion Force printed wiring board connectors.

NATURE OF SURVEY

Manufacturers showing activity in articles and advertisements in trade journals were included in the survey as well as those with whom General Electric has had experience.

The survey was conducted primarily by telephone interviews, with a request to the manufacturer to forward any pertinent data.

DISCUSSION

Zero Insertion Force Connector

Of the 22 manufacturers included in the survey, only 10 (45%) expressed interest, with three manufacturers having parts tooled and available. Of the three, only AMP has a line with many contact positions in production. The rest seem to be waiting for the packaging industry to indicate a definite need and define the configuration. In many instances, our inquiry stimulated questions from the manufacturer exploring our future use of the connector.

The manufacturers hesitation comes from high cost of tooling for a complex part. Except for Singer/Kearpott's special, there seems to be no interest in a contact spacing of 0.050. The restriction in using a printed wiring board run as a contact mating surface by the military is also a cause for lack of interest.

Low Insertion Force Connector

Of the 22 manufacturers included in the survey, 13 (59%) are involved, with eight having parts available. There seems to be no general agreement on what a "low insertion force" is. Those claiming low insertion force connectors include design forces from 6 oz. to 0.5 oz. The contact designs which appear to be most prevalent are:

Contact	Manufacturer	Contact Force	Cost
Brush Contact	Bendix	0.5 oz.	$ .20
Box Contact	AMP	4 oz. 2 Oz.	.30
Hypertac Contact	IEH	1.5 oz.	.50
	Hypertronics		.50
	Smith Industries		.45
Twist Pin	Microdot	6 oz. max.	.45
	ITT Cannon	3 oz. avg.	.50
	TRW Cinch		.50

With the exception of the brush contact by Bendix, the listed contact types have been available for years. We have used the box contact in a 95-pin connector successfully for 10 years. Also, we have a 300-pin connector using the Hypertac contact, which has been used for approximately 6 years. This contact was recently included in a 154 and 100-pin connector. The brush contact is a new concept which appeared on the market this year.

The question "What is an acceptable connector mating force?" is being asked by the connector industry. Acceptable mating forces should be a prime consideration at the time consideration is being given to system mechanical and electrical partitioning. The cost, complexity and reliability penalties in attempting to cram large numbers of contacts on minimum spacing, and relying on the availability of low or zero insertion force connectors to allow mating without complex mechanical devices, may be prohibitive.

The connector industry is apprehensive about making an investment in a new connector type without this answer from the leaders in packaging design in industry.

AREAS TO WATCH

New contact materials that maybe used without plating, such as CDA 725 nickel/berryllium.

Selective plating only in mating area of contact.

Gold stripping or in-laying in mating area of contact.

Wire wrap capability at closer than 0.100 grid. Gordon Wilmington, Product Manager at Gardner-Denver indicates in a feasibility study two years ago, use of a 0.075 grid with 34 AWG wire could be accomplished, but was dropped due to lack of interested customers.

TABLE C - I. MANUFACTURERS CONTACTED

Manufacturer	Zero Insertion Force	Low Insertion Force
AMP	PA	PA
Amphenol	PA	NP
Appleton Elect	FP	NP
Augat	NP	NP
Bendix	NP	PA
Elco	FP	FP
GTE Sylvania	FP	FP
Hypertronics	FP	PA
IEH	NP	PA
ITT Cannon	FP	NP
Methode	FP	NP
Microdot	NP	PA
Molex	NP	PA
Mupac	NP	NP
Singer/Kearfott	PA	NP
Smith	NP	PA
Stanford Applied Eng.	NP	PA
Stuart Ind.	NP	NP
TI	NP	FP
TRW Cinch	FP	FP
Viking	NP	FP
Wells Elec.	NP*	NP

Legend

PA = Parts Available
FP = Future Plans (within next two years)
NP = No Plans

*ZIP Dual In Line Socket Available

TABLE C - 2. ZERO INSERTION FORCE CONNECTORS

Manufacturer	Tooled	Planned In Future
AMP	X	
Amphenol	X	
Appleton Elect.		X
Elco		X
GTE Sylvania		X
Hypertronics		X
ITT Cannon		X
Methode		X
Singer/Kearfott	X	
TRW Cinch		X

TABLE C - 3. LOW INSERTION FORCE CONNECTORS

Manufacturer	Tooled	Planned In Future
AMP	X	
Bendix	X	
Elco		X
GTE Sylvania		X
Hypertronics	X	
IEH	X	
Microdot	X	
MUPAC	X	
Smith	X	
Standard Applied Eng.	X	
T.I.		X
TRW Cinch		X
Viking		X

TABLE C - 4. ZERO INSERTION FORCE CONNECTOR SUMMARY

Manufacturer	Total No. of Contacts	Contact Spacing	BD TUK	Contact Pressure		Terminations	Cost Per Contact $0.00
AMP	64-280 Dual Row	.09		Open	11 oz	Wire Wrap Dip Solder	.08
	130 Dual Row	.100	.06				
Amphenol	76 Dual Row	.100	.06	Close	2 oz	Wire Wrap	.20
Appleton Elect.	PLANNED FOR FUTURE - NO DATA AVAILABLE						
ELCO	120 Dual Row	.100	.06	Close	5 oz	Wire Wrap	.10
GTE Sylvania	144 Dual Row	.100	.06	Open	4 oz	Wire Wrap	.10
Hypertronics	20-200 Dual Row	.050	.06	Close	2.5 oz	Wire Wrap Dip Solder	.15
Cannon	40-160 Dual Row	.100	.06	Open	-	Wire Wrap Dip Solder Flat Cable	.15

TABLE C - 4. ZERO INSERTION FORCE CONNECTOR SUMMARY (Continued)

Manufacturer	Total No. of Contacts	Contact Spacing	BD TUK	Contact Pressure		Terminations	Cost Per Contact $0.00
Method	20-140 Dual	.100 .125 .150 .156	.06	Open	5 oz	Wire Wrap Solder Cup Dip Solder	.12
Singer/ Kearfott	152 Dual Row	.050	.06	Close	8 oz	Wire Wrap	3.30
TRW Cinch	100 Dual Row	.100	.09 & .125	Contacts Actuated by Board Insertion	5 oz.	Wire Wrap Dip Solder	.05

TABLE C - 5. LOW INSERTION FORCE CONNECTOR SUMMARY

Manufacturer	No. of Contacts	Contact Spacing	No. of Key Positions	Terminations	Insertion Per Force Contact	Cost Per Line $0.00
AMP	30-110 120-180 20-128	.100 .075 .050	200	Wire Wrap Dip Solder Planar	4 oz	.30
Bendix	20-300	.100 .050 in Design phase	256	Wire Wrap Crimp Dip Solder Planar	.5 oz	.20
Elco						
GTE Sylvania	120	.100	None	Wire Wrap Dip Solder -	.7 oz	.08
	17-100	.100	216	Wire Wrap Dip Solder Solder Cup Crimp Termipoint Planar	1.5 oz	.50
IEH	100, 154 164, 300 (90, 120 Being tooled)	.100	64	Wire Wrap Dip Solder Crimp Planar	1.5 oz	.50
Microdot	40-128	.050	254	Wire Wrap Dip Solder Planar	6 oz max 3 oz avg	.45
MUPAC	108	.100	-	Wire Wrap Dip Solder	3.5 oz	.19

TABLE C - 5. LOW INSERTION FORCE CONNECTOR SUMMARY (Continued)

Manufacturer	No. of Contacts	Contact Spacing	No. of Key Positions	Terminations	Insertion Per Force Contact	Cost Per Line $0.00
Smith	4-160	.100 .150 .200	254	Wire Wrap Dip Solder Solder Cup Planar	1.5 oz	.45
Stanford Applied Eng.	20, 100 140	.100	-	Wire Wrap Dip Solder Wire	4 oz	.39
Texas Instruments						
TRW Cinch	40-184	.100	254	Wire Wrap Dip Solder Planar	6 oz max 3 oz avg	.50
Viking	20-100	.100	-	Wire Wrap Dip Solder	-	-

APPENDIX D

MODULE THERMAL ANALYSIS

APPENDIX D

LIST OF ILLUSTRATIONS

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D-16	I-2X Size Module (Case 9)
D-17	I-2B Size Module (Case 10)

APPENDIX D. MODULE THERMAL ANALYSIS

D.1 Case 1. (I-2A)

D.1.1 The configuration and assumptions used in defining Case 1 are shown in Figure D-1. A total module power of 10W will be used in the analysis of Case 1 with the components on one side, two sides and with aluminum and copper frames. Both direct-impingement air cooling and conduction cooling will be analyzed.

A. Components on One Side Only

There are 36 chip carriers dissipating a total of 10W or 278 W/carrier.

1. Conduction cooled

Junction-to-case Δ t:

$$0.278\ W \times \frac{30^{o}C}{W} = 8^{o}\ C \qquad (1)$$

Chip carrier to substrate Δ t:

$$\frac{0.278\ W \times 0.004\ IN.}{0.0044\ \frac{W}{IN.^{o}C} \times (0.35\ IN.)^{2}} = 2^{o}\ C \qquad (2)$$

Through substrate Δ t:

$$\frac{0.278\ W \times 0.040\ IN.}{0.469\ \frac{W}{IN.^{o}C} \times (0.35\ IN.)^{2}} = 0^{o}C\ (\text{TO NEAREST DEGREE}) \qquad (3)$$

Substrate-to-heat sink bond Δ t:

$$\frac{10\ W \times 0.004\ IN.}{0.0044\ \frac{W}{IN.^{o}C} \times 5.3\ IN. \times 1.25\ IN.} = 1^{o}\ C \qquad (4)$$

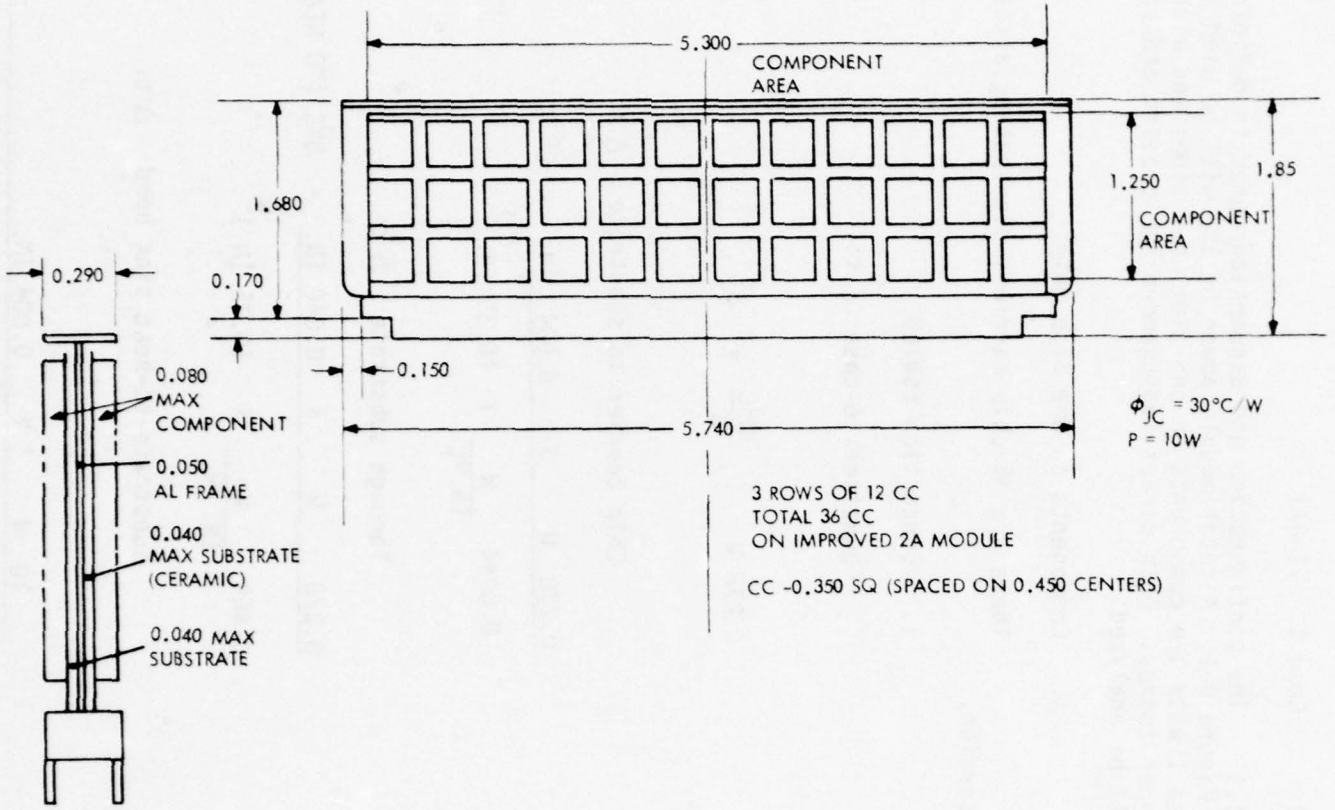


Figure D-1. I-2A Size Module (Case 1)

Worst component position (middle of module) heat sink Δt with aluminum heat sink:

$$\frac{1.67\ W \times 2.97\ IN.}{2 \times 4.35 \frac{W}{IN.\ ^{o}C} \times 0.42\ IN. \times 0.05\ IN.} = 27^{o}C \quad (5)$$

Average component position heat sink rise with aluminum frame:

$$\frac{2}{3} \times 27^{o}\ C = 18^{o}\ C \quad (6)$$

Adjusting the above temperature drops for copper frame.

Worst component position rise:

$$\frac{27^{o}\ C}{2.25} = 12^{o}\ C \quad (7)$$

Average component position rise:

$$\frac{2}{3} \times 12^{o}\ C = 8^{o}\ C \quad (8)$$

2. Direct air cooling of modules:

The following typical Dual In-line Package thermal convection resistance was taken from study by Larry Nash and Ron Lannon at

the Naval Weapons Support Center at Crane, Indiana. It is for modules on 0.3" centers with an air flow velocity of 19 ft/sec.

DIP-to-air:	37.5 °C/W
Flat pack and chip carrier (these are about one half area of DIPS)	70 °C/W

Junction-to-case Δ t:

$$0.278 \quad W \quad X \quad 75^{o} \frac{C}{W} = 21^{o} C \tag{9}$$

B. Components on Two Sides of Module

Power: There are 72 components dissipating a total of 10W or 0.139 W/Chip Carrier.

1. Conduction cooled

Junction-to-case Δ t:

$$0.139 \quad W \quad X \quad 30^{o} \frac{C}{W} = 4^{o} C \tag{10}$$

Chip carrier-to-substrate Δ t:

$$\frac{0.139 \quad W \quad X \quad 0.004 \text{ IN.}}{0.0044 \quad \frac{W}{\text{IN.} \ ^{o}C} \quad X \quad (0.35 \text{ IN.})^{2}} = 1^{o} C \tag{11}$$

Through substrate Δ t:

$$\frac{0.139 \quad W \quad X \quad 0.040 \text{ IN.}}{0.469 \quad \frac{W}{\text{IN.} \ ^{o}C} \quad X \quad (0.35 \text{ IN.})^{2}} = 0^{o} C \text{ (TO NEAREST DEGREE)} \tag{12}$$

Substrate-to-heat sink bond Δt:

$$\frac{5 \text{ W} \times 0.004 \text{ IN.}}{0.0044 \frac{\text{W}}{\text{IN.} \ ^{\circ}\text{C}} \ (5.3 \text{ IN.} \times 1.25 \text{ IN.})^2} = 0^{\circ} \text{ C} \qquad (13)$$

Worst component position heat sink Δt with aluminum heat sink:

$$\frac{1.67 \text{ W} \times 2.97 \text{ IN}}{2 \times 4.35 \frac{\text{W}}{\text{IN.} \ ^{\circ}\text{C}} \times 0.42 \text{ IN} \times 0.05 \text{ IN}} = 27^{\circ} \text{ C} \qquad (14)$$

Average component position heat sink Δt with aluminum heat sink:

$$\frac{2}{3} \times 27^{\circ} \text{ C} = 18^{\circ} \text{ C} \qquad (15)$$

Worst component position heat sink rise with copper heat sink:

$$\frac{27^{\circ} \text{ C}}{2.25} = 12^{\circ} \text{ C} \qquad (16)$$

Average component position rise with copper heat sink:

$$\frac{2}{3} \times 12^{\circ} \text{ C} = 8^{\circ} \text{ C} \qquad (17)$$

2. Forced-convection cooled components

Junction-to-case Δ t:

$$0.139 \text{ W} \times 30^{\circ} \frac{\text{C}}{\text{W}} = 4^{\circ} \text{ C} \quad (18)$$

Case-to-local cooling air:

$$0.139 \text{ W} \times 75^{\circ} \frac{\text{C}}{\text{W}} = 10^{\circ} \text{ C} \quad (19)$$

3. Guide Rib-to-Card Cage Δ t:

A measured thermal resistance of 1.9°C/W will be used in this report for the improved 2-A Module.

$$\therefore \Delta \text{ t} = 10 \text{ W} \times 1.9^{\circ} \frac{\text{C}}{\text{W}} = 19^{\circ} \text{ C} \quad (20)$$

Case I. Tabular Summary (See Figure D-2)

Sub-Case Definitions:

1. Components one side only, conduction cooling, aluminum, worst component position.

2. Component one side only, conduction cooling, aluminum, average component position.

3. Components one side only, conduction cooling, copper heat sink, worst component position.

4. Components one side only, conduction cooling, copper heat sink, average component position.

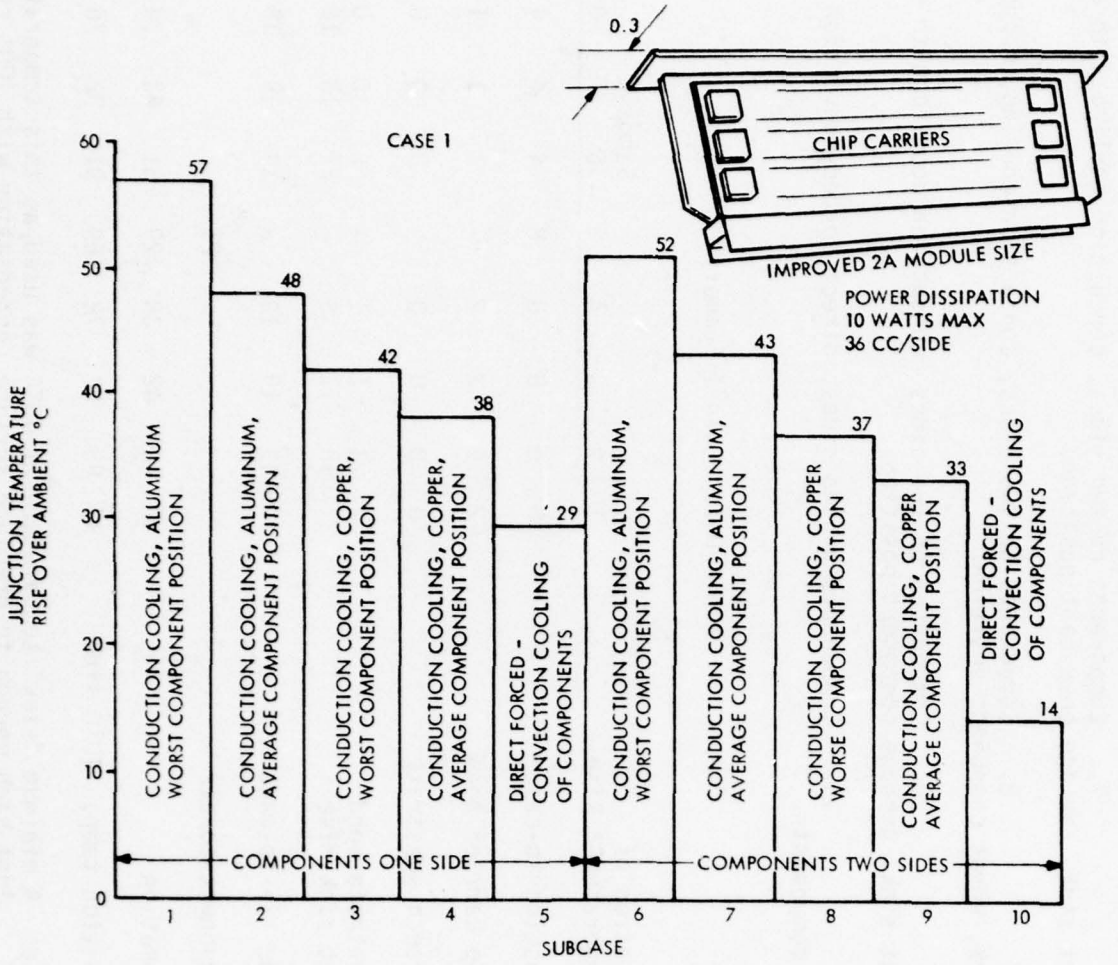


Figure D-2. I-2A Module Subcase Definitions (Case 1)

5. Components on one side only, direct forced-convection cooling of components.

6. Components on two sides, conduction cooling with aluminum heat sink, worst component position.

7. Components on two sides, conduction cooling with aluminum heat sink, average component position.

8. Components on two sides, conduction cooling, copper heat sink, worst component position.

9. Components on two sides, conduction cooling with copper heat sink, average component position.

10. Components on two sides, direct forced-convection cooling of components.

Table D-1. Case I Summary

Location of Temperature* Rise	Subcase 1	2	3	4	5	6	7	8	9	10
Junction-to-case	8	8	8	8	8	4	4	4	4	4
Chip carrier bond	2	2	2	2	-	1	1	1	1	-
Through substrate	0	0	0	0	-	0	0	0	0	-
Substrate bond	1	1	1	1	-	0	0	0	0	-
Heat sink rise	27	18	12	8	-	27	18	12	8	-
Side rib-to-cage	19	19	19	19	-	19	19	19	19	-
Component-to-air					21					10
Summation	57	48	42	38	29	51	42	36	32	13
Junction temp. -40°C sink	97	88	82	78	69	91	82	76	72	53

Note: A minimum "sink" temperature of 40°C was used, as this temperature is just high enough to preclude surface condensation with 100% relative humidity on an Army/Navy Hot Day.

*Temperature-Degrees Celsius

D.2 Case 2 (I-2A)

D.2.1 The Case 2 configuration is defined in Figure D-3.

A. Components on One Side Only

Power: there are twenty-seven integrated circuits dissipating a total of 10W or 0.370 W/intergrated circuit.

1. Conduction cooled

Junction-to-case Δt:

$$0.370 \text{ W} \times 45^{\circ}\frac{\text{C}}{\text{W}} = 17^{\circ}\text{C} \qquad (21)$$

Flat pack case-to-PWB:

$$\Delta t = \frac{0.370 \text{ W} \times 0.004 \text{ IN.}}{0.044 \frac{\text{W}}{\text{IN.}^{\circ}\text{C}} \times 0.28 \text{ IN.} \times 0.40 \text{ IN.}} = 3^{\circ}\text{C} \qquad (22)$$

Through PWB to heat sink:

$$\Delta t = \frac{0.370 \text{ W} \times 0.064 \text{ IN.}}{0.0044 \frac{\text{W}}{\text{IN.}^{\circ}\text{C}} \times 0.251 \text{ IN.}^2 \times 1.36} = 16^{\circ}\text{C} \qquad (23)$$

Note: The 1/1.36 factor is an empirically-determined factor to account for thermal spreading and eyelet conductiances.

Worst component position heat sink Δt with aluminum heat sink:

$$\frac{1.67 \text{ W} \times 2.97 \text{ IN.}}{2 \times 4.35 \frac{\text{W}}{\text{IN.}^{\circ}\text{C}} \times 0.43 \text{ IN.} \times 0.05 \text{ IN.}} = 27^{\circ}\text{C} \qquad (24)$$

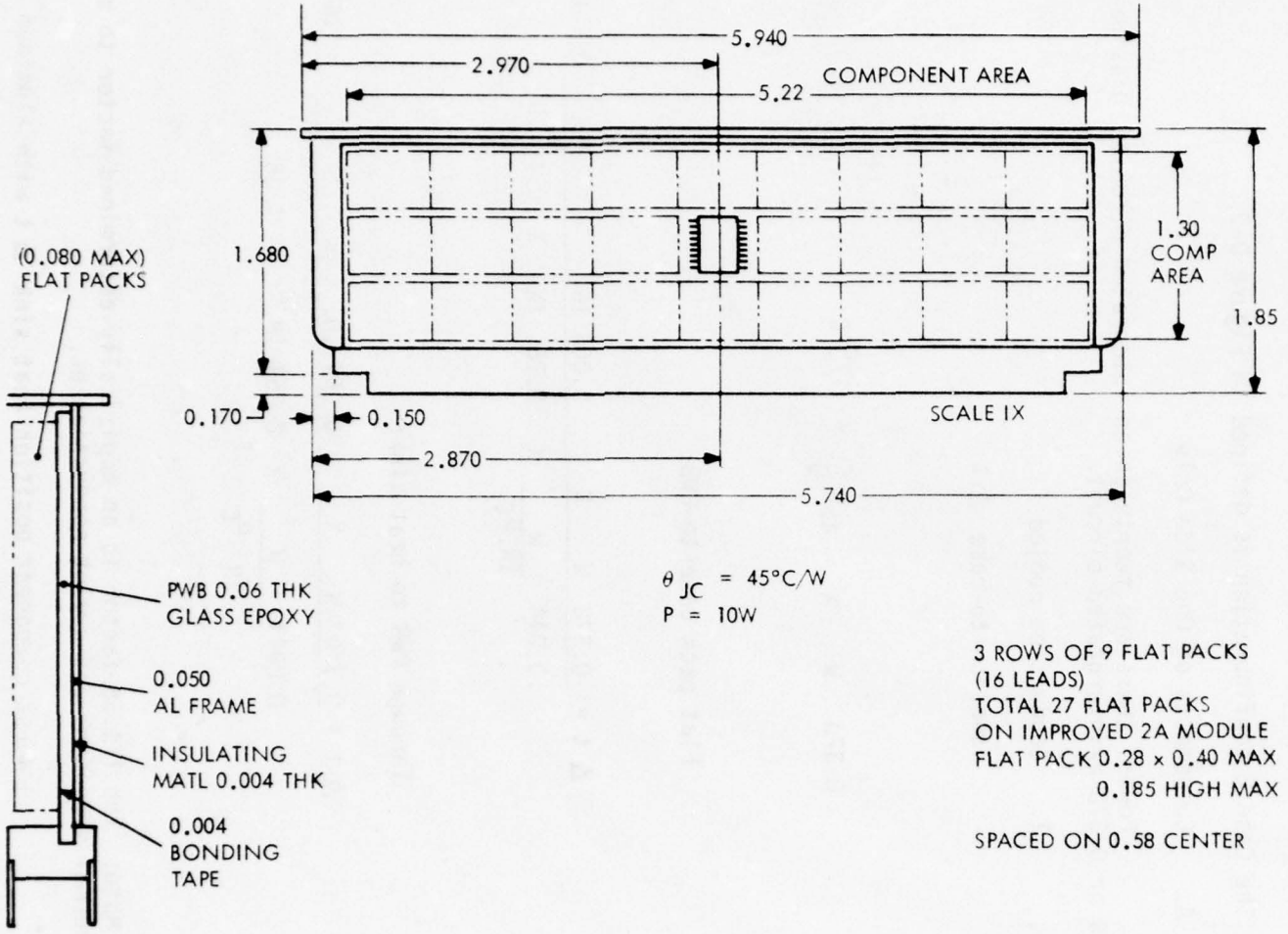


Figure D-3. I-2A Size Module (Case 2)

Average component position heat sink Δ t with aluminum heat sink:

$$\frac{2}{3} \times 27^{o} C = 18^{o} C \quad (25)$$

Worst component position rise with copper heat sink:

$$\frac{27^{o} C}{2.25} = 12^{o} C \quad (26)$$

Average component position temperature rise with copper:

$$\frac{2}{3} \times 12^{o} C = 8^{o} C \quad (27)$$

Guide rib-to-card cage Δ t: (See explanation in Case I)

$$10 W \times 1.9^{o} \frac{C}{W} = 19^{o} C \quad (28)$$

2. Forced Air Cooled Module:

Junction-to-case Δ t:

$$0.370 W \times 45^{o} \frac{C}{W} = 17^{o} C \quad (29)$$

Case-to-local cooling air:

$$0.370 \text{ W} \times 70^{\circ} \frac{\text{C}}{\text{W}} = 28^{\circ} \text{ C} \qquad (30)$$

B. Components on Two Sides of Module

Power: There are 54 integrated circuits (flat packs) dissipating 0.185W each, for a total of 10W.

1. Conduction cooled

Junction-to-case Δ t:

$$0.185 \text{ W} \times 45^{\circ} \frac{\text{C}}{\text{W}} = 8^{\circ} \text{ C} \qquad (31)$$

Flat pack case to PWB: (32)

$$\Delta t = \frac{0.185 \text{ W} \times 0.004 \text{ IN.}}{0.0044 \frac{\text{W}}{\text{IN.}^{\circ}\text{C}} \times 0.28 \text{ IN.} \times 0.40 \text{ IN.} \times 1.36} = 1^{\circ} \text{ C}$$

Through PWB to heat sink:

(33)

$$\frac{0.185 \text{ W} \times 0.064 \text{ IN.}}{0.0044 \frac{\text{W}}{\text{IN.}^{\circ}\text{C}} \times 0.251 \text{ IN.}^2 \times 1.36} = 8^{\circ} \text{ C}$$

(See above for explanation of 1/1.36 factor.)

The heat sink and guide-rib calculations are identical to Case 2A, above.

2. Integrated Circuits air-cooled by forced-convection:

Junction-to-case:

$$0.185 \quad W \quad X \quad 45^{o} \frac{C}{W} = 8^{o} C \tag{34}$$

Case to local cooling air:

$$0.185 \quad W \quad X \quad 70^{o} \frac{C}{W} = 14^{o} C \tag{35}$$

Case II Tabular Summary (See Figure D-4)

Sub-Case Definitions

1. Components one side only, conduction cooling, aluminum heat sink, worst component position.

2. Components one side only, conduction cooling, aluminum heat sink, average component position.

3. Components one side only, conduction cooling, copper heat sink, worst component position.

4. Components one side only, conduction cooling, copper heat sinks, average component position.

5. Components on one side only, direct forced-convection cooling.

6. Like #1 above, but components on two sides.

7. Like #2 above, but components on two sides.

8. Like #3 above, but components on two sides.

9. Like #4 above, but components on two sides.

10. Like #5 above, but components on two sides.

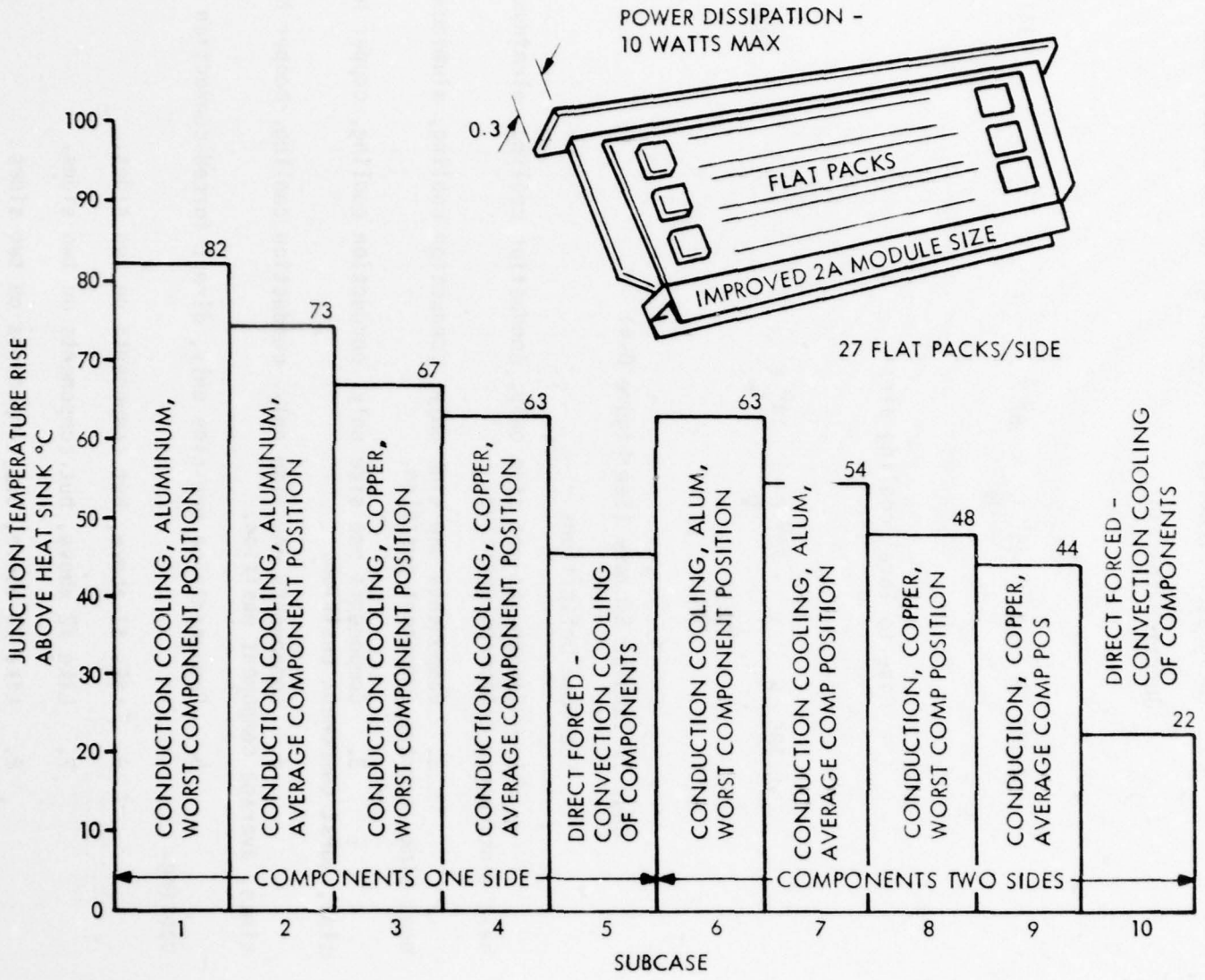


Figure D-4. I-2A Module Subcase Definitions (Case 2)

Table D-2. Case II Tabular Summary

Location of Temperature* Rise	Subcase 1	2	3	4	5	6	7	8	9	10
Junction-to-case	17	17	17	17	17	8	8	8	8	8
I.C. bond	3	3	3	3	-	1	1	1	1	-
Through PWB	16	16	16	16	-	8	8	8	8	-
Heat sink rise	27	18	12	8	-	27	18	12	8	-
Guide rib-card cage	19	19	19	19	-	19	19	19	19	-
I.C. case-cooling air	-	-	-	-	28					14
Summation	82	73	67	63	45	63	54	48	44	22
Junction Temp -40°C Sink	112	113	107	103	85	103	94	88	84	62

*Temperature-Degree Celsius

D.3 Case 3

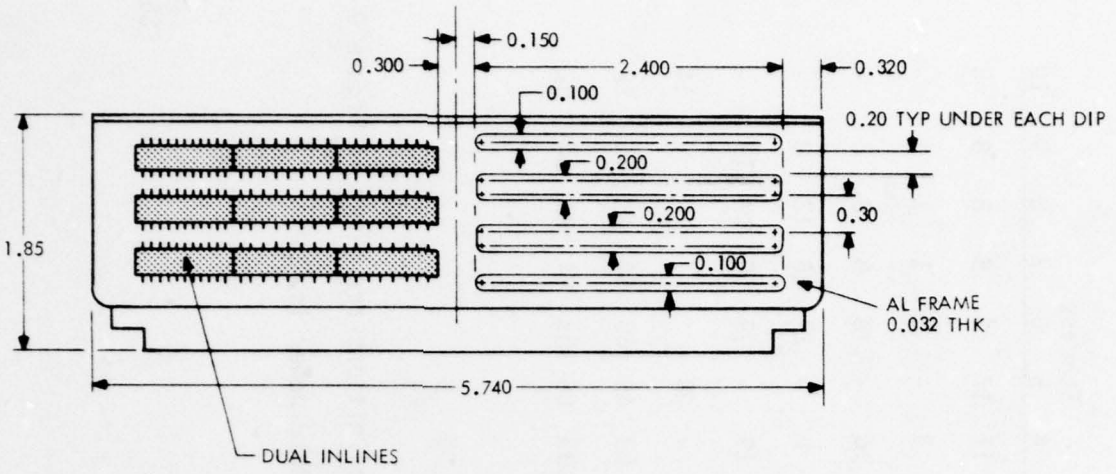
D.3.1 The Case 3 configuration and definitions are given in Figure D-5.

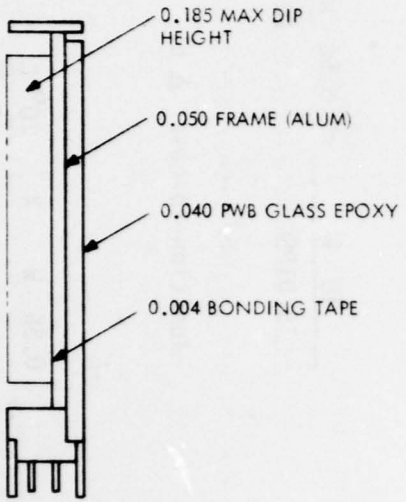
Power per DIP if total module power is 10W

$$\frac{10\ W}{18\ DIPS} = 0.56\ \frac{W}{DIP} \tag{36}$$

Junction-to-case Δ t:

$$0.56\ W \quad X \quad 20^{o}\ \frac{C}{W} = 11^{o}\ C \tag{37}$$





3 ROWS OF 6 DIP SPACED 0.40 APART (VERT)
TOTAL 18 DIP ON IMPROVED 2A MODULE

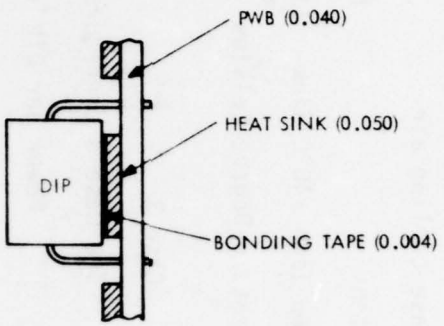


Figure D-5. I-2A Size Module (Case 3)

Case-to-heat-sink:

$$\frac{0.56 \text{ W} \times 0.004 \text{ IN.}}{0.0044 \frac{\text{W}}{\text{IN.}^{\circ}\text{C}} \times 0.2 \text{ IN.} \times 0.8 \text{ IN.}} = 3^{\circ} \text{ C} \qquad (38)$$

Worst case position heat sink rise:

$$\frac{1.667 \text{ W} \times 2.57 \text{ IN.}}{2 \times 4.35 \frac{\text{W}}{\text{IN.}^{\circ}\text{C}} \times 0.2 \text{ IN.} \times 0.5 \text{ IN.}} = 49^{\circ} \text{ C} \qquad (39)$$

Average component position heat sink rise (from above)

$$\frac{2}{3} \times 49^{\circ} \text{ C} = 33^{\circ} \text{ C} \qquad (40)$$

Guide rib-to-card cage as in previous case:

$$10 \text{ W} \times 1.9^{\circ} \frac{\text{C}}{\text{W}} = 19^{\circ} \text{ C} \qquad (41)$$

Table D-3. Case 3 Summary (10 Watt Total Power) (See Figure D-6)

	Δ t	% of Total
Junction-to-case	11°C	13
Case-to-heat-sink	3°	4
Heat sink rise	49	60
Guide rib-to-card-cage	19	
Summ for worst position Σ =	82	
Summ for average component Σ =	66	

B. Forced Convection Cooling

Junction-to-case 11°C

(Same as above.)

Case-to-local cooling air:

$$0.556 \frac{W}{DIP} \times 37.5 \frac{^{o}C}{W} = 21^{o} C \qquad (42)$$

This 31°C rise is small compared with either the conduction-cooled average component position case (66°C) or the worst-position case (82°C). The comparison would be more striking if the fluid-to-heat exchanger Δ t, a Δ t associated in this accounting with the rack rather than the module, were included.

D.4 Case 4 (I-2A)

D.4.1 The Case 4 configuration and definition are given in Figure D-7.

A. Air between multilayered boards with flat packs:

The following temperature rises were calculated in Case 2B above:

Junction-to-case	8°C
I.C. Case to PWB	1°C
Through PWB to extended surface	8°C

Extended surface (fins)-to-air pressure drop:

A worst case, but realistic calculation will be made for the film-coefficient of air in 0.1 in. square passages. The limiting Nusselt number for flow in a square passage is 3.63. (See reference, below.)

Reference: Kays, William and London, A.L., "Compact Heat Exchangers," McGraw Hill, 2nd Edition, 1964; p. 103

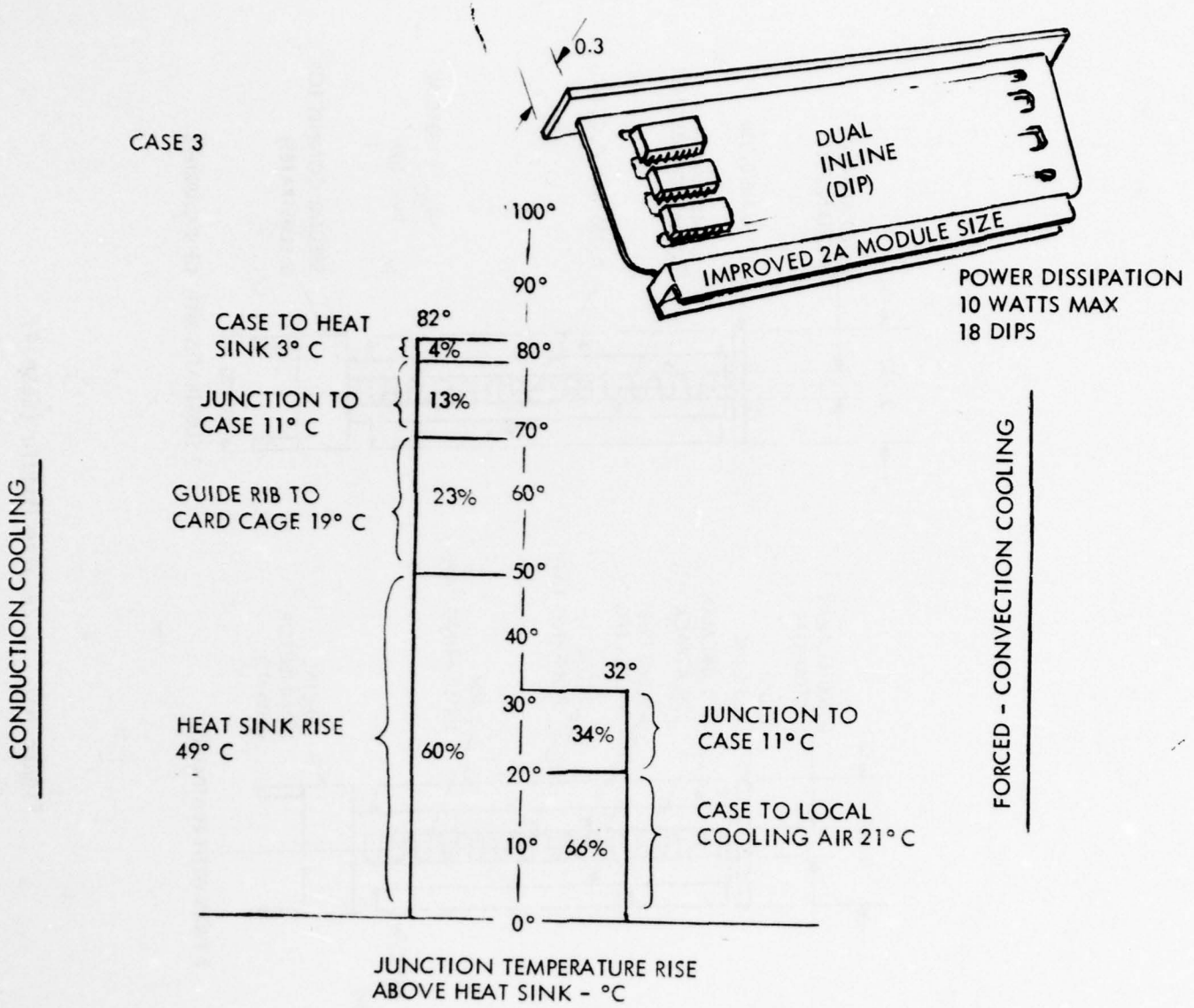


Figure D-6. I-2A Module Summary (Case 3)

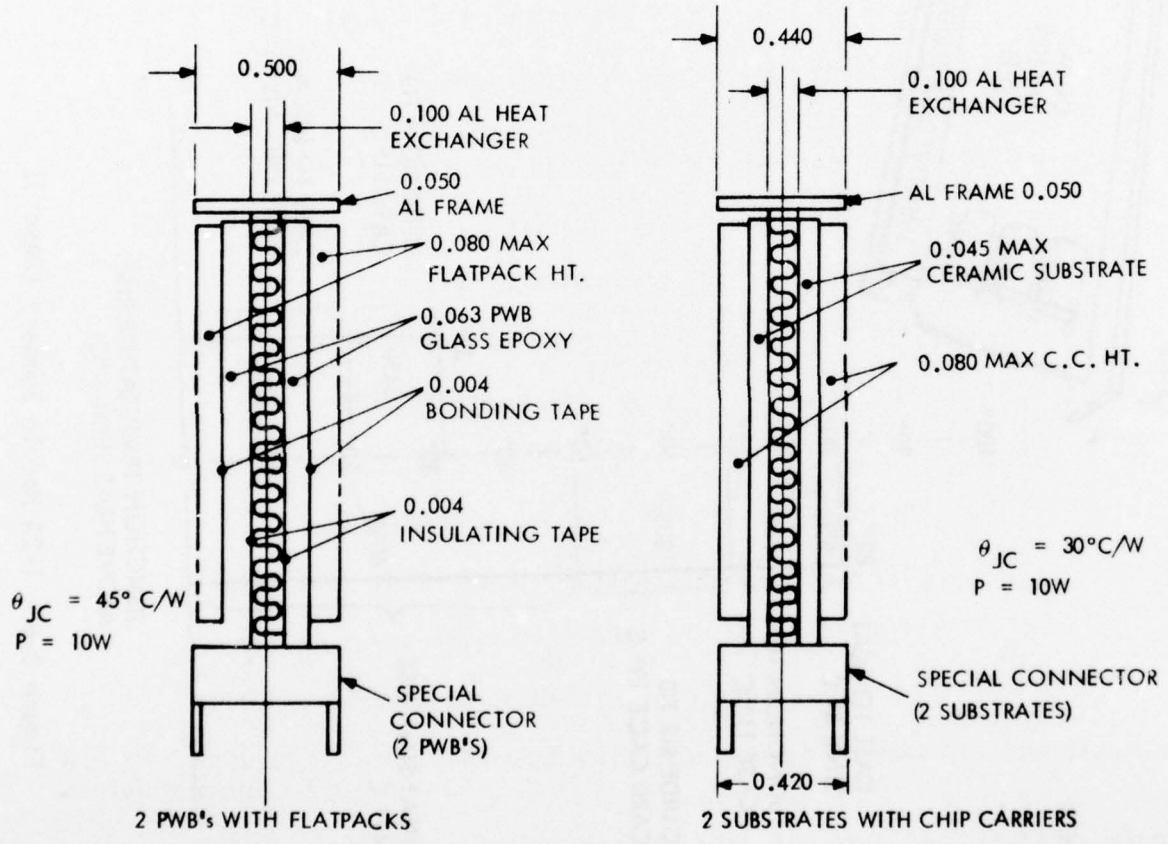


Figure D-7. I-2A Size Module (Case 4)

Hydraulic diameter:

$$D = \frac{0.1 \text{ IN.}}{12 \frac{\text{IN.}}{\text{FT.}}} = 8.33 \times 10^{-3} \text{ FT.} \tag{43}$$

$$\frac{h D}{k} = 3.63 \tag{44}$$

$$h = \frac{k}{D} \times 3.63 = \frac{0.016 \frac{\text{BTU}}{\text{HR FT °F}} \times 3.63}{8.33 \times 10^{-3} \text{ FT}} = 7.0 \frac{\text{BTU}}{\text{HR FT}^2 \text{ °F}} \tag{45}$$

Heat transfer area:

There are thirty passages, each having a perimeter of 0.4" or 3.33×10^{-2} ft. Each passage is 5.3 inches or 0.442 feet in length. The total heat transfer area is:

$$30 \times 3.33 \times 10^{-2} \times 0.442 = 0.442 \text{ FT.}^2 \tag{46}$$

The temperature drop between the air and extended surface, assuming a fin efficiency of 90%, is:

$$\Delta t = \frac{q}{hA} = \tag{47}$$

$$\frac{10 \text{ W} \times 3.412 \frac{\text{BTU}}{\text{HR. W}}}{0.9 \times 7 \frac{\text{BTU}}{\text{HR. FT.}^2 \text{ °F}} \times 0.442 \text{ FT.}^2 \times 1.8 \frac{\text{F}}{\text{C}}} = 7^{\circ} \text{ C}$$

Table D-4. Core 4 Summary (See Figure D-8)

Junction to case	8°C
Flat-pack bond	1°C
Through PWB	8°C
Fin - PWB bond	1°C
Fin - local air	7°C
Total Δ T Junction-Air	25°C

B. Air between multilayered boards with chip carriers and ceramic substrates:

Refer to Case 1-B above for calculation of the following:

Power per chip carrier	0.139W
Δ t Junction-to-case	4°C
Chip carrier bond Δ t	1°C
Through substrate Δ t	0°C
Substrate-to-fin bond	1°C
Fin-to-fin Δ t	7°C
Total rise above local cooling air:	13°C
Junction temperature with 40°C air	53°C

D.5 Case 5 - Liquid Cooled Module (5/4 ATR)

D.5.1 Figure D-9 shows the particular configuration used for the liquid-cooled module.

Calculation of liquid film coefficient, assuming laminar flow using limiting Nusselt number:

The limiting Nusselt number (see reference, following) for a circular tube is:

$$N_{Nu} = 4.364 \qquad (48)$$

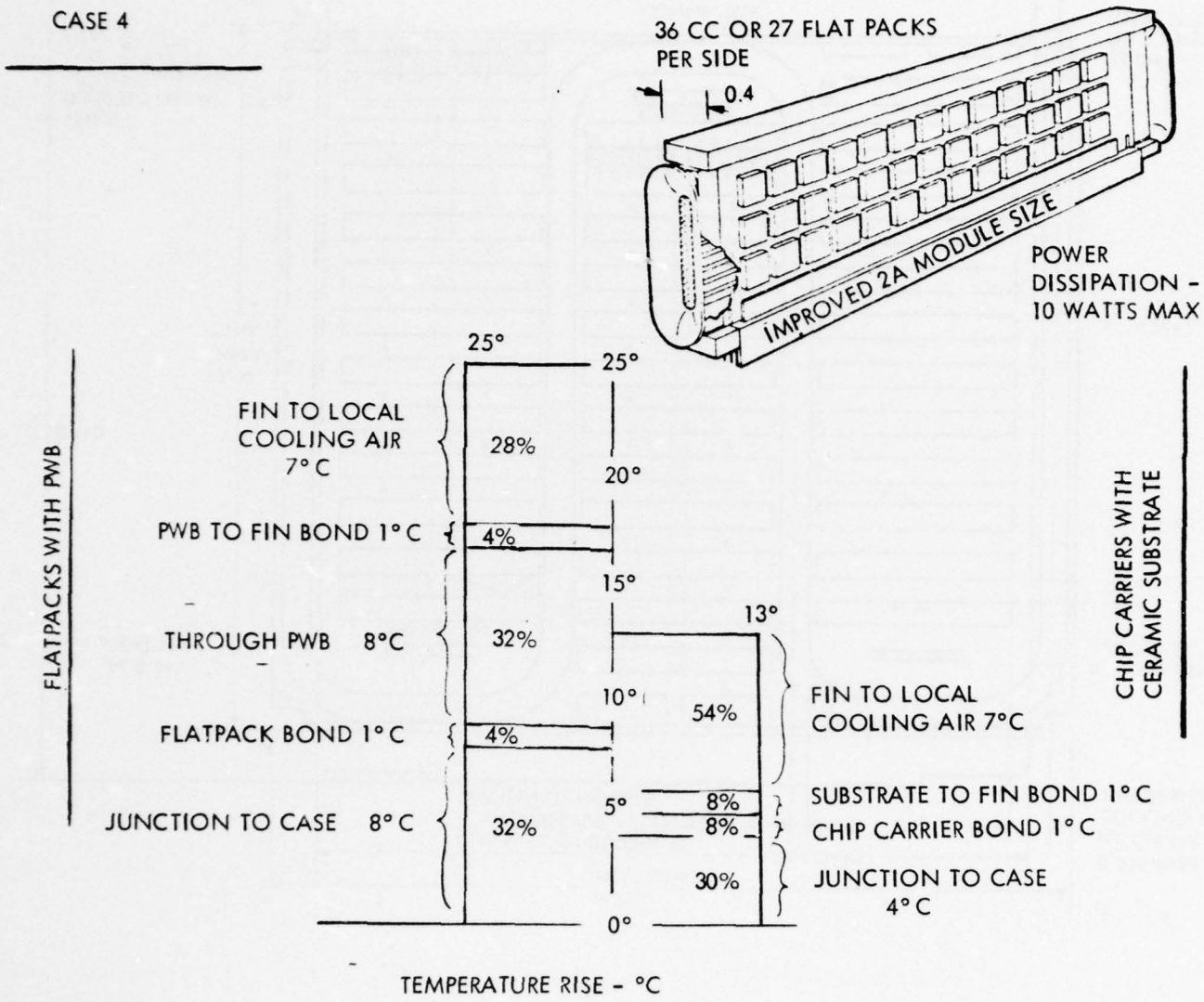


Figure D-8. I-2A Module Summary (Case 4)

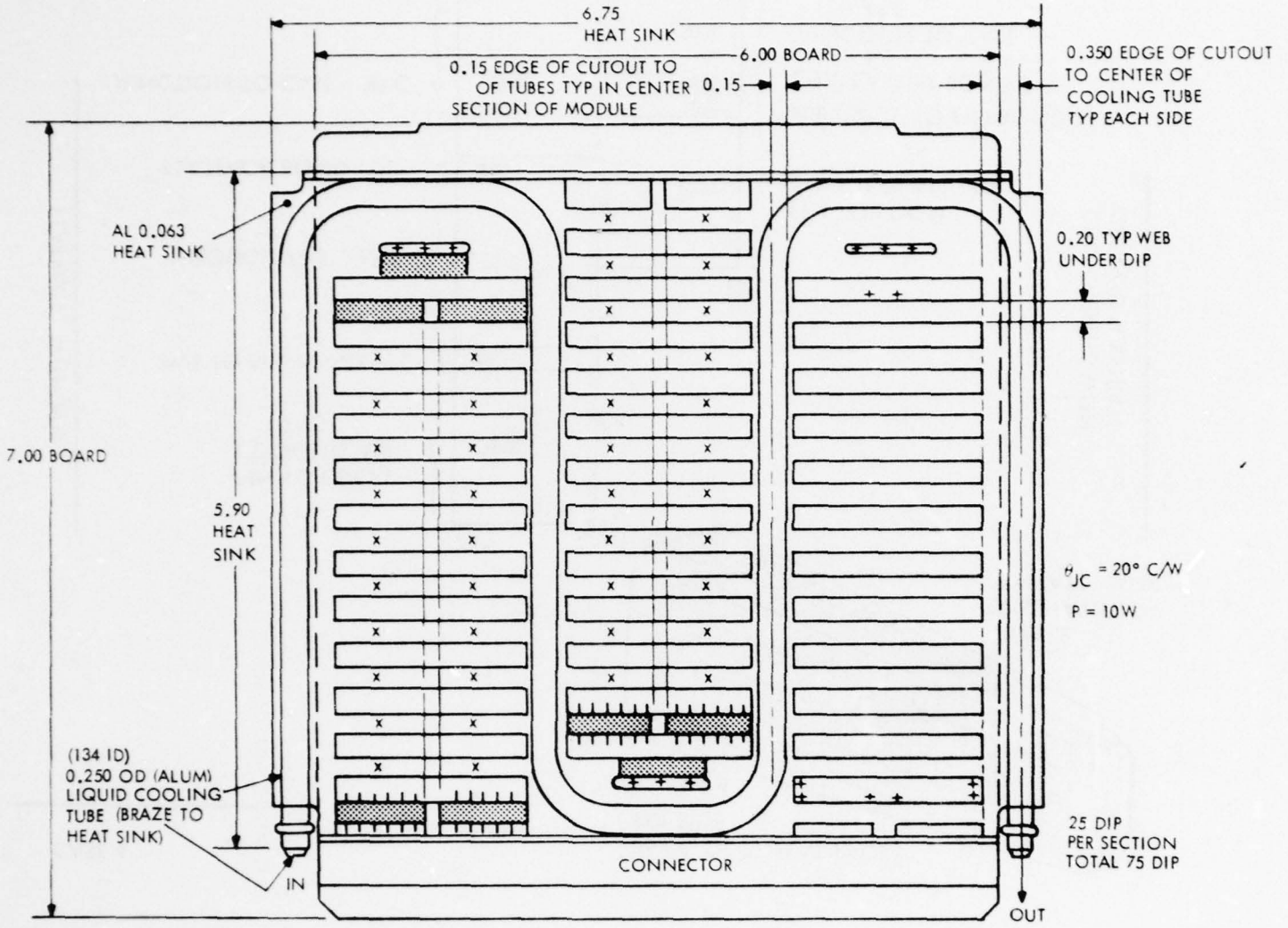


Figure D-9. Liquid-Cooled 5/4 ATR Size Module (Case 5)

$$\therefore h_c = \frac{3.380 \times 10^{-3} \frac{W}{IN.\ ^oC} \times 4.364}{0.134\ IN.} = 0.11 \frac{W}{IN.^2\ ^oC} \quad (49)$$

(This converts to 30 $\frac{BTU}{HR\ FT^2\ ^oF}$.) (50)

Reference: Kays, William and London, A.L., "Compact Heat Exchangers," McGraw Hill, 2nd Edition, 1964; p. 103.

The tube inner area associated with each dip:

$$\pi D\ell = \pi \times 0.134\ IN. \times 0.4\ IN. = 0.168\ IN.^2 \quad (51)$$

The heat transfer resistance of the fluid per DIP is:

$$\frac{1}{0.11 \frac{W}{IN.^{o}C} \times 0.168\ IN.^2} = 54^o \frac{C}{W} \quad (52)$$

Since the above resistance seems high, it will be recalculated for turbulent flow:

Calculation of film coefficient:

Will assume a flow rate which would result in a 10°C temperature rise:

$$w = \frac{q}{C_p \Delta t} = \frac{10\ W \times 3.142 \frac{BTU}{HR.\ W}}{0.47 \frac{BTU}{LB.\ ^oF} \times 18^o\ F} \quad (53)$$

= 4 lb/hr: results in a velocity of 743 FT/HR through 0.134 in. dia. tube with

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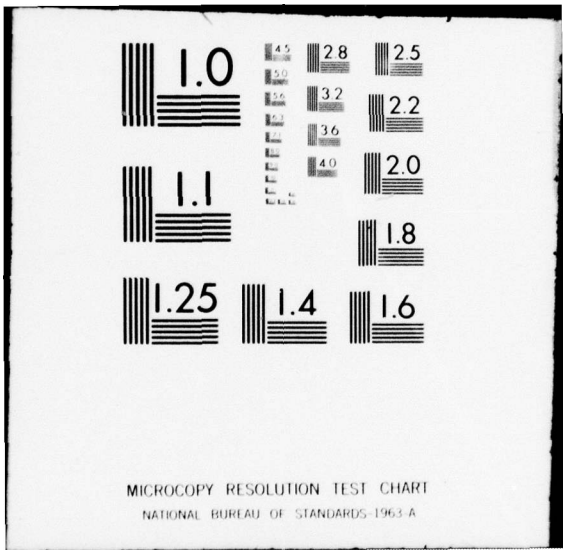
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Reynolds number: $\rho = 55 \frac{LB}{FT^2}$

$$\frac{\rho DV}{\mu} = \frac{55 \frac{LB.}{FT.^3} \times 1.12 \times 10^{-2} FT. \times 743 \frac{FT.}{HR.}}{1.21 \times 10^{-1} \frac{FT.^2}{HR.}} = 3781 \quad (54)$$

$$N_{Pr} = \frac{C_p \mu}{k} = \frac{0.47 \frac{BTU}{LB.\ ^oF} \times 1.21 \times 10^{-1} \frac{FT.^2}{HR.} \times 55 \frac{LB.}{FT.^3}}{0.0731 \frac{BTU}{HR.\ FT.\ ^o F}} \quad (55)$$

$$N_{Pr} = 43 \quad (56)$$

$$\frac{4 \frac{LB.}{HR.}}{55 \frac{LB.}{FT.^3}} = 7.27 \times 10^{-2} \frac{FT.^3}{HR} \quad (57)$$

(58)

$$V = \frac{Q}{A} = \frac{7.27 \times 10^{-2} \frac{FT.^3}{HR.} \times 4 \times 144 \frac{IN.^2}{FT.^2}}{\pi (0.134 \text{ IN.})^2} = 743 \frac{FT.}{HR.}$$

Using the reference cited, p. 108, it is seen that at a Reynolds number of 4000, $N_{NU} = 160$ or 37 times previous value. This reduces the thermal resistance of the laminar case above to:

$$\frac{54^o \frac{C}{W}}{37} = 1.46^o \frac{C}{W} \quad (59)$$

Thermal resistance of the aluminum from under center of DIP to tube wall:

(60)

$$\frac{\ell}{kA} = \frac{1 \text{ IN.}}{4.35 \frac{W}{IN.\ ^oC} \times 0.2 \text{ IN.} \times 0.063 \text{ IN.}} = 18^o \frac{C}{W}$$

DIP bond-heat sink resistance:

$$\frac{\ell}{kA} = \frac{0.004 \text{ IN.}}{0.0044 \frac{W}{IN.^{\circ}C} \times 0.8 \text{ IN.} \times 0.2 \text{ IN.}} = 5.68 \frac{C}{W} \quad (61)$$

DIP Junction-to-case: $20° \frac{C}{W}$

Power per DIP:

$$\frac{10 \text{ W}}{75 \text{ DIPS}} = 0.133 \frac{W}{DIP} \quad (62)$$

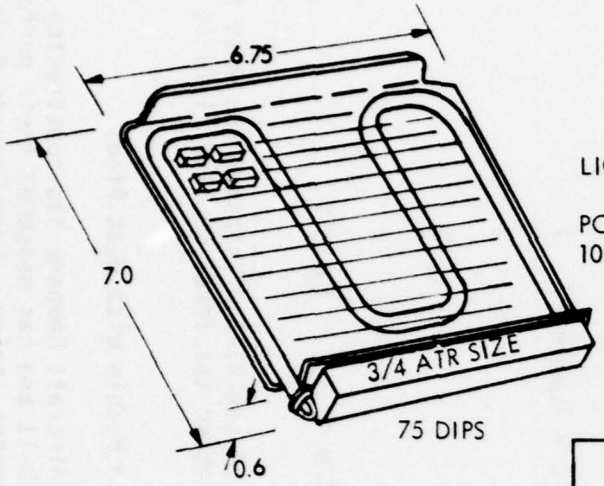
Table D-5. Case 5 Summary (See Figure D-10.)

Thermal Resistances		Temperatures-10W Modules Laminar Flow	Turbulent Flow
Fluid rise 1 C/W (Turbulent); 54°C/W (Laminar)		7	0°C
Heat sink rise	18 C/W	2	2°C
DIP bond	6 C/W	1	1
DIP internal	20 C/W	3	3°C (63)
Σ =	45 C/W; 98°C/W	Σ=13°C	Σ= 6°C

It is seen that if each of the DIPS dissipated one watt for a total of 75W, the rise of any function above the local cooling fluid in the module would be about 45°C.

D.6 Case 6 - Improved 2A Size Module with Heat Pipes

D.6.1 H.H. Token of McDonnell Aircraft Company has constructed heat pipes similar to those shown in Figure D-11 and has measured their performance. He published his results in the reference, below. From Figures 8, 9, and 10 of the reference, one concludes that a representative thermal resistance for a heat pipe of this size for powers up to 5 W per heat pipe is 2°C/W.



CASE 5

LIQUID COOLED MODULE

POWER DISSIPATION
10 WATTS MAX

	THERMAL RESISTANCE		TEMPERATURE 10W MODULE	
	TURBULENT FLOW	LAMINAR FLOW	TURBULENT FLOW	LAMINAR FLOW
FLUID RINSE	1° C/W	54° C/W	0° C	7° C
HEAT SINK RISE	18° C/W	18° C/W	2° C	2° C
DIP BOARD	6° C/W	6° C/W	1° C	1° C
DIP INTERNAL	20° C/W	20° C/W	3° C	3° C
Σ	45° C/W	98° C/W	6° C	13° C

Figure D-10. Liquid-Cooled 5/4 ATR Size Module Summary (Case 5)

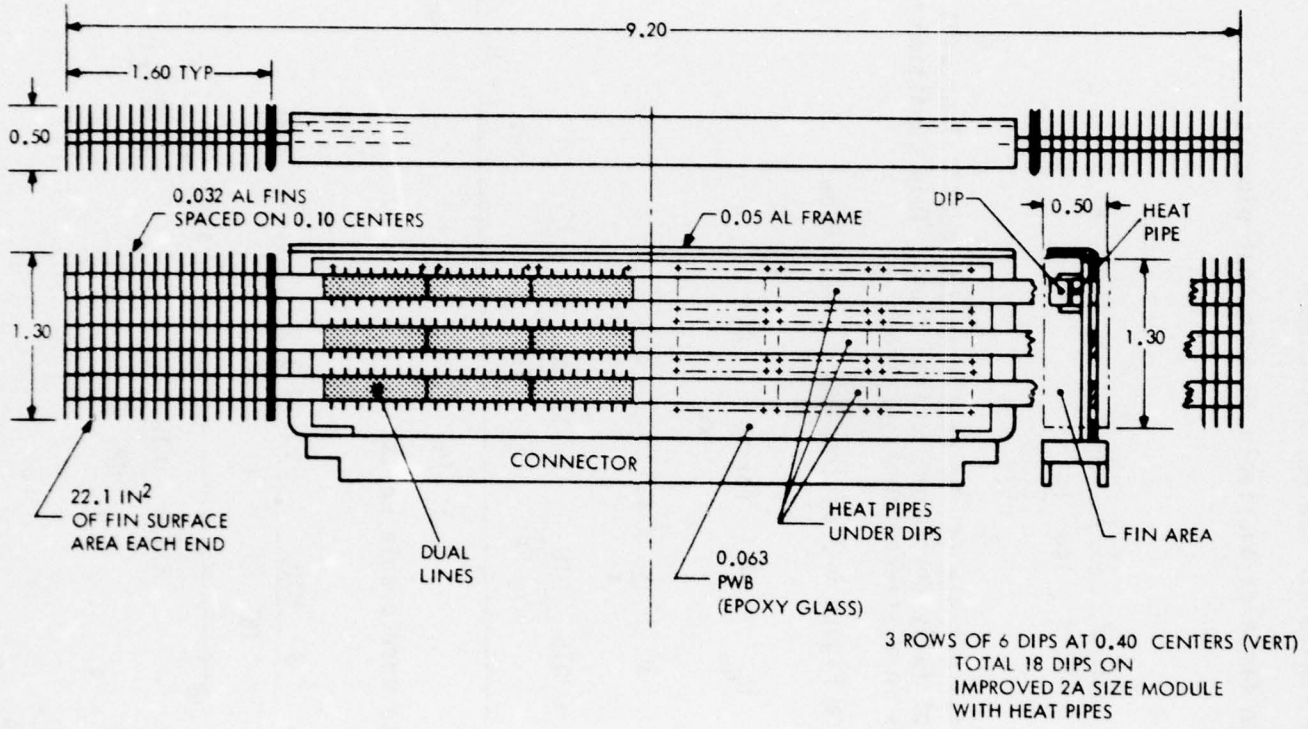


Figure D-11. I-2A Size Module with Heat Pipes (Case 6)

Reference: Token, K.H., "A New Avionics Thermal Control Concept," A.S.M.E Paper 77-ENAS-14, 14 July 1977.

Approximate Fin-to-Air Thermal Resistance

The fin area available to each heat pipe is:

$$\frac{2 \times 22.1 \text{ IN.}^2}{3 \times 144 \frac{\text{IN.}^2}{\text{FT.}^2}} = 0.10 \text{ FT.}^2 \tag{64}$$

A conservative esimate of the heat-transfer coefficient will be made with the assumption of fully-developed laminar flow. This condition might be recycled with modules in a stacked configuration.

From Figure 6-3 of the reference, below:

$$N_{Nu} = 4.1 \text{ for } \frac{1}{\alpha} = 0.5 \tag{65}$$

$$h = \frac{k}{x} \times 4.1 = \frac{0.016 \frac{\text{BTU}}{\text{FT.}\,^{o}\text{F}} \times 12 \frac{\text{IN.}}{\text{FT.}} \times 4.1}{0.1 \text{ IN.}} = 8 \frac{\text{BTU}}{\text{HR. FT.}^2\,^{o}\text{C}} \tag{66}$$

Converting to more usable units:

$$\frac{8 \frac{\text{BTU}}{\text{HR. FT.}^2\,^{o}\text{F}} \times 1.8 \frac{\text{F}}{\text{C}}}{3.412 \frac{\text{BTU}}{\text{HR. W}}} = 4.22 \frac{\text{W}}{\text{FT.}^2\,^{o}\text{C}} \tag{67}$$

Now the areas available to each heat pipe was calculated above to be 0.10 ft^2

$$4.22 \frac{W}{FT.^2\ ^oC} \times 0.10\ FT.^2 = 0.42 \frac{W}{^oC} = 2^o \frac{C}{W_{heat\ pipe}} \quad (68)$$

From Case 3 above:

Junction-to-case for DIP	20°C/W DIP
Case-to-heat sink bond:	6°C/W DIP
From above: Heat exchanger	2°C/W heat pipe
Heat Pipe	2°C/W heat pipe

Reference: Kays and London, ibid., p. 104

There are three such heat pipes and 18 DIPS on a module, therefore on a module basis, the total cooling air-to-junction thermal resistance is:

Junction-to-case:

$$\frac{20^o \frac{C}{W_{DIP}}}{18} = 1.11^o \frac{C}{W_{MODULE}} \quad (69)$$

Case-to-heat sink bond:

$$\frac{6^o \frac{C}{W_{DIP}}}{18} = 0.33^o \frac{C}{W_{MODULE}} \quad (70)$$

Heat Pipe

$$\frac{2^{o}\ C}{3} \quad W_{HEAT\ PIPE} = 0.66^{o}\ \frac{C}{W_{MODULE}} \tag{71}$$

Heat Exchanger

$$\frac{2^{o}\ C}{3} \quad W_{HEAT\ PIPE} = 0.66^{o}\ \frac{C}{W_{MODULE}} \tag{72}$$

$$\Sigma = 2.8°C/W\ module \tag{73}$$

For Case 6 summary, see Figure D-12.

D.7 Case 7 (I-2A)

D.7.1 See Figure D-13 for detailed description.

Since these modules may be stacked and the flow passages may be considerable length, the conservative assumption of laminar flow will be made.

From figure 6-3 of the reference, below, with $\alpha = 10$, the limiting N_{NU} is seen to be:

$$N_{Nu} = \frac{h\,D}{k} = 6.8 \quad \text{where} \quad D = \frac{2\,ab}{a+b} = 0.124\ IN. \tag{74}$$

Solving for typical film coefficient:

(75)

$$h = \frac{6.8 \times 0.016\ \frac{BTU}{HR.\ FT.\ ^{o}F} \times 12\ \frac{IN.}{FT.}}{0.124\ IN.} = 11\ \frac{BTU}{HR.\ FT.^{2}\ ^{o}F}$$

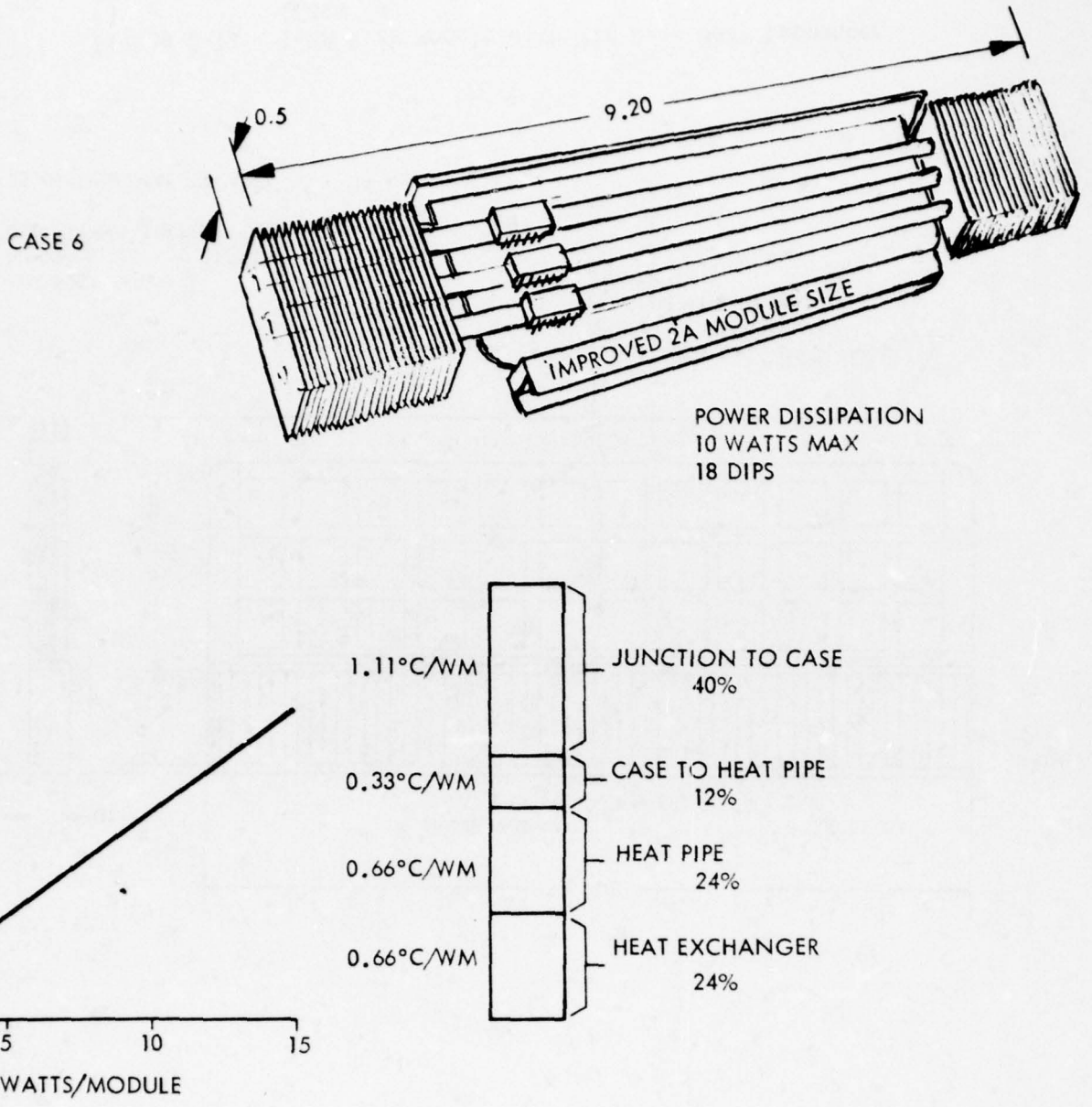
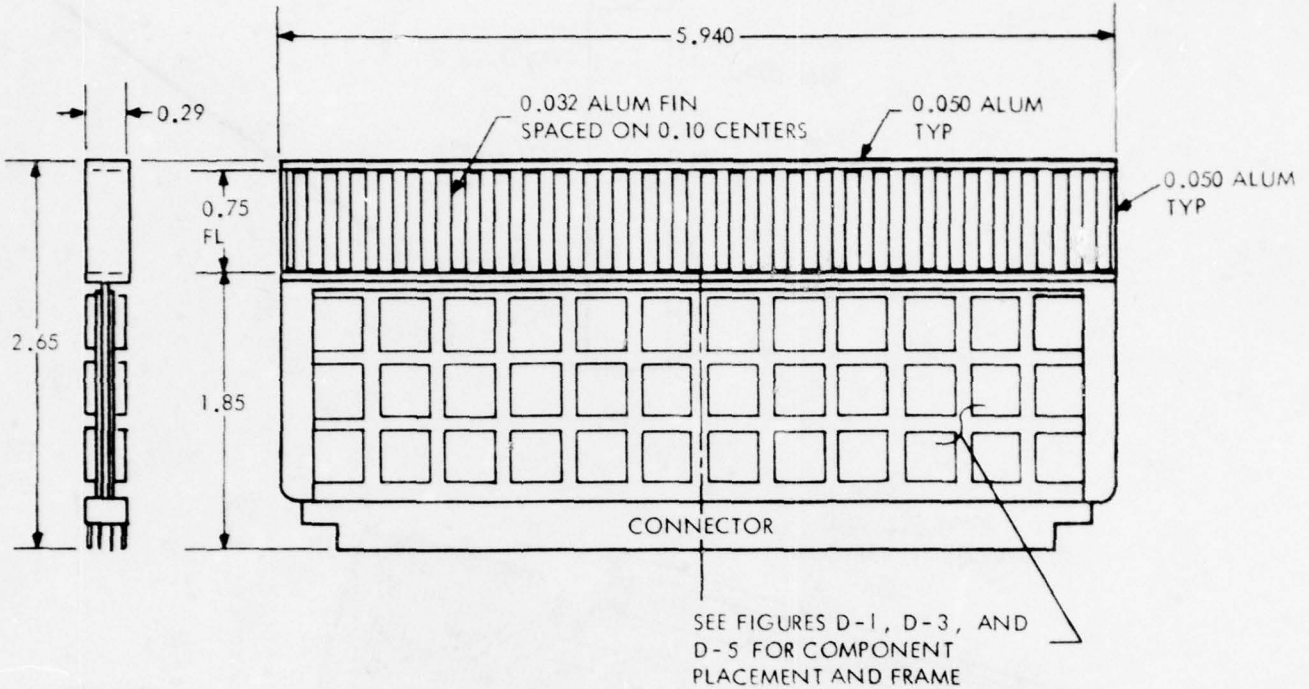


Figure D-12. I-2A Size Module with Heat Pipes, Summary (Case 6)



FIN AREA
$0.290 \times 0.750 = 0.2175\ IN^2$
$0.2175\ IN^2 \times 118$ FIN AREAS $= 25.66\ IN^2$

$25.66\ IN^2$ TOTAL FIN AREA

Figure D-13. I-2A Size Module with Air Over Heat Exchanger (Case 7)

$$h = 0.035 \frac{W}{IN.^2 {}^oC} \tag{76}$$

There are a total of 25.66 in^2 of heat exchange area, so on a module basis:

$$0.035 \frac{W}{IN.^2 {}^oC} \times 25.66 \ IN.^2 = 0.898 \frac{W}{{}^oC} = 1.1^o \frac{C}{W}$$

Aluminum frame (heat sink) temperature rise:

$$\frac{\ell}{kA} = \frac{1.5 \ IN.}{4.35 \frac{W}{IN.{}^oC} \times 0.05 \ IN. \times 0.455 \ IN.} \tag{78}$$

$$= 15^o \frac{C}{W} \ MAX \approx 10^o \frac{C}{W} \ AVERAGE$$

For 10W module with chip carriers:

From Case 1: Junction-to-heat sink (components on one side) 11°C

Power for 3 chip carriers:

$$3 \times 0.278 \ W = 0.834 \ W \tag{79}$$

∴ Max heat sink rise:

$$15^o \frac{C}{W} \times 0.834 \ W = 12.5^o \ C \tag{80}$$

Average heat sink rise: 8°C

From Case 1, components on two sides:

Power/chip carrier = 0.139W

∴ Max heat sink rise	13°C (as above)
Average heat sink rise	8°C (as above)

It is seen that even with the high conductivity, ceramic substrate direct air cooling offers a thermal advantage. The advantage increases, as shown above, for Case 2 when conduction through a glass epoxy board must be included. For Case 7 summary, see Figure D-14.

D.8 Case 8 (HI-2A)

D.8.1 A view of this module is given in Figure D-15.

This single-substrate module is similar to Case 1.1, except for thermal-path width. Substrate width is increased from 1.3 inches (Case 1.1) to 2.2 inches (Case 8), a ratio of 1.7.

There are 60 chip carriers, in similar ratio to Case 1.1. Thermal resistance may therefore be determined by the ratio, as:

$$\text{Case 8: } R_T = \frac{\text{Case 1.1}}{\frac{2.2}{1.3}} = \frac{5.7°C/W}{1.7} = 3.35^{o}\ C/W \qquad (81)$$

D.9 Case 9 (I-2X)

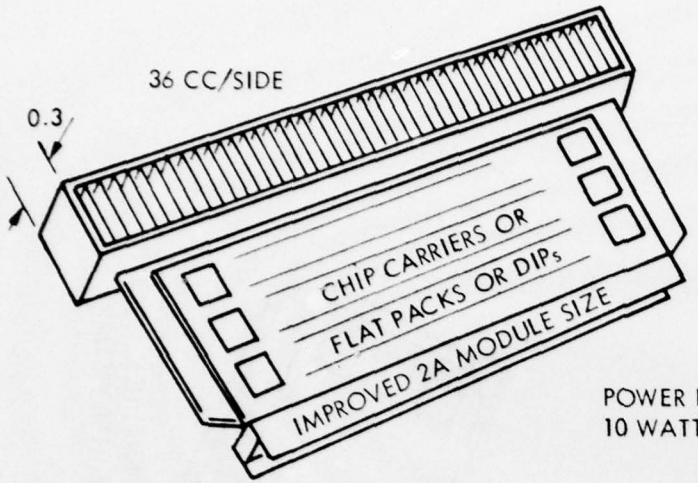
D.9.1 A view of this module is given in Figure D-16.

This single-substrate module is similar to Case 1.6. The thickness of the module heat sink is redesigned to duplicate the performance of Case 8 (HI-2A). Construction and chip-carrier quantity is similar to Case 1.6. Since only the heat-sink thickness is changed, other thermal impedances remain as in Case 1.6. Objective is to lower module thermal resistance from 5°C/W (Case 1.6) to 3.3°C/W (Case 8).

Comparing Case 1.6 and Case 9:

	Case 1.6	Case 9
Junction to case R_t	0.4°C/W	0.4°C/W
Chip carrier bond R_t	0.1	0.1
Through substrate R_t	0	0
Heat sink-to-rib R_t	2.7	0.95*
Guide rib	1.9	1.9
	5.1°C/W	3.35°C/W

*New heat sink-to-rib $R_T = 3.35 - (1.9 + 0.1 + 0.4) = 0.95$ (82)



CASE 7

POWER DISSIPATION
10 WATTS MAX

COOLING AIR THRU HEAT EXCHANGER	COMPONENTS ONE SIDE	COMPONENTS TWO SIDES
JUNCTION TO HEAT SINK	11° C	6° C
HEAT SINK RISE	13° C	13° C
HEAT SINK TO AIR	11° C	11° C
	35° C	30° C
DIRECT FORCED - CONVECTION COOLING OF COMPONENTS (CASE 1)	29° C	14° C

Figure D-14. I-2A Size Module, with Air Over Heat Exchanger, Summary (Case 7)

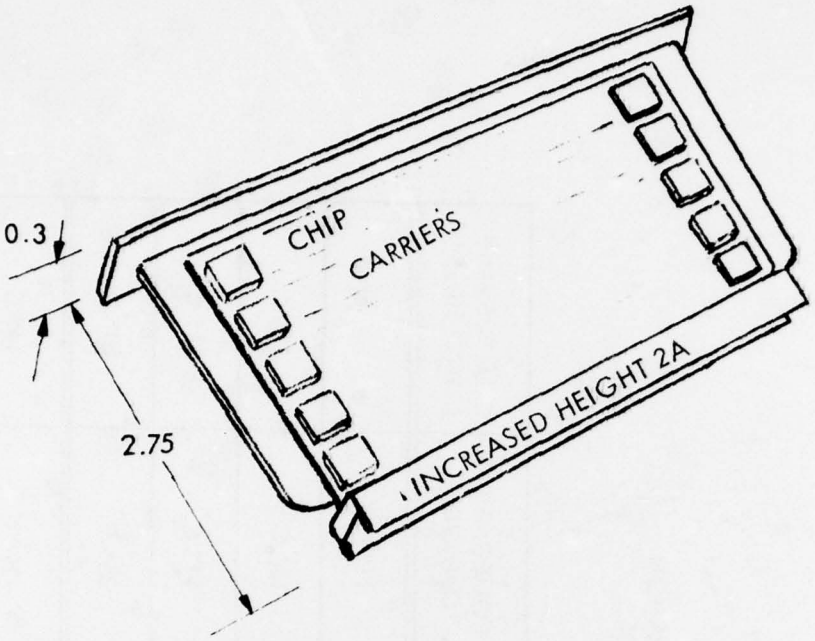


Figure D-15. HI-2A Size Module (Case 8)

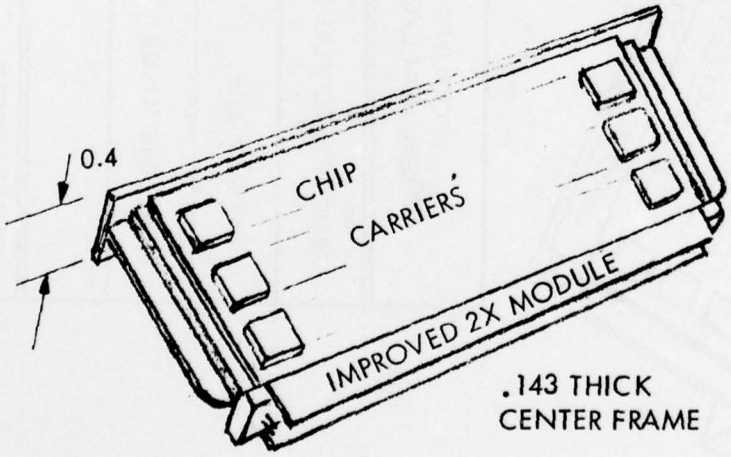


Figure D-16. I-2X Size Module (Case 9)

$$\therefore \text{ New heat sink thickness } = \frac{2.7}{0.95} \times 0.05 \text{ in.} = 0.143 \text{ inches} \qquad (83)$$

D.10 Case 10 (I-2B)

D.10.1 A view of this module is given in Figure D-17.

This module is configured like I-2B, with double guide-ribs, and 0.1 inch heat sink. The module could be compared to a double version of the single-sided I-2A, made with chip carriers. The guide-rib interface, heat-sink thickness, and chip carrier quantities are all twice the case values of 1.1.

The thermal resistance of Case 10 can be closely approximated as one-half that of Case 1.1:

$$\text{For Case 1.1: } R_t = \frac{57°C}{10W} = 5.7°C/W \qquad (84)$$

For Case 10:

Junction-to-case R_t	4°C
Chip carrier bond R_t	1°C
Through substrate	0
Heat sink rise	13.5 (one-half Case 1.6 value)
Rib-to-case	9.5 (two sets of guide ribs)
	28.0°C, or 2.8°C/W

$$\text{Case 10 } R_t = \frac{5.7°C/W}{2} = 2.8°C/W \qquad (85)$$

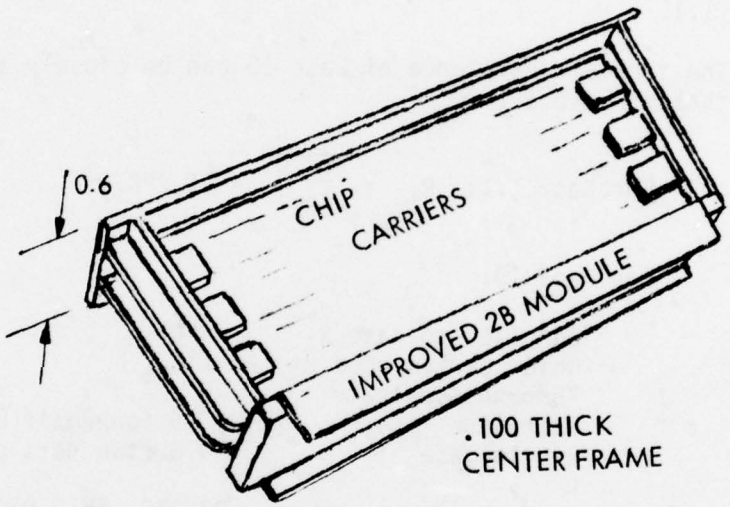


Figure D-17. I-2B Size Module (Case 10)

APPENDIX E

AEW INTEGRATED RACK THERMAL ANALYSIS

APPENDIX E

AEW INTEGRATED RACK THERMAL ANALYSIS

Power: 2642 W = 9014 BTU/hr

Weight rate of cooling air flow for $8^{o}C$ rise:

$$W = \frac{9014 \frac{BTU}{hr}}{0.241 \frac{BTU}{lb\ ^{o}F} \times 14.40^{o}F \times 60 \frac{min}{hr}} = 43 \frac{lb}{min}$$

Using fan standard air density of $0.075 \frac{lb}{ft^3}$ this corresponds to a flow of:

$$\frac{43 \frac{lb}{min}}{0.075 \frac{lb}{ft^3}} = 577 \text{ cfm}$$

Horsepower required with a 40% efficient fan-motor, assuming a 2 in.H_2O p:

$$HP = \frac{577 \text{ cfm} \times 2 \text{ in.} H_2O}{6356 \frac{\text{cfm in.} H_2O}{HP} \times 0.4} = 0.45 \text{ HP}$$

Calculation of pressure drop in 2.7 in. x 5.4 in. supply duct:

Frictional loss in duct interior:

$$P = 4 \frac{fL}{D} \times \frac{PV^2}{2g}$$

$$D = \frac{4A}{P} = \frac{4 \times 2.7 \text{ in.} \times 5.4 \text{ in.}}{2 (2.7 \text{ in.} + 5.4 \text{ in.})} = 3.6 \text{ in.} = 0.3 \text{ ft.}$$

$$N_{RE} = \frac{\rho DV}{\mu} = \frac{0.075 \text{ lb} \times 0.3 \text{ ft} \times 95 \frac{\text{ft}}{\text{sec}}}{1.3 \text{ ft}^3 \times 10^{-5} \frac{\text{lb}}{\text{ft sec}}} = 1.64 \times 10^5$$

$$V = \frac{Q}{A} = \frac{9.62 \frac{\text{ft}^3}{\text{sec}}}{\left(\frac{2.7 \times 5.4}{144}\right) \text{ft}^2} = 95 \frac{\text{ft}}{\text{sec}}$$

$$f = 0.004$$

$$\Delta P = \frac{4 \times 0.004 \times \left(\frac{39}{12}\right) \text{ft} \times 0.075 \frac{\text{lb}}{\text{ft}^3} \left(95 \frac{\text{ft}}{\text{sec}}\right)^2}{0.3 \text{ ft} \times 2 \times 32.2 \frac{\text{ft}}{\text{sec}^2}} =$$

$$1.82 \frac{\text{lb}}{\text{ft}^2} = 0.351 \text{ in.} H_2O$$

Mean V^2: $V = \left(1 - \frac{X}{L}\right) Vo$

where Vo is air velocity on entering duct, and L is duct length

$$V^2 \text{ mean} = \frac{Vo^2}{L} \int_0^L \left(\frac{L-X}{L}\right)^2 \partial x =$$

$$\frac{Vo^2}{L^3} \int_0^L \left(L^2 - 2xL + X^2\right) \partial x =$$

$$\frac{Vo^2}{L^3} \Big|_0^L \left| L^2X - X^2L + \frac{X^3}{3} \right| = \frac{V_o^2}{3}$$

$$\therefore \Delta p = \frac{0.351 \text{ in.} H_2O}{3} \approx 0.1 \text{ in.} H_2O$$

This pressure drop is sufficiently small to have negligible impact on the system. Sizing of distribution orifices:

$$\Delta p_s = C_D \frac{\rho V^2}{2g}$$

where C_D = 2.80 for square-edged orifice

Assuming: p_s = 0.5 H_2O = 2.597 $\frac{lb}{ft^3}$ and solving for V:

$$V = \sqrt{\frac{2g\Delta p}{C_D \times \rho}}$$

$$= \sqrt{\frac{2 \times 32.2 \times 5.193 \times 0.5}{2.8 \times 0.075}}$$

$$= 28 \frac{ft}{sec}, \text{ or } 1693 \frac{ft}{min}$$

$$Q = AV$$

where:

Q is flow in cfm

A is orifice area in ft^2

V is velocity in $\frac{ft}{min}$

$$A = \frac{Q}{V} = \frac{557 \text{ cfm} \times 144 \frac{in^2}{ft^2}}{258 \text{ slots} \times 1693 \frac{ft}{min}} = 0.184 \text{ in}^2$$

If slot is 2.15 in. long, then the width is:

$$\frac{0.184 \text{ in}^2}{2.15 \text{ in}} = 0.085 \text{ in.}$$

Approximate heat exchanger sizing

Air-side volume:

Assumption $\Delta t = 10°F$

Calculation of N_R for heat exchanger:

$$\text{Face area} = \frac{14 \times 4.3}{144} = 0.42 \text{ ft}^2$$

Air flow - minimum free-flow area $= 0.31 \text{ ft}^2$

$$G = \frac{43 \frac{\text{lb}}{\text{min}} \times 60 \frac{\text{min}}{\text{hr}}}{0.31 \text{ ft}^2} = 8323 \frac{\text{lb}}{\text{hr ft}^2}$$

$$N_R = \frac{4 r_h G}{\mu} =$$

$$\frac{*0.00615 \text{ ft} \times 8322 \frac{\text{lb}}{\text{hr ft}^2}}{0.05 \frac{\text{lb}}{\text{hr ft}}} = 1024$$

$$\frac{h_c}{G c_p} N_{PR}^{\frac{2}{3}} = 0.0057$$

$$h_c = \frac{0.0057 \text{ G } c_p}{N_{PR}^{\frac{2}{3}}}$$

$$= \frac{0.0057 \times 8323 \frac{\text{lb}}{\text{hr ft}^2} \times 0.241 \frac{\text{BTU}}{\text{lb °F}}}{0.7}$$

*Assuming Kays and London 10-30 surface.

$$= 16 \frac{BTU}{hr\ ft^2\ °F}$$

*Assumes typical limiting Nusselt Number for laminar flow (high efficiency heat exchange) $Q = H_c A \Delta t$ (basic convection formula).

Solving for A:

$$A = \frac{Q}{h_c \Delta t} = \frac{9014 \frac{BTU}{hr}}{16 \frac{BTU}{hr\ ft^2\ °_f} \times 10°F} = 56\ ft^2$$

With a volumetric efficiency of $561 \frac{ft^2}{ft^3} = 0.1\ ft^3$ the air-side heat

exchanger volume would be:

$$\frac{56\ ft^2}{561 \frac{ft^2}{ft^3}} = 0.1\ ft^3$$

The liquid side of the heat exchanger would be approximately 35% of this volume, so that together with the headers, the heat exchanger volume would be about $0.25\ ft^3$ to handle 2642 W.

Pressure drop through this heat exchanger:

$f = 0.019$, from Figure 10-30 of Kays and London, referenced above.

$$\Delta p = \frac{G^2 f}{2gcP} \frac{A}{A_c}$$

$$= \left(2.312 \frac{lb}{sec\ ft^2} \right) \frac{0.019 \times 56\ ft^2}{0.355\ ft^2 \times 2 \times 32.2 \frac{ft}{sec^2} \times 0.075 \frac{lb}{ft^2}}$$

$$= 3.1317 \frac{lb}{ft^2} \text{ or } 0.64 \text{ in.} H_2O$$

This value is reasonable, and in line with a total system drop of 2 in.H_2O. (For design purposes, entrance and exit loss would also be calculated.)

Emergency operation after ECS failure:

The outside area of the integrated rack is:

$$2 (72 \text{ in} \times 22.6 \text{ in}) + 2 (4.5 \text{ in} \times 72 \text{ in}) = 3902 \text{ in}^2 = 27 \text{ ft}^2$$

(Only vertical faces are included.)

The temperature rise of the integrated rack above cabin temperature, assuming a combined radiative and natural convection coefficient of $4 \frac{BTU}{hr\ ft^2\ °F}$ would be:

$$Q = h_t A \Delta t$$

$$\therefore \Delta t = \frac{Q}{hA} = \frac{9014 \frac{BTU}{hr}}{4 \frac{BTU}{hr\ ft^2\ °F} \times 2\ ft^2 \times 1.8 \frac{°F}{°C}}$$

$$= 46°C$$

Ref: London, A.L. and Kays, W., "Compact Heat Exchangers," McGraw-Hill, Second Edition, pp. 183-227.

There will be an additional rise in temperature of the internal loop air above the rack sides of about half the above. Thus during emergency operation (no ECS or no liquid circulation between rack heat exchanger and ECS), for example, a 21°C cabin temperature would result in the internal loop steady-state air temperature:

$$T_{internal} = 21°C + 23°C + 46°C = 90°C$$

(cabin + internal Δt + external Δt)

An internal rack air temperature of 90°C would permit continued operation without damage to the electronics in the event of an ECS failure. It is true that without ventilation the cabin temperature of the aircraft would climb to higher levels. The thermal time constant for such a change would be expected to be several hours. It is probable that emergency operation of the equipment without serious damage would be possible for any single mission.

The above assumed heat transfer coefficients may prove a bit high. However, more than offsetting any under optimism is this factor will be the high local heat transfer coefficients over the components themselves due to the forced-convection within the integrated rack. It is highly probable that emergency-condition component temperatures will fall under vendor-recommended maximum values.

APPENDIX F

ROVAC CORPORATION LETTER

11 October 1977

Subject: ROVAC Air Cycle Machine Technology
(Military Cooling Applications)

THE ROVAC CORPORATION

ROVAC INDUSTRIAL CENTER • 100 ROVAC PARKWAY • ROCKLEDGE, FLORIDA 32955
TELEPHONE 305/631-0300 • TELEX 56-4444

October 11, 1977

Dr. Earl Gale
General Electric Co.
French Road
Utica, New York 13502

Subject: Summary of ROVAC's Air Cycle Machine Technology for Military Cooling Applications

Reference: October 7, 1977 telecon between Dr. Gale and Mr. Bomstad

Dear Dr. Gale:

I enjoyed talking with you during the referenced telecon regarding the state of development of ROVAC technology as related to military applications. Per your request, I am pleased to submit a summary of this emerging technology for possible inclusion in a modular avionics packaging study that you are performing for the Navy.

To date the U. S. Air Force (AFFDL, WPAFB, Ohio) has purchased five ROVAC positive-displacement rotary-vane air cycle machines (Circulators) under four separate contracts, dating back to 1973. The first and second machines were for feasibility assessment purposes and will not be discussed in this summary.

The third Air Force contract (F33615-74-C-3096) granted to The ROVAC Corporation was an exploratory development program to generate two breadboard Circulators (Models 604 and 605) designed for application in an F-15 sized environmental control system (ECS). Performance testing conducted at the Air Force Flight Dynamics Laboratory clearly showed that the ROVAC Circulator can be more efficient than existing well-developed turbomachinery. An indication of air cycle machine performance for military aircraft use is the compressor adiabatic efficiency multiplied by the expander adiabatic efficiency, sometimes called the "product efficiency". Existing air cycle turbomachinery typically gives a product efficiency of 50 percent. However, the ROVAC Circulator in its early stages of development demonstrated product efficiencies on the order of 90 percent. Additional details on this contract are given in Technical Report number AFFDL-TR-77-6.



The fourth and present Air Force contract in which ROVAC is a sub-contractor to McDonnell Aircraft Company (MCAIR) involves the development of one breadboard and two brassboard flight qualifiable ROVAC Circulators for an advanced closed cycle ECS for the F-15 aircraft. MCAIR performed the system analysis and fabricated the F-15 closed cycle test system and the Air Force will be performing the performance testing. The breadboard machine (Model 607) was delivered on August 19, 1977 and preliminary testing indicates an improvement over previous models. This contract is scheduled for completion in October, 1978.

During the Air Force programs there was a most noteworthy reduction in the weight of the F-15 sized Circulator. (These machines were designed for an approximate 11 ton cooling capacity.) The weight dropped from 135 lb for the Model 604 to 55 lb for the recently delivered Model 607. The ROVAC Circulator is now competitive in size and weight to the existing variable-geometry turbomachine for the same capacity rating.

The ROVAC Corporation also recently completed an exploratory development program with the Army Mobility Equipment Research and Development Command (MERDC) for the generation of a state-of-the-art ROVAC closed cycle system for Army mobile application assessment. Previous Army work on a well-developed shaft-driven turbomachine air cycle system displayed an overall coefficient of performance (COP) of 0.3 to 0.35, according to the Army. Under the same test conditions the ROVAC machine (Model 606) demonstrated a COP of 0.6 excluding the electrical efficiency. Assuming this efficiency to be approximately 0.85 and parasitic losses of 350 watts/ton, the overall COP of the ROVAC system was in excess of 0.5; an improvement of approximately 50 per cent over the well-developed turbomachine equipped system. Under equivalent operating conditions it was estimated (based on Army test data) that the extremely well-developed vapor cycle system presently used by the Army gives a COP of approximately 0.85. Thus, it is apparent that even with a Circulator design over two years old, the ROVAC system has already beat the best previously developed air cycle technology and is now beginning to compete with the very best vapor cycle technology.

The Company is presently under a research and development contract with the Navy (NADC, Warminster, Pa.) to produce an engineering prototype ROVAC personal cooling generator for the pilot and co-pilot in an SH-3 helicopter. Results of this program will be available in mid 1978.

Details on the advantages of the ROVAC closed loop ECS for military high performance aircraft are given in a paper entitled "Performance of a New Positive Displacement Air Cycle Machine" which I recently sent you. In short the closed loop ECS (as compared to the open loop ECS) is potentially less costly and reduces the aircraft power penalty by approximately four times.

In addition to military applications, the Company is also developing an automotive ROVAC system. Light pilot production has already begun and distribution of a limited number of the systems will take place in late 1977 and early 1978. This is a closed loop variable capacity system designed for the automotive aftermarket.

I hope this information will aid in your study. If it is inadequate in any way please feel free to call.

Thank you and please know that we appreciate your interest.

Sincerely,

The ROVAC Corporation

Wayne R. Bomstad, P.E.
Vice President Engineering

WRB:pm

APPENDIX G

ENVIRONMENTAL CONTROL SYSTEM STUDY

AIRESEARCH MANUFACTURING
(GARRETT)

V/STOL A AIRCRAFT DEFINITION

FLIGHT ENVELOPE

MAXIMUM SPEED

250 KNOTS AT SEA LEVEL

0.6 MACH AT OPTIMUM CRUISE ALTITUDE

0.8 MACH AT 20,000 FEET

CONFIGURATIONS

TRANSPORT – 4 CREW + 23 PASSENGERS

TANKER – 3 CREW

ASW – 3 CREW + 22 KW AVIONICS

AEW – 4 CREW +___ AVIONICS

REVIEW ENERGY SOURCES AND HEAT SINKS FOR ECS

PRESSURIZED AIR SOURCES

- ENGINE COMPRESSOR BLEED
- DRIVEN COMPRESSOR
  - ENGINE
  - HYDRAULIC
  - ELECTRIC
  - AIR TURBINE
- AUXILIARY POWER UNIT COMPRESSOR

HEAT SINKS

- AMBIENT AIR
  - RAM AIR
  - ENGINE FAN AIR
- FUEL
- EXPENDABLES
  - WATER
  - OTHERS

COOLING AIR MOVERS

- ELECTRIC MOTOR FAN
- TURBOFAN
- HYDRAULIC MOTOR FAN
- FAN SHAFT-DRIVEN BY AIRCYCLE MACHINE
- EJECTOR PUMP

GARRETT

S-15940

SUMMARY OF OBJECTIVES FOR MILITARY ECS

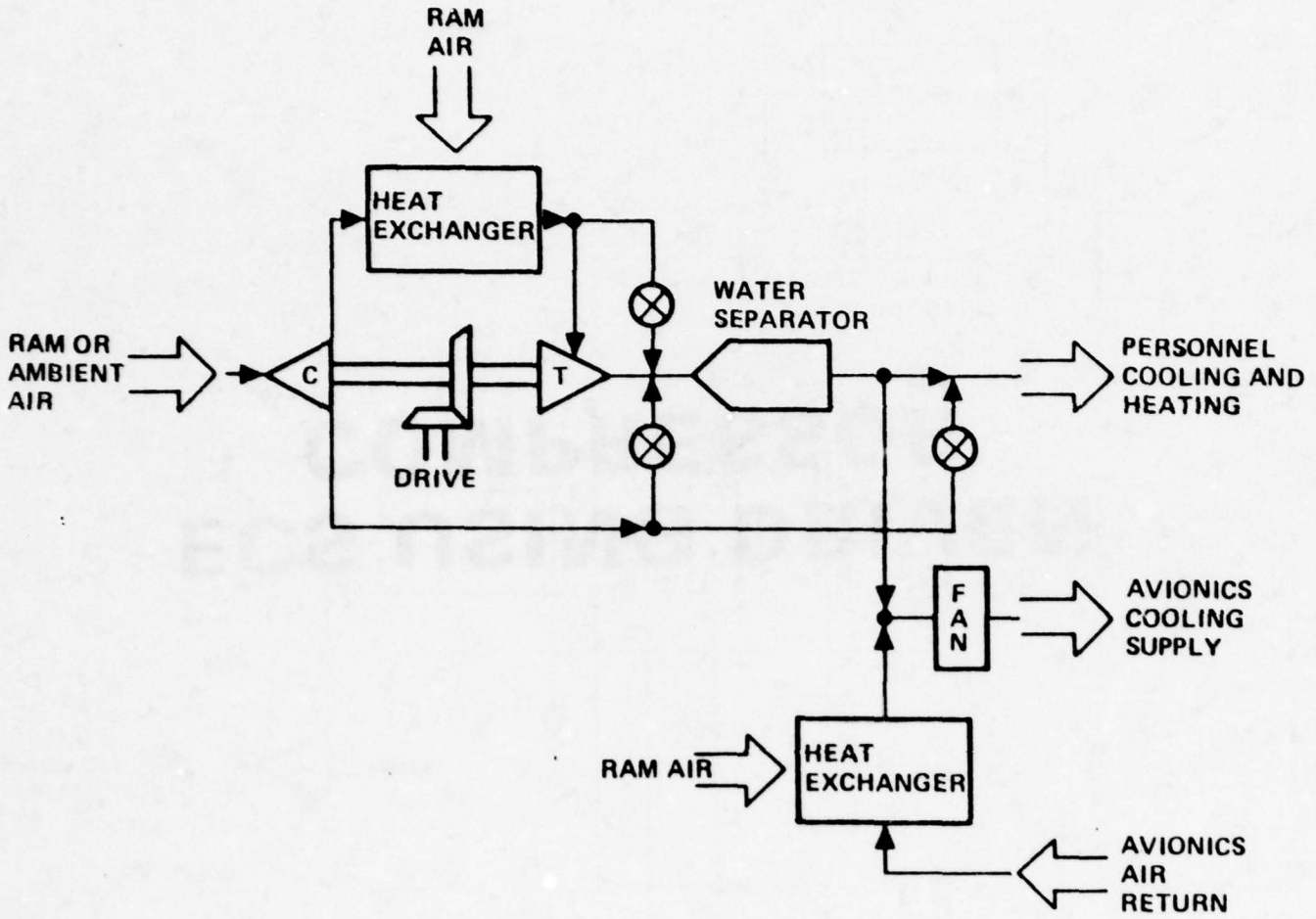
- REDUCE DIRECT OPERATING COSTS
  - MINIMUM PENALTY
  - LOW MAINTENANCE
- MINIMIZE WEIGHT
- MAXIMIZE AVAILABILITY
  - HIGH RELIABILITY
  - HIGH TURNAROUND EFFICIENCY
- MINIMIZE VOLUME
- REDUCE COMPLEXITY AND CREW WORKLOAD
- MAXIMIZE SYSTEM ADAPTABILITY
  - CONTROLS COMPATIBILITY WITH VARIOUS SYSTEM CONFIGURATIONS
  - GROWTH POTENTIAL

ENGINE BLEED VERSUS ENGINE DRIVEN COMPRESSOR
SELECTION CRITERIA

- WEIGHT
- RELIABILITY
- PERFORMANCE
- FUEL PENALTY
- COST
- MAINTAINABILITY

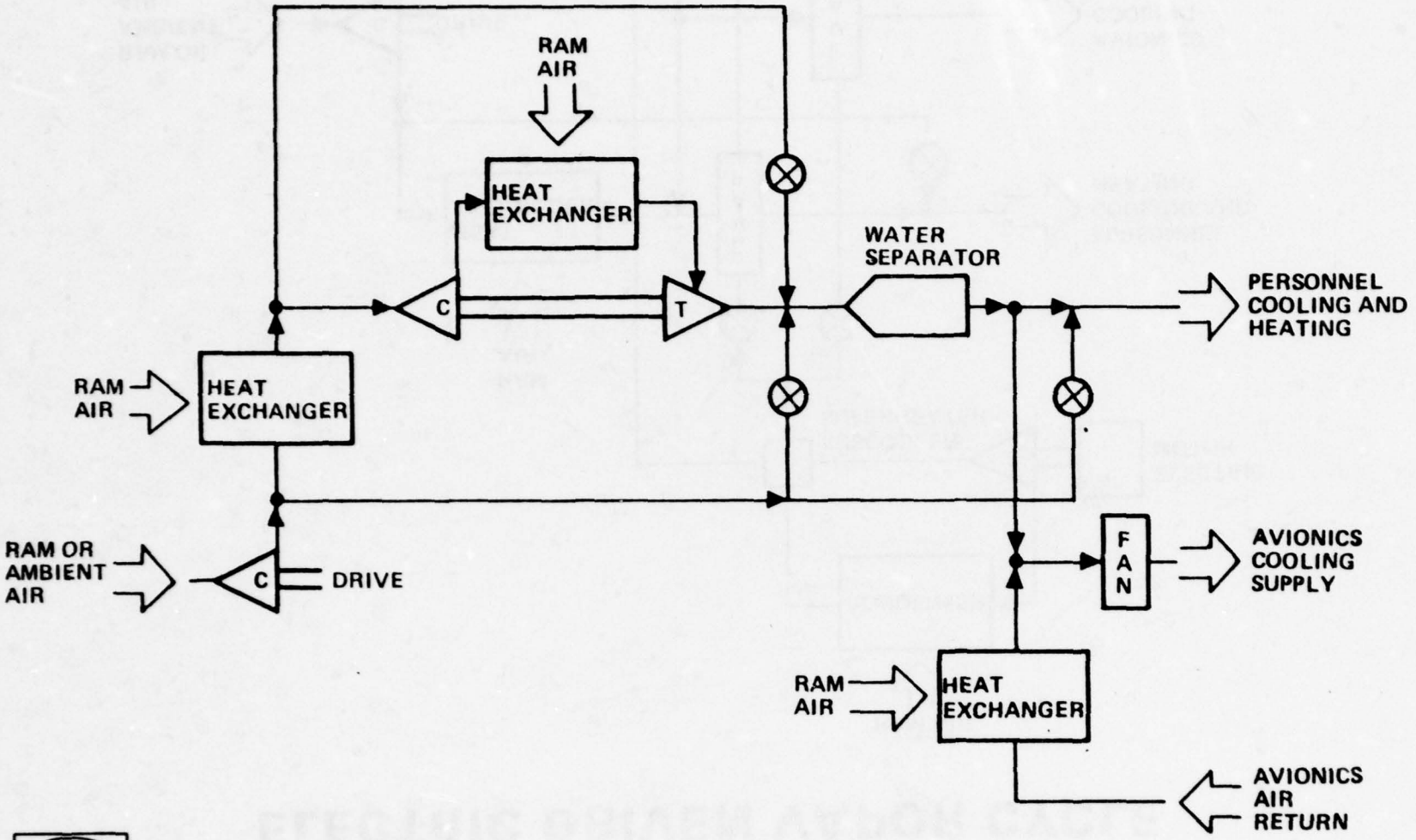
ECS USING DRIVEN COMPRESSOR

OPEN LOOP POWER DRIVEN AIR CYCLE MACHINE



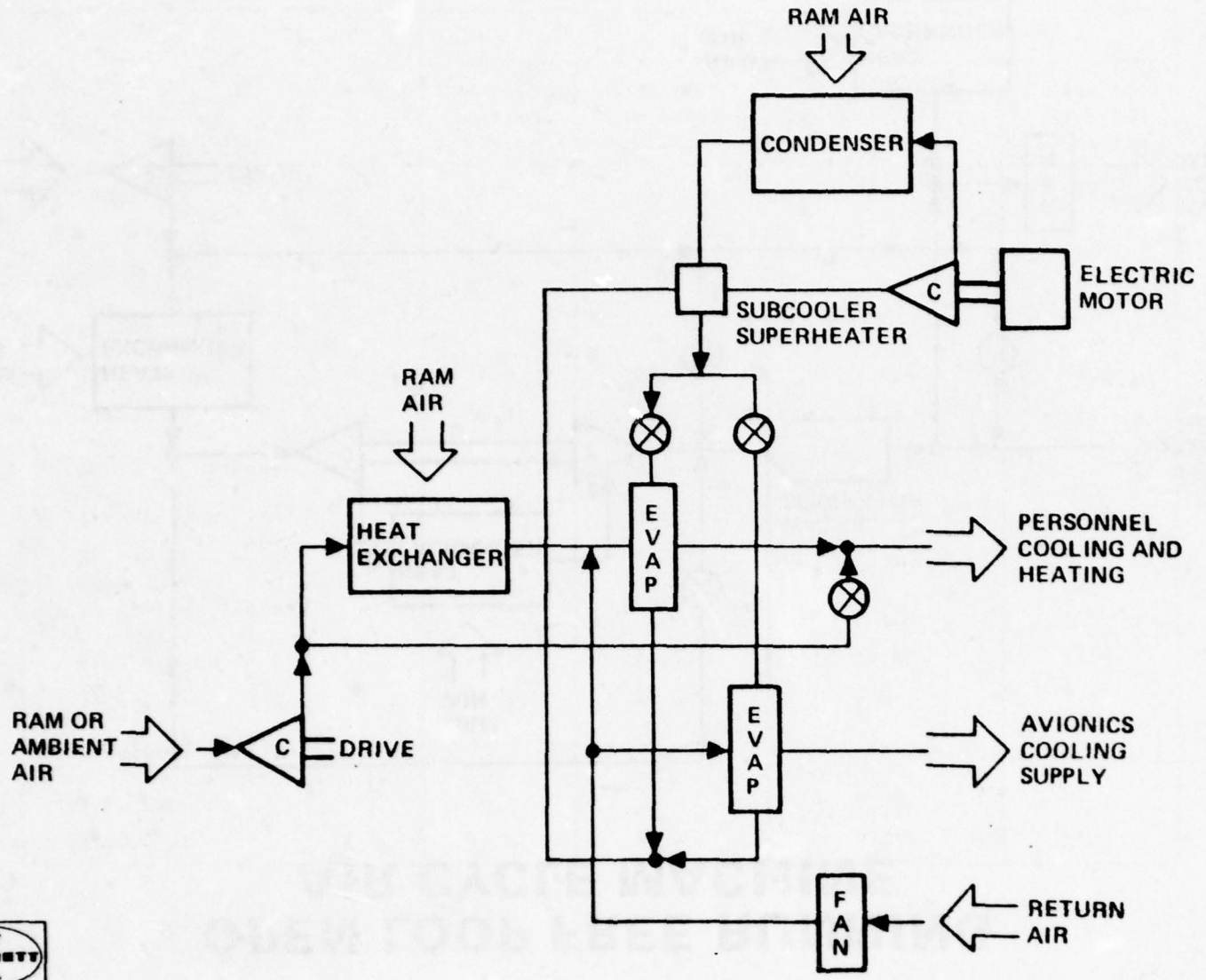
S-15943

OPEN LOOP FREE RUNNING AIR CYCLE MACHINE

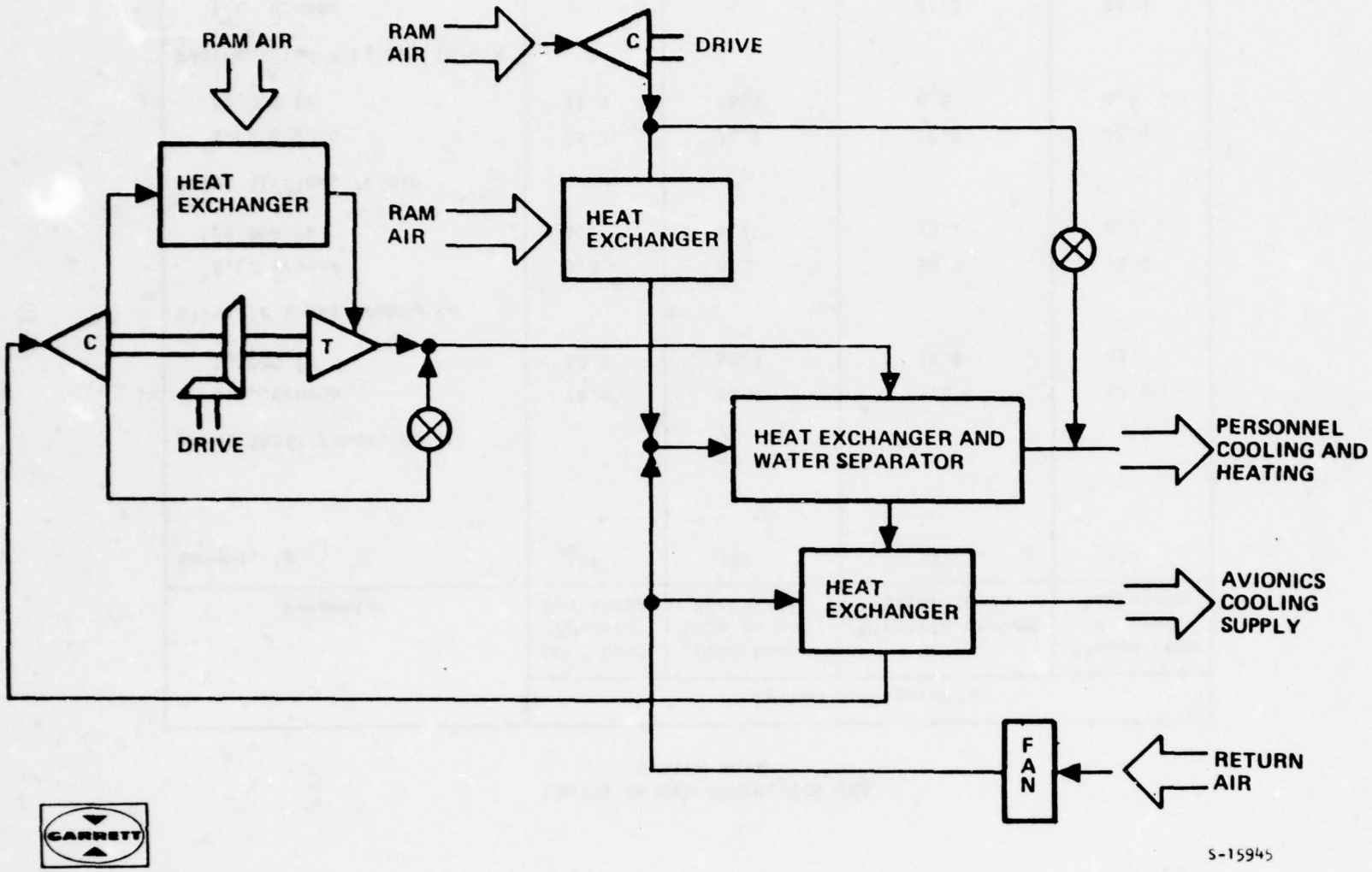


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ELECTRIC DRIVEN VAPOR CYCLE



CLOSED LOOP POWER DRIVEN AIR CYCLE MACHINE



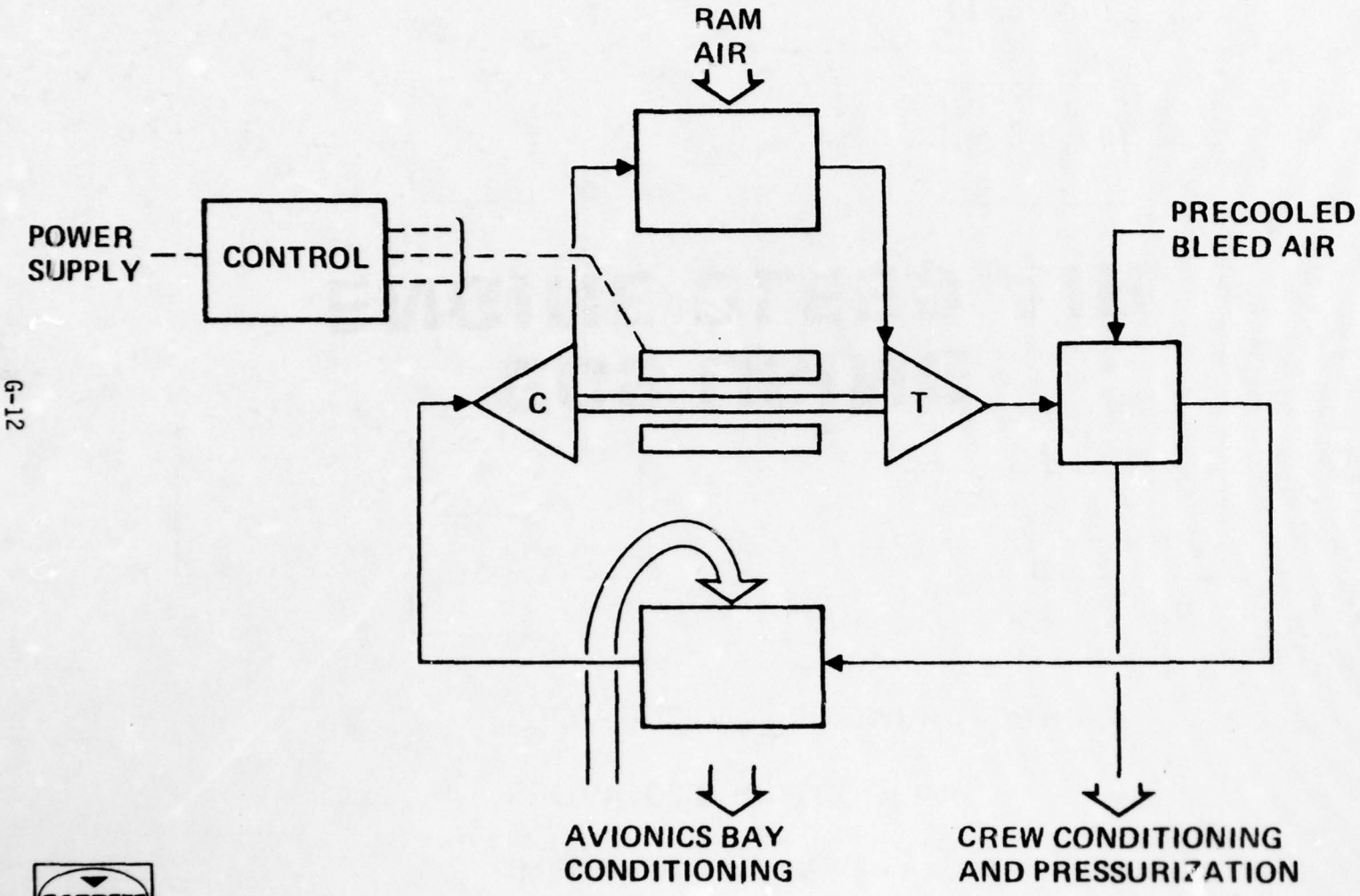
S-15945

ENGINE DRIVEN COMPRESSOR ECS
SYSTEM DATA

Parameter	System Configuration			
	Open Loop Powered Bootstrap	Open Loop Free Running Bootstrap	Electric Driven Vapor Cycle	Closed Loop Powered Bootstrap
Weight, lb	139	152	197	179
Input Shaft Power, hp				
S.L. Ground	78.6	88.1	1.2	64.6
35,000 Ft	50.7	50.7	12.2	42
Electric Input Power, kw				
S.L. Ground	6.5	6.5	38.5	13.8
38,000 Ft	4.1	4.1	15.1	6.0
Fresh Airflow, lb/min				
S.L. Ground	76.7	76.7	12.8	12.8
35,000 Ft	26.5	26.5	6.6	6.6
Recirculated Airflow, lb/min				
S.L. Ground	-	-	91.5	91.5
35,000 Ft	51.4	51.4	71.3	71.3

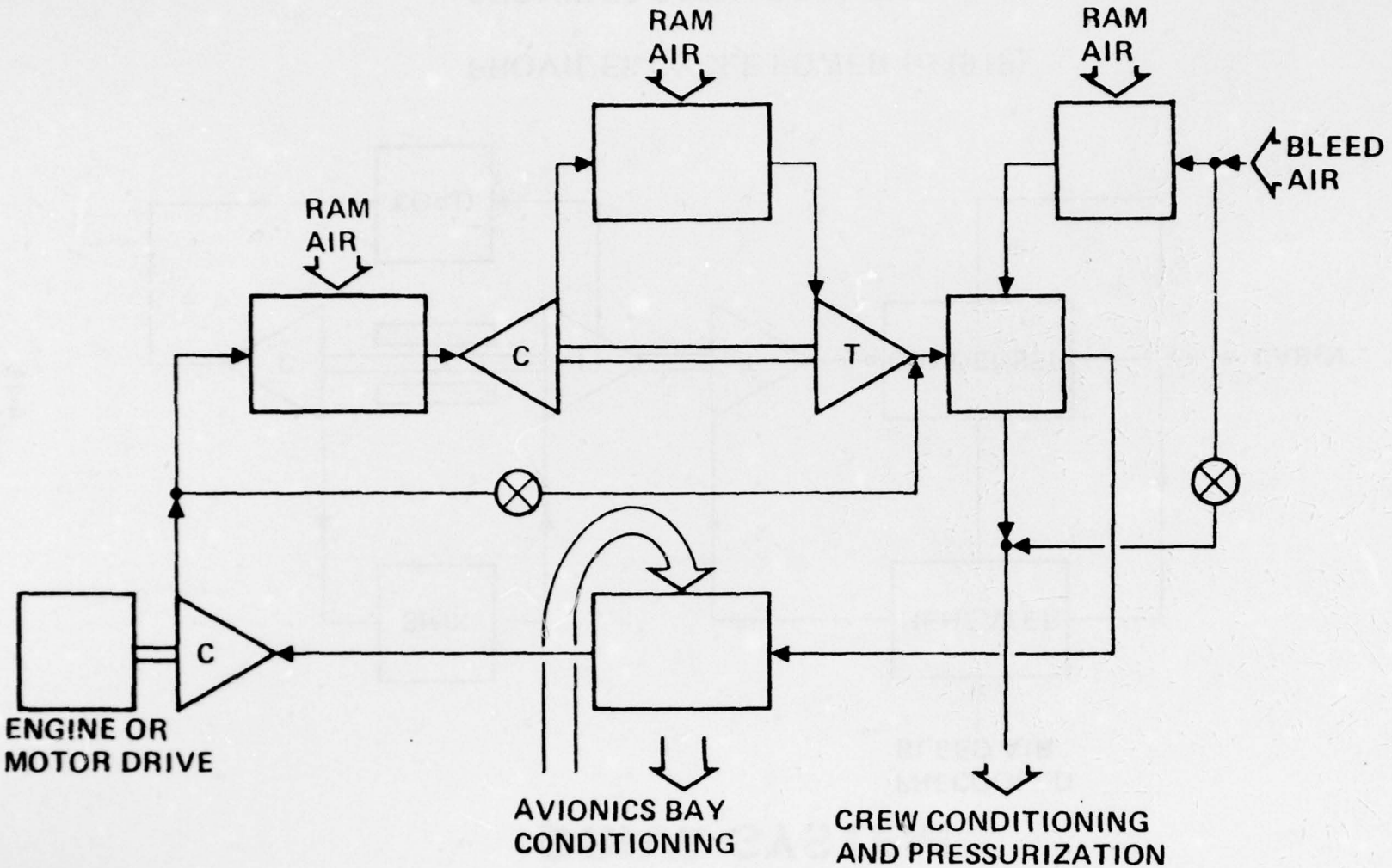
ECS USING ENGINE BLEED AIR

CLOSED LOOP POWER DRIVEN AIR CYCLE MACHINE



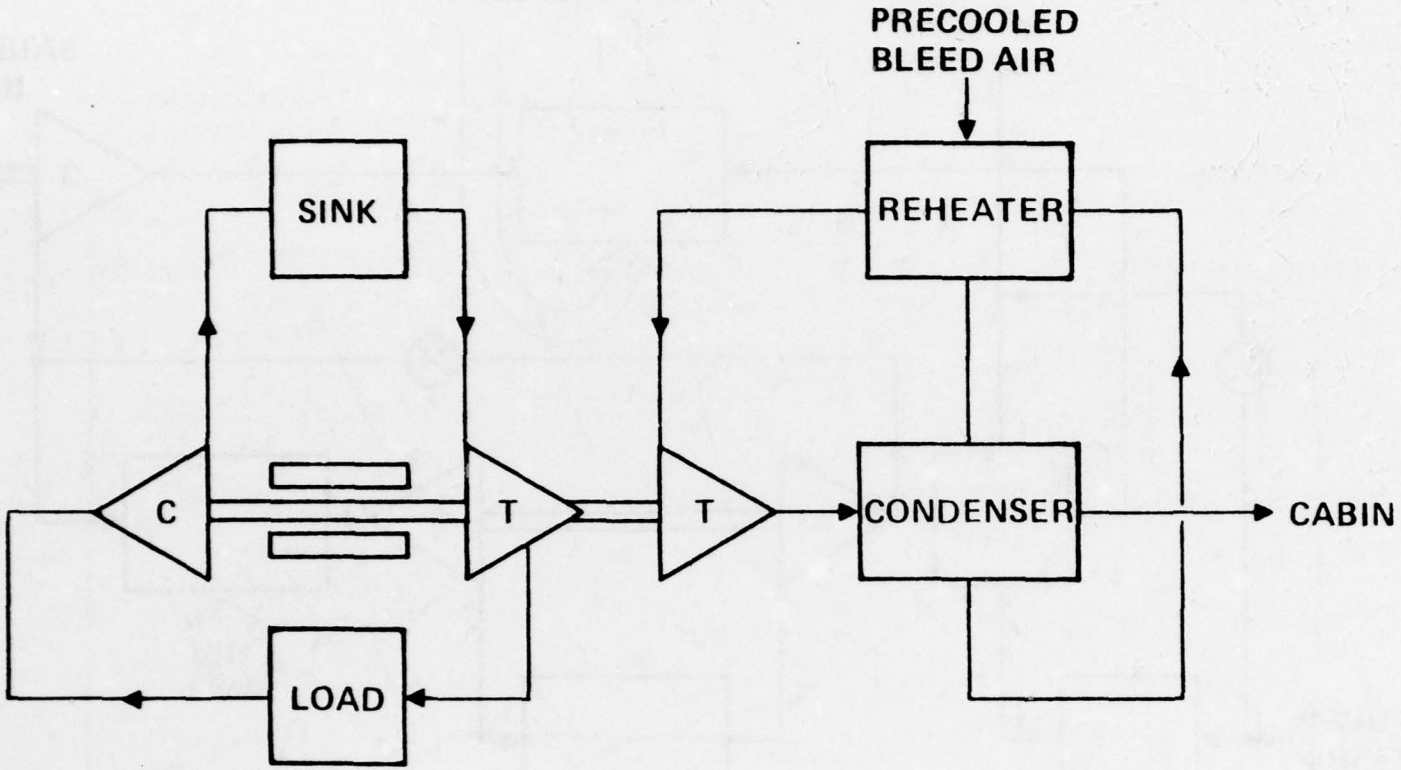
S-14355

CLOSED LOOP FREE RUNNING AIR CYCLE MACHINE



S-14356

INTEGRATED ELECTRO-PNEUMATIC DRIVE SYSTEM



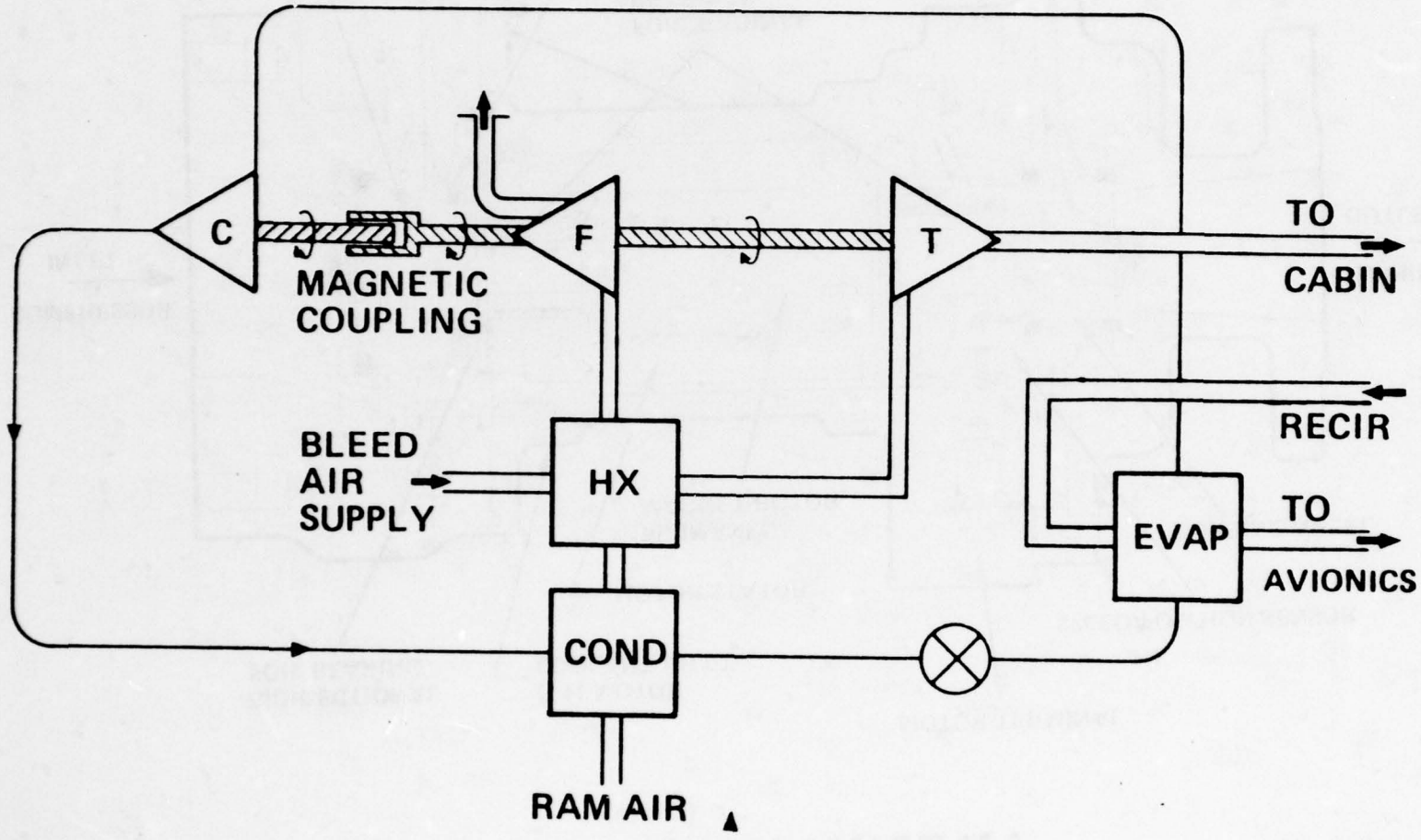
PROVIDES CYCLE POWER (≈19 HP)

PROVIDES CABIN COOLING

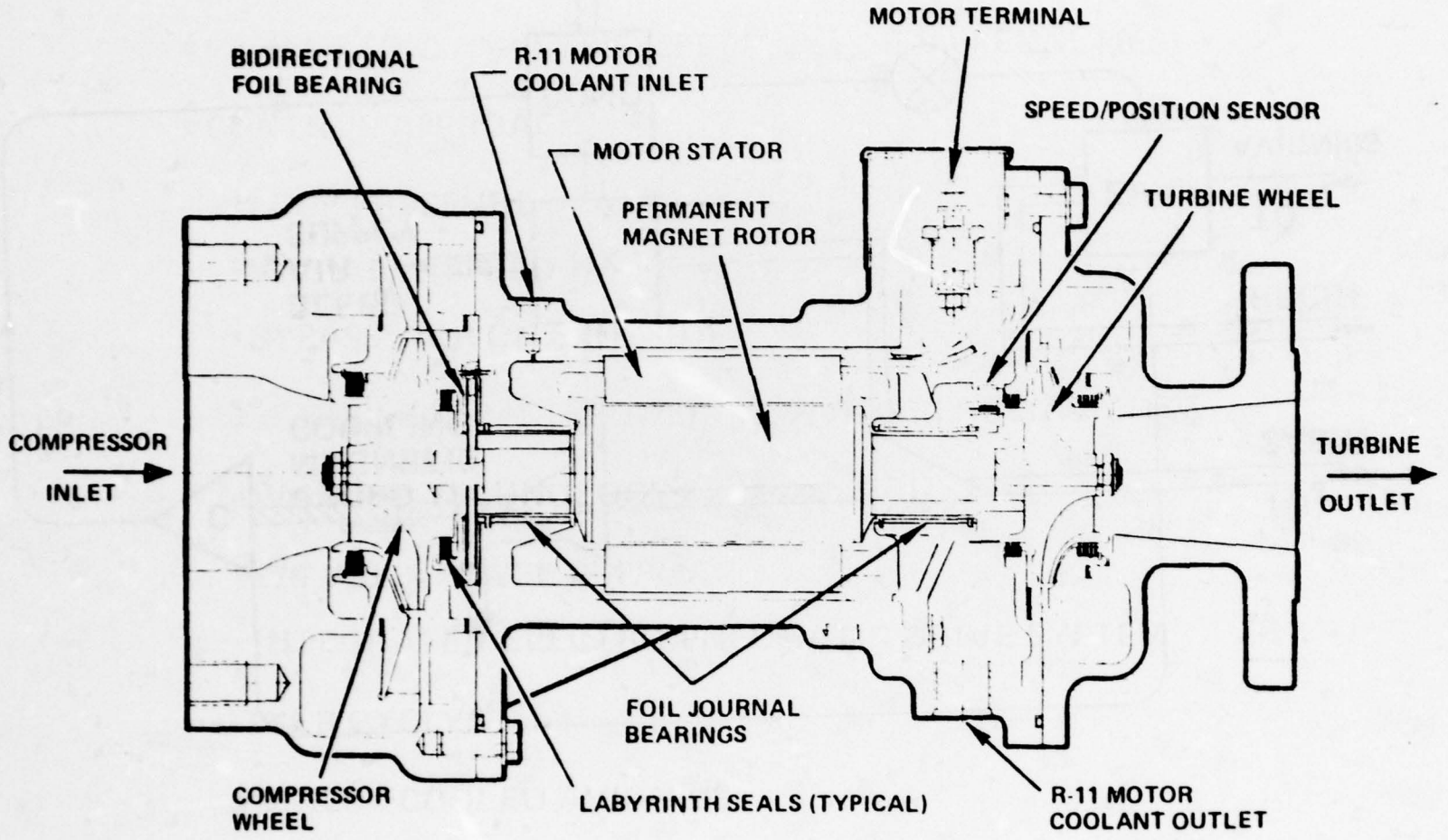
IMPROVED CYCLE PERFORMANCE

S-14362

COMBINATION VAPOR-AIR CYCLE

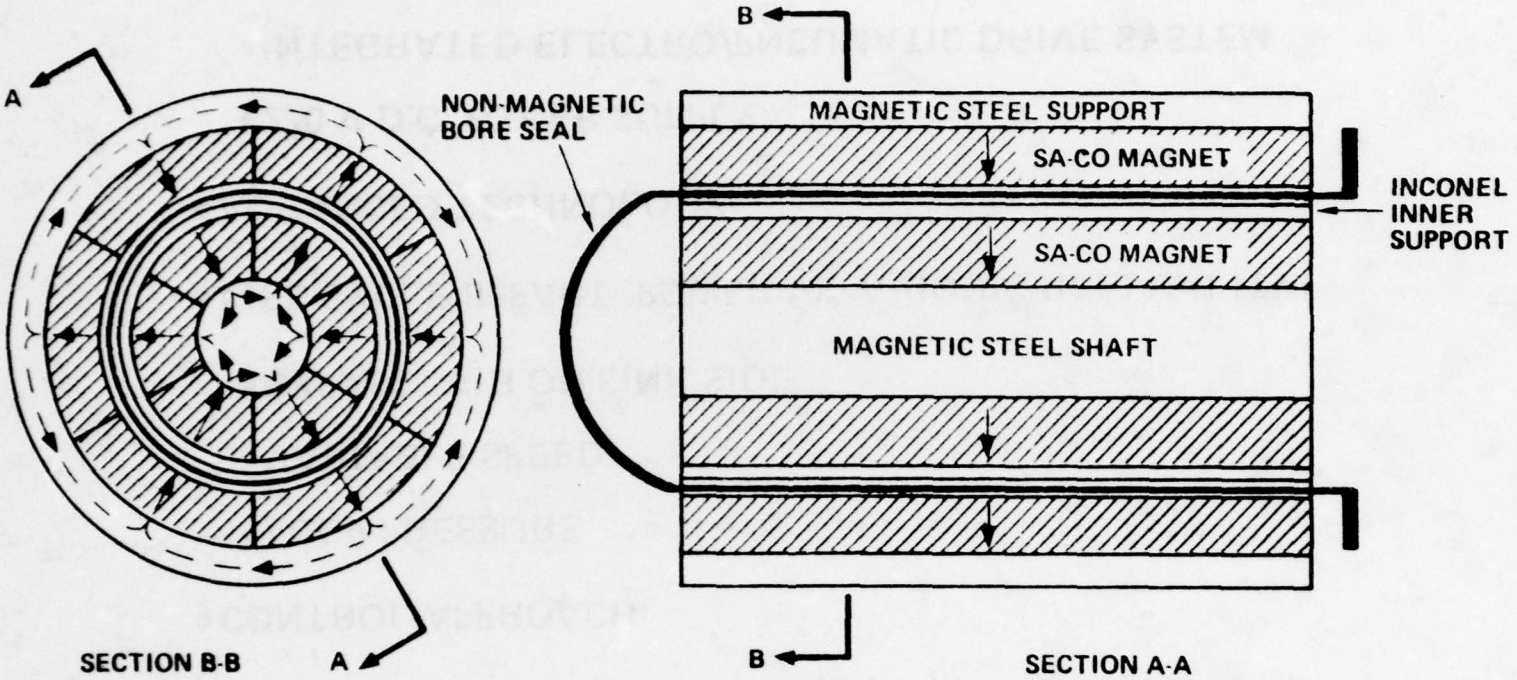


TYPICAL SOLAR SYSTEM TURBOMACHINERY



S-5393-A

MAGNETIC COUPLING CROSS SECTIONS



S-6378

OPTIMIZATION REQUIREMENTS

- PARAMETRIC ANALYSIS (SPEED, β, r_c, E V_S PENALTIES)
- CONTROL APPROACH
  - LOOP PRESSURE
  - VARIABLE SPEED
  - BYPASS - AIR ON SINK SIDE
- LIFE CYCLE IMPACT (POWER VS. AVIONIC RELIABILITY)
- ADVANCED TECHNOLOGY
  - 270 V D.C. POWER SUPPLY
  - INTEGRATED ELECTRO/PNEUMATIC DRIVE SYSTEM
- OTHER CYCLES
  - DIRECT COOLED AVIONICS
  - VAPOR CYCLE

APPENDIX H

MODULAR AVIONICS PACKAGING ENVIRONMENTAL CONTROL SYSTEM STUDY

SUNDSTRAND CORPORATION

14 October 1977

GENERAL ELECTRIC STUDY INPUT
MODULAR AVIONICS PACKAGING STUDY

Sundstrand has investigated the size and performance of cooling system equipment to meet 10KW and 20KW heat loads. Supply temperatures of 85°F and 120°F were evaluated. The low temperature configuration consists of a vapor compression refrigeration cycle using Freon 22, extracting heat from a Coolanol 20 loop, which in turn extracts heat from electronic card racks. (See Figure 1 for schematic arrangement and state point information). The high temperature system consists of an air cooled Coolanol loop as shown in Figure 2.

Ground cooling is effected by rejecting heat to the condenser fan air via the vapor cycle system. Operation in flight is by directing the Coolanol flow directly to the condenser with the vapor cycle inoperative. Temperature control is obtained by modulating the Freon or Coolanol flow to the condenser. This means was selected over condenser air flow modulation based on lower control element weight. A trade study would be required to evaluate this against reduced drag resulting from air flow modulation.

The following describes the component designs and provides a weight and size summary of the major components. Tables 1 and 2 describe the low temperature vapor cycle system for 10KW and 20KW loads, respectively. Table 3 summarizes the equipment for the high temperature system using the air cooled Coolanol loop.

FIGURE 1

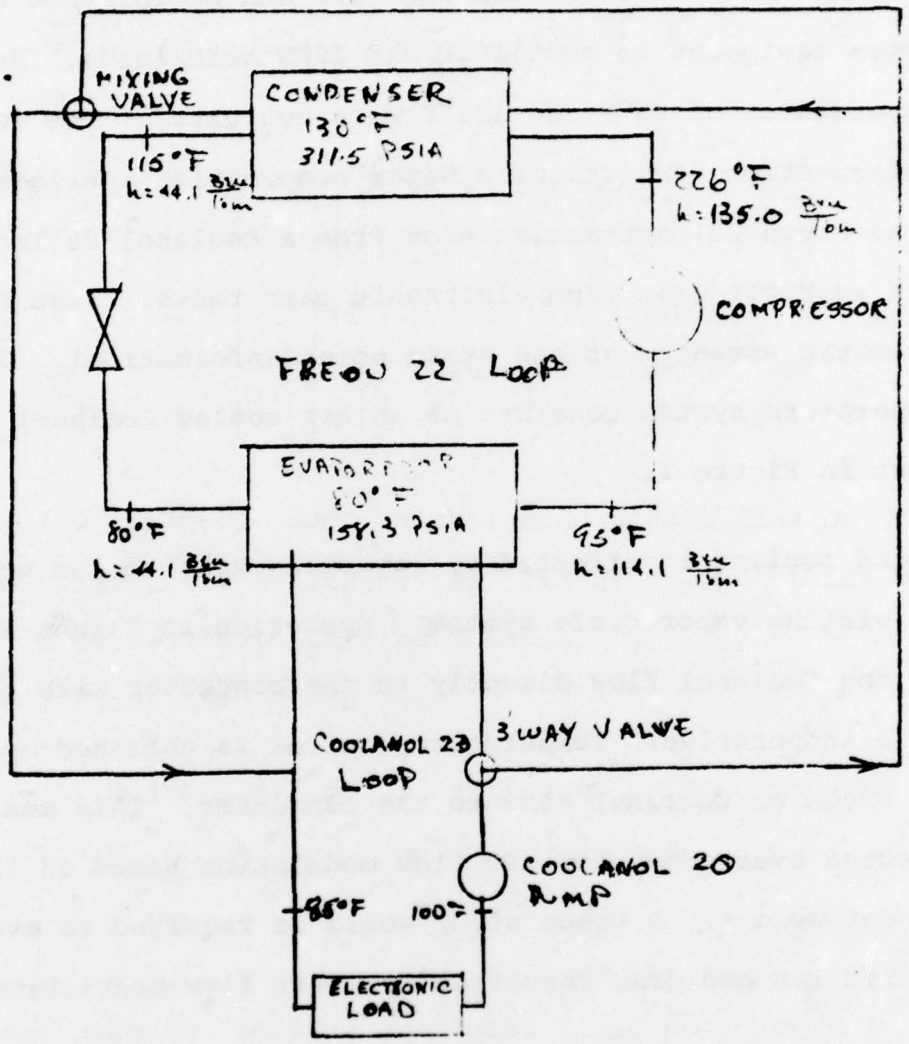
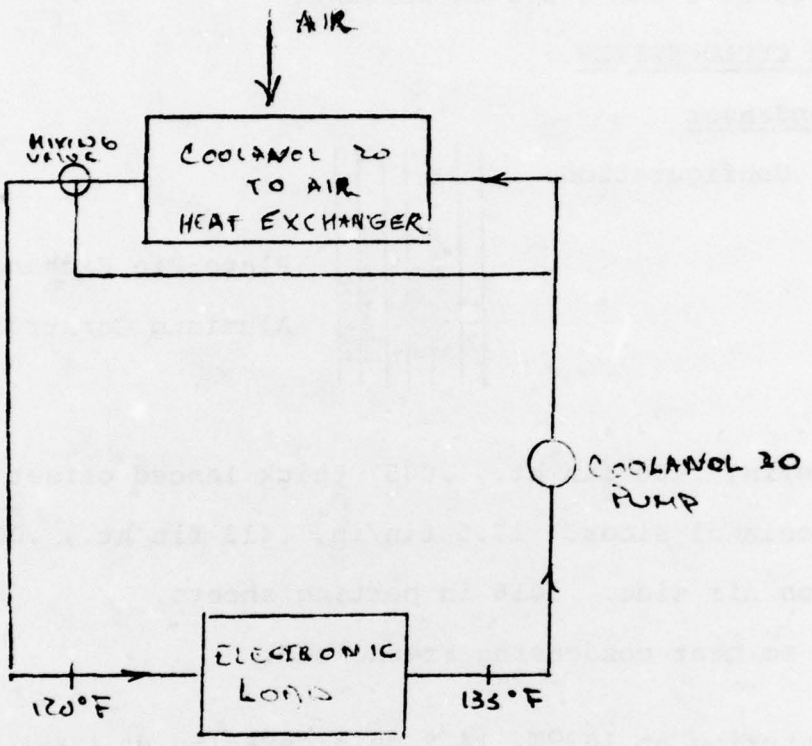

MIXING VALVE
CONDENSER
130°F
311.5 PSIA
115°F
h=44.1 Btu/lbm
226°F
h=135.0 Btu/lbm
COMPRESSOR
FREON 22 Loop
EVAPORATOR
80°F
158.3 PSIA
80°F
h=44.1 Btu/lbm
95°F
h=114.1 Btu/lbm
COOLANOL 20
Loop
3 WAY VALVE
COOLANOL 20
PUMP
85°F
100%
ELECTRONIC LOAD

FIGURE 2


AIR
MIXING VALVE
COOLANOL 20 TO AIR HEAT EXCHANGER
COOLANOL 20 PUMP
ELECTRONIC LOADS
120°F
135°F

MAP - GENERAL ELECTRIC STUDY 14 October 1977

Assumptions made in component sizing for the systems described in Figures 1 and 2 are as follows:

VAPOR CYCLE SYSTEM

Condenser

Configuration:

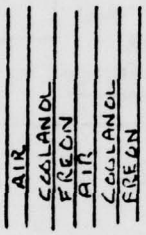


Plate-Fin Exchanger

Aluminum Construction

18 fin/in, .100 fin ht., .005" thick lanced offset fins on Freon and Coolanol sides. 17.5 fin/in, .413 fin ht., .006" thick wavy fins on air side. .016 in parting sheets.
Sized to meet condensing Freon load.

Air entering at 103°F, 14.7 psia; exiting at 125°F. Condenser Freon temperature 130°F. Crossflow configuration.

Evaporator

Sized to meet avionics cooling load plus added pump power. Plate-fin exchanger. Aluminum construction using fins and parting sheets described above. ΔT Coolanol = 15°F. Evaporating Freon temperature 80°F

Cold Plates

Single layer, aluminum plate fin, 18 fin/in, .100 fin ht., .005" thick lanced offset fins. Coolanol entering 85°F, exiting 100°F. Multipass design with plates oriented horizontally.

Compressor

Positive displacement type. Task P/N 13430 for the 20KW unit. Scaled to meet the 10KW application.

Fans & Pump

Sizes, weights, and power based on representative known component hardware size for similar performance requirements.

COOLANOL - AIR SYSTEM

Heat Exchanger

Plate-Fin exchanger, aluminum construction crossflow configuration. Air entering at 103°F, 14.7 psia; exiting 115°F Coolanol 20 entering 135°F exiting 120°F. Cold plates same as in vapor cycle system. Pump and fan data from Task catalog.

Summary for both Systems

All sizing determined for ground operation only, using the fan. No performance was obtained for tnese components using ram air. Weights and sizes of piping required for plumbing the systems have not been determined.

Quantity and weights of the fluids, Freon and Coolanol 20 were not determined.

MAP - GENERAL ELECTRIC STUDY 14 October 1977

G. E. Coolanol System

T evap = 80°F, T cond = 130°F, Freon 22 ΔT Coolanol 20 = 15°F,

i.e. 85-100°F

Coolanol Flow through each cold plate is 0.55 gpm

TABLE 1

10,000 Watt System

Component	Size	Weight
Condenser	20" x 23.6" x 3"	25.1 lbs.
Evaporator	7" x 12" x 4"	8.3 lbs.
Compressor	7" dia. 12.6" high	25 lbs. (3.2KW)
Expansion Valve	-	0.8 lbs.
Hot Gas Bypass Valve	-	2.0 lbs.
Quench Valve	-	0.6 lbs.
Filter, Drier	-	0.6 lbs.
Sight Glass	-	0.6 lbs.
Receiver	-	0.6 lbs.
Cold Plates	6" x 19.5" x 0.2", 20 @ 1.32 lb	26.4 lb
Coolanol Pump		3.0 lbs.
Mixing Valve	-	?
3-Way Valve	-	?
Fan	Task Part No. X702-334	15.4 lbs. (1.25 hp)
Fan Damper	12" Dia.	4.5 lbs.
	Sub Total	112.9 lbs.

TABLE 2

20,000 Watt System

Component	Size	Weight
Condenser	27" x 31.6" x 3"	47.0 lbs.
Evaporator	5.6" x 12" x 8"	13.3 lbs.
Compressor & Motor	Task Part No. 13430	33lbs. (3.88 KW)
Coolanol Pump	Task Part No. 9221-4	4.3 lbs.
Fan	Task Part No. 500702-4290	23.5 lbs. (2.5HP)
Fan Damper	16" Dia.	6 lbs.
Cold Plates	6" x 19.5" x 0.2", 40 @ 1.32 lb.	52.8 lbs.
	Sub Total	179.9 lbs.
Other components (valves, sightglass, etc.)		6.0 lbs. *
	Sub Total	186 lbs.

* Approximately the same as for 10KW system.

TABLE 3

G.E. System, Coolanol - Air Only

T Coolanol = 120°F ——→ 135°F

T Air = Δ103°F ——→ 115°F

10,000 Watt System

In Coolanol = 88.2 lb /min = 12 gpm

In Air = 211 lb /min = 3130 cfm

Exchanger 12.7" x 18" x 1.5", 5.8 lbs.

Fan 20.1 lbs. Task Part No. X702-373 1.85 hp.

Pump 2.94 lbs. (700W)

Total Weight, fan, ex., pump = 28.84 lbs.

20,000 Watt System

In Coolanol = 176.4 16 /min = 24 gpm

In Air = 411.8 lb /min = 6100 cfm

Exchanger 16" x 24" x 1.5", 9.6 lbs.

Fan 30 lbs.

Pump 4.3 lbs. Task Part No. 9221-4

Total weight, fan, ex., pump = 43.9 lbs.

Cold Plates 1.32 lbs. each, 6" x 19.5" x 0.2"

20 required for 10KW system, 40 for 20KW system.