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FABRICATION OF PMOS DIGITAL SHIFT REGISTERS.(U)
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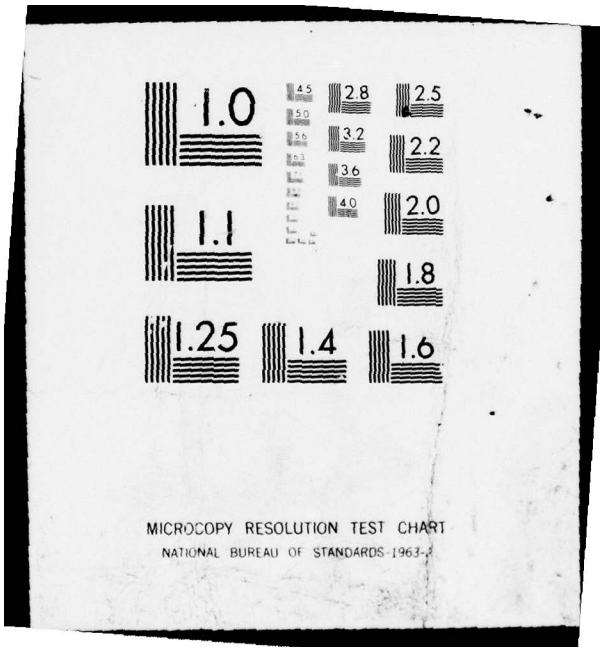
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NRL Memorandum Report 3786

Fabrication of PMOS Digital Shift Registers

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and

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June 1978

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This report contains the design, fabrication process, test conditions, and test results for a digital shift register chip fabricated at the Naval Research Laboratory during 1977. The basic technology used was PMOS, silicon-gate. Four different types of shift register configurations were contained on the test chip; a static shift register, a bucket brigade device, a scanner, and a dynamic ratioless shift register.

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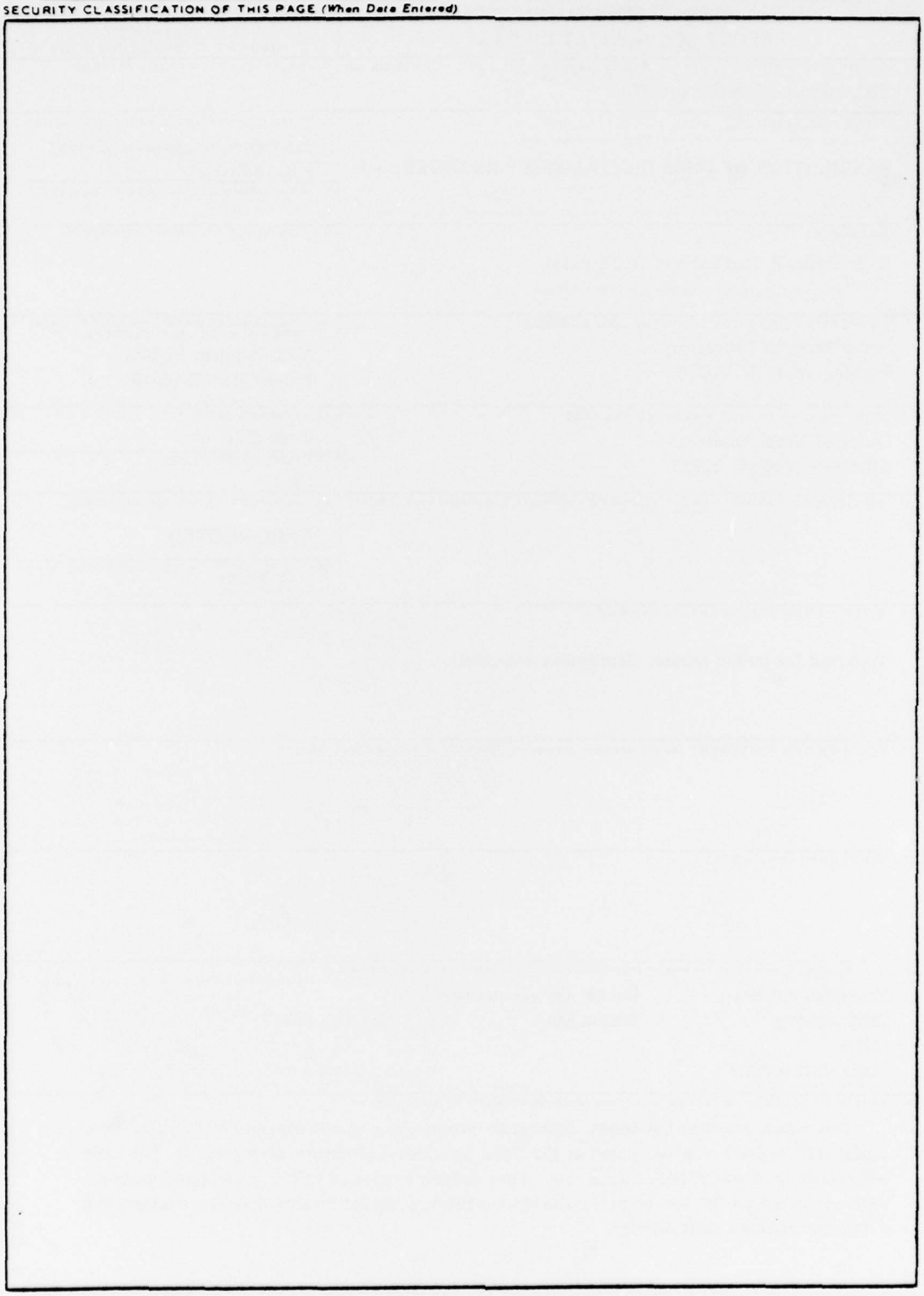

CONTENTS

FABRICATION OF PMOS DIGITAL SHIFT REGISTERS

I. INTRODUCTION

The primary objective of this project was the demonstration of an in-house capability for fabrication of PMOS, silicon-gate integrated circuits. The vehicle chosen for this demonstration was the digital shift register, an important building block in many modern integrated circuits. Two types were emphasized, a static shift register and a bucket brigade device, because their properties were potentially useful for several in-house research projects. During the design phase two other types, a scanner and a ratioless dynamic shift register, were added to the chip. The mask layout and computer generation were done in-house, while the actual mask fabrication was contracted to Electromask. The device fabrication was done completely in-house at the Naval Research Laboratory.

II. DESIGN

For assistance in device design and layout, we frequently referred to a loose-leaf book published by NSA[1] which contains scale drawings of cells for a number of integrated circuits, including several static shift registers. It also contains layout design rules which specify parameters such as minimum allowable lindwidths, line spacings, and contact window sizes. The NSA rules are conservative but reasonable and we violated none of them in the shift register layouts.

The overall chip size is 188 mils × 165 mils; there are over 70 chips on a two-inch wafer. Each chip contains the four different shift registers, assorted test devices, and a surface acoustic wave convolver experiment which occupies approximately one-third of the chip. Details of the surface wave experiment are beyond the scope of this report and will not be discussed here.

The shift register portion of the chip is shown in Figure 1. The layout of each shift register is set up so that the essential functions (i.e., bias supplies, clocks, input/output) are connected to a row of 8 bonding pads which can be probed with a standard probe card in order to simplify electrical tests on the wafer prior to dicing and packaging. All bonding pads that are connected to transistor gates (i.e., clocks and inputs) have gate protection circuits. The design of each of the four devices is described in this section.

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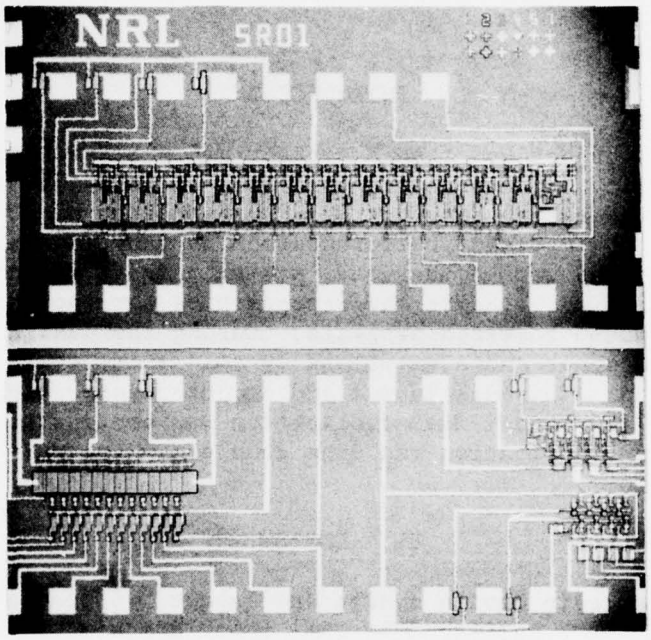


Figure 1 — Shift register chip

STATIC SHIFT REGISTER

The static shift register is the large device occupying most of the upper half of Figure 1. The device is an NSA design, it is the simplest static shift register in reference 1 with 9 transistors per stage and a pitch of 7.0 mils. The cell was digitized directly from page H33 of reference 1. A schematic of a single cell is shown in Figure 2. The circuit is a two-phase design. The load transistors are clocked rather than continuously on, and the two clocks $\phi 1$ and $\phi 2$ are run at low duty cycle to reduce power dissipation. "A" is the input signal terminal, and "B" is the latching clock. When $\phi 2$ and B are simultaneously on, the signal A is inverted and clocked to point SC. SC, the complement of A, is available for tapping in the cell design, but none of the SC points in our shift register layout were tapped. Unbuffered, SC should be capable of driving a 3 pf load. After $\phi 2$ and B turn off, the $\phi 1$ clock is turned on, inverting the signal at SC and clocking it to PC. The static latch is implemented by stopping B ($\phi 1$ and $\phi 2$ continue to run). With B off, the circuit becomes bistable and no new signal at A is allowed to be clocked in.

The static shift register shown in Figure 1 has 12 stages with the output of each (PC in Figure 2) connected unbuffered to a bonding pad. PC should be capable of driving a 5 pf load. The output of the 12th stage is connected to a precharge output buffer from page J02 of reference 1. A schematic of this buffer is shown in Figure 3. The cell width is 7.1 mils and the design drive capability is 75 pf.

BUCKET BRIGADE DEVICE

The bucket brigage device[2,3] is located in the lower left quarter of Figure 1. Each device contains 12 stages; two of these are shown schematically in Figure 4. Each stage contains two MOS transistors connected to form a tetrode which minimizes output drain to input source feedback. The first MOS transistor of each state is self-aligned to minimize parasitic capacitance and is biased so that it always operates in saturation. The second transistor is designed with a large overlap capacitance on the drain output, which provides the necessary charge storage capability for subsequent transfer. The large overlap capacitance is accomplished using a p+ diffusion prior to formation of the gate oxide and polysilicon electrodes.

In addition to the 12 stages, the device requires input and output transistors, plus a buffer transistor at the overlap capacitor of each stage for tapping. The buffer transistor is capable of driving a 10 pf load. The same peripheral circuitry was also incorporated into the scanner and ratioless shift register.

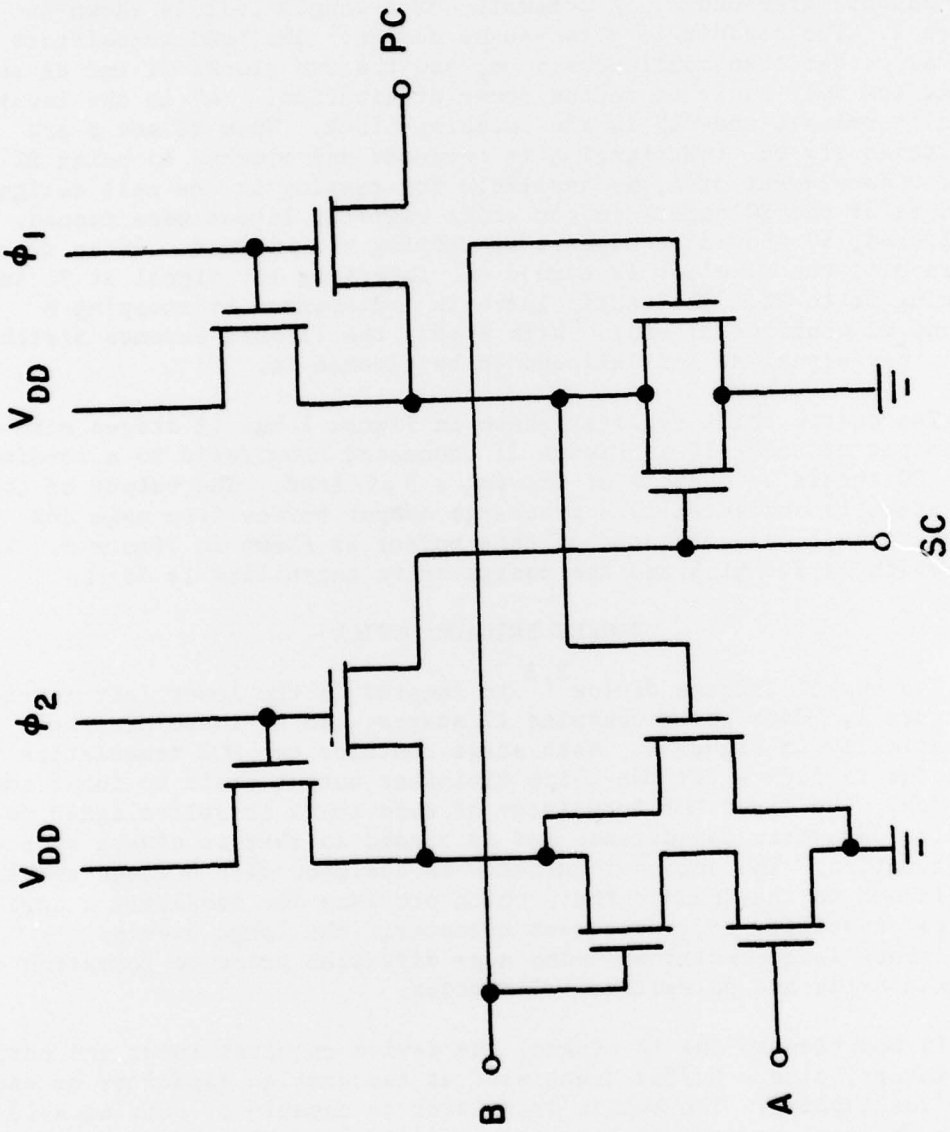


Figure 2 — Schematic of static shift register cell

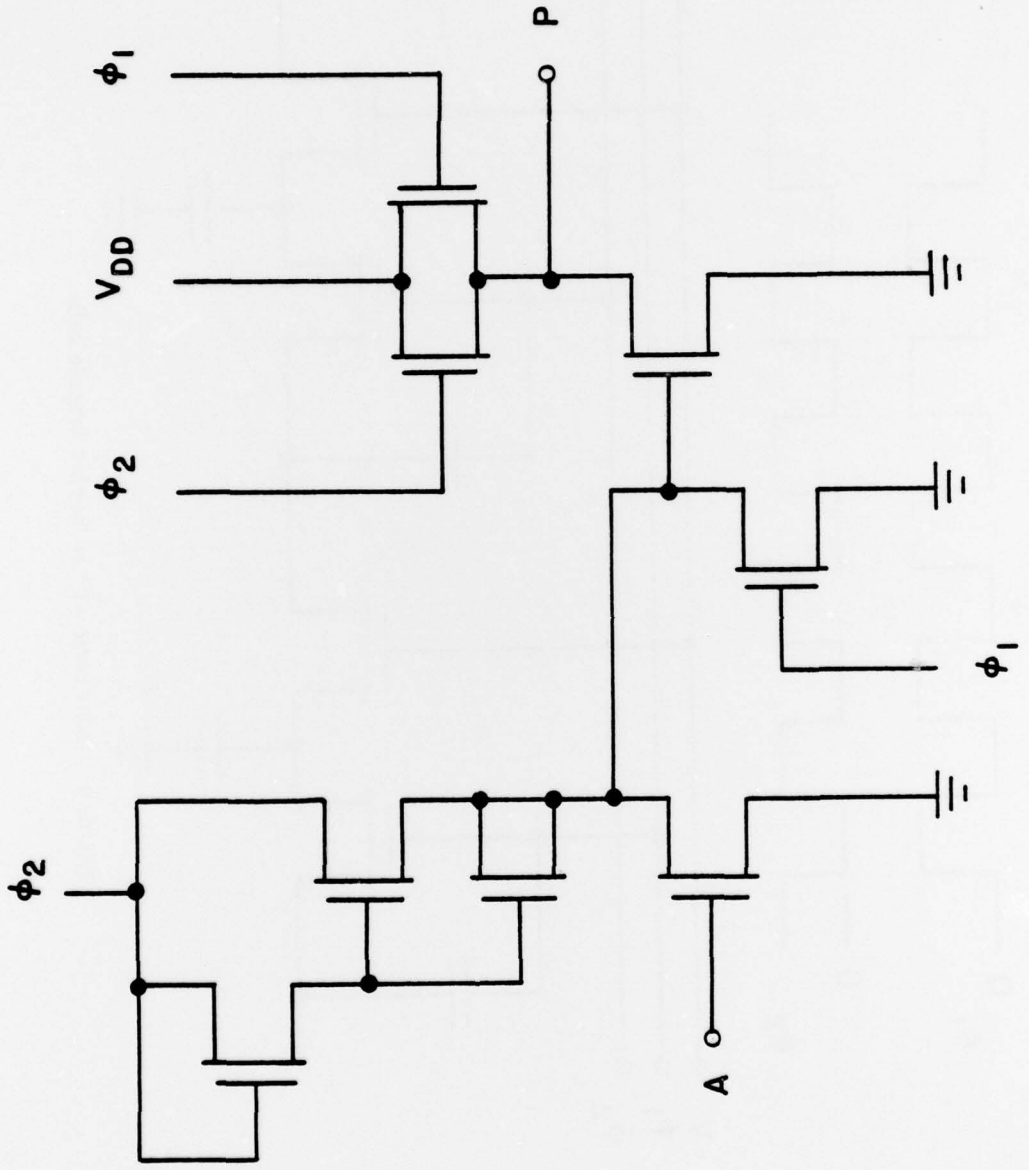


Figure 3 — Schematic of static shift register precharge output buffer

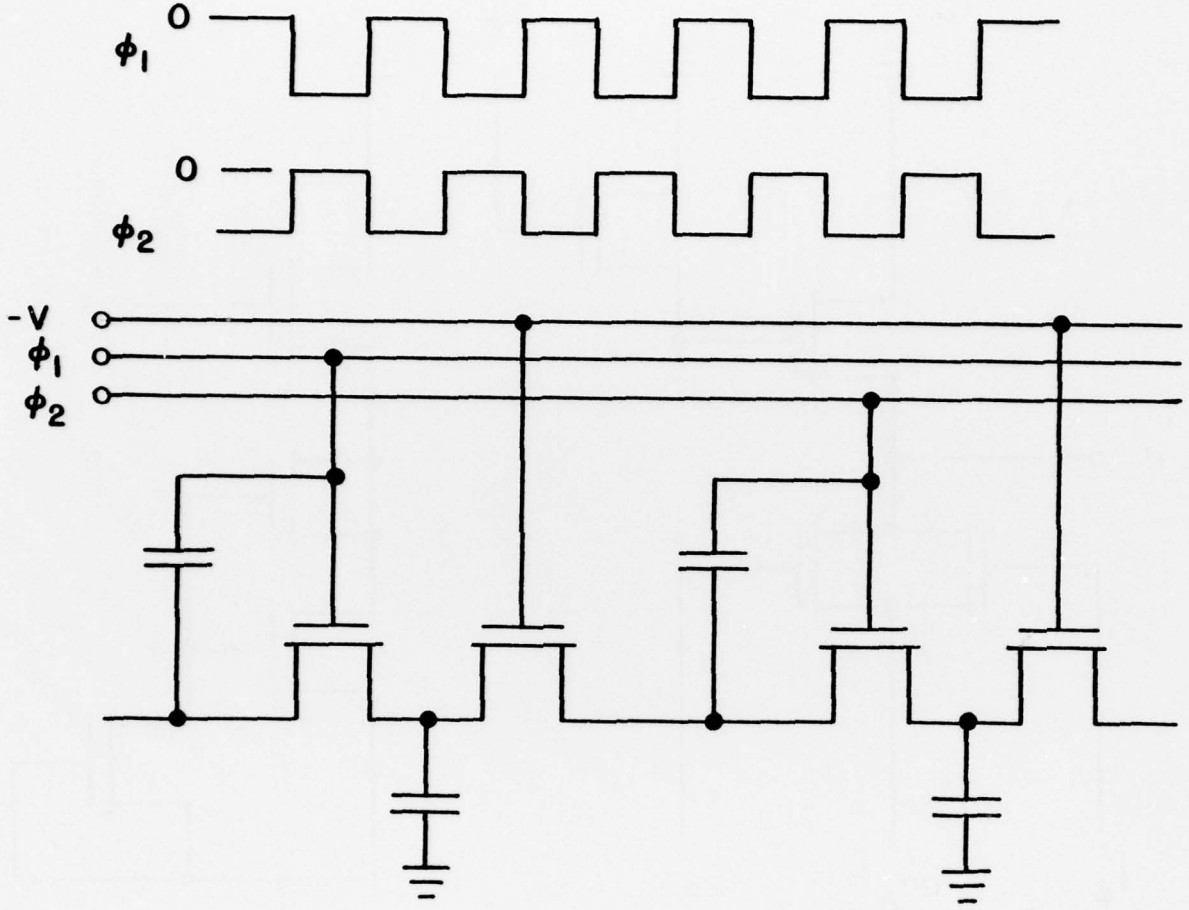


Figure 4 — Schematic of two bucket brigade cells

SCANNER

The third shift register is located in the lower right quarter of Figure 1. It is a copy of the scanner used in the General Electric CID imager. The advantage of this scanner over conventional shift registers is its minimum number of transistors per stage (4), which allows a 3.3 mil pitch. Only four stages were included due to limited space on the chip. The schematic for a single stage of the scanner is shown in Figure 5. Transistor T4 is actually a voltage-variable capacitor which bootstraps transistor T1 when the ϕ1 pulse is applied. This concept is discussed in more detail in reference 4.

RATIOLESS DYNAMIC SHIFT REGISTER

A ratioless shift register test vehicle (4 cells) was also included on the lower right quarter of Figure 1. The design is based on a circuit reported in reference 5, using MOS capacitor pull-up circuits for reducing the number of active elements required for stage. Each stage has 4 MOS transistors and 2 overlap capacitors (similar to the bucket brigade) connected as shown in Figure 6. Although some parasitic bipolar problems were reported for this circuit, the device was included because of its compatibility with the processing sequence required for the bucket brigade device already on the chip.

III. FABRICATION

Six mask levels were required for shift register fabrication:

(1) Diffusion mask used to define the capacitors for the bucket brigade and the ratioless dynamic shift register (see the Design section above).

(2) Mask to define the active regions.

(3) Mask to define the polysilicon pattern.

(4) Mask to open the contact windows.

(5) Mask to define the metal pattern.

(6) Mask to open holes in the passivation layer to the bonding pads. (The shift registers actually tested did not have an overcoat so this mask was not used).

The standard self-aligned silicon gate processing was modified to allow formulation of the p+ diffusion overlap regions prior to formation of the thin oxide active regions. An outline of the process sequence is given in the flow chart in Table 1. Note that the active

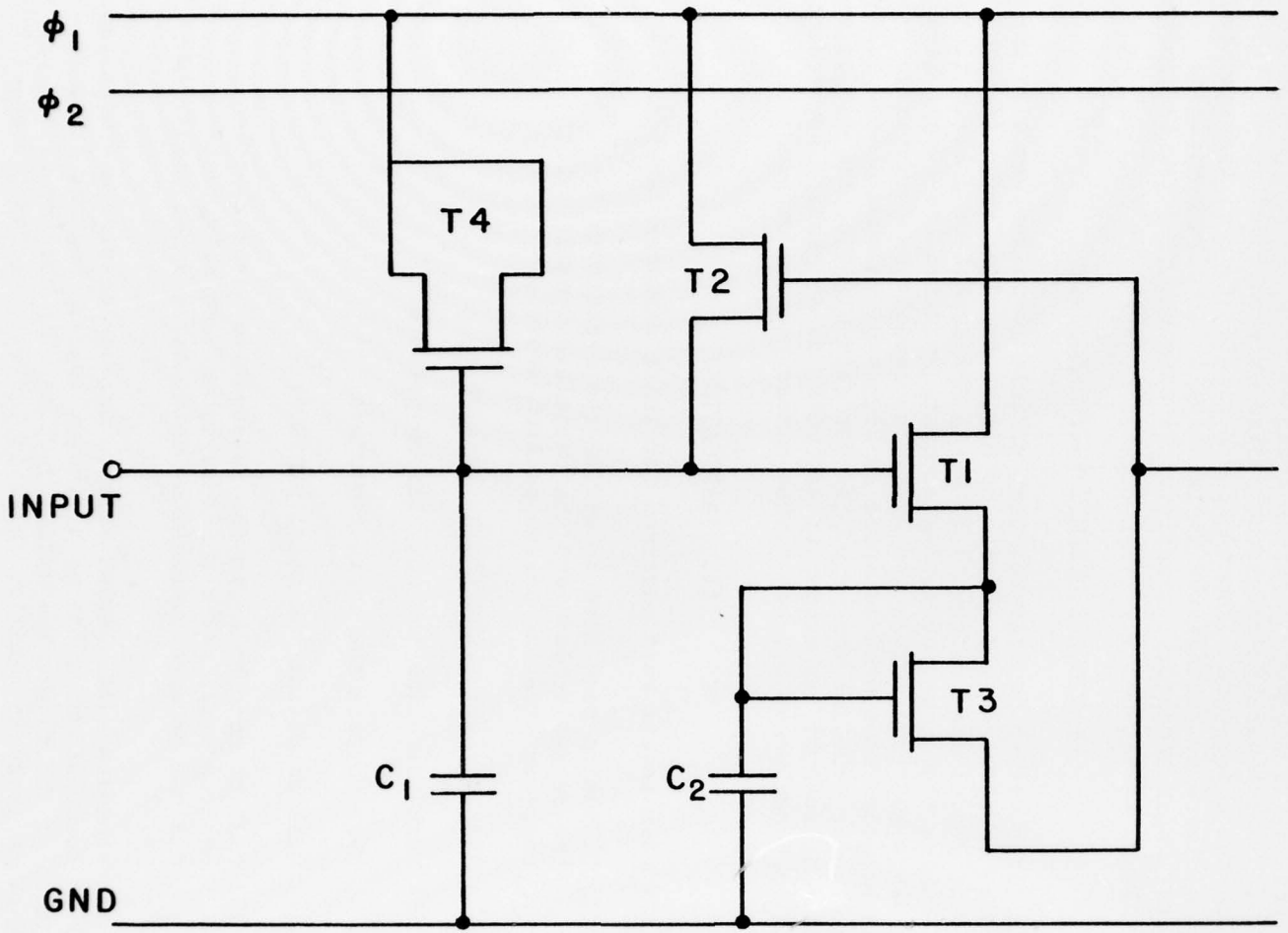


Figure 5 — Schematic of single scanner cell

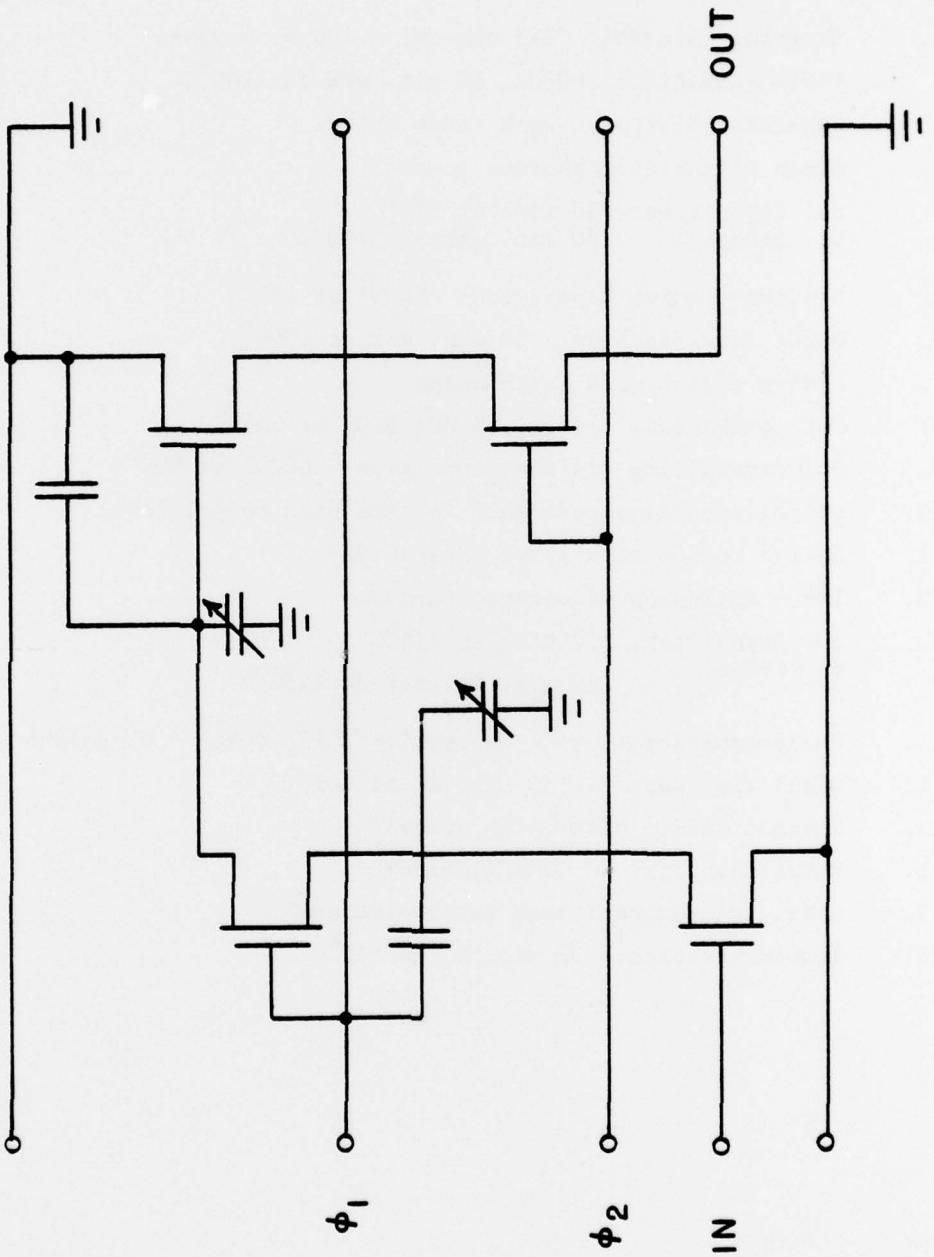


Figure 6 — Schematic of single ratioless shift register cell

TABLE 1: PROCESS FLOW CHART

1. Starting material: 3-5 ohm-cm, < 100 >, n-type
2. Field oxidation: 6000Å, 60 min. wet at 1100°C
3. Capacitor diffusion mask (etch oxide)
4. Boron diffusion (diborane source)
   a. Deposition: 30 min. at 975°C
   b. Drive: 60 min. wet at 1100°C
5. Silicon dioxide deposition: 6000Å at 405°C
6. Oxide densification: 60 min. wet at 1000°C
7. Active region mask (etch oxide)
8. Gate oxidation: 1200Å, 1% HCℓ in O_2 at 1000°C
9. Polycrystalline silicon deposition: 6000Å at 800°C
10. Polysilicon electrode mask (plasma etch polysilicon)
11. Active region mask (etch gate oxide)
12. Boron diffusion (diborane source)
    a. Deposition: 30 min. at 975°C
    b. Drive: 60 min. O_2 only at 1050°C
13. Phosphorus-doped oxide deposition: 12,000Å, ~ 5% phosphorus
14. Glass flow anneal: 20 min. N_2 at 1050°C
15. Contact window mask (etch oxide)
16. Metallization: 10,000Å Aluminum
17. Metal interconnect mask (etch aluminum)
18. Aluminum sinter: 30 min. N_2 at 450°C

region mask is reapplied in step 11 to eliminate aluminum step coverage problems associated with oxide removal under the polysilicon electrodes in the field oxide regions.

IV. TEST

All four shift registers were probed on the wafer with an 8-pin probe card. A rough estimate of yield for the static registers and bucket brigades was made by randomly probing a number of devices. Approximately 2/3 of the static shift registers and a higher percentage of the bucket brigade devices were found to be good. Several of these types of devices were diced and packaged. The oscilloscope traces shown for the static registers and bucket brigades in this section were taken using packaged devices.

STATIC SHIFT REGISTER

Figure 7 shows the various inputs required for device operation. All four traces have a vertical scale of 5 volts/division. The top trace is the $\phi 1$ clock, the second trace is the $\phi 2$ clock, the third trace is the input signal (A in Figure 2), and the bottom trace is the static latching clock (B in Figure 2). The positions of the four traces are staggered on the oscilloscope; none of the clocks or signals has a DC offset. The DC bias (V_{DD} in Figure 2) is -6 volts.

Figure 8 shows the shift register operation, measured directly with a high impedance oscilloscope. The top trace is the B clock. The middle trace is the A input. A sequence of seven pulses is periodically read into the device. The bottom trace is the output of the 12th stage (unbuffered). The output signal is delayed from the input by exactly 12 clock periods.

Figure 9 demonstrates the operation of the static latch. The B clock is turned off periodically for three clock periods ($\phi 1$ and $\phi 2$ continue to run). All seven input pulses in Figure 9(a) are clocked into and partially through the register. Just as the second pulse is detected at the output, B is turned off (Note the relative timing of the top and bottom traces). This stops the transfers, so that the voltage at the output of the 12th state (corresponding to the second input pulse) is repeatedly detected during the three clock periods that B is off. When B starts again the transfers are resumed and the last five input pulses, which were stored in the static register during the time B was off, are sequentially read out. The bottom trace of Figure 9(a) shows 10 output pulses, corresponding to the seven input pulses plus those repetitions of the second pulse.

In Figure 9(b) the input signal is changed to help visualize the static latching operation. Instead of a sequence of seven identical pulses, the first pulse is at a low level (on), the second pulse is at

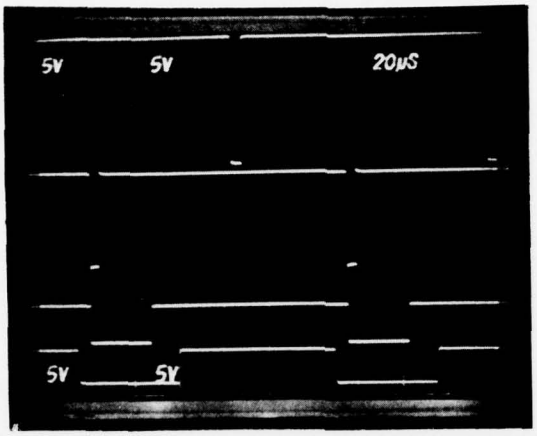


Figure 7: Clocking sequence for static shift register (See Fig.2). Top trace: $\varphi 1$, Second trace: $\varphi 2$, Third trace: A, Bottom trace: B. V_{DD} = -6 volts.

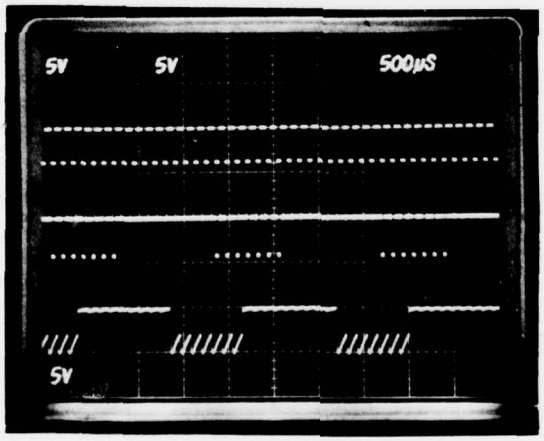
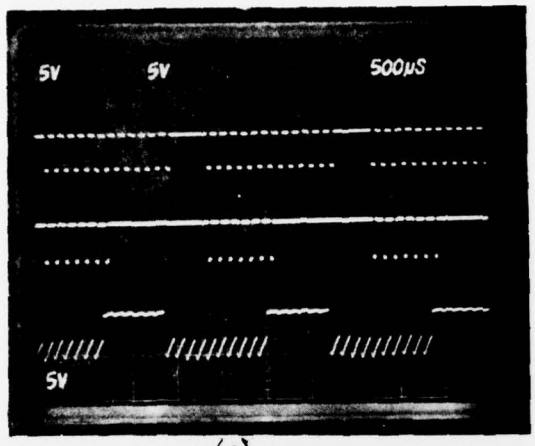
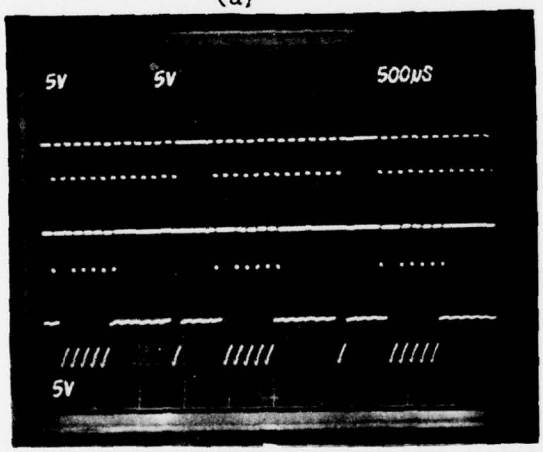


Figure 8: Static shift register operation. Top trace: B, Middle trace: A, Bottom trace: Output of 12th stage (unbuffered) delayed from input by 12 clock periods.



(a)



(b)

Figure 9: Static latch operation. The three traces in both (a) and (b) correspond to the same signals as in Figure 8.

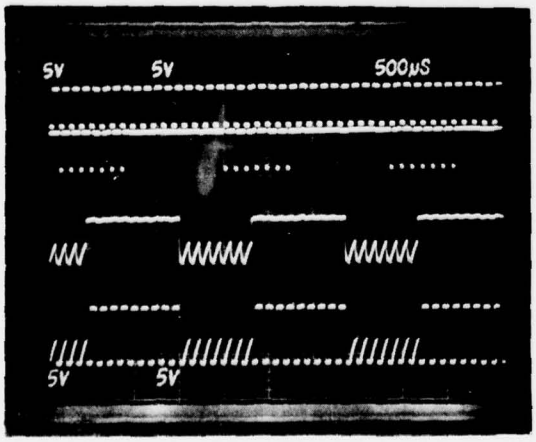


Figure 10: Top three traces: identical to Figure 8, Bottom trace: output of buffer.

a high level (off), and the last five pulses are at a low level. The output trace shows the first pulse and the last five pulses separated by four clock periods of high level signal, corresponding to the high level second pulse and three repetitions of this high level.

The operation of the output buffer is shown in Figure 10. The top three traces are identical to Figure 8 and the bottom trace is the buffer output, which operated as expected.

The clock rate was varied to determine the maximum clocking speed, which was found to be approximately 1 MHz.

BUCKET BRIGADE DEVICE

Figure 11 shows the bucket brigade operation. The complementary clocks ($\phi 1$ and $\phi 2$ in Figure 4) are the two superimposed traces at the top. The levels are -10 volts with no DC offset. The center trace is the input signal, which is offset by -5 volts. This input signal level corresponds to the saturation voltage for the bucket brigade. The bottom trace shows the sampled output of the 12th stage, measured using a 9.5 pf oscilloscope probe shunted by 18 kΩ resistor. The output signal is also offset by -5 volts. The DC input level was -10 volts for this photograph.

The device was found to operate over a fairly wide range of operating parameters. When the input signal was offset by -9 volts, the clocks had to be increased to -17.5 volts and the DC bias increased to -15 volts. With this combination of operating conditions the input voltage saturation level increased to approximately -4 volts. Higher operating voltages were not attempted. Lower voltages than used in Figure 11 are possible, but for input signal offset less than -5 volts, the input signal saturation level begins to drop rapidly.

The response to an analog input signal was measured and the output level was found to be linearly related to the input over a dynamic range of at least 40 dB. The dynamic range appeared to be greater but our measurements were not sufficiently accurate to determine the device limit.

The maximum clock speed was also investigated. Figure 12 shows the device operation at a sample rate of 5 MHz. The two complementary clocks are shown superimposed at the top of the figure on a scale of 5 volts/division. As before, the clocks have no DC offset. The center trace is the input signal, offset by -5 volts, on a scale of 2 volts/division. The sampled output is shown, offset by -2.8 volts, in the bottom trace at 1 volt/division. The output is measured using a 9.5 pf oscilloscope probe shunted by a 4.5 kΩ resistance. For this photograph V_{DC} = -10 volts.

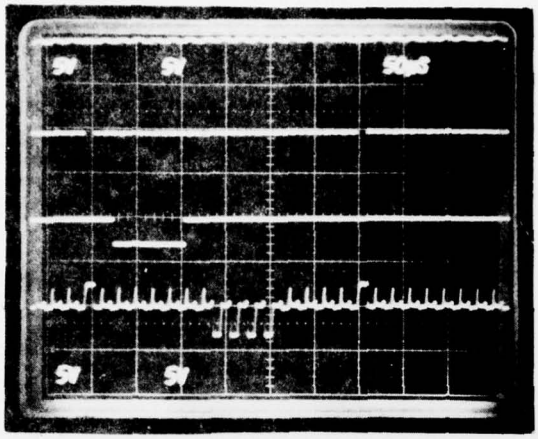


Figure 11: Bucket brigade operation. Top traces: superimposed complementary clocks, Middle trace: input signal, Bottom trace: output signal.

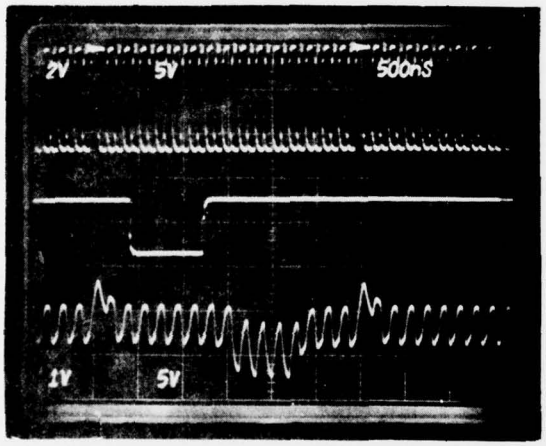


Figure 12: Same as Figure 11 but faster operating speed.

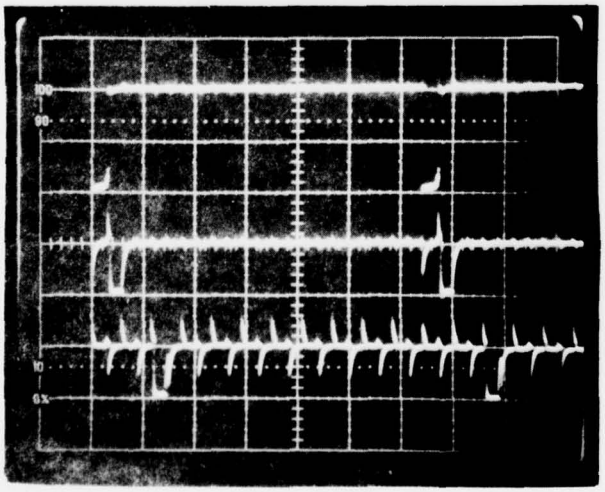


Figure 13: Scanner operation. Top trace: input signal, Middle trace: output of first cell, Bottom trace: output of fourth cell. All traces 50μsec/division, 10 volts/division.

SCANNER

Operation of the scanner is demonstrated in Figure 13. The horizontal scale is 50usec/division and the vertical scale for all three traces is 10/volts/division. The top trace is the input signal, the center trace is the output of the first scanner cell, and the bottom trace is the output of the fourth scanner cell. The two complementary clocks are -20 volts, V_{DD} = -15 volts, and $V_{substrate}$ = +5 volts.

RATIOLESS DYNAMIC SHIFT REGISTER

This shift register failed to operate in preliminary tests. It is unclear whether there is a design error on the chip or whether incorrect voltage levels were used in the test. Time did not permit further study of this device.

V. CONCLUSIONS

The successful completion of this project provides a clear demonstration of the ability of the Naval Research Laboratory Microelectronics Facility to fabricate integrated circuits of significant complexity.

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