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MONOLITHIC MICROWAVE PREAMPLIFIER

TECHNICAL REPORT

OCTOBER 1978

CONTRACT NO. N00014-77-C-0645
CONTRACT AUTH. NO. NR 251-028

Prepared For

OFFICE OF NAVAL RESEARCH
ARLINGTON, VIRGINIA

TRW
DEFENSE AND SPACE SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA 90278

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A computer model of the FET has been developed based on the Pucel model, but with several improvements incorporated. The model has been exercised to produce FET designs, which will be optimized for low noise amplifier performance. The model also predicts device sensitivity to the processing variables, and provides S parameters as a function of frequency and bias. The model has been used to design devices for a low noise monolithic X-band preamplifier.

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CONTENTS

ILLUSTRATIONS

1. INTRODUCTION AND SUMMARY

This technical report describes the results of the investigation on low noise FET devices performed by TRW Systems Group (DSSG) under contract No. N00014-77-C-0645 for the Office of Naval Research. The period of performance was 1 September 1977 to 31 March 1978. The chief purpose of the investigation is to develop a computer model of GaAs microwave field effect transistors in order to predict noise performance as a function of geometry, biasing conditions, doping density, ancilliary region implants and temperature, with aims to minimize the noise figure.

TRW's approach to achieve this goal has been to start with the best mathematical model of FET devices available at the present time and perform systematic variations to this model in order to optimize noise figure, transconductance linearity, and dynamic range.

2. THE INTRINSIC FET

2.1 THE FET MODEL

One of the many FET models that have been developed in the last decade, with the fewest restrictions and assumptions, is the Grebene-Ghandi model. Its fundamental principle is a two-piece linear approximation of the velocity-field characteristic of a semiconductor exhibiting velocity saturation as shown in Figure 2-1.

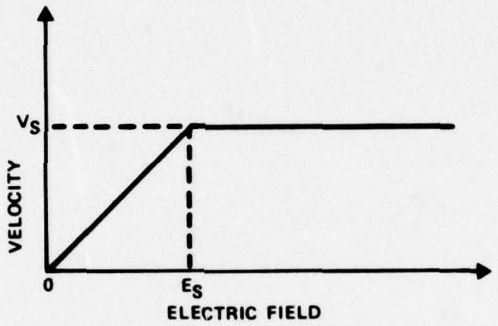
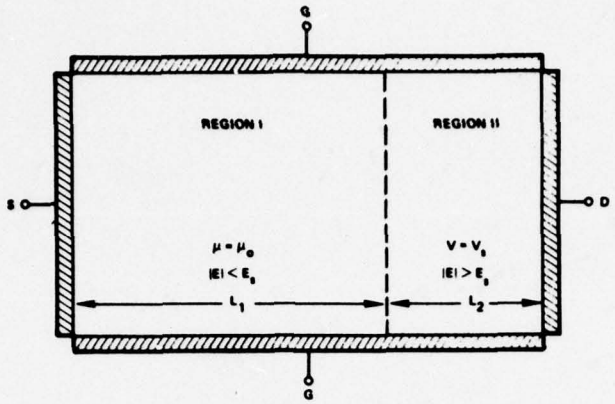


Figure 2-1. Two-Piece Linear Approximation of the Velocity-Field Characteristic of a Semiconductor Exhibiting Velocity Saturation

This velocity-field characteristic divides the intrinsic FET model into two regions: region I of length L_1 the constant mobility region where the velocity is field-dependent; and region II of length L_2 the constant velocity region where the electric field has exceeded the critical field E_s and the carriers travel at the saturation velocity V_s independent of field strength. This two-region model for the intrinsic FET is shown in Figure 2-2. The piecewise linear approximation of the velocity-field characteristic necessarily involves compromise in the choice of values used of E_s, μ_o, and V_s. The mobility (μ_o) is evaluated from the doping density (N_o) by the use of a Taylor Series expansion as

$$\mu_o = 10^{[-2.751 \times 10^{-3} \times \log^3(N_o) + 1.0249 \times 10^{-1} \times \log^2(N_o) - 1.251 \times \log(N_o) + 8.8249]} \quad (2\text{-}1)$$



REGION I: CONSTANT MOBILITY REGION; FIELD DEPENDENT VELOCITY
REGION II: CONSTANT VELOCITY REGION; FIELD INDEPENDENT VELOCITY

Figure 2-2. Two Section Model of the FET

Equation (2-1) is in essence the result of curve fitting techniques applied to the velocity - doping characteristic for type GaAs as given by Sze[1] in the range $10^{14} < N_o < 10^{18}$

For a typical mobility value of μ_o = 4500cm/Volt-sec E_s needs to be chosen as 2.9 kV/cm in order to obtain the typical saturation velocity of

$$V_s = \mu_o E_s = (4500 \text{ cm}^2/\text{v-sec}) (2.9 \text{ kV/cm}) = 1.3 \times 10^7 \text{ cm/sec.}$$

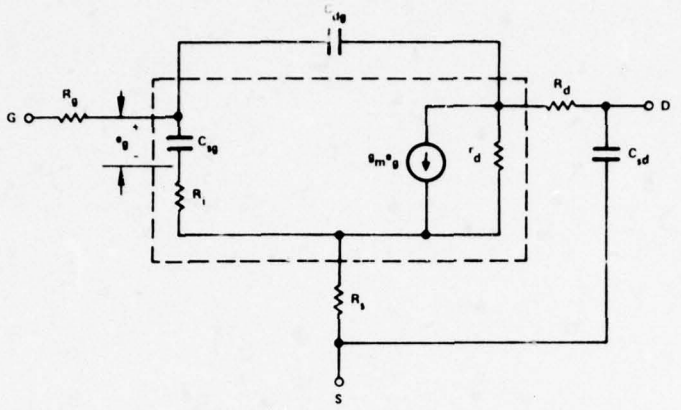
This choice for E_s is somewhat lower than the measured saturation field

$$3 \text{ kV/cm} < E_s < 4 \text{ kV/cm;}$$

however, it is the only compromise made throughout the model, and the choice is certainly justifiable on the basis of good correlation between thoretical and experimental data of noise, dc conditions, and small signal parameters.

2.2 SMALL SIGNAL PARAMETERS

The FET model outlined in Section 2-1 has an equivalent circuit as shown in Figure 2-3.



CIRCUIT ELEMENTS ENCLOSED BY THE DASHED LINES PERTAIN TO THE INTRINSIC DEVICE.
CIRCUIT ELEMENTS NOT ENCLOSED BY THE DASHED LINES INDICATE THE PARASITICS CONTRIBUTED BY THE ANCILLARY REGIONS

Figure 2-3. Small Signal Equivalent Circuit of the FET

The circuit elements enclosed by the dashed line constitute the intrinsic FET (region under the gate) and elements outside the dashed line are the parameters contributed by the ancillary regions. A prospective sketch of the FET indicating the geometric regions responsible for each circuit element is shown in Figure 2-4. Each of these circuit elements can be expressed as a function of the characteristic dimensions of the device, corresponding doping concentration of the region under consideration, and the dc biasing conditions.

Figure 2-5 is a cross-sectional diagram of the intrinsic FET showing various geometrical dimensions and potentials used in the equations to follow. From Figure 2-5 by adding potential drops inside the FET (i.e., in the channel and depletion region) and equating this sum to the externally applied voltages the following equations result:

$$V_{sg} = W(x) - \phi + V(x)$$

or

$$W(x) = V_{sg} + \phi - V(x) \qquad (2\text{-}2)$$

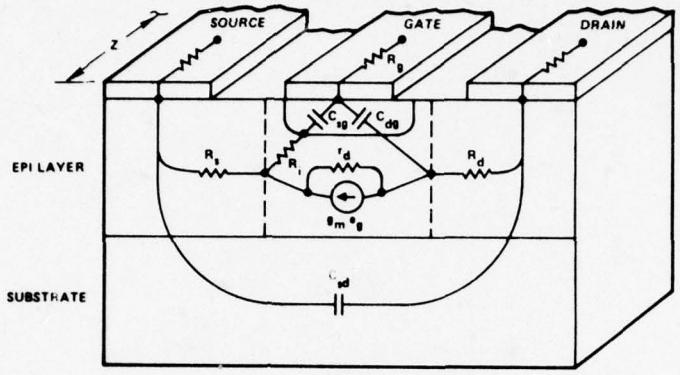


Figure 2-4. Perspective Sketch of the FET Indicating Geometric Regions Responsible for each Equivalent Circuit Element

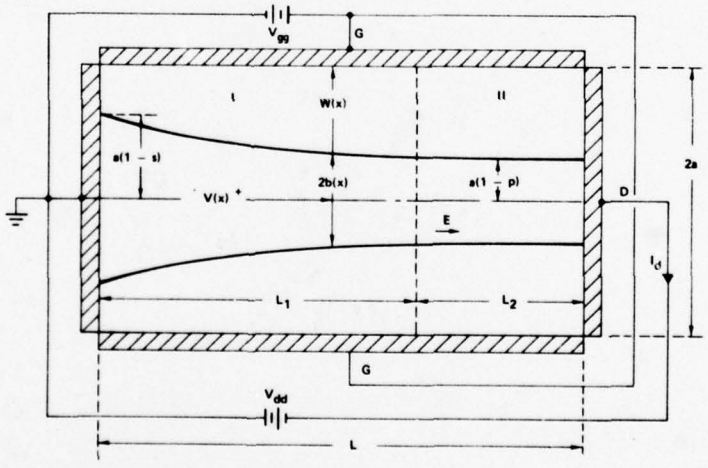


Figure 2-5. Cross-Sectional Diagram of the Idealized FET showing Geometrical Dimensions and Potentials

Here V(x) is the potential at position x in the channel with respect to the source while W(x) is the potential in the channel with respect to the gate. In particular, W(x) is the potential drop across the depletion region. It does not include the built-in potential of the gate, ϕ. Therefore, ϕ adds to the gate bias, V_{sg} and is typically

$$0.6 \text{ volt} \leq \phi \leq 0.7 \text{ volt}$$

for GaAs Schottky barrier junction using aluminum metallization. At the source (x = 0), V(0) = 0, and equation 2-2 becomes

$$W(0) \equiv W_s = V_{sg} +$$

At the interface of regions I and II, $(x = L_1)$, $V(L_1) \equiv V_p$, and equation (2-2) becomes

$$W(L_1) \equiv W_p = V_{sg} + \phi - V_p \tag{2-4}$$

at the drain (x=L), $V(L) = V_{sd}$, and equation (2-2) becomes

$$W(L) \equiv W_d = V_{sg} + \quad - V_{sd} \tag{2-5}$$

The gate-to-channel potential required to totally deplete the channel of carriers is given by the expression [2]

$$W_{oo} = \left(\frac{qN_o}{2\epsilon_r\epsilon_o}\right)a^2 \tag{2-6}$$

where $q = 1.6 \times 10^{-19}$ coulombs, N_o = doping concentration in the channel, $\epsilon_r = 12.5$ is the relative dielectric constant of GaAs, $\epsilon_o = 8.854 \times 10^{-14}$ farads/cm is the permittivity of free space, and 'a' is the half-thickness of the semiconductor between the gate electrodes (see Figure 2-5). Since equations (2-3), (2-4), and (2-5) are simply the potential of the depleted region at three different points along the channel, they can be written in the form of equation (2-6) as

$$W_s = \left(\frac{qN_o}{2\epsilon_r\epsilon_o}\right)(sa)^2 = W_{oo}s^2 \tag{2-7}$$

$$W_p = \left(\frac{qN_o}{2\epsilon_r\epsilon_o}\right)(pa)^2 = W_{oo}p^2 \tag{2-8}$$

$$W_d = \left(\frac{qN_o}{2\epsilon_r\epsilon_o}\right)(da)^2 = W_{oo}d^2 \tag{2-9}$$

From equations (2-6), (2-7), and (2-8) "s" and "p" can be expressed as

$$s = (W_s/W_{oo})^{1/2} \tag{2-10}$$

$$p = (W_p/W_{oo})^{1/2} \tag{2-11}$$

The quantities s, p, and d are reduced or normalized potentials. The following analysis will derive the characteristics of the FET in terms of s and p.

The potential across the depletion region can be found by assuming that the potential changes in the y direction much more rapidly than in the x direction. That is

$$\frac{\partial W(x)}{\partial y} \gg \frac{\partial V(x)}{\partial x}$$

This condition is satisfied when the channel thickness, a, is much smaller than the channel length, L. Making this assumption allows one to calculate the y component of the electric field using Gauss' law. Integrating a second time gives the potential W(x). Since there are no surface charges along the edges of the depletion region, the potential is

$$W(x) = \left(\frac{qN_o}{2\epsilon_r\epsilon_o}\right)[a - b(x)]^2 \tag{2-12}$$

$$= \left(\frac{qN_o}{2\epsilon_r\epsilon_o}\right)a^2[1 - b(x)/a]^2$$

$$= W_{oo}[1 - b(x)/a]^2$$

where b(x) is half the channel opening at point x (see Figure 2-5), and (1 - b(x)/a) is the fractional depth of the depletion region at the same point. It is convenient to define this fractional depth as

$$w(x) = 1 - b(x)/a \tag{2-13}$$

Then equation (2-12) can be written as

$$W(x) = W_{oo}[w(x)]^2 \tag{2-14}$$

Comparing equation (2-14) to (2-7) and (2-8) indicates that s and p correspond to w(x). Therefore, s and p not only represent reduced potentials but are also related to the depth of the depletion region. In Figure 2-5, (1-s) and (1-p) are accordingly

indicated as the fractional channel openings at the source end and in region II, respectively. The drain current at point x is given by Ohm's law as

$$I_d = 2b(x)\, Z\sigma\, [\partial W(x)/\partial x] \tag{2-15}$$

where Z is the gate width,

$$\sigma = q\mu_o N_o$$

the conductivity of the undepleted region of the channel and $\partial W(x)/\partial x = E_x(x)$ the longitudinal field in the channel at point x. From equation (2-14) the expression for the longitudinal field can be written in terms of the fractional channel opening as

$$\frac{\partial W(x)}{\partial x} = 2W_{oo}\, w(x)\, \frac{dw(x)}{dx} \tag{2-16}$$

From equation (2-13) the expression for the half-channel opening can be obtained as

$$b(x) = a[1-w(x)] \tag{2-17}$$

By the use of equation (2-16) and (2-17) equation (2-15) can be written as

$$I_d dx = 4a\sigma Z W_{oo}[1 - w(x)]w(x)dw(x) \tag{2-18}$$

Both sides of equation (2-18) can be integrated for region I in which the limits of integration for x are 0 and L_1, and the limits for w(x) are s and p (see Figure 2-5). The result of this integration yields

$$I_d = \frac{2a\sigma Z W_{oo}}{L_1} f_1(s,p) \tag{2-19}$$

where

$$f_1(s,p) = p^2 - s^2 - \frac{2}{3}(p^3 - s^3) \tag{2-20}$$

In region II the carriers travel at their saturation velocity given by

$$V_s = \mu_o E_s \tag{2-21}$$

where E_s is the critical longitudinal electric field at which the carriers reach their saturation velocity. Also in region II (or the constant velocity region) half the channel opening is given by

$$b = a(1-p) \tag{2-22}$$

and remains constant for $L_1 < x < L$, thus the expression for the drain current in this region is

$$I_d = 2b\sigma ZE_s \tag{2-23}$$

or by equation (2-22), equation (2-23) can be rewritten as

$$I_d = 2a\sigma ZE_s(1 - p) \tag{2-24}$$

Since there is current continuity across the interface of regions I and II, an expression for L_1 can be obtained from equations (2-19) and (2-24)

$$L_1 = \frac{W_{oo}}{E_s}\left[\frac{f_1(s,p)}{(1 - p)}\right] \tag{2-25}$$

Both the drain current and the length of region I are now expressed in terms of s and p. To determine the values of these parameters it also is necessary to express V_{sd} in terms of the reduced potentials.

The source-to-drain potential drop in the channel can be calculated by integrating the longitudinal electric field from x = 0 to x = L; this integration is done in two parts: from x = 0 to L_1 (region I) and from x = L_1 to x = L (region II). For region I the longitudinal electric field is given by equation (2-16)

Thus
$$\int_0^{L_1} \frac{\partial W(x)}{\partial x} = 2W_{oo} \int_0^{L_1} w(x)\left[\frac{dw(x)}{dx}\right]dx \tag{2-26}$$

which yields

$$W(L_1) - W(0) = W_{oo}\left[w^2(L_1) - w^2(0)\right] \tag{2-27}$$

From equation (2-13) the fractional depth of the depletion layer can be obtained as

$$w(L_1) = 1 - b(L_1)/a = p \tag{2-28}$$

$$w(0) = 1 - b(0)/a = s \tag{2-29}$$

Substitution of equation (2-28) and (2-29) on the right-hand side of equation (2-27) and substitution of equation (2-3) and (2-4) on the left-hand side of (2-27) gives

$$-V_p = Woo\ (p^2 - s^2) \tag{2-30}$$

For region II the longitudinal electric field is determined entirely by free charges on the drain electrode (neglecting carrier accumulation). In this region the potential satisfies the two-dimensional Laplace's equation

$$\nabla^2\phi = 0 \tag{2-31}$$

For the asymmetrical transistor the boundary conditions for equation (2-31) are:

$$\begin{aligned} &\frac{\partial\phi}{\partial y}(x,0) = 0 && L_1 < x < L \\ &\phi(x,a) = 0 && L_1 < x < L \\ &\phi(L_1,y) = 0 && -0 < y < a \\ &\frac{\partial\phi}{\partial y}(L_1,y) \quad E_s && -0 < y \cdot a \end{aligned} \tag{2-32}$$

Equations (2-31) and (2-32) form a well-formulated boundary-value problem; the solution to this problem is

$$\phi(x,y) = \sum_{n=0}^{\infty} A_n \cos\left[\frac{(2n+1)}{2a}\pi y\right] \sinh\left[\frac{(2n+1)}{2a}\pi(x - L_1)\right] \tag{2-33}$$

which can be truncated to

$$\phi(x,y) \simeq -\frac{2a}{\pi} E_s \cos\left(\frac{\pi y}{2a}\right) \sinh\left[\frac{\pi(x - L_1)}{2a}\right] \tag{2-34}$$

in which only the first term is considered. This approximation removes the terms with large arguments in the exponentials of the hyperbolic sine term which vary rapidly with y. The voltage across region II is therefore

$$\phi(L,0) - \phi(L_1,0) = -\frac{2a}{\pi} E_s \sinh\left[\frac{\pi(L - L_1)}{2a}\right] \tag{2-35}$$

where $\phi(L_1,0) = 0$ due to the boundary conditions given by equation (2-32). The overall source-to-drain potential drop in the channel is finally obtained from equations (2-30) and (2-36) as

$$\begin{aligned} V_{sd} &= W_{oo}\left\{(p^2 - s^2) + \frac{2a}{\pi}\left(\frac{E_s}{W_{oo}}\right) \sinh\left[\frac{\pi(L - L_1)}{2a}\right]\right\} \\ &= W_{oo}\left\{(p^2 - s^2) + \frac{2}{\pi}\left(\frac{a}{L}\right) \xi \sinh\left[\frac{\pi(L - L_1)}{2a}\right]\right\} \end{aligned} \tag{2-36}$$

where

$$\xi = \frac{E_s L}{W_{oo}} \tag{2-37}$$

Equations (2-3) and (2-7) relate s to the gate voltage. After substituting for L_1, equation (2-36) relates s and p to V_{sd}. Therefore, given the bias conditions and the physical properties of the FET, the reduced potentials s and p may be found. Although these equations have been derived for the intrinsic FET, they are still useful when parasitic resistances in the source and drain region of a practical device are included. These parasitics introduce additional voltage drops which are expressed as a parasitic resistance times the drain current. However, using (2-24) for the drain current, one can still reduce the problem to two equations in the unknowns s and p. The following sections will derive additional device parameters and ultimately the minimum noise figure in terms of s and p.

2.2.1 Transconductance

The transconductance of a FET device is defined as

$$g_m = - \left.\frac{dI_d}{dV_{sg}}\right|_{V_{sd} = \text{constant}} \tag{2-38}$$

From equations (2-27) and (2-38) the transconductance can be expressed alternately as

$$g_m = - \frac{\partial I_d}{\partial p} \frac{\partial p}{\partial V_{sg}} = 2a\sigma Z E_s \left(\frac{\partial s}{\partial V_{sg}}\right) \tag{2-39}$$

$$= 2a\sigma Z E_s \left(\frac{\partial p}{\partial s}\right)\left(\frac{\partial s}{\partial V_{sg}}\right)$$

From equations (2-3) and (2-7) $\partial s/\partial V_{sg}$ can be obtained as

$$\frac{\partial s}{\partial V_{sg}} = \frac{1}{2sW_{oo}} \tag{2-40}$$

Also from equation (2-36) since $dV_{sd} = 0$

$$2pdp - 2sds - \frac{\xi}{L} \cosh\left[\frac{\pi(1 - L_1)}{2a}\right] dL_1 = 0 \tag{2-41}$$

Also from equation (2-25)

$$dL_1 = \frac{W_{oo}}{E_s}\left\{\left[2p + \frac{E_s}{W_{oo}}\left(\frac{L_1}{1 - p}\right)\right]dp - 2s\,\frac{1 - s}{1 - p}\,ds\right\} \tag{2-42}$$

Substituting (2-42) into (2-41) and collecting terms, the ratio dp/ds can be obtained as

$$\frac{dp}{ds} = \frac{2s(1 - s)\cosh\left[\pi(L - L_1)/2a\right] - 2s(1 - p)}{\left[2p(1 - p) + E_s L_1/W_{oo}\right]\cosh\left[\pi(1 - L_1)/2a\right] - 2p(1 - p)} \tag{2-43}$$

substituting of equations (2-40) and (2-43) into equation (2-39) yields for the trandsconductance

$$g_m = \frac{I_s}{W_{oo}}\left\{\frac{(1 - s)\cosh\left[L - L_1)/2a\right] - (1 - p)}{\left[2p(1 - p) + \xi L_1/L\right]\cosh\left[\pi(L - L_1)/2a\right] - 2p(1 - p)}\right\} \tag{2-44}$$

$$= \frac{I_s}{W_{oo}} f_g(s,p)$$

where

$$I_s = 2a\sigma Z E_s$$

$$f_g(s,p) = \frac{(1 - s)\cosh\left[\pi L_2/2a\right] - (1 - p)}{\left[2p(1 - p) + \xi L_1/L\right]\cosh\left[\pi L_2/2a\right] - 2p(1 - p)} \tag{2-45}$$

The quantity I_s is the saturation current and represents the maximum current that could flow through the channel assuming no depleted region. Notice that the transconductance *function*, f_g, *is only a function* of s and p since $L_2 = L - L_1$, and equation 2-25 defines L_1 in terms of s and p.

2.2.2 Output Resistance

The output resistance is defined as

$$r_d = -\left.\frac{dV_{sd}}{dI_d}\right|_{V_{sg} = \text{constant}} \tag{2-46}$$

Following a process similar to that outlined for the transconductance, the output resistance can also be written in terms of I_s, W_{oo} and a function of s and p.

$$r_d = \left(\frac{W_{oo}}{I_s}\right)\left\{\frac{2p(1-p) + \xi(L_1/L)\cosh\left[\pi L_2/2a\right] - 2p\,(1-p)}{1 - p}\right\} \tag{2-47}$$

$$= \left(\frac{W_{oo}}{I_s}\right) f_r\,(s,p)$$

where

$$f_r(s,p) = \left\{\frac{[2P(1-p) + \zeta(L_1/L)] \cosh [\pi L_2/2a] - 2p(1-p)}{1 - p}\right\} \tag{2-48}$$

2.2.3 Gate-Source Capacitance

The gate-source capacitance is defined as the rate of change of the free charge on the gate electrode with respect to the gate bias voltage when the drain potential is held fixed.

$$C_{sg} = \left.\frac{dQ_g}{dV_{sg}}\right|_{V_{sd} = \text{constant}} \tag{2-49}$$

The gate charge can be obtained by a simple application of Gauss' Law as

$$Q_g = \int \vec{D} \cdot d\vec{s} - \varepsilon_r \varepsilon_o \int \vec{E} \cdot d\vec{s} \tag{2-50}$$

In equation (2-50) the differential surface element of the gate is

$$d\vec{s} = \hat{y}\, Z\, dx \tag{2-51}$$

where $\hat{y}$ is a unit vector normal to the gate surface. Also in equation (2-50) the electric field under consideration is

$$\vec{E} = \hat{y}\, E_y \tag{2-52}$$

or the y component of the field. This electric field has two different expressions:

$E_{y1}(x,a)$ in region I and $E_{y2}(x,a)$ in region II.

From equation (2-12) the field in region I can be calculated as

$$E_{y1}(x,a) = \frac{dW(x)}{db(x)} = \frac{2W_{oo}}{a}\,[1 - b(x)/a] \tag{2-53}$$

In region II there is an additional component due to the Laplacian potential of equation (2-34); consequently

$$E_{y2}(x,a) = \left.\frac{dW(x)}{db(x)}\right|_{x = L_1} + \left.\frac{d\phi(x,y)}{d_y}\right|_{y = a} \tag{2-54}$$

$$= \left(\frac{2W_{oo}}{a}\right) p + E_s \sinh \frac{\pi(x - L_1)}{2a}$$

Substitution of equations (2-52) through (2-54) into equation (2-50) yields

$$Q_g = \left(\frac{2W_{oo}\epsilon_r\epsilon_o}{a}\right)\left[\int_0^{L_1} E_{y1}(x,a)dx + \int_{L_1}^{L} E_{y2}(x,a)dx\right] \tag{2-55}$$

$$= \left(\frac{2W_{oo}\epsilon_r\epsilon_o}{a}\right)\left\{\frac{\frac{2}{3}(p^3 - s^3) - \frac{1}{2}(p^4 - s^4)}{(p^2 - s^2) - \frac{2}{3}(p^3 - s^3)} L_1 + p(1 - L_1)\right.$$

$$\left. + \left(\frac{aE_s}{2W_{oo}}\right)\left(\frac{2a}{\pi}\right)\left[\cosh\frac{\pi(L - L_1)}{2a} - 1\right]\right\}$$

$$= 2qN_o aZ\left\{\frac{f_2(s,p)}{f_1(s,p)} L_1 + pL_2 + \left(\frac{\xi a^2}{\pi L}\right)\left[\cosh\frac{\pi(1 - L_1)}{2a} - 1\right]\right\}$$

where

$$f_2(s,p) = \frac{2}{3}(p^3 - s^3) - \frac{1}{2}(p^4 - s^4) \tag{2-56}$$

and the gate-source capacitance expression (2-49) can be obtained from (2-55) by performing the following differentiations[3]

$$C_{sg} = \left.\frac{dQ_g}{dV_{sg}}\right|_{V_{sd} = \text{constant}} = \left.\left(\frac{dQ_g}{dp}\right)\left(\frac{dp}{dV_{sg}}\right)\right|_{V_{sd} = \text{constant}} \tag{2-57}$$

$$= \epsilon_r\epsilon_o Z f_c$$

where $f_c = f_{c1} + f_{c2} + 1.56$

$$f_{c1} = \left(\frac{2}{f_1}\right)\left(\frac{L_1}{a}\right)\left\{f_g\left[\frac{2p^2(1 - p^2) + f_2}{1 - p}\right] - s(1 - s)\right\} \tag{2-58}$$

$$f_{c2}(s,p) = 2\left(\frac{L_2}{a}\right)f_g + (1 - 2pf_g)\left[2\left(\frac{L}{2}\right)\frac{p}{\xi\cosh(\pi L_2/a)} + \tanh\frac{\pi L_2}{2a}\right] \tag{2-59}$$

The first two terms of the capacitance function, f_c, are the contributions due to region I and region II. The numerical term accounts for the fringing capacitance and is taken from the work of Wasserstrom and McKenna[4].

2.2.4 Gate Charging Resistance

At the present, there is no formal analytic expression for R_i in the two section model of the FET. It is simply assumed that the time constant $\tau = R_i C_{sg}$ is proportional to the transit time through the channel. From the experimental data of Brehm and Vendelin [5] this transit time is set to

$$\tau = R_i C_{sg} = 4 \times 10^{-12} \text{ sec} \tag{2-60}$$

From experimental data this product scales with gate length and consequently equation (2-60) can be written as

$$\tau = K L R_i C_{sg} \tag{2-61}$$

where K is a proportionality constant (K = 0.5/μm) then from equations (2-60) and (2-61)

$$R_i = \frac{4 \times 10^{-12}}{KLC_{sg}} = \frac{8 \times 10^{-12}}{LC_{sg}} \tag{2-62}$$

where L is in μm.

2.2.5 Summary of the Small Signal Analysis of the Intrinsic FET

It is useful to review the results of this section before proceeding with the noise analysis. The model is based on the assumption that the channel under the gate can be divided into two regions. In the first region, the carrier behavior is ohmic. In the second region the carriers move at a saturated drift velocity that does not increase with increased electric field.

A pair of reduced potentials, s and p, are then defined. A second assumption gives a physical significance to these parameters. One assumes that the electric field component along the channel is much smaller than the component perpendicular to the channel. Then one can determine the electric field and potential in terms of the charge distribution in the channel. From the form of the potential, s can be related to the fractional opening of the channel at the source end of the gate and p can be related to the opening at the interface between regions I and II. This assumption sets limits on the applicability of the model. In practice, it is satisfied for gate lengths somewhat larger than the channel depth. Fortunately, such conditions also correspond to most devices of practical interest.

After defining s and p, the bias conditions, V_{sg} and V_{sd}, are expressed in terms of these parameters. The resulting equations must be solved numerically for practical situations which include parasitic source and drain resistances, but they provide a means of obtaining values for s and p. It is then possible to express all of the small signal parameters in terms of s, p and the physical properties of the FET. The following sections will develop the form of the noise figure, again in terms of the reduced potentials s and p.

3. NOISE ANALYSIS FOR THE INTRINSIC FET

Noise in a microwave GaAs FET is produced by sources intrinsic to the device and thermal sources associated with the parasitic resistances. The intrinsic noise arises from two mechanisms: first mechanism is the thermal or Johnson noise produced in region I; the second mechanism is the diffusion noise in the velocity saturated section (region II).

It is convenient for noise figure calculations to represent the internal noise sources of the intrinsic FET by noise generators suitably connected to the external terminals as shown in Figure 3-1.

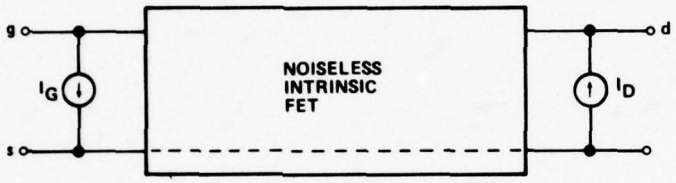


Figure 3-1. The Intrinsic FET with Two Noise Sources
IG Represents the Induced Gate Noise,
ID Represents the Drain Circuit Noise

This representation in terms of external current generators is useful because the output generator can be identified with the short-circuit channel noise generated in the source-drain path, while the input generator can be related to the noise current induced in the gate circuit by the charge fluctuations in the drain current.

3.1 DRAIN CIRCUIT NOISE

The open-circuit drain voltage fluctuation produced by sources in region I is[6]

$$\overline{\left|v_{d1}^2\right|} = \left(\frac{4kT_o\Delta f}{2a\sigma\, Z/L_1}\right)\left(\frac{P_o + P_\delta}{(1-p)^2}\right)\cosh^2\left(\frac{\pi L_2}{2a}\right) \qquad (3\text{-}1)$$

where

$$P_o = (f_1)^{-1}\left[\left(p^2 - s^2\right) - 4/3\left(p^3 - s^3\right) + 1/2\left(p^4 - s^4\right)\right] \qquad (3\text{-}2)$$

and

$$P_\delta = 2\delta\left(f_1^{-1}\right)\left(1-p\right)^3\left[(s-p) + \ln\left(\frac{1-s}{1-p}\right)\right] \tag{3-3}$$

The voltage fluctuations are due to Johnson noise generated in region I. Therefore, a kT_o term occurs in which k is Boltzman's constant and T_o is the reference temperature (300K) of the channel. Noise is produced over a frequency spectrum and equation (3-1) gives the resulting voltage fluctuations at the drain for a frequency bandwidth Δf. There are two terms in this equation. The first (proportional to P_o) represents the normal Johnson noise contribution as calculated for electrons in region I. The second term (containing P_δ) provides for the fact that the effective noise temperature of the carriers is higher than that of the crystal when an electric field is present to move them through the crystal. This "hot" electron term contains an emperical constant, δ, which relates the effective temperature to the reference temperature, T_o. The value of δ is modified from its published value[7] of 6 to a value of 1.19 to provide for the reduced saturation field of 2.9 kV/cm used here.

The open circuit drain voltage fluctuation produced by sources in region II is[6]

$$\left|v_{d2}^2\right| = I_d \frac{64a^2}{\pi^5 V_s^3}\left[\frac{q\,D\Delta f}{(\epsilon_r\epsilon_o)^2 Z^2}\right]\left[\frac{\sin^2 \pi(1-p)/2a}{(1-p)^2}\right]\left[\exp\frac{\pi L_2}{a} - 4\exp\frac{\pi L_2}{2a} + 3 + \frac{\pi L_2}{a}\right] \tag{3-4}$$

This fluctuation in voltage at the drain occurs when dipole layers form in region II of the channel. The layers drift toward the drain with a velocity determined by the diffusion constant, D, of the carriers. When the dipoles form they induce a voltage at the drain and at the region I-region II interface. The voltage appears as a pulse with the pulses described by a frequency spectrum. Equation (3-4) gives the drain voltage fluctuation due to pulses in a frequency bandwidth Δf.

The noise voltage contributions from each region are due to different mechanisms and are uncorrelated. Therefore, their mean squares add. Both contributions are developed across the output resistance, r_d, so the resulting noise fluctuation may be written in terms of a current at the drain, i_d. Specifically:

$$i_{d1} = v_{d1}/r_d \qquad i_{d2} = v_{d2}/r_d \tag{3-5}$$

$$\left|i_{d1}^2\right| + \left|i_{d2}^2\right| = \left|i_d^2\right| \tag{3-6}$$

3.2 GATE CIRCUIT NOISE

Noise voltages produced in the channel are coupled capacitively to the gate. These charge fluctuations on the gate in turn modulate the current through the channel and thus appear as noise at the drain. The short-circuit gate current fluctuation produced by sources in region I is given by[6]

$$\overline{\left|i_{g1}^2\right|} = \omega^2\left(\frac{16kT_o\Delta f}{a\sigma/L_1 Z}\right)\left(\frac{\varepsilon_r\varepsilon_o L_1}{\gamma a}\right)^2 (R_o + R_\delta) \tag{3-7}$$

where

$$= \frac{(1-p)^2 f_r}{f_1 \cosh(\pi L_2/2a)} \tag{3-8}$$

and

$$R_o = \left(f_1^{-3}\right)\left\{(\kappa')^2(p^2 - s^2) - 4/3\kappa'(\kappa' + \gamma)(p^3 - s^3) + 1/2\left[(\kappa')^2 + 4\kappa'\gamma + \gamma^2\right]\right.$$
$$\left. \cdot \left(p^4 - s^4\right) - 4/5\left(\kappa'\gamma + \gamma^2\right)\left(p^5 - s^5\right) + \gamma^2/3\left(p^6 - s^6\right)\right\} \tag{3-9}$$

$$R_\delta = \delta\,(1-p)^3\,(f_1)^{-3}\left\{-2(\kappa'-\gamma)^2\left[p-s + \ln\left(\frac{1-p}{1-s}\right)\right] + (2\kappa'\gamma - \gamma^2)(p^2-s^2) - 2/3\,\gamma^2\,(p^3-s^3)\right\} \tag{3-10}$$

$$\kappa = (f_1)^{-1}\left[-1/3\,(p^3-s^3) + 1/6\,(p^4-s^4) + (s^2-2/3\,s^3)\,(p-s)\right] + \gamma p \tag{3-11}$$

$$\kappa' = \kappa + (L_2/L_1)\,(1 - p) \tag{3-12}$$

Notice that this noise term is similar to the region I channel contribution (3-1). The observation is not surprising because both contributions are due to the same Johnson noise generated in region I. Because the boundary of region I is not a short circuit, but the conditions of region II, γ is included to represent the modified boundary condition. If region II were not present, ($L_2 = 0$) the hyperbolic cosine term in (3-8) would be one and $\gamma = 1$. That is, one would have the short-circuit condition again.

The short-circuit gate current fluctuations produced by sources in region II is given by[6]

$$\overline{\left|i_{g2}^2\right|} = \omega^2 I_d\left(\frac{64a^3 qD\Delta f}{\pi^5 V_s^5}\right)\left[\frac{L_1\kappa'(\gamma = 0)}{\varepsilon_r\varepsilon_o aZ(1-p)^2 r_d}\right]^2 \sin^2[\pi(1-p)/2]$$
$$\cdot \left(\exp \pi L_2/a - 4 \exp \pi L_2/2a + 3 + \pi L_2/a\right) \tag{3-13}$$

This contribution is quite similar to the drain circuit noise (3-4) which is also produced by the formation of dipole layers in region II.

3.3 THE CORRELATION COEFFICIENT

The Johnson noise produced in region I and the noise due to dipole layer generation in region II are independent of each other. However, the noise contributions from gate and drain for a given region are correlated. There is full correlation between i_{g2} and i_{d2} with a capacitive 90 degree phase shift between the currents. Thus,

$$\overline{i_{g2} * i_{d2}} = j \left[\left|\overline{i_{g2}^2}\right|\right] \cdot \left[\left|\overline{i_{d2}^2}\right|\right]^{1/2} \tag{3-14}$$

The correlation between i_{g1} and i_{d1} is not complete and the combined noise current is given by[8]

$$\overline{i_{g1} * i_{d1}} = j \left[\frac{S_o + S_\delta}{(R_o + R_\delta)^{1/2}(P_o + P_\delta)^{1/2}}\right]\left[\left|\overline{i_{g1}^2}\right|\right] \cdot \left[\left|\overline{i_{d1}^2}\right|\right]^{1/2} \tag{3-15}$$

where

$$S_o = (f_1)^{-2}\left\{\kappa'\left[(p^2 - s^2) - 4/3\,(p^3 - s^2) + 1/2\,(p^4 - s^4)\right] + \gamma\left[-2/3\,(p^3 - s^3) + (p^4 - s^4) - 2/5\,(p^5 - s^5)\right]\right\} \tag{3-16}$$

$$S_\delta = 2\delta(f_1)^{-2}(1 - p)^3\left\{(\kappa' - \gamma)\left[s - p + \ln\left(\frac{1 - s}{1 - p}\right)\right] + 1/2\,\gamma(p^2 - s^2)\right\} \tag{3-17}$$

The overall correlation coefficient is defined by the expression

$$jC = \overline{i_g^* i_d} \Big/ \left(\left|\overline{i_g^2}\right|\left|\overline{i_d^2}\right|\right)^{1/2} \tag{3-18}$$

$$= \left[\frac{S_o + S_\delta}{(R_o + R_\delta)^{1/2}(P_o + P_\delta)^{1/2}}\right] \cdot \left(\frac{\overline{i_{g1}^2}}{\overline{i_g^2}}\right)^{1/2}\left(\frac{\overline{i_{d1}^2}}{\overline{i_d^2}}\right)^{1/2} + \left(\frac{\overline{i_{g2}^2}}{\overline{i_g^2}}\right)^{1/2}\left(\frac{\overline{i_{d2}^2}}{\overline{i_d^2}}\right)^{1/2}$$

Substitution of equations (3-1) through (3-7), and equation (3-13) in equation (3-18) yields

$$C = \frac{S_o + S_\delta}{(R_o + R_\delta)^{1/2}\,(P_o + P_\delta)^{1/2}} \quad \sqrt{\frac{P_1 R_1}{PR}} + \sqrt{\frac{P_2 R_2}{PR}} \tag{3-19}$$

where

$$P_1 = \frac{(1 - p)}{f_1 f_g \gamma^2}(P_o + P_\delta) \tag{3-20}$$

$$P_2 = \frac{1 - p}{\xi f_r^2 f_g}\left(\frac{L}{a}\right) f_3 \tag{3-21}$$

$$P = P_1 + P_2 \tag{3-22}$$

$$R_1 = 4\left(\frac{L}{a}\right)^2 \left(\frac{f_1}{1 - p}\right)^3 \left(\frac{1}{\xi\gamma}\right)^2 \left(\frac{f_g}{f_c^2}\right)(R_o + R_\delta) \tag{3-23}$$

$$R_2 = 4\left(\frac{L}{a}\right)^3 \left[\frac{1}{\xi(1 - p)}\right]^3 \left(\frac{f_1^2 f_g}{f_r^2 f_c^2}\right) [\kappa'(\gamma = o)]^2 f_3 \tag{3-24}$$

$$R = R_1 + R_2 \tag{3-25}$$

$$f_3 = \frac{16}{\pi^3}\left(\frac{D}{D_o}\right)\left[\frac{\sin(\pi/2)(1 - p)}{(\pi/2)(1 - p)}\right]^2 \left(\exp\frac{\pi L_2}{a} - 4 \exp\frac{\pi L_2}{2a} + \frac{\pi L_2}{a}\right) \tag{3-26}$$

The final form of the correlated noise, given by (3-19), reflects the partial correlation between region I contributions (the first term) and the total correlation between region II contributions (the second term). The noise figure developed in the following sections will be expressed in terms of the quantities R, P and C listed here.

4. NOISE FIGURE ANALYSIS FOR THE FET

4.1 INTRODUCTION

The noise figure analysis to follow will be based on the equivalent circuit for the FET shown in Figure 2-3. The assumed configuration will be common source, with the gate considered as the input port and the drain considered as the output port. This configuration was chosen because it represents the typical front-end stage of a microwave receiver. Due to the amplification mechanism of the FET; the greater contribution to the overall noise figure of the device is provided by those elements connected to the input port; while the contribution to the noise by the elements connected to the output port is small; under this line of reasoning the noise contribution of the drain resistance and, the drain-gate capacitance C_{dg}, the source drain capacitance C_{sd}, and the parasitic resistance R_d (see Figure 2-3) can be neglected without incurring significant error and greatly simplifying the equivalent circuit to be used in the noise analysis (see Figure 4-1).

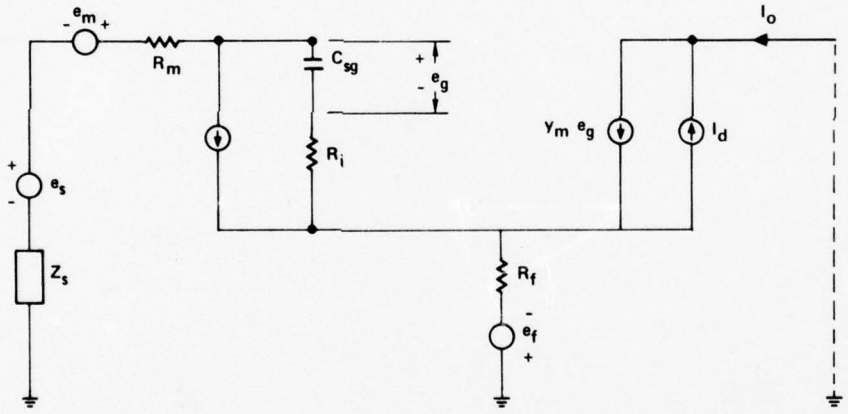


Figure 4-1. Simplified Equivalent Circuit Model

4.2 NOISE FIGURE DERIVATION

The intrinsic FET shown in the simplified schematic of Figure 4-1 can be represented by two short-circuit Y parameters.

$$Y_{11} = \frac{j\omega C_{sg}}{1 + j\omega C_{sg} R_i} \tag{4-1}$$

$$Y_{21} = \frac{g_m}{1 + j\omega C_{sg} R_i} \tag{4-2}$$

Also, the noise Figure F for this simplified circuit can be expressed as

$$F = 1 + \frac{\overline{|i_g + i_s + i_{go} + i_{do}|^2}}{\overline{|i_z|^2}} \tag{4-3}$$

where i_g, i_s, i_{go}, i_{do}, and i_z are the noise components in the short-circuited drain-source path produced by the noise generators e_{gn}, e_{sn}, i_g, i_d, and e_{zn}, respectively. The noise generators representing the extrinsic thermal sources R_g, R_s, and the real part of Z_s are given by their mean square values as

$$\overline{|e_{gn}^2|} = 4kT_o R_g \Delta f \tag{4.4}$$

$$\overline{|e_{s}^2{}_n|} = 4kT_o R_s \Delta f \qquad (T_o = 300^oK) \tag{4.5}$$

$$\overline{|e_z^2{}_n|} = 4kT_o (\mathrm{Re} Z_s) \Delta f \tag{4.6}$$

where "Re" denotes "real part of"

Analyzing the circuit of Figure 4-1, equation (4.3) can alternatively be expressed as

$$F = 1 + \frac{1}{\mathrm{Re} Z_s} \left\{ R_g + R_s + |R_g + R_s + Z_s|^2 \frac{\overline{|i_g^2|}}{4kT_o \Delta f} \right.$$

$$+ \left| \frac{1 + Y_{11} (R_g + R_s + Z_s)}{Y_{21}} \right|^2 \frac{\overline{|i_d^2|}}{4kT_o \Delta f} \tag{4.7}$$

$$\left. - 2\mathrm{Re} \left[(R_g + R_s + Z_s) \left(\frac{1 + Y_{11} (R_g + R_s + Z_s)}{Y_{21}} \right)^* \frac{i_g^* i_d}{4kT_o \Delta f} \right] \right\}$$

The terms of equation (4-7) that contain the intrinsic noise current sources i_g and i_d can be written alternatively as

$$\left|\frac{\overline{i_g^2}}{4kT_o\Delta f}\right| = \frac{\omega^2 C_{sg}^2}{g_m} R \tag{4-8}$$

$$\left|\frac{\overline{i_d^2}}{4kT_o\Delta f}\right| = g_m P \tag{4-9}$$

$$\frac{\overline{i_g^* i_d}}{4kT_o\Delta f} = \frac{jC\left(\left|\overline{i_g^2}\right|\left|\overline{i_d^2}\right|\right)^{1/2}}{4kT_o\Delta f} = jC\,\omega C_{sg}\,(RP)^{1/2} \tag{4-10}$$

where R_1 P and C are defined by equations (3-25), (3-27) and (3-19), respectively.

4.3 MINIMUM NOISE FIGURE

From equation (4-7) and using equations (4-8), (4-9), and (4-10) the minimum noise figure can be evaluated by setting the partial derivative of the noise figure with respect to the source impedance Z_s equal to 0. This yields

$$Z_s\ opt = R_s opt + j\,X_s\ opt \tag{4-11}$$

where

$$R_s opt = \left\{\left(R_g + R_s + Re\left[\frac{1 - C\,(R/P)^{1/2}}{Y_{11}\left[1 - C(R/P)^{1/2}\right]^2 - (1 - C^2)\,R/P}\right]\right)^2 \right. \tag{4-12}$$

$$\left. + \left[\frac{g_m\left(R_g + R_s\right) + K_r\left(1 + \omega^2 C_{sg}^2 R_i^2\right)}{\omega^2 C_{sg}^2 K_g}\right]^2\right\}^{1/2}$$

$$X_s opt = -Im\left[\frac{1 - C(R/P)^{1/2}}{Y_{11}\left[1 - C(R/P)^{1/2}\right]^2 - (1 - C^2)R/P}\right] \tag{4-13}$$

where

$$K_r = \frac{R(1 - C^2)}{\left[1 - C\,(R/P)^{1/2}\right]^2 + (1 - C^2)\,R/P} \tag{4-14}$$

and "Im" denotes "imaginary part of"

$$K_g = P\left\{[1 - C(R/P)^{1/2}]^2 + (1 - C^2)\, R/P\right\} \qquad (4\text{-}15)$$

With this optimum source impedance given by equation (4-11) the minimum noise figure can be found by substitucion of equation (4-11) into equation (4-7). Also since the noise figure is a frequency dependent function, equation (4-7) can be expanded as a power series in ω; this yields

$$F_{min} = 1 + 2\left(\frac{f}{f_T}\right)\left\{PR\,(1 - C^2) + g_m\left(\frac{T}{T_o}\right)(R_g + R_s)\left[P(1 - C(R/P)^{1/2})^2 + R(1 - C^2)\right]\right\}^{1/2}$$

$$+ 2\left(\frac{f}{f_T}\right)^2\left\{g_m\left(\frac{T}{T_o}\right)(R_g + R_s)\,P\left[(1 - C(R/P)^{1/2})^2 + ((1 - C^2)\,R/P)\right]\right. \qquad (4\text{-}16)$$

$$\left. + g_m R_i P\left[1 - C(R/P)^{1/2}\right]\right\}$$

where the term $\omega C_{sg}/g_m$ in the expansion has been expressed as f/f_T ($f_T = g_m/2\pi C_{sg}$). f_T is the gain-bandwidth product of the FET or the frequency at which the current gain of the device drops to unity.

4.4 TEMPERATURE EFFECTS ON NOISE FIGURE

From Equation (4-16) the straight-forward depence of noise figure on the device temperature can be observed in the terms that contain the ratio T/T_o. There is, however, a very strong dependence of gain on the ratio T/T_o given by the expression

$$g_m = \frac{f_g(s,p)}{W_{oo}}\,(2aZE_s)\,(\mu_o N_o)\left(\frac{T}{T_o}\right)^{1.5} \qquad (4\text{-}17)$$

From equations (4-16) and (4-17), it can clearly be observed that the dependence of noise figure on temperature can best be evaluated by a numerical process. After describing the contributions of the ancillary regions to FET noise figure, the results of the numeral analysis will be presented.

5. FET WITH VARIABLE DOPING PROFILE

5.1 SMALL SIGNAL PARAMETERS

Consider the FET as shown in Figure 2-5 with a doping concentration N(y) which is a function of the depth below the gate. It is convenient for the analysis to follow, to change the coordinate system in Figure 2-5 such that y = 0 at the upper left-hand corner of the region under the gate and consider only the upper half of the device. By Poisson's equation

$$\frac{dE_y}{dy} = \frac{q}{\epsilon_r \epsilon_o} N(y) \tag{5-1}$$

and

$$E_y(y) = \frac{q}{\epsilon_r \epsilon_o} \left[\overline{N(y)} + C_1\right] \tag{5-2}$$

where the notation $\overline{N(y)}$ represents

$$\int_o^y N(y)\, dy$$

Similarly, (5-3)

$$\overline{\overline{N(y)}} = \int_o^y \overline{N(y)}\, dy$$

At the depletion depth $y = y_d$, it is required that $E_y = 0$; thus from equation (5-2)

$$E_y(y_d) = \frac{q\left[\overline{N(y_d)}\right]}{\epsilon_r \epsilon_o} + C_1 = 0 \tag{5-4}$$

and

$$E_y(y) = \frac{q}{\epsilon_r \epsilon_o} \left[\overline{N(y)} - \overline{N(y_d)}\right] \tag{5-5}$$

The potential across the depletion layer can be obtained by direct integration of equation (5-5). Thus,

$$W(y) = \int \bar{E_y} \cdot d\bar{y} = \int E_y dy = \frac{q}{\epsilon_r \epsilon_o} \left[\overline{N(y)} - y\ \overline{N(y_d)} + C_2\right] \tag{5-6}$$

since $W(y) = 0$ at $z = 0$ the constant C_2 in equation (5-6) can be evaluated as $C_2 = -\overline{N(0)}$

and

$$W(y) = \frac{q}{\epsilon_r \epsilon_o} \left[\overline{N(y)} - y\ \overline{N(y_d)} - \overline{N(0)}\right] \tag{5-7}$$

Equation (5-7) is analogous to equation (2-12) of the constant doping profile case. It is convenient for the following analysis to introduce the dimensionless variable $\omega = y/a$† where ω runs from 0 to 1 across the epilayer; using this dimensionless variable equation (5-7) can be rewritten as

$$W(\omega) = \frac{qa^2}{\epsilon_r \epsilon_o} \left[\overline{\overline{N(\omega)}} - \omega\ \overline{N(\omega_d)}\right] \tag{5-8}$$

where the term $\overline{N(0)} = 0$ has been dropped.

In equation (5-8)

$$\overline{N(\omega)} = \int_0^{\omega} N(\omega) d\omega \text{ and } \overline{\overline{N(\omega)}} = \int_0^{\omega} \overline{N(\omega)} d\omega$$

The potential across the depletion region is $W(\omega_d)$ where

$$W(\omega_d) = \frac{qa^2}{\epsilon_r \epsilon_o} \left[\overline{N(\omega_d)} - \omega_d\ \overline{N(\omega_d)}\right] \tag{5-9}$$

By considering the integral

$$\int_0^{\omega_d} \omega\ N(\omega) d\omega$$

---

†ω when used as normalized channel depth is not to be confused with angular frequency.

and integrating by parts; it can be shown that:

$$\int_0^{\omega_d} \omega\, N(\omega)\, d\omega = \omega_d\, \overline{N(\omega_d)} - \int_0^{\omega_d} N(\omega)\, d\omega \tag{5-10}$$

thus equation (5-9) can be alternately written as

$$W(\omega_d) = \frac{-qa^2}{\varepsilon_r \varepsilon_o} \int_0^{\omega_d} \omega\, N(\omega)\, d\omega \tag{5-11}$$

Using equation (5-11), the potential required to deplete the entire epilayer of carriers is

$$W_{oo} = \frac{qa^2}{\varepsilon_r \varepsilon_o} \left[\overline{N(1)} - \overline{\overline{N(1)}}\right] = \frac{qa^2}{\varepsilon_r \varepsilon_o} \int_0^1 \omega\, N(\omega)\, d\omega \tag{5-12}$$

The potential expressed by equation (5-12) is analogous to W_{oo} of equation (2-6) for the constant doping profile case.

To calculate the total drain current flowing in the channel, one can follow a procedure very similar to that of Section 2.2, equations (2-16) through (2-20), and by Ohm's law at a distance x from the source

$$I_d = q\mu_o Z \left[\int_{y_d}^{a} N(y_d)\, dy\right] E_x(x) \tag{5-13}$$

Using the dimensionless variable ω, equation (5-13) can also be written as

$$\begin{aligned} I_d &= q\mu_o Z a E_x(x) \int_{\omega_d}^{1} N(\omega)\, d\omega \\ &= q\mu_o Z a E_x(x) \left[\overline{N(1)} - \overline{N(\omega_d)}\right] \end{aligned} \tag{5-14}$$

To evaluate $E_x(x)$ one can start from equation (2-2) properly modified for the variable profile case, thus:

$$E_x(x) = -\frac{dV(x)}{dx} \tag{5-15}$$

$$E_x(x) = -\frac{d}{dx}\left[V_{sg} + \phi - W(\omega_d)\right]$$

$$E_x(x) = \frac{d\omega_d}{dx} \cdot \frac{dW(\omega_d)}{d\omega_d}$$

and from equation (5-11)

$$\frac{dW(\omega_d)}{d\omega_d} = \frac{qa^2}{\varepsilon_r \varepsilon_o}\, \omega_d\, N(\omega_d) \tag{5-16}$$

Using equations (5-15) and (5-16), equation (5-14) becomes:

$$I_d = \frac{\mu_o Z q^2 a^3}{\varepsilon_r \varepsilon_o} \left[\overline{N(1)} - \overline{N(\omega d)}\right] \omega_d\, N(\omega_d)\, \frac{d\omega_d}{dx} \tag{5-17}$$

Integration of equation (5-17) over the length of region I i.e., from $x = 0$ to $x = L_1$ yields (dropping subscripts)

$$I_d = \frac{\mu_o Z q^2 a^3}{\varepsilon_r \varepsilon_o L_1}\, f_1(s,p) \tag{5-18}$$

where

$$f_1(s,p) = \overline{N(1)} \int_s^p \omega N(\omega) d\omega - \int_s^p \omega N(\omega)\, \overline{N(\omega)}\, d\omega \tag{5-19}$$

In equation (5-19) the quantities s and p represent the values of $\omega = y/a$ at $x = 0$ and $x = L_1$, respectively. Also the function $f_1(s,p)$ described by equation (5-19) is analogous to the one described by equation (2-20) in the constant doping profile case.

From the general equations (2-3) and (2-4) it can be concluded that the potential drop from $x = 0$ to $x = L_1$ (across region I) is

$$V(L_1) - V(0) = W_p - W_s \tag{5-20}$$

Also since at $x = L_1$ the carriers reach their saturation velocity and $E_x(x) = E_s$, then the expression for the drain current in region II is

$$I_d = q\mu_o Z a E_s \left[\overline{N(1)} - \overline{N(p)}\right] \tag{5-21}$$

Thus equations (2-3), (2-4), (5-18), (5-19), (5-20), and (5-21) establish relations between the quantities s, p, L_1 and I_d to the potentials V_{sg}, $V(L_1)$ and the corresponding doping density integrals.

In region II the potential function $\phi(x,y)$ is assumed to be determined by the charges in the depleted region and free charges on the drain electrode, consequently,

$$\phi(x,y) = \phi_1(x,y) + \phi_2(x,y) \tag{5-22}$$

where $\phi_1(x,y)$ is the potential due to the depletion charges and $\phi_2(x,y)$ is the potential due to free charges on the drain. To solve for $\phi_2(x,y)$ the process to follow is that of Section 2.2, equations (2-31) and (2-32); this yields the result.

$$\phi_2(x,y) = \frac{2a}{\pi} E_s \sin\left(\frac{\pi y}{2a}\right) \sinh\left[\frac{\pi(x - L_1)}{2a}\right] \tag{5-23}$$

From equation (5-7) the potential $\phi_1(x,y)$ is obtained as

$$\phi_1(x,y) = \frac{q}{\varepsilon_r \varepsilon_o}\left[\overline{\overline{N(y)}} - y\,\overline{N(pa)}\right] \tag{5-24}$$

However, this potential given by equation (5-24) gives no E_x contribution in region II, gives zero electric field at the channel and zero potential at $y = 0$; consequently, the potential due to $\phi_1(x,y) + \phi_2(x,y)$ measured along the channel from $x = L_1$ to $x = L_2$ is due entirely to ϕ_2. Adding the potential drop from $x = 0$ to $x = L$ one can obtain from equations (5-20) and (5-23) the source to drain voltage given by

$$V_{sd} = W(p) - W(s) + \frac{2a}{\pi} E_s \sinh\left[\frac{\pi(L - L_1)}{2a}\right] \tag{5-25}$$

Equation (5-25) with equations (5-18) and (5-20) enables one to solve for the current-voltage relationship of the FET. From equations (5-18) and (5-21) I_d can be eliminated; this yields

$$L_1 = \frac{qa^2}{\varepsilon_r \varepsilon_o E_s}\left[\frac{f_1(s,p)}{\overline{N(1)} - \overline{N(p)}}\right] \tag{5-26}$$

Equation (5-26) is analogous to equation (2-25) for the constant profile case but $f_1(s,p)$ is given in this case by equation (5-19).

Just as in the constant doping profile case, equations (5-25) and (5-26) form a pair that need to be solved simultaneously in order to determine p, s, then L_1 and I_d.

5.1.1 Transconductance

Following the same procedure as the one outlined in Section 2.2.1 and from equations (2-38), (5-11), (5-20), (5-21), (5-25), and (5-26), the expression for the

transconductance for the variable doping profile case can be shown to be

$$g_m = \frac{\varepsilon_r \varepsilon_o \mu_o Z E_s}{a} f_g(s,p) \tag{5-27}$$

where

$$f_g(s,p) = \frac{[\overline{N(1)} - \overline{N(s)}] \cosh(\pi L_2/2a) - [\overline{N(1)} - \overline{N(p)}]}{\left\{p[\overline{N(1)} - \overline{N(p)}] + \varepsilon_r \varepsilon_o E_s L_1/qa^2\right\} \cosh(\pi L_2/2a) - p[\overline{N(1)} - \overline{N(p)}]} \tag{5-28}$$

This expression given by equation (5-28) reduces to that of equation (2-45) when $N(\omega) = N_o$ = constant.

5.1.2 Output Resistance

Following the same procedure as the one outlined in Section 2.2.2 and using equations (2-46), (5-25), and (5-26) the expression for the output resistance can be obtained as

$$r_d = \frac{a}{\varepsilon_r \varepsilon_o \mu_o Z E_s} f_r(s,p) \tag{5-29}$$

where

$$f_r(s,p) = \frac{[\cosh(\pi L_2/2a) - 1]\left\{p[\overline{N(1)} - \overline{N(p)}]\right\} + (\varepsilon_r \varepsilon_o E_s L_1/qa^2)\cosh(\pi L_2/2a)}{\overline{N(1)} - \overline{N(p)}} \tag{5-30}$$

5.1.3 Gate Source Capacitance

From Section 2.2.3 and using equations (2-49), (5-23) through (5-26) the gate-source capacitance can be expressed as

$$C_{sg} = C_1 + C_2 + 1.56\,\varepsilon_r \varepsilon_o Z \tag{5-31}$$

where C_1 and C_2 are the capacitance contributions due to regions I and II, respectively. The numerical term accounts for the fringing capacitance as in the constant profile case. The capacitance contribution due to region I is given by

$$C_1 = \frac{qaZ}{E_s}\left\{f_g(s,p)\left[p\overline{N(p)} + \frac{f_2(s,p)}{[\overline{N(1)} - \overline{N(p)}]^2}\right] - \left[\frac{\overline{N(1)} - \overline{N(S)}}{\overline{N(1)} - \overline{N(p)}}\right]\overline{N(s)}\right\} \tag{5-32}$$

where

$$f_2(s,p) = \overline{N(1)} \int_s^p \omega_d N(\omega_d)\ \overline{N(\omega_d)}\ d\omega_d - \int_s^p \omega_d N(\omega_d)\ \left[\overline{N(\omega_d)}\right]^2 d\omega_d \qquad (5\text{-}33)$$

and the capacitance contribution due to region II is

$$C_2 = \frac{\varepsilon_r \varepsilon_o Z\ L_2}{a} f_g(s,p) + \left[\frac{qaZ\overline{N(p)} + \varepsilon_r \varepsilon_o Z\ E_s \sinh(\pi L_2/2a)}{E_s \cosh(\pi L_2/2a)}\right] \cdot\left[1 - f_g(s,p)\right] \qquad (5\text{-}34)$$

5.1.4 Gate Charging Resistance

On the basis of the assumption of Section 2.2.4 that the time constant $\tau = R_i C_{sg}$ is proportional to the transit time through the channel one can write

$$\tau = \int_0^{L_1} \frac{dx}{\mu_o E_x(x)} + \int_{L_1}^{L} \frac{dx}{v_s} \qquad (5\text{-}35)$$

The first integral on the right-hand side of equation (5-35) can be evaluated using equations (5-14) and (5-17) thus:

$$\frac{1}{\mu_o}\int_0^{L_1} \frac{dx}{E_x(x)} = \frac{q^3 \mu_o Z^2 a^4}{\varepsilon_r \varepsilon_o I_d^{\,2}} \int_0^{L_1} \left[\overline{N(1)} - \overline{N(\omega_d)}\right]\ \omega_d N(\omega_d)\ d\omega_d \qquad (5\text{-}36)$$

The second integral on the right-hand side of equation (5-35) is simply L_2/v_s, consequently, from equations (5-35) and (5-36)

$$R_i = \frac{1}{C_{sg}}\left[\frac{q^3 \mu_o Z^2 a^4}{\varepsilon_r \varepsilon_o I_d^{\,2}} \int_0^{L_1} \left[\overline{N(1)} - \overline{N(\omega_d)}\right]\ \omega_d N(\omega_d)\ d\omega_d + \frac{L_2}{\mu_o E_s}\right] \qquad (5\text{-}37)$$

5.2 NOISE ANALYSIS FOR THE INTRINSIC FET WITH VARIABLE DOPING PROFILE

5.2.1 Drain Circuit Noise

The open-circuit voltage fluctuation produced by sources in region I for the variable doping profile case is

$$\overline{|v_{d1}^2|} = \frac{4kT\,\Delta f}{I_d}\left(\frac{P_o + P_\delta}{[\overline{N(1)} - \overline{N(p)}]^2}\right)\cosh^2\left(\frac{\pi L_2}{2a}\right) \tag{5-38}$$

where

$$P_o = \int_s^p [\overline{N(1)} - \overline{N(\omega)}]^2\,\omega\,N(\omega)\,d\omega \tag{5-39}$$

and

$$P_\delta = \delta\,[\overline{N(1)} - \overline{N(p)}]^3 \int_s^p \frac{\omega\,N(\omega)\,d\omega}{[\overline{N(1)} - \overline{N(\omega)}]} \tag{5-40}$$

whereas the open circuit drain voltage fluctuation produced by sources in region II is given by the same expression as for the constant doping profile case or equation (3-4), equations (5-38) through (5-40) are analogous to equations (3-1) through (3-3), respectively. As in the constant doping profile case, the noise voltage contributions of the two regions are uncorrelated and their mean squares added.

5.2.2 Gate Circuit Noise

The short-circuit gate current fluctuation produced by sources in region I for the variable doping profile is

$$\overline{|i_{g1}^2|} = \omega^2\left(\frac{qaZL_1}{r_d I_d}\right)^2\left(\frac{qa^2}{\varepsilon_r\varepsilon_o I_d}\right)\frac{\cosh^2(\pi L_2/2a)}{[\overline{N(1)} - \overline{N(p)}]^2}(R_o + R_\delta) \tag{5-41}$$

where

$$\gamma = 1 + \left(\frac{qa^2}{\varepsilon_r\varepsilon_o}\right)\frac{p\,[\overline{N(1)} - \overline{N(p)}]}{E_s L_1}\left[1 - \frac{1}{\cosh(L_2/2a)}\right] \tag{5-42}$$

and

$$R_o = \int_s^p \left[-\kappa' + \gamma\,\overline{N(\omega_d)}\right]^2 \left[\overline{N(1)} - \overline{N(\omega_d)}\right]^2 \omega_d\, N(\omega_d)\, d\omega_d \qquad (5\text{-}43)$$

$$R_\delta = \delta\left[\overline{N(1)} - \overline{N(p)}\right]^3 \int_s^p \frac{\left[-\kappa' + \gamma\,\overline{N(\omega_d)}\right]^2}{\left[\overline{N(1)} - \overline{N(\omega_d)}\right]}\, \omega_d\, N(\omega_d)\, d\omega_d \qquad (5\text{-}44)$$

$$\kappa' = \frac{\mu_o q^2 a^3 Z}{\varepsilon_r \varepsilon_o I_d L_1} \int_s^p f_1(\omega_d, s)\, N(\omega_d)\, d\omega_d + \int_o^p \gamma\, N(\omega_d)\, d\omega_d + \frac{L_2}{L_1}\left[\overline{N(1)} - \overline{N(p)}\right] \qquad (5\text{-}45)$$

Equations (5-41) through (5-45) are analogous to equations (3-7) through (3-10) and equation (3-12) respectively for the constant doping profile case.

The short circuit gate current fluctuation produced by sources in region II is given by the same expression as for the constant doping profile case or equation (3-13).

5.2.3 Correlation Coefficient

Following the same argument given in Section 3.3, the correlation coefficient C is given by equation (3-19) in which the expressions for P_o, P_δ, R_o, R_δ are given by equations (5-39), (5-40), (5-43) and (5-44), respectively. For S_o and S_δ the expressions are

$$S_o = -\int_s^p \left[-\kappa' + \gamma\,\overline{N(\omega_d)}\right]\left[\overline{N(1)} - \overline{N(\omega_d)}\right]^2 \omega_d\, N(\omega_d)\, d\omega_d \qquad (5\text{-}46)$$

$$S_\delta = -\delta\left[\overline{N(1)} - \overline{N(p)}\right]^3 \int_s^p \left[\frac{-\kappa' + \gamma\,\overline{N(\omega_d)}}{\overline{N(1)} - \overline{N(\omega_d)}}\right] \omega_d\, N(\omega_d)\, d\omega_d \qquad (5\text{-}47)$$

and for P_1, P_2, P , R_1, R_2 and R the expressions are

$$P_1 = \left(\frac{qa^2}{\varepsilon_r \varepsilon_o r_d^2\, g_m I_d}\right) \frac{\cosh^2(\pi L_2/2a)}{\left[\overline{N(1)} - \overline{N(p)}\right]^2}\,(P_o + P_\delta) \qquad (5\text{-}48)$$

$$P_2 = \left(\frac{aI_d}{4\, g_m r_d^{\,2}\, \mu_o^{\,2}\, E_s^{\,3}\, \varepsilon_r^{\,2}\, \varepsilon_o^{\,2}\, Z^2} \right) f_3 \tag{5-49}$$

$$P = P_1 + P_2 \tag{5-50}$$

$$R_1 = \left(\frac{q^3 a^4 Z^2 L_1^{\,2} g_m}{r_d^{\,2}\, \varepsilon_r \varepsilon_o I_d^{\,3}\, C_{sg}^{\,2}} \right) \frac{\cosh^2 (\pi L_2/2a)}{[\overline{N(1)} - \overline{N(p)}]^2} (R_o + R_\delta) \tag{5-51}$$

$$R_2 = \left(\frac{q^2 a^3 L_1^{\,2} g_m}{4 r_d^{\,2}\, \varepsilon_r^{\,2}\, \varepsilon_o^{\,2}\, I_d\, C_{sg}^{\,2}\, \mu_o^{\,2}\, E_s^{\,3}} \right) (\quad)^2 f_3 \tag{5-52}$$

$$R = R_1 + R_2 \tag{5 53}$$

The function f_3 of equations (5-49) and (5-52) is the same as for the constant doping profile case and is given by equation (3-26).

5.3 NOISE FIGURE ANALYSIS FOR THE INTRINSIC FET

The process to follow in order to obtain the noise figure for the FET with variable doping profile is the same as the one outlined in Section 4.2; this leads to identical expressions as those given in that section; consequently, they will not be rewritten here. It must be understood, however, that the expressions for P_1, P_2, P, R_1 and R_2 are given by equations (5-48) through (5-52), respectively. The same line of argument is followed for the minimum noise figure derivation of Section 4.3 and the temperature effects on noise figure expression of Section 4.4.

$$P_2 = \left(\frac{a I_d}{4\, g_m r_d^2 \mu_o^2 E_s^3 \varepsilon_r^2 \varepsilon_o^2 Z^2} \right) f_3 \tag{5-49}$$

$$P = P_1 + P_2 \tag{5-50}$$

$$R_1 = \left(\frac{q^3 a^4 Z^2 L_1^2 g_m}{r_d^2 \varepsilon_r \varepsilon_o I_d^3 C_{sg}^2} \right) \frac{\cosh^2 (\pi L_2/2a)}{[\overline{N(1)} - \overline{N(p)}]^2} (R_o + R_\delta) \tag{5-51}$$

$$R_2 = \left(\frac{q^2 a^3 L_1^2 g_m}{4 r_d^2 \varepsilon_r^2 \varepsilon_o^2 I_d C_{sg}^2 \mu_o^2 E_s^3} \right) (\quad)^2 f_3 \tag{5-52}$$

$$R = R_1 + R_2 \tag{5-53}$$

The function f_3 of equations (5-49) and (5-52) is the same as for the constant doping profile case and is given by equation (3-26).

5.3 NOISE FIGURE ANALYSIS FOR THE INTRINSIC FET

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6. ANCILLARY REGIONS

For the purpose of developing analytical expressions for the parasitic resistance R_g, R_s, and R_d it is convenient to set up a coordinate system and establish dimensions (see Figure 2-4) as shown in Figure 6-1.

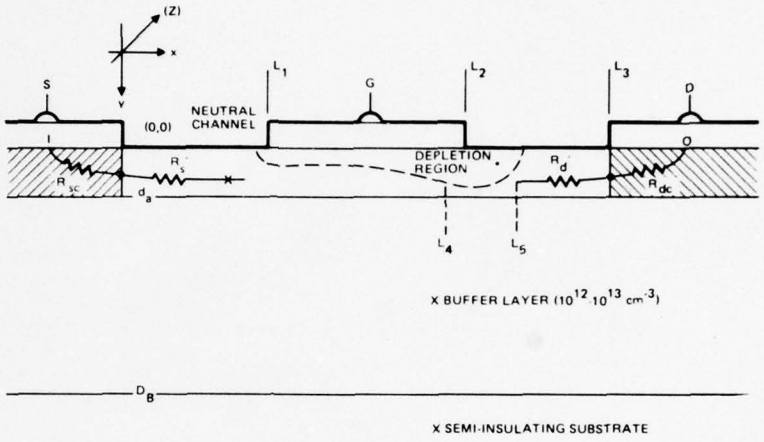

Figure 6-1. FET Cross-section

6.1 PARASITIC SOURCE RESISTANCE

The parasitic source series resistance consists of a metal sheet resistance term similar to the gate series resistance, but also includes contact resistance from metal to GaAs (R_{sc}) and channel resistance between the gate and source contact metallizations (R_s'). If ρ_{sch} is the sheet resistance of the channel, R_s' (Figure 6-1) may be estimated as

$$R_s' = \frac{\rho_{sch}\ L_1}{Z} \tag{6-1}$$

The contact resistance may be described as a distributed resistor network as indicated in Figure 6-2. The equations which describe this system are

$$I(x) = \int_0^x V(x)\ G\ dx\ ;\ \text{or,}\ \frac{\partial I}{\partial x} = V(x)\ G \tag{6-2}$$

$$V(x) = V(0) + \int_0^x I(x)\, R\, dx \;;\; \text{or,}\; \frac{\partial V}{\partial x} = I(x)\, R \qquad (6\text{-}3)$$

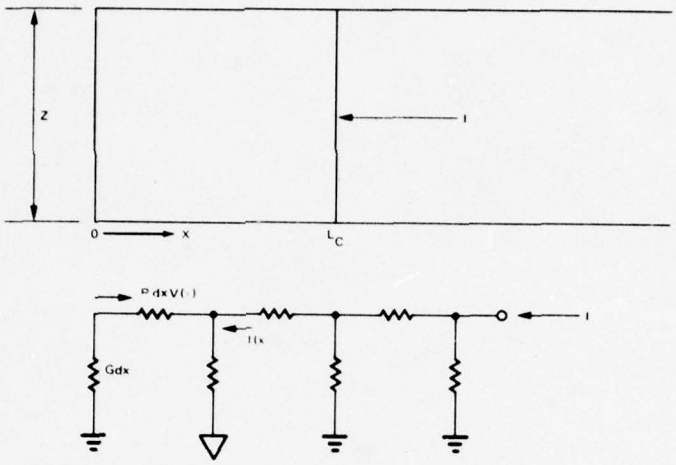

Figure 6-2. Contact Resistance and Equivalent Circuit

These can be combined to a single equation

$$\frac{\partial^2 I}{\partial x^2} = RG\, I(x) \qquad (6\text{-}4)$$

G is determined by the specific contact resistance, ρ_c, which is typically 10^{-4} Ω - cm^2

$$G = \frac{Z}{\rho_c}$$

R is determined by the sheet resistance of the GaAs under the contact metal. For an active implant of $10^{14}/cm^2$, this sheet should be $\rho_{sco} \approx 15\ \Omega/\square$

$$R = \frac{\rho_{sco}}{Z}$$

thus

$$\gamma^2 = RG = \left(\frac{\rho_{sco}}{\rho_c}\right) \approx 1.5 \times 10^5$$

solutions to 6.3 have the form

$$I = Ae^{\gamma x} + Be^{-\gamma x} \tag{6-5}$$

The boundary conditions are that

$$I = 0 \text{ @ } x = 0$$

$$I = I_c \text{ @ } x = L_c$$

thus

$$I = I_c \left(e^{\gamma x} - e^{-\gamma x}\right) \Big/ \left(e^{\gamma L_c} - e^{-\gamma L_c}\right) \tag{6-6}$$

$$V(x) = \frac{1}{G} \frac{\partial I}{\partial x}$$

or

$$V(x) = \frac{I_c \gamma}{G} \left[\frac{\left(e^{\gamma x} + e^{-\gamma x}\right)}{\left(e^{\gamma L_c} - e^{-\gamma L_c}\right)}\right] \tag{6-7}$$

Contact resistance is $V(L_c)/I(L_c)$, so

$$R_{sc} = \frac{(\gamma/G)\left(e^{\gamma L_c} + e^{-\gamma L_c}\right)}{\left(e^{\gamma L_c} - e^{-\gamma L_c}\right)}$$

but

$$\gamma = \sqrt{RG}$$

so

$$R_{sc} = \frac{(\rho_{sco}\,\rho_c)^{1/2}}{Z}\left(\frac{1 + e^{-2\gamma L_c}}{1 - e^{-2\gamma L_c}}\right) \tag{6-8}$$

Clearly, the most effective way to minimize R_{sc} is to minimize both ρ_{sco} and ρ_c and make $2\gamma L_c >> 1$. For the values quoted, $2\gamma L_c \approx 1$ at L_c = 13 μm, indicating that contact resistance cannot be improved by making contacts longer than about 40 μm. Total resistance R_s is therefore

$$R_s = \frac{(\rho_{sco}\,\rho_c)^{1/2}}{Z}\,\frac{\left(1 + e^{-2\,\frac{(\rho_{sco})^{1/2}}{(\rho_c)^{1/2}}\,L_c}\right)}{\left(1 - e^{-2\,\frac{(\rho_{sco})^{1/2}}{(\rho_c)^{1/2}}\,L_c}\right)} + \frac{\rho_{sch}\,L_1}{} + \frac{\rho_{shs}\,L_c}{2Z} \tag{6 9}$$

here

ρ_{sco} = sheet resistance of GaAs under contact metal

ρ_c = specific contact resistivity – metal to GaAs

ρ_{sch} = sheet resistance of channel between contact and gate

L_c = contact length

L_1 = space contact to gate

ρ_{shs} = sheet resistance of source contact metal

Z = device width

6.2 PARASITIC DRAIN RESISTANCE

The parasitic drain resistance R_d is calculated the same way as R_s, with L_1 replaced by $L_3 - L_2$ and L_c replaced by the drain contact length. In fact, most device designs have symmetrical source and drain geometries, leading to $R_d = R_s$.

6.3 PARASITIC GATE RESISTANCE

The parasitic gate series resistance R_g is due to the series resistance of the gate metallization; for the single lump equivalent circuit it is the resistance from the gate terminal to the center of the device

$$R_g \approx \frac{\rho_{shg} Z}{2 L_g} \tag{6-10}$$

where ρ_{shg} is the sheet resistance of the gate metallization, Z is the gate width, and L_g is the gate length ($L_g = L_2 - L_1$ in Figure 6-1). R_g can be minimized by keeping ρ_{shg} low (thick aluminum) or by keeping the effective Z small by paralleling several devices with small gate widths rather than using a single device with large gate width.

6.4 SOURCE-DRAIN AND GATE-DRAIN CAPACITANCES

The expression for inter-electrode capacitances between parallel strips immersed in an infinite dielectric medium was developed by Smythe[9]; modifying his expression to account for the air dielectric above the electrodes the expression for both capacitances C_{dg} and C_{sd} becomes

$$C_{dg},\ C_{sd} = (\varepsilon_r + 1)\ \varepsilon_o Z\ \frac{K\left[(1-k^2)^{1/2}\right]}{K(k)} \tag{6-11}$$

where K(k) is the complete elliptical integral of the first kind given by[10]

$$K(k) = \int_0^{\pi/2} (1 - k \sin^2 \theta)^{-1/2}\ d\theta \tag{6-12}$$

the argument k of equations (6-11) and (6-12) is given by

$$k_{dg} = \left[\frac{L_3 - L_2}{(L_3 - L_2) + (L_2 - L_1)}\right]^{1/2}$$

$$k_{sd} = \left[\frac{(2L_s + L_3)L_3}{(L_s + L_3)^2}\right]^{1/2}$$

7. DC CHARACTERISTICS

The drain gate characteristics of Schockley's FET model are shown in Figure 7-1. Here the bias voltages are expressed in terms of the pinchoff voltage W_{oo} given by equation (2-6); this allows a full analytic treatment of the FET.

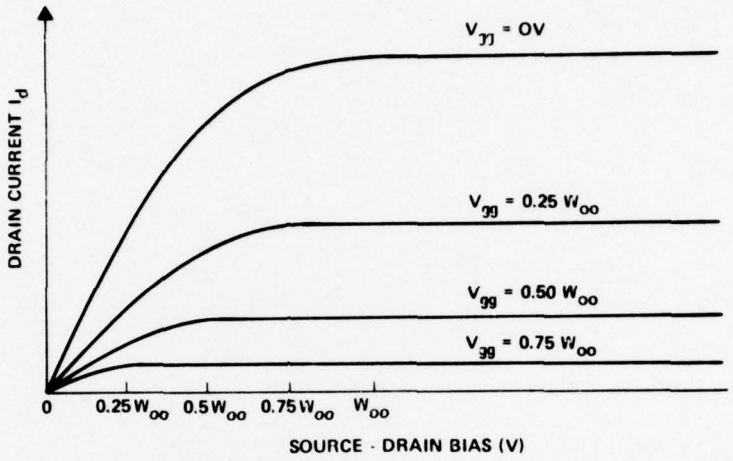

Figure 7-1. Drain Current-Voltage Characteristics for an FET Following Pucel et al[6]. Bias Voltages are Expressed in Terms of the Pinchoff Voltage, W_{oo}.

To obtain the dc characteristics of a FET under study, equations (2-24) and (2-36) must be solved simultaneously; in the case of the FET with variable doping profile the corresponding equations are (5-18) and (5-25). A graph of these dc characteristics for two different cases of doping profile are shown in the next part of this section.

8. COMPUTER MODEL

From the analytical model for the FET developed in Sections 2 through 6, it is obvious that the task of finding the dependence of noise figure, or transconductance on device geometry, doping density, and biasing conditions can best be achieved by numerical methods. The flow diagram of the FET computer model developed by TRW to do this task is shown in Figure 8-1.

The program accepts as initial inputs the physical dimensions of the region under the gate, intended frequency of operation, and doping density of the channel. With these inputs the program proceeds to evaluate every coefficient of equation (4-16) separately and calculates at the end of block 3 the minimum noise figure for the intrinsic FET ($R_g = R_s = 0$). Also if desired, the doping density of the channel can be optimized for minimum noise figure. The results of this optimization process for devices of 1 and 0.5 μm gate lengths can be seen in Figure 8-2. Another option existing at the end of block 3 is noise figure versus frequency. Figure 8-3 shows this relationship for two 1 μm gate length devices that have been optimized for 300 and 77°K operation. From Figure 8-3 it can be concluded that bringing the ambient temperature of the device down from 300 to 77°K reduces the noise figure by a factor of 3. Figure 8-4 shows the behavior of f_T as a function of device temperature for the 1 μm gate length FET; it can be concluded from this figure that with adequate cooling, millimeter wave amplification using FET devices is potentially viable.

Once the design for the intrinsic FET is satisfactory the program proceeds to add the ancillary regions by accepting data such as interelement spacing, contact lengths, and doping concentration of implants. With this information and by the use of the equations of Section 5, the parasitic resistances are calculated as well as the parasitic capacitances. This process takes place in blocks 5 through 7 of Figure 8-1. At this point the noise figure for the nonintrinsic device ($R_g \neq 0$, $R_s \neq 0$) is evaluated and the ancillary regions redesigned if desired. Blocks 8 and 9 compute the dc parameters and the dynamic range of the device under analysis; these intermediate results compared with preliminary tests of production wafers will help decide whether the wafer under test will meet the necessary requirements for low noise FETs or not. The decision at this point is important since the process of finishing a semiconductor wafer is expensive and time consuming; this interaction with the manufacturing process is indicated by blocks 14, 15, 16, and 17. Block numbers 11, 12, and 13 are existing subroutines in TRW/TSS that compute the S parameters, plot constant gain circles, and constant noise figure circles if desired.

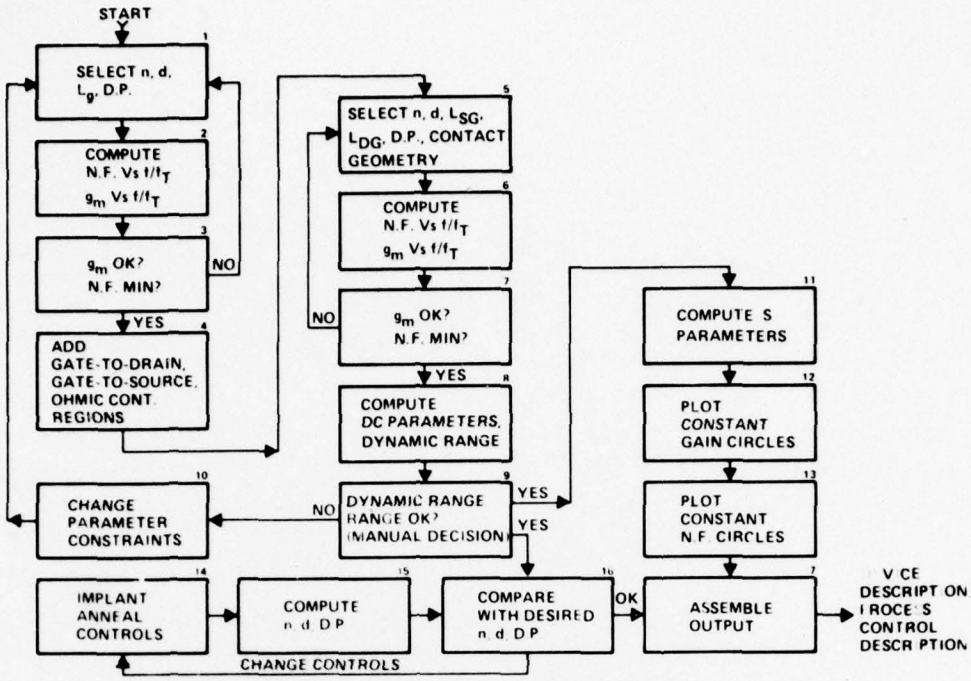

Figure 8-1. Flow Diagram for FET Computer Model

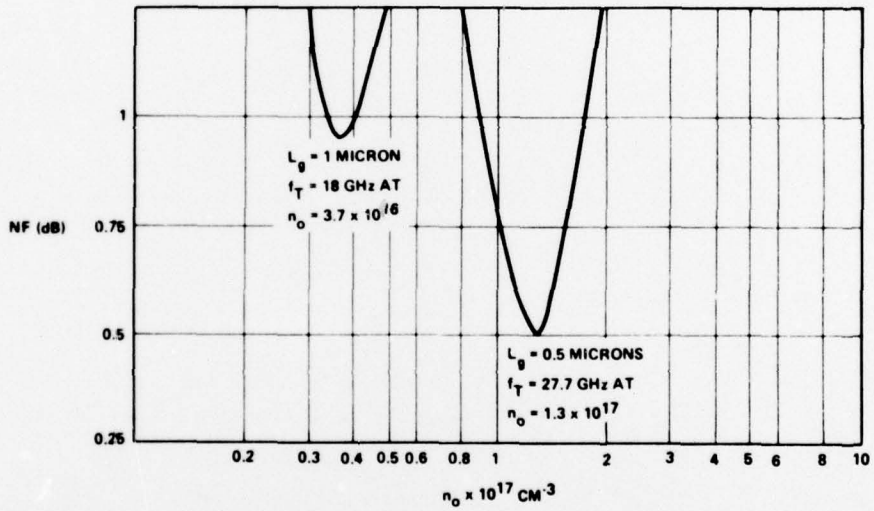

Figure 8-2. Intrinsic FET Noise Figures (12 GHz)
V_{sg} = 0 Volts

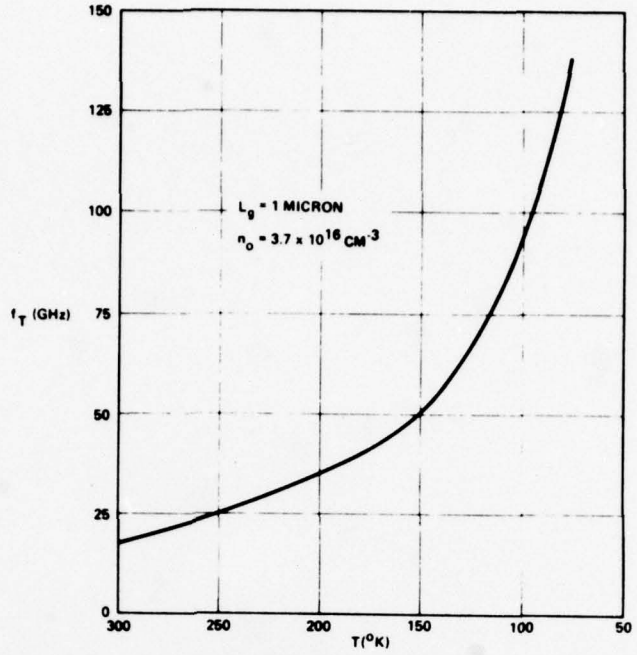

Figure 8-3. Intrinsic FET Noise Figure Versus Temperature

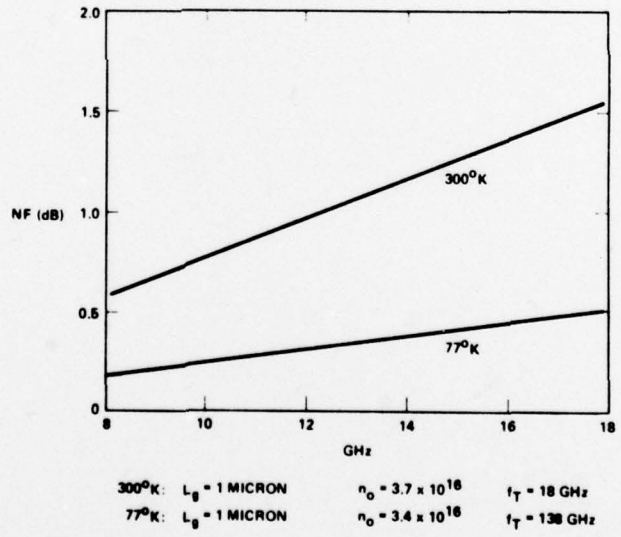

Figure 8-4. Intrinsic FET f_T Versus Temperature

9. CONCLUSIONS OF FET NOISE FIGURE OPTIMIZATION STUDY

There are three basic methods for reducing FET noise figures. The methods are:

1. Optimize lateral doping profile by ion implant (this minimizes R_g and R_s)
2. Reduce gate length via E-beam lithography
3. Cool the device from 300 to 77°K.

The noise figure reduction due to each is NF (ion implanted) = $\frac{\text{NF (uniform epi)}}{2.5}$

Figures 8-5 and 8-6 show numerical evaluation of channel carrier density factor $\overline{N(\omega)}$ and voltage across depleted region $W(\omega_d)$ for the case of a constant doping density and a 10:1 Gaussian doping density, respectively. From the comparison of these two figures, it can be observed that the pinchoff voltage for the Gaussian doping profile is larger than for the constant doping profile case.

Figures 8-7 and 8-8 are numerical evaluations of equations (2-24), (2-36), (5-1), and (5-25) respectively as outlined in Section 7. These figures show the dc characteristics of the devices having doping profile distributions as indicated for Figures 8-5 and 8-6. It can be observed from these figures that the device with the Gaussian distribution presents a family of curves more evenly spaced and consequently a greater transconductance linearity than that of the constant doping profile counterpart. Figure 8-9 represents the numerical evaluation of the transconductance given by equation (5-27) and $f_T = g_m/2\pi C_{sg}$ (the cutoff frequency) as a function of gate potential. The device with the Gaussian distribution displays a greater linearity of these two parameters as a junction of biasing point than the constant profile device.

$$\text{NF } (L_g = 0.5\ \mu\text{m}) = \frac{\text{NF } (L_g = 1\ \mu\text{m})}{2}$$

$$\text{NF } (77^{\circ}\text{K}) = \frac{\text{NF } (300^{\circ}\text{K})}{3}$$

The effect of each method of noise figure reduction is essentially independent of the others, therefore, the noise figure of an optimized FET is

$$\text{NF (opt)} = \frac{\text{NF (nonopt)}}{2.5\text{x}2\text{x}3} = \frac{\text{NF (nonopt)}}{15}$$

In the future, optimized FET front-end amplifiers for microwave applications will replace parametric amplifiers. The present performance of parametric amplifiers is compared with the projected performance of the noise figure optimized FET preamplifiers in Figure 9-1.

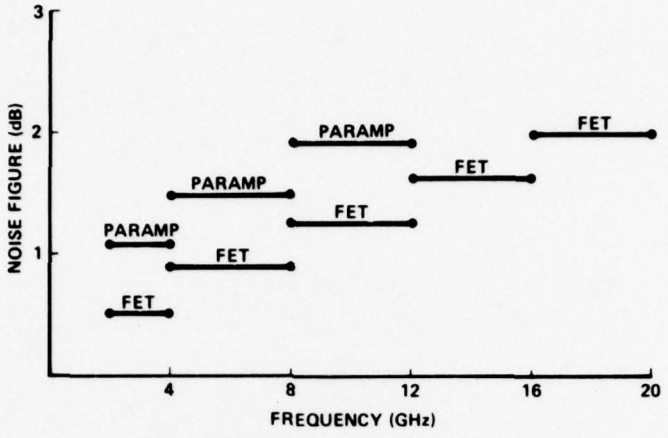

Figure 9-1. Paramp and FET Noise Figures

Basically the FET noise figure performance is unaffected by the variable vertical doping profile. This is an important point, since the vertical profile will inevitably be Gaussian as a result of ion implantation to achieve the desired lateral doping profile. While the Gaussian profile offers no particular advantage or disadvantage with respect to noise figure performance, it does have several other merits. Firstly, the transconductance, and thus the gain, associated with biasing for minimum noise figure is increased. Secondly, the linearity of the gain as a function of input drive level is improved. Thirdly, the dynamic range is increased over the uniform doping profile FET. These improvements are depicted in the plots of Figures 9-2 and 9-3.

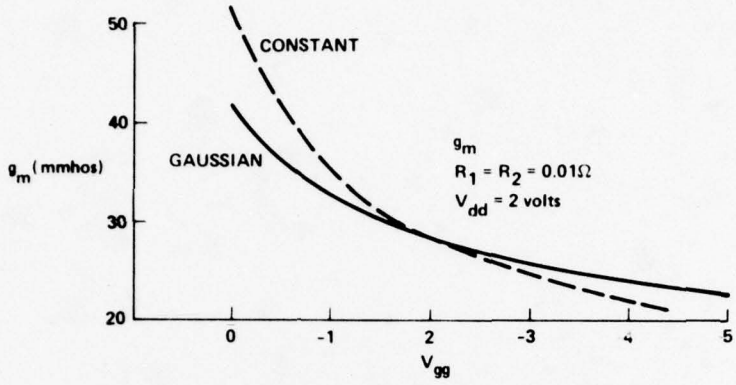

Figure 9-2. Transconductance Versus Gate Bias for Constant and Gaussian Doping Profiles

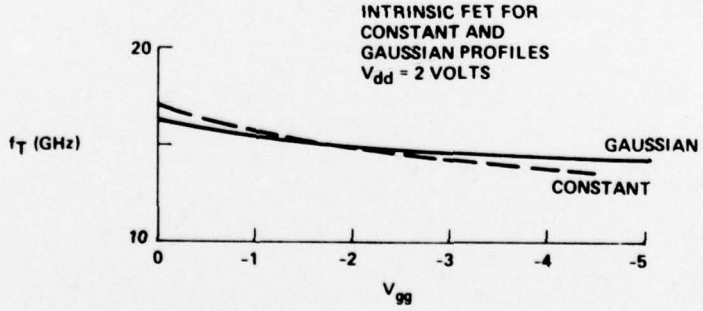

Figure 9-3. f_T Versus Gate Bias for Constant and Gaussian Doping Profiles

10. RECOMMENDATIONS

Research and development of low noise FETs for microwave applications should continue.

REFERENCES

1. S.M. Sze "Physics of Semiconductor Devices," John Wiley and Sons, P. 40, Figure 19 1969.

2. S.M. Sze "Physics of Semiconductor Devices," John Wiley and Sons, P. 347, Eq. 52b 1969.

3. Pucel, R.G. "Signal and Noise Properties of GaAs FETs," Advances in Electronics and Electron Physics, Volume 38, Academic Press PP. 220-221 1975.

4. Wasserstrom, E. and McKenna, J. BSTJ 49, PP. 853-877 1970.

5. Brehm, G.E., and Vendelin, G.D., Microwaves 13, PP. 38-44 1974.

6. Pucel, R.G., "Signal and Noise Properties of GaAs FETs," Advances in Electronics and Electron Physics, Volume 38, Academic Press PP 238-243 1975.

7. Frey, J., "Effects of Internally Scattering on Noise in GaAs and InP Field Effect Transistors," IEEE Transactions on Electron Devices, Volume ED-23 No. 12, PP. 1298-1303 December 1976.

8. Statz, H., Haus, H.A., and Pucel, R.A., "Noise Characteristics of GaAs Field Effect Transistors," IEEE Transactions on Electron Devices, Volume ED-21 PP. 557-558, 9 September 1974.

9. Smythe, W.R., "Static and Dynamic Electricity," Third edition, McGraw-Hill, PP. 100-104, New York 1968.

10. Abramowitz, M. and Stegun, I.A., Editors "Handbook of Mathematical Functions," National Bureau of Standards, AMS 55, PP. 608.

11. Grebene, A.B., and Ghandhi, S.K., "General Theory for Pinched Operation of the Junction-Gate FET." Solid State Electronics, Volume 12, Pergamnon Press 1969, PP. 573-589.

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