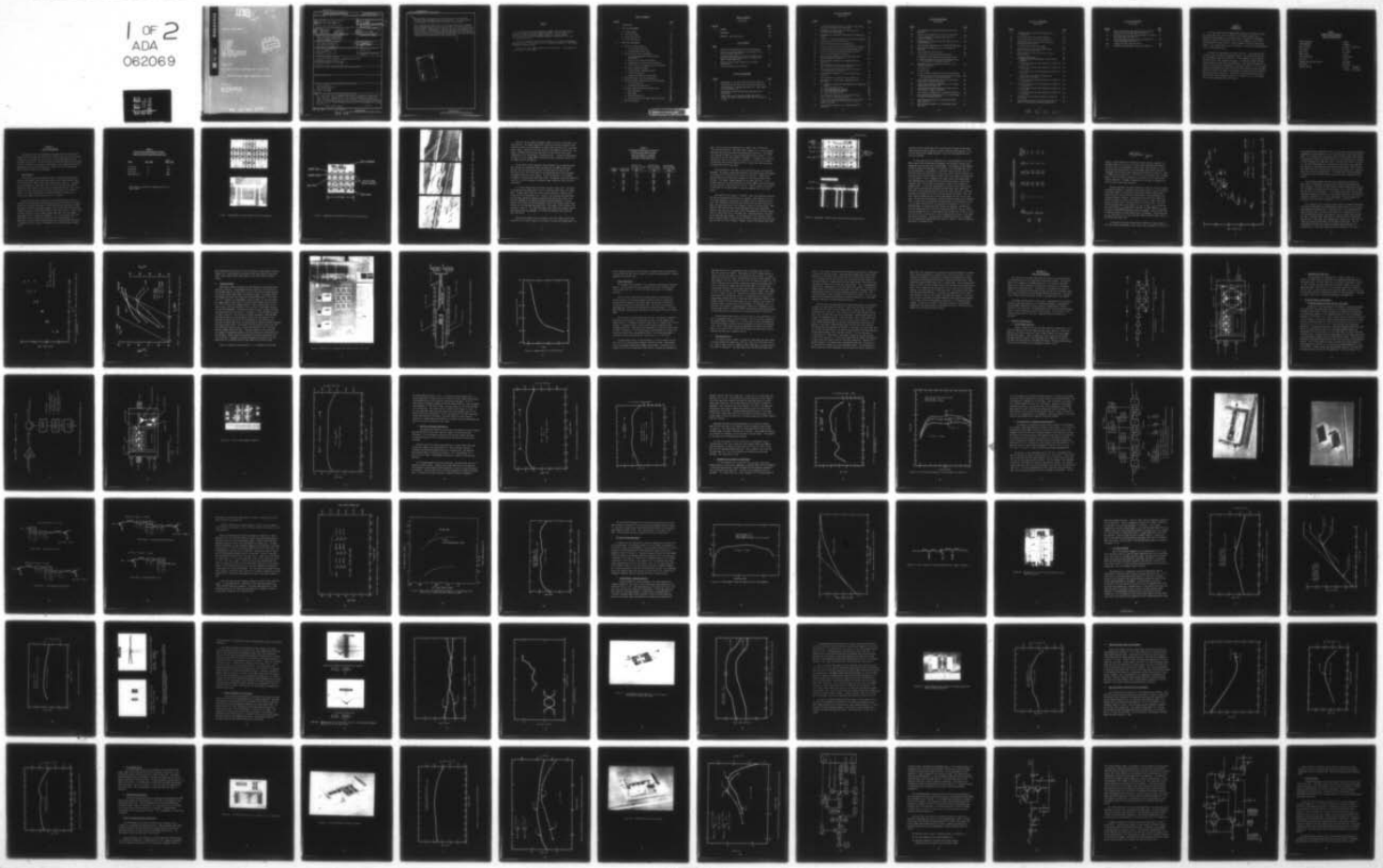
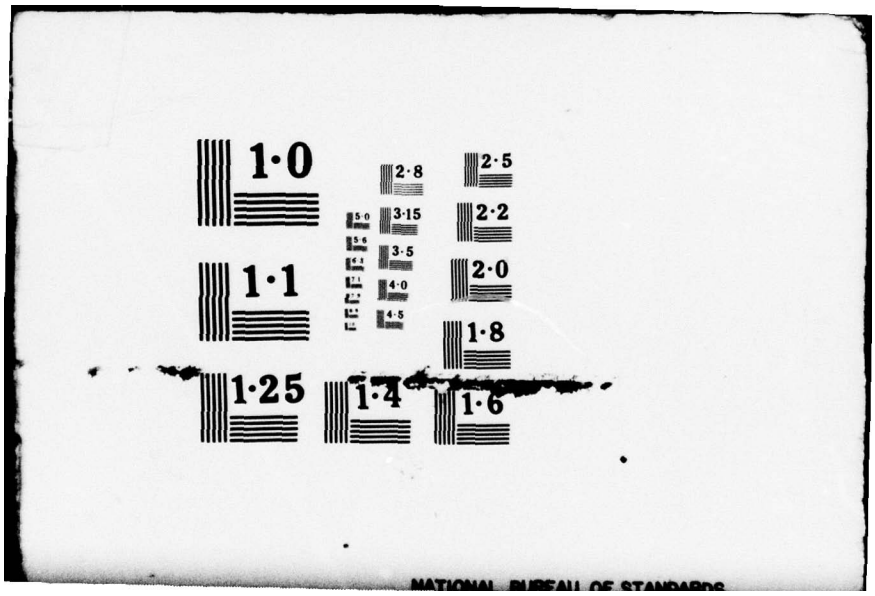
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X-BAND SOLID STATE MODULE

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This report describes an eighteen-month program to develop an X-band solid state amplifier. The amplifier is the critical component of an all solid state tranceiver module for use in active element, airborne, phased array radars. The performance goals were an output power of 4 W (min.) with 25 dB gain over the 9 to 10 GHz frequency band with an efficiency ≥20% under pulsed conditions.

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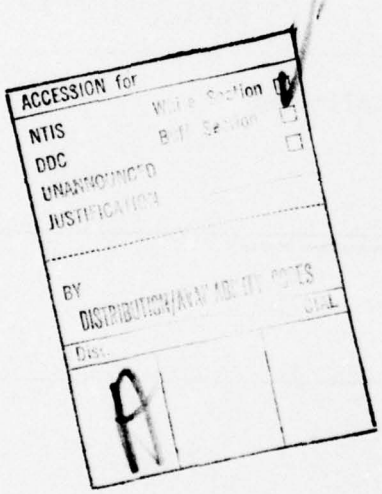
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Two approaches were pursued to meet these goals: an all GaAs FET amplifier and an FET/Read diode hybrid amplifier. At the completion of the program, two amplifiers of each type were delivered.

An all FET amplifier module with a three-stage driver and a balanced output stage delivered an output power of 4W with 24 dB gain over the 8.9 to 9.9 GHz frequency band (1 dB) with 20% efficiency including bias circuit losses. An FET/Read diode hybrid amplifier delivered 5W over with 25 dB gain at 9.5 GHz over a 600 MHz bandwidth with 19% efficiency. Extensive cw and pulsed measurements indicate that the all FET amplifier is best suited for phased array radar applications.



PREFACE

This report was prepared by Texas Instruments Incorporated, Dallas, Texas, under Navy Contract No. N00173-76-C-0384. The work under this contract was administered and funded by Naval Air Systems Command. Mr. Eliot Cohen of the Naval Research Laboratory, Washington, D. C., was the Scientific Officer.

At Texas Instruments the work was performed in the Advanced Components Laboratory under the direction of Dr. W. R. Wisseman, Manager of the Advanced Microwave Components branch.

This is the Final Technical Report for the contract. It was submitted by the authors in June 1978.

TABLE OF CONTENTS

SECTION		PAGE
I	INTRODUCTION	1
II	GaAs FET DEVELOPMENT	3
	A. Device Design	3
	B. Epitaxial Growth	19
	C. Device Fabrication	23
	D. Device Reliability	24
III	AMPLIFIER DEVELOPMENT	27
	A. Amplifier Configurations	27
	1. All FET Power Amplifier	27
	2. FET/Read Hybrid Amplifier	30
	B. FET Driver Amplifier Development	30
	1. Prototype Breadboard Driver Amplifier Development	30
	2. Amplifier Efficiency Optimization	35
	3. Breadboard Driver Amplifier Performance	38
	4. Driver Amplifier Integration and Performance	41
	C. FET Output Stage Development	51
	1. Lumped-Element Impedance Matching	51
	2. 3 dB Hybrid Coupler	56
	3. Balanced FET Amplifier Performance	61
	D. Read Diode Power Amplifier Development	70
	E. Amplifier Module Integration and cw Performance	70
	1. All FET Amplifiers	74
	2. FET/Read Hybrid Amplifier	74
	F. Pulsed rf Characterization of Amplifiers	74
	1. Amplitude Droop	86
	2. Phase Ramp	87
	3. AM-to-PM Conversion	99
	4. Phase Sensitivity to Power Supply Variations	99
	G. Noise Performance	103

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TABLE OF CONTENTS

(continued)

SECTION		PAGE
IV	SUMMARY	107
	REFERENCES	108
	APPENDIX: Device Deliveries	109

LIST OF TABLES

TABLE		PAGE
1	X-Band Solid-State Module Amplifier Requirements	2
2	Power and Gain Requirements for Each Stage of the Driver and Power Amplifiers	4
3	Microwave Performance as a Function of Gate Finger Width for GaAs Power FETs Having 1 μm Gates and 1200 μm Total Gate Width	9
4	Effect of Source Lead Inductance on Microwave Performance	13
5	NRL Four-Stage Amplifier Modules	98

LIST OF ILLUSTRATIONS

FIGURE		PAGE
1	Photographs of Low Noise GaAs FET During Processing	5
2	Photograph of GaAs Power FET Slice During Fabrication	6
3	SEM Photographs of Bonded GaAs Power FET. Gate Length is Approximately 1 μm	7
4	Photographs of 6400 μm Gate Width Devices During Fabrication	11
5	Output Power with 4 dB Gain and 8V Drain Bias at 10 GHz from 1200 μm Gate Width GaAs FETs as a Function of I_{dss}	15

LIST OF ILLUSTRATIONS

(Continued)

FIGURE		PAGE
6	Cw and Pulsed Output Power of a 1200 m Gate Width GaAs FET as a Function of Drain Bias	17
7	Dependence of Output Power on Input Power for Different Gate Length FETs	18
8	Photograph of an Automatic GaAs Epitaxial Deposition System	20
9	Schematic of Epitaxial Reactor with Two $AsC\ell_3$ Bubblers	21
10	Doping Profile of an FET Structure	22
11	An All-FET Power Amplifier Configuration	28
12	Circuit Layout of the All-FET Power Amplifier Module	29
13	Schematic Diagram of the Hybrid FET/Read Amplifier	31
14	Circuit Layout of the Hybrid FET/Read Amplifier	32
15	A 0.5 W, Three-Stage FET Amplifier	33
16	Gain-Frequency Response of the Three-Stage FET Amplifier Shown in Figure 12	34
17	Gain-Frequency Response of a Breadboard Driver Amplifier	36
18	Gain-Frequency and Efficiency Characteristics of the First Stage of the Driver Amplifier	37
19	Gain-Frequency and Efficiency Characteristics of a Two-Stage GaAs FET Amplifier	39
20	Gain-Frequency Response of a Three-Stage Driver Amplifier	40
21	Block Diagram of a Power FET Driver Amplifier	42
22	Photograph of a Three-Stage, Breadboard Driver Amplifier	43
23	a) A Totally Integrated, Three-Stage Driver Amplifier Module	44
	b) Input Matching Circuit	45
	c) Interstage Matching Networks	45
	d) Interstage Matching Networks	46
	e) Output Matching Circuit	46
24	Gain-Frequency Response of a Three-Stage Driver Amplifier with Interstage Matching	48
25	Output Power and Power-Added Efficiency of a Three-Stage Driver Amplifier as a Function of Input Power at 9.5 GHz	49
26	Gain-Frequency Response of a Three-Stage Driver Amplifier	50

LIST OF ILLUSTRATIONS

(Continued)

FIGURE		PAGE
27	A Three-Stage 1 W GaAs FET Amplifier with 2 GHz Bandwidth	52
28	Compression Characteristics of the 1 W Amplifier	53
29	Circuit Topology for Matching GaAs FET with Lumped LC Elements	54
30	Photograph of a Four-Cell GaAs FET Amplifier with Internal Matching	55
31	Gain-Frequency Response of a 3 W GaAs FET Amplifier	57
32	Compression Characteristics of a 3 W GaAs FET Amplifier	58
33	An 8-10 GHz GaAs FET Amplifier	59
34	3 dB Coupler, Design and Coupling Results	60
	a) Comparison of Tandem and Interdigital Design	
	b) Measured Coupled and Direct Port Response from 7 to 12 GHz for Interdigital Coupler	
35	Measured Directivity and Return Loss for 3 dB Interdigital Coupler	62
	a) Directivity	
	b) Return Loss	
36	a) Lang Coupler: Coupled and Direct Port Response	63
	b) Total Insertion Loss (Including Connector Losses) of Lange Coupler on Quartz Substrate	64
37	Single-Stage Balanced Amplifier with 3 dB Coupler Fabricated on Alumina Substrates	65
38	Output Power-Frequency Characteristic of a Single-Stage Balanced FET Amplifier	66
39	Single-Stage Balanced FET Amplifier Module Using 3 dB Coupler on Quartz Substrate	68
40	Gain-Frequency Response of a 4 W GaAs FET Amplifier	69
41	Gain Compression Characteristic of a Single-Stage, Two-Mesa Read Diode Amplifier	71
42	Gain-Frequency Response of a Single-Stage Read Diode Amplifier	72
43	Gain-Frequency Response of a Three-Stage Driver Amplifier	73

LIST OF ILLUSTRATIONS

(Continued)

FIGURE		PAGE
44	Individual GaAs FET Amplifier Modules Prior to Integration	75
45	A Four-Stage GaAs FET Amplifier Module	76
46	Performance of a 4 Watt GaAs FET Amplifier	77
47	CW Performance of the Two All-FET Amplifier Modules Delivered to NRL	78
48	A FET/Read Hybrid Amplifier Module	79
49	CW Performance of the Two FET/Read Hybrid Amplifiers Delivered to NRL	80
50	Block Diagram of Pulse Test Set-up for GaAs FET Amplifiers	81
51	a) Gate Pulsing Circuit	83
	b) Schematic Diagram of Constant Current Pulsed Modulator	85
52	a) Pulsed Amplitude and Phase Response of Module #9 at 9.145 GHz	88
	b) Pulsed Amplitude and Phase Response of Module #9 at 9.5 GHz	89
	c) Pulsed Amplitude and Phase Response of Module #9 at 10 GHz	90
53	a) Pulsed Amplitude and Phase Response of Module #12 at 9.5 GHz	91
	b) Pulsed Amplitude and Phase Response of Module #13 at 9.145 GHz	92
54	a) Pulsed Amplitude and Phase Response of Module #5 at 9.145 GHz	93
	b) Pulsed Amplitude and Phase Response of Module #5 at 9.5 GHz	94
	c) Pulsed Amplitude and Phase Response of Module #5 at 9.8 GHz	95
55	Pulsed Amplitude and Phase Response of Module #4 at 9.5 GHz	96
56	Pulsed Phase Response of a 300 μm Gate Width FET Amplifier Under Various Operating Conditions	97

78 11 22 007

LIST OF ILLUSTRATIONS

(Continued)

FIGURE		PAGE
57	AM to PM Conversion Characteristics of a Single-Stage and a Three-Stage GaAs FET Amplifier	100
58	Bias Sensitivity of the Insertion Phase of a 600 μm Gate Width GaAs FET Amplifier	101
59	Insertion Phase as Function of Bias Voltage for a Three-Stage GaAs FET Amplifier	102
60	AM Additive Noise Measuring Setup	104
61	AM Additive Noise Results for Driver Amplifier	106

SECTION I
INTRODUCTION

This report describes an eighteen-month contract to develop an X-band solid state amplifier, the first phase of a four-phase program that is expected to be completed in a five-year period. The amplifier developed during this phase of the program is the critical component of an all solid state transceiver module for use in active element, airborne, phased array radars. The ultimate goal of the full program is a test bed systems demonstration of a 100-element array.

The amplifier requirements are given in Table I. Two approaches were pursued to meet the amplifier performance goals: an all GaAs FET amplifier and an FET/Read diode hybrid amplifier. At the completion of the program, two amplifiers of each type were delivered. In addition, 50 GaAs FETs and 50 Read diodes were delivered (see Appendix A). The GaAs FET fabrication in support of the amplifier development is described in Section II of this report. The device performance and some reliability considerations are also reported. Section III details the amplifier development, including the driver amplifier and the output power amplifiers. Results of pulse characterization of the amplifiers are also included in Section III. Section IV is a brief summary of the results obtained under the contract.

Table 1

X-Band Solid-State Module

Amplifier Requirements

Center Frequency	9.5 GHz
1 dB Bandwidth	± 500 MHz
Peak rf Output	5 W Goal, 4 W Minimum
Pulse Width	2 - 20 μs
Duty Cycle	Up to 50%
Overall Gain	≥ 25 dB
Final Stage Gain	5 dB minimum
Risetime	< 50 ns
Harmonic and Spurious Output	50 dB Down
Efficiency	Maximized
Spectral Purity	at 10 Hz -48 dB/Hz
	> 1000 Hz -105 dB/Hz

SECTION II
GaAs FET DEVELOPMENT

The power and gain requirements for the power amplifier and for each stage of the driver amplifier are listed in Table 2, assuming no circuit loss. In practice, the devices must deliver 0.5 to 1 dB higher output power to overcome circuit losses. The device designs to meet these goals are described in the first part of this section. The epitaxial layer growth and the device fabrication process are then discussed. Finally, the results obtained to date on device reliability are presented.

A. Device Design

At the time the present contract started, the devices available for amplifier development were a 300 μm gate width, small signal device (Figure 1) and a four-cell, 4800 μm gate width, power device (Figure 2). To remove the heat generated in power devices of this type, the chips are soldered directly to small copper carriers that are clamped between two larger copper blocks containing input and output microstrip matching circuits, shown in Figure 3. In this configuration the measured thermal resistance for a 100 μm thick, 4800 μm gate width device is 15 to 20°C/W.

GaAs FET output power increases with increasing gate width, and it is necessary to make the gate width large enough so that the devices can readily achieve the required output power without employing such high drain voltages that device reliability becomes a problem. With present devices that have a thermal resistance of about 20°C/W (4800 μm gate width) and no n^+ layers under the ohmic contracts, drain voltages greater than about 10 V are probably unacceptable from a reliability standpoint. It is also necessary that the gate width not be so large that the device efficiency decreases. Our experience indicates that the maximum efficiency is obtained when the device is operated so that its gain is compressed 4 to 5 dB from the small signal gain.

Table 2

Power and Gain Requirements for Each Stage of the Driver and Power Amplifiers

Stage	Gain (dB)	Output Power (mW)
1st Driver	9	125
2nd Driver	6	500
3rd Driver	5	1585
Power Amplifier	5	2500*

* The outputs of two FETs are combined to give 5 W output power.

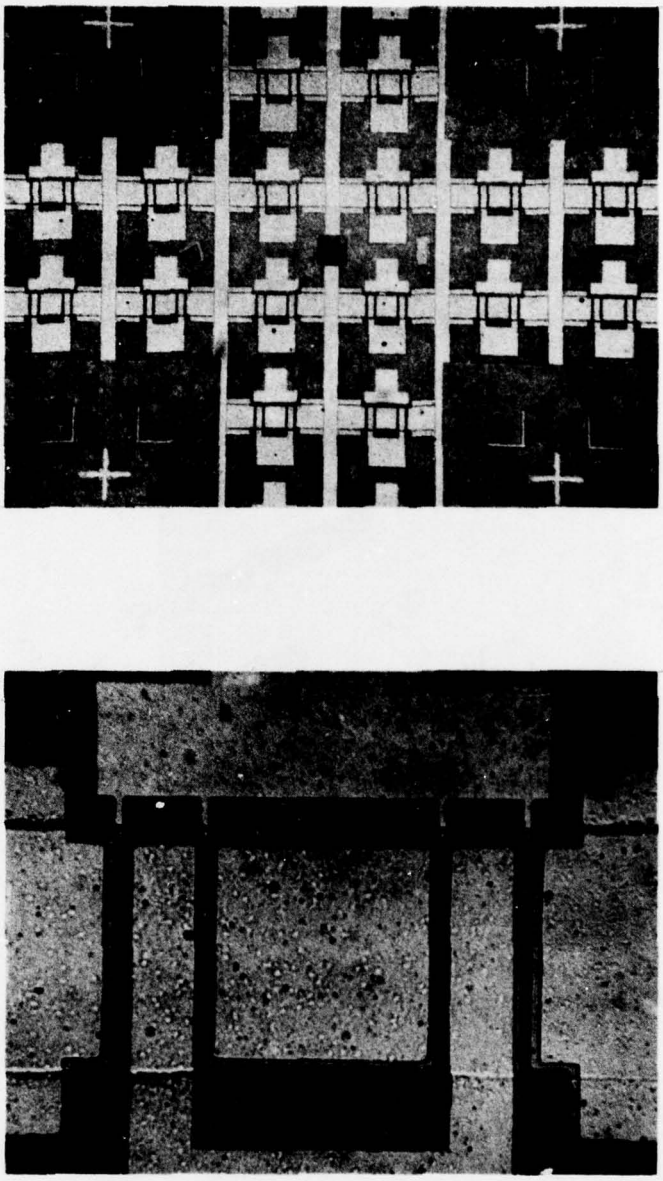


Figure 1. Photographs of Low Noise GaAs FET During Processing

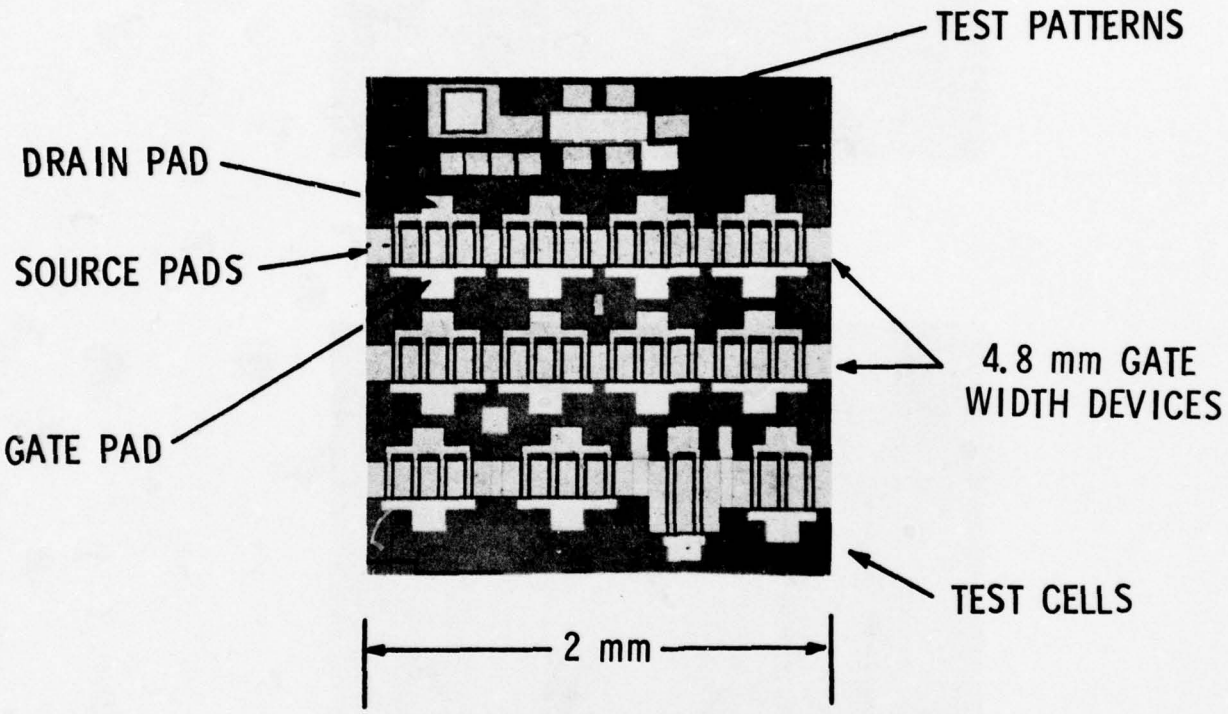


Figure 2. Photograph of GaAs Power FET Slice During Fabrication

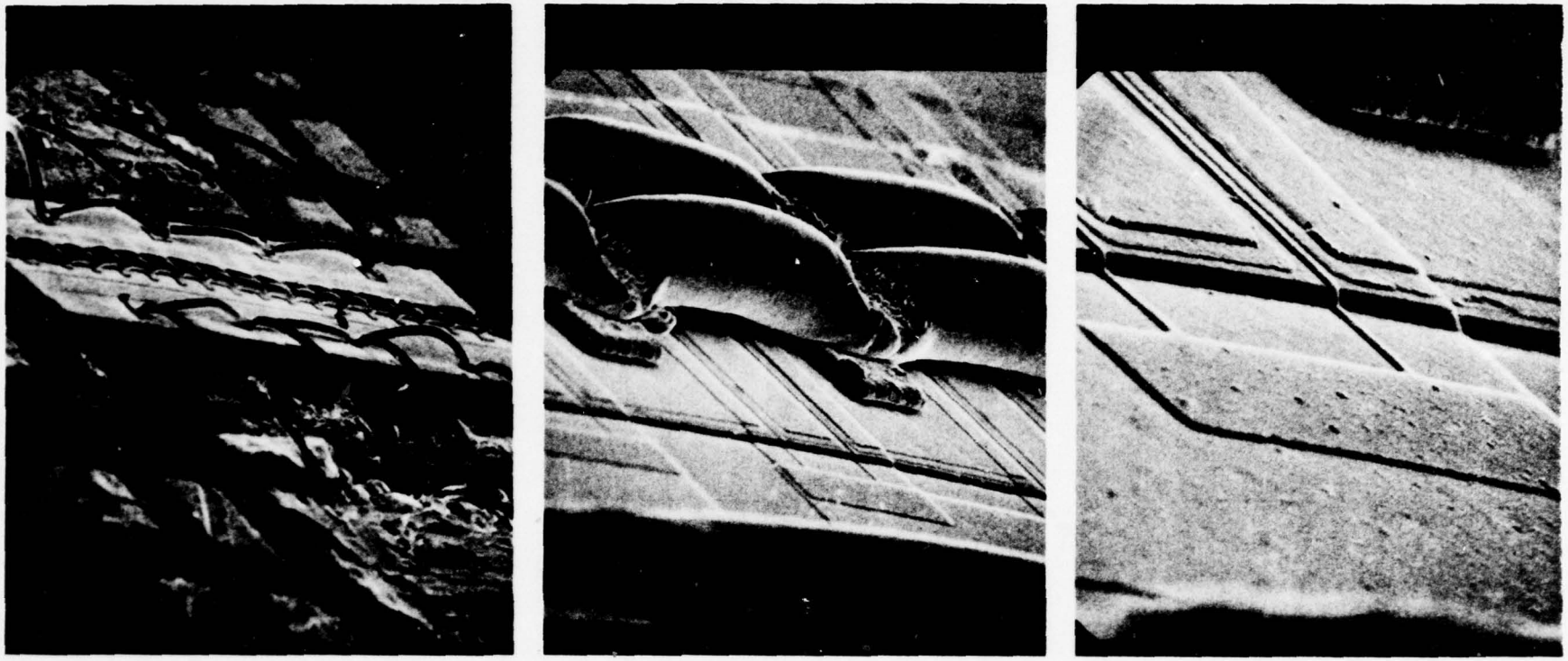


Figure 3. SEM Photographs of Bonded GaAs Power FET. Gate length is approximately 1 μm.

The first driver stage requirements (Table 2) are met by the 300 μm gate width devices. The 1200 μm gate width, single-cell devices have gate widths that are slightly too large (900 μm to 1000 μm would be better) for the second driver stage. Therefore, three 300 μm devices are bonded in parallel for that stage. An added bonus of using three chips is that the low source lead inductance of this configuration increases the gain. To meet the requirements of the third driver stage, 2400 μm total gate width is employed (two cells of the 4800 μm gate width device).

At the outset of this contract, FET performance results obtained under AFAL Contract No. F33615-76-C-1309 indicated that the 4800 μm gate width devices then available would not meet the power amplifier goal at safe drain bias levels (8 to 10 V) when it was considered that 3 W would probably be needed to overcome circuit losses. An obvious approach is to increase the power by increasing the total gate width. The easiest scheme for accomplishing this is just to increase all the gate finger widths and retain the four-cell design.

It is known theoretically that when the gate finger width is too great, the attenuation and phase shift of the rf signal down the finger will reduce gain. A rough idea of when this occurs can be obtained by treating a gate finger as an R-C transmission line. However, the resistance and capacitance are not known accurately enough to determine when device gain begins to be seriously degraded so the effect was determined experimentally. This was done by using a mask-set that had adjacent devices with different gate finger widths, but with the same total gate width. The results from a typical slice are shown in Table 3. At 10 GHz the finger width could be as large as 200 μm before performance was degraded. At 12 GHz this maximum finger width was less than 150 μm.

The data from Table 3 led us to choose a four-cell, 6400 μm total gate width device with 200 μm fingers as the vehicle for meeting the power amplifier

Table 3

Microwave Performance as a Function of Gate Finger Width for GaAs Power FETs Having 1 μm Gates and 1200 μm Total Gate Width

Frequency (GHz)	Gate Finger Width (μm)	Maximum Gain With P_{in} = 15 dBm, 5 V Drain Bias (dB)	Maximum P_{out} With 4 dB Gain, 8 V Drain Bias (mW)	Maximum P_{out} With 6 dB Gain, 8 V Drain Bias (mW)
8	150	8.2	890	810
	200	8.2	910	830
	300	7.4	910	660
10	150	7.0	850	520
	200	7.0	790	480
	300	5.9	600	300
12	150	6.2	660	-
	200	5.7	500	-
	300	5.0	340	-

goal. Figure 4 shows two photographs of a 6400 μm gate width device slice during fabrication. The gate length is about 1 μm. Other parameters have been kept about the same as those determined previously: the source-drain spacing is about 5 μm, the epitaxial doping level is about 1×10^{17} carriers/cm^3, and the basic design is unchanged. Included on the slice are several test patterns for measuring capacitance as a function of voltage (to determine the epitaxial doping profile), contact and sheet resistance, and gate metallization resistance.

The performance of the 6400 μm gate width devices was not as good as expected. The highest output power obtained from a 6400 μm gate width device at 10 GHz with 8 V drain bias was 3.23 W with 4 dB gain. Higher powers could be obtained at higher drain voltages, but the device would be less reliable. This power, though adequate for the power amplifier, is only slightly more than has been obtained from the best 4800 μm gate width devices. The main problem is that the gain is too low. Ideally, about 5 to 6 dB gain is desirable for the power amplifier stage to compensate for the circuit losses.

The reason for the low gain is twofold: lower than expected single-cell gain and gain degradation when cells are combined. Gate lengths of 1.1 to 1.2 μm were employed on many slices to increase yield at the gate definition step. Many measurements had shown that devices with such gate lengths had about the same output power with 4 dB gain as those with shorter gates. More recently, when amplifiers were being developed, device gain became more important than maximum output power, and it became apparent that gate lengths of 0.7 to 0.8 μm had 0.5 to 1 dB higher gain. Another problem is the width of the individual gate fingers. At the beginning of this contract, experiments indicated (Table 3) that devices with 200 μm fingers would have the same gain as those with 150 μm fingers. However, results from devices fabricated

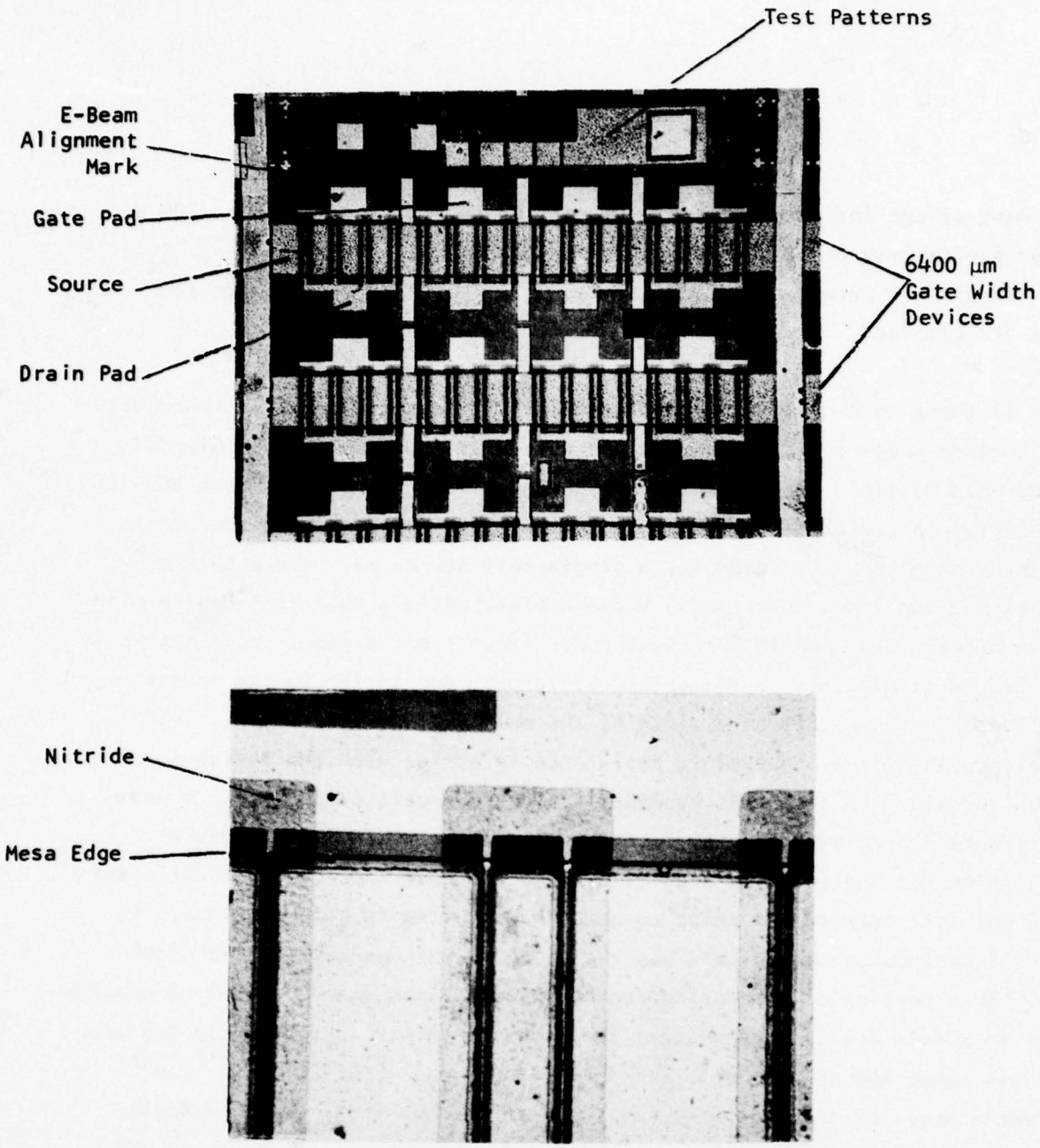


Figure 4. Photographs of 6400 μm Gate Width Devices During Fabrication

from many slices indicate that this is not the case; the gain of the 200 μm finger devices may be as much as 0.5 dB less than the 150 μm devices. Even with the shorter gate lengths the gain is still not high enough when four cells are combined.

If there were no loss in combining cells, the performance of four-cell, 6400 μm gate width devices would be adequate, but the gain is severely degraded when multiple cells are interconnected. This happens for both 4800 μm and 6400 μm gate width devices and is typically 1.5 to 2 dB when four cells are interconnected. For example, a single-cell device may have a gain of 9 dB with 9 dBm input power and 5 V drain bias, while a four-cell device with the same drain bias and 15 dBm input power (four times higher) would have only 7 to 7.5 dB gain. This is thought to be largely due to the larger source lead inductance per unit gate width of the multicell device. Source lead inductance acts like a parasitic resistance in series with the device in degrading gain. To test this hypothesis, four one-cell chips (1200 μm gate width) were broken away from different four-cell chips from a particular fabrication run and soldered side-by-side on the usual heat sink. Sufficient space was left between the chips to bond source wires to ground. Thus, the source lead inductance per cell was the same whether one cell or four were used. This particular processing run had near-optimum values of all parameters known to affect device performance; the gate length was approximately 0.8 μm, I_{dss} was about 400 mA per cell, and doping level was about 1.1×10^{17} cm^{-3}. The performance of these devices was the best yet obtained. With 8V drain bias the output power was 3.4 W with 6 dB gain and 40% efficiency at 10 GHz. The gain degradation due to interconnection was reduced from 1.7 dB for a four-cell chip of this slice to only 0.7 dB, with about half the loss in the input and half on the output. The relative cell-combining efficiency is compared with a conventionally mounted four-cell device in Table 4. The cell combining efficiency is defined here as

Table 4

Effect of Source Lead Inductance on Microwave Performance

	Gain (dB)	# Cells	P_{out} (W)	η_{PA} (%)	V_{DS} (V)	Combining Efficiency (%)
One Chip	4	1	0.91	25.6	8	79.1
		4	2.88	24.1	8	
	6	1	0.83	31.8	8	64.5
		4	2.14	19.9	8	
Four Chips	4	1	0.96	39.3	8	96.9
		4	3.72	36.8	8	
	6	1	0.87	45.3	8	97.4
		4	3.39	40.0	8	

$$\left.\frac{P_{out}(4 \text{ cells})}{4 \times P_{out}(1 \text{ cell})}\right|_{\text{constant gain}} .$$

Clearly, a better approach to obtaining the power and gain necessary for the power amplifier is to use a low source lead inductance configuration. This will result in improvements in gain, power, and efficiency. A new device has been designed and is being developed under another contract to incorporate the low source lead inductance configuration on one chip. There is a 4800 μm total gate width in four cells on a plated heat sink. An added bonus is that this permits the GaAs to be thinned to 50 μm, lowering the thermal resistance. The GaAs is etched down to the heat sink between the cells to permit source lead grounding.

Several experiments have been conducted to optimize single-cell device microwave performance. To determine the optimum value of I_{dss} for achieving high output powers, the epitaxial thickness was purposely varied across several slices by varying the gate recess depth or taking advantage of an existing thickness variation. The maximum output power with 4 dB gain at 10 GHz is plotted in Figure 5 as a function of I_{dss} for 1200 μm gate width devices from two slices. The drain bias was 8 V in all cases. For both slices the output power rose rapidly with I_{dss} at small I_{dss} and then rose less rapidly when I_{dss} reached 350 to 375 mA. At higher values of I_{dss} the efficiency (numbers beside each data point) decreased. This was partly due to heating and partly to gate Schottky barrier breakdown. The optimum value of I_{dss} from Figure 5 is in the range 400 to 480 mA (1200 μm gate width) or 330 to 400 mA/mm gate width.

It should be noted that although device heating is a major factor in limiting microwave performance at the highest drain voltages (12 to 15 V), at

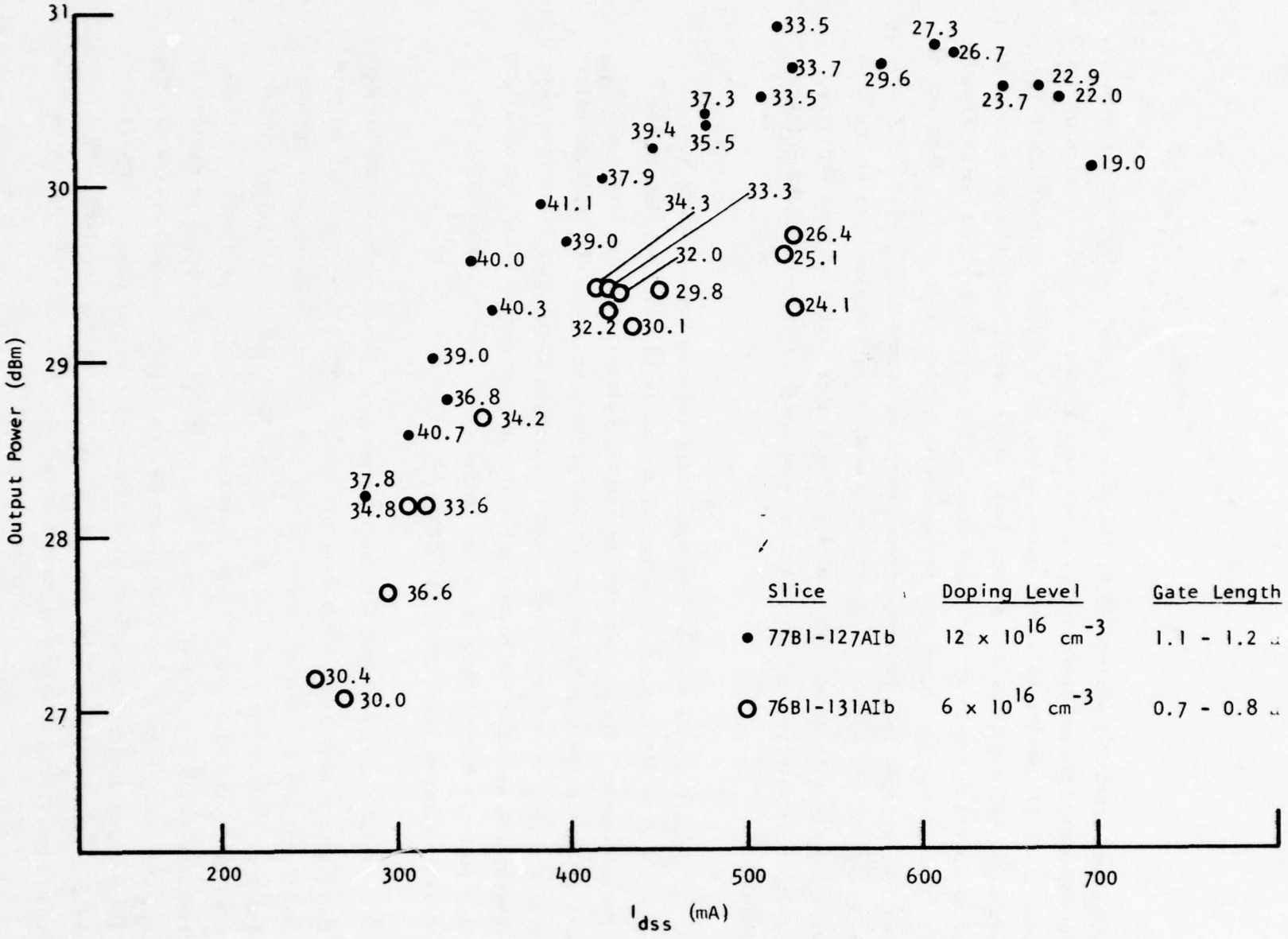


Figure 5. Output Power with 4 dB Gain and 8 V Drain Bias at 10 GHz from 1200 μm Gate Width GaAs FETs as a Function of I_{dss}

the usual operating voltage (8 V) there is only a small effect on performance. Consequently, pulsed operation will not significantly increase device output power. To illustrate this, the output power of a 1200 μm gate width device was measured in both cw and pulsed (very short pulse) operation as a function of drain voltage with 23 dBm input power. The results are plotted in Figure 6. This device was chosen for its excessively high value of I_{dss} (650 mA; see Figure 5) so that heating effects would be accentuated. With 8 V drain bias heating was not very significant even with this device, and it would be even less so with an optimum device. If a plated heat sink were employed, it would be totally negligible and no more power could be expected pulsed than cw.

The difference between the two slices represented in Figure 5 is mainly due to differences in epitaxial doping level, but gate length has some influence. The values of gate length, epitaxial doping level, and I_{dss} all influence the optimum values of each other, so it is difficult to determine the best set of parameters. It is becoming clear that if shorter gate lengths are employed for higher gain, the optimum doping level for obtaining high power is higher than it is for longer gates. With 0.8 μm gates the epitaxial doping level should probably be 1 to 1.5 x 10^{17} cm^{-3}.

As an example of the influence of gate length on microwave performance, the electron beam machine was reprogrammed to define 0.8 μm and 1.6 μm gate length devices on adjacent chips in the same field. The microwave performance of several pairs of devices with identical I-V characteristics, but with different gate lengths, was compared. The 0.8 μm gate length devices had about 2 dB higher small signal gain at 8 GHz than the 1.6 μm devices, but when the rf input power was increased until the gain was only 4 dB, the longer gate devices had 0.3 dB to 0.4 dB higher output power. This is illustrated in Figure 7 for one pair of devices having identical I-V characteristics. The higher output power with 4 dB gain of the 1.6 μm

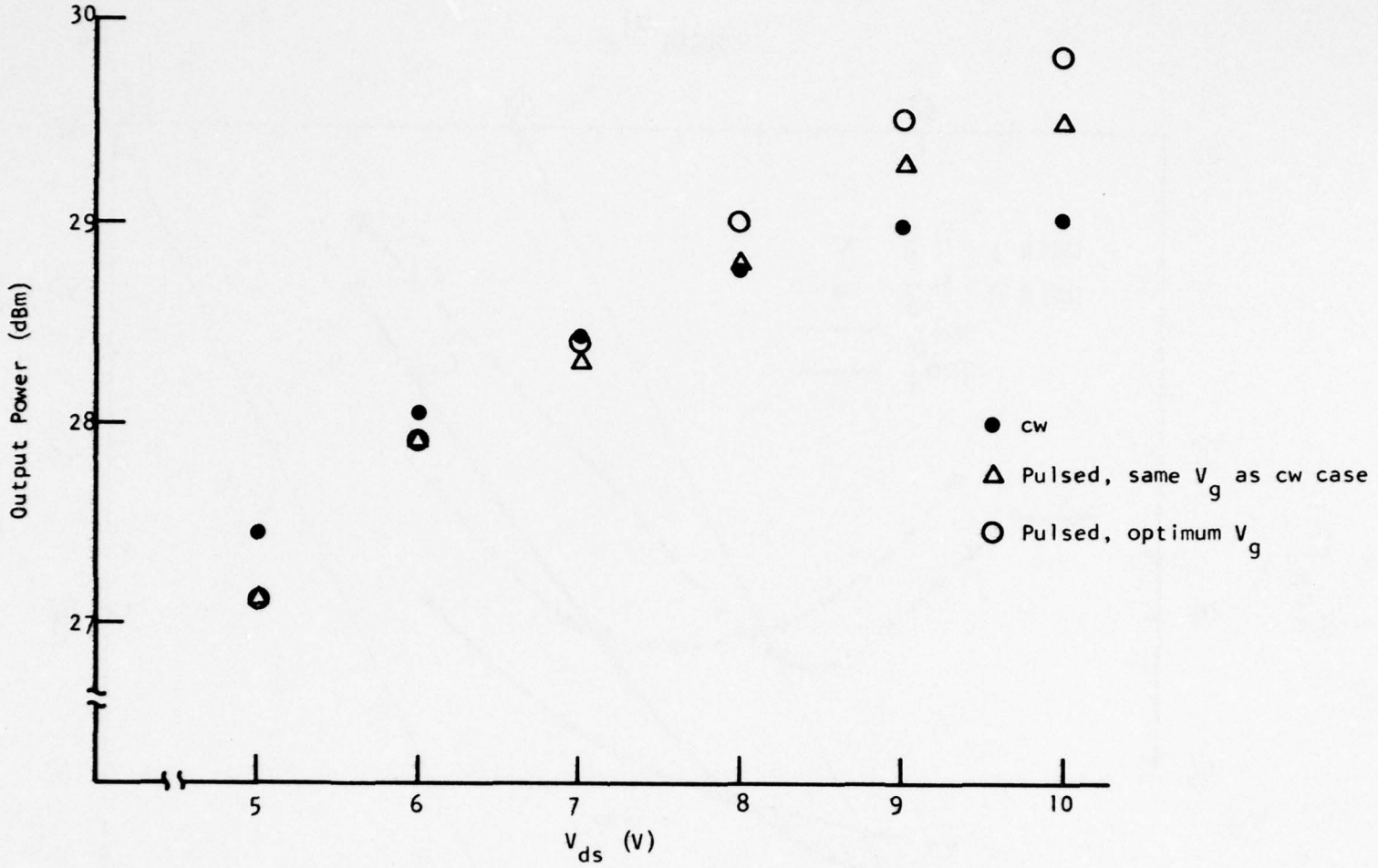


Figure 6. Cw and Pulsed Output Power of a 1200 μm Gate Width GaAs FET as a Function of Drain Bias

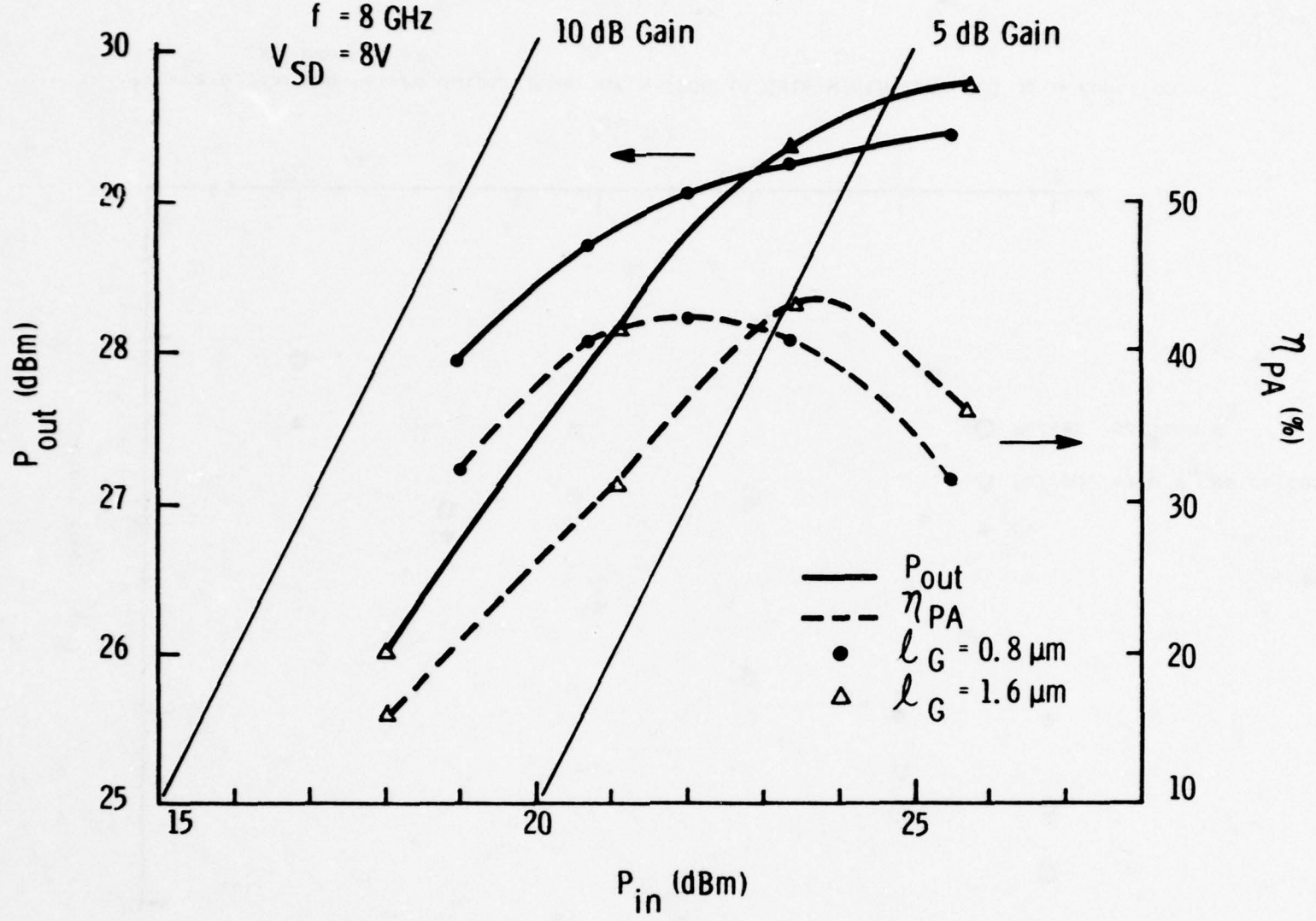


Figure 7. Dependence of Output Power on Input Power For Different Gate Length FETs

gate length device was due to a 10 to 15% increase in power-added efficiency. However, for a typical amplifier application extra gain would be much more useful than slightly higher output power, so the 0.8 μm device would be chosen.

B. Epitaxial Growth

GaAs FETs at Texas Instruments are fabricated using vapor phase grown epitaxial structures. Semiautomated reactor systems are used routinely to provide GaAs material for GaAs FETs, as well as for other microwave devices, such as Gunn diodes, Read diodes, and varactor diodes. The systems employ the Ga-$AsCl_3$-H_2 system, which has been discussed extensively in the literature.[1,2,3] Figure 8 is a photograph of such a system. All FET structures at present contain a high resistivity buffer layer between the active layer ($N \sim 10^{17}$ cm^{-3}) and the Cr-doped substrate. The low doping level of the buffer layers, which are typically 3 to 5 μm thick, is achieved by growing in a HCl-rich atmosphere. An additional amount of $AsCl_3$ is added to the gas flow downstream from the Ga source. A schematic of this two-bubbler system is shown in Figure 9. The principle of such a two-bubbler system has been described previously in the literature,[4] along with the reasons for the observed low doping levels.[5,6] All FET material is grown thicker than required for device fabrication and then thinned by successive anodic oxidation and oxide etching cycles. This process is self-limiting in such a way that the oxide growth stops as soon as the surface depletion layer, with bias applied, reaches the buffer layer. Then the structure is not biased any more beyond the avalanche condition, and holes required for oxide growth are not available. Before submitting the material for device fabrication, the layer thickness is measured on cleaved and etched cross sections, and the doping profile is measured using C-V data taken with a mercury probe.

Figure 10 presents a typical profile. It is important to note that

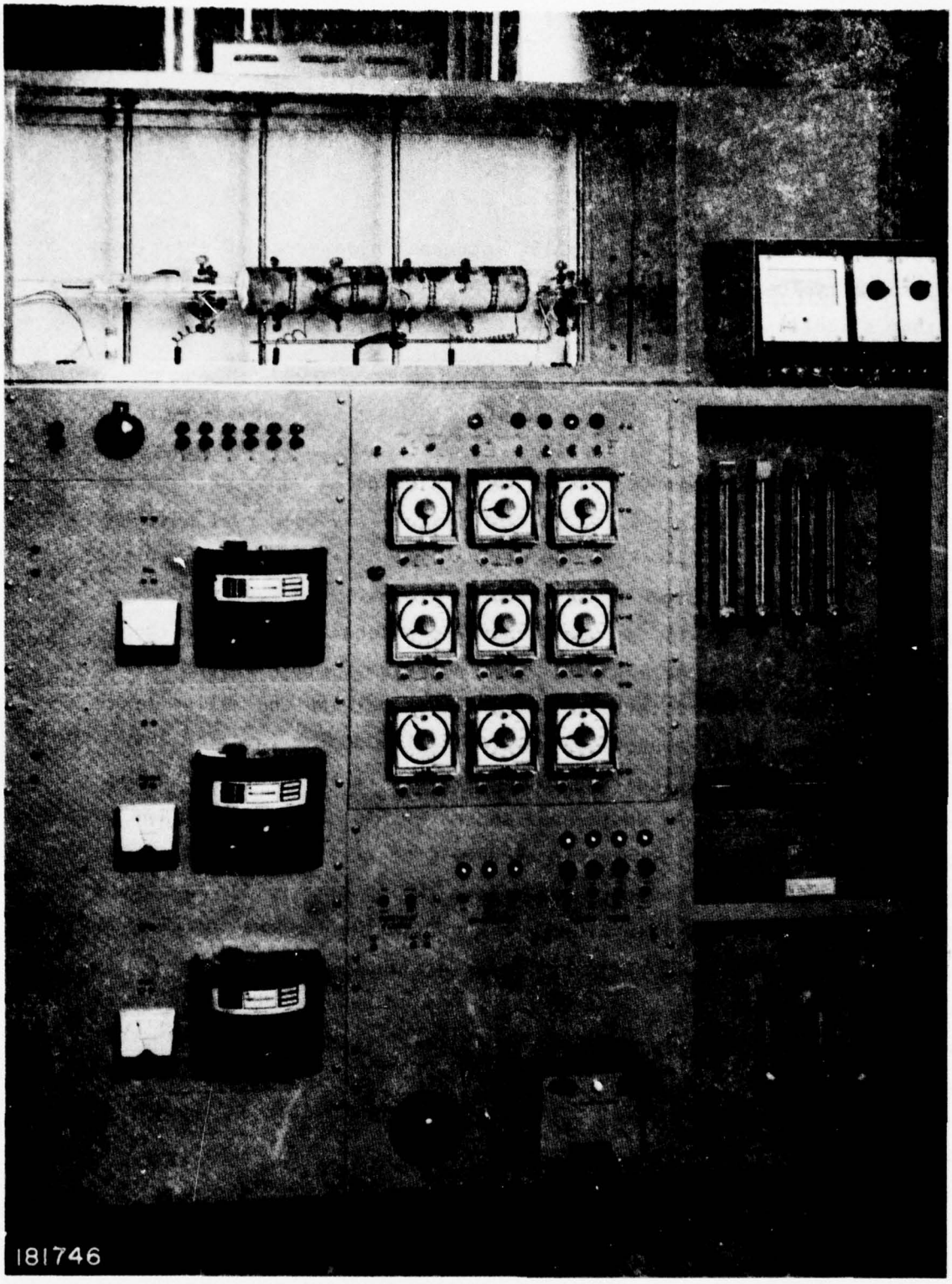


Figure 8. Photograph of an Automatic GaAs Epitaxial Deposition System

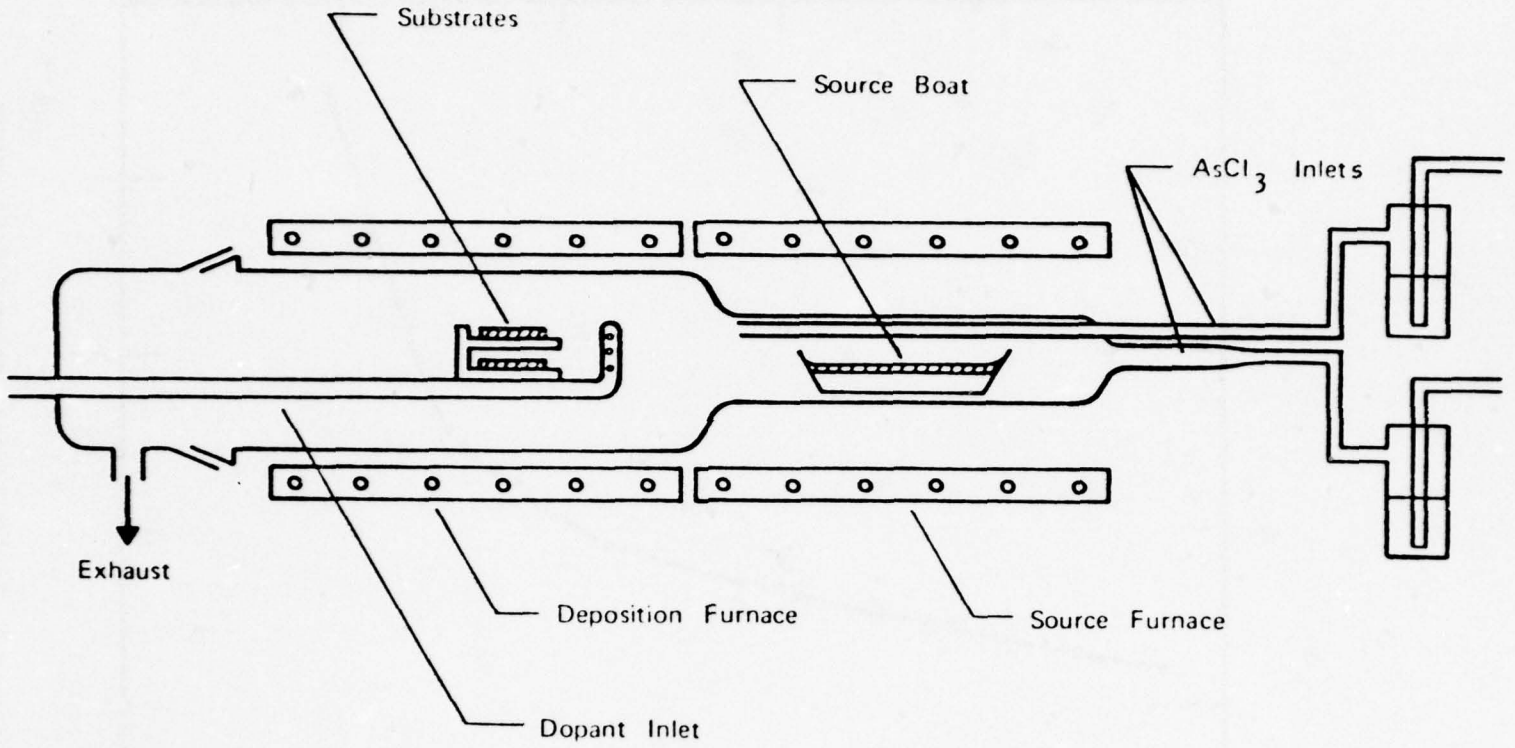


Figure 9. Schematic of Epitaxial Reactor with Two $AsCl_3$ Bubblers

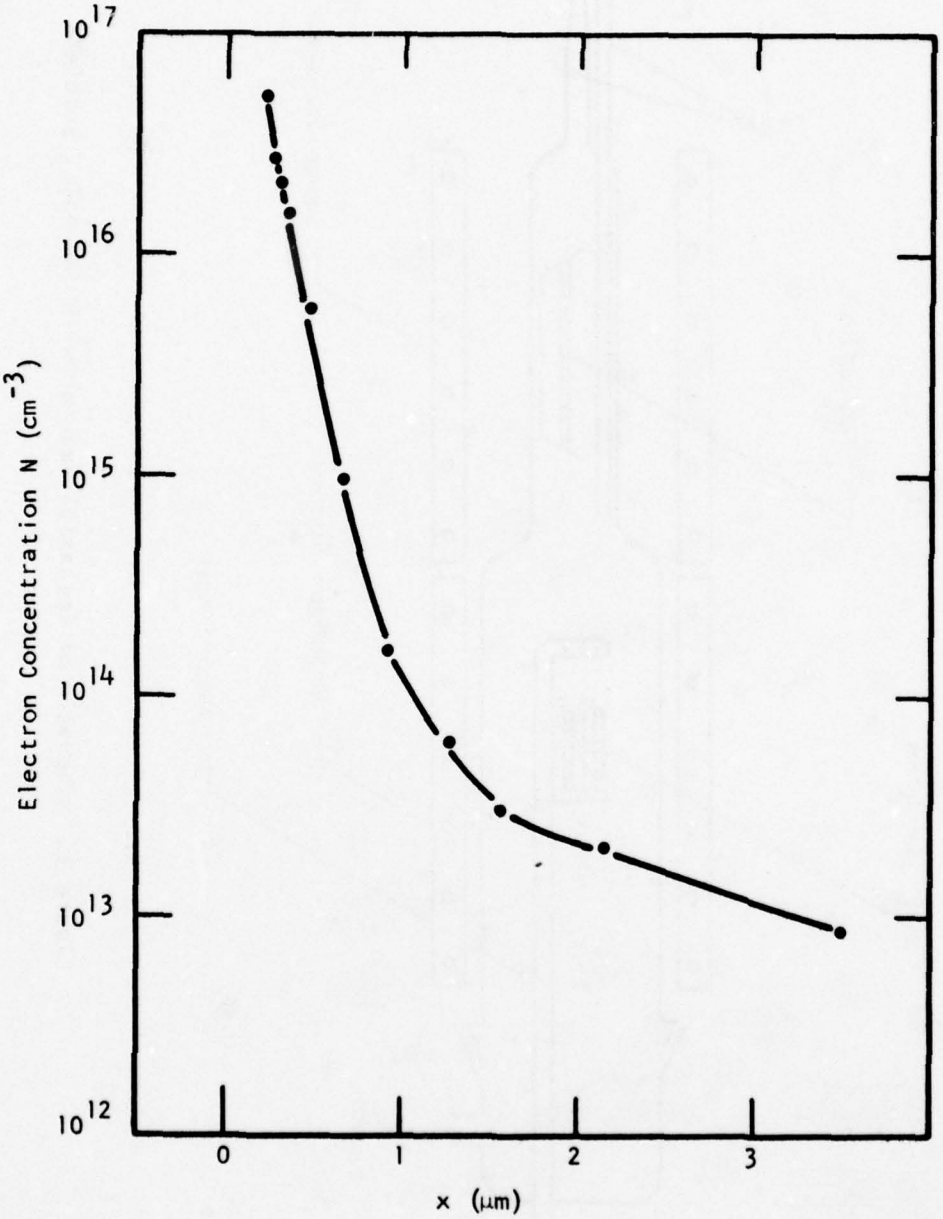


Figure 10. Doping Profile of an FET Structure

series resistance effects of FET structures introduce errors into doping profiles and that the real profile always lies below the measured data in regions approaching the buffer layer.

C. Device Fabrication

All the GaAs FETs discussed in this report were fabricated by the same process. Every slice consists of an undoped buffer layer followed by the n-type active layer ($n \sim 1 \times 10^{17}$ cm^{-3}) grown epitaxially on a Cr-doped substrate.

The first step in fabrication following receipt of the anodically thinned slices is to etch mesas through the active layer to isolate the source and drain except for the channel under the gate and to provide an insulating surface for the gate bonding pad. The slices are etched with $H_2SO_4/H_2O_2/H_2O$: 1/8/40 at room temperature for about 30 seconds. This etch does not attack the photoresist and does not etch excessively near the resist edges.

The next step is source/drain metallization. The pattern is defined in photoresist, and the metal is evaporated over the slice and removed from regions where it is unwanted by dissolving the resist in acetone (the lift-off process). The metallization is about 2100 Å eutectic composition AuGe followed by 500 Å Ni. The contacts are made ohmic by alloying for one minute at 450°C in flowing He. This metallization system provides very smooth, low resistance contacts with sharp edge definition. The contact resistance is typically 0.3 Ω per mm gate width for slices having $n \sim 1 \times 10^{17}$ cm^{-3}.

The gate metallization is also defined by a lift-off process, but the definition is by electron beam instead of ultraviolet light. The electron resist is polymethyl methacrylate (PMMA), and the gate is lifted off with acetone similar to the source/drain metallization. The gates are automatically

realigned within the 5 μm source/drain gap to alignment marks in every 2mm x 2mm "field" to ± 2000 Å. These marks are the "L"-shaped patterns in Figure 2 and were put down with the source/drain metallization. The gate length can be varied by simply reprogramming the electron beam computer, and gate lengths of 0.5 μm or less are well within the machine's capability. The yield of devices with no shorted or open gate fingers following gate definition is substantially higher when electron beam definition rather than conventional contact printing is used, due to mask-slice abrasion and mask run-out with the latter. The PMMA thickness is 5000 to 7000 Å, and a 4000 Å Al film is readily lifted off. Aluminum was originally chosen as the gate metal because of the ease with which it is evaporated and its ability to produce good Schottky barriers to GaAs even after annealing to 400°C or more. However, recent life test results have led us to replace Al with TiPtAu to improve reliability (see Part D of this section). An important step is to etch the slice slightly in $H_2SO_4/H_2O_2/H_2O$: 1/8/40 at 5°C immediately prior to gate metallization in order to recess the gate below the epitaxial surface. This has been found to improve device microwave performance significantly.

Following gate metallization, a 0.5 μm layer of Cr/Au (defined by lift-off) is evaporated onto the source and drain to improve current spreading to the contact edges and bonability. A nitride layer is then plasma-deposited on the active areas to protect them from scratches and shorts to the source wires. This is the stage at which the photographs of Figure 2 were taken. Next, a 10 μm layer of Au is plated to the sources and drain pads to aid in bonding, and the slice is lapped to 100 μm.

D. Device Reliability

For several months a number of single-cell GaAs power FETs were biased at typical operating voltages (V_{ds} = 8V, V_g = -2V) with a 50°C heat sink in air. Many of these failed in periods of 100 to 3300 hours, and some have not yet failed in 4600 hours. The mean-time-to-failure (MTTF) was about 1300

hours. In all cases, the failure occurred because the gate was no longer able to pinch off the drain current. SEM examination showed that on each failed device one or more gate fingers had a small piece missing near the gate pad. It is not known yet why this occurred, but the missing portions appear to have been dissolved. Recent results at other laboratories indicate that this may be due to electrolytic corrosion of the aluminum. This is accentuated by high humidity, temperature (if less than 100°C), and voltage. Although the hottest spots of the gate stripes were hotter than 100°C, the parts near the gate pad were probably not and were therefore subject to corrosion. The nitride overcoat retards, but does not eliminate this process. This failure mode can be eliminated by hermetically sealing the devices in an inert atmosphere or employing a different gate metallization.

The life test set-up was modified by adding the capability for applying rf power to a small number of devices. A Gunn diode oscillator (9.5 GHz) followed by an FET driver with an output power of 1.2W was used to drive several devices in parallel. Four single-cell devices were operated with 8V drain bias, -2V gate bias, and 125 mW input power ($\sim$ 500 mW output power) at a heat sink temperature of 80°C. After 122 hours, none of these devices had failed; I_{dss} decreased about 3%, similar to results with dc bias only. Two other devices operated under the same bias and temperature conditions with 350 mW rf input power ($\sim$ 800 mW output power) did not fail after 118 hours. Two devices were also operated with 350 mW rf input power with 100°C heat sink for 133 hours without failure. One device operated under the latter conditions failed catastrophically after less than 14 hours. This may have been an "infant failure." There were no "open gate" failures of the type observed at 50°C with dc bias only. If the failure mechanism were thermally activated, we should have seen some failures at the higher temperature. Whatever the causative agent for the gate failure, the approach taken was to eliminate it by replacing the Al gates with e-gun evaporated TiPtAu. The TiPtAu metallization system has several advantages, such as potentially better adhesion to

GaAs; much lower susceptibility to attack by processing chemicals or contaminants; lower susceptibility to gate burn-out from high currents or static discharge; compatibility with gold wire bonding; and potential for simultaneous use as a bonding pad metallization, eliminating one mask step. GaAs power FETs have been fabricated with 1 μm TiPtAu gates. The microwave performance is similar to that of other devices from the same slice having aluminum gates. Ten of these devices were put on life test (dc only) with 8V drain bias and -1.5V gate bias with a 100°C heat sink. At the date of this report, they had accumulated 800 hours. There was one catastrophic failure after about 250 hours that was not related to the open gate problem. If the failures are due to a thermally activated mechanism with an activation energy of 1.6 eV, then an MTTF at 25°C ambient in excess of 4×10^6 hours has been reached. By contrast, the MTTF of 1300 hours measured at a 50°C ambient temperature with Aluminum gates is equivalent to only 2×10^4 hours at 25°C ambient using the same activation energy.

SECTION III
AMPLIFIER DEVELOPMENT

This section of the report describes the circuit work performed during the 18-month period of the X-band solid-state module program. The specific goal of this program is the demonstration of a 5 W, 25 dB gain amplifier module (9 to 10 GHz) operated in pulsed mode for airborne, active-element phased-array radar application. The amplifier requirements are listed in Table 1. Two approaches were pursued to meet the amplifier performance goals: an all GaAs FET amplifier and an FET/Read diode hybrid amplifier. Two amplifiers of each type were delivered to NRL at the completion of the program.

The design and fabrication of the totally integrated FET driver amplifier module are described along with its microwave performance. Development of the high-power, balanced FET output stage with lumped-element impedance matching is also described. The design approach and the microwave performance result of the 5 W Read diode output stage are given. The cw as well as the pulsed characteristics of the final, integrated amplifier modules are presented.

A. Amplifier Configurations

1. All FET Power Amplifier

Figure 11 shows an all GaAs FET power amplifier configuration. The amplifier consists of a driver amplifier and a power amplifier. The driver amplifier provides 20 dB gain at 32 dBm (1.58 W) output with three cascaded FET amplifier stages. Figure 12 shows the circuit layout of the all GaAs FET power amplifier module. The three-stage driver amplifier is shown in the upper left-hand section of the amplifier module. The design and optimization of the driver amplifier are discussed in Section III.B.

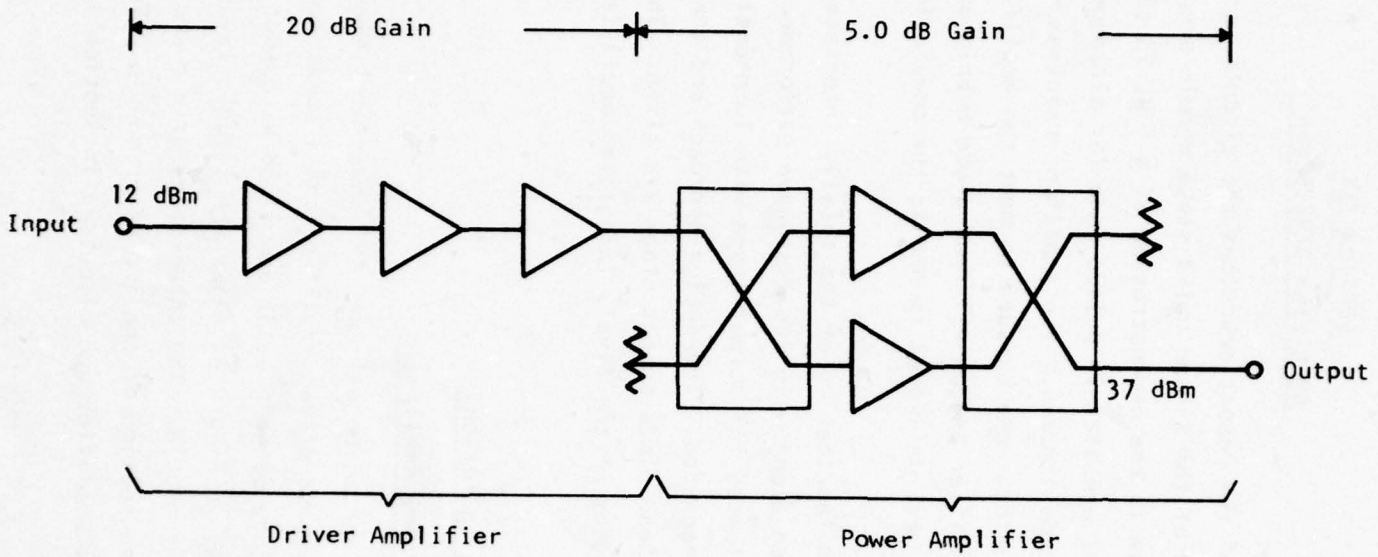


Figure 11. An All-FET Power Amplifier Configuration

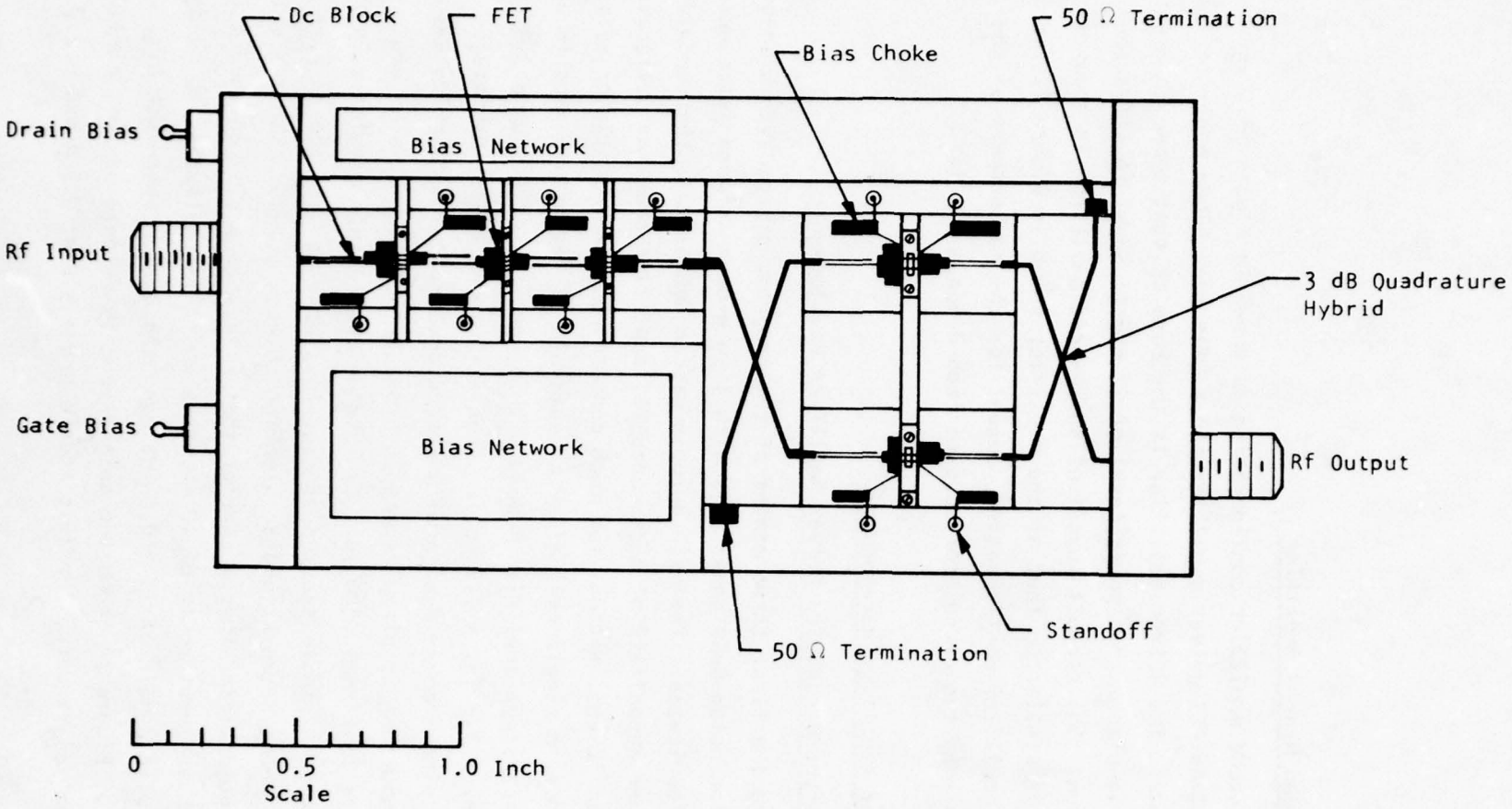


Figure 12 Circuit Layout of the All-FET Power Amplifier Module

2. FET/Read Hybrid Amplifier

The second amplifier configuration is shown in Figure 13. It consists of a GaAs FET driver amplifier and a GaAs Read diode amplifier as the output stage. The driver amplifier is the same as that shown in Figure 11, and is to have an output power level of 32 dBm (1.58 W) to drive the Read diode stage. The circuit layout of the hybrid amplifier is shown in Figure 14 and is similar to that of the amplifier shown in Figure 12 for the all FET power amplifier configuration, except for the replacement of the power FET output stage by the circulator-coupled Read diode amplifier.

B. FET Driver Amplifier Development

1. Prototype Breadboard Driver Amplifier Development

During the first three months of the program, a prototype breadboard driver amplifier using GaAs power FETs with 1 μm e-beam defined gates was designed and fabricated. The main purpose was to demonstrate the bandwidth and output power capability of a cascaded FET amplifier over the designated bandwidth (9 to 10 GHz) without too much concern about the amplifier efficiency. For this purpose, a single-cell (1200 μm gate width) device was used in each stage of a three-stage amplifier module with dimensions of 4.8 cm x 3.3 cm x 1.8 cm (1.9 in. x 1.3 in. x 0.7 in.). Figure 15 shows this three-stage amplifier. A single-ended design with interstage impedance matching was used. Each of the input-output circuits and interstage matching networks was fabricated on a 15.2 mm (0.300 in.) by 15.2 mm (0.300 in.) alumina substrate (0.25 mm thick). A single section of edge-coupled line was used as part of the interstage matching networks and dc blocking between stages. The FET chip was mounted on a gold-plated copper carrier that fits into a slot on the amplifier housing. With an input power of 10 mW, this amplifier delivers 500 mW of output power with a gain of 17 ± 0.15 dB over the design bandwidth of 1 GHz (9 to 10 GHz). Figure 16 shows the gain-frequency resonse of this amplifier. The power supplies required for this module are + 9 V at 0.5 A and - 2.7 V.

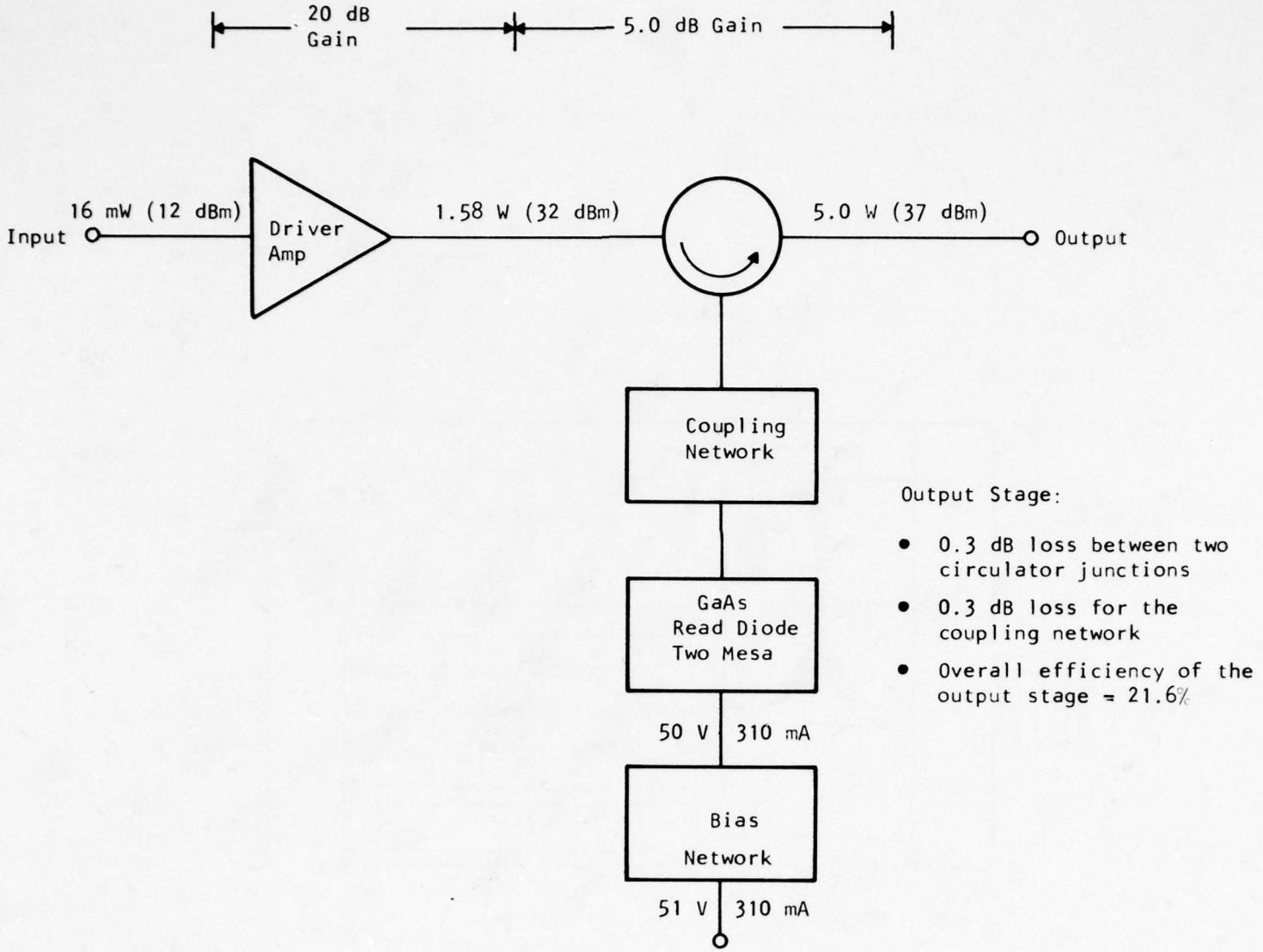


Figure 13. Schematic Diagram of the Hybrid FET/Read Amplifier

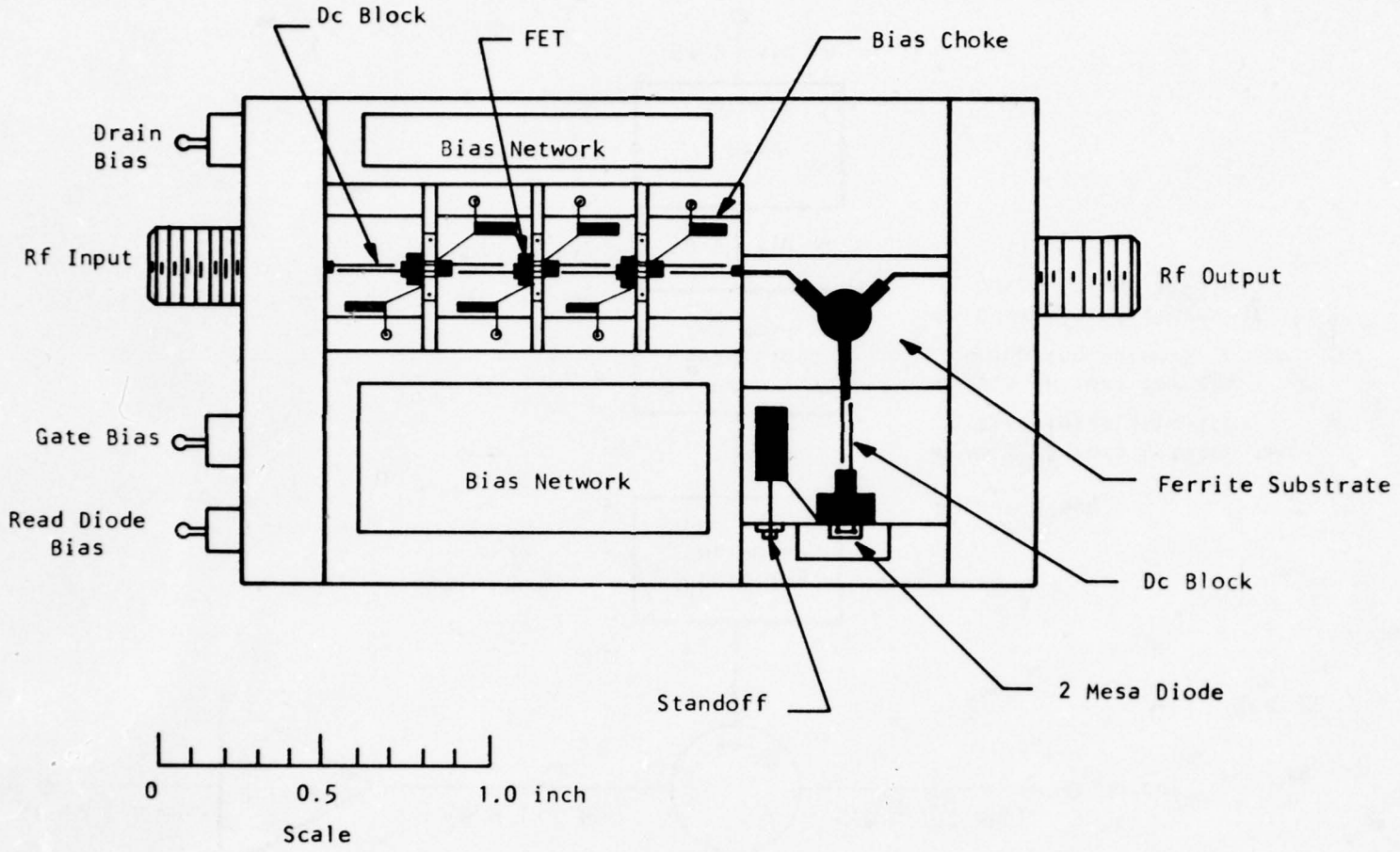


Figure 14. Circuit Layout of the Hybrid FET/Read Amplifier

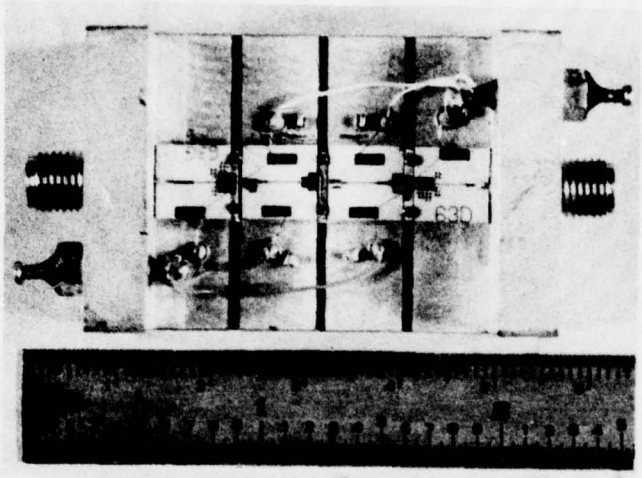


Figure 15. A 0.5 W, Three-Stage FET Amplifier

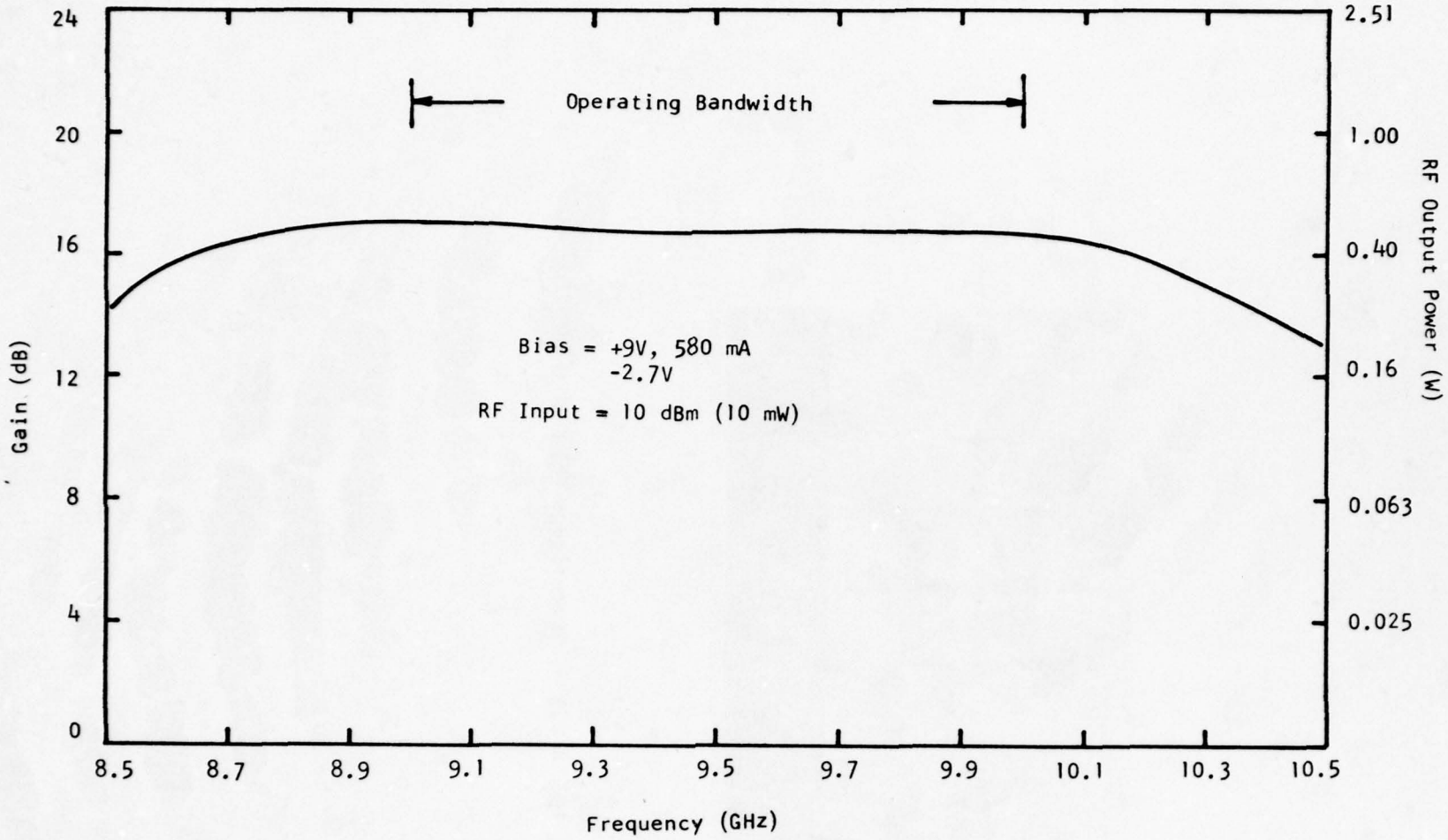


Figure 16. Gain-Frequency Response of the Three-Stage FET Amplifier Shown in Figure 12

The power-added efficiency is 10%. To increase the output power level, a single-stage power FET amplifier with a three-cell device (3600 μm gate width) was cascaded with the 0.5 W amplifier module described above. Figure 17 shows the gain-frequency response of the four-stage amplifier. Over the design 1 dB bandwidth of 1 GHz (9 to 10 GHz), an output power of 1.58 W was achieved with a 20 dB gain. The overall dc-to-rf conversion efficiency is 14.5%. It has thus been shown that the output power, gain, and bandwidth goals of the driver amplifier are achievable. As will be discussed in the next subsection, further optimization of the device size (gate width) for each stage has resulted in a three-stage driver amplifier with about the same output power and gain and an overall efficiency of 20 to 30%.

2. Amplifier Efficiency Optimization

The second three months of the contract were devoted to the efficiency-gain optimization of the driver amplifier stages for obtaining maximum efficiency. For this purpose, devices with various gate widths were used in different microstrip circuits optimized for maximum gain and efficiency at X-band.

GaAs FET devices with 300 μm gate width and 1 μm gate length were used as the first stage of the driver amplifier. Figure 18 shows the gain-frequency and efficiency characteristics of this amplifier. The amplifier has an output power of 100 mW with 8 dB gain. The 1 dB bandwidth is 2.7 GHz (7.7 to 10.4 GHz). Power-added efficiencies in excess of 30% have been achieved.

For the second stage of the driver amplifier, the design goal was 6 to 7 dB gain at 500 mW output. Two 300 μm gate width GaAs FETs on the same chip were mounted in single-stage microstrip amplifier circuits for gain-efficiency optimization. With 6 V drain bias, 151 mW was obtained at 9.5 GHz with 9.8 dB gain. The gains of the amplifier were in excess of 8 dB for frequencies

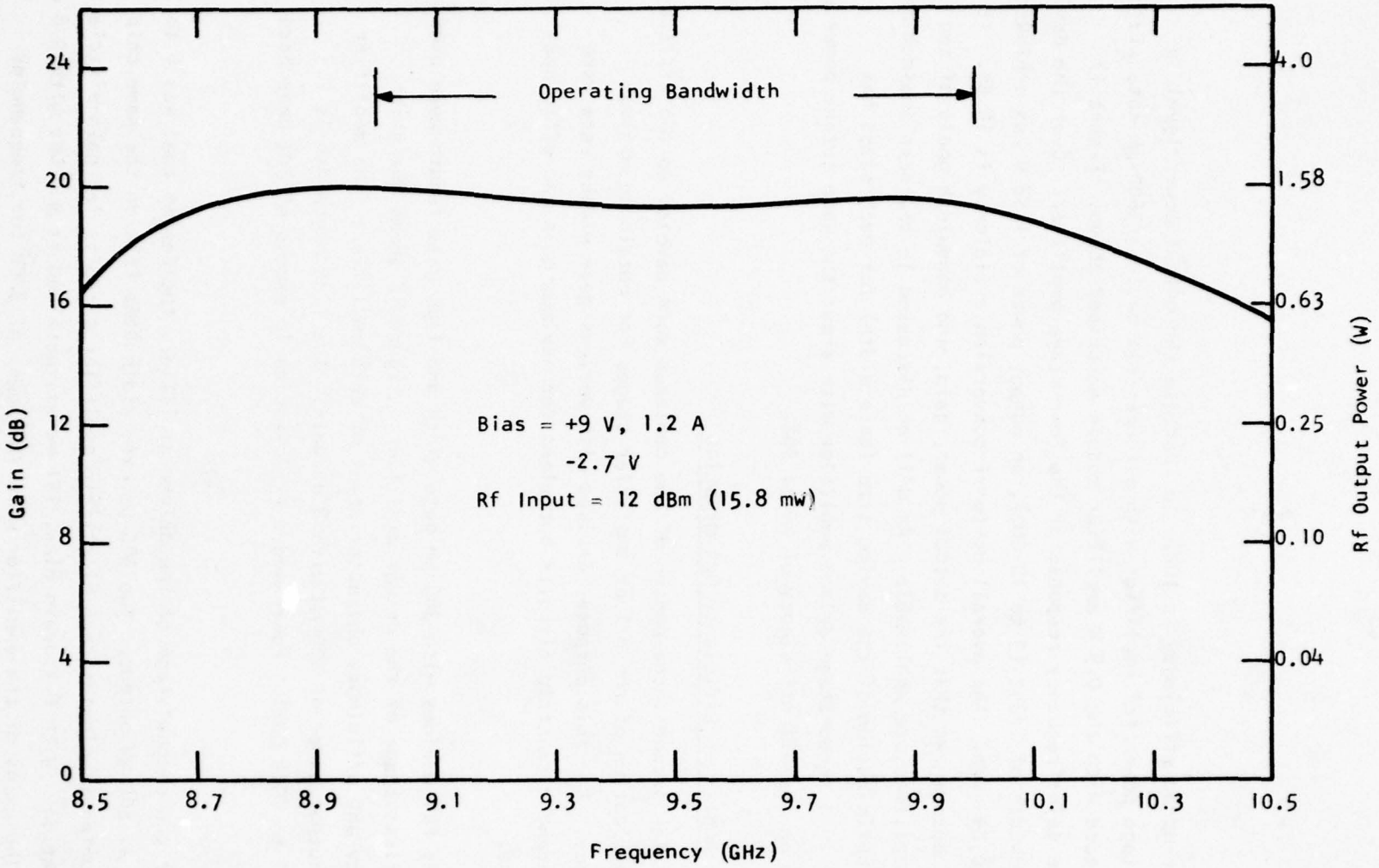


Figure 17. Gain-Frequency Response of a Breadboard Driver Amplifier

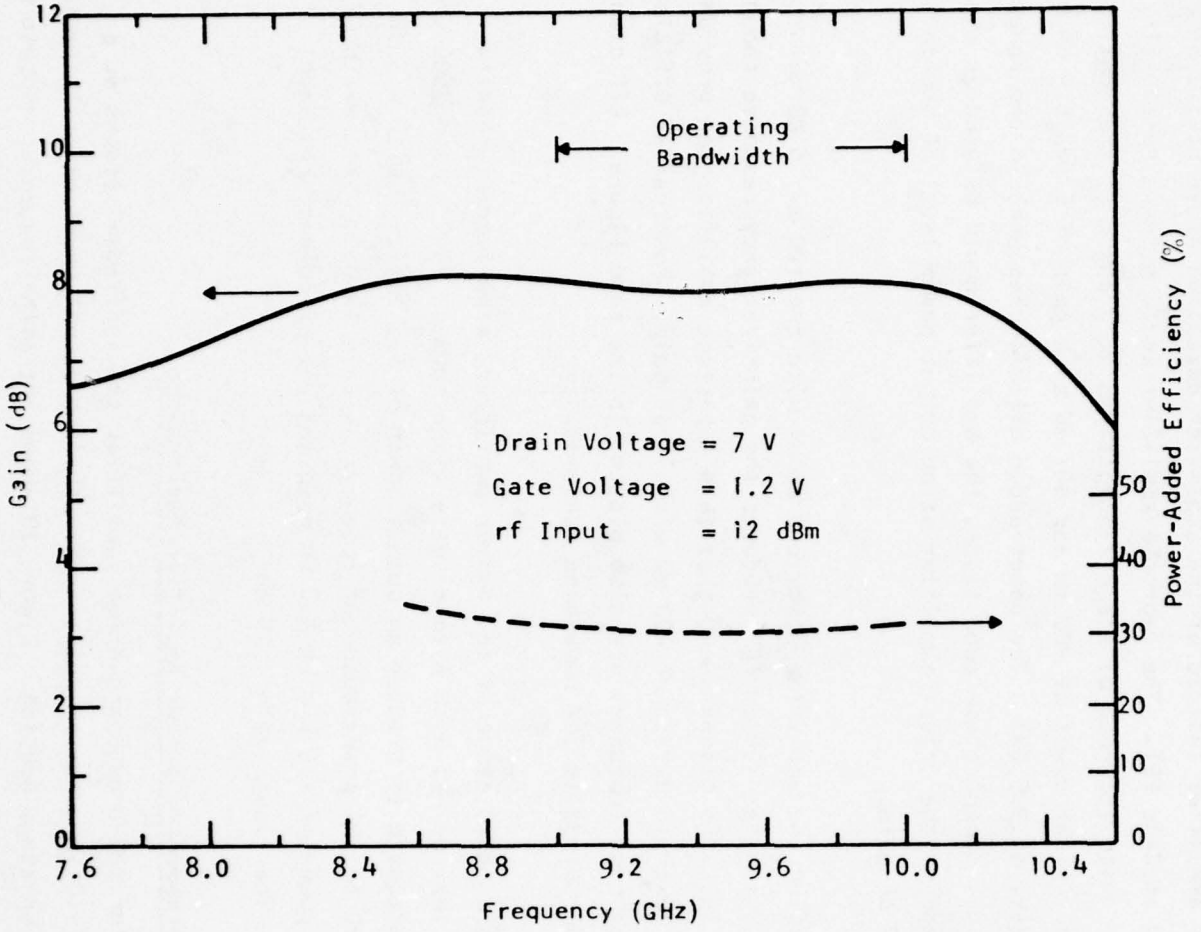


Figure 18. Gain-Frequency and Efficiency Characteristics of the First Stage of the Driver Amplifier

between 7 and 10.1 GHz with 12 dBm input. Within the 9 to 10 GHz band, the gain was 9.5 ± 0.3 dB. This amplifier could be used for the first stage of the driver amplifier instead of the amplifier described above utilizing a single 300 μm GaAs FET. The two-cell amplifier could offer a reliability advantage. With increase of the drain voltages to 7 and 8 V, the amplifier provides an output power of 400 mW and 447 mW at a gain of 6 and 6.5 dB, respectively, at 9.5 GHz. The power-added efficiencies were in the range of 35 to 40%. Under these conditions, the amplifier could be used as the second stage of the driver amplifier at an output power level of 400 to 500 mW and 6 to 7 dB gain.

Cascading the amplifier described above with the 100 mW, 8 dB gain amplifier using the 300 μm FET produces the gain-frequency response shown in Figure 19. The figure shows that this two-stage amplifier can provide an output power in excess of 400 mW with 14 dB gain. Power-added efficiencies as a function of frequency are also plotted in the same figure. Efficiencies on the order of 33 to 36% have been achieved.

For the third stage of the driver amplifier, experimental results indicated that an FET with a total gate width between 2400 μm and 3600 μm would be adequate to produce an output power of 1.5 to 1.6 W with ∿ 5 dB gain and 20 to 30% power-added efficiency. With a 2400 μm gate width FET an output power of 1.5 W with 4.8 dB gain and 24% efficiency has been achieved. The linear gain is 5 dB.

3. Breadboard Driver Amplifier Performance

For the breadboard driver amplifier the individual stages were characterized in terms of gain, bandwidth, and output power prior to cascading in the three-stage housing. Figure 20 shows the gain-frequency response of this three-stage driver amplifier. The drain bias voltage was used as a parameter. It is shown that, at a supply voltage of 9 V, an output power of

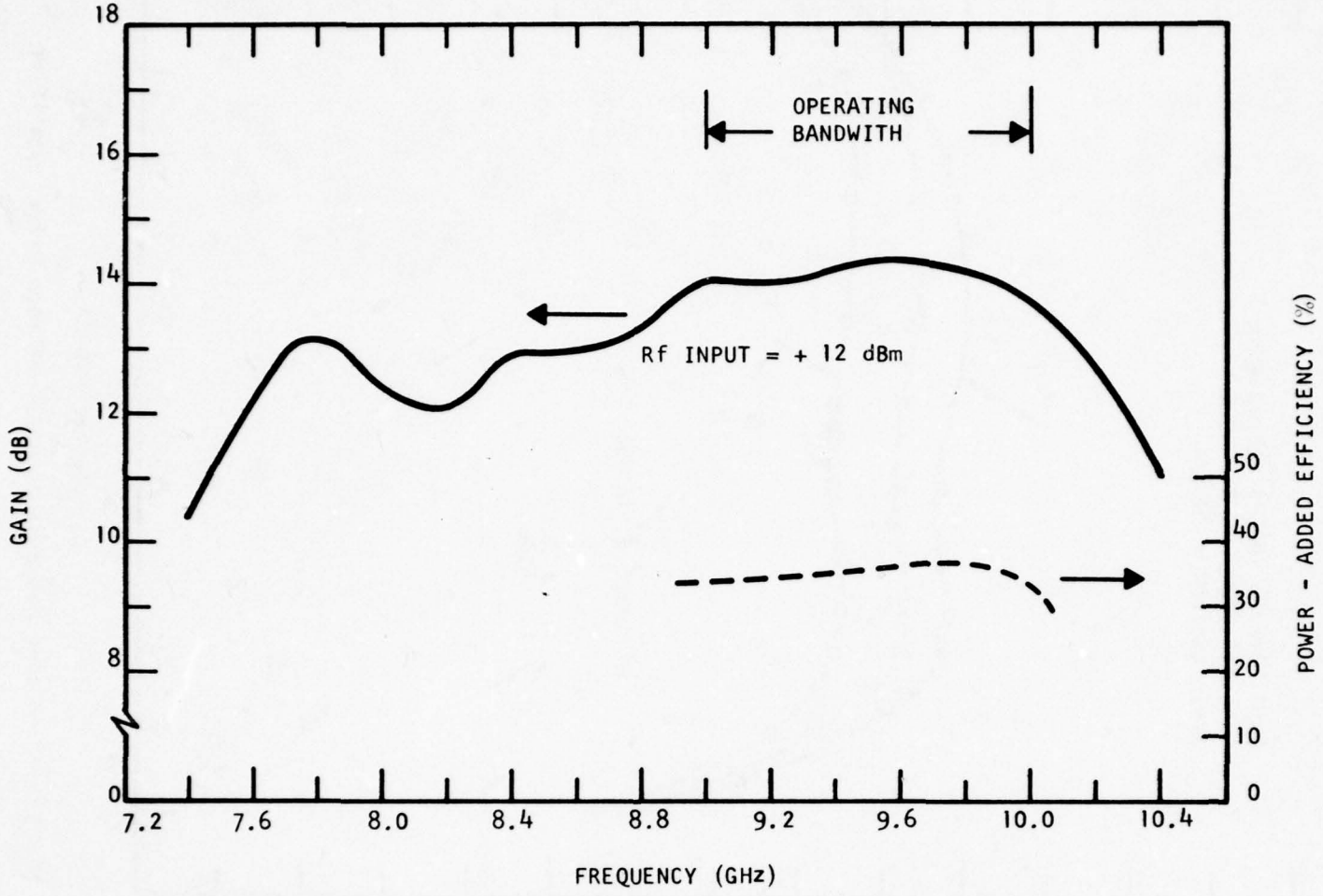


Figure 19. Gain-Frequency and Efficiency Characteristics of a Two-Stage GaAs FET Amplifier

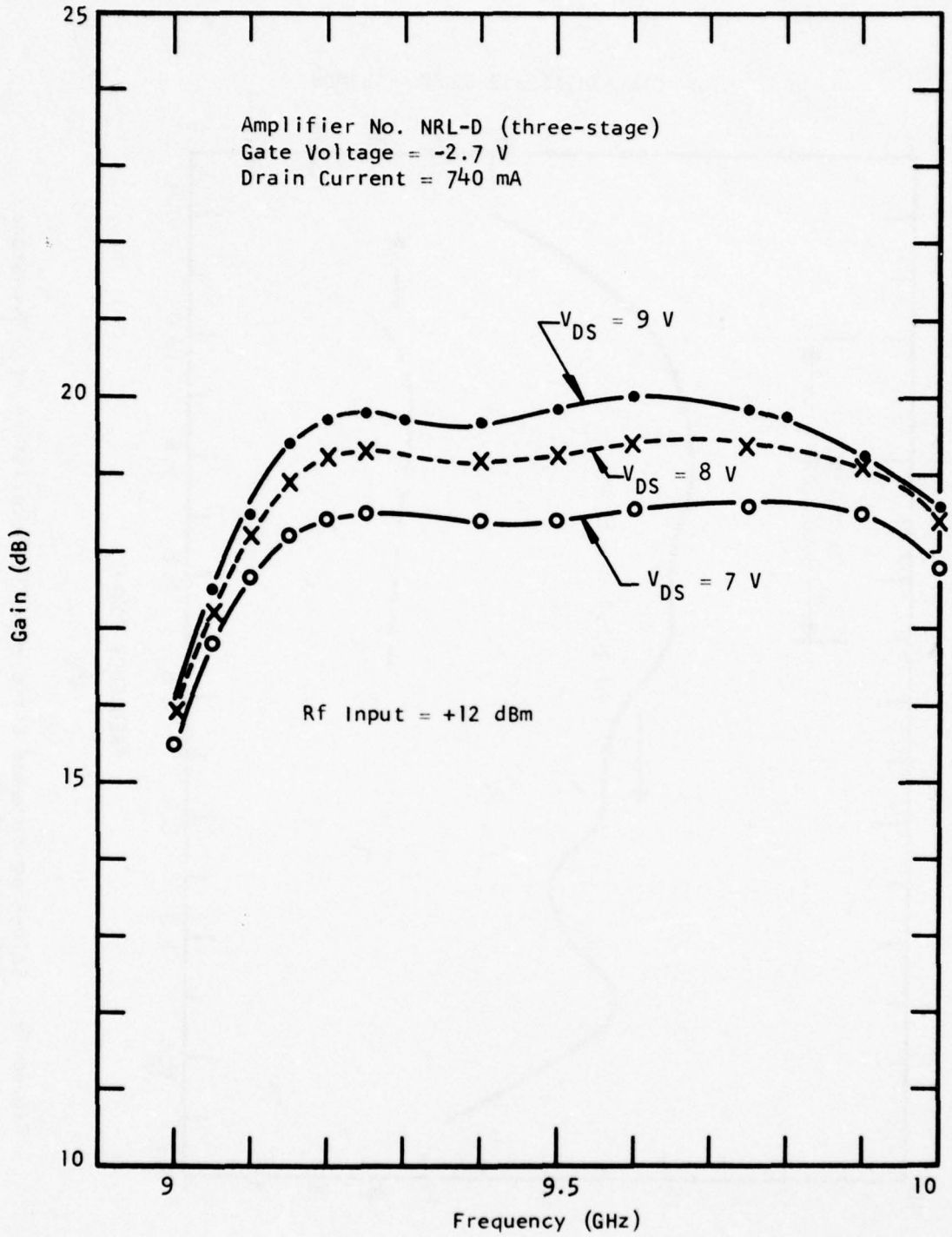


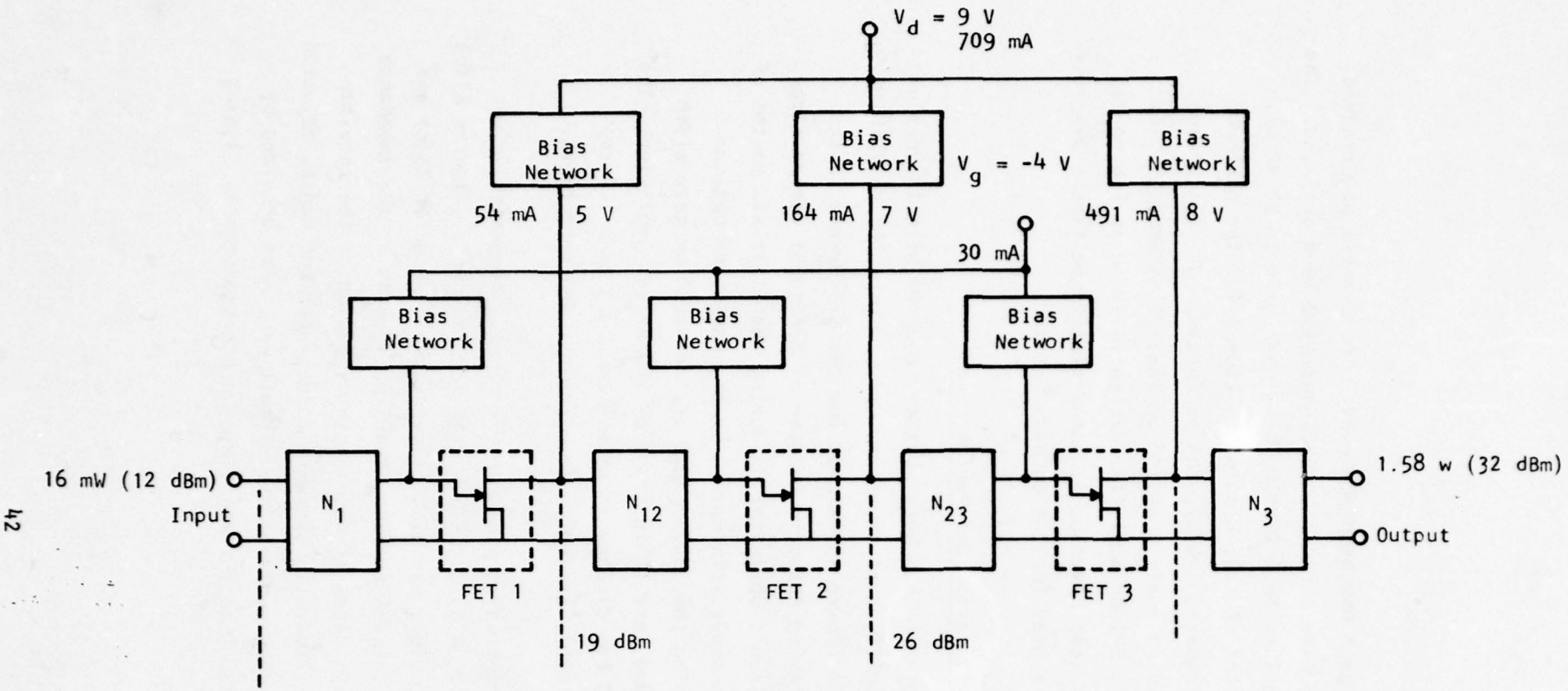
Figure 20. Gain-Frequency Response of a Three-Stage Driver Amplifier

1.58 W (32 dBm) with 20 dB gain has been achieved. The overall power-added efficiency of 24% (including bias circuit losses) has also been achieved. The 1 dB bandwidth is 900 MHz (9.1 to 10.0 GHz). The linear gain is 22 dB with the 1 dB gain compression point of 1.36 W output. Except for the narrower bandwidth (0.9 GHz vs. the required 1 GHz), the performance of this breadboard amplifier meets the design goals proposed by Texas Instruments. The block diagram of the original driver amplifier design is shown in Figure 21. Figure 22 is a photograph of this breadboard, three-stage amplifier. Discrete resistors and capacitors were used for the dc bias network.

4. Driver Amplifier Integration and Performance

The degree of integration has been further advanced with the design of a compact, three-stage amplifier as shown in Figure 23(a). It is similar to the amplifier module shown in Figure 15, except for the difference in the impedance levels for the matching networks because of different device sizes. The results of the device/circuit optimization during the first six months of the program provided the necessary information on the design of optimum circuit topologies for matching the 300 μm, 900 μm, and 2400 μm gate width FETs used in the first, second, and third stage of the driver amplifier. The amplifier shown in Figure 23 has dimensions of 4.8 cm x 3.3 cm x 1.7 cm (1.9 inch x 1.3 inch x 0.7 inch), excluding input/output SMA connectors.

The specific circuit topologies used for the final, integrated driver amplifier design are shown in Figures 23(b), (c), (d), and (e). Figures 23(b) and (e) show the input and output matching circuits, while Figures 23(c) and (d) show the interstage matching networks. The line lengths of the impedance transformers were measured in terms of wavelength at 9.5 GHz. The required lumped inductances were realized with bondwire inductances and can be adjusted empirically. Fine tuning adjustments of the circuit were also provided by small gold tuning pads adjacent to the main impedance transformers. Tuning



Stage	I	II	III
Gain (dB)	7	7	6
Dc Input (watts)	0.27	1.15	3.93
Rf Output (watts)	0.079	0.400	1.58
Rf Power Added (watts)	0.063	.321	1.18
Power-Added Efficiency (%)	23	28	30

- Total dc Power Input = 6.5 watts
- dc Power Loss in Bias Networks = 1.15 watts
- Amplifier Efficiency Excluding Bias Network Losses = 29.2%
- Overall Amplifier Efficiency = 24%

Figure 21. Block Diagram of a Power FET Driver Amplifier

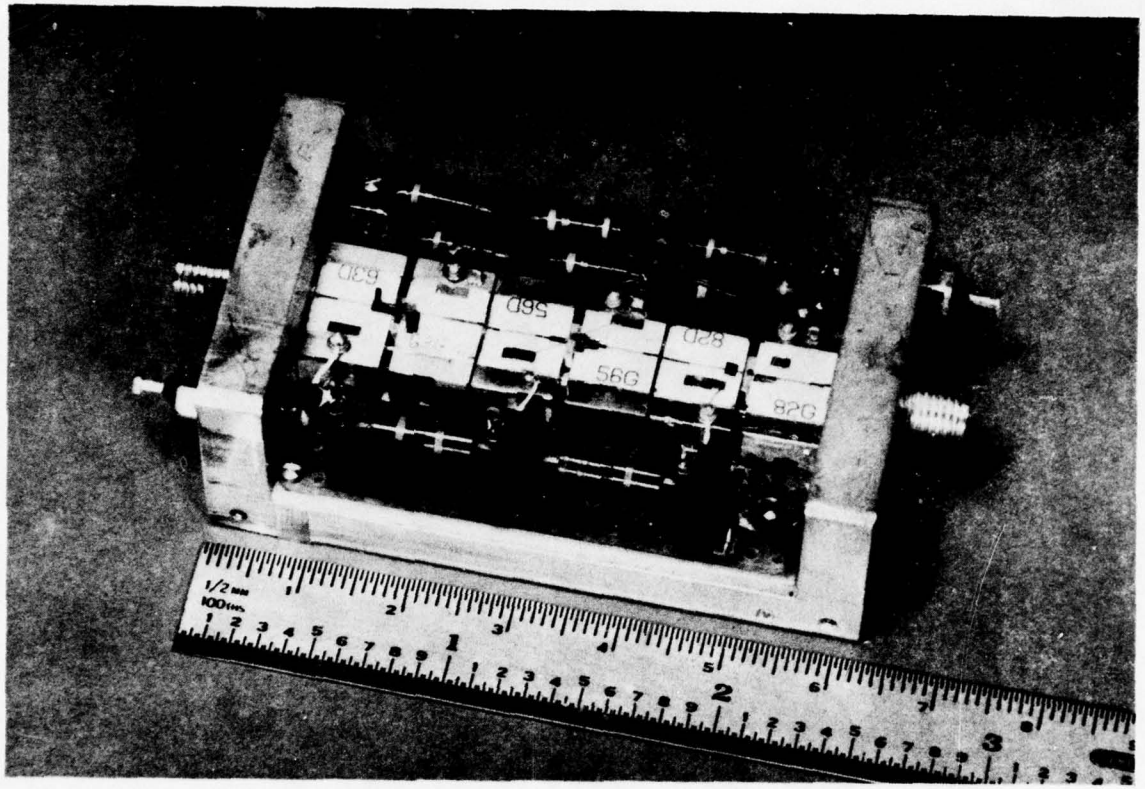


Figure 22. Photograph of a Three-Stage, Breadboard Driver Amplifier

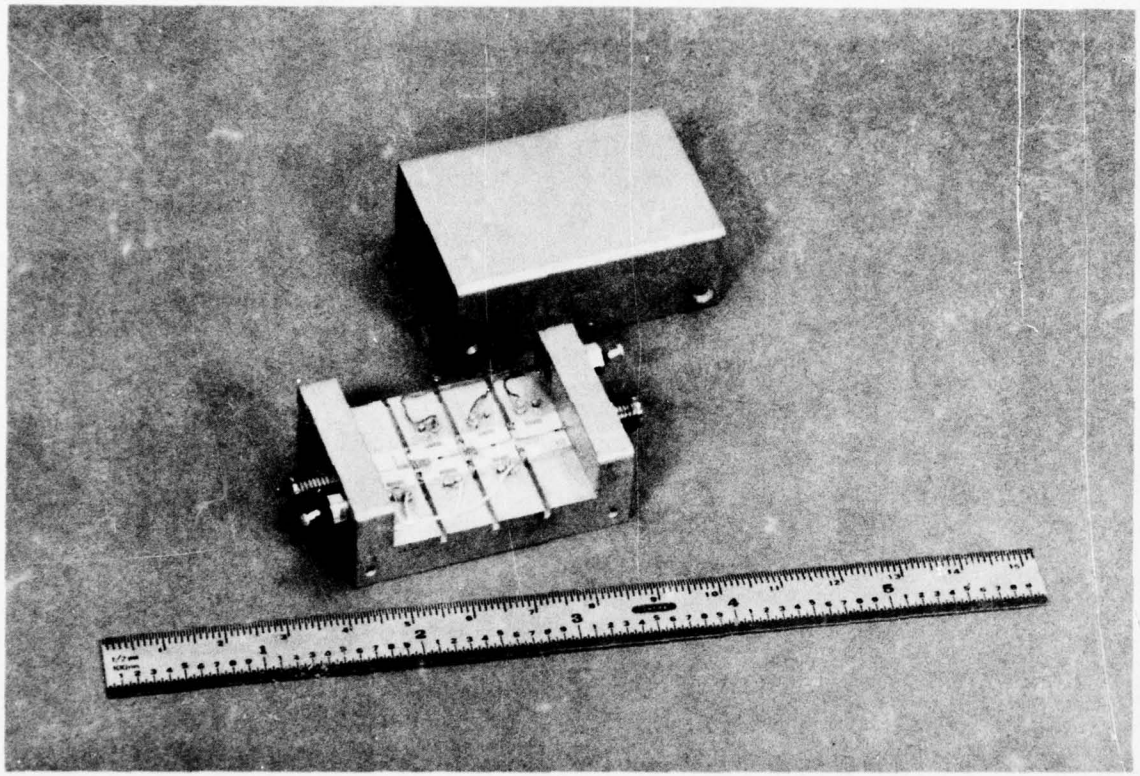


Figure 23(a). A Totally Integrated, Three-Stage Driver Amplifier Module

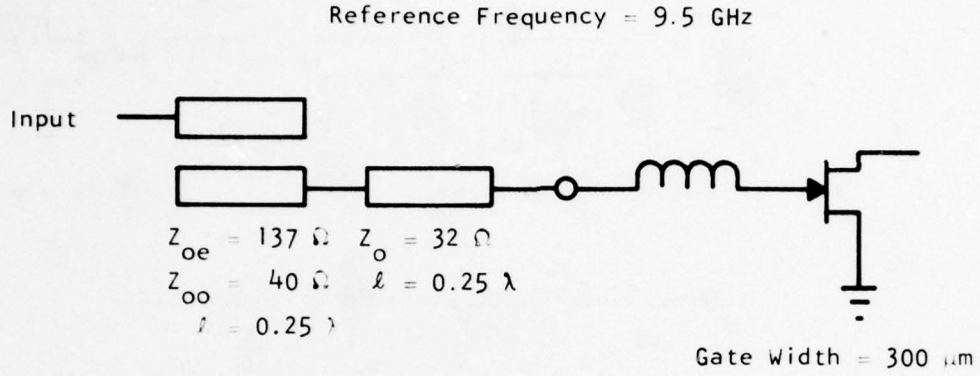


Figure 23(b). Input Matching Circuit

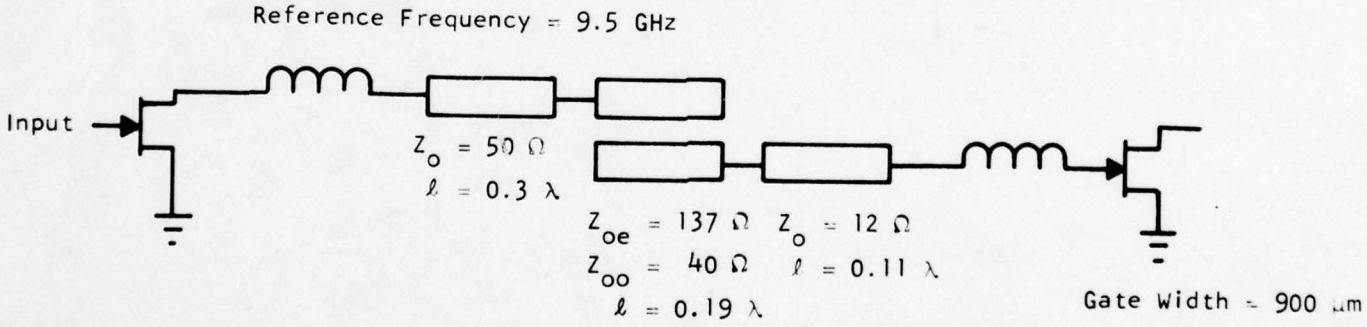


Figure 23(c). Interstage Matching Networks

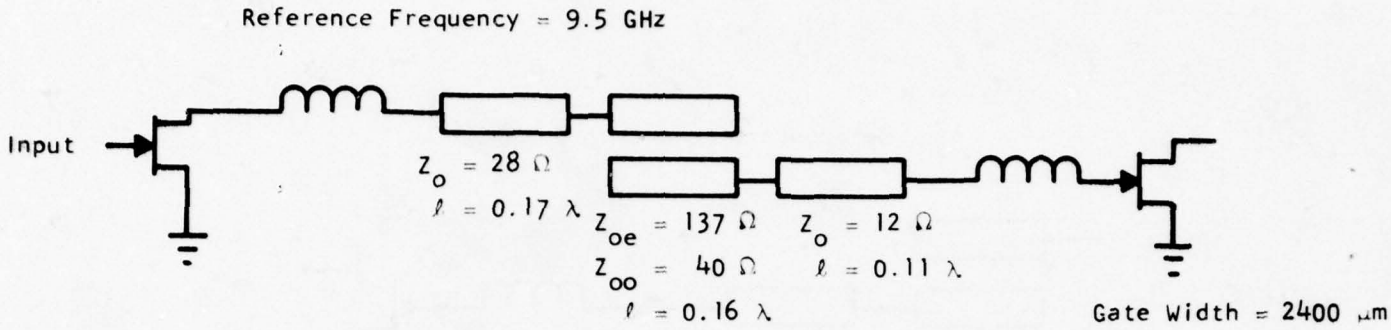


Figure 23(d). Interstage Matching Networks

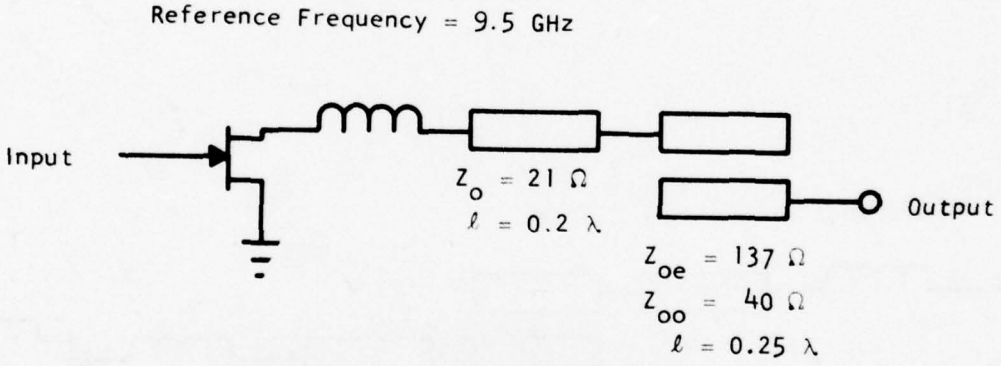


Figure 23(e). Output Matching Circuit

adjustments can be made by connecting one or several tuning pads using the split-tip welder with gold foil.

Although a beam-lead dc blocking capacitor (47 pF) is used as shown in Figure 23(a), a distributed dc block in [Figures 23(b)-(e)] was used for the final amplifier.

Several integrated driver amplifier modules were fabricated. Output powers of up to 1.6 W and efficiencies of greater than 20% can generally be obtained within the 9 to 10 GHz frequency band. Figure 24 shows the gain-frequency response of one of the three-stage driver amplifiers. The power supply requirements for the individual stages are also indicated. At 9.5 GHz an output power of 1.66 W with 28% power-added efficiency was achieved. The 1 dB bandwidth is 0.95 GHz (9.0 to 9.95 GHz). Although not shown in Figure 24, the 3 dB bandwidth extends from 7.5 to 10.2 GHz. Figure 25 shows the gain compression characteristic of this amplifier. Linear gain of 25 dB with an output power of $\sim$ 1.2 W can be obtained. The 1 dB gain compression point is 1.4 W. The results shown in Figures 24 and 25 were obtained when the amplifier module was biased with individual power supplies for the different stages. A bias network using chip resistors was subsequently designed and incorporated into the amplifier module. The final module was biased from two power supplies, one for the drains and one for the gates. Because of the bias network losses, the overall power-added efficiency of the module reduces to 26%.

Figure 26 shows the gain-frequency response of another driver amplifier module. A 1 dB bandwidth of 1.2 GHz (8.9 to 10.1 GHz) was achieved with 1.58 W (32 dBm) output and 20 dB gain. The power-added efficiency is 26%. The design goals for this amplifier have been met or exceeded in terms of output power, bandwidth, gain, and efficiency.

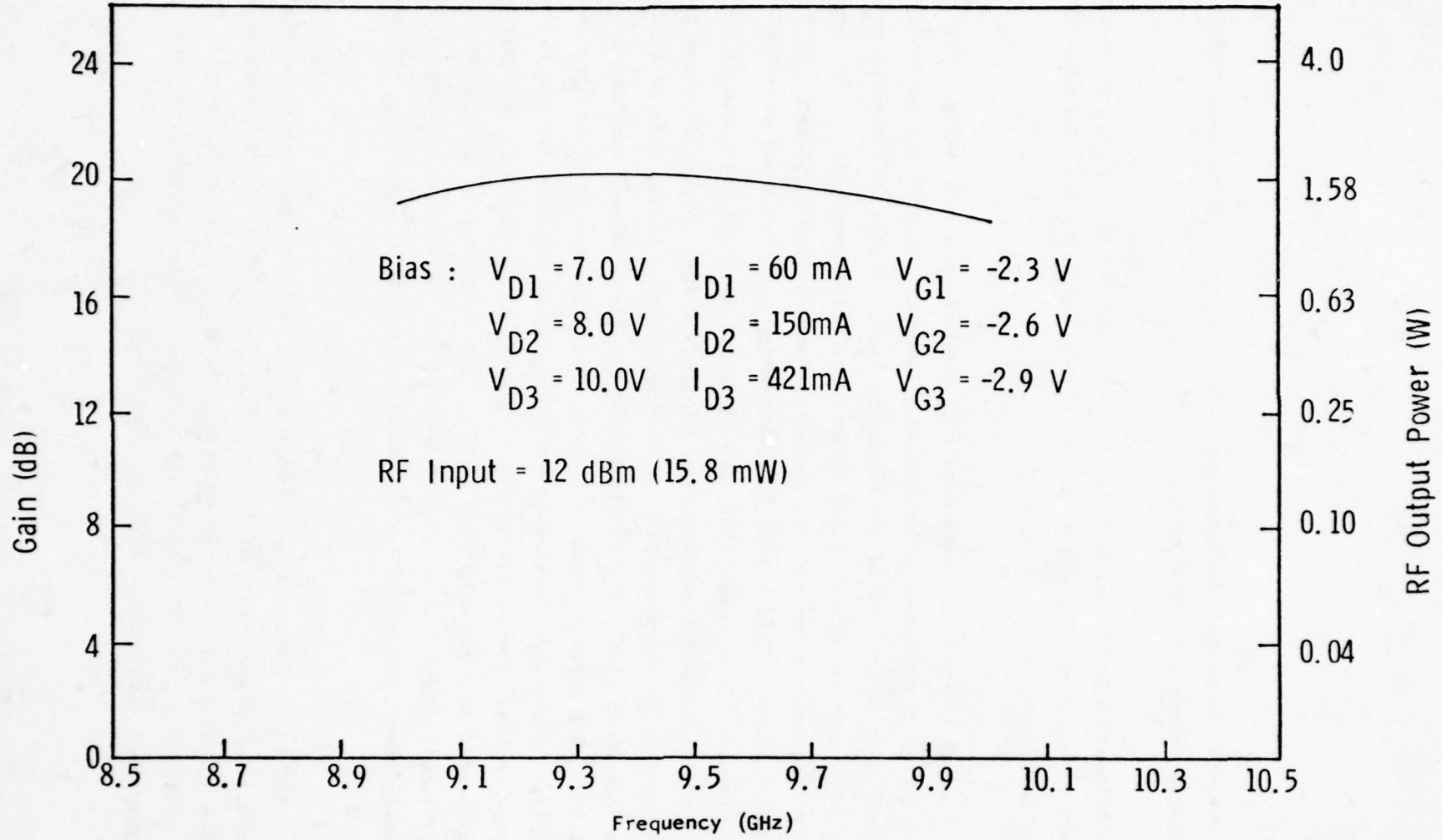


Figure 24. Gain-Frequency Response of a Three-Stage Driver Amplifier With Interstage Matching

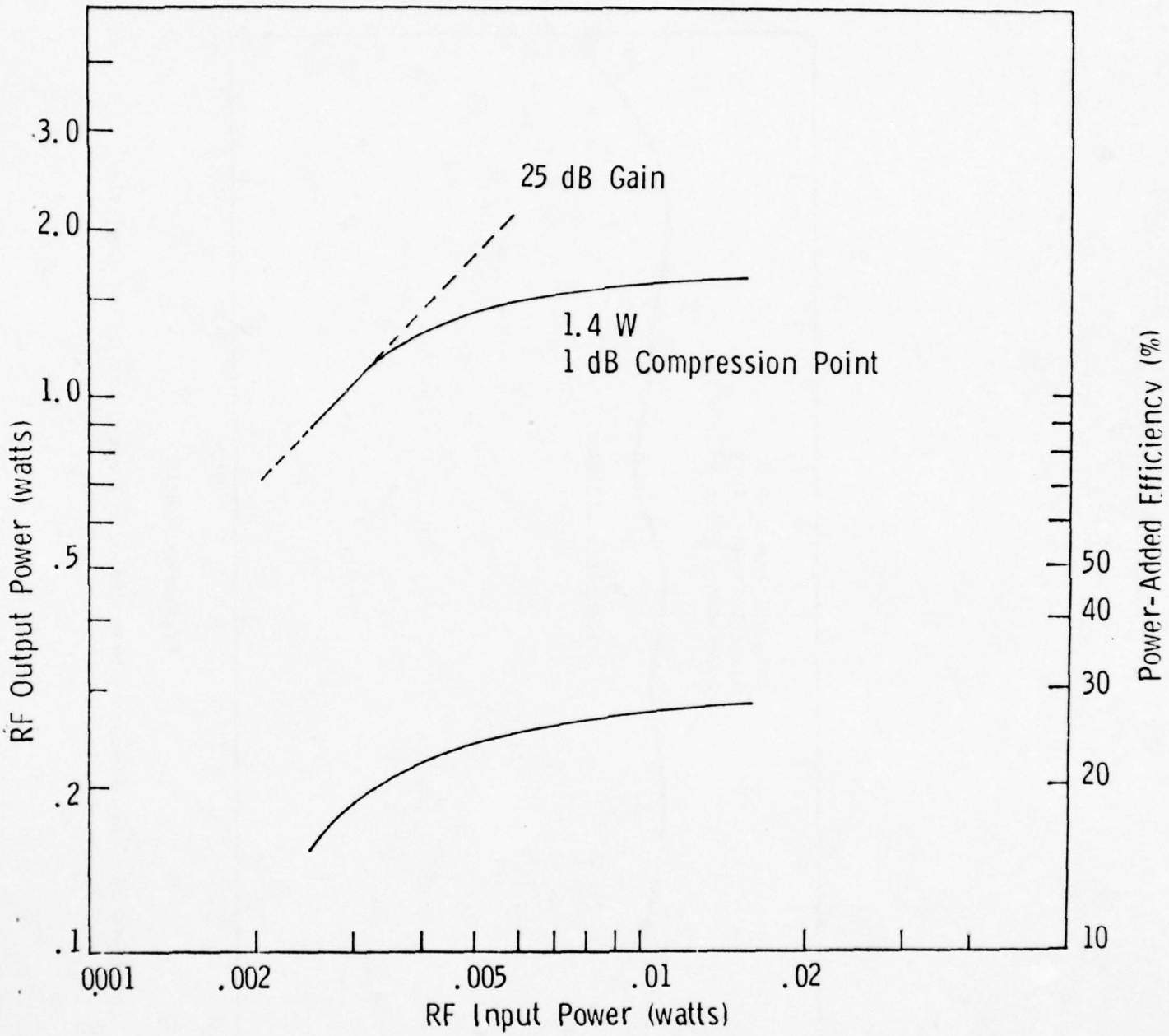


Figure 25. Output Power and Power-Added Efficiency of a Three-Stage Driver Amplifier as a Function of Input Power at 9.5 GHz

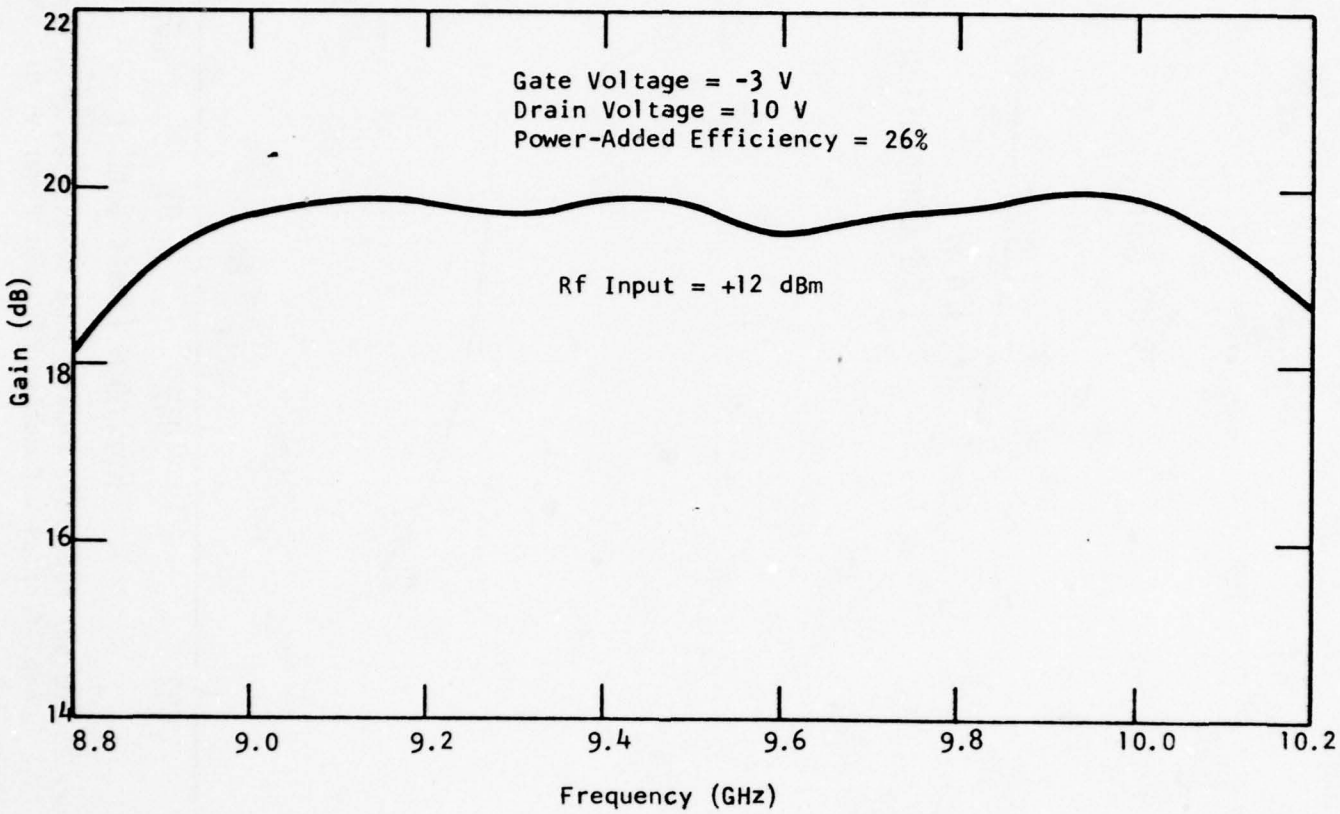


Figure 26. Gain-Frequency Response of a Three-Stage Driver Amplifier

The wide bandwidth capability of the microstrip matching circuits was demonstrated in an amplifier with the microwave performance shown in Figure 27. One watt of output power was achieved with 18 dB gain at 9.5 GHz with a power-added efficiency of 27%. The 1 dB bandwidth is 2 GHz (8.2 to 10.2 GHz). Figure 28 shows the gain compression curve of this amplifier.

C. FET Output Stage Development

In addition to the fabrication of several integrated driver amplifiers, as discussed above, a considerable amount of circuit effort was devoted to the 5 W FET output stage development. An output power design goal of 5 W with 5 dB gain in a balanced amplifier configuration was used as the circuit approach as shown in Figure 10. The output stage, consisting of input/output 3 dB hybrid and the two component amplifier matching circuits, was built on a separate carrier plate for flexibility of characterization prior to module integration. The principal circuit emphasis for the high-power FET output stage development was to devise an optimum circuit for the large gate width device (4800 to 6400 μm). For this purpose, the use of lumped LC elements for "impedance matching on the chip" was extensively pursued. This technique allows for combining more cells at the chip level while still maintaining a manageable impedance level for matching to the 50 Ω source and load.

1. Lumped-Element Impedance Matching

Figure 29 shows the circuit topology using lumped elements for impedance matching.[8] The values of the input/output shunt capacitances can range from 0.6 to 1.2 pF. The inductances are on the order of 0.3 to 1.5 nH and can be realized with bonding wire inductances. Silicon MOS capacitors were used as the matching elements. Figure 30 shows a photograph of an "internally matched" 6400 μm gate width FET. With a four-cell (6400 μm) device, 3 W of output power was obtained at 8.6 GHz with 4.8 dB gain and

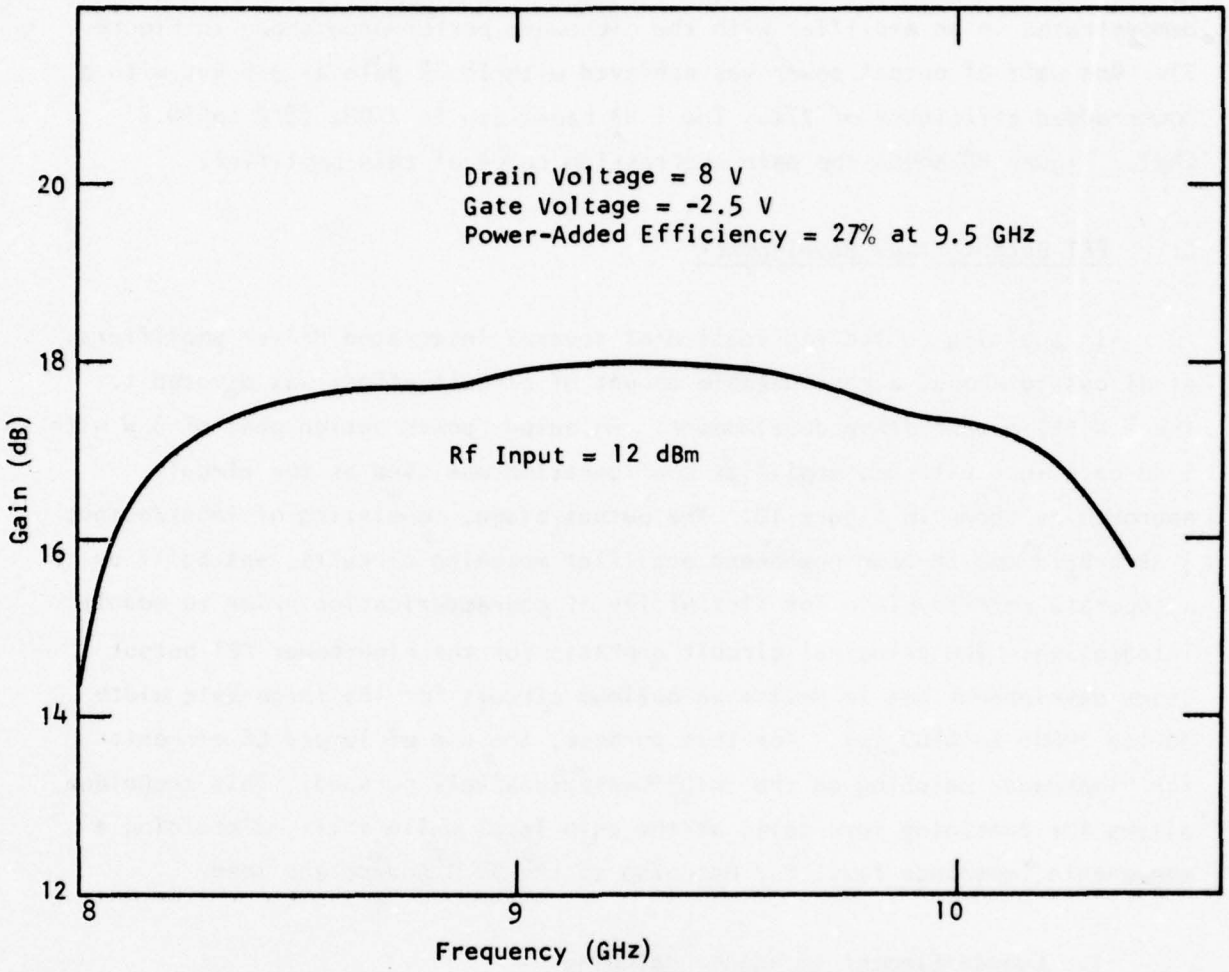


Figure 27. A Three-Stage 1 W GaAs FET Amplifier With 2 GHz Bandwidth

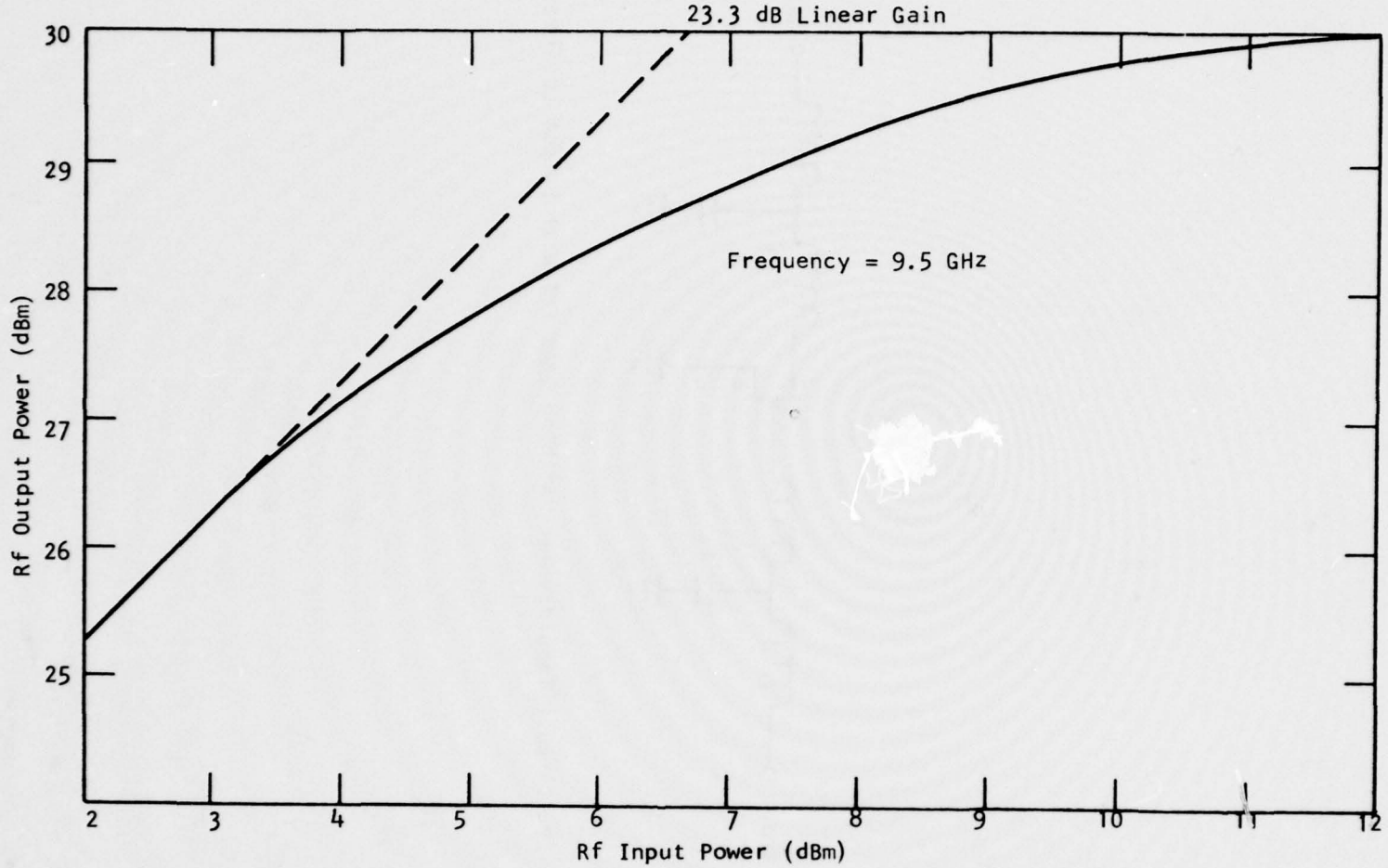


Figure 28. Compression Characteristics of the 1 W Amplifier

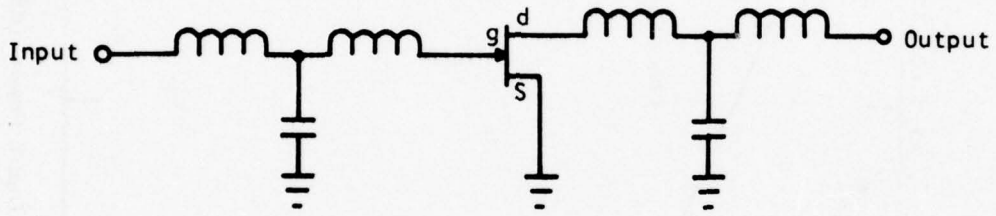


Figure 29. Circuit Topology for Matching GaAs FET With Lumped LC Elements



Figure 30. Photograph of a Four-Cell GaAs FET Amplifier with Internal Matching

26.2% power-added efficiency. Figure 31 shows the gain-frequency response of this 3 W amplifier. The gain compression characteric is shown in Figure 32. A linear gain of 6.2 dB was obtained at 1.7 W output. The 1 dB gain compression occurs at an output power of 2.8 W and 24% power-added efficiency. A 4800 μm gate width device has also produced 2 W output power with 6 dB gain and 1 dB bandwidth of 2 GHz (8 to 10 GHz). A power-added efficiency of 24% was obtained. Figure 33 shows the gain-frequency response. Because the gains of the 4800 μm gate width devices are higher than those of the 6400 μm gate width device, they are used in the balanced output stage, as discussed in Section III.C.3.

2. 3 dB Hybrid Coupler

One of the essential components for a balanced amplifier is a low loss 3 dB hybrid, which is used for power combining as well as for providing a low return loss for the power amplifier stage. Two designs were investigated, the tandem 90° hybrid and the interdigital 90° hybrid, to determine which exhibited the best overall properties with regard to insertion loss, return loss, directivity, and amplitude and phase tracking of the direct and coupled ports over the frequency range of interest.

The tandem hybrid is composed of two 8.3 dB edge-coupled hybrids fabricated on a polished 0.25 mm alumina substrate (see Figure 34). A 3 dB hybrid with a single edge-coupled configuration is difficult to produce because of the extremely tight spacing tolerance between the coupled lines, so the tandem approach was undertaken. Using OSM coax to microstrip transitions on all four ports of the test fixture, the measured output from the direct and coupled ports revealed nearly a 1 dB insertion loss (over and above the nominal 3 dB power split) in the 9 to 10 GHz frequency range. Although it is advantageous to have the hybrid fabricated on 0.25 mm alumina so it will be compatible with the substrate height of the FET matching circuits, the insertion loss observed with the tandem approach was larger

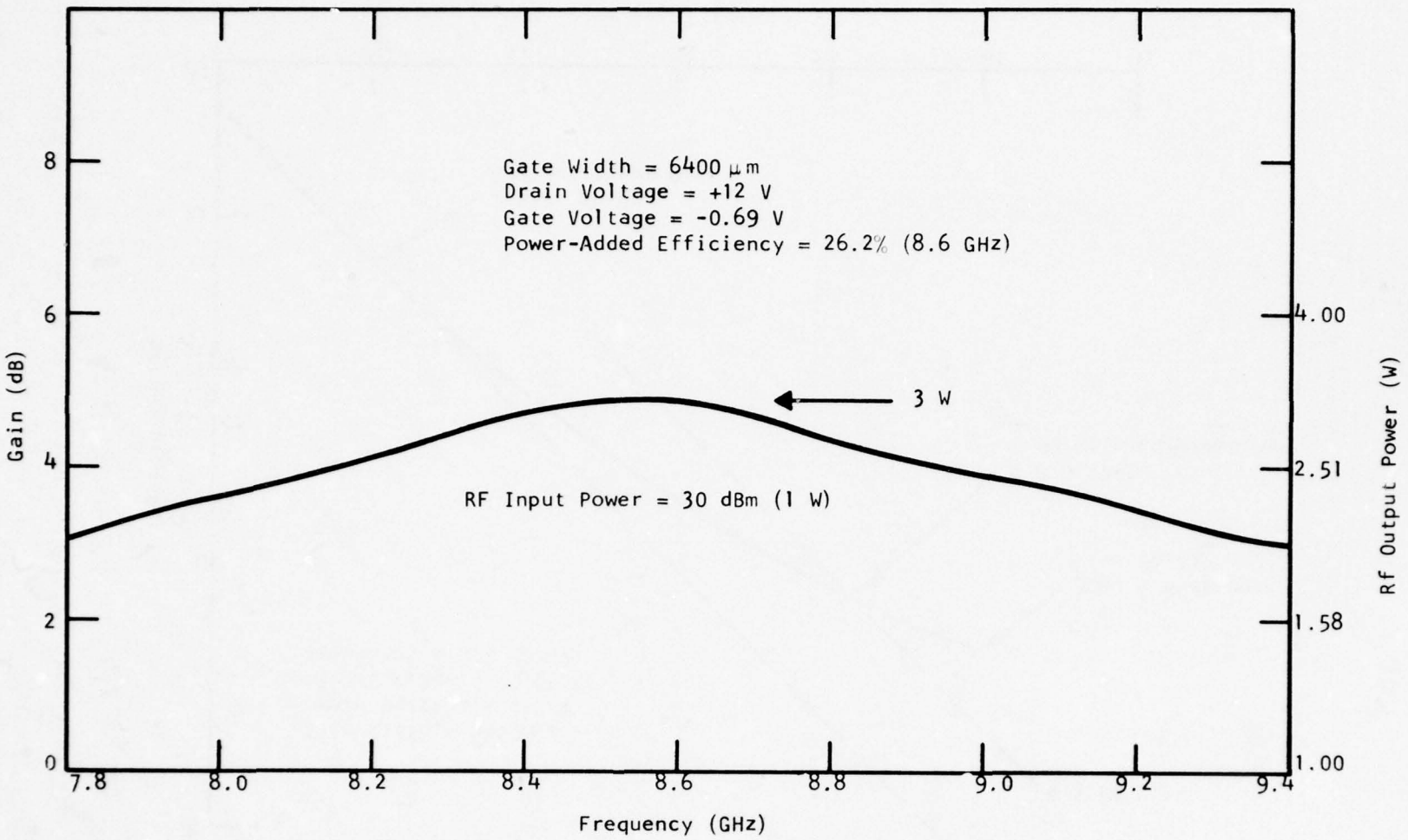


Figure 31. Gain-Frequency Response of a 3 W GaAs FET Amplifier

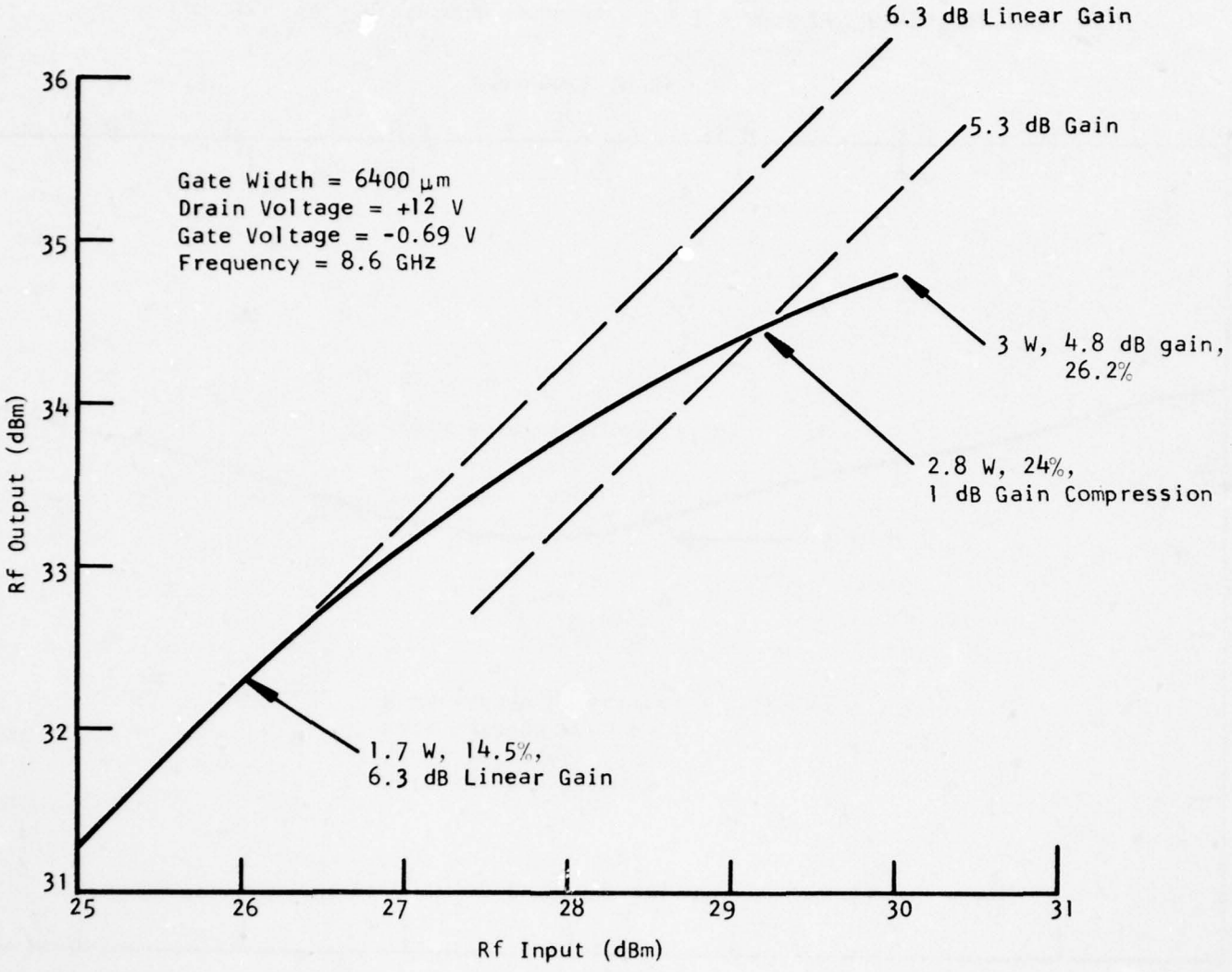


Figure 32. Compression Characteristics of a 3 W GaAs FET Amplifier

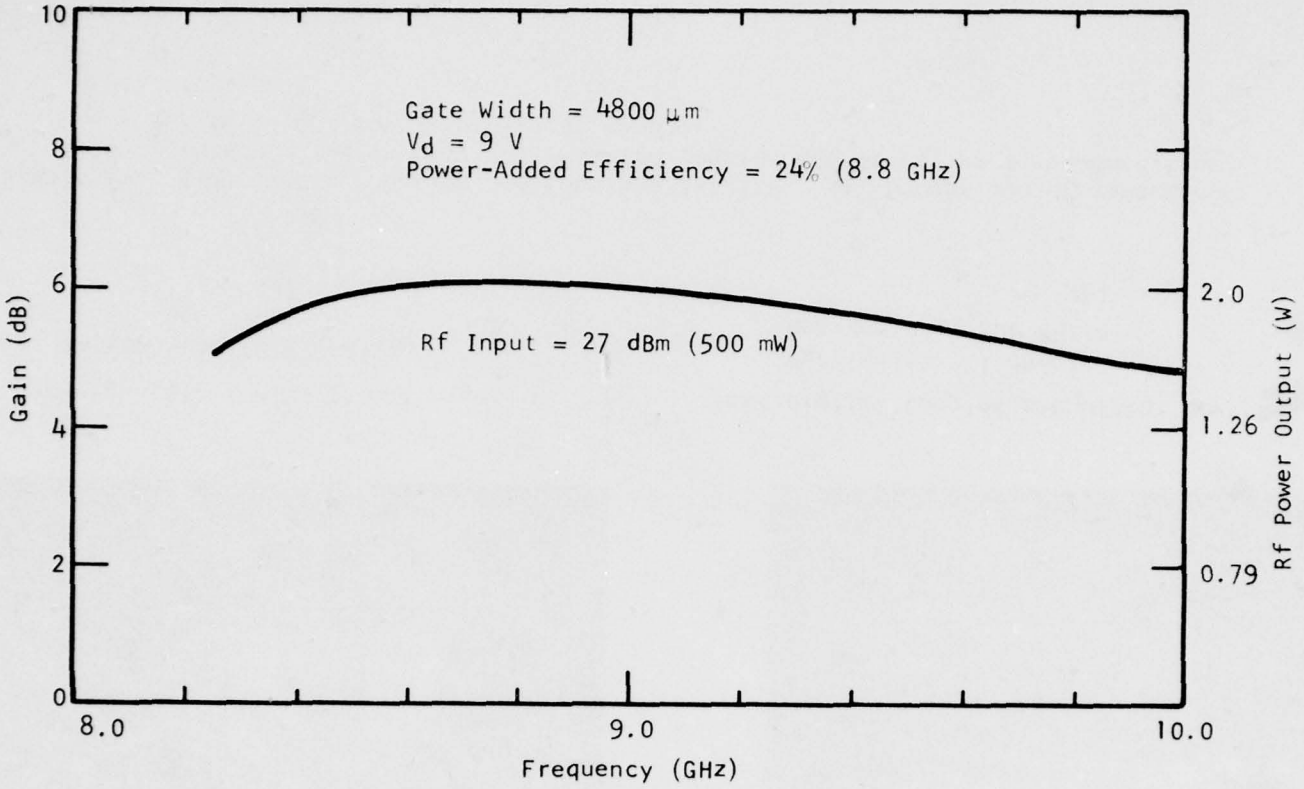
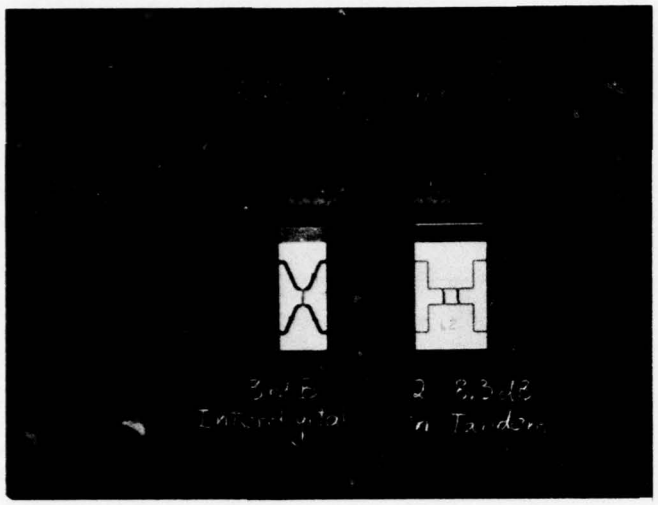
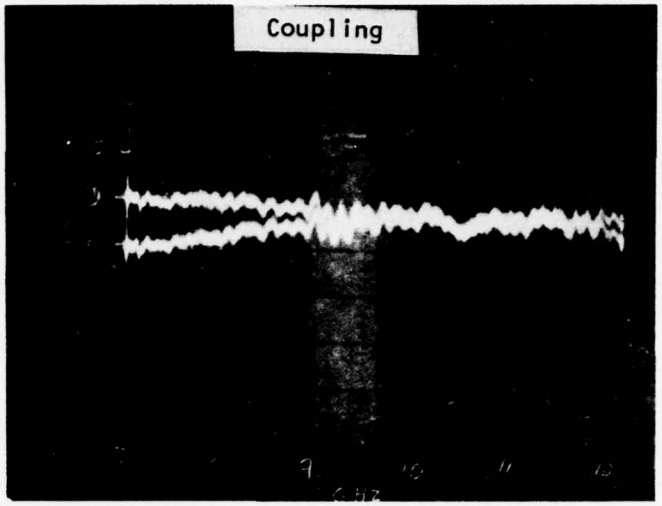


Figure 33. An 8-10 GHz GaAs FET Amplifier



- Interdigital - on 25 mil Al_2O_3
- Tandem - on 10 mil Al_2O_3

(a)



Interdigital Coupled and Direct Port Response

Vertical: 1 dB/div
Horizontal: 500 MHz/div

(b)

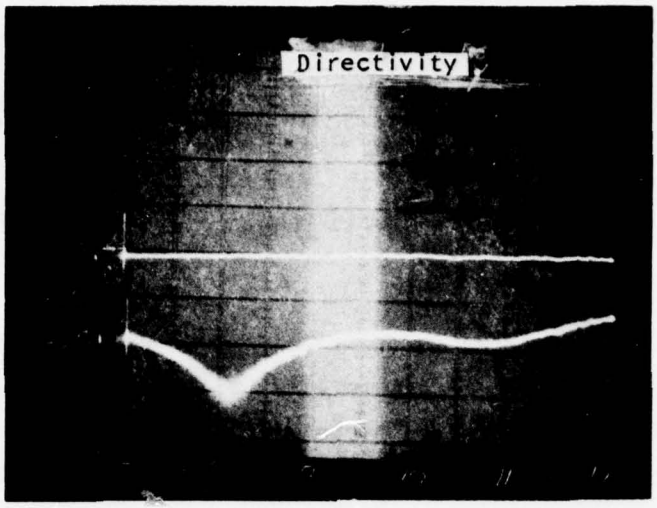
Figure 34. 3 dB Coupler, Design and Coupling Results. (a) Comparison of tandem and interdigital design; (b) measured coupled and direct port response from 7 to 12 GHz for interdigital coupler.

than anticipated. An interdigital hybrid (Lange coupler) design was therefore undertaken.

The coupling region of the interdigital hybrid consists of several parallel microstrip lines with alternate lines tied together (See Figure 34). Due to tight tolerances on the spacings between lines, the interdigital hybrid was fabricated on polished 0.63 mm alumina instead of 0.25 mm alumina. As seen in Figure 34, the insertion loss observed at the coupled and direct ports was 0.4 dB in the frequency range of 9 to 12 GHz. Figure 35 illustrates the directivity (> 13 dB from 7 to 12 GHz) and the return loss (> 15 dB from 7 to 12 GHz) for the interdigital hybrid. Figure 36(a) shows the measured coupled and direct port response from 7 to 11 GHz for a 3 dB Lange coupler etched on a 0.375 mm fuzed quatz substrate. Amplitude tracking is better than 0.5 dB from 8 to 11 GHz. Figure 36(b) shows the total insertion loss for two such couplers in a "divide-combine" configuration. At 9.5 GHz a total insertion loss of 0.75 dB is measured, which corresponds to a 0.37 dB insertion loss for one coupler (over and above the nominal 3 dB power split). The interdigitated coupler on quartz substrate was implemented in the final balanced amplifier design. The isolated port was altered to incorporate an internal termination.

3. Balanced FET Amplifier Performance

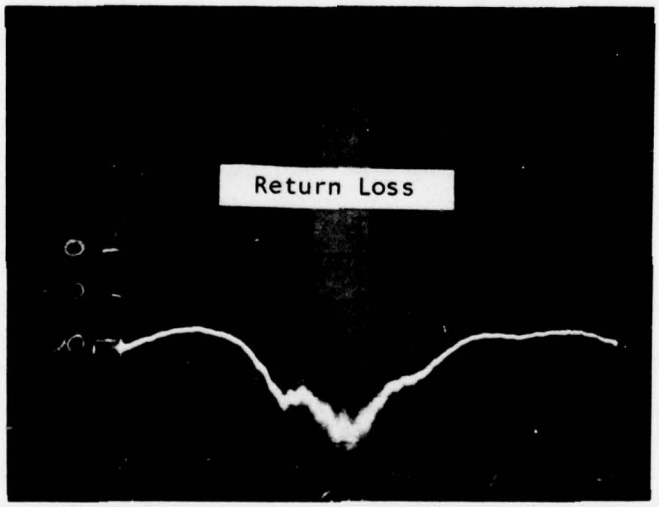
Figure 37 shows a photograph of a prototype single-stage, balanced amplifier using a pair of Lange couplers on an alumina substrate. The component amplifier had an output of 3 W at 5 dB gain prior to hybrid combining. Figure 38 shows the gain-frequency response at two input power levels. An output power of 5 W with 4 dB gain and 19.4% power-added efficiency was achieved at 8.5 GHz. The 1 dB bandwidth is 1.4 GHz (7.6 to 9 GHz). The linear gain of the amplifier was 5.7 dB at 3 W output. The 1 dB gain compression output power was 4.5 W. A GaAs FET with a gate width of 6400 μm was used in each of the component amplifiers. The amplifier operating frequency band was lower than the design 9 to 10 GHz band.



Interdigital Coupled and Isolated Ports Response

Vertical: 10 dB/div
Horizontal: 500 MHz/div

(a)



Interdigital Return Loss

Vertical: 10 dB/div
Horizontal: 500 MHz/div

(b)

Figure 35. Measured Directivity and Return Loss for 3 dB Interdigital Coupler. (a) Directivity; (b) return loss

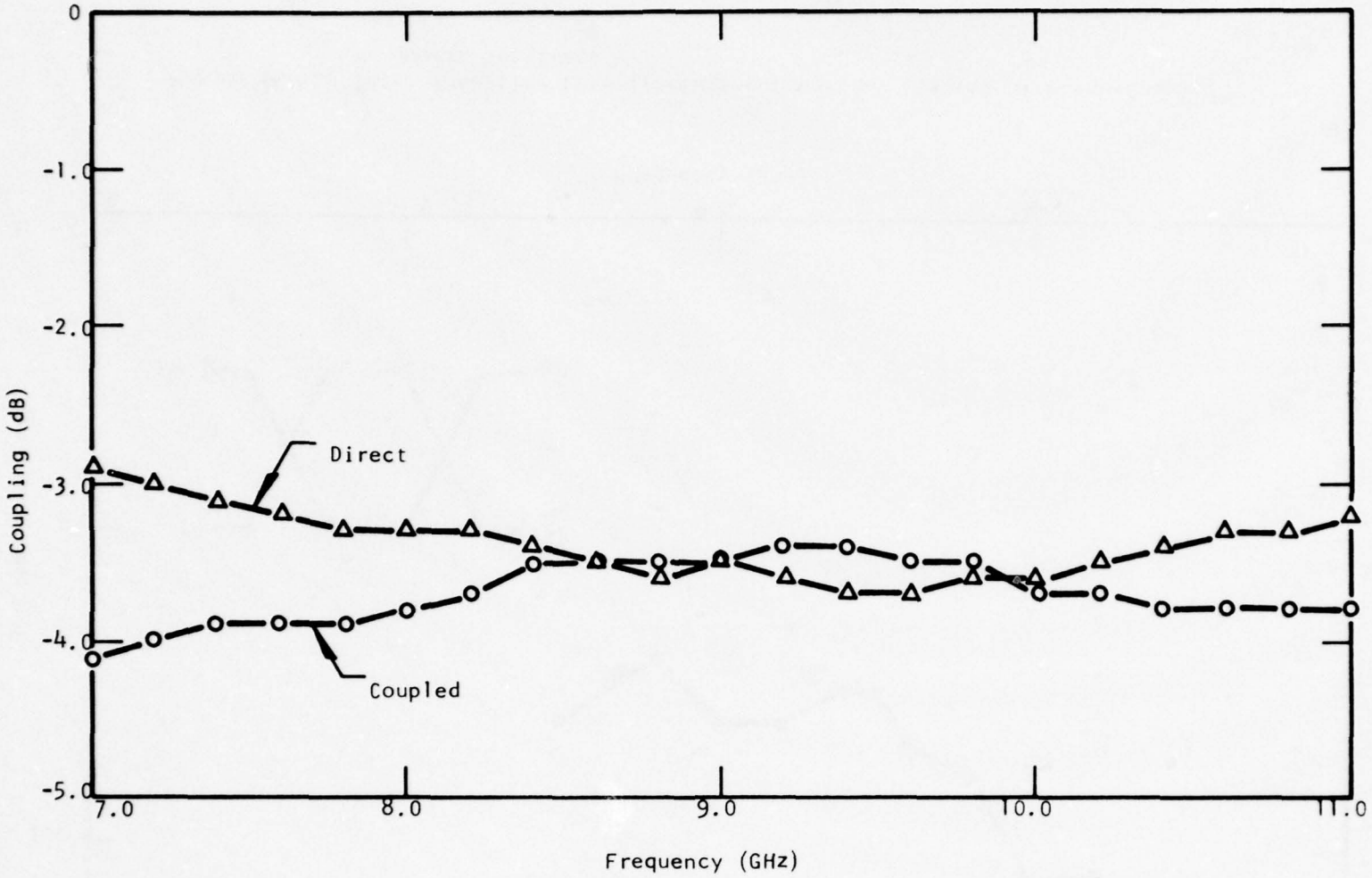


Figure 36(a). Lange Coupler: Coupled and Direct Port Response

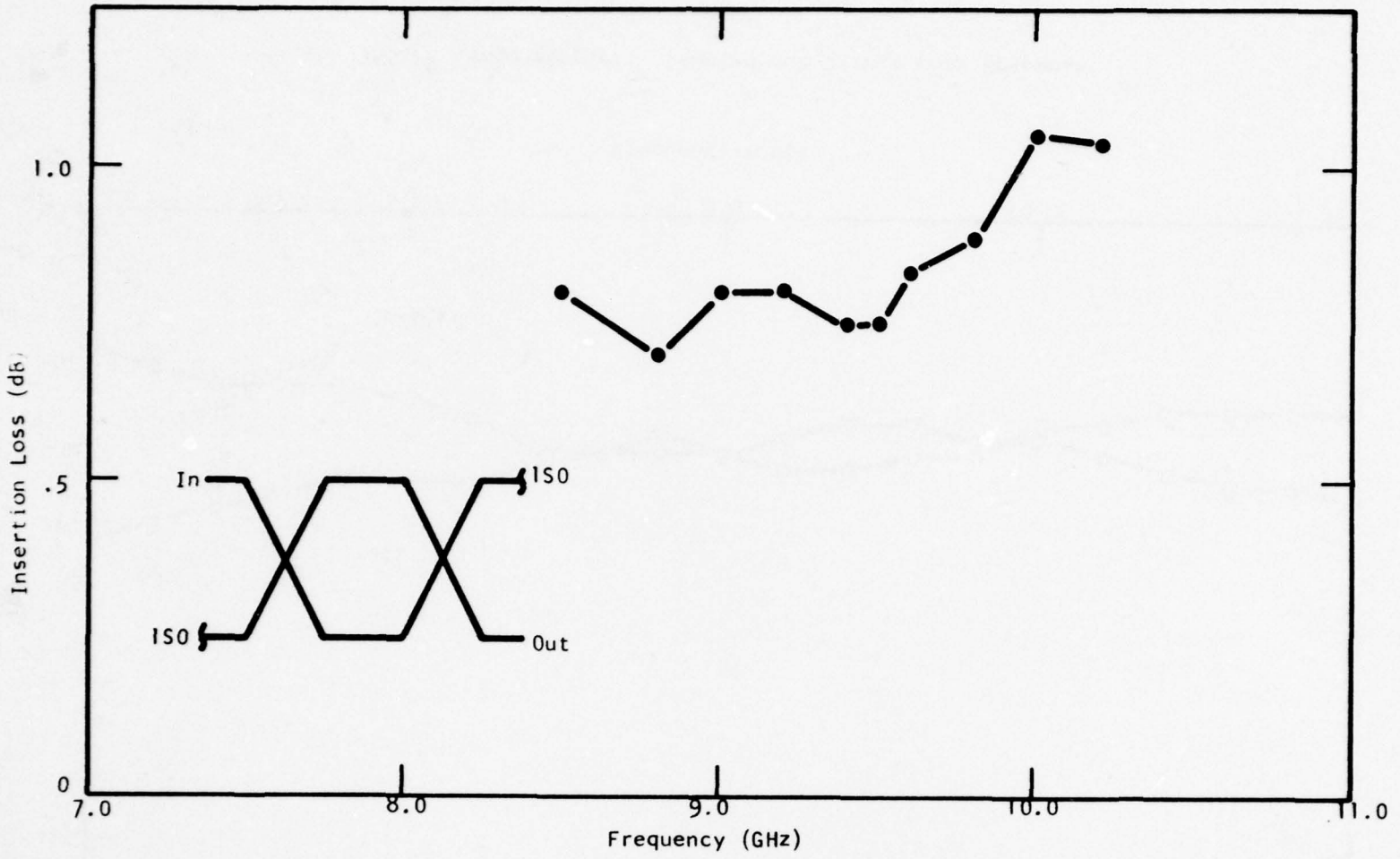


Figure 36(b). Total Insertion Loss (Including Connector Losses) of Lange Coupler on Quartz Substrate

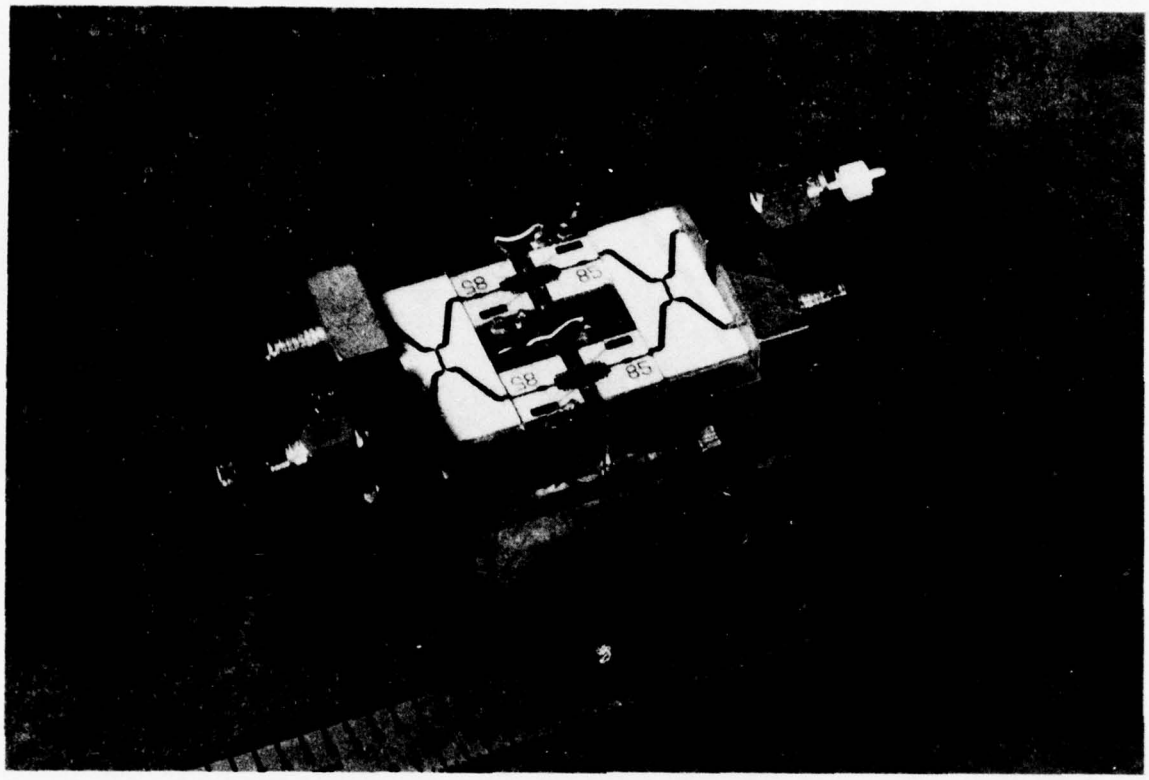


Figure 37. Single-Stage Balanced Amplifier with 3 dB Coupler Fabricated on Alumina Substrates

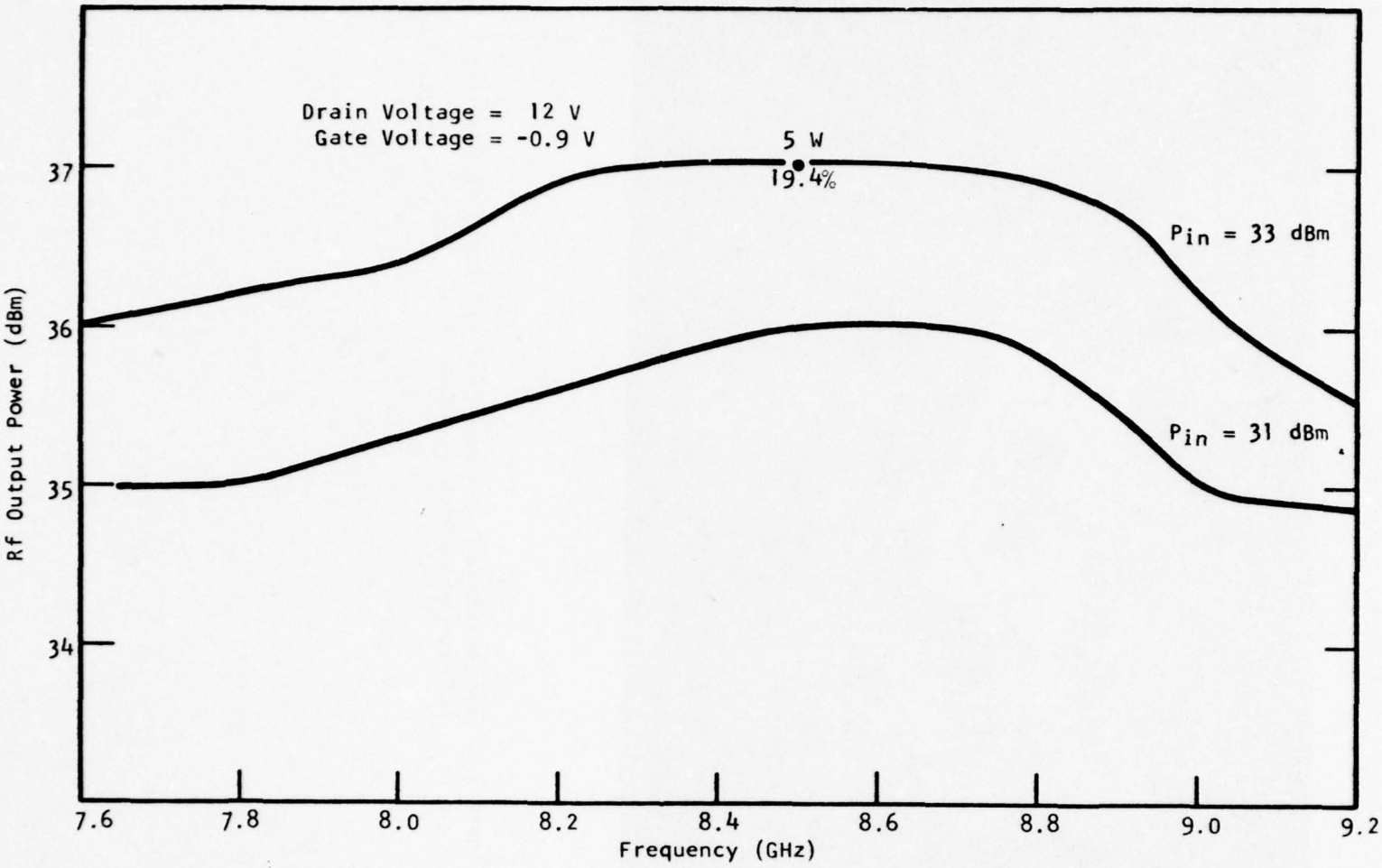


Figure 38. Output Power-Frequency Characteristic of a Single-Stage Balanced FET Amplifier

The balanced amplifier module shown in Figure 38 was obtained by combining two individual amplifier modules, characterized separately, with a pair of 3 dB hybrids. Figure 39 shows a new version of the single-stage balanced amplifier with a 3 dB Lange coupler fabricated on a quartz substrate. To minimize the ground plane and discontinuity problems, both the input/output couplers and the matching circuits were mounted on the same carrier plate. The devices were mounted on gold-plated blocks fitted to a slot in the module housing. A 50 Ω chip resistor was used to terminate the isolation port.

Since the hybrids fabricated on quartz substrates were observed to have lower loss (~ 0.2 to 0.3 dB per hybrid) than those using alumina as substrates, they were used in the final stage design to obtain higher combining efficiencies of the amplifiers. The 4800 μm gate-width FET was chosen for the final stage amplifier instead of the 6400 μm gate width FET originally designed for the output balanced stage on the basis of combining efficiency considerations. While the single-stage, single-ended, 6400 μm FET yields up to 4 W of output power with ~ 4 dB gain in the 7 to 9 GHz range, the gain is not high enough in the 9 to 10 GHz range to be efficiently combined with MIC hybrids. The use of 200 μm gate finger width results in a lower gain than the 150 μm gate finger design. This is due to both amplitude attenuation and phase change along the finger width at higher frequency. Another possible reason for the lower gain is the higher source lead inductance contributed by a larger cell size.

With this integrated balanced amplifier module an output power of 4 W over the 1 dB bandwidth of 1.7 GHz (8.5 to 10.2 GHz) was achieved. An FET with a 4800 μm gate-width device was used in each component amplifier. Figure 40 shows the gain-frequency response. At 9.5 GHz, 4 W was achieved with 4 dB gain and 19% power-added efficiency. The linear gain is 5 dB at 3.1 W output.

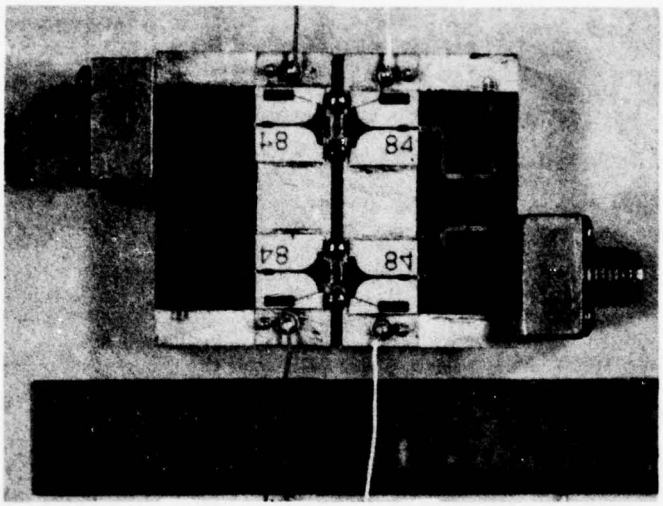


Figure 39. Single-Stage Balanced FET Amplifier Module Using 3 dB Coupler on Quartz Substrate

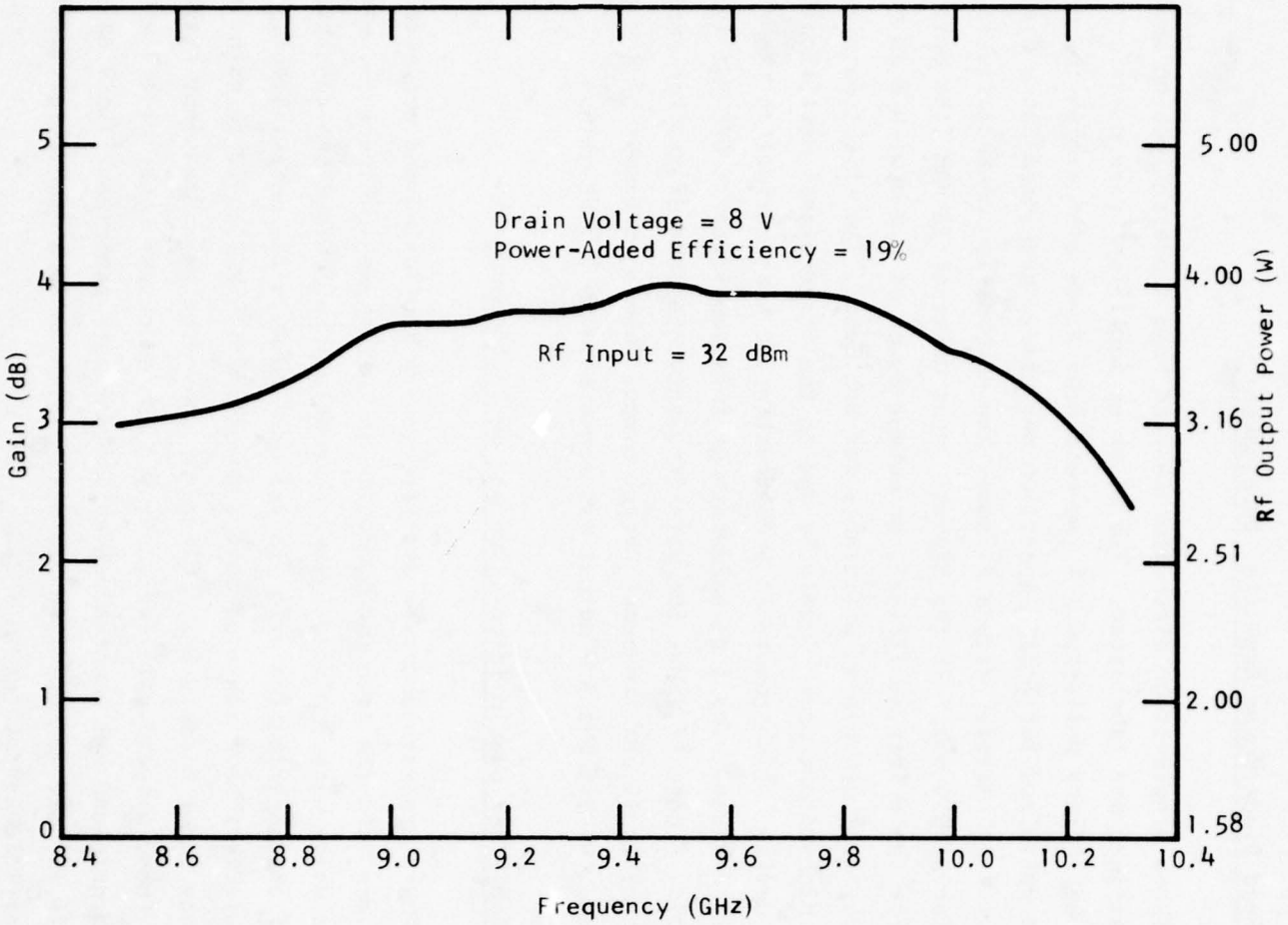


Figure 40. Gain-Frequency Response of a 4 W GaAs FET Amplifier

D. Read Diode Power Amplifier Development

Three single-stage circulator-coupled Read diode reflection amplifiers were designed and fabricated. Two of these amplifiers were used for the two hybrid amplifiers delivered. A two-mesa Read diode with a high-low doping profile optimized for X-band operation was used. Each mesa has a diameter of $\sim$ 150 μm ($\sim$ 6 mils). Figure 41 shows the compression characteristic of one amplifier at 9.5 GHz. At the highest input drive of 32 dBm (the design output power for the driver amplifier), an output power of 6.4 W with 6 dB gain and 21.4% dc-to-rf conversion efficiency was achieved. The slight gain expansion at the high output power levels is due to the large-signal rectification effects of the device, which result in a nonconstant dc bias current as the rf input drive is changed. The 1 dB bandwidth of this amplifier is 600 MHz (9.3 to 9.9 GHz). Figure 42 shows the gain-frequency response of another amplifier. Over the 9 to 10 GHz frequency range, output powers in excess of 4 W can be obtained. At 9.5 GHz 6 W output was achieved with 5.8 dB gain.

E. Amplifier Module Integration and cw Performance

Four three-stage driver amplifiers were fabricated and evaluated. These amplifiers have the same configuration as that shown in Figure 23, except that the end walls were replaced by two removable input/output SMA connectors for ease of characterization prior to integration with the output stage. All the amplifiers have achieved output powers of 1.5 W with 20 dB gain in the frequency range 8 to 10 GHz. Figure 43 shows the gain-frequency response of one of these driver amplifiers. At 9.3 GHz an output power of 1.7 W with 20.3 dB gain and 29% power-added efficiency were achieved. The 1 dB bandwidth is 1.7 GHz (8 to 9.7 GHz). With a bias network incorporated, the power-added efficiency reduces to $\sim$ 25%.

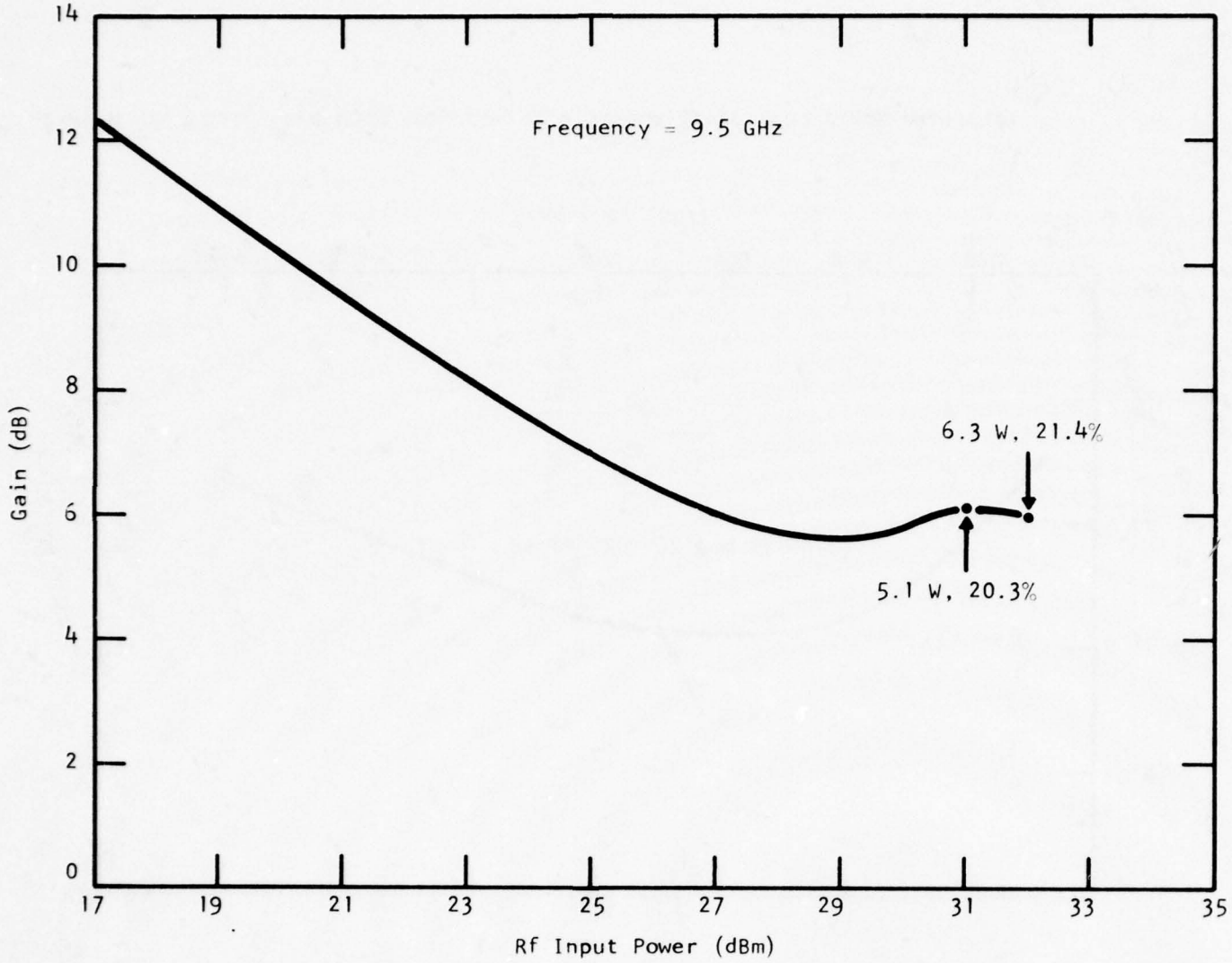


Figure 41. Gain Compression Characteristic of a Single-Stage, Two-Mesa Read Diode Amplifier

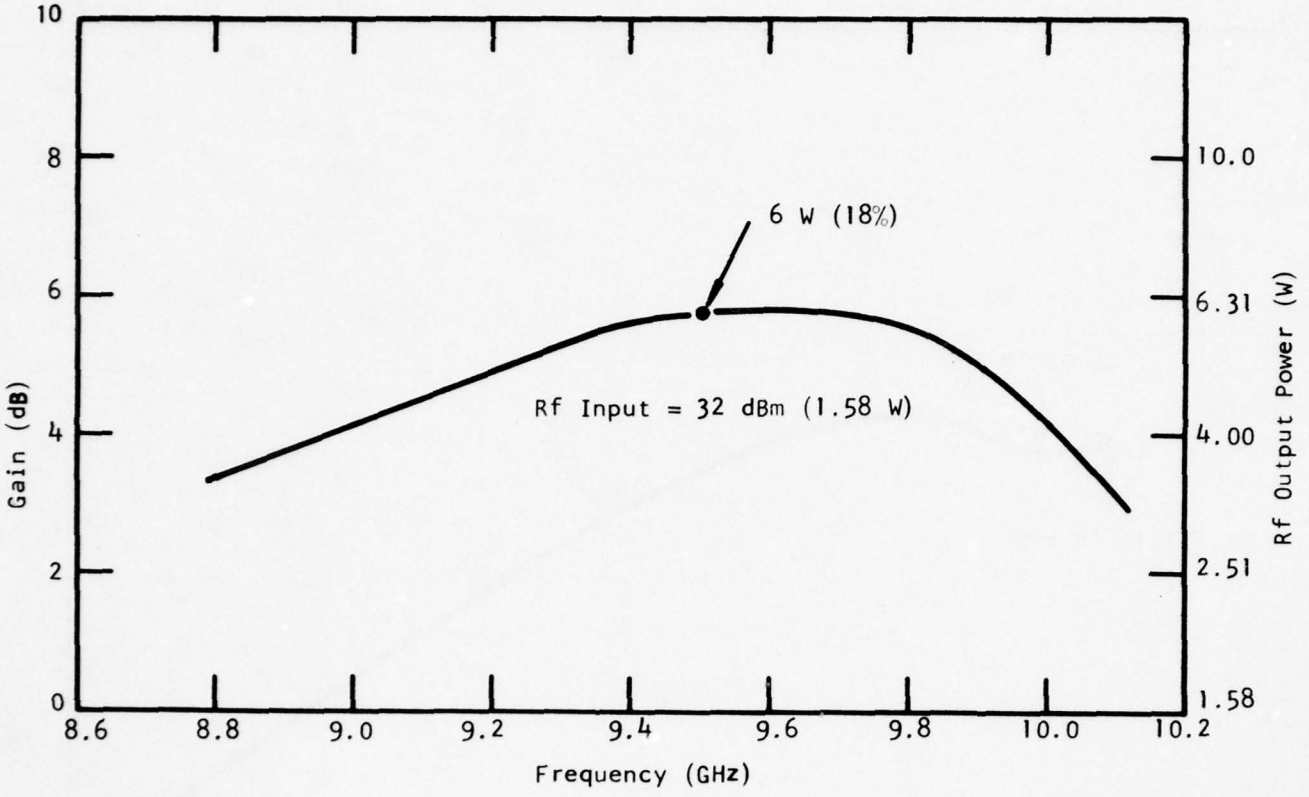


Figure 42. Gain-Frequency Response of a Single-Stage Read Diode Amplifier

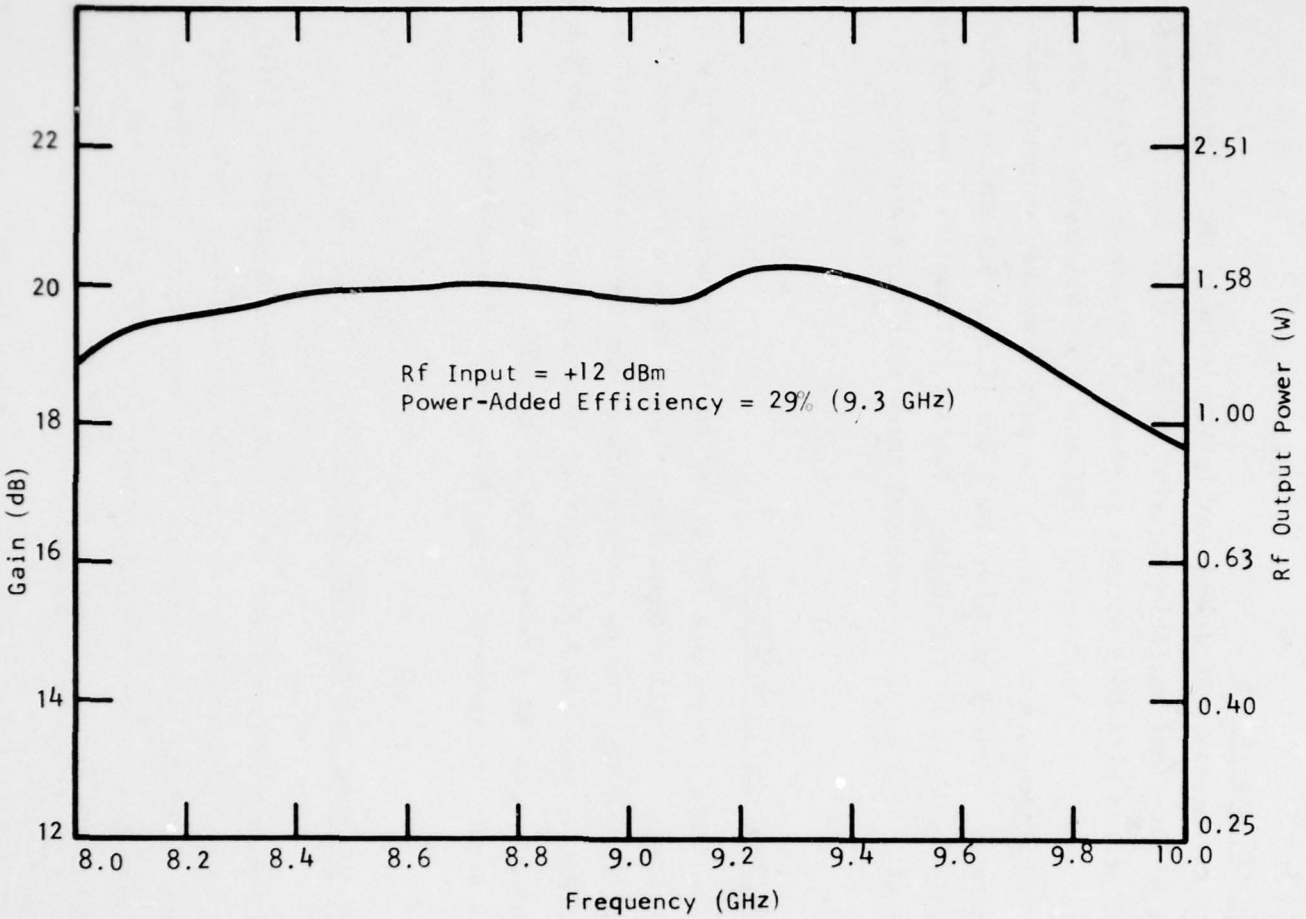


Figure 43. Gain-Frequency Response of a Three-Stage Driver Amplifier

1. All FET Amplifiers

The three-stage FET driver was integrated with the balanced FET output stage in the final amplifier housing as shown in Figure 44. An all FET amplifier module with bias network is shown in Figure 45. The highest power achieved with the integrated all FET amplifier module was 4 W with 24 dB gain and 20% efficiency at 9.5 GHz. The gain-frequency response curve is shown in Figure 46. A 1 dB bandwidth of 1 GHz (8.9 to 9.9 GHz) was obtained. The linear gain is 28 dB at 3 W output. Two all FET amplifier modules were delivered to NRL. The cw performances of these amplifiers are shown in Figure 47.

2. FET/Read Hybrid Amplifier

Two of the three-stage FET driver amplifiers were cascaded with Read diode output stages for hybrid operation. Figure 48 is a photograph of the hybrid amplifier module. The cw performance of the two hybrid amplifiers delivered to NRL is shown in Figure 49. It is shown that, at 9.5 to 9.6 GHz, 5 W of output power can be obtained with 25 dB gain. The power-added efficiencies are in the range of 18 to 19%. The 1 dB bandwidth is on the order of 600 MHz.

F. Pulsed rf Characterization of Amplifiers

Pulse measurements were made on FET amplifiers to determine their suitability in phased-array radar applications. Amplitude droop, phase ramp, AM-toPM conversion, and phase sensitivity to power supply variations were measured extensively on both single and multistage FET amplifiers. The measurement results are described in this section.

Figure 50 shows a block diagram of the basic measuring system suitable for pulsed and cw operation. A tunable Gunn oscillator capable of operating over the frequency band from 8.8 to 10.2 GHz provides frequency control of

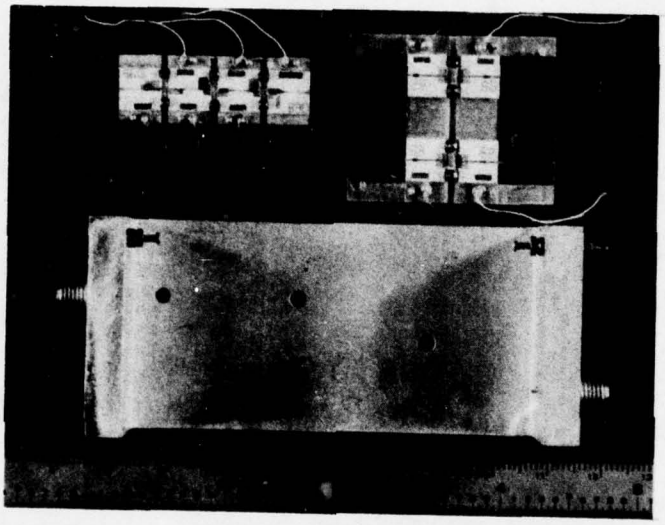


Figure 44. Individual GaAs FET Amplifier Modules Prior to Integration

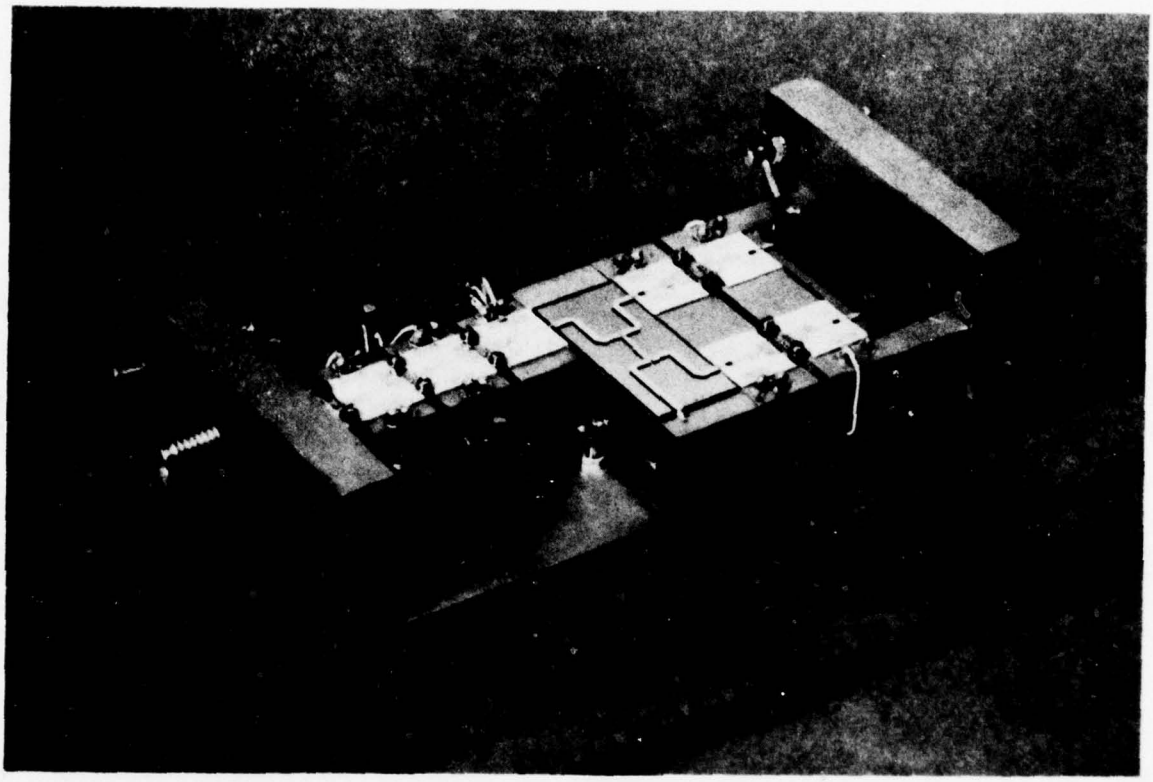


Figure 45. A Four-Stage GaAs FET Amplifier Module

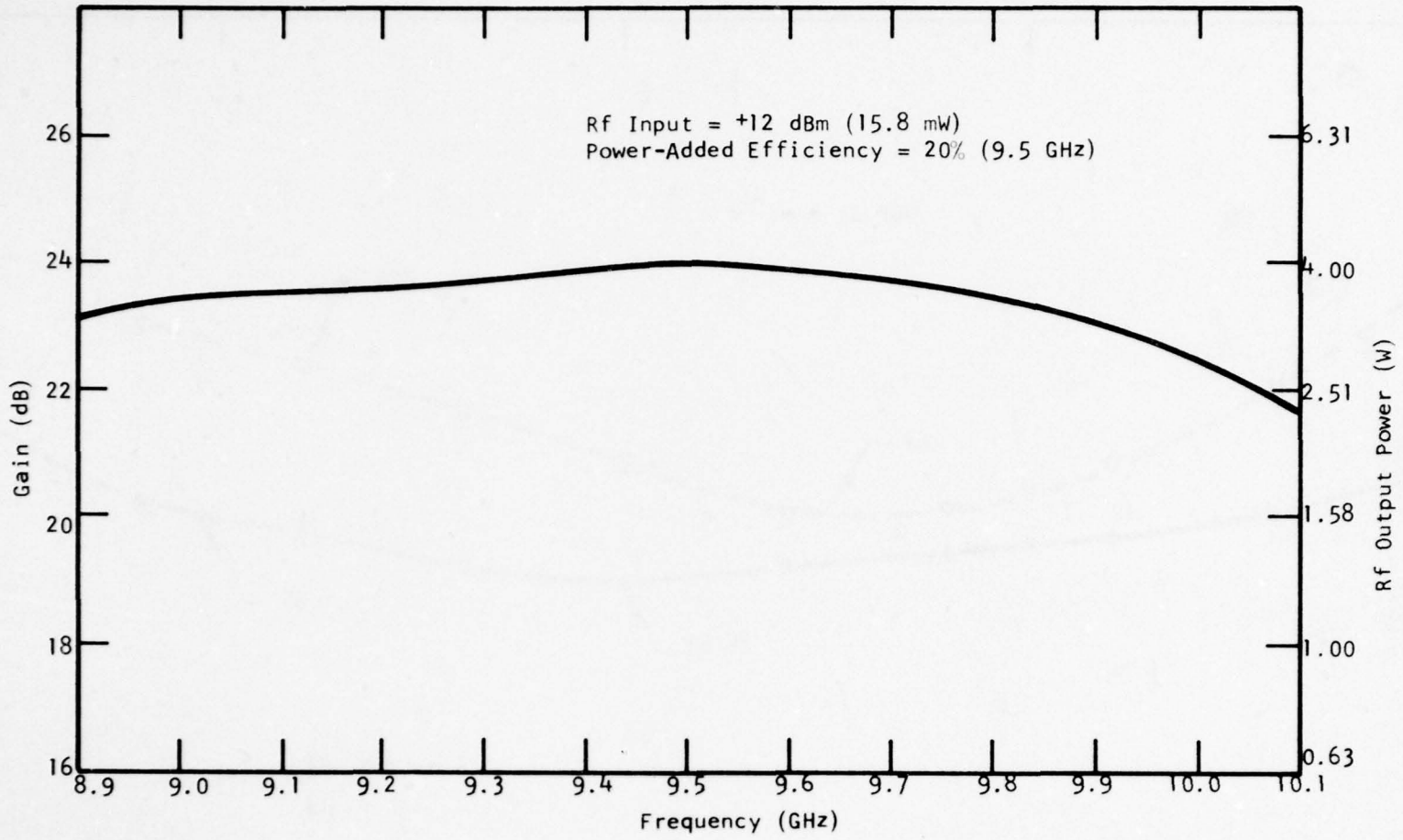


Figure 46. Performance of a 4-W GaAs FET Amplifier

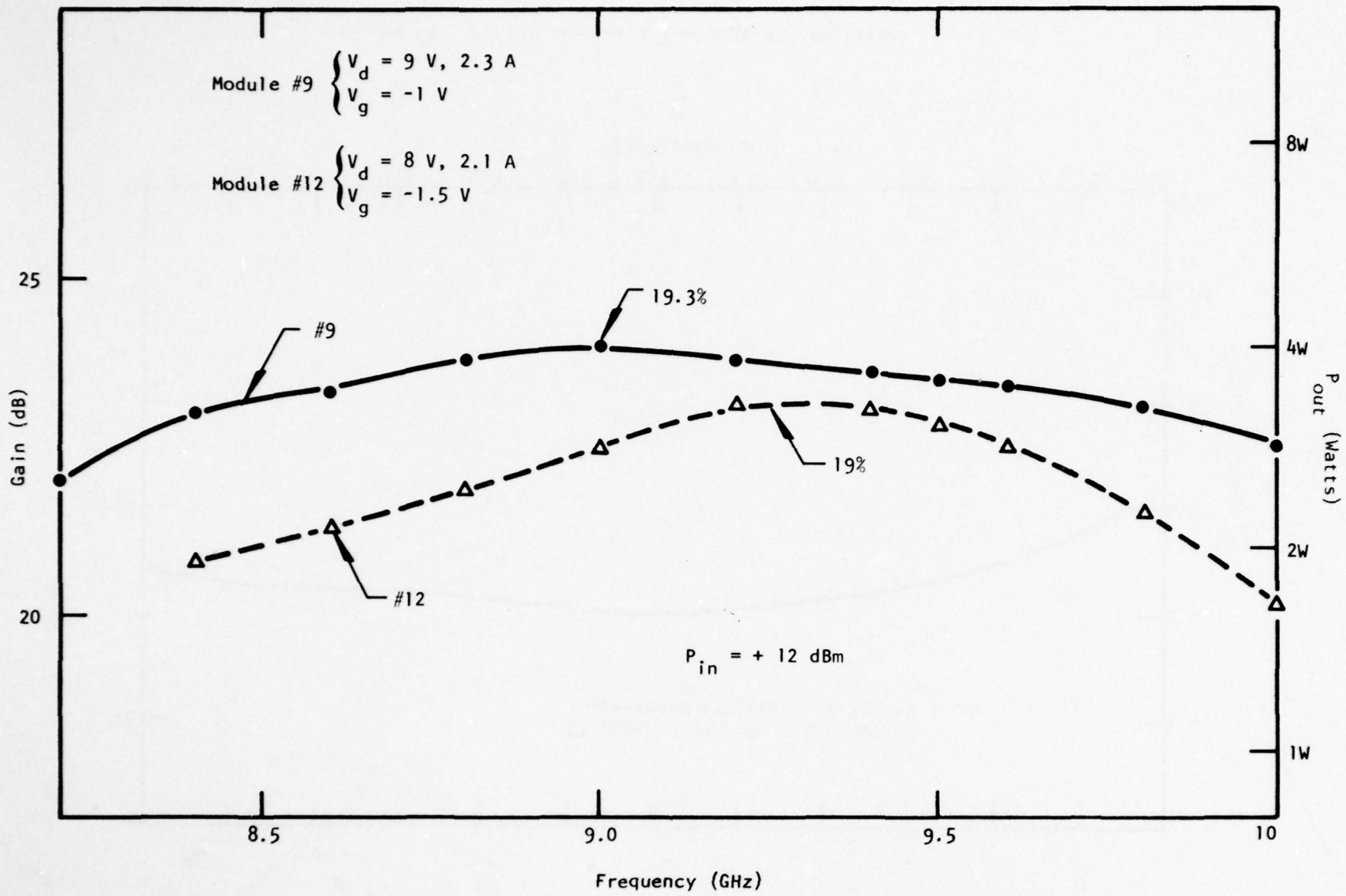


Figure 47 CW Performance of the Two All-FET Amplifier Modules Delivered to NRL

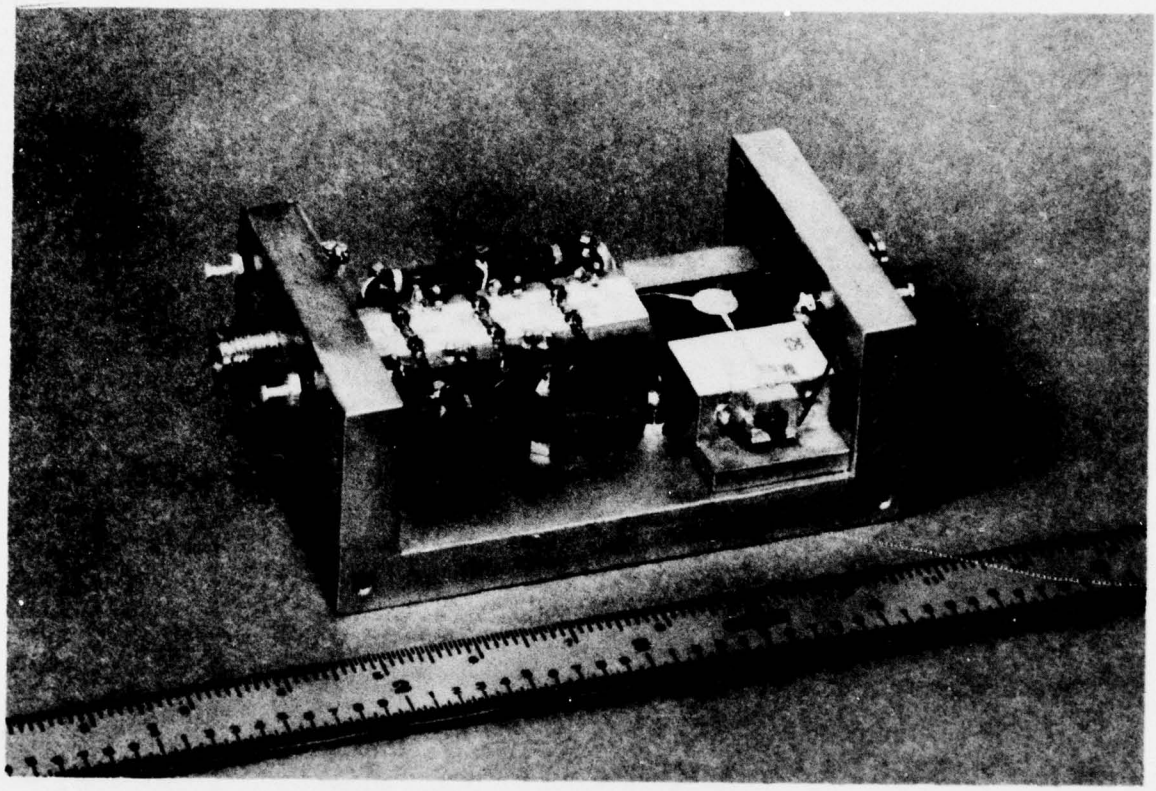


Figure 48. A FET/Read Hybrid Amplifier Module

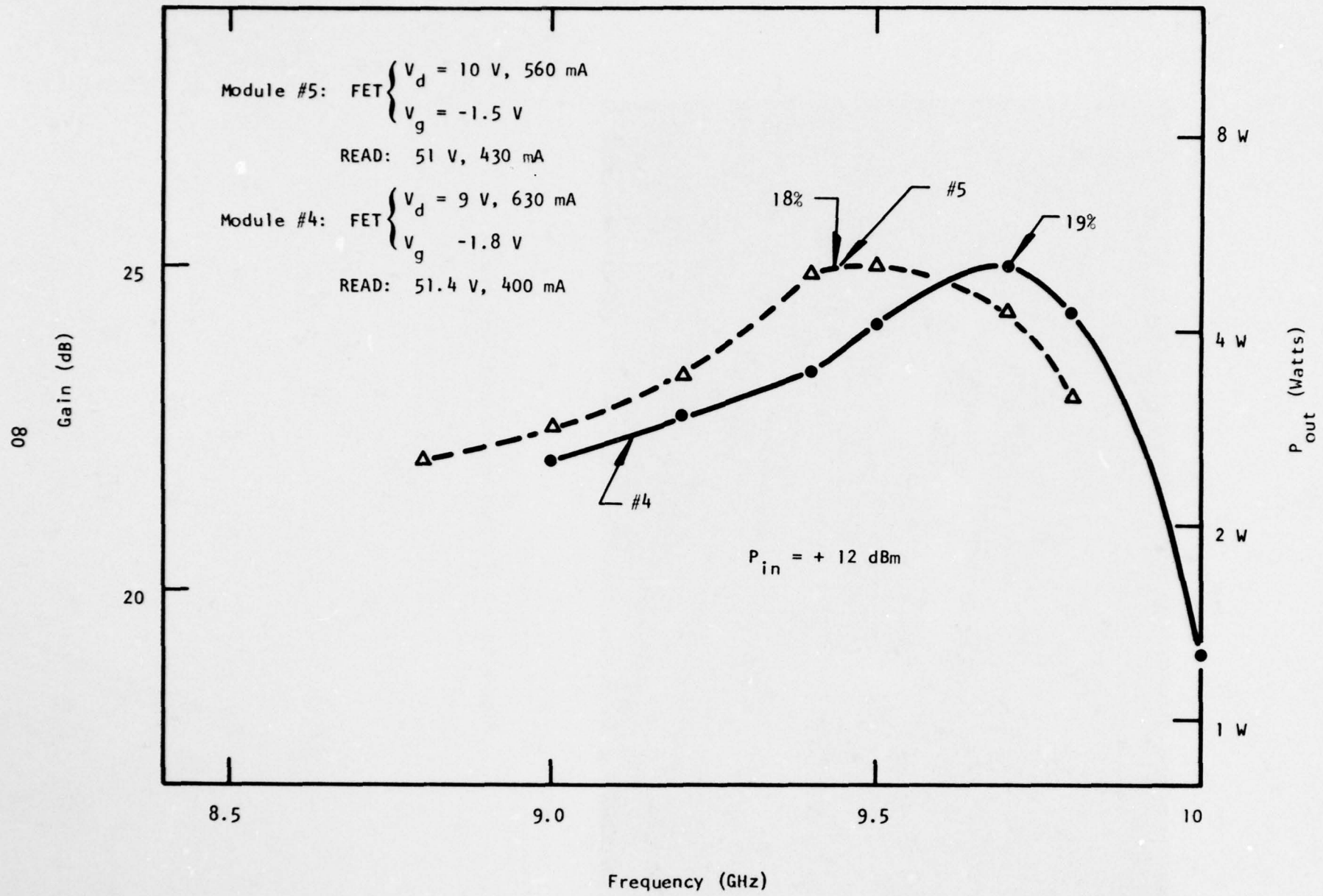


Figure 49 CW Performance of the Two FET/Read Hybrid Amplifiers Delivered to NRL

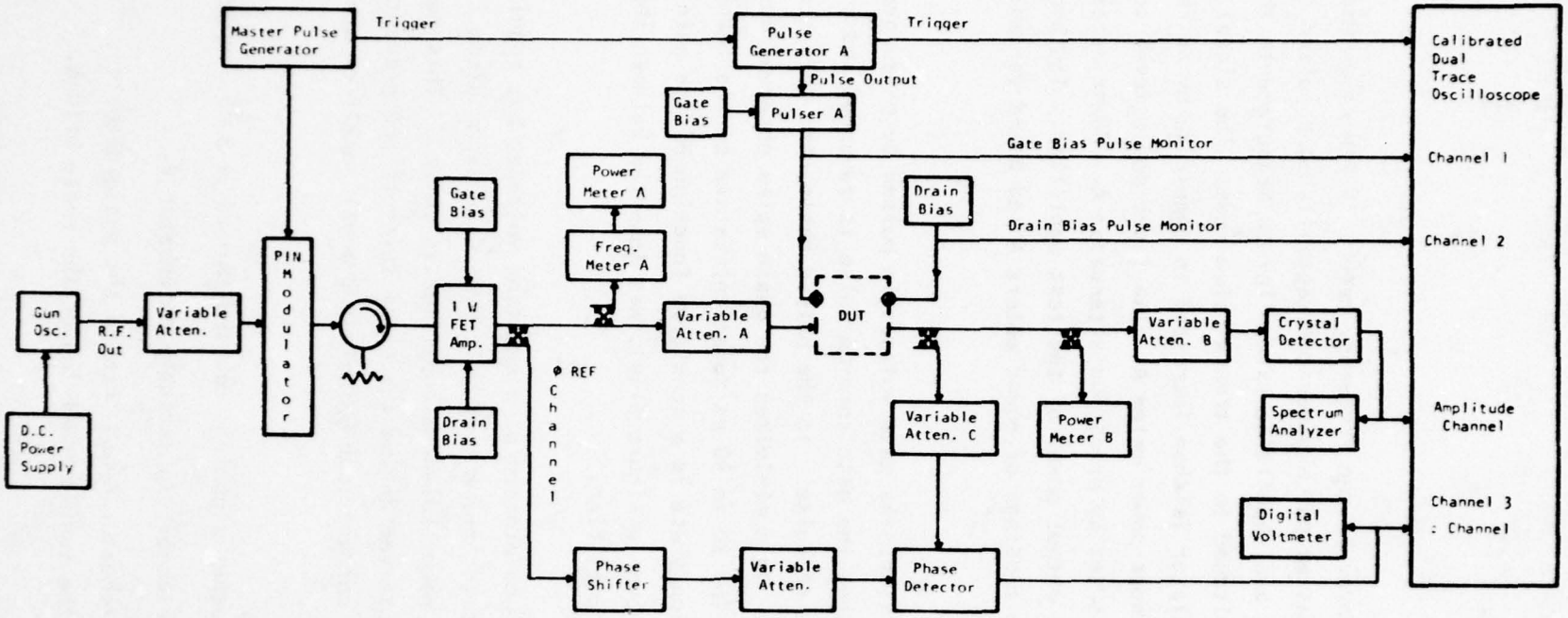


Figure 50 Block Diagram of Pulse Test Set-Up for GaAs FET Amplifiers

the test signal, monitored by the frequency meter. A PIN diode modulator, in conjunction with the master pulse generator, establishes a pulsed rf signal of controlled duration and repetition rate. For cw measurements the PIN modulator is simply switched to the transmission mode. The signal from the output of the PIN modulator is then increased in magnitude by an FET amplifier and monitored by the input power meter A. The input power level to the amplifier under test is set by precision attenuator A. Power meter B is calibrated to read the output power of the test amplifier. The amplifier gain is determined from the readings of power meters A and B and variable attenuator A.

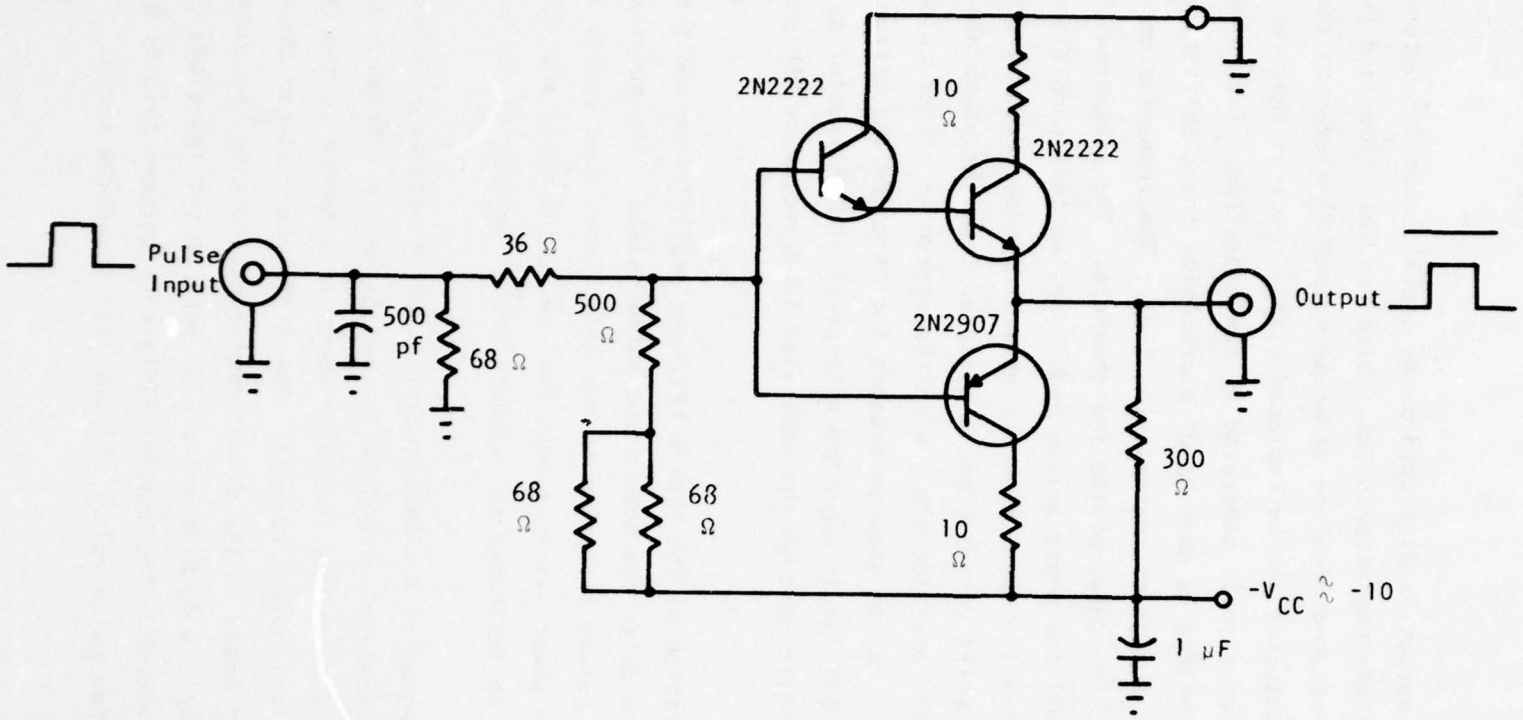
For pulsed operation, the gate voltage is pulsed by pulse generator A and is adjusted such that the gate turn-on pulse is advanced and turn-off delayed with respect to the rf pulse. In the pulsed tests, the FETs are biased at pinch-off for standby. This minimizes the phase spike observed during the turn-on/off transient (of 30 to 40 ns duration) caused by the changing gate voltage, since insertion phase is a sensitive function of the gate voltage. A simple pulser, as shown in Figure 51(a), was inserted between the pulse generator and the FET amplifier.

The drain bias is maintained at a constant voltage, but requires an additional large capacitor and a $\sim$ 10 volt breakdown Zener diode in the bias circuit when the high power balanced amplifier is pulsed. This reduces the drain voltage spike observed during the pulse turn-off and prevents the high power high drain current (approximately 2 amps) amplifier stage from failure.

The amplifier output signal is coupled through a 3 dB coupler to:

(a) A crystal detector via variable attenuator B,

(b) Variable attenuator C and then to the phase detector, completing the test channel leg of the phase bridge.



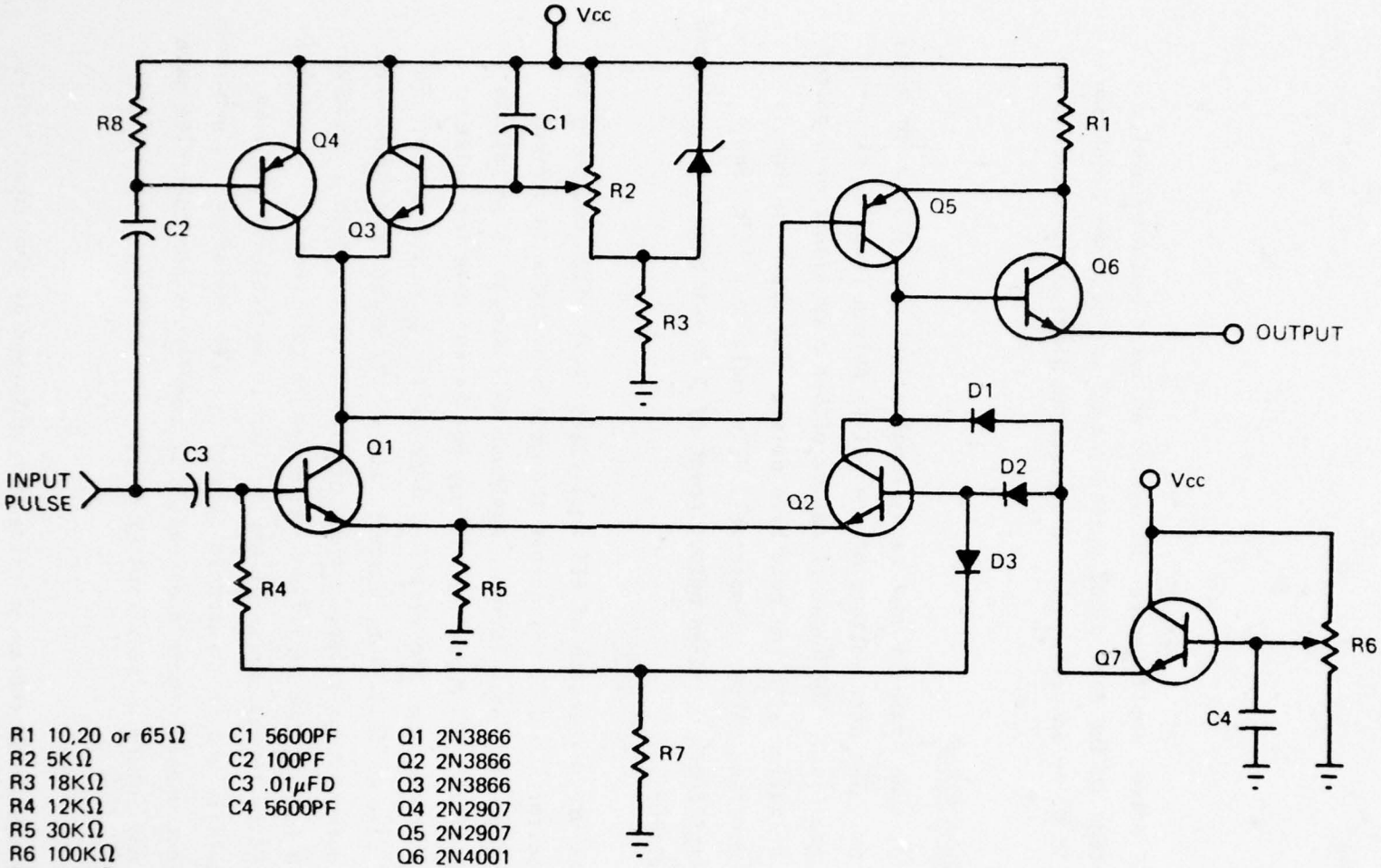
Gate Pulsing Circuit (All Resistors are 1/2 Watt)

Figure 51(a) Gate Pulsing Circuit

The crystal detector output is displayed on an oscilloscope for determination of the pulse rf amplitude characteristics. Rise and fall times and pulse amplitude droop are measured from the detector output displayed on the oscilloscope. The crystal detector can be replaced with a spectrum analyzer for the measurement of spurious signals generated by the amplifier. The reference channel of the phase bridge is made up of a precision phase shifter, a level set attenuator, and a length of transmission line. The transmission line is used to equalize the time delay of the two channels. The precision phase shifter is used to null the phase bridge under varying test conditions and hence provides the relative phase data for phase response characterization. The intrapulse phase shift versus time is measured from the phase detector output displayed on the oscilloscope. With the system in either cw or pulsed mode, the phase bridge can be used to measure the AM-to-PM conversion. The input power to the amplifier is adjusted with precision attenuator A, while any change of phase shift through the amplifier is detected on the phase bridge.

For pulsed operation of the hybrid FET/Read amplifier an additional pulse modulator was used to pulse the Read diode output stage. The pulse modulator required to perform pulsed operation of the Read diodes must supply constant current with minimum power dissipation. Fast switching speed and low dc current drain are also desirable to increase the efficiency of the modulator.

A schematic diagram of a constant-current pulse modulator is shown in Figure 51(b). A pulse-forming network is used to gate a reference voltage to the control amplifier during the pulse which is compared to the feedback signal generated by the output current. The difference between these two signals generates an input to the driver amplifier, forcing the output current to the required value. A dc bias network is used to set the diode dc voltage to a value near breakdown. The smaller difference between this dc bias voltage and the required diode pulse voltage allows fast switching times.



R1 10,20 or 65Ω
R2 5KΩ
R3 18KΩ
R4 12KΩ
R5 30KΩ
R6 100KΩ
R7 100KΩ
R8 2.4KΩ

C1 5600PF
C2 100PF
C3 .01μFD
C4 5600PF

Q1 2N3866
Q2 2N3866
Q3 2N3866
Q4 2N2907
Q5 2N2907
Q6 2N4001
Q7 2N4001

181859

Figure 51(b). Schematic Diagram of Constant Current Pulsed Modulator

The all FET driver amplifier can be pulsed as described previously. The dc bias voltage to the Read diode pulser can be set near the breakdown voltage (20 to 30 V) by adjusting R6. The required diode current can be set by R2.

1. Amplitude Droop

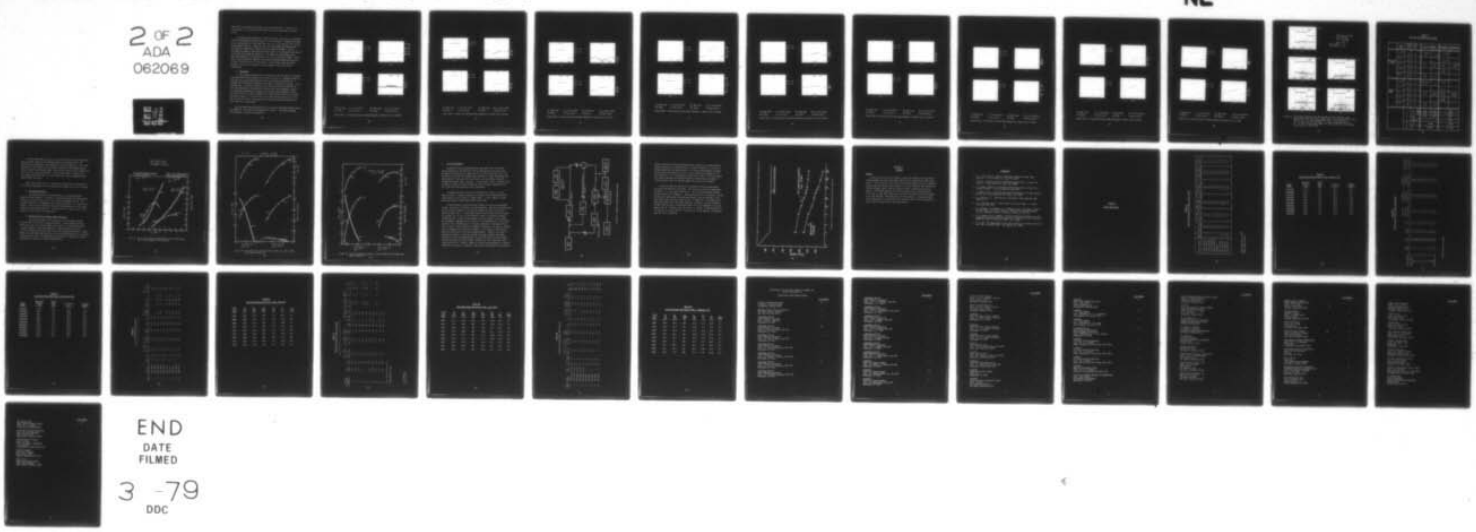
The amplitude droop in most cases remains less than 0.5 dB for pulse widths up to 50 μs. The gate voltage of the FET is pulsed from the pinch-off to the nominal gate bias. The input rf can be either a cw signal or a pulsed signal in synchronization with the gate bias pulse. The drain voltage is maintained at a constant value. Single-cell FETs, multicell FETs, and multistage FET amplifiers up to an output power of 3 to 4 W have been evaluated under pulse conditions.

In the bias circuit design of FET amplifiers it is often necessary to use a shunt capacitor ($\sim$ 0.01 μF) across the gate bias choke to prevent build-up of low-frequency oscillation. Although this scheme is satisfactory for cw operation of the FET amplifier, it may not be suitable for pulse operation, since it degrades the rise/fall time of the gate bias pulse. To preserve a fast rise or fall time, however, the rf pulse can be delayed with respect to the gate voltage pulse. Unless otherwise stated, such a practice has been used in testing the amplifiers described in this report. Although a chip resistor (50 to 100 Ω) can sometimes be used in series with the bias circuit for stability and fast response time of the FET amplifier, it generates a debiasing effect under large-signal operating conditions due to finite gate current flow. Any future pulse circuitry design must address these critical problems.

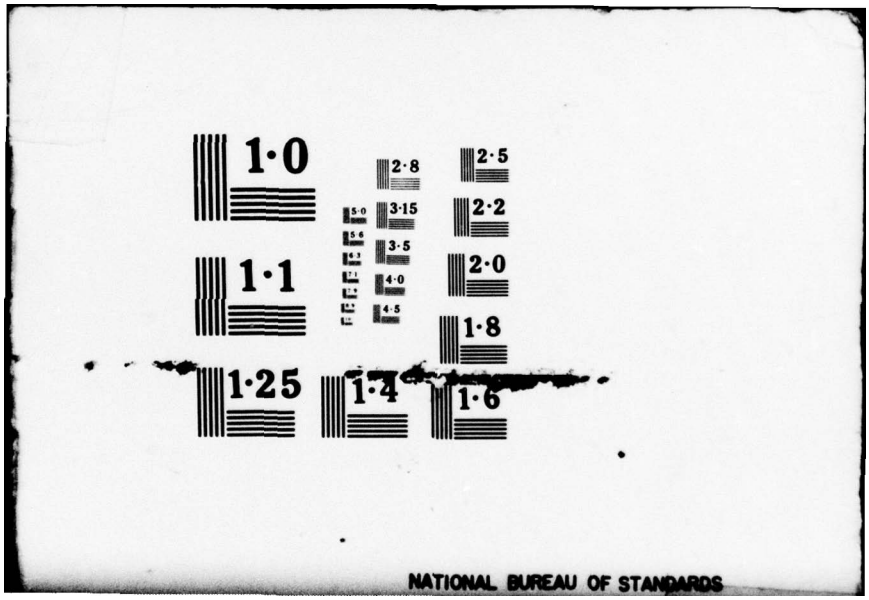
The amplitude droop characteristics were obtained by photographically recording the oscilloscope display made by the crystal detector. Photographs were obtained for multistage, 3 to 4 W all FET amplifiers and 5 W hybrid

AD-A062 069 TEXAS INSTRUMENTS INC DALLAS CENTRAL RESEARCH LABS F/G 9/5
X-BAND SOLID STATE MODULE.(U)
OCT 78 W R WISSEMAN, F H DOERBECK N00173-76-C-0384
UNCLASSIFIED TI-08-77-48-F NL

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NATIONAL BUREAU OF STANDARDS

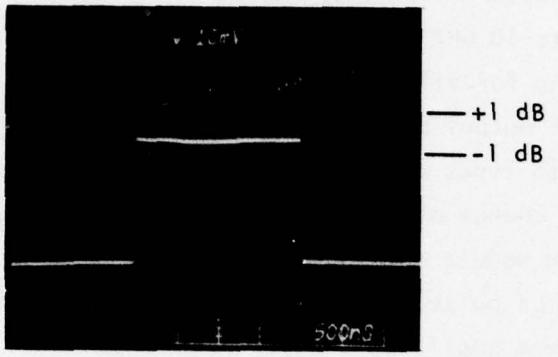
amplifiers (two modules each) under two pulsing conditions: one with 2 μs pulse width, 1% duty cycle and the other with 20 μs pulse width, 10% duty cycle.

All modules were operated at 12 dBm input power level and at frequencies near the band edges and at band center (9 to 10 GHz B.W.). Figures 52 through 55 show the detected rf pulse and phase ramp for all FET modules (#9, 12) and hybrid modules (#5, 4). Total variation of output power and phase within the pulse are summarized in Table 5 for both types of modules. For all FET amplifier modules, the worst amplitude change of 1.2 dB occurred for 20 μs pulse width at 9.5 GHz for module #12. For module #9, the maximum pulse amplitude change of 0.7 dB occurred for 20 μs pulse width at 9.5 GHz. In the case of hybrid amplifier modules, the maximum amplitude change observed was 2.2 dB at 9.2 GHz for 20 μs pulse width. In most cases, amplitude droop exceeded 1 dB for hybrid modules for the frequencies and pulse widths investigated.

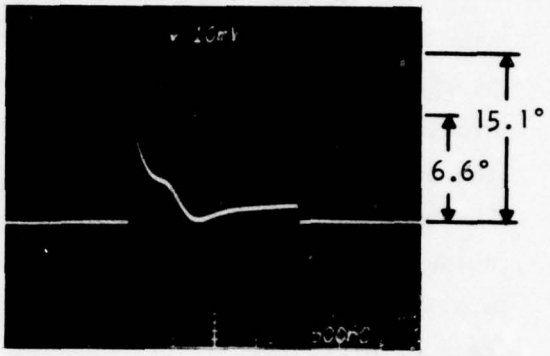
2. Phase Ramp

The intrapulse phase shift was measured to be less than 2° for single-stage amplifiers and for maximum pulse width up to 50 μs. The pulse scheme is such that the turn-on gate pulse (the FETs were biased at pinch-off for standby) can be advanced or delayed with respect to the input rf pulse. It is observed that, to minimize the phase spike during the turn-on transient (of 30 to 40 ns duration), the gate turn-on pulse needs to be advanced. Figure 56 illustrates the effects of changing the relative pulse widths of the rf and gate pulses on the phase transient for a 300 μm gate width FET at 9.5 GHz. From these figures, it is clear that, to minimize the phase transient during the rise and fall times of the gate pulse, the gate pulse width needs to be wider than the rf pulse width.

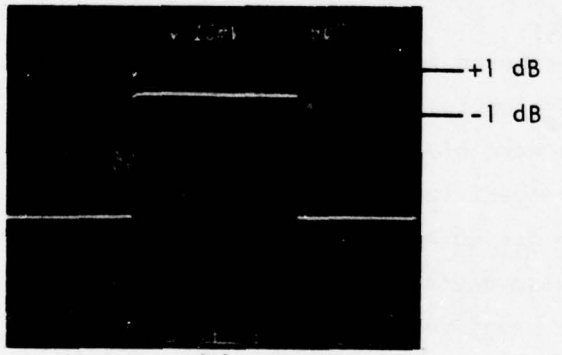
The intrapulse phase characteristics of the four deliverable modules were also measured. The results are summarized in Table 5. The phase responses are displayed in Figures 52 through 55.



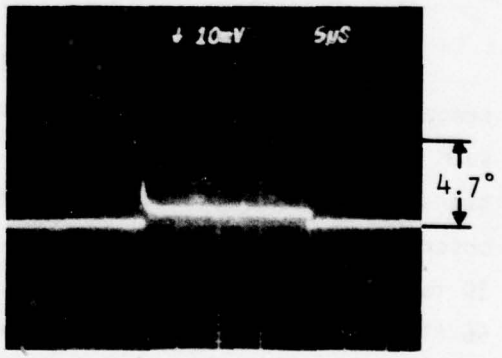
(1)



(2)



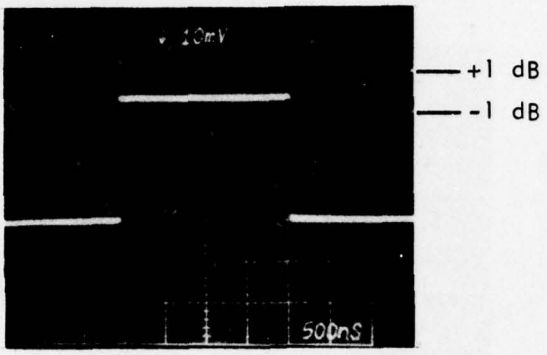
(3)



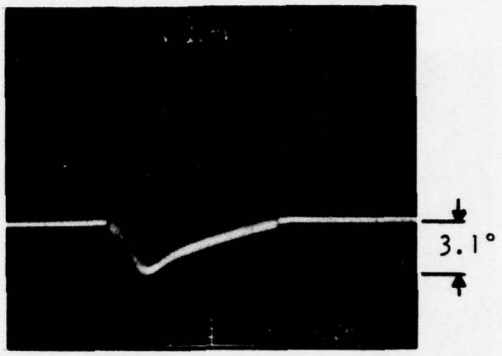
(4)

(1) Amplitude	2 μs Pulse Width	(3) Amplitude	20 μs Pulse Width
(2) Phase	1% Duty Cycle	(4) Phase	10% Duty Cycle

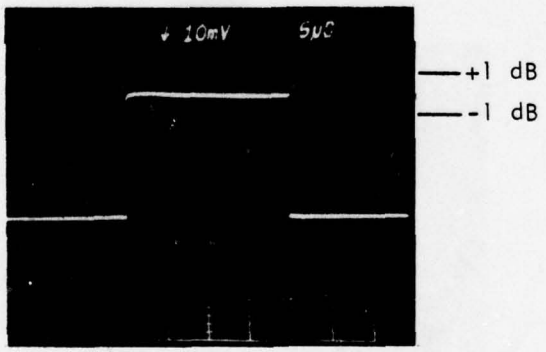
Figure 52(a). Pulsed Amplitude and Phase Response of Module #9 at 9.145 GHz



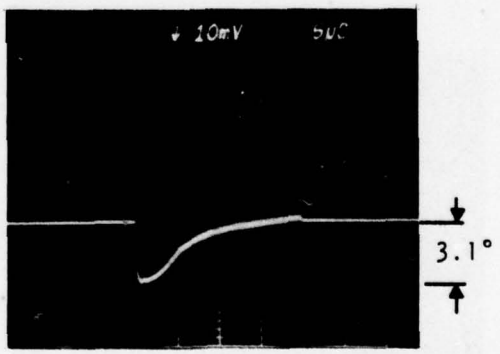
(1)



(2)



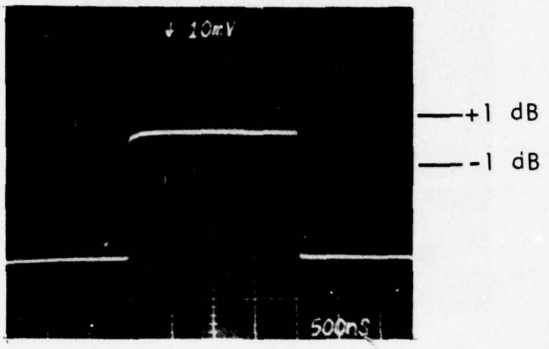
(3)



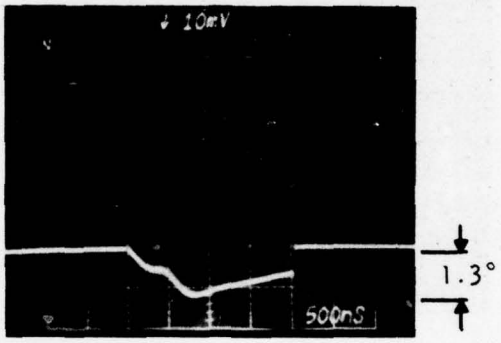
(4)

(1) Amplitude	2 μs pulse width	(3) Amplitude	20 μs pulse width
(2) Phase	1% Duty Cycle	(4) Phase	10% Duty Cycle

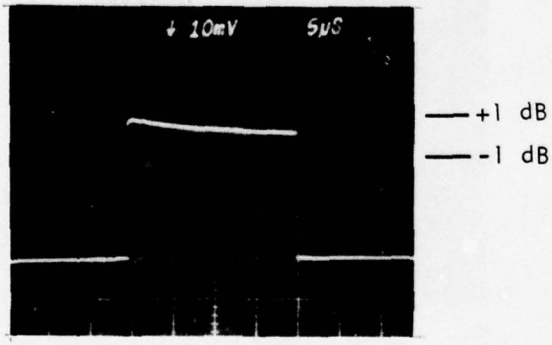
Figure 52(b). Pulsed Amplitude and Phase Response of Module #9 at 9.5 GHz



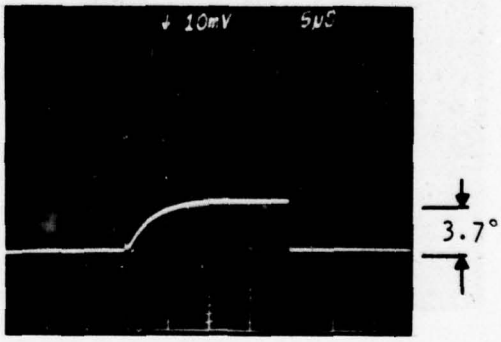
(1)



(2)



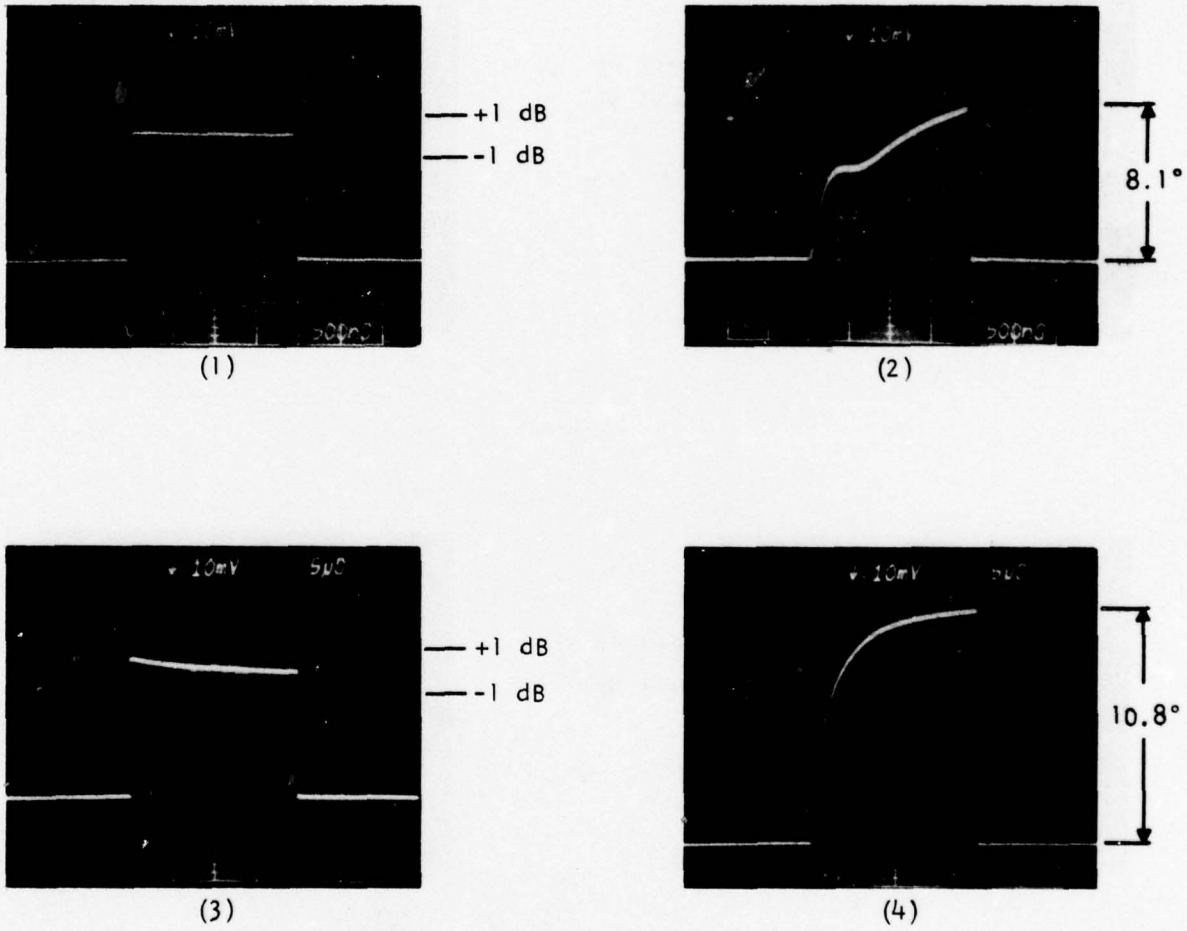
(3)



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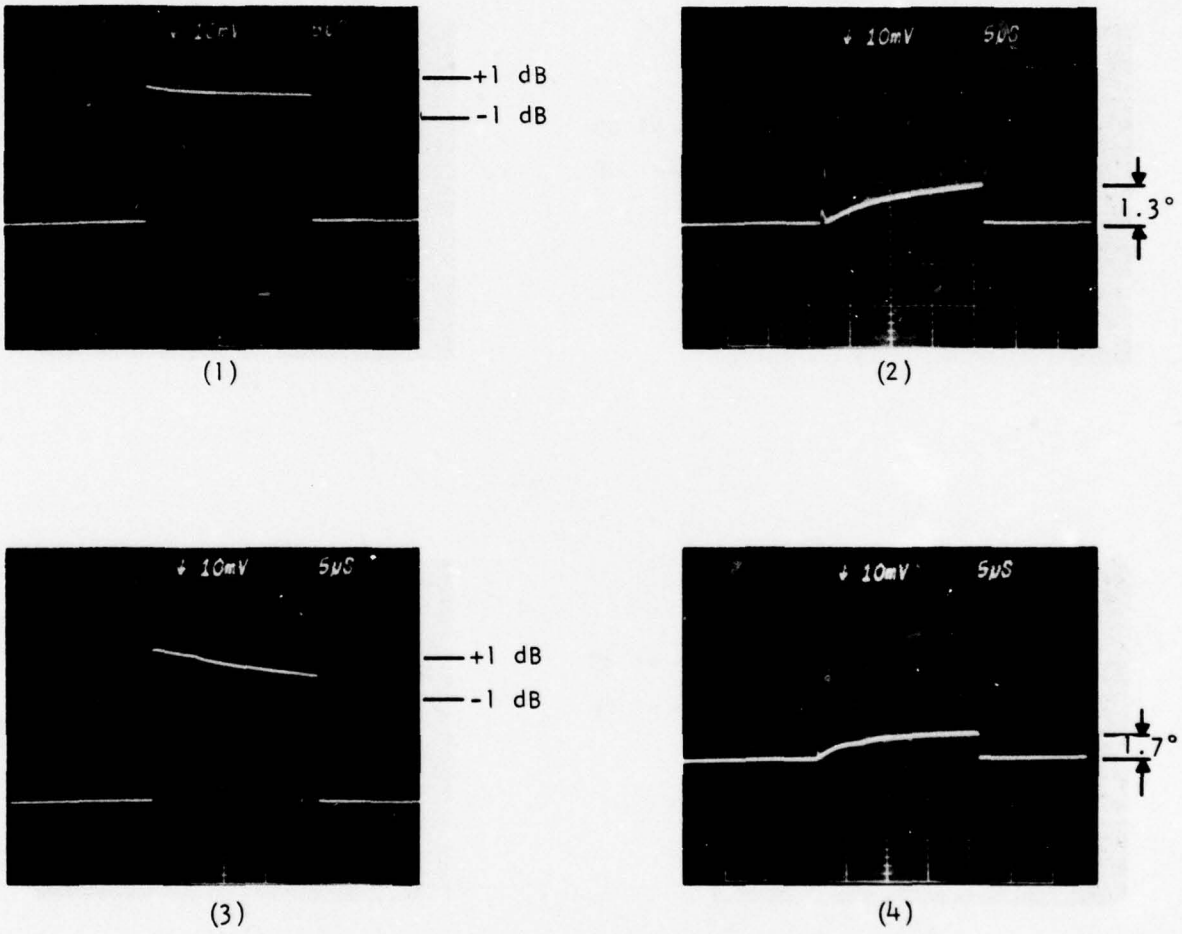
(1) Amplitude	2 μs Pulse Width	(3) Amplitude	20 μs Pulse Width
(2) Phase	1% Duty Cycle	(4) Pulse	10% Duty Cycle

Figure 52(c). Pulsed Amplitude and Phase Response of Module #9 at 10 GHz



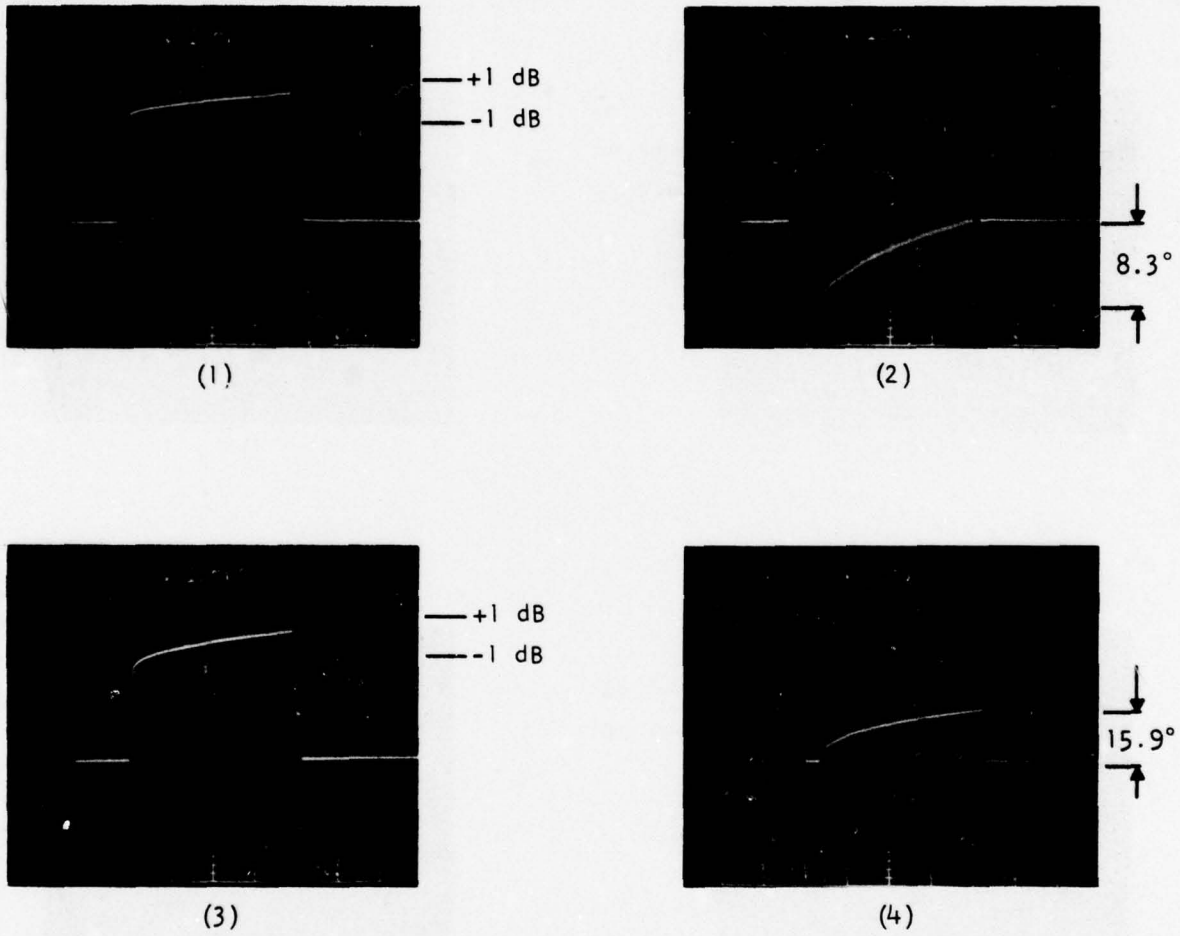
(1) Amplitude	2 μs Pulse Width	(3) Amplitude	20 μs Pulse Width
(2) Phase	1% Duty Cycle	(4) Phase	10% Duty Cycle

Figure 53(a). Pulsed Amplitude and Phase Response of Module #12 at 9.5 GHz



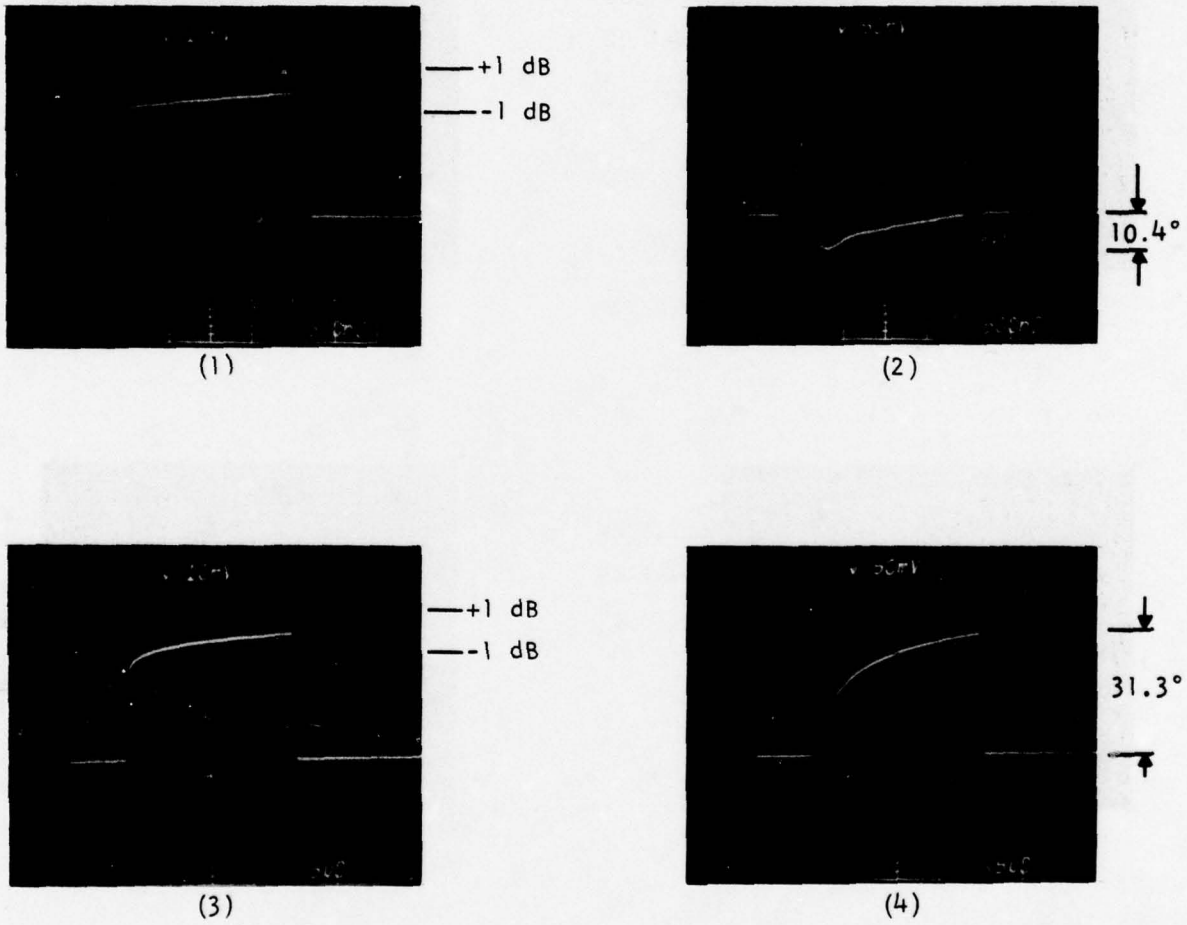
(1) Amplitude	2 μs Pulse Width	(3) Amplitude	20 μs Pulse Width
(2) Phase	1% Duty Cycle	(4) Phase	10% Duty Cycle

Figure 53(b). Pulsed Amplitude and Phase Response of Module #13 at 9.145 GHz



(1) Amplitude	2 μs Pulse Width	(3) Amplitude	20 μs Pulse Width
(2) Phase	1% Duty Cycle	(4) Phase	10% Duty Cycle

Figure 54(a). Pulsed Amplitude and Phase Response of Module #5 at 9.145 GHz

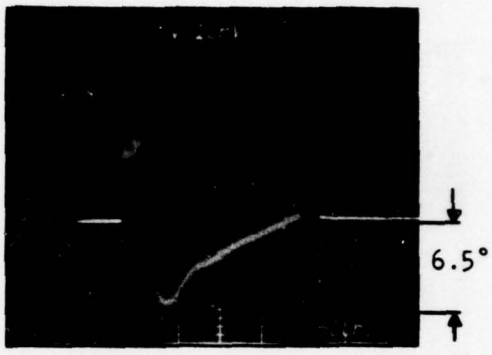


(1) Amplitude	2 μs Pulse Width	(3) Amplitude	20 μs Pulse Width
(2) Phase	1% Duty Cycle	(4) Phase	10% Duty Cycle

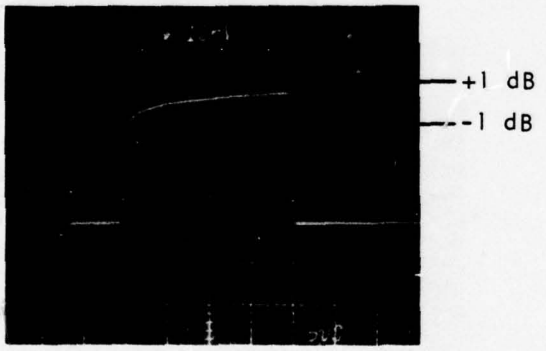
Figure 54(b). Pulsed Amplitude and Phase Response of Module #5 at 9.5 GHz



(1)



(3)



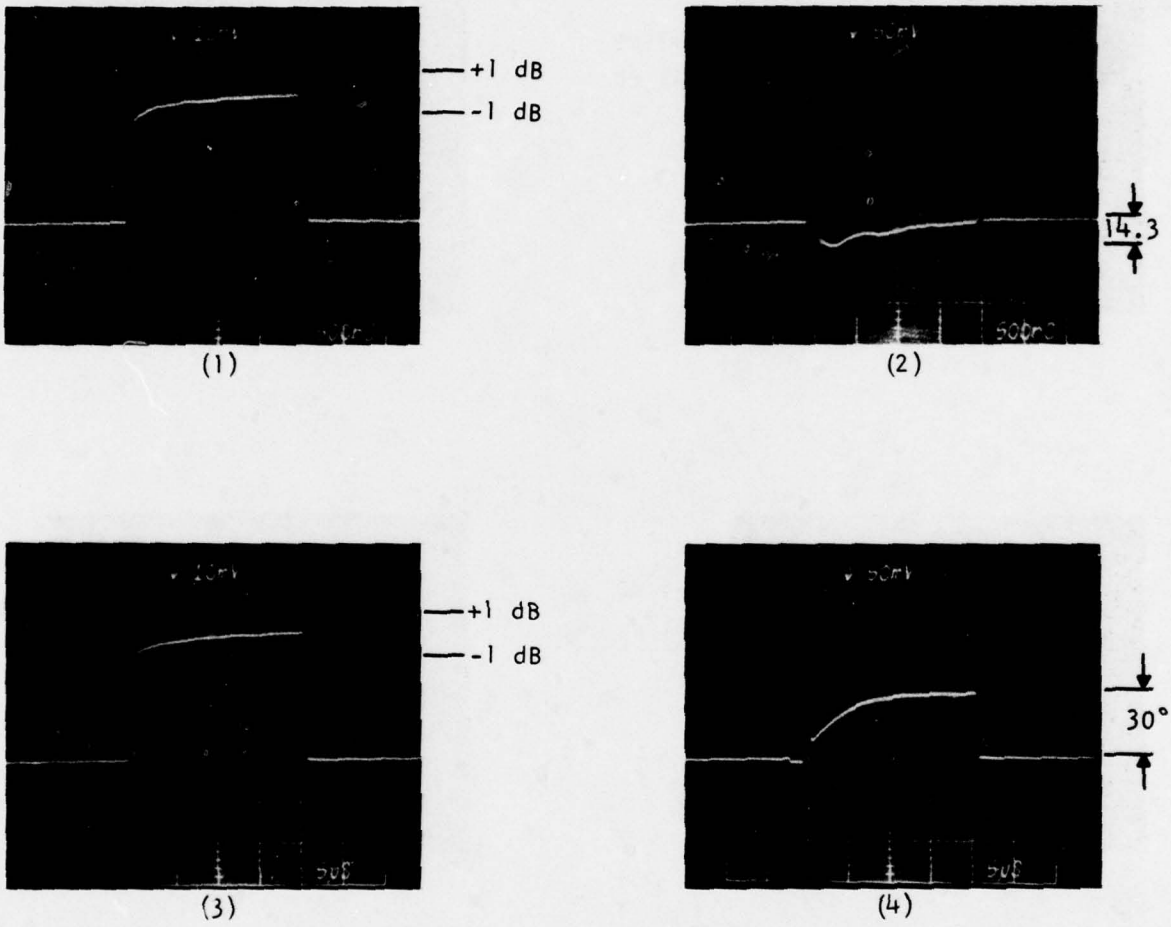
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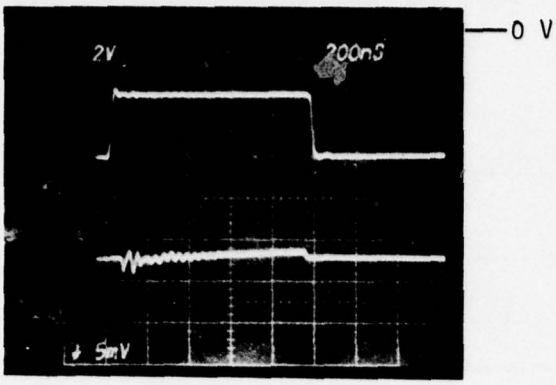
(1) Amplitude	2 μs Pulse Width	(3) Amplitude	20 μs Pulse Width
(2) Phase	1% Duty Cycle	(4) Phase	10% Duty Cycle

Figure 54(c). Pulsed Amplitude and Phase Response of Module #5 at 9.8 GHz



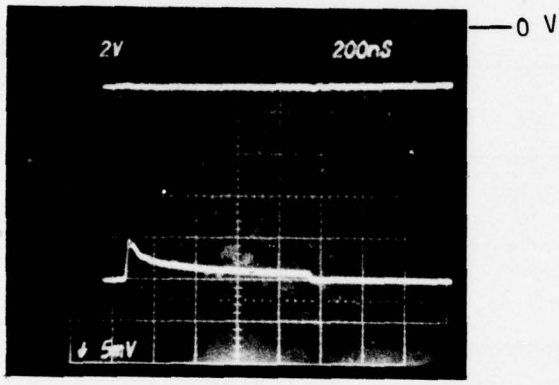
(1) Amplitude	2 μs Pulse Width	(3) Amplitude	20 μs Pulse Width
(2) Phase	1% Duty Cycle	(4) Phase	10% Duty Cycle

Figure 55. Pulsed Amplitude and Phase Response of Module #4 at 9.5 GHz

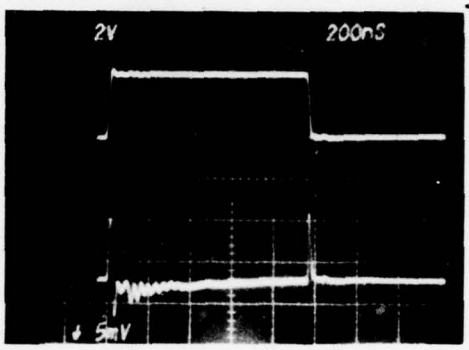


(a)

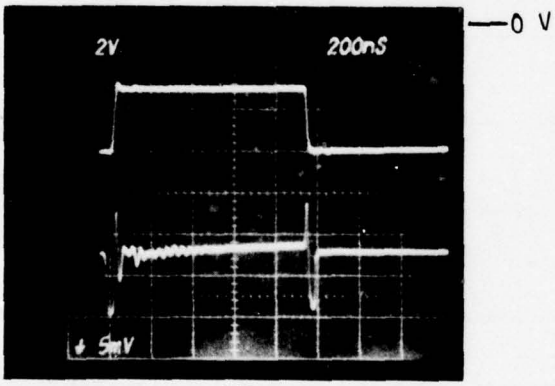
Frequency = 9.5 GHz
P_{in} = 10 dBm
V_{gs} = -6 V OFF
-3 V ON
V_{ds} = 6 V
Pulse Width = 1 μs
Duty Cycle = 5%



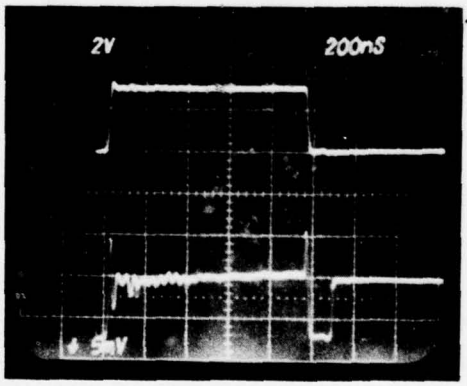
(b)



(c)



(d)



(e)

Figure 56. Pulsed Phase Response of a 300 μm Gate Width FET Amplifier Under Various Operating Conditions. Upper Trace: Gate Voltage; Lower Trace: Phase Shift. (a) Gate Voltage pulse width > rf pulse width; (b) rf pulsed with cw gate bias; (c) gate voltage pulsed with cw rf; (d) gate voltage pulse width = rf pulse width; (e) gate voltage pulse width < rf pulse width

Table 5

NRL Four-Stage Amplifier Modules

	Freq. (GHz)	Pulse Width (μs)	Duty Cycle (%)	All FET Module		FET/Read Hybrid Module	
				# 9	# 12	# 5	# 4
AMPLITUDE DROOP	9.145	2 20	1 10	0.2 dB 0.2	0.4 dB	1.5 dB	
	9.2	2 20	1 10			2.2 dB	
	9.5	2 20	1 10	0 0.3	0.1 0.7	0.9 2.1	1.2 dB 1.8
	9.8	2 20	1 10			1.6 2.0	
	10.0	2 20	1 10	0.4 0.5	1.2		
PHASE RAMP	9.145	2 20	1 10	6.6°-15.1° 4.7°	1.3°	8.3°	
	9.2	2 20	1 10			15.9°	
	9.5	2 20	1 10	3.1° 2.1°	8.1° 10.8°	10.4° 31.3°	14.3° 30.0°
	9.8	2 20	1 10			6.5° 27.8°	
	10.0	2 20	1 10	1.3° 3.7°	1.7° 1.7°		
		BIAS	V_{GS} ON	-1.5V	-1.5V	-1.8V	
			V_{GS} OFF	-6.0V	-4.0V	-6.0V	
			V_{DS}	9.0V	8.0V	9.0V	
			I_{READ}			≈0.4A	
		POWER	P_{IN}	12 dBm		12 dBm	
			P_o	≅36 dBm		≅37 dBm	

From the measurement results it can be seen that the all FET amplifier has less phase ramp than the FET/Read amplifier, although the all FET amplifiers had anomalously large phase ramp at some frequencies. This could be caused by the different tuning effects, especially the balanced output stage. Without the balanced stage, the FET driver amplifier has a phase ramp of 3 to 6° for a 20 μs pulsewidth. Since the Read diode is known to be very temperature-sensitive, it is not surprising to see a tremendous phase change during the pulse.

Under ideal conditions it is shown that a phase shift on the order of 4 to 6° can be expected for an all FET amplifier module with 3 to 4 W output.

3. AM-to-PM Conversion

The AM-to-PM conversion characteristics of some medium power amplifiers were measured. In general, the AM-to-PM conversion remains below 3°/dB for input drive levels up to the 1 dB gain compression point. The AM-to-PM conversion is independent of the operation modes, i.e., either cw or pulsed. Figure 57 shows the AM-to-PM conversion characteristic of a single-stage and a three-stage amplifier. The phase shift is taken as zero at the nominal rf input level of the amplifiers.

4. Phase Sensitivity to Power Supply Variations

The insertion phase is far more sensitive to the gate voltage variation than to the drain voltage variations. Figure 58 shows the bias sensitivities of the insertion phase of a two-cell (2 x 300 μm gate width, 1 μm gate length), single-stage amplifier. The phase sensitivity was $\sim$ 5°/V for changing gate bias versus $\sim$0.3°/V for changing drain bias. Figure 59 shows the insertion phase variation of a three-stage amplifier as a function of gate and drain bias. As expected, the sensitivity is higher for a multi-stage amplifier than for a single-stage amplifier.

Pulse Width = 50 μs
Duty Cycle = 25%
Frequency = 9.5 GHz

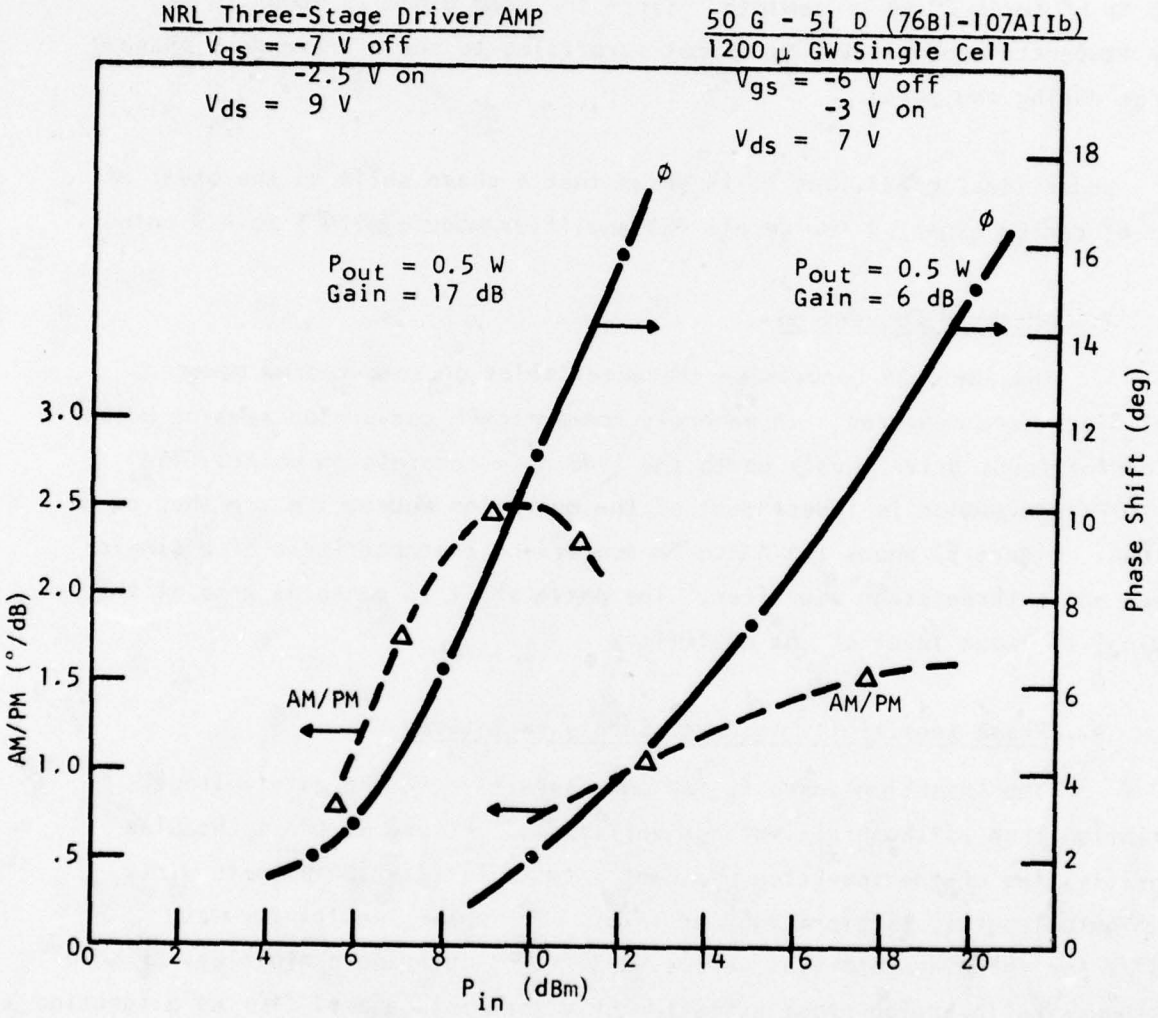


Figure 57 AM to PM Conversion Characteristics of a Single-Stage and a Three-Stage GaAs FET Amplifier

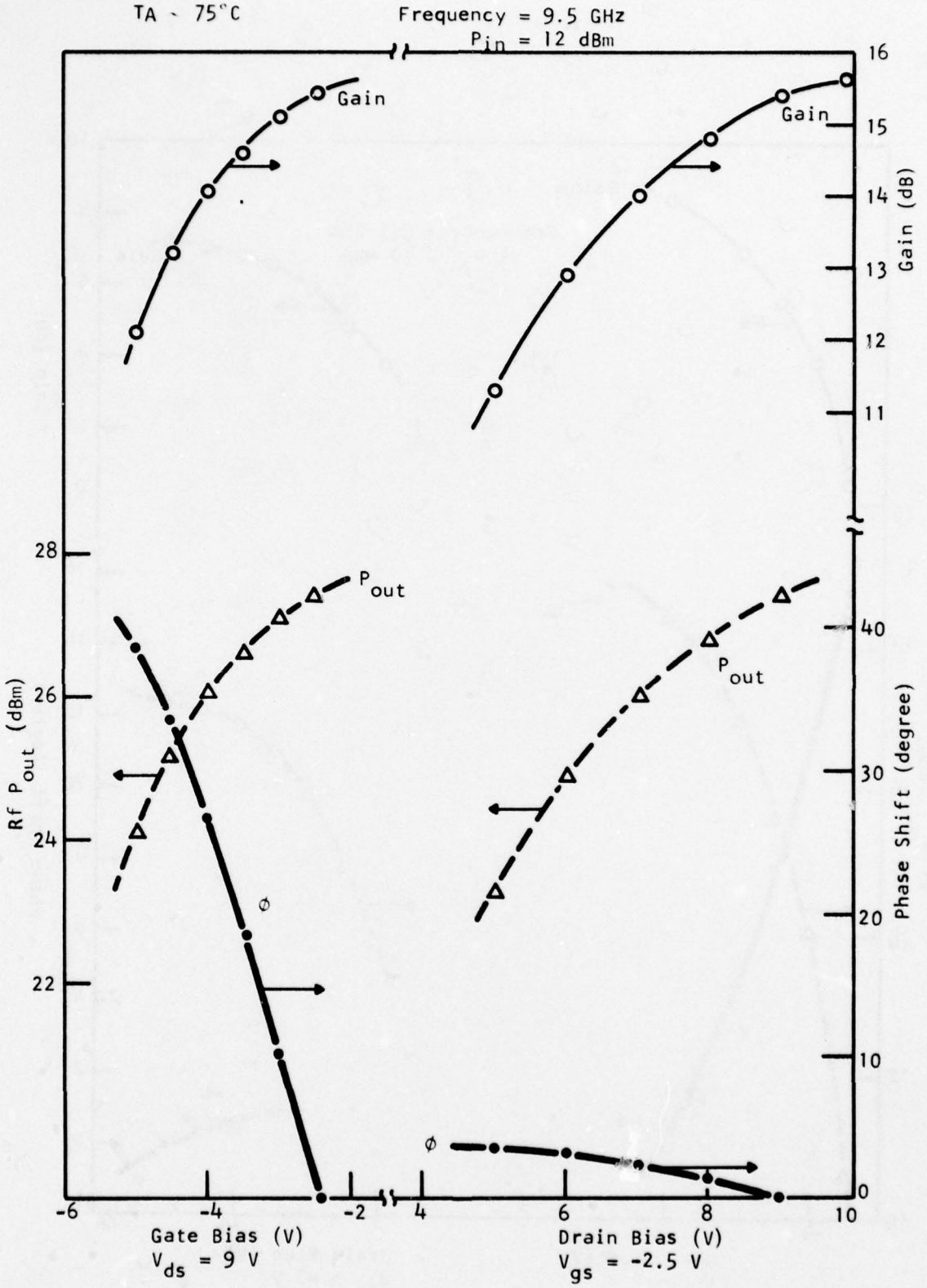


Figure 58 Bias Sensitivity of the Insertion Phase of a 600 μm Gate Width GaAs FET Amplifier

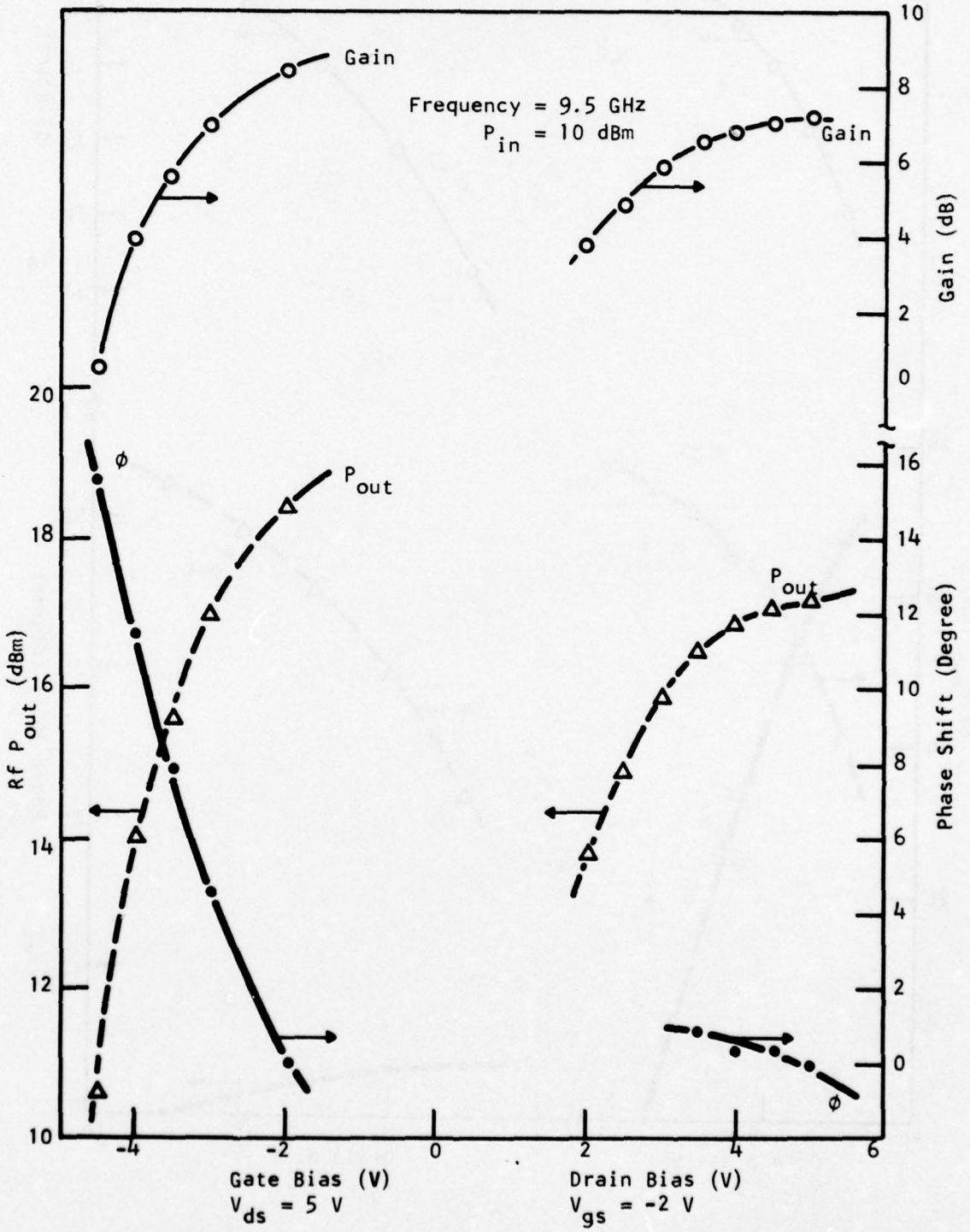


Figure 59 Insertion Phase as Function of Bias Voltage for a Three-Stage GaAs FET Amplifier

G. Noise Performance

AM additive noise measurements have been made on the four-stage driver amplifier at 9.4 GHz from 1 kHz to 200 kHz away from the carrier. Although the design goal is specified for the final 37 dBm amplifier, the AM additive noise for the 32 dBm driver amplifier is about 30 dB below this design goal at 1 kHz away from the carrier, and even further below for frequencies greater than 1 kHz away. In other words, there is roughly a 30 dB margin of additive noise allowed for the final power stage which will still meet the final amplifier noise requirement.

To characterize the noise due to the amplifier alone, i.e., the additive noise, it becomes necessary to exclude from the measurements the noise present in the driving or source signal. In this regard, a noise measuring system as described by Sann[9] can be used.

Figure 60 shows a simplified block diagram of the noise measurement system. The setup is realized in X-band waveguide. The basic system consists of the reference channel A, and the test channel B, which includes the amplifier under test. A single Gunn diode source provides the drive signal to the amplifier as well as the necessary signals to the other channels. A balanced mixer is used to down-convert the noisy signal in test channel B to baseband. Depending on the quality of the balanced mixer, the AM noise present in the reference signal is largely suppressed. The output of the mixer at the i.f. port contains the additive noise near the carrier, shifted down in frequency by the carrier frequency. This signal is amplified and applied to the input of the tunable wave analyzer. Channel C is used to suppress the carrier in the test channel (by proper leveling and phase shifting) so that the balanced mixer can be driven with a stronger signal without saturating the mixer diodes. Effectively, this raises the total system sensitivity. Finally, channel D, the calibration channel, is used to calibrate the system by injecting a known amount of modulation into the test

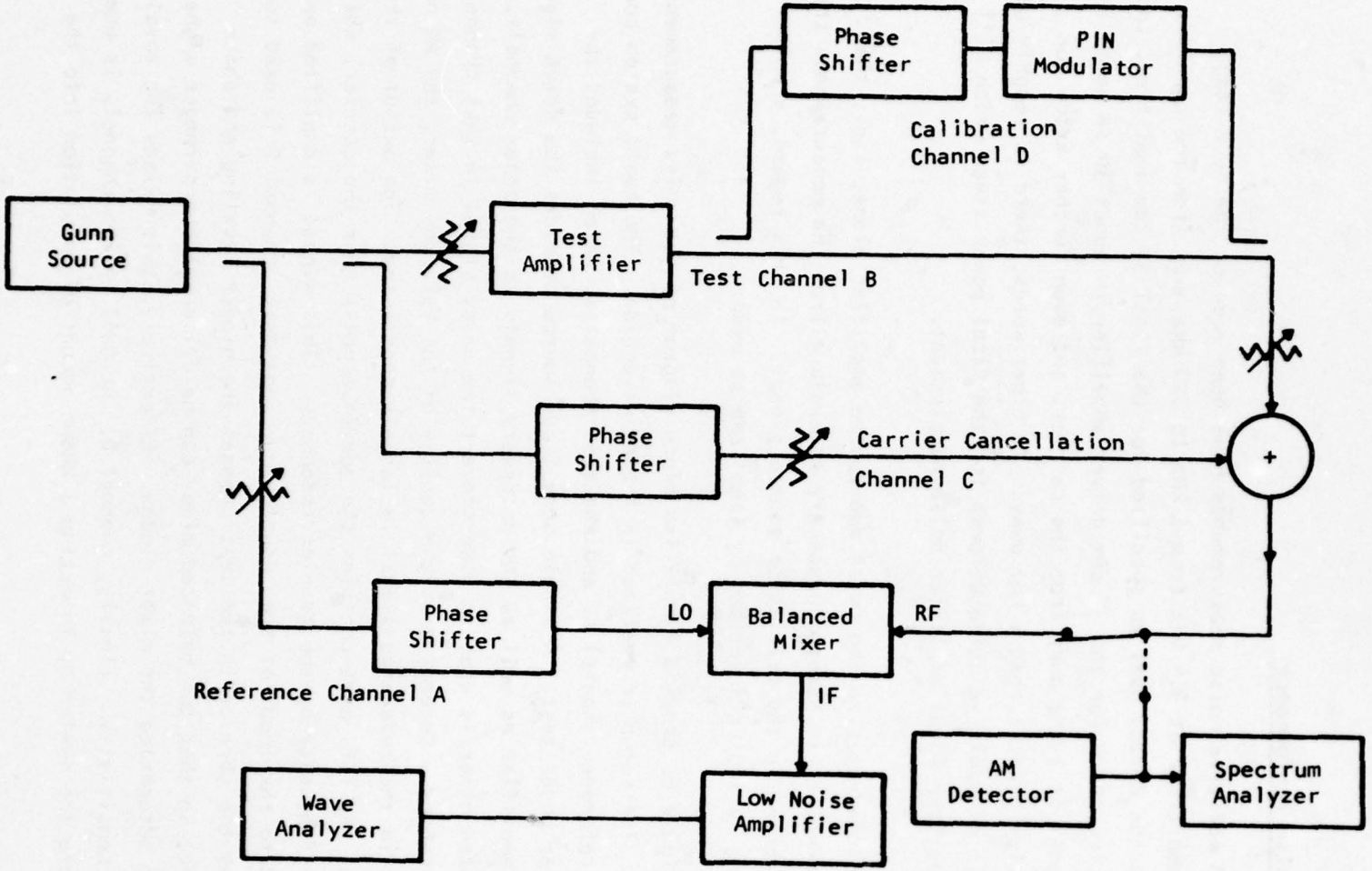


Figure 60 AM Additive Noise Measuring Setup

channel and observing the corresponding meter reading on the wave analyzer. During calibration, the phase shifter in reference channel A is set for a maximum reading on the wave analyzer. For AM noise measurements the phase of the calibration channel D is set so as to produce AM sidebands in the test channel B. This is checked by switching the signal in the test channel to a crystal detector and spectrum analyzer, and adjusting the phase of the calibration signal for maximum output from the crystal detector.

Figure 61 shows the results for the additive AM noise measurements for the driver amplifier at 9.4 GHz. The lower curve shows the measurement threshold, i.e., the system sensitivity. This curve was obtained without the test amplifier in channel B. The system sensitivity is basically limited by the noise contribution from the mixer diodes, the noise present in the Gunn source, and the noise figure of the i.f. amplifier. The middle curve shows the results with the driver amplifier inserted in the test channel B. As seen from the curve, the AM noise power (in a 1 Hz bandwidth) to carrier power ratio of 1 kHz away from the carrier is -136 dB. At 200 kHz away from the carrier it is down -149 dB. The top curve is the additive noise design goal for the 5 W amplifier.

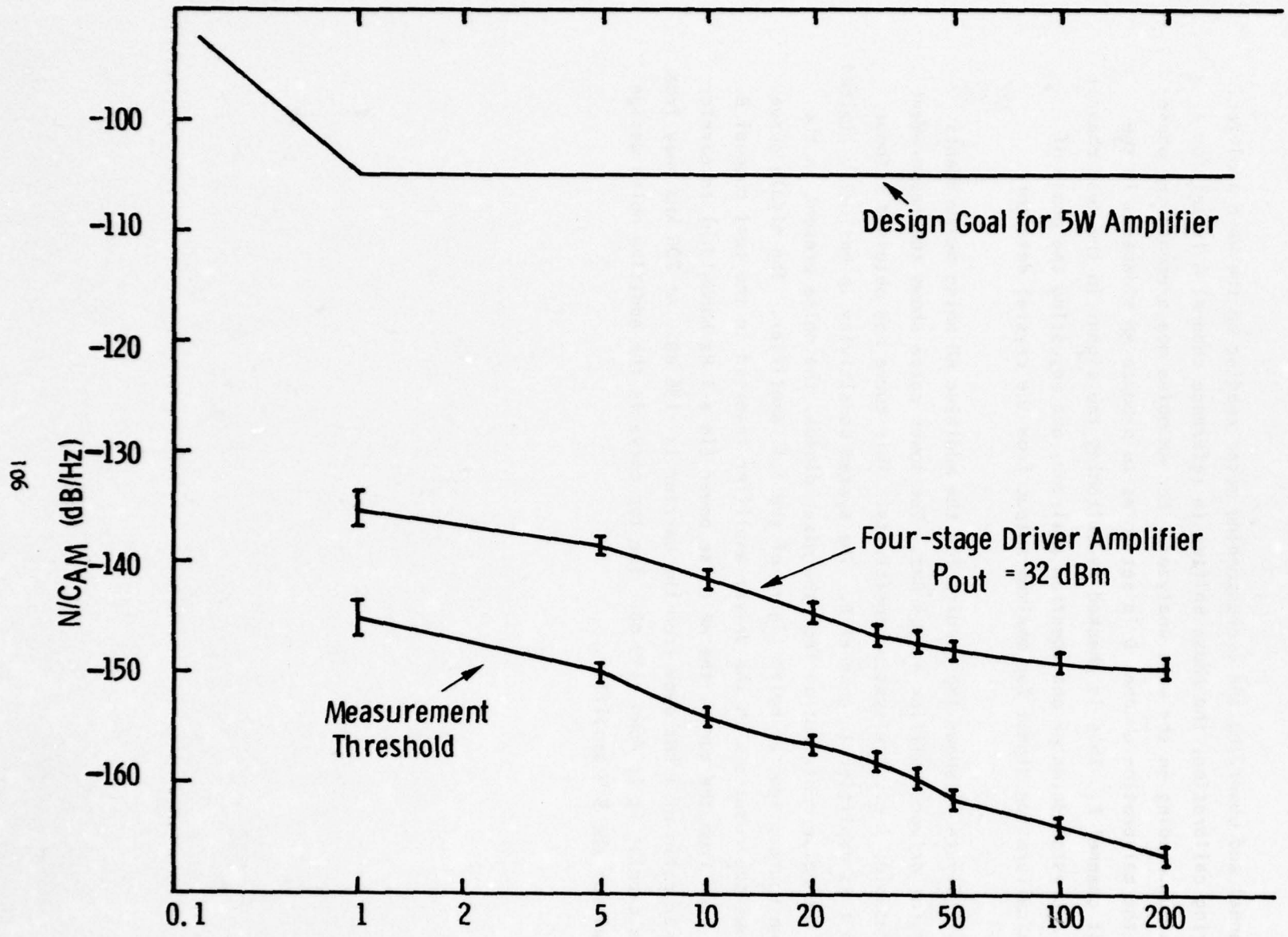


Figure 61 AM Additive Noise Results for Driver Amplifier

SECTION IV
SUMMARY

Summary

During the course of this program, significant advances have been made in the development of solid state power amplifiers for phased array radar applications. An all FET amplifier module with a three-stage driver and a balanced output stage delivered an output power of 4 W with 24 dB gain over the 8.9 to 9.9 GHz frequency band (1 dB) with 20% efficiency including bias circuit losses. An FET/Read diode hybrid amplifier module with a three-stage FET driver and a single Read diode output amplifier delivered 5 W with 25 dB gain at 9.5 GHz (600 MHz 1 dB bandwidth) with 19% efficiency. Extensive cw and pulsed measurements on these amplifiers indicate that the all FET amplifier is best suited for phased array radar applications.

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APPENDIX

DEVICE DELIVERIES

Table A1

GaAs FETs Delivered to NRL, January 1977*

Device Number	Good Cells	Gate Finger Width (μm)	Gain (dB) P_{out}= 15 dBm V_{ds} = 5V	Max. P_{out} with 6 dB Gain V_{ds} = 8V (mW)	Max. P_{out} with 4 dB Gain V_{ds} = 8V (mW)	Power Added Efficiency (4 dB Gain) (%)	Gate Voltage (V)
17623-116B1b#1	1	200	6.6	460	690	32.5	-3.5
17623-116B1b#2	1	200	6.6	500	720	36.3	-3.1
17623-116B1b#3	1	200	6.6	500	720	31.1	-3.2
17623-116B1b#VI	1	200	7.4	540	740	36.0	-3.3
17623-116B1b#IX	1	200	6.8	550	740	34.2	-3.1
A94B1Vb#1	1	200	6.8	630	690	34.7	-1.0
76B1-25A1b#1	1	200	6.8	400	690	32.5	-2.6
76B1-25A1b#2**	1,3	150	8.4	1,350	1,510	33.5	-2.0
76B1-38B1b#1	1,2	150	7.5	810	1,150	36.6	-1.9
76B1-38B1b#III	3,4	150	6.8	525	1,200	29.2	-3.1

*GaAs FET Data at 10 GHz

**Data taken at 8 GHz

Table A2

GaAs Read Diodes Delivered to NRL, January 1977

Diode Number	Operating Voltage (V)	Output Power (W)	Efficiency (%)	Frequency (GHz)
C27B-6001	51.0	3.0	25.0	9.2
C27B-6002	57.8	3.1	24.1	8.9
C27B-6003	59.0	3.2	22.3	9.1
C27B-6004	57.4	3.4	23.2	9.0
C27B-6005	56.4	3.2	24.4	9.0
C27B-6006	57.6	3.9	24.8	9.0
C27B-6007	56.9	3.4	25.3	9.0
C27B-6008	57.9	3.3	24.5	9.0
C27B-6009	57.6	3.2	24.1	9.0
C27B-6010	55.0	3.2	27.4	9.1

Table A3

GaAs FETs Delivered to NRL, March 1977*

Device Number	Good Cells	I_{dss} (mA)	g_m (mmho)	V_P (V)	Gain (dB) P_{in}=15 dBm V_{ds}=5V, $V_{gs}\cong$0	Maximum Output Power (W) 4 dB Gain V_{ds}=8V, V_{gs}=-2V	Maximum Output Power (W) 5 dB Gain V_{ds}=8V, $V_{gs}\cong$-2V	Power-Added Efficiency (%) (5 dB Gain)
76B1-18B1E #1	3	470	118	5.9	7.0	1.02	0.85	32.5
2	4	490	117	~7	7.2	1.07	0.91	31.1
3	1	460	124	5.4	7.1	0.98	0.87	34.6
4	4	460	120	6.0	7.3	1.12	1.05	35.1
5	2	460	122	5.5	7.4	1.00	0.89	31.3
6	2	480	120	~6	7.8	1.16	1.12	38.2
7	3	440	122	~5	7.0	1.05	0.93	37.3
8	2,3	960	240	6.2	7.1	1.55	1.12	21.0
9	1.2	860	220	~5.7	6.0	1.70	1.20	20.2
76B1-18B1E #10	3.4	940	240	~6	8.0	2.00	1.74	31.7

*GaAs FET Data at 10 GHz

Table A4

GaAs Read Diodes Delivered to NRL, March 1977

Diode Number	Operating Voltage (V)	Output Power (W)	Efficiency (%)	Frequency (GHz)
C27B-6011	51.0	3.2	22.5	8.7
C27B-6012	58.3	3.3	23.4	9.0
C27B-6013	59.1	3.4	21.8	9.1
C27B-6014	59.5	3.7	23.0	8.9
C27B-6018	55.5	3.2	26.5	9.3
C62B-6020	44.7	3.4	17.0	10.3
C87B-6021	53.5	4.0	19.6	8.9
C87B-6023	45.3	4.1	19.9	8.5
C51B-6031	51.9	4.1	16.3	9.5
C51B-6033	52.0	4.2	20.2	9.4
C51B-6034	55.9	3.8	16.3	9.4

Table A5

Devices Delivered to NRL - May 1977

GaAs FET Microwave Performance at 10 GHz

Number	Slice Identification	Good Cells	V_p (V)	Gain (dB) P_{in} = 15 dBm V_{ds} = 5V $V_g \cong 0$	Maximum P_{out} (W) with 4dB Gain V_{ds} = 8V	Power-Added Eff. (%)	I_{ds} (mA)	V_g (V)	Maximum P_{out} (W) with 6dB Gain V_{ds} = 8V	Power-Added Eff. (%)	I_{ds} (mA)	V_g (v)	Maximum P_{out} (W) with 4 dB Gain V_{ds} = 10V
1	76B1-108B1e	1,2	5.5	6.9	1.51	28	405	-2.9	-	-	-	-	1.86
2	76B1-108B1e	1,2	8.2	6.4	1.38	20	530	-3.0	-	-	-	-	1.44
3	76B1-108B1e	3	6.1	7.6	1.09	36	230	-2.6	0.76	30	235	-2.6	1.26
4	76B1-108B1e	2	9.1	7.0	0.78	30	190	-3.1	0.48	23	190	-3.4	0.89
5	76B1-137B1e	1,2	4.5	6.5	1.44	29	375	-1.6	-	-	-	-	1.86
6	77B1-2B1e	1	3.4	7.5	0.95	40	180	-1.0	0.76	36	190	-1.1	1.20
7	77B1-2B1e	3,4	3.5	7.7	1.58	36	335	-1.6	1.20	28.5	395	-1.3	1.99
8	77B1-2B1e	1	3.5	7.2	0.95	37	190	-1.75	0.69	29	225	-1	1.17
9	76B1-137B1e	4	3.4	7.2	0.91	39	175	-1.2	0.72	35	190	-1	1.07
10	76B1-137B1e	2	3.9	7.0	0.89	36	185	-1.6	0.63	29	200	-1.5	1.12

Table A6

GaAs Read Diodes Delivered to NRL - May 1977

Diode No.	V_B (V)	V_{op} (V)	I_{op} (mA)	Prf (W)	η (%)	f (GHz)
C27B	6013	59.1	267	3.4	17.2	9.05
C87B	6022	57.1	355	5.0	24.7	8.4
C89B	6026	51.5	471	4.6	19.0	8.5
C89B	6027	54.0	443	4.5	18.8	8.5
C51B	6030	52.7	442	4.0	17.2	9.2
C51B	6037	56.9	392	3.7	16.6	8.8
C21B	6039	56.9	313	3.4	18.4	8.6
C21B	6040	60.7	364	3.8	17.2	8.6
C21B	6047	56.6	386	3.7	16.9	8.8
C122	6043	55.8	275	3.6	23.5	9.6

Table A7

Devices Delivered to NRL - July 1977

GaAs FET Microwave Performance at 10 GHz

Number (Slice 7681-91A IIe)	Good Cells	V_p (V)	Gain (dB) P_{in} = 15 dBm V_{ds} = 5V V_g = -1V	Max P_{out}(W) w/4 dB Gain V_{ds} = 8V	Power-Added Eff. (%)	I_{ds} (mA)	V_g (V)	Max P_{out}(W) w/4 dB Gain V_{ds} = 10V	Max P_{out}(W) w/6 dB Gain V_{ds} = 8V	Power-Added Eff. (%)	I_{ds} (mA)	V_g (V)
1	3,4	5.8	6.6	1.66	31	408	-1.9	2.09	0.91	15	582	-1.1
2*	2,3,4	5.6	7.5	2.40	31	587	-2	2.82	1.44	22	615	-2
3	1,2	5.1	6.4	1.51	32	361	-1.7	1.82	-	-	-	-
4	2	5.7	7.2	1.10	32	255	-2	1.20	0.79	31	240	-2.5
5	1	4.5	6.7	0.83	33	187	-1.4	1.02	0.56	21	248	-1.1
6	2,3	6.5	6.4	1.66	35	356	-2.9	1.95	-	-	-	-
7*	2,3,4	5.6	6.0	2.19	35	471	-2.6	2.51	-	-	-	-
8	2,3	3.8	6.6	1.41	33	323	-1	1.91	1.02	24	405	-0.8
9	1,2	6.7	6.1	1.62	30	404	-2.6	2.19	-	-	-	-
10	2,3	6.0	6.3	1.38	31	337	-2.4	1.70	-	-	-	-

*Data taken at 8 GHz.

H. M. Macksey
July 20, 1977

Table A8

GaAs Read Diodes Delivered to NRL - July 1977

Diode No.	V_B (V)	V_{op} (V)	I_{op} (mA)	P_o (W)	P_{rf} (W)	η (%)	f (GHz)
6038	35.8	54.6	463	25.2	4.84	19.1	8.8
6048	37.2	54.6	443	24.1	5.05	21.0	9.4
6052	37.4	53.1	480	25.4	5.63	22.0	9.2
6054	39.5	56.8	356	20.2	4.5	22.2	9.3
6057	39.6	58.6	339	19.8	4.3	21.6	9.0
6058	40.2	57.7	370	21.3	4.63	21.6	9.4
6058.1	39.4	57.5	368	21.1	4.53	21.6	9.4
6061	38.6	57.9	373	21.6	4.6	21.2	9.3
6063	38.3	56.8	381	21.6	5.0	23.1	8.7
6064	38.0	57.7	392	22.6	5.0	22.0	9.6

Table A9

Devices Delivered to NRL - September 1977

Device Number	Slice Number	Good Cells	V_p (V)	Frequency (GHz)	Gain (dB) P_{in} = 15 dB V_{ds} = 5V V_g = -1V	Max P_{out} (W) with 4 dB Gain V_{ds} = 8V	Power-Added Efficiency (%)	I_{ds} (mA)	V_g (V)	Max P_{out} (W) with 4 dB Gain V_{ds} = 10V	Max P_{out} (W) with 6 dB Gain V_{ds} = 8V	Power-Added Efficiency (%)	I_{ds} (mA)	V_g (V)
1	76B1-91AIIe	1,2,3,4	5.3	8	6.6	2.57	29.3	660	-2.75	3.16	1.20	10.5	1070	-1.0
2	76B1-91AIIe	1,2,3,4	6.2	8	6.8	3.80	30.5	935	-2.1	4.36	1.90	15.3	1160	-1.7
3	76B1-91AIIe	1,2,3,4	5.1	8	6.5	2.51	29.4	640	-2.45	-	1.25	11.2	1050	-1.1
4	77B1-85BIe	1,2,3,4	5.6	8	8.9	3.16	33.2	715	-1.95	4.07	2.34	25.1	870	-1.9
5	77B1-85BIe	1,2,3,4	5.4	8	8.8	2.88	29.5	735	-2.15	3.63	2.09	23.6	830	-1.9
6	77B1-81BIe	1	4.5	10	6.8	0.72	36.0	150	-1.5	0.91	0.50	27.3	170	-1.5
7	77B1-81BIe	1	4.9	10	6.8	0.85	35.6	180	-1.25	1.05	0.56	24.9	210	-1.25
8	77B1-81BIe	1	4.9	10	6.8	0.87	36.0	180	-1.0	1.12	0.62	28.4	200	-1.0
9	77B1-81BIe	1	3.9	10	7.4	0.95	37.6	190	-1.0	1.15	0.72	33.4	200	-0.8
10	77B1-22BIe	1	-9.0	10	7.0	0.69	29.9	175	-2.8	0.81	0.40	15.4	240	-1.8

Table A10

GaAs Read Diodes Delivered to NRL - September 1977

Diode No.	V_B (V)	V_{op} (V)	I_{op} (mA)	P_o (W)	P_{rf} (W)	η (%)	f (GHz)
6056	38.8	55.9	416	23.2	5.32	22.8	9.2
6062	38.9	56.2	393	22.0	5.2	23.5	9.3
6055	40.0	57.0	401	22.8	5.0	21.8	9.3
6059	38.2	56.3	397	22.4	5.25	23.5	9.3
6060	38.4	56.7	402	22.8	5.72	25.0	9.3
6049	41.9	52.5	467	24.5	5.15	21.0	9.2
6050	35.9	52	475	24.7	5.9	23.8	9.2
6066	40.1	58.4	416	24.2	5.0	20.5	8.7
6065	40.7	58.7	447	26.2	6.06	23.0	8.9
6067	38.4	57.2	485	27.7	5.8	20.8	8.9

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