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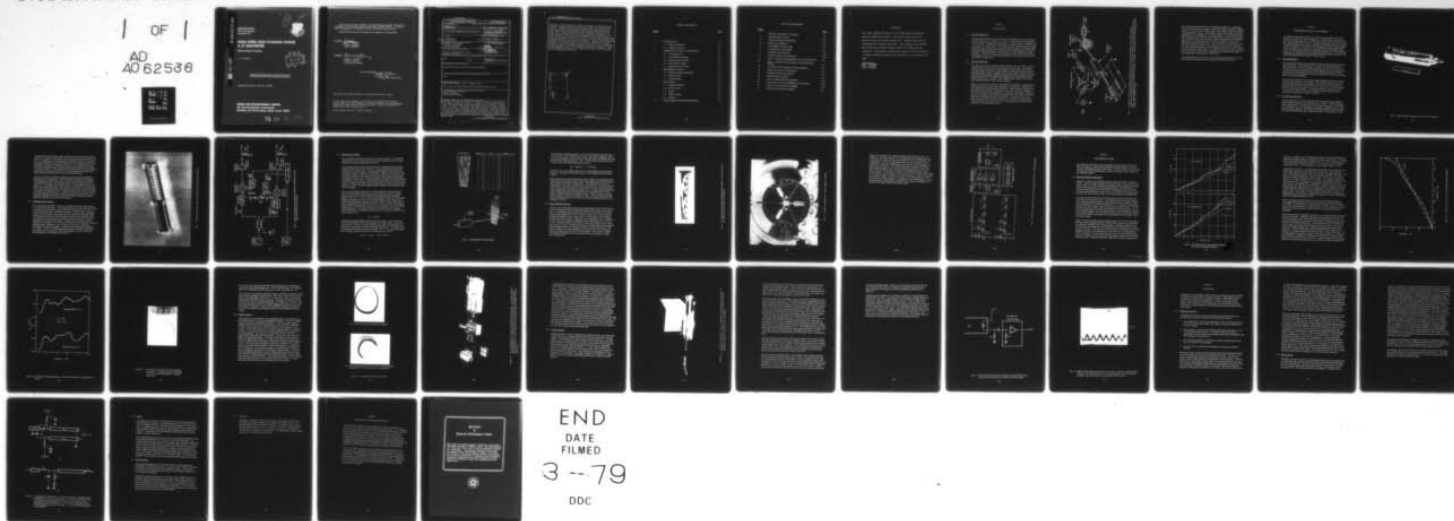
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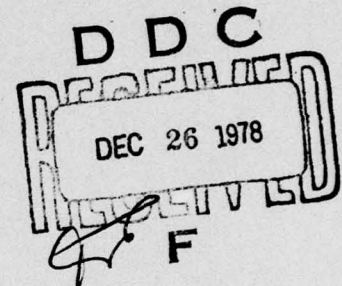
RADC-TR-78-237
Final Technical Report
November 1978



HIGH SPEED HIGH DYNAMIC RANGE A/D CONVERTER

Watkins-Johnson Company

S. K. Brierley



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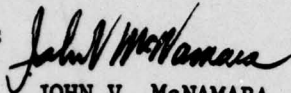
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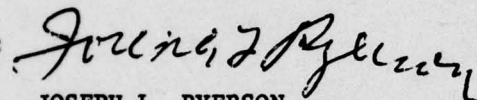
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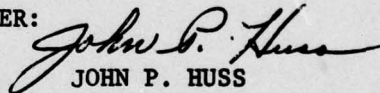
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feasibility. Major components of the EBS A/D converter are an electron gun, orthogonal deflection structures, semiconductor target, and output interface circuitry. A substantial portion of the program effort was devoted to the design and testing of a high impedance lumped element meanderline deflection system capable of generating the large beam displacements required in the target plane. Successful operation of these meanderlines was achieved. The unique semiconductor target sectors were designed and fabricated with good yield. Complete output circuitry was designed, built and tested satisfactorily. A complete A/D converter tube was built in which the diode response under actual operating conditions was successfully demonstrated. Funding and time constraints prevented the full demonstration of A/D conversion. However, all the major components of the tube and output interface circuitry were shown to operate as required. The primary technical challenge identified as a result of this phase is the development of a low-loss, broadband 4:1 impedance transformer. Assuming the successful design of such a transformer, it is felt that the proposed concept is definitely a viable one.

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TABLE OF CONTENTS

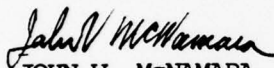
<u>Section</u>		<u>Page</u>
1	INTRODUCTION	1-1
	1.1 Program Objectives	1-1
	1.2 Technical Approach	1-1
2	COMPONENTS OF THE A/D CONVERTER	2-1
	2.1 The Electron Gun	2-1
	2.2 The Deflection Structure	2-1
	2.3 Deflection Input Circuitry	2-3
	2.4 Semiconductor Target	2-6
	2.5 Output Interface Circuitry	2-8
3	EXPERIMENTAL WORK	3-1
	3.1 Deflection System Experiments	3-1
	3.2 Output Circuitry	3-7
	3.3 Target Response	3-10
4	EVALUATION	4-1
	4.1 Deflection Structure	4-1
	4.2 Input Circuitry	4-2
	4.3 Target	4-5
	4.4 Output Circuitry	4-5
	4.5 Summary	4-6
5	CONCLUSIONS AND RECOMMENDATIONS	5-1

LIST OF ILLUSTRATIONS

<u>Figure</u>		<u>Page</u>
1	Schematic of the EBS A/D Converter	1-2
2	High Resolution CRT Gun	2-2
3	Deflection Structure Subassembly	2-4
4	Input Circuit Schematic	2-5
5	Semiconductor Target Coding	2-7
6	Semiconductor Target Wedge	2-9
7	Complete Target Assembly	2-10
8	Output Interface Circuit Schematic	2-12
9	Phase - Frequency Characteristics on Cold Test Structures	3-2
10	Phase - Frequency Characteristics on Actual Deflection Structure	3-4
11	Deflection Versus Frequency of the Meanderlines	3-5
12	Circular Scan Pattern Demonstrated	3-6
13	Modulated Circular Scan Pattern	3-8
14	Output Interface Circuitry	3-9
15	Fully Assembled EBS A/D Converter	3-11
16	Output Circuit Used in Evaluating the A/D Converter	3-14
17	Output From Line Receiver Amplifier	3-15
18	Impedance Transformer Schematic	4-4

EVALUATION

This effort addressed the need for a high speed digital interface for radar and communication systems. The critical elements of the A/D converter concept studied were demonstrated. Complete testing was not accomplished due to funding limitations. The breadboard unit developed by the contractor has been delivered to RADC for in-house test and evaluation. If the results of these tests continue to verify the design, a follow-on contractual effort will be initiated to build an engineering model.


JOHN V. McNAMARA
Project Engineer

Section 1

INTRODUCTION

1.1 Program Objectives

The goal of this program was to determine the feasibility of the A/D converter concept outlined in U.S. Patent No. 4,034,363, "Real Time Data Rate Quantizer and Analog-to-Digital Converter System." This invention is assigned to the U.S. Air Force. John McNamara and Paul Van Etten of the Rome Air Development Center are the inventors. The technical tasks required in support of this objective included design of the deflection system, design of the semiconductor target and output logic circuit, and fabrication of a test vehicle for concept evaluation. The test vehicle was to incorporate a single 6-bit target element, with design goals for the analog input bandwidth and conversion rate of 1 GHz and 200 MHz, respectively.

1.2 Technical Approach

The EBS A/D converter developed on this program uses a circularly scanned electron beam to excite a coded semiconductor target wedge. The energy contained in the electron beam which strikes the target is converted into current pulses which represent a digital coding of the position at which the beam crossed the target wedge. Sufficient output signal level is obtained due to the extremely high (several thousand) current gain of the semiconductor diodes under electron beam excitation. With multiple target wedges, word conversion rates approaching 2 GHz should be possible.

Figure 1 is an overall schematic of the EBS A/D converter. A pencil beam of electrons is produced by the high resolution electron gun (1). This beam is then modulated by the deflection structure (2). This structure consists of two orthogonal lumped element traveling-wave deflection structures (meander-lines) which impart the necessary beam excursions at the target. The proper phase and amplitude of the signals to be applied to the deflection structure is generated in the deflection input circuitry (3). The effect of this circuit, when combined with the deflection structure is to produce a circular scan of the electron beam, the radius of which is proportional to the instantaneous amplitude of the analog input signal.

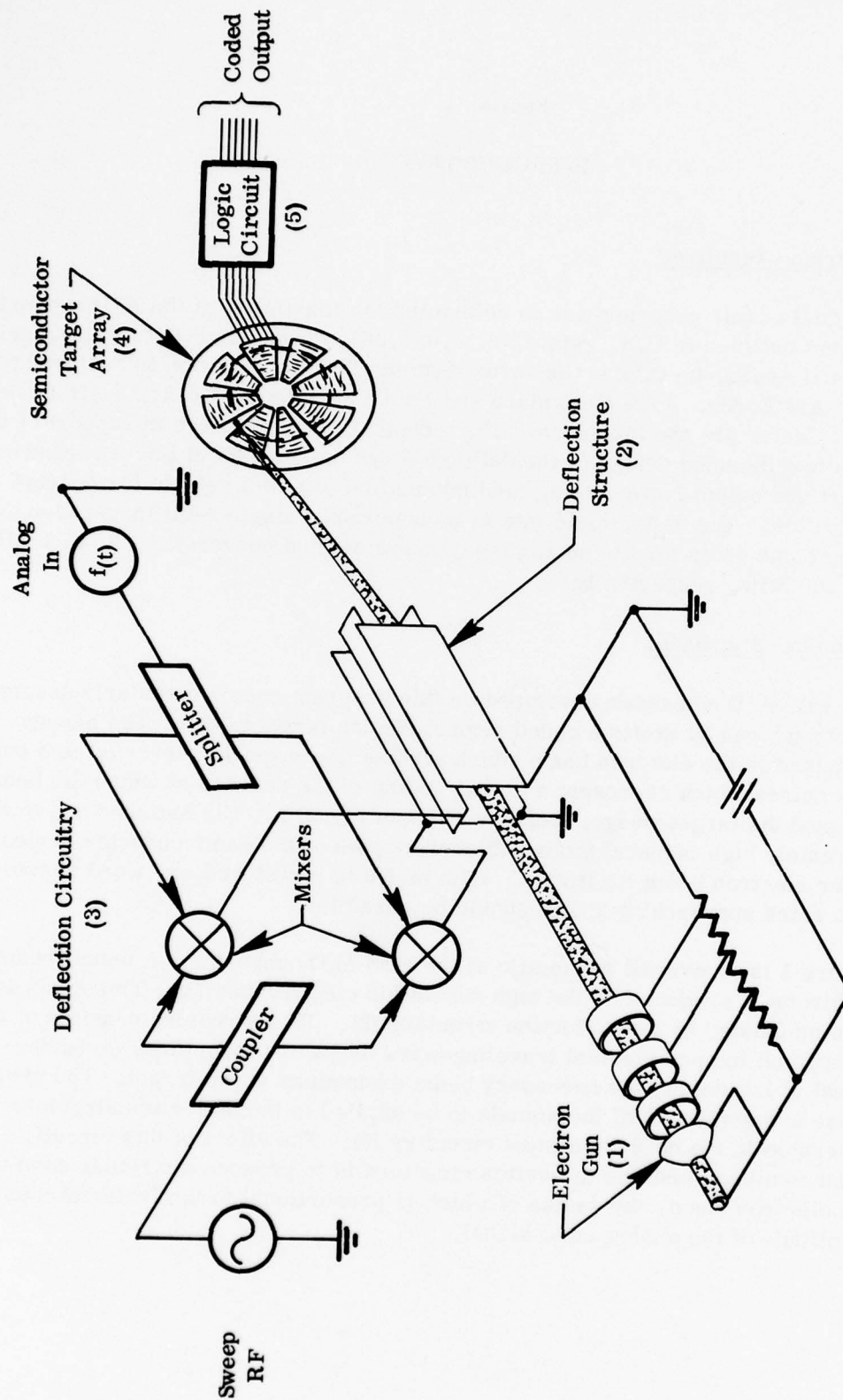


Fig. 1. The EBS A/D converter sweeps an electron beam in a circle on the target plane, the radius of which is proportional to the amplitude of the analog input signal. The radial position is coded using wedge-shaped diode arrays. The sampling rate is proportional to the number of wedges. The aperture time is inversely proportional to the angular width of a wedge.

The electron beam then strikes the semiconductor target (4). Ultimately, this target will consist of a number of individual wedges arranged in a spoke pattern. For the present feasibility study, only a single wedge was employed to demonstrate the concept. Each wedge consists of seven narrow columns arranged in a fan configuration. Six of the columns are appropriately coded with alternate areas of thick and thin metallization -- thin metal corresponding to a logical '1' (the electron beam is able to penetrate the semiconductor and produce a current pulse) and thick metal to a logical '0' (the metal effectively masks the entire beam). The seventh column is entirely covered with thin metal and provides a clock pulse each time the beam strikes it. The pattern of thick and thin metal is arranged in the form of a Gray code in order to minimize coding errors. The sweep of the electron beam across the seven columns of a single target wedge therefore constitutes one sample of the analog signal by encoding its radial position.

The design details and evaluation of the individual elements in the A/D converter will be discussed more thoroughly in the following sections.

Section 2

COMPONENTS OF THE A/D CONVERTER

As outlined in the previous section, the A/D converter under study in this program consists of five major components, or subassemblies: the electron gun, the deflection structure, the deflection circuitry, the semiconductor target, and the output logic circuitry. As might be expected, there are a number of interdependencies among these components which influence the final design of the A/D converter. For instance, the capabilities of the electron gun (in terms of minimum beam diameter) determine the target dimensions, which, in turn, set the requirements for the deflection system, etc. In the following paragraphs the characteristics and design criteria associated with each of the major components will be discussed in some detail.

2.1 The Electron Gun

The electron gun chosen for this design is a high resolution laminar flow gun, shown in Figure 2. The performance of this gun was consistent with the design objectives of the A/D converter program, and the use of such an off-the-shelf electron gun avoided the cost and potential risk to the program of a large electron gun development effort, thus allowing the program to devote greater effort to technical aspects which were more critical to the demonstration of the concept feasibility.

The use of this particular electron gun design established the first reference points for the overall converter design. This electron gun had been used in previous EBS programs in which beam sizes on the order of 2.0 mils and beam currents of 10 μA were achieved with a drift space of 10 inches between the electron gun and the target. For design purposes, a beam diameter of 2.5 mils and a current of 10 μA were assumed, and the drift space was arbitrarily constrained to remain at 10 inches.

2.2 The Deflection Structure

A beam diameter of 2.5 mils established target dimensions which required peak-to-peak deflection at the target plane of 0.7 inches. Early calculations quickly showed that the standard 50-ohm EBS deflection structure consisting of a meanderline over a ground plane would produce a deflection at the target far short of that required. Both higher deflection sensitivity and wider spacing between the deflecting planes would be required. Furthermore, the two

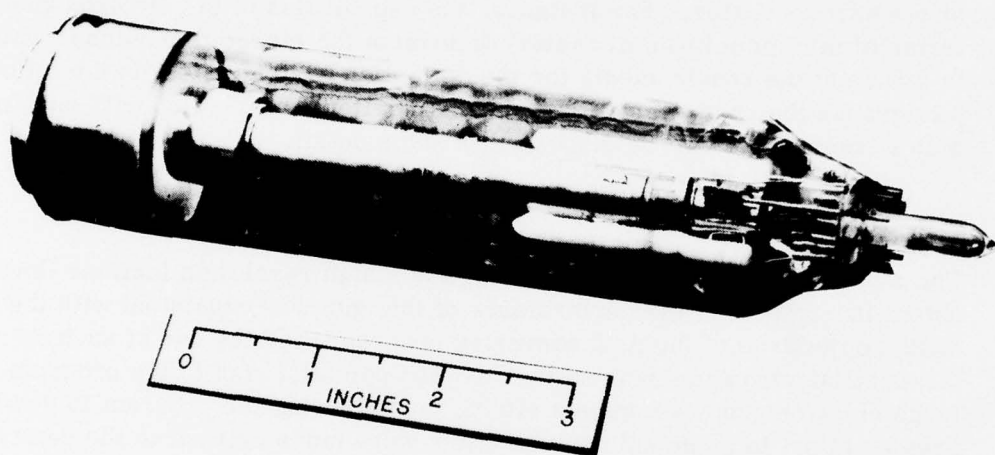


Fig. 2. High resolution CRT gun used in EBS A/D converter.

orthogonal deflection systems, while located at different distances from the target, were required to provide the same peak-to-peak deflection at the target. An extensive set of calculations was performed in order to determine the optimum design for the overall deflection system, taking into account the coupling between the two orthogonal structures. A total drift space of 10 inches was established, and the input power was constrained to be less than 10 watts per channel. The result of these calculations was a lumped-element, high impedance (approximately 200 Ω), balanced deflection structure with variable element spacing, both vertically and longitudinally.

This type of design represented a departure from previous EBS deflection structures and, consequently, called for different construction techniques. The photograph in Figure 3 shows the construction technique that was used. The individual plates are held by glass rods, attached to support plates at either end. The rigidity of the entire structure is maintained by four molybdenum rods running the length of both deflection structures. The alternating wire loops between plates form the lumped inductors, and create an S-pattern traveling wave transmission line. In addition to providing for ease of assembly, this construction technique minimizes the wasted space between the two orthogonal deflection structures, thereby obtaining the maximum possible deflection capability from the overall structure.

2.3 Deflection Input Circuitry

The circuit shown in Figure 4 is used to provide the necessary input signals to the deflection structures. The fundamental 200 MHz scan frequency is split by a hybrid coupler into two channels, 90° out of phase in order to create a circular scan with the two deflection structures. Similarly, the analog input is split into two in-phase components which are then mixed (using very high level balanced mixers to minimize distortion) with the scan oscillator signal. This results in a circularly scanning beam within the tube whose radius is modulated by the analog input signals. Various other components such as attenuators, delay lines, and dc current sources are used to precisely adjust the relative phases, amplitudes, and zero drive levels in the two channels. Following the mixing, the signals are applied to broadband power amplifiers (9.5 watts). The 50 ohm unbalanced output impedance of these amplifiers is then transformed to a balanced, 200 ohm impedance in order to match the input impedance of the deflection structures.

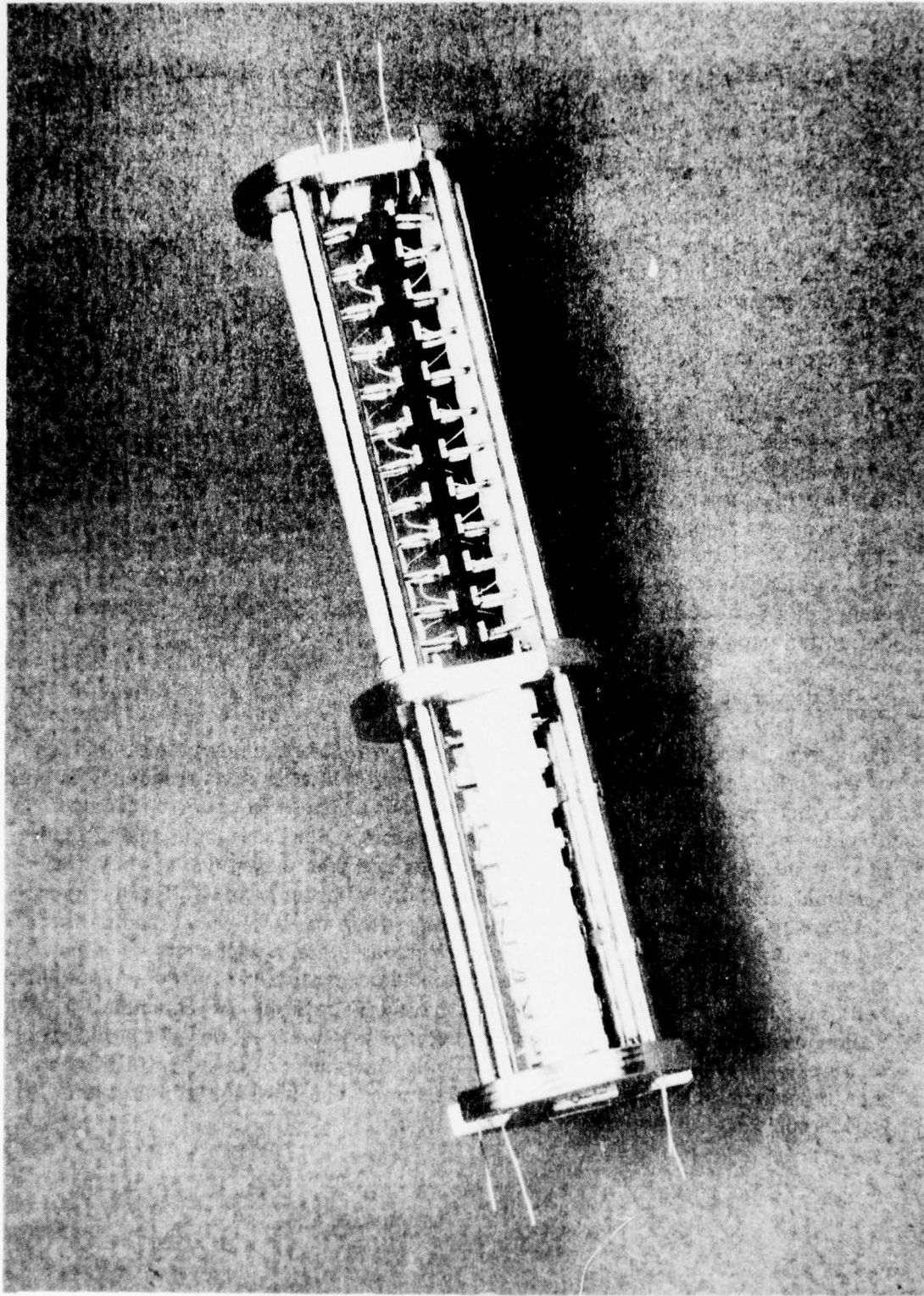


Fig. 3. Deflection structure subassembly used in the EBS A/D Converter.

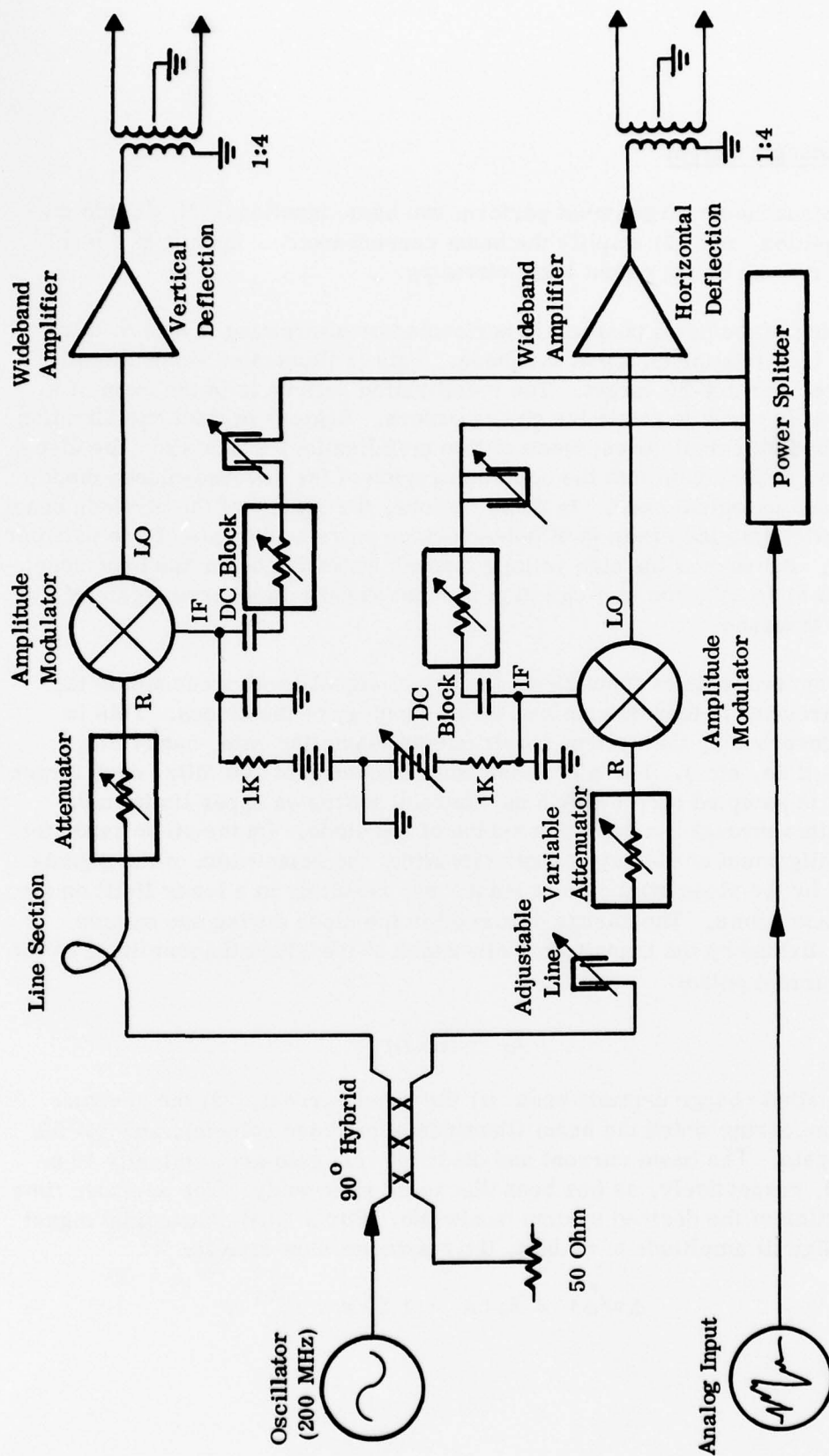


Fig. 4 - Input circuit used to generate the amplitude modulated circular scan of the EBS A/D Converter.

2.4 Semiconductor Target

The semiconductor target must perform two basic functions: (1) decode the beam position, and (2) amplify the beam current incident upon it to a level suitable for use by the output logic circuitry.

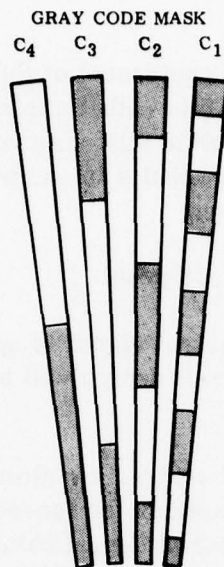
The coding of the beam position is performed by alternating layers of thick and thin metalization on top of the diode. This is illustrated schematically in Figure 5 for a 4-bit target. The metalization pattern is in the form of a Gray code in order to minimize coding errors. Regions of thick metalization correspond to logical zeros; those of thin metalization, which allow the electron beam to penetrate into the depletion region of the reverse-biased diode, correspond to logical ones. In these regions, the energy of the electron beam is converted into the creation of hole-electron pairs at the rate of one pair per 3.66 eV. Because of the high voltage through which the beam has been accelerated (12 to 15 kV), the pair creation process results in a current gain of two to three thousand.

Given a current gain of about 2500, the actual signal level presented to the output circuitry is then determined by the topology of the diodes. This in turn is governed by the system requirements (sampling rate, bandwidth, aperture time, etc.). For a circular scan frequency of 200 MHz, each target segment is sampled once every 5 ns, thereby setting an upper limit on the transit time through the depletion region of the diode. On the other hand, for ease of alignment of the output logic circuitry, the pulse width of the signals supplied by the diode should be at least 3 ns, resulting in a lower limit on the diode transit time. The charge deposited in the diode during one sample interval divided by the transit time discussed above gives the amplitude of the output current pulse:

$$I_0 = Q_d/v_d .$$

The deposited charge depends upon (1) the beam current, (2) the aperture time (time during which the beam illuminates the diode column), and (3) the current gain. The beam current and diode current gain are nominally 10 μ A and 2500, respectively, as has been discussed previously. The aperture time is a function of the desired system bandwidth. For a 1 GHz sinusoidal signal with a (digital) amplitude of 64 bits, the maximum slew rate is:

$$\Delta v/\Delta t = 2\pi fA = 1.28\pi \times 10^{11} .$$



DECIMAL	GRAY				BINARY			
	C ₄	C ₃	C ₂	C ₁	C ₄	C ₃	C ₂	C ₁
15	1	0	0	0	1	1	1	1
14	1	0	0	1	1	1	1	0
13	1	0	1	1	1	1	0	1
12	1	0	1	0	1	1	0	0
11	1	1	1	0	1	0	1	1
10	1	1	1	1	1	0	1	0
9	1	1	0	1	1	0	0	1
8	1	1	0	0	1	0	0	0
7	0	1	0	0	0	1	1	1
6	0	1	0	1	0	1	1	0
5	0	1	1	1	0	1	0	1
4	0	1	1	0	0	1	0	0
3	0	0	1	0	0	0	1	1
2	0	0	1	1	0	0	1	0
1	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0

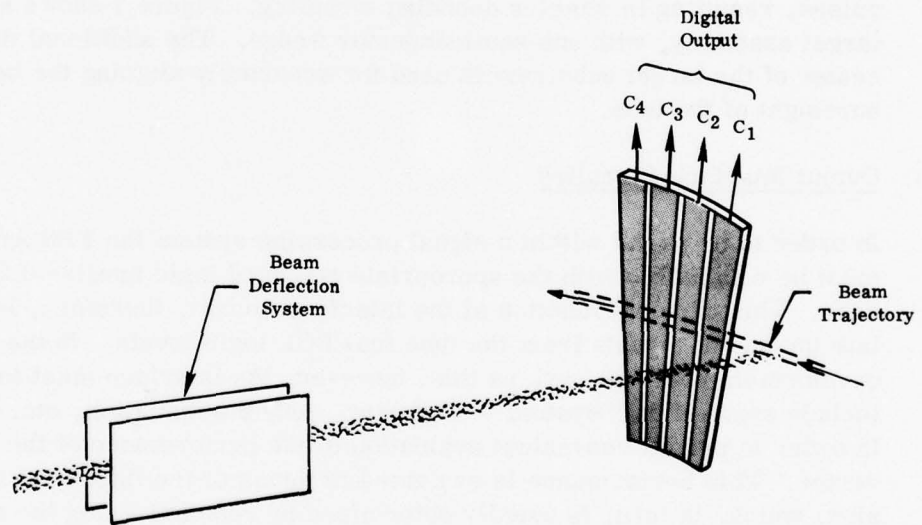


Fig. 5. Semiconductor Target Coding

The theoretical maximum aperture time is the reciprocal of this slew rate, or 2.5 psec in this case. Statistically, however, this rather stringent requirement can be relaxed by about a factor of four while still maintaining an acceptable harmonic distortion (about 2 - 3%). This results in an aperture time of 10 psec. The total charge deposited is given by:

$$Q_d = 2500 I_b \tau_a = 0.25 \text{ pcoul} .$$

Therefore, for a 3 ns diode transit time, the output signal is approximately 0.08 mA. The impact of this on the output circuit design will be discussed shortly.

Figure 6 shows an actual semiconductor target wedge, the alternating metallization pattern being clearly visible (dark areas along the fan-shaped columns are the thin metal regions--logical ones). The right-hand column has no coded pattern and is used as a source of timing pulses for the output circuitry. Every sweep of the beam across the segment will produce a pulse from this column regardless of the digital code generated. Timing command generation in this fashion automatically synchronizes the timing pulses with the data pulses, resulting in simpler decoding circuitry. Figure 7 shows a complete target assembly, with one semiconductor wedge. The additional diode in the center of the target substrate is used for accurately aligning the beam to the boresight of the tube.

2.5 Output Interface Circuitry

In order to be useful within a signal processing system the EBS A/D converter must be compatible with the appropriate standard logic family--ECL in this case. The principal function of the interface circuit, therefore, is to translate the output signals from the tube into ECL logic levels. In the case of a development program such as this, however, the interface must in addition include some of the "system"--buffering, code manipulation, etc.--required in order to permit convenient evaluation of the performance of the A/D converter. This performance is evaluated in terms of the fidelity of the conversion, which, in turn, is usually determined by reconstructing the analog signal from the digital output and comparing it with the original input signal. The complete interface in a test program such as this must have as its ultimate output an analog reconstruction of the input signal. This requires a significant amount of additional circuitry beyond that necessary simply for logic level compatibility.

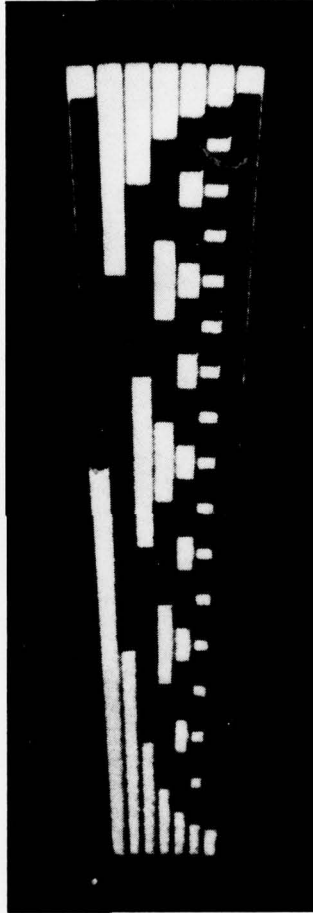


Fig. 6. An individual target wedge showing the alternating 1's (dark areas) and 0's (light areas) of the gray code pattern.

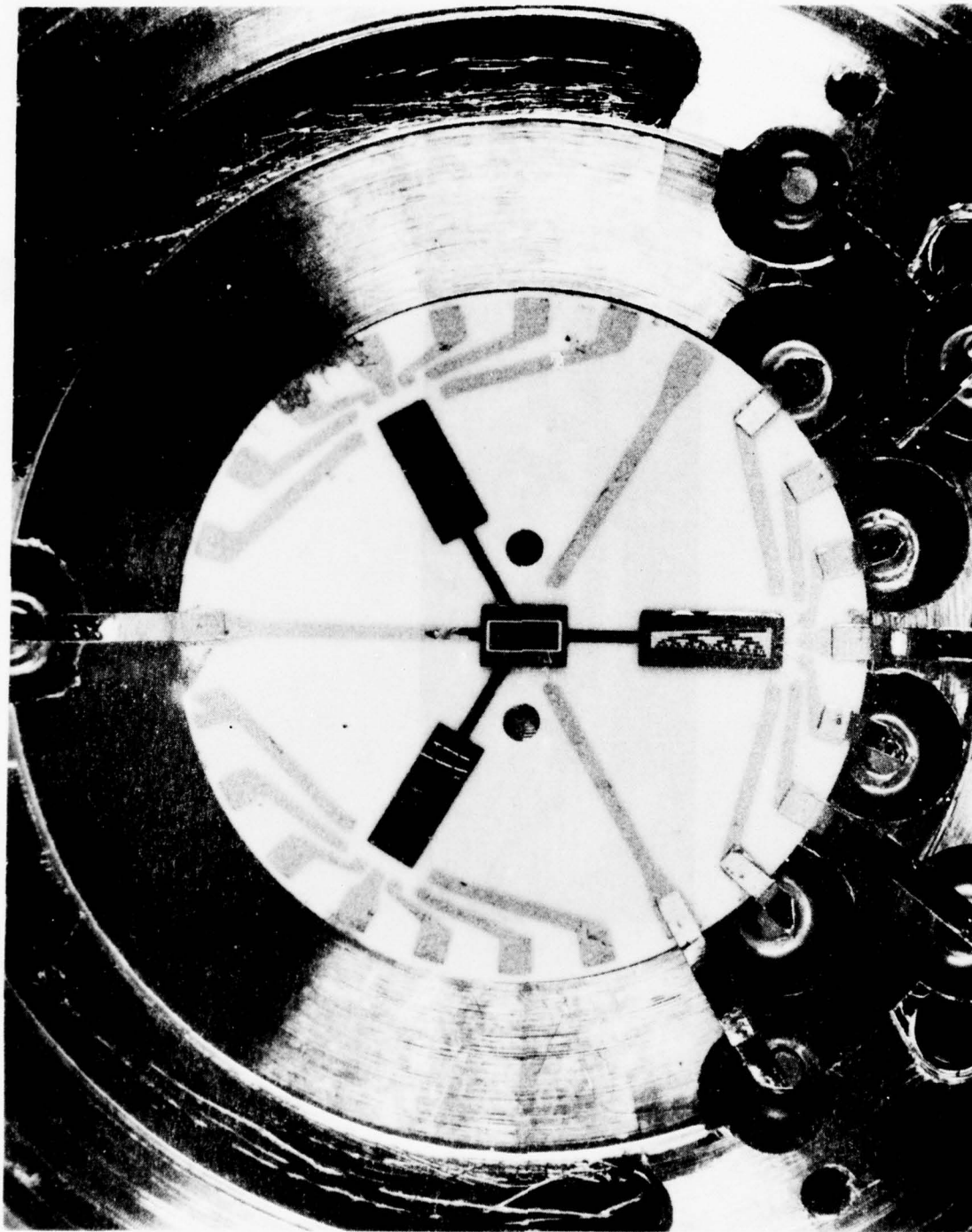


Fig. 7. Complete assembly for a single wedge A/D target.

Figure 8 is a schematic of a sample channel of the interface circuit. It consists of two major functions: pulse amplification and shaping, and code conversion--the output then being in a suitable form for reversion to an analog signal. The 30 mV input signal (0.08 mA into 380 ohms) is first amplified by a sequence of high speed line receivers up to the standard ECL logic levels (-0.95 and -1.7 V) and then stored in a register of flip-flops. The subsequent stages of the circuitry cannot operate nearly as fast as the EBS A/D converter, so only one sample in one thousand is stored in the buffer register. At this point, the data is in a Gray code format, which must be converted to binary in order to be processed further. This is accomplished by an iterative array of exclusive OR gates. The resulting binary code is also stored in a buffer register. Reconstruction of the analog signal can then be performed by a commercially available D/A converter following a level shift from ECL logic levels to TTL logic levels.

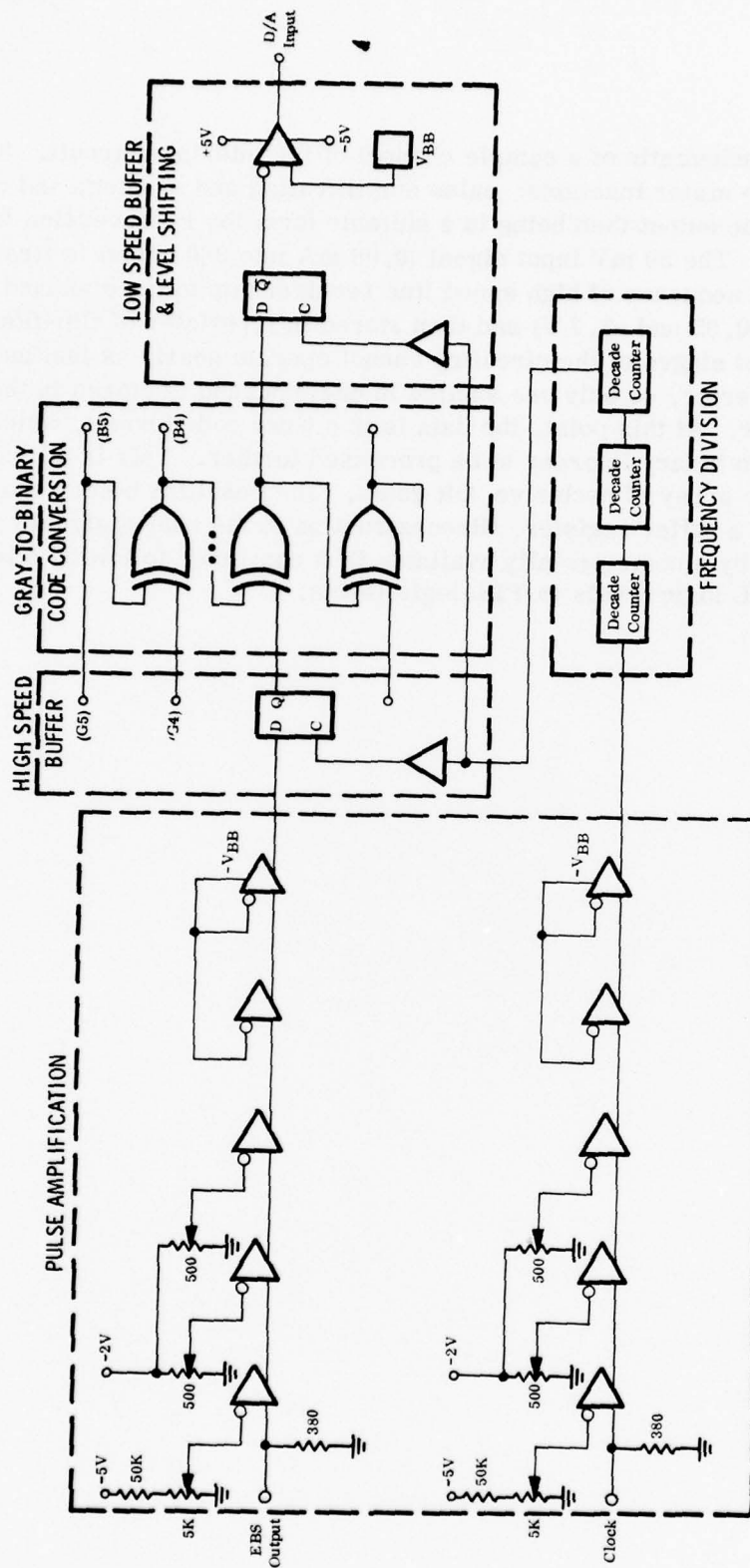


Fig. 8. EBS A/D Converter Interface Typical Data Path from One Diode Segment

Section 3

EXPERIMENTAL WORK

The design and development work undertaken on this program fell into two general categories: that associated with the deflection system of the tube, and that comprising the target performance. For the most part, effort in the two areas proceeded independently, and will be treated in such a manner in the following sections.

3.1 Deflection System Experiments

Within the category of the deflection system, there were also two distinct phases. The first phase consisted of cold tests used to verify, and, in some cases, adjust, the choice of physical parameters as they related to the basic electrical requirements of the meanderline system. The second phase involved measurement of the performance of the deflection structure under actual operating conditions, using a CRT screen in place of the target array in order to be able to observe directly the trace pattern in the target plane.

The requirements imposed upon the deflection structure were discussed in some detail in a previous section. The important electrical characteristics were sufficiently high impedance (at least 200 ohms in the balanced, double-sided configuration) and sufficient bandwidth (i.e., relatively low dispersion through 1 GHz with a signal velocity matched to the beam velocity). The 200 ohm impedance level was readily achieved with the original design. The dispersion and propagation velocity characteristics were somewhat more sensitive to design changes. The important parameter was the dispersion relative to the phase velocity of the beam (which is proportional to the square root of the beam voltage).

Figure 9 shows the phase-frequency characteristics for the two meanderline structures (these measurements were taken using a single side of the deflection structure suspended over a ground plane). A perfectly dispersion less line would have a straight line plot on this graph corresponding to the phase velocity of the line. As can be seen from the figure, the meanderlines become dispersive relative to the natural phase velocity of the line (approximately 0.30 c). However, if a beam phase velocity of 0.25 c is super-imposed upon the curve as shown, it can be seen that the net phase shift deviation remains within about $\pm 20^\circ$. Since the deflection sensitivity is roughly proportional to

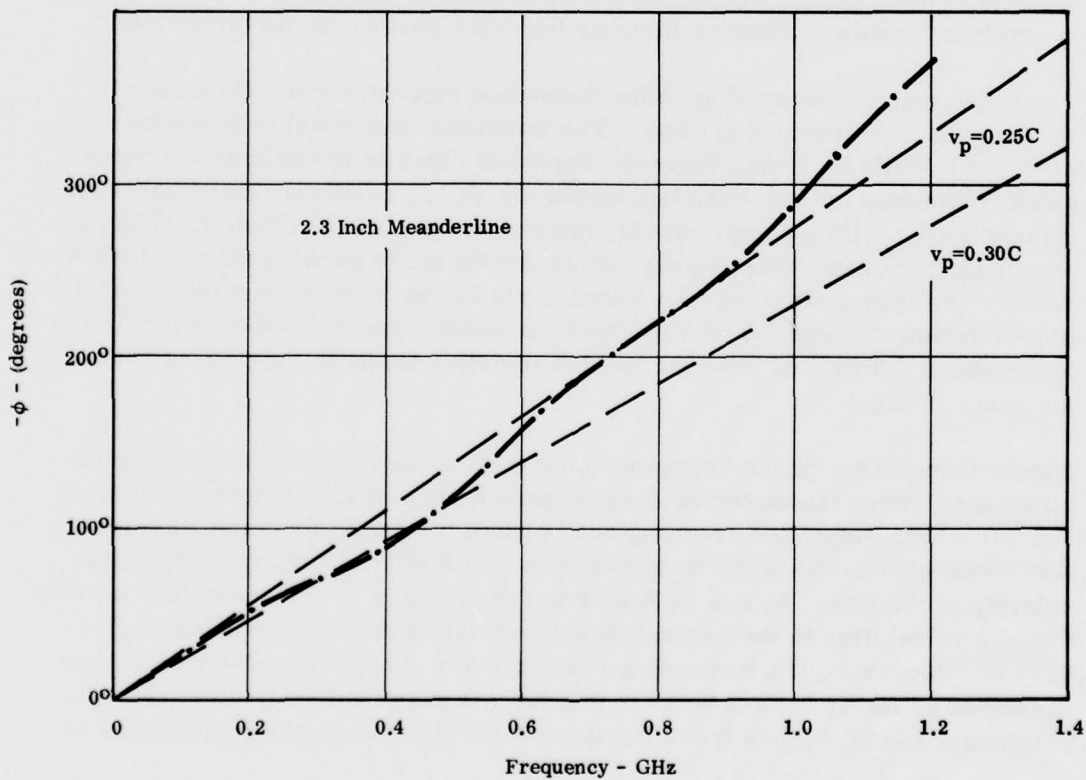
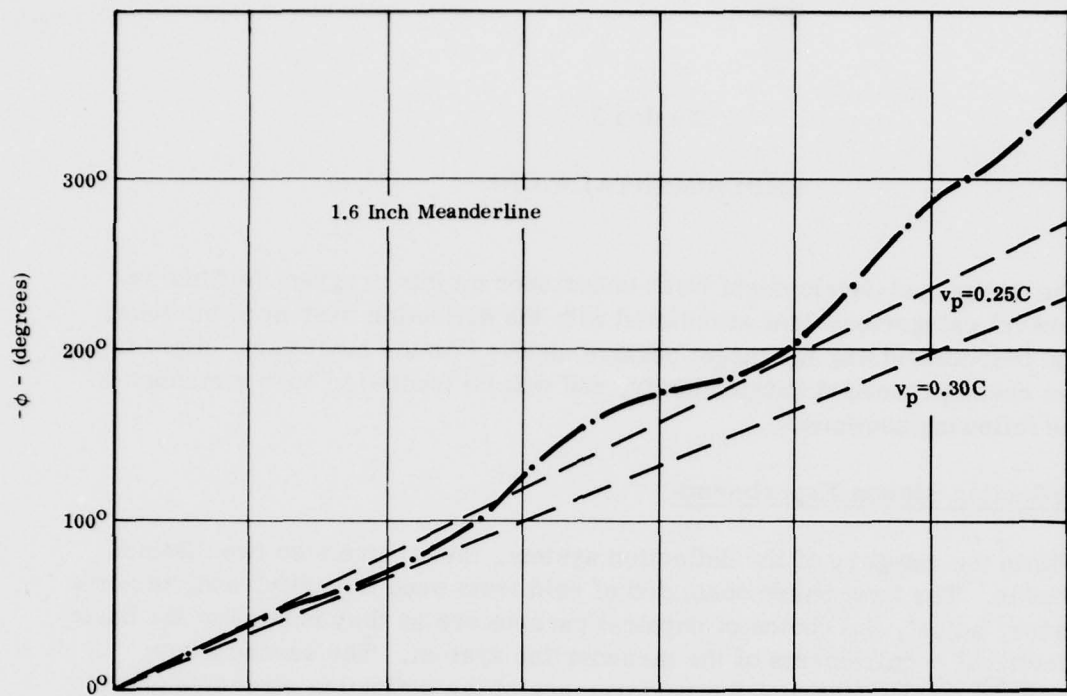


Fig. 9. The phase shift vs. frequency characteristic for the two meanderline designs

$\sin \Delta \phi / \Delta \phi$ (where $\Delta \phi$ is the dispersive phase shift), the net variation in deflection sensitivity relative to the beam velocity is only about 2%. The phase shift of the actual double-sided configuration of one of the meanderlines (the 2.3 inch long one) is shown in Figure 10. The beam velocity for minimum dispersion is 0.23 c, corresponding to a beam voltage of about 13.5 kV.

Following the cold tests, a complete deflection structure was assembled into a tube which contained a CRT screen in the target plane, thus permitting direct observation of the beam pattern under actual operating conditions. The first set of measurements were concerned with the deflection in the target plane as a function of frequency in the two axes. This data is presented in Figure 11. Across the band of 0.15 to 1.0 GHz, the variation in deflection is approximately 15%, comparable to the variation in deflection sensitivity observed with conventional EBS meanderlines. Subsequent tests, in which the beam voltage was varied in an effort to detect changes in response that could be associated with dispersion on the meanderlines, revealed that most of the ripple was due to impedance mismatches with the deflection structure. The data in Figure 11 was taken at a constant drive power of 2W, indicating that full deflection could be achieved with approximately 8W of power, comfortably within the original design goal of 10W.

Figure 12 shows the circular scan achieved with the deflection structure. Test equipment limitations at the time dictated that the operating frequency be 500 MHz. The drive power is again about 2W/channel. Due to the distortion in the driver amplifiers, it was necessary to use low-pass filters in the deflection circuitry in order to achieve the low eccentricity shown in the photograph.

Distortion in the driver amplifiers proved to be a recurring difficulty throughout the test program. Initially, noticeable harmonic distortion appeared on the circular scan at power levels (through the meanderlines) of only 2 to 3 W. A partial explanation was found in the 4:1 impedance transformers going into and out of the deflection structures. These transformers are constructed of coaxial cable pairs, connected in parallel at the low impedance end, and in series at the high impedance end, a standard technique used on EBS power amplifiers. In this configuration, short circuiting of the RF signal is prevented by the choking action of the inductance of the coaxial cable jacket. For the high impedances encountered in this application, however, the inductance was insufficient, resulting in a relatively low impedance RF shunt to ground and an overall insertion loss of about 3 dB. Various attempts to increase this inductance proved unsuccessful, and it was decided to tune the transformers

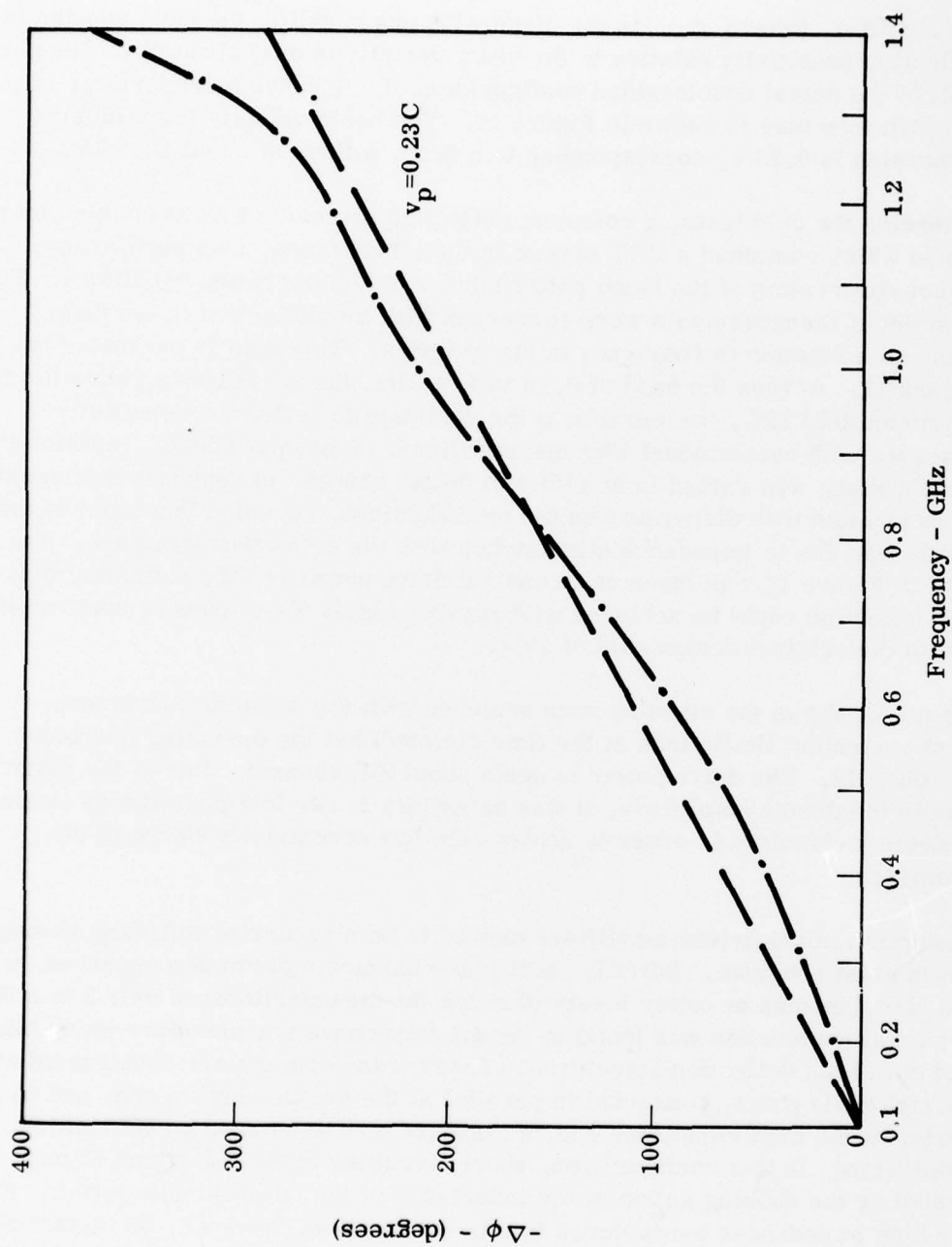


Figure 10. Dispersion on Final 2.3 Inch Double-Sided Meanderline

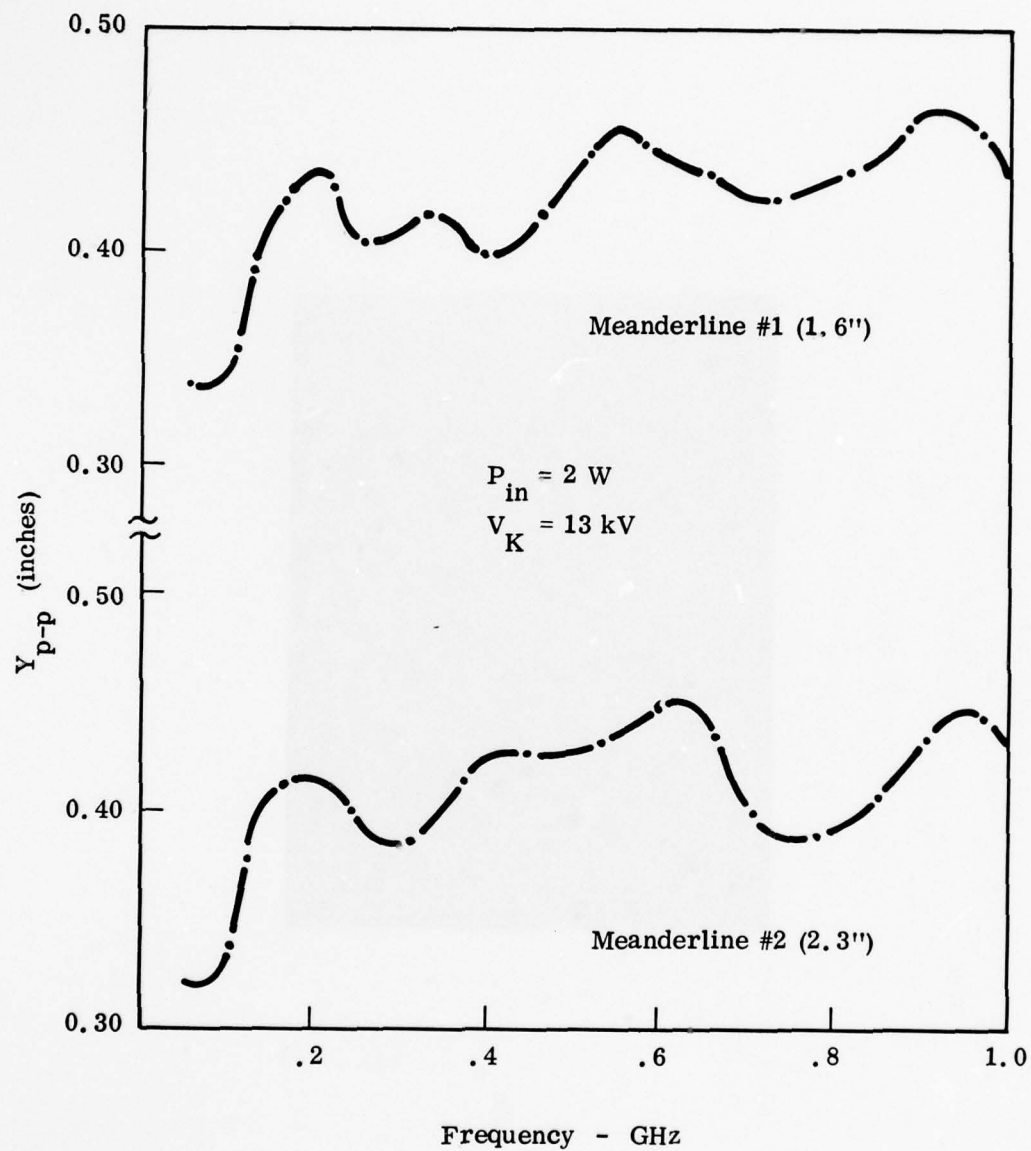


Figure 11. Deflection in the target plane as a function of frequency at constant drive power.

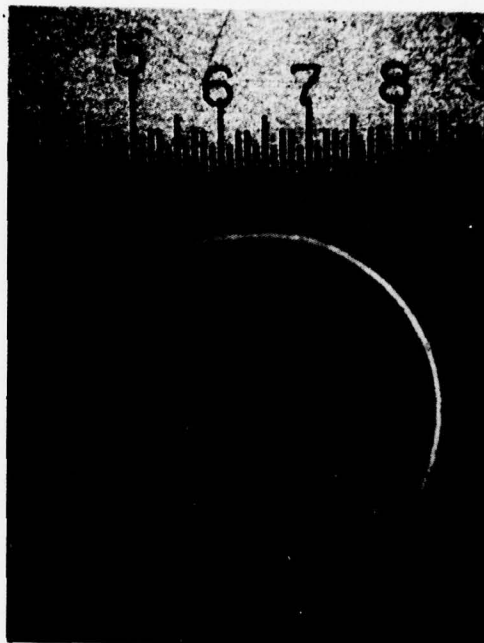


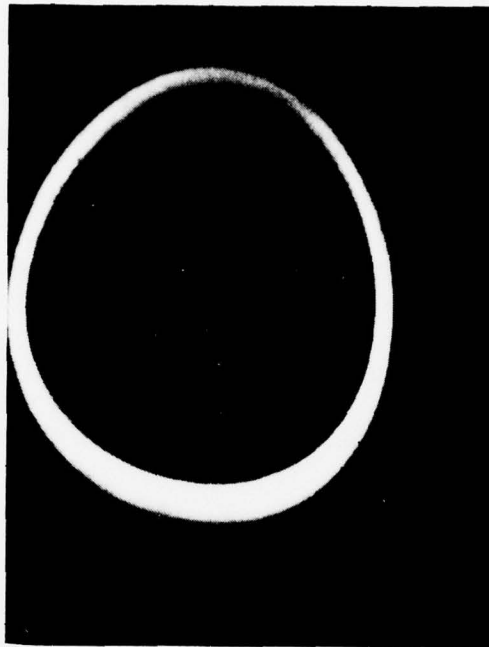
Figure 12. Photograph of CRT screen showing circular scan pattern. Deflection system is operating at 500 MHz with approximately 2 W/channel input power.

for low loss in the vicinity of 200 MHz (the scan frequency) by adding shunt capacitance at the high impedance end. Under these conditions, the insertion loss of the transformers at 200 MHz was reduced to approximately 1 dB.

The operation of the complete deflection system, including the amplitude modulation of the scan signal, was then tested. The traces on the CRT screen are shown in the photographs of Figure 13. As can be seen, there is still some residual distortion in the driver amplifiers. The upper photo shows the basic circular scan, with no amplitude modulation, at a frequency of 198 MHz. The lower photo shows the result of amplitude modulating the basic scan at a signal frequency of 290 MHz. Again, driver amplifier distortion complicates the picture somewhat, but the annular envelope of the modulation is clearly visible.

3.2 Output Circuitry

Concurrently with the evaluation of the deflection system as described above, the output interface circuitry was assembled and tested. The actual components are shown in the photograph of Figure 14. The seven small, square printed circuit boards are the cascaded line receiver amplifier chains which accept the output signal of the EBS (see Figure 8 for the schematic of the circuit). The six data channels are fed into a high speed buffer on a separate PC board. The seventh line receiver cascade contains the clock pulse from the target segment. The output from this board is fed into a frequency divider which selects one pulse per thousand. This is the clock pulse which triggers the high speed buffer. The buffer, while able to capture pulses of only a few nanoseconds duration, is constrained to operate at speeds much below its capacity due to limitations in subsequent components in the interface circuit. This restriction is imposed by the need to reconstruct the analog signal at the output of the interface circuit for evaluation of the operation of the A/D converter. Commercially available D/A converters are limited to data rates significantly below the 200 MHz per channel intended. In the ultimate operational configuration, the clock signal would be fed directly to the clock input of the high speed buffer with no frequency division and the buffer would operate at the full 200 MHz. The output of the buffer is sent to the final board which performs the code conversion from Gray to binary, low-speed buffering of the binary data, level shifting, and D/A conversion.



(a) 198 MHz scan without amplitude modulation.



(b) With amplitude modulation at 290 MHz. Some residual distortion in the driver amplifiers is still evident.

Figure 13. Modulated Circular Scan Pattern

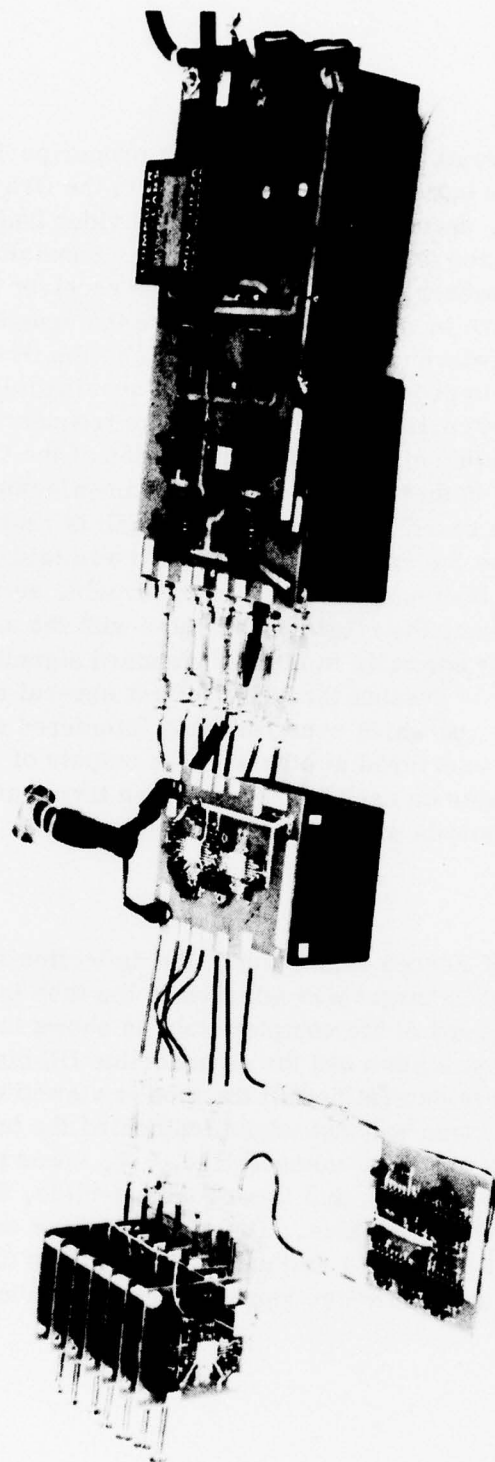


Figure 14. The output interface circuitry for the EBS A/D converter. From left to right the functional blocks are: pulse amplifiers (one per channel); frequency divider, high speed buffer, Gray-to-binary code conversion, low-speed buffer, and D/A conversion.

Each individual circuit board was tested for proper performance (correct output levels in the buffers, proper decoding in the Gray-to-binary circuit, etc.). The buffer, decoding, and frequency divider boards performed satisfactorily with no need for any design changes. Anomalous behavior, was quite apparent, however, in the cascaded line receiver boards. A number of design changes were incorporated to improve the sensitivity and reduce the hysteresis in the reference level adjustments to the first three amplifiers in the chain. These improvements resulted in substantially better performance (i.e., high gain) at certain frequencies. This frequency sensitive behavior was determined to be related to the termination of the transmission lines used on the PC board. In theory, unterminated transmission lines will work satisfactorily with high speed ECL logic if the length is restricted to less than about one inch. As the amplifier chain board was laid out, no transmission lines were longer than one-half inch, a presumable sufficient safety margin. In practice, however, the ringing associated with the unterminated lines, while not sufficient normally to disrupt standard signals, significantly degraded the low level signals present through the first several stages of the chain. The net result was ringing which constructively interfered at certain frequencies, and destructively interfered at others. The outputs of the line receivers of the first three stages on each board were then terminated in 50 ohm resistors (to -2 V) and the boards worked satisfactorily.

3.3 Target Response

Following the CRT screen evaluation of the deflection system, the screen was removed and the A/D target was attached to the tube in preparation for final testing. A photograph of the complete tube is shown in Figure 15. The tube was set up on a test station and the meanderline DC biases required to bore-sight the beam were determined (if the tube is viewed with the electron gun to the left and the vacuum exhaust tubulation behind the tube, the necessary biases are as follows: first meanderline, 5 V, lower plates positive with respect to the upper plates; and second meanderline, 22 V, front plates positive with respect to back plates. These values were established for beam potential of 13.0 kV, anode 1 and anode 2 voltages of 220 and 2590 V, respectively, and will vary somewhat depending upon the beam voltage and anode voltages.

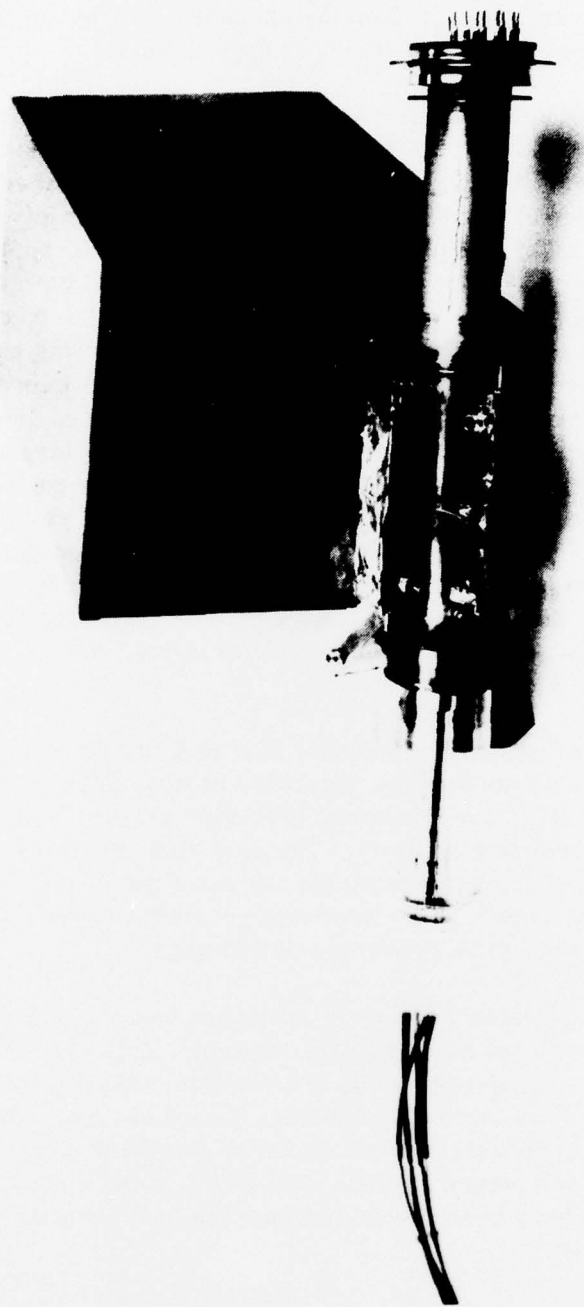


Figure 15. The EBS A/D Converter Tube. Rectangular Boxes Strapped to the Body Are Shielded 4:1 Impedance Transformers. Completed Shielding Around the Meanderline PINs Is Not Shown in This Photograph.

The next step planned was to measure the response of the individual output channels from the target wedge. However, when the input signals were applied to the deflection system, the RF interference with the output was of such a magnitude that it would completely mask the diode response (RF voltages of 0.5 V, p-p, were measured on the grounded body at the target end whereas the expected output signal was only about 30 mV).

The source of the RFI was identified as the 4:1 impedance transformers and their connections to the tube. The transformers were redesigned and encased within a metallic shield in order to reduce the field strength around the tube. This produced an order of magnitude improvement, but still left the unwanted pickup at the target end of the tube at an unacceptable level: approximately 70 mV, at least twice the anticipated signal level. In this configuration, the transformers themselves were encased in the shield, but the transition from the transformer coax to the deflection structure input pins was not shielded. Further shielding was then added to completely enclose the impedance transformer-meanderline pin structure. With seven watts of drive power on one channel, this reduced the unwanted signal pickup at the target pins to approximately 40 mV p-p. Bypassing the 4:1 transformers completely and operating the driver amplifier directly into the termination yielded a residual pickup at the target pins of about 30 mV p-p. This suggested that any further improvements in shielding would have to be made at the target end rather than at the deflection structure input pins. Shielding was therefore provided around the target pins, which reduced the RFI to about 5 mV -- an acceptable level.

The tube was then operated with a 390 ohm load resistor on the clock channel (the same termination as used on the amplifier stages of the output circuitry) at approximately 130 MHz (the frequency limitation arising from the response of the oscilloscope vertical amplifier). The resulting output signal was 30 mV peak-to-peak, which, since adjustment for the response of the oscilloscope and the reduced output at 200 MHz effectively counterbalanced each other, still would yield the desired 30 mV output at 200 MHz.

The only unexpected characteristic of the response was the abnormally high DC level associated with the diode leakage current. This placed the RF signal far enough above ground--about 100 mV--that the amplifier stages could not respond to it (the ECL logic circuits were biased between ground and -5 V). Therefore, in order to operate the line receiver amplifier stage in conjunction with the tube, it was necessary to place a DC block in the circuit. Ideally, this capacitor should have been placed between the load resistor and the input

to the first amplifier stage. However, since the layout of the PC board did not conveniently admit of such a change, it was decided simply to place a dummy load and a DC block in front of the amplifier board as shown in Figure 16.

Using the circuit of Figure 16, the EBS was operated at a scan frequency of approximately 140 MHz. The output of the line receiver amplifier board was monitored in order to determine whether or not the full ECL signal levels, necessary in subsequent stage, could be achieved. As can be seen in the photograph of Figure 17, the tube and logic circuitry did perform as required, with the output pulses of 500 to 800 mV in amplitude (ground level in the figure is the center axis of the screen). Even the lesser amplitude pulses in the photograph are sufficient to trigger a subsequent ECL logic gate since they go above -1.3 V, the approximate switching threshold for ECL gates. This demonstration represented an important confirmation of the target design and verification of the fundamental soundness of the operating concept.

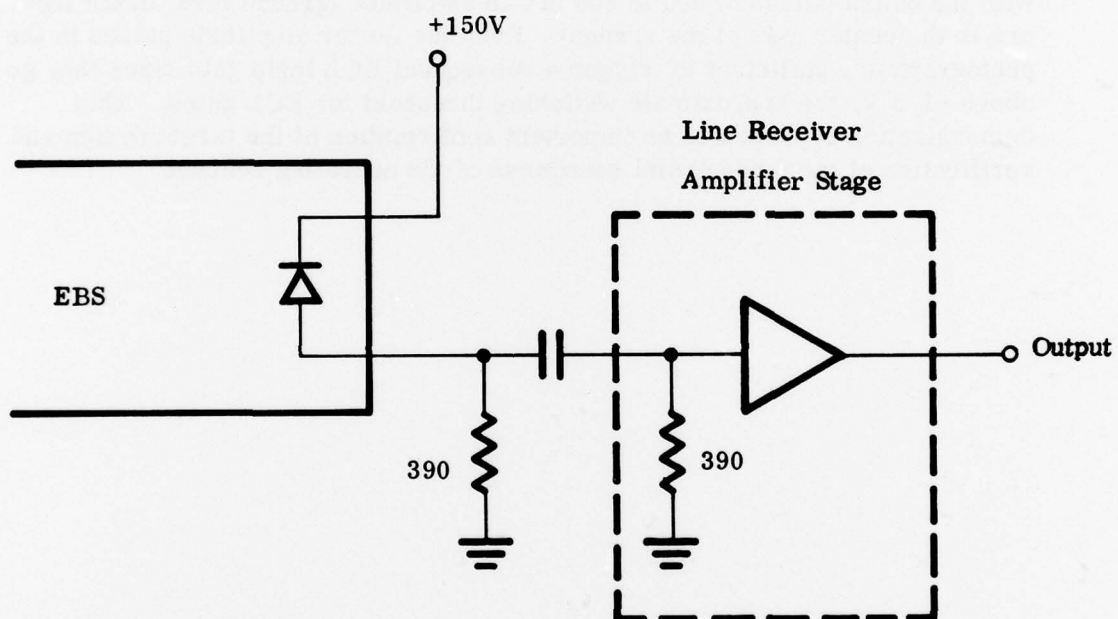


Fig. 16 Circuit used to evaluate the compatibility of the EBS A/D converter and the high-speed line receiver amplifier stages

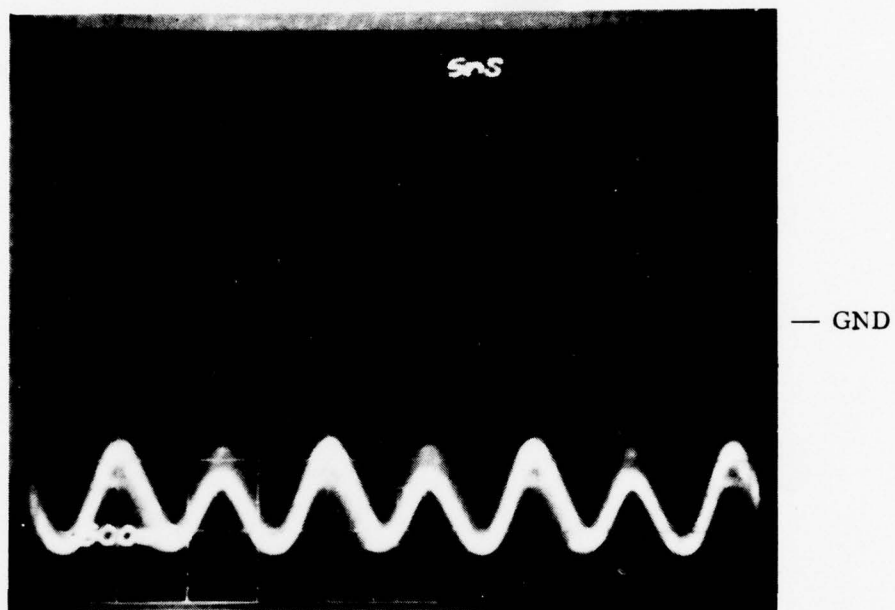


Fig. 17 Single Channel Output of the EBS A/D Converter Operating at Approximately 140 MHz. The Photograph shows the Output Signal from the Line Receiver Amplifier Stage when Driven by the Output of the EBS Itself.

Section 4

EVALUATION

Although it was not possible to fully evaluate the performance of the complete A/D converter within the time and funds available, useful judgments can be rendered on a number of the subsystems involved as well as the overall device. This section will be devoted to a summary of the performance obtained from each of the various subsystems and, based upon that performance data, recommendations on technical improvements for future versions of the device.

4.1 Deflection Structure

The deflection structure was the most intensively investigated of the subsystems involved and met a number of key performance criteria:

1. Full deflection (0.7 inch) in the target plane could be achieved with about 8 W of drive power per channel, well within the original design figure of 10 W per channel.
2. The frequency response of the deflection in the target plane from 0.15 to 1 GHz varied by only about 15%. It is believed that most of this is attributable to small impedance mismatches between the meanderlines and the 4:1 impedance transformers.
3. The deflection structures were shown to possess relatively little dispersion over the full 1 GHz bandwidth.
4. Full circular scan operation was conducted at frequencies as high as 500 MHz.

These performance characteristics verified that the basic deflection structure design was appropriate for the requirements of the device. However, in the course of building and testing the meanderlines, it became clear that two specific design changes should be incorporated in future iterations. The first concerns the construction technique used. The present structures are fabricated using a glass beading technique which is also employed in the fabrication of electron guns. With this method, the pins which support the deflection plates are embedded in a molten glass rod, which, upon cooling, tightly grips

the pins, maintaining the proper positioning of the plates. While this technique was used successfully, it proved to be a very sensitive operation. In particular, the glass frequently would not flow sufficiently around the pins of the end plates to hold them securely. It would typically take several attempts to obtain a completely tight structure (on the other hand, it was a relatively simple matter to repeat the operation: the old glass bar would simply be broken off from the pins, the plates replaced in the aligning fixture, a new glass bar placed in the beading machine, and the process repeated). Consequently, it is recommended that future designs use a ceramic rod with metallized bands in the appropriate locations. The support pins for the deflection plates would then be brazed to these metal bands, thereby forming an extremely rigid structure. This process would provide greater uniformity in the attachment of the support pins with a much higher yield of good deflection structures.

The second suggested design change affects the electrical performance of the deflection structures. The fact that the two orthogonal deflection structures are at different distances from the target plane requires that some other parameter of the deflection structures (length, spacing, drive level) be different in order to produce the same displacements at the target plane in spite of the different drift region lengths. In the original design, the spacings between the two planes of the two deflections structures were kept the same, as was the intended drive level, and the correction for the differing drift region lengths was accomplished by making the second meanderline longer than the first (2.3 inches vs 1.6 inches). Other than the difference in overall length, the two meanderlines are the same (i.e., the first 1.6 inch of the second meanderline is identical to the first meanderline). Although this design approach yielded good frequency characteristics for each meanderline, the two characteristics were not the same--e.g., local maxima in the deflection did not occur at the same frequencies, etc. In retrospect, it appears that a better approach is to make the two meanderlines identical in all respects and simply apply a larger drive signal to the second meanderline in order to compensate for the shorter drift region. This should result in very close correlation between the frequency responses of the two deflection structures.

4.2 Input Circuitry

Generally, the input circuitry to the deflection structure worked satisfactorily, as evidenced by the circular scan patterns (both with and without modulation) that were demonstrated. The key to achieving a good scan pattern is to minimize the harmonic distortion in the input circuitry, of which there are two primary sources: the mixers and the driver amplifiers. Distortion in the

mixers can be effectively eliminated by choosing very high level mixers (+23 dBm LO) for the circuit. Reduction of amplifier distortion requires operating in the linear region of the drivers. This, in turn, places certain requirements upon the insertion loss of the remainder of the circuit. The one, overriding problem in this regard was the 4:1 impedance transformers linking the 50 ohm output of the driver amplifiers to the 200 ohm input of the deflection structures. When placed back-to-back, the transformers exhibited almost 3 dB of insertion loss, forcing the driver amplifiers to operate well into the saturation region in order to provide sufficient deflection (the 500 MHz circular scan shown in Figure 12 was achieved by placing low pass filters on the driver amplifier outputs in order to eliminate the harmonic components). The crux of the problem can be seen by referring to Figure 18. This shows the physical layout of the coaxial transformers (including the DC bias lines) and the RF equivalent circuit (in the actual transformers $Z_0 = 50 \Omega$ and " $2Z_0$ " is in fact, 93Ω). The problem arises from the fact that on one of the high impedance cables, one end of the jacket is "hot", while the other is grounded. The only impediment to shunting the RF current to ground is the choking effect of the jacket inductance (and some resistance) shown as L_1 in series with R in Figure 16b. While this coaxial transformer technique has been used successfully in EBS broadband power amplifiers, the load impedance levels involved in the A/D converter transformation are so high that the impedance due to L_1 and R is no longer large compared to the effective load impedance seen at that point in the transformer. This creates a severe mismatch with its corresponding standing wave, seriously reducing the power delivered to the meanderline.

For purposes of evaluating the deflection structure, the impedance transformers were tuned by means of additional shunt capacitance to minimize the insertion loss over a narrow band (approximately 125 - 180 MHz in this case). This is obviously not an acceptable solution for broadband operation.

In summary, then, the lack of low-loss, broadband impedance transformers is the critical element in the performance of the input circuitry. Acceptable transformers must be developed before the A/D converter can operate at the high speeds of which it should be capable.

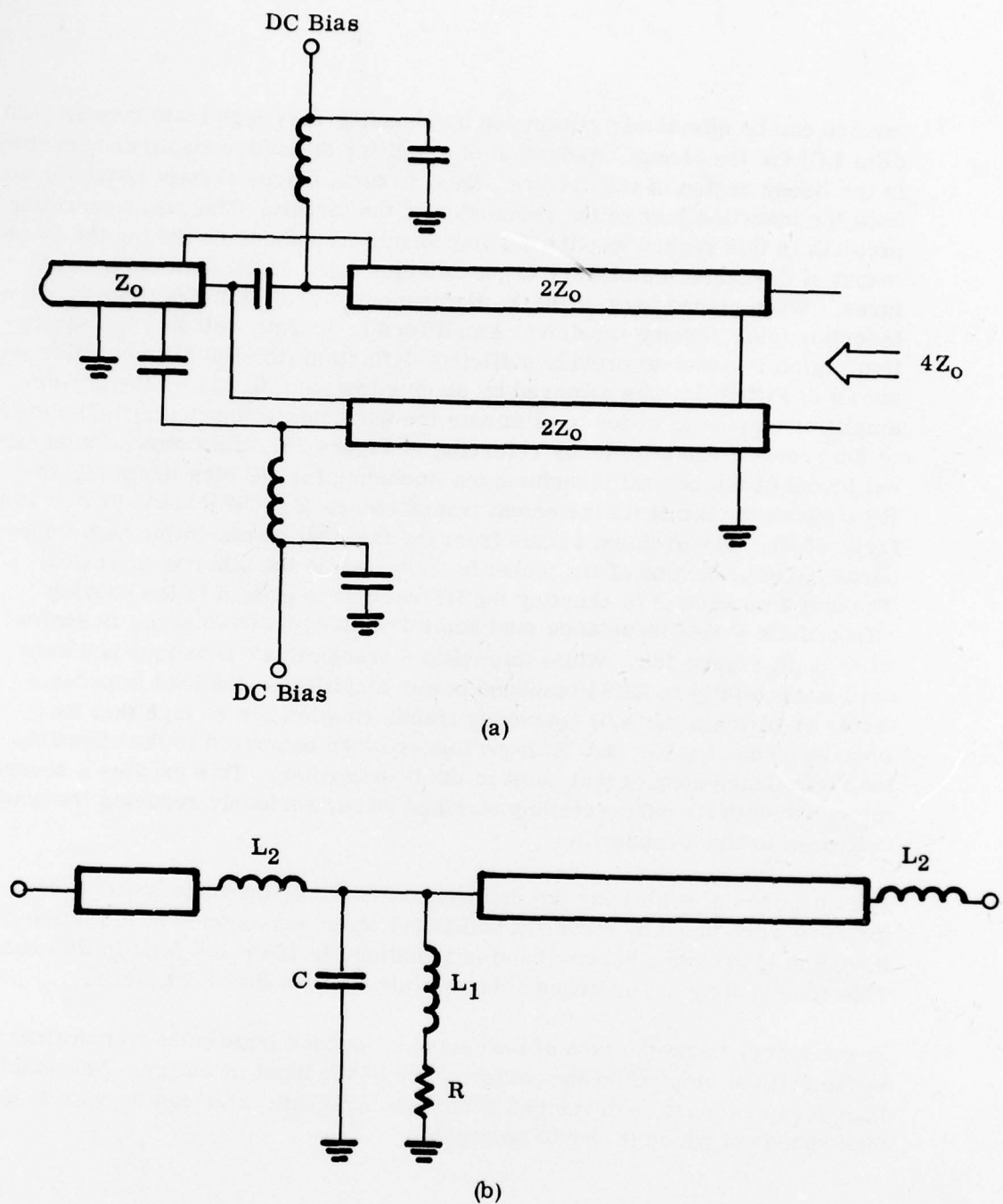


Fig. 18. 4:1 Impedance Transformers (a) shows the physical arrangement of the coaxial cables, (b) is the circuit model. L_1 and R are associated with the surface of the coaxial jacket which carries the signal at the low impedance end of the transformer. C is the shunt capacitance between the grounded jacket and the "hot" jacket. L_2 is the series inductance of the lead lengths.

4.3 Target

The semiconductor target was evaluated under actual operating conditions and performed as required. The output signals levels at a 140 MHz clock rate were sufficient to drive the interface circuit amplifiers as was shown above. Equally important was the fact that the target sectors could be fabricated with good yield in spite of the unusual topology and close tolerances required. Consequently, the semiconductor target should need no further design or process refinements.

The existing target mount, on the other hand, must undergo significant evolution in order to allow the A/D converter to reach its full potential. The present design is satisfactory for the one target wedge used in the breadboard model, and can be easily adapted to handle three target segments. However, when it becomes necessary to incorporate a greater number of segments in order to achieve the high sampling rates intended, space constraints will dictate a different technique for bringing the output lines through the vacuum wall. At this point, it appears that the preferable approach would be to have a miniature 7-pin ceramic socket for each target wedge. A seven element shielded cable would then connect the output pins with the interface circuitry.

4.4 Output Circuitry

The various functional blocks of the output interface circuit were tested individually with satisfactory results. The line receiver amplifier chain and the frequency divider board were tested using 4 ns pulses. The proper response of the remaining functional blocks to their respective input levels was verified at low speeds.

Following the individual bench tests, the line receiver amplifier chain was evaluated using the actual output from the clock channel of the EBS A/D converter at a frequency of approximately 140 MHz. The amplifier chain was the key element of the output circuitry, and it was important that its performance under actual operating conditions be satisfactory. This was indeed the case, the only modification necessary being the insertion of a DC blocking capacitor prior to the input to the amplifier board.

4.5 Summary

Although the complete evaluation of the EBS A/D converter to the extent of generating coded digital outputs corresponding to the analog input was not possible within the funds available, nonetheless, in addition to the testing of the individual elements, the A/D converter was tested as a complete unit in which all of the elements performed together as required (the exception to this being the 4:1 impedance transformers). It is felt that this result strongly supports the viability of the basic design.

Section 5

CONCLUSIONS AND RECOMMENDATIONS

From the work performed on this program, the tentative conclusion to be drawn is that the proposed A/D converter concept is feasible. The conclusion must be tentative at this point due to the fact that funding limitations curtailed the testing phase of the program to the extent that actual A/D conversion could not be demonstrated. Clearly there is still extensive engineering development to be done on the concept. However, the fact remains that the evaluation that was performed on this program, including the testing of the complete device for proper signal outputs under realistic operating conditions, verified the capability of the basic design and revealed no major technical obstacles (with the possible exception of the 4:1 impedance transformers).

In view of the above comments, it is recommended that development of the A/D converter be continued, but that the next phase be limited to a small program to specifically address the question of the impedance transformers. In particular, a 4:1 transformer (200 ohms balanced to 50 ohms unbalanced) must be built with insertion loss less than 0.5 dB up to 1 GHz. A program of this nature will focus on the area of greatest technical risk with minimum cost. The outcome of this phase can then determine whether or not further development is justified.

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