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AIR FORCE AVIONICS LAB WRIGHT-PATTERSON AFB OHIO  
DIGITAL AVIONICS INFORMATION SYSTEM (DAIS) SERIAL INPUT/OUTPUT --ETC(U)  
SEP 78 J C CAFFREY

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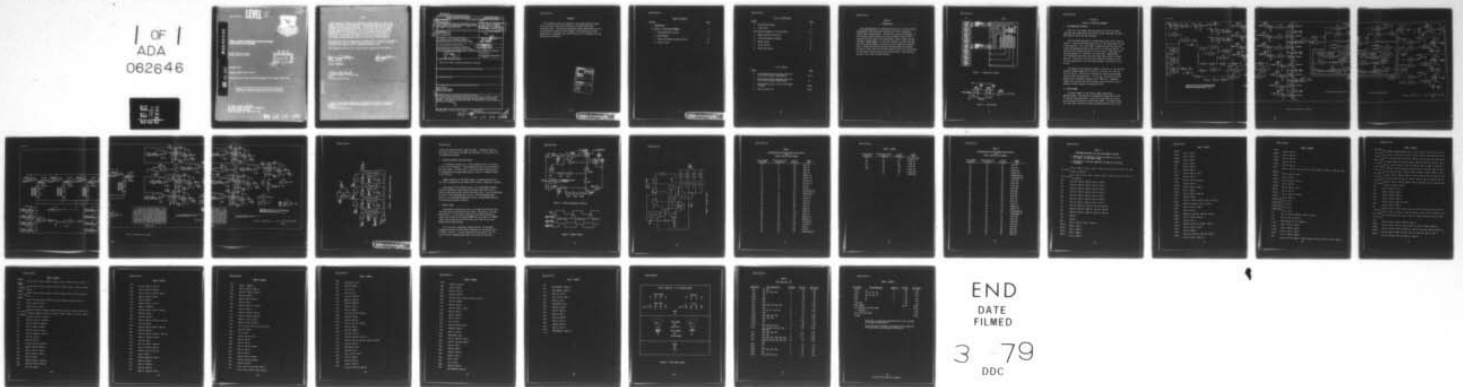
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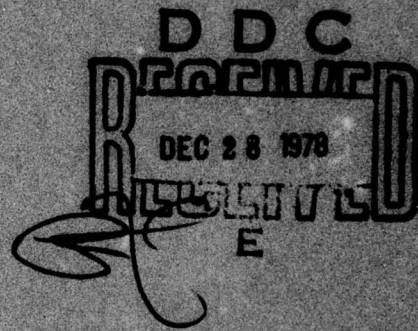
# LEVEL II

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## DIGITAL AVIONICS INFORMATION SYSTEM (DAIS) SERIAL INPUT/OUTPUT (I/O) EXERCISER

System Simulation Branch  
System Avionics Division



September 1978

TECHNICAL REPORT AFAL-TR-78-141

Interim Technical Report for Period November 1977 through January 1978

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AIR FORCE SYSTEMS COMMAND  
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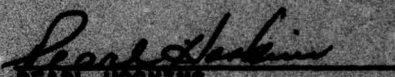
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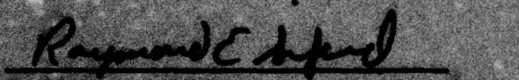
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This technical report has been reviewed and is approved for publication.

  
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) The Digital Avionics Information System (DAIS) Test Facility requires a means for exercising the serial output and input interface devices of the remote terminal. This report describes the design and operation of the unit needed to perform this function.		

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FOREWORD

This technical report was prepared in the System Simulation Branch (AAF) of the Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio. The work was accomplished under project 2052, task 03. The time period covered was from November 1977 through January 1978. Appreciation is extended to Ms. Sue Collins and Mr. Fred Delonti for the typing and illustrations.

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## SECTION I

## INTRODUCTION

This report describes the design and operation of a Digital Serial Input/Output (I/O) Exerciser of the Digital Avionics Information System (DAIS) remote terminal. The exerciser serves two purposes. In one direction, serial digital data from the Remote Terminal (RT) is checked for parity errors while simultaneously being loaded into the exerciser's buffer memory. In the other direction, the data from the exerciser's buffer memory is sent back to the RT where the received data is compared with the previously transmitted data for validity. As Figure 1 shows, the RT can transmit digital serial data from any one of four output interface devices and receive digital serial data via any one of four input interface devices.

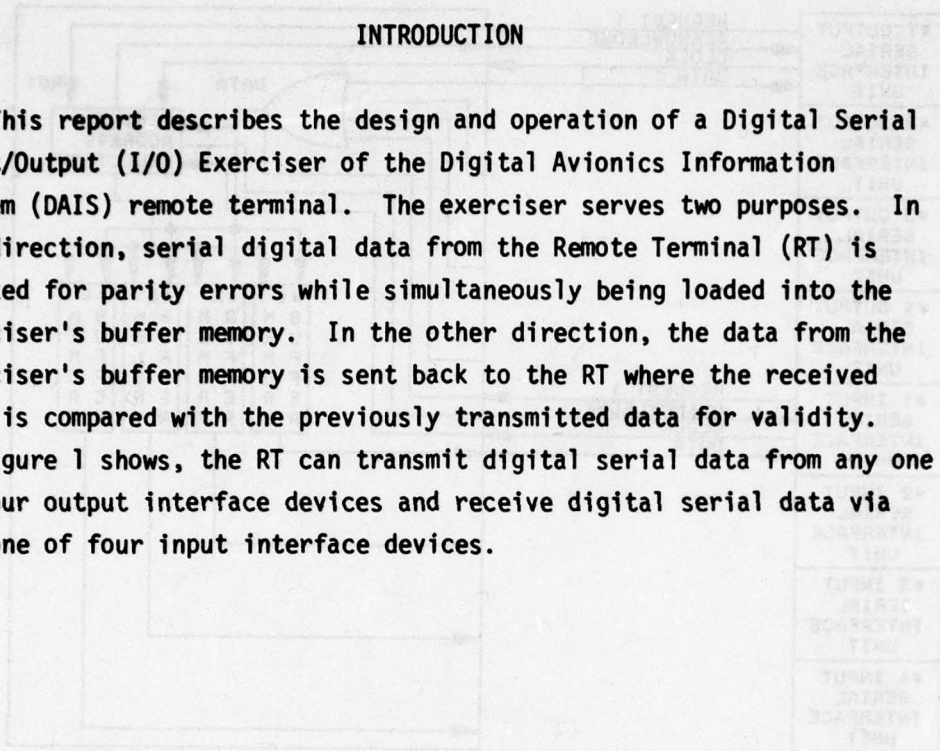


Figure 1. System Block Diagram

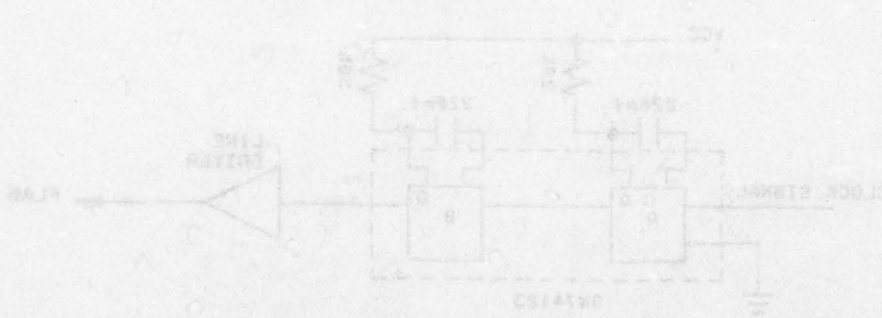


Figure 2. Logic Circuit

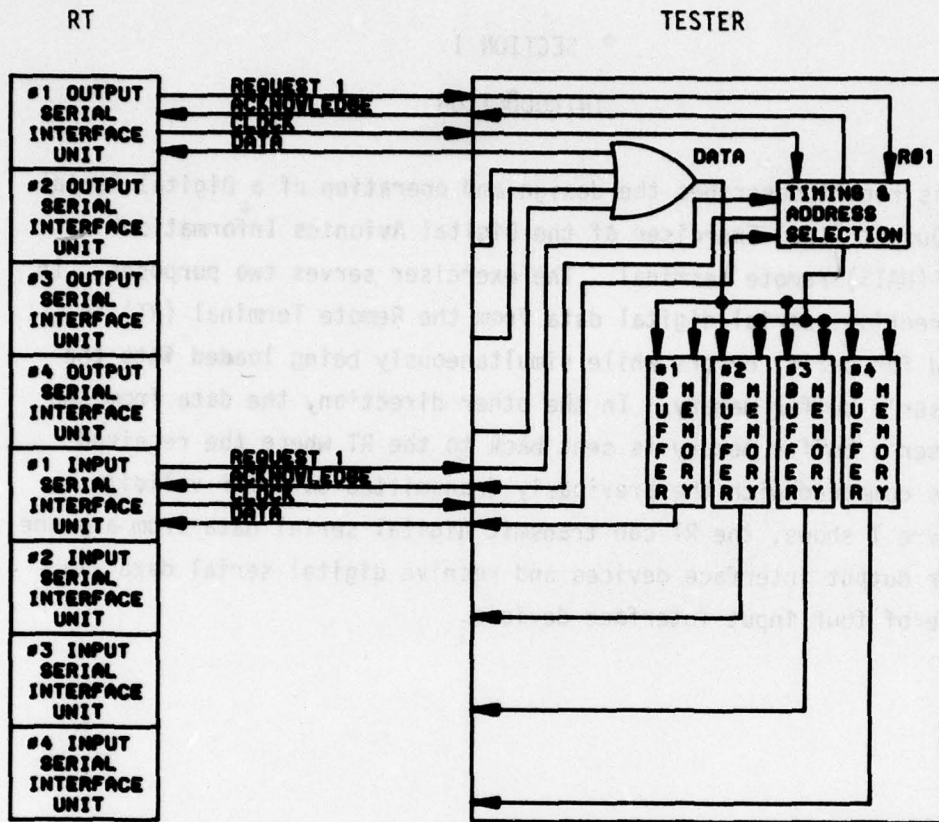


Figure 1. System Block Diagram

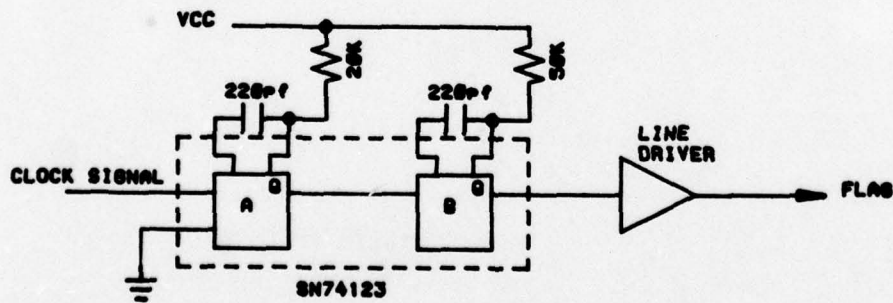


Figure 2. Flag Circuit

## SECTION II

### DIGITAL I/O EXERCISER HARDWARE

#### 1. FLAG GENERATION CIRCUITRY

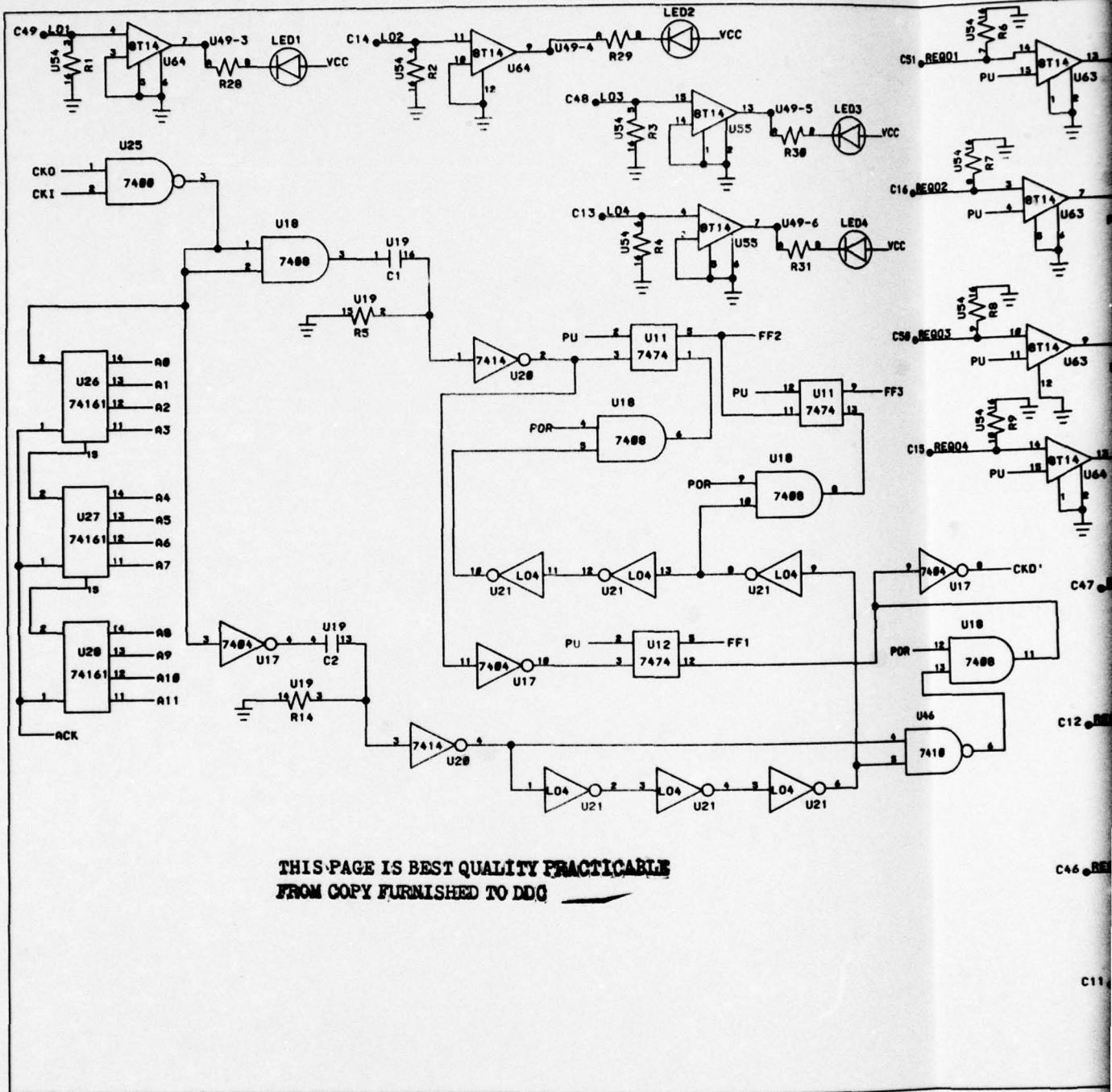
The "Flag" is a signal from the exerciser to the RT unit which indicates that a DATA output from the RT has been completed, and that a DATA input to the RT has been requested.

The flag signal generation is accomplished by the circuit shown in Figure 2. During the RT DATA output cycle, a 1 MHz clock signal is sent to the exerciser. This clock signal is applied to the flag circuitry, a dual retriggerable one-shot action (74123), as shown by Figure 2. The timing on the A section one shot is set up so that a 1 MHz signal will keep retriggering it, holding its "Q" output high. Approximately 1.5 microseconds after the clock signal stops the A section, Q output goes low. This high to low transition causes the B section one shot to fire, generating a 5  $\mu$ sec flag pulse through a line driver to the RT unit.

In reference to the detailed schematic (Figure 3a, b), the resistor capacitor network between pins 14 and 15 of  $\mu$ 43,  $\mu$ 44,  $\mu$ 51,  $\mu$ 52, and Vcc are critical. They must be selected for a time-out cycle greater than the input clock-cycle time. In this case, the time-out must be greater than 1 microsecond because of the 1 MHz clock. Component layout is not critical but the RC networks should be kept as close as possible to their respective integrated circuit.

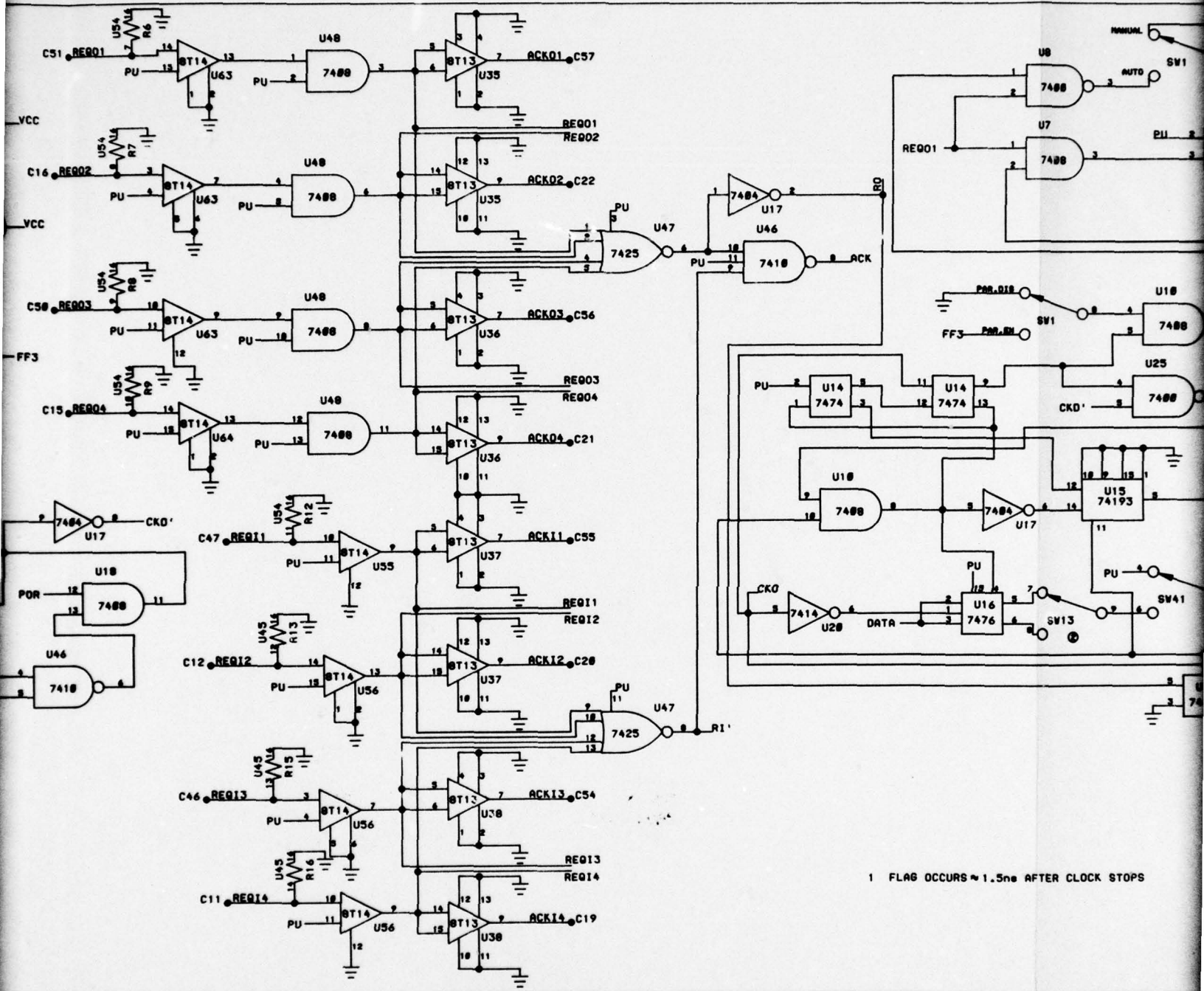
#### 2. BUFFER MEMORY

The buffer memory is four 1024-bit (RAM) random access memories (2102). Each data bit is sequentially loaded into the RAM for each RT interface device. Up to sixty 16-bit words plus parity can be entered into each of the exerciser's RAM's. As Figure 4 shows, the clock signal from the RT steps the address selection logic which



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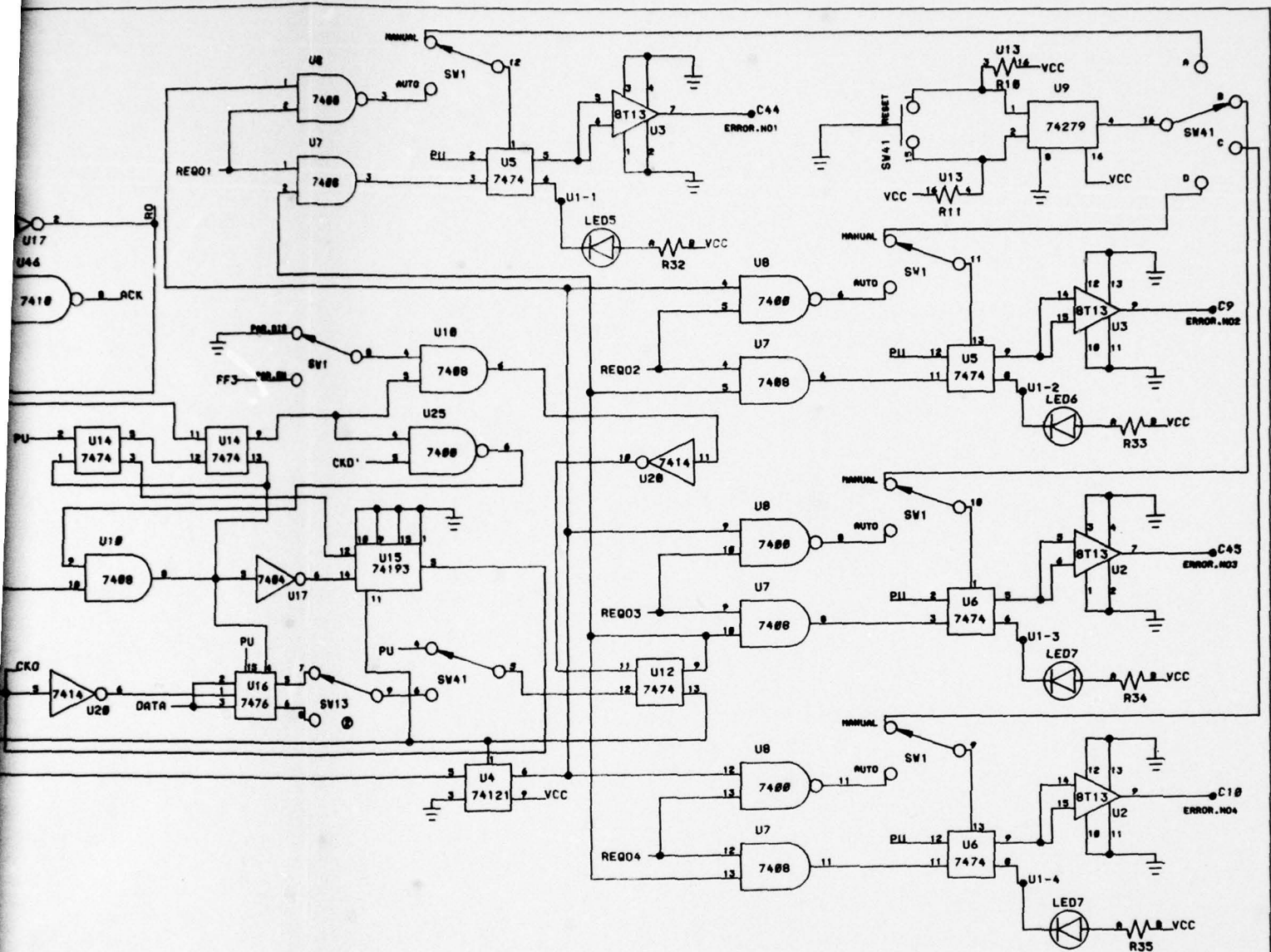
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1 FLAG OCCURS ~1.5ns AFTER CLOCK STOPS

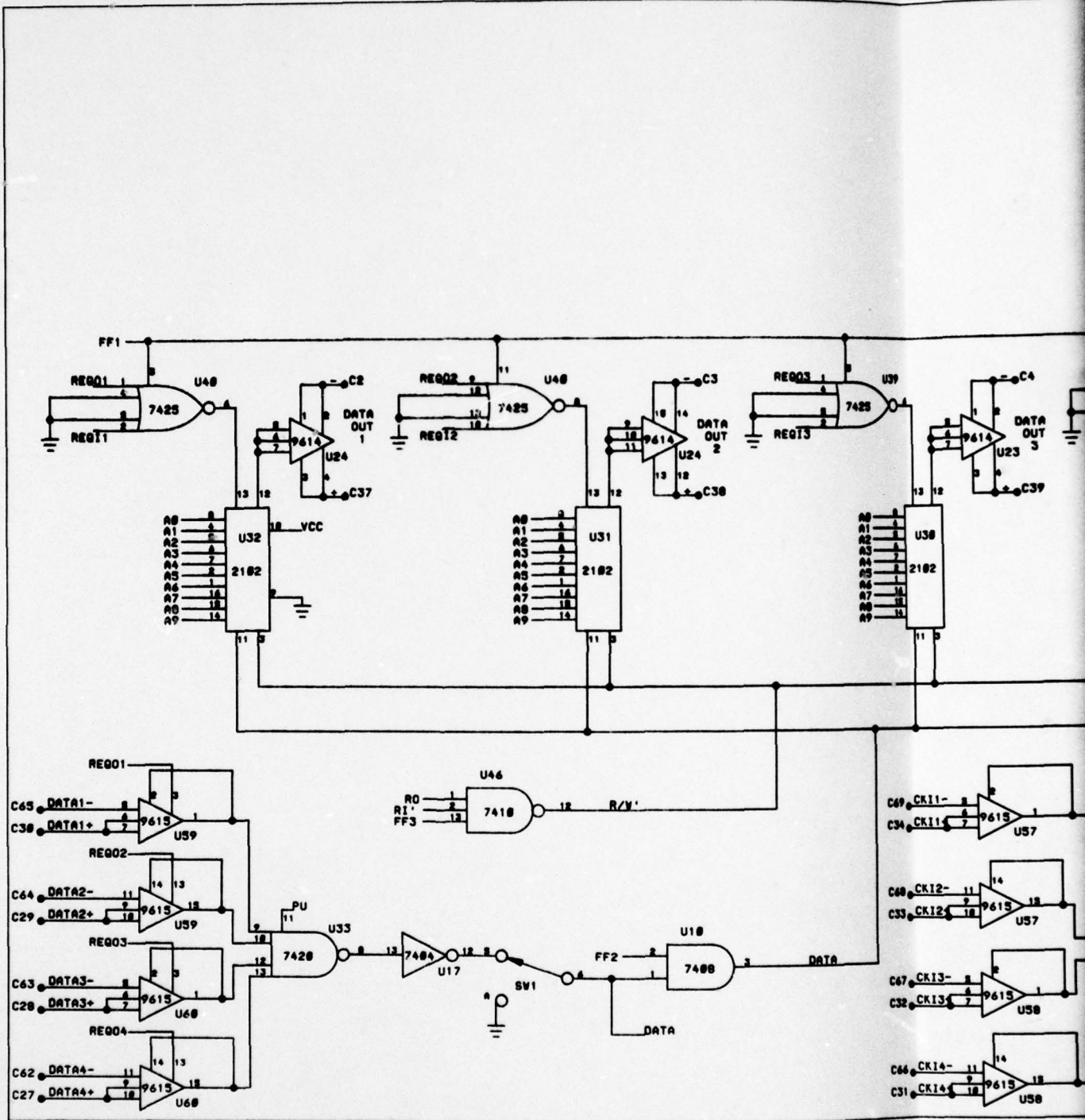
Figure 3a. Detailed Schematic of I/O Exerciser

2

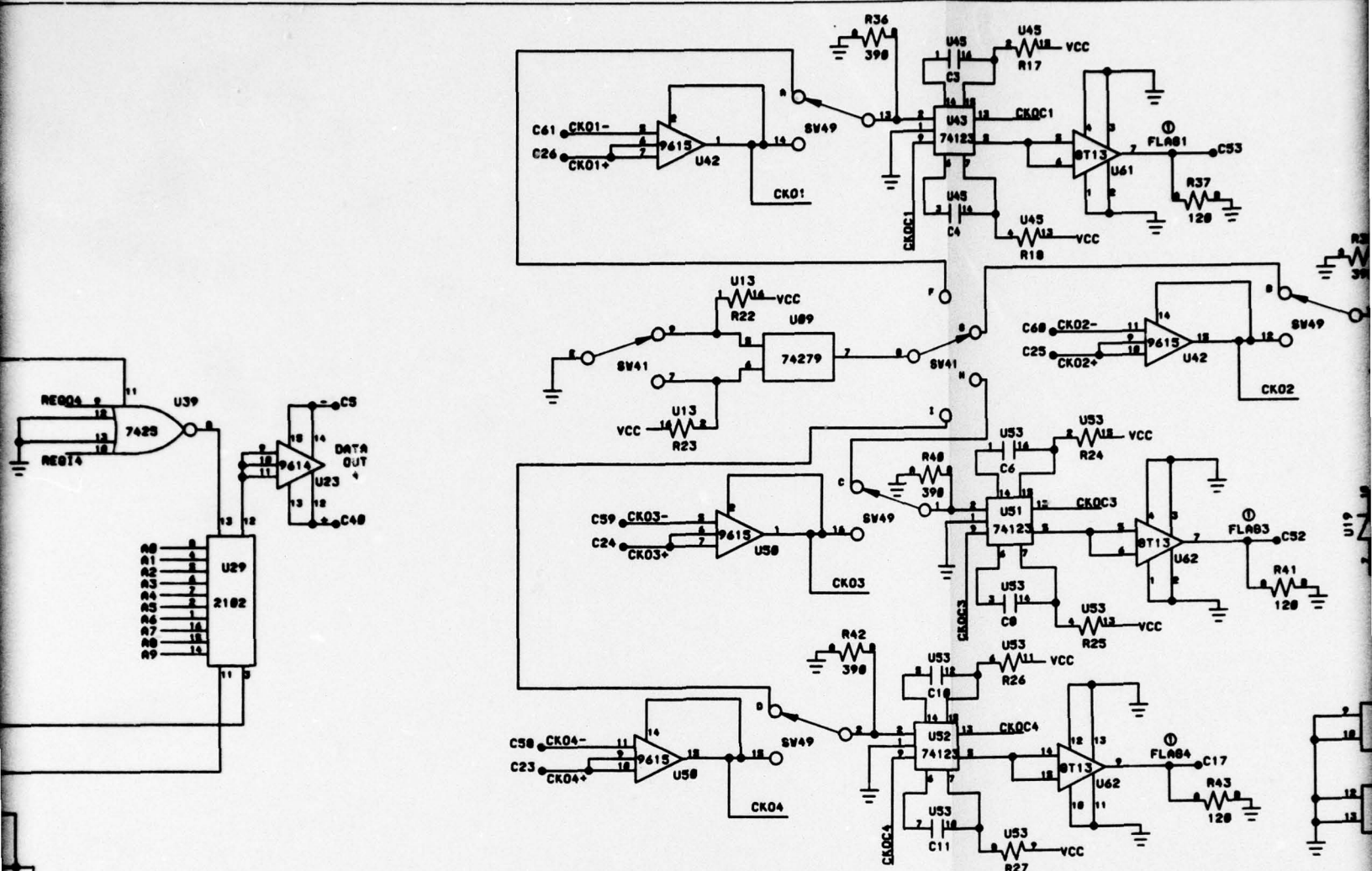


1 FLAG OCCURS ~1.5ns AFTER CLOCK STOPS

3



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	1	9	17	25	33	41	49	57
1		74279	7484	7480	7425	HEADERS		9615
2	8T13	7480	7480	74161	7425	9615	9615	9615
3	8T13	7474	R8C	74161	8T13	74123	74123	9615
4	7412	7474	7414	74161	8T13	74123	74123	9615
5	7474		74L84	2102	8T13	R8C	R8C	8T13
6	7474	7474	7437	2102	8T13	7418	750hm	8T13
7	7480	74193	9614	2102	7425	7425	8T14	8T14
8	7480	74112	9614	2102	7525	7480	8T14	8T14
	8	16	24	32	40	48	56	64

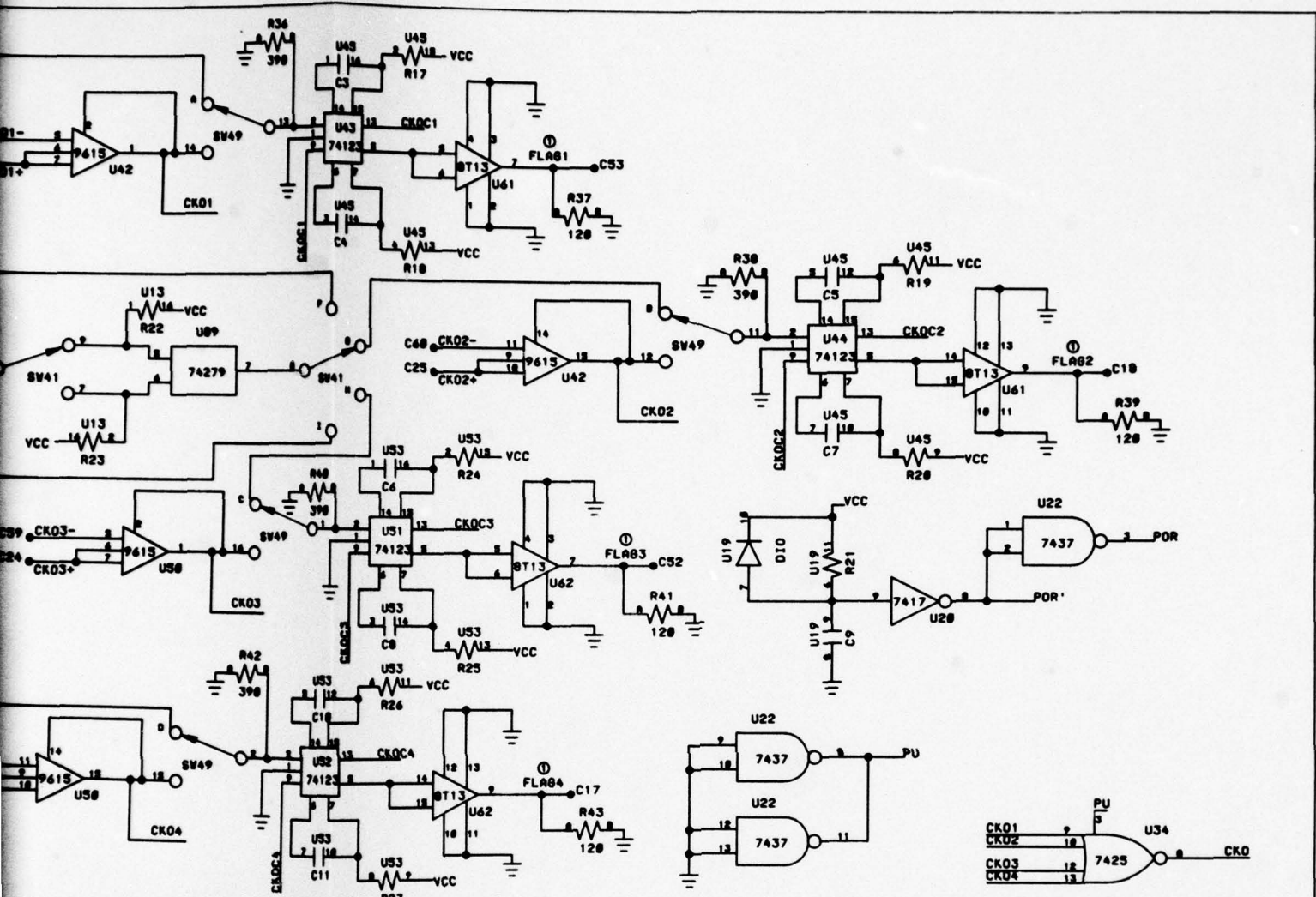
COMPONENT LAYOUT

2 TO TEST FOR ODD PARITY SHORT 13-8 TO 13-9.  
FOR EVEN PARITY SHORT 13-7 TO 13-9.

DAIS

Figure 3b. Detailed Schematic of I/O Exerciser

2



33	41	49	57
7425	HEADERS	9615	9615
7425	9615	9615	9615
8T13	74123	74123	9615
8T13	74123	74123	9615
8T13	R8C	R8C	8T13
8T13	7418	750hm	8T13
7425	7425	8T14	8T14
7525	7488	8T14	8T14
48	48	56	64

LAYOUT

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2 TO TEST FOR ODD PARITY SHORT 13-8 TO 13-9.  
FOR EVEN PARITY SHORT 13-7 TO 13-9.

# DAIS SERIAL I/O EXERCISER

3

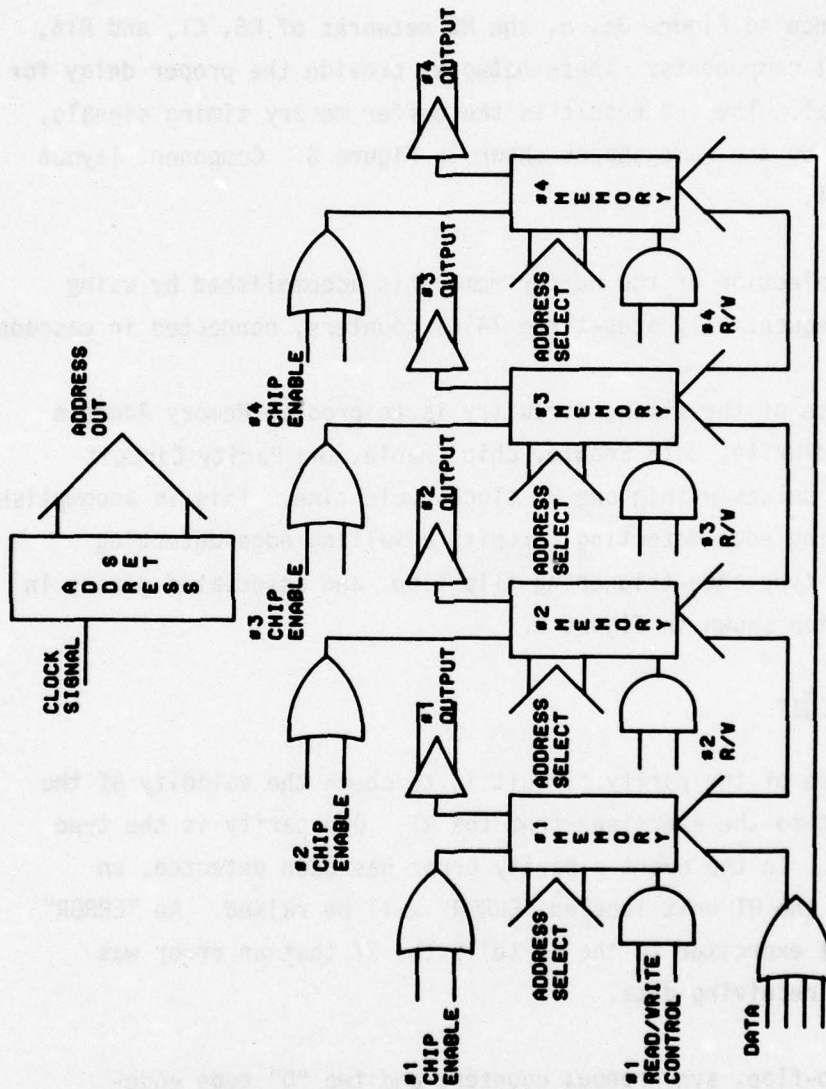


Figure 4. Memory Selection and Timing

selects the address for both input and output. The memory selection and timing logic controls the RAM to be selected, its chip enable, and the read/write functions.

### 3. TIMING AND ADDRESS SELECTION CIRCUIT

In reference to Figure 3a, b, the RC networks of R5, C1, and R14, C2 are critical components. These networks provide the proper delay for the clock signal. The end result is the buffer memory timing signals, as represented by the same shapes shown in Figure 6. Component layout is not critical.

Address selection of the buffer memory is accomplished by using the clock to sequentially step-three 74161 counters, connected in cascade.

The purpose of the timing circuitry is to produce Memory Address Selection, Read/Write, Data Enable, Chip Enable, and Parity Circuit control timing pulses within one RT clock-cycle time. This is accomplished by using a rising edge-detecting circuit, a falling edge-detecting circuit, 3 "D" type edge-triggering flip-flop, and associated gating in the configuration shown in Figure 5.

### 4. PARITY CIRCUIT

The purpose of the parity circuit is to check the validity of the data being sent to the exerciser from the RT. Odd parity is the type used by the RT. In the event a parity error has been detected, an output line to the RT unit labeled "ERROR" will be raised. An "ERROR" signal from the exerciser to the RT tells the RT that an error was detected while receiving data.

A J-K flip-flop, synchronous counter, and two "D" type edge-triggered flip-flops are the primary components of the parity circuit as shown in Figure 7. An error output will set any one of four "D" type flip-flops, depending upon which channel data was received.

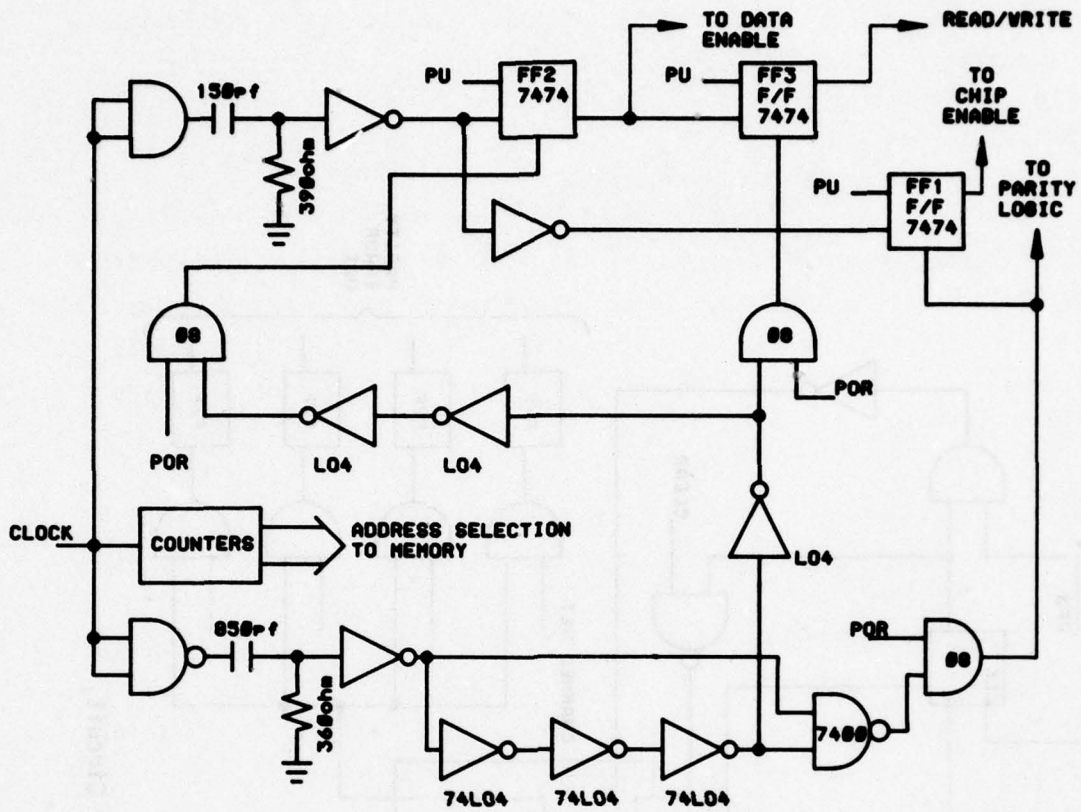


Figure 5. Timing and Address Selection

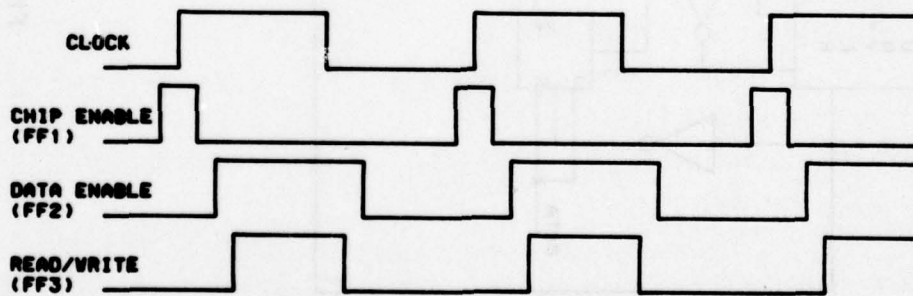


Figure 6. Memory Timing

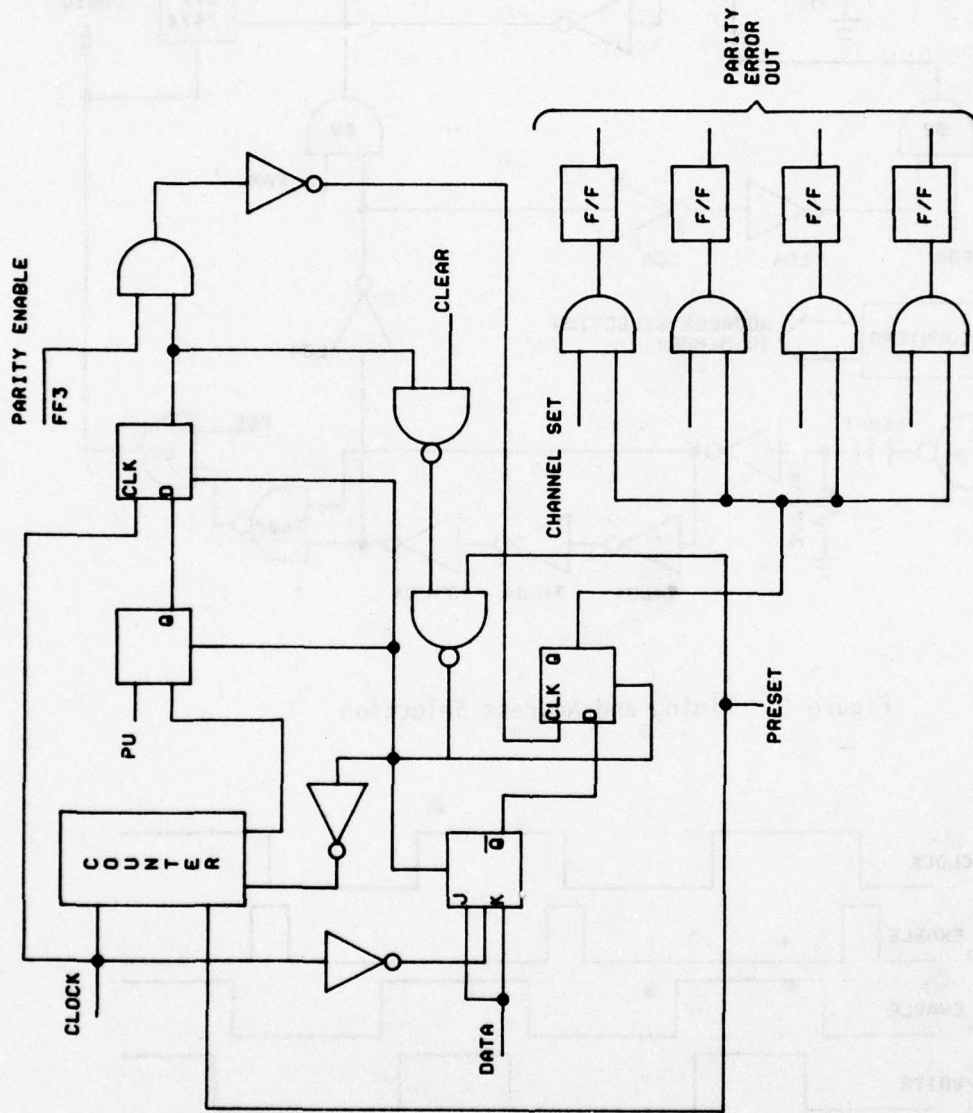


Figure 7. Parity Circuit

TABLE 1

INTERCONNECTING WIRING BETWEEN TESTER AND RT  
FOR  
SERIAL DIGITAL INPUT MODULE

Tester Module Connector	Tester Back Panel Connector	RT J9 Connector	Signal Name
2	2	127	-Data #1
3	3	88	-Data #2
4	4	117	-Data #3
5	5	120	-Data #4
11	11	123	Request #4
12	12	95	Request #2
13	13	110	Lock-Out #4
14	14	106	Lock-Out #2
17	17	111	Flag #4
18	18	112	Flag #2
19	1	98	Acknowledge #4
20	20	101	Acknowledge #2
31	31	84	+Clock #4
32	32	97	+Clock #3
33	33	109	+Clock #2
34	34	86	+Clock #1
37	37	126	+Data #1
38	38	87	+Data #2
39	39	116	+Data #3
40	40	119	+Data #4
46	46	107	Request #3
47	47	122	Request #1
48	48	94	Lock-Out #3
49	49	102	Lock-Out #1
52	52	113	Flag #3
53	53	103	Flag #1
54	54	99	Acknowledge #3

TABLE 1 (CONTD)

Tester Module Connector	Tester Back Panel Connector	RT J9 Connector	Signal Name
55	55	104	Acknowledge #1
66	66	83	-Clock #4
67	67	96	-Clock #3
68	36	108	-Clock #2
69	35	85	-Clock #1
	80	100	Signal GND
	79	8	Signal GND

TABLE 2

INTERCONNECTING WIRING BETWEEN TESTER AND RT  
FOR  
SERIAL DIGITAL OUTPUT MODULE

Tester Module Connector	Tester Back Panel Connector	RT J9 Connector	Signal Name
9	8	57	Error #2
10	10	58	Error #4
15	15	60	Request #4
16	16	79	Request #2
21	21	72	Acknowledge #4
22	22	73	Acknowledge #2
23	23	92	Clock #4H
24	24	54	Clock #3H
25	25	65	Clock #2H
26	26	76	Clock #1H
27	27	81	Data #4H
28	28	63	Data #3H
29	29	56	Data #2H
30	30	49	Data #1H
44	44	45	Error #1
45	45	70	Error #3
50	50	59	Request #3
51	51	78	Request #1
56	56	46	Acknowledge #3
57	57	51	Acknowledge #1
58	58	91	Clock #4L
59	59	53	Clock #3L
60	60	64	Clock #2L
61	43	75	Clock #1L
62	62	80	Data #3L
63	63	62	Data #3L
64	64	55	Data #2L
65	65	48	Data #1L

TABLE 3

## INTERCONNECTING WIRE LIST FOR LOGIC MODULE IN TESTER

- a) Connections to integrated circuits are shown as the chip pin number, not the socket number.
- b) Connections to discrete components are shown as the socket pin number.

+	C37-1, C38-1, C39-1, C40-1, U23-3, U23-4, U23-12, U23-13, U24-3, U24-4, U24-12, U24-13
-	C2-1, C3-1, C4-1, C5-1, U23-1, U23-2, U23-14, U23-15, U24-1, U24-2, U24-14, U24-15
A0	U26-14, U29-8, U30-8, U31-8, U32-8
A1	U26-13, U29-4, U30-4, U31-4, U32-4
A2	U26-12, U29-5, U30-5, U31-5, U32-5
A3	U26-11, U29-6, U30-6, U31-6, U32-6
A4	U27-14, U29-7, U30-7, U31-7, U32-7
A5	U27-13, U29-2, U30-2, U31-2, U32-2
A6	U27-12, U29-1, U30-1, U31-1, U32-1
A7	U27-11, U29-16, U30-16, U31-16, U32-16
AB	U28-14, U29-15, U30-15, U31-15, U32-15
A9	U28-13, U29-14, U30-14, U31-14, U32-14
A10	U28-12
A11	U28-11
ACK	U26-1, U27-1, U28-1, U46-8
ACKI1	C55-1, U37-7
ACKI2	C20-1, U37-9
ACKI3	C54-1, U38-7
ACKI4	C19-1, U38-9

TABLE 3 (CONTD)

ACK01	C57-1, U35-7
ACK02	C22-1, U35-9
ACK03	C56-1, U36-7
ACK04	C21-1, U36-9
CKD'	U17-8, U25-5
CKI	U25-2, U34-6
CKI1+	C34-0, U57-6, U57-7
CKI1-	C69-0, U57-5
CKI2+	C33-0, U57-9, U57-10
CKI2-	C68-0, U57-11
CKI3+	C32-0, U58-6, U58-7
CKI3-	C67-0, U58-5
CKI4+	C31-0, U58-9, U58-10
CKI4-	C66-0, U58-11
CK0	U14-11, U15-5, U20-5, U25-1, U34-8
CK01	SW49-14, U34-9, U42-1, U42-2
CK01+	C26-0, U42-6, U42-7
CK01-	C61-0, U42-5
CK02	SW49-12, U34-10, U42-14, U42-15
CK02+	C25-0, U42-9, U42-10
CK02-	C60-0, U42-11
CK03	SW49-16, U34-12, U50-1, U50-2
CK03+	C24-0, U50-6, U50-7
CK03-	C59-0, U50-5
CK04	SW49-15, U34-13, U50-14, U50-15
CK04+	C23-0, U50-9, U50-10

TABLE 3 (CONTD)

CK04-	C58-0, U50-11
CK0C1	U43-9, U43-13
CK0C2	U44-9, U44-13
CK0C3	U51-9, U51-13
CK0C4	U52-9, U52-13
DATA	SW1-6, U10-1, U10-3, U16-2, U16-3, U29-11, U30-11, U31-11, U32
-11	
DATA1+	C30-0, U59-6, U59-7
DATA1-	C65-0, U59-5
DATA2+	C29-0, U59-9, U59-10
DATA2-	C64-0, U59-11
DATA3+	C28-0, U60-6, U60-7
DATA3-	C63-0, U60-5
DATA4+	C27-0, U60-9, U60-10
DATA4-	C62-0, U60-11
ERROR.NO1	C44-1, U3-7
ERROR.NO2	C9-1, U3-9
ERROR.NO3	C45-1, U2-7
ERROR.NO4	C10-1, U2-9
FF1	U12-5, U39-3, U39-11, U40-3, U40-11
FF2	U10-2, U11-5, U11-11
FF3	SW1-PAR.EN, U11-9, U46-13
FLAG1	C53-1, R37-A, U61-7
FLAG2	C18-1, R39-A, U61-9
FLAG3	C52-1, R41-A, U62-7
FLAG4	C17-1, R43-A, U62-9
GND	R36-A, R37-B, R38-A, R39-B, R40-A, R41-B, R42-A, R43-B, SW1-A,

TABLE 3 (CONTD)

SW1-PAR.  
DIS, SW41-E, SW41-RESET, U2-1, U2-2, U2-3, U2-4, U2-10, U2-11,  
U2-12, U  
2-13, U3-1, U3-2, U3-3, U3-4, U3-10, U3-11, U3-12, U3-13, U4-3  
, U9-8, U  
15-10, U19-8, U19-14, U19-15, U22-9, U22-10, U22-12, U22-13, U  
32-9, U35  
-2, U35-4, U35-11, U35-13, U36-2, U36-3, U36-10, U36-11, U36-1  
3, U37-2,  
U37-3, U37-4, U37-11, U37-13, U38-2, U38-3, U38-11, U38-13, U  
39-4, U39  
-5, U39-12, U39-13, U40-4, U40-5, U40-12, U40-13, U43-1, U44-1  
, U51-1,  
U52-1, U54-16, U55-1, U55-2, U55-3, U55-5, U55-6, U55-12, U55-  
14, U56-1  
, U56-2, U56-5, U56-6, U56-12, U61-1, U61-2, U61-3, U61-4, U61  
-10, U61-  
11, U61-12, U61-13, U62-1, U62-2, U62-3, U62-4, U62-10, U62-11  
, U62-12,  
U62-13, U63-1, U63-2, U63-5, U63-6, U63-12, U64-1, U64-2, U64  
-3, U64-5  
, U64-6, U64-10, U64-12

L01  
C49-0, U54-3, U64-4

L02  
C14-0, U54-4, U64-11

L03  
C48-0, U54-5, U55-15

L04  
C13-0, U54-6, U55-4

POR  
U18-4, U18-9, U18-12, U22-3

POR'  
U20-8, U22-1, U22-2

PU  
SW41-4, U5-2, U5-12, U6-2, U6-12, U11-2, U11-12, U12-2, U14-2,  
U16-15,  
U22-8, U22-11, U33-11, U34-3, U46-11, U47-3, U47-11, U48-2, U4  
8-5, U48-  
10, U48-13, U55-11, U56-4, U56-11, U56-15, U63-4, U63-11, U63-  
15, U64-1  
5

R/W'  
U29-3, U30-3, U31-3, U32-3, U46-12

REQI1  
C47-0, U37-5, U37-6, U40-2, U47-9, U54-11, U55-9, U55-10

REQI2  
C12-0, U37-14, U37-15, U40-10, U47-10, U54-12, U56-13, U56-14

REQI3  
C46-0, U38-5, U38-6, U39-2, U47-12, U54-13, U56-3, U56-7

REQI4  
C11-0, U39-10, U47-13, U54-14, U56-10

TABLE 3 (CONTD)

REQ01	C51-0, U7-1, U8-2, U35-5, U35-6, U40-1, U47-1, U48-3, U54-7, U
59-3	
REQ02	C16-0, U7-4, U8-5, U35-14, U35-15, U40-9, U47-2, U48-6, U54-8,
U59-13,	U63-3
REQ03	C50-0, U7-9, U8-10, U36-5, U36-6, U39-1, U47-4, U48-8, U54-9,
U60-3, U6	3-10
REQ04	C15-0, U7-12, U8-13, U39-9, U47-5, U54-10, U60-13, U64-14
RI'	U46-2, U46-9, U47-8
RO	U4-5, U17-2, U46-1
VCC	LED1-B, LED2-B, LED3-B, LED4-B, R32-B, R33-B, R34-B, R35-B, U4
-9, U9-16	, U13-16, U19-10, U19-11, U32-10, U45-9, U45-11, U45-13, U45-1
5, U53-9,	U53-11, U53-13, U53-15
91	U33-13, U60-14, U60-15
92	U34-5, U58-14, U58-15
93	U34-4, U58-1, U58-2
94	U33-12, U60-1, U60-2
95	U33-10, U59-14, U59-15
96	U17-13, U33-8
97	SW1-5, U17-12
98	U34-2, U57-14, U57-15
99	U52-7, U53-8, U53-10
100	U34-1, U57-1, U57-2
101	U33-9, U59-1, U59-2
102	U52-6, U53-7
103	U52-5, U62-14, U62-15
104	U52-15, U53-6, U53-12
105	U52-14, U53-5

TABLE 3 (CONTD)

106	R42-B, SW49-2, U52-2
107	U51-7, U53-4, U53-14
108	U19-6, U19-7, U19-9, U20-9
109	U51-5, U62-5, U62-6
110	U51-6, U53-3
111	R40-B, SW49-1, U51-2
112	SW41-I, SW49-D
113	U24-5, U24-6, U24-7, U32-12
114	U32-13, U40-6
115	U31-13, U40-8
116	U24-9, U24-10, U24-11, U31-12
117	U30-13, U39-6
118	U23-5, U23-6, U23-7, U30-12
119	U29-13, U39-8
120	U23-9, U23-10, U23-11, U29-12
121	SW41-7, U09A-6, U13-2
122	U51-14, U53-1
123	U51-15, U53-2, U53-16
124	U44-7, U45-8, U45-10
125	U44-5, U61-14, U61-15
126	U44-6, U45-7
127	R38-B, SW49-11, U44-2
128	SW41-H, SW49-C
129	SW41-G, SW49-B
130	SW41-8, U09A-7
131	SW41-9, U09A-5, U13-1

TABLE 3 (CONTD)

132	SW41-F, SW49-A
133	U43-7, U45-4, U45-14
134	U44-15, U45-6, U45-12
135	U44-14, U45-5
136	U43-5, U61-5, U61-6
137	U43-6, U45-3
138	R36-B, SW49-13, U43-2
139	U43-14, U45-1
140	U43-15, U45-2, U45-16
141	U38-14, U38-15, U56-9
142	SW41-1, U9-1, U13-3
143	SW41-15, U9-2, U13-4
144	U7-2, U7-5, U7-10, U7-13, U12-9
145	LED7-B, R35-A
146	U1-4, U6-8
147	U2-14, U2-15, U6-9
148	SW1-9, U6-13
149	U6-11, U7-11
150	U21-6, U21-9, U46-5
151	U21-4, U21-5
152	U21-2, U21-3
153	U20-4, U21-1, U46-4
154	U19-3, U19-13, U20-3
155	SW13-8, U16-6
156	U4-1, U10-10, U12-13, U15-11
157	U4-6, U8-1, U8-4, U8-9, U8-12

TABLE 3 (CONTD)

158	SW1-AUTO, U8-11	281
159	LED7-B, R34-A	282
160	U1-3, U6-6	283
161	U6-3, U7-8	284
162	U12-11, U20-10	285
163	SW41-5, U12-12	286
164	SW13-9, SW41-6	287
165	SW13-7, U16-5	288
166	U16-1, U20-6	289
167	U12-12, U17-9, U18-11	290
168	U18-13, U46-6	291
169	U12-3, U17-10	292
170	U11-3, U17-11, U20-2	293
171	U17-4, U19-4	294
172	U27-15, U28-2	295
173	U21-11, U21-12	296
174	U18-10, U21-8, U21-13	297
175	U10-8, U14-1, U14-13, U16-4, U17-5	298
176	U15-14, U17-6	299
177	SW1-AUTO, U8-8	300
178	SW1-10, U6-1	301
179	U2-5, U2-6, U6-5	302
180	U10-9, U25-6	303
181	U14-5, U14-12	304
182	U14-3, U15-12	305
183	U36-14, U36-15, U48-11	306

TABLE 3 (CONTD)

184	U48-12, U64-13	801
185	U11-1, U18-6	781
186	U18-5, U21-10	061
187	U26-15, U27-2	151
188	U17-3, U18-1, U18-2, U25-3, U26-2	061
189	U11-13, U18-8	741
190	U48-9, U63-9	061
191	U10-5, U14-9, U25-4	061
192	SW1-8, U10-4	061
193	U10-6, U20-11	061
194	U5-11, U7-6	061
195	U1-2, U5-8	061
196	U3-14, U3-15, U5-9	072
197	LED6-B, R33-A	171
198	SW1-11, U5-13	171
199	SW1-AUTO, U8-6	071
200	U17-1, U46-10, U47-6	071
201	U19-2, U19-16, U20-1	071
202	U18-3, U19-1	071
203	U49-6, U55-7	171
204	LED4-A, R31-B	071
205	U48-4, U63-7	071
206	U5-3, U7-3	081
207	U1-1, U5-6	121
208	LED5-B, R32-A	081
209	SW1-MANUAL, SW41-D	081

TABLE 3 (CONTD)

210	SW1-MANUAL, SW41-C
211	SW1-MANUAL, SW41-B
212	SW41-16, U9-4
213	U3-5, U3-6, U5-5
214	SW1-12, U5-1
215	SW1-AUTO, U8-3
216	LED3-A, R30-B
217	U49-5, U55-13
218	U49-3, U64-7
219	LED1-A, R28-B
220	U49-4, U64-9
221	LED2-A, R29-B
222	U48-1, U63-13
223	SW1-MANUAL, SW41-A
~[ ]]	

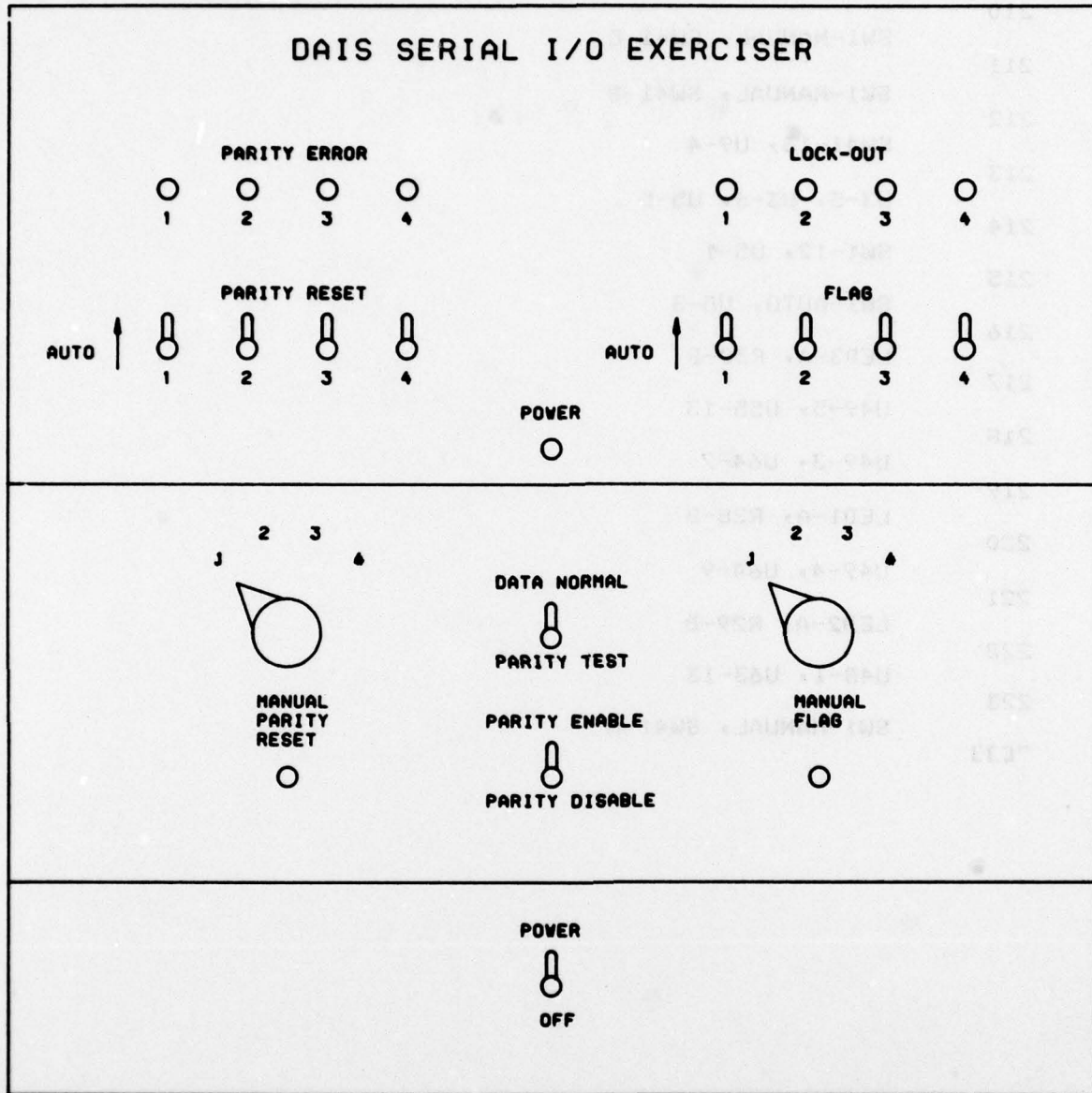


Figure 8. Front Panel Layout

TABLE 4  
PARTS AND COST LIST

<u>Type/Value</u>	<u>Ckt Location(s)</u>	<u>Quantity</u>	<u>Cost/Ea</u>	<u>Total Cost</u>
7400	U8, U25	2	\$ .30	\$ .60
7408	U7, U10, U18, U48	4	.35	1.40
7404	U17	1	.36	.36
74104	U21	1	.40	.40
7410	U46	1	.45	.45
7414	U20	1	1.21	1.21
7425	U33, U34, U39, U40, U47	5	.32	1.60
7437	U22	1	.38	.38
7474	U5, U6, U11, U12, U14	5	.41	2.05
7476	U16	1	.41	.41
74123	U43, U44, U51, U52	5	.77	3.08
74161	U26, U27, U28	3	1.32	3.96
74193	U15	1	1.43	1.43
74279	U9	1	.86	.86
2102	U29, U30, U31, U32	4	3.25	13.00
8T13	U2, U3, U35, U36, U37, U38, U61, U62	8	1.87	14.96
8T14	U55, U56, U63, U64	4	1.87	7.48
9614	U23, U24	2	2.17	4.34
9615	U42, U50, U57, U58, U59, U60	6	2.17	13.02
75Ω	R1 + R4, R6 + R9, R12, R13, R15 R16	12	.25	3.00
240Ω	R14	1	.25	.25
390Ω	R5	1	.25	.25
20KΩ	R17, R19, R24, R26	4	.25	1.00
32KΩ	R21	1	.25	.25
50KΩ	R18, R20, R25, R27	4	.25	1.00

TABLE 4 (CONTD)

<u>Type/Value</u>	<u>Ckt Location(s)</u>	<u>Quantity</u>	<u>Cost/Ea</u>	<u>Total Cost</u>
150pf	C1	1	.25	.25
220pf	C3, C5, C6, C10	4	.25	1.00
250pf	C4, C7, C8, C11	4	.25	1.00
820pf	C2	1	.25	.25
50nf	C9	1	1.00	1.00
Diode D10		1	.50	.50
Power Supply			30.00	30.00
Misc Switches for Front Panel				25.00
" Hardware " " "				5.00
LED's for Front Panel				8.00
Cabinet				15.00

Parts costs are based on approximate retail price listings at the time of fabrication.

Total time spent on project from design through completion of fabrication was approximately 294 manhours.