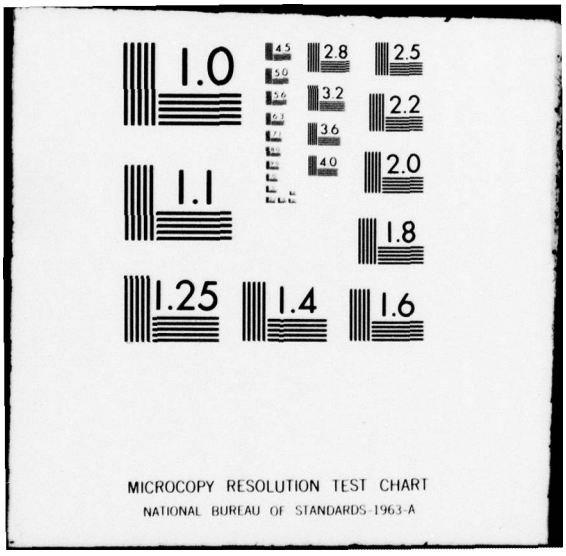
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RADIOSCIENCE LABORATORY

STANFORD ELECTRONICS LABORATORIES
DEPARTMENT OF ELECTRICAL ENGINEERING
STANFORD UNIVERSITY · STANFORD, CA 94305

SEL-78-030

# Instruction Manual for THE AUDIO-FREQUENCY TRACKING FILTER

by

(10) Evans W. Paschal

(11) September 1978

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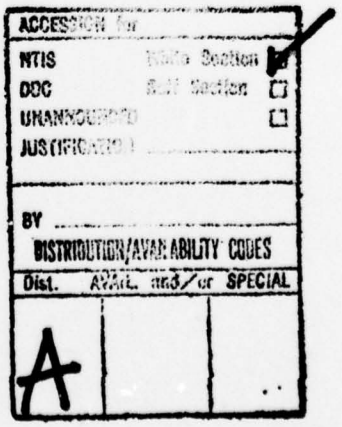
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Radioscience Laboratory
Stanford Electronics Laboratories
Stanford University Stanford, California

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This manual describes an audio-frequency tracking voltmeter developed by the VLF Radioscience Group at Stanford University for measuring the amplitudes of individual components of complex signals. It is intended as a guide to the use and maintenance of the instrument and includes operating instructions, alignment procedures, and detailed circuit descriptions.






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## ACKNOWLEDGMENTS

The Audio-Frequency Tracking Filter was constructed by the VLF Group of the Stanford University Radioscience Laboratory to aid in the analysis of very low frequency radio-propagation data.

The development of the instrument was suggested by Professor Robert A. Helliwell, the leader of the VLF Group. Mark K. Leavitt, a former graduate student at Stanford, built a tracking filter as part of his Frequency-Tracking Direction Finding system for VLF signals. Although not designed for tracking VLF signals to obtain amplitude measurements in the laboratory, his instrument has been used for this purpose for several years. To improve the performance of the tracking filter in Leavitt's system, Professor Helliwell recommended the construction of the instrument described in this manual.

Professor Malcom M. McWhorter's excellent course on the theory and design of linear active networks formed the base for the design of the filter circuits in the Tracking Filter.

Planning began in April 1975, and the system was completed in June 1977.

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# I. OPERATING INSTRUCTIONS

The 50 Hz to 30 kHz Tracking Filter (Figs. 1.1 and 1.2) is an audio-frequency narrowband voltmeter that can track an input signal as it changes in frequency while rejecting signals that may be present at other frequencies. Bandwidth, acquisition frequency, sensitivity, maximum tracking rate, and other parameters are adjustable to tailor the instrument to select and measure a particular signal component. The purpose of this Filter is to analyze very low frequency signals in conjunction with a real-time spectrum analyzer. The operator can observe the input signal and tracking frequency simultaneously on the spectrum analyzer and monitor the tracking behavior. The device generates outputs for recording signal amplitude and tracking frequency on a chart recorder.

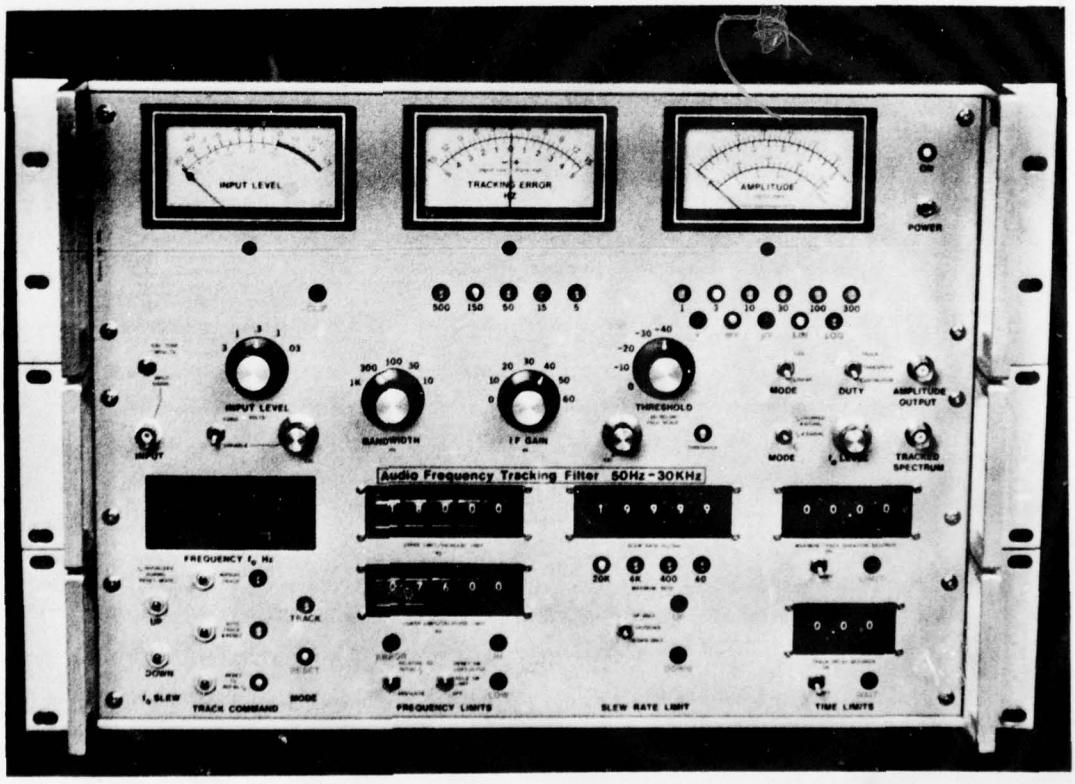



Fig. 1.1. FRONT PANEL OF THE TRACKING FILTER.

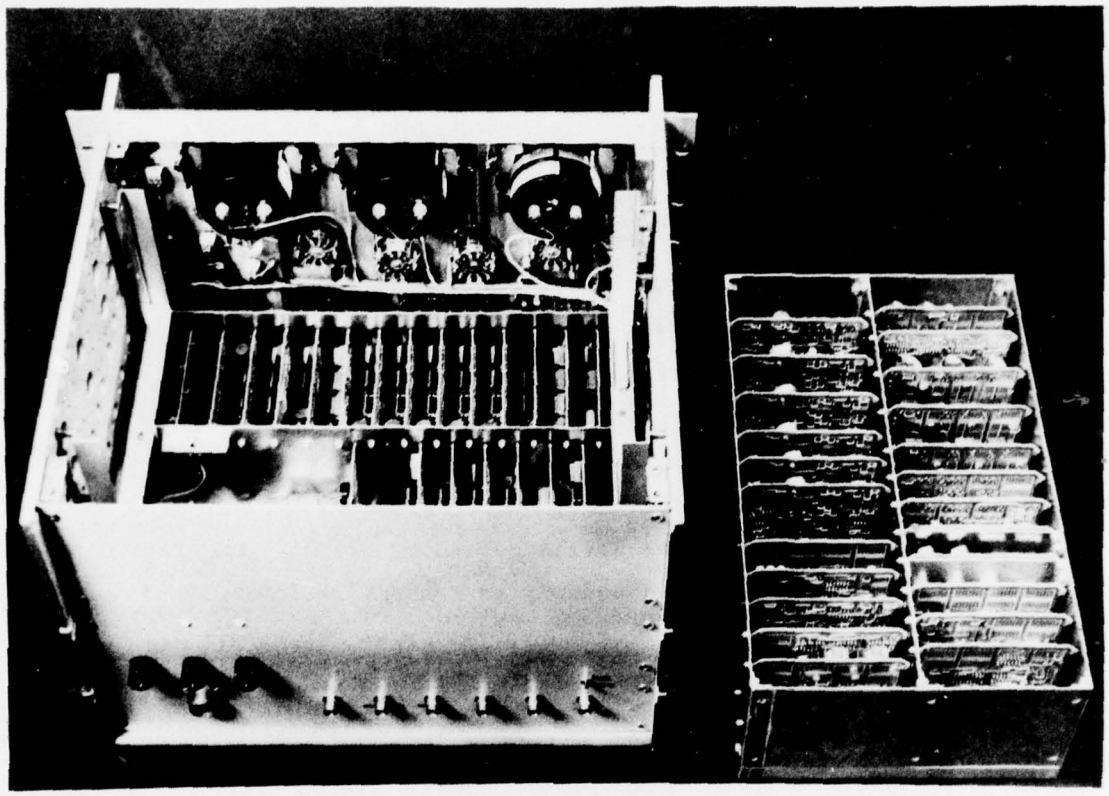


Fig. 1.2. TOP REAR VIEW WITH ANALOG CHASSIS REMOVED.

The Tracking Filter contains the following essential elements:

- frequency synthesizer whose output is mixed with the input signal to raise it to a frequency of 100 kHz
- variable-bandwidth intermediate-frequency (IF) amplifier to filter the signal
- frequency discriminator to detect filtered signal frequency variations and to control the synthesizer so that the desired signal is always in the passband of the IF amplifier

This device always operates in one of two states (or modes). In the RESET mode, the synthesizer is set to some initial or acquisition frequency $f_o$, and signals within the IF passband appear in the output; however, the discriminator is disabled, and the system will not track.

In the TRACK mode, the discriminator measures the difference between the tracking frequency $f_o$ and the strongest signal in the IF passband and causes $f_o$ to change or slew so as to reduce this difference, thus tracking the input signal in frequency. The Filter can be placed in either mode manually, or it may operate automatically--choosing the TRACK mode only when the signal in the IF passband is above a selected threshold amplitude and returning to the RESET mode when the signal amplitude falls to wait for a new signal to track.

The instrument is divided internally into two chassis; the top one contains the IF amplifier and discriminator and all of the analog signal circuits, and the bottom one contains the synthesizer, frequency control, and most of the digital circuits. The front-panel controls are arranged similarly--those on the top relate to the processing of the analog signal, and those on the bottom control the frequency-tracking behavior of the system.

## A. Connections and Controls

### 1. Input Connections

- Signal Input is a BNC connector on the left edge of the front panel. Input signals should be in the range of 30 mV to 3 Vrms. The input is differential, and the connector ring should be grounded through the cable at the source for best noise performance.

- Line is a power connection on the rear panel. A standard three-wire plug into a 120 V 50 to 60 Hz power source should be used.

### 2. Output Connections

- Amplitude Output is a BNC jack on the right side of the front panel. This output generates a dc signal proportional to the average signal amplitude in the IF passband (average-responding, calibrated as rms). The output voltage ranges from 0 to 5 V in the LINEAR mode and from -2.5 to 5 V in the LOG mode--corresponding to -60 to 0 dB from full-scale.

- Tracked Spectrum Output is a BNC jack on the right side of the instrument just below the amplitude output jack. This connection produces a signal for a real-time spectrum analyzer so that the

operator can observe the behavior of the Tracking Filter as it follows a desired signal. The input signal and a tone at the tracking frequency $f_o$ are presented simultaneously to the spectrum analyzer.

The following BNC connectors are located on the rear panel.

- IF Output is the signal from the discriminator of the selected IF filter. This output ranges from -4 to 4 V for signals on the lower and upper edges of the IF passband, respectively.
- Threshold Output is a logic-level signal (-7.5 or 7.5 V) that goes high when the filtered signal is above the chosen threshold.
- $F_{lo}$ Output is a logic-level square-wave signal from the output of the frequency synthesizer at a frequency of 100 kHz + $f_o$.
- $F_o$ Output is a 1 Vrms sine-wave signal at $f_o$.
- $F_{DC}$ Output is a dc signal from -5 to 5 V and is proportional to $f_o$ with respect to the initial or acquisition frequency. The range switch above the connector selects a span of ± 500 Hz (at 100 Hz/V) or ± 5 kHz (at 1 kHz/V) for the output. At the initial frequency (as when in the RESET mode), the output is 0 V. The $F_{DC}$ output indicates frequency changes above or below the initial frequency. If the tracking excursion is greater than the span selected, the output overflows and begins again; for example, tracking continuously upward with a ± 500 Hz span will cause a series of upward ramps at the output--each ramp covering a range of 1000 Hz. The output signal is in increments of 10 mV, with an accuracy of 5 mV.

### 3. Analog Signal Controls

The following controls relate to the amplification and filtering of the analog signals and are located on the top half of the front panel.

- Input Select Switch, just above the input connector, selects either the input signal or a 5 kHz CAL TONE at 0.1 Vrms. The calibration tone can be used as a known source to calibrate the output level for the chart recorder.
- Input Level Range Switch sets the input gain of the Tracking Filter. It is calibrated for input signals of 3, 1, 0.3, 0.1, and 0.03 V full-scale.

- Variable Attenuator and Select Switch are a toggle switch and a variable control located just below the input level range switch, and they provide variable attenuation of the input signal. In the FIXED position, the attenuator is disabled; in the VARIABLE position, it is enabled and can produce greater than 12 dB variable attenuation. The CAL position indicates 0 dB attenuation.

- Input Level Meter displays the average level of the input signal. For best dynamic range, the input range and attenuation should be set so that the meter reads as close to maximum as possible without going into the red region at the top of the scale. Zero VU indicates a full-scale input level.

- Clip Indicator is a light just below the input level meter. Signals above the maximum operating level of the input stage are clipped to prevent overdriving subsequent circuits. This light will flash momentarily with impulsive noise (such as sferics) but should normally be off. Distortion occurs when the input is clipped; the clip light should flash only on sferics, therefore, and not because of strong VLF stations in the input data, or spurious intermodulation components may result.

- Bandwidth is the control that selects the width of the IF amplifier passband. The passband is centered about $f_o$, and its 3 dB bandwidth (BW) can be 1 kHz or 300, 100, 30, or 10 Hz. Signals within 1/2 BW of $f_o$ are passed, but signals farther away are attenuated with an attenuation of at least 60 dB at 3 BW from $f_o$. Selection of the IF bandwidth also determines the maximum tracking slew rate and the minimum tracking frequency (1/2 BW or 50 Hz, whichever is greater).

- Tracking Error Meter displays the output of the selected discriminator to demonstrate the difference between the tracking frequency and the strongest input signal in the IF passband. Its range varies with the IF bandwidth ($\pm$1/2 BW full-scale), and the scale factor is indicated by the scale lights below it. The discriminator will not respond to very weak signals; however, its output (and, therefore, meter reading) is valid if the tracked signal is greater than -60 dB from full-scale output.

- IF Gain is a switch that controls the gain of the IF amplifier. Because tracked signals may comprise only part of the total signal input to the system, it is often useful to increase the IF gain to maximize the output of the Tracking Filter. This gain is adjustable in steps of 10 dB from 0 to 60 dB and should be set to obtain the maximum reading on the amplitude output meter without overdriving it.

  CAUTION: too much IF gain will cause spurious responses to become visible in the output. Instrument-generated spurs are generally at least 80 dB below the maximum operating level except in the 10 Hz position where they are down only 60 dB. Spurious responses

caused by synthesizer spurs mixing with input-signal components may be down only 60 dB. More than 30 dB IF gain should not be used unless precautions are taken to identify or eliminate the spurious responses.

- Threshold Controls set the threshold for automatic tracking. The signal amplitude in the IF passband is compared to the setting of these controls, and the THRESHOLD light turns on when the desired signal is above the threshold. The threshold range switch has five positions in 10 dB steps from 0 to -40 dB below the maximum output level; the variable control below this switch can lower the threshold an additional 13 dB. Threshold levels are with respect to signal amplitudes as indicated on the amplitude meter.

- Amplitude Meter displays the average signal amplitude in the IF passband. In the LOG mode, the meter range is limited to -40 to 0 dB (signals below -40 dB will read off-scale); it has an additional scale that shows the voltage at the amplitude output connector. Scale lights indicate the sensitivity of the system and the output mode.

- Amplitude Mode Switch determines whether the output is linear or logarithmic. In the LINEAR mode, the output level is from 0 to 5 V which generates an amplitude meter reading from 0 to full-scale. In the LOG mode, the output level ranges from less than -2.5 to 5 V at 0.125 V/dB.

- Amplitude Output Duty Switch affects only the signals at the amplitude output jack--the meter reading does not change. This switch inhibits the amplitude output when the system is not tracking a desired signal so as to clean up the chart recorder trace. In the CONTINUOUS position, signal amplitude is continuously available at the output connector. In the THRESHOLD position, signals are presented to the output only when the tracked signal is above the threshold; otherwise, the output is at 0 V. In the TRACK position, they are available at the output only when the system is in the TRACK mode.

- Tracked Spectrum Mode is a switch that controls the signal output of the tracked spectrum connector. In the $f_o$ position, only the $f_o$ tone is available at the output. In the $f_o$ & SIGNAL position, the tone is added to the input signal and the sum is output. In the $f_o$ CHOPPED & SIGNAL position, the tone is chopped at a 10 Hz rate and added to the input signal, and the tracking frequency will appear as a dotted line on the spectrum analyzer display.

- $f_o$ Level is the control that sets the amplitude of the $f_o$ tone in the tracked spectrum output. It should be adjusted so that the tracked frequency tone and the input signal both appear dark on the spectrum analyzer display. Note that the input signal level at the tracked spectrum output depends on the setting of

the input level controls. Changing these controls will necessitate adjustment of the $f_o$ Level control for equal signal brightness. In the $f_o$ CHOPPED & SIGNAL position, it may be necessary to reduce the input signal level slightly so that $f_o$ tone chopping can be observed.

4. Frequency and Tracking Controls

The following controls affect the frequency tracking behavior of the system.

- Frequency $f_o$ Display is a numeric readout that presents the instantaneous frequency generated by the frequency synthesizer and the frequency of the signals in the IF passband. In the RESET mode, the display will be stable and will indicate the initial $f_o$ or acquisition frequency. In the TRACK mode, the display will be constantly changing while the signal is being tracked.

- $f_o$ Slew Pushbuttons are labeled UP and DOWN and enable the operator to manually vary the frequency of the Tracking Filter. In the RESET mode, slewing will alter the initial $f_o$. In the TRACK mode, the tracking frequency will be temporarily changed (except while tracking with a 1 kHz or 300 Hz bandwidth when the manual slew may not be able to overcome the corrective action of the discriminator). Slewing occurs at 10, 100, and 1 kHz/sec during the first 3 sec when the slew buttons are held on and at 5 kHz/sec thereafter. When making small frequency changes, it will be necessary to press the buttons in short bursts to reach the exact frequency required.

- Track Commands and Mode are three pushbuttons used to select the mode of tracking operation. The lights next to these buttons indicate the present command, and the mode lights to the right indicate the actual tracking mode. The RESET TO INITIAL $f_o$ command places the Tracking Filter in the RESET mode and resets the synthesizer to the initial or acquisition frequency. The operator can now change the initial frequency through the manual $f_o$ slew buttons. The MANUAL TRACK command places the Tracking Filter in the TRACK mode where the input signal in the IF passband will be continuously tracked until it falls below the discriminator threshold, at which point the system will slew randomly as it attempts to follow noise. Operating the slew buttons in this mode will vary the tracking frequency but will not alter the initial $f_o$. The AUTO TRACK & RESET command causes the system to track signals only when they are above the threshold set by the threshold controls. When signal levels fall below the threshold, the system reverts to the RESET mode and the synthesizer returns to the initial $f_o$.

- Frequency Limit Section controls the maximum and minimum frequencies at which signals can be tracked. There is an implicit upper bound of 30 kHz and a lower bound of 1/2 BW or 50 Hz, depending on which is greater. The Tracking Filter cannot be made to operate beyond these bounds.

  - Upper Limit/Increase Limit and Lower Limit/Decrease Limit Controls are thumbwheel switches set to the upper and lower frequency limits for tracking.

  - Relative to Initial $f_o$/Absolute Switch determines the interpretation of the limit controls. In the ABSOLUTE position, the frequency limits are considered as absolute frequencies; in the RELATIVE position, they are considered as changes with respect to initial frequency. For example, if the lower limit/decrease limit control is set to 1000 Hz, the tracker in the ABSOLUTE position would never drop below 1000 Hz and, in the RELATIVE position, it would never go more than 1000 Hz below the initial frequency.

  - Mode Switch has three positions. In OFF, the frequency limits are ignored; however, the implicit bounds of 30 kHz and 50 Hz or 1/2 BW are still in effect. In HOLD ON LIMIT, tracking stops when the frequency limit is reached, but the instrument remains in the TRACK mode. In RESET ON LIMIT (AUTO), the system goes to the RESET mode when the limit is reached if it is tracking in response to the AUTO command.

  - Hi and Low Lights indicate when the upper or lower frequency limits are reached. In the RESET ON LIMIT mode, they may flash only briefly because the Tracking Filter is reset as soon as the limit is reached. These lights will also turn on when the implicit bounds are reached.

  - Error Light flashes to indicate that the initial $f_o$ has been set outside the frequency limits or that the frequency limit switches are set improperly; to correct the error, either move the initial $f_o$ or change the limit switches. This light will flash in the RELATIVE position if the decrease limit setting represents a negative frequency limit for a given initial $f_o$ or if the increase limit setting represents a frequency greater than 100,000 Hz. It will also flash if the internal bound disable switch has been left in the ALIGN position after synthesizer alignment.

- Slew Rate Limit Control will limit the maximum rate at which the frequency synthesizer will change frequency and, therefore, the maximum slew rate of the tracked signals. The maximum possible slew rate depends on the IF bandwidth (which determines the time delay of signals passing through the system) and is indicated by scale lights below the control. This slew rate is 20 kHz/sec with 1 kHz or 300 Hz BW, approximately 3.5 kHz/sec with 100 Hz

BW, 350 Hz/sec with 30 Hz BW, and 35 Hz/sec with 10 Hz BW. The slew rate limit control is in addition to the limitation based on bandwidth and is only effective for settings below the system maximum at a given bandwidth. To achieve the maximum possible slew rate, set this control to 19999 Hz/sec.

- Up/Down Control is a three-position switch that controls the slewing direction. In the UP/DOWN position, the system will track signals moving both upward and downward in frequency. In UP ONLY or DOWN ONLY, slewing will occur only to higher or lower frequencies, respectively. Note that this switch controls the direction of possible frequency change during tracking in contrast to the frequency limit controls that determine the amount of change.

- Up/Down Lights indicate that slewing is limited by the slew rate limit circuitry in a given direction. This usually means that the signal is changing faster than the setting of the slew rate limit or that slewing is requested in a prohibited direction. These lights will also turn on if the Tracking Filter has reached a frequency limit and is unable to continue in that direction.

- Time Limit Controls provide time limits when tracking follows an AUTO command.

  - Maximum Track Duration sets the maximum time for the system to track automatically before being reset. Time is adjustable in 10 msec increments to 99.99 sec. The LIMIT light comes on for approximately 0.8 sec when maximum duration is reached and the system returns to the RESET mode. The switch is set to OFF to ignore this maximum.

  - Track Delay introduces a fixed delay time after the THRESHOLD light is on before tracking actually begins. The delay is adjustable in 10 msec steps to 9.99 sec, and the WAIT light turns on during the delay. This control can prevent premature tracking of complex signals by ignoring risers on the leading edge of a pulse signal or rejecting the first component of a multipath whistler. The switch is set to OFF to disable the delay.

## B. Measurement Process

The following steps should be taken to obtain measurements with the Tracking Filter.

1. Turn on the Tracking Filter

- Various lights will appear.
- Frequency display will probably show 30,000 Hz.

2. Calibrate Chart Recorder Amplitude Output

- Connect the amplitude output connector to the chart recorder input for the amplitude channel.
- For the LINEAR mode output, the chart recorder gain should be set for an approximately 5 V span; use a slightly larger span for the LOG mode output.
- Place the Tracking Filter in the RESET mode by pressing the RESET command button.
- Slew the tracking frequency to 5000 Hz.
- Select the CAL TONE 5 kHz input.
- Set the input level switch to 0.1 V and disable the attenuator by moving the switch to the FIXED position.
- Adjust the IF gain to 0 dB and select the desired bandwidth. The system is now measuring the 5 kHz CAL TONE and should produce a full-scale reading on the output meter.
- Move the output duty switch to CONTINUOUS. The output to the chart recorder is now 5 V which represents a full-scale output.
- Set the input level switch to the 0.3, 1, and 3 V positions to generate output levels of 10, 20, and 30 dB below full-scale.
- Move the duty switch to TRACK to obtain a 0 V output.
- Adjust the chart recorder gain and zero for the correct chart trace.

3. Calibrate Chart Recorder Frequency Output

- Connect the $f_{DC}$ output on the rear panel to the chart recorder input for the frequency channel.
- Set the $f_{DC}$ range switch on the rear panel for a $\pm$ 500 Hz or $\pm$ 5 kHz span. When the Filter is in the RESET mode, the $f_{DC}$ output is 0 V which represents the initial frequency.

- Move the slew rate limit control to 00000 Hz/sec to prevent slewing and press the TRACK command to place the instrument in the TRACK mode.

- Manually move the tracking frequency $f_o$ up and down with respect to the initial value by the UP and DOWN pushbuttons and adjust the chart recorder for the correct scale factor.

For a full-scale reading of ± 500 Hz about the initial frequency, the following steps are required.

- Set the range switch to ± 500 Hz.

- Assume the initial frequency is 5000 Hz and increase $f_o$ (while in the TRACK mode) to 5500 Hz. The $f_{DC}$ output will now be 5.00 V --representing $f_{initial}$ + 500 Hz.

- Reduce $f_o$ to 4501 Hz. The $f_{DC}$ output will now be -4.99 V--representing $f_{initial}$ - 499 Hz.

- Decrease $f_o$ to 4500 Hz. The $f_{DC}$ output will underflow and return to 5.00 V.

- Press the RESET command; $f_o$ will reset to 5000 Hz, and again $f_{DC}$ = 0 V.

Any initial frequency can be used for the calibration, and the results will be the same.

4. Set Input Level

- Choose the input signal with the input select switch.

- Adjust the input level switch so that the maximum input does not exceed 0 VU on the input level meter. The CLIP light should be off except for brief flashes caused by sferics.

- Use the variable attenuator if necessary to set the input gain exactly.

5. Adjust Tracked Spectrum

- Connect the tracked spectrum output to the spectrum analyzer input.

- Turn the $f_o$ level control fully counterclockwise to attenuate the $f_o$ tone and set the tracked spectrum mode to $f_o$ & SIGNAL.

- Adjust the spectrum analyzer for the correct display of the input signal.

- Set the instrument into the RESET mode through the RESET command and slew $f_o$ until it is at the required acquisition frequency for the signals to be tracked.

- Increase the $f_o$ level control until the $f_o$ signal is visible on the spectrum analyzer display. If the $f_o$ CHOPPED & SIGNAL mode is to be used, it may be necessary to tweak the spectrum analyzer gain and $f_o$ level control slightly so that $f_o$ chopping is clearly visible; it may not be visible if the analyzer channel bandwidth is less than 10 Hz.

6. Determine Frequency Control Parameters

- Set the frequency limit switches, slew rate limit, and track duration and delay (if desired) to the appropriate values so that the signal can be tracked. The frequency limit switches will determine how far the system will slew to track a signal, and the slew rate limit will set the maximum tracking rate.

- Fix the slew rate limit at 19999 Hz/sec for the maximum tracking rate.

7. Set IF Gain and Threshold

- Set the IF gain to 0 dB and the threshold to -40 dB.

- Press the AUTO command, and the system should begin tracking the input signal.

- Increase the IF gain if necessary to raise the filtered signal amplitude to a reasonable level without overdriving the output. If it is necessary to use more than 30 dB IF gain, be wary of spurious responses in the output.

- Now adjust the threshold control so that the device will track only the required portion of the input signal; it will reset and wait for a new signal when the amplitude of the tracked signal falls below the threshold.

After the above steps have been completed, the instrument should be able to track strong signals in the input signal spectrum.

To track weaker signals, however, a certain amount of experimentation is necessary to determine the optimal system parameters. For example, it may be necessary to adjust the frequency limits or slew rate settings to prevent tracking other signals whose frequencies cross that of the desired signal.

## C. Specifications

### 1. Frequency Range and Accuracy

Instrument response is flat from 50 Hz to 30 kHz. The lower frequency bound for tracking is one-half the IF bandwidth or 50 Hz, depending on which is larger. The frequency synthesizer is controlled in 1 Hz steps and is accurate to within 0.5 Hz. Discriminator zero error will limit accuracy to ±10 percent of the IF bandwidth or ±1 Hz when tracking a constant-frequency signal (discriminator error is fairly constant and can be determined by tracking the 5 kHz CAL TONE which is accurate to ±0.03 Hz).

### 2. IF Amplifier Response

The IF amplifier bandwidth can be set to 1 kHz, 300, 100, 30, or 10 Hz. The amplifier is a cascade of third-order Butterworth bandpass filters with successively narrower bandwidths. Filter response is flat within ±0.25 dB for signals within 0.3 BW of the center frequency and is down 3 dB at 0.5 BW, 20 dB at 1.1 BW, and at least 60 dB at 3 BW from the middle of the passband. The IF filter is centered on the tracking frequency $f_o$ with a maximum error of 5 percent of the IF bandwidth + 1 Hz.

### 3. Sensitivity

Input signals from 30 mV to 3 Vrms will result in full-scale input meter deflection. IF gain is variable from 0 to 60 dB in 10 dB steps, thereby producing a full-scale output deflection with signals as small as 30 μV at the input.

4. Spurious Responses

Spurious responses within the IF passband with 0 dB IF gain are less than -80 dB when no signal is applied except in the 10 Hz BW position; these responses are then -60 dB. Spurious components caused by frequency synthesizer spurs mixing with input signal components will be at least 60 dB below the full-scale output with 0 dB IF gain. Increasing the gain raises the responses accordingly.

5. Amplitude Output Rise Time

The amplitude output rise time is normally determined by the IF bandwidth. With additional postdetection filtering, however, the 10 to 90 percent rise time is 11 msec.

6. Log Output Response

In the LOG output mode, the output voltage is proportional to the logarithm of the average signal amplitude. Output accuracy is within ±0.5 dB for signals from -60 to 0 dB with respect to full-scale output; the scale factor is 0.125 V/dB.

7. Discriminator Linearity

Linearity is within 3 percent for signals within the IF passband in the 1 kHz and 300 and 100 Hz bandwidth positions. Error is somewhat greater at 30 and 10 Hz and may be as much as 10 percent at 10 Hz.

8. Slew Rate

Slew rate depends on bandwidth. In the 1 kHz and 300 Hz positions, the maximum slew rate is 20 kHz/sec; at 100, 30, and 10 Hz, it is approximately 3.5 kHz/sec, 350 Hz/sec, and 35 Hz/sec, respectively. It can be further limited by the slew rate limit control.

9. Power Consumption

Nominal power consumption is 30 W from a 115 V 60 Hz line.

## II. CIRCUIT DESCRIPTION

Figure 2.1 is a simplified block diagram of the major elements in the Tracking Filter. The audio-frequency input signal is amplified, clipped, and filtered in the signal input section. It is then mixed with the synthesizer output (at 100 kHz + $f_o$), and signals at the difference frequency (100 kHz) are filtered in the IF amplifier whose output is detected and appears at the amplitude output. The discriminator measures the deviation of the filtered signal from the center of the IF passband and controls the synthesizer frequency to track the input signal as it changes in frequency. The frequency control section limits the synthesizer frequency in accordance with the parameters set on the front-panel switches.

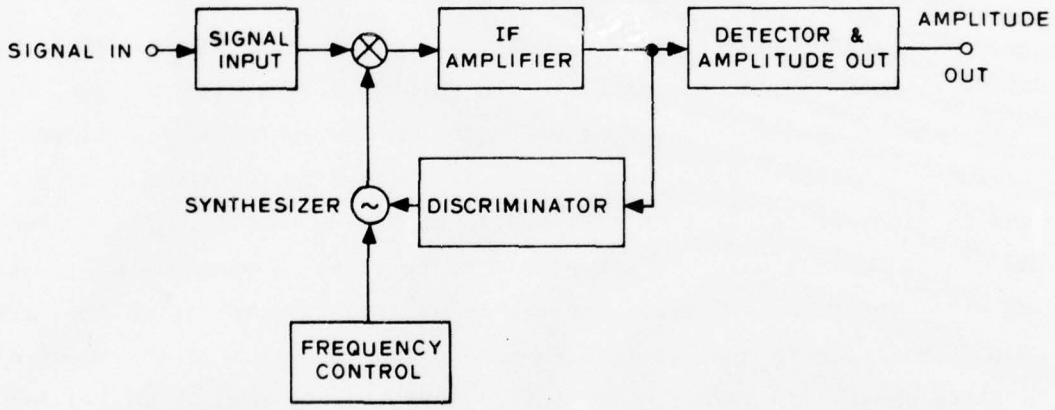



Fig. 2.1. MAJOR ELEMENTS OF THE TRACKING FILTER.

### A. Signal Input

#### 1. Input and VU Meter Amplifier--Card 1

The signal at the input jack is amplified by the differential amplifier U5 (-3.52 dB gain) to generate a single-ended signal for the input select gates U6. These gates choose either the input signal or the 5 kHz calibration tone according to the setting of the input select switch. If the attenuator control switch is in the VARIABLE position,

the selected signal is attenuated by the variable input level potentiometer up to 12 dB. The range select amplifier U11 amplifies the signal from 0 to 40 dB, depending on the setting of the input level switch; this switch controls the input level select gates U7 and U3 that determine the feedback around U11 so as to set the amplifier gain. The signal level at the output of U11 is 2 Vrms full-scale.

The output of U11 is fed to the VU meter amplifier U12. The input level VU meter is a rectifying ac voltmeter that responds to the average level of the input signal, and U12 sets its gain so that a full-scale sine-wave signal will deflect it to 0 VU which is the normal maximum operating level. The 3900 Ω resistors and 0.0015 μF capacitor at the output of U12 provide frequency compensation to produce a flat frequency response to 30 kHz.

2. 5 kHz Calibration Source--Card 13

This card generates a 5 kHz calibration tone of 63.2 mV (equivalent to a 100 mV input signal) to the input select switch on card 1. This tone is used as a calibration signal during system setup and maintenance. An input 40 kHz square wave is divided by U9 and U5 into a 5 kHz square wave and is then filtered to eliminate the third and higher harmonics so that only a 5 kHz sine wave remains. A series-shunt switch U6 kills the 5 kHz cal tone when the input select switch is in the INPUT SIGNAL position to prevent interference. The 50 kΩ pot at the input of a fifth-order 1 dB Chebyshev filter adjusts the cal signal amplitude; this lowpass filter has a 3 dB frequency of 5436 Hz so that the last 0 dB ripple is at 5 kHz. The 5 kHz component is passed without attenuation, but harmonics are attenuated at least 60 dB to leave a pure sine wave. U12 is an output buffer.

3. Clipper--Card 2

The input signal is clipped to eliminate impulsive noise resulting from sferics that might cause ringing in the IF amplifier. A symmetrical clipper, comprised of U5 and U6, limits the maximum positive and negative excursions of the signal to a fixed voltage according to

the adjustment of the CLIP LEVEL pot on the card. The clipping level is set so that a 2 Vrms sine-wave signal is just below clipping. U10 is an output buffer.

A rectifier (U7 and U8) feeds the comparator U11 to form a clip detector. When the input signal is beyond the clipping level, U11 turns on the clip light on the front panel to indicate clipping activity.

4. 30 kHz Lowpass Filter--Card 3

The output of the clipper is now filtered to eliminate any signal components above 30 kHz that may be present in the input signal or may be the result of clipping the lower frequency signals. If the signals are not filtered, components near 100 kHz may appear in the IF amplifier as spurious signals. The filter is a lowpass seventh-order 0.001 dB Chebyshev with an attenuation of 76 dB at 100 kHz.

5. Tracked Spectrum--Card 4

This card produces a signal to drive a real-time spectrum analyzer so as to give the operator a simultaneous picture of the input signal spectrum and the frequency of the Tracking Filter as it follows the input signal. The output of this card is the sum of the clipped and lowpass filtered input signal and a tone at the tracking frequency $f_o$.

A 100 kHz sine-wave tone is mixed with the synthesizer square wave at a frequency of 100 kHz + $f_o$, and the product is lowpass filtered to leave only the difference component at $f_o$. The filter is a fifth-order 0.1 dB Chebyshev with a 3 dB frequency of 35 kHz; its output is amplified to 1 Vrms by U10 and is then attenuated by the $f_o$ LEVEL pot on the front panel. This attenuated $f_o$ tone is added to the 30 kHz lowpass signal (depending on the setting of the tracked spectrum mode switch) by U12, and the sum appears as the tracked spectrum output.

When the mode switch is in the $f_o$ position, $\overline{\text{TCHOP}}$ is high, TSIG is low, and the $f_o$ chop gate sends the $f_o$ tone to the output; the signal gate, however, blocks the lowpass signal. In the $f_o$ & SIGNAL mode, $\overline{\text{TCHOP}}$ and TSIG are both high, and the $f_o$ tone and input signal appear at the output. In the $f_o$ CHOPPED & SIGNAL position, $\overline{\text{TCHOP}}$ is low, and the $f_o$

chop gate is turned on and off at a 10 Hz rate by the output of the 10 Hz divider U4 and the chopped $f_o$ tone is then added to the signal; in this mode, the spectrum analyzer will display the input signal spectrum with the $f_o$ tone superimposed as a dotted line.

The 1 Vrms $f_o$ tone also appears at the $f_o$ out jack on the back panel. Analysis of this tone will determine the spectral purity of the frequency synthesizer output.

### 6. 100 kHz Sine Wave Source--Card 12

This card produces the 100 kHz sine-wave tone that is mixed with the synthesizer output to generate the $f_o$ tone on card 4. An input 100 kHz square-wave signal is filtered by a lowpass fifth-order 1 dB Chebyshev filter to eliminate the third and higher order harmonics so that only a pure 100 kHz sine wave remains. Because the 3 dB frequency of the filter is 108.7 kHz, the 100 kHz signal falls at the last 0 dB ripple of the filter. The third harmonic is attenuated by 62 dB. The 5 kΩ LEVEL ADJUST pot sets the amplitude of the 100 kHz output and thus sets the level of the $f_o$ tone on card 4. U10 is an output amplifier.

## B. Intermediate Frequency (IF) Amplifier

As can be seen in Fig. A.1 in the appendix, the output of the 30 kHz lowpass filter is mixed with the square-wave output of the synthesizer at a frequency of 100 kHz + $f_o$, and the product is applied to the first stage of the IF amplifier. Difference products near 100 kHz are selected by the 100 kHz stage, and these are then mixed with a 70 kHz square wave, down-converted to 30 kHz, and fed to the 30 kHz stage. Depending on the selectivity (bandwidth) required, the signal is successively down-converted and filtered by consecutive stages. Each stage operates at approximately one-third the frequency of the previous stage and has one-third the bandwidth. The output of the last stage is at a frequency of 300 Hz and has a bandwidth of 10 Hz. Image responses are thereby avoided, and the overall filter has a somewhat better frequency characteristic than it would if all the filtering was done at one frequency. The operating frequencies and bandwidths of the various stages are listed in Table 2.1.

Depending on the passband required, the signal is picked off at the output of a certain stage, and the following stages are muted (by turning off their local oscillators) to prevent loading and spurious responses. For example, for an overall bandwidth of 100 Hz, the output signal is taken from the 3 kHz stage, and the 1 kHz and 300 Hz stages are muted.

Table 2.1

IF FILTER STAGES

| Stage | Frequency | Bandwidth |
|---|---|---|
| 1 | 100 kHz | 3 kHz |
| 2 | 30 kHz | 1 kHz |
| 3 | 10 kHz | 300 Hz |
| 4 | 3 kHz | 100 Hz |
| 5 | 1 kHz | 30 Hz |
| 6 | 300 Hz | 10 Hz |

1. IF Selectivity

The frequency response of the IF amplifier is plotted in Fig. 2.2. Each stage is a third-order Butterworth filter with a nominally flat response near the center frequency. Signals more than three bandwidths from the center frequency are attenuated at least 60 dB. Because of drift in the filter components, a small ripple (up to ±0.25 dB) may occur in the IF passband.

2. IF Stage: Theory of Operation--Cards 5-10

The six IF stages are similar and their operation, based on the 10 kHz IF as an example, is described in this section. Figure A.12 is a schematic of the 10 kHz IF filter. Each IF stage has three sets of tuned circuits to generate a third-order Butterworth response that has a flat top in the center of the IF passband. The first stage (L14 and C14 in the 10 kHz filter) is tuned at the center frequency (10,000 Hz) and has a Q of 33 (30 in some stages). The second and third stages are tuned below (9871 Hz) and above (10,131) the center frequency and have Q's of 67 (60 in some filters). The Q of each circuit is set during assembly, but the tuned frequencies are adjustable by a tuning core in each inductor.

The mixer is a set of four analog switches (U9) at the input of the filter. These switches are turned alternately on and off by the

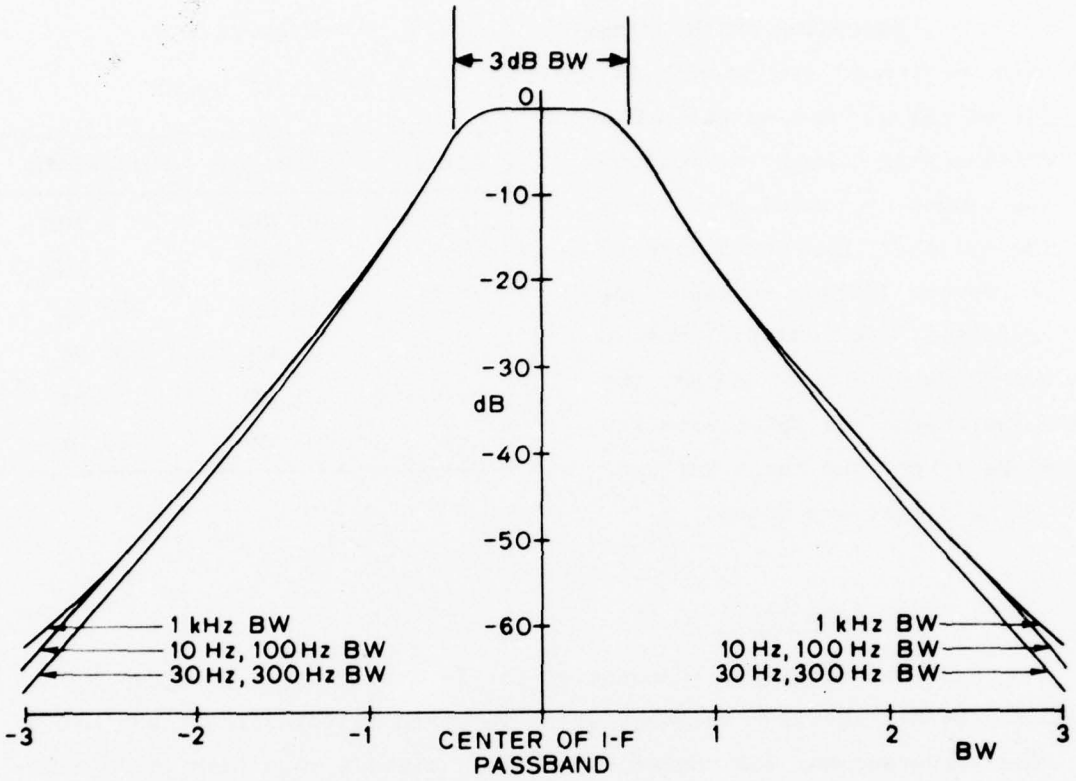



Fig. 2.2. IF AMPLIFIER SELECTIVITY.

input square-wave LO signals. During one-half cycle of the local oscillator, one series switch and the opposite ground switch are on, and signal current flows through the input transformer (L14) in one direction. During the next half cycle, the other two switches are on, and signal current flows through the input transformer in the opposite direction. The result is the full-wave modulation of the input signal by the LO square wave, and this modulation generates two sidebands. The lower band (at the difference of the input frequency, 30 kHz, and the LO frequency, 20 kHz) is passed by the IF filter, but the upper band is attenuated. The input signal is moved down in frequency (from 30 to 10 kHz), therefore, by the frequency of the local oscillator. If the output of the amplifier is selected from a previous filter stage, both LO lines are low and all the mixer switches are held off, thereby disabling this stage of the filter strip.

The input resistor (R14) appears in parallel with the first of the three tuned circuits at the IF frequency and sets the Q of that circuit; a buffer amplifier U10 prevents loading of the circuit. The second and third are parallel-tuned circuits connected in the feedback loops of the amplifiers U11 and U12. This feedback configuration makes the design of high-Q filters with lossy capacitors somewhat simpler than if grounded circuits with voltage followers (as L14 and C14) are used. The Q's of the last two stages are set by R15 and R16, and their gains are set by the series driving resistors R15' + GAIN pot and R16' so that, with a 2 Vrms input signal at any frequency within the IF passband, the voltage at either U11 or U12 is not greater than 2 V. After alignment, the GAIN pot adjusts the overall gain of the filter to 0 dB. Input and output voltages are nominally 2 Vrms full-scale. NPO ceramic capacitors are used in most of the tuned circuits and have a zero temperature coefficient to match that of the pot-core inductors.

### 3. 100 kHz IF Amplifier--Card 5

This is the first stage of the IF amplifier strip and is similar to the general stage described above except that the signal is upconverted to 100 kHz by mixing it with the square-wave output of the synthesizer at a frequency of 100 kHz + $f_o$. The filter selects the mixer product at the difference frequency of 100 kHz + $f_o$ - $f_{sig}$. Note that the signal spectrum is now inverted, and the signals that were above $f_o$ at the input are now below 100 kHz and the signals below $f_o$ are above 100 kHz. This spectrum inversion continues throughout the IF amplifier because the following frequency conversions are noninverting.

The 100 kHz IF filter also has two carrier-balance adjustments. When signals are close to zero frequency, the synthesizer output (100 kHz + $f_o$) will be close to 100 kHz and may fall within the IF passband. If there is any leakage of the synthesizer through the mixer into the filter, it will appear as a spurious input signal. The carrier-balance adjustments balance the mixer to avoid LO feedthrough, thus preventing spurious responses at low tracking frequencies. The R BALance and C BALance controls inject in-phase and quadrature signals into the IF input to balance any LO leakage. If changes are made in the input

circuitry, it may be necessary to vary the value of the 15 pF capacitor to achieve carrier C balance.

4. 30 kHz IF Amplifier--Card 6

This IF stage is also similar to the general stage described above; however, the gain of the third tuned circuit is changed according to the IF gain switch on the front panel. System gain is adjustable in 10 dB steps from 0 to 60 dB, and most of this adjustment is accomplished in the IF select, gain, and detector circuit (card 15) that supplies up to 40 dB of gain. For very weak signals, however, the gain of the amplifier should be increased earlier. At 50 dB, the gain of U12 is raised by 10 dB and, at 60 dB, it is raised by 20 dB through the action of the gain select gates that lower the driving resistance of U12. These very high gains probably will not be used often because synthesizer spurious products are down only 60 dB from full-scale.

5. IF Mixer Local Oscillators--Card 11

This card produces the 70, 20, 7, 2 kHz, and 700 Hz LO signals for down-conversions at the inputs to the 30, 10, 3, 1 kHz, and 300 Hz IF filters, respectively. Card 11 also generates the 100 kHz square-wave signal for card 12.

The 20 and 2 kHz LO signals are derived directly by division of the 1 MHz tone from the time base (card 25). U5 and U9 divide the input 1 MHz by 5 to 200 kHz, and U5 and U1 divide by 5 again to 40 kHz. The symmetrical divider U8 divides this 40 kHz by 2 so that it becomes the two 20 kHz LO signals. U3 also divides the 40 kHz by 10, and U12 divides it by 2 for the 2 kHz local oscillator.

The 70 and 7 kHz and 700 Hz signals are obtained by symmetrical division of a 1.4 MHz tone from a phase-locked loop locked to the 200 kHz tone from U5. U7 and U11 divide this tone from the phase-locked loop VCO (U2 pin 4) by 7 to 200 kHz. This 200 kHz signal is compared to the 200 kHz reference tone from U5 by the phase comparator (U2 pins 3 and 14), and the output is lowpass filtered and used to control the VCO. The VCO generates a phase-stable signal at seven times the 200 kHz reference, or

1.4 MHz. Some 200 kHz jitter occurs in the 1.4 MHz signal, but the resulting spurs are reduced to tolerable levels by the divisions necessary to produce the 70 kHz, 7 kHz, and 700 Hz LO signals. The division is similar to that for the 20 and 2 kHz oscillator signals. The FREQuency OFFSET pot controls the center frequency of the VCO and is adjusted so that the VCO is nominally centered at 1.4 MHz and, as a result, the control voltage at U2 pin 9 is approximately 0 Vdc.

The LO inhibit gates U10 are driven by the bandwidth switch, and they inhibit the outputs of the symmetrical divide-by-2 flip-flops to quench the LO signals to the stages of the IF filter not being used. For example, in the 1 kHz bandwidth position, the output of the IF amplifier is taken from the 30 kHz filter, and only the 70 kHz local oscillator is necessary; the 20, 7, and 2 kHz and 700 Hz LO outputs are held low. In the 10 Hz bandwidth position, the amplifier output is taken from the 300 Hz filter, and all the LO signals are on. These LO signals are inhibited by setting the SET and RESET pins on the associated flip-flops high. Fairchild 34013PC integrated circuits should be used for the output flip-flops because both outputs are low when inhibited. (On most other 4013 chips, the outputs will be high in the inhibited state. This will work, but it will enable all the mixer gates and generate a slight additional loading on the output of the IF stages.)

## C. Detector and Amplitude Output Circuits

The output of the IF amplifier from a selected stage (depending on the bandwidth desired) is now amplified, detected, filtered, possibly converted to logarithmic form, and output. The amplitude signal is also compared to the given threshold.

### 1. IF Select, Gain, and Detector--Card 15

The outputs of the 30, 10, 3, 1 kHz, and 300 Hz IF amplifier stages are presented to the input select gates U9 and U10, and the desired signal is selected by the setting of the IF bandwidth switch. The output of U9 and U10 is amplified from 0 to 40 dB by the gain select amplifier U1. The gain of U1 is determined by the feedback select gates

U6 and U10 according to the setting of the IF gain switch. If gain is set at 50 or 60 dB, U1 has a gain of 40 dB and the remaining 10 or 20 dB gain is provided in the 30 kHz IF amplifier. The output of U1 (2 Vrms full-scale) is fed to the symmetrical detector U2 and U3. To ensure symmetrical rectification of low-level signals, the SYMmetry adjustment corrects for offset voltages in U2 and U3 and enables the detection of signals 70 dB below full-scale. The detector has a gain of 1.10 (to read average calibrated as rms).

The output of the detector goes to a second-order Butterworth lowpass filter U7 whose frequency is selected by U12 and U11 according to the IF bandwidth. The lowpass frequency is three times the bandwidth of the IF stage selected (or 1/10 the IF frequency) to ensure low ripple in the amplitude output. Additional postdetection filtering may be required, and this can be accomplished by removing U11 and U12 and inserting jumper plugs wired as shown in Fig. A.12. This will fix the filter in the 30 Hz lowpass position and set the 10 to 90 percent detector rise time at 11 msec which should provide a smooth enough trace to easily scale the chart records. Some information is lost, however, in all but the 10 Hz bandwidth position. The detector filter output is 2 Vavg full-scale.

The output of the gain select amplifier U1 is also fed to the buffer U4. It appears at the IF out jack on the back panel.

2. Log and Output--Card 16

The filtered detector output from card 15 is amplified by U10 to 5 Vdc full-scale, and any dc offset is corrected by the LIN ZERO adjustment. This amplified signal is fed to the log converter U6 and buffer amplifier U2 and converted to logarithmic form. The log conversion is such that a 5 V input signal produces a 5 V output at U2, and a signal 60 dB below 5 V generates -2.5 V at U2 (the scale factor is 0.125 V/dB). Either the linear signal from U10 or the log signal from U2 is selected by the lin/log select gates U3, depending on the setting of the amplitude mode switch. This signal is buffered by U8 and drives the amplitude meter; it is also switched by the output duty switch U3, buffered by U12, and appears at the amplitude output jack on the front panel. U3 is

controlled by the track and threshold signals in accordance with the duty control setting. In the CONTINUOUS position, it is always on. In the TRACK position, it is on and the amplitude signal appears at the output only when the system is in the TRACK mode; in the RESET mode, the amplitude output is grounded. In the THRESHOLD position, U3 is on only when the amplitude is above the threshold setting; otherwise, the amplitude output is grounded. The TRACK and THRESHOLD duty settings can eliminate the amplitude output when the instrument is not tracking a desired signal, thus cleaning up the output trace on the chart recorder.

The log output of U2 is also sent to the threshold comparator on Card 17.

The LIN ZERO adjustment is set to produce 0 dc output with 0 input signal. The *LO LOG* offset, *HI LOG* offset, and *LOG GAIN* all adjust the operation of the logarithmic converter (see Section III.C.16 for the correct setting of the pots).

3. Threshold--Card 17

The threshold circuit compares the amplitude of the tracked signal to a preset threshold voltage. The output of the threshold circuit controls system operation during automatic tracking and the duty of the amplitude output in the THRESHOLD position.

The logarithmic amplitude signal from card 16 is added to a voltage from the range level shifter U10 that depends on the threshold control setting on the front panel. The output of the summer U5 is at 0 V for a signal at threshold and 1.25 V for a signal 10 dB below threshold. This voltage is compared to a 0 to 1.83 V signal from the variable threshold control in the comparator U7 whose output is high for signals below threshold and low for signals above threshold. This output is inverted by U12 and becomes the internal THRESHOLD signal that controls the threshold lamp on the front panel and is fed to the threshold output jack on the rear panel.

The threshold comparator has 3 dB of dc hysteresis (that is, if the threshold level is set at a given point and the signal amplitude increases to that point and sets THRESHOLD high, the THRESHOLD line will not go low until the signal has fallen 3 dB below the set point). The

comparator also has 3 dB of additional ac hysteresis with a time constant of 6 msec.

### 4. Voltage Range Logic--Card 14

This circuitry controls the scale-factor lights for the amplitude meter in response to the settings of the input-level and IF gain switches. These switch settings are encoded into octal numbers by U9 and U10 and summed by U6. U3, U4, and U2 form a modulo-6 adder whose sum is decoded by U7 into six lines to drive the 1, 3, 10, 30, 100, and 300 lamps. The outputs of U3 and U4 are also arranged to drive the unit lights V, mV, and μV. The operation of the circuit is straightforward, based on the truth table presented in Fig. A.19.

## D. Discriminators

Each filter card in the IF amplifier has an associated discriminator card. When a filter output is selected (according to the bandwidth desired), the discriminator is activated to measure the difference in frequency between the signal in the IF passband and the center frequency of the IF filter. This difference (or error) is used to control the synthesizer and causes it to change frequency or slew so as to follow the input signal.

### 1. Discriminator Circuits--Cards 19-23

Because the five discriminators are similar, this section describes the circuit operation of the 30 kHz discriminator (card 19) whose frequency-voltage characteristics are shown in Fig. 2.3. The input to this card is the limiter U5 which is a very high gain amplifier that converts the input signal from the IF amplifier into a square-wave output. The limiter is ac-coupled for bias stability. U5 is disabled by the 2N3565 transistor connected to pin 8 because its internal current is shunted to the -7.5 V supply when this transistor is on. The discriminator select logic includes the 2N3565 and an inverting transistor driven by the bandwidth select line. Only the limiter for the selected IF

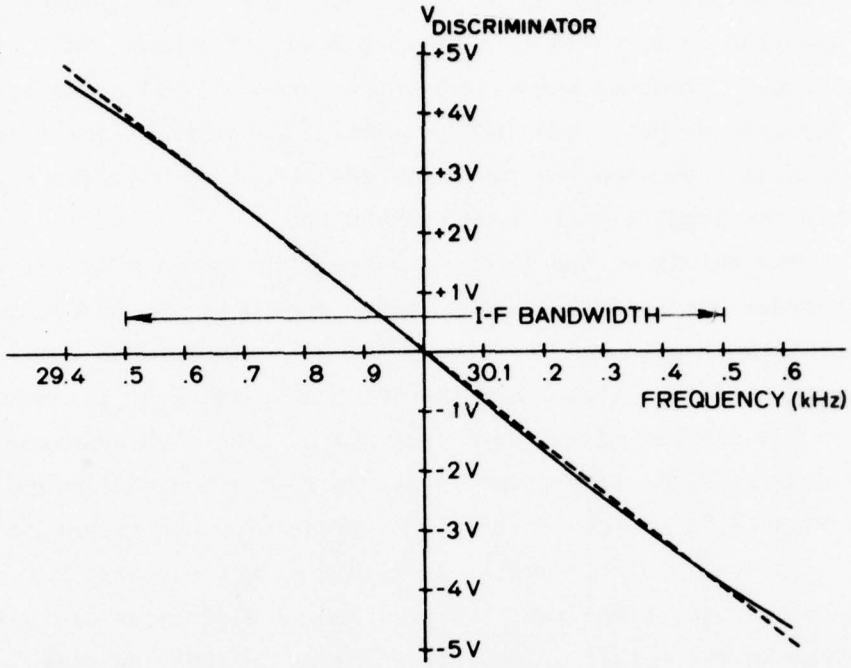



Fig. 2.3. FREQUENCY-VOLTAGE CHARACTERISTICS OF THE 30 kHz DISCRIMINATOR.

amplifier is enabled, and the other four will be disabled to prevent interference.

The output of the limiter drives the balanced-slope discriminator formed by the tuned circuits L12-C12 and L13-C13. L12-C12 is tuned 1 kHz (one IF bandwidth) above the IF center frequency to 31 kHz, and L13-C13 is tuned 1 kHz below to 29 kHz. The Q's of the tanks are set by R12 and R13 to produce a bandwidth of $2\sqrt{2/3}$ BW or 1630 Hz for each circuit. This value provides maximum linearity in the frequency-voltage function of the discriminator.

Because each tank circuit is driven by a constant voltage from the limiter, the voltages in the tanks at TP12 and TP13 depend only on the frequency of the IF amplifier signal and not on its amplitude; the voltage at TP12 is higher for signals above 30 kHz, and that at TP13 is higher for signals below 30 kHz. The peak voltages are picked off by the two 1N4148 diodes, and the difference is summed through the 100 kΩ resistors at the center of the ZERO potentiometer. If the IF signal is above

30 kHz, the output voltage is below 0 V and vice versa. Because the signal spectrum is inverted (see Section B.3), this means that an input signal above $f_o$ produces a positive output and a signal below $f_o$ generates a negative output. The ZERO adjustment compensates for slight differences in loss between the two tanks and is set so that the output is 0 Vdc when the input signal is exactly 30 kHz.

The output of the balanced-slope discriminator is filtered by a fourth-order Butterworth lowpass filter formed by U8 and U12 to eliminate the 30 kHz ripple and leave only the dc component in the output. The bandwidth of the filter is 6 kHz which is sufficient to reduce the ripple to 0.5 percent of the dc output swing. The GAIN adjustment controls the gain of the filter and is set so that frequency swings of 1/2 BW or ± 500 Hz from the center frequency produce output swings of ± 4 Vdc.

Discriminator linearity is within a few percent for outputs from -4 to 4 V except for the 1 kHz and 300 Hz discriminators which are a bit worse as the result of capacitor losses in the tank circuits. (Because of the required capacitance, it was necessary to use Mylar capacitors instead of NPO ceramics.) Error in the 300 Hz discriminator may be as great as 10 percent full-scale or 1 Hz.

### 2. Discriminator Select and Slew--Card 24

The output of the selected discriminator is an analog voltage proportional to the tracking error and is processed to control the synthesizer. It is converted into a pulse train to slew the synthesizer and cause it to track the input signal.

The output of the active discriminator is selected by gates U9 and U10 and buffered by U5. The output of U5 drives the tracking error meter on the front panel, is buffered by U1, and appears at the discriminator output jack on the rear panel; it also drives the up-down comparator U2 whose output is inverted by U12 and becomes the DISC UP/$\overline{DN}$ signal that controls the direction of the frequency synthesizer slew. U2 has 50 mV of hysteresis which prevents the ripple in the discriminator signal from changing the comparator output when the dc component is close to 0 V.

The discriminator signal at U5 is also rectified by U6 and U8 to generate a voltage proportional to the absolute value of the frequency

error. This voltage controls the VCO U11 whose output is a pulse train proportional to the absolute frequency error. This pulse train is buffered by U12 and becomes the DISC PULSE signal which, with the DISC UP/$\overline{\text{DN}}$ signal, will slew the synthesizer frequency. Each pulse of the DISC PULSE will cause a 1 Hz change in frequency.

The constant of proportionality between frequency error and output pulse rate is different for each discriminator. VCO frequency is selected by gates U7 and U10. The SLEW RATE adjustments selected by U7 adjust the pulse rate for each discriminator individually (except that the pulse rates for the 30 and 10 kHz discriminators are the same). The DITHER adjustment sets the minimum value of the VCO control voltage and adjusts for VCO control offset so that the VCO pulses slowly with zero discriminator input.

### 3. Slew Rate Theory

The maximum slew rate of the Tracking Filter depends on the IF bandwidth selected. If the Filter slews too slowly, it may not be able to track a signal that changes quickly in frequency; if it slews too fast, it may overshoot and lose the signal.

Figure 2.4 is a simplified diagram of the elements involved in slew rate calculations. An exact analysis of frequency transient behavior could begin with a Laplace transform of the poles and zeros of the

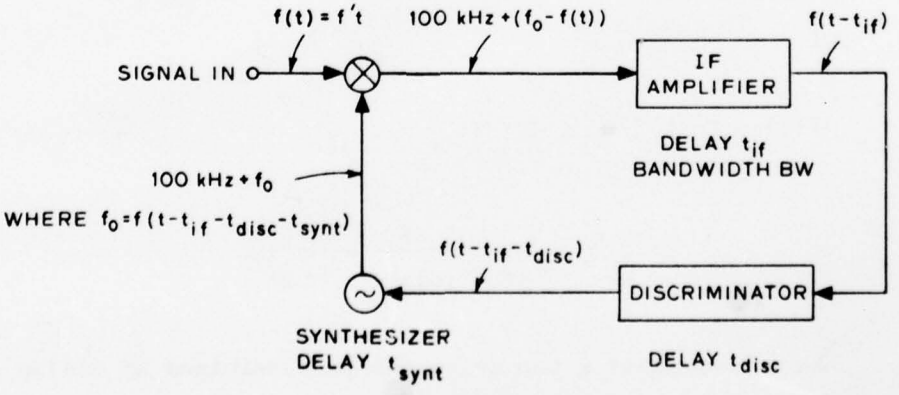



Fig. 2.4. ELEMENTS OF TRACKING FILTER FOR SLEW-RATE CALCULATION.

system, but this would be a very complicated procedure. The following simpler, although somewhat approximate, analysis based on group delays will suffice.

Assume that, at time $t = 0$, the input signal frequency $f(t)$ begins changing at a constant rate $f'$ so that

$$f(t) = f't$$

This signal is mixed with the synthesizer output at 100 kHz + $f_o(t)$, where $f_o(t)$ is the tracking frequency as a function of time. The product at the difference frequency 100 kHz + $f_o(t) - f(t)$ is filtered by the IF amplifier. If the signal is to pass the amplifier, the tracking error must be such that

$$|f_o(t) - f(t)| \leqq \frac{BW}{2}$$

otherwise, the tracked signal would fall outside the IF passband and be lost.

If the group delay of the amplifier is $t_{if}$, the signal at its output represents the input signal at a time $t_{if}$ before the present when it had a frequency of $f(t - t_{if})$. Similarly, if the group delay of the discriminator is $t_{disc}$, its output is the response to the signal at $t_{if} + t_{disc}$ before the present when it had a frequency of $f(t - t_{if} - t_{disc})$. If the synthesizer response time is $t_{synt}$, the tracking frequency $f_o$ is following the signal when it was at $f(t - t_{if} - t_{disc} - t_{synt})$. To remain in track, therefore,

$$|f(t) - f_o(t)| = |f'| \cdot (t_{if} + t_{disc} + t_{synt}) \leqq \frac{BW}{2}$$

or

$$|f'| \leqq \frac{BW}{2(t_{if} + t_{disc} + t_{synt})}$$

The IF amplifier group delay can be determined by adding the group delays of the individual stages. The delay of a Butterworth bandpass filter is a function of the signal frequency within the passband,

but a worst-case estimate for a third-order filter is $t_{if} = 0.87/BW$. For example, the total group delay of the filter at the output of the 10 kHz stage is the sum of the delays of the 10 kHz stage, the 30 kHz stage before it, and the 100 kHz stage before that.

Discriminator delay depends on the response time of the tuned circuits in the balanced-slope circuit and on the delay time of the low-pass filter at the output. The response time of the tuned circuits is approximated by their time constant $t = 2Q/\omega_o$ which is a conservative estimate. For a signal near zero frequency, the group delay of the fourth-order Butterworth filter is $t = 0.86/BW$, where BW is the low-pass bandwidth and is 1/5 of the IF frequency in this design. The output-filter delay is slightly less than the tuned-circuit delay.

The response time of the synthesizer is set by the response time of the slew circuitry which responds to a slew request only when the frequency limit control counter is in state S5. The maximum request latency is 25 μsec, and this yields an average time of 12.5 μsec. A 7.5 μsec delay also occurs before a change in the frequency register actually appears in the output, and an average delay then totals ≈20 μsec which is relatively insignificant compared to the delays of the IF amplifier and discriminator.

The delay times and theoretical maximum slew rates are listed in Table 2.2. The maximum slew rate is limited to 20 kHz/sec in the slew rate limit section--this affects tracking only at 1 kHz or 300 Hz

Table 2.2

GROUP DELAY AND MAXIMUM SLEW RATE

| IF BW | $t_{if}$ (msec) | $t_{disc}$ (msec) | $t_{total}$ (msec) | f' (maximum) |
|---|---|---|---|---|
| 1 kHz | 1.16 | 0.33 | 1.51 | 332 kHz/sec |
| 300 Hz | 4.1 | 1.1 | 5.2 | 29 kHz/sec |
| 100 Hz | 12.8 | 3.3 | 16.1 | 3.1 kHz/sec |
| 30 Hz | 42 | 11 | 53 | 280 Hz/sec |
| 10 Hz | 129 | 33 | 162 | 31 Hz/sec |

bandwidths. Slew rate can be improved by allowing some overshoot in the transient response of the instrument. The discriminator slew adjusts on card 24 are set to produce an overshoot of approximately 10 percent of the bandwidth in response to a large step change in frequency. This slightly raises the slew rates by 10 to 20 percent.

## E. Frequency Synthesizer

The frequency synthesizer serves as a local oscillator in the Tracking Filter. It has an output frequency range of 100 to 130 kHz when tracking signals. At a frequency of 100 kHz + $f_o$, its square-wave output is mixed with the input signal at a frequency near $f_o$ to convert the signal frequency into the passband of the IF amplifier. The synthesizer is controlled by the output of the discriminator in 1 Hz steps and slews in accordance with frequency changes in the input signal it is tracking.

The following specifications are critical in the design of the synthesizer.

- It must be controlled in 1 Hz increments and have a frequency accuracy of at least 1 Hz.
- It should be able to respond quickly to any frequency changes in the input signal so as to provide the maximum tracking rate.
- Its output must be spectrally pure so that spurious components will not appear as signals in the IF amplifier; in particular, it must have phase continuity when changing frequency.

Control precision and stability on the order of 1 Hz dictated a digitally controlled synthesizer design instead of an analog controlled VCO (as used in Leavitt's machine) which would be very difficult to build with a resolution of 1 part in 100,000. The need for fast response required a direct-synthesis approach instead of indirect synthesis with, for example, phase-locked loop dividers. The design that evolved is novel in that it uses only standard 4000-series CMOS devices and generates a square-wave output with spurious components held 60 dB below the fundamental, which is adequate for the Tracking Filter.

1. Theory of Operation

A simple approach to synthesizing a square wave would be to add a number (depending on the frequency desired) periodically to a register and then watch its overflow output. Each overflow would create a phase transition in the output wave, as shown in Fig. 2.5.

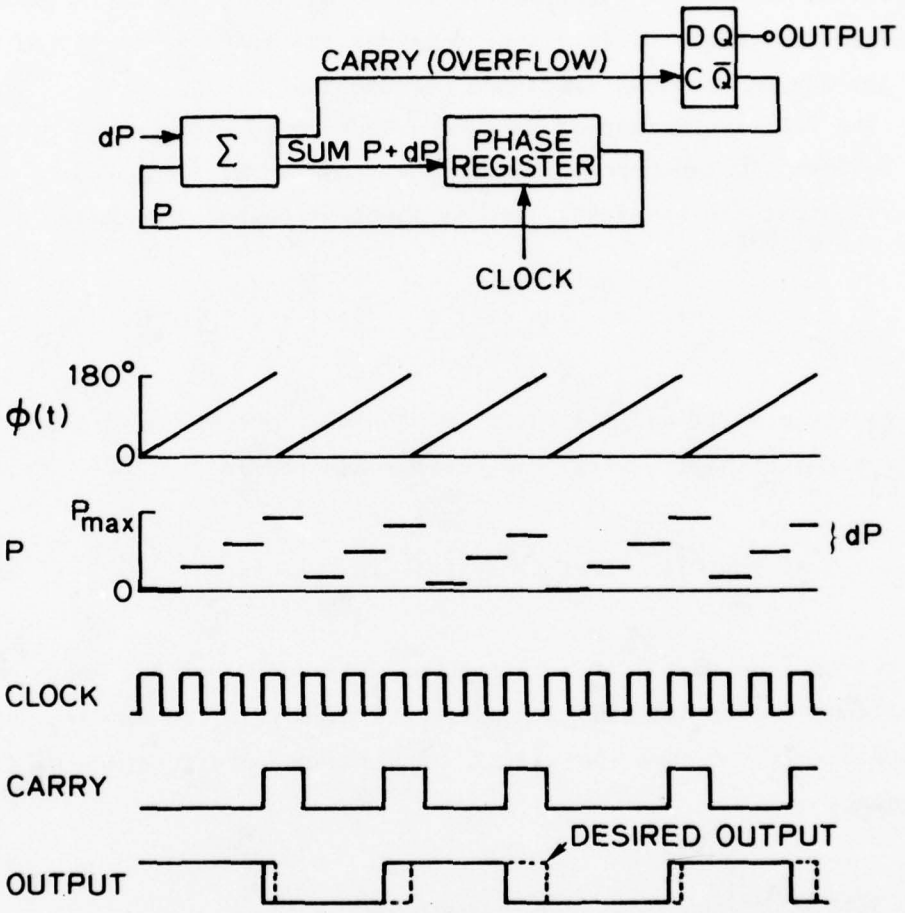



Fig. 2.5. SQUARE-WAVE SYNTHESIZER.

The rate of output transitions is directly proportional to the magnitude of the input number dP which (for an appropriate register capacity $P_{max}$ and clock rate) may be in units of frequency. The register becomes a phase register because the phase $\emptyset(t)$ of the desired output wave is being approximated. The only problem is the discrete nature of the phase addition. If phase could be continuously added, the register

would overflow just as $\phi(t)$ reached 180° and changed sign. By adding phase in finite increments, the register will overflow at some time after $\phi(t)$ has changed sign--possibly almost one clock cycle late. (Note that, in Fig. 2.5, actually the carry from the adder is used to sense the register overflow which occurs one cycle later.) Instead of a square-wave output with transitions at regular intervals, therefore, a wave has been generated whose transition times have a jitter of up to 1/2 clock period about the desired value. This jitter degrades the spectral purity of the wave and introduces spurious frequency components.

The relative amount of these spurious components can be calculated as follows. Only components near the fundamental frequency of the square-wave output are examined. The synthesizer output is written as

$$x(t) = A \cos \left[2\pi f_o t + j(t)\right]$$

where $j(t)$ is a small bounded function of time representing jitter. If it is sufficiently small, $x(t)$ can be approximated as

$$x(t) = A\left[\cos (2\pi f_o t) - j(t) \sin (2\pi f_o t)\right]$$

where it can be seen that jitter introduces spurious sidebands about $f_o$ whose amplitude and frequencies depend on the magnitude and spectrum of $j(t)$, respectively. Assume that $j(t)$ is a square-wave function of time with frequency $f_j$ as

$$j(t) = \frac{4}{\pi} a\left[\cos (2\pi f_j t) - \frac{1}{3} \cos (3 \cdot 2\pi f_j t) + \frac{1}{5} \ldots\right]$$

Generally, $j(t)$ will not have this form but will be a complex series of stepped ramps whose frequency components depend on the clock rate and greatest common divisor of the input number $dP$ and register capacity $P_{max}$. It may be a square wave, however, and this will result in a worst-case analysis. Note that $a$ is the peak value of $j(t)$.

Because spurious responses at all frequencies should be reduced to some maximum level, the principal concern in this analysis is the

largest spurious component. If it can be reduced, the others will appear below the level desired. As a result, only the fundamental component of $j(t)$ need be included, and $x(t)$ can be expressed as

$$x(t) = A\left\{\cos\ (2\pi f_o t) - \frac{2}{\pi} a \sin\left[2\pi(f_o + f_j)\ t\right] - \frac{2}{\pi} a \sin\left[2\pi(f_o - f_j)\ t\right]\right\}$$

The spurious sidebands are smaller than the fundamental component at $f_o$ by a factor of $2a/\pi$.

A design goal is to synthesize a 130 kHz square wave and require that the spurious sidebands be at least 60 dB below the fundamental component so that $2a/\pi = 10^{-3}$. The peak-to-peak jitter in the square-wave synthesizer output $t_j$ must be

$$t_j = \frac{2a}{2\pi f_o} \leq \frac{2\pi}{2 \cdot 2\pi f_o} \times 10^{-3} = 3.85 \text{ nsec}$$

In the simple synthesizer described above, the peak-to-peak jitter is equal to the clock period. To obtain a 130 kHz wave with -60 dB spurs, the phase register must be clocked at 260 MHz which is beyond the capability of CMOS logic.

Fortunately, there is another way to reduce jitter without increasing the clock rate. In Fig. 2.6, the adder carry is assumed to go high at time $kT$, and the output square wave should make a transition

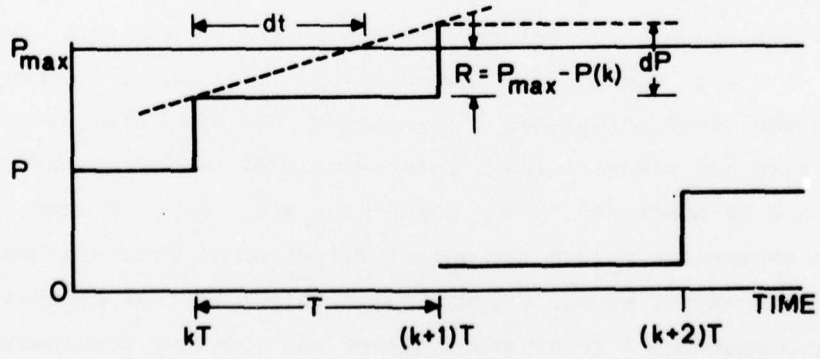



Fig. 2.6. PHASE TRANSITION TIME FROM RESIDUE.

during the next clock period [somewhere from $kT$ to $(k+1)T$]. If the contents of the phase register at $kT$ is known, the time $dt$ after the $k^{th}$ clock pulse when the transition should occur could be calculated as

$$dt = \frac{P_{max} - P(kT)}{dP} T$$

where $P_{max}$ is the capacity of the phase register, $P(kT)$ is the contents at $kT$ before the register overflowed, and $dP$ is the phase increment (proportional to $f_o$) added into the register at every clock pulse. This calculation can be made after the phase register overflows if its previous contents have been saved, and the output phase transition can be generated at a time $dt$ from the $k+1^{st}$ clock pulse or after some future clock pulse. Because the clock pulses occur at a constant rate, the output wave will be delayed in phase by some fixed number of clock pulses from the approximation stored in the phase register, but this constant phase delay is of no concern; only the output frequency is important. Time $dt$ can be calculated by analog means, as illustrated in Fig. 2.7. The residue register is strobed by the adder overflow and thus contains the residue $R = P_{max} - P(kT)$ which is the amount of phase remaining to be added at the previous clock pulse that would cause the phase register to overflow. This is converted by the R digital/analog converter to a voltage proportional to R, and capacitor C is charged to this voltage. At the next clock pulse (k+1), the charge circuit is disconnected and C is discharged by a current source driven by the dP D/A at a rate proportional to the phase increment dP. The value of C, the constants for the D/A converters, and the current source are chosen so that, if $R = dP$, then C would require exactly T sec to discharge to 0 V. After the clock pulse k+1, C discharges, and its voltage drops at a constant rate and passes through zero exactly dt sec after (k+1)T. The voltage on C is monitored by the comparator and, when it goes through zero, the comparator pulses the output flip-flop to create a phase reversal in the output wave. A square-wave output is thus generated at a frequency proportional to dP whose jitter and spurious components depend on the accuracy of the D/A converters and the following analog circuitry.

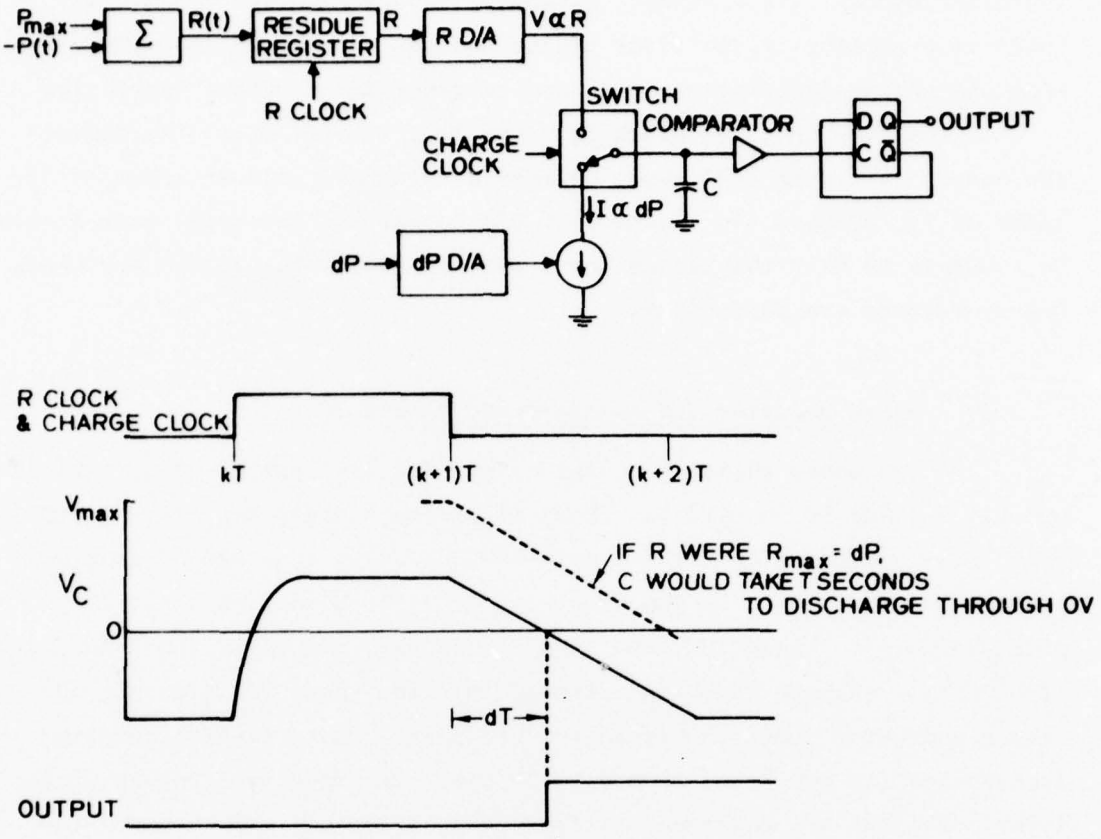



Fig. 2.7. ANALOG CALCULATION OF TIME dt.

The clock rate is relatively unimportant although it should be high to relax the accuracy requirements of the analog circuits. In this analysis, a square wave is to be generated at a frequency of 100 to 130 kHz. The clock must run at least at twice the maximum output frequency (or 260 kHz). A clock rate of 600 kHz was selected for this synthesizer. The maximum capacity of the phase register $P_{max}$ is 300,000. The clock rate and $P_{max}$ were chosen so that dP is in units of Hz; therefore, dP is actually the desired frequency F. For a 100 kHz output wave, dP = F = 100,000, and the phase register overflows every three clock cycles (or every 5 μsec), which generates an output phase transition that is divided by 2 to create the output 100 kHz square wave. At higher frequencies, the phase register will overflow sooner. This synthesizer can produce outputs up to 150 kHz, at which point the phase register overflows every

two clock cycles. As a result, at any frequency from 100 to 150 kHz, there is a minimum of two clock cycles between overflows in which to make the analog computation of dt and to generate an output transition.

At 600 kHz, the clock interval is T = 1.667 μsec. To reduce the output jitter to 3.85 nsec, dt must be computed with an accuracy of 1/433 of T. Because two independent D/A converters are used, each should be accurate to half this value (or 1 part in 866). The 12-bit BCD coded D/A converters are sufficient.

2. Phase Register and Adder--Cards 33 and 34

The phase register contains type-D flip-flops U1-U8 on card 33 and U1, U5, and U6 on card 34. Each flip-flop stores one bit of BCD coded phase information. The modulo-300,000 adder consists of five BCD adders (U9-U12 on card 33 and U9 on card 34) for summation up to 100,000 plus the modulo-3 adder U7, U10, and U11 on card 34. Phase and frequency (frequency = dP) are added and strobed into the phase register on the rising edge of P CLOCK to become the new phase. Bits F1-F19, denoting frequencies (in BCD form) from 0 to 50 kHz, come from the frequency register. Bit F21 = 1 represents a frequency of 100 kHz and is added implicitly in the modulo-3 adder. The carry output of the modulo-3 adder C22 is used to sense phase-register overflow.

3. Residue Register--Card 35

The residue register is composed of type-D flip-flops U2-U4 and U6-U8. Only 12 high-order bits are required to compute the phase residue. When the phase register overflows (C22 goes high), the phase contents are subtracted from 299,999 and the result is strobed by R CLOCK into the residue register. The subtraction is implemented by the three BCD 9's-complement chips U10-U12. (Note that P21 can be used directly for R21.) The contents of the residue register represent the 12 high-order bits of a BCD number from 0 to F-1 (0 to 99,999 or 0 to 149,999 for a 100 or 150 kHz output, respectively).

4. Register Clocking--Card 34

The 600 kHz phase register clock pulse P CLOCK is generated by dividing the 1.2 MHz tone from the time base by 2 in U8 (see Fig. A.3). P CLOCK is buffered by three inverters of U12 to obtain the clock lines that strobe the phase register flip-flops.

The residue register clock pulse R CLOCK, which occurs every two or three P CLOCKs, is generated synchronously with a P CLOCK pulse when the carry from the phase register adder C22 is high which indicates that the phase register is about to overflow. Note that the residue from the previous contents of the phase register is clocked into the residue register at the same time the phase register is clocked with its new contents. The register flip-flops receive the data present at their D inputs on the rising edge of the clock pulses, but their outputs do not change immediately. The old contents of the phase register are still available, while new contents are being strobed in from the adder.

The residue clock pulse R CLOCK also initiates the analog computation of dt. R CLOCK is successively delayed in 1.667 μsec increments by U4 and 0.833 μsec by U3. At 3.33 μsec after the start of R CLOCK, the frequency change inhibit line FCI goes low for 1.667 μsec. This signal is used by the frequency control section to alter the frequency register if desired. Frequency changes are inhibited by FCI when the timing capacitor C may be discharging so as to prevent transients in the F D/A converter during discharge. At this time, the CHARGE line also goes high for 2.50 μsec and charges C to a voltage proportional to R at the output of the R D/A converter. The R D/A thus has 5.83 μsec to settle down after the new contents of the residue register are clocked until the charge circuit is disconnected. At the end of the CHARGE pulse, C discharges and an output transition is generated.

5. Digital to Analog Converters--Cards 36 and 37

The D/A converters convert the BCD-coded phase residue and digital frequency signals into analog voltages to drive the timing capacitor charge and discharge circuits. The R D/A (card 37) and F D/A (card 36) are identical and can be interchanged for testing. The

converters accept 12 bits of BCD-coded data representing the 12 high-order bits of numbers from 0 to 150,000, and the data are thus converted in increments of 200. The output voltage range is from 0 to -4.5 V.

The converters use current-mode switching for high speed. An input reference voltage $V_{ref}$ of approximately 6 Vdc from card 38 is divided by the current-ladder resistors. U2 and U3 are voltage buffers for division between decades, where the voltage between nodes decreases by 0.8 instead of 0.5. Currents from the current ladder are switched by the current-mode switches U9-U11 either to ground or to the summing-point (virtual ground) terminal of U4 in accordance with the input data bits. The resistors in the high-order parts of the divider are all 10 kΩ 1 percent resistors from a single manufacturing batch and are matched to approximately 0.1 percent to provide the required accuracy. The 12 and 47 Ω resistors compensate for the resistance of the current-mode switches.

The input bits for the R D/A come directly from the phase residue register, and the input bits up to D40k for the F D/A come from the frequency register. In the F D/A, D80k is low and D100k is high which indicates the implicit 100 kHz frequency minimum.

6. Synthesizer Output Stage--Card 38

This circuit receives the outputs of the R D/A and F D/A converters and the CHARGE line from the register clock and computes the output transition time dt. When CHARGE is high, the output of the R D/A is buffered by U12 and charges the 0.001 μF timing capacitor C through the charge switch U11. U12 and its circuit have been designed for minimum settling time. The 1.5 kΩ pullup resistor compensates for the discharge current from C through the current source. The 220 kΩ offset resistor supplies a small amount of dc offset in the output of U12 so that, even with zero residue, C still receives enough charge to raise its voltage above the comparator threshold. This introduces a small time delay (slightly dependent on frequency) in the output. The 47 Ω output resistor preserves the stability of U12 when driving a capacitive load. Feedback switching at U11 pin 4 holds the output of U12 at the correct voltage when the charge switch is open.

When CHARGE drops low, the charging circuit is disconnected and C is discharged by the current sink formed by U4, U2, and the 2N5459 field-effect transistor at a rate proportional to the output of the F D/A converter. The $V_F$ output of the F D/A is buffered and level shifted by U4 and compared in U2 to the voltage drop across the 1.54 kΩ resistor and GAIN pot caused by the discharge current from C flowing through the 2N5459. The output of U2 controls the 2N5459 so that $I_{discharge} \times$ (1.54k + GAIN pot) = $-V_F$. Note that the operation of this circuit (with the ZERO pot centered) is not dependent on the exact voltage of the -7.5 V bus. The drain connection of the 2N5459 is used as the current sink terminal. The drain presents a relatively high impedance to C and helps to ensure a discharge current independent of the voltage on C. The 1N4148 discharge limit diode clamps the voltage on C at -0.7 V during discharge to limit the load on the charging circuit during the next cycle.

The voltage on C is sensed by the comparator U6. When C falls through 0 V during discharge, the output of U6 goes high and clocks the output flip-flop U5 and generates an output square-wave transition. U5 is buffered by U10 to produce the synthesizer outputs $F_{lo}$ and $\overline{F}_{lo}$; $F_{lo}$ is also available at the rear-panel $F_{lo}$ jack for system calibration.

The ZERO and GAIN adjustments control the offset and scale factor of the discharge current source. They are set during calibration to minimize the output jitter over the full frequency range.

The D/A reference voltage $V_{ref}$ is obtained on this card from the 7.5 V supply bus. System operation is not greatly dependent on the exact voltage of this bus if both converters track or change together in response to variations in $V_{ref}$.

## F. Frequency Control

This section of the Tracking Filter controls the frequency of the synthesizer in response to information from the discriminator and threshold circuits. With the front-panel controls, the operator can set the parameters that direct the frequency tracking behavior of the system. The Tracking Filter is always in one of two modes of operation--the TRACK or RESET mode. In the TRACK mode, pulses from the discriminator

slew oscillator are combined with the DISC UP/$\overline{DN}$ line to increase or decrease the frequency of the synthesizer in 1 Hz increments. Provision is made to limit the maximum slew rate, maximum and minimum frequencies of the synthesizer, maximum time the system will remain in the TRACK mode, and delay time after receipt of a THRESHOLD signal before the system begins tracking. In the RESET mode, tracking is inhibited and the synthesizer is reset to the initial $f_o$ or acquisition frequency. This initial frequency can be changed by the operator.

Normally, the system operates in the automatic tracking condition, where the TRACK or RESET mode depends on whether the filtered input signal is above or below the given threshold. The operator can manually place the system in these modes through the tracking mode command pushbuttons.

1. Frequency Register--Cards 28-32

The frequency register is a set of five presettable decade up/down counters and is split into five cards, each containing one decade of frequency $f_o$ and some frequency control circuitry. The value of the frequency register plus 100,000 is used as the phase increment dP which is added into the synthesizer phase register to generate the output square wave. Because each decade card is identical except for the wiring of the frequency bound lines, they can be interchanged for testing.

The frequency counter U11 on each card is a BCD up/down counter that counts up or down at each positive transition of the F CLOCK line, depending on whether the UP/$\overline{DN}$ line is high or low. The five counters are connected between cards by their carry lines so that they function as one large five-decade counter. The counter can also be preset asynchronously with the clock input to the value appearing at its jam inputs if the JAM F line is high. The output of each decade counter is coded by the seven-segment driver U8 to drive the frequency display on the front panel. The remaining circuitry on the card generates the jam data for the frequency register and is also used to compare the frequency register value to various frequency limits and bounds.

Latch U3 contains the value of the initial or acquisition frequency. The output of the frequency register is strobed into this latch

by the STROBE FI line when the system is in the RESET mode and the initial frequency is being set. The jam select BND/$\overline{\text{FI}}$ gate selects either initial frequency or frequency bound data for the jam inputs of the frequency register. The initial frequency is jammed by setting SELECT BND/$\overline{\text{LIM}}$,$\overline{\text{FI}}$ low and raising JAM F during the RESET mode to reset the frequency register. When SELECT BND/$\overline{\text{LIM}}$,$\overline{\text{FI}}$ is high and JAM F is raised, the data at the bound lines are jammed into the frequency register when a bound error is detected.

The operation of the frequency synthesizer has implicit frequency bounds. It will not operate with $f_o$ above 30 kHz or below 1/2 IF BW or 50 Hz, whichever is greater (below 500 Hz with 1 kHz BW, 150 Hz with 300 Hz BW, or 50 Hz in the other bandwidth positions). These implicit bounds prevent $f_o$ from occurring above the maximum frequency of the input signal or (essentially) below zero frequency. The bound bits are generated by the frequency limit control circuit and are different for each decade of the frequency register; they are in addition to the frequency limits that may be set by the operator. Frequency bounds may be disabled during instrument alignment.

The remaining circuitry on these cards is used to compare the frequency register contents to the implicit bounds and operator-set frequency limits. The sequence of these comparisons is controlled by the frequency limit control (described below) and are made in the magnitude comparator chips U10. The U10 chips compare the value of the four bits of frequency register output to four bits of frequency test data from the bound/limit select chip U6. The output of the magnitude comparator is a high signal on one of the three lines F>FTEST, F=FTEST, and F<FTEST, depending on whether the register contents are greater than, equal to, or less than the test data. These lines are connected from card to card, and the outputs of U10 on the last card (32) are used by the frequency limit control. The test-frequency data from U6 represent either frequency-bound or frequency-limit data from U1, depending on whether the SELECT BND/$\overline{\text{LIM}}$,$\overline{\text{FI}}$ line is high or low.

The frequency limit data originate in the BCD adder U1 and are compared either in absolute or relative form, depending on the absolute-relative limit switch. In absolute comparisons, the frequency register

contents are compared directly to the settings of the high- and low-frequency limit switches on the front panel, and these switches then control the upper and lower limits of the tracking operation. In relative comparisons, the upper limit setting is added to the contents of the initial $f_o$ register, or the lower limit setting is subtracted from the contents to form the test frequency; the limit switches then become increase- or decrease-frequency-change limits. Higher or lower limits are selected by the limit select hi/lo gate U5 according to the HILIM/$\overline{\text{LOLIM}}$ line. Selection of absolute or relative limits depends on the ABS/$\overline{\text{REL}}$ line. When ABS/$\overline{\text{REL}}$ is high, the high or low limit is fed directly through the BCD adder U1 to the bound/limit select gate, and the initial-frequency inputs to U1 are disabled by U2. When ABS/$\overline{\text{REL}}$ is low and a relative comparison is to be made, the value of the high limit or the negated value of the low limit is added to the initial frequency in U1. The low limit is negated by the 9's-complementer U9. The BCD adder carries are connected from card to card by LIMCIN and LIMCO.

2. Frequency Limit Control--Card 26

This card controls the frequency bound and limit comparisons made in the comparator circuitry on cards 28-32 above. The comparisons are made in a fixed sequence determined by the state counter U1,U2 which is a five-state counter driven through U11 by the CHARGE pulse from the synthesizer clock. At the fall of each CHARGE pulse, the counter advances to the next of its five states S1-S5. Feedback from gate U3 limits the counter to five states (see Table 2.3 for decoding).

Table 2.3

FREQUENCY LIMIT
STATE COUNTER DECODING

| State | SQ1 | SQ2 | SQ3 |
|---|---|---|---|
| S1 | 0 | 1 | 1 |
| S2 | 0 | 0 | 1 |
| S3 | 0 | 0 | 0 |
| S4 | 1 | 0 | 0 |
| S5 | 1 | 1 | 0 |

Note that the state counter advances with the falling edge of each CHARGE clock pulse, which occurs twice during each synthesizer output cycle (or at a rate of $\geq$200 kHz); total cycle time, therefore, is $\leq$25 µsec.

Frequency comparison parameters are selected at the beginning of each state. The output of the frequency comparators is strobed into the bound and frequency limit flip-flops by the falling edge of FCI, which occurs either 2.9 or 4.6 μsec later, to provide ample time for the comparison to settle down. The comparisons made in each state are as follows.

State S1. Frequency $f_o$ is compared to the lower frequency bound whose bits are encoded by U9 and U11 to represent 50, 150, or 500 Hz, depending on the IF bandwidth. SELECT BND/$\overline{\text{LIM}}$,$\overline{\text{FI}}$ (from SQ3) is high to enable bound comparisons. When FCI falls, the F>FTEST line from the comparator is clocked into the LOBND OK flip-flop U7 to indicate whether $f_o$ is above the lower bound. (If BOUND DISABLE from the internal normal-align switch is high, the LOBND OK is held set to disable the bound circuitry during instrument alignment.) If F<FTEST is high, the BOUND ERROR line from U3 goes high for the remainder of the state to indicate that $f_o$ is below the lower bound.

State S2. Frequency $f_o$ is compared to the upper frequency bound of 30 kHz. $\overline{\text{SQ2}}$ becomes the appropriate bound bits. SELECT BND/$\overline{\text{LIM}}$,$\overline{\text{FI}}$ is high to enable bound comparisons. When FCI falls, the F<FTEST line is clocked into the HIBND OK flip-flop U7 to indicate whether $f_o$ is below 30 kHz. (Again, if BOUND DISABLE is high, the HIBND OK is held set.) If F>FTEST is high, the BOUND ERROR line goes high for the remainder of the state to indicate that $f_o$ is above 30 kHz.

State S3. Frequency $f_o$ is compared to the lower frequency limit set by the front-panel frequency limit switches. SELECT BND/$\overline{\text{LIM}}$,$\overline{\text{FI}}$ is low to enable limit comparison, and SELECT HILIM/$\overline{\text{LOLIM}}$ (from SQ1) is low to select the lower limit. Whether the comparison is to an absolute frequency limit or relative to the initial $f_o$ depends on the ABS/$\overline{\text{REL}}$ line (described above). At the falling edge of FCI, the F>FTEST line is clocked into the LOLIM OK flip-flop U8 to indicate whether $f_o$ is above the limit; at the same time, F<FTEST is clocked into the LOLIM ERROR flip-flop U4 to indicate a lower limit error if $f_o$ is less than the lower limit. When the limit mode switch is OFF, F LIMIT DISABLE is high and sets the OK flip-flop and resets the ERROR flip-flop to disable the comparison.

Step S4. Frequency $f_o$ is compared to the higher frequency limit set by the front-panel switches. Again, SELECT BND/$\overline{\text{LIM}}$,$\overline{\text{FI}}$ is low, but SELECT HILIM/$\overline{\text{LOLIM}}$ is high to select the upper limit. Absolute or relative limit comparison depends on ABS/$\overline{\text{REL}}$. At the falling edge of FCI, the F<FTEST line

is clocked into the HILIM OK flip-flop U8 to indicate whether $f_o$ is below the higher limit; at the same time, F>FTEST is clocked into the HILIM ERROR flip-flop U4 to indicate a higher limit error if $f_o$ is greater than the higher limit. If the limit-mode switch is OFF, the OK and ERROR flip-flops are held set and reset, respectively.

State S5. No frequency comparisons are made. The frequency register may be changed during this state, depending on the track control and slew control circuits. The S5 and S5·$\overline{\text{FCI}}$ signals are decoded by U6 and U10 so that they can be used by these circuits.

The OK and ERROR flip-flop clocks are decoded by U5 and U6. U6, U10, and U11 control the limit error light that flashes at a 5 Hz rate if either the limit error flip-flop is set or if BOUND DISABLE is high (indicating that the internal bound disable switch is in the ALIGN position). The outputs of the bound and limit OK flip-flops are summed by U10 to generate the LO OK and HI OK lines which are high if $f_o$ has not reached the respective bounds or limits (as long as slewing in that direction is still possible). These signals also control the LO LIMIT and HI LIMIT lights.

3. Track Control--Card 27

The track control circuit determines whether the Tracking Filter is in the TRACK or RESET mode. It also controls the setting of the initial $f_o$ register and the resetting of the frequency register.

The operator tracking commands TRACK, AUTO, and RESET are decoded and latched by the command latches U9 and U10. If the RESET command is received, the MODE flip-flop is set to the RESET state and remains there until a new command is given. If the TRACK command is received, the MODE flip-flop is reset to the TRACK state. With an AUTO command, the flip-flop changes between TRACK and RESET automatically according to the tracking behavior of the system. The command and mode signals are used by U6 and U2 to drive the front-panel command and mode lights.

The MODE flip-flop is clocked in state S5 when FCI falls with the contents of the RESET REQuest flip-flop U7. The tracking mode changes automatically only in S5. The RESET REQuest flip-flop is set at the

beginning of S5 according to the output of U12 which depends on the LO OK and HI OK lines, setting of the limit mode switch, and DURATION OK and DELAY OK lines from the track duration and delay circuits.

The RESET REQuest flip-flop is set to request the RESET mode as follows. If LO OK or HI OK is low ($f_o$ is at a frequency or bound limit) and RESET ON LIMIT is high (the limit mode switch is in the AUTO position), a reset request is made. If the DURATION OK or DELAY OK line is low, the RESET mode is requested because the maximum duration in the TRACK mode has been exceeded, the correct delay time from a signal above the threshold state has not occurred, or the tracked signal is below threshold.

If a reset request is made but the MODE flip-flop is not in the RESET mode, the AUTO RESET PULSE flip-flop U3 (plus the MODE flip-flop) is set by U6 to issue an AUTO RESET PULSE to the track delay circuit. This flip-flop will be reset at the next cycle of the state counter, and the reset pulse thus lasts up to 25 μsec. If the manual track command is being used, the AUTO RESET PULSE is inhibited.

The STROBE FI and JAM F lines are controlled by U8 and U11 to set the initial $f_o$ register or to reset the frequency register. In states S1 or S2 when a bound error has been detected, JAM F is high if the BOUND ERROR line goes high and the BOUND DISABLE line is low. At this time, the bound bits are selected by the jam select switches on the frequency register cards, and the register is set to the appropriate frequency bound. This will not occur during normal signal tracking; however, it may happen when the Tracking Filter is first turned on, if $f_o$ is very low and the bandwidth switch changes to a wider bandwidth (and higher low bound), or if the internal bound disable switch is moved from ALIGN to NORMAL. The STROBE FI line is also driven high when a bound error is detected, and the bound bits are jammed into the frequency register.

The JAM F line will go high at the end of S5 when FCI is low, the system is in the RESET mode, and a manual slew is not in progress. At this time, the contents of the initial-frequency register are placed on the jam lines and the register is reset to the initial frequency. Frequency $f_o$ is thus reset when entering the RESET mode. If the system is in RESET mode and a manual slew is in progress, the STROBE FI line

(instead of the JAM F line) will go high during S5·$\overline{FCI}$, and the initial-frequency register is changed. Note that this happens during manual slewing only in the RESET mode; slewing during the TRACK mode will not change the initial frequency.

Manual slew, generated by pushing either the UP or DOWN buttons on the front panel, is detected by U6 and entered into the MAN SLEW REQuest flip-flop at the beginning of S5. The MAN SLEW REQuest line is also used by the slew control clock on card 41.

Part of U10 also controls the LIMIT CARRY IN line to the limit frequency low-bit adder on card 28. This line is high while the frequency limit switch is in the RELATIVE position during S3 when $f_o$ is being compared to the lower limit. This adds one bit into the low-order position of the limit adder to facilitate the subtraction of the lower limit from the initial frequency. (Complementing the lower limit and adding 1 is equivalent to negating it which is necessary for subtraction.)

4. Track Duration Limit--Card 39

This card generates the DURATION OK signal to the track control card. A clock counts the time since the start of the TRACK mode and holds DURATION OK high until the clock reading equals the setting of the duration limit switches. At this time, the clock stops and DURATION OK goes low to request a RESET mode.

The 1 kHz signal from the time base is divided by 10 in U5, and the output 100 Hz clock signal drives the four decades of clock dividers U5, U6, and U3--counting time in 10 msec increments up to 99.99 sec. The contents of the clock dividers are compared to the setting of the duration limit switches by the magnitude comparators U9, U10, U11, and U7 whose output is entered into the DURation OK flip-flop by the 1 kHz signal. When the DUR OK flip-flop falls, the LIMIT LED latch and the LIMIT light on the front panel are turned on. The MIN LED ON counter is also enabled and counts 10 Hz pulses to hold the LIMIT light on for a minimum of 0.8 sec even if the system resets and enters a new track period.

When TRACK falls, indicating that the system is in RESET mode, the clock dividers are reset to zero and the DURATION OK line is made

high again, and the system then waits for a new track period. If the duration limit switch is set to OFF, the duration limit circuitry is disabled and DURATION OK remains high at all times.

5. Track Delay Control--Card 40

This circuit controls the delay time in automatic tracking from when the filtered signal rises above threshold to when the TRACK mode is entered and tracking begins. A clock counts the time from the rising edge of the THRESHOLD signal and, when the time set on the front-panel delay time switches has elapsed, the DELAY OK line goes high to enable tracking.

The 1 kHz signal from the time base is divided by 10 in U5, and the output 100 Hz clock signal drives the clock dividers U5,U6--counting time in 10 msec increments up to 9.99 sec. The contents of the clock dividers are compared to the setting of the delay time switches by the magnitude comparators U9, U10, and U11 whose output is entered into the DELAY OK flip-flop by the 1 kHz signal. When the indicated time has elapsed, DELAY OK goes high and the clock is disabled. While the clock is counting, the WAIT light is on to signify that a delay is in progress.

If the signal falls below threshold or a reset pulse (approximately 25 μsec long) occurs, the clock and DELAY OK flip-flop are reset and wait for another delay interval. If the delay time switch is set to OFF, the track delay circuit is disabled, and DELAY OK follows the input THRESHOLD signal without any delay time.

6. Slew Rate Multiplier--Card 43

This card generates a pulse train at a rate depending on the setting of the slew rate limit switches. It is used by the slew rate limit circuit to limit the maximum rate of frequency change when tracking a signal.

The multiplier output is a pulse train whose rate (0 to 19,999 Hz) is equal to the setting of the slew rate switches. The 500 kHz signal from the time base is buffered by U9 and used to clock the multiplier

sections. U5 divides the clock pulse by 2, and U9 encodes the high-order digit of the slew rate (either 1 or 0) which will generate a 250 kHz pulse train if the 10 kHz switch is set to 1. Rate multiplier chips (U2, U6, U3, U7) increase the number of pulses in the output, depending on the four lower decade switch settings. The output of U7 is a pulse train at 25 times the desired rate (0 to 499,975 Hz) and is divided by 25 by the dividers U8 and U12 to generate the slew rate multiplier output. There is substantial jitter in the output of U7; however, this is reduced by a factor of 25 in U8 and U12, and jitter in the output pulse train is only a few percent.

7. Slew Rate Limit--Card 42

This card receives the pulse train from the discriminator and the output of the slew rate multiplier and generates slew requests to change the frequency of the synthesizer when tracking a signal. These slew requests are generated in response to the discriminator signal but are limited in frequency to less than or equal to the pulse rate from the multiplier. As a result, the Tracking Filter will only change at a rate less than or equal to the maximum slew rate setting.

Input pulses from the multiplier and discriminator set the RM OK and DISC OK flip-flops U12 and U8. When both are set, U7 sends a 500 kHz clock pulse from U9 to the DISC UP REQ or DISC DN REQ flip-flops U11 and one or the other is set, depending on the DISC UP/$\overline{\text{DN}}$ line. The output slew request is passed to the slew control circuit, and the returning SLEW ACKNOWLEDGE signal starts the acknowledge reset counter U2,U3 to reset the slew rate limit circuit.

The setting of U11 depends also on the slew direction switch on the front panel. In the UP/DOWN position, a slew request in either direction will be generated in accordance with the state of the DISC UP/$\overline{\text{DN}}$ input. In the UP ONLY or DOWN ONLY position, only a slew-up or slew-down request can be generated, and requests to slew in the other direction are ignored. The UP OK and DN OK signals that form data for U11 are coded by U9.

After a slew has been requested, the circuitry must wait up to one state counter cycle (25 μsec) for an acknowledgment from the slew

control. While waiting, the RM OK and DISC OK flip-flops are reset by the SLEW REQUEST PENDING output of U7, and the RM PEND and DISC PEND flip-flops are enabled. If a rate multiplier or discriminator pulse arrives during this time, it is entered into the pending flip-flops and strobed into the OK flip-flops by U4 during the acknowledge reset cycle so that no incoming pulses will be overlooked. If the DISC UP/$\overline{\text{DN}}$ line changes during a request, the SLEW REQUEST PENDING line goes low as a result of the action of the change-release gates U4 and enables another slew request in the opposite direction. This prevents the slew rate limit circuit from hanging up if a request in one direction is not acknowledged because a frequency limit in that direction, for example, has been reached.

The UP LIMIT or DN LIMIT flip-flops U6 and associated front-panel lights are activated by U5 on the receipt of a discriminator pulse if the RM OK flip-flop is not set (indicating discriminator pulses are at a higher rate than the slew rate multiplier pulses) or if a slew is requested in a direction disabled by the slew direction switch. The associated error light remains on until another discriminator pulse arrives (at which time it may remain on if the limiting condition persists) or until it is reset by a slew acknowledgment.

When the SLEW ACKNOWLEDGE line goes high, U2 is clocked and starts the slew acknowledge reset counter that counts the 500 kHz clock line from the time base through the buffer U9. At the first 500 kHz pulse, ACK is set. This resets the request and limit flip-flops, strobes the pending data into the OK flip-flops, and resets U2. At the next 500 kHz pulse, ACK is cleared and ACK+1 is set, and this clears the pending flip-flops. At the third pulse, the ACK+1 flip-flop is cleared and the reset cycle is completed. If the RESET line from the track control goes high (indicating RESET mode operation), ACK and ACK+1 are held high to reset the slew rate limit circuit.

### 8. Slew Control--Card 41

This card controls the F CLOCK and UP/$\overline{\text{DN}}$ count and direction lines to the frequency register counters. These lines cause the register to count up or down in 1 Hz steps in response to the discriminator and manual slew requests.

When a discriminator slew-up or slew-down request (in addition to HI OK or LOW OK and TRACK) is present, the appropriate SLEW UP REQ or SLEW DN REQ flip-flop U8 is set at the beginning of control state S5 by the output of gates U7 and U11. For either request, the F CLOCK line is driven high by U12 and U10 as soon as the frequency change inhibit line FCI falls and causes the frequency register to count up or down 1 Hz. The direction of counting is controlled by the UP/$\overline{\text{DN}}$ output of the SLEW UP REQuest flip-flop which is high for a slew-up request and low for a slew-down request.

The slew request flip-flops may also be set by the MAN SLEW UP REQ and MAN SLEW DN REQ flip-flops U3 in response to a manual slew command from the UP and DOWN switches. These switches set the data line to the appropriate flip-flop and start (via MANUAL SLEW REQ) the manual slew clock (counters U9 and U5 and gates U10, U6, and U2). The counter begins at 00 and counts 10 Hz pulses from the time base. During the first second (from 00 to 09), the 10 Hz signal is multiplexed onto the manual slew clock line and generates slew requests at a 10 Hz rate which causes the synthesizer to change at 10 Hz/sec. During the next second, the 100 Hz signal is multiplexed onto the manual slew-clock line and, during the third second, the 1 kHz signal is used. After 3 sec of continuous slewing, the counter reaches 30 and holds, and the 5 kHz signal from the time base becomes the slew clock and causes the synthesizer to change at 5 kHz/sec. If the SLEW pushbutton is released, the slew counter is reset to 00.

If slew-up and slew-down requests are made simultaneously (as may occur if the discriminator is attempting to slew the system in one direction while a manual slew is being requested in the other) or if both UP and DOWN manual slew buttons are depressed at the same time, the coincidence inhibit gate U12 prevents the generation of an F CLOCK pulse. A SLEW ACKNOWLEDGE pulse, however, is created. Note that, if both slew buttons are depressed simultaneously, there will be no slewing action, but the manual slew counter is not reset. It is possible, therefore, to slew manually at high rates either up or down and in one direction after the other by holding down both buttons and then releasing one or the other momentarily.

9. $F_{DC}$ Counter and DAC--Card 44

This card generates a dc signal output proportional to the tracking frequency $f_o$ relative to the initial frequency. The F CLOCK and UP/$\overline{DN}$ lines that drive the frequency register counters control the four up/down counters U5, U1, U2, and U3. When TRACK is low (during the RESET mode), the counters are reset to 4995 by jamming; when TRACK is high, they count up or down as the frequency synthesizer changes. The $f_{DC}$ range switch determines the scale factor of the $f_{DC}$ output. In the ± 5 kHz position, the $\overline{carry}$ out from U5 is used as the $\overline{carry}$ in of U1, and U1 counts once for every 10 counts in U5 (or in units of 10 Hz). In the ± 500 Hz position, the $\overline{carry}$ in of U1 is held low, and U1 counts once for each F CLOCK pulse (or in units of 1 Hz).

The outputs of U1, U2, and U3 are buffered by U6 and U7 and drive the BCD-coded resistor ladder connected to the D/A converter amplifier U12. The resistor ladder is offset so that a count of 499 in U3-U2-U1 generates a 0 V output, and counts of 999 and 000 produce 5.00 and -4.99 V outputs, respectively. The output, therefore, represents frequency relative to the initial $f_o$ with a range of ± 5 kHz or ± 500 Hz at scale factors of 1 kHz/V or 100 Hz/V quantized in 10 mV steps. The ZERO and GAIN adjustments set the D/A converter offset and span.

If the frequency change exceeds the range of the counter, it will overflow or underflow, and the output signal will jump from 5.00 to -4.99 V, or vice versa. As a result, the output actually represents the relative frequency modulo 10 or 1 kHz.

10. Time Base--Card 25

This card contains a crystal oscillator operating at 1.000 MHz and generates outputs at 1.2 and 1.0 MHz, 500, 5, and 1 kHz, and 100, 10, and 5 Hz to produce timing signals for the rest of the system. All signals except the 1.2 MHz are derived from the 1.0 MHz crystal oscillator output by successive division in the dividers U10, U6, U11, and U12.

The 1.2 MHz signal originates in a phase-locked-loop oscillator whose frequency is locked to the crystal oscillator. The divide-by-5 circuit U6,U7 supplies a 200 kHz reference signal for the phase-locked

loop; this is compared to a 200 kHz signal generated by dividing the 1.2 MHz VCO output by 6 in the divider U3-U7. The phase difference between the two signals is compared in the phase comparator U4 pins 14 and 3, and the filtered output controls the VCO in U4 to hold its output phase-stable and at exactly 1.2 MHz. The FREQ OFFSET adjustment keeps the VCO operating in the center of its range and is set so that the control voltage at U4 pin 9 is approximately 0 V.

G. Power Supply and Regulator--Card 46

The Tracking Filter derives all of its power from the positive and negative 7.5 Vdc busses. The ac power line is stepped down, rectified, and regulated by the ± 7.5 V regulators. The +7.5 V regulators use a 723C voltage-regulator chip to drive the 2N3053 and RCA31 series pass transistors to generate the +7.5 V output. The 2N3565 current-limit transistor senses the current flowing into the +7.5 V bus and limits the output current to ≈1 A. The voltage on the +7.5 V bus is sensed through the +7.5 ADJust pot and is applied to control the 723C.

In the -7.5 V regulator, the +7.5 V output is a reference. The sum of the +7.5 and -7.5 V outputs is compared to ground in the 2N4250 differential pair, and the error voltage controls the 2N3053 and RCA31. The 2N3565 limits the output current to approximately -1 A.

The ac ON light is driven by the regulated output bus. The two 1N4001 diodes limit the bus transients during turn-on and turn-off to protect the integrated circuits from being back-biased.

The +7.5 ADJust pot is set so that the positive bus is at 7.45 to 7.50 V. The voltage of the negative supply should then be equal in magnitude to the positive supply within 20 mV.

## III. SERVICE INFORMATION

The following information is included to aid a technician in servicing the Tracking Filter. No periodic maintenance is required, but components occasionally drift out of spec or an integrated circuit may break down and must be replaced. If the cause of the problem is not known, the performance check below will help to isolate the trouble to a particular area in the instrument. The notes on trouble-shooting in Section B describe the general procedures to follow when working on the Filter, and Section C explains in detail the necessary steps for recalibration.

### A. Performance Check

The following performance check can be made to isolate a problem to a particular portion of the Filter. Except where noted, no instruments are required. The performance check can be made step-by-step, or steps can be skipped if certain sections are known to be working correctly.

#### 1. Manual Track Commands, Mode Selection, Manual Slew

- Turn on the Filter.
- Press the RESET, AUTO, and TRACK command buttons, and the associated command and mode lights should come on.
- Place the instrument in the RESET mode by pressing RESET.
- Press the UP and DOWN pushbuttons, and the frequency display should slew up and down at an increasing rate as the buttons are held down.

  The manual slew pushbuttons should cause the frequency to change at 10 Hz/sec during the first second, at 100 Hz/sec during the next second, at 1 kHz/sec during the third, and at 5 kHz/sec thereafter until the upper bound of 30 kHz or the lower bound of 1/2 BW or 50 Hz is reached.

2. Frequency Limits

- Set the instrument in the RESET mode and the IF bandwidth to 10 Hz.
- Switch the frequency limit control to OFF.
- Hold the DOWN manual slew button, and the frequency display should decrease and stop at the lower frequency bound of 50 Hz; when this bound is reached, the LOW limit light should come on.
- Turn the bandwidth to 30 Hz and then to 100 Hz; the frequency display should stay at 50 Hz, and the LOW light should remain on.
- Switch the bandwidth to 300 Hz, and the frequency display should jump to 150 Hz.
- Switch the bandwidth to 1 kHz, and the frequency display should jump to 500 Hz.
- Press the UP button and hold it; the frequency display should stop at 30,000 Hz, and the HI limit light should come on.

  The above steps test the implicit frequency bounds.

- Slew the instrument to a frequency of 10,000 Hz.

  It will be necessary to press the UP and DOWN buttons in short bursts to hit the exact frequency when you come close to it.

- Switch the frequency limit mode to ABSOLUTE.
- Set the upper limit to 10,050 Hz and the lower limit to 9950 Hz.
- Switch the frequency limit control to HOLD ON LIMIT.
- Increase the frequency.

  At 10,050 Hz, the HI limit light should come on. At 10,051 Hz, the ERROR light should start flashing.

- Lower the frequency.

  At 9950 Hz, the LOW limit light should come on. At 9949 Hz, the ERROR light should start flashing.

- Set the slew rate limit to 00000 Hz/sec to disable tracking.
- Set $f_o$ to 10,000 Hz.

- Place the Filter in the TRACK mode with the TRACK command.

  The initial frequency is now 10,000 Hz and will not change with slewing.

- Set the frequency mode switch to the RELATIVE TO INITIAL position and the increase limit and decrease limit switches to 50 Hz.

- Raise and lower $f_o$.

  The HI and LOW limit lights should come on at 10,050 and 9950 Hz, and the ERROR light should start flashing at 10,051 and 9949 Hz as before.

3. Slew Rate Limit

- Set the input select switch to CAL TONE to select the internal 5 kHz calibration tone.

- Turn the input level switch to 0.1 V and the attenuator to FIXED.

- Move the bandwidth to 1 kHz and the IF gain to 0 dB.

- Turn the threshold switch to -40 dB.

- Set the slew rate direction to UP/DOWN and the maximum slew rate to 00001 Hz/sec.

- Switch the frequency limit control to OFF.

- Place the Filter in the RESET mode and slew $f_o$ to 4500 Hz.

  The THRESHOLD light should be on.

- Place the instrument in the TRACK mode with the TRACK command, and $f_o$ should begin slewing upward at a rate of 1 Hz/sec.

- Set the slew-rate limit to 10 Hz/sec, and slewing should continue at a rate of 10 Hz/sec.

- Press RESET, and $f_o$ should reset to 4500 Hz.

- Press TRACK, and slewing should start over again.

- Set the slew rate direction switch to DOWN ONLY, and slewing should stop.

  The UP light should be on during these steps to indicate that the slew rate circuit is limiting the slew rate of the Filter.

- Press RESET and set the initial frequency to 5500 Hz.
- Press TRACK, and $f_o$ should begin slewing down at 10 Hz/sec.
- Set the slew direction switch to UP ONLY, and slewing should stop.

  The DOWN light should be on during these steps.

  Be sure that the maximum track duration and track delay control switches are off.
- Set the frequency limit mode to the RELATIVE TO INITIAL $f_o$ position and the decrease limit to 300 Hz.
- Set the frequency limit control to RESET ON LIMIT (AUTO).
- Set the slew rate limit to 100 Hz/sec and the slew direction to UP/DOWN.
- Press the AUTO track command button.

  Frequency $f_o$ should drop at a rate of 100 Hz/sec from 5500 Hz to 5200 Hz and then reset to 5500 Hz to begin again. The RESET mode light and LOW limit light may flash briefly.

4. Track Duration and Delay

- Tracking down from 5500 Hz at 100 Hz/sec on the cal tone, set the maximum track duration time to 2.50 sec and the duration control switch to ON.
- Set the track delay time to 2.00 sec and the delay control switch to ON.

  The system should start at 5500 Hz and slew down at a rate of 100 Hz/sec for 2.50 sec to reach a frequency of 5250 Hz. At this time, the duration limit light should come on for approximately 0.8 sec; the mode light should change from TRACK to RESET, and the WAIT light should turn on while the Filter waits to begin tracking. After a delay of 2.00 sec, the TRACK light will come on, the WAIT light will turn off, and tracking will begin again.

## 5. Input Circuits

- Set the input select switch to CAL TONE.
- Turn the input level switch to 0.1 V and the attenuator to FIXED.

  The input level meter should read 0 VU, indicating full-scale input.

- Turn the input level switch to 0.3, 1, and 3 V.

  The input level meter should drop to -10, -20, and -30 VU. (The -20 and -30 VU readings are at the bottom of the meter scale and are only approximate.)

- Turn the input level switch back to 0.1 V and the attenuator to VARIABLE.

  With the attenuator in the CAL position, the meter should again read 0 VU.

- Turn the attenuator down, and the input level meter should drop to less than -12 VU.
- Set the input level switch to 0.03 V.
- Turn the attenuator clockwise; the CLIP light should come on just above 0 VU.

## 6. IF Amplifier

- Place the Filter in the RESET mode and slew $f_o$ to 5000 Hz.
- Adjust the input section for a full-scale reading (0 VU) on the calibration tone.
- Switch the bandwidth to 1 kHz and the IF gain to 0 dB.
- Turn the amplitude output mode to LINEAR, and the amplitude meter should read full-scale.
- Change the bandwidth to 300, 100, 30, and 10 Hz, and the amplitude meter should read the same at all bandwidths.

  Note that the IF amplifier is a cascade of filters, and a low reading at one bandwidth as a result of reduced IF filter gain will produce low readings at lower bandwidths.

- Set the bandwidth to 1 kHz and move the frequency up and down with the manual slew buttons.

  The amplitude output should be down 3 dB (to 70.7) at 4500 and 5500 Hz and should have a very flat response from 4700 to 5300 Hz.

  Make similar checks at each of the other bandwidths.

  The 3 dB down points should be 1/2 BW from 5000 Hz, with a flat response in the center of the passband.

7. Amplitude Output Circuits

- Set the initial frequency to 5000 Hz and the IF bandwidth to 1 kHz, and the amplitude meter should read full-scale.
- Change the input level to 0.3, 1, and 3 V, and the amplitude output meter should drop to 0.32, 0.10, and 0.03 of full-scale.
- Turn the output mode to LOG, and the amplitude-output meter should indicate readings of 0, -10, -20, and -30 dB for input-level settings of 0.1, 0.3, 1, and 3 V, respectively.
- Increase IF gain to 10, 20, and 30 dB when the input level is set at 3 V; the amplitude output should increase in 10 dB steps to full-scale.
- Reduce the gain to 0 dB when the output is in the LOG mode.
- Set the input level to 0.1 V and turn the attenuator completely down; the amplitude output should now be -12 or -13 dB.
- Turn the threshold range switch to 0 dB and move the variable threshold control to the center of its range.
- Increase the input signal, using the attenuator control; the THRESHOLD light should come on at an output amplitude reading of -7 or -8 dB.
- Lower the input signal, and the THRESHOLD light should go off exactly 3 dB below the point where it came on.

  The threshold circuit has 3 dB of dc hysteresis.

8. Discriminators

- Place the Filter in the RESET mode and slew the frequency to 5000 Hz.

- Monitor the tracking error meter at different bandwidth settings, using the cal tone; the meter should read close to 0 error in each bandwidth.

  Before the discriminator is activated, there is a turn-on delay of up to 3 sec after the bandwidth is selected.

- Set the bandwidth to 1 kHz.

- Increase the frequency to 5500 Hz; the tracking error meter should read -500 Hz which indicates that the calibration tone is 500 Hz below the tracking frequency.

- Lower the frequency to 4500 Hz, and the meter should read +500 Hz.

  Make similar checks at each of the other bandwidths.

  The tracking error meter should read close to ±full-scale for $f_o$ below and above the 5 kHz cal frequency by 1/2 BW.

  The error may be slightly larger in the 30 and 10 Hz positions, with a maximum error of 10 percent or 1 Hz at 10 Hz BW.

- Set the slew rate to maximum (19,999 Hz/sec) and the slew direction to UP/DOWN and disable the frequency limit, duration time, and delay time circuits by turning them to OFF.

- Slew the frequency to 5500 when the Filter is in the RESET mode.

- Switch the bandwidth to 1 kHz and press TRACK.

  Frequency should slew rapidly to 5000 Hz and then dither 2 Hz at a rate of a few counts per sec.

- Change the bandwidth and set the initial frequency 1/2 BW above 5000 Hz; with a TRACK command, the Filter should slew 5000 Hz and dither slowly.

  Dithering will become progressively slower as the bandwidth is reduced; it is ±1 Hz in 300 Hz BW or less.

- To test transient frequency response, set the slew direction switch to DOWN ONLY and repeat the above steps, using initial frequencies of 1 BW above 5000 Hz.

  In the 1 kHz bandwidth position, the system will slew to 5000 Hz and stop.

In the other bandwidth positions, the system will overshoot 5000 Hz by 10 percent of the bandwidth and stop 10 percent BW below 5000 Hz (at approximately 4970, 4990, 4997, and 4999 Hz for 300, 100, 30, and 10 Hz bandwidths). This amount of overshoot produces the fastest transient response.

9. Spurious Response Level

- Place the Filter in the RESET mode and slew the frequency to 5000 Hz.
- Set the IF gain to 0 dB and the output mode to LOG.
- Adjust the input circuits for a full-scale reading on the 5 kHz cal tone.
- Measure the spurious response by changing the frequency at least 3 BWs from 5000 Hz and increasing the IF gain to 40 dB.

  Spurs should be less than -20 dB on the amplitude output meter (60 dB below the maximum level) at all frequencies greater than 3 BWs from 5000 Hz.

  In the 10 Hz bandwidth position, the spurious level will probably be close to -20 dB output.

- Turn the 5 kHz cal tone off by selecting the INPUT SIGNAL (with none selected) and set the input level to 3 V.

  Spurious responses should now be -40 dB or less (80 dB below full-scale) at any frequency above 1 kHz and any bandwidth except for the 10 Hz bandwidth where they most likely will be -20 dB (60 dB below full-scale).

  As frequency is lowered to the minimum tracking frequency, the output level will rise which indicates carrier feedthrough in the 100 kHz IF stage. This effective dc frequency component should be -20 dB or less on the output meter (-60 dB or less from full-scale).

B. Trouble-Shooting

The first step in trouble-shooting is to isolate the cause of the problem to one particular section of the instrument, using the above

performance check. Remember that problems in one part of the Filter may create others in later stages. For example, the failure of the mixer in an IF stage will cause the signals fed to successive stages to be faulty, and problems that occur at one bandwidth setting may also appear at smaller bandwidths.

After the trouble has been isolated, refer to the appropriate circuit description in Chapter II to aid in understanding the operation of that section and to the internal adjustment procedures in Section C for corrections.

The Tracking Filter is divided internally into two chassis. The upper one is removable and contains the input circuits, IF amplifiers, output circuits, and discriminators. The lower one contains the power supply, frequency synthesizer, and frequency control circuits. To gain access to the lower chassis, grip the upper chassis and pull upward uniformly on all edges. The interchassis connectors will release, and the upper chassis will slip out. Because the functions of the two units are distinct, they can be trouble-shot separately. It is not necessary, in most cases, for the upper chassis to be in place to discover a problem in the lower one.

All of the digital circuits, and some of the analog circuits, operate with CMOS logic chips. These chips are sensitive to static electricity and care must be taken when changing a suspected chip to discharge the body to the chassis before inserting the chip into its socket. It is best to use B-grade CMOS when replacing a chip because it has a power-supply rating of 18 V. The power bus in the Filter provides voltages of $\pm 7.5$ V, or 15 V total, which is maximum for an A-grade CMOS circuit.

It will be necessary to use a card extender to measure waveforms or voltages on individual cards. The power should be turned off before inserting or removing a card to prevent damage to the integrated circuits. This is especially important when working on the IF amplifier because the IF mixers may latch on and burn out if their cards are inserted into a hot chassis.

All of the digital signals in the instrument are pulled down (or up) by 100 k$\Omega$ resistors on each card so that a previous card can be removed without having the digital inputs undefined (which would cause the

integrated circuits to overheat). If the card that drives a particular digital line is removed, the line can be set high or low by jumping it to either supply (but not to ground), or an external generator can be used for testing. For example, when the analog chassis is removed, it is possible to test the slew circuitry by connecting the external signal sources to the DISC UP/$\overline{\text{DN}}$, DISC PULSE, and THRESHOLD lines as required.

## C. Internal Adjustments

The following adjustments achieve a complete recalibration of the Filter. These steps must be followed in the order given. A high-speed oscilloscope, digital voltmeter, and audio-frequency oscillator and attenuator are necessary for some of the adjustments.

### 1. Power Supply

- Remove the top and bottom covers of the Filter.
- Turn the instrument on and check the voltages on the +7.5 and -7.5 V busses (card pins 2 and 3) with respect to ground; the +7.5 V bus should read from 7.45 to 7.50 V, and the -7.5 V bus should be within 20 mV of the reading for the +7.5 V bus.
- To change the power supply voltage, remove the upper chassis and adjust the +7.5 ADJ pot on card 46 for the correct reading on the +7.5 V output.

> Note: If the power supply has a low voltage and/or blows fuses, the problem is likely to be a defective digital integrated circuit. Pull all the cards and successively reinsert them while monitoring the current from the supplies (via the 0.56 Ω current-limit resistors on card 46) to find the defect.

### 2. Time Base Phase-Locked Loop

- Use a card extender to obtain access to the time base (card 25).
- Adjust the FREQ OFFSET pot (below U4) so that the voltage on U4 pin 9 (the CD4046AE chip) is approximately 0 ± 1 Vdc.

The 1 MHz oscillator frequency can be checked with a frequency counter and the trimmer capacitor can be adjusted for 1.000 MHz, but this step is not necessary.

3. Frequency Synthesizer Jitter

This step sets the zero and gain of the timing circuit in the synthesizer output to minimize synthesizer jitter and spurious frequency components.

- Remove the upper chassis.
- Turn the internal bound disable switch (located above the power supply mounting plate) to the ALIGN position.
- Connect the $f_{lo}$ output at the rear panel to the oscilloscope and turn the Tracking Filter on.
- Place the system in the RESET mode and slew $f_o$ to $\approx$710 Hz.
- Set the oscilloscope to display 20 cycles of the 100,710 Hz output wave and use the delayed oscilloscope sweep to expand the display after 10 cycles.
- Extend the sweep until the jitter on the output wave can be measured.
- Adjust the ZERO pot on card 38 until the least jitter is obtained; it should now be approximately 10 nsec peak-to-peak or less.

  Note that this measurement of jitter will indicate twice the actual peak-to-peak value because the oscilloscope is being triggered off one cycle that may have jitter in one direction, and jitter is being measured from another output cycle that may have jitter in the opposite direction.

- Slew $f_o$ to 49,290 Hz and adjust the GAIN pot on card 38 to minimize jitter.

  These adjustments interact, and it may be necessary to repeat the above steps several times until jitter is minimum at both ends of the frequency range.

- Check the tracking behavior of the output circuit by examining the jitter at several frequencies between 0 and 50,000 Hz $f_o$ (100 to 150 kHz output); it should be less than 10 nsec peak-to-peak throughout this range.

4. IF Mixer Local Oscillators Phase-Locked Loop

- Use a card extender to obtain access to the IF mixer local oscillators (card 11).
- Adjust the phase-locked loop FREQ OFFSET pot (below U2) so that the voltage on U2 pin 9 (the CD4046AE) is 0 ± 1 Vdc.

5. 5 kHz Calibration Source Amplitude

- Set the input select switch to CAL TONE, input level to 0.1 V, and input attenuator control to FIXED. Adjust the CAL AMPLITUDE pot on card 13 so that the 5 kHz cal tone reads exactly 0 VU on the input level meter.
- Check that the cal voltage at the test point on card 13 is 63.2 mV.

6. Clip Level

- Adjust the CLIP LEVEL pot on card 2 so that the cal tone (at 0 VU) is just below clipping (the CLIP light is off). The input and output voltages on card 2 should be 2 Vrms.

7. 100 kHz Sine-Wave Level

- Place the Filter in the RESET mode by the RESET command and slew $f_o$ to 5000 Hz.
- Monitor the voltage at the $f_o$ output on the rear panel.
- Turn the 100 kHz sine-wave LEVEL adjustment on card 12 so that the $f_o$ output is 1 Vrms.

8. 100 kHz IF Amplifier

- Set the input to CAL TONE input, input level to 0.1 V, input attenuator to FIXED, bandwidth to 1 kHz, IF gain to 0 dB, output mode to LINEAR, mode to RESET, and $f_o$ to 5000 Hz.

- Use a card extender to obtain access to the 100 kHz IF stage (card 5).

- Peak L6 for a maximum amplitude output reading.

  If the output meter reads off-scale, slightly lower the input, using the variable attenuator.

- Slew $f_o$ to 3709 Hz and peak L7; then set $f_o$ to 6308 Hz and peak L8.

  It will be necessary to increase the IF gain to 20 dB to achieve a sufficient amplitude meter reading when adjusting L7 and L8.

- Slew $f_o$ to 500 Hz, and alternately adjust the R BAL pot and C BAL trimmer capacitor for a minimum amplitude reading.

- Increase the IF gain as necessary for a sufficient amplitude reading.

  These two adjustments interact, and they must be repeated several times to obtain the best null. It should be possible to null the LO feedthrough in the mixer to less than 60 dB below full-scale output. If the C BAL trimmer is at the end of its range, it may be necessary to change the 15 pF balance capacitor on the card.

9. 30 kHz IF Amplifier

- Use a card extender to obtain access to the 30 kHz IF stage (card 6).

- Set up the instrument as in Section C.8.

- Be sure that the input attenuator control is in the FIXED position.

- Slew $f_o$ to 5000 Hz and peak L9 for a maximum amplitude reading.

- Lower $f_o$ to 4570 Hz and peak L10.

- Raise $f_o$ to 5436 Hz and peak L11.

- Reset $f_o$ to 5000 Hz and adjust the GAIN pot for an exactly full-scale meter reading (100 mV).

10. 10 kHz IF Amplifier

- Use a card extender to obtain access to the 10 kHz IF stage (card 7).
- Set the bandwidth to 300 Hz.
- Slew $f_o$ to 5000 Hz and peak L14 for a maximum amplitude reading.
- Lower $f_o$ to 4871 Hz and peak L15.
- Raise $f_o$ to 5131 Hz and peak L16.
- Reset $f_o$ to 5000 Hz and adjust the GAIN pot for an exactly full-scale meter reading (100 mV).

11. 3 kHz IF Amplifier

- Use a card extender to obtain access to the 3 kHz IF stage (card 8).
- Set the bandwidth to 100 Hz.
- Slew $f_o$ to 5000 Hz and peak L19 for a maximum amplitude reading.
- Lower $f_o$ to 4957 Hz and peak L20.
- Raise $f_o$ to 5044 Hz and peak L21.
- Reset $f_o$ to 5000 Hz and adjust the GAIN pot for an exactly full-scale meter reading (100 mV).

12. 1 kHz IF Amplifier

- Use a card extender to obtain access to the 1 kHz IF stage (card 9).
- Set the bandwidth to 30 Hz.
- Slew $f_o$ to 5000 Hz and peak L24 for a maximum amplitude reading.
- Raise $f_o$ to 4987 Hz and peak L25.
- Bring $f_o$ up to 5013 Hz and peak L26.
- Reset $f_o$ to 5000 Hz and adjust the GAIN pot for an exactly full-scale meter reading (100 mV).

13. 300 Hz IF Amplifier

- Use a card extender to obtain access to the 300 Hz IF stage (card 10).
- Set the bandwidth to 10 Hz.
- Slew $f_o$ to 5000 Hz and peak L29 for a maximum amplitude reading.
- Change $f_o$ to 4996 Hz and peak L30.
- Set $f_o$ to 5004 Hz and peak L31.
- Reset $f_o$ to 5000 Hz and adjust the GAIN pot for an exactly full-scale meter reading (100 mV).

14. IF Detector Symmetry

- Use a card extender to obtain access to the IF select, gain, and detector card (card 15).
- Connect an external signal source and attenuator to the input connector.
- Select the INPUT SIGNAL and inject a 5000 Hz sine-wave tone of sufficient amplitude to achieve a full-scale reading on the input level meter.
- Set the bandwidth to 300 Hz and the IF gain to 0 dB.
- Slew $f_o$ to 5000 Hz, and the output meter should read full-scale.
- Connect the oscilloscope to the detector output on card 15 at U3 pin 6 (the LM301AN) and adjust it to trigger on the rectified sine-wave signal.
- Lower the signal input by 60 dB, using the external attenuator.
- Increase the oscilloscope gain accordingly and adjust the SYMMETRY pot on card 15 for symmetrical peaks in the rectified signal.

  A few millivolts of dc offset may appear in the rectified signal, but this offset is unimportant.

- Decrease the input signal another 10 dB and trim the SYMMETRY pot.

  It should be possible to symmetrically rectify signals at least 70 dB below full-scale.

- Disconnect the external source.

15. Final Adjustment of IF Amplifier Gains

- Connect the dc voltmeter to the amplitude output connector.
- Set the input to CAL TONE, input level to 0.1 V, input attenuator to FIXED, IF gain to 0 dB, output mode to LINEAR, and $f_o$ to 5000 Hz.
- With all cards in place, turn the bandwidth to 1 kHz and adjust the GAIN pot on the 30 kHz IF stage (card 6) for a 5.00 Vdc reading on the voltmeter.
- Change the bandwidth to 300 Hz and adjust the GAIN pot on the 10 kHz IF stage (card 7) for an identical reading.
- Successively reduce the bandwidth and adjust the GAIN pots on the respective IF cards so that the output meter reading is 5.00 Vdc.

  This equalizes the gain between the IF stages. Absolute gain will be trimmed in the next step.

16. Linear and Log Output

- Leave the Filter and external dc voltmeter setup as in the previous stage.
- Set the bandwidth to 300 Hz.
- Temporarily disable the 5 kHz calibration tone by selecting the INPUT SIGNAL. Adjust the LIN ZERO pot on the log and output card (card 16) for a 0.00 Vdc output.
- Turn the 5 kHz cal tone back on and adjust the 30 kHz GAIN pot on card 6 for exactly 5.00 Vdc output, which will adjust the LINEAR mode zero and gain.
- Connect an external 5 kHz signal source and attenuator to the input and select the INPUT SIGNAL.
- Be sure that the attenuator is properly terminated (or use a minimum of 25 dB attenuation) so that the additional attenuation required in the following steps is correct.
- Switch the source level and input level controls for exactly 5.00 Vdc amplitude output.

- Change the output mode to LOG.
- Adjust the HI LOG offset pot on card 16 so that the output is 5.00 Vdc.
- Attenuate the signal 20 dB and adjust the LOG GAIN pot for 2.50 Vdc output.
- Attenuate the signal 60 dB and adjust the LO LOG offset pot for -2.50 Vdc output.

It will be necessary to repeat the above steps to achieve maximum linearity in the LOG output. The HI LOG pot sets the upper end of the scale, the LOG GAIN pot sets the scale span, and the LO LOG pot sets the lower end of the scale. With the correct adjustment, it may be possible to obtain correct readings to -70 dB (-3.75 V output) or -80 dB (-5.00 V output) although the last will not be stable. The output should decrease by 1.25 V for each 10 dB reduction in input level. Note that the LO LOG adjustment depends on the setting of the LIN ZERO pot which should not be varied during this procedure.

17. 30 kHz Discriminator

- Use a card extender to obtain access to the 30 kHz discriminator (card 19).
- Monitor the voltages at the test points on the card with the oscilloscope.
- Set the bandwidth to 1 kHz.
- Adjust the input for a full-scale amplitude reading with the 5 kHz cal tone.
- Increase $f_o$ to 6000 Hz and peak L12 for maximum signal level at TP12.
- Lower $f_o$ to 4000 Hz and peak L13 for maximum level at TP13.
- Raise $f_o$ to 5000 Hz and adjust the ZERO pot for zero deflection on the tracking error meter.
- Drop $f_o$ to 4500 Hz and adjust the GAIN pot for +500 Hz deflection.
- Bring $f_o$ up to 5500 Hz and check the tracking error meter for a reading of -500 Hz.

- Trim the GAIN pot to split the error between the -500 and +500 Hz readings if necessary.

18. 10 kHz Discriminator

- Use a card extender to obtain access to the 10 kHz discriminator (card 20).
- Set the bandwidth to 300 Hz.
- Slew $f_o$ to 5300 Hz and peak L17 for maximum voltage at TP17.
- Lower $f_o$ to 4700 Hz and peak L18 for maximum voltage at TP18.
- Raise $f_o$ to 5000 Hz and adjust the ZERO pot for zero tracking error.
- Drop $f_o$ to 4850 Hz and adjust the GAIN pot for +150 Hz tracking error.
- Bring $f_o$ up to 5150 Hz and check the tracking error meter for a reading of -150 Hz.
- Trim the GAIN pot to split the error between the -150 and +150 Hz readings if necessary.

19. 3 kHz Discriminator

- Use a card extender to obtain access to the 3 kHz discriminator (card 21).
- Set the bandwidth to 100 Hz.
- Slew $f_o$ to 5100 Hz and peak L22 for maximum voltage at TP22.
- Lower $f_o$ to 4900 Hz and peak L23 for maximum voltage at TP23.
- Raise $f_o$ to 5000 Hz and adjust the ZERO pot for xero tracking error.
- Drop $f_o$ to 4950 Hz and adjust the GAIN pot for +50 Hz tracking error.
- Bring $f_o$ up to 5050 Hz and check the tracking error meter for a reading of -50 Hz.
- Trim the GAIN pot to split the error between the -50 and +50 Hz readings if necessary.

20. 1 kHz Discriminator

- Use a card extender to obtain access to the 1 kHz discriminator (card 22).
- Set the bandwidth to 30 Hz.
- Slew $f_o$ to 5030 Hz and peak L27 for maximum voltage at TP27.
- Lower $f_o$ to 4970 Hz and peak L28 for maximum voltage at TP28.
- Raise $f_o$ to 5000 Hz and adjust the ZERO pot for zero tracking error.
- Drop $f_o$ to 4985 Hz and adjust the GAIN pot for +15 Hz tracking error.
- Bring $f_o$ up to 5015 Hz and check the tracking error meter for a reading of -15 Hz.
- Trim the GAIN pot to split the error between the -15 and +15 Hz readings.

21. 300 Hz Discriminator

- Use a card extender to obtain access to the 300 Hz discriminator (card 23).
- Set the bandwidth to 10 Hz.
- Slew $f_o$ to 5010 Hz and peak L32 for maximum voltage at TP32.
- Lower $f_o$ to 4990 Hz and peak L33 for maximum voltage at TP33.
- Raise $f_o$ to 5000 Hz and adjust the ZERO pot for zero tracking error.
- Drop $f_o$ to 4995 Hz and adjust the GAIN pot for +5 Hz tracking error.
- Bring $f_o$ up to 5005 Hz and check the tracking error meter for a reading of -5 Hz.
- Trim the GAIN pot to split the error between the -5 and +5 Hz readings, which may be as much as 1 Hz.

22. Discriminator Zero Adjustments

- Set the slew rate limit to 19,999 Hz/sec and the slew direction to UP/DOWN.

  The discriminator zeros are trimmed by tracking on the 5 kHz cal tone.

- Slew the initial frequency $f_o$ to 5000 Hz.

- Set the bandwidth to 1 kHz and place the Filter in the TRACK mode with the TRACK command; the system should track the 5 kHz cal tone.

- Adjust the 30 kHz discriminator ZERO pot on card 19 so that the frequency display indicates 5000 Hz.

  This display will be dithering between 4999 and 5001 Hz at a few pulses per sec.

- Set the bandwidth to 300 Hz and adjust the 10 kHz discriminator ZERO pot for $f_o$ = 5000 Hz.

  The frequency display will be dithering between 5000 and 5001 Hz.

- Successively lower the bandwidth and adjust the ZERO pots on the 3 and 1 kHz and 300 Hz discriminators for 5000 Hz $f_o$.

  Note that, after the discriminator is selected, there is up to 3 sec of delay before it turns on.

23. Discriminator Slew Rates

The following adjustments will set the discriminator slew rate pulse generator (VCO) for an optimal slew rate and transient settling time.

- Set the bandwidth to 1 kHz and track the 5 kHz cal tone. Adjust the DITHER pot on the discriminator select and slew card (card 24) so that the frequency display is dithering between 4999 and 5001 Hz at 5 to 10 cycles/sec.

  If the dither is set too low, the display will not reach 5000 Hz and will remain stationary; if it is set too high, the system may dither by many hertz in $f_o$.

- Connect the oscilloscope to the discriminator output on the rear panel.

- Set the bandwidth to 300 Hz.

- Turn the track delay time to 0.01 sec and the control switch to ON.

- Turn the maximum track duration time to 0.10 sec and the control switch to ON.

- Set the slew rate limit to 19,999 Hz/sec and the direction switch to UP/DOWN.

- Switch the frequency limit control to OFF.

- In the RESET mode, slew the initial frequency to 5300 Hz.

- Press the AUTO command, and the system should begin tracking the 5 kHz cal tone and then reset to 5300 Hz.

- Trigger the oscilloscope on the down-going portion of the output discriminator waveform.

  A signal should appear that limits at -5 or -6 V while the system is reset and it should increase rapidly when the system begins to track.

- Set the 10k/30k slew rate adjustment on card 24 so that the discriminator output increases to +1 V and then settles down to 0 V without undershooting zero.

  This maximizes the slew rate and minimizes the settling time. If the slew rate adjustment is set too low, the system will take too long in slewing to 5000 Hz; if it is set too high, the system will ring as it settles down. To check the adjustment, set the slew direction switch to DOWN ONLY and increase the track duration to 1 sec. The system will track down and overshoot 5000 Hz, but it will be unable to track back up and will remain at the lowest frequency reached. The overshoot should be approximately 10 percent of the IF bandwidth or 30 Hz.

- Set the bandwidth to 100 Hz, initial frequency to 5100 Hz, track delay to 0.02 sec, and track duration to 0.20 sec.

- Repeat the above procedure--adjusting the 3k slew rate adjustment for a 1 V discriminator overshoot; the frequency overshoot will be approximately 10 Hz.

- Set the bandwidth to 30 Hz, initial frequency to 5030 Hz, track delay to 0.06 sec, track duration to 0.40 sec, and adjust the 1k slew rate adjustment for a 1 V discriminator overshoot; the frequency overshoot will be 3 Hz.

- Set the bandwidth to 10 Hz, initial frequency to 5010 Hz, track delay to 0.20 sec, track duration to 1.50 sec, and adjust the 300 slew rate adjustment for a 1 V discriminator overshoot; the frequency overshoot will be 1 Hz.

24. $F_{DC}$ Zero and Gain

This step adjusts the $F_{DC}$ D/A converter on card 44. This adjustment need not be performed unless desired because the circuit is stable and does not affect system accuracy.

- Remove the upper chassis.
- Connect the digital dc voltmeter to the $F_{DC}$ output on the rear panel.
- Set the $F_{DC}$ range switch to the $\pm 500$ Hz range.
- Turn the instrument on and, in the RESET mode, slew $f_o$ to 5000 Hz.
- Adjust the ZERO pot on card 44 for a 0.00 Vdc output.
- Press the TRACK command and increase $f_o$ to 5500 Hz.
- Adjust the GAIN control on card 44 for 5.00 Vdc output.
- Slew back to 5000 Hz and check the zero output.
- Drop to 4501 Hz and check the output for -4.99 Vdc.

# APPENDIX

This appendix contains system block diagrams, card cage layouts and wiring diagrams, and schematics for each card of the Tracking Filter.

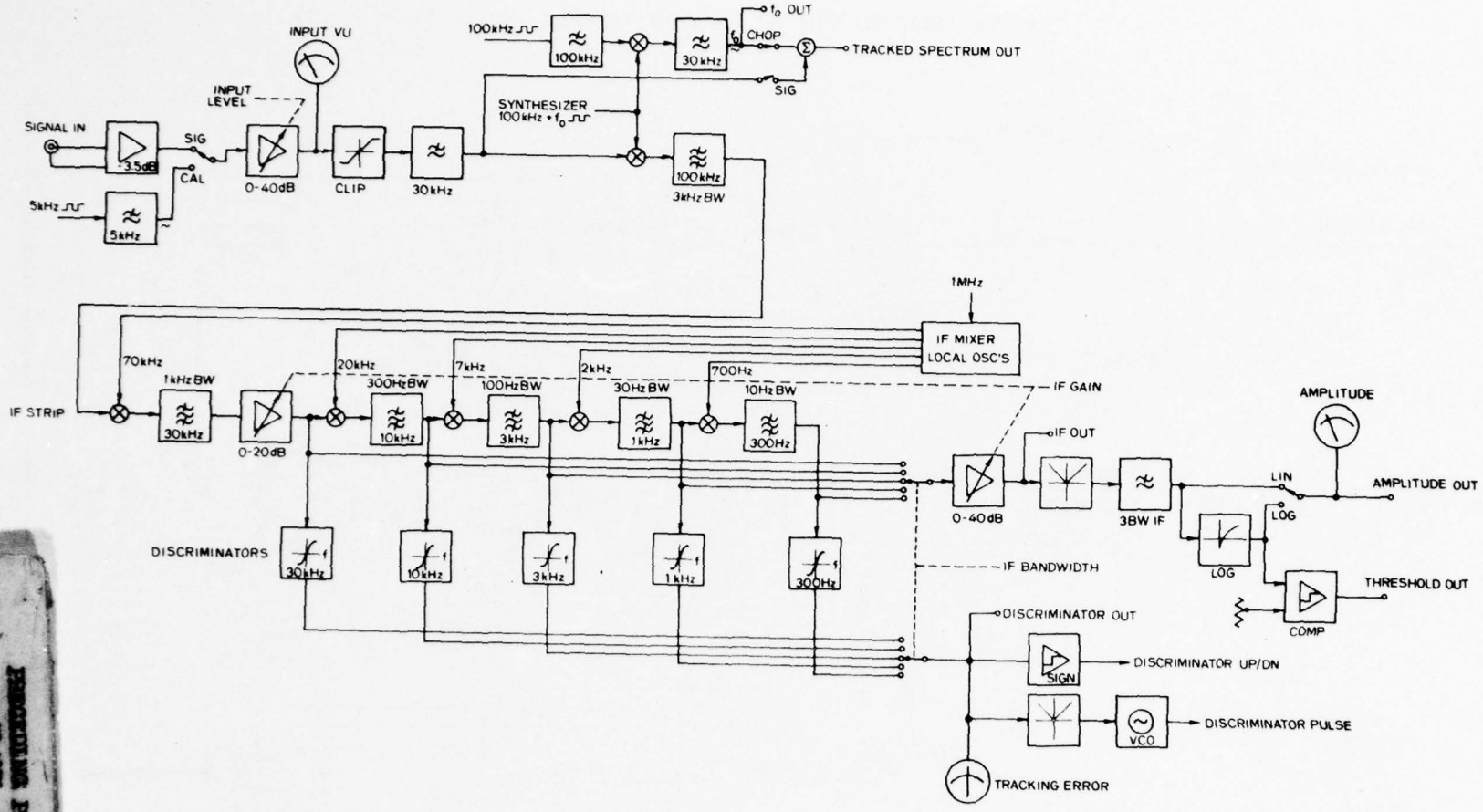



Fig. A.1. ANALOG SECTION OF THE TRACKING FILTER.



REPRODUCTION BADE NOT FILMED
BLANK

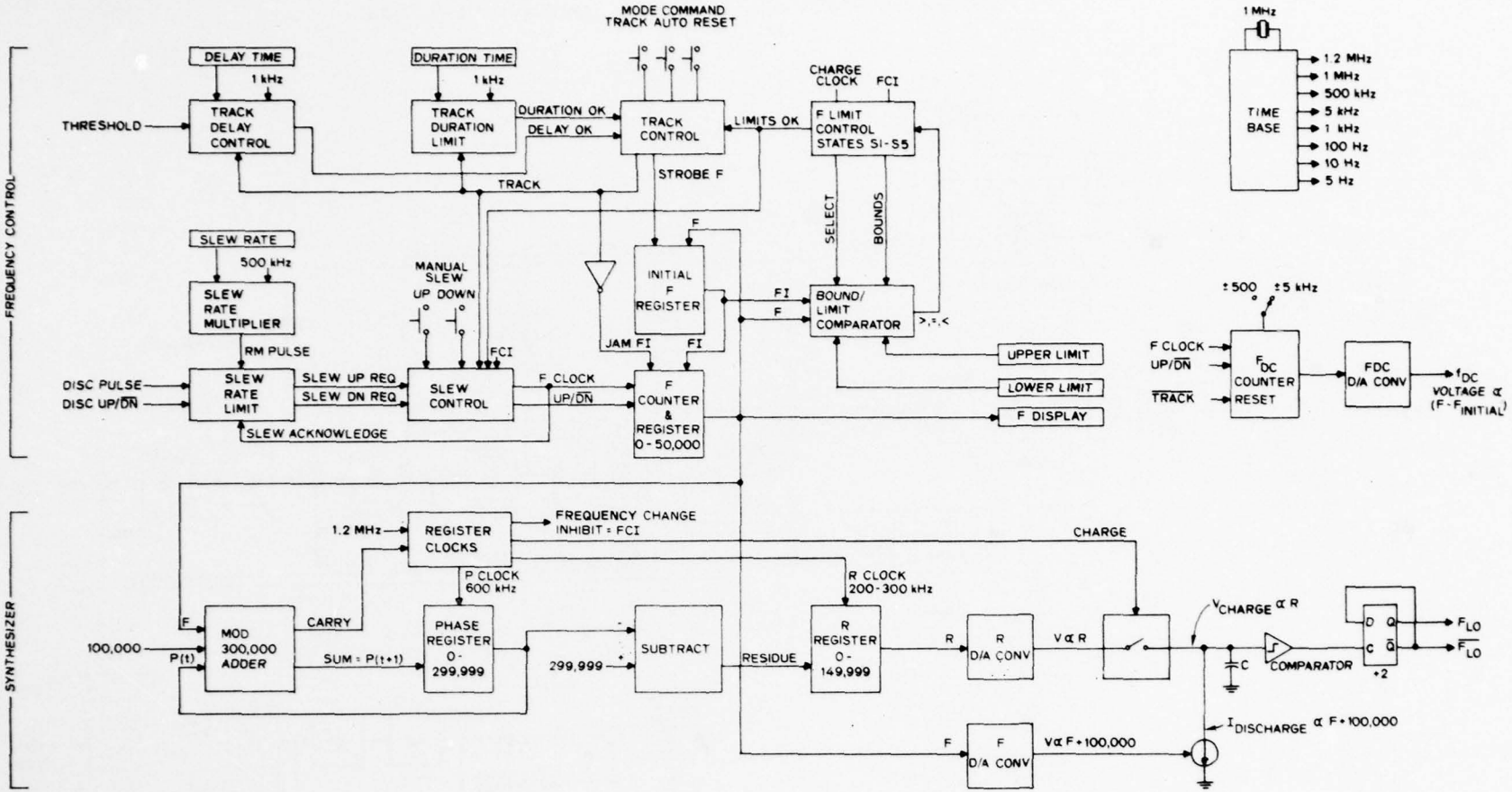



Fig. A.2. DIGITAL SECTION OF THE TRACKING FILTER.

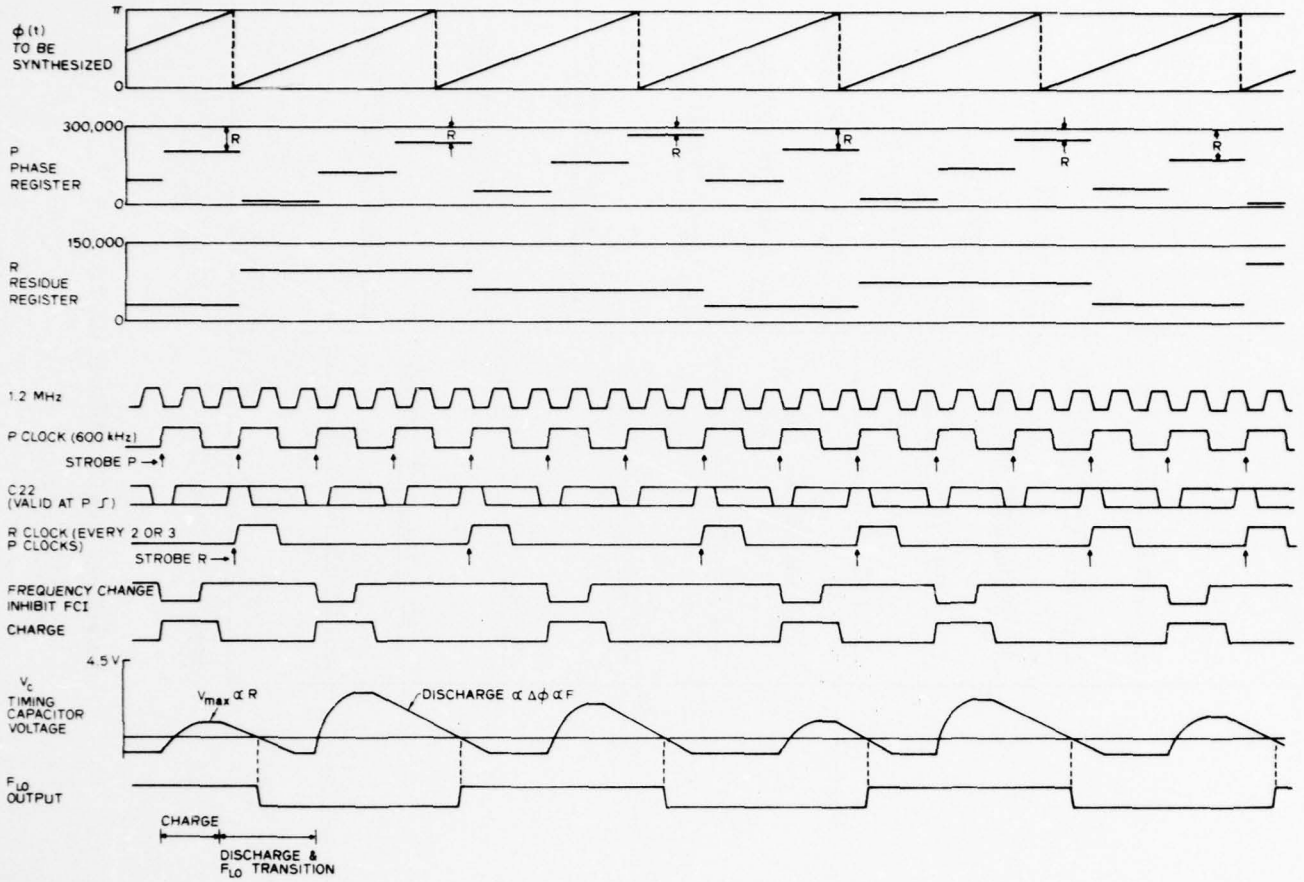



Fig. A.3. SYNTHESIZER TIMING.

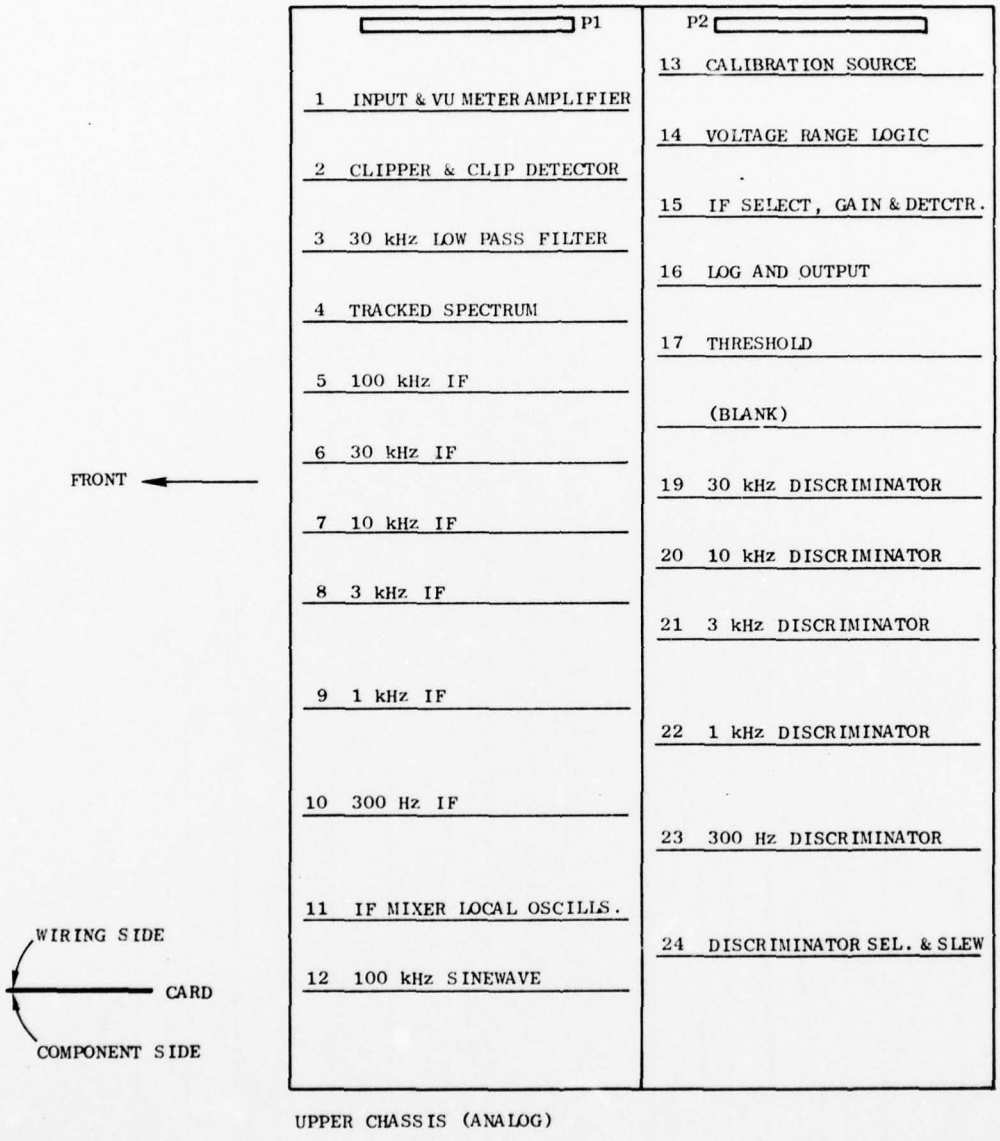



Fig. A.4. CARD CAGE LAYOUT.

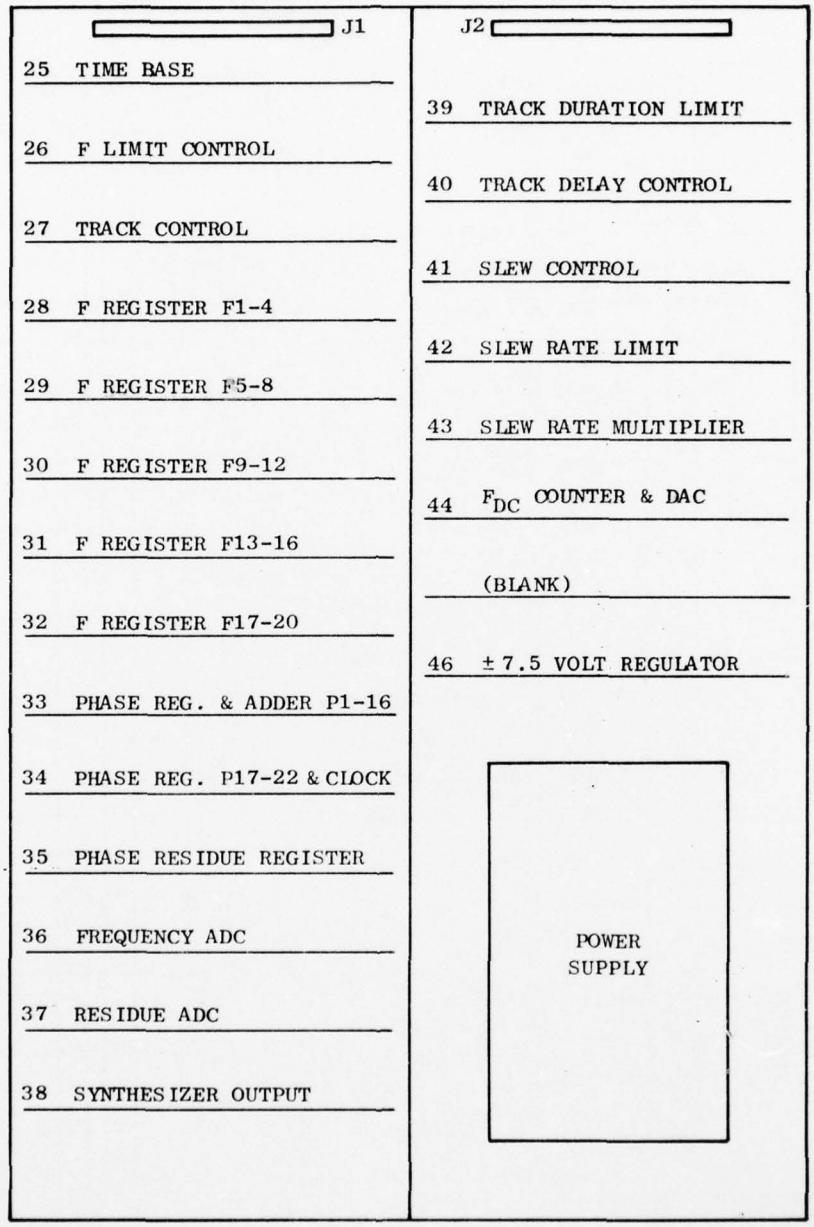
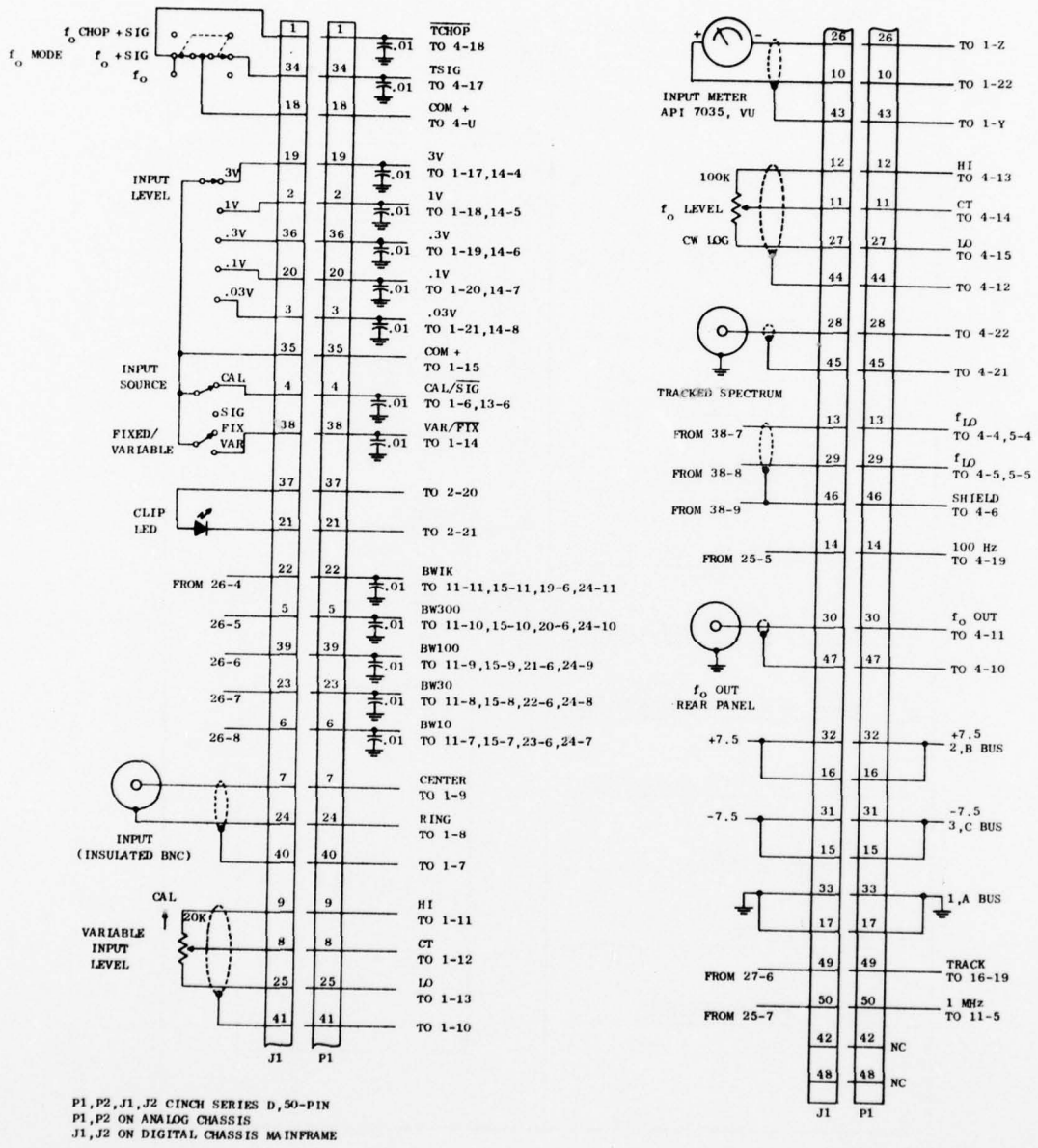



Fig. A.4. CONTINUED.




P1,P2,J1,J2 CINCH SERIES D,50-PIN
P1,P2 ON ANALOG CHASSIS
J1,J2 ON DIGITAL CHASSIS MAINFRAME

Fig. A.5. INTERCHASSIS WIRING.

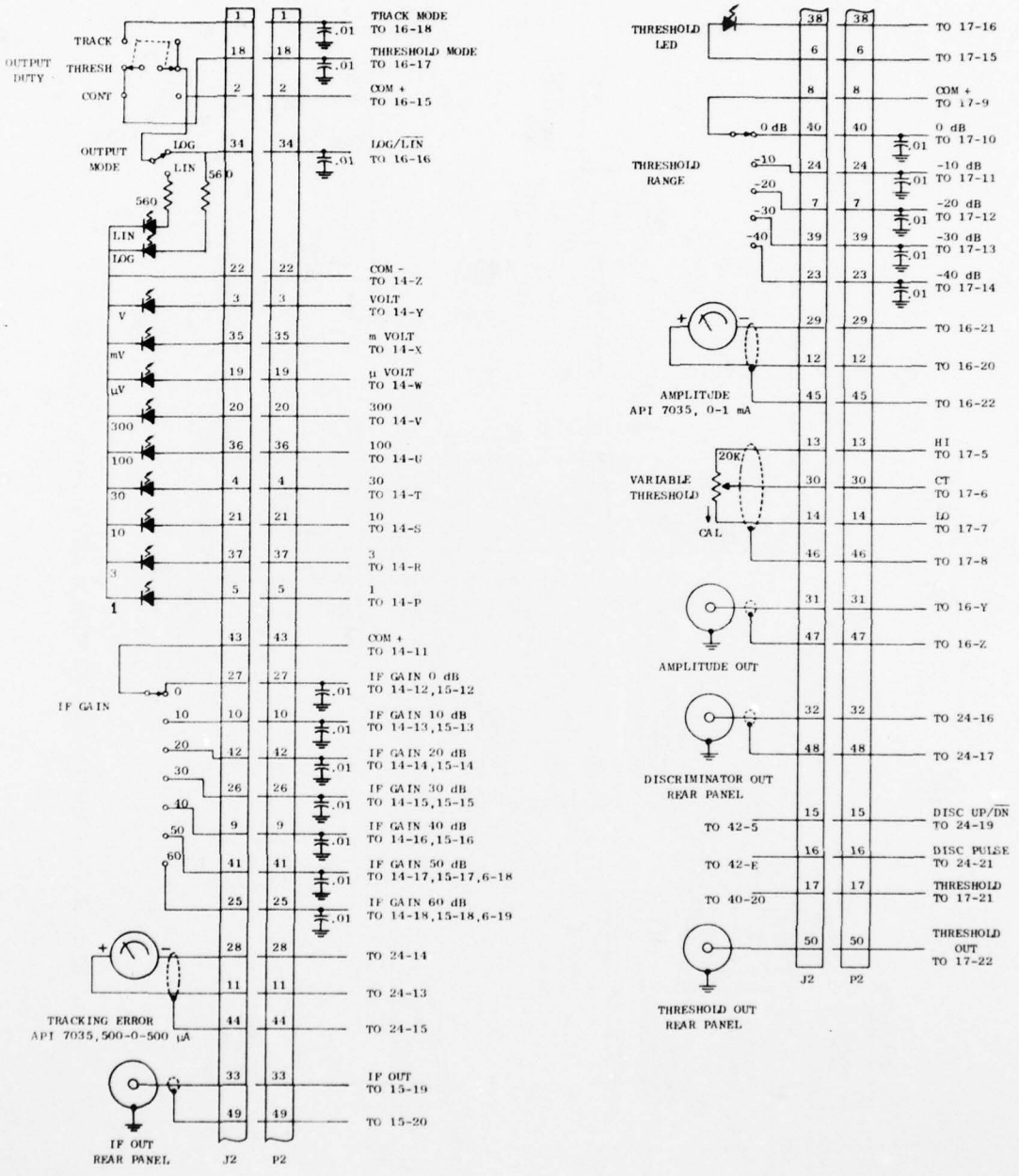



Fig. A.5. CONTINUED.

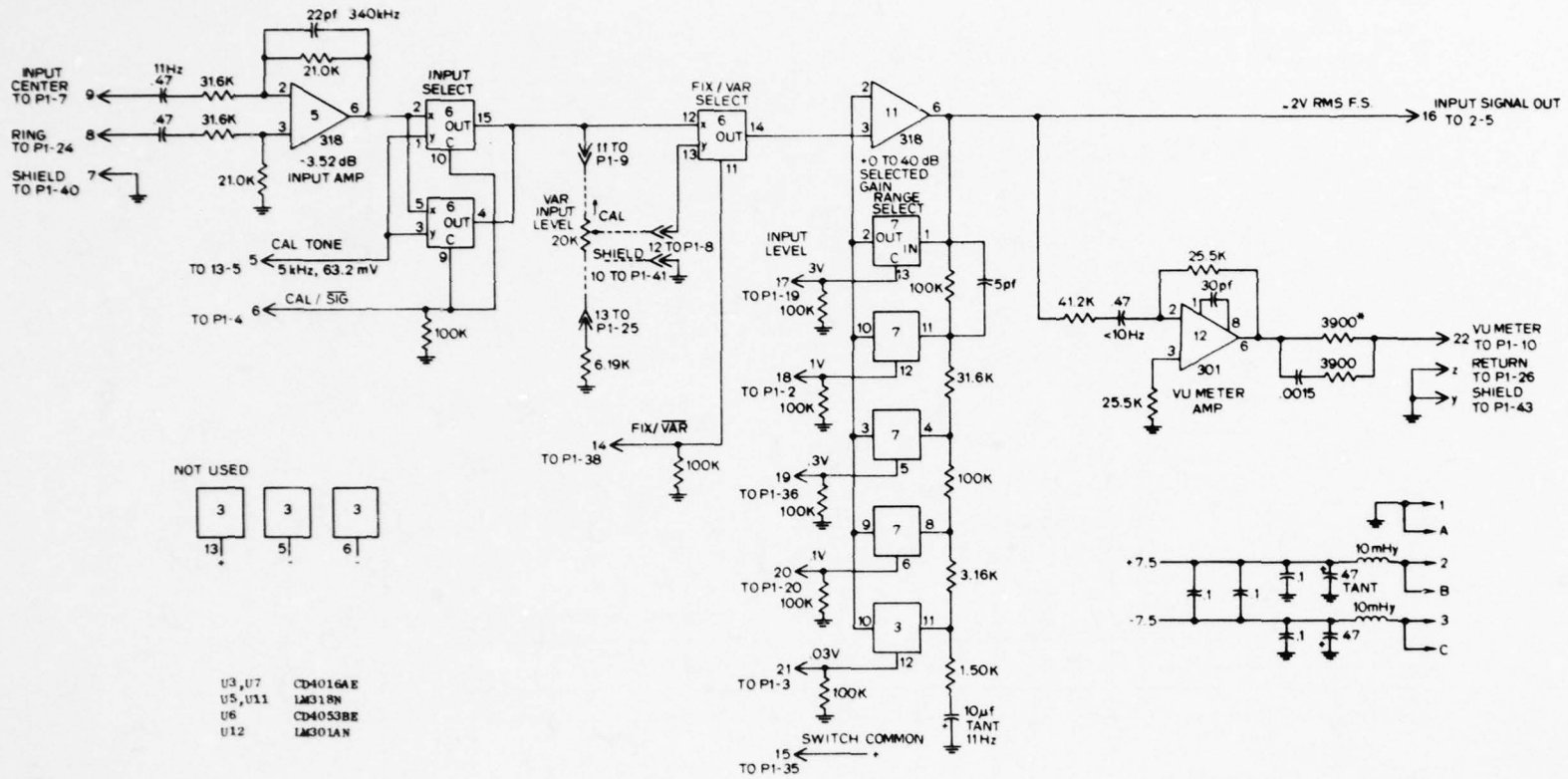


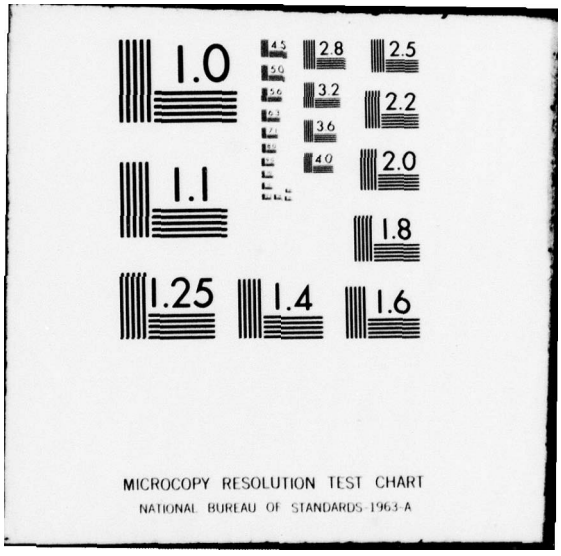

Fig. A.6. INPUT AND VU METER AMPLIFIER (CARD 1).

AD-A062 687 STANFORD UNIV CALIF STANFORD ELECTRONICS LABS F/G 14/2
INSTRUCTION MANUAL FOR THE AUDIO-FREQUENCY TRACKING FILTER.(U)
SEP 78 E W PASCHAL. N00014-75-C-0601
UNCLASSIFIED TR-3477-2 NL

2 OF 2
AD
A062887



END
DATE
FILMED
3-79
DDC


1.0
1.1
1.25
1.4
1.6
2.8
3.2
3.6
4.0
2.5
2.2
2.0
1.8
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

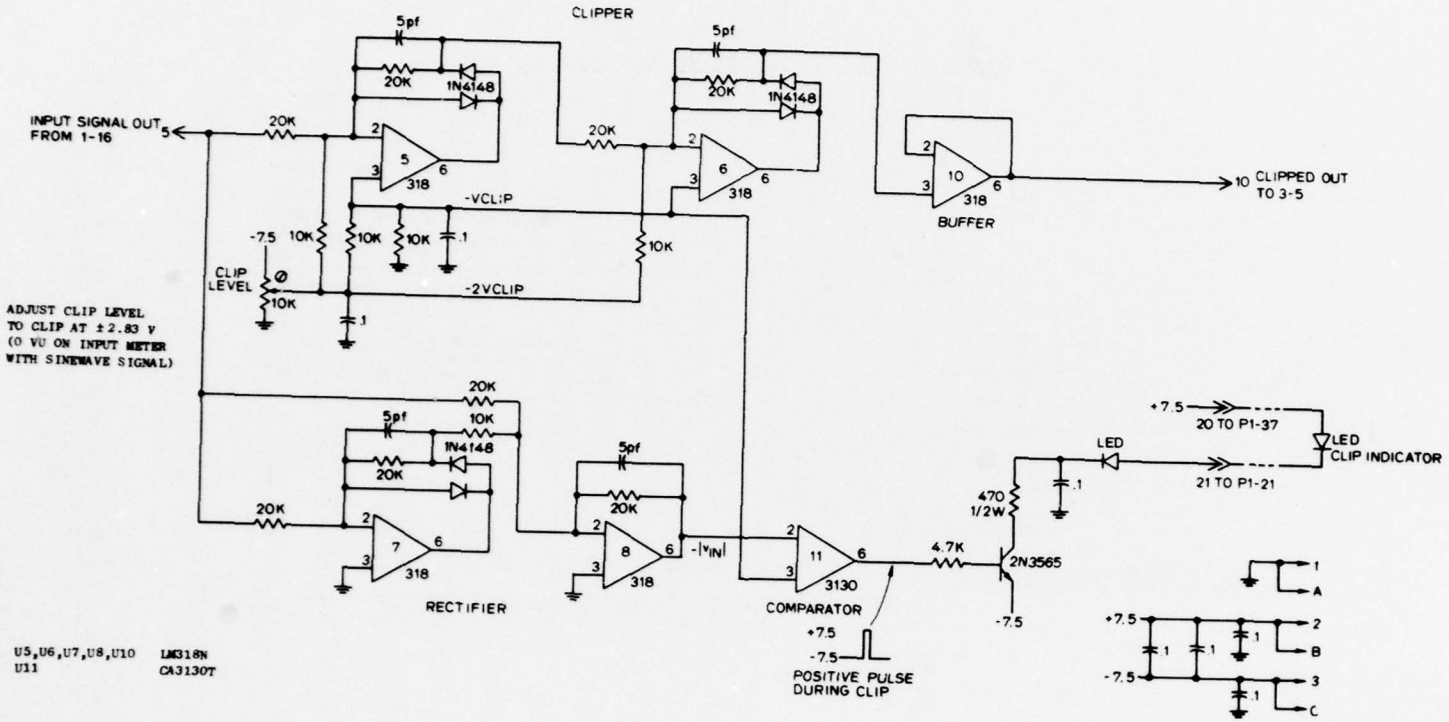
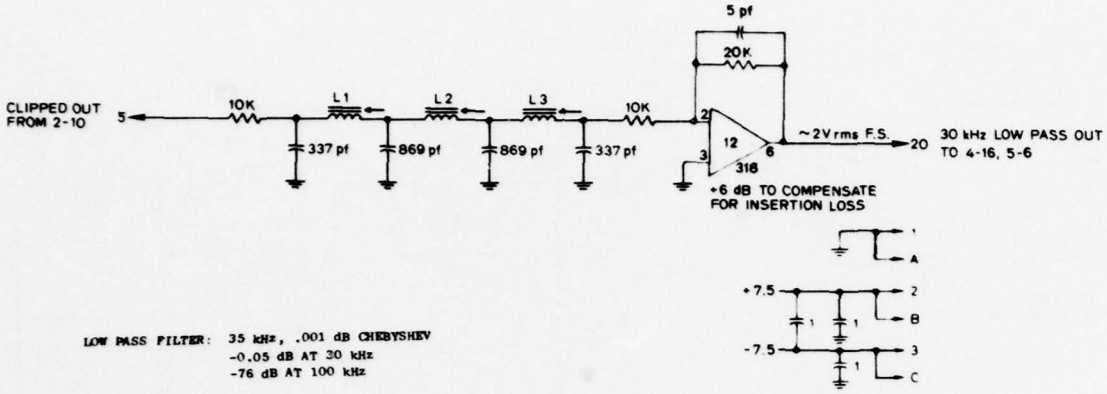



Fig. A.7. CLIPPER AND CLIP DETECTOR (CARD 2).




LOW PASS FILTER: 35 kHz, .001 dB CHEBYSHEV
-0.05 dB AT 30 kHz
-76 dB AT 100 kHz

POT CORES: MAGNETICS G-41811-25

$L_1, L_3$: 52OT #36, L = 71.0 mHy, Q(1 kHz) = 18, 24 Ω dc

$L_2$: 58OT #36, L = 88.3 mHy, Q = 20, 28 Ω dc

INDUCTORS ADJUSTED DURING ASSEMBLY

U12: LM318N

Fig. A.8. 30 kHz LOWPASS FILTER (CARD 3).

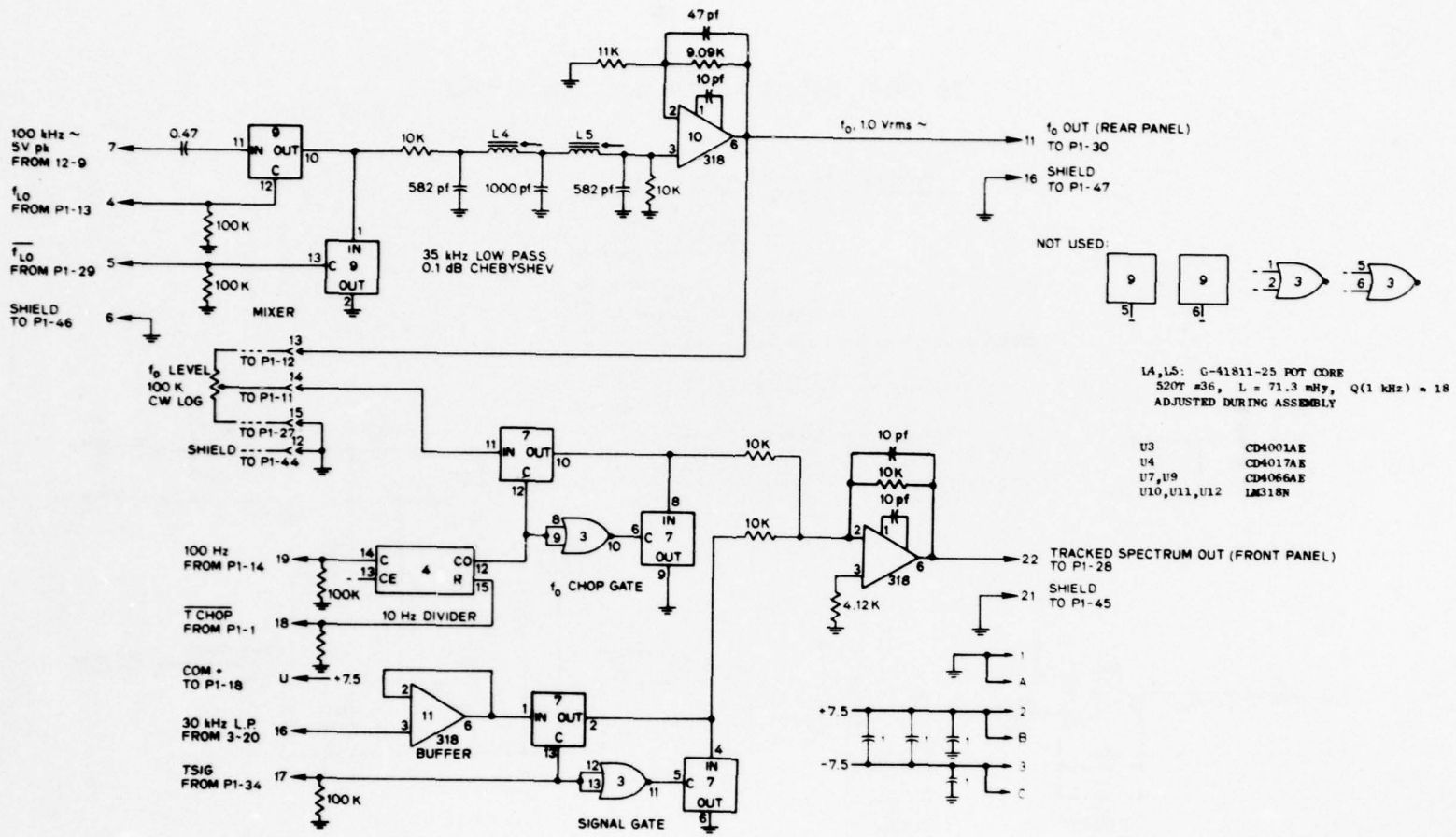
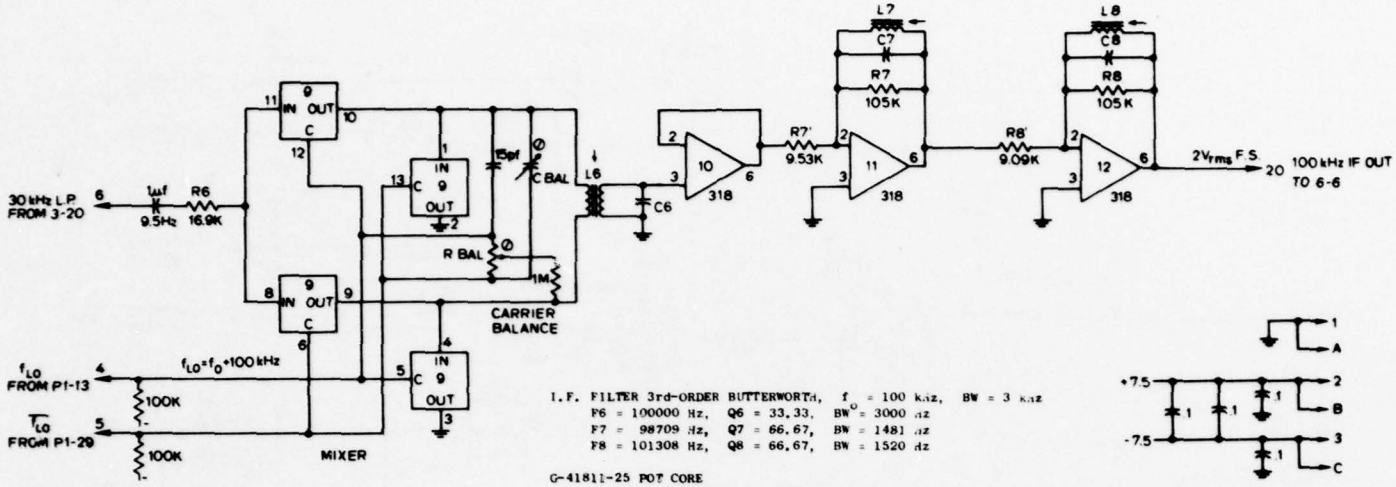



Fig. A.9. TRACKED SPECTRUM (CARD 4).



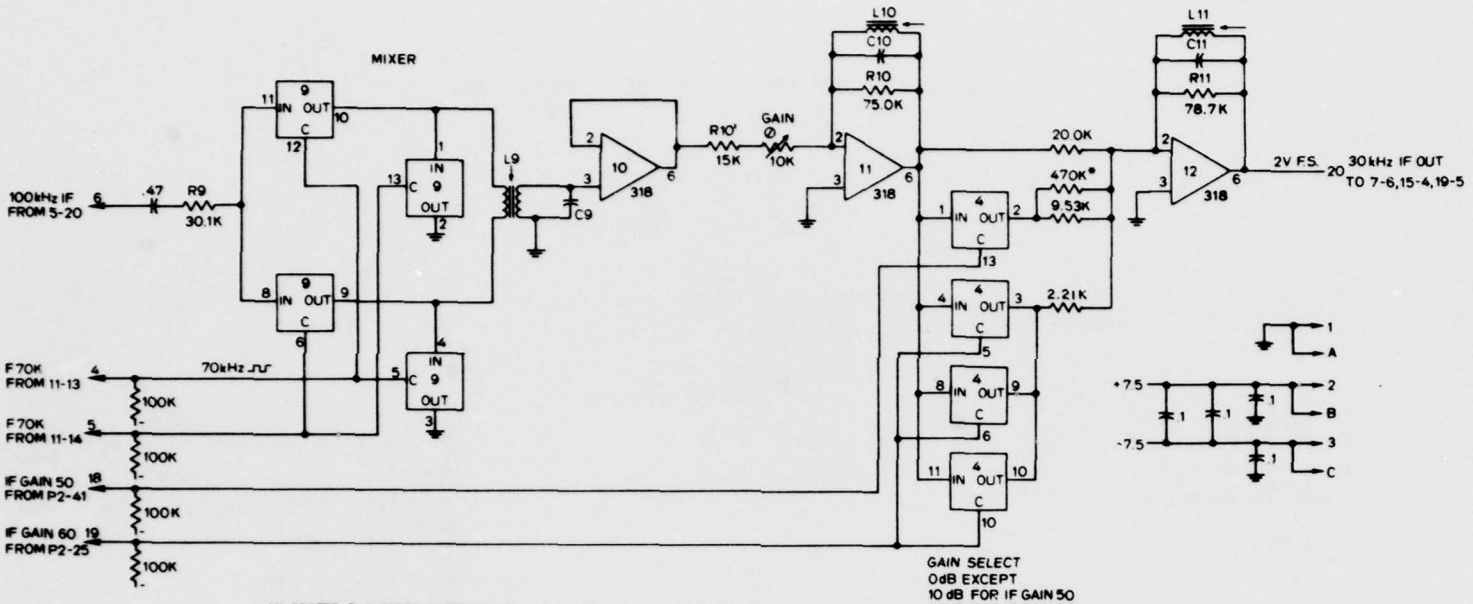

I.F. FILTER 3rd-ORDER BUTTERWORTH, $f_o$ = 100 kHz, BW = 3 kHz
F6 = 100000 Hz, Q6 = 33.33, BW = 3000 Hz
F7 = 98709 Hz, Q7 = 66.67, BW = 1481 Hz
F8 = 101308 Hz, Q8 = 66.67, BW = 1520 Hz

G-41811-25 POT CORE
L6: 2 × 49T #28, L = 650 µHy, Q(1 kHz) = 8
L7, L8: 49T #24, L = 650 µHy, Q = 13

C6, C7, C8: ≈ .0039 µf (1800 pf POLYSTYRENE + GLASS TO RESONATE)
R6, R7, R8 SELECTED FOR Q's
R7', R8' SELECTED FOR 0 dB OVERALL GAIN
U9 CD4016AE
U10, U11, U12 LM318N

*ALIGNMENT WITH 5 kHz CAL:*
PEAK L6 @ 5000 Hz
PEAK L7 @ 3709 Hz
PEAK L8 @ 3308 Hz
ADJUST CARRIER BALANCE CONTROLS FOR MINIMUM OUTPUT
WITH NO SIGNAL AT MINIMUM TRACKING FREQUENCY

Fig. A.10. 100 kHz IF FILTER (CARD 5).



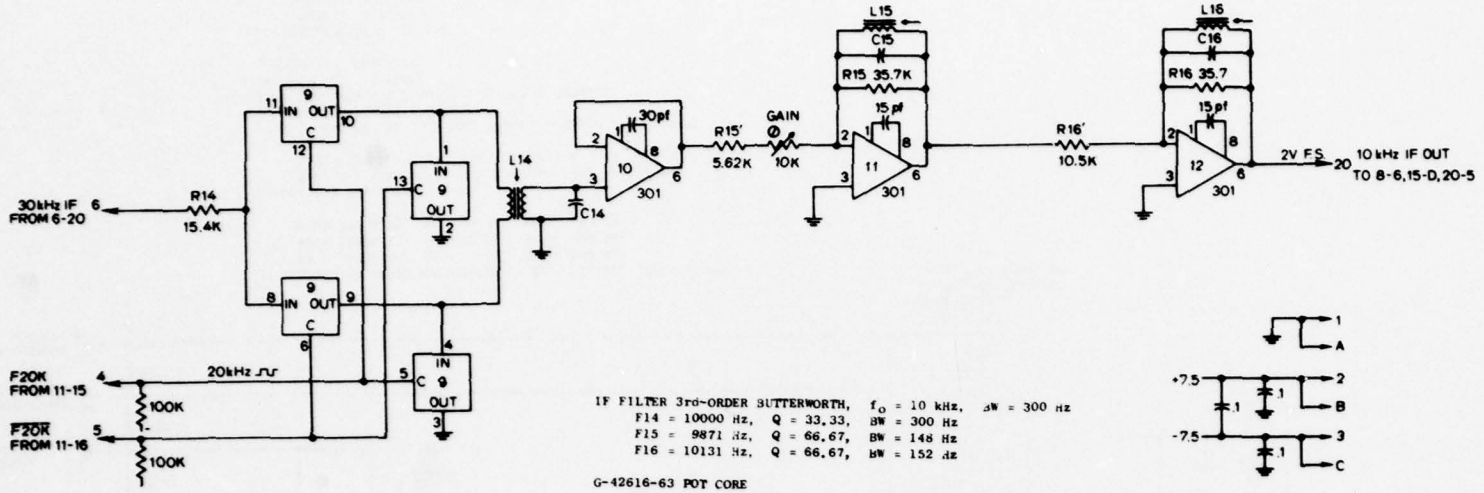

IF FILTER 3rd-ORDER BUTTERWORTH, $f_o$ = 30 kHz, BW = 1 kHz
F9 = 30000 Hz, Q = 30.00, BW = 1000 Hz
F10 = 29570 Hz, Q = 60.01, BW = 493 Hz
F11 = 30436 Hz, Q = 60.01, BW = 507 Hz

G-42213-40 POT CORE
L9: 2 × 108T #28, L = 5.0 mHy, Q(1 kHz) = 28
L10, L11: 108T #26, L = 5.0 mHy, Q = 44

C9, C10, C11: ≈ .0056 μF NPO CERAMIC + GLASS TO RESONATE
R9, R10, R11 SELECTED FOR Q's
R10' SELECTED FOR GAIN (0, 10, 20 dB OVERALL)
U4, U9 CD4066AE
U10, U11, U12 LM318N

ALIGNMENT WITH 5 kHz CAL:
PEAK L9 @ 5000 Hz
PEAK L10 @ 4570 Hz
PEAK L11 @ 5436 Hz

Fig. A.11. 30 kHz IF FILTER (CARD 6).



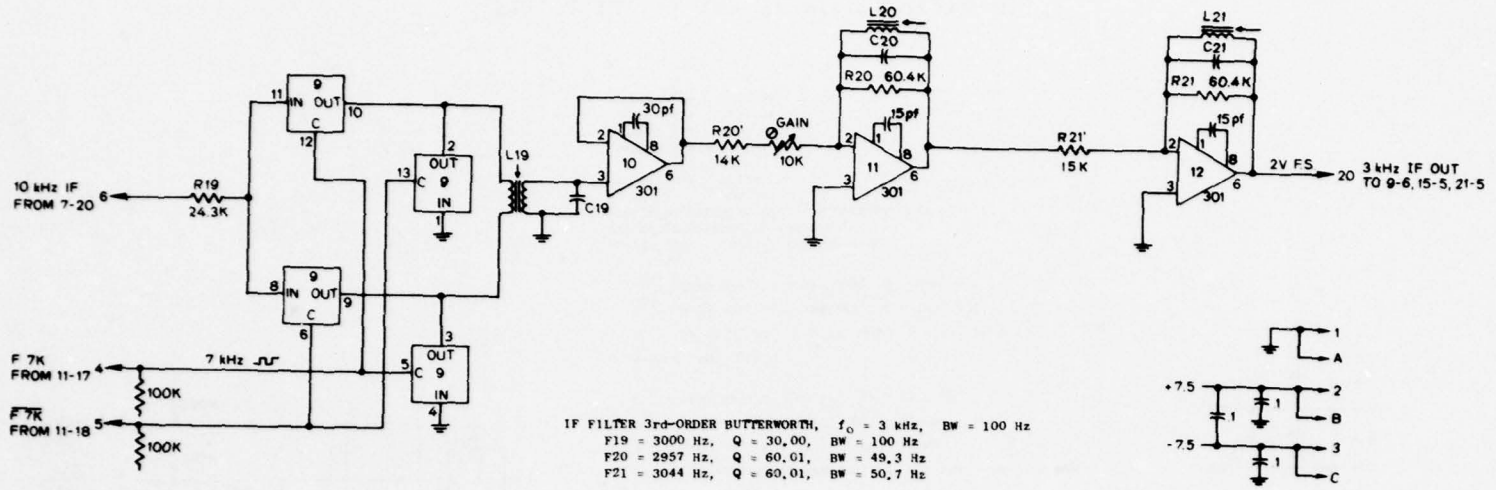

IF FILTER 3rd-ORDER BUTTERWORTH, $f_o$ = 10 kHz, $\Delta W$ = 300 Hz
F14 = 10000 Hz, Q = 33.33, BW = 300 Hz
F15 = 9871 Hz, Q = 66.67, BW = 148 Hz
F16 = 10131 Hz, Q = 66.67, BW = 152 Hz

G-42616-63 POT CORE
L14: 2 × 100T #28, L = 6.55 mHy
L15, L16: 100T #24, L = 6.55 mHy

C14, C15, C16: = .038 μF (.033 μF NPO CERAMIC + GLASS TO RESONATE)
R14, R15, R16 SELECTED FOR Q's
R15', R16' SELECTED FOR GAIN, 0dB OVERALL
U9 CD4066AE
U10, U11, U12 LM301AN

ALIGNMENT WITH 5 kHz CAL:
PEAK L14 @ 5000 Hz
PEAK L15 @ 4871 Hz
PEAK L16 @ 5131 Hz

Fig. A.12. 10 kHz IF FILTER (CARD 7).



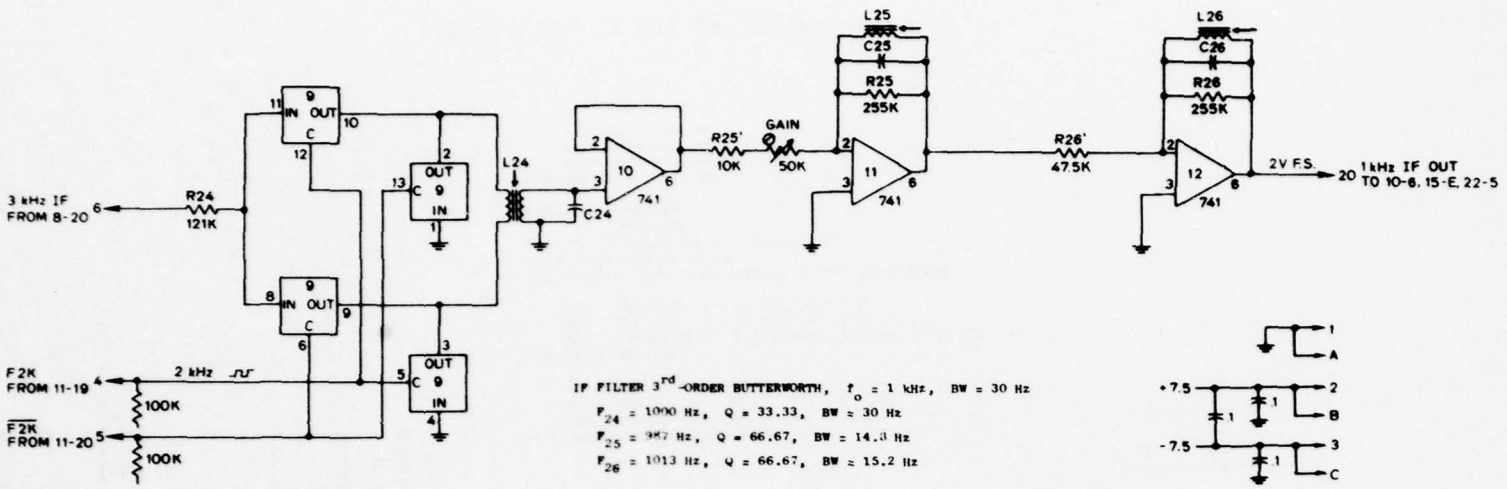

IF FILTER 3rd-ORDER BUTTERWORTH, $f_o$ = 3 kHz, BW = 100 Hz
F19 = 3000 Hz, Q = 30.00, BW = 100 Hz
F20 = 2957 Hz, Q = 60.61, BW = 49.3 Hz
F21 = 3044 Hz, Q = 60.01, BW = 50.7 Hz

G-43019-X1 POT CORE
L19: 2 × 200T #28, L = 39 mHy, Q(1 kHz) = 85, 2.5 Ω dc
L20: 204T #26, L = 41 mHy, Q = 135, 1.7 Ω
L21: 198T #26, L = 39 mHy, Q = 135

C19, C20, C21: .068 μF NPO CERAMIC + GLASS TO RESONATE
R19, R20, R21 SELECTED FOR Q's
R20', R21' SELECTED FOR 0 dB OVERALL GAIN
U9 CD4066AE
U10, U11, U12 LM301AN

ALIGNMENT WITH 5 kHz CAL:
PEAK L19 @ 5000 Hz
PEAK L20 @ 4957 Hz
PEAK L21 @ 5044 Hz

Fig. A.13. 3 kHz IF FILTER (CARD 8).




IF FILTER 3rd-ORDER BUTTERWORTH, $f_o$ = 1 kHz, BW = 30 Hz

$F_{24}$ = 1000 Hz, Q = 33.33, BW = 30 Hz

$F_{25}$ = 987 Hz, Q = 66.67, BW = 14.8 Hz

$F_{26}$ = 1013 Hz, Q = 66.67, BW = 15.2 Hz

G-43019-X1 POT CORE

$L_{24}$: 2X 571T #34, L = 320 mHy, Q = 73, 25.5 Ω dc

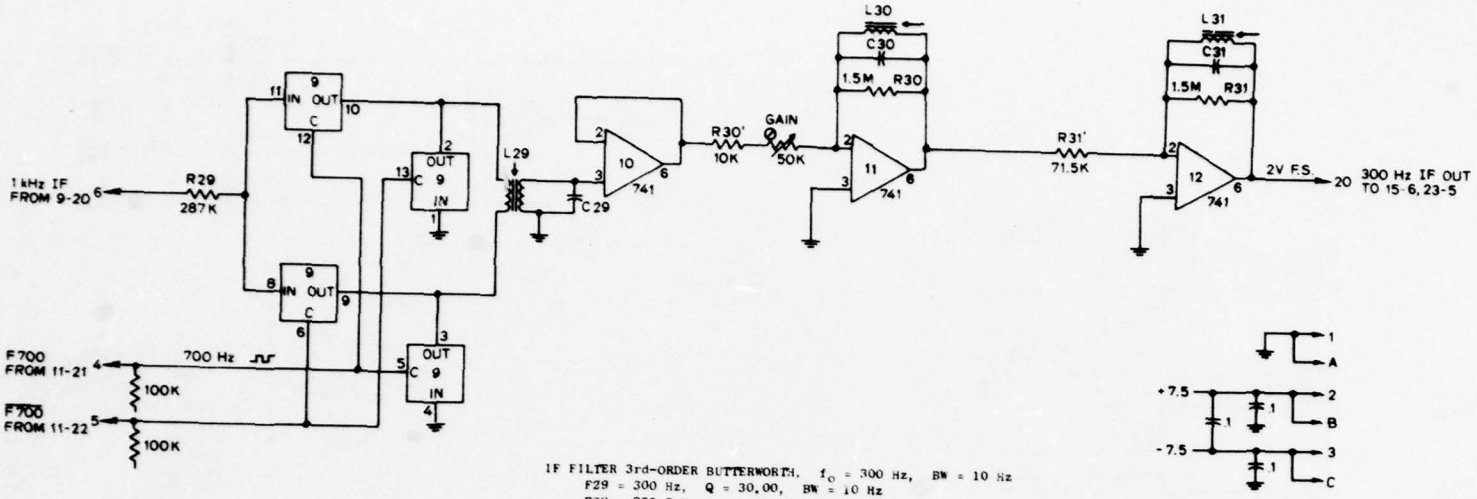
$L_{25}$: 577T #30, L = 326 mHy, Q = 135, 9.4 Ω

$L_{26}$: 556T #30, L = 331 mHy, Q = 135, 9.4 Ω

C24,C25,C26: .082 μF NPO CERAMIC
R24,R25,R26 SELECTED FOR Q's
R25',R26' SELECTED FOR 0 dB OVERALL GAIN
U9 CD4066AE
U10,U11,U12 MC1741CP

ALIGNMENT WITH 5 kHz CAL:
PEAK L24 @ 5000 Hz
PEAK L25 @ 4987 Hz
PEAK L26 @ 5013 Hz

Fig. A.14. 1 kHz IF FILTER (CARD 9).




IF FILTER 3rd-ORDER BUTTERWORTH, $f_o$ = 300 Hz, BW = 10 Hz
F29 = 300 Hz, Q = 30.00, BW = 10 Hz
F30 = 295.7 Hz, Q = 60.01, BW = 4.9 Hz
F31 = 304.4 Hz, Q = 60.01, BW = 5.1 Hz

G-43428-X1 POT CORE
L29: 2 × 1275T #34, L = 1.72 Hy, Q(1 kHz) = 150, 71 Ω dc
L30: 1278T #32, L = 1.76 Hy, Q = 250, 44 Ω
L31: 1250T #32, L = 1.66 Hy, Q = 250, 42 Ω

C29, C30, C31: .164 μF NPO CERAMIC
R29, R30, R31 SELECTED FOR Q's
R30', R31' SELECTED FOR 0 dB OVERALL GAIN
U9 CD4066AE
U10, U11, U12 MC1741CP

ALIGNMENT WITH 5 kHz CAL:
PEAK L29 @ 5000 Hz
PEAK L30 @ 4996 Hz
PEAK L31 @ 5004 Hz

Fig. A.15. 300 Hz IF FILTER (CARD 10).

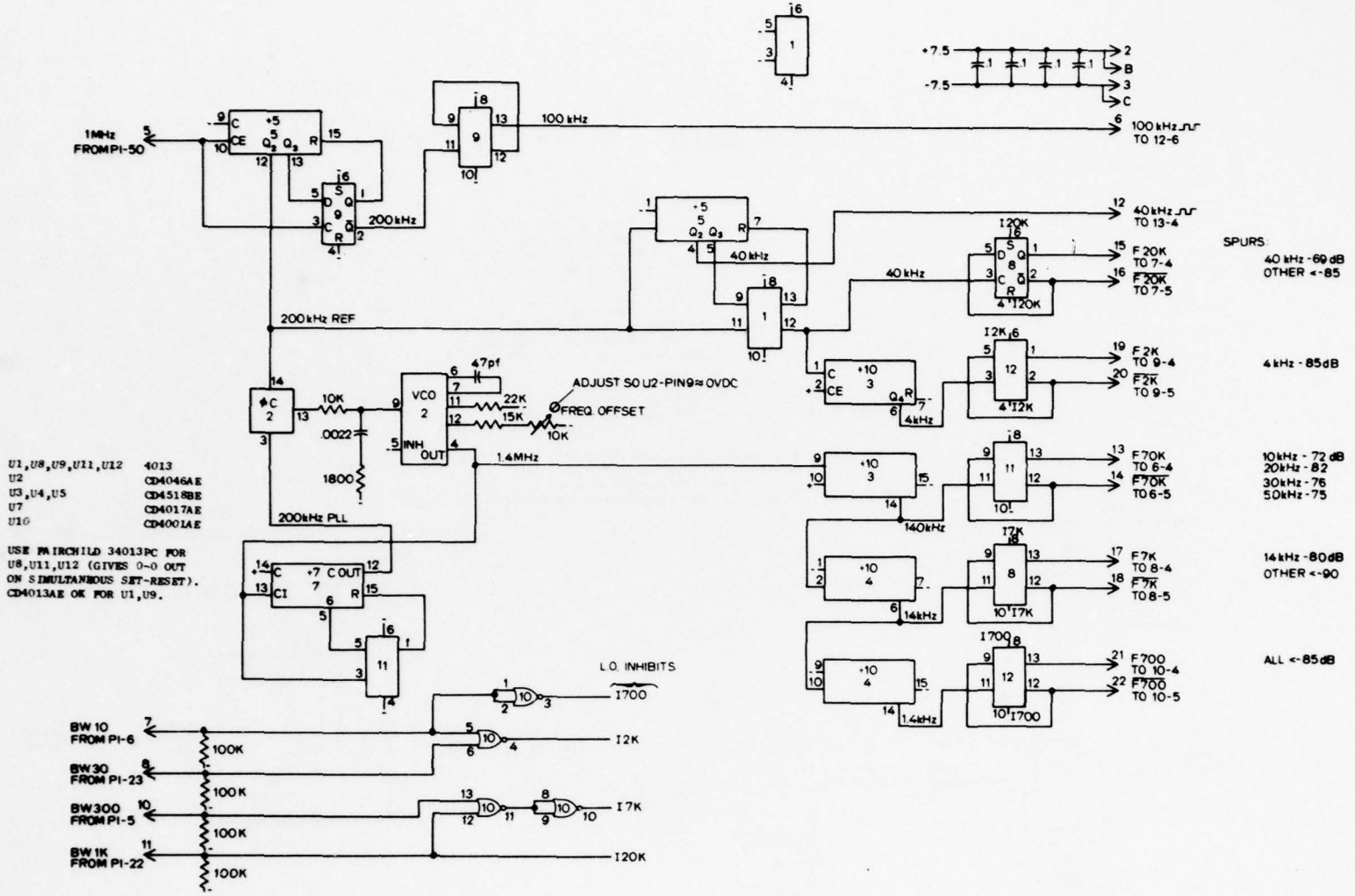
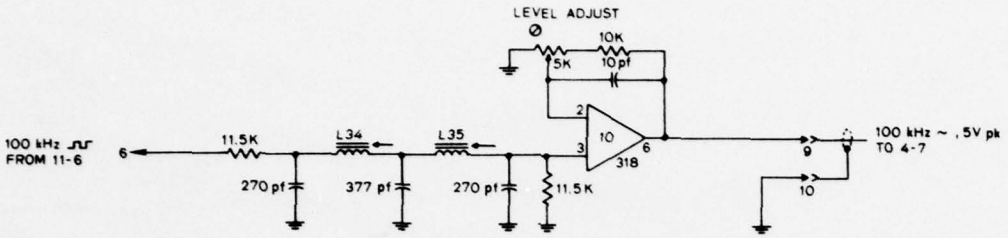



Fig. A.16. IF MIXER LOCAL OSCILLATORS (CARD 11).




LOW PASS FILTER: 5th-ORDER 1 dB CHEBYSHEV
$f_{3dB}$ = 108.7 kHz
~ 0 dB @ 100 kHz
~ -62 dB @ 300 kHz

L34,L35: G-41811-25 POT CORE
260T #32 ON DOUBLE BOBBIN
18.0 mHy, Q = 21 (1 kHz)
~ 19.4 mHy @ 100 kHz

U1) LM318N

LEVEL ADJUST SETS $f_o$ OUTPUT AMPLITUDE

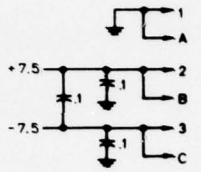
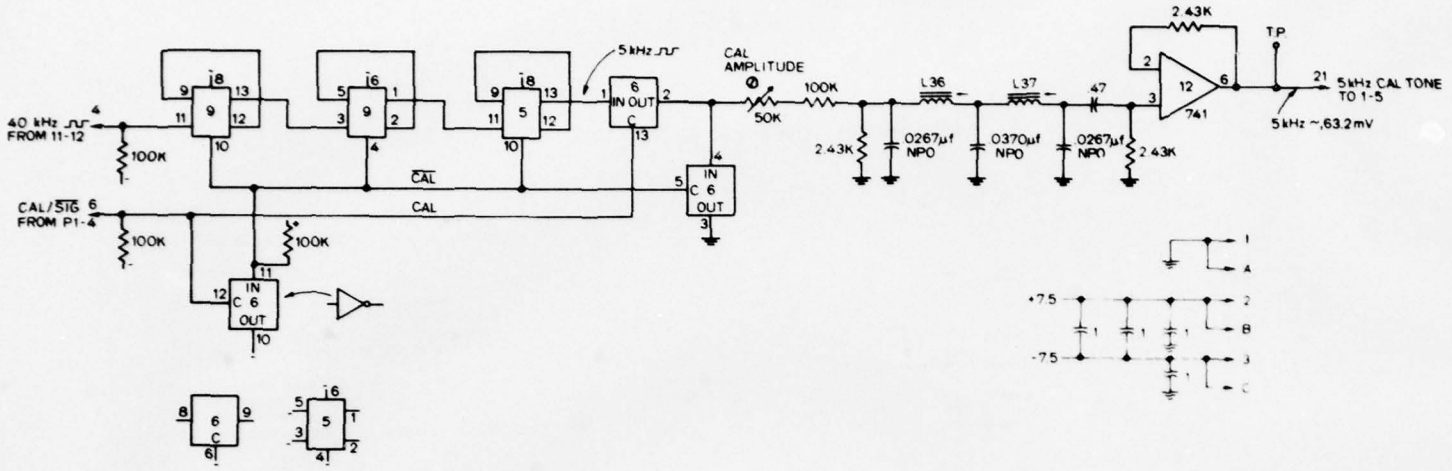



Fig. A.17. 100 kHz SINE WAVE (CARD 12).

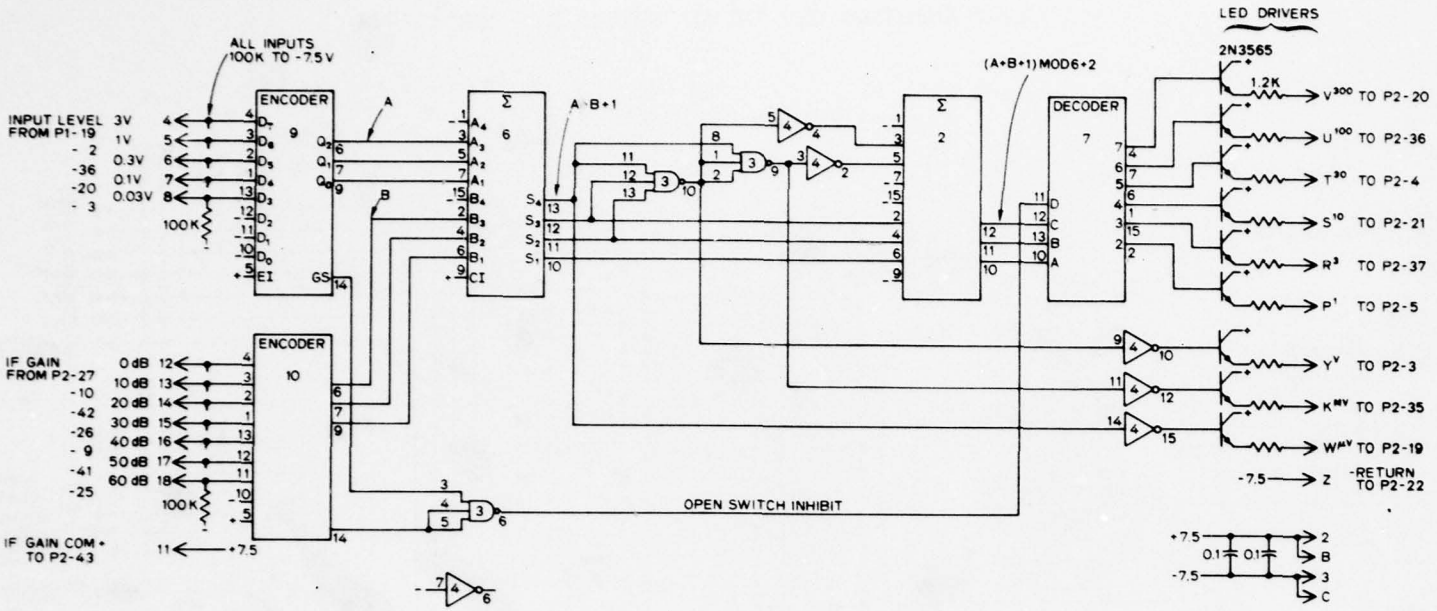



LOW PASS FILTER: $5^{th}$-ORDER 1.0 dB CHEBYSHEV, $f_{3dB}$ = 5436 Hz, -60 dB = 15 kHz

L36,L37: G-42213-40 POT CORE
434T #32, L = 80 mHy, Q(1 kHz) = 47

U5,U9 CD4013AE
U6 CD4066AE
U12 MC1741CP

Fig. A.18. CALIBRATION SOURCE (CARD 13).




| | |
|---|---|
| U2,U6 | CD4008BE |
| U3 | CD4023AE |
| U4 | CD4049AE |
| U7 | CD4028AE |
| U9,U10 | CD4532BE |

| INPUT LEVEL | A | IF GAIN | B |
|---|---|---|---|
| 3 V | 7 | 0 dB | 7 |
| 1 V | 6 | 10 dB | 6 |
| .3 V | 5 | 20 dB | 5 |
| .1 V | 4 | 30 dB | 4 |
| .03 V | 3 | 40 dB | 3 |
| | | 50 dB | 2 |
| | | 60 dB | 1 |

| A + B + 1 | $S_4$ $S_3$ $S_2$ $S_1$ | (A + B + 1) MOD 6 + 2 | OUTPUT |
|---|---|---|---|
| 15 | 1 1 1 1 | 0 1 1 = 3 | 3 V |
| 14 | 1 1 1 0 | 0 1 0 = 2 | 1 V |
| 13 | 1 1 0 1 | 1 1 1 = 7 | 300 mV |
| 12 | 1 1 0 0 | 1 1 0 = 6 | 100 mV |
| 11 | 1 0 1 1 | 1 0 1 = 5 | 30 mV |
| 10 | 1 0 1 0 | 1 0 0 = 4 | 10 mV |
| 9 | 1 0 0 1 | 0 1 1 = 3 | 3 mV |
| 8 | 1 0 0 0 | 0 1 0 = 2 | 1 mV |
| 7 | 0 1 1 1 | 1 1 1 = 7 | 300 μV |
| 6 | 0 1 1 0 | 1 1 0 = 6 | 100 μV |
| 5 | 0 1 0 1 | 1 0 1 = 5 | 30 μV |

Fig. A.19. VOLTAGE RANGE LOGIC (CARD 14).

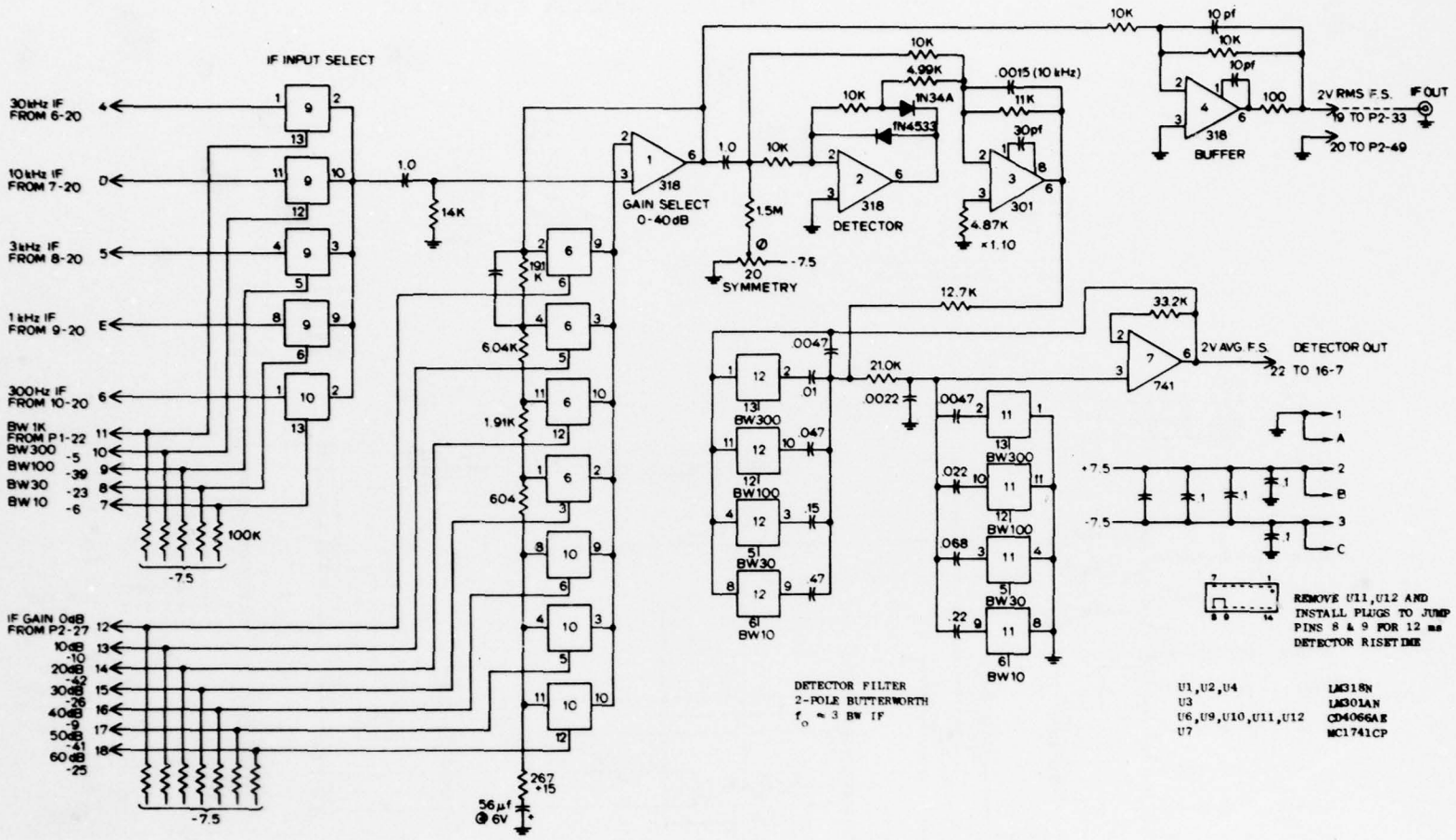



Fig. A.20. IF SELECT, GAIN, AND DETECTOR (CARD 15).

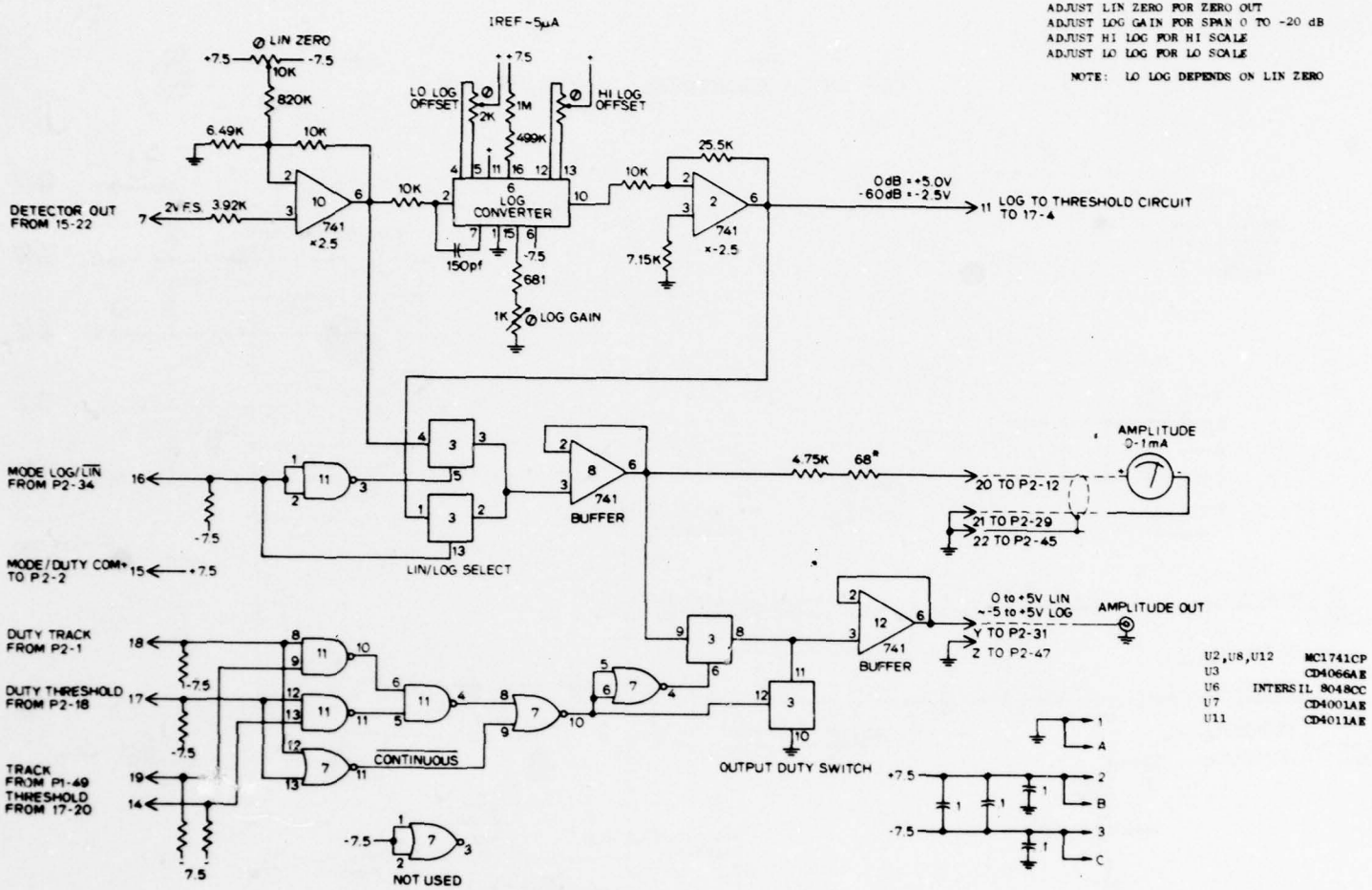



Fig. A.21. LOG AND OUTPUT (CARD 16).

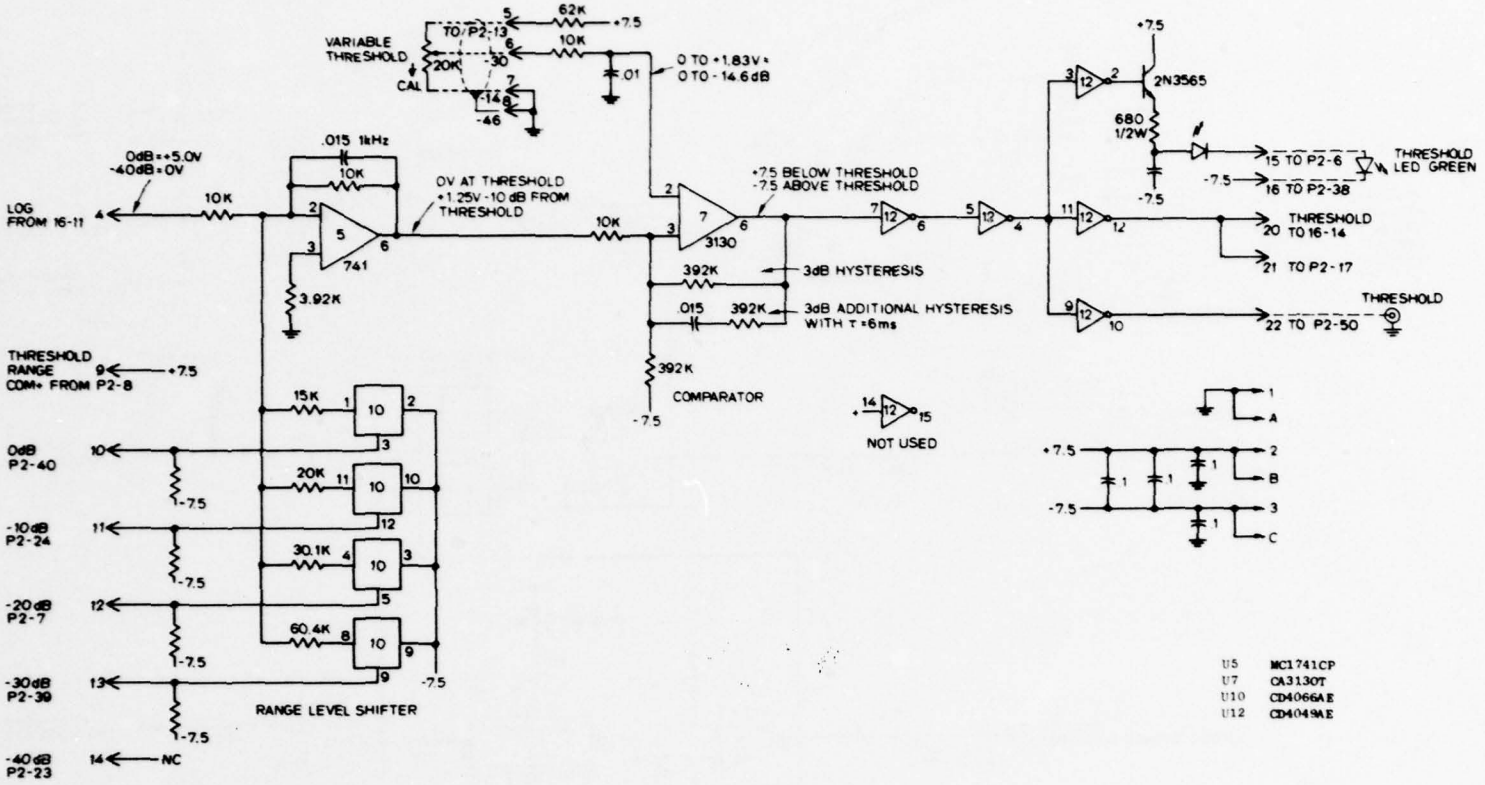
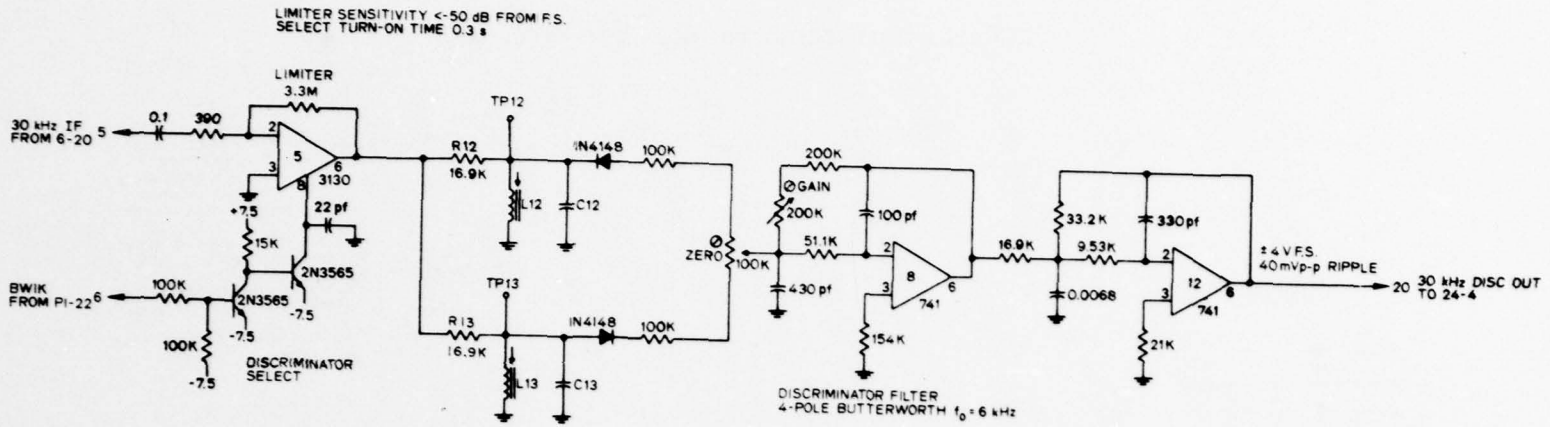


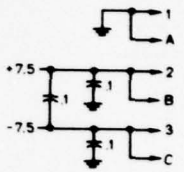

Fig. A.22. THRESHOLD (CARD 17).




$F_{12}$ = 31 kHz, Q = 18.98, BW = 1630 Hz
$F_{13}$ = 29 kHz, Q = 17.76, BW = 1630 Hz

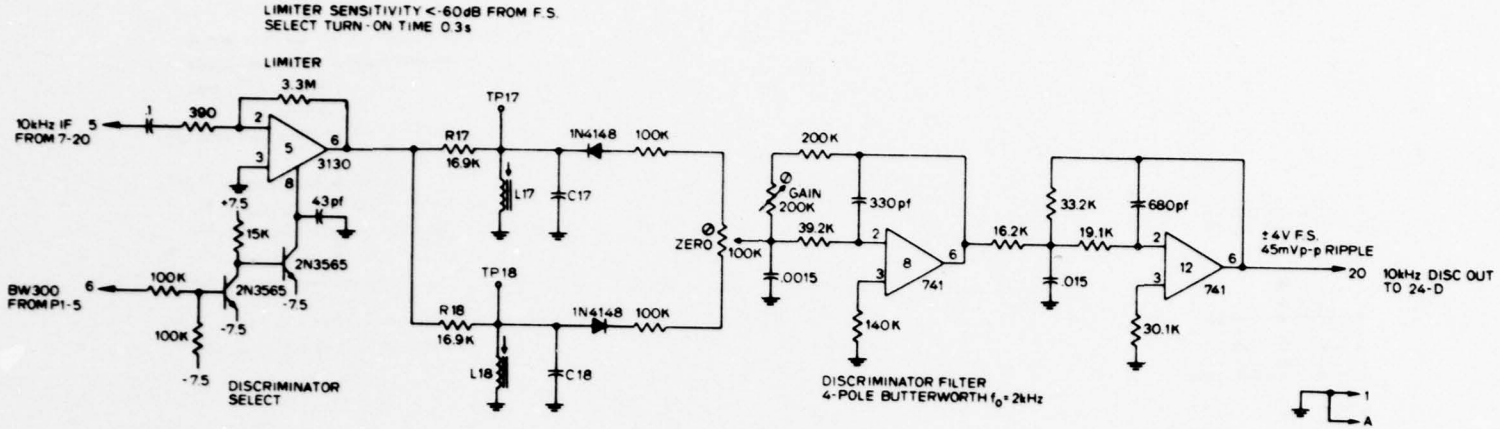
$C_{12}$,$C_{13}$ = 0.0068 NPO CERAMIC
$L_{12}$,$L_{13}$: G-42213-40 POT CORE
$L_{12}$: 96T #26, 3.8 mHy, Q(1 kHz) = 41, 0.55 Ω
$L_{13}$: 102T #26, 4.4 mHy, Q = 43, 0.6 Ω
$R_{12}$,$R_{13}$ SELECTED FOR PROPER Q's

ALIGNMENT WITH 5 kHz CAL:
PEAK $L_{12}$ @ 6000 Hz
PEAK $L_{13}$ @ 4000 Hz
ADJUST ZERO FOR 0 V OUT @ 5000 Hz
ADJUST GAIN FOR +/- 4 V OUT AT 4500/5500 Hz




U5 CA3130T
U8, U12 MC1741CP

Fig. A.23. 30 kHz DISCRIMINATOR (CARD 19).




F17 = 10.3 kHz, Q = 21.02, BW = 490 Hz
F18 = 9.7 kHz, Q = 19.80, BW = 490 Hz

C17,C18 = 0.022 μF NPO CERAMIC
L17,L18: G-42213-40 POT CORE
L17: 158T #28, 10.7 mHy, Q(1 kHz) = 46, 1.35
L18: 167T #28, 11.4 mHy, Q = 46, 1.45
R17,R18 SELECTED FOR PROPER Q's

ALIGNMENT WITH 5 kHz CAL:
PEAK L17 @ 5300 Hz
PEAK L18 @ 4700 Hz
ADJUST ZERO FOR 0 V OUT @ 5000 Hz
ADJUST GAIN FOR +/- 4 V OUT @ 4850/5150 Hz

Fig. A.24. 10 kHz DISCRIMINATOR (CARD 20).

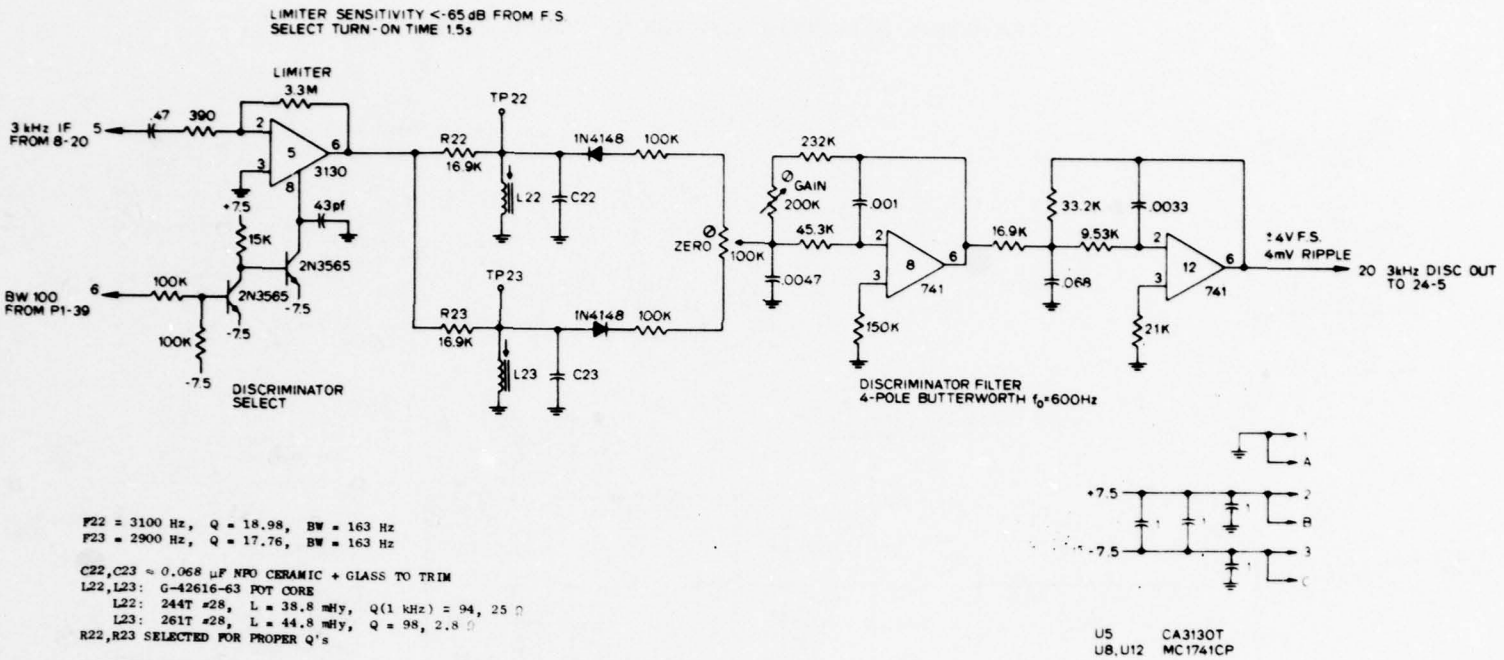
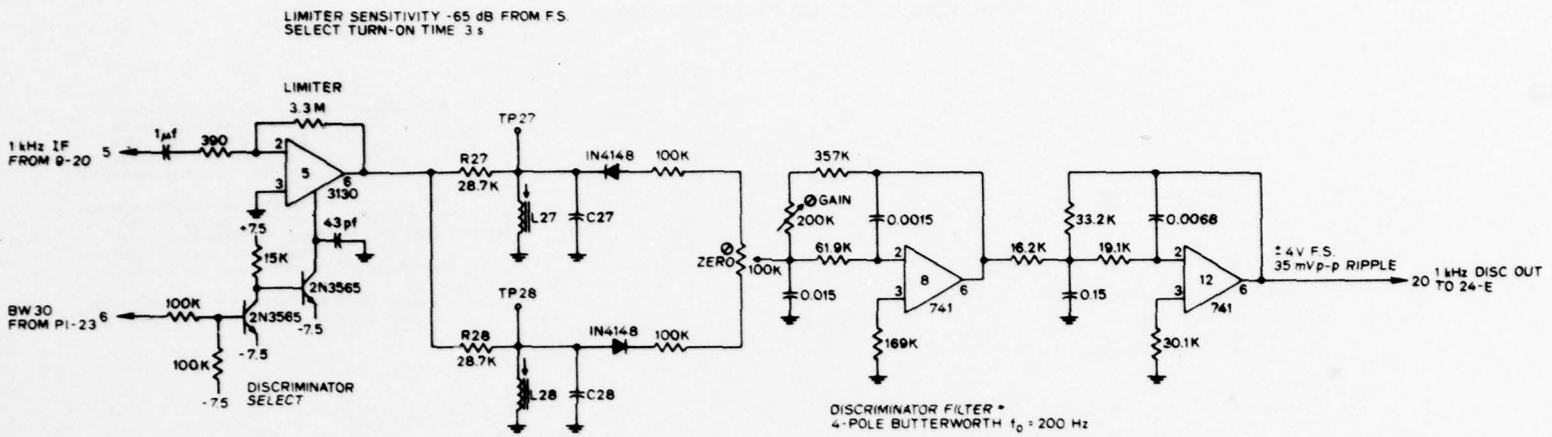


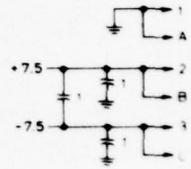

Fig. A.25. 3 kHz DISCRIMINATOR (CARD 21).




F27 = 1030 Hz, Q = 21.02, BW = 49 Hz
F28 = 970 Hz, Q = 19.80, BW = 49 Hz

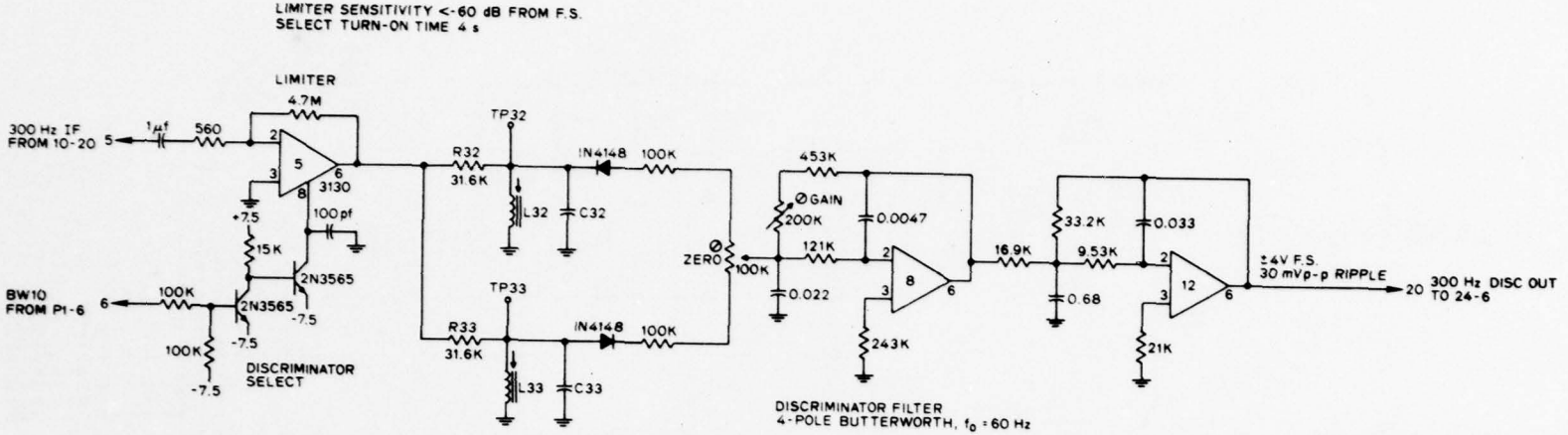
C27, C28 = 0.22 μF MYLAR
L27, L28: 0-42616-63 POT CORE
L27: 408T #30, L = 109 mHy, Q = 85, 7.4 k
L28: 435T #30, L = 122 mHy, Q = 90, 7.7 k
R27, R28 SELECTED FOR PROPER Q's

ALIGNMENT WITH 5 kHz CAL:
PEAK L27 @ 5030 Hz
PEAK L28 @ 4970 Hz
ADJUST ZERO FOR 0 V OUT @ 5000 Hz
ADJUST GAIN FOR +/- 4 V OUT @ 4985/5015 Hz




U5 CA3130T
U8, U12 MC1741CP

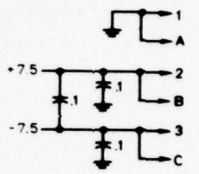
Fig. A.26. 1 kHz DISCRIMINATOR (CARD 22).




F32 = 310 Hz, Q = 18.98, BW = 16.3 Hz
F33 = 290 Hz, Q = 17.76, BW = 16.3 Hz

C32, C33 = 0.68 μF MYLAR
L22, L33: G-43019-X1 POT CORE
L32: 612T #30, L = 380 mHy, Q(1 kHz) = 190, 12.4 Ω
L33: 656T #30, L = 440 mHy, Q = 200, 13.6 Ω
R32, R33 SELECTED FOR PROPER Q's

ALIGNMENT WITH 5 kHz CAL:
PEAK L32 @ 5010 Hz
PEAK L33 @ 4990 Hz
ADJUST ZERO FOR 0 V OUT @ 5000 Hz
ADJUST GAIN FOR +/-4 V OUT @ 4995/5005 Hz




U5 CA3130T
U8, U12 MC1741CP

Fig. A.27. 300 kHz DISCRIMINATOR (CARD 23).

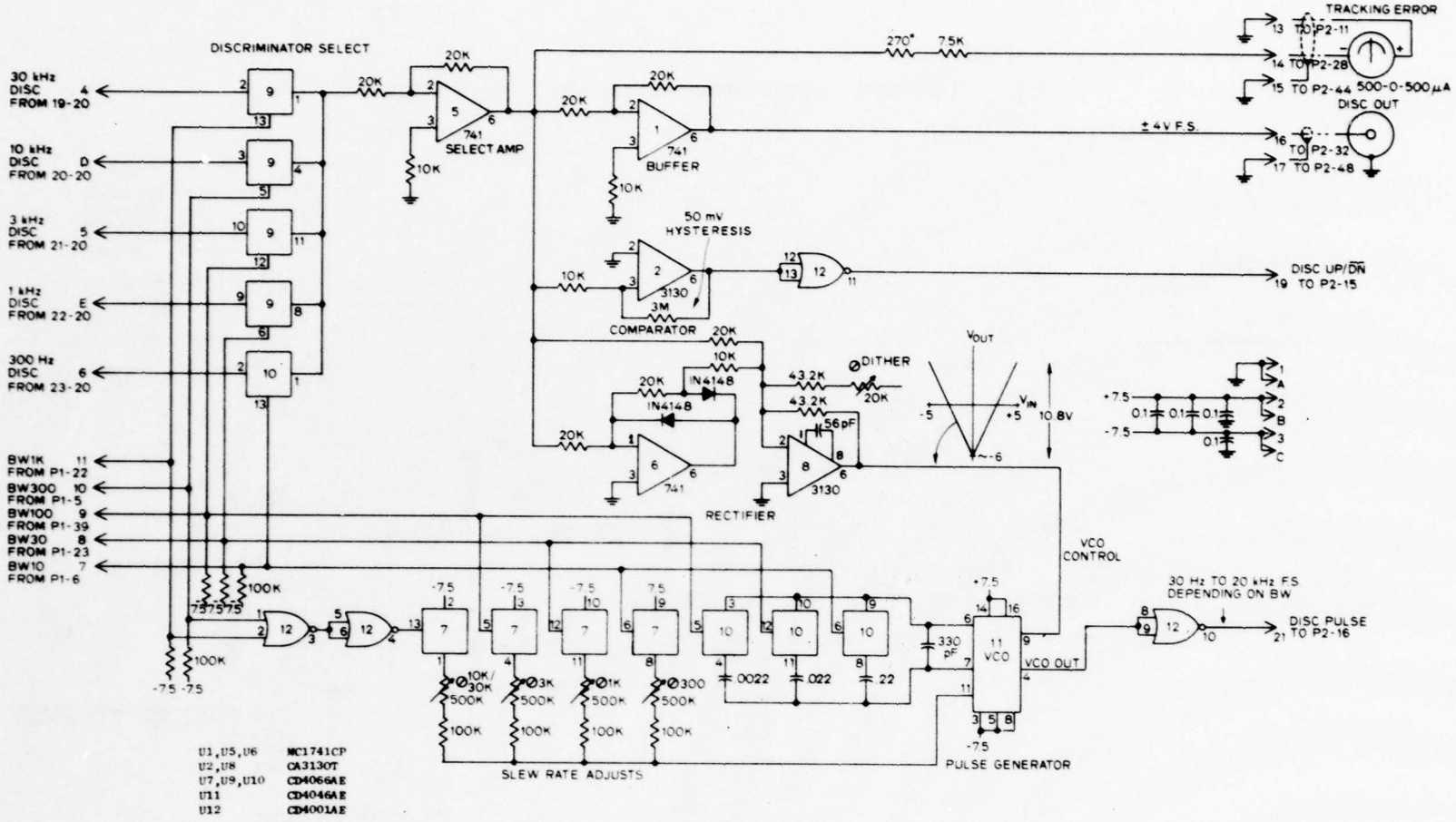



Fig. A.28. DISCRIMINATOR SELECT AND SLEW (CARD 24).

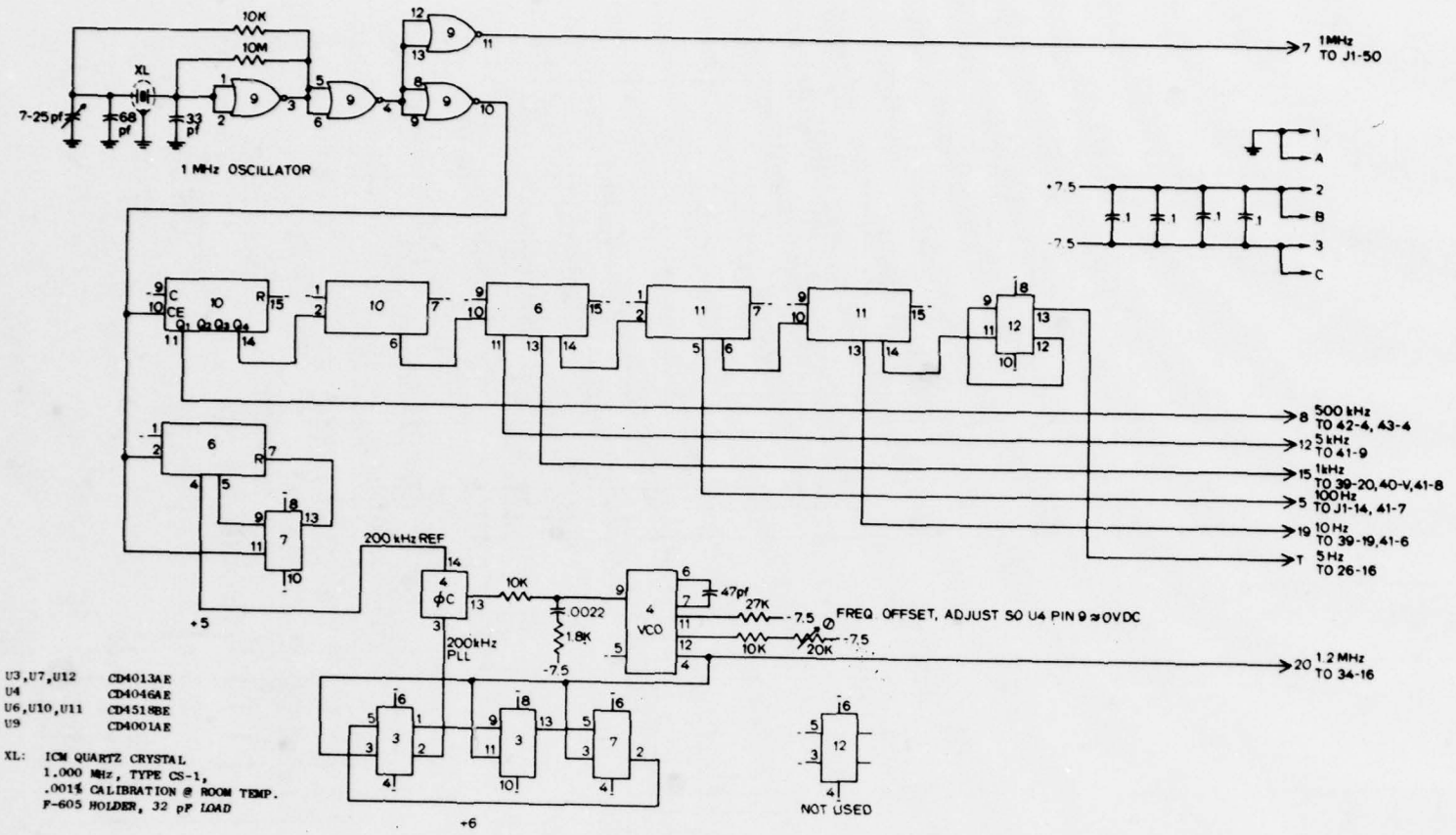



Fig. A.29. TIME BASE (CARD 25).

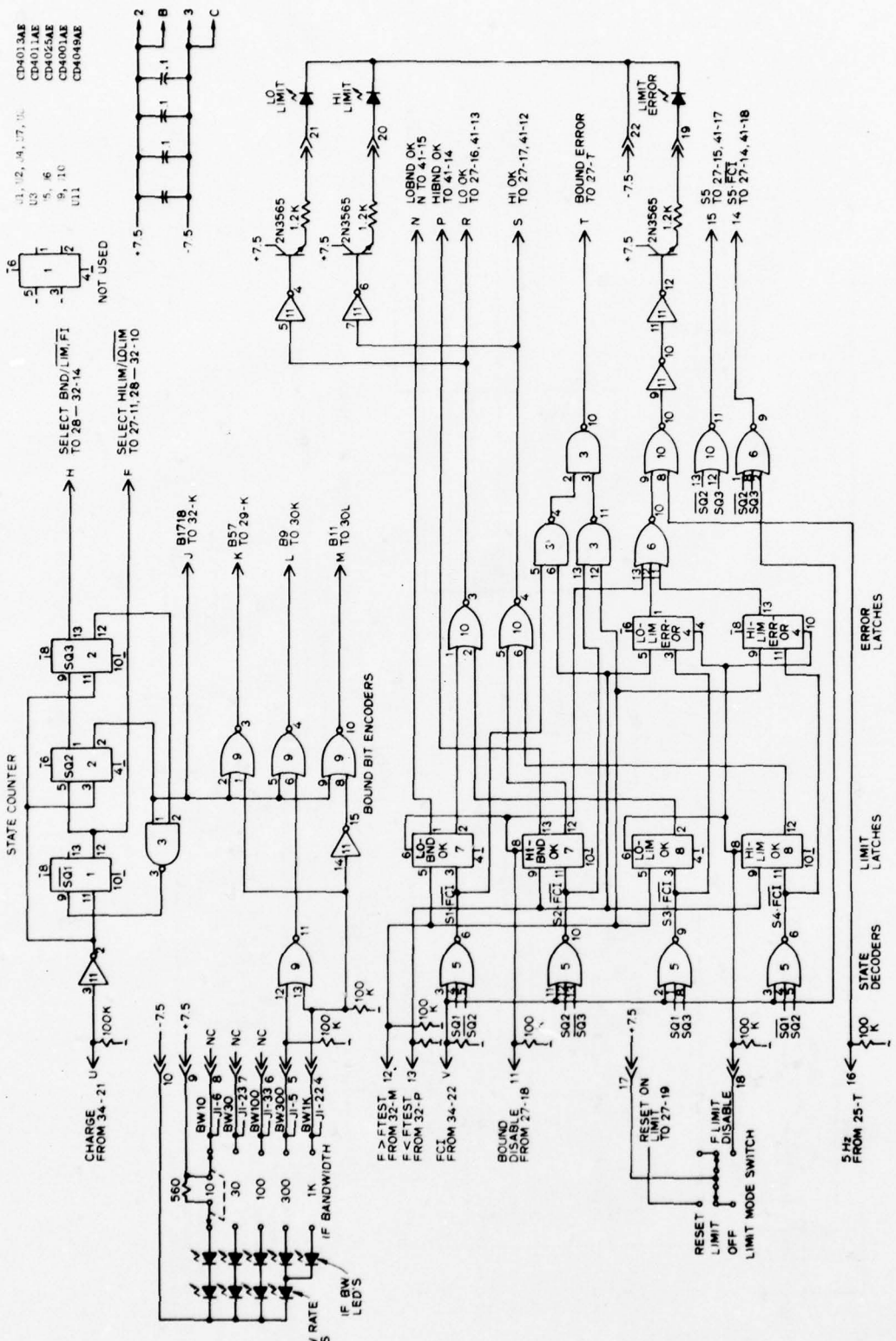



Fig. A.30. F LIMIT CONTROL (CARD 26).

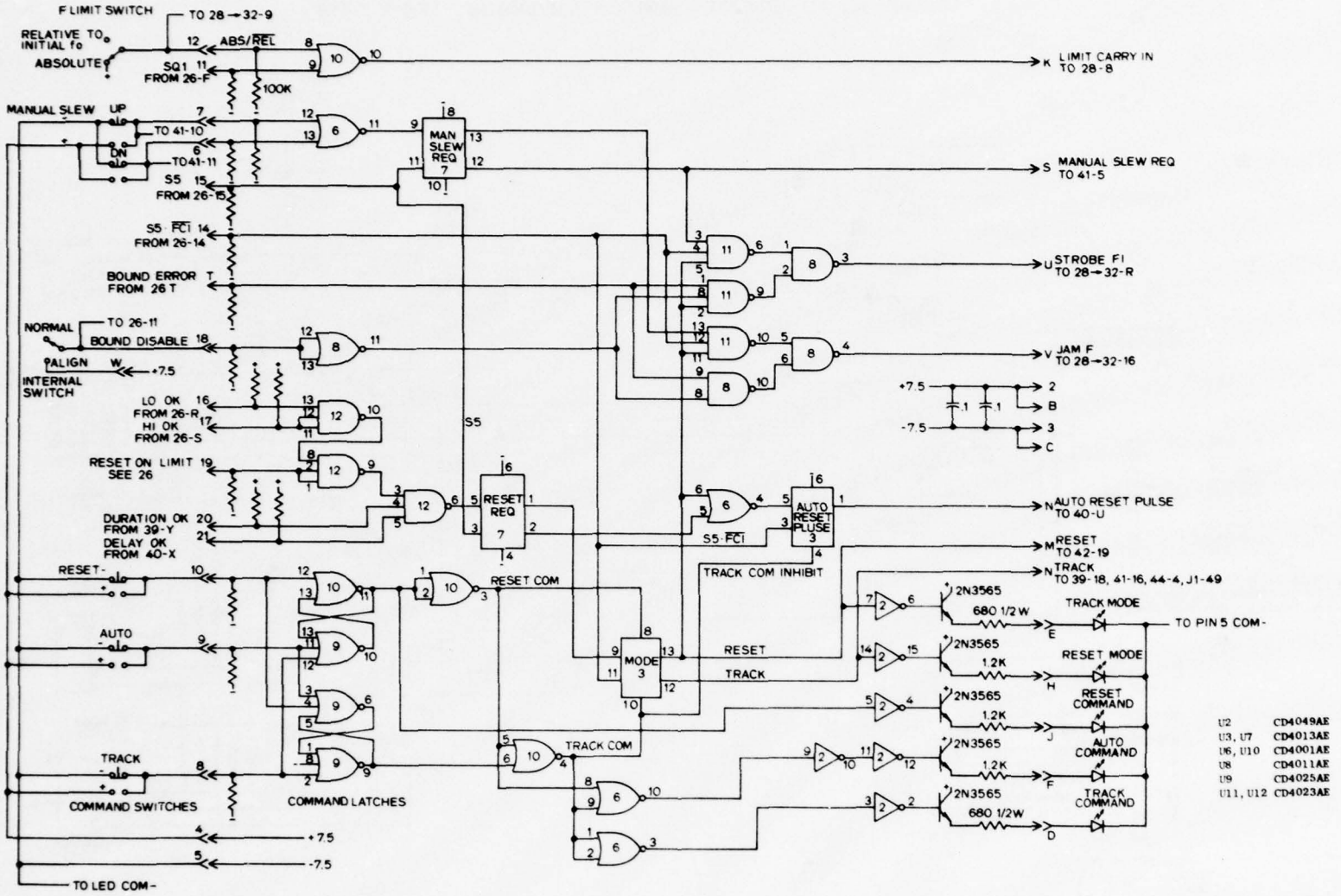



Fig. A.31. TRACK CONTROL (CARD 27).

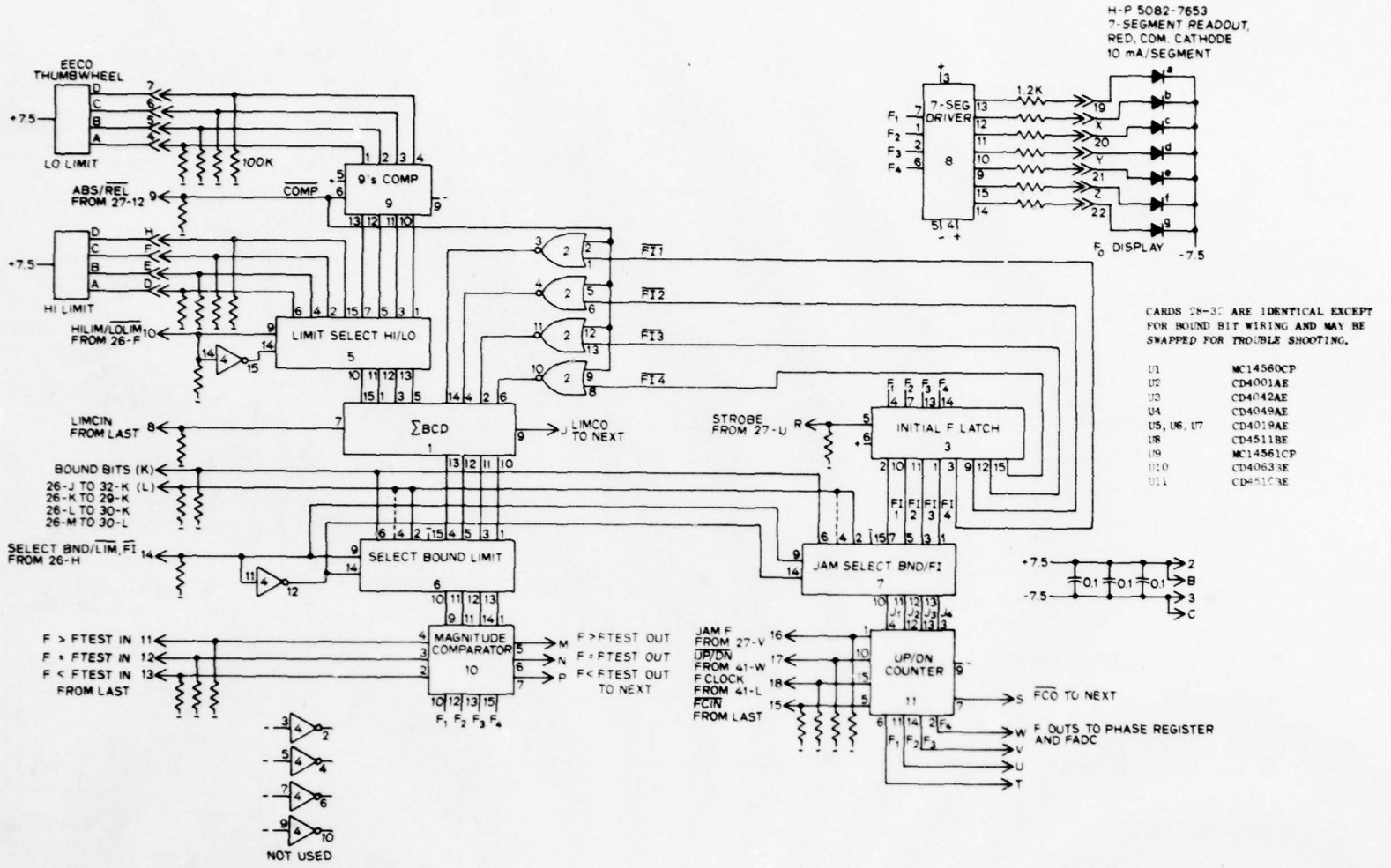



Fig. A.32. FREQUENCY REGISTER DECADE (CARDS 28-32).

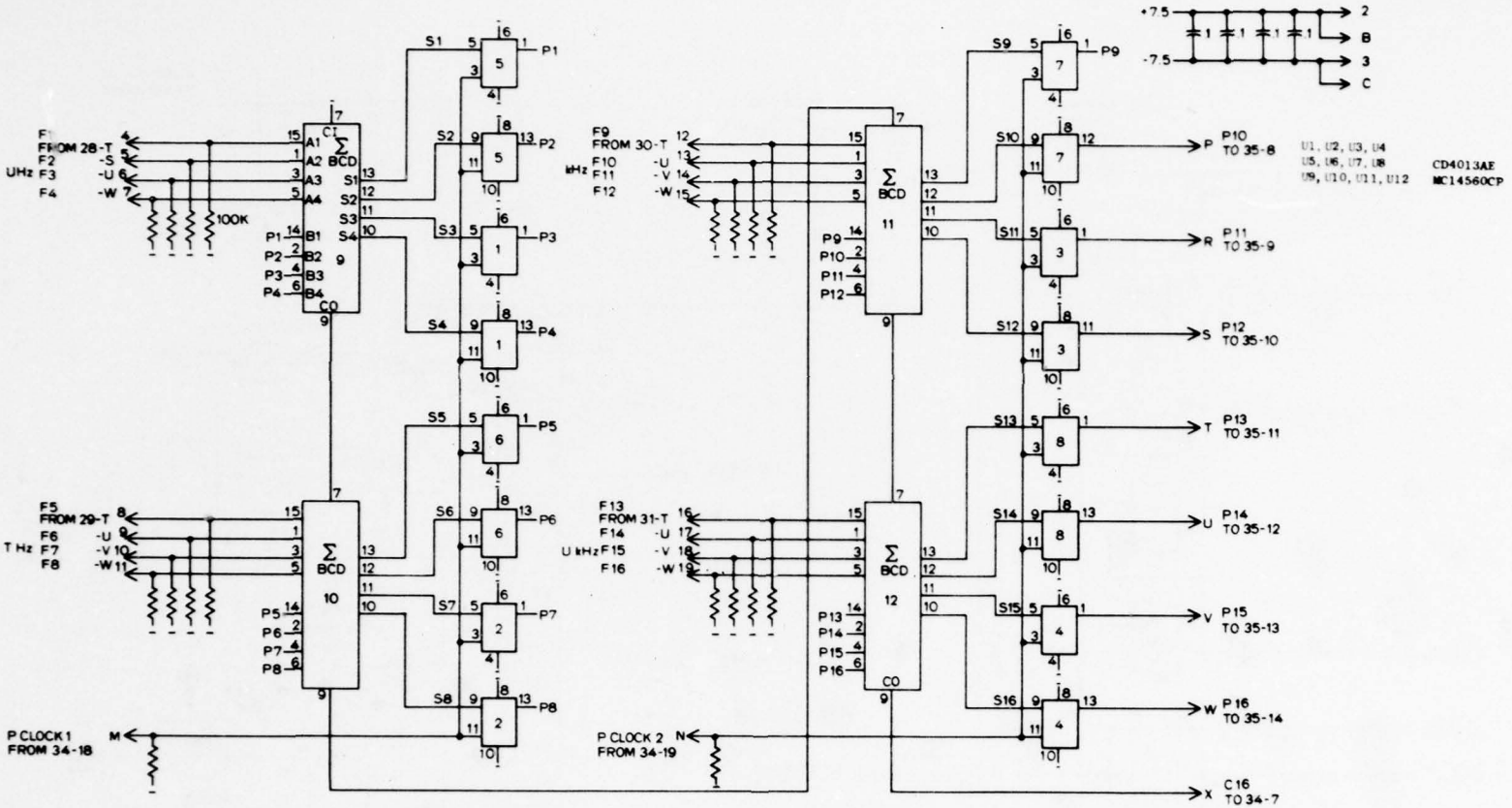
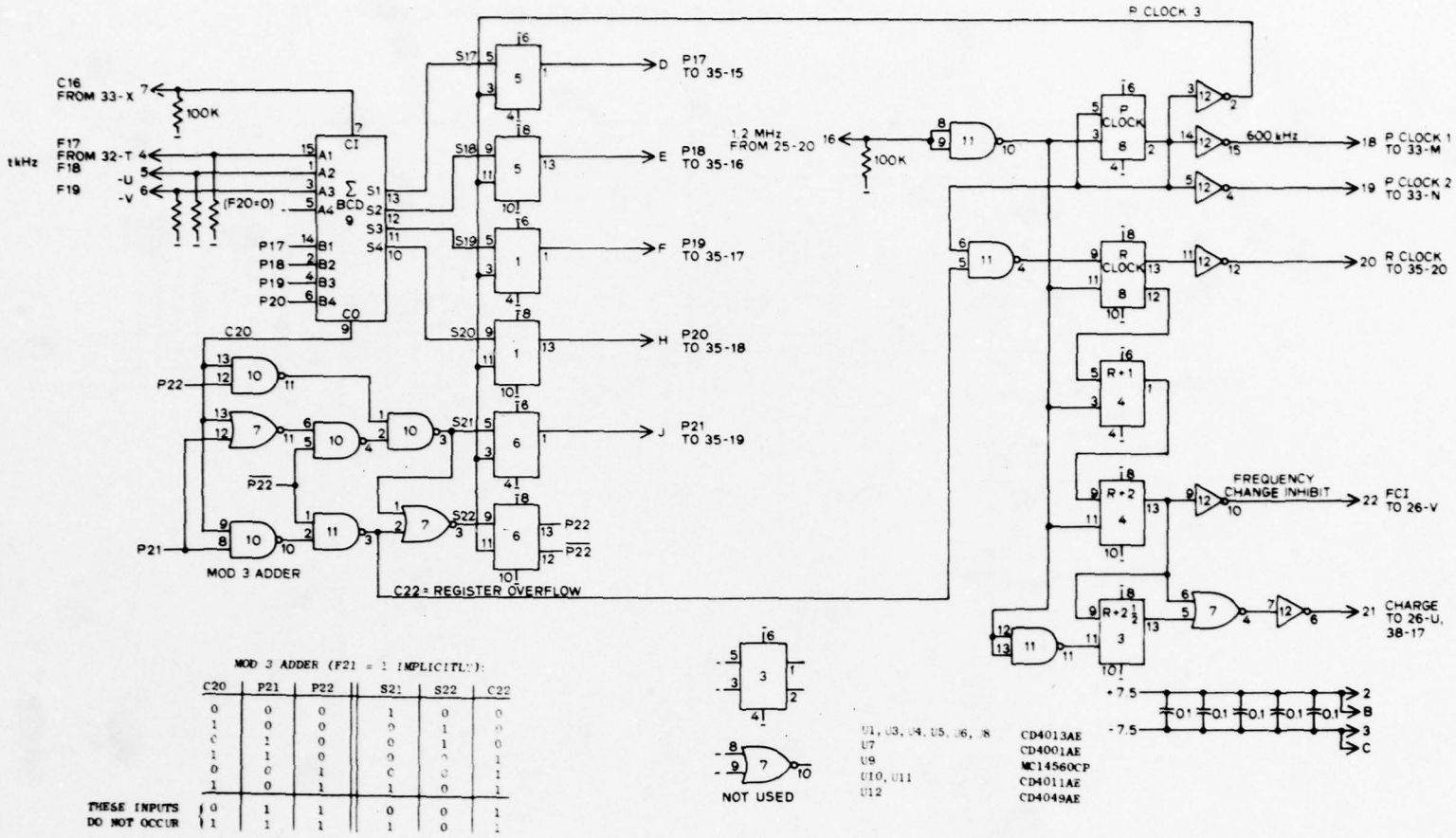



Fig. A.33. PHASE REGISTER AND ADDER, BITS P1-P16 (CARD 33).




MOD 3 ADDER (F21 = 1 IMPLICITLY):

| C20 | P21 | P22 | S21 | S22 | C22 |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| THESE INPUTS DO NOT OCCUR | 0 | 1 | 1 | 0 | 0 | 1 |
| | 1 | 1 | 1 | 1 | 0 | 1 |

Fig. A.34. PHASE REGISTER BITS P17-P22 AND CLOCK (CARD 34).

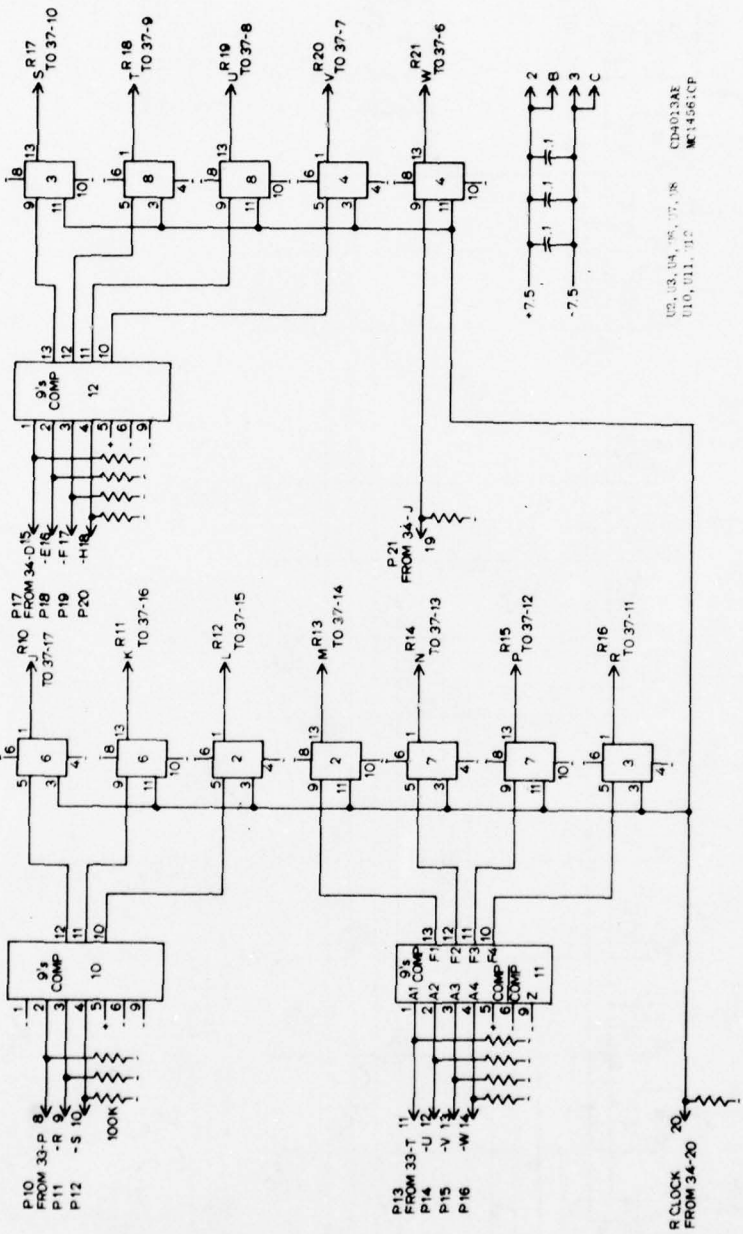
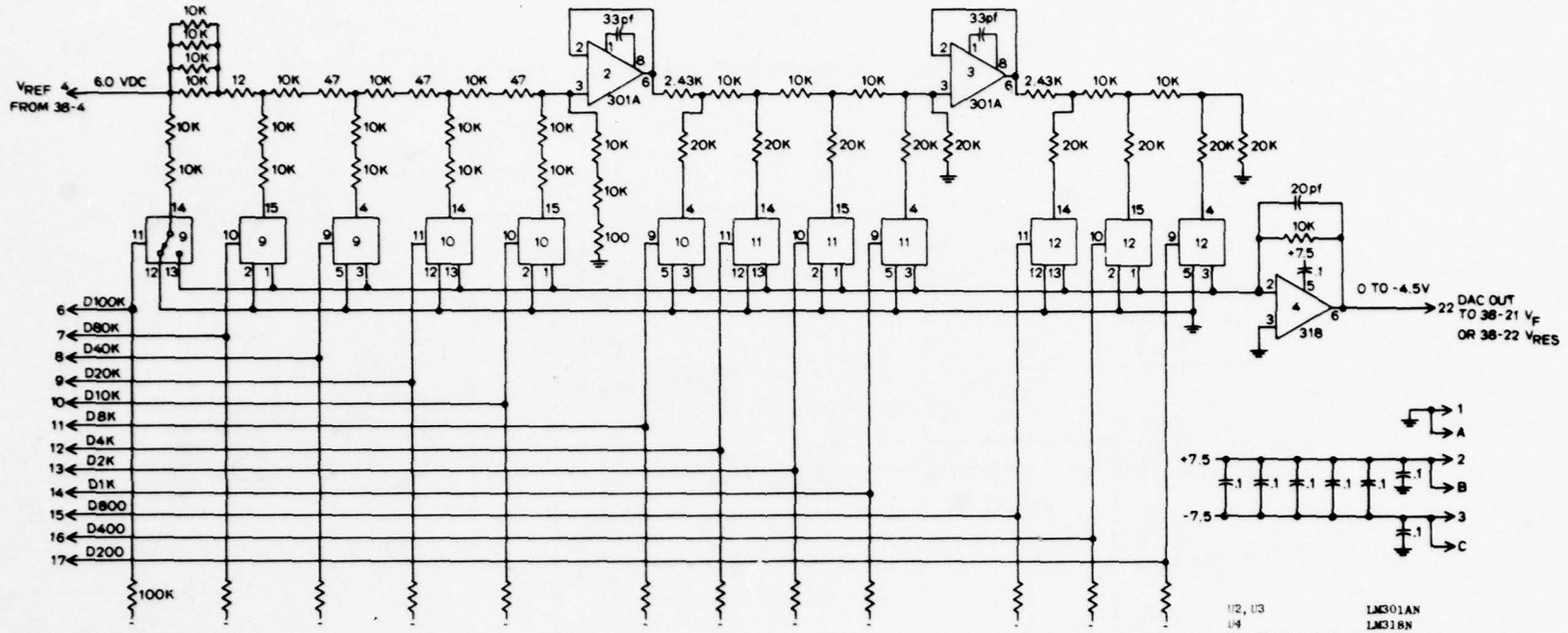



Fig. A.35. PHASE RESIDUE REGISTER (CARD 35).




| CARD 36 FDAC INPUT | | | CARD 37 RDAC INPUT | | |
|---|---|---|---|---|---|
| 36-6 | FROM | +7.5(F21=1) | 37-6 | FROM | 37-W, R21 |
| 7 | | 32-W, F20(=0) | 7 | | 37-V, R20 |
| 8 | | 32-V, F19 | 8 | | 37-U, R19 |
| 9 | | 32-U, F18 | 9 | | 37-T, R18 |
| 10 | | 32-T, F17 | 10 | | 37-S, R17 |
| 11 | | 31-W, F16 | 11 | | 37-R, R16 |
| 12 | | 31-V, F15 | 12 | | 37-P, R15 |
| 13 | | 31-U, F14 | 13 | | 37-N, R14 |
| 14 | | 31-T, F13 | 14 | | 37-M, R13 |
| 15 | | 30-W, F12 | 15 | | 37-L, R12 |
| 16 | | 30-V, F11 | 16 | | 37-K, R11 |
| 17 | | 30-U, F10 | 17 | | 37-J, R10 |

| | |
|---|---|
| U2, U3 | LM301AN |
| U4 | LM318N |
| U9, U10, U11, U12 | CD4053BE |

ALL 10K AND 20K RESISTORS 1%, SELECTED FROM MATCHED LOT. CARDS 36 AND 37 ARE IDENTICAL AND MAY BE INTERCHANGED FOR TEST PURPOSES.

Fig. A.36. FREQUENCY D/A CONVERTER AND RESIDUE D/A CONVERTER (CARDS 36,37).

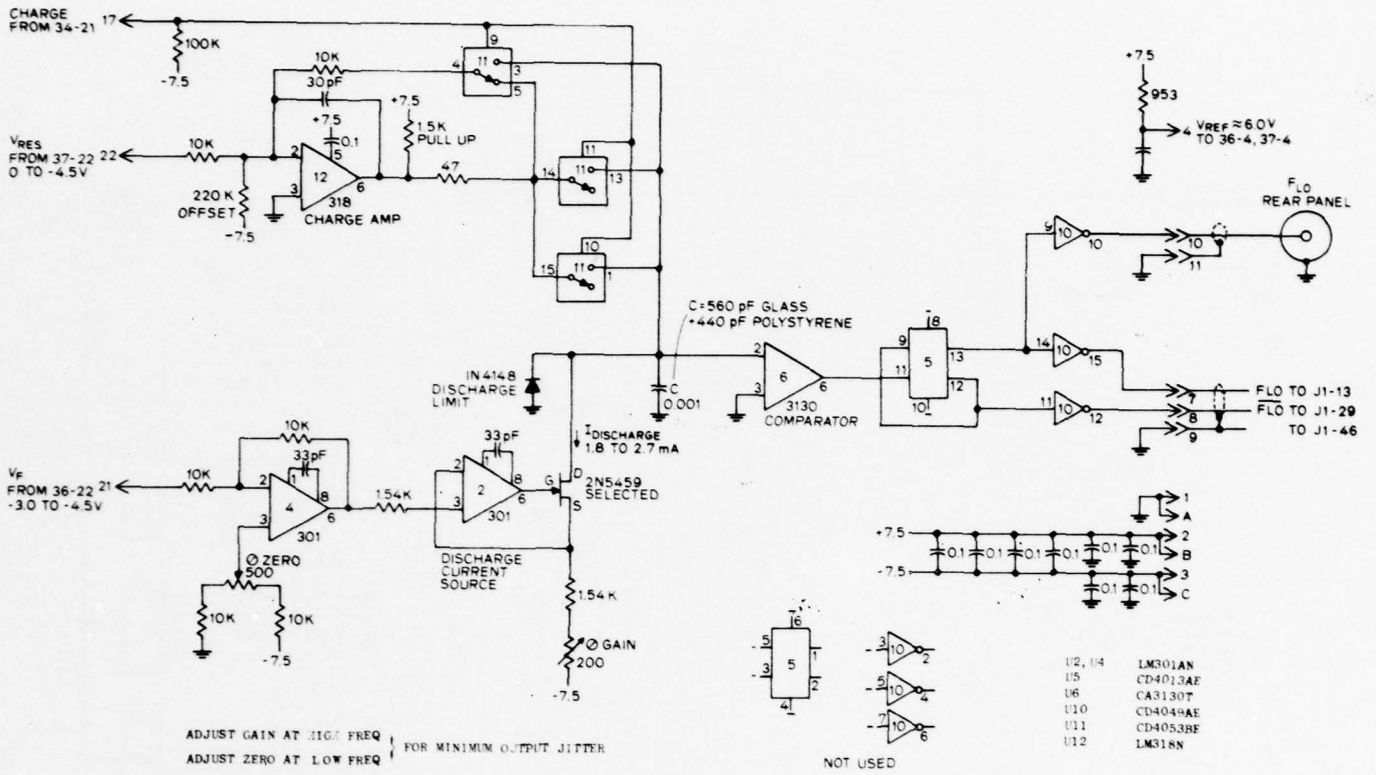



Fig. A.37. SYNTHESIZER OUTPUT (CARD 38).

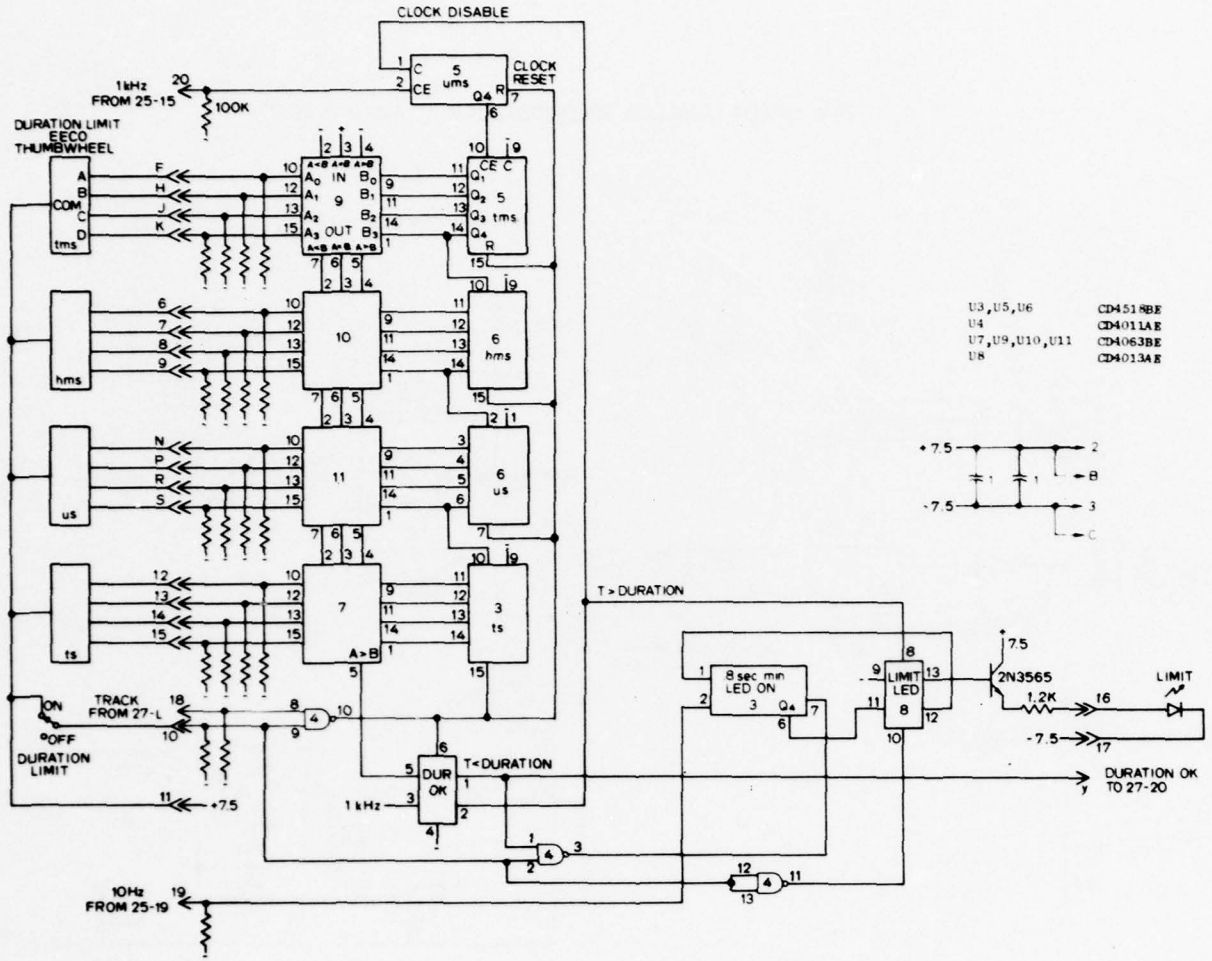
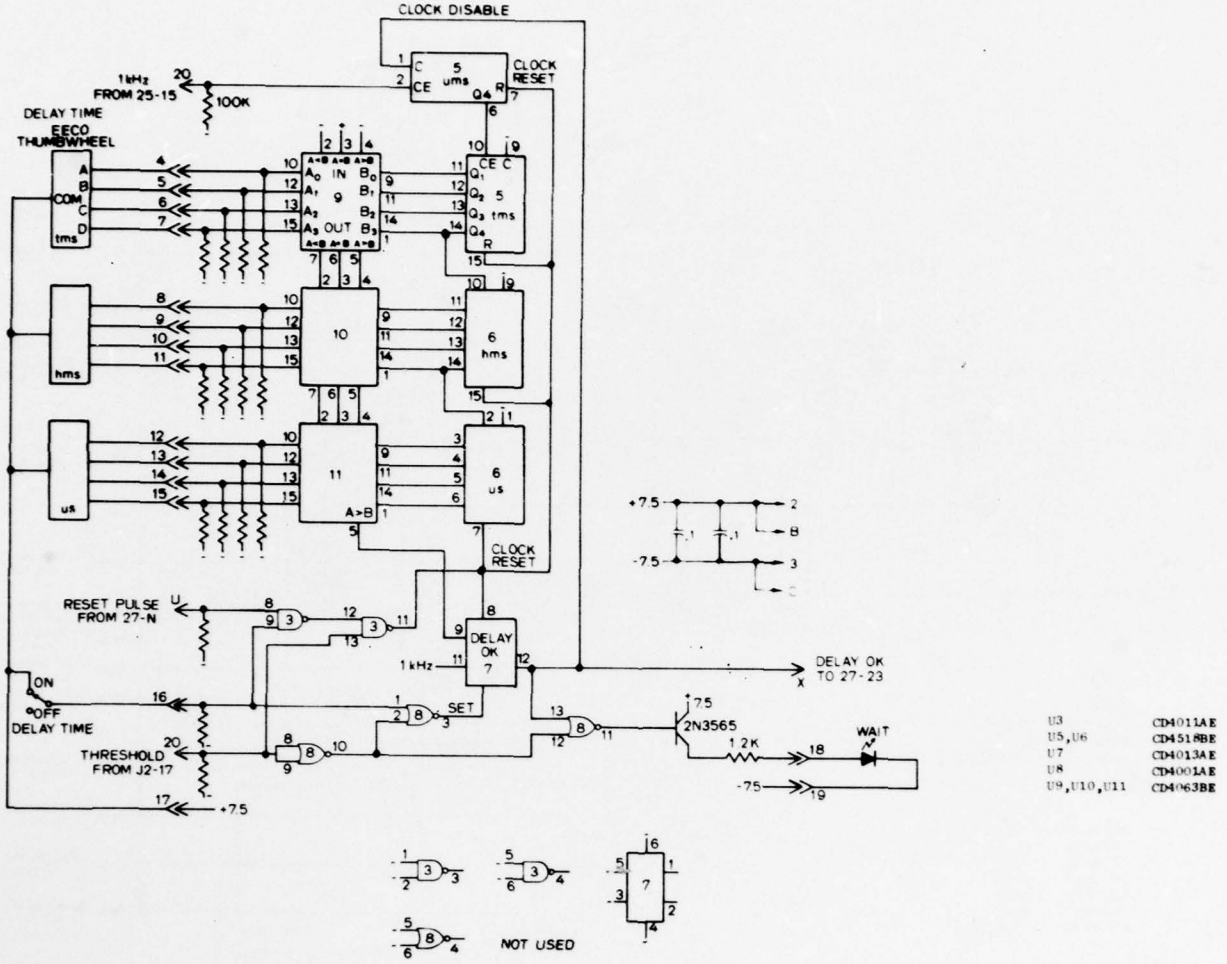



Fig. A.38. TRACK DURATION LIMIT (CARD 39).




| | |
|---|---|
| U3 | CD4011AE |
| U5,U6 | CD4518BE |
| U7 | CD4013AE |
| U8 | CD4001AE |
| U9,U10,U11 | CD4063BE |

Fig. A.39. TRACK DELAY CONTROL (CARD 40).

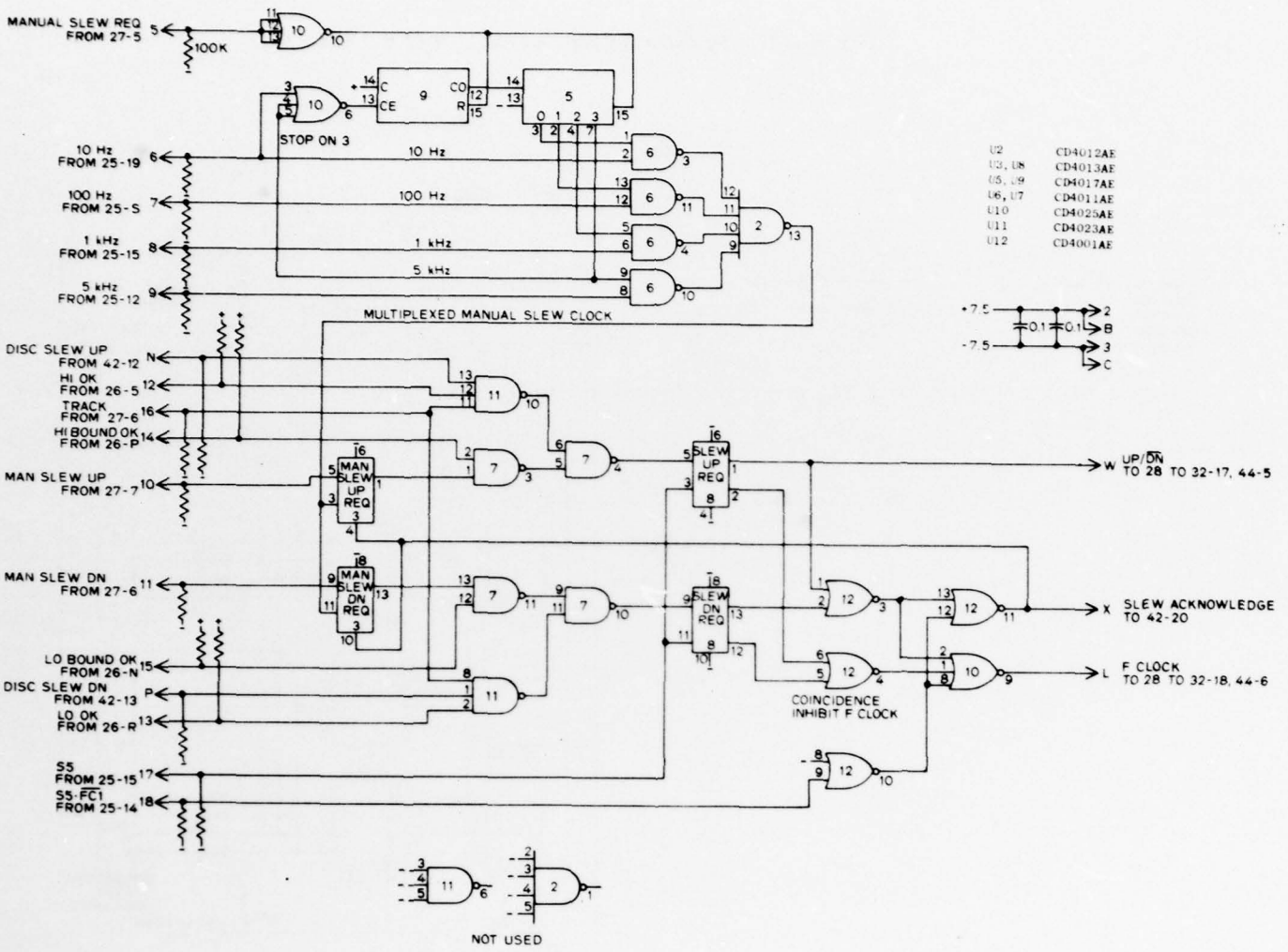



Fig. A.40. SLEW CONTROL (CARD 41).

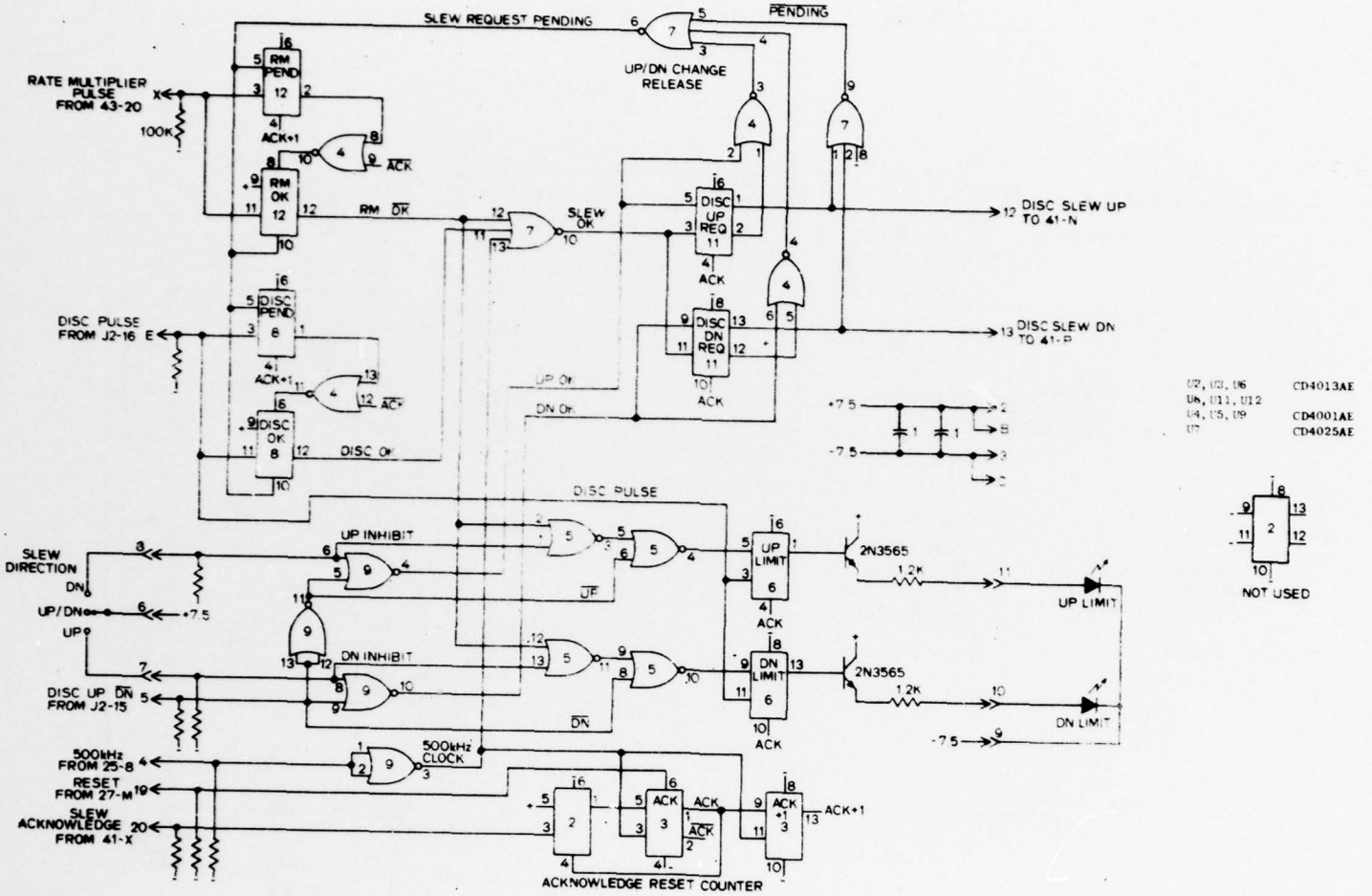



Fig. A.41. SLEW RATE LIMIT (CARD 42).

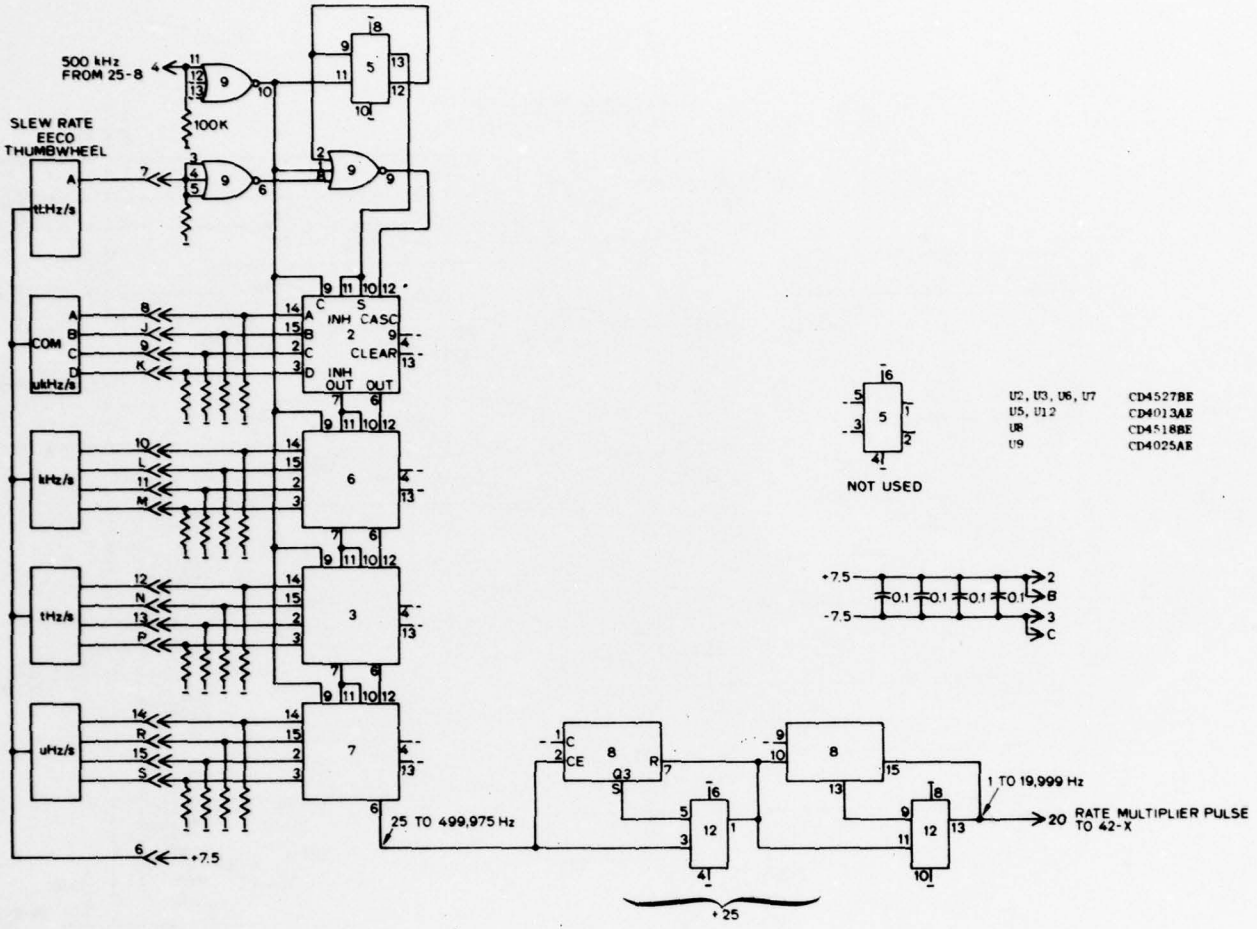



Fig. A.42. SLEW RATE MULTIPLIER (CARD 43).

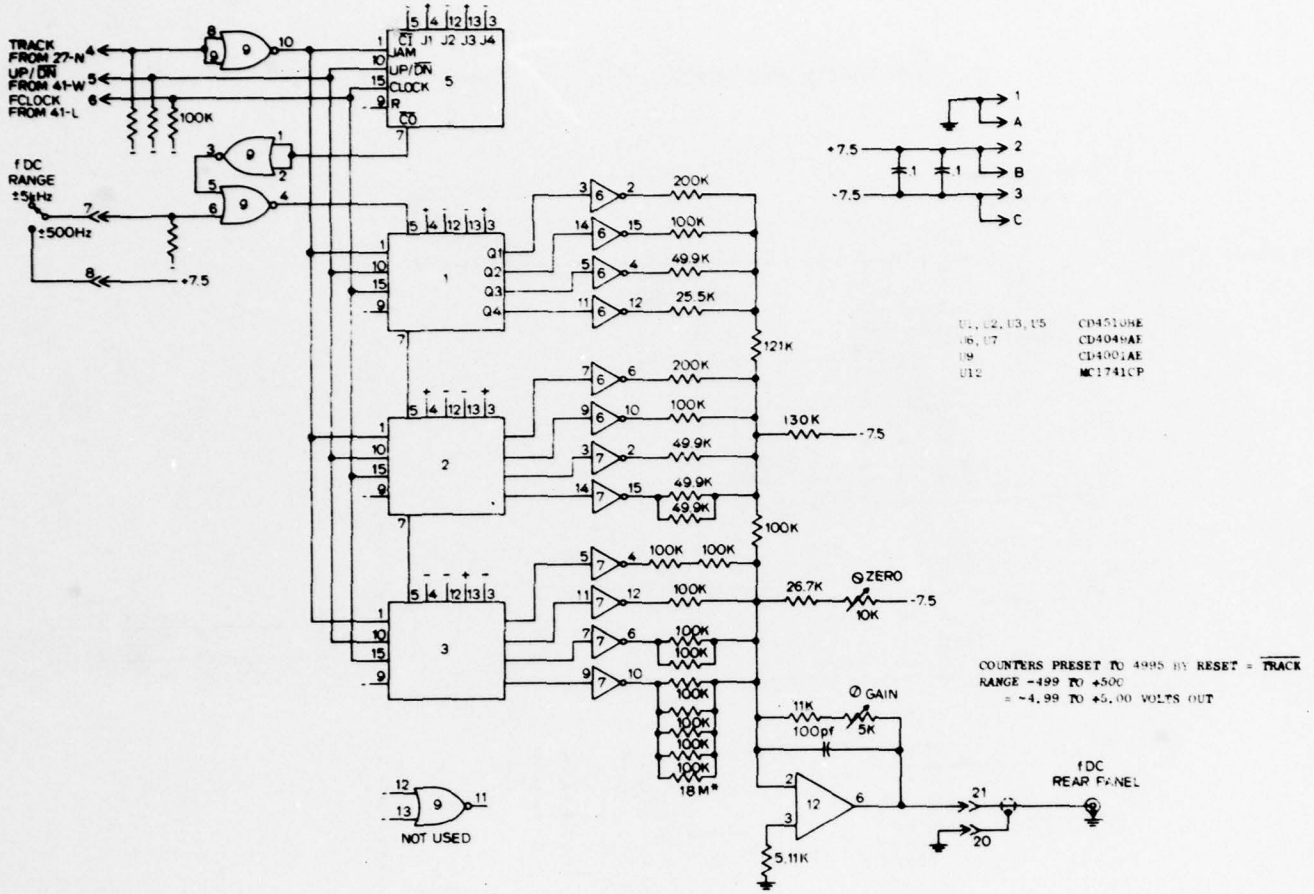



Fig. A.43. $f_{DC}$ COUNTER AND D/A CONVERTER (CARD 44).

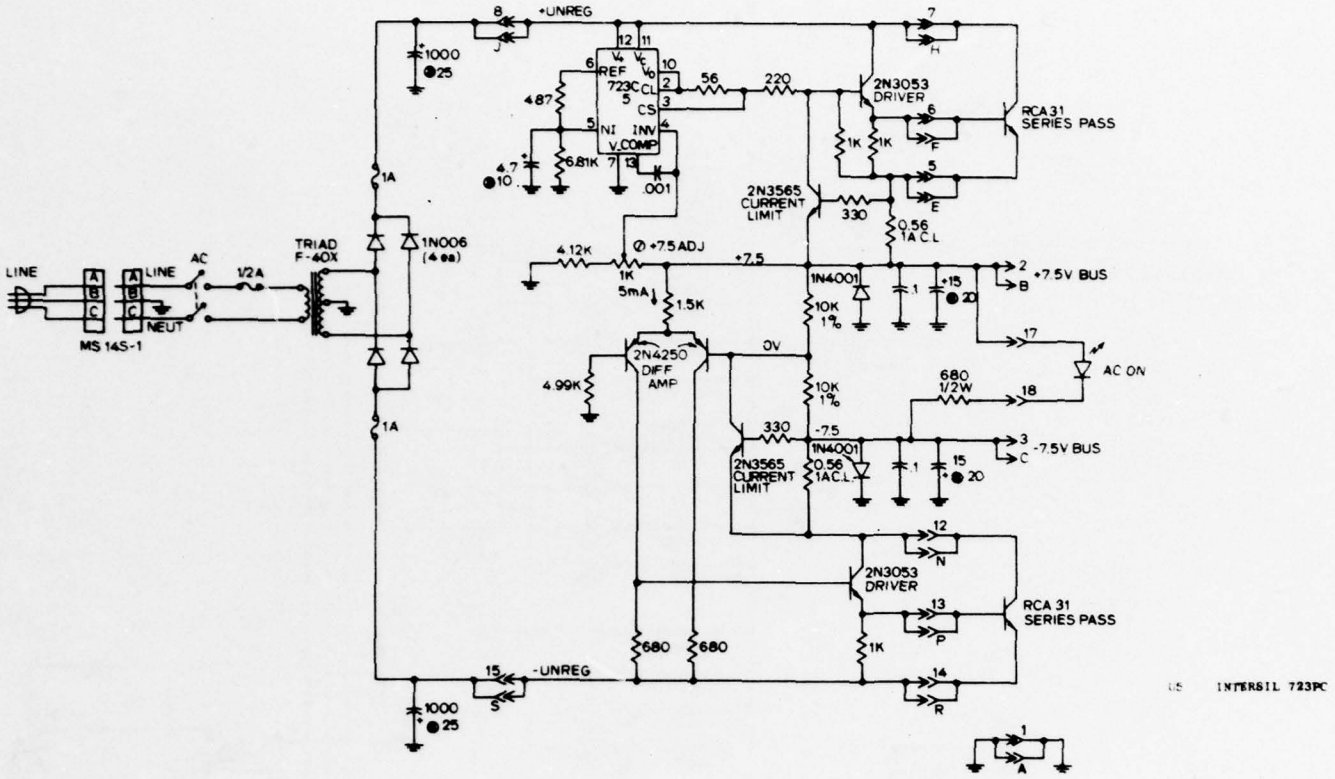



Fig. A.44. ± 7.5 V REGULATOR (CARD 46).

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This manual describes an audio-frequency tracking voltmeter developed by the VLF Radioscience Group at Stanford University for measuring the amplitudes of individual components of complex signals. It is intended as a guide to the use and maintenance of the instrument and includes operating instructions, alignment procedures, and detailed circuit descriptions.

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