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DEVELOPMENT REPORT FOR HIGH-RELIABILITY, LOW-COST INTEGRATED CI--ETC(U)
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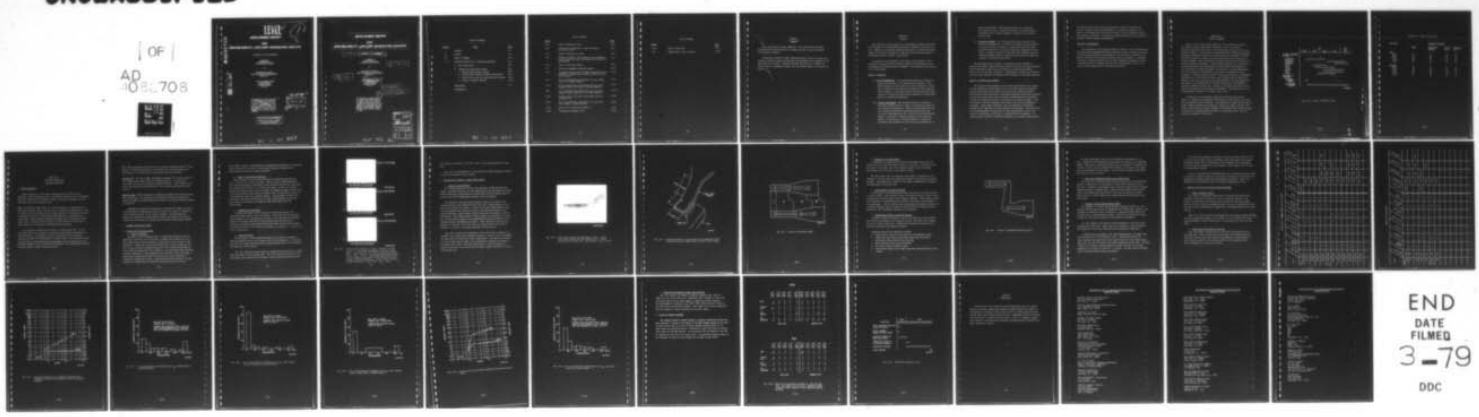

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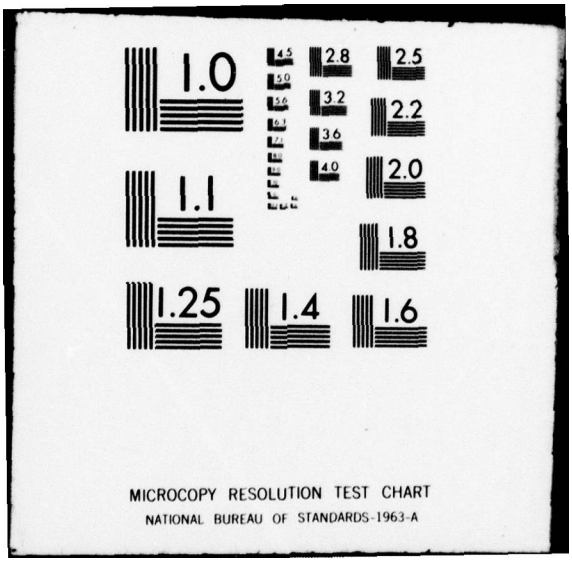
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LEVEL II

DEVELOPMENT REPORT

FOR

HIGH-RELIABILITY, LOW-COST INTEGRATED CIRCUITS

3 NOVEMBER 1977 TO 3 SEPTEMBER 1978

Prepared By
RCA Solid State Divison
Route 202, Somerville, N.J. 08876

For

DEPARTMENT OF THE NAVY
NAVAL ELECTRONICS SYSTEMS COMMAND
Washington, D.C.

Contract No. N00039-76-C-0240
Project No. 62762N
Subproject No. XF54586
Task No. 002

(6)

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DEPARTMENT OF THE NAVY
NAVAL ELECTRONICS SYSTEMS COMMAND
Washington, D.C.

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SECTION I

ABSTRACT

Wafer fabrication has been completed. The control units (aluminum metallized DIC and DIP devices and trimetal devices in open DIC packages are 90-percent complete.

Thermal-shock testing of HRLC (high-reliability, low-cost) product has defined a beam-tape design problem which has necessitated the redesign of the beam tapes on all types. Life-test matrices have been run on CD4012 and CA741 to gain a preliminary insight into the failure modes to be expected in Phase III.

SECTION II

PURPOSE

The objective of this program is to investigate alternate approaches to MIL-M-38510 for achieving high reliability integrated circuits at low cost. Emphasis is on adapting existing technology to industry mainstream products to achieve semiconductor reliability which will meet military requirements without a severe cost penalty.

The approach to achievement of the goals of this program is the integration and application of existing sealed-chip integrated-circuit processing with automated plastic packaging. The program is being carried out in three phases.

Phase I - Completed

(a) Process Feasibility - The required photomasks were generated using existing masks to the maximum extent possible. Then, small quantities of each device type were fabricated to assure that the masks and processes were available for the production runs of Phase II. Also, each device type was fabricated using a matrix of carefully varied process parameters to assess their impact on yields and reliability.

(b) Process Development - The processes required to fabricate the eight integrated-circuit types to be produced in Phase II were defined and documented. Silicon nitride passivation and the titanium-platinum-gold metallization system were used to achieve chip hermeticity and a corrosion-free metallization system. In addition, a silicon nitride overcoat layer was applied for protection of the metallization. A series of experiments was completed at each critical processing step to

assure repeatability. Real-time indicators and accelerated life tests were used to assess the effects of process changes on reliability and to measure progress in achieving the required failure rate.

(c) Automated Assembly - The technology being used in Phase II was defined and documented. The effect of assembly process parameters on cost and yield was assessed. Bonding tapes and lead-frames compatible with each of the device types were designed and fabricated. A number of devices of each type were assembled using the automated assembly system. Reliability was monitored continually by means of accelerated life tests.

The photomasks, wafer process, and assembly process required to fabricate the eight integrated-circuit types in the low-cost high-reliability device-fabrication phase have been defined and documented and sample devices of each type were fabricated. Additionally, preliminary reliability data have been generated to demonstrate the soundness of the chosen approach.

Phase II - Fabrication (Current)

The low-cost high-reliability device fabrication phase of the program involves significant quantities of each of the eight selected integrated-circuit types fabricated according to the processes defined in Phase I. Both silicon nitride passivated, titanium-platinum-gold metallized integrated circuits and conventional silicon dioxide, aluminum-metallized integrated circuits are being constructed in both plastic and ceramic packages. This will permit a detailed comparison to be made of the new and conventional processes. During these production runs, any significant differences between the two processes are being defined and documented. The utilization of existing equipment and mask sets is being demonstrated, and the cost impact of converting to this type of processing will be estimated. In-process quality controls, real-time indicators, and parameter distributions

at wafer probe and final test are being used to monitor the production run and to assure process reproducibility. All devices produced in this phase of the program will be utilized in Phase III for reliability testing and delivery to the Navy. Finally, the testing facilities for the Phase III program are being defined and assembled.

Phase III - Reliability

The reliability of the devices produced in Phase II will be demonstrated. The conventional aluminum-metallized integrated cirucits, packaged and tested to military high-reliability requirements, will be used as a baseline from which to appraise the new process developed under the program. In addition, the level of testing required over and above commercial screening to assure a reliable product for military end use will be determined, and the cost impact of this testing will be analyzed and verified.

SECTION III

PHASE II PROGRAM

Phase II, the low-cost high-reliability device-fabrication phase of the program, involves significant quantities of each of the eight selected integrated-circuit types to be fabricated according to the process defined in Phase I. Both silicon nitride passivated, titanium-platinum-gold metallized integrated circuits and conventional silicon dioxide, aluminum-metallized integrated circuits are being constructed in both plastic and ceramic packages. This plan permits a detailed comparison to be made of the new and conventional processes. During these production runs, significant differences between the two processes are being defined and documented. The utilization of existing equipment and mask sets is being demonstrated, and the cost impact of converting to this type of processing is being estimated. In-process quality controls, real-time indicators, and parameter distributions at wafer probe and final test are being used to monitor the production run and to assure process reproducibility. Devices produced in this phase of the program will be utilized in Phase III for reliability testing and delivery to the Navy. Finally, the testing facilities for the Phase III program are being defined and assembled. The milestone chart for the completion of Phase II is shown in Fig. III-1.

In addition to initiating the long-term 125°C life tests during Phase II, a program of accelerated life testing for two circuits, the CA741 and the CD4012B has been initiated. This program will verify the reliability goals, compare encapsulation techniques, compare the results achieved with devices in dual-in-line ceramic packages, and establish the activation energy to be used for extrapolating the results of accelerated tests. The test matrices are shown in Table III-1.

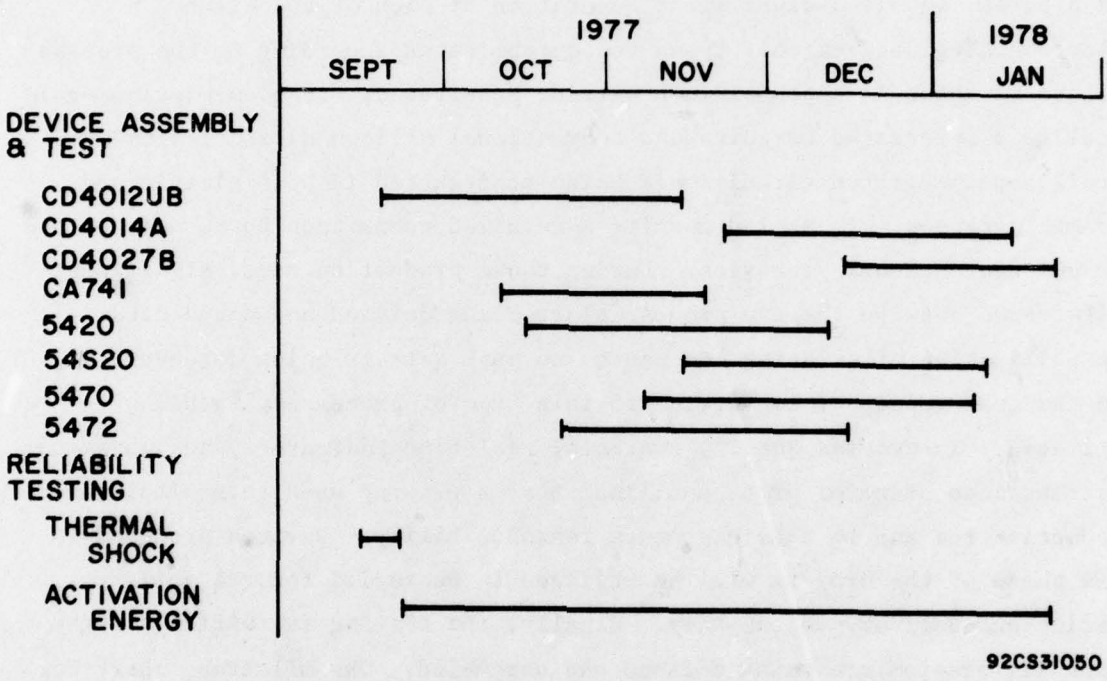

Fig. III-1 - Phase II milestone chart.

TABLE III-1 - Phase II Test Plan

Life Test	Assembly Technique			
	HRLC	Wire Bond Plastic	Sealed DIC	Unsealed DIC
Bias				
250°C	30	30	30	30
225°C	30	30	30	30
200°C	30	30	30	30
175°C	30	30	30	30
150°C	30	30	30	30
Storage				
250°C	30	30	30	30
225°C	30	30	30	30
200°C	30	30	30	30
175°C	30	30	30	30
150°C	30	30	30	30

SECTION IV

DETAILED FACTUAL DATA

TECHNICAL DISCUSSION

A. WAFER FABRICATION

Wafer fabrication of the eight integrated-circuit types has been completed. HRLC processing has been successfully adapted to four technologies, CMOS, T^2L, Schottky T^2L and bipolar linear. The wafer processing for each technology is briefly discussed below.

CMOS - Processing of CMOS wafers for the HRLC program is conventional up to the channel oxidation step. At this point a thinner than normal channel oxide is grown so that the composite SiO_2 - Si_3N_4 dielectric is equivalent in terms of threshold voltage to a conventional SiO_2 dielectric. Metallization of these wafers utilizes magnetron-sputtered titanium and platinum and electroplated gold. Electrical characteristics of HRLC devices are equivalent to those observed on conventional aluminum-metallized devices.

The processing of CMOS wafers results in tapered oxide cuts. It was found that this type of geometry is amenable to sputter-etch techniques for metal definition. Accordingly, sputter etching was used to define the platinum film using the plated gold as a sputter mask. This technique obviates the need for the platinum-definition photoresist step and allows the use of tightened design rules to increase packing density. This development indicates the applicability of HRLC processing to LSI.

T^2L - HRLC processing has been found to be entirely compatible with T^2L technology. No deleterious effects of the CVD silicon nitride deposition or metallization on any electrical characteristic has been observed.

Schottky T^2L - The use of HRLC technology on Schottky T^2L circuits results in the clamping diode being formed of platinum silicide. In conventional structures, this device is formed by aluminum silicide. This change did not impact the electrical characteristics of the circuits fabricated under the contract.

Bipolar Linear - HRLC processing is completely compatible with bipolar-linear wafer fabrication. No variations from conventional wafer processing are required through the emitter-diffusion process, at which point HRLC processing is initiated.

Independent of whether the devices are conventional or HRLC, the use of a surface-field ion implantation has been found to be useful in raising the field inversion voltage of the collector regions. This precludes the formation of conductive p-type channels between base regions and isolation regions when the devices are operated from relatively high-voltage supplies.

B. ASSEMBLY RELIABILITY ISSUES

1. Phase-II HRLC Bonding Problem

a. Nature of Problem

The Phase II HRLC bonding problem, as originally understood, was not immediately visible in all pellet types. Digital logic devices that do not drive high-current loads may require a longer time to fail because of this phenomenon. CD4012 units being stressed in Phase II bias and storage life did not show parametric degradation because of the bonding problem whereas CA741 operational-amplifier units stressed in the same manner showed selected parameter degradation. This degradation was visible only from the higher temperature stresses where many down periods were taken, resulting in single-cycle temperature cycling. High-temperature bias operation or high-temperature storage without intermittent down periods did not reveal

the problem. However, thermal-shock and temperature-cycling tests on suspected units did bring out the defect if units were subjected to high-current hot-continuity tests after thermal stressing.

b. Phase II Down-Period Indicators

Down periods for 250°C bias and storage life tests were specified at 2, 4, 8, 16, 32, 64, 128 and 256 hours. After 4 hours of high-temperature life (two down periods) input-offset voltage failures for the CA741 were noted for storage and bias life. At 32 hours, the number of units out of specification for the same reason was 26 percent for combined storage and bias life. In the same 32-hour stress period, the CD4012 250°C tests produced three out of specification units for unrelated reasons. Later analysis revealed that the CD4012 units were suffering from the same package defects as were the CA741 units, and required hot testing to make these defects visible electrically.

c. Thermal-Shock Indicators

On subjecting Phase-II CA741 devices to thermal shock tests, the same input-offset voltage drift was detected. After 100 cycles of liquid-to-liquid thermal shock, approximately 90 percent of the devices tested failed. Normal 25°C testing revealed few open-circuited pins, but testing for continuity at elevated temperatures showed many units open-circuited, mainly on the central pins on each side of the package (i.e., pins 3, 4, 5 and 10, 11, 12 on a 14-pin DIP).

d. Failure Analysis

The decapping of thermal-shocked devices that failed hot-continuity testing revealed bond-wire heel cracks at the device bonding pad. The cracks were such that high-resistance paths developed through them at a 25°C ambient, but opened at a 100°C ambient.

Fig. IV-1 shows curve-tracer photos of input-continuity tests for a CA741 after 128 hours of 250°C storage life. The "on" portion of the slope of the failed-unit trace indicates the increase in input resistance resulting from

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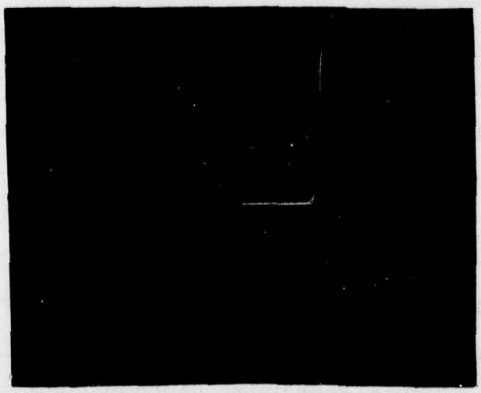

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Fig. IV-1 - Curve tracer examination of input resistance in CA741 at pin 4. (a) Control measurement. Good DIC, slope ≈ 60 kΩ. (b) HRLC device on 250°C 128-hour storage-life test. Slope ≈ 330 kΩ. Unit failed input-offset voltage test. (V_{IO} > 17 mV) (c) Same HRLC device as in (b) on 250°C 128-hour storage-life test after curve-tracer stress to close resistive gap. Slope ≈ 60 kΩ. Unit now passes input-offset voltage test. (V_{IO} < 1 mV)

the fracture at the heel of the bond. Pin 4 is the inverting input to the unit.

Fig. IV-2 is a photograph of a cross sectioned device showing the typical location and character of heel breaks.

2. Thermal-Shock Program to Improve HRLC System

a. Analysis of Heel Breaks

The cross-sectional view in Fig. IV-2 was made to show the beam-tape finger, the inner-lead bond, and the bumped chip in the area where electrical testing indicated a high-resistance connection so that the failure mode for devices that failed thermal-shock cycling could be analyzed.

The fracture in the beam tape is shown to occur at the heel of the inner-lead bond in the 0.003-inch width, Fig. IV-3, which extends 15 to 20 mils from the end of the finger. A study of the tape design revealed that, in this localized area, the total stress on the beam-tape finger is concentrated and that, under fatigue stress conditions, the failures could be anticipated. Such failures begin as small cracks on the surface of the part and, as the cracks propagate, they progressively reduce the ability of the weakened section to withstand the strain. This condition is particularly important at the heel of the bond where the cross section of the lead is reduced as a result of the thermocompression bonding process.

Fig. IV-4 illustrates the magnitude of the strain that is present in a straight, short finger under mechanical loading. Sections I and IV represent the inner- and outer-lead bond areas, respectively. The strain in sections II and III under load is shown to be concentrated in section II because of the higher unit stress. The point where section I ends and section II begins is the heel of the inner-lead bond where, again, virtually all of the lead breaks occur.

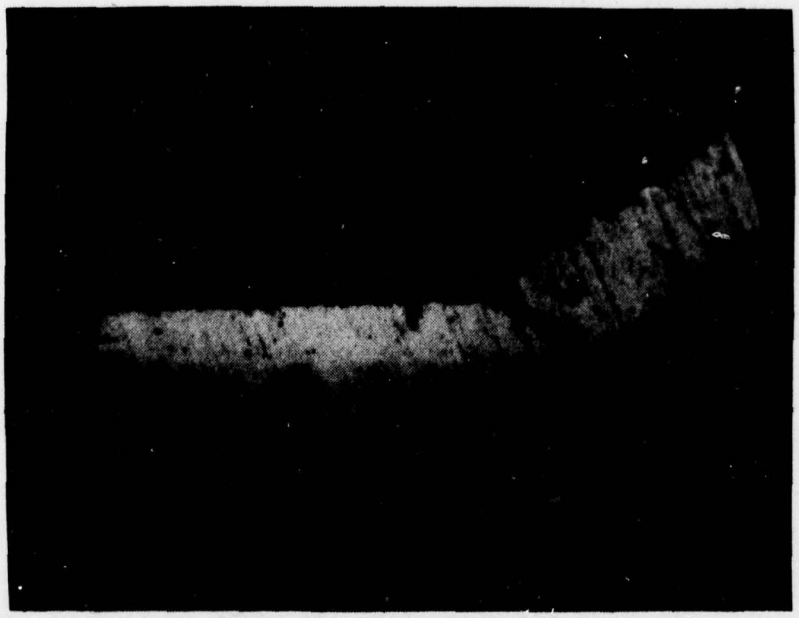

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Fig. IV-2 - Typical heel break (high resistance - 200 k) of pin 11 on CA741 stressed at 250°C standard life. Device failed after 128 hours and 7 down periods. (V_{IO} = 17 mV)

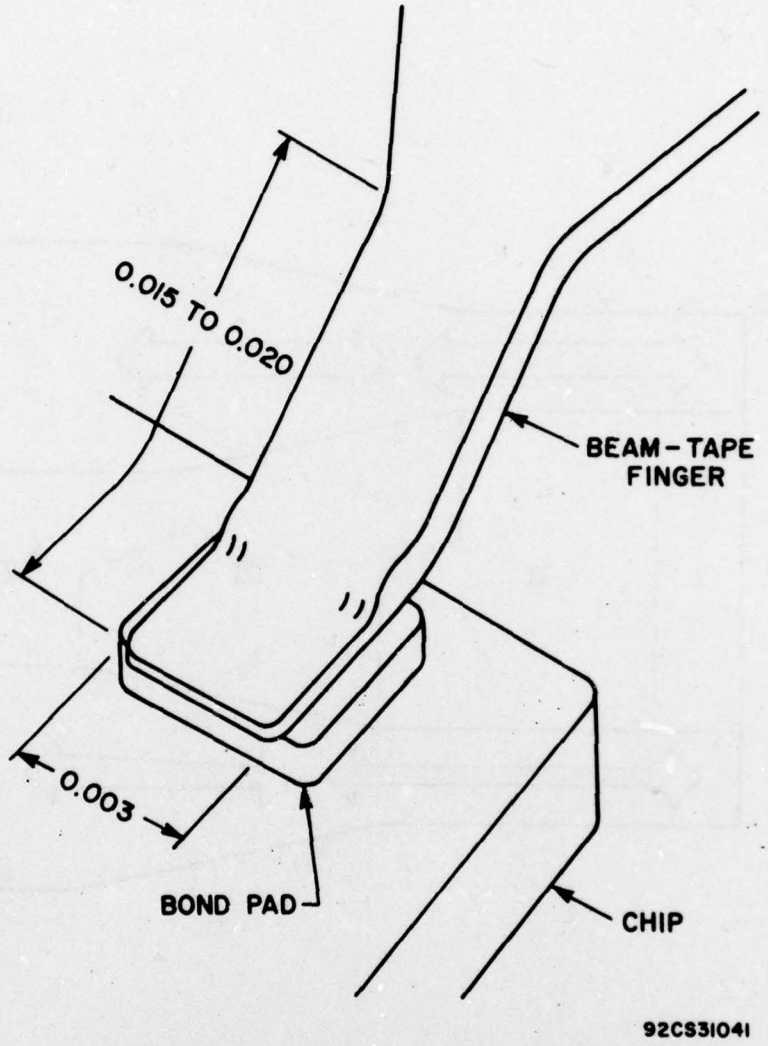

Fig. IV-3 - Schematic drawing of the portions of the beam-tape finger, inner-lead bond, and bumped chip involved in heel breaks.

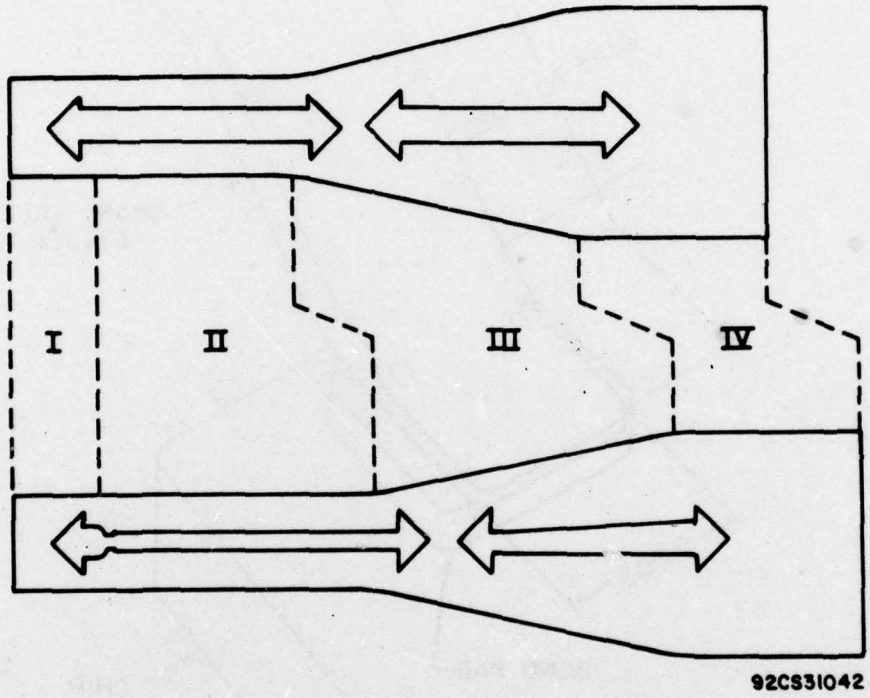

Fig. IV-4 - Strain in beam-tape finger.

b. Redesign of the Beam Shapes

A redesign of the beam-tape was made which minimized the stress concentration in the 0.003-inch-width sections of the tape. A 90° bend in the plan view of the finger, Fig. IV-5, prevents tensile strain from being transferred from one section of the beam to another.

The CA741 device type was selected as the means of evaluation of the redesign of the beam tape, and engineering samples of the tape were produced in-house. The samples were etched in bare copper, unsupported by polyimide, and subsequently plated with gold.

c. Plated Copper to Improve Strength

In the process of fabricating beam tape, the copper is cleaned by means of a mild etchant. This operation leaves an irregular surface in which stress cracking can originate during severe loading conditions. This surface is also more vulnerable to oxidation defects because of the greater area exposed to the environment. These conditions can be minimized by plating the copper with a suitable material; gold on copper and gold on nickel on copper have been selected as the metallurgical systems to be evaluated.

d. Thermal-Shock Tests for Improved Results

A matrix of tests was devised to aid in an evaluation of the variables that affect the strength of the beam-tape system. The tests were arranged in cells of twenty units each. Thermal-shock testing was selected as the method of exercising the assembled devices.

Variables selected for comparison included:

1. Stress relief versus no stress relief in the beam-tape design
2. Copper beam tape versus gold plated copper beam tape versus gold-plated nickel-plated copper beam tape
3. With polyimide versus without polyimide
4. RCA copper versus 3M Company copper
5. Silver-plated copper lead frames versus spot gold-plated steel lead frames.

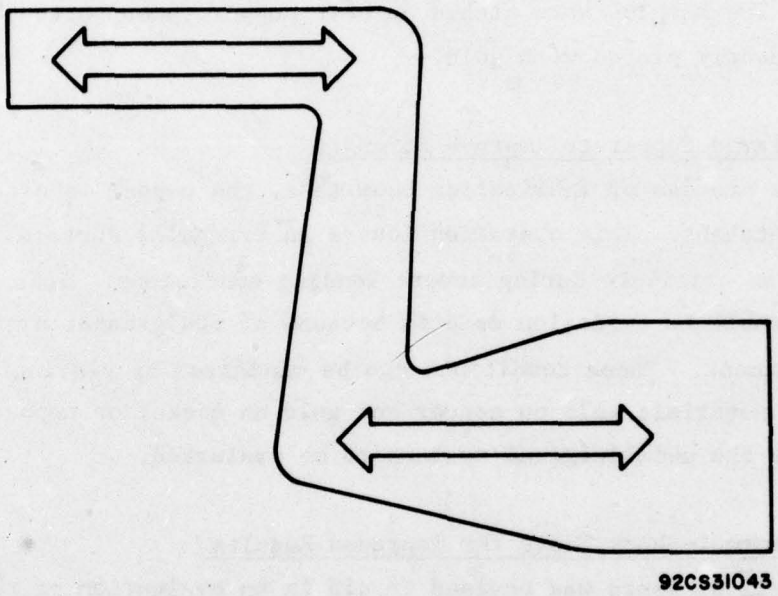

Fig. IV-5 - Strain in redesigned beam-tape finger.

The most significant factors in the reliability performance of the cells tested were the stress-relief pattern and the plating on the beam-tape copper. There was no conclusive evidence that the presence of polyimide was a factor, nor was there any significant difference in the use of the copper from the 3M Company over RCA copper. The lead frames performed identically and proved not to be a factor.

e. Gold and/or Nickel-Gold Plate with Stress Relief

The results of the matrix tests clearly indicate that the stress-relief pattern is essential to the reliability of HRLC devices made with copper beam tape. Similarly, gold plating, with or without nickel plating, improved system resistance to thermal shock. Where most units made without stress-relief, gold-plated beam tape failed at less than 400 cycles of thermal shock (-65° to + 150°C), devices with these features were functional after 2000 cycles.

f. Results of Total Thermal-Shock Problem

The assembly of IC chips using beam-tape technology results in a far stronger finished device than one assembled with flying wires. However, this strength can adversely affect reliability by causing very high stress concentrations in a rigid mechanical system. High stress coupled with fatigue cycling is a very severe problem in the mechanics of materials.

For this program, beam tapes are being redesigned to avoid the stress concentration conditions. These tapes will be produced by the 3M Company; the designs for four device types have been released for fabrication.

In addition to the changes in the lead configurations, the copper tape will be plated with 75 microinches of gold. Gold plating without the nickel barrier was selected after the thermal shock test cells using plated beam tape, both with and without the nickel, performed equally well. Although nickel is an excellent barrier between the copper and gold, the plating thickness of the nickel is difficult to control, and thick layers adversely affect thermocompression bonding parameters.

The tape from 3M Company will differ from the tape made in-house by RCA in that it will include a ring of polyimide, which will support the fingers. To promptly assure that this difference is not significant to performance, the first tape was expedited by the 3M Company so that samples could be made for thermal-shock testing.

A cell of approximately 600 CD4012UB units are assembled and will be used to perform the complete reliability evaluation on devices that incorporate the improvements achieved through the thermal-shock test matrix. Table IV-1 delineates the thermal-shock tests and results accomplished to date.

3. Phase-II Life Tests and Pellet-Oriented Problems

a. CD4012 Leakages & Deltas

Fig. IV-6 is a log-normal failure plot for CD4012 wire-bonded units packaged in silicone and stressed at 250°C in bias-life circuits. The failures for MIL limits at 128 hours were 33 percent of the total sample. Most of the units failed for leakage currents. All out of specification units and many not out of specification exeeded the 10 nanoampere MIL delta criteria for I_{SS}.

Figs. IV-7, IV-8 and IV-9 are histograms of the prevalent leakage problems, and show distributions based on total number of out of specification units. A large percentage of limit failures occur in the region just above the MIL limit.

b. CA741 Input Bias Current and Deltas

Fig. IV-10 shows a failure plot for the CA741 wire-bonded silicone-packaged units. Most of these failed units were out of specification for input bias current; Fig. IV-II shows the distribution of these failures. All failures and most of the units that did not fail exceeded the MIL delta requirement of 12 nA for end points.

TAB:E IV-1 - THERMAL SHOCK -65°C to +150°C

Test	Beam Tape	Stress Relief	Polyimide	Au Plate	Ni-Au Plate	Cu Lead Frame	Fe Lead Frame	DC480	100 Cycles	500 Cycles	1000 Cycles	1500 Cycles	2000 Cycles
741 Ø2	3M		X			X		X	29/29				
E19	3M				X		X	X		20/20			
E20	3M		X		X		X	X		20/20			
E21	3M		X				X	X		20/20			
E22	RCA	X			X		X	X		0/20	0/20	0/20	0/20
E23	RCA	X					X	X		0/20	8/20		
E26	RCA	X			X	X		X		0/20	0/20	1/20	
E27	RCA	X				X		X		1/20	8/19		
E29	RCA	X				X		X		7/20			
E30	RCA	X		X		X		X		0/20	0/20	0/20	1/20
E31	RCA	X			X	X		X		0/20	0/20	0/20	3/20
E32	RCA	X			X		X	X		0/20	0/20	0/20	3/20

TABLE IV-1 (Continued)

Test	Beam Tape	Stress Relief	Polyimide	Au Plate	Ni-Au Plate	Cu Lead Frame	Fe Lead Frame	DC480	100 Cycles	500 Cycles	1000 Cycles	1500 Cycles	2000 Cycles
3046 E12	RCA						X	X	1/20	3/19			
E13	3M	X		X			X	X		0/14	0/14	0/14	
E15	3M	X					X	X		0/16	0/16	2/16	0/14
E20	3M		X		X		X	X	0/20	0/20	20/20		
E21	3M	X			X		X	X		0/20		0/20	
E22	3M	X	X		X		X	X		6/20			
E23	3M		X	X			X	X		4/20			

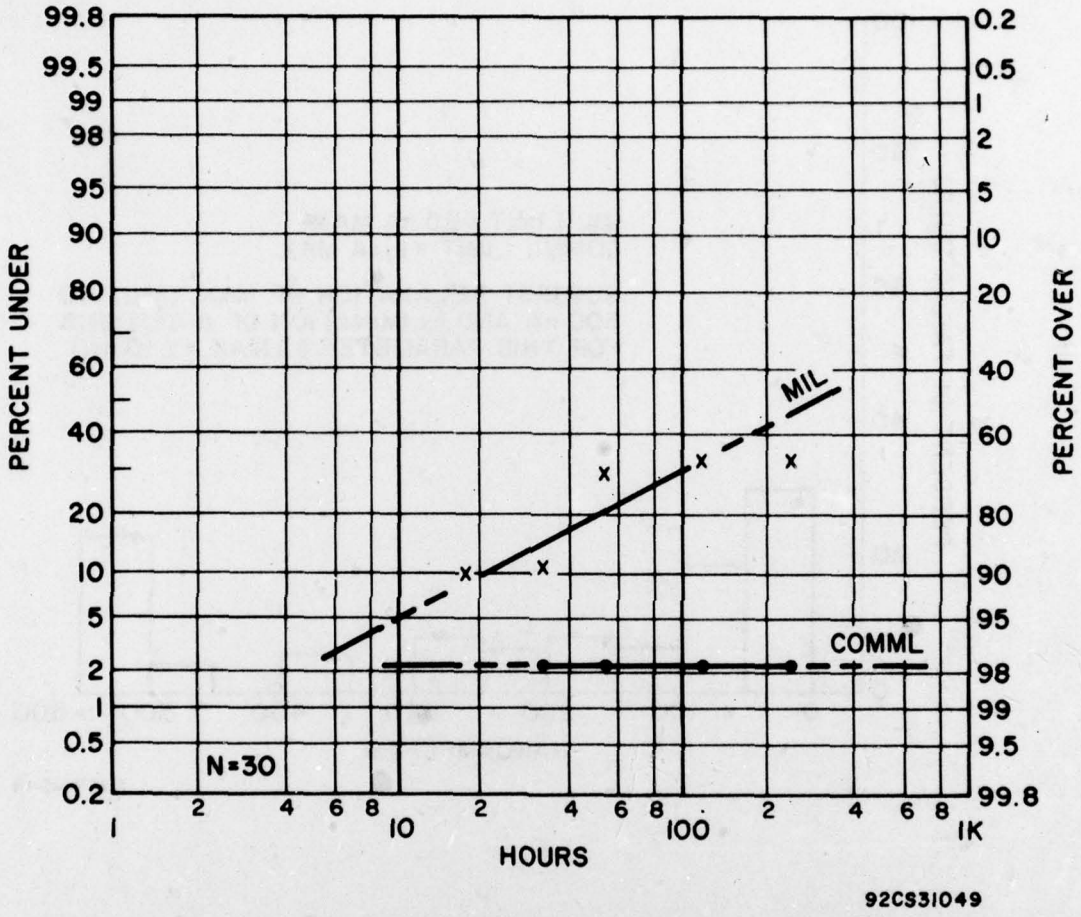

Fig. IV-6 - Log-normal failure plot for CD4012 wire-bonded units packaged in silicone and stressed at 250°C in bias-life circuits.

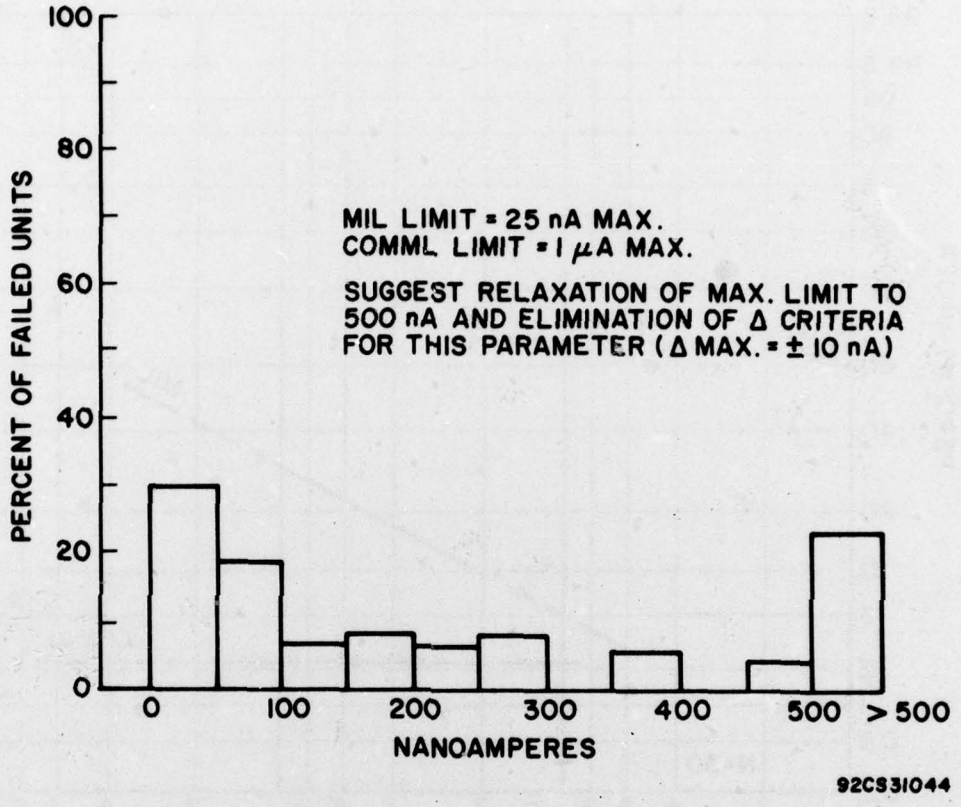

Fig. IV-7 - Out of specification distribution for I_{SS}, supply current, in CD4012 devices.

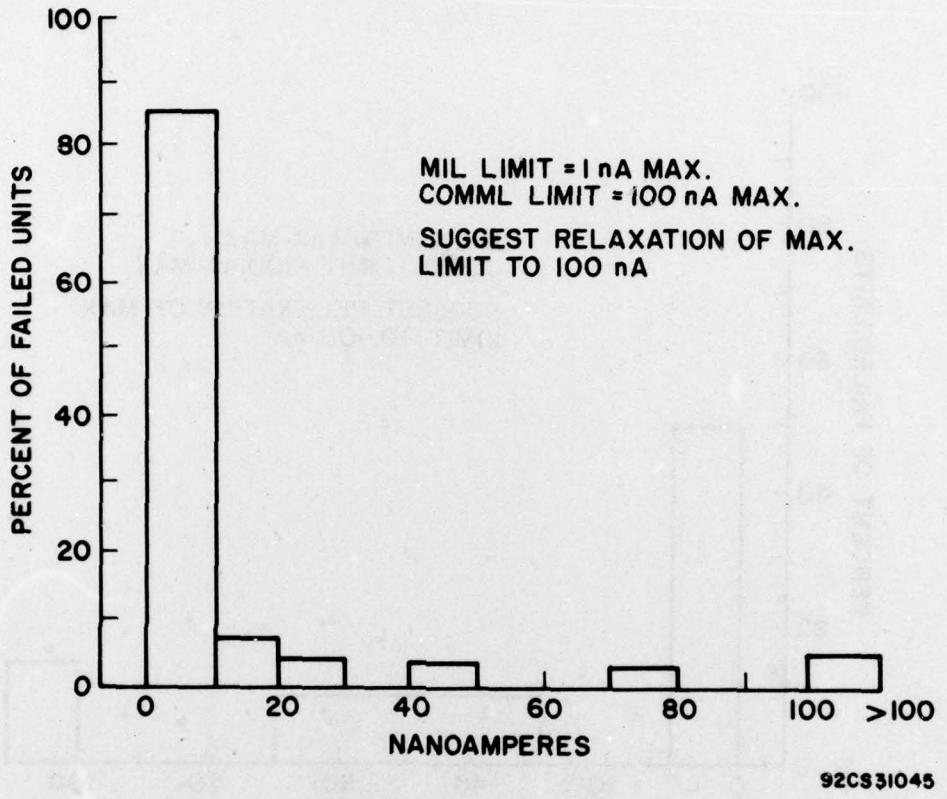

Fig. IV-8 - Out of specification distribution for I_{IL}, input leakage current, low level, in CD4012 devices.

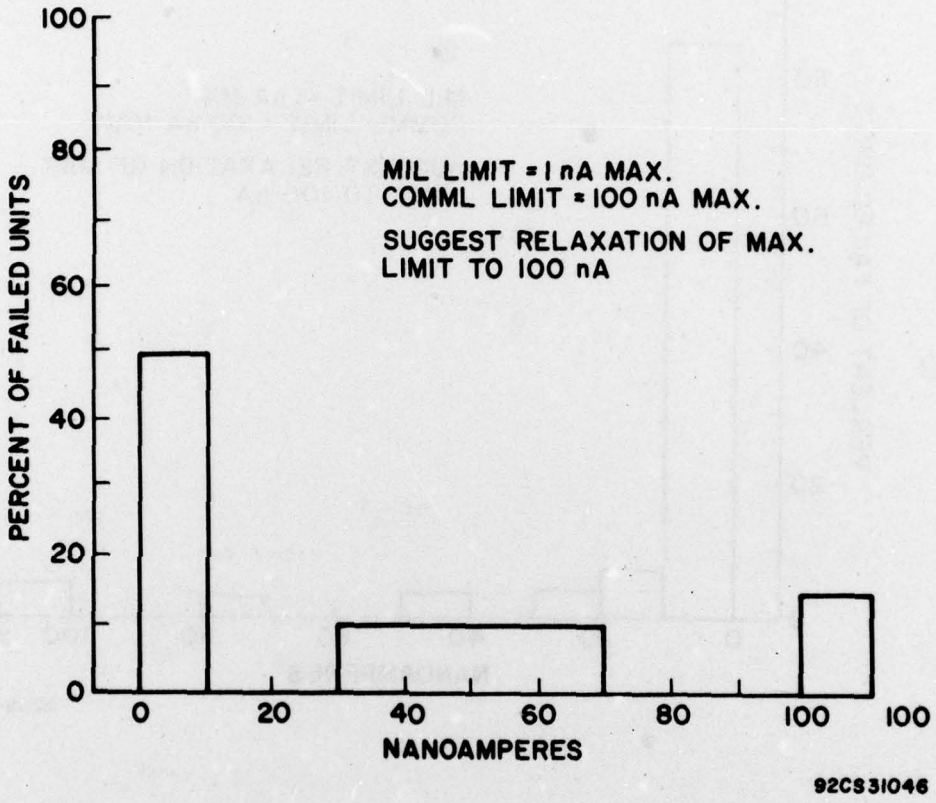

Fig. IV-9 - Out of specification distribution for I_{IH}, input leakage current, high level, in CD4012 devices.

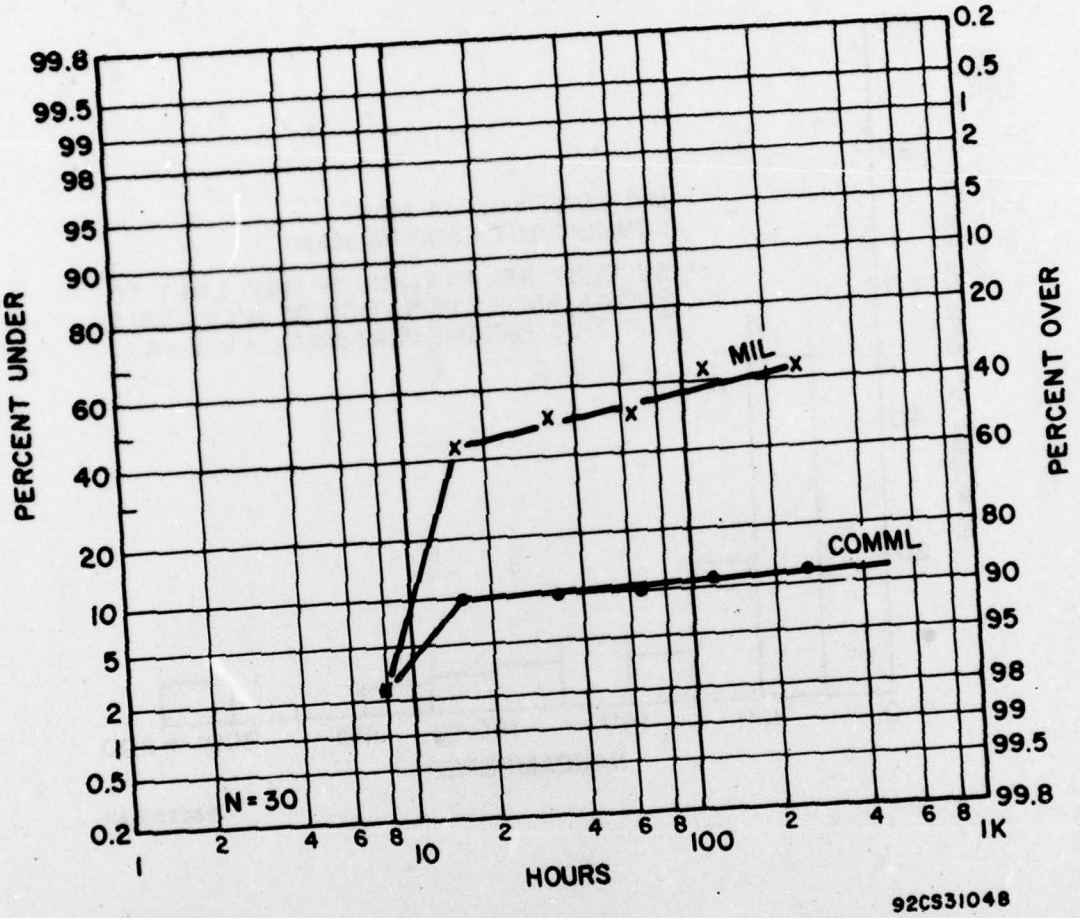

Fig. IV-10 - Failure plot for the CA741 wire-bonded silicone-packaged units.

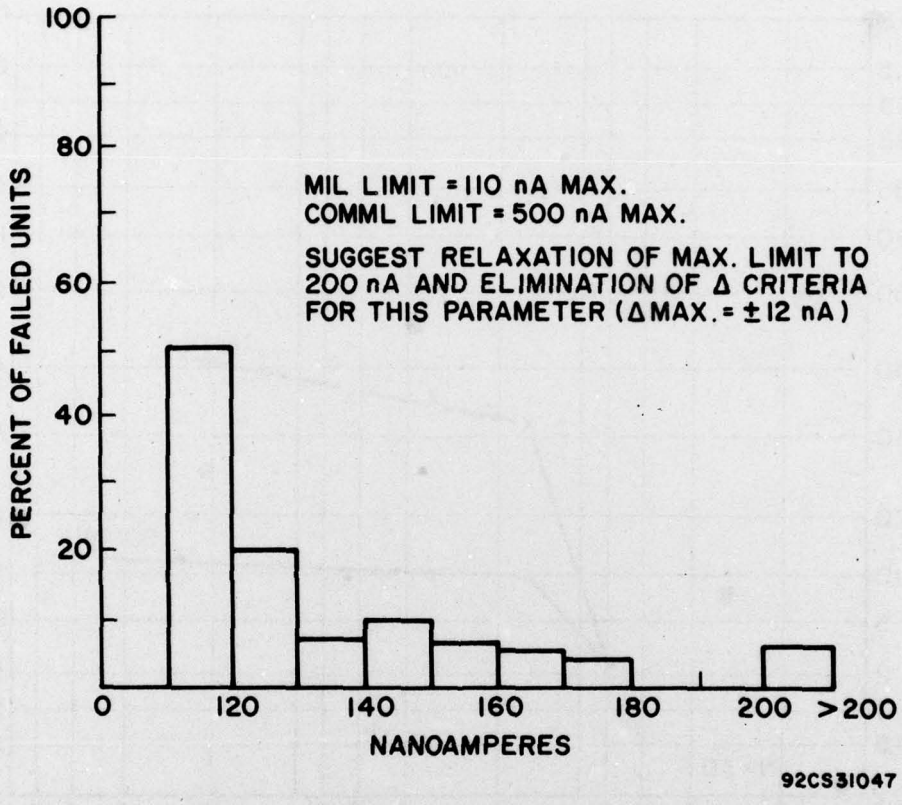

Fig. IV-11 - Out of specification distribution for I_{IB}, input bias current, in CA741 devices.

c. Military and Commercial Limit Failure Matrix

Fig. IV-12 depicts all Phase II failures in matrix form. The top number in a box is the quantity of commercial limit failures for that cell; the bottom quatity is the total number of commercial and MIL failures. The high numbers of failures in the 250°C, CA741, HRLC boxes is a result of the above mentioned bond-wire problem. Other higher than average quantities were the results of devices drifting just over MIL limits.

4. Status of Phase-II Testing

The original Phase-II testing program to develop acceleration factors has been completed. Because of the effect of the HRLC bonding problem on the data, the HRLC portion must be rerun with newly designed bonding tapes; one of these tapes is presently in house. Thermal-shock tests have begun to qualify these tapes for the HRLC process. It is expected that the Phase-II rerun will be completed by the end of the current year. A reliability milestone chart for the remainder of Phase II and for Phase III is shown in Fig. IV-13.

CD4012

	BIAS LIFE					STORAGE LIFE				
	250°C, 256 Hr	225°C, 256 Hr	200°C, 256 Hr	175°C, 1344 Hr	150°C, 1500 Hr	250°C, 256 Hr	225°C, 256 Hr	200°C, 256 Hr	175°C, 1344 Hr	150°C, 2000 Hr
HRLC	2	2	2	2	0	0	0	0	1	1
	12	8	5	5	7	6	3	6	2	5
PLASTIC	1	1	1	2	1	0	1	0	0	0
W.B.	10	9	9	7	5	1	4	5	2	2
DIC	2	2	3	1	4	1	1	0	0	0
SEALED	9	7	7	4	20	8	5	5	30	30
DIC	3	1	0	1	4	1	1	2	1	2
UNSEALED	25	21	6	9	12	22	22	18	27	30

CA741

	BIAS LIFE					STORAGE LIFE				
	250°C 256 Hr	225°C, 256 Hr	200°C, 256 Hr	175°C 1344 Hr	150°C 1500 Hr	250°C, 256 Hr	225°C, 256 Hr	200°C, 256 Hr	175°C, 1344 Hr	150°C, 2000 Hr
HRLC	15	5	0	3	1	18	5	0	4	0
	21	5	1	3	2	18	5	0	5	0
PLASTIC	4	0	0	1	1	0	1	1	0	0
W.B.	20	3	2	1	2	1	2	1	1	0
DIC	1	2	1	1	0	0	2	0	1	0
SEALED	17	2	4	1	1	0	2	0	2	2
DIC	3	0	0	1	0	0	0	0	0	0
UNSEALED	22	0	2	1	1	0	1	1	1	1

Fig. IV-12 - Matrix of all failures in Phase II. N=30 for each cell. Top number in box is total commercial limit failures; bottom number is total commerical and MIL failures.

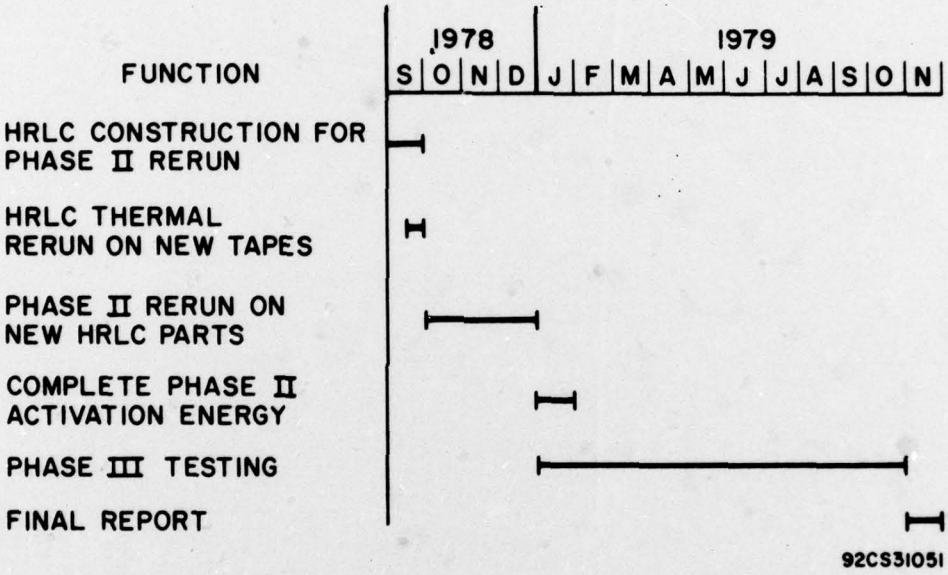

Fig. IV-13 Reliability milestone chart.

SECTION V
CONCLUSIONS

Tests indicate that integrated circuits fabricated with an automatic system of beam-tape bonding and packaged in DC480 silicone are capable of withstanding an average of 2000 cycles of -65°C to +150°C liquid-to-liquid thermal shock before bonding system failure. Preliminary data also indicate that this type of package is at least equal to that of a hermetic package with respect to the electrical performance characteristics of gold-chip tri-metal integrated circuits.

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