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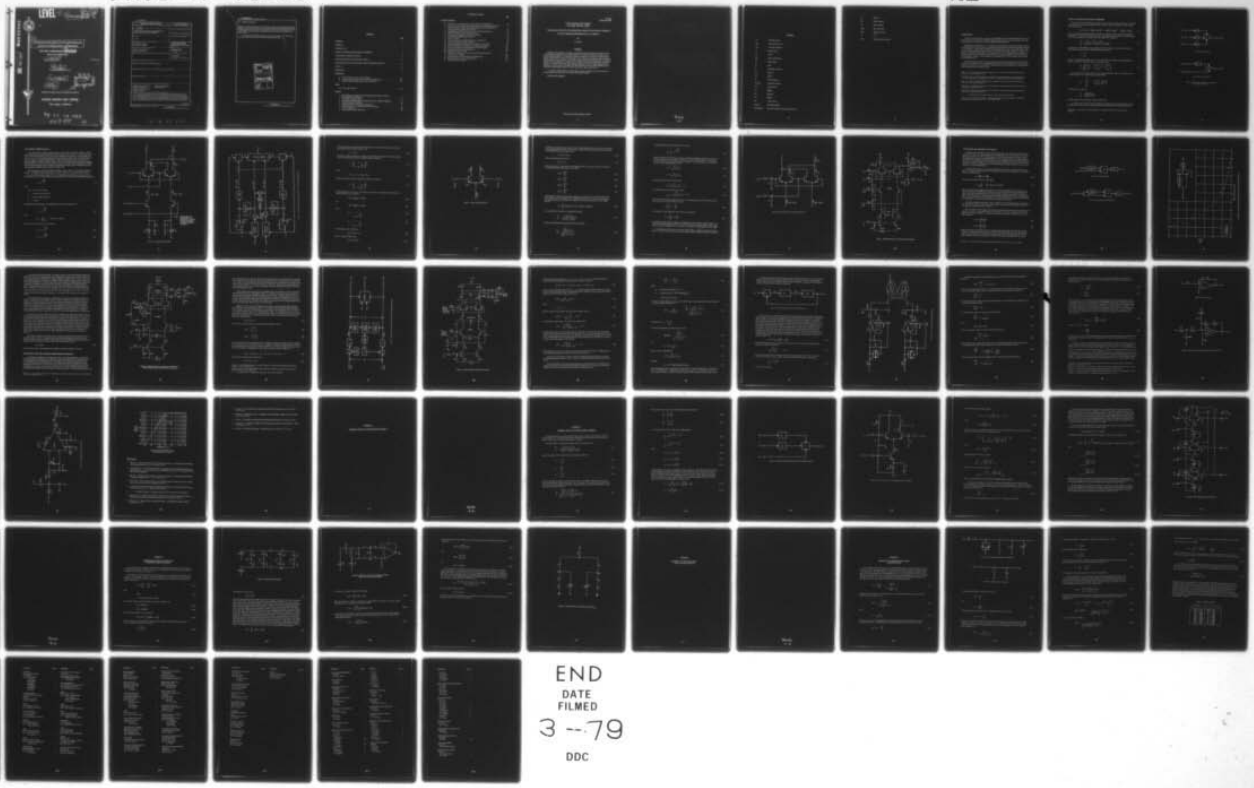

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Following a brief discussion of the theory of predetection diversity combining, this report is devoted to developing the detailed circuitry and design equations of the major components for implementing an AM/AGC weighted combiner. An optimum two-channel combining circuit is described as well as a multichannel combiner with near optimum characteristics. The circuitry for a wide dynamic range, noncoherent AM detector with output proportional to the absolute value of signal plus noise is

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A two-channel AM/AGC weighted combiner using the circuits described in this report has been constructed and shown to outperform a conventional AGC weighted combiner.

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TECHNIQUES AND CIRCUITS FOR IMPLEMENTING PREDETECTION DIVERSITY COMBINERS

(AIRTASK A6306302-054D-8W06040000, Work Unit A6302D-02)

By

E. R. HILL

SUMMARY

Following a brief discussion of the theory of predetection diversity combining, this report is devoted to developing the detailed circuitry and design equations of the major components for implementing an AM/AGC weighted combiner. An optimum two-channel combining circuit is described as well as a multichannel combiner with near optimum characteristics. The circuitry for a wide dynamic range, noncoherent AM detector with output proportional to the absolute value of signal plus noise is developed. A differential phase-locked loop configuration in conjunction with a 10-MHz to tape-carrier (900-kHz) down converter is analyzed. A sensitive, wide dynamic range, digital phase-frequency detector incorporating ECL Schmitt triggers and a set-reset flip-flop is presented. The VCO requirements for the combiner application are discussed and a suitable design using an LC oscillator with varactor diode control is given.

A two-channel AM/AGC weighted combiner using the circuits described in this report has been constructed and shown to outperform a conventional AGC weighted combiner.

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GLOSSARY

AC	Alternating current
AGC	Automatic gain control
AM	Amplitude modulation
^{o}C	Degrees Celsius
dB	Decibel
ECL	Emitter coupled logic
^{o}K	Degrees Kelvin
Hz	Hertz
IF	Intermediate frequency
kHz	Kilohertz
kΩ	Kilohm
LC	Inductor-Capacitor
Log Amp	Logarithmic amplifier
LPF	Low-pass filter
mA	Milliamp
mH	Millihenry
mV	Millivolt
OR	A logic function
Op Amp	Operational amplifier
PCM (NRZ-L)	Pulse code modulation (non-return-to-zero-level)

pF	Picofarad
RC	Resistor-capacitor
RF	Radio frequency
RMS	Root mean square
SNR	Signal-to-noise ratio
V	Volt
VCO	Voltage-controlled oscillator

INTRODUCTION

The work reported herein was conducted under AIRTASK A6306302-054D-8W06040000, Missile Flight Evaluation Systems, and Work Unit A6302D-02, Range Telemetry Support, which was established to provide technical support to the Telemetry Group of the Range Commanders Council.

Methods have been proposed [1,2,3,4] for improving the performance of conventional automatic gain control (AGC) weighted diversity combiners in the presence of fast-fading radio frequency (RF) signals. Methods [1,2] are described for obtaining wider bandwidth weighting signals by use of the receiver AM (envelope of the linear intermediate frequency) voltage in addition to the receiver AGC voltages to weight the combiner. Also, methods for improving the phase-locked loop performance in the combiner application were investigated.[4] Experimental circuitry has been developed and initial evaluation has been conducted under both laboratory[3] and operational[5,6] conditions. The descriptions in these publications [1,2,3,4] were confined to the functional and block diagram level.

Following a brief introduction to the theoretical basis for predetection diversity combiners, this report is devoted to the detailed circuitry and design equations necessary for their implementation. The principal motivation for this work was an investigation[7] at Vandenberg Air Force Base, California, of combiner requirements during the launch of multistage missiles.

[1]Hill, E. R. "Time Domain Analysis of an AGC Weighted Combiner," in *Proceedings of International Telemetering Conference,* Vol. 9, pp. 475-494, Oct 1973.

[2]Naval Missile Center. *Time Domain Analysis of an Automatic Gain Control Weighted Diversity Combining System,* by E. R. Hill. Point Mugu, Calif., NAVMISCEN, 14 Dec 1973. (Technical Publication TP-73-47) UNCLASSIFIED.

[3]Hill, E. R. "AM/AGC Weighted Pre-Detection Diversity Combining," in *Proceedings of International Telemetering Conference,* Vol. 13, pp. 215-238, Oct 1977.

[4]Novak, M. E. "An Investigation of Phase Lock Loop Requirements in Diversity Combiners," Master's thesis, California State University, Northridge, Calif., 1977.

[5]Vandenberg AFB. *Diversity Combiner A-M/AGC Control Technique.* Vandenberg AFB, Calif., Space and Missile Test Center, 1976. (Report No. PA 100-76-48)

[6]_____. *A-M/AGC Combiner.* Vandenberg AFB, Calif., 1976. (Report No. PA 100-76-68)

[7]Streich, R. G., D. E. Little, and R. B. Pickett. "Dynamic Requirements for Diversity Combiners," in *Proceedings of International Telemetering Conference,* Vol. 8, pp. 635-642, Oct 1972.

THEORY OF PREDETECTION DIVERSITY COMBINING

The object of diversity combining is to combine a number of diversity signals such that the output SNR (signal-to-noise ratio) is greater than the SNR of any of the input signals. The output of a linear combiner can be represented by

$$S_o(t) + N_o(t) = a_1\left[S_1(t) + N_1(t)\right] + \cdots + a_i\left[S_i(t) + N_i(t)\right] + \cdots + a_n\left[S_n(t) + N_n(t)\right] \tag{1}$$

where a_i are weighting coefficients and $S_i(t)$ and $N_i(t)$ are the signal and noise voltages. A block diagram implementation of equation (1) appears in figure 1(a). If the signal components are coherent (phase aligned) and the noise components are uncorrelated the output SNR can be expressed by

$$\frac{S_o}{N_o} = \frac{a_1S_1 + \cdots + a_iS_i + \cdots + a_nS_n}{\sqrt{(a_1N_1)^2 + \cdots + (a_iN_i)^2 + \cdots + (a_nN_n)^2}} \tag{2}$$

where S_i and N_i are the RMS (root mean square) signal and noise voltages. It has been shown[8] that the output SNR is maximized when the weighting coefficients are equal to

$$a_i = \frac{S_i}{N_i^2} \tag{3}$$

where S_i are the RMS signal voltages and N_i^2 are the mean square noise voltages. When all weighting coefficients are optimum, equation (2) reduces to its maximum value

$$\frac{S_o}{N_o} = \sqrt{\left(\frac{S_1}{N_1}\right)^2 + \cdots + \left(\frac{S_i}{N_i}\right)^2 + \cdots + \left(\frac{S_n}{N_n}\right)^2} \tag{4}$$

For an optimum two-channel combiner a single weighting coefficient, called the combining ratio, can be defined as the ratio of the individual weighting coefficients

$$a_R = \frac{\dfrac{S_1}{N_1^2}}{\dfrac{S_2}{N_2^2}} = \left(\frac{S_1}{S_2}\right)\left(\frac{N_2^2}{N_1^2}\right) \tag{5}$$

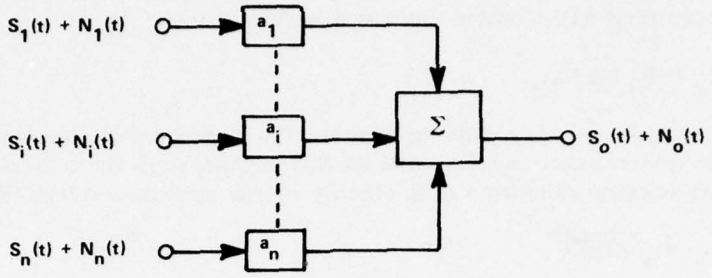
and equation (2) now reduces to

$$\frac{S_o}{N_o} = \frac{a_RS_1 + S_2}{\sqrt{a_R^2N_1^2 + N_2^2}} \tag{6}$$

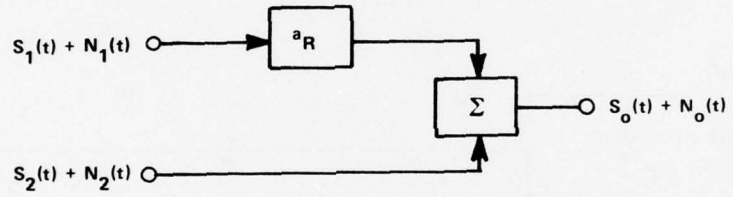
The block diagram for this configuration appears in figure 1(b).

For the predetection diversity combiner application, the signal S (t) and noise N(t) voltages are those appearing at the output of the linear IF (intermediate frequency) amplifiers of an RF telemetry receiver.

[8] Brennan, D. G. "Linear Diversity Combining Techniques," in *Proceedings of the Institute of Radio Engineers*, June 1959.



(a) N-Channel Linear Combiner.



(b) Two-Channel Linear Combiner.

Figure 1. Block Diagrams of N-Channel and Two-Channel Linear Diversity Combiners.

The output voltage of the receiver is determined by an AGC system, as shown in figure 2, where the AM (amplitude modulation) detector and AGC integrator have been brought out for illustration. It is assumed that the baseband information is impressed upon the carrier by either phase or frequency modulation.

For fading frequencies which are low compared to the AGC system bandwidth, the RMS value e_s of the receiver input signal voltage $e_s(t)$ is related to the receiver AGC voltage e_g by

$$e_g = -K_1 \log K_2 e_s \tag{7}$$

where K_1 and K_2 are constants associated with the receiver. The receiver output noise is thermal in origin and is generated in the receiver source impedance and the first amplifier stages (or in the preamplifier of the antenna). This can be expressed in terms of an effective receiver input noise voltage (RMS)

$$n_e = \sqrt{kTBRF} \tag{8}$$

where

k = Boltzmann's constant (joules/^{0}K)

T = absolute temperature (degrees Kelvin)

B = effective receiver bandwidth (hertz)

R = receiver source impedance (ohms)

F = receiver noise figure

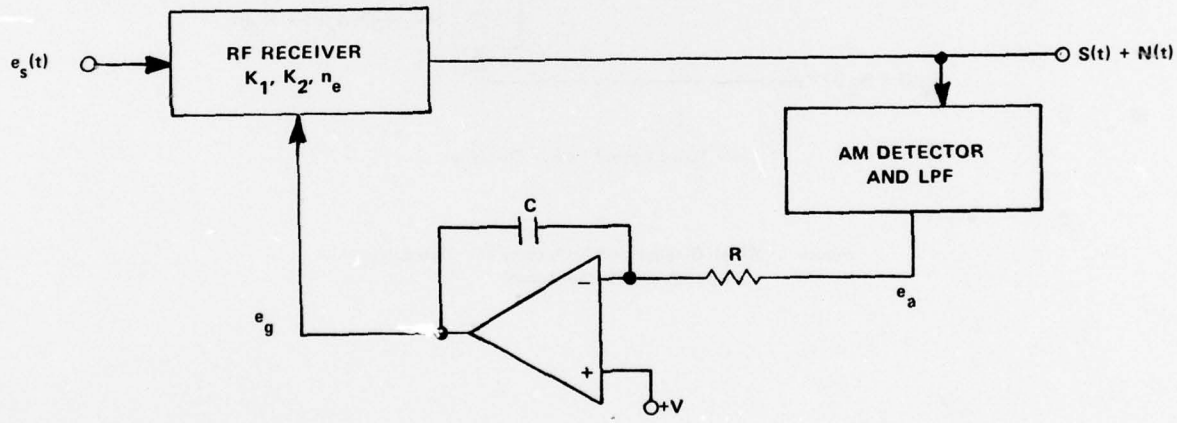


Figure 2. RF Receiver With AGC System.

The mean square noise voltage at the receiver output can be expressed[1] in terms of the AGC voltage e_g and the receiver parameters defined by equations (7) and (8)

$$N^2 = \left(\frac{\pi}{2\sqrt{2}}\right)^2 (K_2 V n_e)^2 \; 10^{\frac{2e_g}{K_1}} \tag{9}$$

where V is the AGC integrator bias voltage.

An AGC weighted combiner is implemented on the assumption that the receiver AGC systems are able to track the RF fading frequencies, thus maintaining the receiver output signals S_1 and S_2 equal. This assumption causes the optimum combining ratio of equation (5) to reduce to

$$a_R = \frac{N_2^2}{N_1^2} \tag{10}$$

which after the substitution of equation (9) becomes

$$a_R = \frac{N_2^2}{N_1^2} = 10^{\frac{2}{K_1}(e_{g2} - e_{g1})} \tag{11}$$

These two equations of course assume that both receivers have the same parameter values K_1, K_2, and n_e.

When the RF fading frequencies are too high for the receiver AGC system to track, the assumption that S_1 and S_2 are equal is no longer valid and the AGC weighted combiner is no longer optimum. An optimum combiner must account for the variations in the receiver output signal voltages S_1 and S_2. To place equation (5) in a form more suitable for implementation, replace the RMS voltages S_1 and S_2 by the average absolute values (full-wave rectified averages) of $S_1(t)$ and $S_2(t)$ and designate these by e_{a1} and e_{a2}, respectively. This is done since it is easier to approximate the average absolute value of a sinusoid embedded in noise than to approximate its RMS value. With this substitution and the defintion in equation (11) the optimum combining ratio in equation (5) now becomes

$$a_R = \frac{e_{a1}}{e_{a2}} \; 10^{\frac{2}{K_1}(e_{g2} - e_{g1})} \tag{12}$$

The weighting function in equation (12) is easier to implement if it is written in an exponential form similar to equation (11)

$$a_R = 10^{\frac{2}{K_1}(e_{w2} - e_{w1})} \tag{13}$$

where the weighting signals e_{w1} and e_{w2} are equal to

$$e_{w1} = e_{g1} - \frac{K_1}{2} \log\left(\frac{e_{a1}}{V}\right) \tag{14}$$

$$e_{w2} = e_{g2} - \frac{K_1}{2} \log\left(\frac{e_{a2}}{V}\right) \tag{15}$$

which are functions of the AGC and AM voltages.

[1] Hill, E. R. "Time Domain Analysis of an AGC Weighted Combiner," in *Proceedings of International Telemetering Conference*, Vol. 9, pp. 475-494, Oct 1973.

TWO CHANNEL COMBINING CIRCUIT

It was shown that the optimum combining ratio for both the AGC and AM/AGC weighted combiners can be represented by an exponential function as shown in equations (11) and (13). It will be shown in this section that the basic balanced modulator circuit, when configured as shown in figure 3, will implement this function. Figure 4 is a block diagram showing the combiner circuit in relation to the other major components of a complete two-channel combining system. Figure 4 also includes the option for either AGC or AM/AGC weighting. The AGC integrators in figure 4 are shown with inputs from the external, wide dynamic range AM detectors. Normally the AGC integrators are internal to the RF receivers with inputs from AM detectors with limited dynamic range. This does not degrade the performance since the AM signals at the Log Amp (logarithmic amplifier) outputs compensate for these errors.

The fundamental component of the balanced modulator circuit in figure 3 is the transistor differential amplifier. To establish the relationship between the control voltages e_{x1}, e_{x2}, and the collector currents I_{c1}, I_{c2} consider the differential amplifier in figure 5. Neglecting second-order effects, the collector current as a function of the base to emitter voltage of a single transistor can be written from the Ebers-Moll equations as

$$I_c = I_s\, e^{\frac{qV_{BE}}{kT}} \tag{16}$$

where

V_{BE} = base to emitter voltage

I_S = saturation current (constant)

q = electron charge (coulombs)

e = 2.71828 · · ·

To benefit the present derivation, write equation (16) in terms of an exponent of 10

$$I_c = I_s\, 10^{\frac{V_{BE}}{K_3}} \tag{17}$$

where

$$K_3 = \frac{kT}{q\log_{10}e} = 59 \text{ mV @ } T = 298^{\circ}K$$

The collector currents in figure 5 can be written as

$$I_{c1} = I_s\, 10^{\frac{V_{BE1}}{K_3}} \tag{18}$$

$$I_{c2} = I_s\, 10^{\frac{V_{BE2}}{K_3}} \tag{19}$$

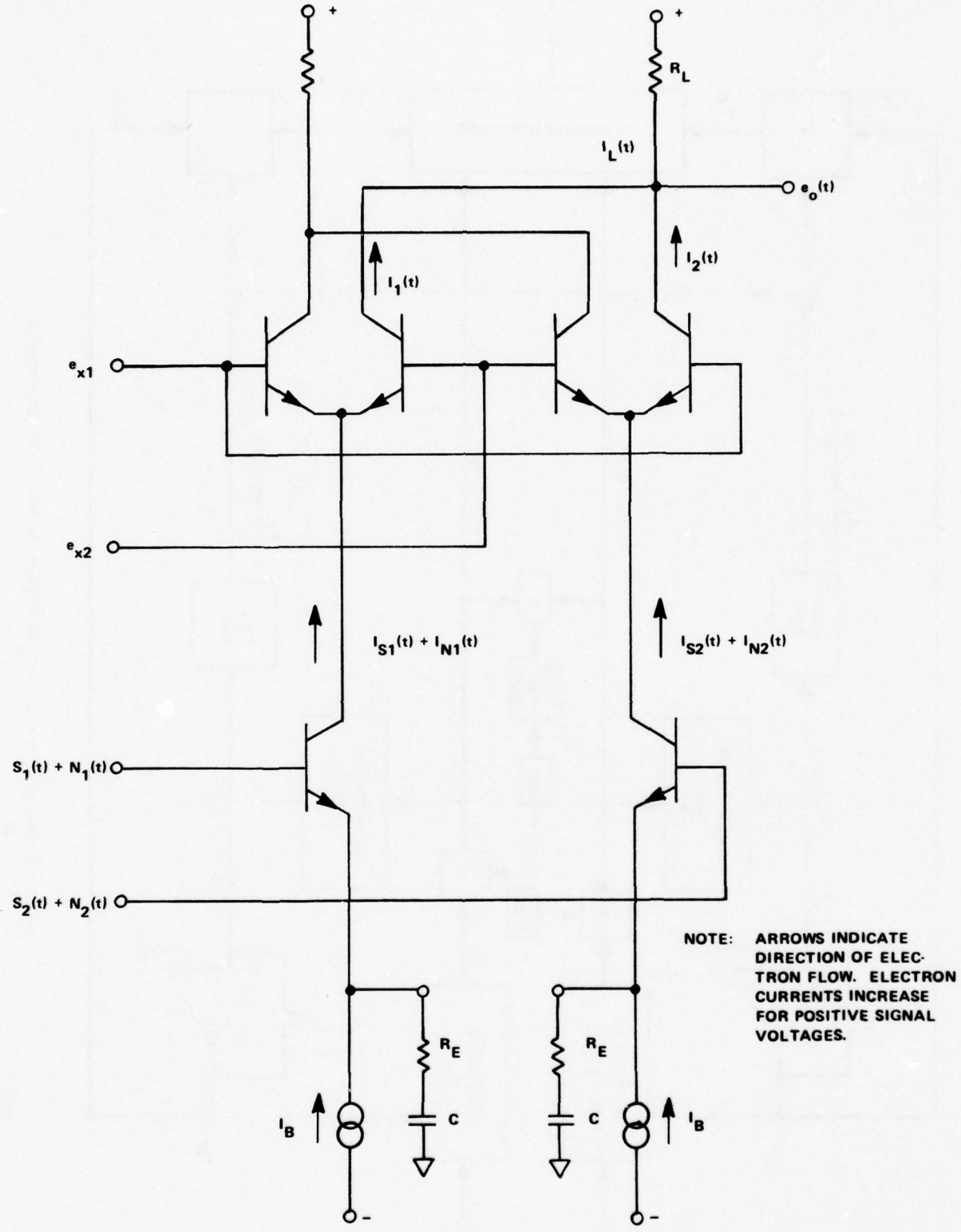


Figure 3. Two-Channel Combiner Circuit.

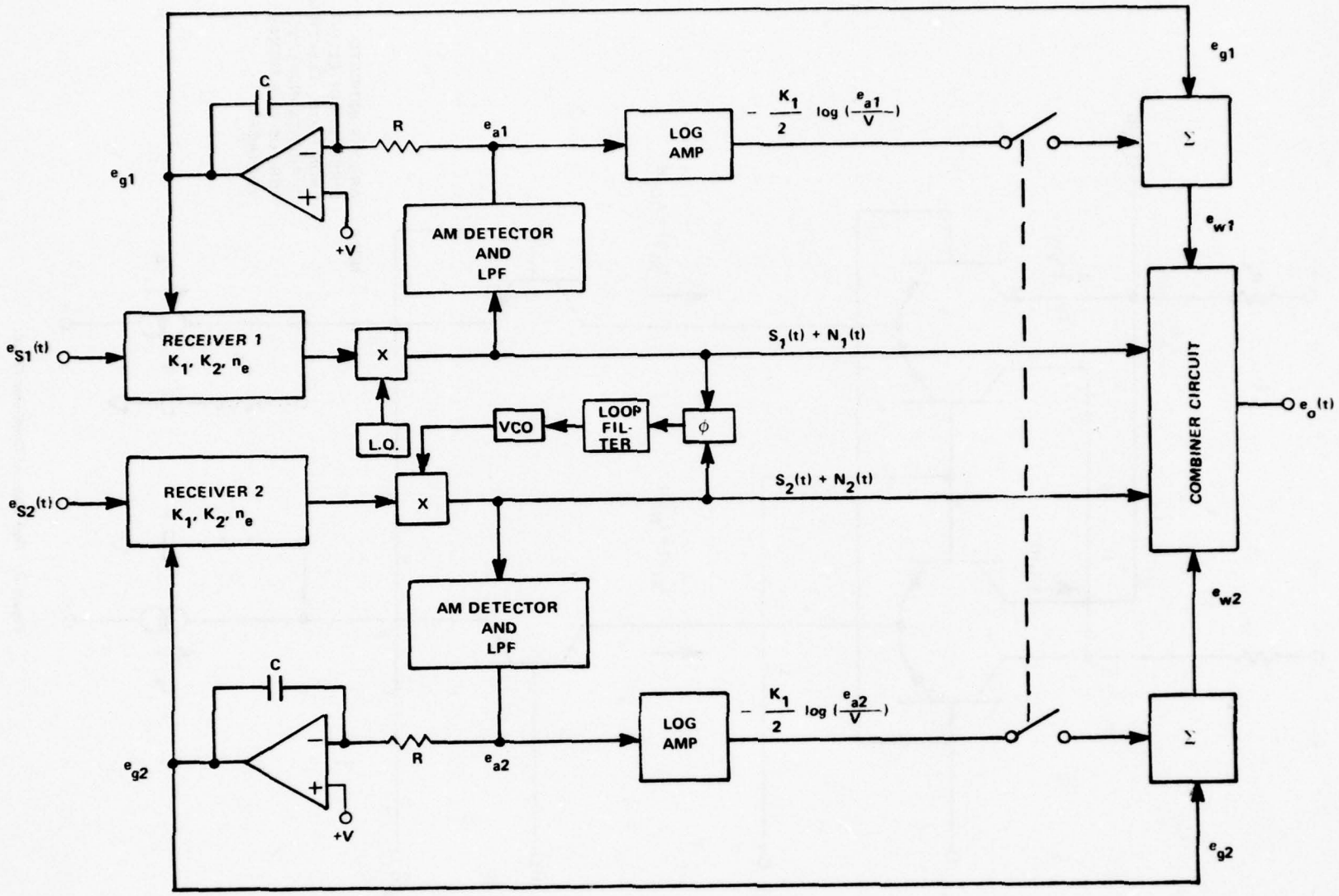


Figure 4. Two-Channel Combining System With Option for AGC or AM/AGC Weighting.

and if the transistor current gains are large compared to unity, the sum of the collector currents will approximately equal the common emitter current

$$I_{c1} + I_{c2} = I_o \tag{20}$$

The collector current of transistor T_1 in figure 5 can be obtained as a function of the common emitter current by the simultaneous solution of equations (18), (19), and (20).

$$I_{c1} = \left(\frac{1}{1 + 10^{\frac{\Delta e_x}{K_3}}} \right) I_o \tag{21}$$

where

$$\Delta e_x = e_{x2} - e_{x1} = V_{BE2} - V_{BE1} \tag{22}$$

Likewise the collector current of transistor T_2 in figure 5 is found to be

$$I_{c2} = \left(\frac{1}{1 + 10^{\frac{-\Delta e_x}{K_3}}} \right) I_o \tag{23}$$

Applying equations (21) and (23) to the combiner circuit in figure 3, the signal currents flowing to the common load R_L can be expressed by

$$I_1(t) = \mu_1 \left[I_{S1}(t) + I_{N1}(t) \right] \tag{24}$$

and

$$I_2(t) = \mu_2 \left[I_{S2}(t) + I_{N2}(t) \right] \tag{25}$$

where

$$\mu_1 = \frac{1}{1 + 10^{\frac{-\Delta e_x}{K_3}}} \tag{26}$$

$$\mu_2 = \frac{1}{1 + 10^{\frac{\Delta e_x}{K_3}}} \tag{27}$$

The total signal current to the load is

$$I_L(t) = I_1(t) + I_2(t) \tag{28}$$

and the total signal voltage is thus

$$e_o(t) = -R_L \, I_L(t) \tag{29}$$

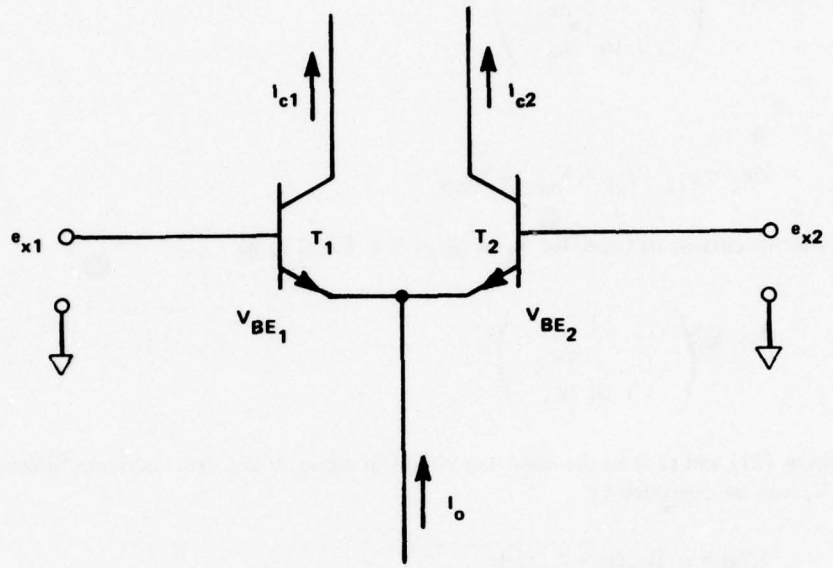


Figure 5. Transistor Differential Amplifier.

In addition to the signal currents, there is a DC bias current flowing in each section of the circuit in figure 3 which is independent of the signal or noise currents. If these bias currents are each equal to I_B as shown, the contribution flowing to the output load is

$$I_L = (\mu_1 + \mu_2)\, I_B \tag{30}$$

which is constant and equal to I_B since

$$\mu_1 + \mu_2 = 1 \tag{31}$$

If the bias current I_B is large compared to the signal and noise currents, these currents can be written as the following functions of the signal or noise voltages

$$I_{S1}(t) = \frac{S_1(t)}{R_E} \tag{32}$$

$$I_{N1}(t) = \frac{N_1(t)}{R_E} \tag{33}$$

$$I_{S2}(t) = \frac{S_2(t)}{R_E} \tag{34}$$

$$I_{N2}(t) = \frac{N_2(t)}{R_E} \tag{35}$$

provided that the transistor dynamic emitter resistance r_e and the reactance of C (in series with R_E) are small compared to R_E at frequencies in the IF bandwidth (centered at the combiner carrier frequency). By substituting these last four equations into equations (24), (25), (28), and (29), the output voltage becomes

$$e_o(t) = \frac{R_L}{R_E}\left[\mu_1 S_1(t) + \mu_1 N_1(t) + \mu_2 S_2(t) + \mu_2 N_2(t)\right] \tag{36}$$

The output SNR can be written as in equation (2) as follows

$$\frac{S_o}{N_o} = \frac{\mu_1 S_1 + \mu_2 S_2}{\sqrt{(\mu_1 N_1)^2 + (\mu_2 N_2)^2}} \tag{37}$$

which, after dividing numerator and denominator by μ_2, becomes

$$\frac{S_o}{N_o} = \frac{\left(\frac{\mu_1}{\mu_2}\right) S_1 + S_2}{\sqrt{\left(\frac{\mu_1}{\mu_2}\right)^2 N_1^{\,2} + N_2^{\,2}}} \tag{38}$$

Comparing equation (38) with equation (6) it is seen that

$$a_R = \frac{\mu_1}{\mu_2} = 10^{\frac{\Delta e_x}{K_3}} \tag{39}$$

which shows that the circuit in figure 3 produces an exponential weighting coefficient the same as the optimum combining ratio in equation (13) except for a constant of proportionality. A scaling factor can be introduced by resistor networks as shown in figure 6. The control voltages can be expressed as functions of the weighting signals as follows

$$e_{x1} = \left(\frac{R_2}{R_1 + R_2}\right) e_{w1} \tag{40}$$

$$e_{x2} = \left(\frac{R_2}{R_1 + R_2}\right) e_{w2} \tag{41}$$

Subtracting equation (40) from equation (41)

$$\Delta e_x = \left(\frac{R_2}{R_1 + R_2}\right) (e_{w2} - e_{w1}) \tag{42}$$

and substituting equation (42) into equation (39)

$$a_R = 10^{\frac{R_2}{K_3(R_1 + R_2)} (e_{w2} - e_{w1})} \tag{43}$$

the desired constant of proportionality is introduced. Comparing equation (13) with equation (43), it is seen that the proper scaling coefficient is given by

$$\frac{R_2}{R_1 + R_2} = \frac{2K_3}{K_1} \tag{44}$$

from which the relative magnitudes of the resistors can be expressed

$$R_1 = \left(\frac{K_1}{2K_3} - 1\right) R_2 \tag{45}$$

A complete functional schematic, designed for a 900-kHz tape carrier frequency, appears in figure 7. An Op Amp (operational amplifier) is used to sum the output signal currents and provide an output voltage source. The circuit components are selected to drive a 75-Ω load at a nominal signal level of 0.5V RMS.

Unfortunately, the circuit in figure 3 does not expand readily to combine more than two diversity signals. A circuit which will, however, combine any desired number of channels is described in Appendix A.

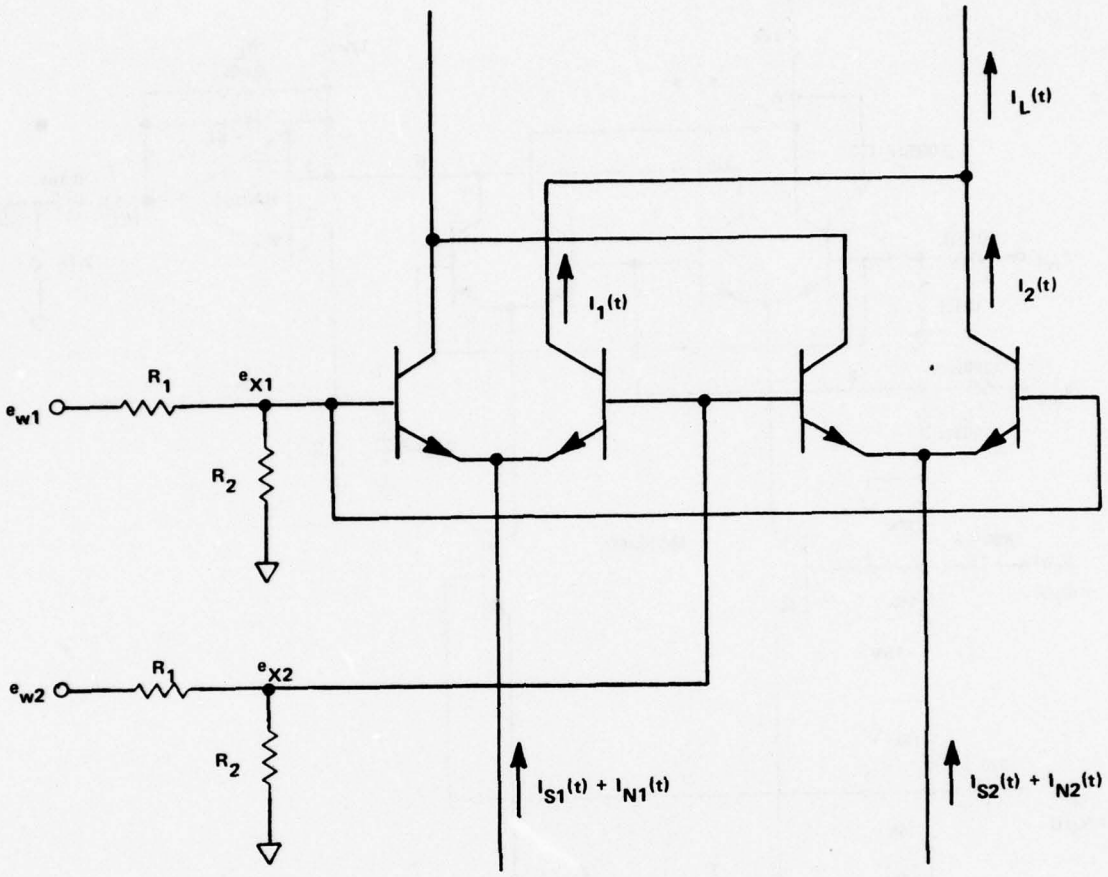


Figure 6. Resistor Networks for Introducing a Scaling Factor.

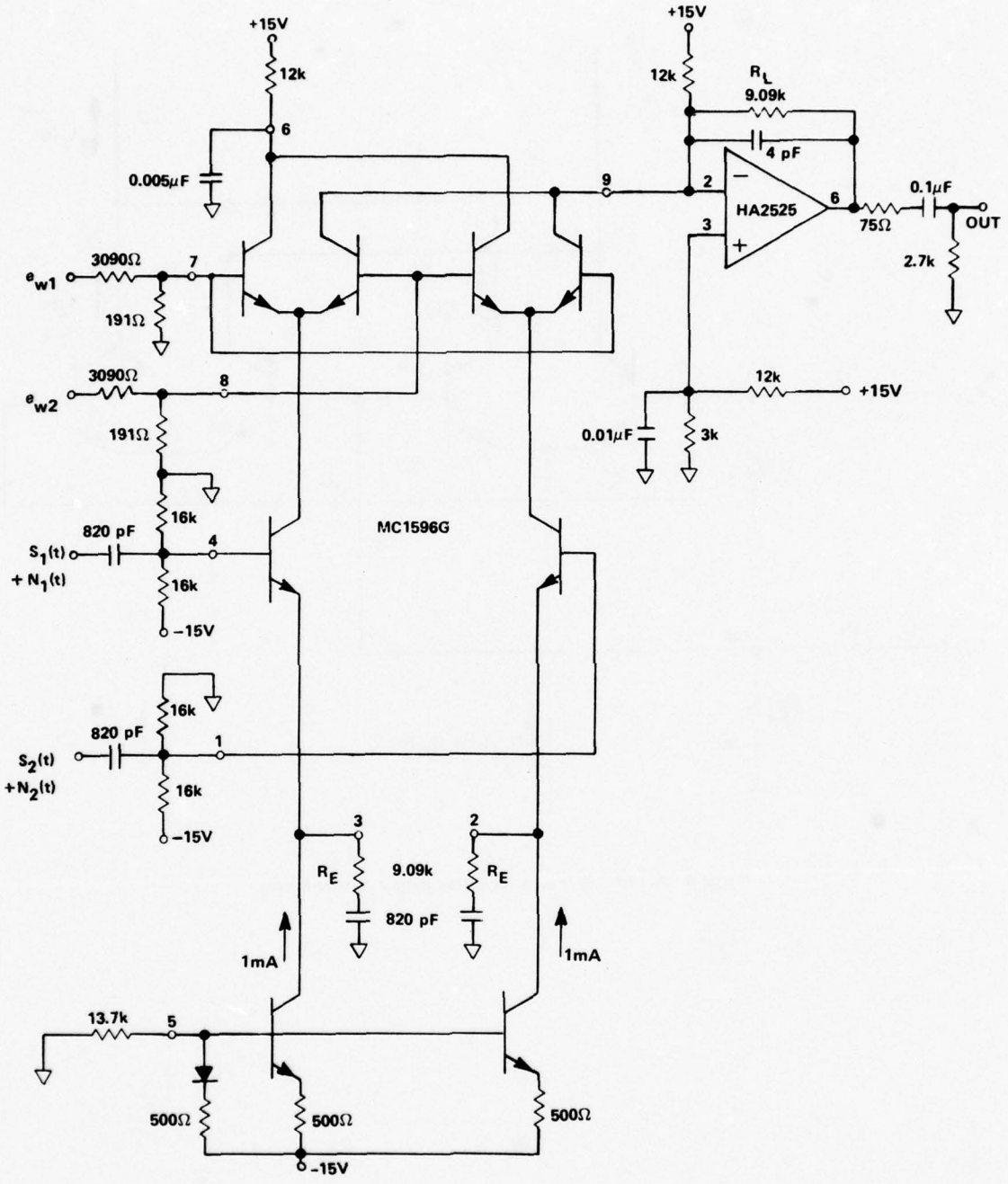


Figure 7. Complete Schematic of a Two-Channel Diversity Combiner.

AM DETECTOR AND LOW-PASS FILTER CIRCUIT

The AM detectors indicated in figure 4 should ideally produce a DC component proportional to the average absolute value of the signal component and be independent of the noise component. The coherent AM detector in figure 8 is a very close approximation to this ideal, limited only by the output low-pass filter (LPF) which is required to reject high-frequency product components and limit the noise bandwidth. The difficulty in implementing the coherent AM detector is in obtaining the phase of the signal component accurately. A phase-locked loop is the most practical method for obtaining this information but with wide-band phase or frequency modulation on the carrier and with high noise levels, the phase errors become too large for use in a coherent AM detector.

A practical approximation to the coherent AM detector which involves no feedback loops appears in figure 9. The DC component at the output of this AM detector is equal to the expectation of the absolute value of the signal plus noise

$$e_o = E\left\{\left| S(t) + N(t)\right|\right\} \tag{46}$$

which can be expressed as a function of the SNR[9]

$$e_o = \frac{A}{\sqrt{2\pi x}} \left[(1+2x)I_o(x) + 2xI_1(x)\right] e^{-x} \tag{47}$$

where x is equal to half the signal-to-noise power ratio, A is the peak amplitude of the sinusoidal carrier, and $I_o(x)$ and $I_1(x)$ are modified Bessel functions of the first kind. The theoretical DC component at the output of an absolute value AM detector as a function of SNR, calculated from equation (47) appears in figure 10 where the output has been normalized by dividing by the average absolute value of the sinusoidal carrier. This plot shows about a 10% error relative to the ideal AM detector at an SNR of 4 dB. Figure 10 also includes data for an experimental AM detector which will now be described.

The balanced modulator-demodulator is also a convenient circuit for implementing the average absolute value AM detector (at least for tape carrier frequencies which are assumed here) and the basic circuit (not including the low-pass filter) is shown in figure 11.

When the signal plus noise voltage exceeds the limiter threshold (with the polarities indicated in figure 11) transistors T_1 and T_4 are completely turned on and transistors T_2 and T_3 are completely turned off. The signal current flowing in transistor T_5 is positive and the signal current flowing in transistor T_6 is of equal value but negative.

$$I_1(t) = \frac{S(t) + N(t)}{R_E + 2r_e} \tag{48}$$

$$I_2(t) = -\frac{S(t) + N(t)}{R_E + 2r_e} \tag{49}$$

When the signal plus noise voltage is positive, it is seen that the positive signal current $I_1(t)$ flows through transistor T_1 and becomes load current $I_{L1}(t)$ and likewise the negative signal current $I_2(t)$ flows through transistor T_4 and becomes load current $I_{L2}(t)$. In a similar manner, when the signal plus noise voltage is negative (polarities opposite from those shown in figure 11) the conditions described above are reversed

[9]Thomas, J. B. *An Introduction to Communication Theory*, John Wiley & Sons, Inc., New York, p. 352, 1969.

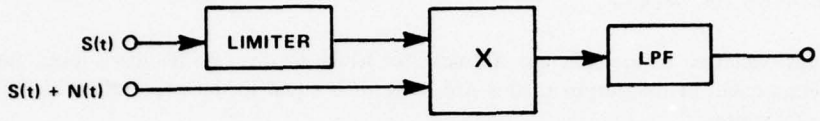


Figure 8. Coherent AM Detector.

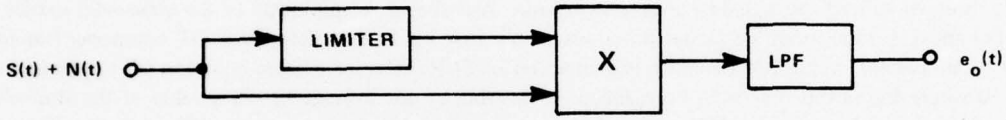


Figure 9. Average Absolute Value AM Detector.

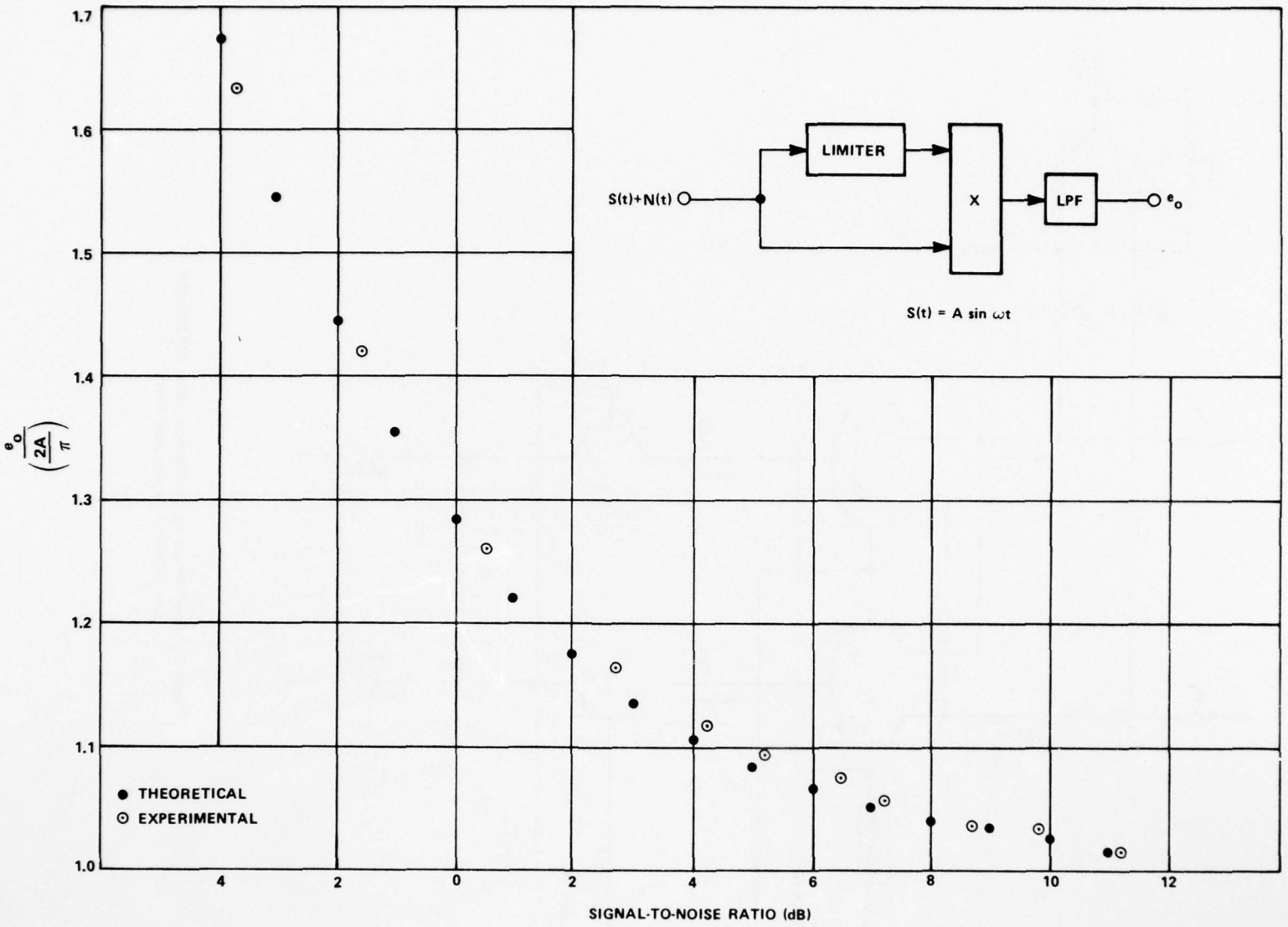


Figure 10. Theoretical and Experimental Data for the Absolute Value AM Detector.

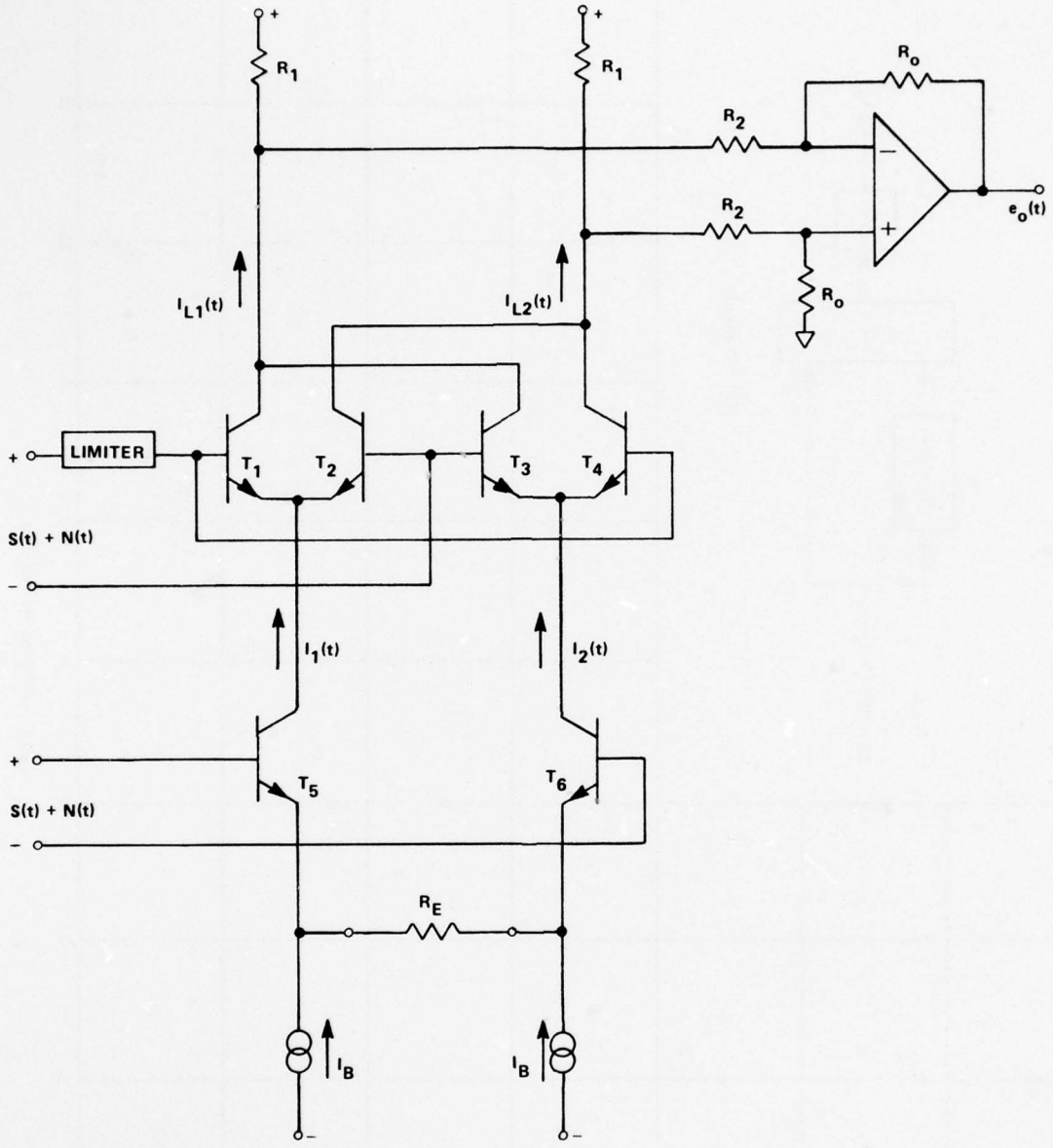


Figure 11. Basic Circuit for an Absolute Value AM Detector (not including the low pass filter).

and the positive signal current now flows through transistors T_6 and T_3 and again becomes load current $I_{L1}(t)$ and the negative signal current flows through transistors T_5 and T_2 to become $I_{L2}(t)$. From this it is seen that the load currents can be expressed in terms of the absolute values of the signal plus noise voltages

$$I_{L1}(t) = \frac{|S(t) + N(t)|}{R_E + 2r_e} \tag{50}$$

$$I_{L2}(t) = -\frac{|S(t) + N(t)|}{R_E + 2r_e} \tag{51}$$

The voltage at the output of the operational amplifier in terms of these load currents is given by

$$e_o(t) = \frac{R_1 R_o}{R_1 + R_2} \left[I_{L1}(t) - I_{L2}(t)\right] \tag{52}$$

When equations (50) and (51) are substituted into equation (52) the output voltage is obtained as a function of the absolute value of the signal plus noise voltage

$$e_o(t) = \left(\frac{2R_1 R_o}{R_1 + R_2}\right) \frac{|S(t) + N(t)|}{R_E + 2r_e} \tag{53}$$

In the absence of noise, the output is proportional to the absolute value (full wave rectified) of the sinusoidal carrier

$$|A \sin \omega t| = \frac{2A}{\pi}\left(1 + \frac{2}{3} \sin 2\omega t - \frac{2}{15} \sin 4\omega t + \cdots\right) \tag{54}$$

which has a DC component plus spectral components at integral multiples of twice the carrier frequency. When these higher frequency components are filtered out, the output voltage (in the absence of noise) is seen from equations (53) and (54) to be directly proportional to the amplitude of the sinusoidal carrier

$$e_o = \frac{4R_1 R_o A}{\pi(R_1 + R_2)(R_E + 2r_e)} \tag{55}$$

The constant of proportionality here is not absolutely constant since the dynamic emitter resistance r_e is a function of the absolute temperature T

$$r_e = \frac{kT}{qI_B} \tag{56}$$

However, this effect can usually be minimized by choosing R_E large compared to r_e (r_e is only 26Ω at 25°C for each mA of bias current I_B).

When a bandpass of noise is superimposed upon the carrier, the effect of the circuit in figure 11 is to translate both signal and noise down to baseband frequencies where the noise produces perturbations on the output depending on the bandwidth of the low-pass filter used.

It is assumed that the limiter in figure 11 has sufficient gain to switch the differential amplifiers completely on or off for input signals which are small compared to the nominal input. Satisfactory switching occurs (with a device such as the MC1596) for input differential voltages of 100 mV or more. Thus, for tape carrier signals with a nominal value of 1 VRMS a satisfactory dynamic range is achieved without additional voltage amplification. A complete AM detector circuit designed for a 900-kHz carrier frequency and incorporating a three-pole, low-pass, linear phase filter with a -3-dB bandwidth of 200 kHz appears in figure 12. An explanation of the procedure for incorporating the LC filter into this differential circuit is given in Appendix B. The gain of the circuit in figure 12 was set such that for a sinusoidal input signal the output is equal to the average absolute value ($\frac{2A}{\pi}$) of the input signal. For $R_1 = R_2$, it is seen from equation (55) that this results when R_o equals $R_E + 2r_e$ (in figure 12 $R_E = R_o$ since $2r_e$ is less than 1% of R_o).

For the application shown in figure 4 the AM detector should have a step response with little or no overshoot. This is true since the Log Amp output is forced to its limit if the input passes through zero voltage. An RC rather than an LC filter can be used if desired to guarantee a monotonic step response. With regard to combiner performance, however, a small overshoot of the AM detector step response is probably not serious since the effect is to cut off the weaker channel at a faster rate when a deep fade occurs. Good analog Log Amps are available and their design will not be discussed here. The main concern is that a bandwidth of at least 150 kHz be maintained over a dynamic range of about 30 dB (the Teledyne-Philbrick 4350 with a nominal bias current of 0.1 mA performs satisfactorily in this application).

The circuitry at the carrier input (pin 7) of figure 12 satisfies several important functions. First, the bias voltage plus dynamic signal at pin 6 in conjunction with the dynamic signal at pin 7 must be such that the transistors of the upper differential amplifiers are not saturated. The diodes from pin 7 to ground in conjunction with the 1-kΩ series resistor serve the function of limiting the signal voltage amplitude at pin 7 which reduces carrier feedthrough to the output by capacitive coupling. The bias voltage at pin 6 in this circuit is set by resistor R_B and the calculation and justification of this biasing resistor is covered at the end of Appendix B. The 1-mH inductor from pin 7 to ground prevents attenuation at low signal levels (below diode conduction level) and thus extends the circuit's dynamic range (measured to be less than 10 mV departure from a straight line down to 20-mV RMS). The inductor also provides a low resistance path to ground for the transistor base bias currents. The design details for this input circuit are provided in Appendix C.

There are two additional considerations that set a limit on the maximum peak voltage at the input to the circuit in figure 12. First, the transistors in the lower differential amplifier and the current source transistors must not saturate on peak input voltages. Second, for good linearity the peak input voltage V_p should not exceed the product of the bias current and the common emitter resistor

$$V_p \leq I_B R_E \tag{57}$$

For the circuit in figure 12 these limitations are satisfied for peak input voltages up to ±5 volts.

PHASE-LOCKED LOOP AND FREQUENCY DOWN CONVERTER CIRCUITRY

An experimental investigation of the phase-locked loop in the combiner application was conducted.[4] Three phase detector configurations were evaluated in a type 2 second-order system: the multiplier, with a sinusoidal phase detector characteristic; the exclusive-OR gate, with a triangular characteristic; and the set-reset flip-flop, with a sawtooth characteristic. The phase detector range of the multiplier and exclusive-OR gate is ±90° while it is ±180° for the set-reset flip-flop. The set-reset flip-flop has the added advantage that it produces a DC component proportional to the frequency difference between the two input signals which eliminates the need for frequency acquisition circuitry. Of these three phase detectors, the

[4]Novak, M. E. "An Investigation of Phase Lock Loop Requirements in Diversity Combiners," Master's thesis, California State University, Northridge, Calif., 1977.

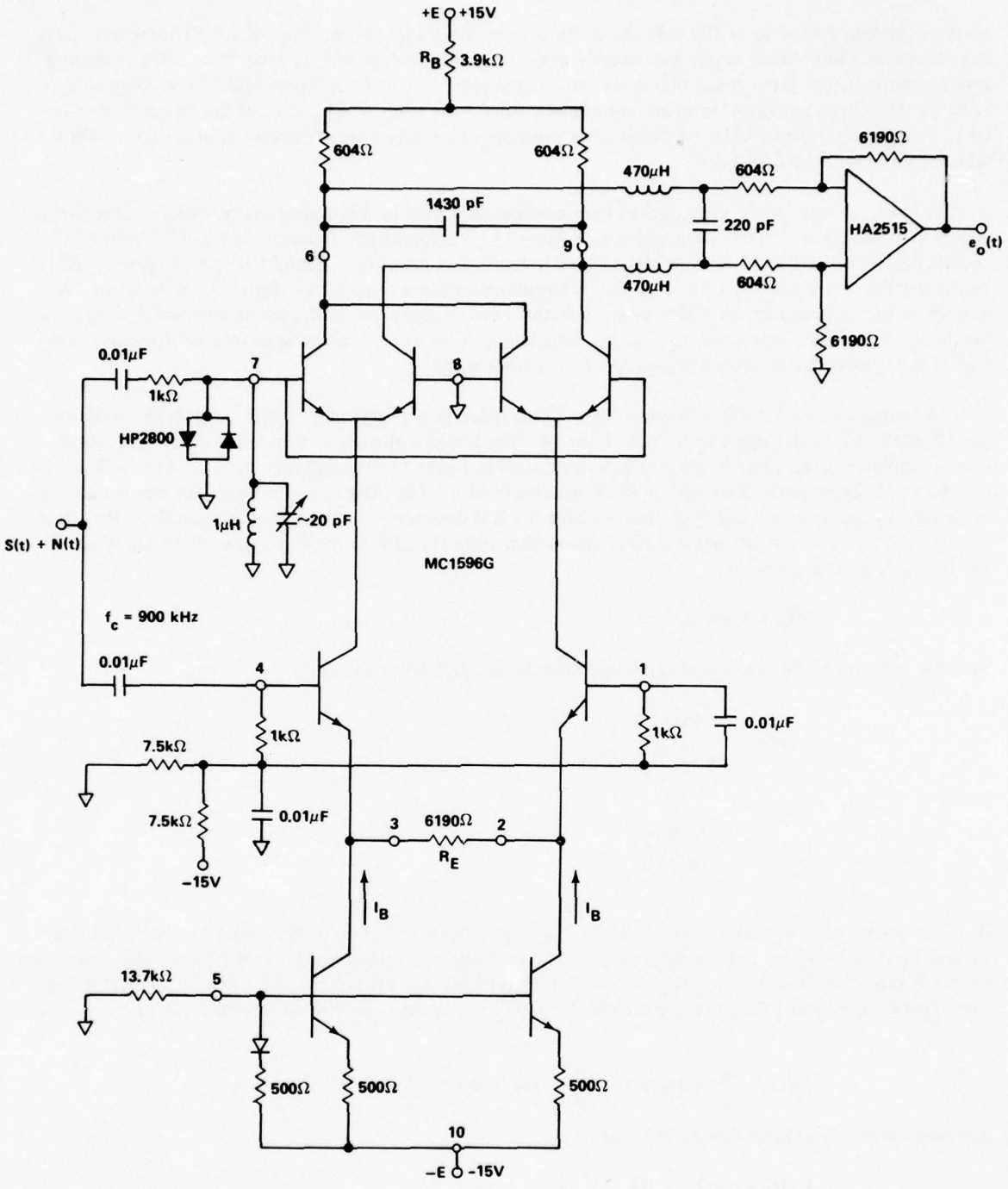


Figure 12. Complete Schematic of an Absolute Value AM Detector for a 900-kHz Carrier and Incorporating a 200-kHz Low Pass Filter.

set-reset flip-flop proved to be the best choice for the combiner application. The MC12040 three-state phase detector (with $\pm 360^{o}$ linear range) was recently evaluated and found to be unsuitable since extra or missing zero crossings of the carrier signal plus noise results in slipped cycles of the phase-locked loop. Slipped cycles cause the two input signals to be added out-of-phase for a short time, which increases the probability of bit errors in the output data. Extra or missing zero crossings cause only a small increase in phase error with the set-reset flip-flop phase detector.

A block diagram of the phase-locked loop configuration used in this evaluation, as well as in the experimental combiner study[3,5,6] to date, appears in figure 13. The phase and frequency control is effected in conjunction with the 10-MHz to 900-kHz frequency translation circuitry. Schmitt trigger circuits are used to convert the sinusoidal tape carriers to the rectangular waveforms required by digital phase detectors. As a result of this requirement, all digital phase detectors have the potential of producing an error component at low SNR. This occurs when it is possible for the additive noise to produce extra or missing threshold crossings of the Schmitt trigger within any cycle of the carrier signal.

A frequency down converter with sufficient conversion gain to translate typical 10-MHz IF signals to the 1V RMS tape carrier signal appears in figure 14. The low-pass filter is incorporated with a differential output amplifier as was done in the AM detector circuit in figure 12 (see appendix B). The LPF in figure 14 is a three-pole linear phase filter with a -3-dB bandwidth of 2 MHz. The conversion gain for this circuit can be derived by an argument similar to that used for the AM detector. First consider the gain from the signal input to the Op Amp output, not including attenuation from the LPF or the finite gain of the Op Amp. If the IF input signal is given by

$$S(t) = A \sin \omega_s t \tag{58}$$

then the collector signal currents of the lower differential amplifier are equal to

$$I_1(t) = \frac{A \sin \omega_s t}{R_E + 2r_e} \tag{59}$$

$$I_2(t) = - \frac{A \sin \omega_s t}{R_E + 2r_e} \tag{60}$$

If it is assumed that the carrier input signal $e_c(t)$ is a squarewave of sufficient amplitude to switch transistors T_1 and T_4 completely on and transistors T_2 and T_3 completely off when $e_c(t)$ is positive (and vice versa when $e_c(t)$ is negative) then the current $I_{L1}(t)$ consists of $I_1(t)$ when $e_c(t)$ is positive and $I_2(t)$ when $e_c(t)$ is negative. This is equivalent to multiplying the current $I_1(t)$ by a squarewave with an amplitude of ± 1

$$e_c(t) = \frac{4}{\pi} \left(\cos \omega_c t - \frac{1}{3} \cos 3 \omega_c t + \frac{1}{5} \cos 5 \omega_c t - \cdots \right) \tag{61}$$

The load current $I_{L1}(t)$ can thus be expressed by

$$I_{L1}(t) = e_c(t) \cdot I_1(t) \tag{62}$$

[3]Hill, E. R. "AM/AGC Weighted Pre-Detection Diversity Combining," in *Proceedings of International Telemetering Conference*, Vol. 13, pp. 215-238, Oct 1977.

[5]Vandenberg AFB. *Diversity Combiner A-M/AGC Control Technique.* Vandenberg AFB, Calif., Space and Missile Test Center, 1976. (Report No. PA 100-76-48)

[6]------. *A-M/AGC Combiner.* Vandenberg AFB, Calif., 1976. (Report No. PA 100-76-68)

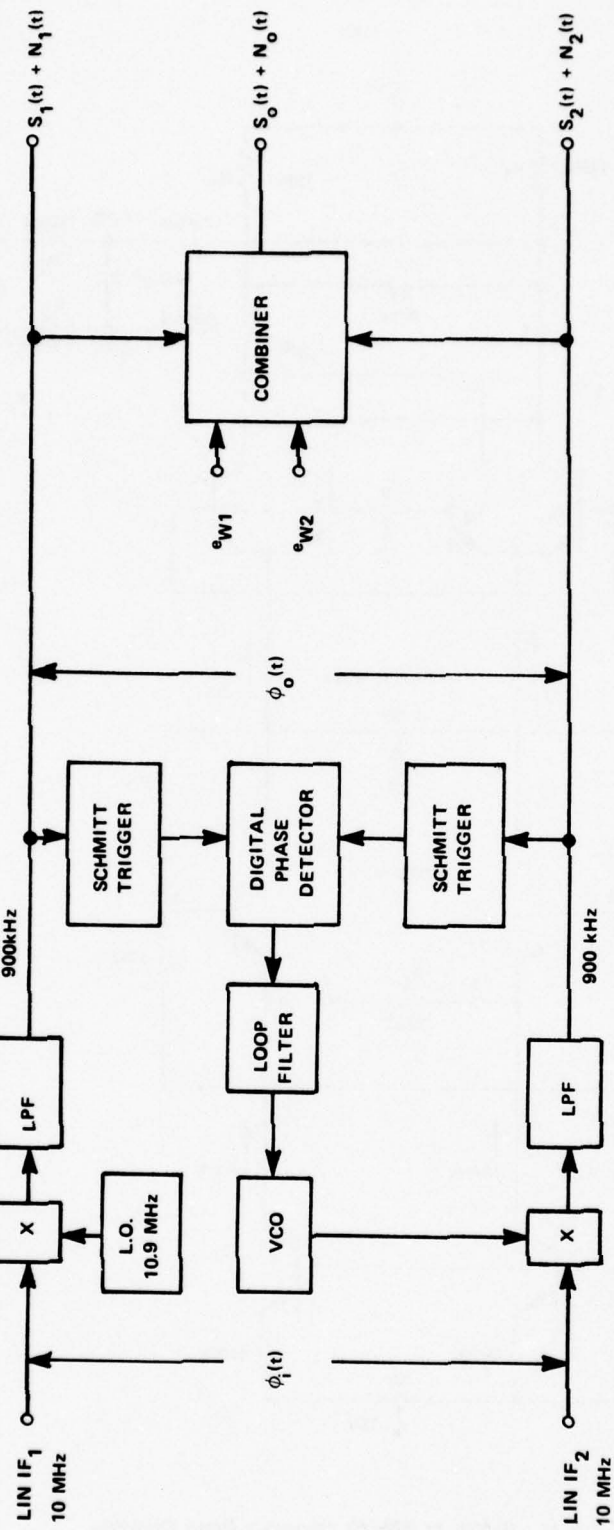


Figure 13. Block Diagram of Frequency Down Converters and Phase-Locked Loop.

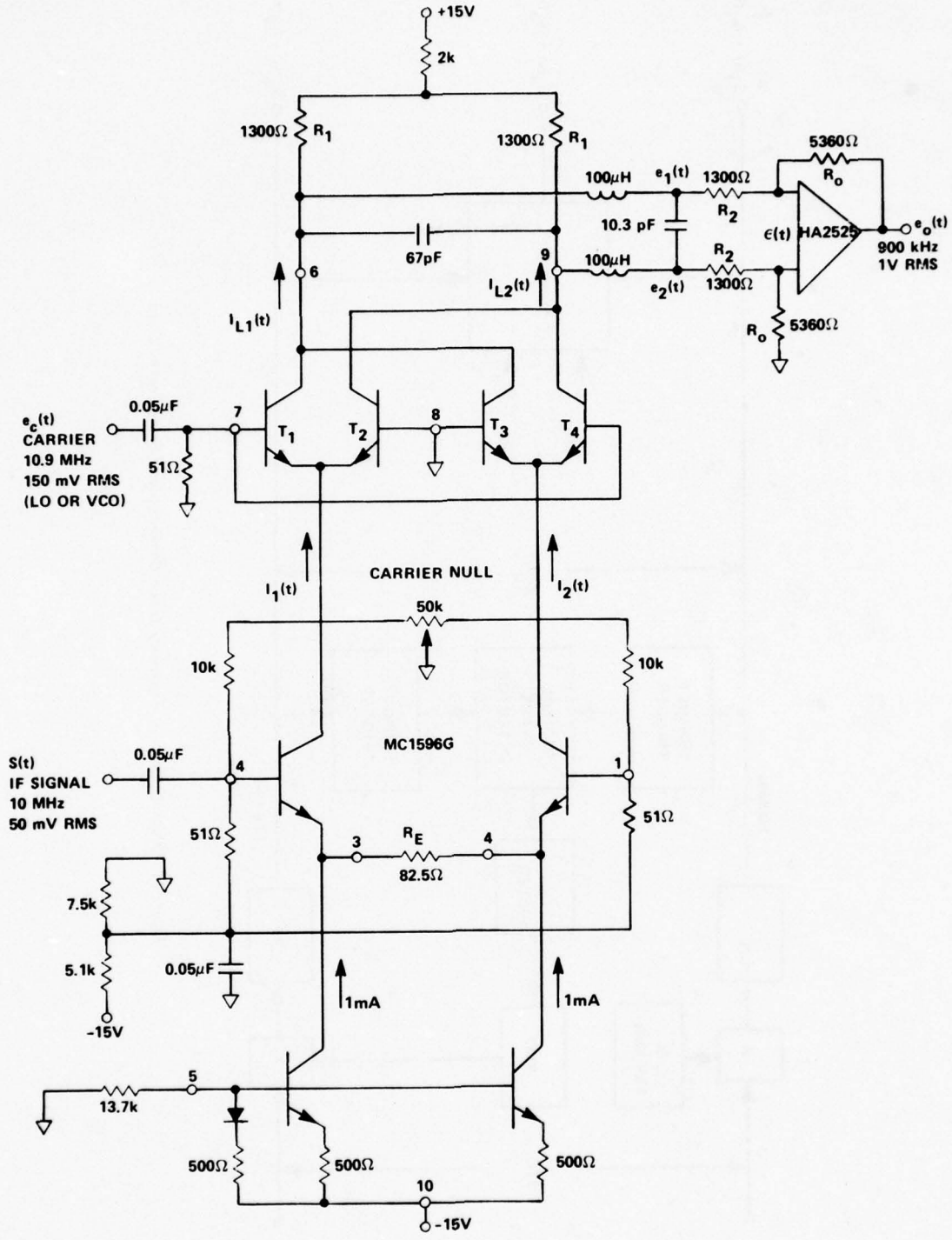


Figure 14. 10-MHz to 900-kHz Frequency Down Converter.

which produces spectral components at $\omega_c \pm \omega_s$, $3\omega_c \pm \omega_s$, $5\omega_c \pm \omega_s$, etc. The only component that falls within the LPF bandwidth arises from the product of the first-order terms

$$\sin \omega_s t \cos \omega_c t = \frac{1}{2} \sin (\omega_c - \omega_s)t + \frac{1}{2} \sin (\omega_c + \omega_s)t \tag{63}$$

and here only the difference frequency term $\omega_c - \omega_s$ falls within the LPF bandwidth. With these considerations it is seen from equations (59), (61), and (62) that the only component of load current $I_{L1}(t)$ that will influence the Op Amp output voltage $e_o(t)$ is given by

$$I_{L1}(t) = \frac{2A}{\pi(R_E + 2r_e)} \sin \omega t \tag{64}$$

where

$$\omega = \omega_c - \omega_s \tag{65}$$

Since the load current $I_{L2}(t)$ differs from $I_{L1}(t)$ only in polarity, therefore,

$$I_{L2}(t) = - \frac{2A}{\pi(R_E + 2r_e)} \sin \omega t \tag{66}$$

and the Op Amp output voltage $e_o(t)$ is given from equation (52) by

$$e_o(t) = \frac{4R_1 R_o A}{\pi(R_1 + R_2)(R_E + 2r_e)} \sin \omega t \tag{67}$$

Equation (67) was derived on the assumption that the carrier input was a squarewave. When a sinusoidal carrier is used, the gain is a function of the carrier amplitude. This is true since switching between currents $I_1(t)$ and $I_2(t)$ occurs over a finite period of time which has the effect of reducing the gain. For a sinusoidal carrier of 150-mV RMS (about the optimum value for best carrier suppression for the MC1596), the conversion gain is given approximately by the expression

$$e_o(t) = \frac{R_1 R_o A}{(R_1 + R_2)(R_E + 2r_e)} \sin \omega t \tag{68}$$

The conversion gain of the circuit in figure 14 was set by use of equation (68) to give 1-V RMS output for 50-mV RMS input (neglecting the attenuation of the LPF and Op Amp).

The carrier null circuit shown in figure 14 operates to equalize the average collector currents in the lower differential amplifier; however, in this circuit any carrier feedthrough is also attenuated by 33 dB by the LPF.

A good approximation to the Op Amp attenuation (at the output frequency) can be obtained from a single pole model, since most wide-band Op Amps have one dominant pole. In terms of the symbols used in figure 14, the Op Amp transfer function in operational notation thus becomes

$$\frac{e_o(s)}{\epsilon(s)} = -\frac{A_o\omega_o}{s + \omega_o} \tag{69}$$

where

A_o = Op Amp open loop gain (@ ω = o)

ω_o = Op Amp open loop -3 dB bandwidth $\left(\frac{\text{rad}}{\text{sec}}\right)$

s = Laplace transform variable

In terms of the signal voltages at the output of the LPF in figure 14 (see Appendix B) the transfer function of the Op Amp differential amplifier is

$$T(S) = \frac{e_o(s)}{e_1(s)-e_2(s)} = -\frac{\frac{R_o}{R_2}\left(\frac{R_2}{R_2 + R_o}\right)A_o\omega_o}{s + \left(\frac{R_2}{R_2 + R_o}\right)A_o\omega_o} \tag{70}$$

provided that $A_o >> \frac{R_2 + R_o}{R_2}$

The steady state amplitude and phase response are thus

$$\left|T(j\omega)\right| = \frac{\left(\frac{R_o}{R_2}\right)}{\sqrt{1 + \left(\frac{\omega}{\omega_3}\right)^2}} \tag{71}$$

and

$$\phi = -\tan^{-1}\left(\frac{\omega}{\omega_3}\right) \tag{72}$$

where ω_3 is the -3-dB bandwidth

$$\omega_3 = \left(\frac{R_2}{R_2 + R_o}\right)A_o\omega_o \tag{73}$$

and where

$$A_o\omega_o = \sqrt{2}\ \text{(gain-bandwidth product)} \tag{74}$$

The gain-bandwidth product of the HA2525 shown in figure 14 is about 20 MHz which, from equation (73), gives a -3-dB bandwidth of 5.5 MHz and an attenuation from equation (71) at 900 kHz of about 0.1 dB. For a frequency deviation of ±200 kHz, equation (72) gives a peak-to-peak phase variation of less than 5°.

A functional equivalent of the block diagram in figure 13 appears in figure 15 in terms of the transfer functions of the three basic components: the phase detector, the loop filter, and the voltage-controlled oscillator (VCO). These three components will be briefly described before considering the closed-loop characteristics and parameter values relative to performance.

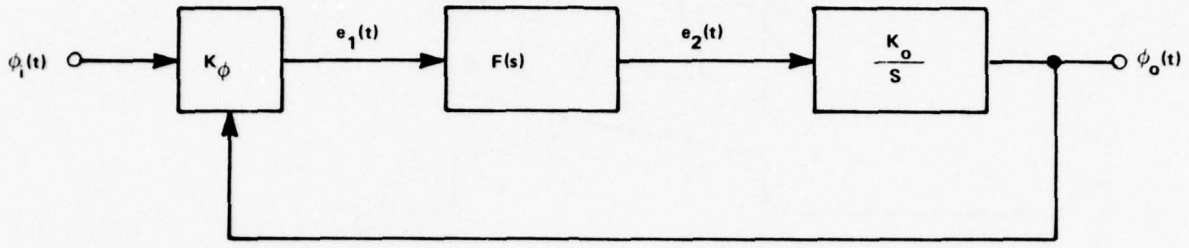


Figure 15. Functional Block Diagram of the Phase-Locked Loop.

The schematic of a set-reset flip-flop phase detector including the Schmitt trigger wave shaping circuits appears in figure 16. This circuit was implemented with emitter coupled logic (ECL) devices. The MC1035 with appropriate positive feedback (see MECL Integrated Circuit Data Books) implements a high-speed Schmitt trigger with a hysteresis of about 20 mV. The MC1024 was used to implement the set-reset flip-flop with the set and reset pulses provided by the differentiated outputs of the Schmitt trigger circuits. The input circuitry preceding the Schmitt triggers of figure 16 serves the same function (see Appendix C) as in the AM detector circuit of figure 12. The Schmitt trigger outputs are taken from complementary pins of the MC1035. This produces a squarewave at the output of the set-reset flip-flop when the tape carrier inputs $S_1(t)$ and $S_2(t)$ are in phase. Thus, the average output $e_1(t)$ of the phase detector will equal the midvoltage V_{BB} of the ECL output when the input signals are in phase. Therefore, since the average output voltage will change linearly with phase error, the phase detector output can be expressed in terms of the symbols of figure 15 by

$$e_1(t) = V_{BB} + K_\phi\left[\phi_i(t) - \phi_o(t)\right] \tag{75}$$

By taking the Laplace transform of equation (75), the phase detector transfer function (which does not include initial conditions) is obtained

$$\frac{E_1(S)}{\phi_i(s) - \phi_o(s)} = K_\phi \tag{76}$$

Since the average phase detector output will increase from V_{BB} to the ECL logic "1" level E_1 for an increase in phase error from zero to π radians, the phase detector constant K_ϕ can be evaluated from

$$K_\phi = \frac{E_1 - V_{BB}}{\pi} \tag{77}$$

in units of volts per radian.

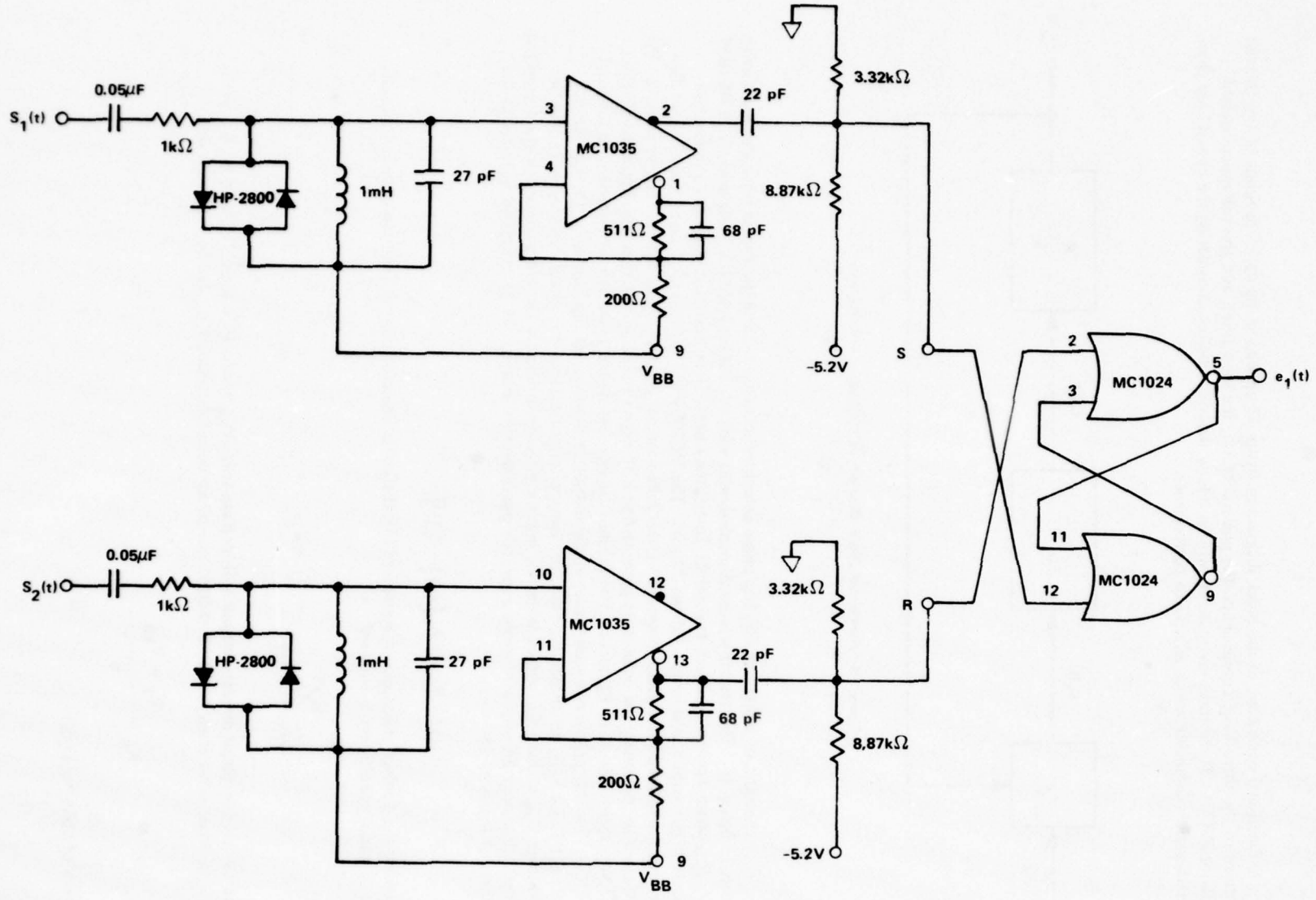


Figure 16. Set -- Reset Flip-Flop Digital Phase Detector.

An idealized expression for the output frequency $\omega(t)$ of a VCO in terms of the input voltage $e_2(t)$ is given by

$$\omega(t) = \frac{d\phi_o(t)}{dt} = \omega_c + K_o\, e_2(t) \tag{78}$$

where ω_c is the center frequency (for zero control voltage) and K_o is the sensitivity in radians per second per volt. By taking the Laplace transform of equation (78) the VCO transfer function is obtained

$$\frac{\phi_o(s)}{E_2(s)} = \frac{K_o}{s} \tag{79}$$

The closed-loop transfer function of the phase error with respect to the input phase can be obtained in terms of the loop filter transfer function

$$\frac{E_2(s)}{E_1(s)} = F(s) \tag{80}$$

by the simultaneous solution of equations (76), (79), and (80)

$$\frac{\phi_\epsilon(s)}{\phi_i(s)} = \frac{s}{s + K_\phi K_o F(s)} \tag{81}$$

where

$$\phi_\epsilon(s) = \phi_i(s) - \phi_o(s) \tag{82}$$

The active loop filter in figure 17 with the idealized transfer function

$$F(s) = \frac{\frac{R_2}{R_1}\left(s + \frac{1}{R_2 C}\right)}{s} \tag{83}$$

makes possible a type 2 second-order transfer function. By substituting equation (83) into equation (81), the complete transfer function of output phase error with respect to input phase is obtained

$$\frac{\phi_\epsilon(s)}{\phi_i(s)} = \frac{s^2}{s^2 + \left(\frac{K_\phi K_o R_2}{R_1}\right) s + \frac{K_\phi K_o}{R_1 C}} \tag{84}$$

which can be expressed in terms of the damping factor ζ and undamped natural frequency ω_n

$$\frac{\phi_\epsilon(s)}{\phi_i(s)} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n{}^2} \tag{85}$$

By equating the coefficients of s and the constant terms in equations (84) and (85), two equations are obtained which can be solved for R_2 and C as functions of R_1 and the constants and parameters of the phase-locked loop

$$R_2 = \frac{2\zeta\omega_n R_1}{K_\phi K_o} \tag{86}$$

$$C = \frac{K_\phi K_o}{\omega_n{}^2 R_1} \tag{87}$$

Values for R_2 and C can be calculated from equations (86) and (87) after determining appropriate values for parameters ζ and ω_n. An experimental study[4] with PCM(NRZ-L) [pulse code modulation (non-return-to-zero-level)] baseband signals has shown that the damping factor ζ for the diversity combiner application is not critical; with a value of $1/\sqrt{2}$ being an appropriate choice. Extensive plots are also available [10,11,12] of the transient response and noise performance of the phase-locked loop as a function of damping factor. After a choice of damping factor has been made, the undamped natural frequency ω_n can be obtained[13] from a function of the damping factor ζ and the -3-db bandwidth ω_{3dB} (based on output phase with respect to input phase)

$$\omega_n = \frac{\omega_{3dB}}{\left[2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}\right]^{1/2}} \tag{88}$$

which for $\zeta = 1/\sqrt{2}$ reduces to

$$\omega_n = \frac{\omega_{3dB}}{2.06} \tag{89}$$

The choice of ω_{3dB} in the combiner application is a compromise between noise performance and performance with high-frequency phase dynamics. The experimental study[4] found a value of about 10 kHz to be a good compromise.

It is often necessary to limit the dynamic range of the voltages at the output of the active loop filter in figure 17 and/or to limit the frequencies reaching the Op Amp in this filter. This can be accomplished by dividing resistor R_1 in half and inserting a bypass capacitor as shown in figure 18. To avoid altering the phase-locked loop characteristics, the cutoff frequency $\left(\frac{4}{R_1 C_1}\right)$ of this network should be at least an order of magnitude larger than ω_n. Experience has shown, however, that with the set-reset flip-flop phase detector this cutoff frequency may need to be much wider to prevent the VCO from locking at frequencies other than the input frequency. The set-reset flip-flop phase detector is prone to this problem since for certain difference frequency and phase combinations the average output voltage can deviate greatly from the monotonic trend of average

[4] Novak, M. E. "An Investigation of Phase Lock Loop Requirements in Diversity Combiners," Master's thesis, California State University, Northridge, Calif., 1977.

[10] Blanchard, A. *Phase-Locked Loops – Application to Coherent Receiver Design,* John Wiley & Sons, Inc., New York, 1976.

[11] Viterbi, A. J. *Principles of Coherent Communications,* McGraw-Hill Book Co., New York, 1966.

[12] Lindsey, W. C. *Synchronization Systems in Communications and Control,* Prentice-Hall, Inc., Englewood Cliffs, N.J., 1972.

[13] Gardner, F. M. *Phaselock Techniques.* John Wiley & Sons, Inc., New York, p. 11, 1967.

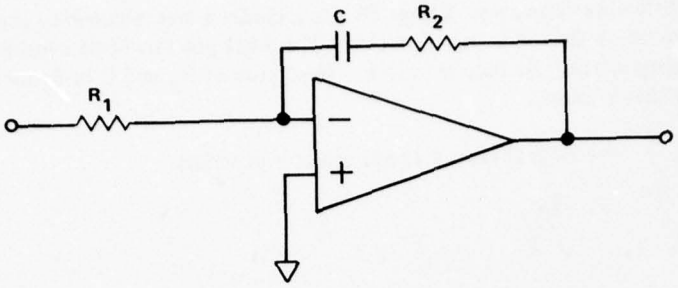


Figure 17. Active Loop Filter.

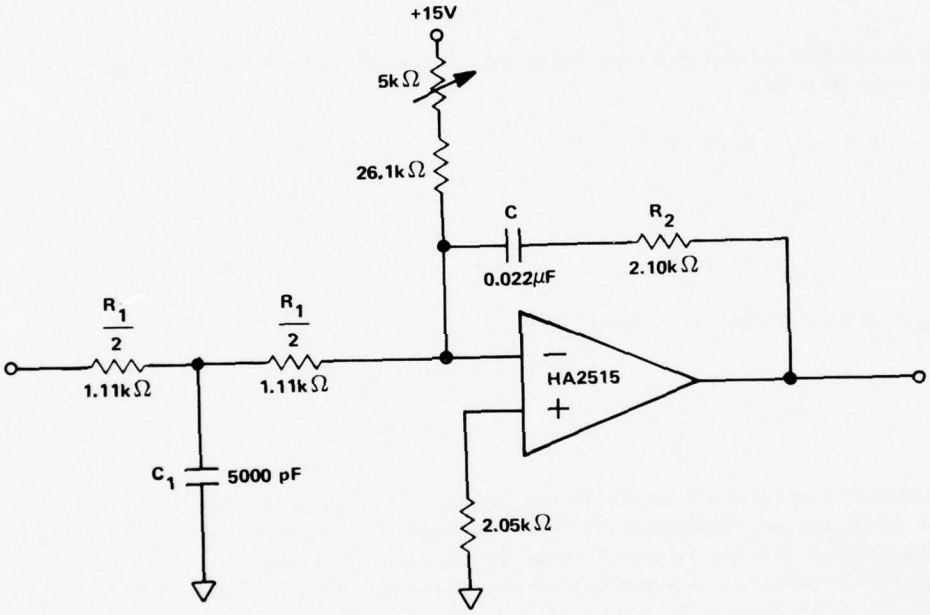


Figure 18. Active Loop Filter for Use With Phase Detector in Figure 16.

output voltage versus difference frequency. Figure 18 also includes a bias network to compensate for the phase detector offset voltage indicated in equation (75). The 5-kΩ pot should be adjusted for a squarewave at the phase detector output when the loop is in lock. The values of R_2 and C in figure 18 were calculated from the following parameter values

$$R_1 = 2.22\text{k}\Omega \text{ (two 1.11-k}\Omega \text{ resistors in series)}$$

$$\zeta = \frac{1}{\sqrt{2}}$$

$$\omega_{3dB} = 62.8 \times 10^3 \ \frac{\text{rad}}{\text{s}} \ (10 \text{ kHz})$$

$$K_o = 358 \times 10^3 \ \frac{\text{rad/s}}{\text{V}} \ \left(57 \ \frac{\text{kHz}}{\text{V}}\right)$$

$$K_\phi = 0.127 \ \frac{\text{V}}{\text{rad}}$$

where the phase detector constant K_ϕ was calculated from equation (77) for the following typical ECL logic levels and midpoint voltage

$$E_1 = -0.75\text{V}$$

$$E_o = -1.55\text{V}$$

$$V_{BB} = -1.15\text{V}$$

where V_{BB} is defined in terms of E_1 and E_o by

$$V_{BB} = \frac{E_1 + E_o}{2} \tag{90}$$

Equation (78) describes a VCO with perfect linearity (no variation of sensitivity K_o with control voltage), infinite bandwidth (output frequency responds instantaneously to changes in control voltage), and complete stability (no variation of output frequency except for changes in control voltage). The actual VCO requirements depend upon the phase-locked loop configuration and bandwidth. When in phase lock, the average frequency of the VCO in the configuration of figure 13 is nearly equal to that of the local oscillator (it is equal if common local oscillators are used in the receiver). Thus, the VCO is not required to track variations of the input frequency (due to transmitter drift, doppler shift, etc.) and needs a linear range sufficient only to handle the closed-loop dynamics. For this purpose an adequate linear range (with less than 20% variation of K_o) of the VCO is given by twice the peak phase detector output voltage times the high-frequency gain of the active loop filter times the VCO sensitivity

$$\Delta\omega_L = (E_1 - E_o)\left(\frac{R_2}{R_1}\right) K_o \tag{91}$$

where $\Delta\omega_L$ represents frequency deviation either side of the center frequency. Although linearity beyond $\Delta\omega_L$ is not critical, for proper frequency acquisition the VCO output frequency must be a monotonic function of the control voltage over the full range of control voltage from the active loop filter. A varactor

controlled LC oscillator is a good choice for most combiner applications and an example, designed for 10.9-MHz center frequency, appears in figure 19. The VCO bandwidth is determined by the input resistive bias network and the bypass capacitor C to ground. This bandwidth (-3 dB) is given (in radians per second) by

$$\omega_{VCO} = \frac{R_1 + R_2}{R_1 R_2 C} \tag{92}$$

and should be at least an order of magnitude greater than the phase-locked loop bandwidth ω_{3dB} expressed in equation (88). The primary function of the bypass capacitor C is to provide an AC ground return for the varactor diode (1N5464). The center frequency ω_c of the oscillator in figure 19 is set by grounding the input and adjusting the trimmer capacitor for 10.9 MHz at the output. The required short-term frequency stability (or phase noise bandwidth) of the VCO can be determined from the steady-state magnitude of the phase error transfer function in equation (84)

$$\left| \frac{\phi_\epsilon(j\omega)}{\phi_i(j\omega)} \right| = \frac{(\frac{\omega}{\omega_n})^2}{\sqrt{[1 - (\frac{\omega}{\omega_n})^2]^2 + 4\zeta^2 (\frac{\omega}{\omega_n})^2}} \tag{93}$$

This is a high-pass function with the -3-dB cutoff frequency at ω_n if the damping factor is equal to $1/\sqrt{2}$. A plot of this function appears in figure 20. Differential input phase variations at frequency ω will be attenuated according to this function. Since VCO phase jitter arising from oscillator instability is indistinguishable from the differential input phase errors, the VCO phase noise will be attenuated by the phase-locked loop by the function in equation (93). Thus the bandwidth of the VCO phase noise should be narrow compared to the frequency ω_n calculated from equation (88). The phase noise bandwidth of the VCO in figure 19 is less than 100 Hz and the sensitivity factor K_o changes less than 15% for a frequency deviation of ±100 kHz.

RESULTS

A two-channel AM/AGC weighted combiner has been constructed using the circuits described in this report and has been shown to outperform[3,5,6] a conventional AGC weighted combiner under both laboratory and operational conditions.

[3] Hill, E. R. "AM/AGC Weighted Pre-Detection Diversity Combining," in *Proceedings of International Telemetering Conference,* Vol. 13, pp. 215-238, Oct 1977.

[5] Vandenberg AFB. *Diversity Combiner A-M/AGC Control Technique.* Vandenberg AFB, Calif., Space and Missile Test Center, 1976. (Report No. PA 100-76-48)

[6] _____. *A-M/AGC Combiner.* Vandenberg AFB, Calif., 1976. (Report No. PA 100-76-68)

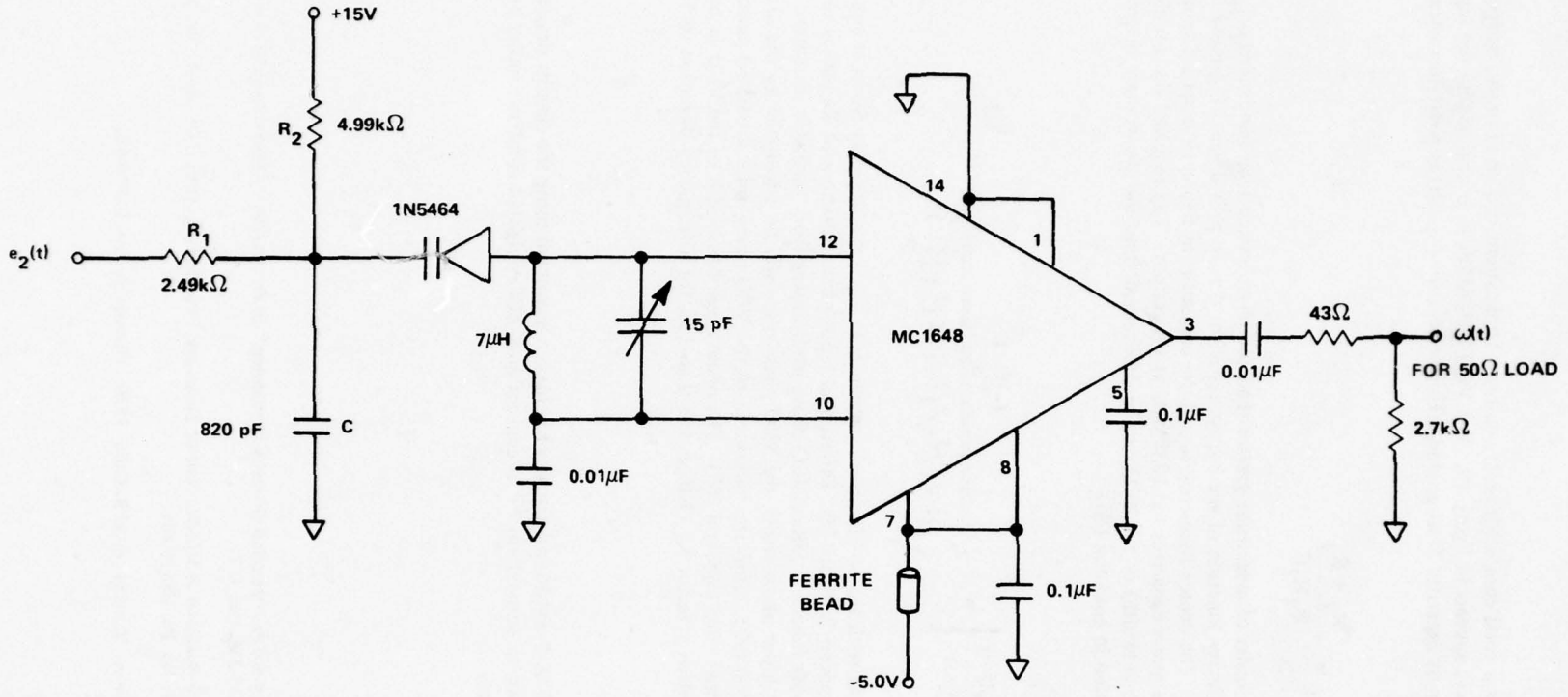


Figure 19. Varactor-Controlled LC Oscillator (VCO).

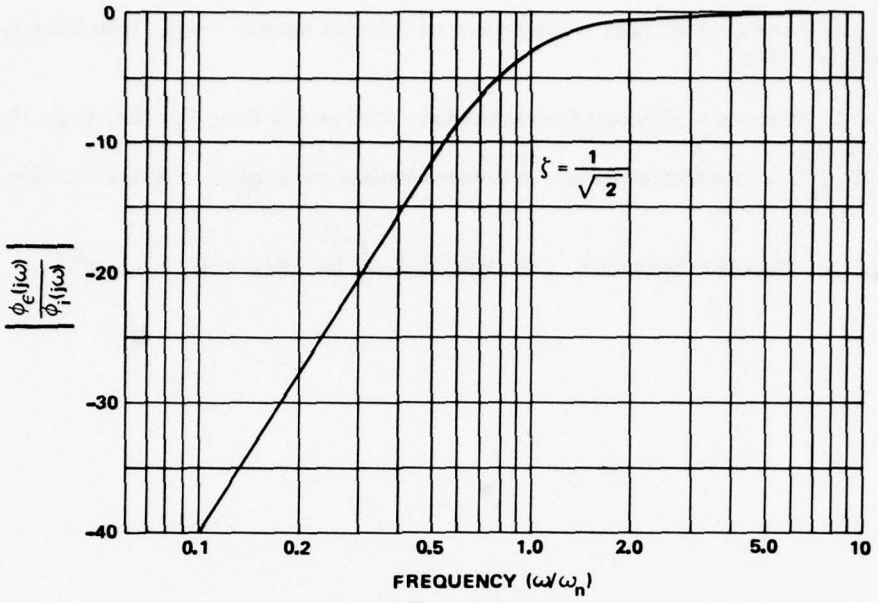


Figure 20. Steady-State Magnitude of Phase Error With Respect to Input Phase.

REFERENCES

1. Hill, E. R. "Time Domain Analysis of an AGC Weighted Combiner," in *Proceedings of International Telemetering Conference,* Vol. 9, pp. 475-494, Oct 1973.

2. Naval Missile Center. *Time Domain Analysis of an Automatic Gain Control Weighted Diversity Combining System,* by E. R. Hill. Point Mugu, Calif., NAVMISCEN, 14 Dec 1973. (Technical Publication TP-73-47) UNCLASSIFIED.

3. Hill, E. R. "AM/AGC Weighted Pre-Detection Diversity Combining," in *Proceedings of International Telemetering Conference,* Vol. 13, pp. 215-238, Oct 1977.

4. Novak, M. E. "An Investigation of Phase Lock Loop Requirements in Diversity Combiners," Master's thesis, California State University, Northridge, Calif., 1977.

5. Vandenberg AFB. *Diversity Combiner A-M/AGC Control Technique.* Vandenberg AFB, Calif., Space and Missile Test Center, 1976. (Report No. PA 100-76-48)

6. - - - - -. *A-M/AGC Combiner.* Vandenberg AFB, Calif., 1976. (Report No. PA 100-76-68)

7. Streich, R. G., D. E. Little, and R. B. Pickett. "Dynamic Requirements for Diversity Combiners," in *Proceedings of International Telemetering Conference,* Vol. 8, pp. 635-642, Oct 1972.

8. Brennan, D. G. "Linear Diversity Combining Techniques," in *Proceedings of Institute of Radio Engineers,* June 1959.

9. Thomas, J. B. *An Introduction to Communication Theory,* John Wiley & Sons, Inc., New York, p. 352, 1969.

10. Blanchard, A. *Phase-Locked Loops – Application to Coherent Receiver Design,* John Wiley & Sons, Inc., New York, 1976.

11. Viterbi, A. J. *Principles of Coherent Communications,* McGraw-Hill Book Co., New York, 1966.

12. Lindsey, W. C. *Synchronization Systems in Communications and Control,* Prentice-Hall, Inc., Englewood Cliffs, N. J., 1972.

13. Gardner, F. M. *Phaselock Techniques.* John Wiley & Sons, Inc., New York, p. 11, 1967.

APPENDIX A

COMBINER CIRCUIT FOR THREE OR MORE CHANNELS

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COMBINER CIRCUIT FOR THREE OR MORE CHANNELS

A three-channel diversity combiner will be described and the extension to any number of additional channels will be clear. The optimum three-channel combiner will be described and it will then be shown that the subject circuit is an accurate approximation to the ideal.

The output SNR of a three-channel combiner is given from equation (2) by

$$\frac{S_o}{N_o} = \frac{a_1S_1 + a_2S_2 + a_3S_3}{\sqrt{(a_1N_1)^2 + (a_2N_2)^2 + (a_3N_3)^2}} \tag{A-1}$$

which, from equation (3), is maximized when the weighting coefficients are

$$a_1 = \frac{S_1}{N_1{}^2} \tag{A-2}$$

$$a_2 = \frac{S_2}{N_2{}^2} \tag{A-3}$$

$$a_3 = \frac{S_3}{N_3{}^2} \tag{A-4}$$

where the quantities are defined as in the body of the report. It is possible to designate one channel as a reference and weight the other two with respect to it. For example, if the number three channel is selected as the reference, the new weighting coefficients (combining ratios) can be found by dividing numerator and denominator of equation (A-1) by a_3

$$\frac{S_o}{N_o} = \frac{\left(\frac{a_1}{a_3}\right)S_1 + \left(\frac{a_2}{a_3}\right)S_2 + S_3}{\sqrt{\left(\frac{a_1}{a_3}\right)^2N_1{}^2 + \left(\frac{a_2}{a_3}\right)^2N_2{}^2 + N_3{}^2}} \tag{A-5}$$

From equation (A-2), (A-3), and (A-4) these weighting coefficients become

$$\frac{a_1}{a_3} = \frac{S_1}{S_3}\frac{N_3^2}{N_1^2} \tag{A-6}$$

$$\frac{a_2}{a_3} = \frac{S_2}{S_3}\frac{N_3^2}{N_2^2} \tag{A-7}$$

or from equation (13) in terms of the receiver weighting signals

$$\frac{a_1}{a_3} = 10^{\frac{2}{K_1}\left(e_{w3} - e_{w1}\right)} \tag{A-8}$$

$$\frac{a_2}{a_3} = 10^{\frac{2}{K_1}\left(e_{w3} - e_{w2}\right)} \tag{A-9}$$

where

$$e_{w1} = e_{g1} - \log\left(\frac{e_{a1}}{V}\right) \tag{A-10}$$

$$e_{w2} = e_{g2} - \log\left(\frac{e_{a2}}{V}\right) \tag{A-11}$$

$$e_{w3} = e_{g3} - \log\left(\frac{e_{a3}}{V}\right) \tag{A-12}$$

A block diagram for this combiner configuration appears in figure A-1. The basic circuit used to approximate the weighting coefficients in equations (A-8) and (A-9) appears in figure A-2 where the subscript "r" denotes the reference channel and the subscript "i" denotes any other channel. The bias current I_{B2} in figure A-2 is employed to force the weighting coefficient of the circuit to approximate an exponential function as will be shown. The voltages at the bases of the differential amplifier in figure A-2 can be expressed in terms of the weighting signals and the bias current

$$e_{xi} = \left(\frac{R_2}{R_1 + R_2}\right) e_{wi} + \left(\frac{R_1 R_2}{R_1 + R_2}\right) I_{B2} \tag{A-13}$$

$$e_{xr} = \left(\frac{R_2}{R_1 + R_2}\right) e_{wr} \tag{A-14}$$

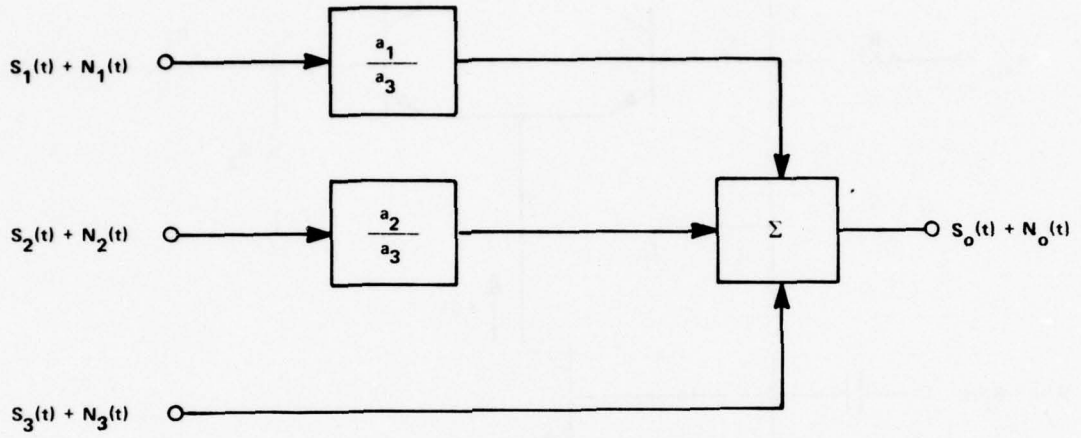

Figure A-1. Combiner Configuration with Channel 3 as the Reference Channel.

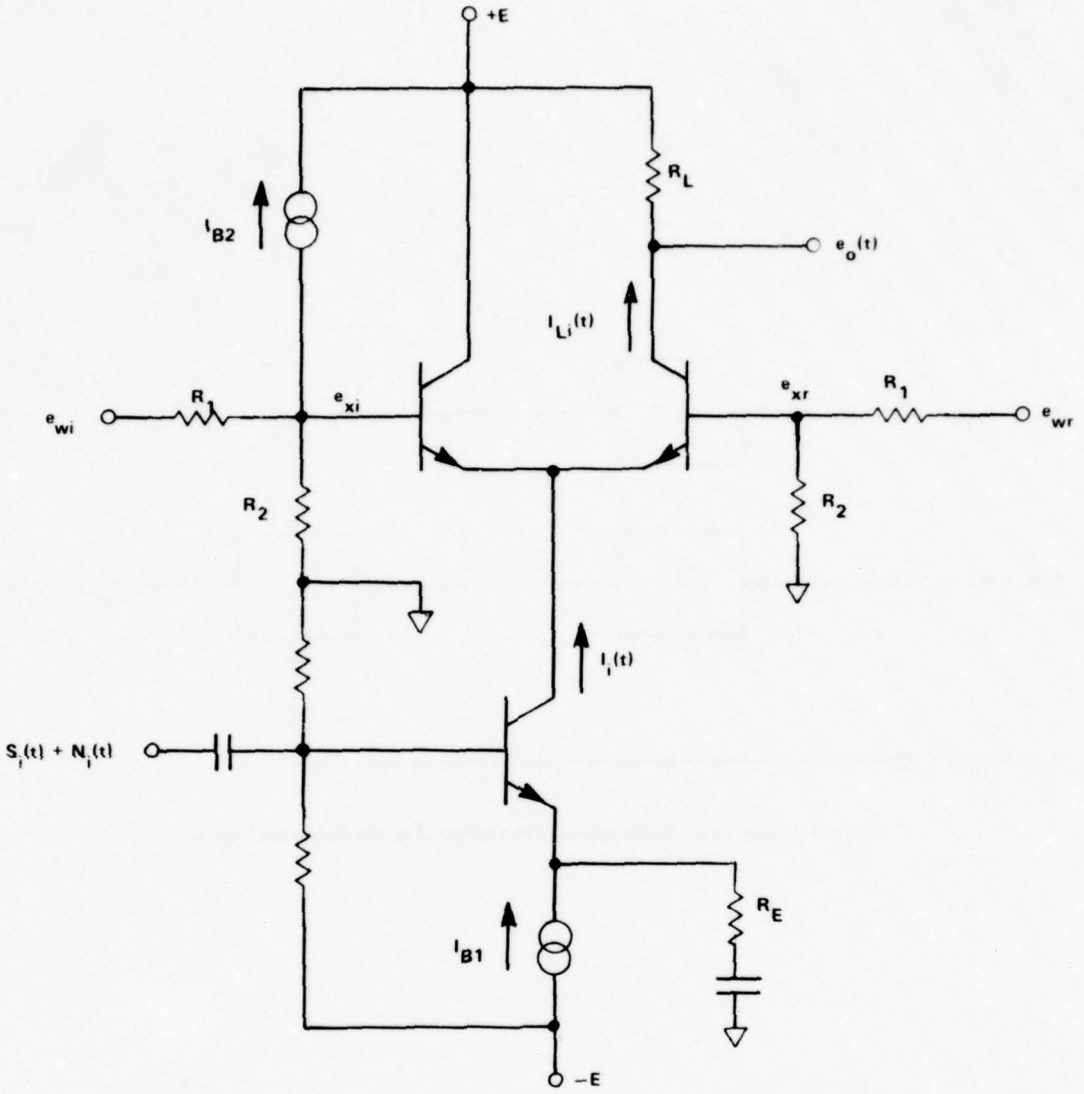

Figure A-2. Basic Circuit Element for Combining More Than Two Channels.

from which the differential base voltage is

$$\Delta e_x = e_{xr} - e_{xi} = \left(\frac{R_2}{R_1 + R_2}\right)(e_{wr} - e_{wi}) - E_B \tag{A-15}$$

where

$$E_B = \left(\frac{R_1 R_2}{R_1 + R_2}\right) I_{B2} \tag{A-16}$$

Referring to figure 5 and equations (22) and (23), it is seen that the signal and noise current to the load in figure A-2 can be written in terms of equation (A-15) as

$$I_{Li}(t) = \left(\frac{1}{1 + 10^{\frac{E_B}{K_3}} 10^{-\frac{R_2(e_{wr} - e_{wi})}{K_3(R_1 + R_2)}}}\right) I_i(t) \tag{A-17}$$

where

$$I_i(t) = \frac{S_i(t) + N_i(t)}{R_E} \tag{A-18}$$

By adjusting the bias current I_{B2} such that

$$10^{\frac{E_B}{K_3}} 10^{-\frac{R_2(e_{wr} - e_{wi})}{K_3(R_1 + R_2)}} >> 1 \tag{A-19}$$

equation (A-17) is closely approximated by

$$I_{Li}(t) = 10^{-\frac{E_B}{K_3}} 10^{\frac{R_2(e_{wr} - e_{wi})}{K_3(R_1 + R_2)}} I_i(t) \tag{A-20}$$

which is an exponential function of the differential weighting signal as required.

Examination of equations (7), (14), and (15) indicates that the channel with the larger RF signal level e_s, and thus the larger SNR, will also have the more negative weighting signal e_w. Thus, if the channel with the better SNR (most negative weighting signal) is always selected as the reference channel, the inequality in equation (A-19) reduces to

$$10^{\frac{E_B}{K_3}} >> 1 \tag{A-21}$$

The worst-case error in this approximation is about 2% for T = 298°K and E_B = 100 mV.

Three circuits similar to the one in figure A-2 can be coupled with their output currents linearly summed in a common load resistor as in figure A-3. Selection of the reference weighting signal is accomplished with diode D_2 in series with each weighting signal on the right side of figure A-3. The input points of the weighting signal resistive networks on the right side are common, which dictates that the voltage at this point will be determined by the channel with the more negative weighting signal (and thus the greater SNR). The diode D_1 in series with each weighting signal on the left side of figure A-3 compensates for the drop across diode D_2 on the right side. Resistors R_3 and R_4 provide bias currents for diodes D_1 and D_2 to equalize and stabilize the voltage drops across these diodes.

The total output signal voltage across the common load resistor is equal to the product of this resistor and the sum of the output currents given by equation (A-20).

$$e_{RL}(t) = R_L\left[I_{L1}(t) + I_{L2}(t) + I_{L3}(t)\right] \tag{A-22}$$

By substituting equations (A-18) and (A-20) into equation (A-22), this output voltage becomes

$$e_{RL}(t) = \frac{R_L}{R_E}\ 10^{-\frac{E_B}{K_3}}\left[a_1S_1(t) + a_1N_1(t) + a_2S_2(t) + a_2N_2(t) + a_3S_3(t) + a_3N_3(t)\right] \tag{A-23}$$

where

$$a_1 = 10^{\frac{R_2(e_{wr} - e_{w1})}{K_3(R_1 + R_2)}} \tag{A-24}$$

$$a_2 = 10^{\frac{R_2(e_{wr} - e_{w2})}{K_3(R_1 + R_2)}} \tag{A-25}$$

$$a_3 = 10^{\frac{R_2(e_{wr} - e_{w3})}{K_3(R_1 + R_2)}} \tag{A-26}$$

Note that the coefficient in equations (A-24), (A-25), and (A-26) corresponding to the channel with the better SNR will be unity. The other two coefficients will be less than unity in the proper amount to maximize the output SNR (within the accuracy determined by the inequality in equation (A-21)).

The bias current I_{B2} can normally be introduced by a fixed resistor since the voltages at the bases of the differential amplifiers are small compared to the power supply voltage. The attenuation introduced by this bias current is given by the second factor in equation (A-23) and can be compensated for by proper choice of resistors R_L and R_E as indicated by the first factor in equation (A-23).

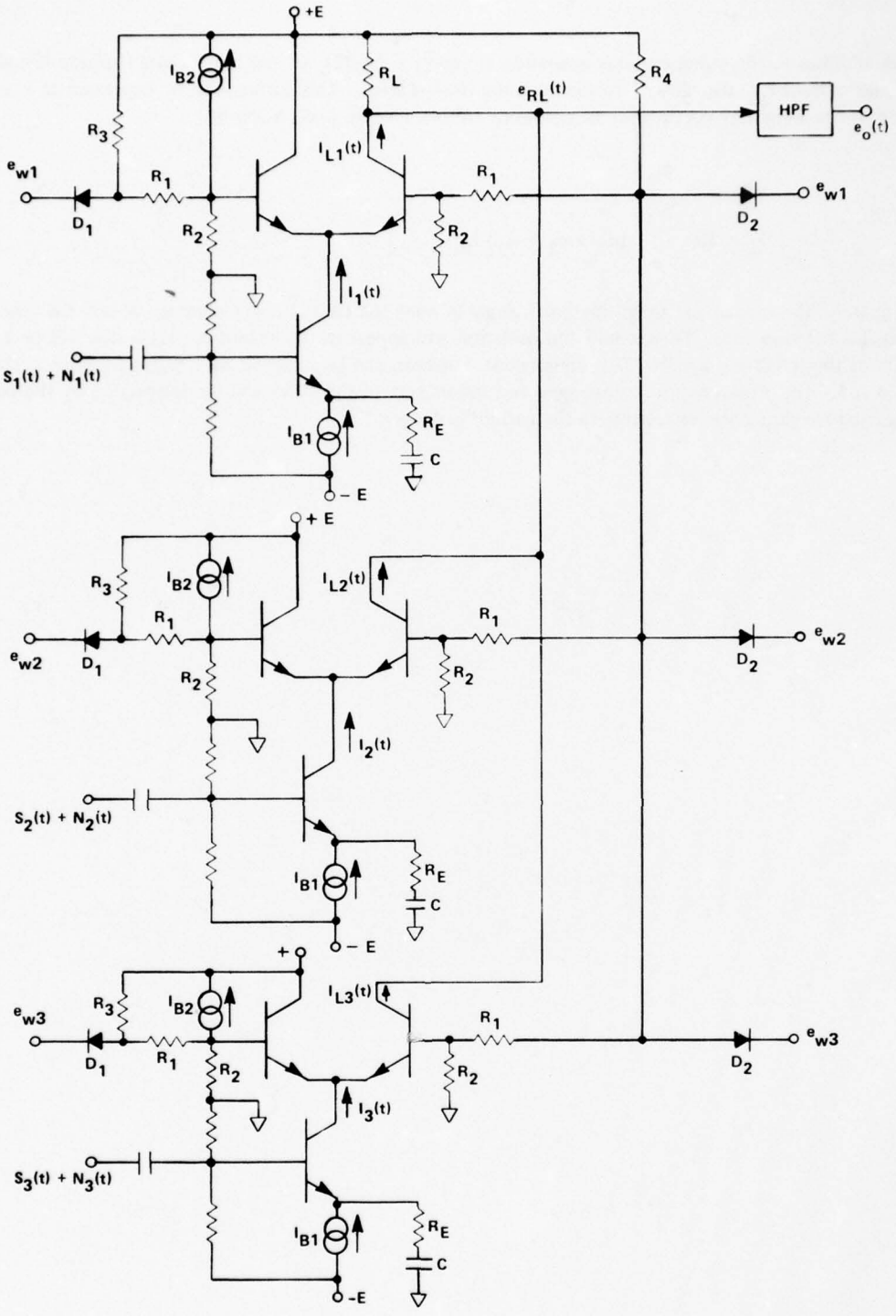

Figure A-3. Three-Channel Diversity Combining Circuit.

In addition to the signal currents appearing in equation (A-22), an additional current proportional to the bias current I_{B1} also flows into the common load resistor. This current can be expressed as a function of the weighting coefficients in equations (A-24), (A-25), and (A-26) by

$$I_L = 10^{-\frac{E_B}{K_3}} (a_1 + a_2 + a_3) I_{B1} \tag{A-27}$$

Unfortunately, the sum of the weighting coefficients in equation (A-27) is not constant as was the case in the two-channel combiner. Thus, a base-line variation will appear in the output $e_{RL}(t)$ which will be a function of the weighting signals. This component, however, can be removed by a high-pass filter as shown in figure A-3. The required cutoff frequency and rolloff rate of this filter will be determined by the bandwidth of the weighting signals relative to the carrier frequency.

APPENDIX B

INCORPORATING PASSIVE FILTERS INTO A DIFFERENTIAL AMPLIFIER CIRCUIT

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B-2

APPENDIX B

INCORPORATING PASSIVE FILTERS INTO A DIFFERENTIAL AMPLIFIER CIRCUIT

The procedure for incorporating a passive filter into the basic differential amplifier circuit of figure 11 is described in this appendix. The inputs are assumed to be differential current sources (equal but 180^{o} out of phase) such as $I_{L1}(t)$ and $I_{L2}(t)$ in figure 11.

For illustration, the steps necessary to make the transition from the configuration in figure B-1 to that in figure 12 will be outlined. Figure B-1 shows two independent LC filter sections selected (from tables for example) for a desired filter characteristic which can be described by the following output voltage to input current transfer function

$$T(s) = \frac{E_1(s)}{I_1(s)} = \frac{E_2(s)}{I_2(s)} = KA(s) \tag{B-1}$$

where

$$A(0) = 1 \tag{B-2}$$

s = the Laplace transform variable.

From equation (B-1) the Laplace transforms of the output voltages become

$$E_1(s) = KA(s)I_1(s) \tag{B-3}$$

$$E_2(s) = KA(s)I_2(s) \tag{B-4}$$

and the differential output can be expressed by

$$E_2(s) - E_1(s) = KA(s)\left[I_2(s) - I_1(s)\right] \tag{B-5}$$

For this example it is seen from figure B-1, equations (B-2) and (B-3) or (B-4) that the constant factor is equal to the parallel combination of R_1 and R_2

$$K = \frac{R_1 R_2}{R_1 + R_2} \tag{B-6}$$

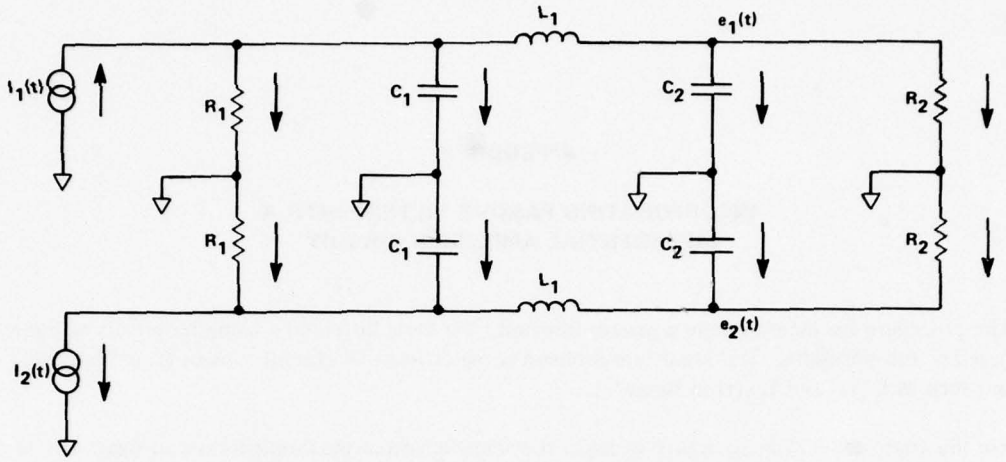

Figure B-1. Differential LC Filter Network.

From figure B-1 it is seen that if

$$I_2(t) = -I_1(t) \tag{B-7}$$

the current in all equal valued components will be equal but opposite in direction. From this it is concluded that no current flows to ground from the junctions of the equal valued components R_1, C_1, C_2, and R_2. Thus, if only the differential output voltage is of interest, these ground connections can be removed without effect. And, in fact, these junctions can be connected to voltage or current sources without affecting the differential output voltage, since the effect would be to produce only common-mode currents and voltages. (From a practical standpoint, however, saturation of inductors, dissipation in resistors, etc. would set limitations.) Also, when a junction is left disconnected, the two corresponding equal components can be replaced by their series equivalent. Applying these rules it is possible to transform the circuit of figure B-1 into that of figure B-2. The junction of the R_1 resistors has been connected to a fixed potential E for bias purposes. The junction of the R_2 resistors has been separated and connected to the input terminals of an operational amplifier for purposes of gain and impedance transformation. This satisfies the requirements of the original circuit with small error since the negative feedback provided by resistor R_o (from the output to the inverting input) maintains the input terminals of the Op Amp at nearly equal voltages. A signal voltage does appear at the input terminals of the Op Amp; however, this is a common-mode voltage and produces no differential voltage. The voltage at the output of the Op Amp in terms of the passive filter output voltages is

$$e_o(t) = \frac{R_o}{R_2} \left[e_2(t) - e_1(t)\right] \tag{B-8}$$

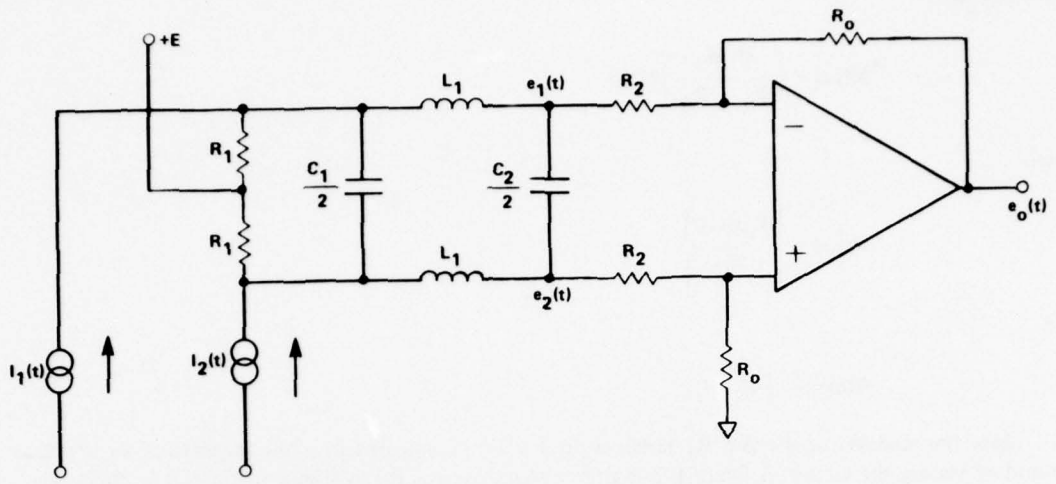

Figure B-2. Differential LC Filter Circuit Incorporated With a Bias Voltage and an Op Amp Output Amplifier.

or in terms of the Laplace transforms of these signals

$$E_o(s) = \frac{R_o}{R_2} [E_2(s) - E_1(s)] \tag{B-9}$$

When equations (B-5) and (B-6) are substituted into equation (B-9), the transform of the output voltage is obtained in terms of the transforms of the input currents

$$E_o(s) = \left(\frac{R_1 R_o}{R_1 + R_2}\right) A(s)[I_2(s) - I_1(s)] \tag{B-10}$$

which is seen to be identical to equation (52) (in Laplace transform notation) except for the presence of the normalized transfer function of the passive filter in equation (B-10). By the use of equation (B-7), equation (B-10) becomes

$$E_o(s) = -\left(\frac{2 R_1 R_o}{R_1 + R_2}\right) A(s) I_1(s) \tag{B-11}$$

Thus the gain of the circuit in figure B-2 at any given frequency (within the Op Amps capability) can be expressed as

$$M(\omega) = \left(\frac{2R_1R_o}{R_1 + R_2}\right)A(\omega) \tag{B-12}$$

where

$$M(\omega) = \frac{\left| E_o(j\omega) \right|}{\left| I_1(j\omega) \right|} \tag{B-13}$$

and

$$A(\omega) = \left|A(j\omega)\right| \tag{B-14}$$

Since the junction of the two R_1 resistors need not be connected to a low impedance, an alternate method of biasing the circuit in figure B-2 is with a series resistor R_B as shown in figure 12. Since the signal currents produce no voltage across this resistor, an appropriate equivalent circuit for determining this bias resistor is shown in figure B-3 where E is the supply voltage and E_B is the bias voltage at output pins 6 or 9 of figure 12. The straightforward application of Kirchhoff's Law to the equivalent circuit in figure B-3 leads to the following expression for the bias resistor

$$R_B = \frac{(R_o + R_2)(E - R_1I_B) - (R_o + R_1 + R_2)E_B}{2(R_o + R_2)I_B + 2E_B} \tag{B-15}$$

where E_B should be selected such that

$$E_B > V_D + R_1I_B \tag{B-16}$$

where V_D is the maximum voltage drop across the diodes from pin 7 to ground and R_1I_B is the maximum peak signal at pin 6 or 9 of the circuit in figure 12.

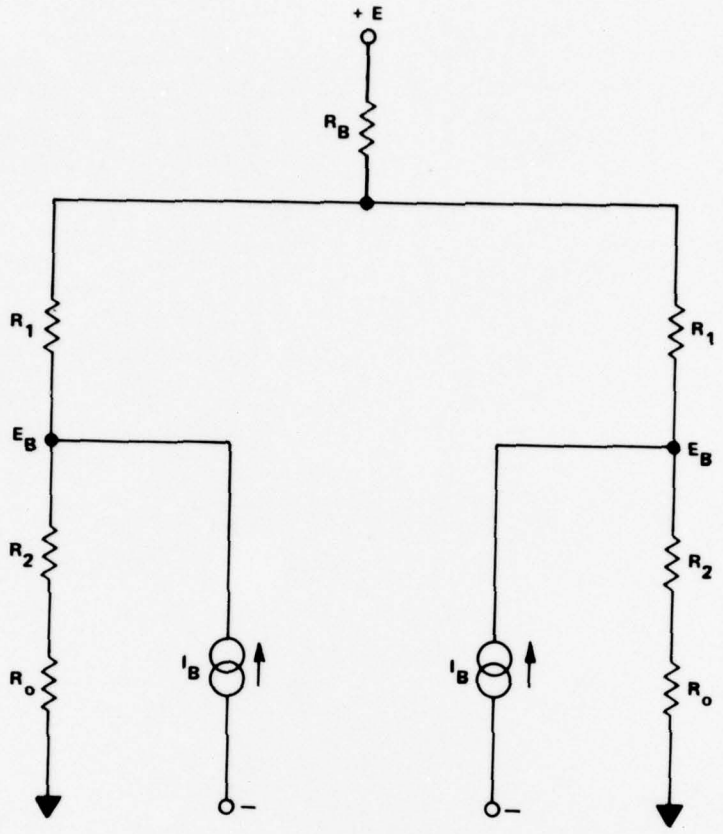

Figure B-3. Equivalent Circuit for Determining the Bias Resistor R_B

APPENDIX C

DESIGN OF RLC AND DIODE INPUT CIRCUIT FOR AM DETECTOR

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APPENDIX C

DESIGN OF RLC AND DIODE INPUT CIRCUIT FOR AM DETECTOR

The complete diode and RLC input circuit of the AM detector in figure 12 appears in figure C-1 where the reactance of the series input capacitor C_1 at the input carrier frequency is assumed to be large compared to the series resistor. The shunt capacitor C_2 represents all circuit loading capacitance including the capacitance of the voltage limiting diodes. The adjustable capacitor C_3 is for tuning purposes; however, since this adjustment is not critical this capacitor is normally fixed or nonexistent depending upon the carrier frequency and choice of inductor value. For input voltages that are below the conduction level for the diodes, the equivalent circuit is shown in figure C-2 which has the following transfer function

$$T(s) = \frac{E_o(s)}{E_i(s)} = \frac{\left(\frac{1}{RC}\right)s}{s^2 + \left(\frac{1}{RC}\right)s + \frac{1}{LC}} \tag{C-1}$$

Equation (C-1) is recognized as the transfer function of a bandpass filter which can be expressed in terms of Q and the center frequency ω_o by

$$T(s) = \frac{\left(\frac{\omega_o}{Q}\right)s}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2} \tag{C-2}$$

where

$$Q = \frac{\omega_o}{\omega_H - \omega_L} \tag{C-3}$$

and where ω_H and ω_L are the upper and lower angular frequencies at which the attenuation is -3 dB. From equation (C-3) the -3-dB bandwidth can be expressed in terms of Q and the center frequency

$$\omega_H - \omega_L = \frac{\omega_o}{Q} \tag{C-4}$$

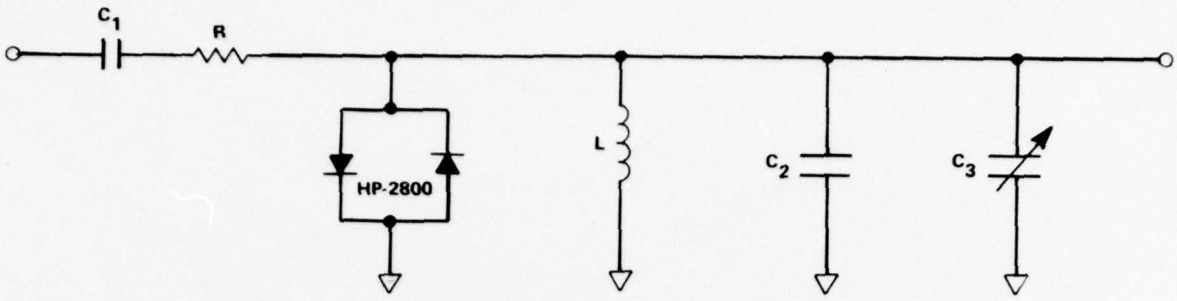

Figure C-1. RLC and Diode Input Circuit for AM Detector.

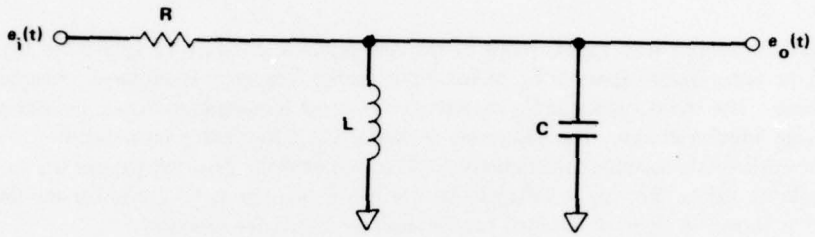

Figure C-2. Equivalent Circuit for Figure C-1.

Comparing the coefficients of equations (C-1) and (C-2)

$$\frac{\omega_o}{Q} = \frac{1}{RC} \tag{C-5}$$

and

$$\omega_o = \sqrt{\frac{1}{LC}} \tag{C-6}$$

Comparing equations (C-4) and (C-5) the -3-dB bandwidth is seen to be equal to

$$\omega_H - \omega_L = \frac{1}{RC} \tag{C-7}$$

Thus the center frequency is equal to the square root of the reciprocal of the LC product and the -3-dB bandwidth is equal to the reciprocal of the RC product. To obtain information on the transient behavior of the circuit, equation (C-1) can also be expressed in terms of the damping factor ζ and the undamped natural frequency ω_n

$$T(s) = \frac{2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{C-8}$$

Comparing the coefficients of equations (C-1) and (C-8) the damping factor is given by

$$\zeta = \frac{1}{2RC\omega_n} \tag{C-9}$$

and the undamped natural frequency by

$$\omega_n = \sqrt{\frac{1}{LC}} \tag{C-10}$$

which is at the center frequency as would be expected. Substituting equation (C-10) into equation (C-9) gives the damping factor in terms of the circuit parameters of figure C-2

$$\zeta = \frac{1}{2R} \sqrt{\frac{L}{C}} \tag{C-11}$$

The damping factor should be greater than one for good circuit stability.

For this application the circuit gain should be nearly constant and the phase shift should be small over the frequency deviation of the carrier. This corresponds to a wide bandwidth and equation (C-7) indicates that for a given value of R, C should be small. The lower limit on the value of C is set by the circuit capacitance. The circuit gain and phase shift as a function of frequency are obtained from the steady state (sinusoidal input) response by use of equation (C-1)

$$T(j\omega) = \frac{\omega^2 L^2 + j\omega LR(1 - \omega^2 LC)}{R^2(1 - \omega^2 LC)^2 + \omega^2 L^2} \tag{C-12}$$

where the denominator has been rationalized by multiplying numerator and denominator by the complex conjugate of the denominator. The phase shift and steady state amplitude response are obtained from equation (C-12)

$$\phi = \tan^{-1} \frac{R(1 - \omega^2 LC)}{\omega L} = \tan^{-1} \frac{R[1 - (\frac{\omega}{\omega_o})^2]}{\omega L} \tag{C-13}$$

$$A(\omega) = \left|T(j\omega)\right| = \frac{1}{\sqrt{\left(\frac{RC}{\omega}\right)^2 \left(\frac{1}{LC} - \omega^2\right)^2 + 1}} \tag{C-14}$$

or in terms of the center frequency

$$A(\omega) = \frac{1}{\sqrt{(\omega RC)^2 \left[\left(\frac{\omega_o}{\omega}\right)^2 - 1\right]^2 + 1}} \tag{C-15}$$

By equating equation (C-14) to $\frac{1}{\sqrt{2}}$ and solving for ω, expressions for the upper and lower −3-dB frequencies ω_H and ω_L are obtained

$$\omega_{H,L} = \sqrt{\frac{1}{LC} + \left(\frac{1}{2RC}\right)^2} \pm \left(\frac{1}{2RC}\right) \tag{C-16}$$

where the plus sign gives ω_H and the minus sign gives ω_L. By use of equation (C-16) it can be shown that the center frequency is equal to the geometric mean of the upper and lower −3-dB cut-off frequencies

$$\omega_o = \sqrt{\omega_H \omega_L} \tag{C-17}$$

As a result of the phase shift through the RLC network, the phase at pin 7 in figure 12 will differ from that at pin 4 by an amount given in equation (C-13). For a sinusoidal input to figure 12, the output voltage will be reduced by a factor equal to the cosine of this phase angle. Therefore to account for this error, equation (55) can be written as

$$e_o = \frac{4R_1 R_o A \cos\phi}{\pi(R_1 + R_2)(R_E + 2r_e)} \tag{C-18}$$

The circuit in figure 12 was designed for a carrier frequency of 900 kHz and the inductor from pin 7 to ground is 1 mH. The required capacitance to place the center frequency of the RLC network at 900 kHz is calculated from equation (C-6) to be approximately 31 pF. The circuit capacitance, including that of the diodes, is approximately 11 pF, which means that an additional capacitance of approximately 20 pF should be added from pin 7 to ground. With these values, in addition to the 1-kΩ input resistor of figure 12, the upper and lower cutoff frequencies as calculated from equations (C-16) are 5.29 MHz and 155 kHz, respectively, and the damping factor calculated from equation (C-11) is 2.8. The circuit gain and phase as calculated from equations (C-13) and (C-14) are listed (along with cos ϕ) in table C-1 for frequencies from 500 kHz to 1.3 MHz.

Table C-1. Circuit Gain and Phase

(f_o = 900 kHz, R = 1 kΩ, L = 1 mH, C = 31 pF)

f(kHz)	A(ω)	ϕ(deg)	cos ϕ
500	0.977	12.4	0.977
600	0.989	8.4	0.989
700	0.996	5.1	0.996
800	0.999	2.4	0.999
900	1.000	0.0	1.000
1000	0.999	-2.1	0.999
1100	0.997	-4.1	0.997
1200	0.995	-5.9	0.995
1300	0.991	-7.6	0.991

This frequency range corresponds to a deviation of 400 kHz with maximum errors of approximately 2%. If more range were desired, the circuit capacitance would permit an inductor as high as 2.8 mH to be used at the 900-kHz carrier frequency.

All of the above calculations were for the linear conditions that exist for input signal levels that are below the conduction level of the diodes. The effect of diode conduction is to reduce the effective circuit resistance, since the resistor R of this analysis will be replaced by R in parallel with the diode dynamic resistance. This effective resistance will be a function of the input amplitude but for this application it is only important to determine the effect that reducing R has on the bandwidth, phase shift, and damping factor. The effect of reducing R is seen from equation (C-7) to increase the bandwidth, from equation (C-13) to reduce the phase shift, and from equation (C-11) to increase the damping factor; all of which lead to smaller errors and better stability. The most important requirement of the diodes in this application is that they have a very short recovery time, usually measured by the effective minority carrier lifetime. Schottky barrier diodes such as the HP 5082-2800 shown in figure 12 perform well in this application.

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