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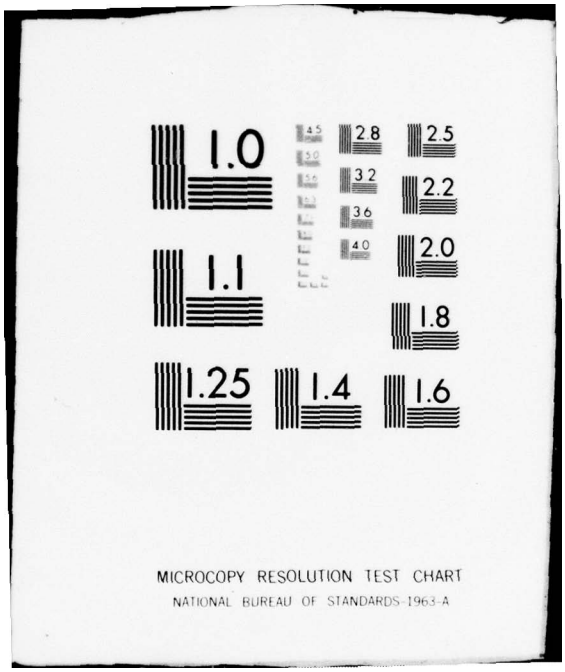
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RADC-TR-78-236
Interim Report
November 1978

CCD LONG-TIME DELAY LINE

RCA Laboratories

W. F. Kosonocky
D. J. Sauer

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A low-loss mode for operating CCDs is described that should lead to a decrease of the transfer losses in long CCD structures by more than two orders of magnitude. The analysis indicates that a buried-channel CCD operating in the low-loss mode should have an effective transfer loss of less than 10^{-7} per transfer. This report also describes the design of a low-loss CCD test chip containing 256- and 1024-stage, closed-loop CCDs. Operating as low-loss CCDs, these devices can store and recirculate 128 and 512 signal samples, respectively. The closed-loop CCD structures include a provision for adding input signal to

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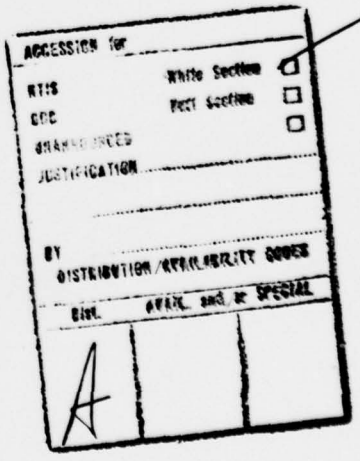
the signal already present in the loop. In addition to the low-loss signal regeneration stages (one in the smaller loop and two in the larger loop), each closed-loop CCD also includes two floating-gate outputs for nondestructive output sensing, a floating-diffusion output for a destructive readout, and a dark-current subtraction stage. Also described in the report is the design of a programmable tester for operating the closed-loop CCDs on the low-loss CCD test chip.

PREFACE

This Interim Report was prepared by RCA Laboratories, Princeton, New Jersey, under Contract No. F19628-77-C-0176. It describes work performed from May 15, 1977 to February 15, 1978, in the Integrated Circuit Technology Center, J. H. Scott, Director. The Project Supervisor was D. E. O'Connor and the Principal Investigator was W. F. Kosonocky. Other Members of the Technical Staff who participated in this program were P. A. Levine, D. J. Sauer, and F. V. Shallcross. The coding of the chip layout was done by G. M. Meray. J. V. Groppe, and C. Y. Tayag worked on the development of the programmable CCD tester. The Air Force Technical Monitor was B. R. Capone of RADC (ET).

The manuscript of this report was submitted by the authors on March 30, 1978.



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GLOSSARY OF SYMBOLS*

ε	= fractional charge loss per transfer.
ε_s	= fractional charge loss per transfer for surface-channel CCD due to surface-state trapping.
N_{SS}	= density of fast surface states per unit area (cm^{-2}).
N_D	= substrate doping density per unit volume (cm^{-3}).
SCCD	= surface-channel CCD.
BCCD	= buried-channel CCD.
n	= number of transfers between low-loss signal-regeneration stages.
$L_{SIG} = n\varepsilon$	= total transfer loss of the signal after n transfers.
L_{T_1}	= total transfer loss of the first trailing well.
L_T	= total transfer loss of a CCD register.
Q_{SIG}	= signal charge.
N	= total number of transfers in a CCD register.
M	= number of signal-regeneration stages (N = nM)
S	= signal (charge)
F	= trailing bias charge.
ϕ_1, ϕ_2	= two-phase clocks.
ϕ_R	= low-loss regeneration clock combining the signal charge (S) with the trailing bias charge (F).
ϕ_F	= trailing bias-charge (fat zero) regeneration clock.
V_F	= transfer barrier for regeneration of the trailing bias charge.
G_{1S}	= dark-current subtraction-stage storage gate powered by ϕ_1.
G_{DCS1}, G_{DCS2}, and G_{DCS3}	= gates of the dark-current subtraction stage. (see Fig. 9, p. 17 and Fig. 17, p. 28)
V_{DCS1}, V_{DCS2}, and V_{DCS3}	= voltages for operation of the dark-current subtraction stage. (see Fig. 9, p. 17 and Fig. 17, p. 28)

* Presented in the order used in the report.

C_{DCS2} = capacitance of the dark-current subtraction-stage gate G_{DCS2}. (see Fig. 9, p. 17 and Fig. 17, p.28)

Q_{DC} = subtracted dark-current charge at each clock cycle. (see Fig. 9, p. 17 and Fig. 17, p. 28)

V_{DCS} = drain voltage of the dark-current subtraction stage (see Fig. 9, p. 17, and Fig. 17, p. 28).

N_{rms} = rms noise due to N-charge carriers with Gaussian distribution.

snr = signal-to-noise ratio.

N_{kTC} = rms kTC noise.

ϕ_{1S} and ϕ_{1T} = phase clock ϕ_1 applied to the storage gates and to the transfer gates, respectively.

ϕ_{2S} and ϕ_{2T} = phase clock ϕ_2 applied to the storage gates and to the transfer gates, respectively.

S_{1A} and S_{1B} = input-source diffusions for introduction of the trailing bias charge (F) and the signal charge (S), respectively (see Fig. 13, p. 24).

G_S = first-level polysilicon gate extending the source diffusion S_{1A} and S_{1B} to the gates G_{1A} and G_{1B}.

G_{1A} and G_{1B} = input-signal barrier gates of the charge preset input stage (see Fig. 13, p. 24).

G_2 and G_3 = signal-storage gate (G_2) and the output-barrier gate (G_3) of the charge preset input stage (see Fig. 13, p. 24).

G_{RGS} and G_{RGT} = storage and transfer gates of the charge combining well of the signal-regeneration stage (see Fig. 14, p. 25).

G_{BCS} and G_{BCT} = storage and transfer gates of the trailing bias-charge regeneration stage (see Fig. 14, p.25 and Fig. 4, p. 10).

ϕ_{RGS} and ϕ_{RGT} = clock voltages applied to the gates G_{RGS} and G_{RGT} for combining the signal charge (S) with the trailing bias charge (F) (see Fig. 14, p. 25 and Figs. 4 & 5 on p. 10 & 11).

ϕ_{BCS} and ϕ_{BCT} = clock voltages applied to the gates G_{BCS} and G_{BCT} for regeneration of the trailing bias charge (see Fig. 14 on p. 25 and Figs. 4 & 5 on p. 10 & 11).

FG1 and FG2 = second-level polysilicon gates on both sides of the floating gate of the floating-gate amplifier (see Fig. 15, p. 26).

V_{FG} = floating-gate reset drain (see Fig. 15, p. 26).

ϕ_{FG} = floating-gate amplifier reset gate (see Fig. 15, p. 26).

ϕ_{FDT} = floating-diffusion amplifier transfer pulse (see Fig. 16, p. 27).

ϕ_{REC} = recirculation transfer pulse (see Fig. 16, p. 27).

S_{OUT} and D_{OUT} = source and drain of the output MOS device of the floating-gate amplifier (See Fig. 18, p. 26).

ϕ_{OUT} = output pulse for transferring charge to the floating diffusion (see Fig. 16, p. 27).

D_1 = floating-diffusion reset drain (see Fig. 16, p. 27).

ϕ_R = floating-diffusion reset gate (see Fig. 16, p. 27).

S_2 and D_2 = source and drain of the floating-diffusion amplifier-output MOS device (see Fig. 16, p. 27).

SECTION I

INTRODUCTION

The general objective of this program is to investigate the possibility of operating very long CCD delay lines with effective charge transfer loss on the order of 10^{-7} per transfer and a time-delay-bandwidth product on the order of 10^{6}. More specifically, the goal of this program is to demonstrate the operation and performance of a low-loss CCD concept. The low-loss CCD concept consists of operating a CCD structure with each signal-charge well being followed by one or more trailing wells. A very low effective transfer loss is achieved by periodically recombining the charge transfer losses collected by the trailing wells with the corresponding signal-charge packets at low-loss signal-regeneration stages. Furthermore, to minimize the charge trapping losses of the CCD channel, the trailing wells are filled with a trailing bias charge that is adjusted to be larger than the maximum signal charge.

Section II of this report describes the low-loss concept and an experimental verification of the low-loss CCD mode of operation in a 128-stage, surface-channel CCD. Section III describes a dark-current-subtraction technique included in the devices on the low-loss test chip. Section IV describes the design and operation of the low-loss CCD test chip. This test chip contains two devices in the form of 256- and 1024-stage, closed-loop two-phase CCDs. For operation in the low-loss CCD mode these devices can store and recirculate 128 and 512 signal samples, respectively.

The closed-loop CCD structures have the following features:

- Two parallel inputs are provided at each loop. One of the inputs is used to sample the input signal and the other input is used to form the trailing bias charge following the signal-charge packets.
- Each loop has one floating-diffusion output with a signal switch. The voltage pulses applied to the signal-switching gates determine whether the signal is to be circulated in the loop or transferred out of the loop via the floating-diffusion output stage.

- Two floating-gate, nondestructive signal-sensing stages are placed in each loop on both sides of the low-loss signal-regeneration stage. In the case of the large loop, with a 1024-stage, two-phase CCD, the operation of only one signal-regeneration stage can be tested with the floating-gate output stages.

- Two independently clocked, low-loss signal-regeneration stages are placed in the larger, 1024-stage loop. One signal-regeneration stage is included in the smaller, 256-stage loop. This will enable us to study the performance of the low-loss CCD operation with signal regenerations after 512, 1024, and 2048 transfers.

- Each loop is constructed with a dark-current subtraction stage. The dark-current subtractor is designed to remove a fixed amount of charge out of the CCD loop. The dark-current subtractor can remove the charge, but not the noise introduced by dark-current generation.

- The dark-current subtractor has been designed so that it can also be operated in the charge proportional mode. In this mode of operation, it will allow removal of 25% of the charge signal out of the loop.

- Each loop has a merged input junction to allow the addition of the input signal to the signal already circulating in the loop.

The design of the electronic system for operating the low-loss CCD test chip is described in Section V. This system is a programmable tester using a microprocessor and a high-speed static random-access memory (RAM) auxiliary system for storing the pulse patterns of the output drivers.

SECTION II

LOW-LOSS CCD CONCEPTS

A. TRANSFER LOSSES OF SURFACE- AND BURIED-CHANNEL CCDs

Typical results [1,2] on charge transfer losses (charge transfer inefficiency) of surface-channel CCDs (SCCDs) are illustrated in Fig. 1. Similar data have also been reported by other investigators [3,4]. According to the available data the transfer losses of SCCDs (with 7- to 10-μm gates) operating with bias charge (fat zero) tend to have a relatively constant fractional transfer loss of about 1 to 3×10^{-4} per transfer for clock frequencies up to 5 to 10 MHz. At higher frequencies the transfer loss of SCCDs becomes limited by free-charge transfer mechanisms [3,5] and tends to increase exponentially with the clock frequency. The relatively constant transfer losses at the intermediate and low frequency have been attributed to the so-called "edge effects" [2,3,6,7]. According to the edge-effect model illustrated in Fig. 2, the potential wells storing the signal-charge packets have sloping sides. Hence, the edges of these potential wells do not benefit from the presence of the bias charge (fat zero) and result in charge trapping by the fast

1. W. F. Kosonocky and J. E. Carnes, "Two-Phase Charge-Coupled Devices with Overlapping Polysilicon and Aluminum Gates," RCA Rev. 34, 164-202 (1973).
2. W. F. Kosonocky and J. E. Carnes, "Design and Performance of Two-Phase Charge-Coupled Devices with Overlapping Polysilicon and Aluminum Gates," Digest of Technical Papers, 1973 International Electron Device Meeting, Washington, D.C., 123-125, Dec. 3-5, 1973.
3. C. H. Sequin and M. F. Tompsett, *Charge Transfer Devices* (Academic Press Inc., New York, 1975), pp. 70-108.
4. A. M. Mohsen and T. F. Retajczyk, Jr., "Fabrication and Performance of Offset-Mask Charge-Coupled Devices," IEEE J. of Solid State Circuits SC-11, 180-188 (1976).
5. J. E. Carnes, W. F. Kosonocky, and E. G. Ramberg, "Free Charge Transfer in Charge-Coupled Devices," IEEE Trans. Electron Devices ED-19, 798 (1972).
6. M. F. Tompsett, "The Quantitative Effects of Interface States on the Performance of Charge-Coupled Devices," IEEE Trans. Electron Devices ED-20, 45-55 (1973).
7. A. M. Mohsen and M. F. Tompsett, "The Performance of Bulk Channel Charge-Coupled Devices," IEEE Trans. Electron Devices ED-21, 701-712 (1974).

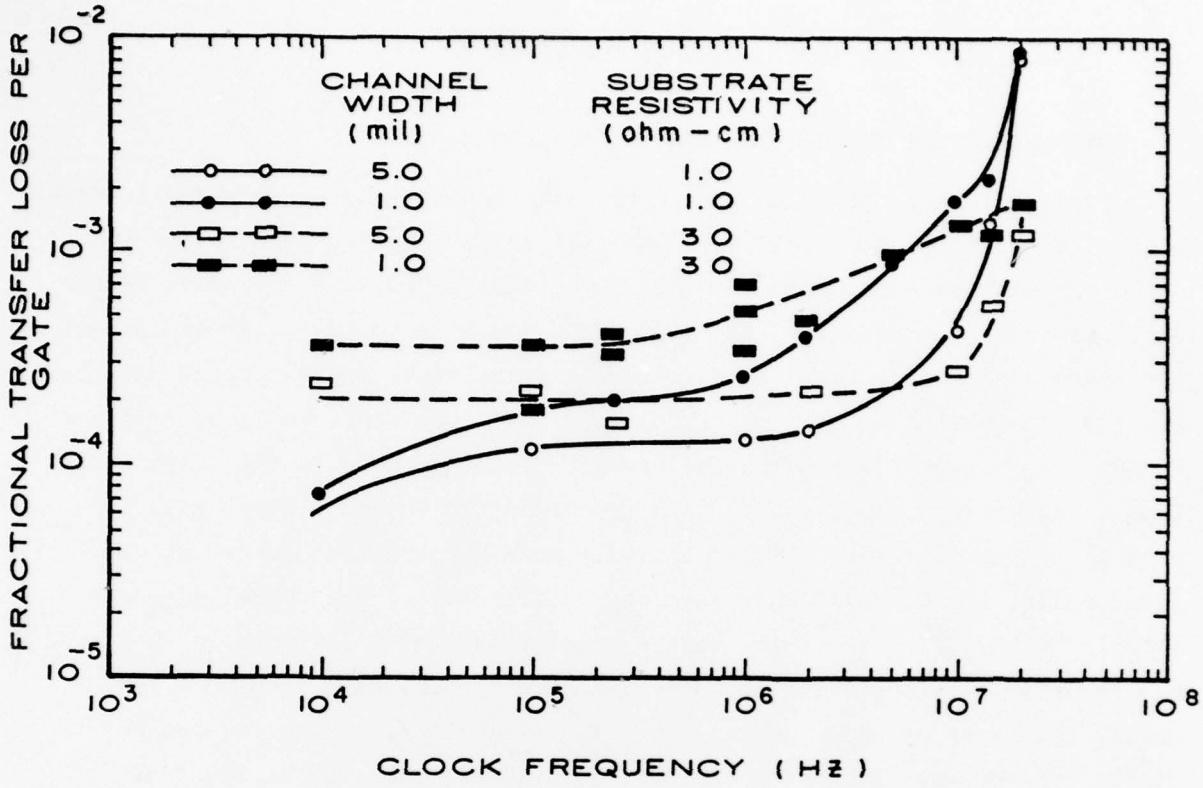
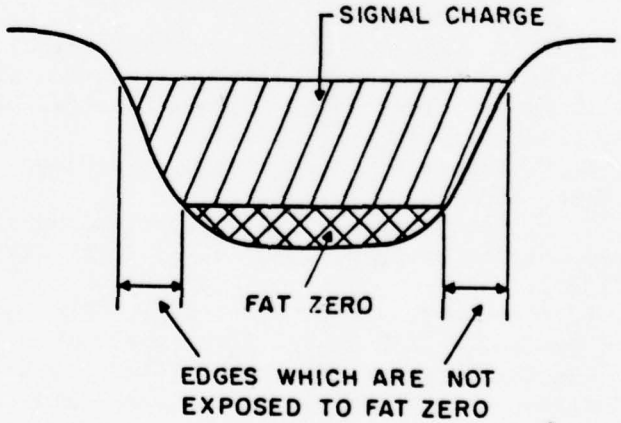


Figure 1. Transfer losses of surface-channel CCDs as function of clock frequency.



$$\epsilon_{EDGE} = 3.9 \times 10^{-4} \left(\frac{1}{W_{mil}}\right) \left(\frac{N_{ss}}{10^{10}}\right) \left(\frac{10^{15}}{N_D}\right)^{1/2}$$

Figure 2. Edge-effect model for surface-channel CCD.

interface states. A single model for the parallel edge loss [2] predicts a fractional loss per transfer given by

$$\varepsilon_{s,\ \text{edges}}^{\text{parallel}} = 3.9 \times 10^{-4} \left(\frac{1}{W_{mil}}\right) \times \left(\frac{N_{SS}}{10^{10}}\right) \left(\frac{10^{15}}{N_D}\right)^{1/2} \qquad (1)$$

for clock frequency of 1.0 MHz, signal of 4 V, and oxide thickness of 1000 Å; where W_{mil} is the channel width in mil, N_{SS} is the density of the fast interface states, and N_D is the substrate doping. In two-phase CCDs, where the signal charge is being transferred between the potential wells under the storage gates via the charge transfer barriers under the transfer gates, there is an additional edge effect under the transfer gates. Both of these edge effects, however, tend to be proportional to the charge signal as a larger charge packet tends to cover a proportionally larger surface of the CCD channel.

In buried-channel CCDs (BCCDs) operating with a bias charge (fat zero) the charge-transfer losses also tend to be relatively constant in the range of 1 to 3×10^{-5} per transfer for clock frequencies up to 20 to 100 MHz [7,8]. At a higher frequency that depends on the gate length and the thickness of the BCCD top layer, the transfer losses become limited by the free-charge transfer mechanisms and tend to increase exponentially with the clock frequency. In a manner similar to the SCCD case, the transfer losses of BCCDs operating with a bias charge (fat zero) at low and intermediate frequencies may also be attributed to the edge effects [7]. According to the edge-effect model for the SCCDs, the surface of the CCD channel exposed to the signal charge tends to be proportional to the magnitude of the signal charge. In BCCDs the signal charge tends to be distributed in the volume of the top layer [8,9]. Therefore, in the case of BCCDs, the edge-effect losses due to the charge trapping by the bulk states are attributed to the fact that proportionally larger volume is exposed to the signal charge as the magnitude of the charge signal is increased. Typical transfer losses of BCCDs are in

8. W. F. Kosonocky and J. E. Carnes, "Basic Concepts of Charge-Coupled Devices," RCA Rev. 36, 566-593 (1975).
9. H. El-Sissi and R. S. Cobbold, "One-Dimensional Study of Buried-Channel Charge-Coupled Devices," IEEE Trans. Electron Devices ED-21, 437-447 (1974).

the range of 1.0 to 3.0×10^{-5} per transfer and are difficult to measure exactly with the available devices. The performance of a two-phase BCCD register with 680 stages developed at RCA Laboratories, Princeton, NJ, is illustrated by output waveforms shown in Fig. 3. Note, for operation with 10% fat zero the measured transfer loss is 1.0×10^{-5} per transfer, which corresponds to only 1.4% of the full well signal.

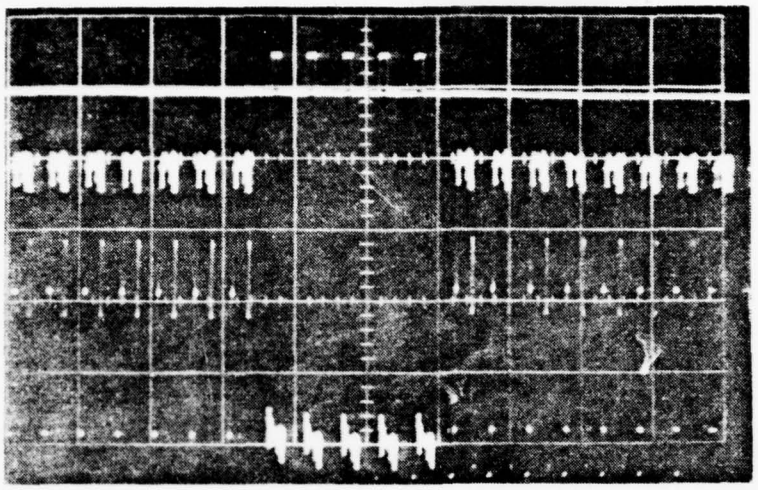
B. EFFECTIVE TRANSFER LOSSES OF LOW-LOSS CCD

The low-loss CCD concept is based on operating a CCD register in such a way that each signal-charge well is followed by at least one trailing well. The function of the trailing well (or wells) is to collect the charge left behind during each transfer of the signal-charge packet. Then, periodically after a number of transfers, the charge collected by the trailing wells is recombined with the corresponding charge-signal packet at a low-loss signal-regeneration stage. Therefore, a low-loss CCD with one trailing well following each signal-charge well will recover the first-order transfer losses, i.e,. the losses of the first loss trailer of a conventional CCD register.

In operation of the low-loss CCD, the trailing well (or wells) may be empty. But, to achieve the best performance, the trailing wells should contain a large bias charge (fat zero) that is adjusted to be larger than the maximum charge in the signal wells. Such a large bias charge placed in the trailing wells between each signal well is expected to have the maximum effect on maintaining the trapping states of the CCD channel filled, hence, minimizes the edge-effect losses. It should be noted that the charge left behind in each transfer of the large bias charge will be practically the same at each stage. Therefore, such steady-state transfer loss of the large trailing bias charge will not appear as the transfer loss of the signal, but rather as a small shift of the signal bias-charge level. At this point we should also add that for the optimum performance the signal wells should also contain a certain amount of bias charge in addition to the signal charge.

In the following analysis, we will develop an approximate expression for the effective charge-transfer loss of a low-loss CCD operating with one trailing well between each signal well. The main assumption in this analysis is that the fractional charge-transfer loss*, ε, is constant [10] and independent of the

*The fractional charge-transfer loss, or transfer loss, is also referred to as the transfer inefficiency parameter.



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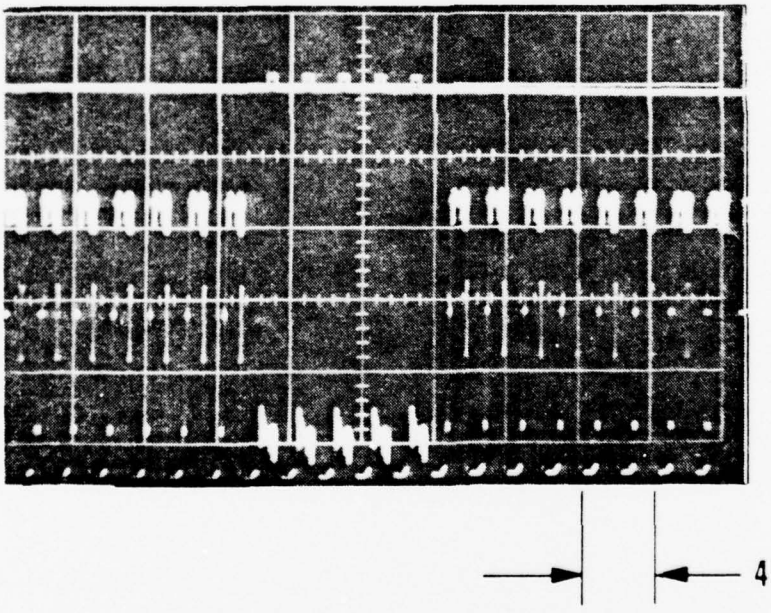

(B)

Figure 3. Output waveforms of a 680-stage, two-phase, buried-channel CCD.

charge being transferred out of the signal well plus out of the trailing well, and that the transfer-loss mechanism does not involve charge trapping for a longer time than one clock cycle.* Further assumptions for this analysis are that there are n charge transfers between the low-loss signal-regeneration stages and that the nε loss product is much smaller than unity, i.e.,

$$n\varepsilon << 1$$

In this case, the total charge left behind the signal charge, $Q_{SIG} = 1$, after the n transfers will be

$$L_{SIG} = n\varepsilon \tag{2}$$

and the total charge left behind each trailing well, i.e., the total transfer loss of the first trailing well, L_{T_1}, will be

$$L_{T_1} = \varepsilon^2 + 2\varepsilon^2 + 3\varepsilon^2 + \ldots (n + 1)\ \varepsilon^2 \tag{3}$$

or

$$L_{T_1} = \frac{(n + 1)\ (n)\ \varepsilon^2}{2} \approx \frac{n^2\varepsilon^2}{2} \tag{4}$$

for

$$n >> 1.$$

Thus, according to this approximate analysis after n transfers of the signal charge, Q_{SIG}, the total charge left behind the signal charge will be $n\varepsilon Q_{SIG}$, the charge accumulated in the trailing well will be $Q_{SIG}(n\varepsilon - \frac{n^2\varepsilon^2}{2})$, and the effective total charge loss after the content of the first trailer well is combined with the charge signal in the signal well at the signal-regeneration stage will be $Q_{SIG}(\frac{n^2\varepsilon^2}{2})$.

However, in operation of the low-loss signal-regeneration stage, that will be illustrated in the next section, there is an additional uncompensated

*The observed transfer loss for operation of conventional SCCDs and BCCDs with a bias charge tend to exhibit the characteristics of such a proportional charge-transfer loss. Furthermore, the operation of the low-loss CCD with large bias charge in the trailing wells will tend to keep filled charge traps with long time constants.

10. R. W. Brodersen, D. D. Buss, and A. F. Tasch, "Experimental Characterization of Transfer Efficiency in Charge-Coupled Devices," IEEE Trans. Electron Devices ED-22, 40-46 (1975).

first-order transfer loss, ε, due to the first transfer of the combined charge. Therefore, a low-loss CCD with N total transfers, M signal-regeneration stages, and with n transfers between the signal-regeneration stages (where N = nM) will have a total transfer loss

$$L_{T\ (\text{low-loss CCD})} = \frac{n^2\varepsilon^2}{2} M + \varepsilon M \tag{5}$$

or an effective loss per transfer

$$\varepsilon\ (\text{low-loss CCD}) = \frac{n\varepsilon^2}{2} + \frac{\varepsilon}{n} \tag{6}$$

Since Eq. (6) has a minimum value for

$$n_{\text{optimum}} = \sqrt{\frac{2}{\varepsilon}} \tag{7}$$

Therefore

$$\varepsilon_{(\text{low-loss CCD})/\text{min}} = \sqrt{2}\ \varepsilon^{3/2} \tag{8}$$

If the low-loss CCD is constructed in the form of a two-phase CCD register with one trailing stage for each signal stage, then the same number of information samples can be stored in a conventional two-phase CCD register with N/2 charge transfers. Therefore, the effective improvement in transfer loss, or transfer inefficiency, of the low-loss CCD over a conventional CCD can be expressed as

$$\frac{L_{T\ (\text{low-loss CCD})}}{L_{T\ (\text{std. CCD})}} = n\varepsilon + \frac{2}{n} \tag{9}$$

and

$$\left.\frac{L_{T\ (\text{low-loss CCD})}}{L_{T\ (\text{std. CCD})}}\right/_{\text{min}} = \sqrt{8\varepsilon} \tag{10}$$

The above comparison was based on the assumption that the transfer losses are proportional to the magnitude of charge in the wells and that they are constant with clock frequency. Therefore, this comparison will not apply to the transfer losses that are free-charge-transfer limited [5], because for the same rate of input signal sampling, the low-loss CCD will have to be operated at a

clock frequency twice as large as the conventional CCD. For the free-charge-transfer limited case the low-loss CCD register is expected to have about the same effective transfer loss per transfer as the conventional CCD register.

C. LOW-LOSS SIGNAL REGENERATION

The construction and operation of a low-loss signal-regeneration stage is illustrated in Figs. 4 and 5. The charge-coupling structure of the signal-regeneration stage is shown schematically in Fig. 4(a) in the form of a two-phase CCD. The transfer of the charge packets in and out of the signal-regeneration stage is illustrated in Fig. 4(b) by means of channel potential profiles at time instants (t_1, t_2, t_3, and t_1') which are indicated on the clock waveforms shown in Fig. 5. To explain the operation of the low-loss signal-regeneration

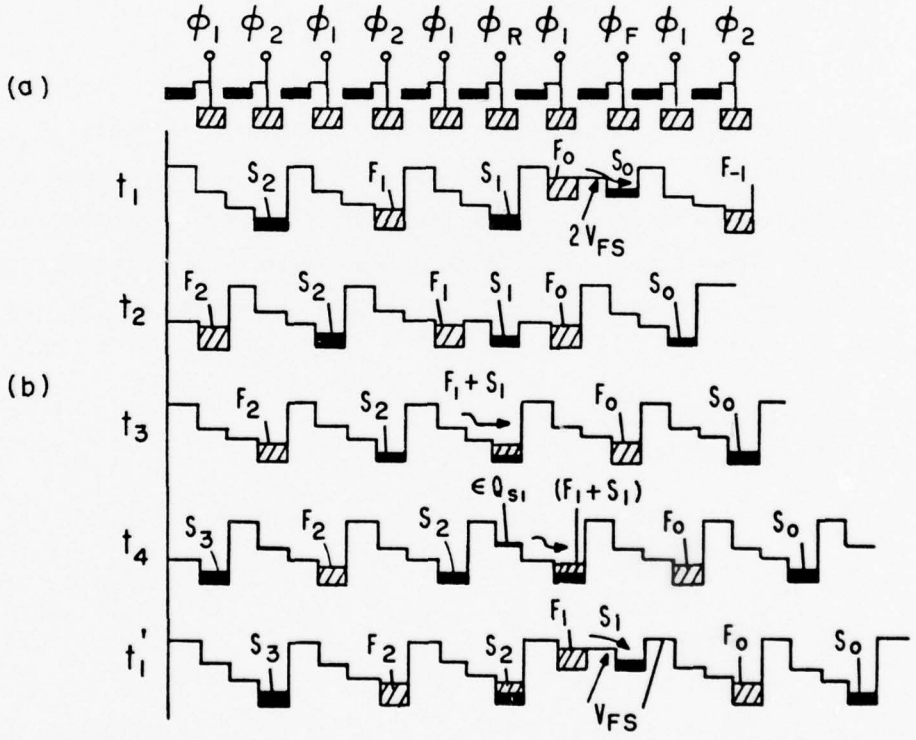

Figure 4. Low-loss CCD. (a) Charge-coupling structure. (b) Potential wells illustrating the operation.

stage, we will focus our attention on the transfers of signal charge S_1 and its trailing bias charge (fat zero) F_1. The signal-regeneration stage first combines the signal charge S_1 with the contents of the trailing well, which in

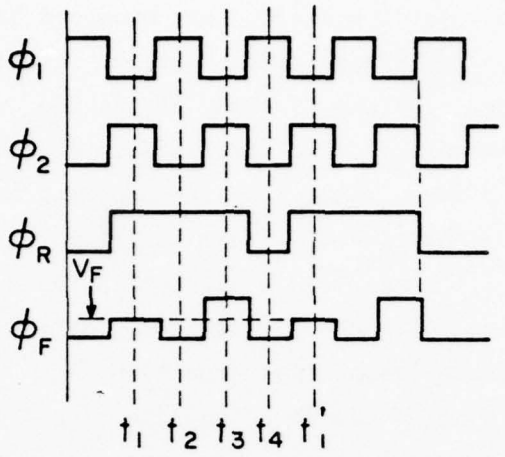

Figure 5. Clock waveforms for operation of the low-loss CCD shown in Fig. 4.

addition to the trailing bias charge F_1, also contains the first-order transfer losses. Then, one clock cycle later the regenerated signal S_1 is separated from its trailing bias charge F_1. To accomplish the above functions two additional clocks, ϕ_R and ϕ_F, are required. The clock ϕ_R delays the signal charge S_1 by one clock cycle, i.e., from time t_1 to t_3. Because of this delay at time t_3, the signal charge S_1 is combined with the trailing bias charge F_1 and the first-order transfer losses contained in the trailing well. At time t_4, the combined charge $(S_1 + F_1)$ is transferred to the adjacent potential well induced by clock ϕ_1. At time t_1', the regenerated signal charge S_1 is skimmed off of the combined charge $(S_1 + F_1)$ and transferred to the well formed by the clock ϕ_F. The function of the clock ϕ_F is to establish the transfer-barrier potential V_F which leaves the trailing bias charge (fat zero) in the well induced by the clock ϕ_1. The same type of separation of the trailing bias charge from the signal charge is also illustrated at time t_1 for the preceding charge packets S_o and F_o. The full potential well powered by the clock ϕ_1, storing the trailing bias charge F_1 at time t_1', or F_o at time t_1, equilibrates with the adjacent potential well formed by the clock ϕ_F in the same way as the conventional charge preset (fill-and-spill) CCD input stage [8]. At this point it should be noted that in the operation of a long low-loss CCD with a large number of signal-regeneration stages, small threshold voltage

variations resulting in small changes of the regenerated trailing bias charges will not affect the performance, provided that measures are taken to assure that the trailing bias charge stays larger than the signal charge, and also does not exceed the charge-handling capacity of the CCD wells.

Referring to the channel potential profiles in Fig. 4(b), we see that the signal charge S_1 is always followed by the trailing bias charge F_1, except during the transfer at time t_4. This is the only transfer where the first-order transfer loss, ε, results in a net transfer loss of εQ_{S_1}, that, at time t_1' will be combined with the following signal charge S_2. Another charge transfer that may require special attention is the transfer involved in separating the trailing bias charge F_1 and the signal charge S_1 at time t_1'. This transfer is referred to as an incomplete (or bucket-brigade type) charge transfer [1,8]. To assure higher charge-transfer efficiency at this point, the transfer barrier (corresponding to the barrier potential V_F) should be made longer than all the other barriers involving a complete charge transfer, so that transfer-barrier modulation by the signal charge is minimized.

D. TEST OF THE LOW-LOSS CCD CONCEPT

To test experimentally the expected performance of a low-loss CCD, we have used a 128-stage, surface-channel CCD register. The device chosen for this test was a p-channel CCD [1] fabricated in RCA in 1972, that had rather large transfer losses due to charge-trapping by the fast interface states. The measurement of the transfer losses of this register operating as a conventional two-phase CCD is illustrated in Fig. 6. The output waveform shown in this figure represents the pulse response of the 128-stage register to five input charge samples. When operating this device with a 20% fat zero (bias charge), the resulting charge-transfer loss is estimated to be 5×10^{-4} per transfer.

The waveform in Fig. 7 shows the same CCD register operating with 20% fat zero in the signal stages and also a 20% fat zero in the alternate (empty) trailing stages. The measured charge-transfer loss for this low-loss CCD mode of operation is 2.7×10^{-4} per transfer.

The operation of the 128-stage, CCD register with a large trailing bias charge in the alternate stages and 20% fat zero at the signal stages is illustrated in Fig. 8. In this case the large trailing bias charges were adjusted

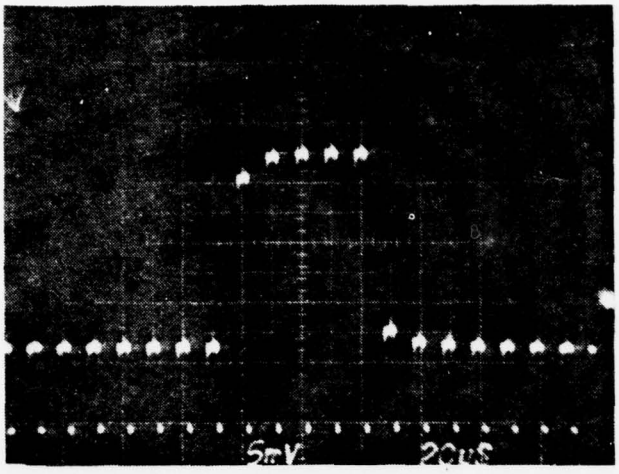

Figure 6. Output waveform of a 128-stage, two-phase SCCD operating in conventional CCD mode with an input signal in the form of five input samples. Vertical scale: 50 mV/div. Horizontal scale: 20 μs/div.

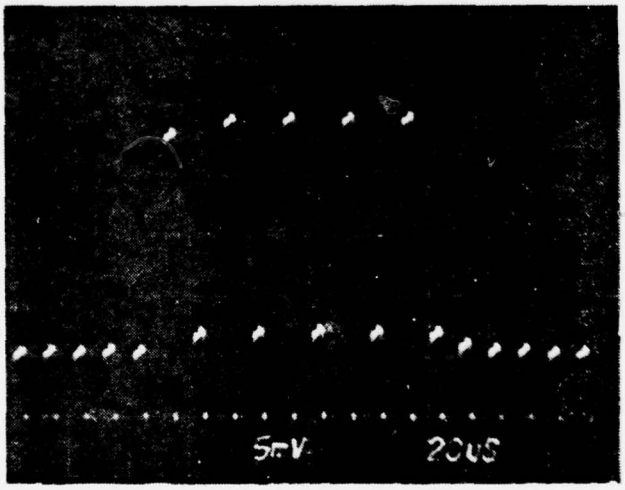

Figure 7. Output waveform of 128-stage, two-phase SCCD operating with 20% bias charge and 20% trailing bias charge in alternate register stages. Vertical scale: 50 mV/div. Horizontal scale: 20 μs/div.

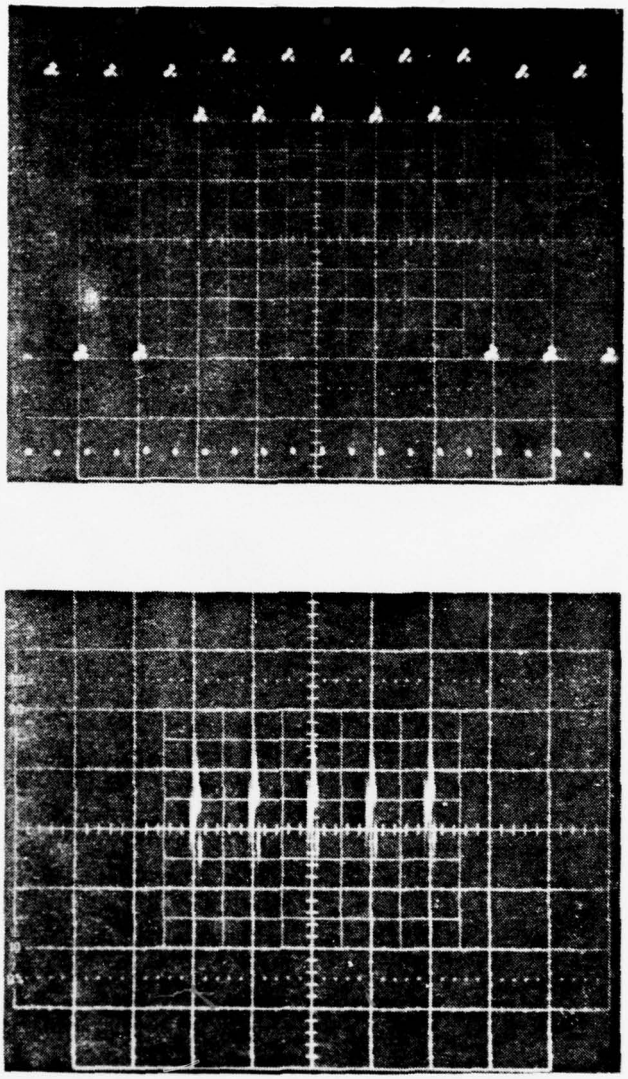

Figure 8. Output waveforms of 128-stage, two-phase SCCD operating with 20% bias charge in the signal stages and large (~100%) trailing bias charge in the alternate register stages. (a) Vertical scale: 50 mV/div. Horizontal scale: 20 μs/div. (b) Vertical scale: 5 mV/div. Horizontal scale: 20 μs/div.

very close to the full well level while the maximum signal charge was set to about 80% of the full well level. The charge-transfer loss estimated from the output waveforms shown in Fig. 8 is about 10^{-5} per transfer.

This experiment demonstrated that in the case of a surface-channel CCD with large, trapping-type transfer losses, the full benefit of the low-loss CCD mode of operation can be achieved only by operating the CCD structure with large trailing bias charge between the signal-charge packets. In the case of the tested device operating with the large trailing bias charge, the measured transfer loss was decreased by a factor of 50 in comparison with the conventional two-phase CCD. However, because in this low-loss CCD mode the signal-charge packets are placed in every other stage of the device, the effective decrease in the transfer loss is only by a factor of 25.

SECTION III

DARK-CURRENT COMPENSATION

A. DARK-CURRENT-COMPENSATION TECHNIQUE

Dark-current generation also imposes a limit to the construction of a very long CCD delay line in the form of an open-loop or a closed-loop structure. Maximum delay time that can be achieved with present CCDs at room temperature is between 0.1 and 1.0 second. CCDs must be cooled to achieve longer time delays. In addition to a more-or-less constant level of dark current, most CCDs exhibit also local dark-current spikes. The actual magnitude of both the uniform background dark current, as well as that of the spikes, depends strongly on the quality of the starting silicon substrate and on the device processing.

One circuit technique to minimize the effect of the dark-current spikes is to design the CCD structure so that all the signal-charge packets are transferred through the same CCD stages and that each signal-charge packet spends the same time duration at each location of the CCD structure. In this case, the effect of the dark-current spikes will be evenly averaged over all signal-charge packets.

The second limitation is due to the uniform dark-current accumulation in the CCD well which first will start limiting the available charge-handling capacity of the CCD structure. Then, as the time delay is increased, eventually the average uniform dark current will completely fill the CCD wells. The dark-current-compensating circuit described in this section may be used to increase the available time delay by one to several orders of magnitude by periodically removing from the CCD fixed amounts of dark-current generated charge. In this type of dark-current compensation there is a trade-off between the resulting increase in the signal delay and a reduction of the signal-to-noise ratio (snr). This results from the fact that this dark-current-compensating circuit, by removing fixed amounts of charge from the register, can reduce (to a small value) the average accumulated dark-current charge, but it will not remove the shot noise introduced by the dark current.

B. DARK-CURRENT SUBTRACTION STAGE

The construction and operation of a dark-current subtraction stage are illustrated in Fig. 9. The cross-sectional view of one gate of a CCD register, G_{1S}, and three gates of the dark-current subtraction stage are illustrated in Fig. 9(a).* Operation of the dark-current subtraction stage is illustrated by the channel potential profiles shown in Figs. 9(b), (c) and (d). In Fig. 9(b),

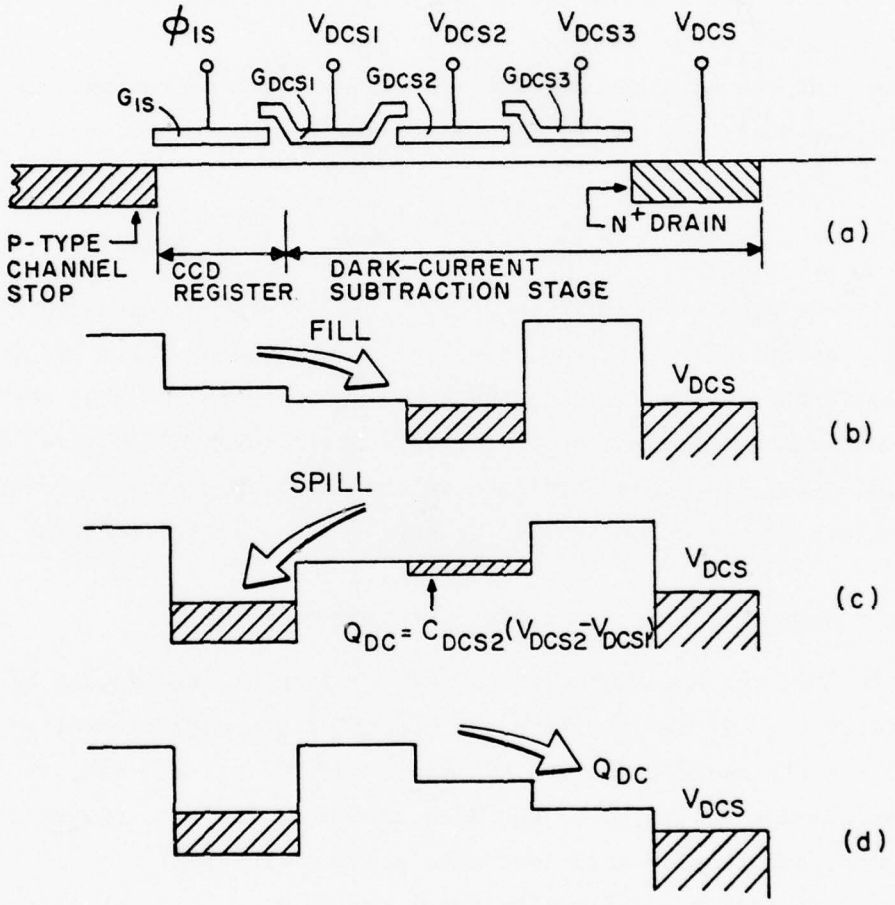

Figure 9. Construction and operation of the dark-current subtraction stage.

*The top view of the dark-current subtraction stage used in the dark-current closed-loop, low-loss CCD test chip is shown later in Fig. 17. (Also see the waveform diagram in Fig. 19.)

the charge signal introduced into the storage gate G_{1S} of the CCD register spills over into the potential well under the gate G_{DCS2}. Then, in Fig. 9(c), the charge signal is spilled back into the potential well under the gate G_{1S} while a small, fixed amount of charge Q_{DC} is left behind in the potential well under the gate G_{DCS2}. Finally, as shown in Fig. 9(d), the charge subtracted from the CCD channel, Q_{DC}, is spilled to the drain V_{DCS}. This operation can be accomplished at the same time as the signal charge is transferred out from the well under the gate G_{1S}.

Assuming that the same type of surface-channel is constructed under all the gates in Fig. 9(a), the charge Q_{DC} removed by the above process is

$$Q_{DC} = C_{DCS2} (V_{DCS2} - V_{DCS1}) \tag{11}$$

where C_{DCS2} is the capacitance of the gate G_{DCS2}. For a buried-channel CCD, C_{DCS2} will represent an effective capacitance associated with the gate G_{DCS2}. The only requirement of the above charge-scooping operation is that the charge Q_{DC} be constant and independent of the signal-charge magnitude. Also, for any given long CCD delay line, the magnitude of the charge Q_{DC} to be removed from the CCD structure should be controlled by some form of active feedback circuit.

C. NOISE INTRODUCED BY THE DARK-CURRENT SUBTRACTION STAGE

Since the dark-current subtraction stage removed a fixed amount of charge from a CCD structure, it can suppress the effect of the dark current on the reduction of the charge-handling capability of the CCD wells. But, it cannot remove the shot noise generated by the dark current. In fact, the process of the dark-current subtraction will introduce a kTC noise [11].

Let us assume that the full-well signal charge in a buried-channel CCD corresponds to 10^6 charge carriers and has snr = 5×10^3. Now, if this CCD is operated with 10 dark-current subtraction stages, each removing 10% of full

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11. J. E. Carnes and W. F. Kosonocky, "Noise Sources in Charge-Coupled Devices," RCA Rev. 33, 327-343 (1972).

well of dark-current generated charge, the total generated dark-current charge will correspond to 10^6 charge carriers. The resulting rms noise will be

$$N_{rms} = \sqrt{10^6} = 10^3 \tag{12}$$

and the snr will be decreased to

$$\text{snr} = 10^3 \tag{13}$$

Now, let us assume that the time delay is increased 100 times by operating the above CCD as a closed-loop structure with 100 signal recirculations. The resulting shot noise introduced by the dark current will be increased to

$$N_{rms} = \sqrt{10^8} = 10^4 \tag{14}$$

and the snr will be decreased to

$$\text{snr} = 100 \tag{15}$$

The above analysis, however, did not include the additional kTC noise introduced by the dark-current subtraction stages. For m dark-current subtractions, this kTC noise at room temperature can be expressed as

$$N_{kTC} = 400m\sqrt{C_{DCS2}} \tag{16}$$

where G_{DCS2} is the effective capacitance of the dark-current scooping well in picofarads (i.e., the potential well under the gate G_{DSC2} in Fig. 9).

SECTION IV

LOW-LOSS CCD TEST CHIP

A. GENERAL DESCRIPTION OF THE LOW-LOSS CCD TEST CHIP

To study the characteristics and the performance limitations of the low-loss CCD concept, we have designed a low-loss CCD test chip, TC1230. A photograph of the superimposed check plots for TC1230 is shown in Fig. 10. This chip has dimensions of 198 mil x 172 mil. The chip is divided into two parts: Part "A" of the test chip (TC1230A) contains a 1024- (or 1023-) stage, closed-loop structure illustrated schematically in Fig. 11. This closed-loop structure was designed to be operated either with one or two low-loss signal-regeneration stages. Part "B" of the test chip (TC1230B) contains a 256- (or 255-) stage, closed-loop structure illustrated schematically in Fig. 12. The second closed loop has only one low-loss signal-regeneration stage.

The closed-loop CCD structures were designed with 1.0-mil-wide CCD channels and two-phase CCD operation with a dc offset voltage to be applied between the storage gates and the transfer gates, i.e., between the clock phases ϕ_{1S} and ϕ_{1T}, as well as ϕ_{2S} and ϕ_{2T}. The charge-coupling corners of both closed loops were designed for a complete charge-transfer operation with the available two-phase CCD clocks.

Originally, the two closed-loop structures were designed with 1024- and 256-stages of two-phase CCDs. When operating in the low-loss CCD mode these loops would store 512 and 128 signal samples, respectively. However, during the detailed design of the timing pulses required to test these structures, we realized that, because of the delay by one clock cycle at the signal regeneration stage, it is inconvenient to operate these devices with one signal-regeneration stage in the loop, unless these loops are constructed with an odd number of CCD stages. To correct this situation we have fabricated two additional masks for the two levels of polysilicon. With these additional available masks we will be able to fabricate the low-loss CCD test chips with either the 1024- and 256-stage, closed loops or with the 1023- and 255-stage, closed loops.

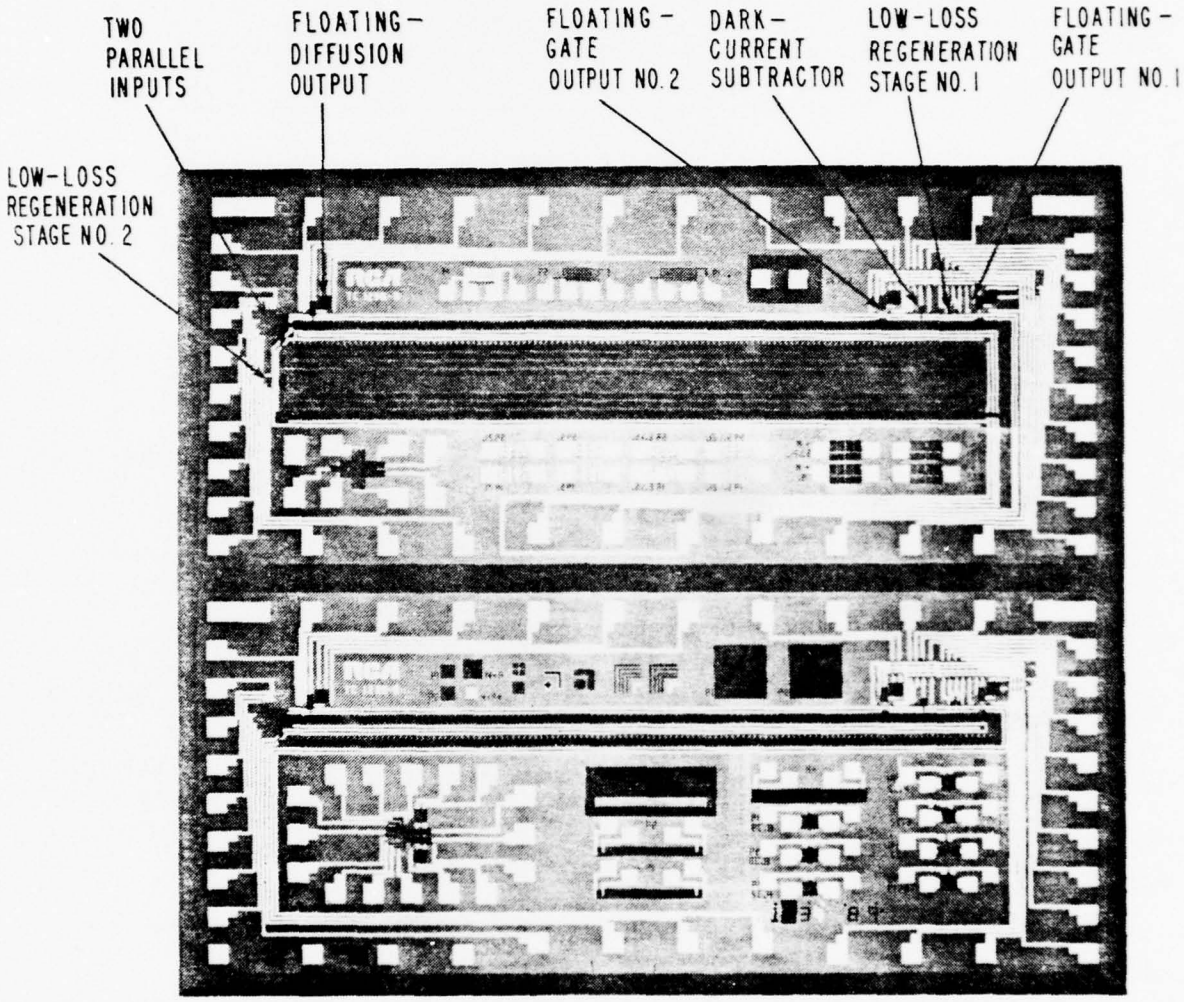

Figure 10. Photograph of the composite of the mask layers of the low-loss CCD test chip, TC1230.

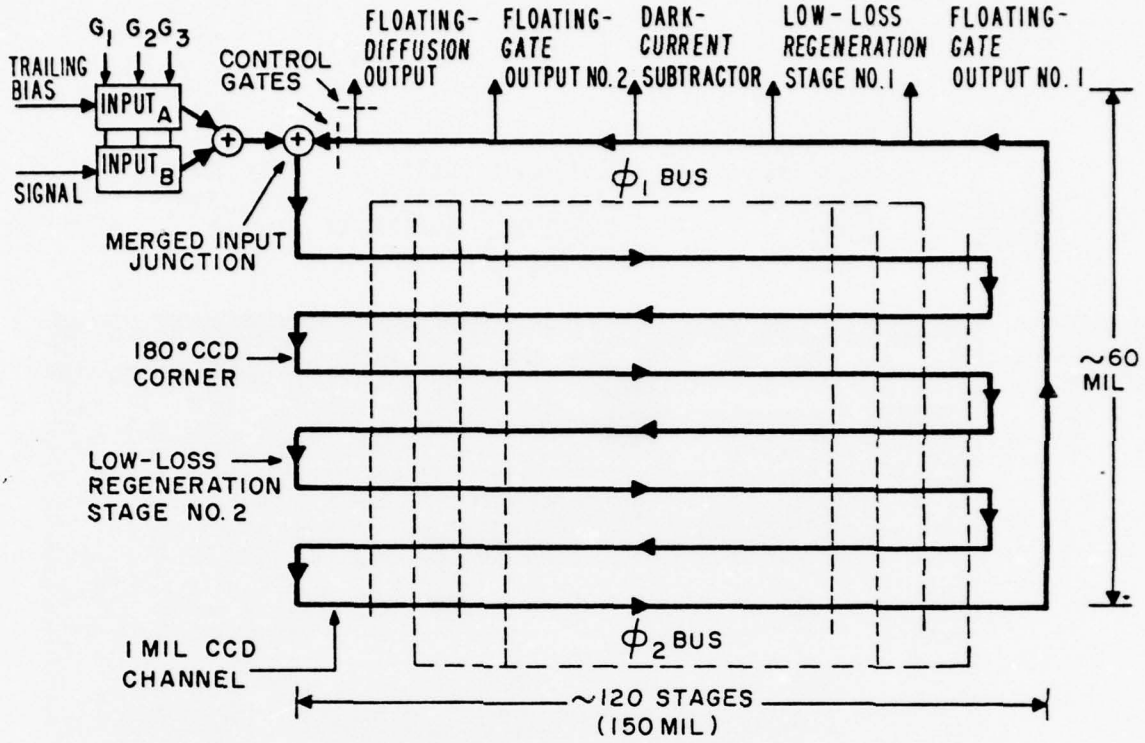

Figure 11. Schematic of the layout of the 1024- (or 1023-) stage CCD loop.

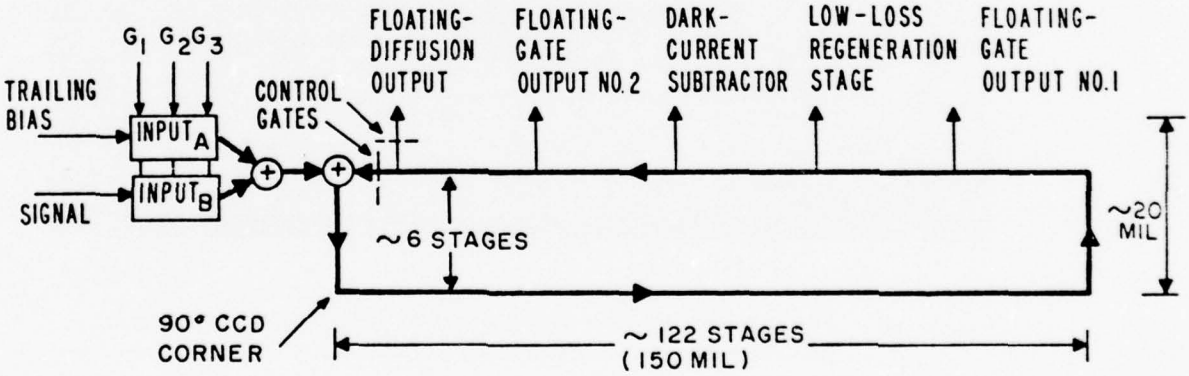

Figure 12. Schematic of the layout of the 256- (or 255-) stage CCD loop.

As will be illustrated in the layouts in Figs. 13 to 18, the masks for the low-loss CCD test chip were designed for processing the devices with two levels of polysilicon gates. The channel stops can be either in the form of p^+ diffusions or p-type implants. The n^+ diffusions in this process are not self-aligned with the polysilicon gates.

B. CHARGE-COUPLING FEATURES OF THE CLOSED-LOOP CCD STRUCTURES

The schematics of the 1024- (or 1023-) stage and 256- (or 255-) stage, closed-loop CCDs are shown in Figs. 11 and 12, respectively. Except for the fact that the larger closed-loop structure has two low-loss signal-regeneration stages, both of these structures have the same charge-coupling features described below.

1. Input Structure

The detailed layout of the input structure of the closed-loop CCDs is shown in Fig. 13. Two parallel input channels are provided: one is for the signals, and the other is for introducing the trailing bias charge between the signal samples. These input channels have a channel width of 1.4 mil to provide sufficient dynamic range for a full well in the main CCD register. The inputs are operated using standard charge preset (fill-and-spill) with a negative pulse on the input-source diffusions.

The input signals are introduced into the closed-loop CCD at the merged input junction. This junction is designed to operate as a signal adder. Thus, if the closed loop is empty, a new signal can be introduced into the loop. However, the input signal can also be added to a signal already circulating in the loop. The direction of the signal flow is built into the merged input junction as designated by the arrows in Fig. 13.

2. Low-Loss Signal-Regeneration Stage

The detailed layout of the low-loss signal-regeneration stage #1 shown in the photograph in Fig. 10 is illustrated in Fig. 14. The operation of this signal regeneration stage is described in Section II-C, and illustrated in Fig. 4. To increase the charge-handling capacity of the potential wells

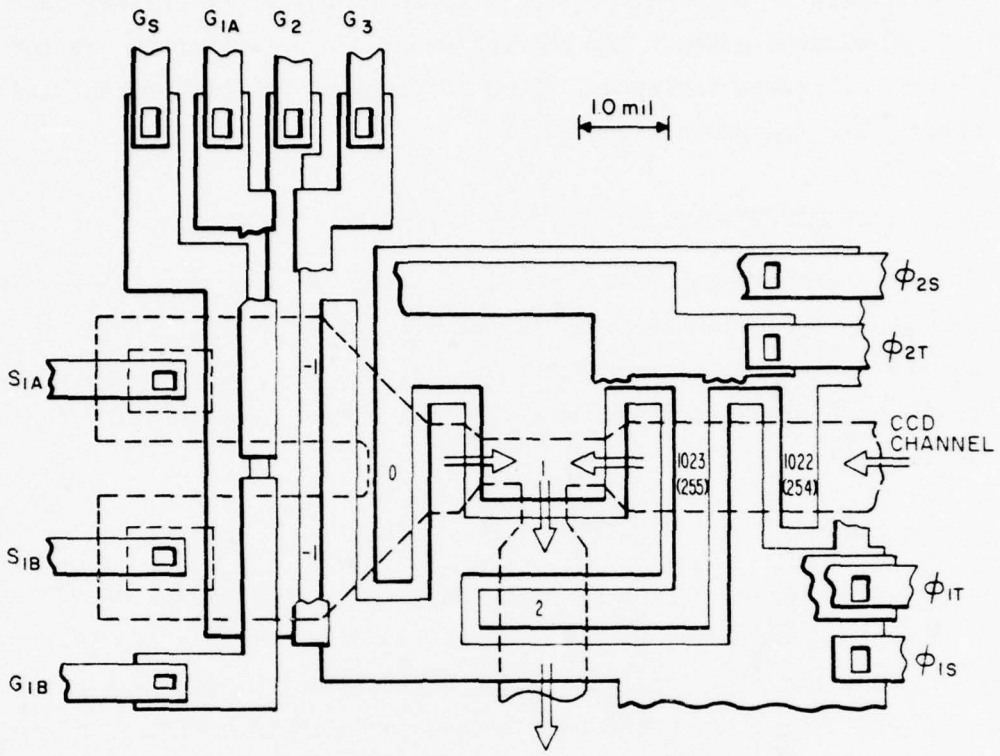

Figure 13. Layout of parallel inputs and merged input junction.

carrying the signal charge, combined with the trailing bias charge, the width of the CCD channel at this stage was increased from 1.0 to 1.5 mil and the length of the storage gates G_{RGS} and G_{1S} was increased from 0.4 to 0.6 mil.

Another design feature of the signal-regeneration stage that should be mentioned is the increased length of the trailing bias-charge generating transfer gate, G_{BCT}. The length of this gate was increased from the typical value of 0.2 to 0.4 mil. The longer barrier formed under this transfer gate is expected to give lower charge-transfer loss at this incomplete charge transfer [1] which separates the signal charge from the trailing bias charge.

The two low-loss signal-regeneration stages in the 1024- (or 1023-) stage loop are laid out for operation with separate clock pulses. Thus, this loop can be operated either with one or two low-loss signal regenerations. Of course, there is always the possibility of operating the closed loop as a conventional two-phase CCD not involving the low-loss signal regeneration.

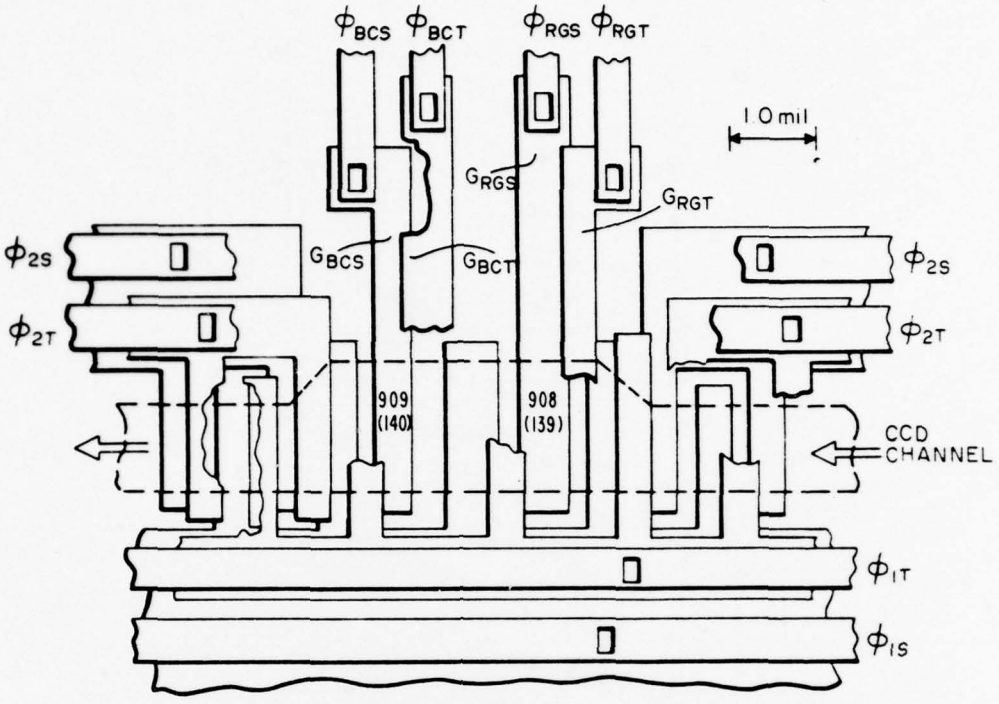

Figure 14. Layout of the low-loss signal-regeneration stage.

3. Floating-Gate Outputs

Two floating-gate, nondestructive signal-sensing stages are placed in each loop on both sides of the low-loss signal-regeneration stage. In the case of the large loop, with a 1024-stage, two-phase CCD, the operation of only one signal-regeneration stage can be tested with the floating-gate output stages. The layout of the floating-gate output stage is illustrated in Fig. 15. The signal-sensing floating gate of this stage can be periodically reset to a reference potential V_{FG} by a clock pulse ϕ_{FG}. The function of two externally controllable dc levels, FG1 and FG2, is to provide isolation from the two-phase clocks and to assure a complete charge transfer at this floating-gate output [8].

4. Floating-Diffusion Output

The signal is removed from the closed-loop CCDs by the floating-diffusion output stage. This stage provides the destructive readout from the loop. The

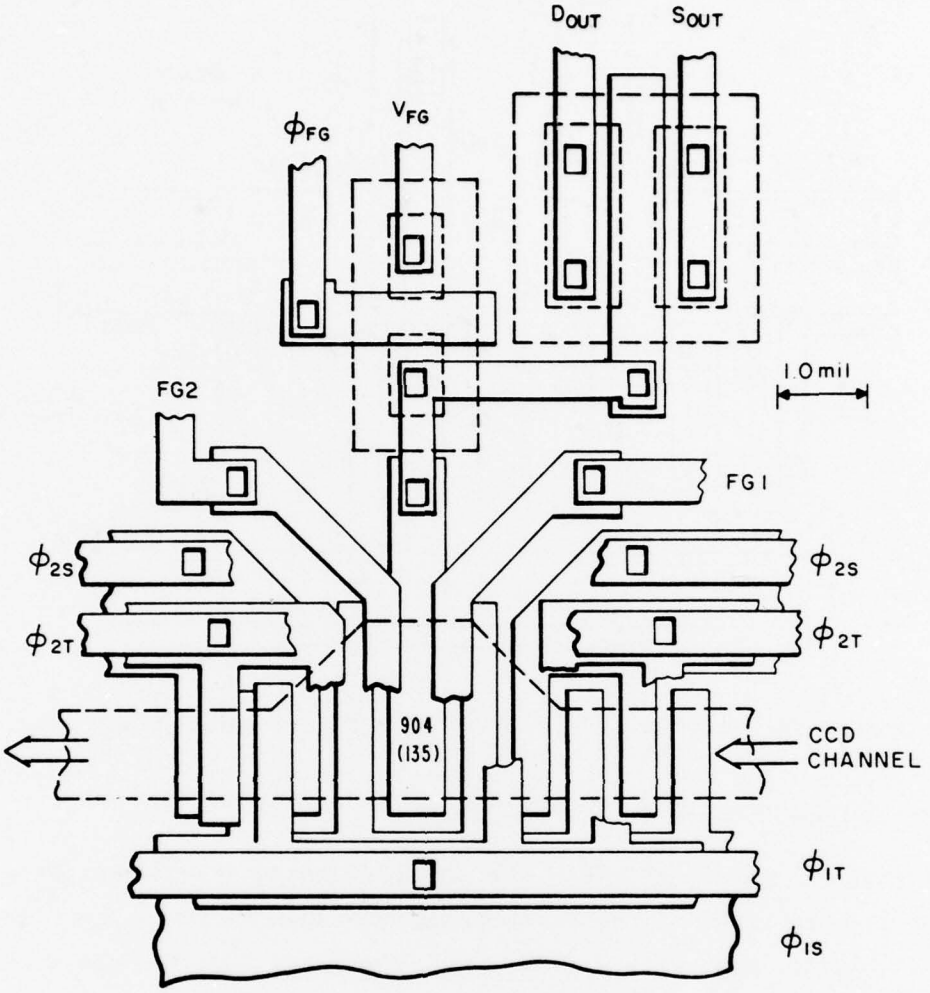

Figure 15. Layout of the floating-gate output stage.

layout of the floating-diffusion output stage is shown in Fig. 16. The floating-diffusion output is controlled by the transfer pulses ϕ_{FDT} (floating-diffusion transfer) and ϕ_{REC} (recirculation transfer) operating in conjunction as complementary pulses.

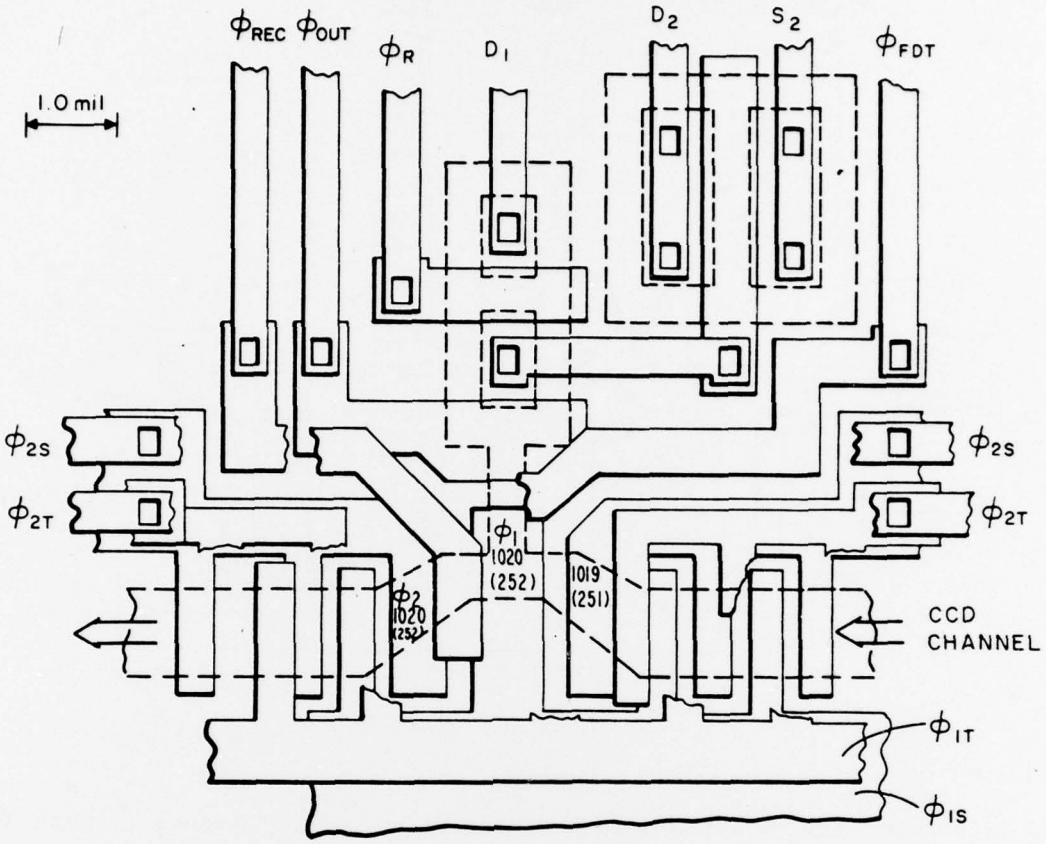

Figure 16. Layout of the floating-diffusion output stage.

5. Dark-Current Subtraction Stage

Each loop is constructed with a dark-current subtraction stage illustrated by the layout shown in Fig. 17. The operation of this stage which can be adjusted to remove a fixed amount of charge from the loop was described in Section III. This dark-current subtraction stage, however, can be also operated as a proportional charge subtractor. In this mode of operation, this stage will allow a removal of 25% of charge from the signal-charge packets and/or the trailing bias-charge packets.

C. OPERATION OF LOW-LOSS CCD LOOPS

The operation of the low-loss CCD loops described in this section will cover only the case with one low-loss signal-regeneration stage active in each

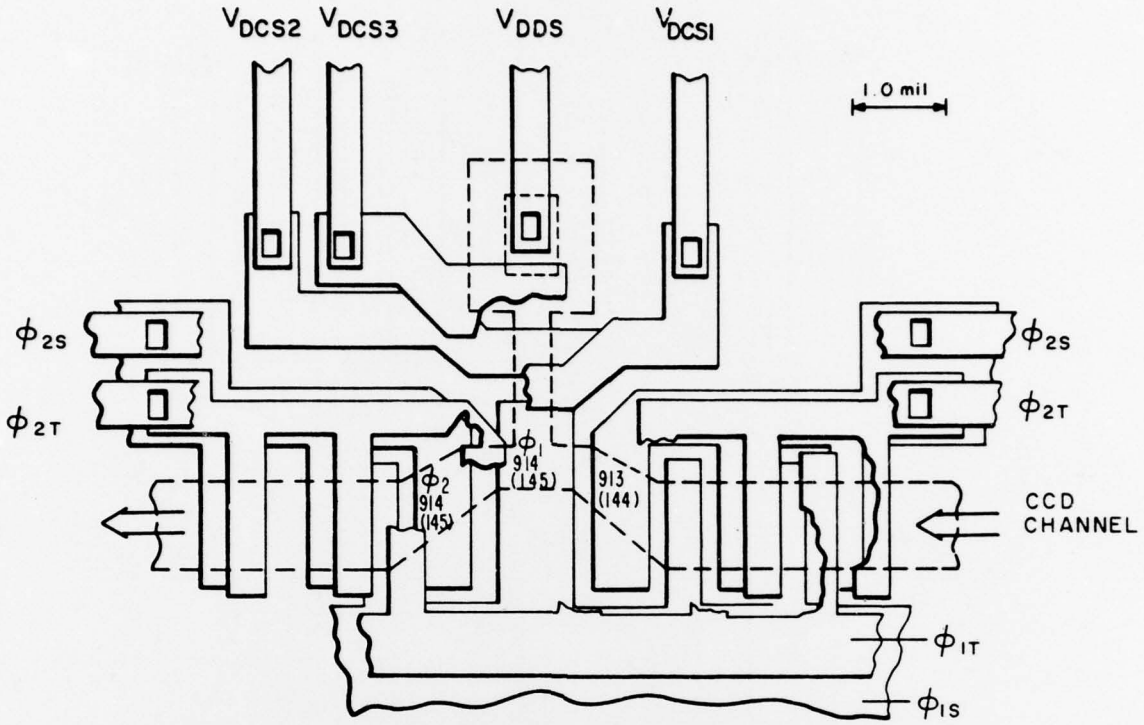

Figure 17. Layout of the dark-current subtraction stage.

loop. Also, we will consider only the case of the polysilicon-gate mask option for which the test chip will have the 255-stage and 1023-stage, closed-loop CCDs.

When operating in the low-loss mode, the 255-stage loop stores 128 signal-charge packets, and the 1023-stage loop stores 512 signal-charge packets. The exact positions of the output stages described above along the CCD delay line are listed in Table I. The merged input junction (under the ϕ_{2S} storage electrode) is stage #1 (see Fig. 3), and subsequent stages are numbered in order counterclockwise around the CCD loop. Note that from the dual-channel input metering wells under gate G_2 to the merged input junction, there is a two-stage delay. Thus, the input may be considered to be at stage #-1 since these two stages are not actually part of the closed-loop CCD.

Figure 18 is a timing diagram for the 255- and 1023-stage, closed-loop CCDs operating in the low-loss mode. A more detailed timing diagram for loop

TABLE 1. LOCATIONS OF FUNCTIONAL STAGES

Item	Position of Stage Along CCD Loops	
	255-Stage Loop	1023-Stage Loop
1. Dual-Channel Input (Fig. 13)	-1 (ϕ_2)	-1 (ϕ_2)
2. Merged Input Junction (Fig. 13)	1 (ϕ_2)	1 (ϕ_2)
3. Floating-Gate Output #1 (Fig. 15)	135 (ϕ_2)	904 (ϕ_2)
4. Signal Regenerator(s) (Fig. 14)	139 (ϕ_2)	(506)(ϕ_2) 908 (ϕ_2)
5. Dark-Current Subtractor (Fig. 17)	145 (ϕ_1)	914 (ϕ_1)
6. Floating-Gate Output #2	151 (ϕ_2)	920 (ϕ_2)
7. Floating-Diffusion Output (Fig. 16)	252 (ϕ_1)	1020 (ϕ_1)

cycle 0 is shown in Fig. 19. Four bit times of the microprocessor-based, test system CCD master clock are used for each CCD clock cycle so that timing edges are available to generate the narrower V_{DCS1}, V_{DCS2}, ϕ_{FG}, and ϕ_R pulses. During loop cycle 0, new signals are introduced into the CCD register at the dual-channel input stage. (Just prior to loop cycle 0, i.e., during the previous loop cycle N, all charge in the CCD is removed by clocking it out of the floating-diffusion output.) The input signal is applied to gate G_{1A}. In the timing diagram a data input pattern of 0 1 1 0 is used. Note that a '1' level corresponds to a more negative level on the input gate G_{1A} and the negative S_{1A} strobe pulses occur when ϕ_1 is off. The S_{1A} pulses occur during even clock cycle times and the S_{1B} pulses (for introducing trailing bias charge in the second input channel) occur at odd clock cycle times. A total of 128 S_{1B} pulses occur during loop cycle 0. At the beginning of loop cycle 1, the S_1 pulses are inhibited and no further charge is introduced to the CCD via the dual-channel input stage.

At the beginning of loop cycle 0, the transfer out of the floating-diffusion stage ends by terminating the ϕ_{FDT} pulses, and the recirculation mode is started by initiating the ϕ_{REC} pulses. In the 255-stage loop, the first signal S_1 appears at the floating-gate output #1 during clock time 136

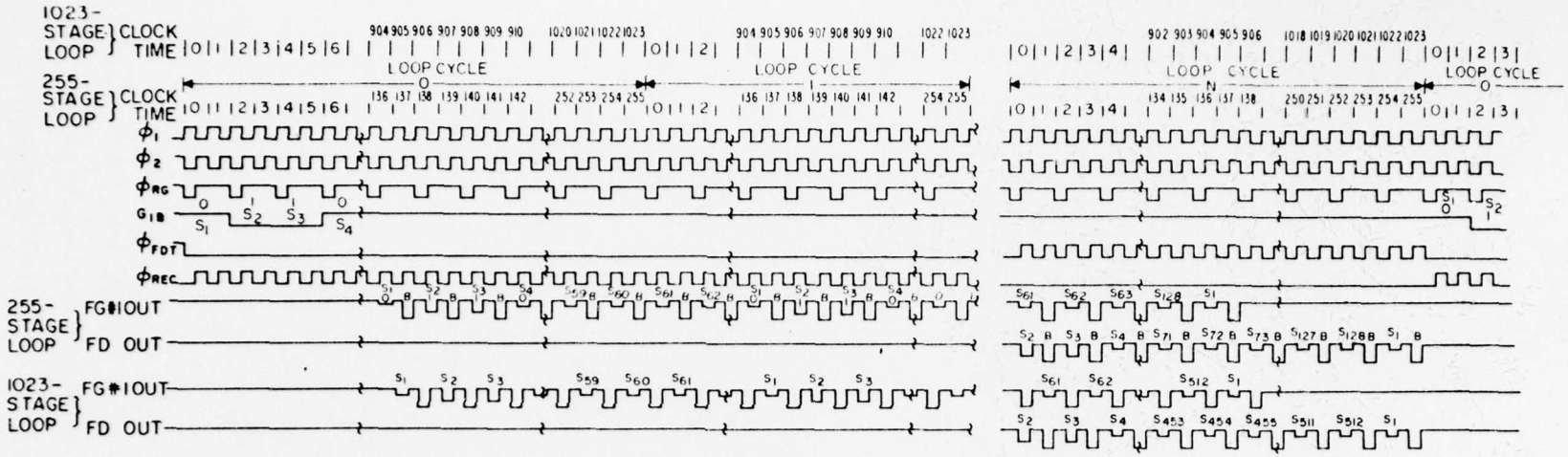

Figure 18. Timing diagram for the 255-stage and 1023-stage, closed-loop CCDs.

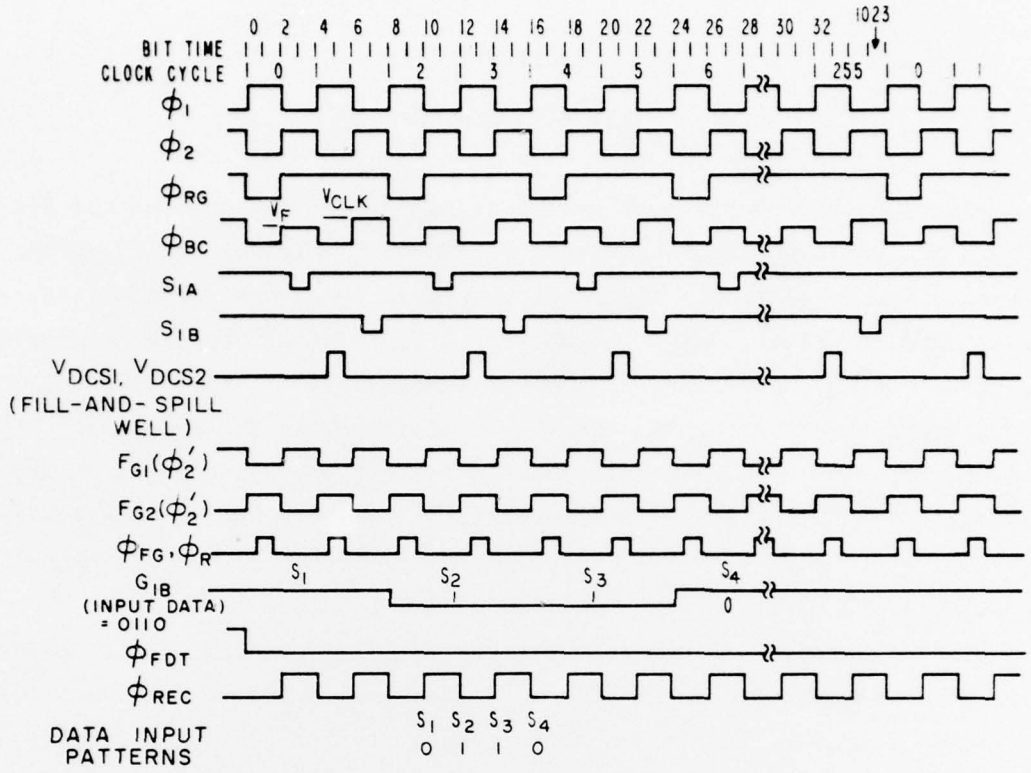

Figure 19. Detailed timing diagram of loop cycle 0 in Fig. 18.

in each loop cycle, and the bias charge trailing behind signal S_1 appears at clock time 137 as shown in Fig. 18.

During loop cycle N the signals are transferred to the floating-diffusion output by applying pulses to ϕ_{FDT} and inhibiting ϕ_{REC}. The first signal to appear at the floating-diffusion output (during clock time 0) is S_2. Signal S_1 appears during clock time 254 after signal S_{128} at the end of the data stream. This reordering of data is due to a two-stage differential delay between the input stage to the merged input junction and the floating-diffusion output stage to the merged input junction. A total of 256 clock cycles are used per loop cycle in the 255-stage CCD loop because of the extra 1-clock cycle delay in the regeneration stage.

The timing for operation of the 1023-stage, CCD loop is very similar to that for the 255-stage, CCD loop and is also shown in Fig. 18. In this case, a total of 512 signals are stored in the low-loss mode of operation.

SECTION V

TEST ELECTRONICS

A microprocessor-based test system is being designed to test the TC1230 low-loss, closed-loop CCDs rather than a hard-wired digital logic system. This will allow considerable flexibility in generating the various clock pulses needed to drive the CCD so that the effects of alternative timing configurations and operating modes may be evaluated more readily. The TC1230 test system is based on the RCA COSMAC VIP (Video Interface Processor) which is a complete computer on a single printed-circuit board and includes the following: (1) RCA CDP1802 Microprocessor, (2) 4K-byte RAM, (3) built-in hexidecimal keyboard, (4) graphic video display interface, and (5) magnetic-tape cassette interface.

A block diagram of the microprocessor-based TC1230 test system is shown in Fig. 20. The microprocessor is used to initially load an auxiliary high-speed static Schottky TTL RAM which can then be cycled to provide any desired CCD clock rate up to about 10 MHz. This, in effect, provides a programmable high-speed multichannel word generator. The TTL outputs on each channel are further buffered by MH0026 MOS clock drivers and clamping circuits to provide variable amplitude pulses with adjustable dc bias for driving the CCD. Each timing configuration can be stored on a magnetic-tape cassette for later use in loading the auxiliary TTL RAM.

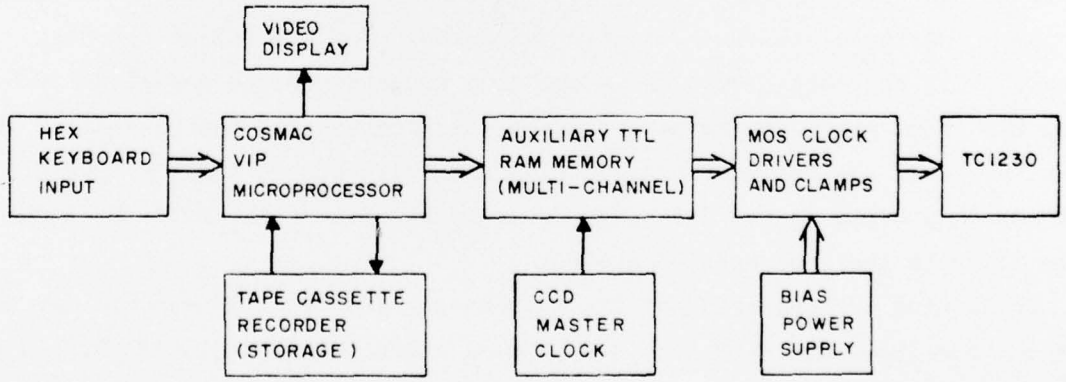

Figure 20. TC1230 test system.

A more detailed block diagram showing the auxiliary high-speed TTL RAM for one output channel is contained in Fig. 21. During the initial loading operation of the high-speed RAM by the microprocessor (μP), each 82S09 RAM is loaded in sequence with 64 bytes of waveform data from the μP 8-bit data bus. The Driver Address from the μP data bus is decoded with a CD4515 decoder latch to select the 82S09 RAM to be written to. The RAM address is obtained from the Load Address on the μP data bus through a CDP1852 8-bit output port and a 74157 address-line select switch (multiplexer). When the loading operation for the RAMs is completed, all of the RAMs are selected in a Read mode. The memory addresses are now obtained from the bit time counter 74161 (or cycle counter 74161) through the 74157 address multiplexer. The 8-bit output from the 82S09 RAMs are converted to a serial waveform data stream by a 82S30 high-speed 8-bit multiplexer. Thus, a serial output up to 512 bits long is obtained for each channel. By using a second 82S09 RAM together with an AND gate as a sequencer on the same channel, a pattern length of 262,144 bits may be obtained. This 256K-bit-long pattern length is needed on channels which control data input and CCD loop-switching functions. Other channels, such as the 2-phase clock, will be running continuously and therefore do not require the additional 512-cycle RAM sequencer. Table 2 lists the driver channels and signal names which are required by the TC1230 low-loss CCD test chip.

The format of the data for specifying clock waveforms on a particular driver channel is illustrated in Fig. 22. Each 32-bit data word consists of four 8-bit (2 hexidecimal digit) fields. The first field specifies the driver address (DA). The second field specifies the load address (LA) (which is equal to the bit time divided by 8) at which 8 bits of waveform data contained in the fourth field begin. The third field may be used to repeat the same waveform byte in the next load address in sequence up to a maximum of 63 times which would fill the entire 512-bit capacity of the RAM. As mentioned, the fourth field contains the 8 bits of waveform data (waveform byte) which start at the specified load address. An example of the data format specifying the beginning of the waveform on driver #7 is shown in Fig. 23. If the waveform is highly repetitive, a single 32-bit data word is sufficient to specify the entire waveform by using the repeat feature. This is illustrated in Fig. 24 which shows the waveform for ϕ_1 on driver #11.

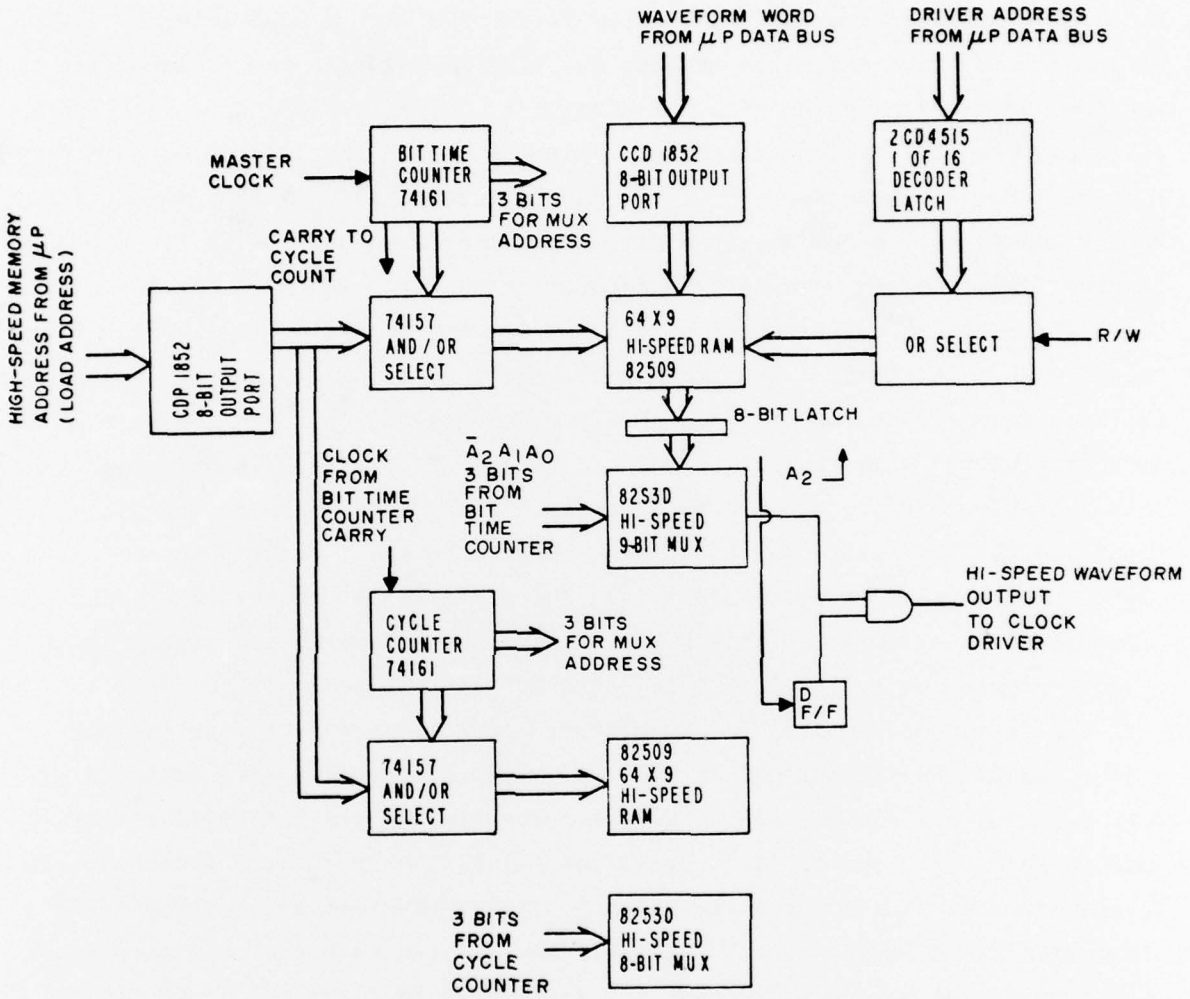

Figure 21. Auxiliary high-speed RAM for TC1230 test system.

TABLE 2. TC1230 DRIVER CHANNELS

DRIVER CHANNEL	PATTERN LENGTH	SIGNAL	DESCRIPTION
1	256K	S_{1A}	INPUT SOURCE STROBE (DATA)
2		S_{1B}	INPUT SOURCE STROBE (BIAS CHARGE)
3		ϕ_{FDT}	FLOATING-DIFFUSION TRANSFER GATE
4		ϕ_{REC}	RECIRCULATION GATE
5		G_{1A}	DATA INPUT
6		(SYNC)	PROGRAMMABLE EXT. SYNC
7		(SPARE)	
8	512	$\phi_{RGT,RGS}$	REGENERATOR GATES
9		$\phi_{BCT,BCS}$	BIAS CHARGE GATES
10			
11		ϕ_1	CLOCK ϕ_1
12		ϕ_2	CLOCK ϕ_2
13		V_{FG}	FLOATING-GATE RESET DRAIN
14		ϕ_{FG}	FLOATING-GATE RESET GATE
15		ϕ_{DCS1}	DARK-CURRENT SUBTRACTION GATES
16		ϕ_{DCS3}	
17		ϕ_{DCS2}	
18		ϕ_R	FLOATING-DIFFUSION RESET GATE

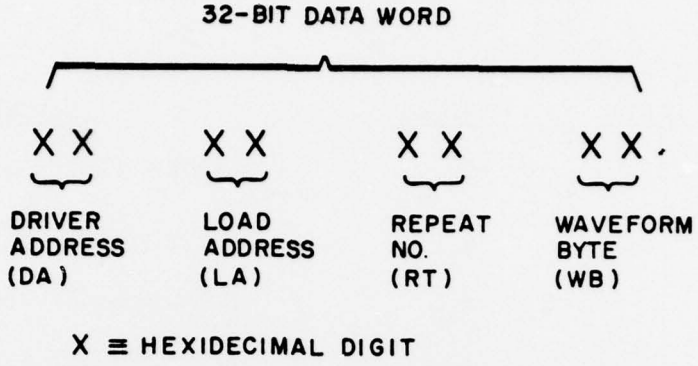

Figure 22. Waveform data format of TC1230 test system.

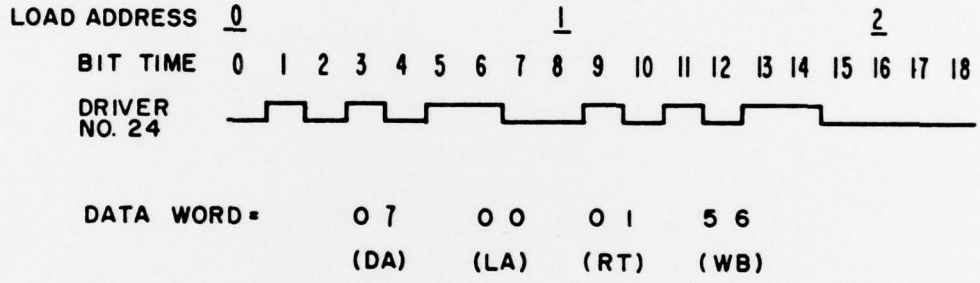

Figure 23. Example waveform for driver #7 of TC1230 test system.

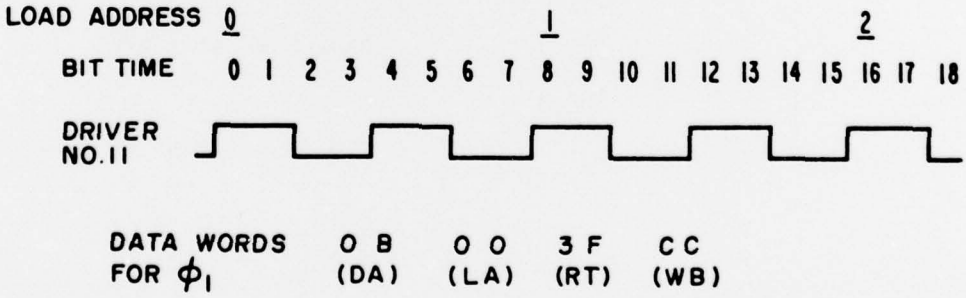

Figure 24. Clock ϕ_1 waveform of driver #11 of TC1230 test system.

SECTION VI

CONCLUSIONS

Experiments with the 128-stage, surface-channel CCD register demonstrated the general validity of our low-loss CCD concept. This test demonstrated that to achieve a substantial reduction of the transfer losses, the low-loss CCD must be operated wih a large trailing bias charge. In this test the measured transfer loss of the conventional CCD mode was about 5×10^{-4} per transfer, while in the low-loss CCD mode with large trailing bias charge, the transfer loss was estimated to be about 10^{-5} per transfer.

On the basis of the analysis in Section II B, a buried-channel CCD that in the conventional CCD mode has a transfer loss of 10^{-5} per transfer should have a minimum effective charge-transfer loss of about 5×10^{-8} per transfer for signal-regeneration stages spaced every 447 transfers. Clearly, such very low transfer losses can be demonstrated experimentally only with either a very long CCD register or the closed-loop CCD structures such as will be constructed as part of the low-loss CCD test chip.

The low-loss CCD test chip will be fabricated and studied in the second half of this program and the results will be reported in the Final Report. In this report we have described the design, layout, and the operation of two closed-loop, low-loss CCD structures. Operating in the low-loss CCD mode, these closed-loop CCDs will be able to store or recirculate 128 and 512 signal samples, respectively.

The dark-current subtraction stages included in the closed-loop CCD structures of the low-loss CCD test chip should extend the maximum useful delay time of long CCD delay lines for applications where the signal-to-noise ratio of the input signal is inherently lower than the dynamic range of the CCD. The upper limit on the effectiveness of the dark-current subtraction stage will depend on to what extent the dark current is independent of the signal level. The operation of the dark-current compensation stage described in this report should be capable of removing from the trailing bias-charge wells the excess charge due to the dark-current generation. But removal of the signal-charge-dependent component of the dark current will require a more sophisticated dark-current subtraction procedure.

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