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RADC-TR-78-231
Final Technical Report
October 1978

# RADIATION HARDENED MICROPROCESSOR TECHNOLOGY STUDY

J. P. Spratt
D. Z. Harbert

QUESTRON Corporation

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# REPORT DOCUMENTATION PAGE

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|---|---|
| 1. REPORT NUMBER: RADC-TR-78-231 | 2. GOVT ACCESSION NO. |
| 3. RECIPIENT'S CATALOG NUMBER | |
| 4. TITLE (and Subtitle): RADIATION HARDENED MICROPROCESSOR TECHNOLOGY STUDY. | 5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report. June 1977 - March 1978. |
| 6. PERFORMING ORG. REPORT NUMBER: N/A | |
| 7. AUTHOR(s): J. P. Spratt, D. Z. Harbert | 8. CONTRACT OR GRANT NUMBER(s): F19628-77-C-0177 |
| 9. PERFORMING ORGANIZATION NAME AND ADDRESS: QUESTRON Corporation, 2727 Camino Del Rio S., Suite 125, San Diego CA 92108 | 10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62702F, 46002021 |
| 11. CONTROLLING OFFICE NAME AND ADDRESS: Deputy for Electronic Technology (RADC/ESE), Hanscom AFB MA 01731 | 12. REPORT DATE: October 1978<br>13. NUMBER OF PAGES: 108 |
| 14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same | 15. SECURITY CLASS. (of this report): UNCLASSIFIED<br>15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A |

16. DISTRIBUTION STATEMENT (of this Report)

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17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Walter M. Shedd (ESE)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Metal-oxide-semiconductor
Radiation hardening
Large scale integration
Integrated injection logic
Transistor-transistor logic
Complementary MOS
N-channel MOS

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report discusses four LSI technologies-NMOS, TTL, CMOS and $I^2L$-relative to their current and projected capabilities in both the commercial and the radiation hardened markets. The state-of-the-art in radiation hardened digital electronics is described along with a discussion of design techniques that may be used to apply LSI to hardened systems. Finally, a preliminary analysis of radiation testing of a microprocessor bit slice is provided.

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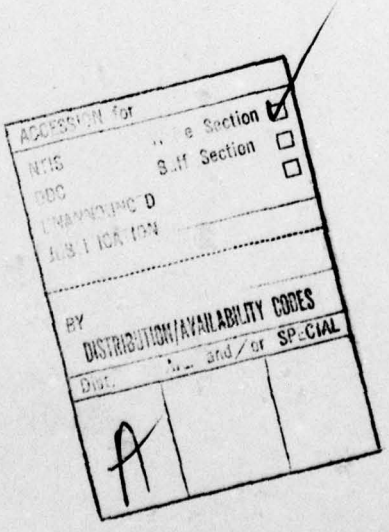
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1. This report is the Final Report on the contract. It contains a state of the art technology survey on radiation hardened, large scale integrated circuits and microprocessors. The work was performed over a 12 month period from June 1977 to June 1978. The objective of the work was to assess the state of the art in the radiation tolerance of microprocessors and to formulate recommendations for future R&D programs. The report can be used as a review of the current state of art in radiation hardened microprocessors and an assessment of the ability of commercial LSI circuitry to meet nuclear radiation requirements.

2. The above work is of value since it provides an assessment of the capability of current hardened and commercial LSI circuits to meet nuclear radiation requirements as well as an estimate of the manufacturability and commercial viability of various LSI technologies.

Walter M. Shedd

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## 1.0 Introduction

The Department of Defense has been studying and designing radiation hardened weapon systems since the late 1950's. Hardened system deployment began in 1965 when Minuteman II's were fielded which incorporated electromagnetic pulse (EMP) hardening. Radiation hardened integrated circuits were deployed somewhat later in Minuteman II and were used in Minuteman III and Poseidon. The computers in these missiles were built with bipolar, dielectrically isolated small scale integrated circuits. These IC's were developed specifically for the ICBM's and never found any other significant applications.

During the late 50's and 60's, the government heavily influenced the direction of IC development by spending tens of millions of dollars for the hardened IC's and for the ultra-reliable IC's used in Apollo. In the late 60's several semiconductor firms including Radiation Inc. (now Harris Semiconductor), Bendix Fairchild, National, Philco-Ford, Signetics, Texas Instruments, and Motorola, were actively pursuing the radiation hardened semiconductor market. The radiation hardened parts were functionally equivalent to the popular commercial diode-transistor logic (DTL) and/or transistor-transistor logic (TTL) of the time, and thus the manufacturing processes were similar to the processes being used for the commercial product. Certainly there were differences in the processes such as junction isolation and diffused resistors for the commercial IC's versus dielectric isolation and thin film resistors for the hardened IC's. But by and large, the two product lines complemented each other very well.

At about the time initial Minuteman III deployment began ($\sim$1970), the semiconductor world began to produce Schottky clamped bipolar TTL and various forms of metal – oxide – semiconductor (MOS) such as P-channel MOS, N-channel MOS, and complementary MOS. The bipolar and MOS technologies were also competing in the radiation hardened world, and when the Navy made the technology decision for Trident C4 (in about 1972), they selected the more traditional approach – dielectrically isolated TTL. TTL was selected primarily because it had a proven reliability and radiation performance record and because the MOS processes were very sensitive to total ionizing dose. The Navy developed two variations of hardened TTL – Schottky clamped and non-Schottky clamped.

The family of Schottky DI parts includes nine part types functionally equivalent to IC's being used in commercial computers in 1972. These parts were developed over a five year span and are the most advanced radiation hardened digital IC's available today. The Navy has one qualified source for the Schottky parts (RCA) and the Air Force is developing similar parts at Harris and Texas Instruments as well as RCA for application in Missile-X.

As the Navy was developing radiation hardened SSI and MSI, the IC manufacturers were rapidly developing and producing both MOS and bipolar LSI. In fact, during the time the ICBM community has been developing hardened versions of 1972 SSI/MSI, the commercial IC world has come from 1024-bit random access memories (RAMS) and four-bit microprocessors to 16384-bit RAMS and 16-bit microprocessors. Not only is the hardened IC world currently some 5 years behind the commercial world, the gap is very likely going to widen because the most popular LSI technology today and for the foreseeable future is the radiation sensitive N-channel MOS. This situation is developing primarily because there is not enough of a market for radiation hardened IC's to entice the manufacturers to use their top engineering talent and modern production facilities to address hardening problems. On the other hand, performance requirements for many military systems, especially avionics, satellites, and command, control, and communication ($C^3$) almost mandate LSI. In fact, systems with total dose radiation requirements are already developed using NMOS LSI, so that applications for which radiation hardness has not previously been a problem must now include this in their technical requirements list.

The dilemma is then simply that the radiation hardened IC technology is 5 years behind the main thrust of the semiconductor industry and falling further behind all the time. The problem is complicated by the fact that microprocessor testing is still an evolving art and techniques for functional and electrical testing have been slow in developing while techniques for radiation testing are, at best, very rudimentary.

This report addresses the dilemma by analyzing LSI technologies relative to radiation hardening, current and projected military computers, and radiation testing of LSI. The LSI microprocessor technologies selected for analysis are NMOS, TTL, $I^2L$, and CMOS. Each is assessed relative to two basic criteria – commercial viability and hardenability. Several subelements are used to analyze each criterion:

- Commercial Viability
  - Speed
  - Power
  - Density
  - Product Base
  - Market Projections
  - Technical Vitality
  - Technical Problems
- Hardenability
  - Fast Neutrons
  - Transient Gamma and X-Rays
  - Total Dose Gamma and X-Rays
  - Energetic Electrons
  - Thermal Radiation
  - EMP

To put the microprocessors in perspective relative to military computers, three classes of hardened systems are analyzed – ICBM's, satellites, and manned systems. These three categories cover virtually all the possible radiation environments and encompass all types of applications including $C^3$ systems. Computers currently being used are described along with some prognostication about the next generation of hardened computers. The problem of microprocessor radiation testing is also considered and testing techniques are suggested.

## 2.0 Technology Assessment

This portion of the report is an assessment, from the point of view of the computer designer, of the state of the art of radiation hardened LSI/VLSI technology as of 1978, and a projection as to directions which this technology might profitably take in the 1980-1990 time frame.

### 2.1 Basis For Assessment

This section presents the basis of the assessment, viz. the factors to be used, and a discussion of the weighting to be given to these factors.

#### 2.1.1 Factors

The factors to be used in this assessment are the commercial viability of a technology and the "hardenability" of the technology. Commercial viability will be estimated from the technical characteristics of the technology (speed, power, etc.), the present product base, market projections, technical vitality (as judged from recent technical publications), and technical problem areas. The "hardenability" of a technology will depend upon the detailed nature of the expected environment, and the nature of the failure modes to which a given technology is susceptible. These will obviously be different for the different application categories and the different technologies, so that the definition of "hardness" is to some extent variable. In general, the environmental components to consider in assessing radiation hardness are:

- Fast neutrons (energy $>$ 10 keV)
- Gamma rays, both total dose and dose rate
- Energetic electrons (both flux and fluence)
- X-rays
- Thermal radiation
- EMP

These components interact with LSI/VLSI devices in a complex fashion to introduce transient (T), semipermanent (S), and permanent (P) effects. The interaction proceeds in any of four possible ways, viz. ionization, atomic displacement, electromagnetic induction, and heating. Electrical changes can be produced by these interactions which affect the properties of the basic devices used in LSI/VLSI. Figure 2-1[1] indicates the nature of some of these damage mechanisms, their temporal nature (i.e. temporary, semipermanent, or permanent), and the type of devices which are susceptible (e.g. bipolar, MOS, etc.). In the hardness assessments which follow, the damage mechanism(s) felt to be most important for the technology in question will be addressed – the others can be assumed to be substantially less important, in terms of system performance degradation.

### 2.1.2 Weighting

The weight to be given to the factors cited above (commercial viability vs. hardenability) will depend upon the existence of and cost of alternate ways to accomplish the system mission. ICBM guidance computers must obviously place great emphasis on radiation hardening. On the other hand, their computational requirements are not particularly demanding. Such systems might, therefore, opt for a much lower level of integration than would be acceptable in other high performance applications, since conventional hardening approaches are less expensive to implement at low levels of integration. Section 3.0 of this report deals with radiation hardened computer applications, both present and projected, and indicates some considerations involved in establishing weighting factors.

## 2.2 Candidate Technologies

The technologies which have shown potential for use in military LSI/VLSI applications are NMOS, TTL, $I^2L$, and CMOS (on bulk silicon, or silicon on sapphire), listed in order of decreasing 1977 commercial LSI/VLSI sales. Each has demonstrated its utility in both random logic and

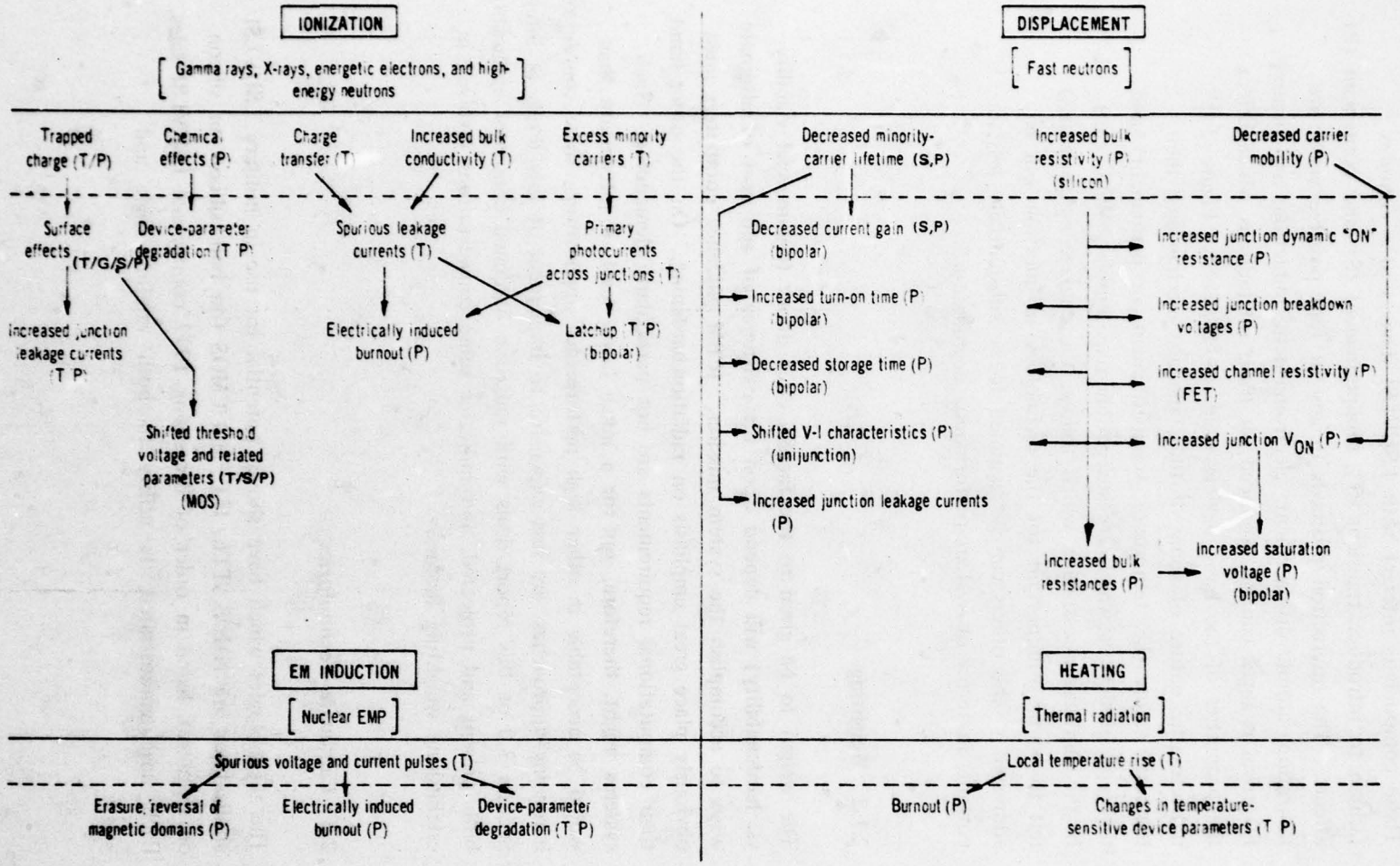



FIGURE 2-1 TREE/EMP DAMAGE MECHANISMS IN ELECTRONIC DEVICES

memory applications, and consequently must be regarded as a candidate for the role of radiation hardened LSI/VLSI technology. (Non-volatile memory technologies will not be discussed here. Their importance and technical complexity require separate treatment).

### 2.2.1 NMOS

#### 2.2.1.1 Commercial Viability

MOS devices can be of two types, viz. P-channel and N-channel. The latter gives superior performance because of its higher speed (due to higher mobility of electrons in N-channels than can be achieved for holes in P-channels, all other relevant parameters being assumed equal). For this reason almost all second generation microprocessors use N-channel technology. Only now, with the advent of high performance 16 bit microcomputers, is any serious process competition to NMOS appearing. (Fairchild's 9440 $I^2L$ microcomputer), and it will have a difficult time beating out the NMOS competitors (Intel's 8086, Zilogs Z8000, and Texas Instruments 9900).

##### 2.2.1.1.1 Description of Process

To date, almost all NMOS microprocessors have used self-aligned silicon gate technology, <100> orientation silicon, thin gate oxide, and ion implantation doping techniques to achieve low threshold voltages for TTL compatibility and to permit attainment of the speed inherent in N-channel. It is not yet clear, however, which N-channel MOS processes will be used in the future. Several alternatives have been suggested,[2,3,4] viz. HMOS (Intel and AMD), VMOS (AMI and T.I.), and DMOS (Japan).

- HMOS is the name used by Intel (the first manufacturer to announce products using this technique) to describe an advanced form of short channel silicon gate NMOS technology in which improved performance is obtained by device scaling. Table 2-I[5] compares 1977-1978 versions of HMOS to its predecessors in the NMOS genealogy, and indicates where Intel feels the scaling approach will take them by the early 1980's. The high speed

TABLE 2-1

Evolution of MOS Device Scaling

| Device/Circuit Parameter | Enhancement Mode NMOS, 1972 | Depletion Mode NMOS, 1976 | HMOS 1977 | MOS 1980 |
|---|---|---|---|---|
| Channel Length, L($\mu$m) | 6 | 6 | 3.5 | 2 |
| Lateral Diffusion, $L_D$ ($\mu$m) | 1.4 | 1.4 | 0.6 | 0.4 |
| Junction Depth, Xj($\mu$m) | 2.0 | 2.0 | 0.8 | 0.8 |
| Gate Oxide Thickness $T_{ox}$(Å) | 1200 | 1200 | 700 | 400 |
| Power Supply, $V_{cc}$(V) | 4-15 | 4-8 | 3-7 | 2-4 |
| Shortest Gate Delay, $\tau$ (ns) | 12-15 | 4 | 1 | 0.5 |
| Gate Power, $P_D$ (mw) | 1.5 | 1 | 1 | 0.4 |
| Speed-Power Product | 18 | 4 | 1 | 0.2 |

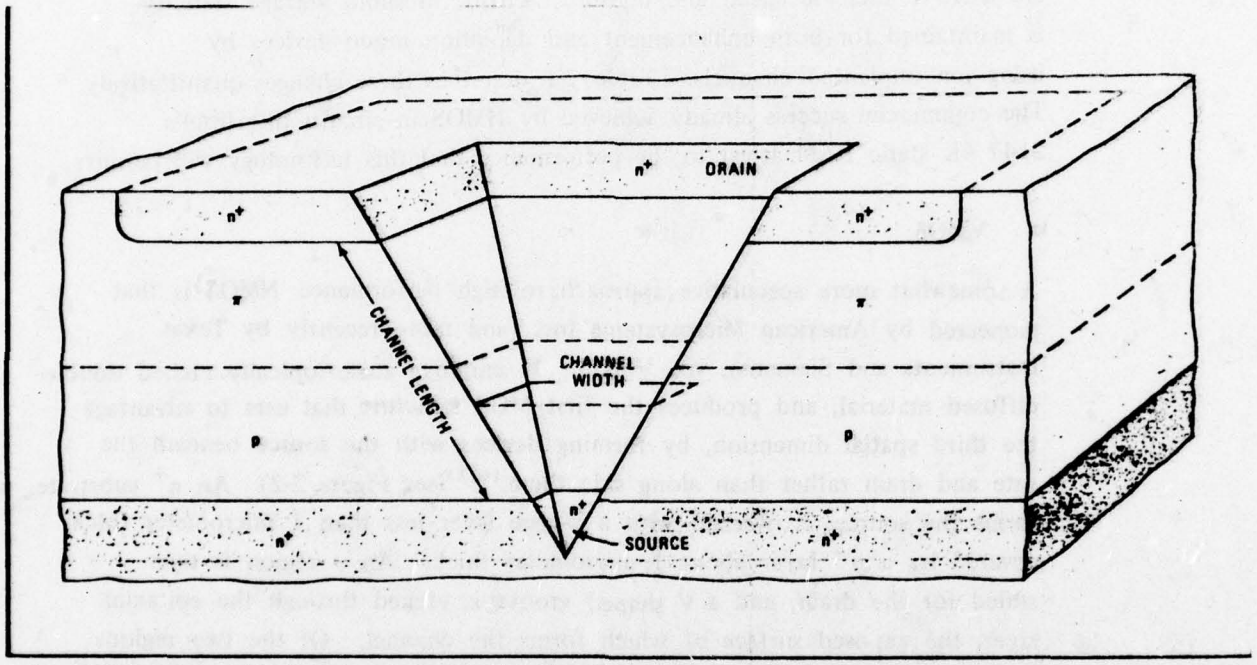
and high density of HMOS are achieved through five major changes in the older Si gate NMOS technology. First, a high resistivity substrate (50 ohm-cm, p-type material) is used to lower junction capacitance, reduce substrate body effects, and increase effective carrier mobility. Second, the gate oxide thickness is decreased to improve device gain and punch-through voltage, and reduce body and short channel effects. Third, junction depth is decreased by using arsenic as the source-drain dopant. This reduces parasitic junction capacitance and gate-drain Miller capacitance, and permits higher packing density. Fourth, narrow channels are used to increase speed and density. Fifth, threshold voltage stability is maintained for both enhancement and depletion mode devices by using ion implanted channels. Table 2-1 describes these changes quantitatively. The commercial success already achieved by HMOS in circuits like Intel's 2147 4K static RAM attest to the performance that this technology will permit.

- VMOS

A somewhat more speculative approach to high performance NMOS is that pioneered by American Microsystems Inc. (and more recently by Texas Instruments and Siemens), viz. VMOS. It employs anisotropically etched double-diffused material, and produces the first MOS structure that uses to advantage the third spatial dimension, by forming devices with the source beneath the gate and drain rather than along side them.[6,7](see Figure 2-2) An $n^+$ substrate, which forms the source, is overlaid with a p-type layer less than 1 micrometer thick, covered by a $p^-$ layer about 1 micrometer thick. An n region is then added for the drain, and a V shaped groove is etched through the epitaxial layer, the exposed surface of which forms the channel. Of the two regions in the channel, the p layer has the higher threshold and thus usually determines the overall transistor threshold and effective channel length over a wide region of operation. The $p^-$ region reduces the drain-to-source capacitance, prevents punch-through, and prevents drain-induced threshold reduction (short channel effects). The channel width, W, is determined by the perimeter of the V groove, and hence is large, permitting high drive currents. Since the source is below the drain, it occupies no surface area, thereby improving packing densities. Furthermore, the $n^+$ source also serves as a

**FIGURE 2-2**

**The V-MOS Structure**




**1. The V-MOS structure.** A V-shaped groove is etched into the surface of the silicon down through all the n+ and p layers, and the channel is formed on the slopes of the groove. To save surface area, the source is in the body of the silicon, beneath the drain.

ground plane, which helps chip utilization (VMOS provides four unrestricted levels of interconnection, viz. the ground plane, diffusions, polysilicon, and metal).

Table 2-2 compares today's HMOS, and the performance expected from HMOS in the early 1980's to today's VMOS. It can be seen that VMOS, in principle, has a better packing density, but pays for this advantage with a more complex process. Also, VMOS yields an asymmetric device that must be used in one direction only. Thus LSI logic configurations are more difficult to achieve than with more conventional n-channel approaches. Finally, the producibility and long term reliability of VMOS has yet to be shown. New technologies can give rise to peculiar problems which have not previously been met, delaying or even preventing customer acceptance. For example, VMOS devices have been found to have lower gate oxide breakdown voltages for a given oxide thickness than HMOS devices. VMOS processing of 1000Å oxide results in 25-35 volt performance, as opposed to 60-80 volt performance for HMOS. This is due to higher electric fields in the oxide at the bottom of the V-groove. The ability to scale VMOS processes down to the 400 to 700Å range may be affected by the presence of this failure mode, unless a fix can be found.

- DMOS

The third approach to high performance N-channel MOS is the so-called diffusion self-aligned, enhancement-depletion MOS process,[4,8] called DSA-MOS or DMOS. It permits short-channel performance levels to be obtained within present photolithographic limits (i.e. without short channels). Speed-power products less than 1 pj, switching times in the ns. regime, and packing densities of 200 gates/mm$^2$ or higher are claimed for it. Several counter arguments are presented against it, however. First, despite being around for about seven years, it has developed no strong supporters among American semiconductor manufacturers. In fact, even Japanese manufacturers appear at the moment to be concentrating on HMOS. This may be due to the processing complexity associated with DMOS. Second, the technology seems to have a high sensitivity of threshold voltage to process variations[9]—obviously undesirable in an LSI/VLSI process. Process variations designed to eliminate this sensitivity result in something looking very much like VMOS.

TABLE 2-2

Comparison of HMOS and VMOS Technologies

| Parameter | HMOS 1977-78 | HMOS 1980+ | VMOS 1977-78 |
|---|---|---|---|
| Layout Density (gates/mm$^2$) | 170 | 200 | ~220 |
| Gate Delay(ns) | 1 | 0.4 | ~1 |
| Gate Power(mw) | 1 | 0.5 | ~1 |
| Speed Power Product | 1 | 0.2 | ~1 |
| Number of Thin Films | 2 | 2 | 3 |
| Number of Implants | 3 | 3 | 3 |

#### 2.2.1.1.2 Present and Projected Commercial Product Base

The original MOS technology, and the one applied to the first monolithic processors, was P-channel. Because of inherent speed shortcomings it has been almost completely eclipsed by N-channel devices. Table 2-3[10] describes the commercial market for microcomputer kits. This market is representative of the total LSI/VLSI market from 1977 through 1980. All the chips listed as examples up to the 9440 are NMOS (expect for the Cops Chip). Based on this data, it appears that about 90% of 1977 microcomputer sales were NMOS products (The 9440 was not formally introduced until January 1978[11], and therefore was assumed not to have been a factor in 1977 sales). Clearly, NMOS meets the requirement of commercial viability.

#### 2.2.1.1.3 Technical Vitality

Of 37 papers presented at the 1978 International Solid State Circuits Conference which dealt with LSI/VLSI (papers dealing with microwave devices, linear devices, etc. were not included) the division according to the technology addressed was as follows:

TABLE 2-4

LSI/VLSI Papers at 1978 Solid State Circuits Conference

| Technology | Number of Papers |
|---|---|
| NMOS | 16 |
| TTL | 6 |
| Miscellaneous | 6 |
| CMOS(Bulk) | 5 |
| $I^2L$ | 3 |
| CMOS/SOS | 1 |
| TOTAL | 37 |

Such emphasis on one technology over all others is an indication of the direction which technical effort in the commercial LSI/VLSI area is taking. It would be virtually impossible for a new technology to burst, fully

## TABLE 2-3

### Total Available Market, Microcomputer Components (CPU, RAM, ROM, I/O)

| | | 1977 | 1978 | 1979 | 1980 |
|---|---|---|---|---|---|
| VERY LOW END | DOLLARS IN MILLIONS | 10 | 20 | 40 | 75 |
| (TMS1000, 8021, COPS) | NUMBER OF KITS | 2.5M | 6.6M | 16M | 38M |
| | CPU ASP * | $4 | $3 | $2.50 | $2 |
| | UNIT/KIT | 1 | 1 | 1 | 1 |
| LOW END | DOLLARS IN MILLIONS | 50 | 70 | 90 | 115 |
| (8048, 3870, F-8, SC/MP) | NUMBER OF KITS | 1.4M | 2.8M | 4.5M | 9M |
| | CPU ASP | $15 | $10 | $8 | $6 |
| | UNIT/KIT | 5 | 4 | 3 | 2 |
| MID-RANGE | DOLLARS IN MILLIONS | 95 | 145 | 175 | 225 |
| (8080, 8085, Z-80, 6800) | NUMBER OF KITS | 1.12M | 1.81M | 2.3M | 3.2M |
| | CPU ASP | $6 | $6 | $6 | $5 |
| | UNIT/KIT | 17 | 17 | 17 | 18 |
| HIGH END | DOLLARS IN MILLIONS | 5 | 35 | 65 | 90 |
| (8086, Z-8000, 9900, 9440) | NUMBER OF KITS | 140K | 620K | 1M | 1.31M |
| | CPU ASP | $30 | $27 | $24 | $20 |
| | UNIT/KIT | 29 | 28 | 28 | 25 |
| BIT SLICE | DOLLARS IN MILLIONS | 14 | 21 | 28 | 32 |
| (2900) | NUMBER OF KITS | 120K | 235K | 340K | 450K |
| | CPU ASP | $9 | $7 | $6 | $5 |
| | UNIT/KIT | 60 | 55 | 65 | 45 |
| TOTAL | DOLLARS IN MILLIONS | $174 | $291 | $398 | $537 |

*AVERAGE SALES PRICE

developed, on the technical scene without having enjoyed a development period of several years during which its progress was reported at this conference. One can therefore assume that NMOS will continue to be the prime candidate for the role of commercial LSI/VLSI technology for several years, at least.

#### 2.2.1.1.4 Problem Areas in Commercial NMOS Technology

Technical problems which may inhibit further development of NMOS in the 1980's occur in the area of power dissipation, speed, size reduction, and reliability.

- Power Dissipation

Pashley, etal,[5] have shown that scaling HMOS down to the short channel (L=2$\mu$m) region will require reducing the power supply voltage, $V_{DD}$, to the 2 to 4 volt range. Customers may be reluctant to do this, especially since it is not necessary with VMOS[12].

Reductions in power dissipation can be achieved by reducing the logic signal swing, thereby reducing the power dissipated in charging and discharging nodal capacitances.[13] Noyce[14] has shown, however, that there is a limit to how far this can be carried. The logic swing $\Delta v$ obviously must exceed kT/q for logic states to be stable, and should be $\gg$ kT/q for speed. Thus $\Delta v$ probably cannot be reduced below .25 to .5 volts. An OFF/ON ratio of 10 kT/q gives a junction current ratio of $e^{10}$, or 22,026. This is a much smaller ratio than has been used to date, and would lead one to favor static memories rather than dynamic to avoid the excessively high refresh rates which would be required for dynamic memories. In short, ultimate memory performance will be obtained in static memories, where refresh is not required.

- Speed

Short channels are required to get high speed performance from NMOS. In addition, however, parasitic resistance must be reduced. This is especially true

since the device current will rise as $V_{DD}$ is reduced (since total power stays the same). Sheet resistance of poly silicon runs is already becoming a speed limiting factor. Thus, pressure will grow for refractory metal self-aligned gate processes such as molybdenum gate processes.[15] Substantial reductions in the series resistance of runs can thereby be made.

- Size Reduction

Dimensional reduction is essential to achieve the technological limits in speed and level of integration. Advanced lithography methods are under development to permit this reduction, and of the three schemes which have been suggested[16], X-ray lithography appears to offer the best ultimate performance. Noyce[14] has estimated that the continuing improvement in dimensional reduction seen for the past twenty years will eventually stop at about 1$\mu$m minimum line width, which should be achieved about 1990. Substantial effort will be required to achieve this goal, and problems such as radiation effects in sensitive gate oxides resulting from X-ray or E-beam lithography operations will have to be solved in the process.

- Reliability

Electromigration of metallization lines will become increasingly troublesome as chip currents increase. Copper or manganese doping of aluminum is already being used to reduce electromigration, but more work must be done in this area.

VMOS has been found to have a unique failure mode which could affect its utilization, viz. oxide breakdown voltages reduced from that of HMOS devices of comparable gate oxide thickness[17] Rodgers[12], however, feels that this will not prevent the utilization of the excellent packing densities achievable in VMOS memories, since gate breakdown voltages, although lower, are much more tightly bunched than with conventional planar oxides.

### 2.2.1.2 Hardenability of NMOS

Few studies of the radiation hardness levels of N-channel microprocessors have been reported in the open literature. Consequently, estimates of the hardenability of the technology will have to be based on the most general considerations. With this warning, an assessment will be attempted of the total ionizing dose, ionizing dose rate, and neutron hardness of NMOS.

#### 2.2.1.2.1 Total Dose Hardness

Both Measel [18] and Myers[19, 20] have studied total dose effects on commercial NMOS products, and have found the onset of failures to occur at about $10^3$ rads(Si), with essentially all parts failed by $3 \times 10^3$ rad(Si) if the radiations took place with bias applied. Samples irradiated while unbiased showed failures beginning to occur at $10^4$ rads(Si). Myers found these failures to be due to threshold voltages shifts in excess of the 0.2 volt shifts which these designs will tolerate. He also found that certain process changes (such as thinner gate oxides, and lower temperature postgate processing) resulted in a ten-fold increase in hardness ($10^4$ rads(Si) was the onset of failures) at the cost of reduced chip yield. Another radiation induced failure mode of concern in NMOS devices is that arising from surface inversion under the field oxide. It has been estimated[21] that this mechanism will cause LSI/VLSI failure at approximately $5 \times 10^4$ rads(Si). If success is achieved in hardening NMOS processes against excessive threshold voltage shifts as proposed by Myers[19,20] then the next task to be addressed would be field oxide hardening. The possibility exists that standard memory chip or microprocessor designs, implemented in chips processed according to special "rad. hard processing rules" and used in systems taking advantage of dormancy and chip redundancy, may be capable of meeting total dose hardness goals of manned systems. In view of the ubiquitous nature of NMOS LSI/VLSI in military electronic systems, and the importance of software and support commonality, such a possibility merits careful study by DOD users.

#### 2.2.1.2.2 Dose Rate Hardness

Even less information is available about dose rate effects in NMOS than is available about total dose effects. Measel[18] and Myers[22] report upset dose rate levels of $1.8 \times 10^5$ and $1 \times 10^5$ rads(Si)/sec respectively.

This relatively low level is somewhat surprising in view of the self-isolating nature of NMOS technology. Further study is required here to determine whether this premature logic upset is due to photocurrent generation, or to severe rapid annealing factors in commercial oxides. If the latter is responsible, hardening the oxide may improve logic upset as well as total dose hardness.

#### 2.2.1.2.3 Neutron Hardness

Neutron hardness is generally conceded to MOS devices of all types. In view, however, of the very high resistivities being used in advanced NMOS processes (up to 200 ohm-cm), carrier removal (resistivity changes) must be considered as a real potential damage mechanism. The resistivity of the P-type wafer on which NMOS is fabricated will, after being exposed to a neutron fluence $\emptyset$ neutrons/cm$^2$, be related to $\rho_0$, the pre-radiation value by the equation

$$\rho(\emptyset) = \frac{\rho_0}{1-\frac{\emptyset}{\emptyset_C}} \qquad \text{Eqn. 2-1}$$

where $\emptyset_C = \dfrac{p_0}{(dp_0/d\emptyset)}$

$p_0$ = initial carrier concentration

$\dfrac{dp_0}{d\emptyset}$ = initial carrier removal rate

$= 2.9 \times 10^{-3}\ p_0^{0.224}$ Eqn. 2-2[23]

[Note: As $\emptyset \rightarrow \emptyset_C$, $\rho(\emptyset)$ gets large and the material approaches intrinsic resistivity. Care must be used in applying eqn. 1 quantitatively in this range of fluences].

Using eqn. 2-1 and 2-2 one can show that 200 ohm-cm material will undergo a 10% resistivity increase at a neutron fluence of about $2.5 \times 10^{12}$ $n/cm^2$. Depending on the details of contacts, etc. structures like these could experience increases in series resistance due to neutron induced carrier removal. Failures could be caused at these low neutron fluences, making advanced NMOS as susceptible to neutron degradation as the softest bipolar technology.

#### 2.2.1.2.4 Summary

NMOS technology as it is practiced and will be practiced in the commerical world is seriously degraded by ionizing radiation and might become sensitive to neutrons. On the plus side, it does not seem to exhibit radiation induced latchup[22] as some other technologies do, and its resistance to transient radiation induced burnout is expected to be no worse than that of other technologies. In view of its commercial importance, much more data is required on its radiation degradation, and how this degradation might be ameliorated, before it should be written off for radiation hardened LSI/VLSI applications.

### 2.2.2 Transistor-Transistor Logic (T.T.L.)

Classical bipolar technology reached its highest development stage in TTL technology, which has completely dominated commercial SSI and MSI applications for the last 15 years.

#### 2.2.2.1 Commercial Viability

The 1974 market for TTL has been reported as $700,000,000 of which about 10% was LSI (largely memories). The popularity of this family resulted from the following:

- Performance adequate for most SSI and low MSI applications
- Low Cost
- Large product family (more than 300 product types)
- Multiple sources
- User familiarity

As the level of integration implemented on a given chip rises, several TTL disadvantages come to light. These include:

- Low packing density
- High power dissipation
- Complex processing

Gold doped TTL (e.g. the 7400 and 9300 families, which constitute the bulk of TTL sales) were particularly vulnerable to these shortcomings. Modern versions of TTL have reduced power dissipation, and use Schottky clamping rather than gold doping to minimize minority carrier storage. As a result, packing densities have improved and up to 400 gates can be put on a single chip. Power dissipation has been reduced to 1 to 2 mw per gate, and gate delays reduced from 10 nsec to 5 nsec. A good example of what can be achieved with state-of-the-art TTL technology are the various processor oriented bit slice products and other LSI products available today. (AMD 2901, Monolithic Memories MM 6701, etc.). The portion of the LSI/VLSI market which these represent can

be seen from Table 2-3,which shows bit slice chips representing 8% of 1977 microcomputer component sales. While not comparable to NMOS, TTL is clearly a commercially viable LSI technology.

#### 2.2.2.1.1 Description of Process

Some idea of the processing complexity of current TTL processing can be had from an examination of Fairchilds Isoplanar I process, which has been used to fabricate high performance TTL. This process has the following features[24]:

- $N^+$ buried layer diffused into P-type silicon
- P-type epitaxial layer, 1-2 $\mu$m thick
- Thermally grown oxide
- Deposited nitride
- Deposited oxide
- Pattern nitride
- Etch silicon for isolation oxide
- Field region pre-deposition (channel stop)
- Thick field oxide growth
- Pattern nitride for sink diffusion
- N diffusion
- Strip nitride
- Pattern oxide
- $P^+$ implant for extrinsic base
- Washed emitter diffusion
- First layer metal (Aℓ-Si)
- Vapox deposition
- Second layer metal
- Vapox or plasma nitride

Since the introduction of Isoplanar I, Fairchild has modified the process to include N-type epi layers (to permit Schottky clamp diodes) and walled emitters instead of washed emitters (for additional area reduction). Despite this high level of process complexity, reasonable performance and yield have been obtained with TTL. Table 2-5 gives relevant performance levels.

**TABLE 2-5**

**Characteristics of TTL Technology[25]**

| Parameter | |
|---|---|
| Layout Density (gates/mm$^2$) | 25-80 |
| Gate Delay (nsec) | 3-10 |
| Gate Power (mw) | 1-3 |
| Speed Power Product (pj) | 10 |
| Number of Masking Steps | 7 |
| Number of Diffusions or Implants | 4 |
| Ease of Interface | Excellent |

#### 2.2.2.1.2 Present LSI/VLSI Base

Table 2-3 above indicates the product base (Bit Slice Products) which TTL has at present and expects to enjoy through 1980 in the microcomputer components area. Its use is limited to higher performance applications compatible with its lower density higher power characteristics. It is also well-suited to peripheral controllers and emulators. (See Section 3.0 of this report).

#### 2.2.2.1.3 Technical Vitality

Table 2-4 indicates that TTL continues to enjoy the attention of a reasonable segment of the advanced engineering community. It can hardly be considered obsolete, although it seems fair to describe it as obsolescent.

#### 2.2.2.1.4 Technical Problem Areas

Fundamental limitations in speed and packing density limit further development of this technology. Newer bipolar processes (such as ECL and $I^2L$) threaten to displace it, even if MOS processes do not. One must remember, however, that this technology has proven itself to be amazingly resilient, and should not be counted out yet. Substantial opportunities for improvement exist in defect control and geometry reduction, while methods for fabricating small area high value resistors would improve power dissipation. In the area of defect control, progress is being made in controlling damage introduced during processing through the use of wafer edge rounding. Damage gettering to reduce problems with precipitates has also helped reduce the biggest cause of poor yield, viz., C-E shorts. (These same techniques will become important in MOS technology as dimensions shrink). In the area of geometry reduction, improved resolution will permit emitter area reduction by ½ to 1 order of magnitude, with resultant improvement in performance and yield. Resistor technology is critical because these components represent a significant fraction of the chip area and power dissipation in a typical TTL

circuit. Active devices can be reduced in size with improved resolution. Resistors, on the other hand, require increased sheet resistance, which is often difficult to achieve without unacceptably high TCR (temperature coefficient of resistance) process sensitivity factors. Each of these three opportunity areas will require continued advancements for TTL to keep up with the NMOS technologies.

#### 2.2.2.2 Hardenability of TTL

TTL has been the subject of intensive study by the radiation effects community because of its use in systems such as Minuteman, Trident C-4, MX, and others. Myers[22] has summarized the hardness levels achievable with the commercial version of this technology, as shown in Table 2-6. The following sections discuss methods used (such as dielectric isolation) to improve the transient upset level and the survival level of TTL.

##### 2.2.2.2.1 Transient Hardness of Commercial TTL

Transient ionizing radiation generates photocurrents in silicon integrated circuits which can, at lower levels, cause logic upset, and at higher levels cause catastrophic permanent damage. The former problem is usually addressed by circumvention, i.e., an ionizing dose rate threshold $\dot{\gamma}_T$ is established below which no logic upsets will occur. If the ionizing dose rate exceeds $\dot{\gamma}_T$, temporary system shutdown is permitted until the transient event passes, at which time critical variables are recalled from a hardened store and computer operation resumes. If $\dot{\gamma}_T$ is too low, as a result of technology shortcomings, scenarists point out that system performance is degraded from excessive shutdowns. Once a reasonable level is obtained for $\dot{\gamma}_T$, however, further technology development is of limited value until a transient upset level is reached such that no system shutdown is required during the entire mission. Commercial TTL has a transient radiation logic upset level falling in the first category – $\dot{\gamma}_T$ must be increased. This has been done by eliminating the isolation junction[26,27], and compensating photocurrents flowing into critical nodes by judicious addition of P-N junctions not otherwise required for circuit operation[28,29]. The result has been the development of the logic parts described in Table 3-2, viz., a family of dielectrically isolated, photocurrent compensated SSI/MSI parts which require circumvention at high dose rate, but for which logic upset occurs at a reasonably high level.

TABLE 2-6

Radiation Hardness Levels of Commercial
TTL and Low-Power Schottky TTL

| Parameter | TTL | LSTTL |
|---|---|---|
| Neutrons ($n/cm^2$) | $10^{14}$ | $10^{14}$ |
| Total Dose (rads(Si)) | $10^6$ | $10^6$ |
| Transient Upset Level (rads(Si)/sec) | $10^7$ | $5 \times 10^7$ |
| Transient Survival Level (rads(Si)/sec) | $>10^{10}$ | $>10^{10}$ |

The second problem encountered by commercial TTL in a transient radiation environment is that of burnout. A transient radiation event can trigger a junction isolated TTL chip into a very high power dissipation mode of either permanent or temporary duration, which can result in permanent damage to chip metallization or to device junctions. The permanent condition, called latchup, requires a feedback mechanism which is usually the result of on-chip parasitic interactions[30].

Such interactions can be minimized or eliminated by either of two methods, viz., the use of dielectric isolation (D.I.) instead of junction isolation (J.I.) between adjacent devices on a chip[26,27], or the use of stringent chip design and layout rules[31]. The former approach has been preferred for the last 15 years, and is the baseline approach for all present day ICBM computer logic (Cf. Table 3-1). This technology is discussed further in section 2.2.2.2.2 below. When D.I. cannot be used, however, and J.I. must be coped with, a combination of chip design techniques and system latchup management techniques have been shown to prevent burnout due to transient radiation. The chip design techniques include latchup suppression[30] and burnout prevention, techniques for which are being developed under the Trident C-4 and the MX Program[32,33,34]. The system latchup management techniques include turning the power off to interrupt latchup, so that burnout can be prevented, and normal chip operation can be restored. This can be done in a periodic fashion (power strobing) as part of a power management regimen, or on an "as needed" basis when triggered by a radiation detector.

#### 2.2.2.2.2 Dielectrically Isolated TTL

All three (Harris, RCA, and T.I.) of the semiconductor manufacturers presently building radiation hardened TTL use single poly DI processes[26] in which anisotrophic etching of <100> material is used to produce oxide isolated wafers in which the single crystal buckets can be packed relatively tightly. Photocurrent compensated, Schottky clamped TTL circuits with a speed power product of 250 picojoules represent the

state of the art (5.5 volt supply). Diffused resistors are used in all cases (except as noted in Table 3-2) permitting better packing density than would be allowed with metal film resistors. Chip layout efficiency can be illustrated by comparing the size of the D.I. version of the ALU being designed for the MX program (111 mils x 104 mils) to the size of the J.I. version of the same circuit (75 mils x 85 mils). The D.I. chip is seen to be 80% larger in area.

Dielectric isolation has been the preferred technique for radiation hardening bipolar SSI/MSI. Serious questions have arisen, however, about this technology. This concern arises because of the low yield which can be expected from the very complicated D.I. process when used to fabricate large area chips. To illustrate the problem, consider the photomasking yield which would be predicted for a J.I. chip and a D.I. chip designed to perform a given logic function. Because of the less efficient packing density associated with D.I. chips, the area of the radiation hardened device would be larger than the commercial version. For comparison purposes we shall assume the area ratio given for the ALU chip, viz., 1.8:1. Further, D.I. material produces a higher mask defect density than J.I. because of wafer curvature and particles resulting from the D.I. process. Quantitative estimates of this difference are lacking, but a 1.5:1 estimate will be made. Finally, the D.I. process currently in use for TTL is more complicated, requiring 11 photolithographic operations vs. 7 for commercial TTL. Using these quantities and the relationship[35] between the number of good devices per wafer (D/W), chip area (A), wafer radius (r), defect density (D), and number of masking operations (n)

$$Y_{D/W} = \frac{\pi\ (r - A^{1/2})^2}{A\ (1 + AD)^n} \quad ; \quad \text{Eqn. 2-3}^{(34)}$$

one can compare yields for J.I. and D.I. versions of the same logic function. Such a comparison was made for an assumed defect density of 12 defects per $in^2$ for J.I. (2 defect/$cm^2$)(therefore, 18 defects per $in^2$ for D.I.) and two inch wafers (D.I. process is assumed to permite 80% of this area to be used). It can be shown that, subject to these assumptions, J.I. chips cease to be cost effective (i.e. $< 1$ good device per wafer) at a chip size of about 225 mils x 225 mils. D.I. chips, however, cease to be cost effective if they try to implement logic

functions more complex than those which can be put in a J.I. chip 106 mils x 106 mils. Therefore, any logic function more complex than the ALU cited above (63 gates) can probably not be built in D.I. To improve this situation, it is necessary either to reduce the complexity of the D.I. process substantially, to reduce the defect density associated with D.I. material substantially, or to improve the gate density of circuits in D.I. material by a significant amount relative to that of J.I. material. Therefore, it appears that dielectric isolation has reached its limit as a means of radiation hardening bipolar I.C.'s. When higher levels of integration are required with bipolar I.C.'s, junction isolated structures will have to be employed, and system approaches to latchup management (such as power strobing) developed to prevent burnout from high ionization dose rates.

### 2.2.3 Complementary MOS Processes

#### 2.2.3.1 Commercial Viability

In the development of MOS circuits there has been a progression in the circuit configurations of simple one transistor gates as a function of the element chosen as the load for the transistor. The simplest option calls for use of a resistor load. This gives poor performance, however. A much more popular choice has been that of an enhancement mode n-channel transistor similar to that used for the active element in the gate. N-channel depletion mode load devices have recently come into wide usage, and they permit the highest packing densities. There is, however, a fourth type of load possible for an n-channel FET, viz., a p-channel FET. A gate utilizing such a combination is called, for obvious reasons, complementary MOS (CMOS), and offers several potential advantages over uni-channel MOS circuits. These are:

- Low power dissipation
- Single supply voltage
- Wide operating range of supply voltage and ambient temperature
- High noise immunity

(The speed advantage sometimes claimed for CMOS over n-channel MOS is offset somewhat by the greater process complexity of the former technology).

The price paid for these advantages is lower packing density, with a given set of design ground rules (minimum dimensional tolerance). In view of the overriding importance of packing density, CMOS technologists will have a difficult job making this approach to VLSI competitive with NMOS in commercial applications.

CMOS is built in two forms, bulk CMOS and CMOS on sapphire (CMOS/SOS). Differences of opinion exist among CMOS practitioners as to the

relative merits of the two approaches. Bulk CMOS advocates point to basic process commonality with the mainstream commercially oriented LSI/VLSI community, greater off-chip drive capability, and the use of reasonably priced substrates, while SOS advocates claim reduced parasitics, higher packing density and higher speed.

#### 2.2.3.1.1 Description of Process

Table 2-7 compares CMOS and NMOS technologies as they exist today and as they expect to be in 1980. The following conclusions can be drawn from this data:

- NMOS is the leading candidate for commercial LSI/VLSI applications when compared with CMOS technologies for equal critical dimensions.

- CMOS/SOS practitioners think they can catch NMOS in density by 1980, but do not project catching it in speed. They will apparently rely on other advantages of CMOS/SOS to sell it.

- Bulk CMOS can today compete with NMOS if critical dimensions are pushed to the limit. Whether it can continue to do so when NMOS scales down remains to be seen.

#### 2.2.3.1.2 Present LSI/VLSI Base

Bulk CMOS has evolved through SSI and MSI, and is currently manufactured by several companies. It has been used in the fabrication of three microprocessors (the RCA COSMAC family, including the 1802 microprocessor chip, the Intersil IM6100, and a CMOS version of the 6800 chip[36]), and various memory chips. It has been estimated[37] that the 1977 sales of the 1802 were 147,000 units, with the IM6100 even less.

## TABLE 2-7

### Comparison of CMOS and NMOS Technologies

| Parameter | NMOS 1977-78 | NMOS 1980 | BULK CMOS 1977-78 Vendor A/ Vendor B | BULK CMOS 1980 | BULK CMOS 1980 | CMOS/SOS 1977-78 | CMOS/SOS 1980 |
|---|---|---|---|---|---|---|---|
| Density (gates/mm$^2$) | 170 | 200 | 170 | 75 | N.A. | 150 | 200 |
| Gate Delay (ns) | 1 | .5 | 2-5 | 5 | N.A. | 2 | 1 |
| Power (mw/gate) | 1 | .4 | .05-.8 | .5* | N.A. | .1* | .05* |
| Speed-power prod. (pj) | 1 | .2 | .1-4 | 2.5 | N.A. | .2 | .05 |
| Mask levels | 6 | 6 | 7 | 7 | N.A. | 7 | 8 |
| Critical dimensions ($\mu$m) | 4 | 2 | 2.5 | 7 | N.A. | 5 | 3.5 |

*1MHZ, 5V

N.A. = Data not available

CMOS/SOS is strictly an LSI technology, and significant production is currently confined to two manufacturers of integrated circuits, RCA Corporation (who markets chips commercially) and Hewlett-Packard Company (who builds a wide variety of custom SOS memories, microprocessors, and peripheral circuits for its own in-house needs). Several other companies, notably Hughes, Rockwell, and Westinghouse, are doing contract and internal R&D in this area.

#### 2.2.3.1.3 Technical Vitality

The technical vitality of CMOS, as seen by the commercial world, can be seen from Table 2-4 above. Workers in the field, however, seem convinced that the low power dissipation possible with this technology will eventually prove to be an overriding consideration in comparisons with other technologies.

#### 2.2.3.1.4 Technical Problem Areas

Several problem areas have been identified which will affect the success enjoyed by CMOS/SOS in the commercial world. First of these is the well known problem of substrate cost. Sapphire wafers would have to experience a substantial price reduction to permit CMOS/SOS circuits to compete with NMOS in price sensitive applications. Proponents of this technology look to Edge Film Growth (EFG) techniques to permit growth of ribbons of sapphire which can be sliced and used directly without polishing. One problem encountered with EFG sapphire is its square shape. Wafer fabrication techniques developed to date (such as spun-on photoresist) assume round wafers . RCA is in the process of transferring sapphire ribbon growth from their Princeton Laboratories to a pilot line in their Mountain Top, PA plant. Sample quantities of this material are being evaluated in the West Palm Beach, FL CMOS/SOS production facility. The question of the utility of EFG sapphire and its cost effectiveness should be resolved in 1978.

The second problem is that of speed. Table 2-7 shows that CMOS/SOS will not keep pace with HMOS in scaling down to smaller dimensions, and consequently will not be able to match N-channel technology in high speed applications. This may indicate that CMOS/SOS has a fundamental problem in achieving short channel dimensions. If so, the prospects for commercial success for this technology are dimmed, since parity in packing density with HMOS (and superiority in power dissipation) will not offset the advantages HMOS has in speed and cost.

Another problem which has faced those trying to bring CMOS/SOS to large scale commercial utilization was the difficulty experienced in enlisting second sources. Despite a recent willingness on the part of manufacturers to enter into technology and product exchanges, RCA (the only company with a standard product line[38] of CMOS/SOS devices) had been unable to induce a major semiconductor manufacturer to agree to second source. This was taken to indicate a general skepticism on the part of industry leaders about commercial prospects in this area. However, on March 29, 1978, RCA announced signing of an agreement to supply Intel with manufacturing information on CMOS/SOS in exchange for assistance in designing a CMOS/SOS version of Intel's 8085 and 8048 microprocessors. This development may impact considerably the commercial viability of CMOS/SOS technology.

#### 2.2.3.2 Hardenability of CMOS

Radiation effects in complementary MOS integrated circuits have been studied extensively, and the phenomenology is well known[39]. The circuit degradation resulting from radiation is addressed two ways: first, by process modifications which are designed to reduce device parameter degradation, and second by circuit design techniques which maximize the ability of the circuit to tolerate device parameter degradation. Both of these approaches have a price tag associated with them (else the commercial world would pick them up and use them). The price is usually one of performance degradation and/or

reduction in allowable level of integration, rather than one of dollar cost of starting materials. The question to be answered by the radiation effects community in the immediate future is whether usable LSI/VLSI can be built with CMOS technology when radiation hardening ground rules are imposed. (Since high levels of performance and high levels of integration are obviously desired, this discussion will assume that self-aligned silicon gate technology[40,41] will be used. Silicon gate CMOS/SOS circuits are generally preferred over their metal gate counterparts because the Si-gate versions provide higher density, higher speed, and simpler fabrication procedures).

#### 2.2.3.2.1 Bulk CMOS Hardness

Several manufacturers have reported hardened metal gate bulk CMOS[42,43,44] product lines, but much less work has been done on hardened silicon gate bulk CMOS. Sandia Labs has been the technical leader in this area. Sandia has chosen to pursue bulk technology rather than SOS because they feel that radiation hardened LSI must draw on commercial technology to be viable. In their opinion, bulk CMOS will continue to have commercial applications for some time, while CMOS/SOS will not attract industry backing.

They feel that without such industry support, SOS technology will "dry up within a year" if government funding is cut back[45].

Concerning the ability to harden bulk CMOS, Sandia feels it is superior to CMOS/SOS in total dose hardness of gate oxides, and of course does not have the back channel leakage problem which CMOS/SOS has. Transient hardness, however, is not good because of the possibility of latchup.

A major disadvantage of bulk CMOS integrated circuits is that they can exhibit SCR behavior when exposed either to modest levels of ionizing irradiation ($\dot{\gamma} \simeq 10^8$ rads(Si)/sec) or to an overvoltage (which is typically less than the substrate to p-well avalanche voltage). This latch-up behavior occurs because the gain product, $\beta pnp \cdot \beta npn$ of the parasitic lateral p-n-p and vertical n-p-n transistor is typically greater than unity, and with sufficient photocurrent generation, or over-voltage, the bulk IR drops cause forward-biased junctions. Since the SCR holding currents are typically below the power supply capability, the circuits will sustain the latch-up until the power supply is turned off.

Several possible techniques can be used to prevent CMOS latch-up, including circuit layout and control of material parameters such as bulk minority carrier lifetime. Sandia Labs has shown that the application of gold-doping to CMOS integrated circuits to control substrate minority carrier lifetime can maintain the parasitic $\beta_{pnp} \cdot \beta_{npn}$ below unity and thus prevent latch-up[46]. The low concentration of gold required to prevent latch-up can hopefully be controlled by typical oxide annealing temperatures.

Transient radiation induced logic upset levels are not appreciably improved by gold doping. The upset level remains at about $\dot{\gamma}_U \simeq 6 \times 10^8$ rads(Si)/sec.

Sandia's current bulk CMOS process is a seven mask sequence using three (3) implantations (P well, $N^+$, and $P^+$) and a diffused $N^+$ gate (850°C). Their gate oxide is 550 Å (1000°C, dry $0_2$), and their sources and drains are very shallow (0.7 $\mu$m) with deep P-wells (8.8 $\mu$m). To avoid spiking through sources and drains when making contact, they evaporate silicon doped aluminum onto a hot (150°C) wafer. This metal requires care in etching, but provides good step coverage and very shallow ohmic contacts.

An earlier version of this process used diffused $N^+$ sources and drains instead of implanted. Closed CMOS Logic ($C^2L$) 1802 microprocessor chips were built with this process (1370 gates on a chip 181 mils x 237 mils give a density of ~50 gates/mm$^2$). Samples have been tested for total dose response and transient hardness. Chips were operated at 250KHz in a $Co^{60}$ cell. At intervals, some would be removed and tested at 2MHz, using a 50 pf. load. Table 2-8 gives the total dose for failure at these two frequencies at 5V and at 10V.

TABLE 2-8

Total Dose Hardness of Sandia $C^2L$ 1802[45]

| | 250KHz | 2MHz |
|---|---|---|
| 5V | $5 \times 10^5$ rads(Si) | $4 \times 10^5$ rads(Si) |
| 10V | $1.3 \times 10^6$ rads(Si) | $1 \times 10^6$ rads(Si) |

Transient testing was conducted in a Febetron, and showed no latchup to 5 x $10^9$ rads(Si)/sec. Upset occurred at 5 x $10^8$ rads(Si)/sec. If the chips were pre-irradiated with neutrons to further reduce lifetime, the upset level was increased to 1 x $10^9$ rads(Si)/sec at 10V. (This data point must be regarded as a "best case" number since the radiation pulse was not synchronized with the clock pulse to determine worst case upset levels).

Sandia plans to continue the study of the effects of gold doping on these chips, and evaluate transient annealing and reliability. They will also evaluate a high density version of bulk CMOS, called Expanded Linear Array Technology (ELA), as a possible approach to LSI/VLSI. ELA is felt to offer a two-fold improvement in packing density over $C^2L$ (100 gates/$mm^2$).

Harris Semiconductor has been involved in silicon gate bulk CMOS development, both on internal funding and under government contract. They are presently under contract with Sandia Labs to determine the feasibility of latchup suppression in their process by gold doping. Results are expected during the second quarter of 1978 which will tell whether bulk CMOS can be made hard to transient ionizing radiation by gold doping.

RCA has also been active in the study of radiation hardened silicon gate bulk CMOS. The CDP 1802 microprocessor and the CDP 1832 ROM have been hardened with Navy and Sandia Labs support. Test data on the microprocessor [47] indicates that a hardness level of 5 x $10^5$ rads(Si) has been achieved.

In summary, bulk CMOS offers good performance potential (at least vendor A of Table 2-7 thinks so), and good total dose hardness. Research currently underway will determine whether its transient radiation hardness can be improved to the extent needed to qualify it as a candidate technoloy for a radiation hardened LSI/VLSI applications. If this research is successful, microprocessor chip set development with this technology should be considered.

#### 2.2.3.2.2 CMOS/SOS Radiation Hardness

CMOS/SOS technology is generically neutron-hard, and has been shown by several experimeters to be hardened to radiation induced logic upset[48]. Total dose hardness is the remaining hurdle for CMOS/SOS.

A large amount of government sponsored research has been conducted over the past 10 years in developing radiation hardened CMOS/SOS technology, yet today there are no commercially available CMOS/SOS microprocessors capable of exceeding the performance and/or total dose hardness level of the special F-8 PSU (3851) described by Myers[20]. These devices are, of course, NMOS, and have long been felt to represent the "ridiculous extreme" of semiconductor technology as far as radiation sensitivity is concerned. Yet by making a few relatively minor changes in the process, Myers was able to achieve total dose failure levels of $10^4$ rads(Si). King and Martin[47] report that an "early developmental CMOS/SOS version" of the 1802 microprocessor was found to fail at $1.2 \times 10^4$ rads(Si). Considering the millions of dollars of government funding which has been expended to develop radiation hard CMOS/SOS LSI, the 1802 hardness is not outstanding.

Advocates of CMOS/SOS point to impressive results obtained in custom designs for use in radiation environments[49,50,51] to prove that this technology is in fact a radiation hard LSI technology. Actual product experience, however, with high performance silicon gate CMOS/SOS which is reliable and producible is quite limited. The best results which have been reported for LSI produced for a system-related program are those reported by Palkuti[52,53] for the P-Code Generator Chip developed by Naval Research Labs and manufactured by RCA for the GPS system. This chip has 2660 devices is an area of 190 x 202 mils, for a gate density of 28 gates/mm$^2$. It has a clock frequency of 10MHz at 10V (gate delay of 3.5 to 5 nsec/gate) and a dynamic power of approximately 20 mw/MHz. Radiation testing of this chip showed less than 20% speed degradation after a dose of $1 \times 10^6$ rads(Si). Transient testing showed

a logic upset level of 1 x $10^{11}$ rads(Si)/sec for short pulses, and 6 to 8 x $10^{10}$ rads(Si)/sec for long pulses. RCA hopes to accumulate process stability data to support this device in the near future. This chip clearly represents a milestone in the development of radiation hardened LSI/VLSI. More work in necessary, however, to prove that CMOS/SOS will meet performance, reliability and radiation requirements at the same time.

The microprocessor chip set being developed by RCA under a Manufacturing Technology Program with the Air Force Materials Lab is more representative of the present state of the art in radiation hardened CMOS/SOS LSI. This chip set, five of which are described in Table 2-9, will be designed to operate through 5 x $10^4$ rads(Si) total dose. The effort is scheduled for completion in 1980. It is estimated that a major effort would be required to redesign these parts so that greater radiation hardness could be achieved (3 x $10^5$ rads(Si) would probably be the next goal in radiation hardness). By the time this level of performance is reached (early to mid 80's), commercial LSI/VLSI will have reached 32 bit microcomputers on a chip, 256K dynamic RAMS, etc. (Cf. Fig.2-3). Without in anyway denigrating the above chip set, it is plain that radiation hardened CMOS/SOS technology is not keeping pace with commercial LSI/VLSI.

### 2.2.4 Integrated Injection Logic

#### 2.2.4.1 Commercial Viability

Bipolar integrated circuits have traditionally represented a larger market than the MOS market. This has been due almost exclusively to the tremendous quantity of SSI and MSI devices which have been built in TTL technology. Approximately five years ago, this began to change, and in that time the number of MOS gates sold per year has risen to about 10 times that of bipolar. Recently, however, bipolar memories and other LSI products have appeared. Established technologies like TTL and ECL have developed renewed vitality, while newer technologies like $I^2L$ have attracted a substantial following. Table 2-10 compares performance levels available in 1978 in static RAM's made by various technologies. Clearly, $I^2L$ is in the fight for applications such as cache,

## RCA CMOS/SOS MANUFACTURING TECHNOLOGY IC'S

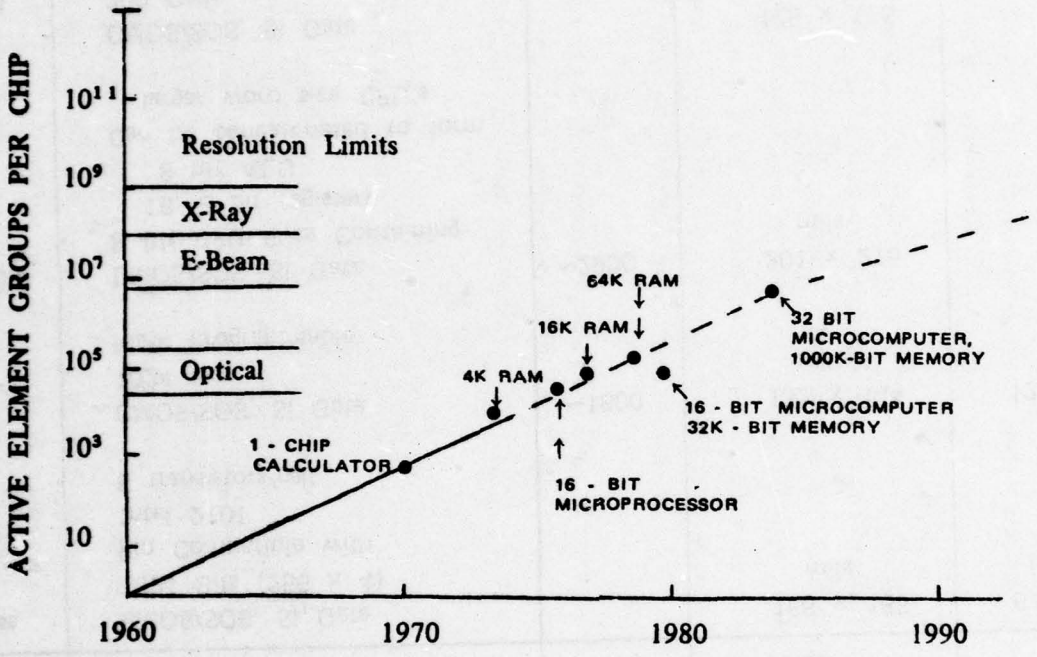
| Part Type | Description | FETS | Size | Power[1] | Speed[1] |
|---|---|---|---|---|---|
| Random Access Memory (TCS072) | CMOS/SOS, Si Gate<br>1024 Bits (256 x 4)<br>Pin Compatible with Intel 2101<br>5 transistors/cell | | 156 x 185 mils | 6.5mW/MHz (5pf load) | Access: 110ns (85pf load) |
| Read Only Memory (TCS075) | CMOS/SOS, Si Gate<br>1024 Bits<br>Mask Programmable | ~1600 | 132 x 144 mils | 12mW/MHz (60pf load) | Access: <150ns (60pf load) |
| General Processor Unit (TCS074) | CMOS/SOS, Si Gate<br>8 Bit CPU Slice Containing<br>16, 8 bit registers<br>8 bit ALU<br>Can be concatenated to form larger word size CPU's | ~2900 | 201 x 215 mils | | Register-Register On Chip Operations: <80ns<br>Register to Data Off Chip Operations <200ns |
| Gate Universal Array (TCS091) | CMOS/SOS, Si Gate<br>300 Cells<br>256 Internal<br>44 I/O & Driver<br>Circuit Function Defined By metal mask | | 175 x 175 mils | | 3.0ns Pair Delays |
| Multiplier (TCS077) | CMOS/SOS, Si Gate<br>8 Bit Expandable 2's Complement | ~2200 | 181 x 175 mils | 72mW/MHz | 8 x 8 Multiply: <280ns (18pf load) |

**Notes:** 1. Typical, 25°C, 10V, Prerad

**Table 2-9**

FIGURE 2-3

SEMICONDUCTOR CHIP COMPLEXITY[54]



## TABLE 2-10

### Static RAM Memory Designs[55]

| | HMOS | VMOS | Schottky $I^2L$ | $I^3L$ | TTL (FAIRCHILD) | TTL[56] (NIPPON) |
|---|---|---|---|---|---|---|
| DENSITY | 1K–4K | 1K–8K | 1K–16K | 4K–16K | 1K–4K | 4K |
| ACCESS TIME | 50-70 NS | 50-70 NS | 70-100 NS | 100-125 NS | 30-70 NS | 35 NS |
| CYCLE TIME | 50-70 NS | 50-70 NS | 70-100 NS | 240-280 NS | 30-70 NS | ---- |
| PWR. DISS. | | | | | | |
| ACTIVE | 500 MW | 500 MW | 450 MW | 500 MW | 750 MW | 500 MW |
| STANDBY | 50 MW | 50 MW | 25 MW | ---- | ---- | ---- |
| PACKAGE | 18 PINS | 18 PINS | 18 PINS | 16 (MULTIPLEX) | 18 PINS | ---- |

buffer, and scratch pad memories in main frame applications or in controllers, minicomputers, CRT terminals, peripherals, or add–on memories.

In the processor chip area, two recent developments are of significance. First, Fairchild has announced[57] that they regard $I^2L$ as their preferred technology for LSI/VLSI applications. Furthermore, they have announced their 9440 16-bit $I^2L$ microprocessor chip[58]. These two facts indicate strong commercial support for this technology at a major semiconductor house - a very welcome development.

The second development of importance to $I^2L$ apologists is the announcement[59] that Texas Instruments will introduce peripherals for the integrated-injection-logic version of its 16-bit 9900 processor. In the next few months, the 9900 will gain an $I^2L$ 16,384-bit read-only memory, priority-interrupt controller and interval timer, plus a serial input/output expander. But even more important are several programmable peripherals, including another I/O expander and an interface adapter, that are software-alterable.

Thus, while $I^2L$ has no large commercial LSI/VLSI base at present, it now appears that such a base may develop in 1978, fulfilling a major requirement for a radiation hardened LSI/VLSI technology.

#### 2.2.4.1.1 Description of Process

$I^2L$ has changed the picture of the long standing struggle between bipolar technology and MOS technology by permitting packing densities equal to or higher than MOS technologies (250 gates/mm$^2$), power dissipation comparable to that of CMOS, and at the same time, retaining high speed (propagation delays better than 5ns per gate have been reported).[60] First generaton $I^2L$ has already proven competitive with CMOS. Second generation processes have received significant emphasis at a number of I.C. houses. This rapid progress has come about by eliminating all resistors and merging the p-n-p and n-p-n devices in a gate into one device to increase packing density; by using a 1-V supply rather than a 5-V supply to reduce power dissipation; and by minimizing stray capacitance, eliminating storage time problems, and using very low voltage swings at the signal nodes to increase speed. Technology

development work is continuing, especially in areas such as interfacing and development of a good second layer interconnection method.

Detailed descriptions of the second generation processes developed at the two main domestic commercial advocates of $I^2L$ have been published[60,61] Both processes employ ion implanted intrinsic base regions, and heavily doped extrinsic base regions. In addition, Hennig, et al,[54] describes features which third generation processes may use, viz., oxide side-wall isolation, narrow base p-n-p lateral transistors, and diode saturation clamping of the n-p-n transistor. Table 2-11 compares isoplanar $I^2L$ to NMOS technologies based on Hennig's paper. Also notable in this paper is the use of P-type starting material. This removes the self-isolated characteristic of earlier $I^2L$ processes which was so attractive to radiation effects analysts. This modification is necessary for commercial applications, however, where buffer and/or linear devices are desired on the same chip. It appears that commercial devices will use junction isolation so system approaches to latchup management may be necessary if commercial $I^2L$ products are to be used.

#### 2.2.4.1.2 Present LSI/VLSI Base (Discussed Above)

#### 2.2.4.1.3 Technical Vitality

Table 2-4 does not properly indicate the technical vitality of the $I^2L$ field. The April 1977 issue of IEEE Journal of Solid State Circuits is a Special Issue on $I^2L$ and gives a better idea of the breadth of the interest in this new technology, especially on the parts of commercial semiconductor houses. Among major semiconductor manufacturers, Texas Instruments and Fairchild have significant process and product development programs in $I^2L$.

#### 2.2.4.1.4 Technical Problem Areas

The main performance problem area facing $I^2L$ is that of achieving higher speed. The excellent speed-power products achieved to date are usually

TABLE 2-11

Comparison of $I^2L$ & NMOS Production Technologies

| Parameter | HMOS 1977-78 | HMOS 1980+ | $I^2L$ [57, 61] (1980) |
|---|---|---|---|
| Layout Density (gates/mm$^2$) | 170 | 200 | 300 |
| Gate Delay(ns) | 1 | 0.4 | 3 |
| Gate Power(mw) | 1 | 0.5 | .7 |
| Speed Power Product | 1 | 0.2 | |
| Number of Thin Films | 2 | 2 | 2 |
| Number of Implants | 3 | 3 | 3 |

obtained by demonstrating modest speeds at very low power levels. NMOS is just plain faster. Improvements are needed in this area. Peltzer [24] indicates that expected improvements in lithography over the next 5-10 years will help $I^2L$ more in this regard than they will help NMOS. Thus he expects $I^2L$ performance to approach that of NMOS in speed, while surpassing it in density, power dissipation, off-chip drive capability, etc.

Interconnects are a problem of particular importance to $I^2L$, since it is a current logic, and parasitic resistances are particularly troublesome. Refractory metal interconnects would be particularly helpful here. Also of interest is the growth and control of very thin (1-2 $\mu$m) layers of epitaxial silicon. It may even be necessary to develop the capability of depositing two different N-epi layers on the same chip, one for $I^2L$ logic, and a thicker layer for high voltage buffer capability.

Finally, defect control techniques such as the ones mentioned in section 2.2.1.4 will also contribute to the commercial success of $I^2L$.

### 2.2.4.2 Hardenability of $I^2L$

Numerous studies have been conducted on the effects of radiation on $I^2L$ gates and test devices[62-66], but Air Force experience with CMOS/SOS technology programs has shown that the feasibility of hardening gates does not guarantee the feasibility of hardening LSI. Therefore, data on radiation effects on $I^2L$ LSI should be given greater weight.

The most extensive testing of $I^2L$ LSI done to date is that conducted on Texas Instruments' SBP 9900 microprocessor chips by Naval Weapon Support Center personnel during May - June 1977 [67]. Total dose, dose rate, and neutron fluence tests were conducted, with the following results.

- **Total Dose Tests**

Three samples were irradiated in the JPL dynamitron to total dose levels of $1 \times 10^5$, $3 \times 10^5$, $1 \times 10^6$, and $3 \times 10^6$ rads(Si). Two units were exposed

with inputs low and one with inputs high. Total injector current was set at 10 ma. After radiation, two units were tested at 520 ma, 2.0 MHz using a modified T.I. 990 evaluation module[68]. (One of these two units had been irradiated with inputs low, the other high). Both units operated after $10^6$ rads(Si) and failed after 3 x $10^6$ rads(Si). One of these (inputs high) recovered 35 minutes after receiving 3 x $10^6$ rads(Si) and operated successfully.

The third unit was tested for $f_{max}$ at 90 ma and 520 ma. Table 2-12 presents measured values of $f_{max}$ after each total dose level.

- Dose Rate Tests

Two units were tested for logic upset levels in the White Sands LINAC. The machine was used in the electron mode at 20 Mev with pulse widths of 40 nsec, 100 nsec, and 1 $\mu$sec.

The test circuit was developed by TI and is used for final inspection test on commercial parts. The program is a self test utilizing 90% of the micro-instruction set. The software is stored in ROM. The test requires approximately 180,000,000 clock pulses for completion. When failure occurs the tester stops and 4 place hexadecimal readout gives the software location of the failure. Test devices were continually exercised and the dose rate adjusted to give upset. The test circuit was shielded from the LINAC beam and the 4 place LED readout monitored with a TV camera. The upset levels acquired are upper bounds since the most vulnerable operations could not be determined with high confidence.

The tests showed that the ionization dose rate for logic upset, $\dot{\gamma}_U$ for 100 nsec pulses was between 2.0 and 2.5 x $10^8$ rads(Si)/sec, and was independent of the injector current between 50 ma and 500 ma (unlike substrate fed logic, where $\dot{\gamma}_U$ varies inversely with $I_{EE}$[67]). The dose rate for logic upset was also determined at $I_{EE}$ = 500 ma and f = 2.0 MHz for LINAC pulse widths of 40 nsec and 1 $\mu$sec (Cf. Table 2-13).

TABLE 2-12

$f_{MAX}$ vs. Total Dose For SBP 9900

| TOTAL DOSE | $f_{MAX}$ | |
|---|---|---|
| | I = 90 ma | I = 520 ma |
| 0 | 950 KHz | 2.6 MHz |
| $1 \times 10^5$ | 900 KHz | 2.6 MHz |
| $3 \times 10^5$ | 850 KHz | 2.55 MHz |
| $1 \times 10^6$ | 750 KHz | 2.4 MHz |
| $3 \times 10^6$ | Failed | Failed |

## TABLE 2-13

**Ionization Dose Rate For Logic Upset vs. Pulse Width For SBP 9900**

| PW | $\dot{\gamma}_U$ (rads(Si)/sec) | |
|---|---|---|
| | Unit #1 | Unit #2 |
| 40 nsec | $4.4 \times 10^8$ | $7 \times 10^8$ |
| 1 $\mu$sec | $7.5 \times 10^7$ | $1.1 \times 10^8$ |

- Neutron Tests

Two units were irradiated passively in the Sandia Pulsed Reactor III. The same circuit used for the dose rate tests was used to test these samples after neutron exposure. Devices were measured for minimum operating injector current, maximum clock frequency at $I_{EE}$(MIN), and $f_{MAX}$ at $I_{EE}$ = 100 ma, 200 ma, and 500 ma. Results are given in Table 2-14.

NWSC is presently testing the SBP9900A (oxide side-wall isolated version of the SBP 9900) and the Fairchild 9440 using similar techniques. Preliminary results[70] indicate that the radiation hardness levels of these parts is only slightly inferior to the above.

When one considers that the SBP9900 is a 300 mil x 300 mil chip, having 6000 gates (gate density of 107 gates/mm$^2$) and is by anyone's standards a "high end microprocessor", these are very impressive results indeed, and show that $I^2L$ meets all the criteria for a radiation hardened LSI/VLSI technology.

## TABLE 2-14

### $f_{max}$ vs Neutron Fluence for SBP 9900

| UNIT NO. | PARAMETER | RADIATION LEVEL ($N/CM^2$) 1 MeV eq | | | | |
|---|---|---|---|---|---|---|
| | | 0 | $3.61 \times 10^{12}$ | $1.66 \times 10^{13}$ | $5.28 \times 10^{13}$ | $8.4 \times 10^{13}$ |
| 1190 | $I_{Total}$(MIN) | 33mA | 35mA | 67mA | 170mA | |
| | AND $F_{MAX}$ | 320KHZ | 335KHZ | 545KHZ | 1.05 MHZ | |
| | $f_{MAX}$ @ 100mA | 875K | 877KHZ | 780KHZ | ------ | |
| | $f_{MAX}$ @ 200mA | 1.6MHZ | 1.5MHZ | 1.4MHZ | ------ | |
| | $f_{MAX}$ @ 300mA | ----- | ----- | ----- | 1.65 MHZ | |
| | 500mA | 2.7MHZ | 2.55MHZ | 2.7MHZ | 2.25 MHZ | |
| 1189 | $I_{Total}$(MIN) | 25mA | 28mA | 58mA | 150mA | 320mA |
| | AND $f_{MAX}$ | 245KHZ | 260KHZ | 470KHZ | 900KHZ | 1.2MHZ |
| | $f_{MAX}$ @ 100mA | 890KHZ | 845KHZ | 755KHZ | ----- | ----- |
| | $f_{MAX}$ @ 200mA | 2.1MHZ | 1.53MHZ | 1.38MHZ | ----- | ----- |
| | $f_{MAX}$ @ 300mA | ----- | ----- | ----- | 1.55MHZ | ----- |
| | $f_{MAX}$ @ 500mA | 2.82MHZ | 2.76MHZ | 2.62MHZ | 2.2MHZ | 1.82MHZ |

### 2.2.5 Conclusions and Recommendations

The foregoing assessment estimated the ability of various candidate LSI/VLSI technologies to meet future military requirements in the area of performance and nuclear radiation hardness. This section summarizes these findings, estimates what the technology picture is expected to be in the 1980's and discusses the system implications of this technology picture.

#### 2.2.5.1 Current Status of Radiation Hardened LSI/VLSI Technologies.

There is, at present no technology that has the required combination of proven high performance, reliability, and radiation hardness to meet military LSI/VLSI needs. Today's military electronic systems designers are forced to make concessions in one or more of these key areas to make gains elsewhere. The factors which are involved in this tradeoff are many and varied, but an effort can be made to quantify it. Table 2-15 attempts to summarize the present performance levels which a system designer could reasonably expect to obtain in the various technologies with minimum development time. Table 2-16 attempts to project the performance levels which will be available to the system designer in the early 1980's (under the same assumptions). Tables 2-17 and 2-18 estimate the radiation hardness levels which will accompany these performance levels, neglecting radiation induced latchup as a failure mode, and assuming that recently developed burnout prevention techniques are employed. (These assumptions are felt to be reasonable since the overhead associated with system level approaches to latchup management and burnout prevention become more acceptable as the level of integration rises).

The conclusions to be drawn from this data are as follows:

- If burnout is attacked at the system level no candidate technology can be automatically excluded.
- A substantial effort is required in radiation testing of LSI/VLSI to keep pace with the rapid process and product development in this dynamic field. Because of the wide use of NMOS in current products, and because relatively little radiation testing of this technology has been done, this testing effort should initially emphasize NMOS.

- The little data available on NMOS radiation effects indicates that it is quite "soft". It may be possible, however, to improve the hardness of this technology significantly by slight process changes. The wide usage of NMOS gives this approach to hardened technology development great leverage, and it should be pursued.

- TTL will continue to be useful in higher performance bit slice oriented processing elements and in emulators. It does not appear, however, that TTL can overcome its fundamental limitations in power and packing density to become a useful VLSI technology.

- $I^2L$ appears to have all the requirements needed to qualify as the prime radiation hardened LSI/VLSI technology. It has the beginnings of a strong commercial base (with all the performance advantages this entails) and a proven ability to meet high radiation levels with chips which are true LSI/VLSI. Here too it would be profitable to determine how much the commercial process could be hardened by slight process changes, rather than to develop an entirely new version of $I^2L$ which may not have the producibility or reliability of the commercial version.

- There is a sharp difference of opinion between commercial producers of bulk CMOS LSI as to its potential for VLSI. In view of the weight which Questron attaches to commercial viability, it would be inconsistent for this report to recommend major action in the bulk CMOS technology until the market place has adjudicated this dispute.

- The recent agreement between RCA and Intel would seem to put new life into CMOS/SOS for commercial applications. Questron recommends that the radiation hardness of the commercial version of CMOS/SOS be investigated so that the comparison between this technology and others can be done on an equitable basis.

- In general, Questron recommends that commercial viability be a prerequisite for technologies to be considered for radiation hardened LSI/VLSI applications.

Table 2-15

**Present performance levels available in different LSI/VLSI technologies.**

| CHARACTERISTIC | NMOS | TTL/JI | TTL/DI | CMOS | CMOS/SOS | $I^2L$ |
|---|---|---|---|---|---|---|
| DENSITY (gates/$mm^2$) | 170 | 25-80 | 10 | 75-170 | 150 | 100 |
| PROP DELAY (nsec) | 1 | 3-10 | 10 | 2-5 | 2 | 10 |
| POWER/GATE (mW) | 1 | 1-3 | 25 | .05-.5* | .1 | 1 |
| SPEED X POWER (pj) | 1 | 10 | 250 | .1-2.5 | .2 | 10 |
| CHIP SIZE ($mm^2$) | 25 | 24 | 6 | 25 | 25 | 25 |
| EASE OF INTERFACE | Reasonable | Excellent | Excellent | Good | Reasonable | Good |

T = 25°C, Pre-radiation

Table 2-16

Projected (1980) performance levels available in different LSI/VLSI technologies.

| CHARACTERISTIC | NMOS | TTL/JI | TTL/DI | CMOS | CMOS/SOS | $I^2L$ |
|---|---|---|---|---|---|---|
| DENSITY (gates/mm$^2$) | 200 | 50-100 | 10 | NA | 200 | 300 |
| PROP DELAY (nsec) | 0.4 | 2-5 | 10 | NA | 1 | 3 |
| POWER/GATE(mW) | 0.5 | 1 | 25 | NA | 0.05 | 0.7 |
| SPEED X POWER (pj) | 0.2 | 2-5 | 250 | NA | 0.05 | 2 |
| CHIP SIZE (mm$^2$) | 30 | 25 | 6 | NA | 30 | 30 |
| EASE OF INTERFACE | Reasonable | Excellent | Excellent | Good | Reasonable | Good |

T = 25 ℃, Pre-radiation

Table 2-17

Radiation hardness level associated with 1978 LSI/VLSI performance level.

| RADIATION | NMOS [19, 20] | TTL/JI [21] | TTL/DI [71] | CMOS [72] | CMOS/SOS [72] | $I^2L$ [67] |
|---|---|---|---|---|---|---|
| NEUTRON FLUENCE ($n/cm^2$) | $10^{15}$ | $10^{14}$ | $1\text{-}5 \times 10^{14}$ | $10^{15}$ | $10^{15}$ | $3\text{-}5 \times 10^{13}$ |
| TOTAL DOSE (rads/(Si)) | $10^3$ | $10^6$ | $10^6 - 10^7$ | $1\text{-}3 - 10^5$ | $10^3 - 10^4$ | $10^6$ |
| DOSE RATE, LOGIC UPSET, SHORT PULSE (rads(Si)/sec) | $10^5$ | $1\text{-}5 \times 10^7$ | $.5 - 1 \times 10^9$ | $1 \times 10^9$ | $1 \times 10^{11}$ | $5 \times 10^8$ |
| DOSE RATE, SURVIVAL(1) (rads(Si)/sec) | $10^{12}$ | $10^{12}$ | $10^{12}$ | $10^{12}$ | $10^{12}$ | $10^{12}$ |
| DOSE RATE, LOGIC UPSET, LONG PULSE (rads(Si)/sec) | $5 \times 10^4$ | $1 \times 10^7$ | $2 - 5 \times 10^8$ | $6 \times 10^8$ | $1 \times 10^{10}$ | $10^8$ |

(1) Neglecting latchup & assuming burnout prevention procedures are utilized.

Table 2-18

Radiation hardness levels projected for 1980 LSI/VLSI performance levels.

| RADIATION | NMOS [73] | TTL/JI | TTL/DI | CMOS [73] | CMOS/SOS [74] | $I^2L$ [73] |
|---|---|---|---|---|---|---|
| NEUTRON FLUENCE ($n/cm^2$) | $10^{14}$ | $10^{14}$ | $1-5 \times 10^{14}$ | $10^{15}$ | $10^{15}$ | $10^{14}$ |
| TOTAL DOSE (rads(Si)) | $10^3$ | $10^6$ | $10^6 - 10^7$ | $10^5 - 10^6$ | $10^5$ | $10^6$ |
| DOSE RATE, UPSET, SHORT PULSE (rads(Si)/set) | $10^5$ | $2-5 \times 10^7$ | $.5 - 1 \times 10^9$ | $10^9$ | $1 \times 10^{11}$ | $5 \times 10^8$ |
| DOSE RATE, UPSET, LONG PULSE (rads(Si)/sec) | $5 \times 10^4$ | $1 \times 10^7$ | $2\text{-}5 \times 10^8$ | $6 \times 10^8$ | $3 \times 10^{10}$ | $2 \times 10^8$ |
| DOSE RATE, SURVIVAL(1) (rads(Si)/sec) | $10^{12}$ | $10^{12}$ | $10^{12}$ | $10^{12}$ | $10^{12}$ | $10^{12}$ |

(1) Neglecting latchup and assuming burnout prevention procedures are utilized.

### 2.2.5.2 Recommendations

Questron recommends that R&D in radiation hardened LSI/VLSI should be directed toward the goal of making available to military system designers the full range of performance available to commercial systems designers. To achieve this end, military systems should not exclude arbitrarily any candidate technology because of susceptibility to failure mechanisms which can be addressed at a system level.

Evaluation of the radiation sensitivity of processes should emphasize those of known commercial potential. Only those modifications which are considered minor should be permitted in this evaluation. (Ingenuity and innovation will be required to determine exactly what modifications are "minor".)

Unique LSI/VLSI processes will be extremely expensive to develop, and should be attempted only when the most compelling reasons exist. When such reasons are judged to exist, appropriate funding must be made available to provide the technology development effort with the resources needed to accomplish the enormous task of unique process development.

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## 3.0 RADIATION HARDENED COMPUTER APPLICATIONS

Radiation hardened electronic systems can be divided into three categories according to the severity of the overall nuclear environment encountered in each situation:

- ICBM's (including reentry vehicles)
- Space Systems
- Manned Systems

Generally, the ICBM's have the most severe overall radiation environment and the on board electronics must be designed to withstand all nuclear weapon generated effects. (Certain special application reentry vehicles (RV's) may have a radiation specification even more stringent than the booster, but these RV's are not considered separately in this report). The primary radiation concern with space systems is survival against total ionizing dose accumulated from the natural space radiation. When man-made radiation environments are considered for satellites, some of the specifications can be even more severe than for ICBM's, but because of the fundamental differences in missions between satellites and ICBM's, the design philosophies can be different. Therefore, for the purposes of this report, ICBM's and space systems will be considered separately. The radiation limitation in manned systems is the ability of man to perform his mission so the electronics need not be any more tolerant to radiation than the human body.

This section discusses computer technology relative to each of the three selected classes of hardened systems. Descriptions of current computers are presented followed by some prognostication about the next generation of hardened computers.

### 3.1 ICBM Computers

Computers that fly on ICBM's must live in a severe radiation environment that covers all the effects - neutron fluence, total ionizing dose,

multiple X-ray and gamma-ray transients, EMP, etc. Because of the strategic importance, and severe radiation environment of ICBM's, they historically have driven the world of hardened system design and hardened semiconductor development. Two ICBM's are currently in development – the Navy Trident C4 which is being flight tested and the Air Force MX which is in advanced development. The baseline computer logic technology for both missile systems is bipolar small and medium scale integrated circuits (SSI/MSI). MX is also addressing an advanced metal - oxide - semiconductor (MOS) computer. (See Tables 3-1 and 3-2).

### 3.1.1. Trident C4

The computational load on C4 is distributed between two computers - guidance and autopilot.

#### 3.1.1.1 C4 Guidance Computer

The C4 guidance computer is a circumventable, list processor which uses dielectrically isolated (DI), TTL IC's for logic, junction isolated (JI) programmable read-only-memories (PROM) for program storage, and plated wire memory for hardened read/write storage. The cycle time for the plated wire is ~ 1$\mu$sec. The program memory is power strobed both to save power and to recover the IC's from possible latchup. Power is applied to the PROM's (when addressed) only for the period of time necessary to fetch the instruction. Power is then automatically removed. The 1024 bit bipolar PROM's have NiChrome thin film resistors on the chip to limit the power supply current and thereby prevent burnout during a transient radiation event. The DI logic parts are standard power (not Schottky) TTL MSI gate arrays incorporating NiChrome resistors. The development of the basic parts began in about 1973 at Harris Semiconductor. Two logic gate arrays are programmed with metalization masks to form the 6 logic parts. Harris is qualified for IC production and TI is being qualified.

## ICBM COMPUTERS

| | TRIDENT C4 GUIDANCE | TRIDENT C4 AUTOPILOT | MX FLIGHT COMPUTER (3) | MX ADVANCED COMPUTER |
|---|---|---|---|---|
| ARCHITECTURE | LIST PROCESSOR<br>FIXED POINT | GENERAL REGISTER<br>FIXED POINT | TO BE DETERMINED | GENERAL REGISTER<br>FLOATING POINT |
| DATA WORD SIZE | 24 BITS | 16 BITS | TO BE DETERMINED | 32 BITS |
| LOGIC PARTS: COMPLEXITY | 50 GATES MAX | 70 GATES MAX | 70 GATES MAX (2) | ~500 GATES (4) |
| PART TYPES | 6 (2 MSI ARRAYS) | 9 | 10 | TO BE DETERMINED |
| TECHNOLOGY | DI, TTL | DI, LSTTL | DI, LSTTL | CMOS/SOS; Al GATE |
| SPEED | 5-15 ns/GATE | ~8 ns/GATE (1) | ~8 ns/GATE (1) | 10 ns/GATE |
| POWER | ~10 mW/GATE | ~6 mW/GATE (1) | ~6 mW/GATE (1) | 5 μW/GATE (5) |
| VENDORS | HARRIS, T.I. | RCA | T.I., RCA, HARRIS | (6) |
| PROGRAM MEMORY: SIZE | ~6000 WORDS | 4096 WORDS | < 524,288 TOTAL BITS | TO BE DETERMINED |
| TYPE | JI, TTL, 1K BIT PROM | JI, LSTTL, 2K BIT ROM | | MNOS/SOS |
| READ/WRITE MEMORY: SIZE | 2048 WORDS | 256 WORDS | | TO BE DETERMINED |
| TYPE | PLATED WIRE | JI, LSTTL, 256 BIT RAM | | MNOS/SOS |
| STATUS | FLIGHT TESTED<br>PARTS QUALIFIED | FLIGHT TESTED-COMMERCIAL PARTS<br>PARTS QUALIFIED | IN SOURCE SELECTION<br>PARTS IN DEVELOPMENT | COMPUTER ARCHITECTURE COMPLETE<br>(6) |

NOTES:
1.) BASED ON ALU SPECIFICATION.
2.) BASED ON MX ADVANCED DEVELOPMENT MICROCIRCUITS ON THE PREFERRED PARTS LIST.
3.) SPECIFICATIONS TO BE DEFINED DURING MX SYSTEM DEFINITION.
4.) ROCKWELL ACT I ALU.
5.) 1 MHz, 11V
6.) ROCKWELL IS DEVELOPING A CMOS/SOS ALU, A CMOS/SOS HARDENED REGISTER FILE, AND AN MNOS/SOS PERMANENT STORE MEMORY. WESTINGHOUSE IS DEVELOPING AN MNOS/SOS TEMPORARY STORE MEMORY AND AN MNOS/SOS PERMANENT STORE MEMORY.

TABLE 3-1

# ICBM IC FAMILIES

## TRIDENT C4 GUIDANCE COMPUTER

DIGITAL IC'S (MSIA)

1. 4 TO 1 DECODER
2. 2 BIT ADDER
3. 4 TO 1 MULTIPLEXER
4. 4 BIT SYNCH COUNTER
5. MEMORY DRIVER
6. 4 BIT SHIFT REGISTER
7. 1024 BIT PROM

LINEAR IC'S

1. OPERATIONAL AMPLIFIER
2. QUAD J-FET
3. LOW NOISE PRE AMP
4. PRE AMP
5. BUFFER AMP

COMMENTS:

1. ALL IC'S EXCEPT PROM ARE DI
2. ALL IC'S USE THIN FILM NICHROME
3. ALL IC'S USE Al METALIZATION
4. PROM IS JI

## TRIDENT C4 AUTOPILOT COMPUTER

DIGITAL IC'S

1. QUAD 2 NAND
2. DUAL 4 NAND
3. DUAL JK
4. DUAL 4-1 MULTIPLEXER
5. DUAL 2-4 DECODER
6. 4 x 4 REGISTER FILE
7. 4 BIT ALU
8. 4 BIT COUNTER
9. 4 BIT SHIFT REGISTER
10. 256 BIT RAM
11. 2048 BIT ROM

LINEAR IC'S

1. OPERATIONAL AMPLIFIER
2. FET DRIVER

COMMENTS:

1. ALL DIGITAL IC'S ARE LSTTL
2. ALL IC'S BUT ROM, RAM ARE DI, Au BEAM LEAD, DIFFUSED RESISTOR.
3. ROM, RAM ARE JI, Al METAL

## MX FLIGHT COMPUTER AND AIRS IMU

DIGITAL IC'S

1. QUAD 2 NAND
2. DUAL 4 NAND
3. DUAL JK
4. DUAL 4-1 MULTIPLEXER
5. DUAL 2-4 DECODER
6. 4 x 4 REGISTER FILE
7. 4 BIT ALU
8. 4 BIT COUNTER
9. 4 BIT SHIFT REGISTER
10. 1024 BIT ROM
11. 1024 BIT PROM

LINEAR IC'S

1. OPERATIONAL AMPLIFIER
2. ANALOG SWITCH
3. QUAD J-FET
4. VIDEO AMPLIFIER
5. VCO
6. LINE RECEIVER
7. PLATED WIRE SENSE AMP

COMMENTS:

1. ALL DIGITAL IC'S ARE LSTTL
2. ALL IC'S ARE DI EXCEPT PROM
3. PROM IS JI
4. ALL IC'S ARE Al METALIZED
5. ALL IC'S EXCEPT OP AMP USE DIFFUSED RESISTORS
6. OP AMP USES THIN FILM NICHROME RESISTORS

**TABLE 3-2**

#### 3.1.1.2 C4 Autopilot Computer

The C4 autopilot computer is a non-circumventable general register computer which is reinitialized by the guidance computer in the event of logic upset caused by transient radiation. The program storage uses 2048 bit JI, bipolar, mask programmable, read-only-memories (ROM) and the read/write storage uses 256 bit JI, bipolar random access memory (RAM). Both memory IC's are built by Monolithic Memories. Each memory IC uses an external current limiting resistor to prevent burnout during transient radiation, and the memory power supplies are shorted to ground upon detection of a radiation event to prevent burnout and recover the memories from latchup. All IC's are low power Schottky TTL, and no thin film resistors are used. All the parts except the ROM and RAM are DI, gold beam lead. The ROM and RAM use aluminum metalization. Development of the DI IC's was begun in 1972 at RCA, TI, and Motorola. The original DI part family also included a 1024 bit ROM and a 64 bit RAM. In the spring of 1977 the decision was made to use the JI memories, and RCA was selected as the supplier for the remaining DI IC's.

### 3.1.2 Missile–X

MX is currently in advanced development. Contracts will be issued in the spring and summer of 1978 to perform system definition of the aerospace vehicle equipment (AVE) (the missile). Full scale development of MX will proceed following the DSARC II.

#### 3.1.2.1 MX Flight Computer

The baseline processor for the missile is the MX Flight Computer and the development program was in source selection when this report was written. The performance requirements, architecture, memory technology, etc. will be defined during System Definition. A preferred parts list has been developed for MX AVE and the list is presented in Table 3-2. All the logic IC'S except for the 1K PROM are low power Schottky TTL, DI using aluminum metalization

and diffused resistors. The parts are based upon the technology developed for the C4 autopilot computer. The 1K PROM is the IC used in the C4 guidance computer, i.e. JI, NiChrome resistors, and power supply current limiting on chip.

#### 3.1.2.2 MX Advanced Computer Technology (ACT)

Early in 1975, MX began parallel, competitive contracts to develop an advanced AVE computer. The programs were to provide basic computer designs and a demonstration that the CMOS/SOS and MNOS/SOS technologies could support the development and qualification of an MX AVE computer. Computer designs were provided by both Rockwell and Northrop. From those designs, three MNOS/SOS memory IC's and 3 CMOS/SOS logic IC's were selected for development. Tables 3-3 and 3-4 describe the basic characteristics of the IC's being developed by Westinghouse (under Northrop subcontract) and Rockwell[1]. The MX Advanced Computer Technology Program is continuing its CMOS and MNOS developments to improve fundamental characteristics of the technologies such as gate oxide stability, radiation tolerance, and MNOS write speed, retention, and endurance.

### 3.2 Spaceborne Computers

Computers are flown on spacecraft that perform a wide range of missions from weather satellites to deep space probes to Mars landers. Every mission has its own set of processing and radiation requirements. This report will consider only a subset of the broad range of missions– military satellites.

Most computers on military satellites are designed for the natural radiation environment with the JCS hardening criteria as a goal for certain missions. Several computers are currently available that will withstand the natural radiation for some period of time and a sampling of these computers is described in Table 3-5. As the Table shows, many types of IC's are

## NORTHROP/WESTINGHOUSE ACT I IC'S

| PART TYPE | DESCRIPTION | FETS | SIZE | POWER[1] | SPEED[1] |
|---|---|---|---|---|---|
| TEMPORARY STORE MEMORY | –MNOS/SOS, Al GATE<br>–512 BITS (512 x 1) | ~ 3200 | 260 x 264 MILS<br>68640 $MIL^2$ | STANDBY: 1.5 mW<br>READ: 170 mW<br>WRITE: 122 mW | READ ACCESS: 250 NS<br>READ CYCLE: 450 NS<br>WRITE CYCLE: 1.2 $\mu$S<br>WRITE PULSE: 1.0 $\mu$S<br>(10 SEC RETENTION) |
| PERMANENT STORE MEMORY | –MNOS/SOS, Al GATE<br>–1024 BITS (256 x 4)<br>–PMOS DECODING<br>–WORD CLEAR | ~2700 | 237 x 260 MILS<br>61620 $MIL^2$ | STANDBY: 1.6 mW[2]<br>READ: 220 mW[2]<br>WRITE: 100 mW | READ ACCESS: 400 NS<br>READ CYCLE: 1 $\mu$S<br>WRITE CYCLE: 200 $\mu$S<br>(3 YR RETENTION)[2] |
| READ ONLY MEMORY | –CMOS/SOS, Al GATE<br>–1024 BITS (256 x 4)<br>–NITRIDE/OXIDE GATE INSULATOR | ~1600 | 140 x 200 MILS<br>28000 $MIL^2$ | STANDBY: 200 $\mu$W<br>READ: 90 mW<br>@ 2.5 MHz | READ ACCESS: 100 NS<br>READ CYCLE: 120 NS |

NOTES: 1. 25°C, PREREAD, TESTED WITH VARIOUS SAMPLE SIZES
2. SIMULATED

TABLE 3-3

## ROCKWELL ACT I IC's

| PART TYPE | DESCRIPTION | FETS | SIZE | POWER[1] | SPEED[1] |
|---|---|---|---|---|---|
| ELECTRICALLY ALTERABLE READ ONLY MEMORY | –MNOS/SOS, Aℓ GATE<br>–1024 BITS (1K x 1)<br>–PMOS DECODING<br>–BLOCK CLEAR | ~3200 | 143 x 232 MILS<br>33176 $MIL^2$ | STANDBY: 0.1 mW<br>READ: 600 mW<br>WRITE: 800 mW | READ ACCESS: 270 NS<br>READ CYCLE: 1 $\mu$S<br>WRITE CYCLE: 200 $\mu$S<br>CLEAR CYCLE: 2 MS |
| ARITHMETIC LOGIC UNIT | –CMOS/SOS, Aℓ GATE<br>–8 BIT ADDER/SUBTRACTOR, LEFT, RIGHT SHIFT PATHS, LOGICAL OPERATION | ~2100 | 202 x 234 MILS<br>47268 $MIL^2$ | 100 mW at 3 MHz<br>15 $\mu$W/GATE | 32 BIT PROPAGATION TIME: 320 NS<br>10 NS/GATE |
| HARDENED REGISTER FILE | –CMOS/SOS, Aℓ GATE<br>–8 x 8 BIT REGISTER<br>–FILE WITH DUPLICATION FOR HARDNESS | ~4000 | 248 x 248 MILS<br>61504 $MIL^2$ | ? | READ ACCESS: 110 NS<br>WRITE TIME: 125 NS |

NOTES: 1. 25°C, PRE RAD, TESTED WITH VARIOUS SAMPLE SIZES.

TABLE 3-4

## SATELLITE COMPUTERS

| | CDC 469 | DF 224 | SCP-234 | Alpha 16 |
|---|---|---|---|---|
| Architecture | General Register<br>Fixed Point | General Register<br>Fixed Point | Single Accumulator<br>Fixed Point | General Register<br>Fixed Point<br>PDP 11/40 Software Compatible |
| Data Word Size | 16 Bits | 24 Bits | 16 Bits<br>32 Bits Double Precision | 16 Bits |
| Logic | PMOS Custom | PMOS Custom | CMOS/Bulk, Aℓ Gate 4000 Series and Custom | Bipolar STTL – AMD 2901 Family |
| Memory | Plated Wire or Semiconductor(1) | Plated Wire | 256 x 1 CMOS/Bulk RAMS<br>PMOS/Bulk ROM | Semiconductor(1) |
| Status | In Production<br>Mid 70's | In Production<br>Mid 70's | In Production Since Early 70's<br>Used on DMSP Block 5D | Brassboard - Fall 1977<br>To be used for DSCS III Attitude Control |
| Manufacturer | Control Data Corp | Autonetics | RCA | GE |

**Notes:** 1. Technology is optional.
2. All computers hardened to natural environment.

TABLE 3-5

being used on board satellites. Because of the minimum power and weight constraints placed on satellites, custom MOS has been in use for quite some time, and bit slice LSI is already being applied. (A further discussion of bit slices can be found in section 3.4.1). The 4000 series CMOS/bulk IC's used in the SCP-234 are part of a family of 38510, Class A, SSI/MSI devices built by RCA. The current radiation hardened family is listed in Table 3-6. Another popular logic family for space applications is JI, low power Schottky, TTL, SSI/MSI which can be procured from several manufactures to 38510, Class A screens and from TI it can be procured to Class S. TI will sell any IC in its LSTTL catalogue to Class A or Class S up to and including parts as dense as the 54L187 1024 bit PROM.

### 3.3 Avionics Computers

The ICBM and satellite computers receive a great deal of emphasis (especially in the radiation hardening community) but by far the largest number of computers that the Air Force uses go into avionics or even ground based systems. This category encompasses most of the data processing functions found in Command, Control, and Communication ($C^3$) systems (Table 3-7). The worst case radiation that these machines are designed for is that which a human can tolerate. Current computers in the man-rated radiation class employ any IC that is Class B qualified including NMOS microprocessors such as the 8080 and 6800. In fact, the 8080A was designed into several systems (including the B-1) on nonstandard part waivers even before it completed qualification.

Even though new designs are evolving toward microprocessors, many of the avionics computers in production today use TTL logic and either core or NMOS memory. An example of a modern avionics computer is the ANYK-15 built by Westinghouse:

- 16 bit fixed point
- 32 bit floating point
- 48 bit extended precision floating point
- 16 general registers
- TTL logic

## RCA CLASS A CMOS PARTS

| Functions | RCA CD Part Type | 38510 Slash Sheet |
|---|---|---|
| Quad 2 Input Nand | 4011A | 5001 |
| Dual 4 Input Nand | 4012A | 5002 |
| Triple 3 Input Nand | 4023A | 5003 |
| Dual D Flip-Flop | 4013A | 5101 |
| Dual J-K Flip-Flop | 4027A | 5102 |
| Dual 3 Input NOR + Inverter | 4000A | 5201 |
| Dual 2 Input NOR | 4001A | 5202 |
| Dual 4 Input NOR | 4002A | 5203 |
| Triple 3 Input NOR | 4025A | 5204 |
| Dual Complementary Pair & Inverter | 4007A | 5301 |
| Quad And-Or Select | 4019A | 5302 |
| 4 Bit Full Adder | 4008A | 5401 |
| Hex Buffer-Inverting | 4009A | 5501 |
| Hex Buffer-Non Inverting | 4010A | 5502 |
| Hex Buffer-Inverting | 4049A | 5503 |
| Hex Buffer-Non Inverting | 4050A | 5504 |
| Quad True/Complement Buffer | 4041A | 5505 |
| Decade Counter | 4017A | 5601 |
| Divide By N Counter | 4018A | 5602 |
| 14 Stage Counter | 4020A | 5603 |
| Divide By 8 Counter | 4022A | 5604 |
| 7 State Binary Counter | 4024A | 5605 |
| 18 Stage Static Shift Register | 4006A | 5701 |

Note: The parts are CMOS/bulk, aluminum gate. RCA will sell them on a lot jeopardy basis to a $10^5$ rads total dose specification at no additional cost and will accept orders for $10^6$ rad parts.

**TABLE 3-6**

# $C^3$ DATA PROCESSING FUNCTIONS

- SENSORY DATA PROCESSING FUNCTIONS
  - RADAR INPUT
  - RADAR SCHEDULING & RE-DIRECTION
  - DATA COMPRESSION
- COMMUNICATIONS DATA PROCESSING FUNCTIONS
  - LINK/NETWORK PROTOCOL HANDLING
  - MESSAGE ASSEMBLY/DISASSEMBLY
  - MESSAGE BUFFERING
  - MESSAGE ROUTING
  - MESSAGE RECORDING
- INFORMATION PROCESSING FUNCTIONS
  - DATA BASE MANAGEMENT
    - –ENTERING DATA
    - –RETRIEVING DATA
    - –MODIFYING DATA
    - –DELETING DATA
  - INFORMATION PRESENTATION
    - –HARD COPY
    - –DISPLAY SCREEN
  - OPERATIONAL SUPPORT
    - –MISSION PLANNING
    - –SCHEDULING
    - –MONITORING
  - OPERATOR INPUT PROCESSING
    - –PRIORITY PROCESSING
    - –STATUS INFORMATION DISPLAY
  - TESTING AND TRAINING
    - –SIMULATION
    - –COMPUTER AIDED INSTRUCTION
    - –MODELING
- MAN-MACHINE INTERACTION
  - FORMATTING
  - CURSOR CONTROL
  - INTELLIGENT TERMINALS
- INTEROPERABILITY CONSIDERATION
  - COORDINATION OF JOINT COMMAND ACTIVITES
  - UNIFORM LEVEL OF INFORMATION
  - INTERFACE WITH OTHER $C^3$ SYSTEMS
    - –SECURITY
    - –CONVERSION
    - –COMPATIBILITY

**Table 3-7**

**(Reference 1)**

The ANYK-15 has been selected by the Air Force Avionics Laboratory as the computer for the Digital Avionics Information System (DAIS) and DOD is considering specifying the ANYK-15 as a standard architecture for the Air Force.

## 3.4 Advanced Hardened Computers

### 3.4.1 Microcomputers

The trend in all systems, military or commercial, hardened or unhardened, is toward the use of more and more microcomputers to give the computing capability and flexibility that all systems desire in a small, inexpensive package. The military, near term microcomputer based systems will primarily use devices that are already on the market, have a good history, are supported with adequate hardware and software aides, and are Class B qualified (or qualifiable).

A list of 8 microprocessors representative of what is available to the military system designer is presented in Table 3-8. The processors were selected from a field of 70 plus candidates available today for the following reasons:

- MCS-8080A: The 8080 is an NMOS device introduced about 5 years ago as the original 8 bit microprocessor, and it is one of the most popular (if not the most popular) 8 bit microprocessor today. As such, it has a broad base of application and support (assemblers, simulations, etc.) software available. Prices are currently in the $4-$5 range for quantity orders of commercial parts, and shipments from all suppliers for 1977 were 1,100,000[2]. The 8080A is available from Intel as a Class B part and is already designed into military systems as a non-standard component.

- **MC68B00:** The 6800 is also a very popular 8-bit NMOS microprocessor being qualified as a Class B part. The 6800 microprocessor and support family is designed with digital communications applications in mind. Its 1977 shipments were 745,000.[2]

- **MCS6502:** The 6502 is similar to the 6800 in its orientation to digital communications and is supplied by a company with experience in MOS radiation hardening (Rockwell). Its 1977 shipments were 755,000.[2]

- **Z80-A:** The Z80 is an NMOS, upgraded version of the 8080A with an enhanced instruction set and a higher clock frequency. Much of the popularity of the Z80 results from its similarity to the 8080A. Its 1977 shipments were 180,000.[2]

- **CDP-1802:** The 1802 was selected because it is a CMOS device (the only 8-bit CMOS microprocessor readily available) and reportedly may be developed as a CMOS/SOS product. The great deal of government sponsored research into radiation hardening of CMOS may be applicable to the 1802 and its SOS counterpart. Its 1977 shipments were 147,000.[2]

- **TMS9900:** The N-channel version of the 9900 was selected because it was one of the first 16-bit microprocessors. Its 1977 shipments were 95,000.[2]

- **SBP9900:** The $I^2L$ version of the 9900 was selected because it is a 16-bit microprocessor, it was developed as a military product by SAMSO, and preliminary, small sample radiation tests indicate that the process may be relatively hard.

- **Am2901A:** A bit slice is included in the study because of the speed and flexibility offered by the bit slice approach to processors. The Schottky TTL 2901 was selected because of its high performance and its popularity. It is being qualified as a 38510 part.

## REPRESENTATIVE MICROPROCESSORS

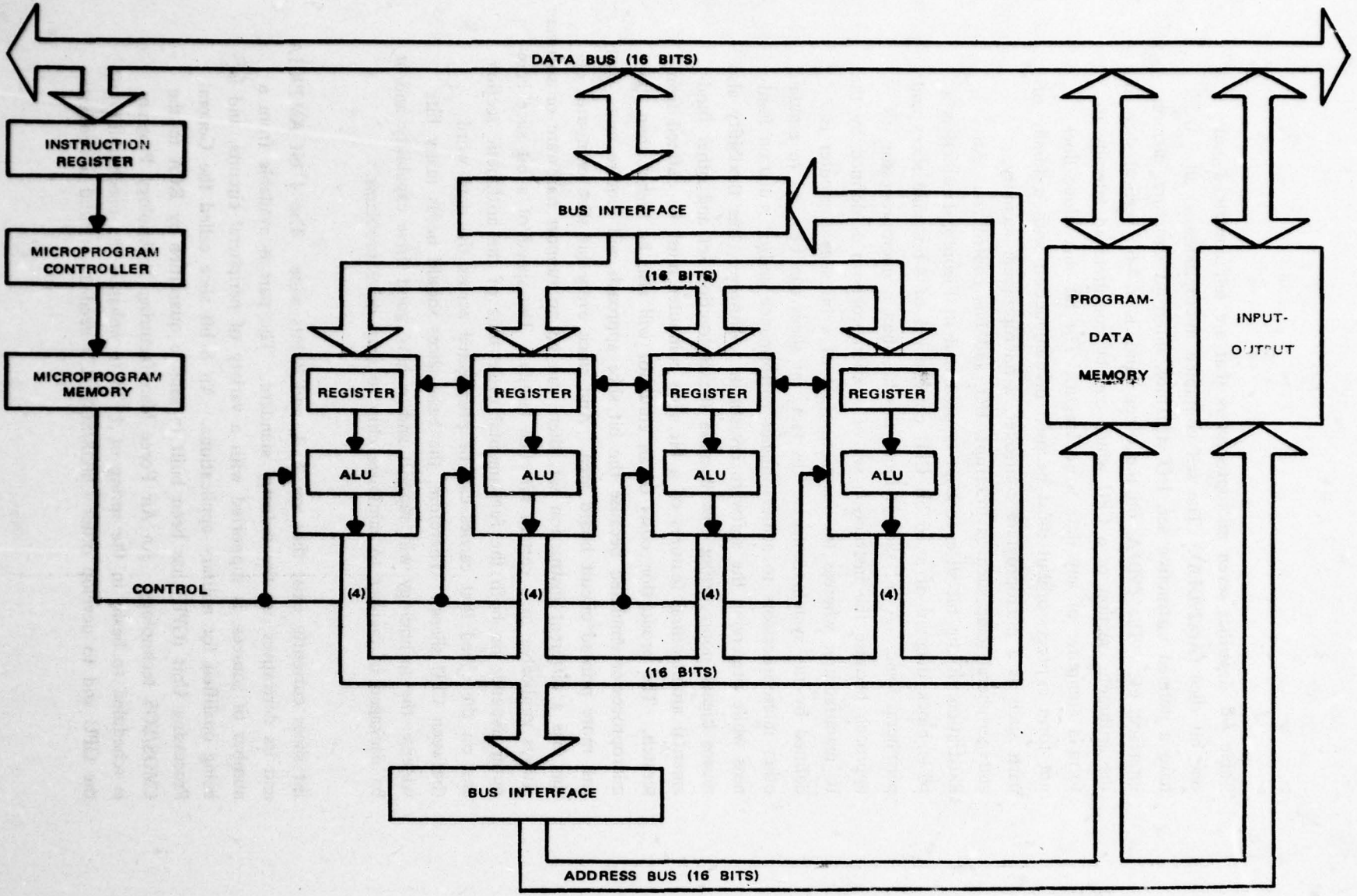
| | MCS-8080A | MC6800 | MCS6502A | Z80-A | CDP1802 | TMS9900 | SBP9900 | Am2901A[4] |
|---|---|---|---|---|---|---|---|---|
| Data Word Size (Bits) | 8 | 8 | 8 | 8 | 8 | 16 | 16 | 16 |
| Max Clock Frequency (MHz) | 3 | 2 | 2 | 4.5 | 6.4 | 3 | 2 | 5[5] |
| Representative Instruction Execution | | | | | | | | |
| Memory to Register Add[1] | | | | | | | | |
| Min Time ($\mu$s)/(Memory Accesses) | 2.1/(2) | 1.5/(3) | 1.5/(3) | 1.5/(2) | 2.5/(2) | 4.6/(4) | 7/(4) | 0.6/(3) |
| Register to Register Add | | | | | | | | |
| Min Time ($\mu$s)/(Memory Accesses) | 1.3/(1) | 1.0/(2) | — | 0.9/(1) | — | — | — | 0.2/(1) |
| Load[1] | | | | | | | | |
| Min Time ($\mu$s)/(Memory Accesses) | 2.1/(2) | 1.0/(2) | 1.5/(3) | 1.5/(2) | 2.5/(2) | 4.6/ (4) | 7/(4) | 0.6/(3) |
| Required Memory Cycle Time ($\mu$s) | 0.333 | 0.500 | 0.500 | 0.222 | 0.400 | 0.333 | 0.500 | 0.200 |
| Directly Addressable Memory (Words) | 64K | 64K | 64K | 64K | 64K | 32K | 32K | 64K |
| Power (Watts) | 0.850 | 0.500 | 0.700 | 0.300 | 0.150[2] | 0.850 | 0.500 | 3.2[6] |
| Technology | NMOS | NMOS | NMOS | NMOS | CMOS | NMOS | $I^2L$ | STTL |
| Sources | Intel[2]<br>NEC<br>AMD<br>National<br>Signetics<br>TI | Motorola[7]<br>American Microsystem<br>Fairchild | Mostec<br>Rockwell<br>Synertek | Zilog<br>Mostec<br>Sharp | RCA[7]<br>Hughes<br>SSS | TI[7]<br>American Microsystem | TI | AMD[7]<br>Fairchild<br>Motorola<br>National<br>Raytheon<br>Signetics |

NOTES:
1. Memory referenced instructions usually assume zero page addressing (address 0 → 256)
2. Mil Qualified Part Available (38510 Class B)
3. Executing a Branch Instruction, 10V supply.
4. Am2901 is a 4-bit slice, the 16 bit application shown is based on an AMD Application Note.
5. The Am2901 will clock up to 15 MHz.
6. Four 4-bit Am2901's.
7. Being qualified to 38510

TABLE 3-8

Table 3-8 describes seven microprocessors that are self contained and one bit slice (Am2901A). The self contained microprocessors all have a defined instruction set, I/O structure, interrupt structure, memory interface, etc. The 2901A, on the other hand, is a 4-bit vertical slice of the arithmetic section of a CPU which can be concatenated laterally to form a computer of any data word length. The bit slice alone does not form a processor but must be used in conjunction with a family of parts such as a microprogram controller, a microprogram memory, and peripheral logic such as interrupt, I/O, and bus controllers. An illustration of the bit slice concept is presented in Figure 3-1 which is a basic block diagram of a 16 bit CPU constructed of 4-bit wide slices and peripheral logic. A bit slice is more flexible than a microprocessor approach because the instruction set of a microprocessor is defined by the IC manufacturer whereas the instruction set of a bit slice computer is defined by the system designer. In fact, bit slices can be used to emulate other microprocessors to achieve higher performance and/or radiation hardness while preserving the software investment. However, this flexibility also means higher nonrecurring cost because the instruction set and other fundamental architectural features of a bit slice computer must be defined from scratch. The production costs of an emulator will also be higher than the microprocessor emulated because the bit slice approach will require more parts and more printed circuit board area. And since every bit slice computer design has a different instruction set, there can be no support hardware or software always applicable to a certain bit slice family. The speed of a bit slice computer depends on both the fundamental cycle time of the arithmetic section and on the speed that carries can be propagated across the data word (between CPU slices). Therefore, the basic slices should be as many bits wide as the technology will support and/or have good drive capability and/or be packaged in manner to minimize chip to chip drive problems.

Bit slices currently exist that are 2, 4, and 8 bits wide. The 4 bit AM2901A and its derivatives are the industry standard. The part is available from a number of sources, is supported with a variety of peripheral circuits, and is being qualified for military applications. An 8 bit slice called the General Processing Unit (GPU) has been built in sample quantities by RCA in the CMOS/SOS technology. An Air Force Manufacturing Technology Program is scheduled to begin in the spring of 1978 to enhance the producibility of the GPU and to develop other CMOS/SOS IC's needed to build a computer




BASIC ARCHITECTURE OF A 16 BIT COMPUTER USING 4 BIT SLICES

FIGURE 3-1

with the GPU. Five of the parts to be fabricated are described in Table 3-9. All of the IC's in the Table have been built in sample quantities. In addition, two different microprogram controllers will be built during the Manufacturing Technology program. One will be a functional equivalent of the Am2910 which is the latest controller for the 2901 family and the other will be a special purpose design. The CMOS/SOS IC's will be designed to operate through 50,000 rads of total ionizing dose and will be qualified to 38510 Class B. The effort is scheduled for completion in the spring of 1980.

### 3.4.2 ICBM Computers

Beyond C4 and the current MX designs, the trend in ICBM computers may be toward task distributed microcomputer based systems. The on board missile processing would be divided into tasks such as guidance/ navigation, autopilot, I/O, telemetry, etc. each of which could be handled by a separate microcomputer. Such an approach could conceivably achieve higher bandwidth computers while using hardened read/ write memory that is one to two orders of magnitude slower in write speed than plated wire.

Although the potential benefits of a task distributed ICBM processor are many, it is really only practical if true LSI or even VLSI can be used for the logic. For instance, if one assumes that 10 separate task processors are needed and that the SBP9900 microprocessor could perform each task, then the comparison between a 9900 based distributed system and a system built with LSTTL MSI might be (not considering memory):

| | | Single Processor | 10 Processors |
|---|---|---|---|
| Estimated Gates | 9900 | 6000 | 60,000 |
| | LSTTL | 6000 | 60,000 |
| Parts Count | 9900 | 1 | 10 |
| | LSTTL | ~ 250 | ~ 2500 |
| Power Supply Current | 9900 | ~ 500 mA | ~ 5 A |
| | LSTTL | ~ 7200 mA | ~ 72 A |

## RCA CMOS/SOS MANUFACTURING TECHNOLOGY IC'S

| Part Type | Description | FETS | Size | Power[1] | Speed[1] |
|---|---|---|---|---|---|
| Random Access Memory (TCS072) | CMOS/SOS, Si Gate<br>1024 Bits (256 x 4)<br>Pin Compatible with Intel 2101<br>5 transistors/cell | | 156 x 185 mils | 6.5mW/MHz (5pf load) | Access: 110ns (85pf load) |
| Read Only Memory (TCS075) | CMOS/SOS, Si Gate<br>1024 Bits<br>Mask Programmable | ~1600 | 132 x 144 mils | 12mW/MHz (60pf load) | Access: <150ns (60pf load) |
| General Processor Unit (TCS074) | CMOS/SOS, Si Gate<br>8 Bit CPU Slice Containing<br>16, 8 bit registers<br>8 bit ALU<br>Can be concatenated to form larger word size CPU's | ~2900 | 201 x 215 mils | | Register-Register On Chip Operations: <80ns<br>Register to Data Of Chip Operations <200ns |
| Gate Universal Array (TCS091) | CMOS/SOS, Si Gate<br>300 Cells<br>256 Internal<br>44 I/O & Driver<br>Circuit Function Defined By metal mask | | 175 x 175 mils | | 3.0ns Pair Delays |
| Multiplier (TCS077) | CMOS/SOS, Si Gate<br>8 Bit Expandable 2's Complement | ~2200 | 181 x 175 mils | 72mW/MHz | 8 x 8 Multiply: <280ns (18pf load) |

**Notes:** 1. Typical, 25°C, 10V, Prerad

Table 3-9

The parts count, power, etc. associated with a distributed system probably means that LSI would have to be available before the concept makes sense for an ICBM, and of course, the distributed system must be radiation hard. But just as LSI allows consideration of new computer architectures not practical with MSI, LSI may also allow different hardening techniques to be used. Specifically a system approach to hardening might be used, i.e., shield penalties might be reduced because the box is smaller and transient survivability could be addressed as a system power management problem because the parts count and power supply currents are lower.

The critical concern with transient survivability is to prevent catastrophic failure. The failure mode of concern is burnout of an IC junction or metalization run because of high current drain from the supply. The high current can be caused by large photocurrents or by a combination of junctions demonstrating latchup. The latchup also creates another problem – even if the circuit does not burn out, it can no longer function as logic. Therefore, to guard against the failure, (1) the power supply current that an IC can draw must be limited to a safe level and/or the power supply must be turned off before the IC receives enough energy to burn out and (2) latchup must be prevented and/or the SCR action must be stopped. The classical approach to the problem has been to fabricate DI IC's to prevent the latchup and limit the current on the IC with resistors. C4, however, has chosen to design semiconductor read only program memories with JI IC's and address latchup at a system level. The memories employ either on chip (guidance computer) or off chip (autopilot computer) current limiting resistors and address possible latchup with either a power strobe (guidance) or power shutoff (autopilot). The resistors and the timing of the power supply shutoff are designed so that between the time the radiation event begins (photocurrents begin to flow) and the time the power supply current is shutoff, the IC does not receive enough energy to burn out. Then, since the power has been shut off, any junctions that did latch are unlatched and normal operation can be resumed when the event is over and power is restored.

Thus, C4 has chosen a system design approach to transient radiation survivability. As digital devices become denser, the more attractive it becomes to consider system approaches for the entire computer. As logic devcies move toward VLSI and an entire CPU on a chip, more gates will be on each IC and each gate will consume less power. Therefore, as hardened computers evolve from MSI to LSI, the parts counts and the power will be lower. Fewer limiting resistors will be needed and less power supply current will have to be switched to protect against catastrophic failure caused by transient radiation. Clearly, the overhead of a limiting resistor and a transistor power supply switch for each IC should be seriously considered before LSI is rejected for hardened systems because of latchup or before DI LSI is attempted solely to prevent latchup.

Of course, the hardened LSI computer must contend with the other radiation problems of EMP, neutron induced failure, total dose failure, logic upset, etc. But before the technology is asked to support high failure levels, other system approaches such as shielding must be fully explored. It is also possible that a distributed LSI computer will have such high throughput that the upset threshold can be lower and more upsets per mission can be tolerated without degradation of mission performance.

Another important consideration with task distributed ICBM computers is the range of requirements that the various tasks place on the processor. For instance, the guidance task might need 48 bit floating point words but minimal throughput while the autopilot task might require high speed calculations but only 16 bit fixed point words. It might not be practical to strive for a single microprocessor that will perform all tasks. A more credible approach could be to consider a basic microprocessor that fits most tasks and a bit slice family for tasks that require unique capabilities such as 48 bit words. The bit slice processor(s) could be designed to emulate the microprocessor so all the software aids would apply, and the bit slices could be built from the same technology on the same process line as the microprocessor.

Thus, LSI brings to ICBM computers the possibility for

- –Task distributed processing
- –Elimination of plated wire memories
- –Higher bandwidth computers
- –System approaches to transient survivability and elimination of the requirement for DI IC's solely for latchup prevention.

### 3.4.3 Satellite Computers

The thrust in requirements for the next generation of satellite computers seems to be in four general areas.

- Very high throughput for sensor data compression and other purposes. (Some planned sensor systems desire computers of several hundred million operations per second.)
- Gigabit and larger memories.
- Ultra high reliability for longer life, autonomous systems.
- Increased survivability.

The throughput goals will likely be addressed with distributed processors performing tasks on a parallel basis, and because of the power, weight, and volume contraints of spaceborne systems, LSI and VLSI will be needed. As the level of integration increases, the reliability requirements can possibly be approached with redundant processors while still meeting the throughput goals and physical constraints.

Continued emphasis on survivability will force consideration of all the nuclear weapon related effects. It is anticipated that design techniques similar to those postulated for ICBM's can be used to harden satellite systems. In fact, most spaceborne computer applications such as attitude control and sensor data compression can tolerate longer down times following a transient radiation upset than can ICBM computers. The control

algorithms for spacecraft have much longer time constants than the ICBM algorithms, and thus a satellite attitude control computer can be off for longer periods of time than an ICBM computer can before attitude control of the respective vehicle is lost. As for sensor data compression, if one frame of data is lost because of transient upset, another frame can be taken with minimal loss of information. Thus, the transient survivability problem for satellite computers is one of preventing catastrophic failure and the system level approaches being considered for latchup and burnout protection for ICBM's can be applied to spaceborne processors. Therefore, non-DI LSI can be considered for hardened space computers.

The memory problem for future spaceborne systems will be just as demanding as the processor problem [3,4,5]. By the year 2000, spaceborne sensors may be capable of collecting as much as $10^{10}$ to $5 \times 10^{11}$ bits/sec of data. In order to alleviate a tremendous burden on the space communication system, the desire is to compress this data to about $10^7$ bits/sec without loss of significant information. Therefore, in the worst case, $5 \times 10^{11}$ bits/sec would have to be stored on the spacecraft so the processor(s) could manipulate the data. The $5 \times 10^{11}$ rate is based on high resolution imagery (photographic quality) which would require approximately 250,000 x 250,000 picture elements (pixels), per frame at 8 bits/pixel. If one assumes 1024 parallel, 16 bit processors compressing the data, then each processor data memory would have to store $5 \times 10^{11} \div 1024 = 4.88 \times 10^8$ bits/sec. If each memory were 16 bits wide, then $4.88 \times 10^8 \div 16 = 3.05 \times 10^7$ words/sec would be stored which means the memory cycle time would have to be 32 nanosec just to store the data. Therefore, in this worst case, 1024 memories, 16 bits x 30 million words with a write cycle time of 32 nanosec would be required. This memory could probably be either random access or serial so high density serial memories such as bubbles are clearly interesting to the space community. In addition to the requirements for high density, high speed, low power, low weight, and small size, spaceborne mass memories should be nonvolatile so that data can be stored on one orbit and down linked on a later orbit.

It is obvious that the space planners are counting on VLSI to support the processing needs of the future.

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### 3.4.4 Manned Systems

The majority of Air Force computer applications will continue to be in system that have man-rated radiation requirements. Since these systems have already started to use microprocessors, they will undoubtably continue to apply the latest LSI as soon as it becomes MIL qualified. For instance, Table 3-10 illustrates some $C^3$ systems in development that have identified microprocessor applications. Hardness of the technology will be considered but the primary microprocessor selection criteria will be performance (speed, word length, instruction length, etc.), availablity, software support, number of sources, reliability, etc. However, the prospect of producting microcomputers of the required man-level hardness is not totally bleak.

It may be possible to approach hardened microcomputers by using hardened bit slices to emulate soft devices that are already designed into systems. This approach allows the investment in software to be preserved while achieving hardness. The family of devices used for emulation:

- Should allow insertion into the system with a minimum of redesign-possibly change one board.
- Must be at least as fast as the microprocessor to be replaced.
- Must use no more power than the device replaced.

This approach is already being studied by Air Force Avionics Laboratory for at least two different processors[6,7]. An emulation of the 8080 using the AFML CMOS/SOS family is being studied, and an evaluation of bit slice approaches to emulating the DAIS ANYK-15 is being conducted.

The 2901A family could probably be used today for emulation and thereby provide a microcomputer that meets man-level hardness. The basic problems in emulating an 8080 with the 2901 series would be power and parts count. Two 2901's are nominally twice the power of an 8080A(0.8W vs 1.6W), to say nothing of the external devices that would be needed to completely emulate the 8080. Furthermore, the emulator would not fit in a 40 pin dual in-line package as the 8080 does. Other technologies such as CMOS/SOS and $I^2L$ look more attractive

## REPRESENTATIVE MICROPROCESSOR $C^3$ APPLICATIONS

| Project | Current/Planned Microprocessor Applications | | |
|---|---|---|---|
| | Number of Types | Total Number | Uses |
| ATEC | ? | 500-1000 | Controller subsystem<br>Interface communication subsystem<br>Station subsystem |
| AFSATCOM | 2 | 600 | Modems<br>Teletypes<br>High Speed Printers |
| NORAD CMC Improvement Program | 3 | 30 | Translator for digital display |
| E-4 Airborne Command and Control | 1 | 25 | Intelligent Terminals<br>Link control modules |
| TACC Automation 485L | ? | ? | Communication line controllers<br>Display stations<br>Computer processor<br>Peripheral control unit |

**Table 3-10**
**(Reference 1)**

than LSTTL for emulation because of their higher density and lower power.

Another approach to increase the hardness of a system which already uses a soft microprocessor would be to increase the fundamental hardness of the device to the environments to which it is susceptible. For instance, it would be desirable to increase the total dose hardness of an NMOS IC to a level above the man related specification. This might be achieved by having an existing manufacturer process devices with the only process modification being a temperature reduction, to say less than 900°C, for all steps after gate oxide growth.

In addition, if the selected commercial technology is susceptable to latchup at least three options are available for achieving pin-to-pin (or almost) replacement.

- External power limiting and switching as described in previous sections of this report can be used.

  –Advantage: No change to the LSI is needed to protect against latchup and burn out.

  –Disadvantage: The system design is complicated somewhat by the addition of a limiting resistor, a radiation detector, a one shot, and a power switch.

- Dielectric isolated LSI can be developed.

  –Advantage: The device will probably be a pin-for-pin replacement of the soft device.

  –Disadvantage: The technology potentially will not be in the mainstream commercially.

- The devices needed for radiation detection, power limiting, and power switching could be put directly on the LSI device.

  –Advantages: Potentially a pin-for-pin replacement of the soft part.
  Potentially could use the same basic process as the commercial product with different masks.

  –Disadvantages: A custom circuit element must be designed and added to the basic LSI device.
  Potentially the power dissipation will be higher than the commercial LSI.
  The IC will be larger.
  Quality control and assurance on the detector may be difficult.

### 3.5 Summary

Hardened computers can be grouped into three general categories according to the severity of the radiation environment.

- ICBM's
- Space Systems
- Manned Systems

Because each of the three categories of applications are quite different, each class of system uses logic IC's that are quite different. The current ICBM computers all use TTL because it is the only mature technology that has demonstrated the required across the board (neutron, transient, total dose) hardness. The space systems are concerned with high reliability, low power and total dose hardness and therefore primarily use LSTTL and CMOS/bulk aluminum gate. The logic IC's in most manned systems are constrained only to be qualified to 38510 Class B.

The trend in all categories is toward LSI computers. In some cases the LSI is desirable to remove current design constraints (plated wire in ICBM computers) and in other cases the LSI is mandatory to achieve desired system performance (spaceborne sensor data compression). In all hardened LSI computers the technology will have to be carefully selected by considering p[e]rformance, availability, commercial interest, hardness, etc. Systems approaches to certain aspects of hardening such as transient radiation survivability should also be carefully considered before the development of exotic LSI is attempted. Even after all the system level hardening design is incorporated, certain constraints will undoubtedly be placed on the IC (such as total dose hardening for NMOS). The desire is that these constraints be minimized so that hardened LSI can be a derivative of commercial LSI. To achieve the proper balance between specifications, computer design, and LSI design, close cooperation between the government, the system designer, and the semiconductor designer will be needed.

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## 4.0 LSI Testing

### 4.1 Background

Testing is being recognized as one of the most difficult and costly aspects of LSI development and production. Testing for most products and applications can be divided into two categories: (1) design verification testing, and (2) production or screen testing.

Design verification tests are necessary to validate that the LSI meets all the functional and electrical requirements as specified. In the purest sense, complete functional testing means that all the possible logic states should be explicitly tested. However, full explicit testing is impossible because for even reasonably complex devices, the number of tests is astronomical. For instance, the GPU (Table 3-9) has $2^{180}$ states to be tested. $2^{180}$ states equates to $10^{48}$ tests and even at 1 nanosec per test it would take $10^{31}$ years to complete the tests. Therefore, the test vectors to be run during design verification testing must be judiciously chosen and designed to achieve acceptable coverage of the device within reasonable time bounds. LSI vendors typically use a limited set of vectors to perform design verification testing and let the users find the subtle errors. This has happened with several of the popular microprocessors such as the 8080A, the 6800 and the 2901A. In addition to functional testing, design verification includes testing of all the electrical parameters of the part in all specified combinations of power supply variations, temperature, etc. This testing requires expensive, sophisticated equipment such as Fairchild Sentry VII's or Tektronix 3260's.[1] The LSI manufacturer usually performs this electrical parametric testing rather carefully so that he understands his process and can maximize his yield.

Once the LSI device goes into production, the flavor of testing that the manufacturer performs changes. Since much of the final cost of an LSI product is determined by how long it was tested and how much the test equipment cost to buy and operate, the manufacturer strives for the minimum production line testing (screening) that will satisfy the customers. Screening normally consists of exercising 90% - 95% of the nodes to test for stuck

ats and varying the clock speed and power supply levels above and below specification while monitoring a selected set of outputs. A relatively small number of vectors are used. Motorola currently uses 850 vectors for the 6800 and performs the testing at several frequencies and voltages. Each device is on test for 2 to 3 seconds in a Sentry VII tester.[1] This kind of screening can lead to a product being shipped that will just not perform the job as advertised over the full range of specified temperature/voltage/speed combinations. The problem has forced the Jet Propulsion Laboratory (JPL) to conduct an exhaustive LSI test program.[2] After three years of testing, W. Richard Scott, group supervisor of the electronic parts section for JPL, comments, "the manufacturer is more concerned with getting his product out the door than in nailing down all the specifications," and Larry Hess, LSI system task leader for JPL complains, "Our test managers notice time after time that memory parts will not meet timing requirements of the spec. A setup or hold time that should be 0 is actually 10 nanoseconds."

The LSI testing problem, which is a headache for the commercial user, is even worse for the military user. Microprocessors are just beginning to be Class B qualified with the Intel 8080A completing qualification in January 1978, after over a year of test vector design and testing by RADC, Intel and GE. The manufacturers are constantly improving products and introducing new ones so that military qualification will probably get further behind the commercial market. And, of course, radiation testing of LSI is in an even more embryonic stage than electrical qualification. Some exploratory radiation testing of microprocessors such as the 8080A and the SBP9900 has been done, but no one has yet reported completing a full radiation characterization of a microprocessor. Now is the time for the government to take the lead in LSI radiation testing before industry applies devices of unknown hardness to military systems. The next section describes a basic approach to microprocessor testing that could be applied by the government to begin a comprehensive LSI radiation evaluation program.

### 4.2 Radiation Testing

To assess the problems and complexities involved in radiation testing of LSI, Questron analyzed the 2901A relative to types of tests to be considered and the parameters of interest. It was assumed that the characterization would be done in anticipation of applying the 2901A in an ICBM system so all the radiation environments (i.e., neutrons, total dose, transient and EMP) should be considered.

The radiation tests for LSI devices should be approached in two phases:

- Quick-look failure assessment.
- Detailed characterization.

The objective of the quick-look radiation testing of a new LSI device is to roughly determine the failure level of the device in the environment expected to be the most destructive (which happens to be neutrons for the bipolar 2901A). The testing should be as inexpensive as possible and used only to determine if the device shows enough promise for the intended application. If the device does show promise, more detailed characterization testing should be conducted.

For the 2901A, the quick look testing could be conducted as follows:

- Fabricate a printed circuit board test fixture that contains a 40-pin socket for the 2901A. This board should have power supply, ground and clock connections, and it should provide a method for hardwiring (via jumpers) the data and control inputs to either $V_{cc}$ or ground. Connectors for oscilloscope monitoring of outputs should also be provided.

- Wire the test fixture so the 2901A repetitively cycles through one calculation. For instance, address any register in the A field, set the control pins (I) for incrementing, add a carry-in, and monitor the outputs. The register will count up.

- Perform pre-radiation characterization of the 5-part test sample to determine the frequency range of operation of the IC in the test fixture.

- Passively irradiate the devices to some initial neutron fluence, such as $10^{12}$ n/cm$^2$.

- Determine the performance degradation of the parts.

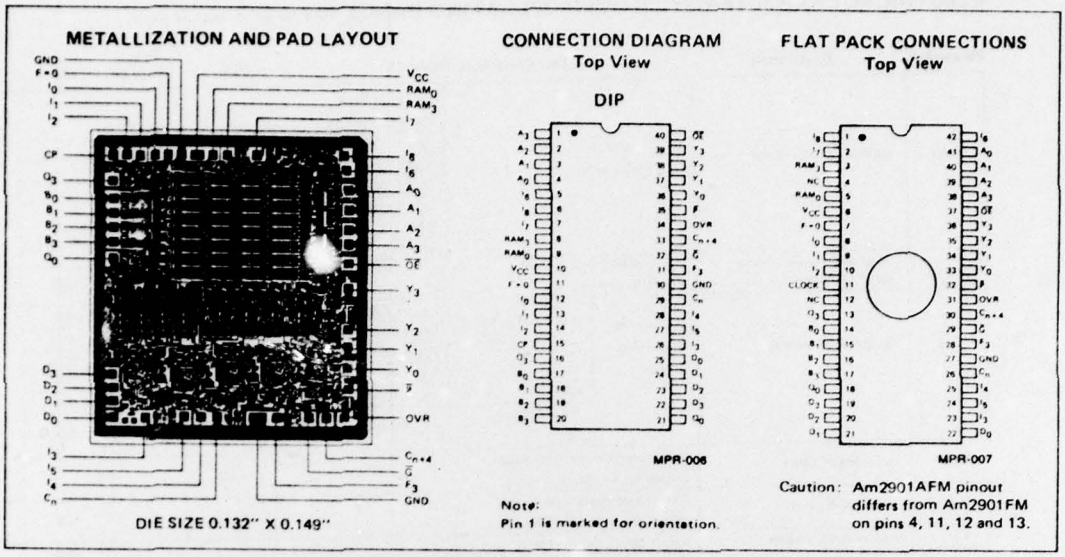
- Continue the irradiation and characterize the parts after each half or full order of magnitude of fluence. Continue testing until the parts fail.

This very basic approach can be embellished by using a more elaborate test fixture that exercises other portions of the 2901A and/or performing the characterizations on a programmable LSI tester.

If the results of the quick-look assessment are promising, then detailed characterization must be performed to collect the data that is required in order to use the 2901A in a hardened system. As a minimum, the following parameters must be determined: the speed and fanout degradation of all outputs and data paths as a function of neutron fluence, the upset threshold, the neutron annealing characteristics, photocurrent generation, performance degradation as a function of total dose, and susceptibility to EMP transients.

For the 2901A, the detailed characterization will be tedious and difficult to instrument. For instance, there are 14 outputs (Table 4-1, Figure 4-1[3]) using four different types of output drivers ($I_{ON}$ varies from $-1.6$mA to $600\mu$A) (Table 4-2). The fanout characteristics of each output as a function of neutron fluence must be determined, i.e., the $V_{OH}$, $V_{OL}$, $I_{OH}$, and $I_{OL}$ changes must be characterized. This test will almost certainly require a pin programmable LSI tester such as a Tektronix 3260 or Fairchild Sentry VII.

To determine the speed degradation as a function of neutron fluence in enough detail to allow a computer to be designed with adequate margin, 51 different propagation delays (Table 4-3, Table 4-4) must be measured. The delay paths are the appropriate combination of exercising 10 types of inputs while monitoring 8 types of outputs. Of course, some of the inputs such as the RAM address (A,B) have multiple combinations and the dependence on set-up and hold times (Table 4-5) must be determined so the number of possible test vectors can become very large. A judicious selection of vectors should be made by analyzing the gate diagram to determine the longest path and the gates with the highest internal fanout. Again, a programmable LSI tester would be the best way to perform the characterization. In the case of the 2901A, it might be possible to procure the basic test software from either the IC manufacturer or the tester manufacturer so the radiation test designer can select a subset of vectors from software that is already debugged. The total dose testing of the 2901A can be conducted with a Cobalt 60 source and data taken in a manner similar to that used to take steady state neutron data.




## PIN DEFINITIONS

**$A_{0-3}$** The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

**$B_{0-3}$** The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

**$I_{0-8}$** The nine instruction control lines to the Am2901A, used to determine what data sources will be applied to the ALU ($I_{012}$), what function the ALU will perform ($I_{345}$), and what data is to be deposited in the Q-register or the register stack ($I_{678}$).

**$Q_3$ $RAM_3$** A shift line at the MSB of the Q register ($Q_3$) and the register stack ($RAM_3$). Electrically these lines are three-state outputs connected to TTL inputs internal to the Am2901A. When the destination code on $I_{678}$ indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the $Q_3$ pin and the MSB of the ALU output is available on the $RAM_3$ pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

**$Q_0$ $RAM_0$** Shift lines like $Q_3$ and $RAM_3$, but at the LSB of the Q-register and RAM. These pins are tied to the $Q_3$ and $RAM_3$ pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

**$D_{0-3}$** Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the Am2901A. $D_0$ is the LSB.

**$Y_{0-3}$** The four data outputs of the Am2901A. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code $I_{678}$.

**$\overline{OE}$** Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

**$\overline{P}$, $\overline{G}$** The carry generate and propagate outputs of the Am2901A's ALU. These signals are used with the Am2902 for carry-lookahead.

**OVR** Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

**F = 0** This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs $F_{0-3}$ are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

**$F_3$** The most significant ALU output bit.

**$C_n$** The carry-in to the Am2901A's ALU.

**$C_{n+4}$** The carry-out of the Am2901A's ALU.

**CP** The clock to the Am2901A. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

**Table 4-1**

## Am2901A
## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | $I_{OH}$ = −1.6mA $Y_0, Y_1, Y_2, Y_3$ | 2.4 | | | Volts |
| | | | | $I_{OH}$ = −1.0mA, $C_{n+4}$ | 2.4 | | | |
| | | | | $I_{OH}$ = −800μA, OVR, $\overline{P}$ | 2.4 | | | |
| | | | | $I_{OH}$ = −600μA, $F_3$ | 2.4 | | | |
| | | | | $I_{OH}$ = −600μA $RAM_{0,3}$, $Q_{0,3}$ | 2.4 | | | |
| | | | | $I_{OH}$ = −1.6mA, $\overline{G}$ | 2.4 | | | |
| $I_{CEX}$ | Output Leakage Current for F = 0 Output | $V_{CC}$ = MIN., $V_{OH}$ = 5.5V $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | 250 | μA |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $Y_0, Y_1, Y_2, Y_3$ | $I_{OL}$ = 20mA (COM'L) | | | 0.5 | Volts |
| | | | | $I_{OL}$ = 16mA (MIL) | | | 0.5 | |
| | | | $\overline{G}$, F = 0 | $I_{OL}$ = 16mA | | | 0.5 | |
| | | | $C_{n+4}$ | $I_{OL}$ = 10mA | | | 0.5 | |
| | | | OVR, $\overline{P}$ | $I_{OL}$ = 8.0mA | | | 0.5 | |
| | | | $F_3$, $RAM_{0,3}$, $Q_{0,3}$ | $I_{OL}$ = 6.0mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 7) | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 7) | | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | | Clock, $\overline{OE}$ | | | −0.36 | mA |
| | | | | $A_0, A_1, A_2, A_3$ | | | −0.36 | |
| | | | | $B_0, B_1, B_2, B_3$ | | | −0.36 | |
| | | | | $D_0, D_1, D_2, D_3$ | | | −0.72 | |
| | | | | $I_0, I_1, I_2, I_6, I_8$ | | | −0.36 | |
| | | | | $I_3, I_4, I_5, I_7$ | | | −0.72 | |
| | | | | $RAM_{0,3}$, $Q_{0,3}$ (Note 4) | | | −0.8 | |
| | | | | $C_n$ | | | −3.6 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | Clock, $\overline{OE}$ | | | 20 | μA |
| | | | | $A_0, A_1, A_2, A_3$ | | | 20 | |
| | | | | $B_0, B_1, B_2, B_3$ | | | 20 | |
| | | | | $D_0, D_1, D_2, D_3$ | | | 40 | |
| | | | | $I_0, I_1, I_2, I_6, I_8$ | | | 20 | |
| | | | | $I_3, I_4, I_5, I_7$ | | | 40 | |
| | | | | $RAM_{0,3}$, $Q_{0,3}$ (Note 4) | | | 100 | |
| | | | | $C_n$ | | | 200 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | | 1.0 | mA |
| $I_{OZH}$ $I_{OZL}$ | Off State (High Impedance) Output Current | $V_{CC}$ = MAX. | | $Y_0, Y_1, Y_2, Y_3$ $V_O$ = 2.4V | | | 50 | μA |
| | | | | $Y_0, Y_1, Y_2, Y_3$ $V_O$ = 0.5V | | | −50 | |
| | | | | $RAM_{0,3}$, $Q_{0,3}$ $V_O$ = 2.4V (Note 4) | | | 100 | |
| | | | | $RAM_{0,3}$, $Q_{0,3}$ $V_O$ = 0.5V (Note 4) | | | −800 | |
| $I_{OS}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. + 0.5V, $V_O$ = 0.5V | | $Y_0, Y_1, Y_2, Y_3, \overline{G}$ | −30 | | −85 | mA |
| | | | | $C_{n+4}$ | −30 | | −85 | |
| | | | | OVR, $\overline{P}$ | −30 | | −85 | |
| | | | | $F_3$ | −30 | | −85 | |
| | | | | $RAM_{0,3}$, $Q_{0,3}$ | −30 | | −85 | |
| $I_{CC}$ | Power Supply Current (Note 6) | $V_{CC}$ = MAX. (See Fig. 12) | Am2901APC, DC | $T_A$ = 25°C | | 160 | 250 | mA |
| | | | | $T_A$ = 0°C to +70°C | | 160 | 265 | |
| | | | | $T_A$ = +70°C | | 160 | 220 | |
| | | | Am2901ADM, FM | $T_C$ = −55°C to +125°C | | 160 | 280 | |
| | | | | $T_C$ = +125°C | | 160 | 190 | |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. *These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with $I_{678}$ in a state such that the three-state output is OFF.*
5. "MIL" = Am2901AXM, DM, FM. "COM'L" = Am2901AXC, PC, DC.
6. Worst case $I_{CC}$ is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

Table 4-2

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR Am2901A

Tables **3, 4,** and **5** below define the timing characteristics of the Am2901A over the operating voltage and temperature range. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with $V_{IL}$ = 0V and $V_{IH}$ = 3.0V. For three-state disable tests, $C_L$ = 5.0pF and measurement is to 0.5V change on output voltage level. Input rise and fall times are 1ns/V. All outputs fully loaded.

**TABLE 4-3**

**CYCLE TIME AND CLOCK CHARACTERISTICS**

| TIME | COMMERCIAL | MILITARY |
|---|---|---|
| Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle) | 100ns | 110ns |
| Maximum Clock Frequency to Shift Q Register (50% duty cycle) I = 432 or 632 | 15MHz | 12MHz |
| Minimum Clock LOW Time | 30ns | 30ns |
| Minimum Clock HIGH Time | 30ns | 30ns |
| Minimum Clock Period | 100ns | 110ns |

| |
|---|
| Commercial = Am2901APC, DC, XC<br>$T_A$ = 0°C to +70°C<br>$V_{CC}$ = 4.75 to 5.25V |
| Military = Am2901ADM, FM, XM<br>$T_C$ = -55°C to +125°C<br>$V_{CC}$ = 4.50 to 5.50V |

**TABLE 4-4**

**GUARANTEED COMBINATIONAL PROPAGATION DELAYS** (all in ns, $C_L$ = 50pF (except output disable tests))

| From Input \ To Output | COMMERCIAL | | | | | | | | MILITARY | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Y | $F_3$ | $C_{n+4}$ | $\overline{G}$, $\overline{P}$ | F=0 $R_L$= 270 | OVR | Shift Outputs $RAM_0$ $RAM_3$ | Shift Outputs $Q_0$ $Q_3$ | Y | $F_3$ | $C_{n+4}$ | $\overline{G}$, $\overline{P}$ | F=0 $R_L$= 270 | OVR | Shift Outputs $RAM_0$ $RAM_3$ | Shift Outputs $Q_0$ $Q_3$ |
| A, B | 80 | 80 | 75 | 65 | 87 | 85 | 95 | – | 85 | 85 | 80 | 70 | 97 | 90 | 100 | – |
| D (arithmetic mode) | 45 | 45 | 45 | 35 | 57 | 55 | 65 | – | 50 | 50 | 50 | 40 | 62 | 60 | 70 | – |
| D (I = X37) (Note 5) | 40 | 40 | – | – | 52 | – | 60 | – | 45 | 45 | – | – | 57 | – | 65 | – |
| $C_n$ | 30 | 30 | 20 | – | 47 | 30 | 50 | – | 35 | 35 | 25 | – | 52 | 35 | 55 | – |
| $I_{012}$ | 55 | 55 | 50 | 45 | 67 | 65 | 75 | – | 60 | 60 | 55 | 50 | 72 | 70 | 80 | – |
| $I_{345}$ | 55 | 55 | 55 | 50 | 67 | 65 | 75 | – | 60 | 60 | 60 | 55 | 72 | 70 | 80 | – |
| $I_{678}$ | 30 | – | – | – | – | – | 30 | 30 | 35 | – | – | – | – | – | 35 | 35 |
| $\overline{OE}$ Enable/Disable | 35/25 | – | – | – | – | – | – | – | 40/25 | – | – | – | – | – | – | – |
| A bypassing ALU (I = 2xx) | 45 | – | – | – | – | – | – | – | 50 | – | – | – | – | – | – | – |
| Clock ↓ (Note 6) | 60 | 60 | 60 | 50 | 72 | 70 | 80 | 30 | 65 | 65 | 65 | 55 | 82 | 75 | 85 | 35 |

**GUARANTEED SET-UP AND HOLD TIMES** (all in ns) (Note 1) **TABLE 4-5**

| From Input | Notes | COMMERCIAL | | MILITARY | |
|---|---|---|---|---|---|
| | | Set-Up Time | Hold Time | Set-Up Time | Hold Time |
| A, B Source | 2, 4<br>3, 5 | 100<br>$t_{pw}L$+30 | 0 | 110<br>$t_{pw}L$+30 | 0 |
| B Dest. | 2, 4 | $t_{pw}L$+15 | 0 | $t_{pw}L$+15 | 0 |
| D (arithmetic mode) | | 70 | 0 | 75 | 0 |
| D (I = X37) (Note 5) | | 60 | 0 | 65 | 0 |
| $C_n$ | | 55 | 0 | 60 | 0 |
| $I_{012}$ | | 80 | 0 | 85 | 0 |
| $I_{345}$ | | 80 | 0 | 85 | 0 |
| $I_{678}$ | 4 | $t_{pw}L$+30 | 0 | $t_{pw}L$+30 | 0 |
| $RAM_{0, 3}$, $Q_{0, 3}$ | | 25 | 0 | 25 | 0 |

Notes: 1. All times relative to clock LOW-to-HIGH transition.
2. If the B address is used as a source operand, allow for the "A, B source" set-up time; if it is used only for the destination address, use the "B dest." set-up time.
3. Where two numbers are shown, both must be met.
4. "$t_{pw}L$" is the clock LOW time.
5. D V 0 is the fastest way to load the RAM from the D inputs. This function is obtained with I = 337.
6. Using Q register as source operand in arithmetic mode, Clock is not normally in critical speed path when Q is not a source.

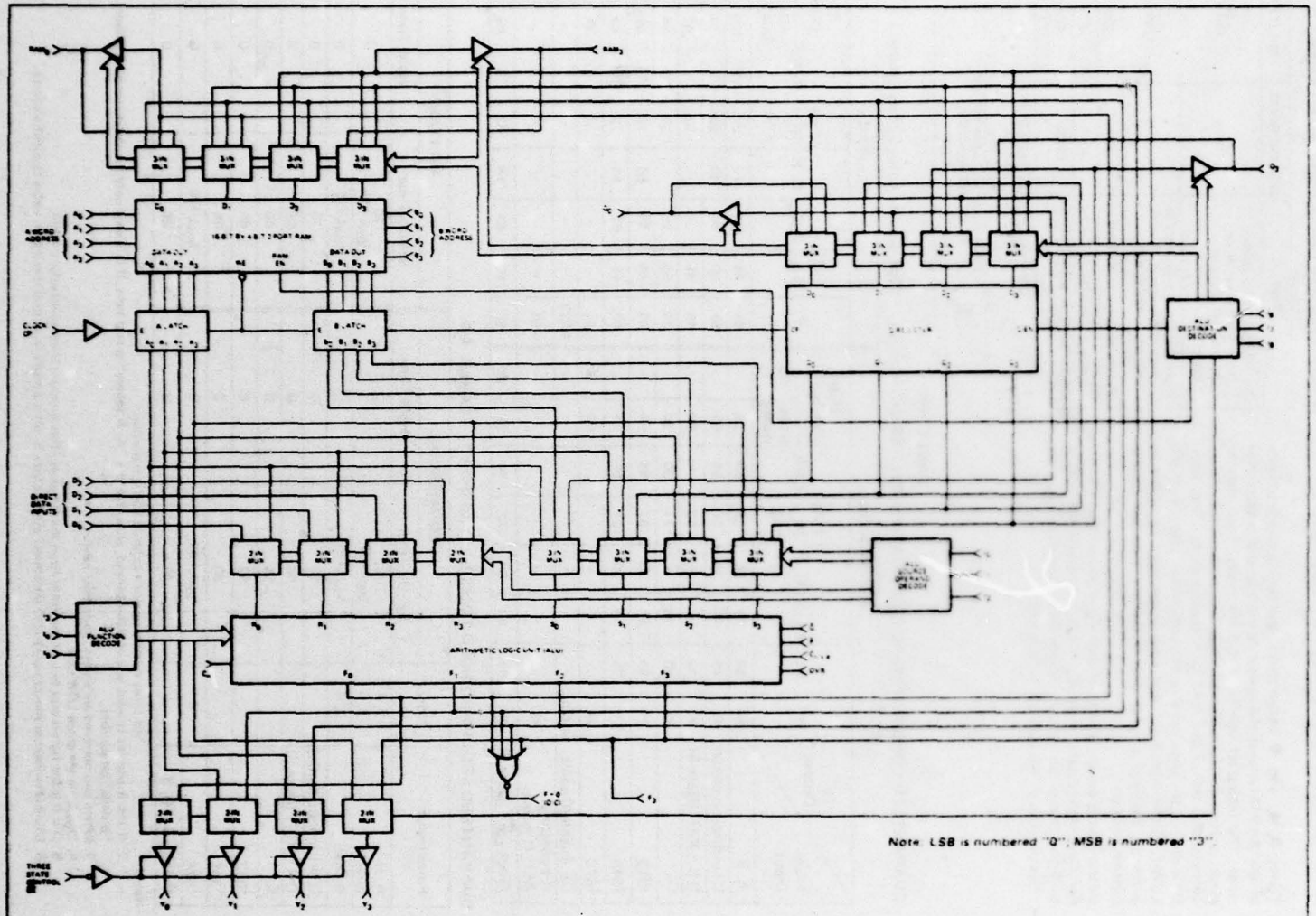



**FIGURE 4-1.** Detailed Am2901A Microprocessor Block Diagram.

The transient and neutron annealing tests require the most sophisticated instrumentation, but the data must be available before a rad hard computer can be designed. The 2901A will have to be exercised with a series of vectors chosen to enhance the failure probability. The 2901A's actual outputs during the test will have to be stored for post test comparison with expected outputs or compared in real time using test fixture hardware.

One approach to upset testing is to design and fabricate a test "box" that contains some number of test vectors (say 256) in a ROM. The test "box" drives the 2901A and performs a hardware comparison of actual versus expected outputs. With a 200ns clock, it will take 51.2$\mu$s to complete the vector set, and thus a LINAC delivering a pulse of a few microseconds in width could be used to completely test the vector field with fewer than 15 shots synchronized to coincide with various sections of the vector field. For instance, a LINAC pulse of 4$\mu$s full-width-half-maximum would encompass about 20 vectors. If the first shot was centered on vector 10, the second would be centered on vector 30, the third on vector 50, etc., until all vectors were covered. The advantage of the long pulse for upset testing is that the pulse is slow enough relative to the 2901A cycle speed that the opportunity exists to detect the threshold as the dose rate increases; i.e., actually monitor the onset of failures as a function of dose rate.

The same test box could be used for survivability and neutron annealing tests with appropriate cabling and shielding. The 2901A, being a bipolar device, will be able to drive some length of cable without resorting to buffers.

The purpose of photocurrent testing is to determine the IC's survivability against very high dose rate environments. A flash X-ray with a short pulse (several tens of nanoseconds) will have to be used to achieve the high dose rates. For this test, the 2901A could almost be statically biased into one state rather than being cycled through a series of vectors. The power supply current will have to be monitored to determine the photocurrent generation. This data, along with an analysis of the current carrying capability of the metalization and junctions, would determine how big the off chip current limiting resistors would have to be to prevent burnout induced by transient radiation.

EMP testing could be conducted in the standard manner; i.e., a high voltage pulse generator can drive the outputs to determine the energy required to destroy the transistors.

The purpose of detailed characterization is to determine the 2901A's radiation performance in enough detail to allow a computer designer to apply the part in a system designed for a specific radiation environment. Obviously, the expensive testing (probably the transient and neutron annealing tests) should be conducted only after it has been determined that the device performs well enough in the other environments (fan out, speed, etc.).

Radiation testing of LSI is a difficult, costly and time consuming endeavor. It will require much more cooperation and coordination between the physicist, the test engineer and the computer designer than testing SSI/MSI ever did. With the proliferation of LSI types, manufacturers and applications, ways must be found to perform quick-look testing as a rather routine matter to weed out the IC's that clearly cannot support radiation hardened applications. Quick-look testing seems to be a natural for a government agency that has access to radiation sources, LSI test equipment and the computer design expertise necessary to design and conduct the tests. The field of devices to chose from is already large (microprocessors, memories and bit slices) and selection can be influenced by already existing applications (8080's, for instance) and by SPO plans for future systems. A government agency can also perform some of the detailed characterization and can certainly provide the expertise in radiation facility utilization and instrumentation needed to guide the computer design contractor in his efforts to complete the detailed characterization. Therefore, Questron recommends that an appropriate government organization with adequate facilities and manpower be designated as the agency responsible for performing quick-look radiation testing of LSI and for collaborating with SPO's on detailed characterization.

## REFERENCES FOR 4.0


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2.) L. Waller, "Tests Show Spotty LSI Record", Electronics; February 2, 1978; Vol. 51, No. 3.

3.) Advanced Micro Devices, Inc., Am2900 Bipolar Microprocessor Family, 1976.

## 5.0 Conclusions and Recommendations

### 5.1 Conclusions

The next generation of radiation hardened computers will need LSI/VLSI to reach desired performance levels (space-based sensors) or to eliminate undesirable aspects of current system implementations (plated wire memories in ICBM's). The state-of-the-art and the projections for commercial LSI/VLSI indicate that it will support the military performance requirements–speed, density, etc. However, it is questionable whether the IC technologies that have traditionally been thought of as radiation hard will be able to support the future military LSI/VLSI applications. Developers of hardened, digital systems should remove any a priori judgment of what the LSI/VLSI technology should be and let the system requirements and the market place select the technology(ies).

The benefits of LSI/VLSI cannot be fully utilized if undo constraints are placed on the IC in order to meet system radiation specifications. Thus, the system designer ought to apply all available hardening design techniques (current limiting, power strobing, shielding, etc.) before specifying unique or exotic semiconductor technologies.

Before LSI/VLSI can be applied to hardened systems, extensive radiation characterization is required. There is currently no systematic approach to LSI radiation testing. Since electrical and functional testing of LSI has proven to be a bigger problem than originally anticipated, radiation characterization efforts should get underway immediately.

#### 5.1.1 Technology Conclusions

- *The little data available on NMOS radiation effects indicate that it* is quite "soft". It may be possible, however, to improve the hardness of this technology significantly by slight process changes. The wide usage of NMOS gives this approach to hardened technology development great leverage, and it should be pursued.

- TTL will continue to be useful in higher performance bit slice oriented processing elements and in emulators. It does not appear, however, that TTL can overcome its fundamental limitations in power and packing density to become a useful VLSI technology.

- $I^2L$ appears to have all the requirements needed to qualify as the prime radiation hardened LSI/VLSI technology. It has the beginnings of a strong commercial base (with all the performance advantages this entails) and a proven ability to meet high radiation levels with chips which are true LSI/VLSI. Here too, it would be profitable to determine how much the commercial process could be hardened by slight process changes rather than to develop an entirely new version of $I^2L$ which may not have the producibility or reliability of the commercial version.

- There is a sharp difference of opinion between commercial producers of bulk CMOS LSI as to its potential for VLSI. In view of the weight which Questron attaches to commercial viability, it would be inconsistent for this report to recommend major action in the bulk CMOS technology until the market place has adjudicated this dispute.

- The recent agreement between RCA and Intel would seem to put new life into CMOS/SOS for commercial applications. Questron recommends that the radiation hardness of the commercial version of CMOS/SOS be investigated so that the comparison between this technology and others can be done on an equitable basis.

- In general, Questron recommends that commercial viability be a prerequisite for technologies to be considered for radiation hardened LSI/VLSI applications.

## 5.2 Recommendations

Questron recommends that R&D in radiation hardened LSI/VLSI should be directed toward the goal of making available to military system designers the full range of performance available to commercial systems designers. To facilitate this end, military systems should not exclude arbitrarily any candidate technology because of susceptibility to failure mechanisms which can be addressed at a system level.

Evaluation of the radiation sensitivity of processes should emphasize those of known commercial potential. Only those modifications which are considered minor should be permitted in this evaluation. (Ingenuity and innovation will be required to determine exactly what modifications are "minor".)

Unique LSI/VLSI processes will be extremely expensive to develop, and should be attempted only when the most compelling reasons exist. When such reasons are judged to exist, appropriate funding must be made available to provide the technology development effort with the resources needed to accomplish the enormous task of unique process development.

Specific technology development recommendations which build on these principles are as follows:

- A systematic program of LSI/VLSI radiation testing should address both the development and refinement of testing techniques, and the actual conduct of the tests. A government laboratory should take the lead in this activity.

- A study of commercial LSI/VLSI fabrication processes should be undertaken to determine specific modifications which can be made to these processes to increase radiation hardness without affecting producibility. (One indication that producibility has been maintained would be the preservation of all design rules).

- A widely used microprocessor (such as the 8080) should be manufactured in one or more of the candidate technologies, using commercial processes modified as described above to enhance hardness without degrading producibility. This sort of an exercise is the only way to resolve arguments about the relative superiority of one technology over another for radiation hardened LSI/VLSI applications.

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