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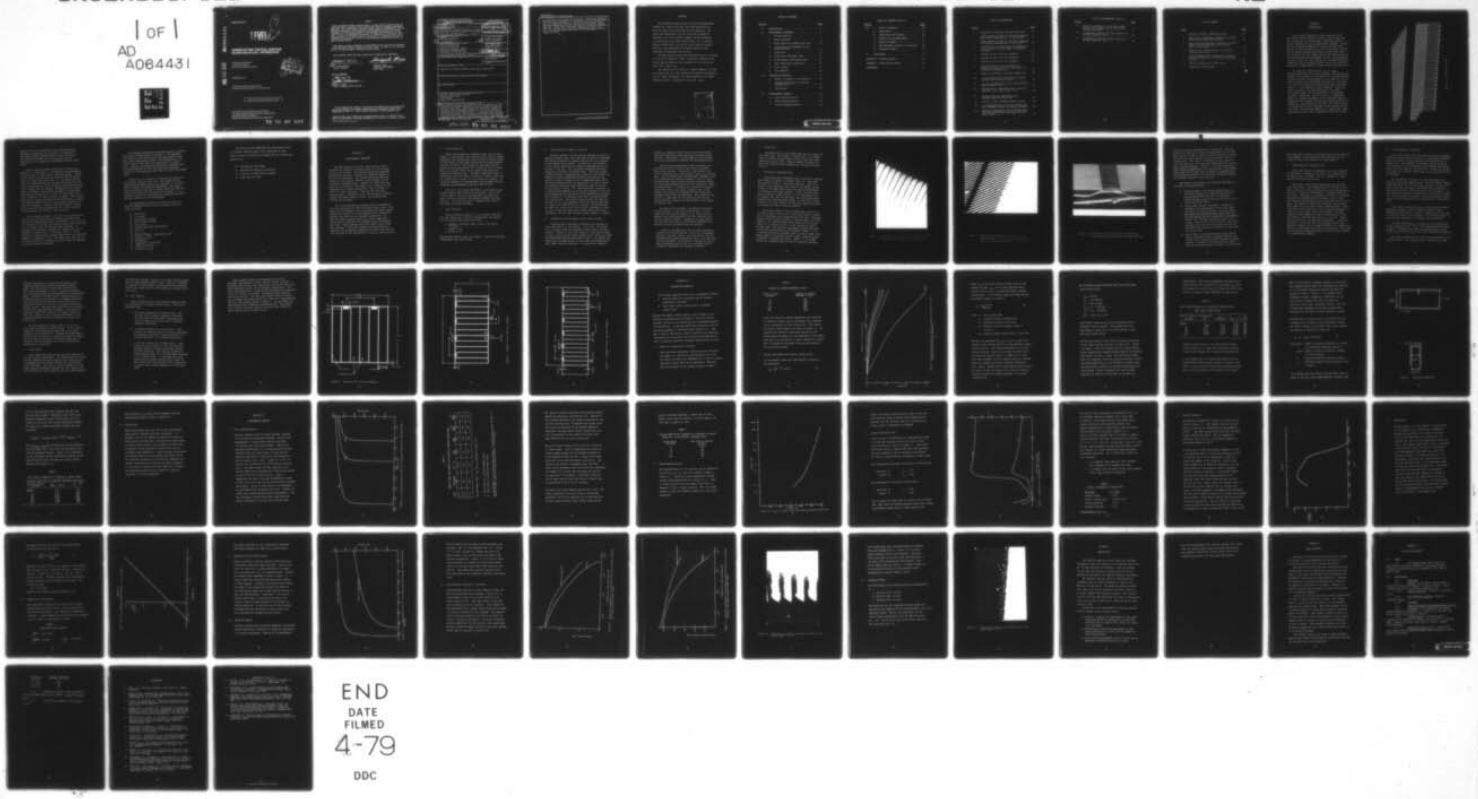

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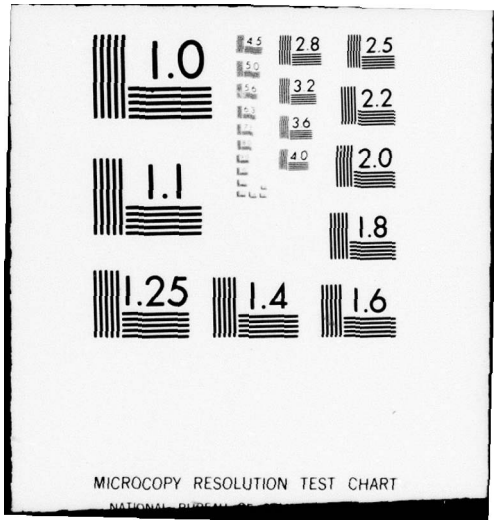
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Final Report for Period April 1976 – November 1978

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This technical report has been reviewed and is approved for publication.

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FOR THE COMMANDER

James D. Reams
Chief, Aerospace Power Division

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This research program has resulted in the development of high conversion efficiency radiation resistant vertical junction silicon solar cells. New techniques of oxidation growth and the use of photolithography enable the use of an orientation dependent etch to produce grooves 5 - 10 microns wide and up to 100 microns deep. These silicon wafers have been processed into solar cells with all processes performed at temperatures compatible with producing high efficiency solar cells. Theoretical

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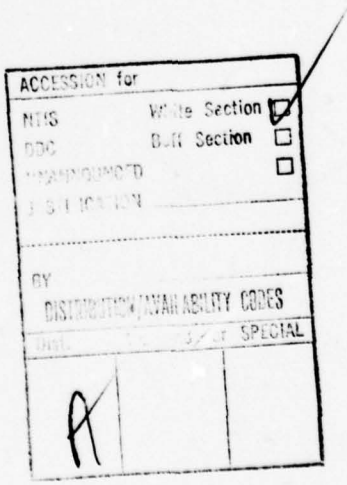
calculations of the expected current as a function of radiation dose have been performed. An explanation of the observed open-circuit voltage is provided. Vertical junction solar cells have been fabricated with AM0 conversion efficiencies greater than 14%. These cells have shown superior radiation resistance. Vertical junction cells have been fabricated in 2cm x 2cm, 2cm x 4cm and 2cm x 6cm sizes with no size dependence on efficiency or yield.

FOREWORD

This Technical Report covers all work performed under Contract No. F33615-75-C-2058, entitled "Nonreflecting Vertical Junction Silicon Solar Cell Optimization." The effort was sponsored by the Air Force Aero Propulsion Laboratory, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio under Project 3145. Dr. W. Patrick Rahilly (AFAPL/POE-2) was the Air Force Project Engineer, while Dr. John Wohlgemuth of Solarex Corporation was technically responsible for the work.

The work reported herein was performed during the period 15 May 1976 to August 31, 1978. Report No. AFAPL-TR-77-38 was an Interim Report on this project for the time period April 1976 - April 1977.

The authors wish to thank Dr. Joseph Lindmayer for helpful suggestions, Mr. Alan Scheinine for computer programming and Mr. Daniel Whitehouse, Mr. Donald Warfield, Mr. Robert Merkling and Mr. R. Edwards for cell fabrication.



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SECTION I

INTRODUCTION

This research program at Solarex has led to the development of the vertical junction silicon solar cell into a practical high efficiency radiation resistant device available for use in space power systems. Solarex has now fabricated hundreds of these high efficiency devices in various sizes up to 12 cm^2 cell area. Because of thin improved radiation resistance these cells offer the potential for the highest end-of-life efficiencies of any silicon solar cells produced to date. This radiation resistant solar cell can prolong the lifetime of missions, reduce the initial weight of solar arrays and allow the placement of experiments in certain orbits now prohibited.

The vertical junction solar cell has deep grooves etched into the silicon surface. The grooves are etched close together (on the order of 15 microns between centers) so that only thin walls (on the order of 5 to 10 microns thick) are left between the grooves. The solar cell junction follows the surface up and down the walls. Figure 1 is a diagram of such a geometry. Since the walls are narrow, carriers generated in the walls, by incident light, are already close to a collecting junction. Therefore, even if the cell is exposed to radiation causing a decrease in the diffusion length (a measure of the distance the carriers can move without recombining), the carriers in the walls will still be able to transverse the short distance to the junction and be collected. This may be compared to a planar cell, where many carriers must travel from deep in the bulk to the

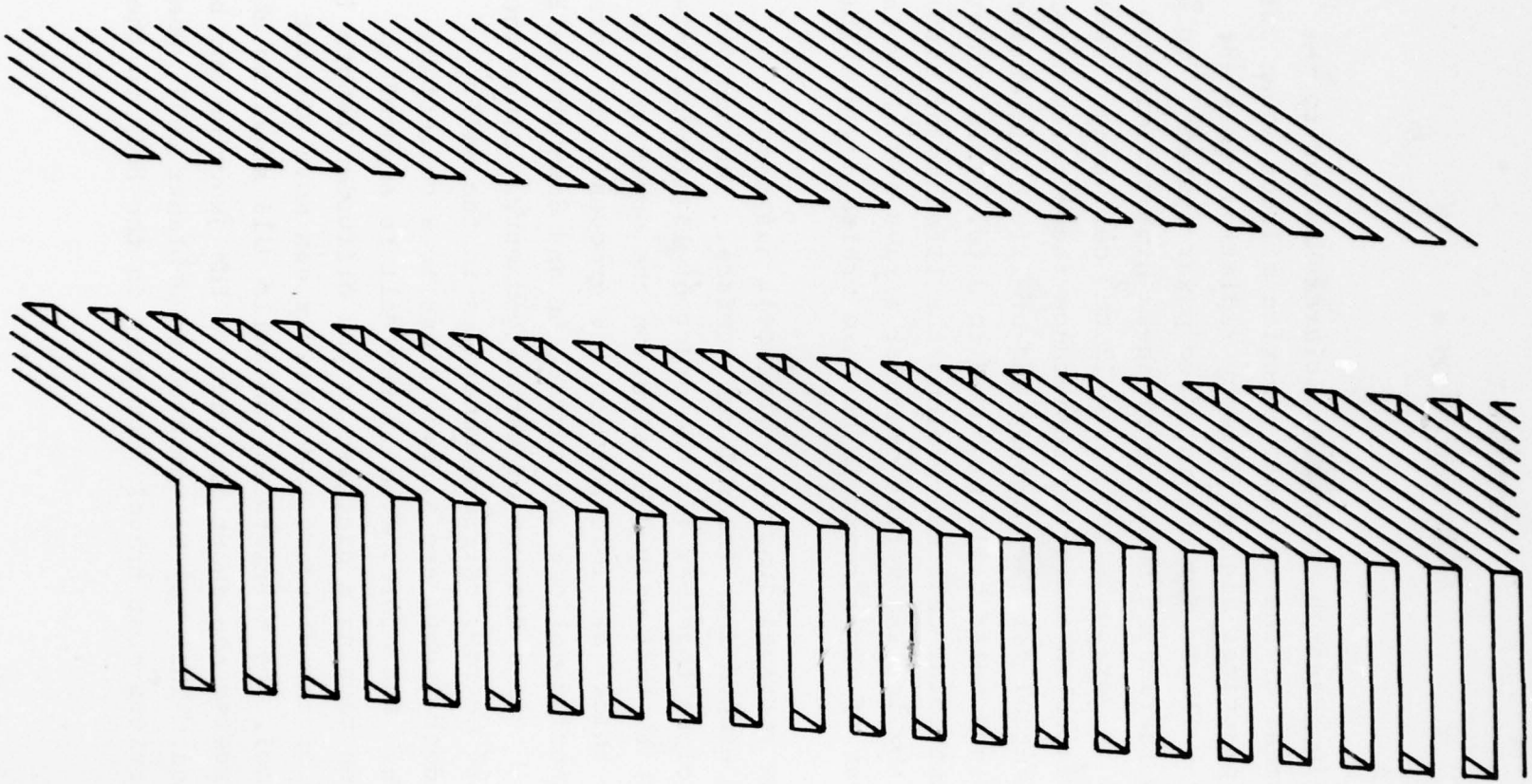


Figure 1. Structure of VJ Cell

junction so that a decrease in the diffusion length (because of radiation) will result in a decrease in collected carriers and therefore in cell efficiency. The vertical junction cell will display less degradation due to irradiation than planar silicon solar cells.

Vertical junction solar cells were initially proposed by J.F. Wise (Ref. 1) to alleviate the degradation of solar cells in space due to radiation damage. Theoretical analysis of the vertical junction cell by Rahilly (Ref. 2), Stella and Gover (Ref. 3), and Chadda and Wolf (Ref. 4) predicted that the vertical junction solar cell theoretically can be a high efficiency radiation resistant cell. Because of the inherent advantage of the vertical junction geometry, experimental attempts at fabrication were begun by Smeltzer, et al (Ref. 5), and Lloyd et al (Ref. 6 and Ref. 7) under contract to AFAPL. This initial experimental program resulted in the fabrication of vertical junction cells with some indications of improved radiation resistance. However, the efficiencies of these cells were very low and therefore not a valid indicator of the potential of vertical junction cells.

This research program at the Solarex Corporation has resulted in the fabrication of vertical junction solar cells with dramatically higher efficiencies. For 2 x 2 cm , 2 x 4cm and 2 x 6cm vertical junction solar cells, efficiencies of greater than 14% AM0 have been obtained. As expected, the radiation resistance of these cells is far superior to planar cells. With these cells it is now possible to design space missions where high level radiation exposure is expected. Also, with these cells the size of the solar array can be reduced and still retain an adequate end-of-life-power performance.

The processes developed to fabricate vertical junction solar cells are described in Section II. The processes are compatible with scaling up of the fabrication to produce larger quantities of cells. The fabrication is, of course, more involved than the fabrication of a planar cell. However, the masking and orientation dependent etch are batch processes so that the additional processing involved is only marginally more than for ordinary pyramided cells.

Section III is a review of a theoretical analysis of the vertical junction solar cell. The purpose of this study was to determine the current generated in this cell and to evaluate the radiation degradation. The theoretical calculations can help us choose geometries that will optimize the efficiency and radiation resistance. It is especially useful for indicating the parameters that have the most influence on cell performance.

The experimental results are given in Section IV. Various characteristics of vertical junction cells are given including:

- efficiency
- I-V curves
- open-circuit voltage
- short circuit current
- fill factor
- optical absorption and emission
- dark I-V
- V_{oc} vs I_{sc}
- spectral response and Quantum yield
- thermal cycling
- capacitance
- temperature coefficients
- radiation testing
- production yields

The final section summarizes the advancements made in vertical junction solar cells technology to date. There is also a discussion of suggestions for future work required to:

- increase the efficiency
- improve the radiation resistance
- simplify the fabrication process
- lower the cell cost

SECTION II

EXPERIMENTAL PROCEDURE

The fabrication of vertical junction solar cells requires the formation of deep grooves into the surface of the silicon wafer. This process should be performed economically and with a minimum of structural damage to the silicon substrate. The process which has made manufacture of the vertical junction cells feasible is the orientation dependent etch. Kendall (8) found that the etch rate of silicon in KOH varies up to a factor of 400 depending upon crystal orientation. The 111 plane of silicon is more resistant to the etch than the other crystal planes. Therefore if the silicon can be properly aligned and masked before etching, the required deep grooves can be etched.

All of the processing procedures must be compatible with the fabrication of high efficiency solar cells. This means that no processes can be employed that would require placing the silicon in an environment with a temperature greater than 900°C for an extended time period. In addition these processes should be readily adaptable to larger scale production with adequate yields and reasonable cost. Only processes that meet these criteria have been employed. Particular emphasis has been placed on improving the processing techniques to reduce the time and cost involved in the fabrication of vertical junction cells.

1. Silicon Material

During the orientation dependent etch, the 111 plane etches at a much slower rate than the other silicon planes. Therefore, the silicon wafer should have 111 planes normal to the surface so that deep grooves can be etched leaving vertical 111 walls. The surface of the proper silicon wafers for this application are oriented on the 110 plane. While 110 silicon ingots can be grown, they cannot be obtained dislocation free. The most convenient source of dislocation free 110 wafers is from 111 ingots aligned and cut perpendicular to the 111 axis leaving 110 wafers. To facilitate alignment of the etching mask to the 111 planes, the 110 slices are x-ray oriented and a flat cut on the 111 plane.

Since fine line photolithography is performed on the silicon wafers, the surface must be smooth. All of the silicon used to date has been chem-mech polished with cupric nitrate solution as developed by Mendel and Yang (Ref. 9). To facilitate the p^+ formation both sides of the wafers have been polished.

2. Wafer Cleaning

Before processing begins, it is extremely important that any impurities or surface contamination be removed. For this purpose the wafers have been:

- Cleaned in peroxide glass cleaner (66% H_2SO_4/ 33% H_2O_2)
- Soaked in HCl
- Etched in HF

This process should remove all organic, metallic and oxide contaminants from the surface.

3. Oxide Growth for Masking the Etch

Etching grooves into the silicon requires an effective alkaline etchant mask. This mask must be able to withstand the etching solution for enough time so that the required groove depths can be etched. In addition, the formation of the etchant mask must not result in degradation of the silicon in any way. Two successful techniques have been employed for forming the etchant mask. The first method involves growing a phosphosilicate glass on the surface by means of a short phosphorous diffusion followed by the growth of oxide in steam all at a temperature below 860°C. The second method entails the deposition of silicon oxide by performing Chemical Vapor Deposition (CVD) of silicon by pyrolysis of silane. The "fake-diffusion" technique is a batch process amenable to large scale production, but has the disadvantage of requiring a short phosphorous diffusion which creates a P-N junction which must be removed before cell fabrication. The silane technique does not dope the silicon but is a more expensive and time consuming process. At present the "fake-diffusion" process is being employed for most cell fabrication and is highly successful as long as care is taken to remove the surface layer before cell fabrication, so that any possible surface damage is removed.

4. Orientation and Placement of the Groove Pattern

Standard photolithography techniques are employed to place the pattern on the silicon. Fine lines (as narrow as 2.5 microns) must be repeatedly placed across the whole surface. Because of this fine geometry, care must be taken to have a clean silicon oxide surface and to remove any lumps and aggregates from the photoresist itself. To improve the adhesion of the photoresist to the oxide, Hexamethyldisilozane (HMDS) has been employed. It serves as an adhesion

promoter, eliminating those sites on the oxide surface that repel photoresist when applied to untreated oxide surfaces. The benefits of using HMDS are fewer rejects due to poor photoresist adhesion and less undercutting.

The photolithography pattern must be aligned very accurately to the 111 plane so the etch will produce deep, narrow grooves. Originally, a fan pattern with fingers separated by 0.2° was aligned to the x-ray oriented flat. The fan pattern was orientationally dependent etched to determine the optimal alignment to the 111 plane. The photo-mask groove pattern was then optically aligned to the narrowest etched groove in the fan pattern. While the method works, it requires two orientation dependent etches and either a very thick original oxide or the growth of two oxides to withstand the two orientation dependent etches that are performed. This technique also required a great deal of time analyzing the etch fan pattern and then aligning the mask grooves to the chosen fan pattern line.

To simplify the procedure, the mask was optically aligned directly to the x-ray oriented flat. It was found that this process resulted in an orientation dependent etch indistinguishable from that obtained from the fan pattern alignment. Therefore, to save process time and cost, the initial orientational dependent fan pattern etch was eliminated from the procedure.

Finally, the masks have had flat stops optically aligned to the groove pattern. The stop is permanently mounted to the mask itself. Then the flat on the cell is mechanically placed against the flat on the mask and the cell exposured. This pattern is aligned as well as those aligned by the previous two techniques and the orientation dependent etch proceeds as before.

5. Oxide Etch

The photoresist on the surface now acts as a mask for the oxide etch. The etchant is $6NH_4F$:1 HF. The etchant does not attack the photoresist or the silicon but does remove all of the oxide. Several minutes of etching removes the oxide from the windows with a minimum of undercutting.

6. Orientation Dependent Etch

The orientational dependent etch of silicon in KOH has been studied in detail by Kendall (Ref. 8). Etch rate differences of 400 to 1 have been obtained. While the largest rate difference would lead to the deepest groove depths at the same width, there are other considerations in choosing a particular etchant. Since the oxide does slowly dissolve in KOH solution, it is necessary to use an etchant that does not etch away the oxide mask before reaching the required groove depth. It would also be desirable to have an etchant that does not require an excessive amount of time to form the grooves.

The etchant found to satisfy best these criteria is 30% KOH in H_2O at 70° to 75°C. With this etchant, grooves up to 4 mils deep can be etched within one hour. Typically, grooves with an initial width of 5 microns result in final grooves 7 to 8 microns wide, while those with an initial width of 2.5 microns result in final grooves at least 5 microns wide. The walls are extremely straight and parallel as well as exhibiting uniform depth. Figure 2 is a Scanning Electron Microscope (SEM) picture at 500X of the broken edge of a vertical junction wafer, exhibiting this uniformity of grooves and walls. Figure 3 is an SEM picture at a magnification of 250 of a vertical junction

Figure 2. An SEM Picture at 500x of a Vertical Junction Cell Broken Perpendicular to the Grooves

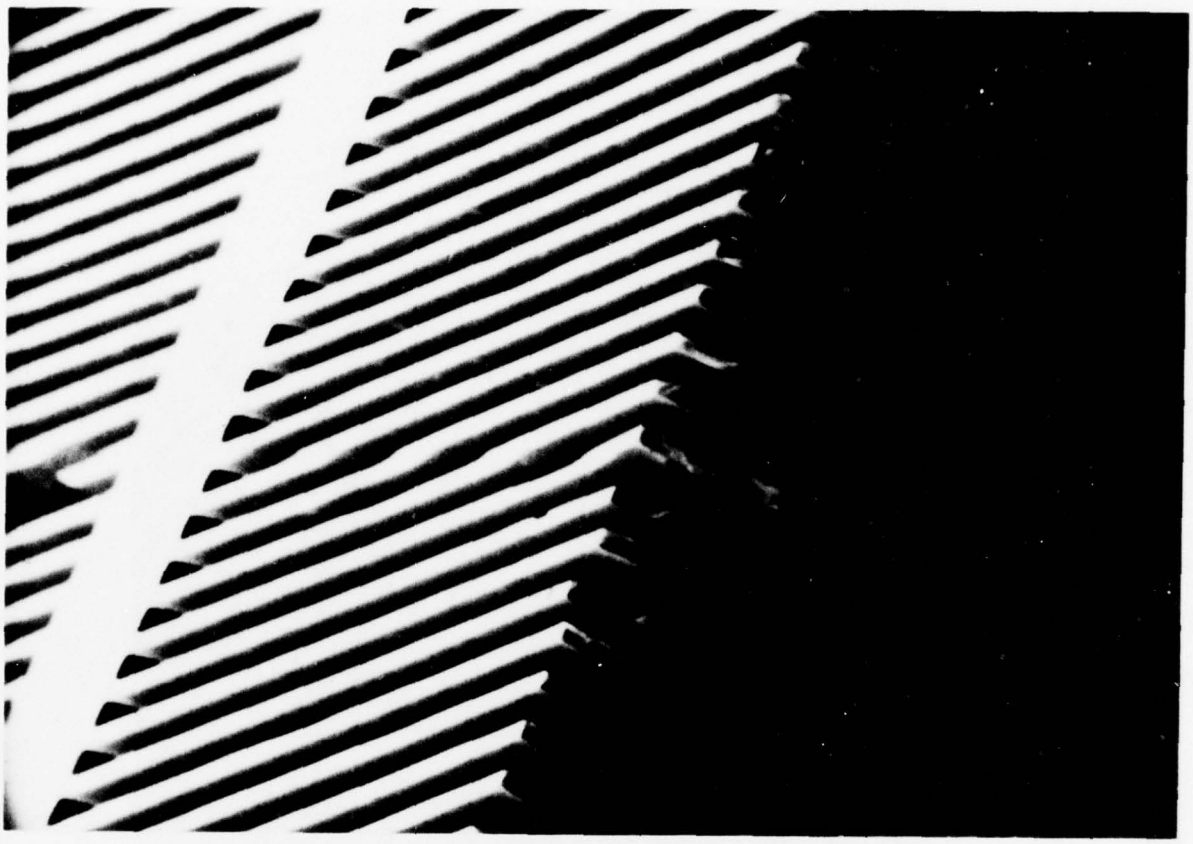


Figure 3. Scanning Electron Microscope Picture at a Magnification of 250 of a Vertical Junction Solar Cell Broken Perpendicular to the Grooves

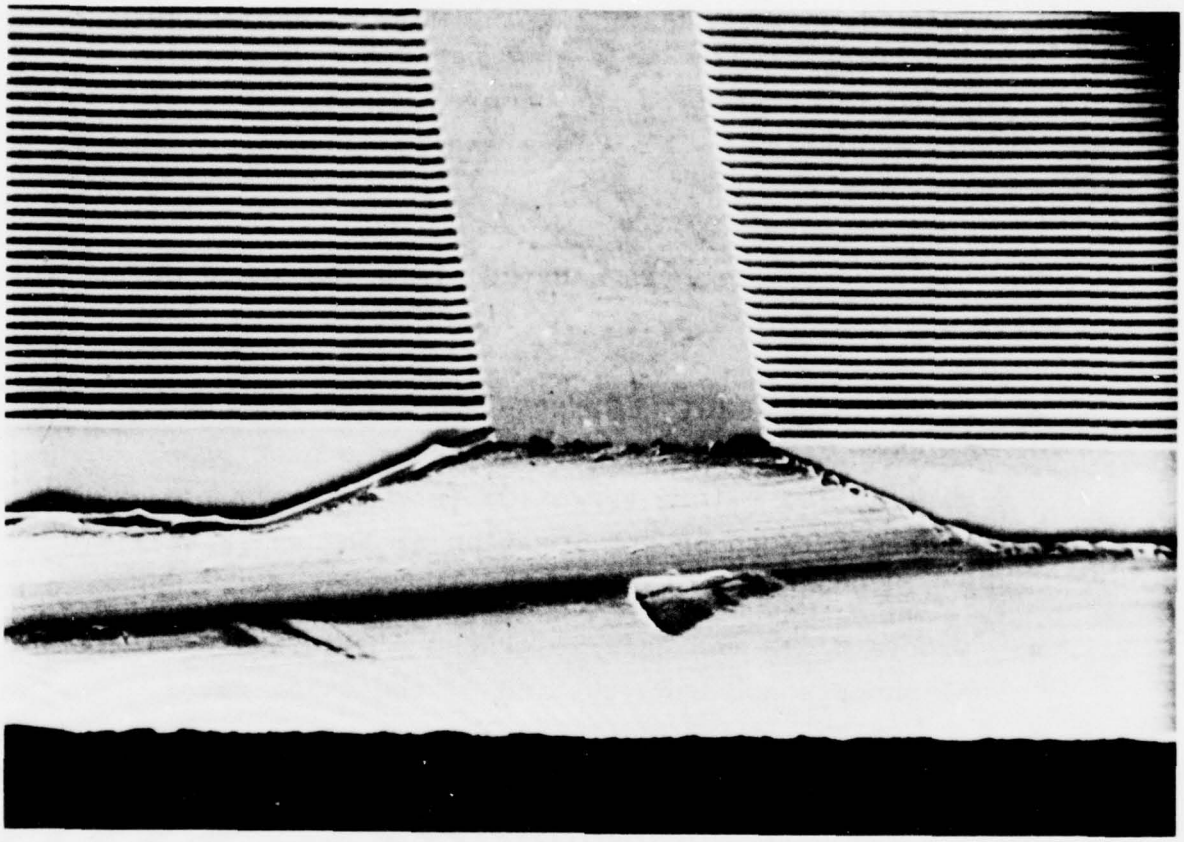


Figure 4. An SEM Picture at 100x Looking Perpendicular to the Groove Along the Edge of a Broken Buss Bar

solar cell broken perpendicular to the groove. The flat portion near the top of the picture shows one of the ribs which are not etched in order to insure structural strength and which are metallized to carry the current to the collection pads. This region is typically 8 mils wide but ribs are narrow as 1 mil have been employed without resulting in excess breakage. Figure 4 is an SEM picture at 100X looking perpendicular to a buss bar rib. The gradual slope from the rib down into the groove is determined by the presence of another (111) plane and provides strength to the cells even for 1 mil wide ribs.

The depth of the grooves and the width and shape of the walls are determined by:

- Oxide Thickness - The oxide thickness must be monitored throughout the ODE and the etch process halted before the oxide is completely etched through in any location or the walls will rapidly be etched away.
- Groove Width and Wall Thickness - Slight misalignments and undercutting of the oxide cause the walls to slowly etch away. The wall thickness must also be monitored during the ODE and the etch halted when the appropriate relationship between wall thickness and groove depth is obtained. Thinner walls can be used for solar cell processing but they are more fragile and do not provide as much radiation resistance as obtainable from wider walls.
- Groove Depth - The optimum groove depth depends upon a trade-off between increased radiation resistance and lower open-circuit voltage for deeper grooves. Practically the desired groove depth can only be obtained when the oxide is sufficiently

thick and etch resistant to withstand the required ODE and the alignment is good enough so that the walls are not etched too thin for practical cell fabrication.

7. Oxide Removal and Shaping Etch

After the orientation dependent etch, the remainder of the oxide is removed by an etch in 5:1 mixture of H_2O and 49% HF for 15 minutes. The etch removes the oxide without affecting the silicon.

During the oxide growth, phosphorous was diffused into the silicon. Some phosphorous still remains in the top of the walls. Also to maximize the light absorption by the cell, it would be advantageous to shape the tops of the walls. Therefore, an isotropic etch must be performed to remove the phosphorous and to shape the wall tops. Both alkaline and acid etches have been used for this purpose. The alkaline etches tend to produce very pointed and jagged walls with many crystal planes exposed. While this type of wall does aid in total optical absorption, it results in very fragile walls and because of the many crystal planes exposed can lead to deterioration of the fill factor. The acid etch used is a 1:3:8 (by volume) mixture of 49% HF, 70% HNO_3 and 98% CH_3COOH. A long etch (minutes) in this acid will also produce pointed tops. However, a short etch (15 seconds) results in rounded walls, which are both strong and nearly non-reflecting. This type of etch has been employed on most of the cells and results in a satisfactory geometry.

8. Cell Fabrication Processing

The silicon wafers that have been orientation dependent etched are fabricated into solar cells by refined processes that are similar to those employed in the fabrication of planar cells. The presence of multiple crystal planes as well as the need to diffuse down narrow grooves are special features of the vertical junction cell. Neither has proved to be much of a problem (except where low resistivity silicon is employed).

The phosphorous diffusion has been performed using phosphine gas as the dopant source. While diffusion temperatures from 840°C to 913°C have been employed (see Ref. 10), most of the cells have been fabricated using a diffusion temperature of 860 to 870°C for from 12 to 16 minutes. The gas flow rates have been maximized for the vertical junction cell, but in reality the entire diffusion procedure is quite similar to that employed for the fabrication of some planar cells.

The P+ back junction has been fabricated using vacuum deposited aluminum. The P+ formation technique being employed for the majority of cells involves an alloy at 860 to 870°C for from 15 to 20 minutes. This process appears to give the best enhancement in voltage and red response.

The back metallization is formed by vacuum evaporated Ti-Pd, covered with Ag. This is the metallization employed on many of Solarex's cells and can withstand humidity and thermal cycling tests and can be either soldered or welded to.

The front metallization is also vacuum evaporated Ti-Pd, covered with Ag. This metallization is applied by shadow

masking. The majority of cells were fabricated using standard commercially available bi-metallic shadow masks. The mask opening is optically aligned to the cell ridge and clamped in place. We have experimented both with photolithography and mechanically aligned shadow masks. Because of the step walls, liquid photoresist is extremely difficult to use while the problems associated with pressing dry film photoresist over the walls and etching out narrow (2 to 4 mil) lines have not been completely solved. Some cells were fabricated using silicon shadow masks with mechanical alignment. This technique promises a significant reduction in process time and in mask cost, however it still requires improvement in the alignment design before being employed for large scale fabrication.

The anti-reflective coating used on the cells is Ta_2O_5 vacuum deposited by election beam. It is a quarter wavelength film deposited perpendicular to the wafer surface as for a planar cell. Attempts have been made to evaporate the AR coating at various tilt angles to improve the AR coating on the walls, but these methods have resulted in less satisfactory results than obtained by a perpendicular evaporation.

9. Cover Slides

Ceria doped glass cover slides have been employed for all cover sliding experiments. The conventional Dow Corning silicone adhesives have been employed with attention paid to outgassing of the channels through the liquid before cover attachment. This type of cover attachement has produced effective mechanical adhesion and such covered cells have successfully passed humidity testing and been employed

for radiation testing. However, this cover sliding system does not pass thermal cycling tests. Section IV contains a discussion of the thermal cycling results and recommendations for future work on cover sliding of vertical junction cells.

10. Cell Geometry

Three different initial wall-groove dimensions have been employed for vertical junction cells. These three geometries are:

1) 50 micron grooves and 50 micron walls. This was the initial pattern employed to develop the etch and cell fabrication technology and did not produce fine enough walls to enhance radiation resistance.

2) 5 microns grooves and 10 micron walls. This pattern was used for most of the cell fabrication It typically resulted in etched grooves 7 or 8 microns wide with 7 to 8 micron thick walls.

3) 2.5 micron grooves and 10 micron walls. This pattern was used mainly to show that narrower openings could be etched and narrower grooves diffused adquately. This pattern resulted in etched grooves from 5 to 7 microns wide with walls 5 to 7 microns thick. It was shown that such narrow initial groove openings can be used, so that future work can use cells with a larger wall to groove ratio without changing the final wall width.

While several overall cell geometries have been employed, the geometry of 2cm x 2cm cell shown in Figure 5 has been used for most cell fabrication and for all 2cm x 2cm cells delivered as part of the contract requirements. The 2cm x 2cm pattern has 7 ridges 8 mils wide that are metallized with 4 to 6 mils of Ti-Pd-Ag. The metallization pads are 80 mils by 40 mils. The 2cm x 4cm pattern shown in Figure 6 has 12 ridges for metallization and 4 pads for interconnection The 2cm x 6cm pattern shown in Figure 7 has 19 ridges for metallization and 6 pads for interconnection. The grooves are initially 122 mils long and 5 microns wide, while the walls are initially 10 microns wide.

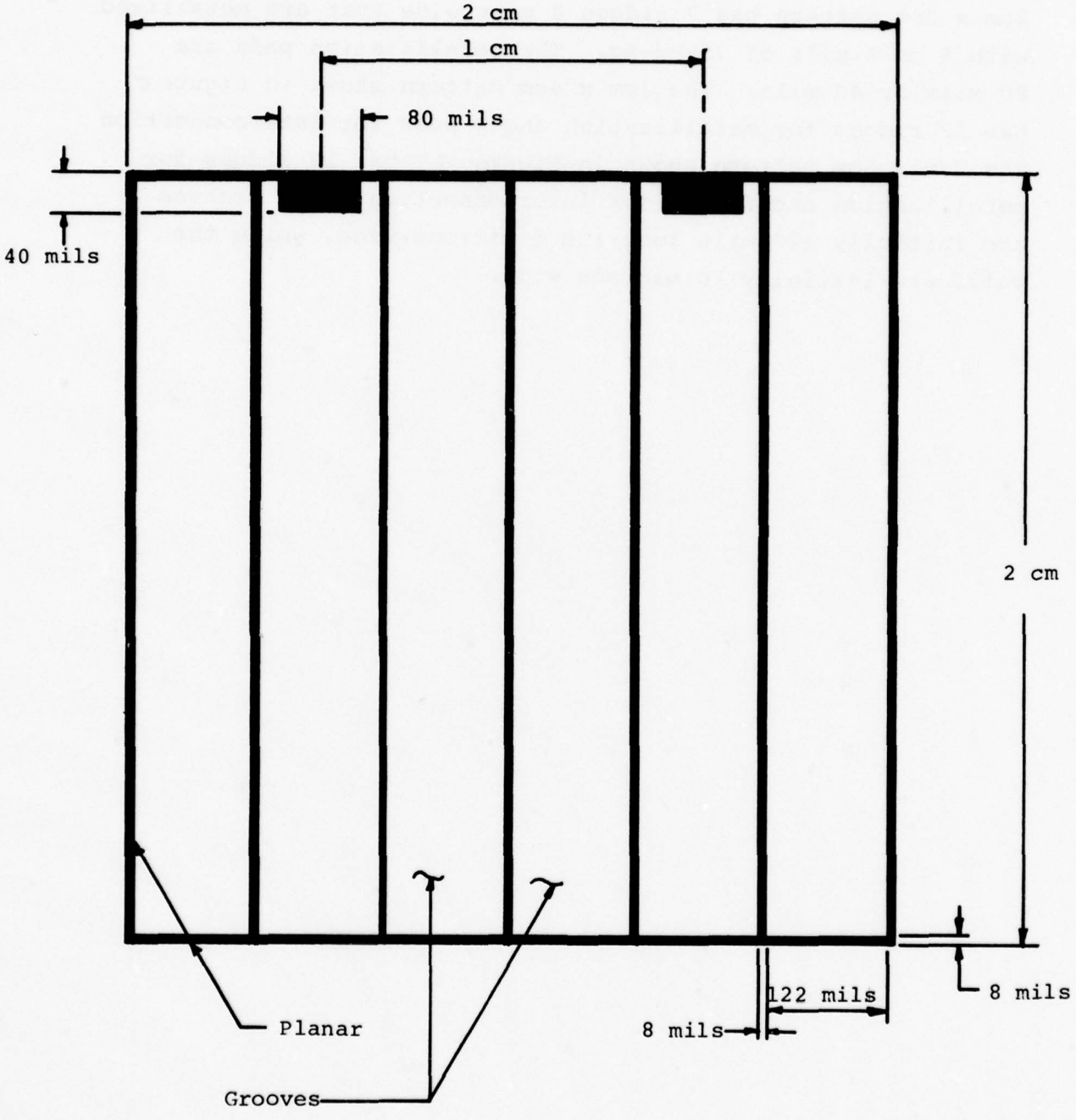


Figure 5. Diagram of 2cm x 2cm Cell Geometry

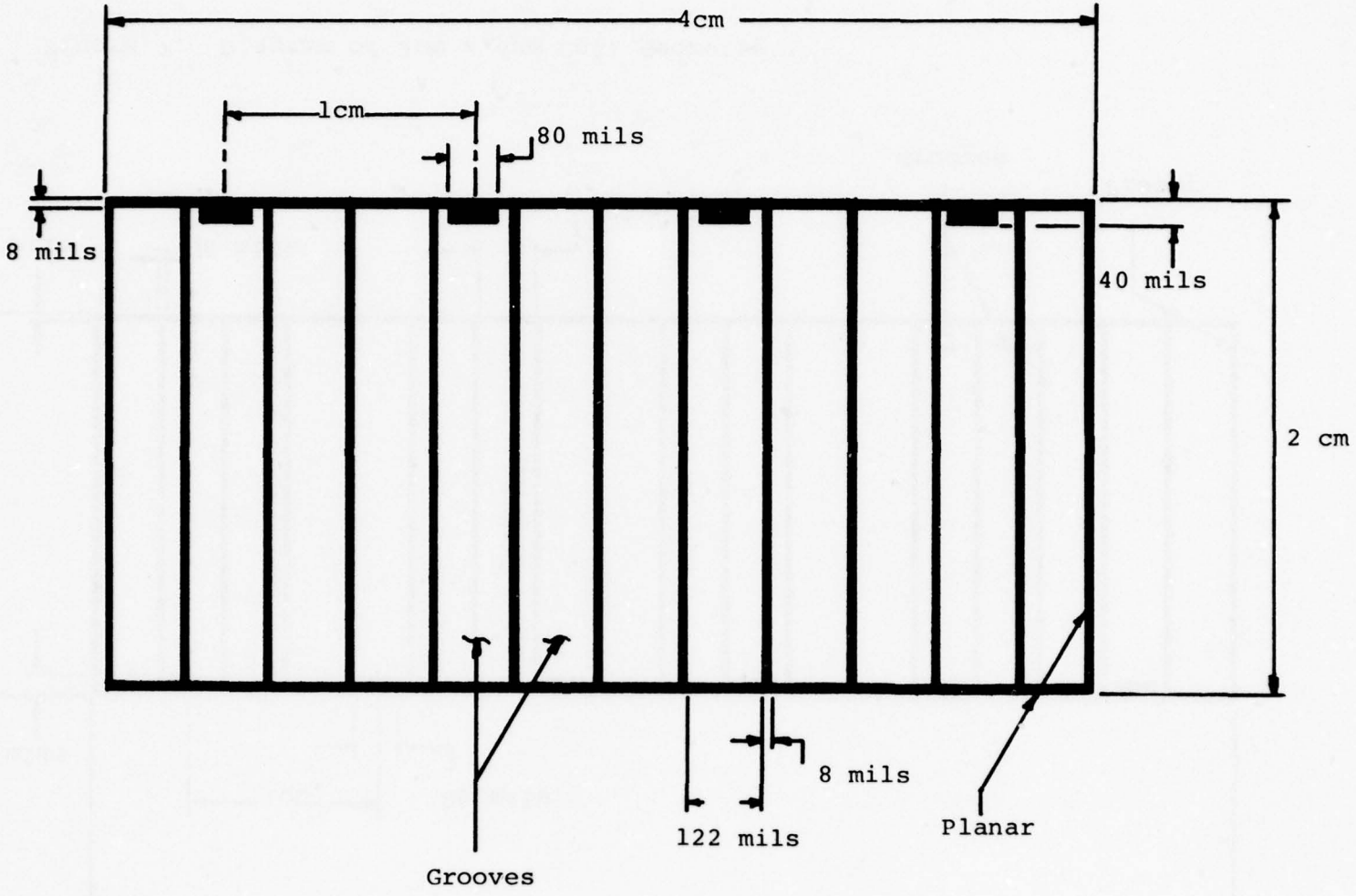


Figure 6. Diagram of 2cm x 4cm Cell Geometry.

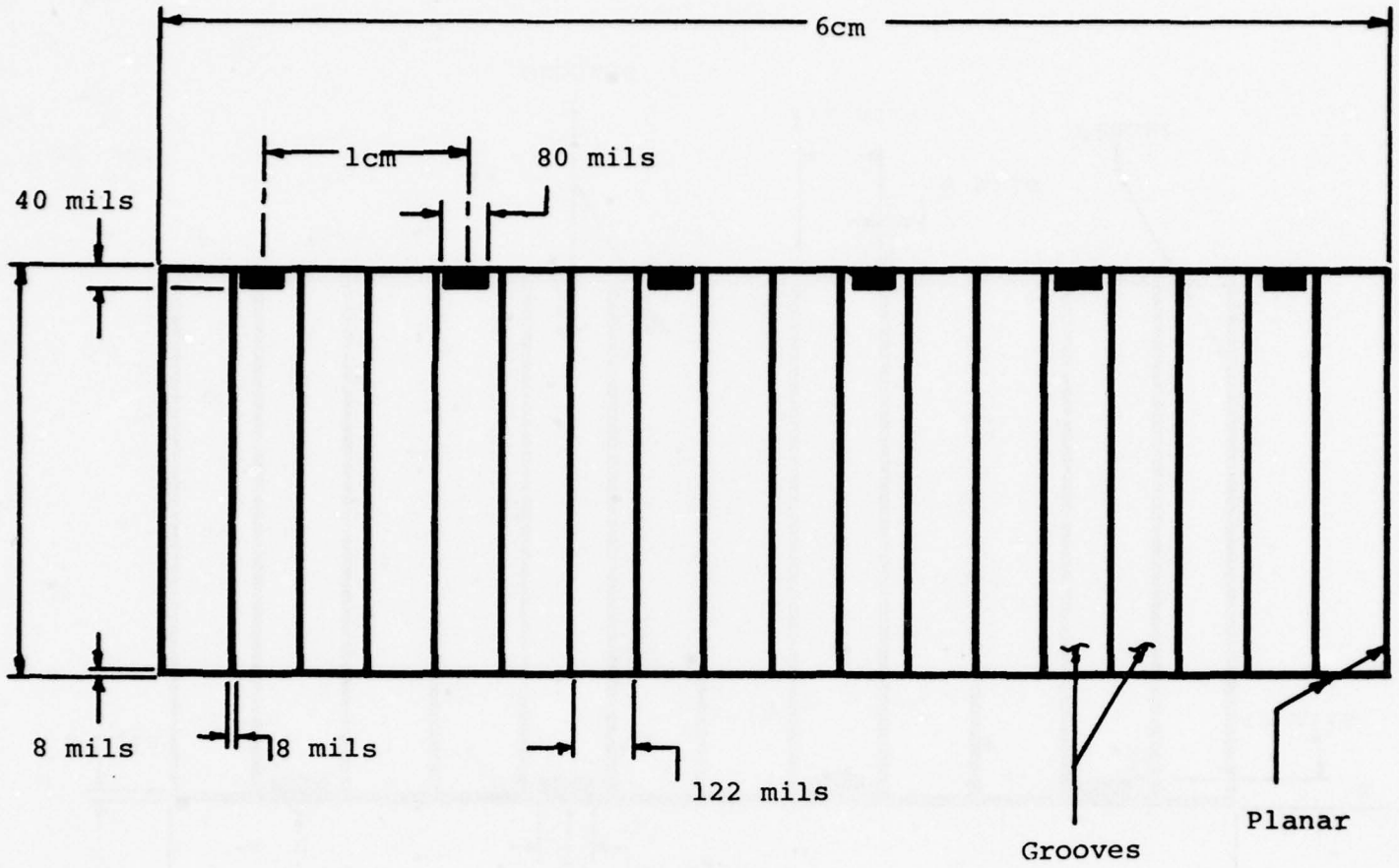


Figure 7. Diagram of 2cm x 6cm Cell Geometry

SECTION III

THEORETICAL ANALYSIS

The vertical junction solar cell is expected to exhibit

- improved radiation resistance due to carriers generated in the walls.
- lower open-circuit voltage due to increased surface area.

Because the deeper grooves result in an increase in the radiation resistance and a decrease in the open-circuit voltage, the final cell design must be a compromise between the two effects. A detailed theoretical analysis of the VJ structure appeared in the first yearly report (10). This was a study of the carrier current collection and radiation resistance for a particular VJ structure and predicted the type of improved radiation resistance obtained for VJ cells.

1. Effect of Irradiation on Current

Using published absorption coefficient data from Dash and Newman (11) and Phillip and Ehrenreich (12) and the photon flux data from Thekaekara (13) a table of photon absorption versus depth can be generated. Equating the silicon depth to wall height results in Table 1.

TABLE 1

PERCENT OF PHOTONS ABSORBED IN WALL

Height of Wall (microns)	Percent of Photons Absorbed in Wall
5	55%
10	69%
20	78%
50	86%
75	89%
100	91%
200	95%

Using this data the current degradation as a function of radiation fluence can be calculated (See reference 11 for the details of this calculation). The results for various groove depths are shown in Figure 8. As expected the radiation resistance improves as the groove depth increases, but the magnitude of the change from say 50 to 100 microns is small compared to improvement in radiation resistance in going from planar to 50 micron deep grooves.

2. Voltage Performance of Vertical Junction Cell

In the simplest model the diode equation results in the expression

$$V_{oc} = \frac{kT}{q} \ln (I_{sc}/I_o) \qquad (1)$$

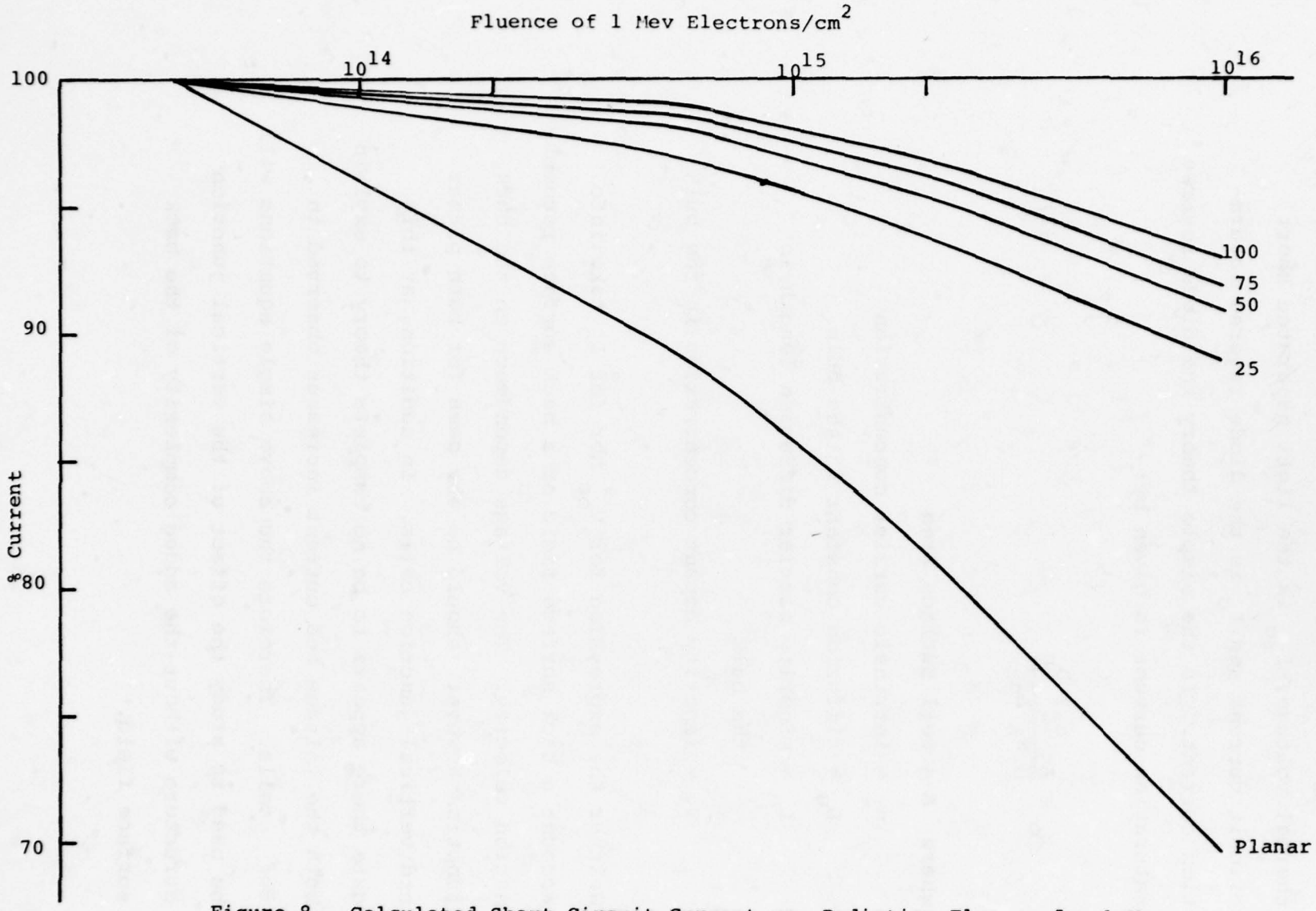


Figure 8. Calculated Short Circuit Current vs. Radiation Fluence for 1 Mev Electrons for Various Cell Geometries.

where V_{oc} is the open-circuit voltage, kT/q is the thermal voltage, I_{sc} is the light generated short circuit current and I_o is the diode reverse saturation current. In the simple theory the diode reverse saturation current is given by:

$$I_o = \frac{Aq\, n_i^2\, D_n}{N_A\, L_n} \qquad (2)$$

where A = cell surface area

n_i = intrinsic carrier concentration

D_n = diffusion constant in the bulk

L_n = minority carrier diffusion length in the bulk

N_A = impurity dopant concentration in the bulk

Neither the expression for V_{oc} nor for I_o take into account a back surface field or a back surface recombination velocity. The voltage dependence on the back junction however should be the same for both planar and vertical junction cells. In addition, at this date there appears to be no complete theory to explain both the voltage and current increases observed in BSF cells. Therefore the above simple equations will be used to study the effect of the vertical junction structure without the added complexity of the back surface field.

The following values have been used for 2Ω-cm p-type silicon solar cells.

I_{sc} = 160 mA

D_n = 34 $cm^2/sec.$

L_n = 250 microns

$N_A = 7.5 \cdot 10^{15}/cm^3$

$n_i^2 = 2.2 \cdot 10^{20}/cm^6$

$\frac{kT}{q}$ = 0.026 mV at 25°C

Using these values the V_{oc} can be calculated with a resultant value of 588 mV. This agrees well with experimental results for 2Ω-cm cells without a very good back surface field.

The grooved surface of the vertical junction cells has a much larger surface area than a planar cell. Column 2 of Table 2 lists the surface area for various groove depths assuming the standard Solarex pattern (15 microns from center to center - equal wall and groove width). Under the assumption that the reverse saturation current increases proportional to the increase in surface area the open-circuit voltage will decrease appreciably with groove depth. Table 2 tabulates the results using equations (2) and (1) to calculate I_o and then V_{oc}

respectively. The silicon parameters are identical to those used for the calculation of the planar V_{oc} with the exception of using an I_{sc} of 170 mA for the VJ cell, which is a typical current obtained for such cells.

TABLE 2

OPEN CIRCUIT VOLTAGE AS A FUNCTION OF GROOVE DEPTH

USING SIMPLE AREA SCALING

Depth of Grooves (microns)	Surface Area (cm^2)	$\frac{A}{A\ (Planar)}$	I_o (amp. 10^{-11})	V_{oc} (mV)
Planar	4	1	2.56	588
5	6.44	1.61	4.12	576
10	8.87	2.22	5.68	567
20	13.7	3.43	8.78	556
50	28.3	7.08	18.12	537
75	40.45	10.11	25.88	528
100	52.61	13.15	33.66	521

Comparing these values to the experimental results given in Section 4.1, shows that the theory predicts a much lower voltage than is obtained experimentally.

It now appears that this simplified theory has over-estimated the diode reverse saturation current in the walls. Planar junction injects the saturation current into a thick bulk region (250 microns or so) where

most of the carriers recombine. However, in the walls the injected current must only transverse the thin wall (5 to 10 microns) before the carriers re-enter the opposite n-region. Figure 9 is a sketch of the different injection geometries. Therefore, all of the carriers injected from the wall cannot be counted in the reverse saturation current. Only the fraction that recombine in the wall p-region will contribute to the actual reverse saturation current.

Considering an n-region injecting electrons into the p-region with an infinite sink for electrons (namely the other n-region) on the other side of the p-region, the density of electrons is given by:

$$N_p(X) = N_p(o)\ \exp(-X/L_n) \qquad (3)$$

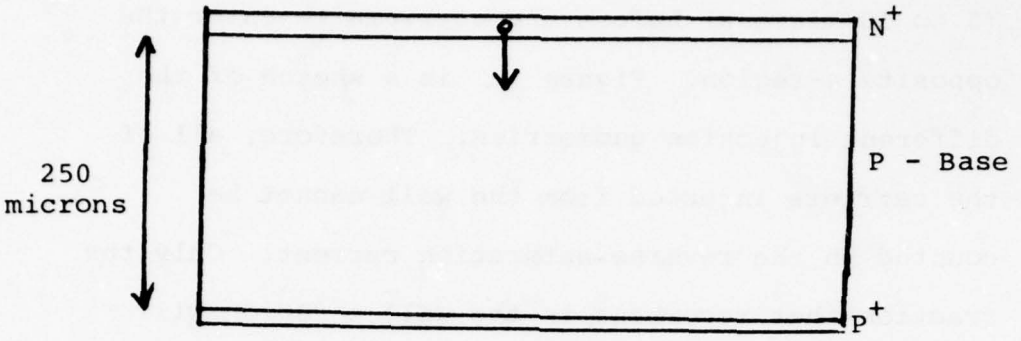
where $N_p(X)$ = number of minority electrons in p-region at a distance X from the junction.

$N_p(o)$ = number of minority electrons injected into the p-region.

X = Distance from the injecting junction.

L_n = Diffusion length of the electrons in the p-region.

If we assume that the distance the electrons travel is equal to one wall width (approximately 7 microns) then



a. Planar

b. Vertical Junction

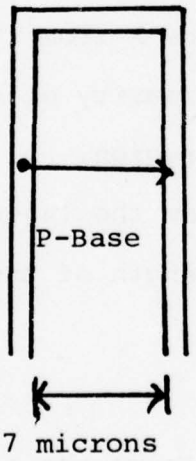


Figure 9. Injection Geometries

97.2% of the electrons will traverse the wall and re-enter the n-region. Therefore, only 2.8% of the thermally generated current in the walls will contribute to the total cell reverse saturation current. The total cell reverse saturation current can then be written

$$I_{o(Cell)} = I_{o(Planar\ Area)} + 0.028\ I_{o(Walls)} \quad (4)$$

The $I_{o(Planar\ Area)}$ will be identical to that obtained for the planar cell, since the total horizontal cell area has remained constant. Table 3 is a tabulation of the calculated reverse saturation currents and the expected open-circuit voltages for various groove depths using equation (4).

TABLE 3

OPEN-CIRCUIT VOLTAGE AS A FUNCTION OF GROOVE DEPTH INCLUDING THE EFFECT OF CARRIERS TRAVERSING THE WALLS

Depth of Grooves (microns)	I_o (amp · 10^{-11})	V_{oc} (mV)
Planar	2.56	588
5	2.6	588
10	2.65	587
20	2.73	586
50	3.00	584
75	3.21	582
100	3.43	580

These values for V_{oc} show better agreement with the experimental values as shown in Section 4.1.

3. Conclusions

These calculations show that the VJ cell should have significantly improved radiation resistance. In addition, the VJ cell should be capable of exhibiting open-circuit voltages only a few millivolts below those of similar planar cells, while producing currents well in excess of those produced by planar cells (due to increased light absorption). While further calculations are required before one can predict the actual output and radiation resistance of a particular geometry, our present calculations do indicate the basic parameters of the vertical junction cell and enable us to predict the approximate open-circuit voltage and radiation tolerance of various geometries.

SECTION IV

EXPERIMENTAL RESULTS

1. Cell Characteristics

Vertical junction cells with efficiencies in excess of 14.5% AM0 25°C have been obtained. The cell had approximately 75 micron deep grooves with equal (7-8 micron) wall and groove widths. (Cells with extremely narrow walls 1 to 2 microns wide have been fabricated but the output power is lower and the radiation resistance is worse than the standard 1:1 wall to groove ratio cells. Figure 10 is an I-V curve of one of the best 2cm x 2cm vertical junction cells. The three curves are AM0, AM0 with a red Corning #2408 filter and AM0 with a blue Corning #9788 filter at 25°C on 2Ω-cm CZ silicon. Table 4 summarizes the state of the art achievements to date on 2cm x 2cm, 2cm x 4cm and 2cm x 6cm vertical junction solar cells. As can be seen there is no degradation of performance with increasing cell size. Indeed, the larger cells showed somewhat better performance. This was attributed to both fabricating experience and better tolerance on the large area etching masks.

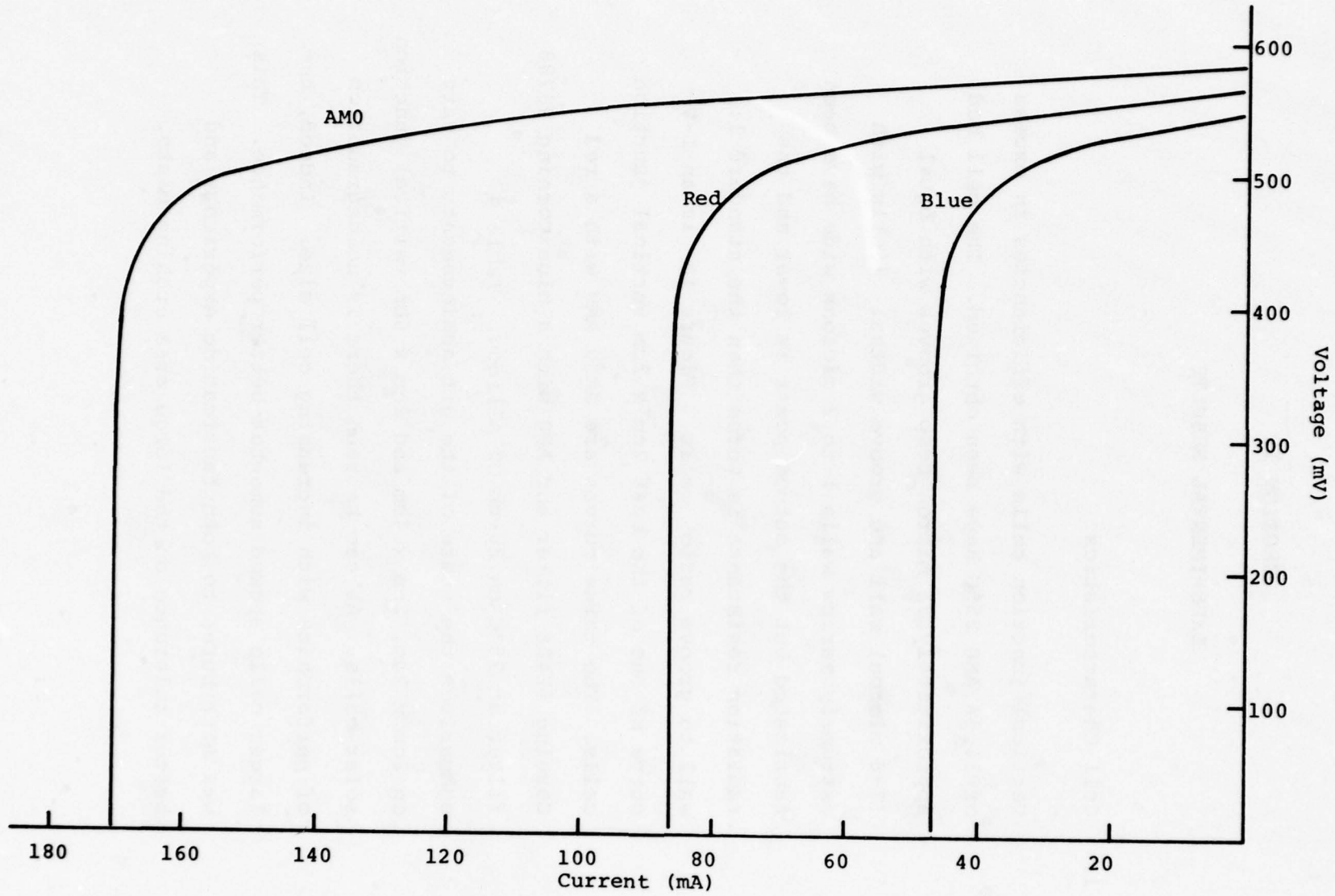


Figure 10. I-V Characteristics at AM0 for a Vertical Junction 2cm x 2cm Solar Cell

TABLE 4

STATE OF THE ART VALUES FOR VERTICAL JUNCTION SOLAR CELL

SIZE	MAX POWER (mW)	Eff. (%)	V_{oc} (mV)	I_{scr} (mA)	I_{scr} (1) (mA)	I_{scr} (2) (mA)
2 x 2	76	14.0	575	170	88	52
2 x 4	150	14.0	572	324	180	104
2 x 6	235	14.5	578	528	274	160

The Max Power, Eff., V_{oc} and I_{sc} measured at AM0, 25°C

1) Red Filter is a Corning #2408 filter

2) Blue Filter is Corning #9788 filter

All measurement for 75 micron deep grooves, 15 microns from center of wall to center of wall, equal wall and groove width, 2 Ω-cm silicon.

The vertical junction structure has excellent optical absorption properties (see Section 4.3). Because of the enhanced absorption the current collection in the vertical junction cell is improved over planar cells and can be as efficient as any surface texturing technique. The best short circuit current for a VJ cell of 44 mA/cm^2 is very close to the best value ever obtained for any silicon solar cell.

The open-circuit voltage for VJ cells is a function of groove depth. Table 5 summarizes the results for various groove depths for the standard geometry VJ cells measured at AM0 and 25°C. These values agree quite well with those calculated in Section 3. The value at 100 microns is probably lower than that which can be achieved, since this value only represents one sample lot in which the bulk below the grooves was very thin (≈50 microns). From these results it can be seen that not much open-circuit voltage need be sacrificed in using the VJ structure.

Because of the large surface area of the VJ cell, the sheet resistance of this cell type is negligible. Therefore, the VJ cell may have its current carrying bus bars spaced further apart without encountering

series resistance problems. Indeed, the VJ cells exhibit very high fill factors, typically above 0.78 with some in excess of 0.80.

TABLE 5

TYPICAL OPEN-CIRCUIT VOLTAGE AS A FUNCTION OF GROOVE DEPTH FOR 2 Ω-CM VERTICAL JUNCTION CELLS

Groove Depth (microns)	Open-Circuit Voltage At 25°C (mVolts)
25	585
50	580
75	575
100	540

2. *Diode Characteristics*

The characteristics of the junction can be studied by plotting I_{sc} vs. V_{oc}. One such example is shown in Figure 11. This cell has an exponential current-voltage relationship with an n factor of 1.1. This is fairly typical of VJ and planar cells with n's between 1.0 and 1.5 being observed. The low voltage regime is quite well behaved indicating a high shunt resistance.

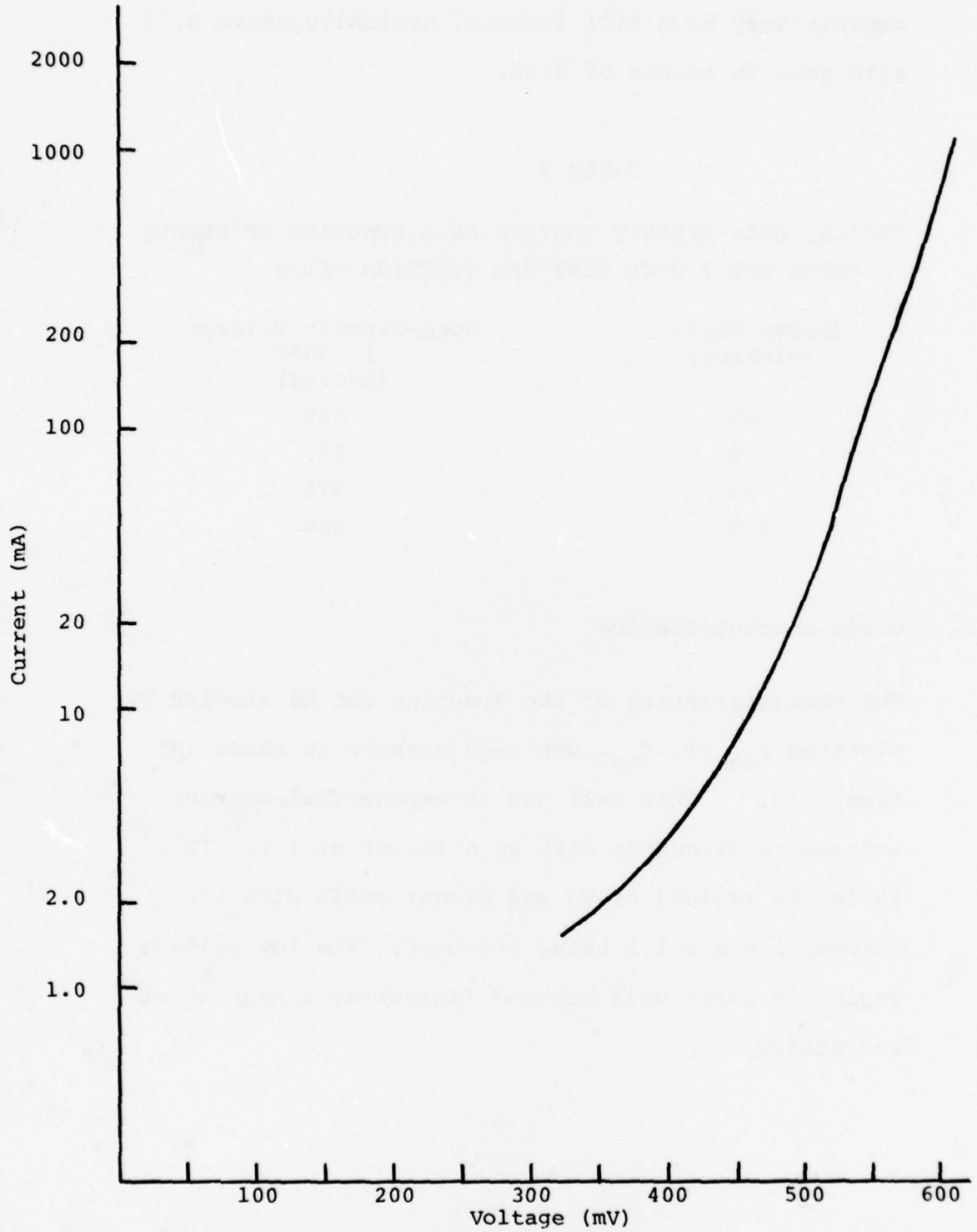


Figure 11. I_{sc} vs. V_{oc} for a 2cm x 2cm Vertical Junction Solar Cell.

Overall the diode characteristics of the VJ cell are very much like those of planar cells indicating as expected that the junction itself is equivalent to a planar junction independent of geometry.

3. Optical Characteristics

A typical plot of Reflectance vs. Wavelength for both a VJ cell and a planar silicon cell with a single layer AR coating is shown in Figure 12. Both cells are without covers. These curves show the flattened spectral response of the VJ structure and indicate the overall improved optical absorption of these cells.

The hemispherical emittance of VJ cells is given below.

Uncovered VJ	$\varepsilon_n = 0.77$
Covered VJ	$\varepsilon_n = 0.86$

The absorptance of VJ cells is given below:

Uncovered VJ	$\alpha = 0.87$
Covered VJ	$\alpha = 0.89$

The α values are higher than for planar cells but somewhat lower than for pyramid textured, while the ε values are somewhat higher than for other covered cells.

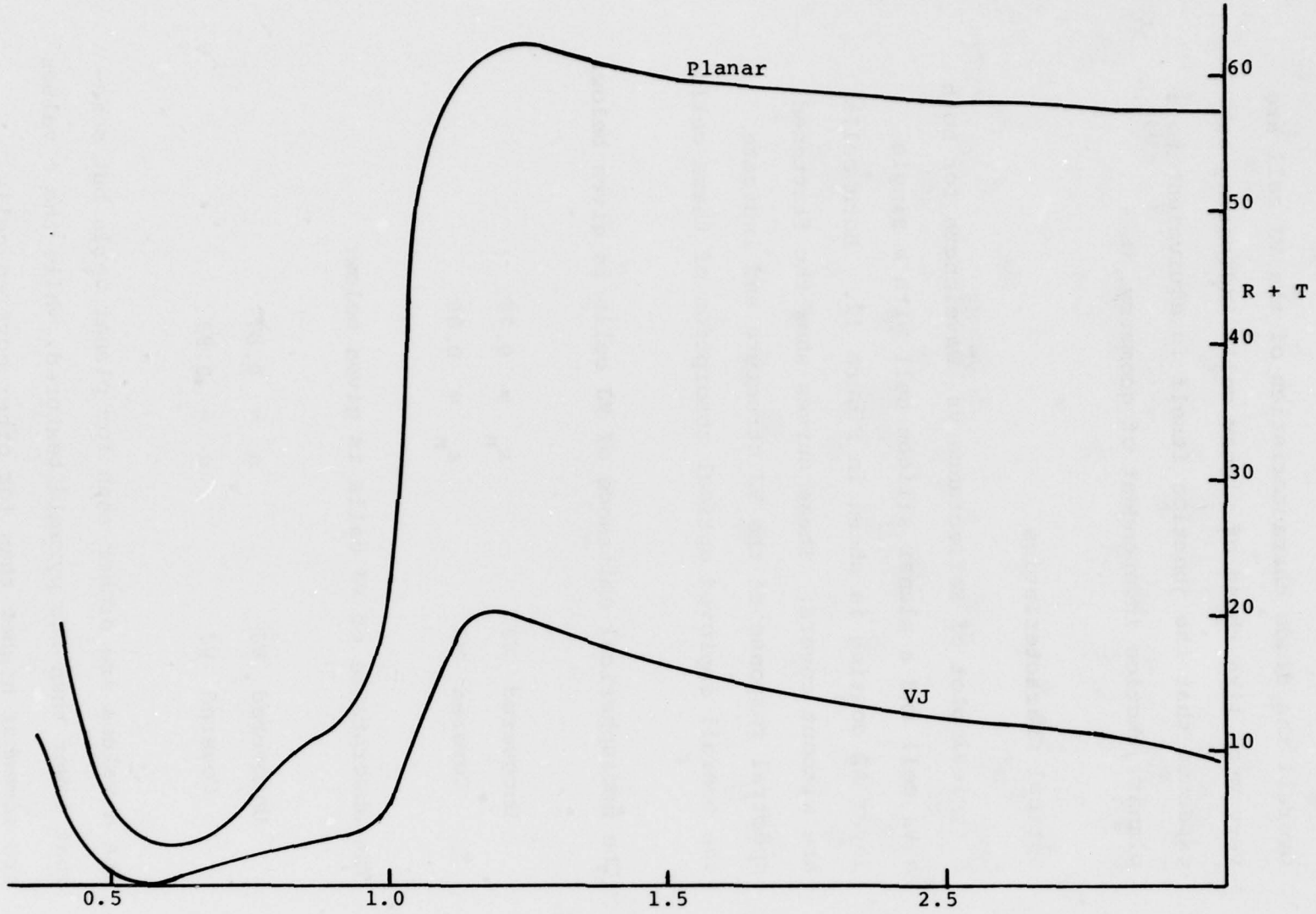


Figure 12. Reflectance vs. Wavelength for a Planar CELL.

The ratio of total absorption to emissivity (α/ε) is an extremely important parameter for a solar cell. A higher α/ε ratio means the cell will absorb more energy from the sun and therefore operate at a higher temperature at a lower overall cell efficiency. Covered planar cells typically exhibit an α/ε ratio of slightly greater than 1.0 as shown in Table 5. Pyramid textured cells when covered have an α/ε ratio of 1.03 to 1.04. This is a considerably lower ratio than for any other textured cell and indicates that VJ cells will operate at a lower temperature under equivalent deployment conditions. The VJ cells have a lower α/ε ratio because:

1. α is somewhat lower than for other textured cells because of the rounded wall tops.
2. ε is higher than for other silicon cells because of the large surface for emission.

TABLE 6

OPTICAL PROPERTIES OF SOLAR CELLS

Cell Type	α/ε Ratio
Solarex Planar	1.02*
Planar - Violet Type	1.06 to 1.12*
Pyramid Textured	1.18*
Vertical Junction	1.03

*See Meulenberg Ref. 14.

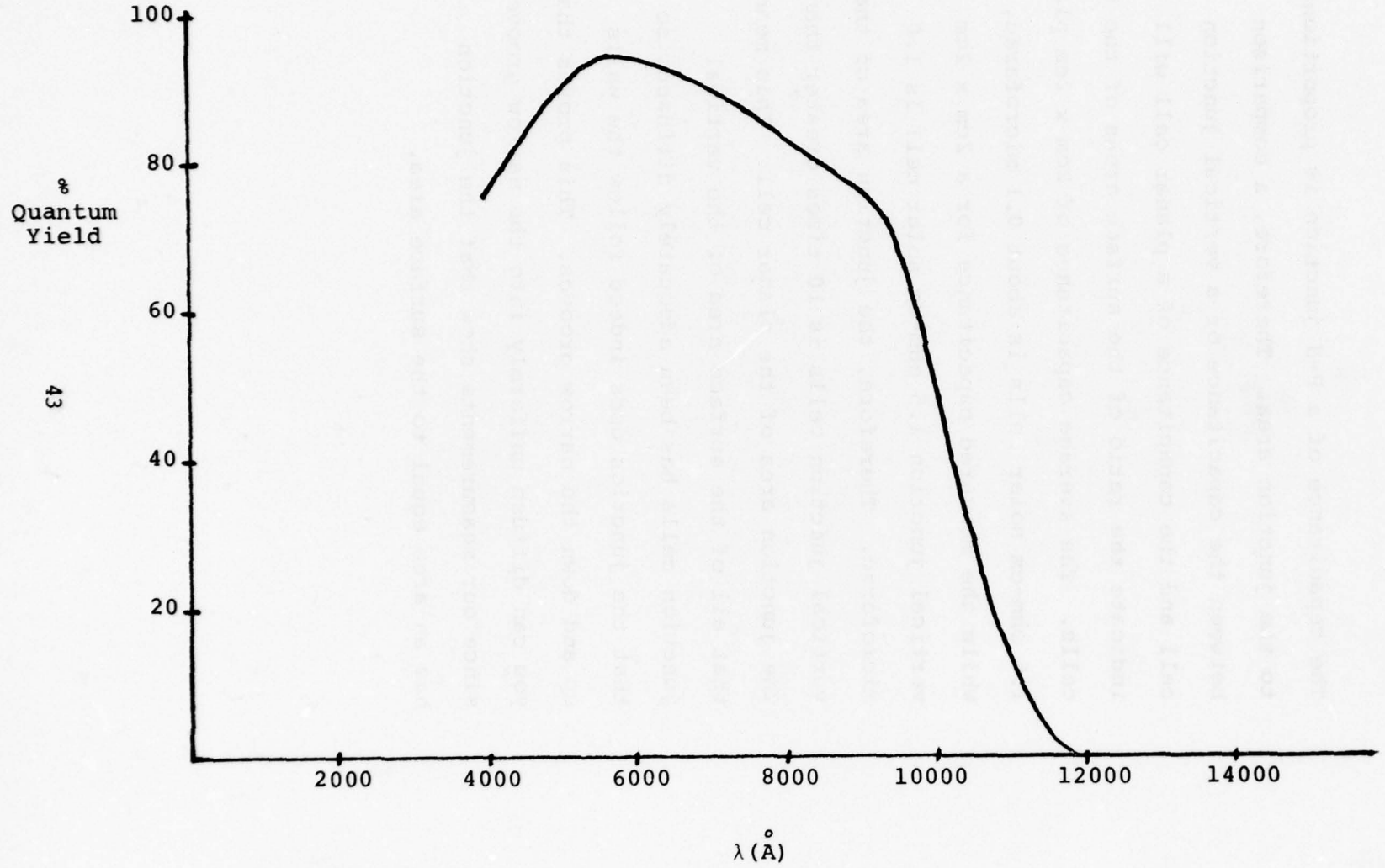
4. Spectral Response

The spectral response of a typical 2 Ω-cm VJ cell is shown in Figure 13. The quantum yield of this cell peaks at over 90% at a wavelength of approximately 6000 Å. The peak is quite broad with over 75% yield between 4000 Å and 9000 Å. The red response is excellent since there is a significant response at wavelengths beyond 10,000 Å.

A second way to study the spectral response of cells is by measuring the I-V curve using different filters so that the cell is only responding to light in a particular segment of the spectrum. Using a blue filter enables one to study the response to the high energy portion of the spectrum, which is absorbed near the surface of the cell. A red filter enables one to look at the lower energy portion of the spectrum, where the light penetrates deep into the bulk of the cell. Table 4 shows the maximum values of red and blue current obtained for the various size cells. The blue component is extremely high, indicating that the cells indeed do absorb well and that the diffused layer produces a high quality shallow junction optimized for space applications. The red current is also good indicating that the cells have good optical absorption, no degradation in bulk lifetime and a back surface field.

Figure 13

Quantum Yield vs. Wavelength for a 2cm x 2cm Vertical Junction Solar Cell



5. Capacitance

The capacitance of a P-N junction is proportional to the junction area. Therefore, a comparison between the capacitance of a vertical junction cell and the capacitance of a planar cell will indicate the ratio of the surface areas of the two cells. The average capacitance of 2cm x 2cm planar 1.5 ohm-cm solar cells is about 0.1 microfarad, while the measured capacitance for a 2cm x 2cm vertical junction 1.5 ohm-cm solar cell is 1.0 microfarad. Therefore, the junction area of the vertical junction cells is 10 times greater than the junction area of the planar cell. This means that all of the surface area of the vertical junction cells has been adequately diffused, so that the junction does indeed follow the walls up and down the narrow grooves. This proves that you can diffuse uniformly into the narrow grooves, since our measurements show that the junction has an area equal to the surface area.

The capacitance per unit area of a uniformly doped P-N junction can be written as

$$1/C^2 = \frac{2(V_d + V)\ (N_a + N_d)}{e\varepsilon_0\varepsilon \qquad N_a N_d} \qquad (5)$$

Therefore, a plot of $1/C^2$ vs. V, where V is the reverse bias voltage will be a straight line for a uniform P-N junction. Figure 14 is a plot of $1/C^2$ vs. V for a typical VJ cell. Vertical Junction cells consistently produce straight lines as shown in this graph. The intercept yields

$V_d = 0.75$ Volts

which is also typical of VJ and planar cells.

6. Temperature Coefficients

The temperature coefficient of open-circuit voltage, maximum power and short circuit current from 0°C to 90°C have been measured. The results are summarized in Table 7. These temperature coefficients are constant over the range of temperatures studied.

TABLE 7

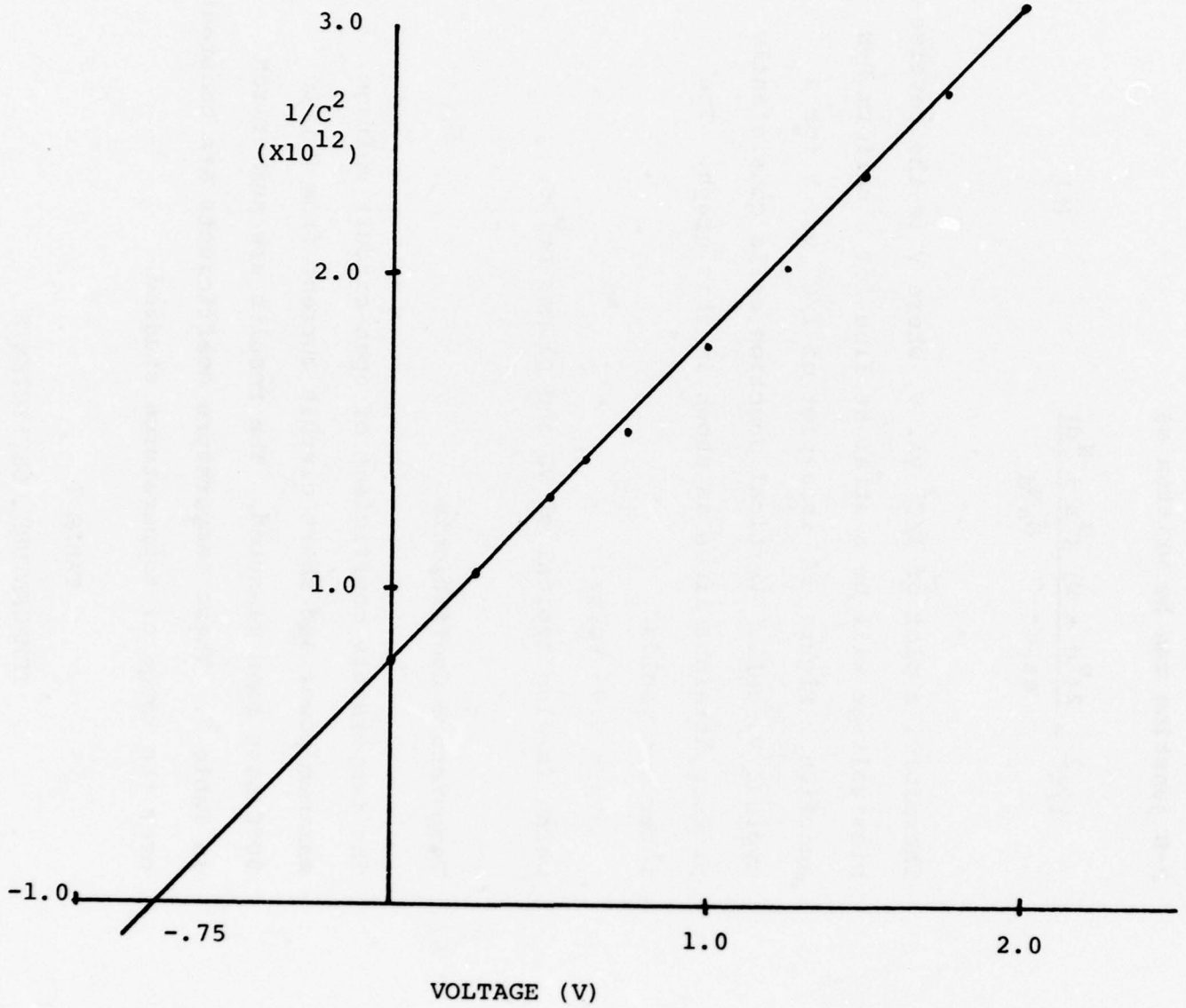
TEMPERATURE COEFFICIENTS

$$\frac{\Delta V_{oc}}{\Delta T} = -2.05 \text{ mV/°C}$$

$$\frac{\Delta P_{max}}{\Delta T} = -0.5\text{%/°C} \qquad \frac{\Delta I_{sc}}{\Delta T} = +0.07\text{%/°C}$$

Figure 14.

$1/C^2$ vs. V for a Reverse Biased VJ Cell (2 x 2 VJ #2)



The values obtained are not significantly different from those measured for other 2Ω-cm silicon cells.

7. Temperature Cycling Experiments

Thermal cycling of vertical junction cells both with and without covers have been performed. Cycling from -196°C to 140°C thru 5 cycles resulted in no change in the uncovered VJ cell I-V characteristics. However, the covered cells degraded as shown in Figure 15. Visual inspection indicates that walls have cracked in these samples. A study of the relationship between the speed of the thermal cycling and the amount of wall destruction shows that slower cycling results in more cell deterioration. Therefore, it is not the thermal shock which is destroying the walls, but rather a result of some mismatch of coefficient of thermal expansion. At this writing no cover sliding technique has been perfected for the VJ cells that can withstand this thermal cycling routine.

8. Radiation Damage

Vertical junction cells have been subjected to electron, proton and neutron irradiation to study the improvement in radiation resistance. Details of the experiments

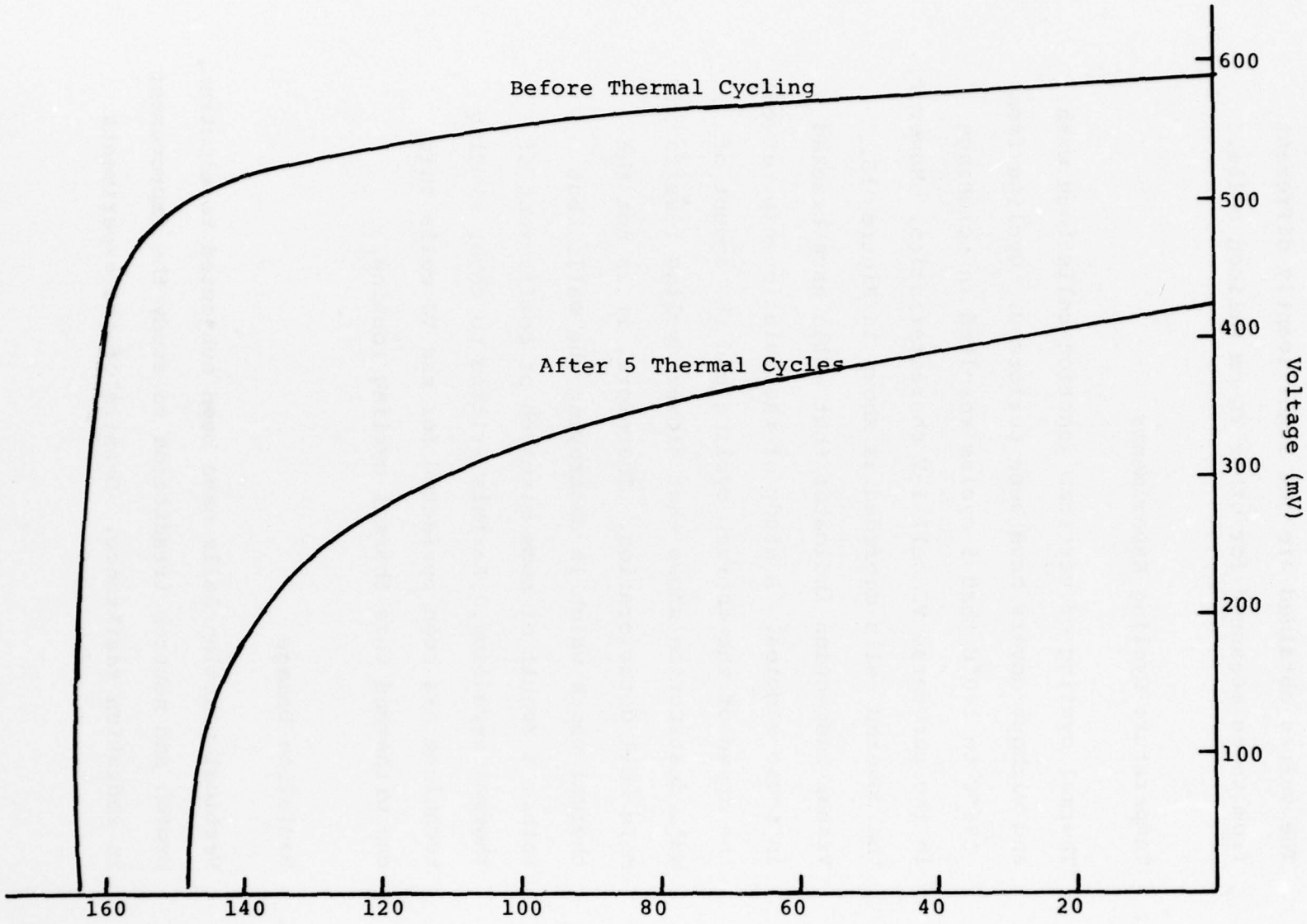


Figure 15. I-V Characteristics of VJ Cell Before and After Thermal Cycling with Cover Attached.

and the results can be dound in work by Rahilly and Anspaugh (Ref. 15) and Anspaugh (Ref. 16). Figure 16 is a plot of power vs. fluence for both a VJ and a planar 2 Ω-cm silicon solar cell under 1 Mev electron irradiation. Figure 17 is a plot of short circuit current vs. fluence for both VJ and planar 2Ω-cm silicon solar cells under 1 Mev electron irradiation. This shows that vertical junction cells are significantly more radiation resistant than planar cells.

9. Metallographic Analysis of Junctions

Metallographic analyses of angle lapped VJ front and back junctions have been performed. Figure 18 is a photograph at 960X of the front junction of an angle lapped VJ cell. The light region is the bulk silicon showing the wall structure. This sample has been decorated with a copper stain showing the diffused n+ junction following the wall surface. The apparent thicker diffusion region at the top of the walls is due to the angle of polishing. The deeper appararent junction penetration at the bottom of the grooves may be due to enhanced copper plating in this area although future work is required to verify this.

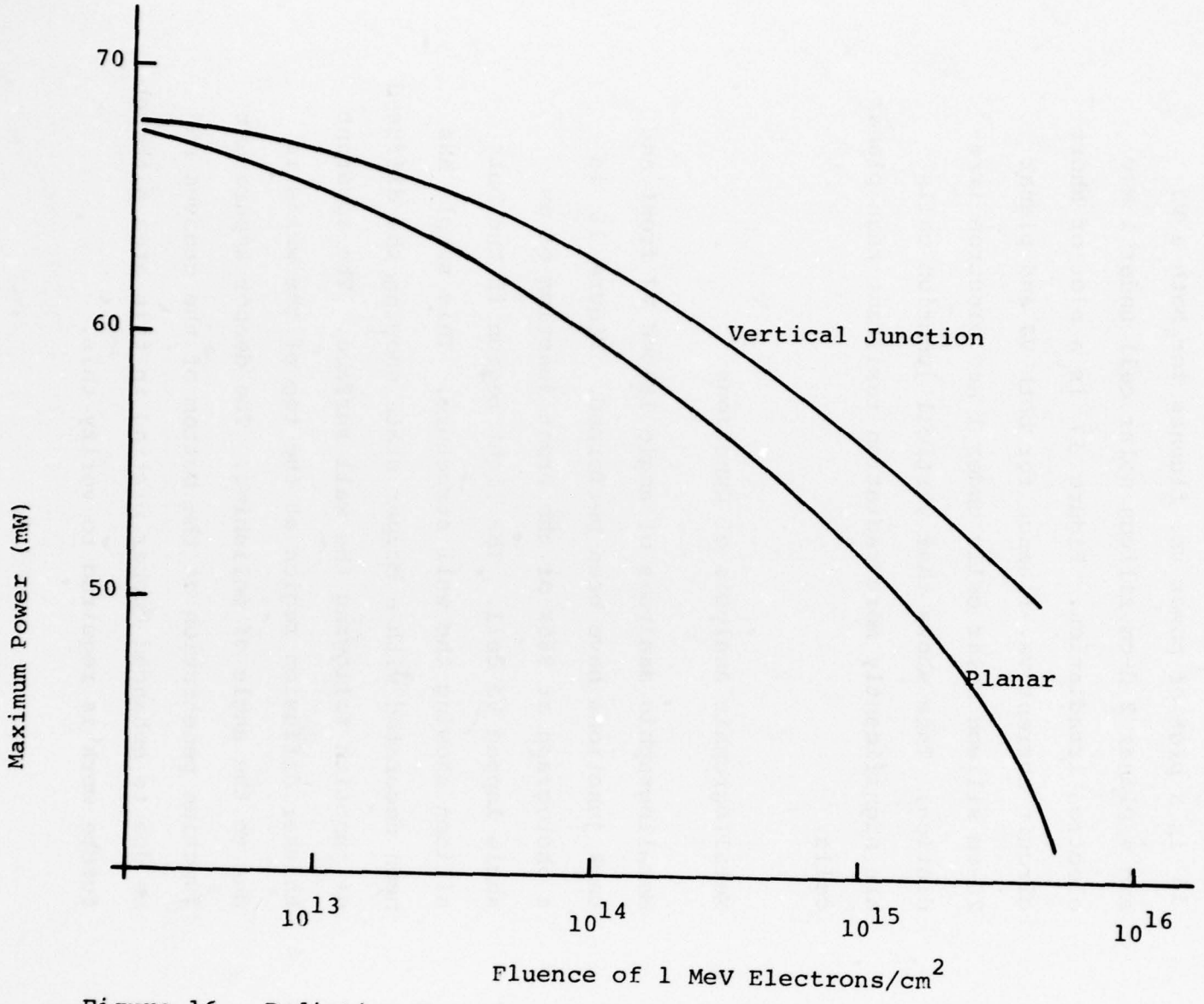


Figure 16. Radiation Degradation of the Maximum Power for Vertical Junction and Planar Silicon Solar Cells.

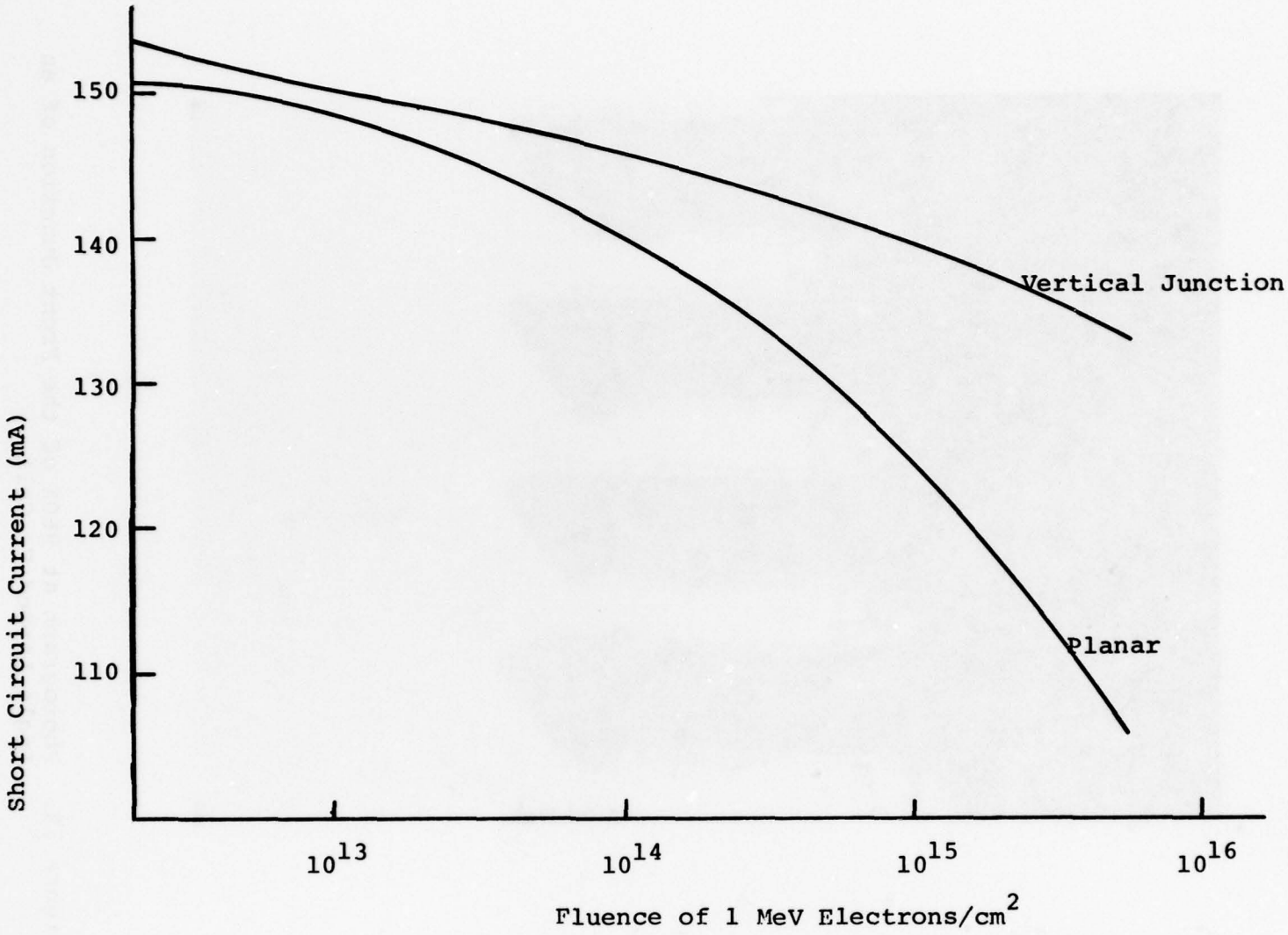


Figure 17. Radiation Degradation of the Short Circuit Current for Vertical Junction and Planar Silicon Solar Cells.

Figure 18. Photograph at 960X of the Front Junction of an Angle Lapped VJ Cell.

The VJ cells have been fabricated using an aluminum alloy back surface field. Figure 19 is a photograph at 480X of such a back junction. The white area to the left is silicon, while the dark area to the right is Al covered with clear plastic. Note the Al spikes into the silicon. In these regions the Al has alloyed into the silicon creating spikes surrounded by a heavily doped p^+ layer.

10. Production Phase

The final phase of this program entailed the production of

- o 100 2cm x 2cm VJ cells
- o 300 2cm x 4cm VJ cells
- o 100 2cm x 6cm VJ cells

This phase was run as a separate delivery phase and resulted in the fabrication of high performance cells with excellent yields. During this production run the yield of cells with greater than 12% AM0 efficiency was 68%. The yield of cells with greater than 13% AM0 efficiency was 42 %.

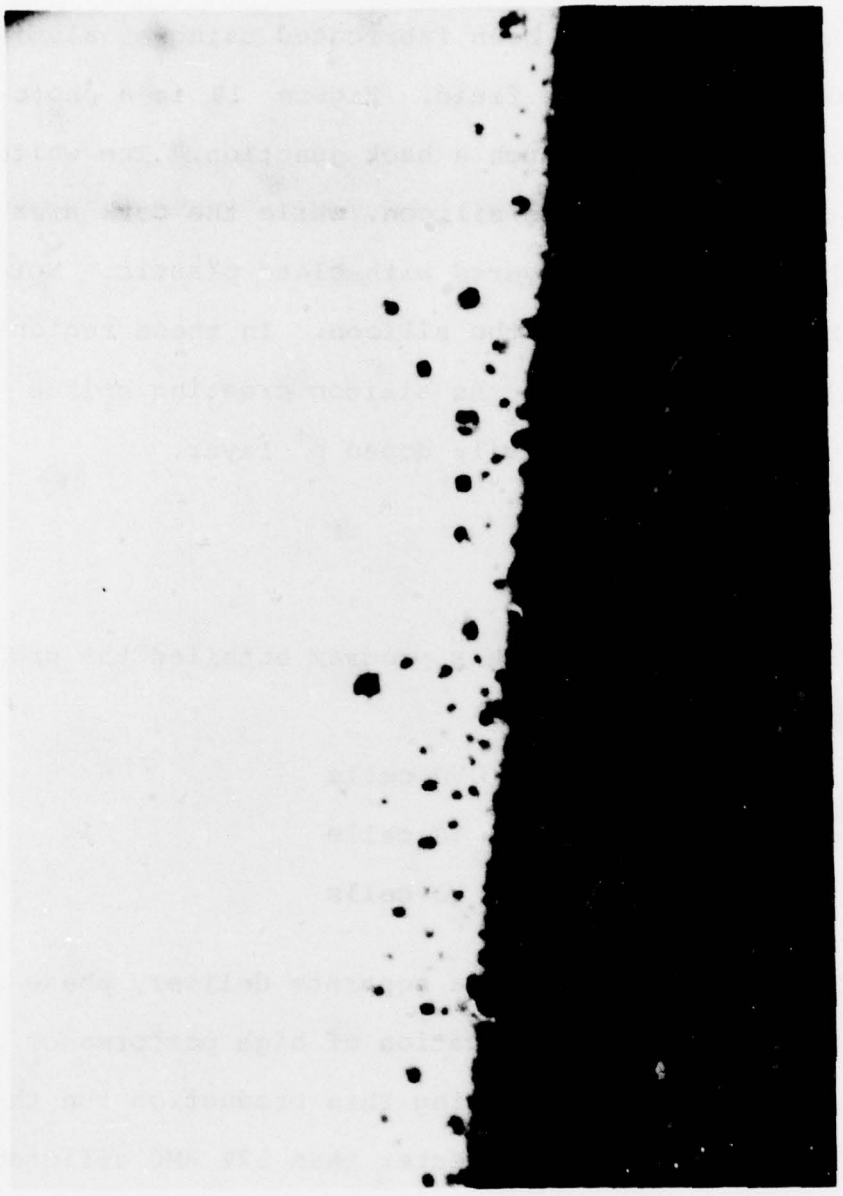


Figure 19. Photograph at 480X of the Back Junction of an Angle Lapped VJ Cell.

SECTION V

CONCLUSIONS

The vertical junction silicon solar cell has been developed to the point where it is a practical device for use in high radiation environments. Even the present initial AM0 efficiencies of greater than 14% are not prohibitive because of the improved radiation resistance.

The vertical junction cells are fabricated with processes that are readily adaptable to quantity production and high yield. The production phase indicated that these cells can be produced with larger sizes and in larger numbers with excellent results. The vertical junction cell has been moved from the realm of experimentation to the realm of practicality ready for use in space missions today.

Future work in the development of vertical junction cells is needed in the following areas:

- Continue research and development on cell fabrication and design to increase the initial cell efficiency and to improve even further the radiation resistance.
- Manufacturing engineering development so that large quantities of VJ cells can be produced at lower cost per Watt.
- Cover sliding development so that VJ cells can be adequately protected during use in space.

With these developments the vertical junction cell could offer an improved power source for space missions and even supplant conventional silicon solar cells as the standard power source for many space applications.

APPENDIX A

SAFETY ANALYSIS

The safety of vertical junction solar cells involves the safety; 1) during manufacture of the VJ cells and 2) during handling for test or array manufacture.

The vertical junction solar cell is fabricated using standard solar cell and semiconductor manufacturing techniques. Acid, base, and solvent handling procedures are performed in compliance with OSHA regulations. Handling of the devices is generally performed using tweezers so the danger of lacerations is a minimum. Processing of vertical junction cells presents no unique safety hazards to the production personnel.

The vertical junction solar cell produces approximately 0.6 volt at typical illumination levels. This voltage level is too low to have any effect at all on personnel handling the finished cells. When large numbers of cells are strung together in arrays they can pose an electrical danger to personnel. Such arrays or panels of cells (as for all solar cells) must be maintained in a short circuit condition when not actually in use so that no dangerous voltage is present. When assembling systems, care must be taken to shadow the cells and/or ground each section as it is connected together.

The vertical junction cell poses no safety hazards beyond those normally encountered for semiconductor processing and solar cell array fabrication.

APPENDIX B

SPECIFICATION SHEET

1.0 SCOPE

1.1 This specification sheet covers all quantitative parameters referenced by the general specification for silicon solar cell assemblies to be used for space flight.

2.0 REQUIREMENTS

2.1 Materials

2.1.1 Silicon - Boron doped, single crystal P-type with resistivity between 1.5 and 2.5 ohm-cm. Crystal oriented 110 side for orientation dependent etch.

2.1.2 Contact Materials - Titanium - Palladium - silver.

2.1.3 Anti-Reflection Coating - Tantalum Pentoxide (Ta_2O_5).

2.1.4 Uncovered

2.2 Contact Thickness and Surface Finish (3.3.5.1)

2.2.1 Thickness - The thickness of the contact system required in Paragraph 2.1.2 shall be no less than 8 μm in the contact areas shown in Figure 1.

2.2.2 Surface Finish - Vertical Junction structure with grooves 5-10 microns wide and walls 5-10 microns wide. Spacing 15 microns from center to center. Grooves 75 microns deep.

2.3 Electrical Output (3.3.1) - The minimum cell current and lot minimum average current measured at 460 mV shall be as follows:

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Cell Size	Minimum I MA Group
2 x 2 cm	150
2 x 4 cm	300
2 x 6 cm	450

2.4 Marking of Product - Each cell marked as to lot number with I_{sc}, V_{oc}, Max P, I_{scRed} and I_{scBlue} given.

2.5 Solar Cell Dimensions - See Figure 5, 6 and 7.

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