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# MONOLITHIC 20W 2GHz TRANSISTOR AND MONOLITHIC 5W 4GHz TRANSISTOR

QUARTERLY REPORT NO. 5

14 JUNE 1978 - 13 SEPTEMBER 1978

CONTRACT NO. DAAB07-77-C-0431

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PREPARED FOR:

DEPARTMENT OF THE ARMY
US ARMY COMMUNICATIONS AND
ELECTRONICS MATERIEL READINESS COMMAND
FORT MONMOUTH, NEW JERSEY 07703

TRW SEMICONDUCTORS
DIVISION OF TRW INC.
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Pin Epi — V-groove
Edge Crown — Buffered Epi
Via

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)


Two metallization processes were developed for metallization of the deep V-grooves used as vias. These processes are being implemented on several lots of L-10 devices.

A shipment of engineering samples of Type A and Type B devices was made to ERADCOM during this quarter.


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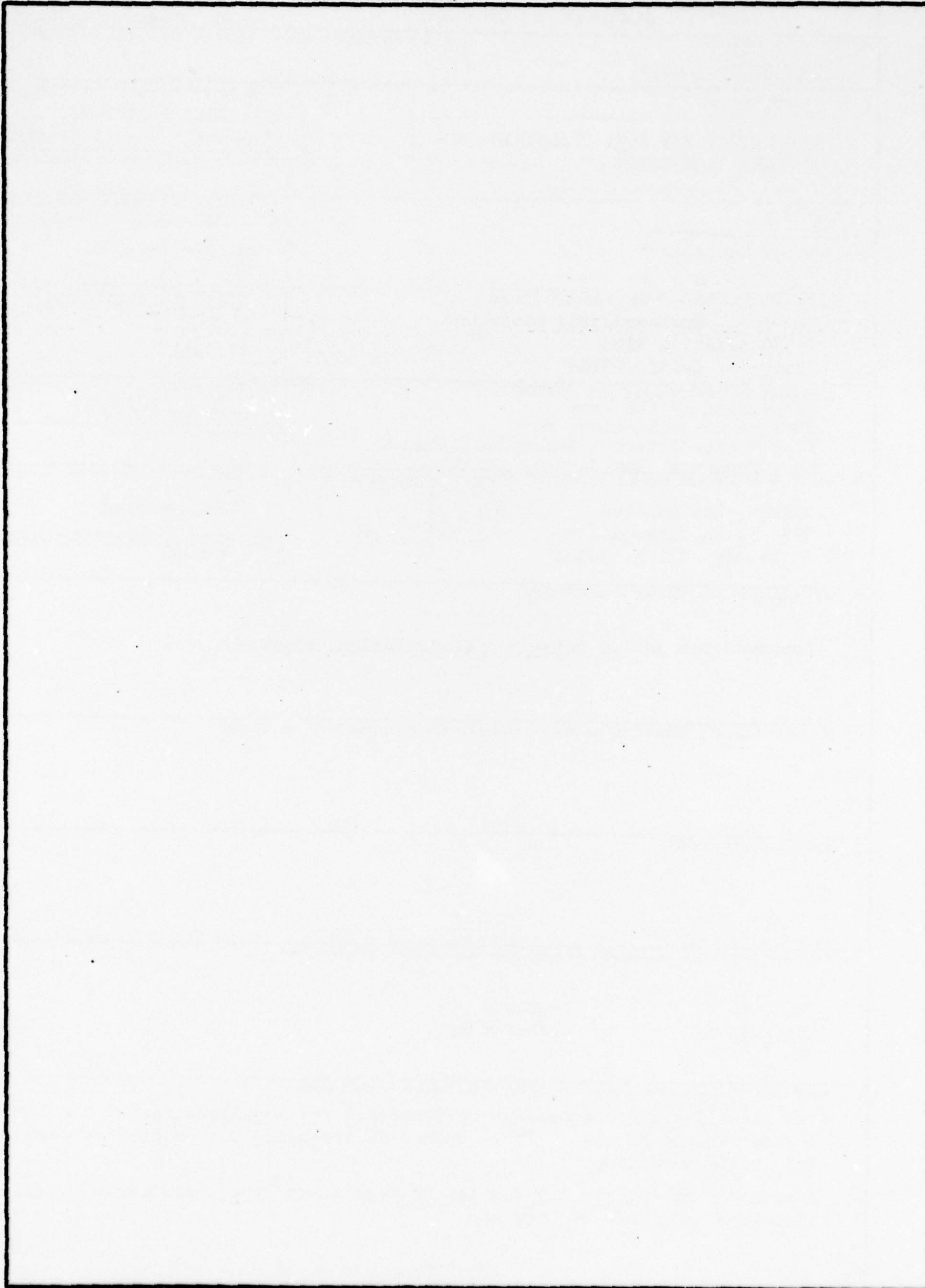

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## SECTION I

## INTRODUCTION

During this period of work, significant progress was made toward the solution of the critical processing problem of via formation for the monolithic Type A device. Two processes for formation of the ground via were developed and readied for implementation.

The first shipment of engineering samples was delivered to ERADCOM during this period. Test data for the shipment is included in this report.

The present work is in the stage of developing the active transistor elements with isolation and integral ground connection. Following the development of the monolithic transistor, the program will go to the pilot production phase, followed by the production feasibility demonstration.

No printing on this page.

## SECTION II

## TECHNICAL WORK THIS QUARTER

### 2.1 INTRODUCTION

The post-via and pre-via processes were finalized during this period. All work was done on dummy wafers so as not to ruin nearly completed wafers during process development.

For the purposes of definition, in the pre-via process the via is etched prior to finger metallization, and in the post-via process the via is etched after finger metallization.

### 2.2 PRE-VIA PROCESS

When the deep (3.5 mil) V-groove used for the via is etched prior to finger metallization, normal photoresist processing for the definition of the fine finger geometry ($\sim 2\mu$) becomes impossible. Normal photoresist processing involves spin coating of the photoresist onto the wafer. However, the spin process requires a planar wafer surface to provide the very important uniform thickness coat of photoresist. The deep via disrupts the planar surface and prevents the application of a uniform photoresist coating unless special precautions are taken.

The pre-via process sequence is desirable due to the fact that the via is etched and open during platinum deposition and conversion so that ohmic contact regions are formed in the via

and active transistor contact regions simultaneously. A normal one-layer metallization process is adequate to complete the active device if desired, although two-layer metal may still be used for other reasons such as feeder bar build-up. However, the two-layer metal plate-up still requires only one sputter deposition of the refractory metallization and background gold.

Several months of effort were expended on attempting to apply a thin, controlled, and uniform coating of photoresist. Many different photoresist compositions and coating methods, such as spin-on, spray-on and roll-on, were tried with only marginal success. The conclusions at the end of this effort were that the surface of the wafer must be planar, and there was no way around that fact.

One method of obtaining a planar surface was to etch the via later; however, there were other serious problems with that approach, as described later in Section 2.3. Another method of obtaining a planar surface was to backfill the via with some compound after it had been etched and the ohmic contacts were formed. The material used to backfill the via would be present only during the normal spin-on of the normal metallization photoresist and would be removed before plate-up. The material chosen was a high viscosity positive photoresist which was applied by flooding the wafer and baked on without a spin. The photoresist covering all areas of the wafer except the vias is exposed and

developed off, leaving the via filled to the surface with acceptable planarity. Then the normal metallization negative photoresist could be spun-on as normal. Some problems were encountered in hard baking the backfill in that the photoresist filling the via would crack or actually pop out of the via; however, this problem was solved by optimization of the baking technique. The negative metallization could be exposed as normal and then developed. The particular negative photoresist developer used is also an effective positive photoresist stripper, so that during the development of the negative photoresist the positive photoresist backfill is completely removed. The wafer could then proceed to metal plate-up as normal.

If a second level metallization is used, normal spin-on photoresist processes are adequate due to the fact that the second metal pattern definition is of gross geometry and far enough away from the vias so that photoresist difficulties are not a problem.

## 2.3 POST-VIA PROCESS

The alternative approach to ground via fabrication is the post-via process. In this process, the via is etched after the ohmic contacts and finger metallization are formed so that planarity is not a problem. However, since the via is etched after the formation of ohmic contacts on the transistor, an additional low temperature ohmic contact for the via must be formed. The

maximum temperature of contact formation is limited to 400°C so that the previously defined metallization will not be disturbed. Also, a pinhole free passivation and masking layer must be used over the regions which do not receive the V-groove etch to prevent etching in undesired areas. This passivation must stick to silicon, $SiO_2$, and gold and must conformally coat over large steps and slight re-entrant angles, must hold up against hydrazine at 100°C, and must be deposited at less than 400°C. The ohmic contact and passivation schemes will be discussed in the next section.

### 2.3.1 Passivation

The passivation issue has been a major problem. Many different passivants were tried and most failed at least one of the necessary criteria.

Photoresist won't hold up to hydrazine. Silox doesn't adhere well to gold and tends to crack when deposited over large metal areas such as feeder bars. Ethyl silicate cannot be deposited at a low enough temperature.

Plasma deposited silicon nitride ($Si_3N_4$) appears to work fairly well. It will hold up to hydrazine, sticks to gold, can be deposited at 300°C, and it forms a comformal coat due to the very short mean free path of particles in the plasma. We have been using outside vendors to deposit the $Si_3N_4$ until our

own plasma system is installed, so control of the process is difficult; however, acceptable films have been obtained. The silicon nitride layer is deposited over the metallized wafers and then the areas to be V grooved are opened and etched. The silicon nitride is then opened again to expose the feeder bar areas to be plated up, and the wafers are transferred to second layer metallization.

The remaining silicon nitride forms the final device passivation.

### 2.3.2 Ohmic Contacts

An ohmic contact must be used in the via to prevent rectifying metal-semiconductor junctions and to provide the lowest possible contact resistance. Platinum is normally used as the contact metal but is not useful in this application, as the 400°C temperature limit will not allow proper conversion to PtSi.

The first lot of L-10 devices had no special ohmic contact at all, TiW was the only contact metal. The contacts obtained were ohmic but had 30 times the desired resistance.

Aluminum has been employed as the ohmic contact metal with good results on test vias. The aluminum is sputtered onto the wafer and is removed everywhere except in the via. Then the

refractory metallization for the second layer metallization is sputtered on, and the second level metallization is plated up in the via and wherever else it is necessary.

## 2.4 L-10 STATUS

One lot each of L-10 devices was run through the pre-via and post-via process. Both failed due to an unrelated metal adhesion problem caused by a contaminated plating bath. The lots were stripped and will be re-metallized.

## 2.5 ENGINEERING TEST SAMPLES

Fifteen each Type A and Type B devices were shipped to ERADCOM during this quarter. The test report for these devices is included for reference in this report.

Universal Report No. ____________

Originator's Report No. 77-0431

Revision ____________

REPORT OF TEST ON: Engineering Samples - 1st Submission Type A and Type B

TEST PERFORMED BY:

George Schreyer

TEST AUTHORIZED BY:

Fred Mayer

Contract No. DAAB07-77-C-0431

July 21, 1978

Report Written By: ____________

Technician: ____________

Test Engineer: ____________

Supervisor: ____________

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GENERAL REPORT SUMMARY SHEET

Report No.: 77-0431

Engineering Samples-1st Submission
Type A and Type B

8. OUTLINE, TABLE OF CONTENTS, SUMMARY, OR EQUIVALENT DESCRIPTION


ABSTRACT

This report presents the test data for 15 type A and 15 type B devices. These devices were assembled from the best available lots at the date of testing.


TYPE A DEVICES

The type A devices are a single cell of the L-10 design. The chip was mounted directly to a copper flange for testing, as shown in Figure 2.

DC data was taken on 29 devices, 15 of which passed dc test. The data for the passed devices is shown on page 9.

RF testing was done in the station diagrammed on page 3 at 2.0GHz in the CW mode.

Two levels of power were measured, maximum saturated power and gain and efficiency were recorded, and gain and efficiency at 5 watts output were recorded. No devices failed during RF testing. Data is shown on pages 10 and 11.

TYPE B TESTING

15 type B devices, Figure 3, were assembled in a BeO package and tested.

DC data was recorded on all devices and is shown on page 8. None failed dc test.

RF data was recorded at 4GHz in the CW mode in the test station diagrammed on page 6 at a saturating drive level of

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GENERAL REPORT SUMMARY SHEET

| 1. COMPONENT/PART NAME PER GENERIC CODE | 2. PROGRAM OR WEAPON SYSTEM |
| --- | --- |
| | 5. ORIGINATOR'S REPORT NO. 77-0431 |
| 4. ORIGINATOR'S REPORT TITLE: Engineering Samples-1st Submission Type A and Type B | 6. TEST TYPE, ETC. |

7. THIS TEST (SUPERSEDES) (SUPPLEMENTS) REPORT NO:

8. OUTLINE, TABLE OF CONTENTS, SUMMARY, OR EQUIVALENT DESCRIPTION

300mw. Power output and efficiency are shown on page 7. None failed RF testing. No tuning was done on any type B device after initial fixture adjustment.

SUMMARY

The type A devices have poor RF performance as described in Quarterly Reports No. 3 and 4.

The type B devices have excellent RF performance and excellent yield.

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Figure 1. S-Band Test Station

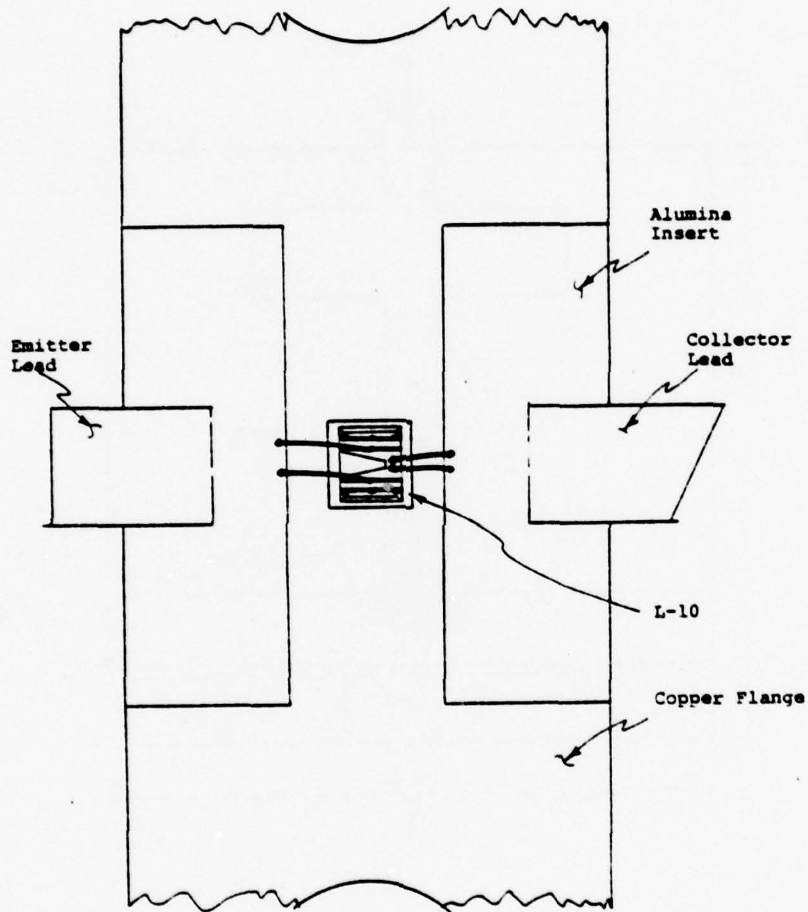


Figure 2. L-10 Device

-4-

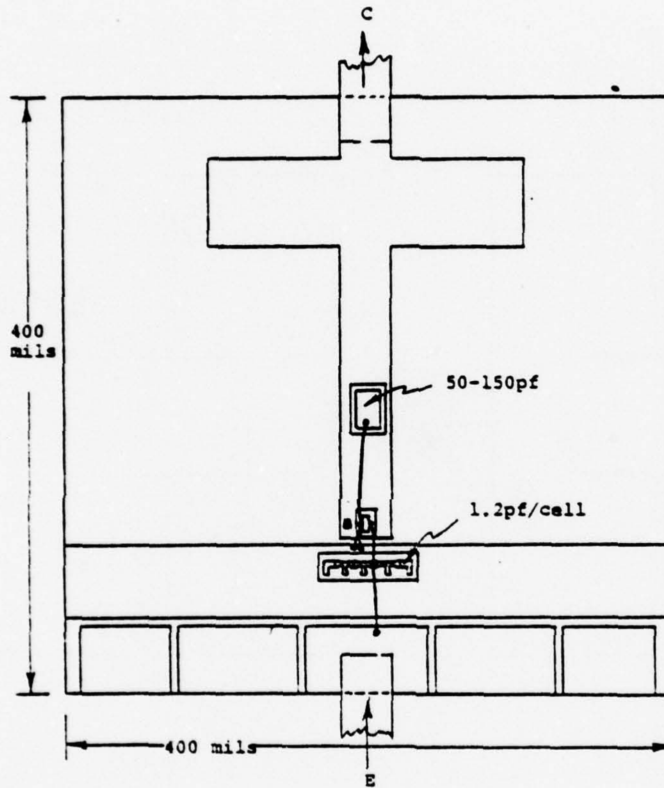


Figure 3. 4GHz Test Vehicle

Figure 4. Drawing of Test Setup for 4GHz Tests

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2. PROGRAM OR WEAPON SYSTEM

3. ORIGINATOR'S REPORT NO.
77-0431

4. ORIGINATOR'S REPORT TITLE
Engineering Samples-1st Submission
Type A and Type B

6. TEST TYPE, ETC.
SB-4000 RF Tests

7. THIS TEST SUPERSEDES/SUPPLEMENTS REPORT NO.

8. OUTLINE, TABLE OF CONTENTS, SUMMARY, OR EQUIVALENT DESCRIPTION

SB-4000 RF TESTS

$V_{cc}$=24V f=4.0GHz

| # | $P_o$ W | $P_{in}$ W | $I_c$ A | Gain dB | $\eta_c$ % |
|---|---|---|---|---|---|
| 1 | 1.6 | .3 | .199 | 7.3 | 33.5 |
| 2 | 1.62 | .3 | .206 | 7.3 | 32.8 |
| 3 | 1.5 | .3 | .202 | 7.0 | 30.9 |
| 4 | 1.66 | .3 | .202 | 7.4 | 34.2 |
| 5 | 1.75 | .3 | .213 | 7.7 | 34.2 |
| 6 | 1.64 | .3 | .214 | 7.4 | 34.1 |
| 7 | 1.66 | .3 | .202 | 7.4 | 34.2 |
| 8 | 1.75 | .3 | .203 | 7.7 | 35.9 |
| 9 | 1.72 | .3 | .210 | 7.6 | 34.1 |
| 10 | 1.66 | .3 | .206 | 7.4 | 34.1 |
| 11 | 1.75 | .3 | .206 | 7.7 | 35.4 |
| 12 | 1.78 | .3 | .207 | 7.7 | 35.8 |
| 13 | 1.68 | .3 | .196 | 7.5 | 35.7 |
| 14 | 1.64 | .3 | .210 | 7.4 | 32.5 |
| 15 | 1.63 | .3 | .195 | 7.4 | 34.8 |

9. GIDEP 10. CONTRACTOR SUBCONTRACTOR

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77-0431

Engineering Samples-1st Submission
Type A and Type B

SB-4000 dc Tests

7. THIS TEST (SUPERSEDES) (SUPPLEMENTS) REPORT NO.

8. OUTLINE, TABLE OF CONTENTS, SUMMARY, OR EQUIVALENT DESCRIPTION

### SB-4000 dc TESTS

| # | $h_{fe}$ 5V@100mA | $BV_{ceo}$ @10mA | $BV_{ces}$ @10mA | $BV_{cbo}$ @10mA | $BV_{ebo}$ @10mA | $R_e$ Ω |
|---|---|---|---|---|---|---|
| 1 | 16 | 24 | 42 | 46 | 5 | 1.81 |
| 2 | 17 | 24 | 42 | 47 | 5 | 1.83 |
| 3 | 16 | 24 | 42 | 46 | 5 | 1.90 |
| 4 | 16 | 24 | 43 | 47 | 5 | 1.84 |
| 5 | 20 | 22 | 42 | 47 | 5 | 1.80 |
| 6 | 17 | 25 | 41 | 46 | 5 | 1.77 |
| 7 | 17 | 24 | 42 | 46 | 5 | 1.75 |
| 8 | 17 | 24 | 42 | 47 | 5 | 1.71 |
| 9 | 20 | 23 | 42 | 47 | 5 | 1.66 |
| 10 | 17 | 24 | 42 | 46 | 5 | 1.78 |
| 11 | 20 | 23 | 42 | 46 | 5 | 1.68 |
| 12 | 20 | 23 | 42 | 46 | 5 | 1.71 |
| 13 | 17 | 23 | 42 | 46 | 5 | 1.72 |
| 14 | 16 | 24 | 43 | 46 | 5 | 1.77 |
| 15 | 16 | 24 | 43 | 47 | 5 | 1.78 |

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4. ORIGINATOR'S REPORT TITLE
Engineering Samples-1st Submission
Type A and Type B

6. TEST TYPE, ETC.
L-10 dc Tests

7. THIS TEST (SUPERSEDES) (SUPPLEMENTS) REPORT NO:

8. OUTLINE, TABLE OF CONTENTS, SUMMARY, OR EQUIVALENT DESCRIPTION

L-10 dc TESTS

| S/N | $h_{fe}$ 5V@100mA | $BV_{ces}$ @10mA | $BV_{cbo}$ @10mA | $BV_{ebo}$ @10mA |
|---|---|---|---|---|
| 7 | 60 | 37 | 38 | 5 |
| 8 | 60 | 41 | 42 | 5.6 |
| 10 | 55 | 42 | 42 | 5.1 |
| 12 | 60 | 42 | 42 | 5.1 |
| 14 | 60 | 42 | 42 | 5.4 |
| 15 | 60 | 32 | 33 | 5.0 |
| 18 | 60 | 42 | 42 | 5.6 |
| 20 | 60 | 42 | 42 | 5.7 |
| 21 | 60 | 30 | 31 | 4.4 |
| 23 | 60 | 35 | 36 | 5.1 |
| 24 | 60 | 42 | 42 | 5.6 |
| 26 | 50 | 29 | 33 | 4.9 |
| 27 | 60 | 39 | 40 | 5.2 |
| 28 | 60 | 40 | 42 | 5.8 |
| 29 | 50 | 42 | 43 | 5.7 |

9. DONOR | 10. CONTRACTOR | SUBCONTRACTOR

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GENERAL REPORT SUMMARY SHEET

Report No.: 77-0431

Engineering Samples-1st Submission
Type A and Type B

L-10 RF Tests

## L-10 RF TESTS

f=2.0GHz

| S/N | $P_o$ W | $P_{in}$ W | $I_c$ A | $V_{cc}$ V | Gain dB | $\eta_c$ % |
|---|---|---|---|---|---|---|
| 7 | 5.8 | 6.4 | 1.27 | 20 | -0.42 | 22.8 |
| | 5.0 | 4.4 | 1.06 | 20 | 1.05 | 23.6 |
| 8 | 6.4 | 6.0 | 1.32 | 20 | 0.28 | 24.2 |
| | 5.0 | 3.2 | 0.98 | 20 | 1.94 | 25.5 |
| 10 | 6.2 | 6.2 | 1.34 | 20 | Ø | 23.1 |
| | 5.0 | 3.5 | 1.02 | 20 | 1.55 | 24.5 |
| 12 | 5.0 | 5.2 | 1.16 | 20 | -0.17 | 21.5 |
| 14 | 6.2 | 6.4 | 1.36 | 20 | -0.14 | 22.8 |
| | 5.0 | 3.5 | 1.01 | 20 | 1.55 | 24.7 |
| 15 | 6.2 | 6.4 | 1.30 | 20 | -0.19 | 23.8 |
| | 5.0 | 3.8 | 1.00 | 20 | 1.19 | 25.0 |
| 18 | 5.7 | 5.7 | 1.22 | 20 | Ø | 23.3 |
| | 5.0 | 4.0 | 1.02 | 20 | 0.97 | 24.5 |
| 20 | 5.2 | 6.4 | 1.28 | 20 | -0.91 | 20.3 |
| | 5.0 | 5.6 | 1.20 | 20 | -0.49 | 20.8 |
| 21 | 6.0 | 6.7 | 1.31 | 20 | -0.48 | 22.9 |
| | 5.0 | 4.0 | 1.02 | 20 | 0.97 | 20.8 |
| 23 | 5.6 | 6.4 | 1.31 | 20 | -0.58 | 21.[illegible] |
| | 5.0 | 4.6 | 1.11 | 20 | 0.36 | 22.5 |
| 24 | 5.8 | 5.5 | 1.26 | 20 | 0.23 | 26.1 |
| | 5.0 | 3.7 | 1.04 | 20 | 1.31 | 24.[illegible] |
| 26 | 6.6 | 6.6 | 1.34 | 20 | Ø | 24.6 |
| | 5.0 | 3.5 | 0.98 | 20 | 1.55 | 24.5 |
| 27 | 6.1 | 6.6 | 1.31 | 20 | -0.34 | 23.8 |
| | 5.0 | 4.1 | 1.02 | 20 | 0.86 | 24.5 |

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| | 3. ORIGINATOR'S REPORT NO. 77-0431 |
| 4. ORIGINATOR'S REPORT TITLE: Engineering Samples-1st Submission Type A and Type B | 6. TEST TYPE, ETC. L-10 RF Tests (continued) |

7. THIS TEST (SUPERSEDES) (SUPPLEMENTS) REPORT NO.

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L-10 RF TESTS (Continued)

| S/N | $P_o$ | $P_{in}$ | $I_c$ | $V_{cc}$ | Gain | $\mu_c$ |
|---|---|---|---|---|---|---|
| 28 | 6.2 | 7.2 | 1.38 | 20 | -0.65 | 22.5 |
| | 5.0 | 3.9 | 1.02 | 20 | 1.08 | 24.5 |
| 29 | 5.9 | 6.8 | 1.30 | 20 | -0.62 | 22.7 |
| | 5.0 | 4.3 | 1.04 | 20 | 0.65 | 24.0 |

9. 10. CONTRACTOR

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# SECTION III

# CONCLUSIONS

## 3.1 CONCLUSIONS

Two via processes were developed during this period of work. Both processes appear to provide a way to directly connect the bases of the isolated devices to ground without disrupting the active devices themselves. Both processes are acceptable from a manufacturing point of view.

Metallization process problems not associated with any of the special metallization requirements of the monolithic devices have prevented actual application and testing of either process. As of the close of this quarter, the metallization problem appears to have been solved, and L-10 devices will be metallized by both via process as soon as possible.

No printing on this page.

## SECTION IV

## EFFORT FOR THE NEXT PERIOD

### 4.1 L-10

Work for the next period will be to process further lots of L-10 devices and further develop the manufacturing techniques necessary to produce acceptable performance at 2.0GHz. Circuit development will be done on L-10 devices to optimize a monolithic shunt inductor to be fabricated on the same chip as an L-10 device.

### 4.2 4GHz

The design process will begin on a 5W 4GHz isolated device. However, some performance and manufacturing data will be required from the L-10 before the 4GHz design can be finalized.

No printing on this page.

## SECTION V PUBLICATIONS, REPORTS, AND CONFERENCES

There were no publications during this quarter.

The following program review conferences were held during this quarter.

July 24, 1978 Program Review at Harry Diamond Lab

Government Personnel: Mr. Horst Gerlach
TRW Semi. Personnel: Bernie Lindgren
Alan Harrington
George Schreyer

August 22/23, 1978 Program Review at Lawndale, Calif.

Government Personnel: Mr. Konrad Fischer
TRW Semi. Personnel: Bernie Lindgren
Alan Harrington
George Schreyer

Monthly Report Nos. 13, 14, 15 were submitted during this reporting period.

No printing on this page.

## SECTION VI IDENTIFICATION OF PERSONNEL

| | Hours |
|---|---|
| Joseph Courier | 150 |
| Alan Harrington | 325 |
| Robert Jenkins | 318 |
| Bernie Lindgren | 85 |
| James Scheppele | 135 |
| George Schreyer | 50 |
| George Skelly | 152 |
| Frank Bartel | 150 |
| Harold Bjornson | 137 |
| Dorothy May | 76 |
| Norman Nissen | 143 |
| Eugenia Nunez | 126 |
| Lois Reed | 73 |
| Stephanie Wesche | 74 |
| William Imhauser | 315 |
| Ken Kam | 24 |
| Chet Winham | 83 |
| Antonio Morawski | 100 |
| Anne Bayard | 140 |
| Arthur Durschlag | 144 |
| Carl Bridges | 139 |
| Ruth Moore | 32 |
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