AD-A065 161 IRT CORP SAN DIEGO CALIF F/G 18/6
HARDNESS ASSURANCE GUIDELINES FOR DISPLACEMENT EFFECTS FOR BIPO--ETC(U)
MAY 78 R A BERGER DAAG39-77-C-0135
UNCLASSIFIED IRT-8166-003 HDL-CR-78-135-1 NL

1 OF 2
AD
A065161



DDC FILE COPY

AD A065161

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

(18) REPORT NUMBER: HDL-CR-78-135-1

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

(6) 4. TITLE (and Subtitle): Hardness Assurance Guidelines for Displacement Effects for Bipolar Devices

5. TYPE OF REPORT & PERIOD COVERED: Contractor Report, July 1977 - March 1978

(14) 6. PERFORMING ORG. REPORT NUMBER: IRT-8166-003

(10) 7. AUTHOR(s): Robert A. Berger

(15) 8. CONTRACT OR GRANT NUMBER(s): DAAG39-77-C-0135

9. PERFORMING ORGANIZATION NAME AND ADDRESS
IRT Corporation
P. O. Box 80817
San Diego, CA 92138
409 388

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
(11) May 78
Prog. El. 62704

11. CONTROLLING OFFICE NAME AND ADDRESS
Harry Diamond Laboratories
2800 Powder Mill Road
Adelphia, MD 20783
Technical Monitor: Harvey Eisen

12. REPORT DATE: 4 April 1978

13. NUMBER OF PAGES

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)
(9) Rept. for Jul 77-Mar 78

15. SECURITY CLASS. (of this report): Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

(12) 115 p.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

(16) Z99QAX (17) TD072

18. SUPPLEMENTARY NOTES
HDL Project No. 243728
AMCMS Code 697000.00.00000
This work was sponsored by the Defense Nuclear Agency under subtask Z99QAX TD072.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)
Hardness Assurance
Guidelines
Integrated circuits
Bipolar transistors

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of this document is to provide an effective means of obtaining semiconductor devices whose neutron-induced response is within known and acceptable limits. The scope of the effort was limited to those procedures for the neutron environment for bipolar transistors, zener diodes, TTL (54/74) series digital integrated circuits, 741-type operational amplifiers, and junction field effect transistors. The objective is met by imposing two levels of Hardness Assurance controls on → next page

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

409 388

79 02 27 010

both the supplier and the user. The supplier levels are called control levels, whereas for the user they are quality levels. For the supplier the difference between levels 1 and 2 are the numbers of Hardness Assurance controls to which the part is subjected in order to be qualified (control level 2 requires screens and process controls, and level 1 is achieved by adding inspection lot radiation tests. For the user, the difference between quality levels 1 and 2 is their lot quality, i.e., the percent of devices in each lot which pass the failure criteria. In level 2 lots, $\geq$ 80 percent of the devices will pass the K_D criteria with 90 percent confidence. Level 1 screening is designed such that 99.9 percent of the devices in bipolar transistor lots will pass.

> or =

sub D

ACCESSION for
NTIS White Section
DDC Buff Section
UNANNOUNCED
JUSTIFICATION
BY
DISTRIBUTION/AVAILABILITY CODES
Dist. AVAIL. and/or SPECIAL
A

CONTENTS

		Page
1.	INTRODUCTION	9
	1.1 Objective and Scope.	9
	1.2 How To Use This Document	9
	1.3 Hardness Assurance (HA) for Pieceparts	9
	1.4 HA Applications to Systems	9
	1.5 Statistical Methods.	14
	1.5.1 Lot Statistical Characterization for Design Margin Calculations	15
	1.5.2 Lot-Sample Statistics for Procurement	22
	1.6 Effect of Screens on Statistical Distributions.	22
2.	HA PLAN FOR SUPPLIER-QUALIFIED PARTS	23
3.	HA PLAN FOR USER-QUALIFIED PARTS	27
4.	HA CONTROLS FOR BIPOLAR TRANSISTORS	31
	4.1 Effects of Neutron Radiation on Bipolar Transistors	31
	4.1.1 Small Signal.	31
	4.1.2 Power Operation.	36
	4.1.3 Switching Operation	37
	4.2 Transistor HA Controls for Supplier-Qualified Parts	38
	4.3 HA Controls for User-Qualified Parts	41
	4.4 User Parts Selection for HA (Small Signal Application)	43
	4.5 User Parts Selection and HA Example Using 2N2222 (Small Signal Application)	47
	4.5.1 Part Selection Procedure	48
	4.5.2 Hardness Assurance Procedure	50
	4.6 User Parts Selection and HA Example Using 2N2222 (Switching Application)	51
5.	HA CONTROLS FOR SILICON ZENER DIODES	59
	5.1 Effects of Neutron Radiation on Zener Diodes	59
	5.2 HA Controls for Supplier- and User-Qualified Parts	60

		Page
6.	HA CONTROLS FOR TTL (54/74 series) DIGITAL INTEGRATED CIRCUITS	61
	6.1 Effects of Neutron Radiation on TTL 54/74 NAND GATES	61
	6.2 HA Controls for Supplier-Qualified Parts	68
	6.3 HA Controls for User-Qualified Parts	69
	6.4 HA Example Using SN54L00	72
7.	HA CONTROLS FOR OPERATIONAL AMPLIFIERS (741)	76
	7.1 Effects of Neutron Radiation on Type 741 Operational Amplifiers	76
	7.1.1 Operational Amplifier (741) Circuit Analysis	76
	7.1.2 Terminal Parameter Neutron Degradation	78
	7.1.3 Special Methods for HA	82
	7.1.4 Operational Amplifier HA Considerations	83
	7.2 HA Controls for Supplier-Qualified Parts	84
	7.3 HA Controls for User-Qualified Parts	87
	7.4 User Part Selection and HA Example Using the UA741	90
8.	HA CONTROLS FOR JFET's	92
	8.1 Effects of Neutron Radiation on Planar JFET's	92
	8.2 HA Controls for Supplier-Qualified Parts	95
	8.3 HA Controls for User-Qualified Parts	96
9.	SUMMARY	96
	9.1 Supplier Control Levels	99
	9.2 User Quality Levels	101
	GLOSSARY	104
	LITERATURE CITED	107
	APPENDICES: A - Standards	109
	B - Certification	113
	DISTRIBUTION	115

FIGURES

1	Hardness Assurance (HA), hardness surveillance (HS), hardness assessment, and hardness validation flow diagram	12
2	Cumulative frequency ℓnK_D data for the 2N2222	18
3	One-sided tolerance limit factors (K_{TL}) for normal distributions at 90 % confidence	19
4	Lot worst-case values and cumulative sample data for 2N2222	21
5	Example of how screens can alter distribution of K_D; (a) distribution of f_T of 16 devices ordered by pre-irradiated values, and (b) distribution of K_D of 16 devices after irradiation	24
6	Histogram of $V_{CE(SAT)}$ at fluence of 0.310E+15 and an I_E of -0.120E+-2 and an I_B of 0.200E+01 for the 2N5399 on a sample of 156 devices	25
7	HA screen effectiveness demonstration	26
8	Supplier HA control levels.	28
9	User (U) HA quality level flow diagram.	30
10	Transistor base current components	32
11	User part selection for small signal applications	44
12	Probability chart for hardness assurance decisions for bipolar silicon NPN transistors (small signal application)	46
13	First (Sect. 1.5) and second 2N2222 lot statistics.	53
14	Logic circuit example of forced beta (β_F) calculation.	55
15	User part selection where $V_{CE(SAT)}$ is the important parameter (switching application)	56
16	54/74 family input-output comparison	62
17	TTL 54L00 logic gate.	63
18	SN54L00 output transistor ℓnK_D cumulative statistics	75

19 741-type operational amplifier schematic 77

20 A comparison of transistor cross sections. 86

21 Type 741 open-loop gain degradation ($\Delta 1/A_{VOL}$) at 3×10^{13} n/cm^2 91

22 N-channel JFET cross section 93

TABLES

I Cumulative frequency statistics of ℓnK_D for one lot of 2N2222 transistors measured with I_C of 10 mA and V_{CE} of 5 V . . . 17

II Calculation of worst-case ℓnK_D value 20

III Transistor supplier-qualified part procurement specification example (2N2222) 39

IV Transistor user-qualified part procurement specification example (2N2222) 42

V Second lot 2N2222, Test 660811. I_C = 10 mA, V_C = 3V 52

VI Candidate TTL screening and quality conformance parameters 66

VII TTL supplier-qualified part procurement specification example (54L00 for power gate) 70

VIII TTL user-qualified part procurement specification example (54L00 low-power gate) 71

IX Calculation of output transistor damage factor from I_{SK} measurements of SN54L00 TTL gate 74

X Operational amplifier definitions 79

XI 741-Type MIL-M-48510/101E specification 80

XII IC technology comparison 85

XIII Operational amplifier supplier-qualified part procurement specification example (741) 88

XIV Operational amplifier user-qualified part procurement specification example (741) 89

XV JFET supplier-qualified part procurement specification example (2N42220) . . . 97

XVI JFET user-qualified part procurement specification example (2N4220) 98

XVII Summary of supplier HA control levels. 100

XVIII Summary of user HA quality levels 103

1. INTRODUCTION

1.1 Objective and Scope

The objective of this document is to provide a cost-effective means of obtaining semiconductor bipolar active elements whose response to neutron radiation is within known and acceptable limits. The scope of this document is limited to hardness assurance (HA) procedures for the neutron environments for silicon bipolar transistors, zener diodes, TTL (transistor-transistor logic) digital integrated circuits (54/74 series), type 741 operational amplifiers, and junction field-effect transistors (JFET's).

1.2 How To Use This Document

This document addresses two problems: (1) what design guidelines should be used by design engineers for a cost-effective HA plan and (2) what HA controls should be specified in the obtaining of semiconductor pieceparts. Knowledge of the interaction of radiation with semiconductor devices and lot-sample statistical techniques are used to solve both problems. The statistical approaches to design and procurement are covered in Section 1.5. The effects of neutron radiation in each type of device covered in this document is given in the first subsection in each device section.

The concept of supplier and user HA controls is introduced in Sections 2 and 3 to separate the two problems of defining specifications for MIL-SPEC devices and calculating system survivability probabilities. In the first case parameters are identified that should be specified and controlled to reduce neutron response variability. In the second case methods are identified for calculating minimum lot quality levels based on a particular system-defined failure criteria.

1.3 Hardness Assurance For Pieceparts

Statistical information is used to determine the variability in the pre-irradiation characteristics and the subsequent radiation response of a population of parts. However, statistical data alone is inadequate in many cases to produce acceptable confidence and probability levels for part survival. In this document, an approach has been used which is centered around existing knowledge of the physical causes for neutron radiation effects on the important parameters of bipolar semiconductor devices. By examining the

existing knowledge base and constructing a model, it is possible to identify those parameters and screens of the device manufacturing process that control the radiation response. From this understanding a reasonable hierarchy of HA procedures can be formulated

For any specific piecepart application, a tradeoff exists between the magnitude of the design margin and the extent of parts control. If all parts respond in a similar way, one can design with very little margin; if the design has a large enough safety margin, very wide variations in parts characteristics can be tolerated. The optimum choice depends on the circuit requirements and should be determined by minimizing cost. For example, as the part variability is allowed to increase, the cost per part usually decreases; however, the number of parts required increases and the total cost will pass through a minimum. The fundamental requirement for an intelligent tradeoff analysis is the knowledge of the relationship between alternative choices for parts controls and their cost, and the resulting part population performance under operational stresses. This relationship can be established for each environment from empirical piecepart data and knowledge of the physical principles underlying electron device operation. Costs of different alternative design solutions are then estimated. From this tradeoff the optimum design margin and parts control can be determined.

1.4 Hardness Assurance Application To Systems

HA, hardness maintenance, hardness surveillance, hardness assessment, and hardness validation are all requirements which are placed on a system to insure that the system will perform its mission in spite of nuclear radiation stresses. The relative interaction of these terms is shown in figure 1. Hardness assurance is the procedure during the production phase that ensures that the production line end product is in accord with the hardened design and in compliance with nuclear specifications. Hardness maintenance is the procedure during the operational phase that ensures that the system's operational procedures, maintenance procedures, and aging characteristics do not degrade the system's operational capability below mission completion level. Hardness surveillance is the periodic test inspection during the operational phase that verifies the adequacy of the hardness maintenance program. Hardness assessment is the determination of a system vulnerability to nuclear

environments; hardness validation is a verification of system survivability in a nuclear environment. (These and other terms, with definitions, are listed in the glossary.)

The three reports required for HA documentation are represented by the three blocks at the upper part of figure 1: (1) the HA design guideline, (2) the HA categorization, and (3) the HA plan. The content of each of these volumes is listed below. This documentation requirement closely follows that outlined by Patrick and Ferry.[1]

The Hardness Assurance Design Guidelines (Volume 1) consists of the HA design margin restrictions, the statistical methods employed, the shielding factors, the derating factors, and can be organized as follows:

1. Hardness Assurance Documentation Requirements
2. Hardness Assurance Design Restrictions
3. Hardness Assurance Design Margins
4. Statistical Methods
5. Shielding Factors
6. Derating Factors.

Volume 2 of the documentation consists of the Hardness Assurance Categorization. This is a categorization of the circuits and pieceparts which are critical to mission completion in the environment of interest. For each circuit or part, the categorization includes a discussion of the radiation derating factor, the selection of critical parameters, the hardness confidence at Category 1 and 2 levels (see Section 3 for definitions of categories, the design criteria, the design techniques, the design margins, the methods for determining parameter limits, and the HA cost-benefit tradeoffs. Volume 2 can be organized as follows:

---

[1] R. Patrick and J. Ferry, Nuclear Hardness Assurance Guidelines For Systems With Moderate Requirements, Air Force Weapons Laboratory (September 1976).

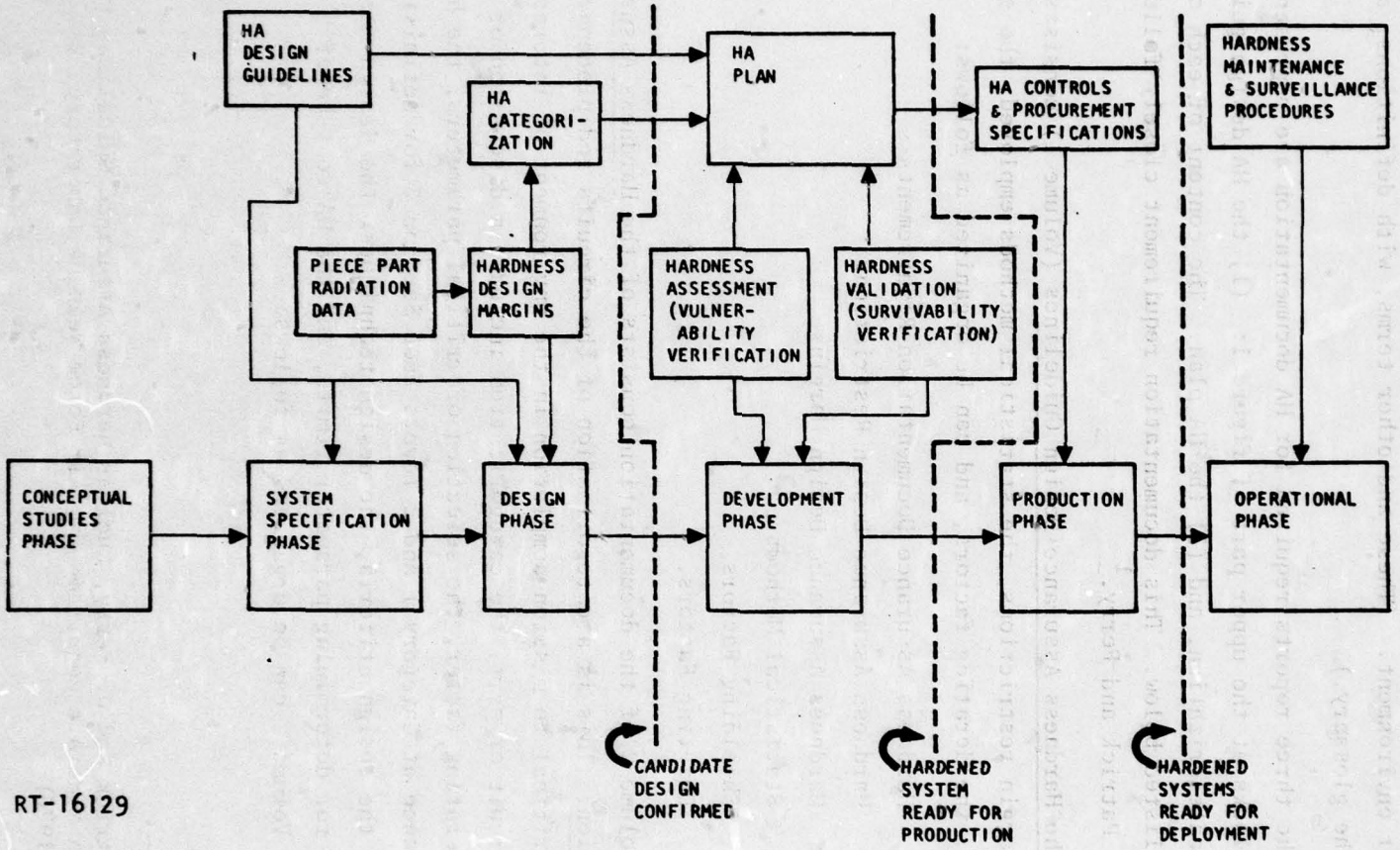


Figure 1. Hardness assurance (HA), hardness surveillance (HS), hardness assessment, and hardness validation flow diagram.

1. Mission-Critical Circuits*

    1.1 Category 1 Circuits
    1.2 Category 2 Circuits

2. Mission-Critical Pieceparts*

    2.1 Category 1 Pieceparts
    2.2 Category 2 Pieceparts

3. Piecepart Application and Location List

Volume 3 is the Hardness Assurance Plan. This includes the management controls as exemplified by the configuration control boards, parts control boards, or the quality control boards. Also included in the plan are the test procedures for radiation testing, electrical testing, and dosimetry. The pieceparts procurement specifications are also included in the plan, as are the necessary procurement procedures. HA controls listed in the plan are applied during the production phase as shown in the flow diagram. Volume 3 can be organized as follows:

1. Management Controls

    1.1 Configuration Control
    1.2 Parts Control
    1.3 Quality Control

2. Organizations

    2.1 Certification Organizations
    2.2 Parts Control Boards
    2.3 Configuration Control Boards
    2.4 Quality Control Board

3. Test Procedures

    3.1 Radiation Dosimetry Procedures
    3.2 Radiation Testing Procedures
    3.3 Electrical Testing Procedures

4. Piecepart Procurement Specification

5. Procurement Procedures

---

*The description must include a discussion of radiation derating factors, selection of critical parameters, hardness confidence at Category 1 and 2 levels, design criteria, design techniques, design margins, methods for determining parameter limits, and HA cost/benefit tradeoff for each radiation environment.

Hardness maintenance procedures and surveillance procedures are different; both are employed during the operational phase of the system, even though the documentation and plan for hardness maintenance and surveillance must be developed during the design, development, and production phases of the system.

1.5 Statistical Methods

Quality-conformance (lot sample) tests are performed with realistic environmental stresses on samples of devices. Since these tests are performed on random samples of devices, the results can be used to place statistical limits on the total device population. These tests can be degrading or destructive since the test devices may be rejected for use.

The use of quality-conformance testing means that some statistical sampling plan must be followed in order to obtain meaningful information. There are two general types of sampling plans: attribute sampling plans, and variable sampling plans.

Accept/reject criteria for attribute sampling plans are based on the individual device. An example of an attribute LTPD (Lot Tolerance Percent Defective) plan is given in Appendix B of MIL-M-38510D, "General Specification for Microcircuits." To illustrate the use of the LTPD plan, suppose we desire to find the required sample size for a lot size of 100 items with no rejects in the sample. If a 0.1 probability of accepting a lot of 100 with 20 defective units (LTPD = 20 % can be tolerated, Table B-2 in MIL-M-38510D yields a sample size of 10. The next step is to select 10 sample units at random from the lot of 100. If there are no values of the parameter greater than the critical value in the random sample of 10 units, then the lot of 100 is accepted with the realization that there is one chance in 10 that the lot may have 20 defective units.

Accept/reject criteria for variable sampling plans are based on sample statistics. For design margin statistical characterization, a variable sampling plan is preferred over an attribute plan because the sample sizes are smaller and a statistical data base is generated. The variable sampling plan discussed next will result in a cost-effective approach to HA using adequate design margins.

1.5.1 Lot Statistical Characterization For Design Margin Calculations

The variable sampling plan discussed in this section uses one-sided statistical tolerance limit factors for a normal distribution to place confidence limits on population parameter estimations. The resulting probability charts allow cost-effective HA decisions to be made by design engineers, project officers, and procurement officers.

The first step in any statistical quality-conformance test is to select the device parameter which is critical to the circuit function and which can be related to the specified radiation environment of the system. For the statistics which follow, the parameter must also be characterized by a normal distribution. An example of a device parameter which meets these requirements is the logarithm of the damage factor (K_D) for bipolar transistors in a neutron environment. Since K_D has a lognormal distribution, the logarithm of K_D will have a normal distribution.

The following is a step-by-step procedure and example calculation of lot worst-case probability at 90 % confidence for one lot of 2N2222 transistors measured at an I_C of 10 mA and a V_{CE} of 5 V.

(1) Calculate $\ell n K_D$ for a sample of 10 devices over 3 neutron fluences from[2]

$$1/\beta_\phi = 1/\beta_o + K_D \Phi$$

where β_ϕ is the post-irradiated common emitter current gain, β_o is the pre-irradiated value, Φ is the neutron fluence, and K_D is the composite neutron damage factor. In practice $(1/\beta_\phi - 1/\beta_o)$ is plotted versus Φ over at least three data points and the straight line fit to the data is the value for K_D.

---

[2] G. C. Messenger and E. L. Steele, Statistical Modeling of Semiconductor Devices for the TREE Environment, IEEE Trans. Nucl. Sci. NS-15 (December 1968), 133.

(2) Order the ℓnK_D data as in table I, and plot the data on normal probability paper as in figure 2. Draw a straight line through the data. If the data fits a straight line, the parameter has a normal distribution.

(3) Calculate the lot worst-case values at the X_{80}, X_{90}, X_{99}, $X_{99.9}$, and $X_{99.99}$ points from

$$L_\sigma = sK_{TL} + m$$

where m is the sample mean (the point in the sample data line at 50 %) and s is the sample standard deviation calculated from[3]

$$s = \frac{X_{93.3} - X_{6.7}}{3}.$$

$X_{93.3}$ and $X_{6.7}$ are the values of the sample line at the 93.3 % and 6.7 % points. The fitted line of figure 2 yields a mean of -36.28 and a standard deviation of 0.20. L_σ is calculated from figure 3, given that N is 10, by obtaining the quantity K_{TL} from figure 3 at the X_{80}, X_{90}, X_{99}, $X_{99.9}$, and $X_{99.99}$ points. The resulting L_σ values are calculated in table II and plotted in figure 4.

K_{TL} is obtained from tables of one-sided tolerance limit factors for a normal distribution.[4] It is a factor such that for 90 % confidence at least some proportion of the distribution will be less than $m + K_{TL}\sigma$, where m and σ are estimates of the mean and the population standard deviation compared from a sample of size N.

---

[3] J. R. King, Probability Charts for Decision Making, Industrial Press (1962).

[4] A. J. Duncan, Quality Control and Industrial Statistics, R. D. Irwin, Inc. (1959).

TABLE I. CUMULATIVE FREQUENCY STATISTICS OF ℓnK_D FOR ONE LOT OF 2N2222 TRANSISTORS MEASURED WITH I_C OF 10 mA AND V_{CE} OF 5 V

	Pre-Irradiation	$h_{FE\Phi}$ at fluence Φ			K_D		%
		5.2×10^{12}	2.5×10^{13}	1.3×10^{14}	$(\times 10^{-16})$	ℓnK_D	Cumulative Distribution (1)
1	241	202	125	47	1.3	-36.6	9.1
2	151	138	84	38	1.4	-36.5	18
3	220	184	111	42	1.4	-36.5	27
4	160	137	96	37	1.5	-36.4	36
5	188	152	100	36	1.7	-36.3	45
6	200	166	100	36	1.7	-36.3	54
7	147	123	84	32	1.8	-36.3	64
8	178	150	100	31	1.9	-36.2	73
9	142	121	78	30	2.0	-36.1	82
10	166	137	85	31	2.0	-36.1	91

(1) Calculated from n/N+L = n/11

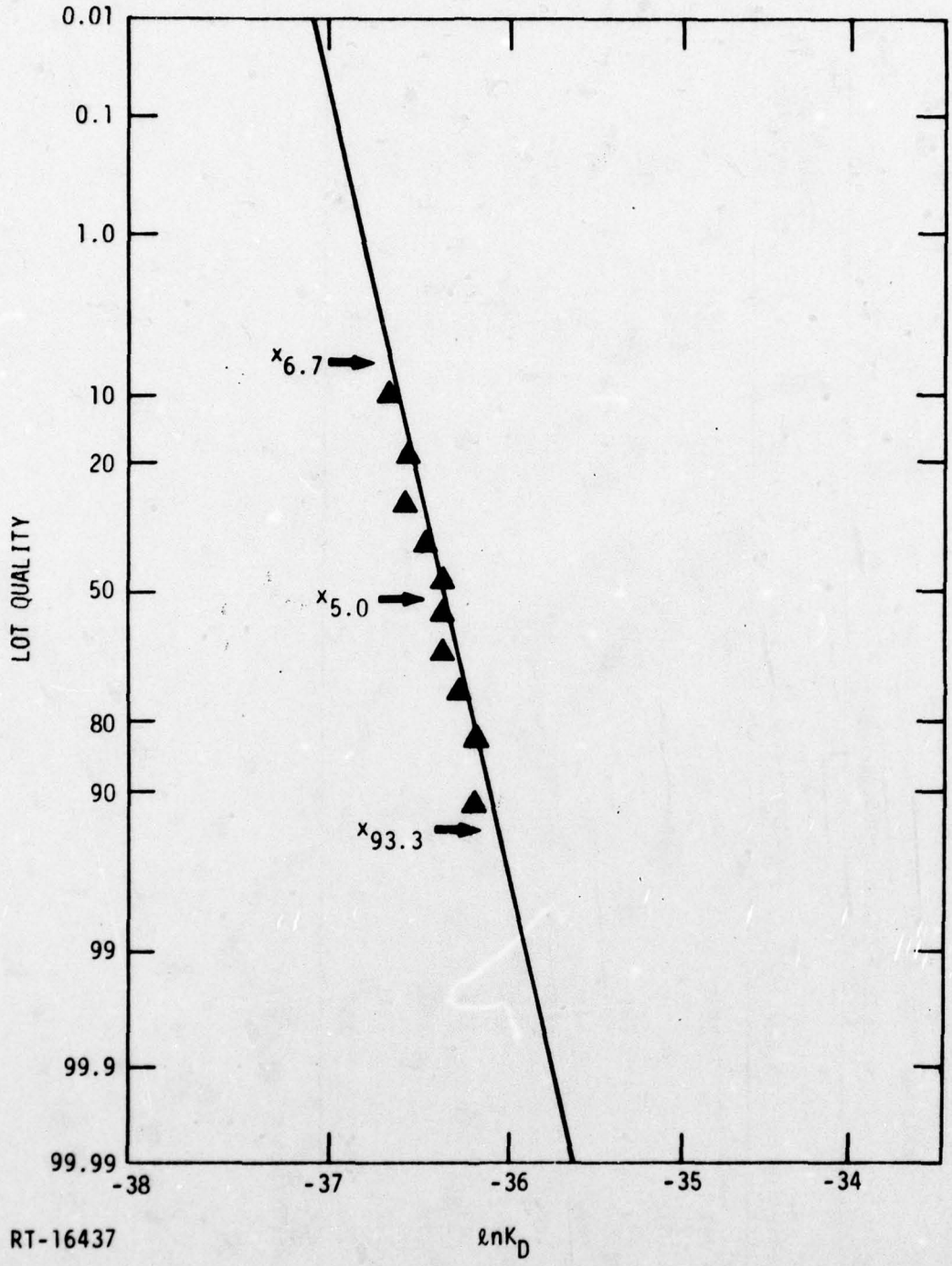


Figure 2. Cumulative frequency ℓnK_D data for the 2N2222.

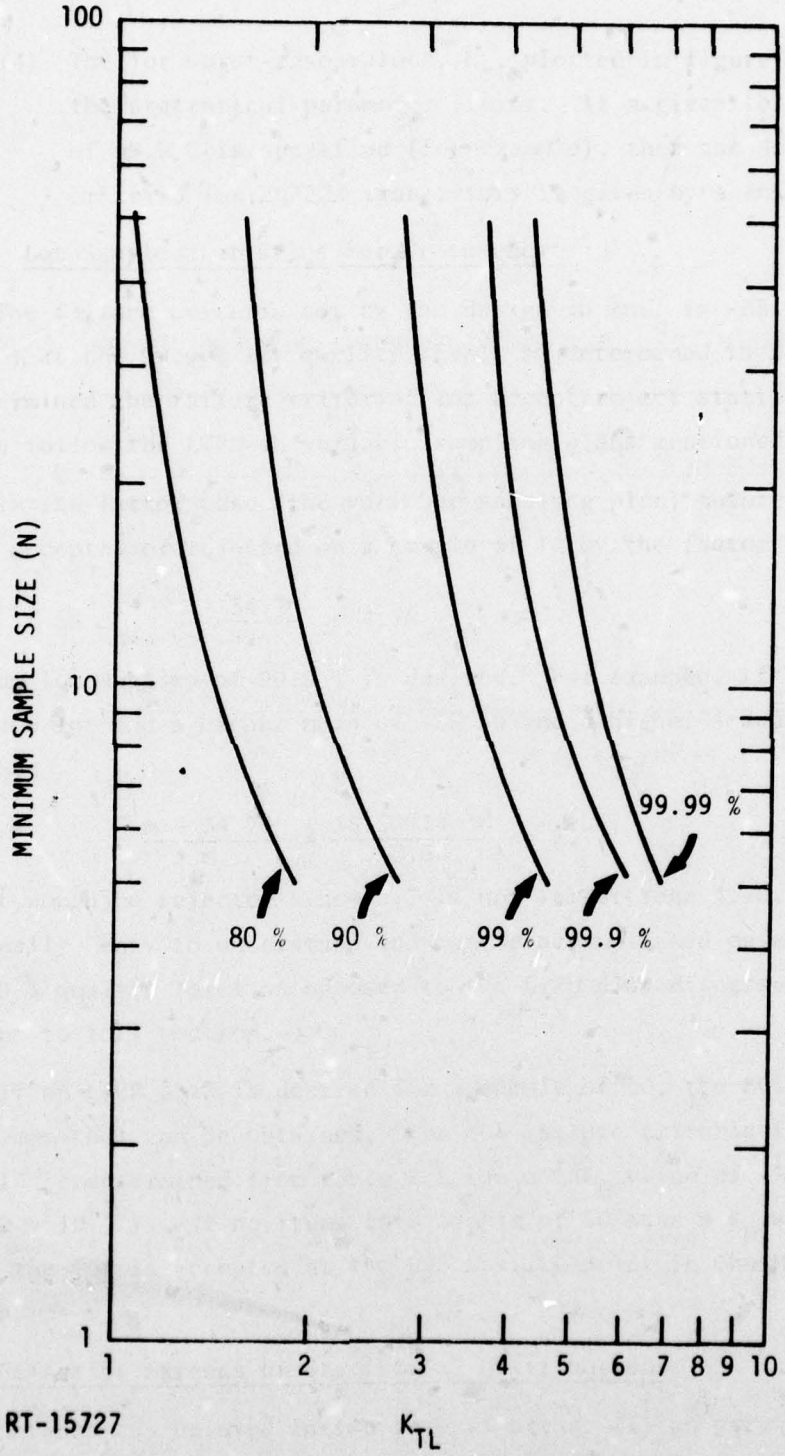


Figure 3. One-sided tolerance limit factors (K_{TL}) for normal distributions at 90 % confidence.

TABLE II. CALCULATION OF WORST-CASE ℓnK_D VALUE

Lot Quality %	K_{TL}	L_σ (1)
80	1.40	-36.00
90	2.10	-35.86
99	3.60	-35.56
99.9	4.70	-35.34
99.99	5.40	-35.20

(1) $L_\sigma = sK_{TL} + m$

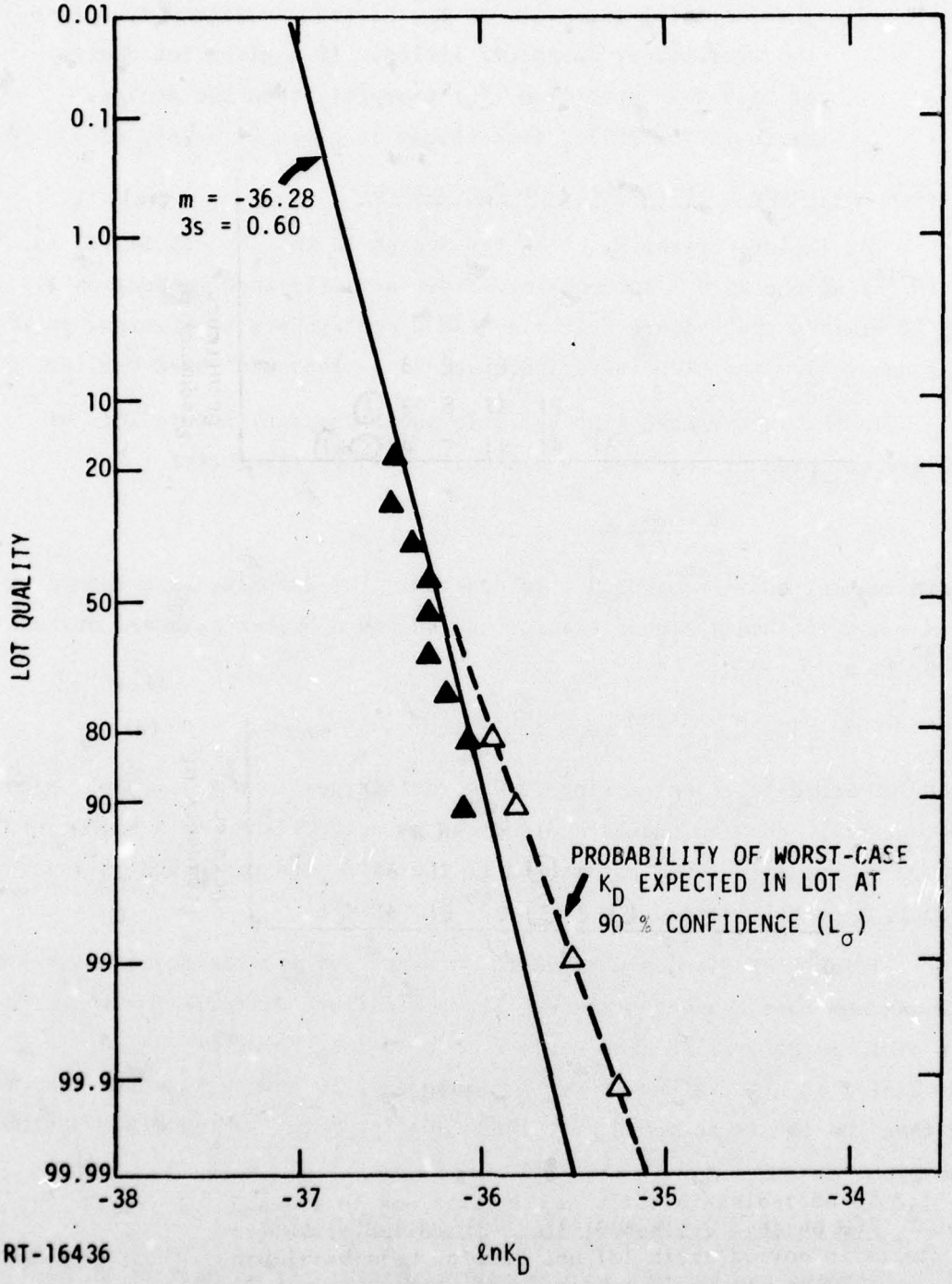


Figure 4. Lot worst-case values and cumulative sample data for 2N2222.

(4) The lot worst-case values, L_σ, plotted in figure 4, define the statistical parameter limits. If a given lot quality of 99.9 % is specified (for example), then the design criteria for 2N2222 transistors is given by a ℓnK_D of -35.34.

1.5.2 Lot-Sample Statistics For Procurement

The failure criteria set by the design in ℓnK_D is -35.34 (K_D is 4.5×10^{-16}) at the 99.9 % lot quality level, as determined in Section 1.5.1. Having determined the failure criteria, lot accept/reject statistical procedures can follow the LTPD in variable sampling plans mentioned earlier.

In the latter case (the variable sampling plan) future lots of 2N2222 are accepted or rejected on a sample of 10 by the factor

$$\frac{m - 34.70}{s} \geq 4.70 \quad ,$$

if a minimum lot quality of 99.9 % is desired. For example, if a sample of 10 from a new lot had a higher mean of -35.50 and a higher standard deviation of 0.30, then

$$\frac{m - 34.70}{s} = \frac{35.50-34.70}{0.30} = 2.7$$

and the lot would be rejected since 2.7 is not larger than 4.70. This plan is conceptually easy to understand and can be accomplished on a sample of 10 at the 99.9 % quality level as opposed to the LTPD plan discussed in the introduction to this section.

If an LTPD plan is desired for a sample of 10, the 80% quality level is the maximum that can be obtained. The 80% failure criteria for the LTPD sample of 10 is determined from table 2 to be a ℓnK_D value of -36.00 (K_D is 2.32×10^{-16}). If no items in a sample of 10 have a K_D worse than this value then the lot is accepted at the 80% quality point in the MIL-M-38510D sample plan.

1.6 Effect of Screens on Statistical Distributions

Screens can be used in two general areas: (1) as part of an HA plan to alter a piecepart distribution, or (2) as a hardening technique to truncate a distribution.

Screening as part of an HA plan to alter a distribution is demonstrated in figure 5. Suppose the pre-irradiation distribution of f_T is given by figure 5(a), where the devices are numbered in ascending order of f_T. Suppose the post-irradiation distribution of these devices is given in figure 5(b). Note that in figure 5(b) the devices are not in order; hence, the screen f_T is not perfectly correlated with K_D. However, a screen on f_T could remove devices 1, 2, and 3, thus altering the distribution of K_D by reducing the mean. Also, the standard deviation of K_D would be reduced. Thus it can be seen that perfectly correlated screens are not required to alter a distribution. In fact, practically any measurement which is correlated to some degree with radiation can be useful as an HA screen.

As another example, consider the correlation between the pre- and post-irradiation $V_{CE(SAT)}$ in figure 6. The "T" devices had the highest pre-irradiation value and, as can be seen, if they had been pulled from the lot by a screen the post-irradiation "tail" would have been eliminated.

Screening as a hardening technique to truncate a distribution is demonstrated in figure 7. The K_D data shows a normal distribution before screening. A screen on K_D to remove all devices beyond point A will truncate the distribution at point A. Radiation hardening by screening to identify only the hardest parts in the lot appears to be useful only as a last resort. It is usually much more cost-effective to use device substitution to obtain a harder system.

2. HA PLAN FOR SUPPLIER - QUALIFIED PARTS

HA can be applied by two groups: (1) the supplier (manufacturer) who is interested in part qualification to MIL-Standard specification and (2) the user who is interested in part selection and procurement for a specific system application. The supplier is defined to be the manufacturer, testing contractor, or any other organization which qualifies parts for more than one specific system application. This means that the supplier wants to control the radiation response of all those parameters which are of importance in many different applications.

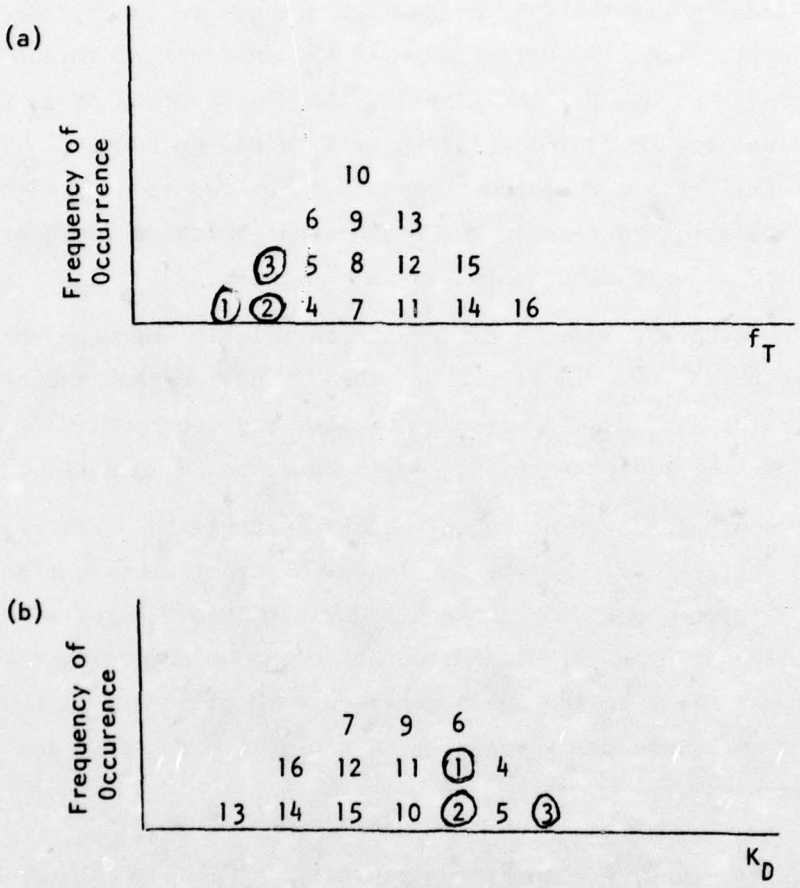


Figure 5. Example of how screens can alter distribution of K_D; (a) distribution of f_T of 16 devices ordered by pre-irradiated values, and (b) distribution of K_D of 16 devices after irradiation.

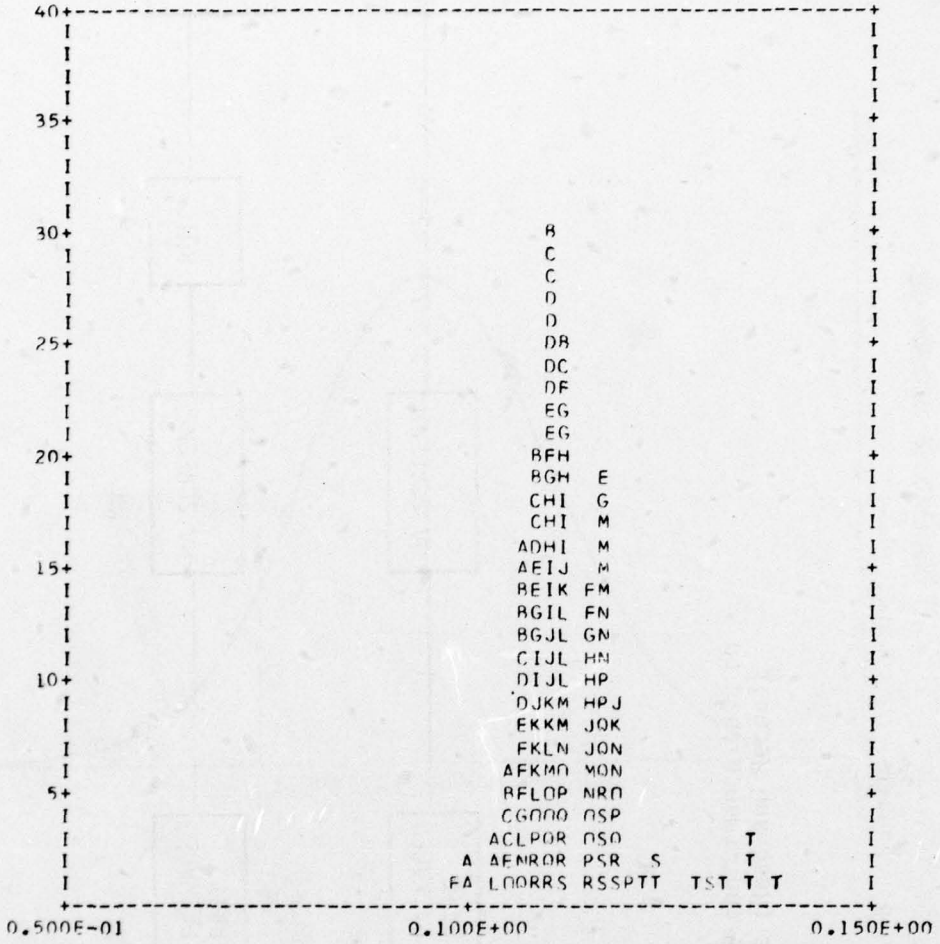


Figure 6. Histogram of $V_{CE(SAT)}$ at fluence of 0.310E+15 and an I_E of -0.120E+-2 and an I_B of 0.200E+01 for the 2N5399 on a sample of 156 devices.

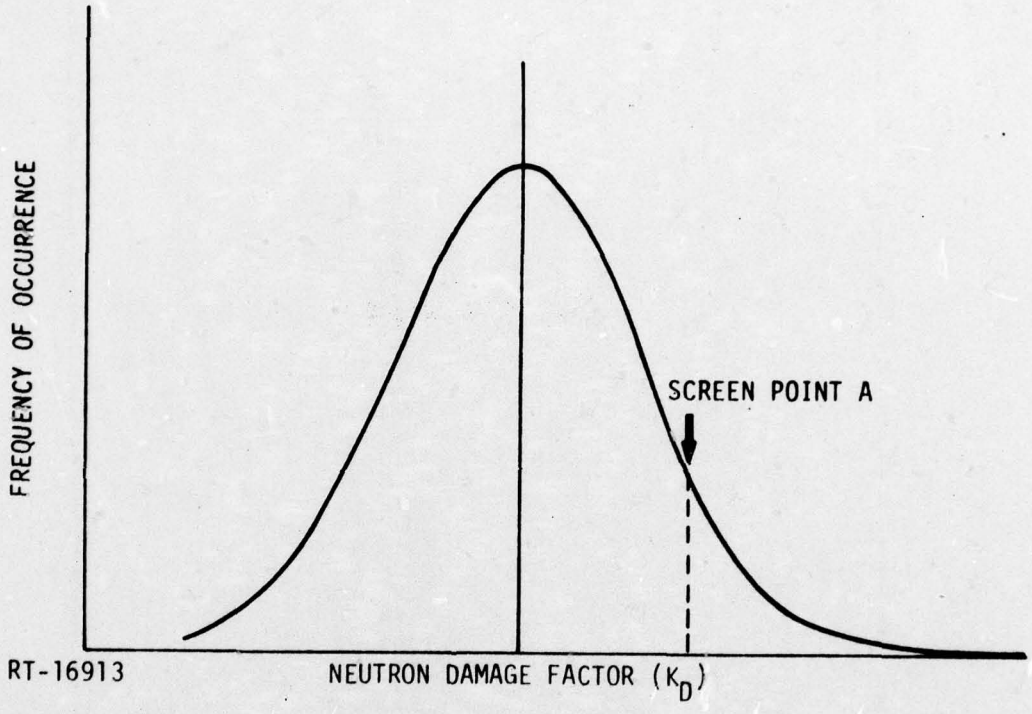


Figure 7. HA screen effectiveness demonstration.

For the supplier, HA control levels are defines as follows:

S-1 (Control Level 1)

Process Controls + Screens + Radiation Characterization Test Data (Read and Record)

S-2 (Control Level 2)

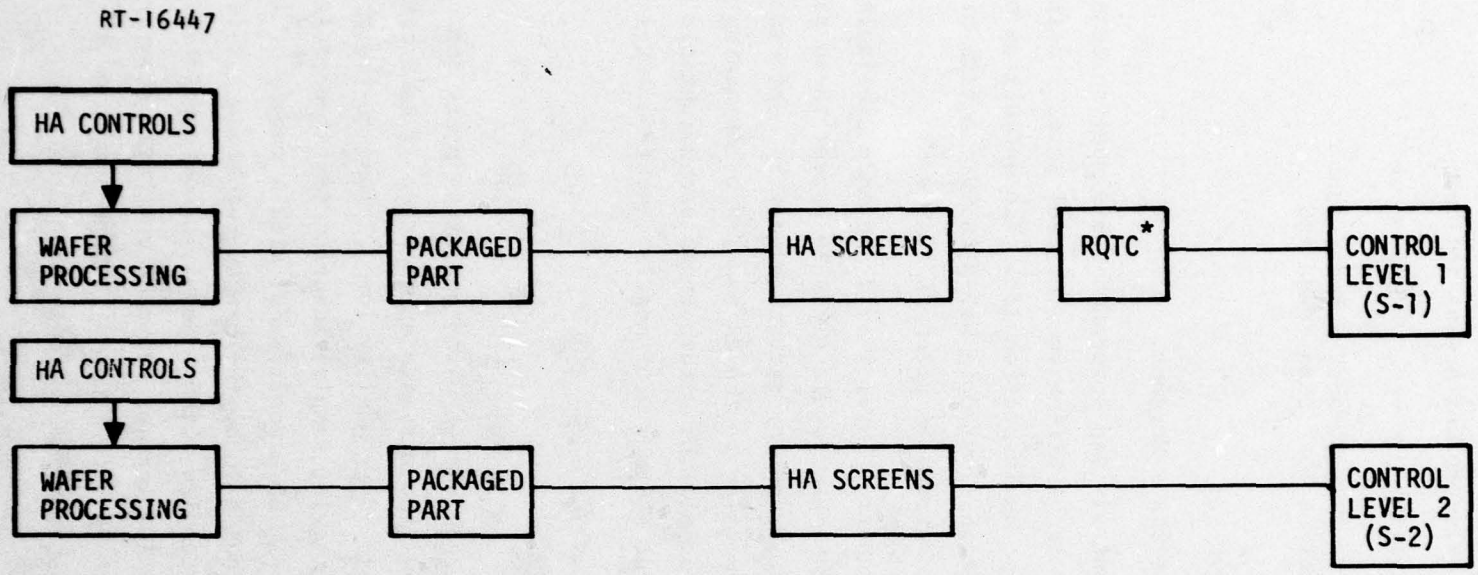
Process Controls + Screens.

Control level 2 calls for process controls and screens because most screens need some degree of process controls to be effective. Control level 1 calls for the addition of radiation tests on an inspection lot. The definition of an inspection lot follows the definitions listed in MIL-M-38510. A flow diagram for the two levels of supplier controls is given in figure 8.

If supplier-qualified parts at control level 1 or 2 are made available by the manufacturer to the user, then a user could elect to accept these parts without going through any additional screens or radiation quality conformance testing. This is a cost-effective solution to the HA problem of obtaining quality parts whose radiation response will be within known and acceptable limits for a large number of different systems with moderate neutron level environments.

3. HA PLAN FOR USER-QUALIFIED PARTS

The user is defined to be the organization which qualifies parts for a specific system. Since the user knows the ultimate application of each part, the user HA levels are quality levels. User quality level 2 imposes those HA controls (process controls, screens, lot sample radiation tests) necessary to achieve minimum 80 % lot quality (at 90 % confidence) with a sample of 10 devices. The 80 % lot quality was chosen to be the breakpoint because this qualify level can be achieved by 10 samples without requiring extrapolation of the statistics. User quality level 1 imposes those HA controls necessary to achieve lot quality above 80 % (at 90 % confidence) with a sample of 10 devices. These requirements can be summarized as follows:



*RQCT - Radiation quality conformance test on an inspection lot (Read and Record)

Figure 8. Supplier HA control levels.

U-1 (Quality Level 1)

Hardness Assurance controls necessary to achieve lot quality above 80% with a sample of 10 devices

U-2 (Quality Level 2)

Hardness Assurance controls necessary to achieve minimum 80% lot quality with a sample of 10 devices.

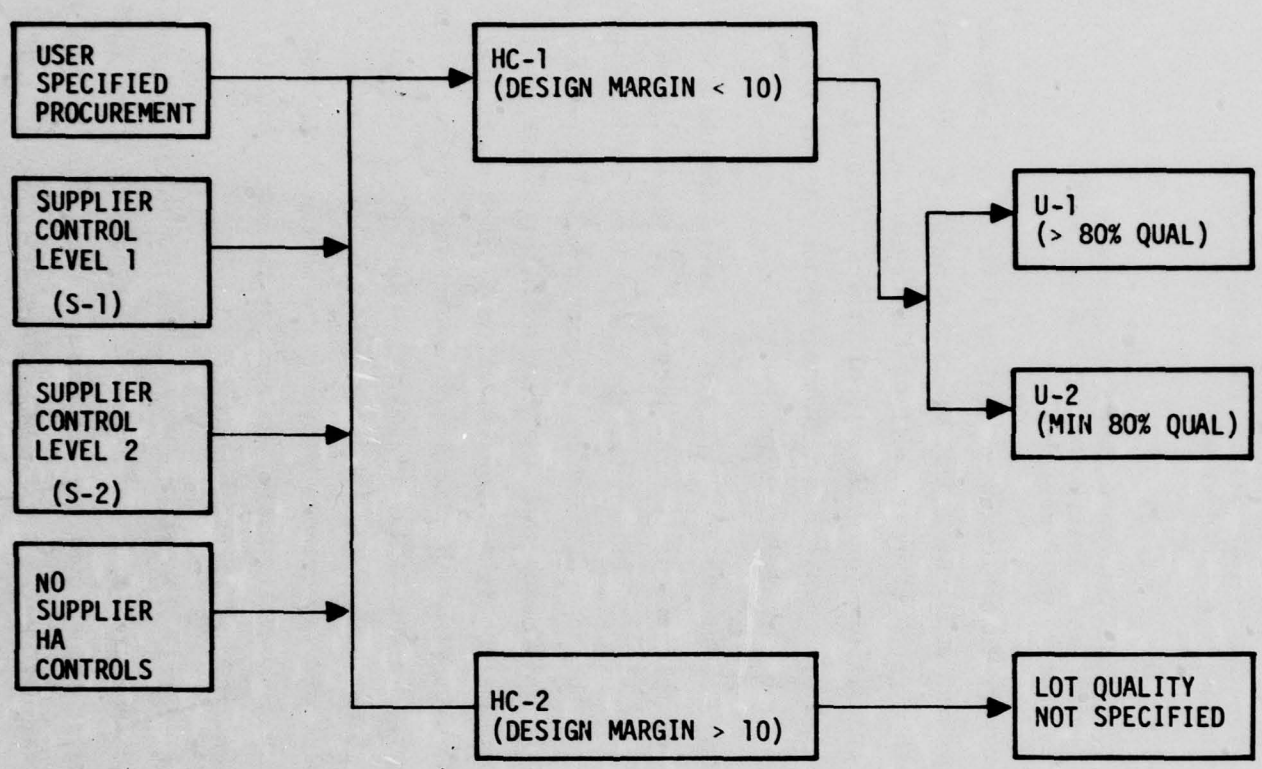
The HA controls necessary to achieve user quality level 2 or 1 depends on the type of device involved and the amount of data available. For parts from a mature process with a good physical model of the neutron effects (mature process bipolar transistors for example), electrical screens alone can provide user quality level 2 as a minimum and probably reach quality level 1, depending on the choice of the failure criteria.

An HA user flow diagram is presented in figure 9. Parts are obtained from the supplier at one of the various control levels. If the design margin (or safety margin) is a factor of 10 or greater for the neutron environment, then no HA controls need to be imposed. The design margin of 10 for transistor small-signal applications means that the mean of a lot sample of 10 devices irradiated at 10 times the system specification fluence meets the circuit failure criteria. Note that this is a safe operating margin only for bipolar transistors operated in the linear region in a neutron environment. For other devices which do not have a good physical model of the neutron effects (operational amplifiers for example), the design margin of 10 is based on the population 99.9 % quality point (instead of the mean) at a neutron fluence of 10 times the specification fluence.

If the design margin is less than 10, then HA controls need to be imposed to insure lot quality and the part is designated as a Hardness Category 1 (HC-1) device. Depending on the HA controls imposed and the choice of the parameter failure criteria, user parts are obtained at quality levels 1 or 2.

For HC-1 bipolar transistors, process controls on the base width and base doping, together with electrical screens on h_{FE} and f_T, will reduce the variation encountered in the neutron radiation response of the composite damage factor K_D. A neutron radiation lot sample test on a sample of 10 devices will

RT-16446



HC - Hardness (Assurance Procurement) Category

Figure 9. User (U) HA quality level flow diagram.

yield lot quality at level 1 or 2 for failure criteria (L) at 90 % confidence using the variable sample statistical plan discussed in section 1.

4. HA CONTROLS FOR BIPOLAR TRANSISTORS

4.1 Effects of Neutron Radiation on Bipolar Transistors

4.1.1 Small-Signal (Linear) Operation

There are three major base current contributions to gain degradation of transistors used as small-signal amplifying devices (figure 10): (1) minority carrier recombination of the base region (I_{RB}), (2) a mechanism related to the emitter efficiency of the transistor (I_D') and (3) recombination-generation in the emitter-base depletion region (I_{RG}). In NPN transistors, I_{RB} reduces the number of electrons reaching the collector from the emitter through recombinations in the base region. Since a recombination requires an electron and a hole, the base contact must supply additional holes to preserve space charge neutrality in the base region (figure 10). Therefore, this component of base current increases; this increase results in a reduction of the gain. I_{RB} is dependent on the square of the base width and inversely dependent on the minority carrier lifetime and diffusion constant in the base region. Narrow base widths minimize the effects from this mechanism.[5]

The increase in base current which can be related to the emitter efficiency is known as I_D'. Emitter efficiency is defined as the ratio of the current injected into the base region divided by the total current across the emitter-base junction. As the reverse diffusion current (holes diffusing from the base into the emitter) increases, the base contact must supply additional holes to the base to maintain space charge neutrality which results in an increase in the base current. The contribution of the ratio between the reverse diffusion current and the forward electron diffusion current is proportional to the ratio of the sheet resistivity of the emitter and base regions. For maximum efficiency and hence higher gains, the sheet resistance of the base region should be as large as possible with respect to the

[5]A. R. Hart et al., Parameter Sensitivities for Hardness Assurance: Displacement Effects in Bipolar Transistors, Final Report, Mission Research Corporation Report MRC/SD-R-20 (December 1977).

RT-16443

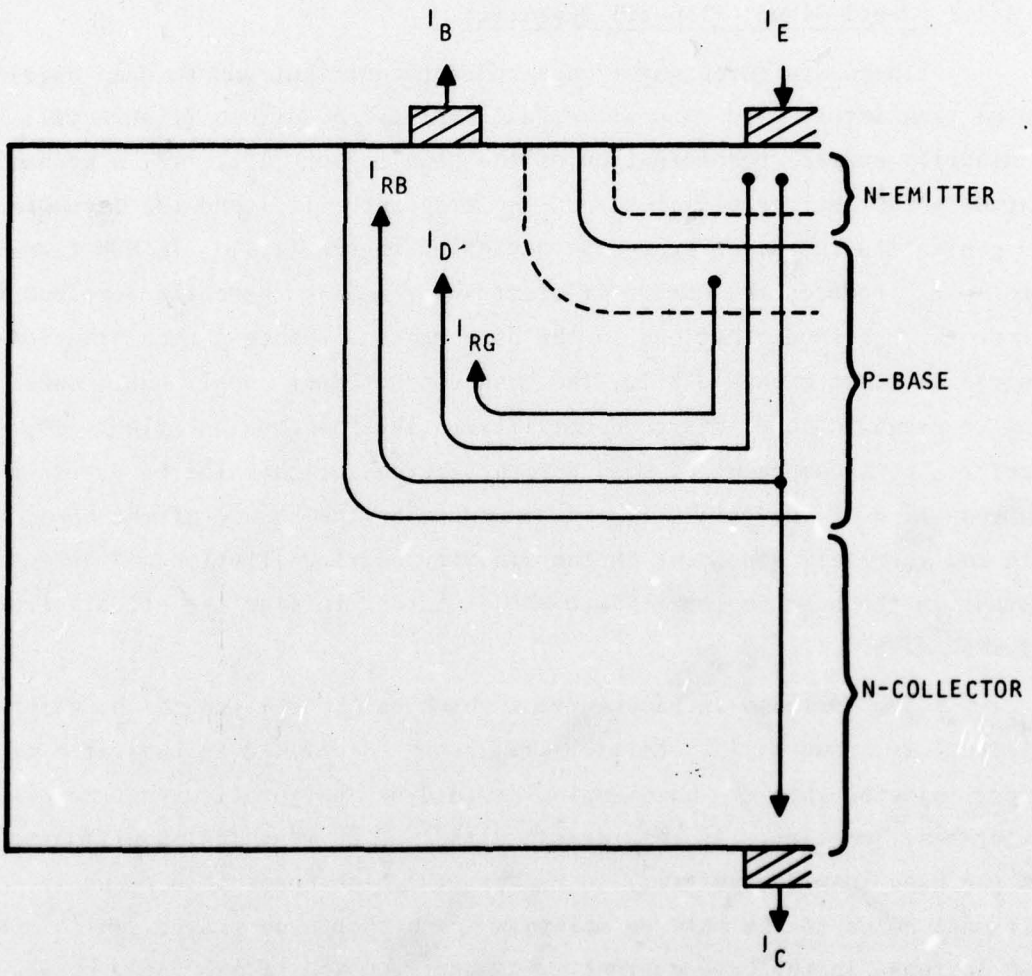


Figure 10. Transistor base current components.

sheet resistance of the emitter region. In other words, the emitter should be much more highly doped than the base. Other design problems, such as base push-out, limit the extent to which this principle can be implemented.

The other important base current contribution is the generation-recombination current in the emitter depletion region, I_{RG}. This current is the result of recombination-generation of electrons and holes in the emitter-base depletion layer. In a junction at thermal equilibrium, the net recombination rate equals the net generation rate. When a forward bias is applied, the carrier concentration rises, and thus, the recombination rate rises; this rise requires that the base contact supply more current (holes).

In a complete transistor model, there are two other contributions to the reduction of transistor gain. One of these, I_{CBO}, the collector-base junction leakage, represents the hole current which flows from the collector to the base with the emitter considered as open circuited. The mechanism is similar to that of I_{RG}, except for the reverse bias condition. This current only becomes significant at very low emitter currents, where I_{CBO} contributes a major portio of the effects on gain. It will not be considered in this analysis.

The other contribution which will not be considered is the surface-recombination current I_S. This contribution is the result of recombination of holes and electrons at the surface. The major relative significance of this term occurs at low injection levels. The change in this term is not significant for neutron displacement damage effects and hence will not be considered in this analysis.

The transistor β degradation equation relating decreases in common emitter current gain (β) to neutron exposure is given by[6]

$$\frac{1}{\beta_\phi} = \frac{1}{\beta_o} + K_D\phi \quad ,$$

where β_o is the pre-irradiated common emitter gain, β_ϕ is the post-irradiation

---

[6] G. C. Messenger, Hardness Assurance Considerations for the Neutron Environment, IEEE Trans. Nucl. Sci. NS-22 (December 1975), 2308.

common emitter current gain, K_D is the neutron damage factor, and ϕ is the neutron fluence. This equation predicts a linear dependence for the delta reciprocal β upon fluence. It is generally observed that this linear dependence occurs in experimental data; hence, knowing the neutron damage factor at a given fluence, a reasonable prediction of transistor gain degradation at another neutron fluence level can be made at fluences up to 10^{15} n/cm^2. The linear dependence of delta reciprocal β is caused by the predominance of the minority carrier lifetime degradation mechanism over the carrier removal and mobility degradation mechanisms. Above 10^{15} n/cm^2 this dependence starts to become nonlinear as carrier removal starts to become a more important mechanism.

The neutron damage factor K_D is sometimes considered to be an effective composite damage factor. K_D is related to K_S, the silicon damage constant, through the equation $K_D = K_S/(2\pi f_T)$ where f_T is the transistor gain-bandwidth product. K_S is a function of injection level and resistivity. At normal transistor operating levels and base resistivities K_S has the value 6.3×10^{-7} cm^2/ns.[5] K_D is a function of collector current and voltage (because f_T is a function of voltage).

The effects of permanent gain degradation can be minimized by operating the transistor at higher levels of emitter current. There are two reasons for this: (1) the minimum in the damage factor (K_D) occurs at higher collector currents, and (2) the recombination-generation term is negligible at higher collector currents. Thermal variations have also been shown to influence the resulting neutron effects.[5] For ambient temperature greater than room temperature, decreased effects are noted which are probably caused by thermal annealing. Therefore, characterization for passive device conditions and devices assumed to be irradiated at 25°C will produce a worst-case estimate of the effect of neutron displacement damage on bipolar devices. This report considers only neutron irradiation on devices with no applied biases during irradiation and room temperature conditions existing for all measurements.

---

[5]A. R. Hart et al., Parameter Sensitivities for Hardness Assurance: Displacement Effects in Bipolar Transistors, Final Report, Mission Research Corporation Report MRC/SD-R-20 (December 1977).

The process-related parameters which contribute to the composite damage factor are the base width, the base doping, the emitter area, and the collector doping. A sensitivity analysis[5] reduces this list to the base width and the base doping. Effects on the damge factor from variation in emitter area and from variations in collector doping are generally less than the effects produced by varying the base width and the base doping. For this reason, process controls for HA purposes on transistors should consist of controls on the base width and the base doping.

The transistor terminal electrical parameters that correspond to the four physical parameters above are the peak value of the gain-bandwidth product (f_T), the minimum emitter-base breakdown voltage (BV_{EBO}), the maximum input capacitance (C_{ib}), and the minimum collector-base breakdown voltage (BV_{CBO}). For transistors operated as small-signal amplifiers, the most effective electrical screen appears to be a screen on $f_{T(MIN)}$. While this screen will have some effect on the HA of the transistors, an even more dramatic effect can be realized by the imposition of process controls on the base width and the base doping (in that order). For example, if the base width and the base doping are both allowed to increase by 10 %, the resulting influence on the damage factor is predicted to be an increase of 22 %.[5]

The important process controls for neutron degradation and their related terminal parameters are summarized as:

Process controls	Terminal parameters which monitor process controls
Upper bound base width (W_b)	Minimum gain bandwidth product (f_T)
Upper and lower bounds base doping	Minimum emitter-base breakdown voltage (BV_{EBO})
	Minimum collector-base breakdown voltage (BV_{EBO})
Upper bound on emitter area	Maximum input capacitance (C_{ib})

[5] A. R. Hart et al., Parameter Sensitivities for Hardness Assurance: Displacement Effects in Bipolar Transistors, Final Report, Mission Research Corporation Report MRC/SD-R-20 (December 1977).

4.1.2 Power Operation

Power bipolar transistors are similar to small-signal bipolar transistors except that they possess much larger total area and operate at higher currents (and most often at high current densities). Power transistors generally operate at collector current levels higher than the maximum β point. Small-signal devices, on the other hand, operate either at the maximum β or below this optimum region. Higher current densities also mean that adequate derating with neutron dose must be taken into account in circuit design in order to allow for increase power dissipation with increased saturation collector-emitter voltages [$V_{CE(SAT)}$].

Emitter crowding is more likely to occur in power devices because of the higher collector currents which these devices require. In the construction of an epitaxial bipolar transistor, the base contact is positioned at the surface of the base region. As a result, there is a finite resitance difference from the base contact to various points under the emitter diffusion. The base current that flows from the base contact to the base region under the emitter produces a voltage gradient over this base region. The maximum potential occurs farthest from the base contact. If the external emitter-bias voltage is assumed to be applied uniformily over the entire base-emitter junction, then the effect of the internal base voltage is to produce a net junction potential that decreases from the periphery to the center of the emitter. The higher edge forward potential causes a crowding of the injected emitter current into the peripheral areas of the emitter well, which results in an effective reduction in the active cross-sectional area. The internal base bias may be such that the injected carrier density in the center of the emitter junction may actually be almost zero. Any resultant increase in the base current produced by neutron bombardment further aggravates this current-crowding effect and thus complicates the analysis of gain degradation.

One of the most severe limitations in making radiation-resistant power transistors arises because of the increased area required. The larger area needed to handle the higher power levels reduces the gain-bandwidth product of the transistor, which is directly proportional to failure threshold. More importantly, the large area reduces the yield of power transistors

in production. High-voltage operation also compounds the neutron resistance problem for bipolar transistors because of the light doping needed to achieve it. A hardened power transistor is difficult to achieve above 60 to 75 V.

4.1.3 Switching Operation

The parameter $V_{CE(SAT)}$ is given by[1]

$$V_{CE(SAT)} = I_C R_S + \frac{kT}{q} \ln \left[\frac{\alpha_I (1-\beta_F/\beta_o)}{1+\beta_F(1-\alpha_I)} \right]$$

where β_F is the circuit forced β, α_I is the inverse common base gain, and R_S is related to the collector resistivity. This equation works but is not used in everyday S/V neutron degradation calculation because its use requires the measurement of α_I (and its damage constant), which is difficult. The α_I parameter is the most sensitive parameter in this equation (for neutron effects) because it is related to minority carrier lifetime degradation. The S/V evaluation of a transistor is usually made based on β_F and β_o (the "normal" transistor gain) to determine when the transistor will come out of saturation. This is the approach used in the example in section 4.6.

For logic devices in a moderate neutron environment a transistor will come out of saturation when the common emitter current gain of the unit is degraded to the point where it equals or is less than the forced β imposed by the circuit. This effect can be minimized, however, by increasing base drive. Increasing the base drive, however, has the undesirable side effect of increasing the turn-off time. High-speed hardened logic therefore requires a compensation technique, such as a speedup capacitor across the base drive resistor, to maintain an adequate switching time.

Bipolar transistors operated as switches are required to pass a considerable amount of current. As a result of this large current, emitter crowding, discussed in the previous section, sometimes occurs. Emitter crowding is the major cause for gain roll-off at high currents. If a high collector current is to be used, then certain techniques such as an

---

[1] F. Larin, Radiation Effects on Semiconductor Devices, John Wiley, 1968.

effective area ratio (EAR) would need to be implemented to model the effect.[5]

In a few situations, gain is of less importance than the parameter $V_{CE(SAT)}$ (the collector-to-emitter saturation voltage). The effect of neutron damage on $V_{CE(SAT)}$ at neutron fluences above $\sim 10^{15}$ n/cm^2 is to increase this parameter by increasing the bulk resistivity of the transistor. In theory, three components determine the saturation voltage: The junction saturation voltage and two ohmic voltage drops in the emitter and in the collector regions. The emitter resistance is usually very small when compared with the collector because of the high doping in the emitter region and hence it is usually neglected. Note that the lowering of the net impurity concentration by neutron displacement damage does not occur until relatively high fluences. The measured values of the carrier removal rate range between 1 and 4 carriers per n/cm. Therefore, fluences of 10^{14} n/cm^2 and above are required for greater than 1 % changes in the net doping concentrations in the net base or emitter of most devices. Thus, effects from resulting changes in net impurity concentrations in moderate neutron environments are minor.

4.2 HA Controls for Supplier Qualified Parts

For supplier-qualified parts, transistor HA controls (levels 1 and 2) can be broken down into three general areas: Process controls, screens, and quality conformance tests. To produce a supplier-qualified part (see figure 8 and table 2 for definition), which is the objective of this program, the HA controls mentioned above must be imposed on the supplier. These controls are implemented through a procurement specification. An example of a supplier transistor procurement specification (using the 2N2222) is given in table 3.

4.2.1 Process Controls

The neutron-sensitive transistor model developed as a result of this program[5] has identified two processing parameters which should be monitored for neutron HA. These two parameters are the base doping level (N_A) and the base width (W_B). Configuration control must be added also. All

---

[5] A. R. Hart et al., Parameter Sensitivities for Hardness Assurance: Displacement Effects in Bipolar Transistors, Final Report, Mission Research Corporation Report MRC/SD-R-20 (December 1977).

Table III. TRANSISTOR SUPPLIER-QUALIFIED PART PROCUREMENT SPECIFICATION EXAMPLE (2N2222)

HA controls	Parameter	Test method	Test conditions	Control level failure criteria (S-2)	Control level failure criteria (S-1)	units
Process controls	Base Width	(3)	-	+10%	+10%	μm
	Base Resistivity	(3)	-	+10%	+10%	cm^{-3}
	Configuration	-	-	-	-	-
Screens[1]	MIN h_{FEO}	ASTM-F528-77T	I_C = 10 mA V_C = 10 V	>75	>75	-
	MIN f_T	750B-3306	I_C = 20 mA V_{CE} = 20 V f = 100 MHz	>250	>250	MHz
Radiation[2] quality conformance test	K_D		I_C = 10 mA V_{CE} = 10 V	-	(3)	cm^2/n

Notes: (1) Failure criteria for screens are identical to slash sheet or manufacturer specifications.

(2) Radiation tests are read and record on 10 samples at three neutron levels which cause 20%, 50%, and 80% degradation in $1/h_{FE}$ (up to 10^{15} n/cm^2).

(3) To be determined.

three items are to be specified and maintained by the manufacturer for control levels S-2 and S-1. The idea is not to put tight tolerance limits on the manufacturer so that a significant number of parts would be rejected, but merely to call for the specification and maintenance of any important parameter so that lot-to-lot variability in the radiation response of the device is reduced. Any manufacturer desiring to produce an S-2 or S-1 level part would have to meet a specified base width, base sheet resistivity, and configuration. The actual numbers would be decided after examining several lots from different manufacturers. A sensitivity analysis performed on the transistor model[5] indicates that holding the tolerance on the base width to +10 % and the tolerance on the base sheet resistivity to +10 % will cause a maximum shift in the worst-case K_D by 22 % for the 2N2222.

4.2.2 Screens

The neutron-sensitive worst-case transistor model[5] and an experimental data base analysis have identified screens which are effective in reducing lot-to-lot radiation response variability. A screen on the minimum h_{FEO} and the minimum f_T will reduce the variability in K_D over the small-signal current range of normal operation. These screens need to be imposed for level 2 and level 1 parts. The minimum h_{FEO} is already a screen for transistors, so only the f_T screen needs to be added. The model[5] indicates that holding the tolerance on f_T to -10 % will cause a maximum shift in K_D by +7 % for the 2N2222.

4.2.3 Radiation Quality-Conformance Tests

Radiation quality-conformance (lot sample) tests must be made by a supplier (manufacturer or a testing house) for control level 1 parts (see table 3. These tests must be done on 10 samples at three neutron fluences which will cause 20 % to 50 %, and 80 % degradation in $1/h_{FE}$ (up to 10^5 n/cm^2). These fluences are of interest for systems with moderate requirements; the three data points are the smallest number that test for linearity of K_D. K_D is measured at or slightly below that collector current at which h_{FEO} is

---

[5] A. R. Hart et al., Parameter Sensitivities for Hardness Assurance: Displacement Effects in Bipolar Transistors, Final Report, Mission Research Corporation Report MRC/SD-R-20 (December 1977).

a maximum. The sample size is 10 because this number of data points will yield a minimum lot quality of 80 % at 90 % confidence without extrapolating the statistics, as was discussed in section 1.5 of this document.

The natural logarithm of the neutron damage factor, ℓnK_D, at the three fluence levels is calculated and statistically plotted according to the procedure discussed in section 1.5.1. After a statistical data base has been established for the point in question, using the process controls and screens outlined in the procurement specification, we can establish a failure criterion for L_σ,

$$\frac{m - L_\sigma}{s} \geq K_{TL} \quad ,$$

at a desired lot quality. Samples of 10 from future lots would then be accepted or rejected on the basis of the mean (m) and standard deviation (s) of the sample, as discussed in section 1.5.2. The values for L_σ and K_{TL} would be set so that almost all the parts would be accepted. A record would be kept on the statistics of each lot so that both the supplier and the user would have a statistical data base established to show trends in the quality control history.

4.3 HA Controls for User-Qualified Parts

For user-qualified parts (quality levels 1 and 2), transistor HA controls can be broken down into two general areas: Screens and quality-conformance tests. User HA controls follow a plan implemented through procurement specifications. An example of a user procurement specification (using the 2N2222) is given in table 4. Note the difference between the supplier procurement specification (table 3) and the user procurement specifications (table 4). The user cannot usually specify process controls and is interested in testing at fluence levels specified by the particular system (1x, 5x, and 10x, where 1x is the specification fluence). The user has the advantage over the supplier of knowing the circuit application for the transistors in his system.

The user screen (table 4) follows those screens stated in the previous section for the supplier. The big difference between the supplier and the user is in the radiation quality-conformance test. In general, the

TABLE IV. TRANSISTOR USER-QUALIFIED PART PROCUREMENT SPECIFICATION EXAMPLE (2N2222)

HA controls	Parameters	Test method	Test conditions	Quality level[1] failure criterion (U-2)	(U-1)	Units
Screens[2]	MIN h_{FEO}	ASTM F528-77T 750B-3076.1	I_C = 150 mA V_C = 10 V	>75	>75	-
	MIN f_T	750B-3306	I_C = 20 mA V_{CE} = 20 V f = 100 mHz	>250	>250	MHz
Radiation[3] quality-conformance test	K_D, $\Delta 1/h_{FE}$	-	Determined by application	(80%, K_D)	5x(50%, $\Delta 1/h_{FE}$)	

NOTES: (1) Level U-2 yields minimum 80% lot quality while level U-1 yields minimum lot quality of 99.9%.
(2) Failure criterion for screens are identical to slash sheet or manufacturer specifications.
(3) Radiation tests are read and record on 10 samples.

radiation tests are carried out on a sample of 10 from the lot at the specification neutron fluence (1x) for level 2 and at five times the specification fluence (5x) for level 1. The level 2 failure criterion is set at the 80 % lot quality estimate point at 90 % confidence on the parameter K_D. This insures that future lot purchases will not have lot qualities below 80 %. For level 1 the failure criterion is set at the mean of the sample at the 5x fluence point on the parameter $\Delta 1/h_{FE}$. This insures that the lot quality will be 99.9 % at the minimum.

The level 1 failure criterion could also be stated as being at the 99.9 % lot quality estimate point at 90 % confidence on the parameter K_D. The failure criterion comes out to be about the same as the mean at 5x on $\Delta 1/h_{FE}$. The 5x mean method of choosing the failure criterion has the advantage of not requiring the extrapolation of sample statistics. The reason for the 99.9 % quality at the 5x sample mean is discussed by Berger.[7]

The determination of K_D for level 2 should be done over a minimum of three fluences, preferably at 1x, 5x, and 10x to verify the design margin; however, this is not generally necessary as long as the specification fluence is below 1×10^{17} (10^{17} is the approximate limit for K_D parameter linearity).

A screen and a radiation test on $V_{CE(SAT)}$ is not required for moderate neutron environments because the dominant mechanism for changes in this parameter is the $1/h_{FE}$ degradation which causes the transistor to go out of saturation.

4.4 User Part Selection for HA (Small-Signal Application)

Figure 11 is a block diagram of a typical user part selection approach to meet a circuit specification for small-signal applications. The first step is to analyze the circuit to determine the important parameters for neutron effects. The next series of steps are taken to determine the amount of degradation in various candidate devices in order to select the part from a mature line with the largest design (safety) margin. The idea is to obtain

---

[7] R. A. Berger, Hardness Assurance for Neutron-Induced Displacement Effects in Semiconductor Devices, IRT Report IRT-8166-004 (March 1978).

RT-16448

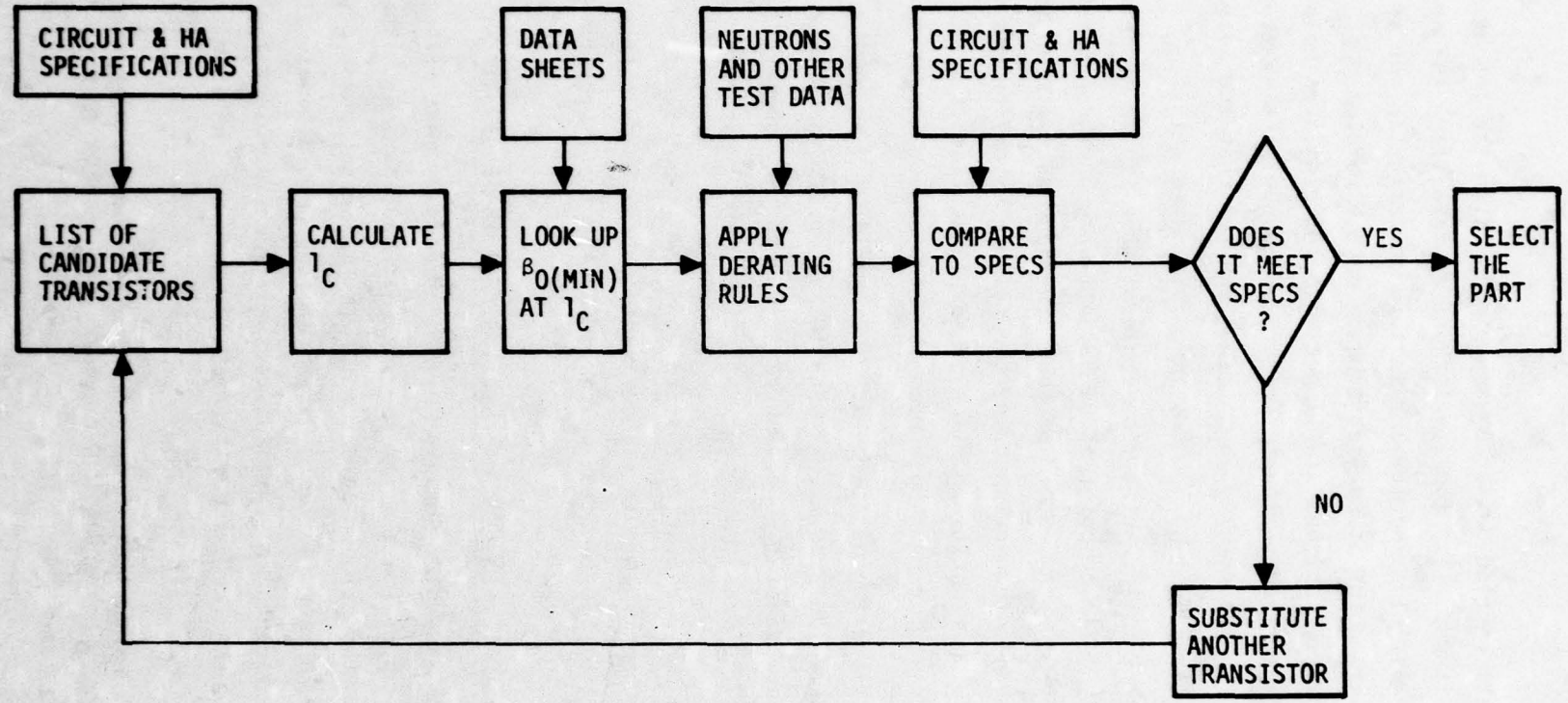


Figure 11. User part selection for small signal applications.

a device that meets all circuit specifications and has a design margin of at least 10 so that it will be a HC (2) device for HA purposes. It should also be from a mature process line so that future lot parameter variability will be at a minimum. In addition, it should be selected so that the total system part count is kept to a minimum, to lower the cost of procurement quality-conformance testing.

The selection of a harder transistor can take several forms. The simplest would be to search through some data base (such as the book put out by the Components Response Information Center at the Harry Diamond Laboratories) for a transistor with a higher minimum h_{FE} and a lower K_D maximum specification. Since the gain-bandwidth product f_T has been identified as a good screen for K_D, one should look for a device with a high f_T. A good listing of f_T values can be found in Downs.[8]

A second approach is to use a circuit tolerance factor (CTF) in conjunction with the statistical margin chart of figure 12 (for NPN transistor) or the nomograph in Alexander et al.[9] Both of these approaches are based on the standard deviation of 0.445 of the 344 unit data of Messenger and Steele.[2] The statistical margin chart (figure 12) is discussed by Berger.[7]

To illustrate the use of figure 12, suppose the circuit will fail when the degraded h_{FE} reaches 40 and the minimum transistor specification sheet pre-irradiated h_{FE} is 75. The CTF is then

---

[2] G. C. Messenger and E. L. Steele, Statistical Modeling of Semiconductor Devices for the TREE Environment, IEEE Trans. Nucl. Sci. NS-15 (Decmber 1968), 133.

[7] R. A. Berger, Hardness Assurance for Neutron-Induced Displacement Effects in Semiconductor Devices, IRT Report IRT-8166-004 (March 1978)

[8] J. W. Downs, Relative Hardness of Bipolar Transistors to Tactical Levels of Neutron Irradiation, Naval Surface Weapons Center/WOL/TR-75-126 (October 1975).

[9] D. R. Alexander et al., Hardening Options for Neutron Effects - An Approach for Tactical Systems, IEEE Trans. Nucl. Sci. NS-23 (December 1976), 1691.

RT-15422(2)

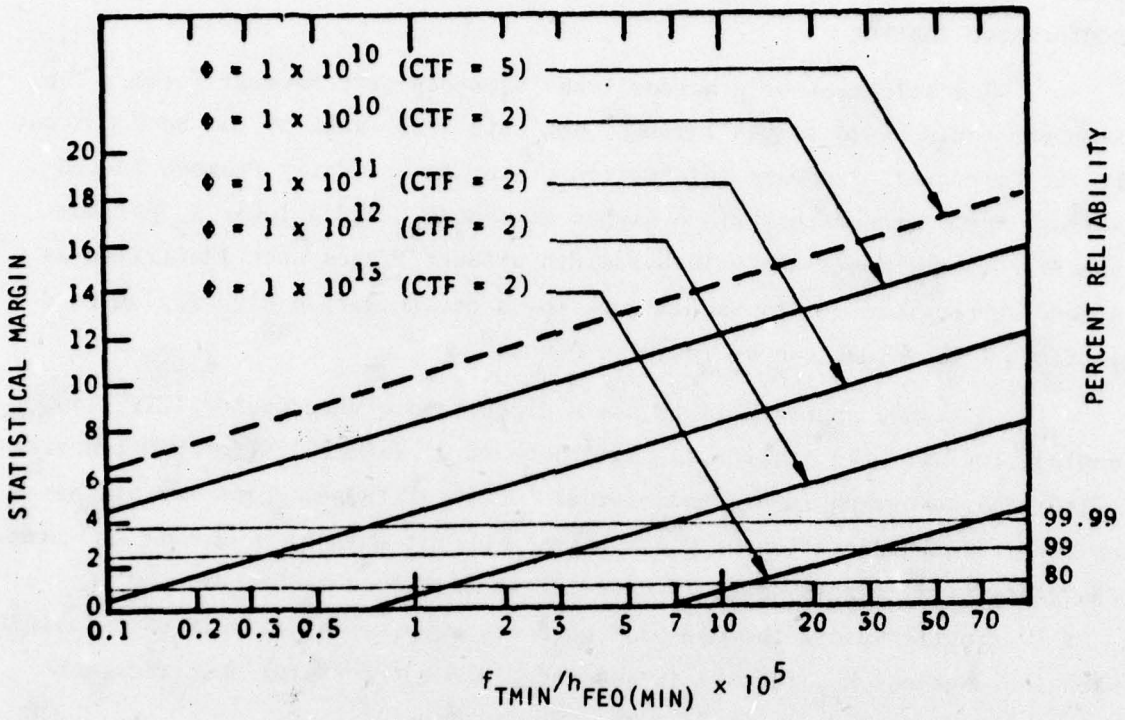


Figure 12. Probability chart for hardness assurance decisions for bipolar silicon NPN transistors (small signal application).

$$CTF = \frac{h_{FEO(MIN)}}{h_{FE\phi}} = \frac{75}{40} \approx 2 \quad .$$

Suppose also that 99 % lot quality is desired at a fluence of 1×10^{13} n/cm^2 (the statistical margin is then 2.5 in figure 12). From figure 12 these criteria yield

$$f_{T(MIN)}/h_{FEO(MIN)} = 30 \times 10^5 \quad .$$

A search of various data bases (such as in Downs[8] yields a 2N2222 transistor with

$$f_{T(MIN)}/h_{FEO(MIN)} = \frac{250 \times 10^6}{75} = 33 \times 10^5$$

at an I_C of 10 mA. Thus a 2N2222 transistor would meet the specifications of 99 % quality at 1×10^{13} n/cm^2 with a CTF of 2.

The above two methods are valid only over the current ranges at which

$$1/h_{FE\phi} = 1/h_{FEO} + K_D \Phi$$

is valid (below the maximum h_{FE} current but above very low currents). Transistor selection over broader current ranges can be accomplished by using the computer program in Mart et al, Appendix D,[5] to calculate the worst-case neutron damage factor (K_D) at any current level below the point where emitter crowding effects occur.

4.5 User Part Selection and HA Example Using the 2N2222 (Small-Signal Application)

In this section an example of a transient part selection (PS) and a subsequent HA plan for neutron effects are given. The part selection follows the procedures of figure 11 and the HA plan follows the user procedure of figure 9 for neutron effects.

This problem is to select a part which will work in the worst-case situation (most critical circuit in which the device will be used) and to

---

[5] A. R. Hart et al, Parameter Sensitivities for Hardness Assurance: Displacement Effects in Bipolar Transistors, Final Report, Mission Research Corporation Report MRC/SD-R-20 (December 1977).

[8] J. W. Downs, Relative Hardness of Bipolar Transistors to Tactical Levels of Neutron Irradiation, Naval Surface Weapons Center/WOL/TR-75-126 (October 1975).

specify an HA plan for procuring and qualifying that part. The circuit specifications are

h_{FEO} (circuit failure criterion) = 40,

I_C = 10 mA,

V_C = 10 V, and

$\Phi = 1 \times 10^{13}$ n/cm^2.

Minimum lot quality is 99.9 %, at 90 % confidence.

4.5.1 Part Selection (PS) Procedure

PS STEP 1: CANDIDATE DEVICES

The 2N2222 is a small signal NPN device for which radiation data exists; it is a military-qualified part. It therefore will be on the list of candidate parts for the system.

PS STEP 2: DETERMINE COLLECTOR CURRENT FOR DEVICE

The collector current (I_C) is given as 10 mA.

PS STEP 3: DETERMINE MINIMUM DEVICE GAIN

For an I_C of 10 mA and a V_{CE} of 10 V, the minimum gain $h_{FEO(MIN)}$ for a 2N2222 is specified in its slash sheet to be 75.

PS STEP 4: APPLY DERATING RULES

Applying derating rules to the minimum value allows a comparison to the circuit specifications to see if the part will meet the system specifications after the derating. Examples of deratings include temperature, leadage currents, and neutron degradation. If the selected device with the derating applied meets circuit and HA specifications then the device can be specified for use. If the derated device does not meet specifications, then a new device must be selected.

A derating factor for neutron degradation for the 2N2222 can be obtained from figure 4. Thus:

Average $K_D = 1.74 \times 10^{-16}$ at $I_C = 10$ mA, $V_{CE} = 5$ V

99.9 % lot quality $K_{D(MAX)} = 4.50 \times 10^{-16}$ at $I_C = 10$ mA, $V_{CE} = 5$ V.

In the absence of actual data, figure 12 could be used to obtain a valid derating factor.

Thus the derating rule is given by

$$1/\beta_\phi = 1/75 + (4.5 \times 10^{-16})(\Phi)$$

PS STEP 5: COMPARE DERATED β TO SYSTEM SPECIFICATION

At the 1x system specification of 1×10^{13} n/cm^2,

$$1/\beta_\phi = 1/75 + (4.5 \times 10^{-16})\ (1 \times 10^{13})$$

$$\beta_\phi = 56 \quad .$$

The value 56 is above the minimum specification of 40.

PS STEP 6: SELECT PART

After considering several devices, the 2N2222 is the best device available for this application and is therefore selected for use in the circuit.

PS STEP 7: DETERMINE HA PROCUREMENT CATEGORY

The breakpoint between Category 1 and Category 2 is the 1x fluence requirement. If the 2N2222 has a degraded β less than 40 (the circuit failure criterion) at the 10x fluence level (1×10^{14} n/cm^2), then the 2N2222 would be a Category 1 part for HA purposes. That is, at 10x and using the 99.9 % point for K_D

$$1/\beta_\phi = 1/75 + (4.5 \times 10^{-16})(1 \times 10^{14})$$

$$\beta_\phi = 17 \quad .$$

Thus, the 2N2222 is a Category 1 part for HA purposes since 17 is less than 40.

PS STEP 8: IF PART IS HA CATEGORY 1, DETERMINE IF EXPECTED LOT QUALITY CAN MEET CIRCUIT SPECIFICATION

The failure criterion for this Category 1 part example is

$$K_{DF} = \frac{1/h_{FE\phi} - 1/h_{FEO}}{\Phi} \approx \frac{1/40 - 1/75}{1 \times 10^{13}} = 1.17 \times 10^{-15}$$

or

$$\ell n K_{DF} = -34.4 \quad .$$

The cumulative frequency distribution of a sample of 10 of one lot of 2N2222 transistor was calculated and plotted in section 1.5. The dotted line in figure 4 (calculated with the aid of figure 3) is the probability of finding a device in a lot with a failure criterion (L_σ) given the sample statistics of table 1. The dotted line intersects the -34.4 point a t lot quality much greater than 99.9 %, so we can state with 90 % confidence that there is only a very small (less than 0.016) chance of finding a device in this lot with a K_D exceeding 11.7×10^{-16}. Since the lot quality requirement is only 99.9 %, the 2N2222 can meet the circuit specifications.

4.5.2 HA Procedure

HA STEP 1: PROCUREMENT

Since the 2N2222 is HA Category 1, a supplier level 2 (or 1) control part should be specified if available. This would reduce the lot-to-lot variability through the imposition of the process con-rols and screens called for by the supplier S-2 level.

HA STEP 2: USER ELECTRICAL SCREENS

Table 4 lists those screens which should be imposed on a Category 1 part. Thus, a screen on the minimum f_T (250 MHz at an I_C of 20 mA, V_{CE} of 20 V, and an f of 100 MHz) and on $h_{FEO(MIN)}$ is needed.

HA STEP 3: USER RADIATION QUALITY CONFORMANCE TESTS

The 2N2222 was specified in PS Step 7 as being a Category 1 device and hence subject to radiation quality-conformance tests. Analysis of the radiation quality-conformance test on the 2N2222 lot revealed that the devices

from this lot could be used in the system since the lot quality is way above the desired 99.9 % point.

Suppose now that a new lot of 2N2222's were purchased and a lot sample radiation test yielded the raw data given in table 5 (actual CRIC data). If this data is plotted in the same manner as in section 1.5, the histogram of figure 13 results. In figure 13 the first lot and the second lot data are combined to show the degradation in the second lot data. In the second case, the do-ted line (the probability of finding a device in the lot with a failure criterion greater than that specified) intersects the -34.4 failure point at the 99.99 % point. Thus there is a 0.01 chance (with 90 % confidence) of finding a device in this new lot with a K_D exceeding 11.7×10^{-16}. This is above the desired 99.9 % lot quality, so the second lot would be accepted also.

Drawing the dotted line in figure 13 is not necessary. The 90 % confidence, 99.9 % lot quality requirement can be stated mathematically for 10 devices (from section 1.5) as

$$\frac{m - 34.4}{s} \geq 4.7 \quad .$$

Since for the second lot of 10 devices we have

$$\frac{35.61 - 34.4}{0.2} = 6.05 \quad ,$$

the requirement is met, so the second lot would be accepted.

4.6 User Part Selection and HA Example Using 2N2222 (Switching Application)

The problem is to select a part which will work in the worst-case situation where $V_{CE(SAT)}$ is the parameter of interest in a 1×10^{13} neutron environment. Also, a HA plan must be specified for procuring and qualifying that part. The circuit specifications call for an I_C of 11 mA and an I_B of 1 mA which yields a forced $\beta(\beta_F)$ of

$$\beta_F = I_C/I_B = 11 \quad .$$

The forced $\beta(\beta_F)$ is a circuit concept, not a device concept. It is used to specify that point at which the transistor will come out of

TABLE V. SECOND LOT 2N2222, TEST 660811, I_C = 10 mA, V_C = 3 V

N	PRE	h_{FE} at fluence ϕ			$K_D \times 10^{-16}$	$\ell n K_D$	n/n+1 (%)
		9.13×10^{12}	2.12×10^{13}	5.8×10^{13}			
1	208	131	91	50	2.6	-35.9	9
2	138	97	72	41	2.9	-35.8	18
3	171	110	78	43	3.0	-35.7	27
4	189	119	80	42	3.2	-35.7	36
5	136	94	67	36	3.5	-35.6	45
6	143	94	66	36	3.6	-35.6	55
7	156	99	68	36	3.7	-35.5	64
8	125	83	59	32	4.0	-35.5	73
9	138	89	61	32	4.1	35.4	82
10	105	72	55	29	4.3	-35.4	91

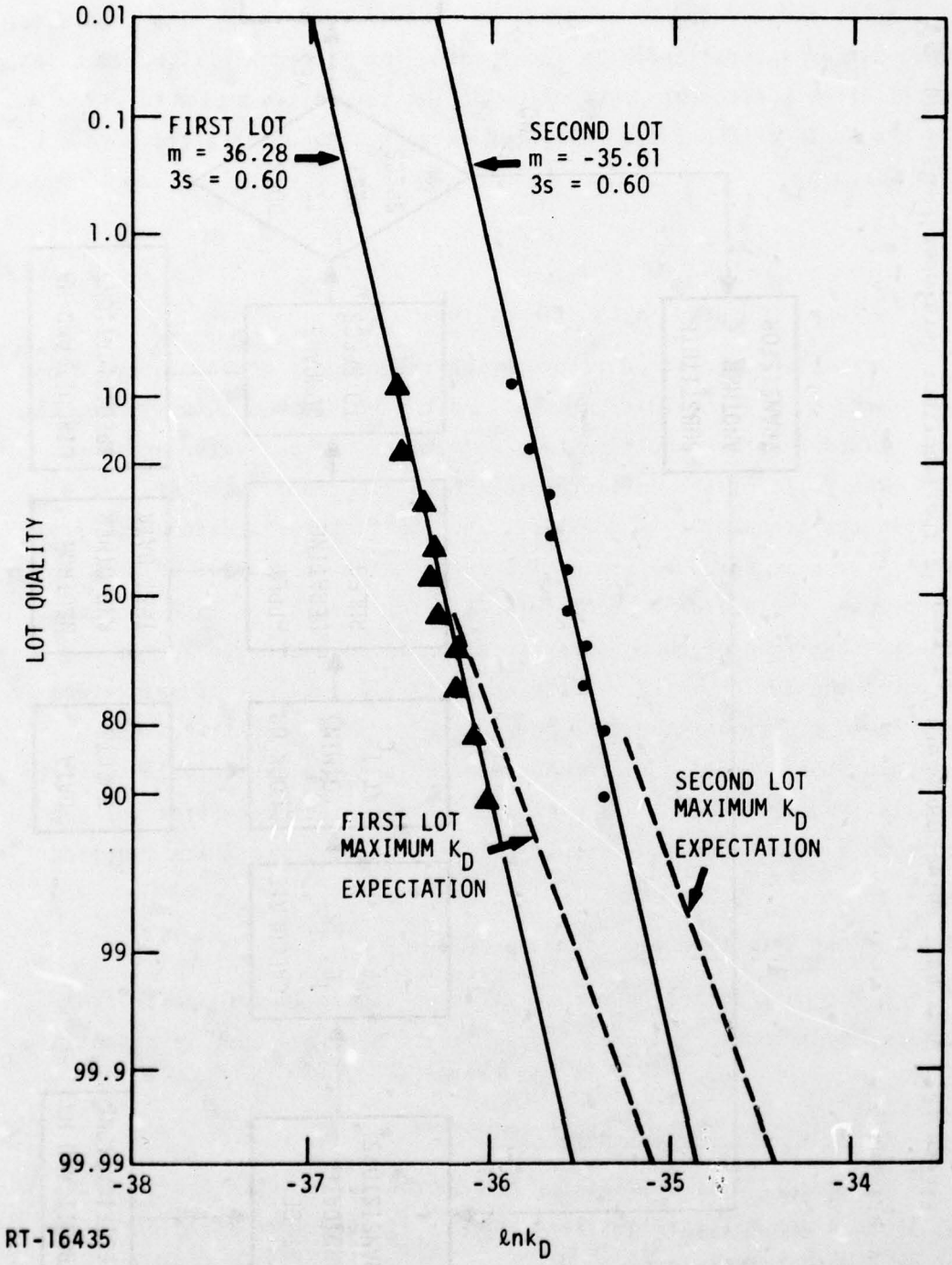


Figure 13. First (Sect. 1.5) and second 2N2222 lot statistics.

saturation. When the transistor β (which is measured in the active region with V_{CE} > IV) is degraded by neutrons to the forced β value, the transistor will come out of saturation. The ideal value for forced β will be that value which will allow sufficient penetration of the saturation region to allow V_{CE} to be a linear function of the collector current. A conservative rule-of-thumb is given by

$$\beta_F = \frac{\beta_0}{2.5} \quad ,$$

where β_0 is the β measured in the linear region.[10]

A simple calculation illustrating the concept of the forced β and the transistor β is given in figure 14. As can be seen in this figure, the resistor values and the supply voltage determined the collector and base current. The ratio of the collector to the base current is the forced β. If the selected transistor is a 2N2222, the manufacturer's data sheet lists the transistor β measured in its active region at a current of 10 mils to be 75. Therefore, the overdrive factor (β_0/β_F) for saturation is 6.8. Since the conservative rule of thumb for saturation is an overdrive factor of 2.5 or more, the device is in saturation. It will come out of saturation if neutrons cause the transistor β to be reduced from 75 to (11)(2.5) or 28. At that point the overdrive factor becomes 2.5 and the device will start to go into its linear region. This will cause the collector-emitter voltage to rise to such a point that the circuit will no longer perform its required function.

4.6.1 Part Selection Procedure

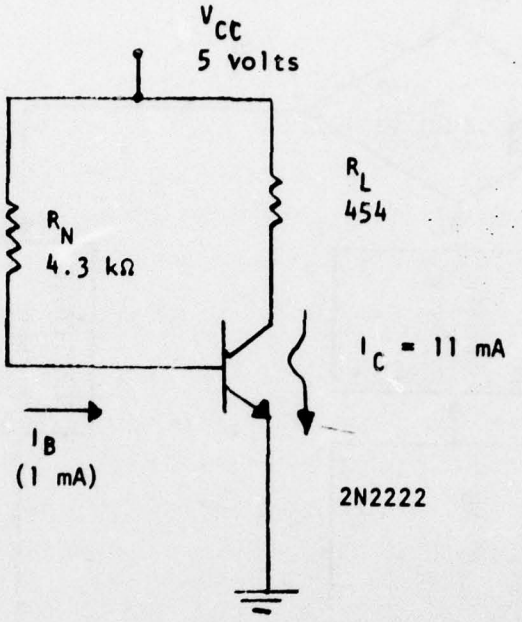
The part selection method given in figure 14 for small-signal application, modified to the case for switching applications, is given in figure 15.

PS STEP 1: DEVICE SELECTION

The 2N2222 is a switching NPN device for which radiation data exists; it is a JAN military qualified part. It therefore would be on the list of candidate transistors.

---

[10] Motorola Corporation, Switching Transistor Handbook (1963).

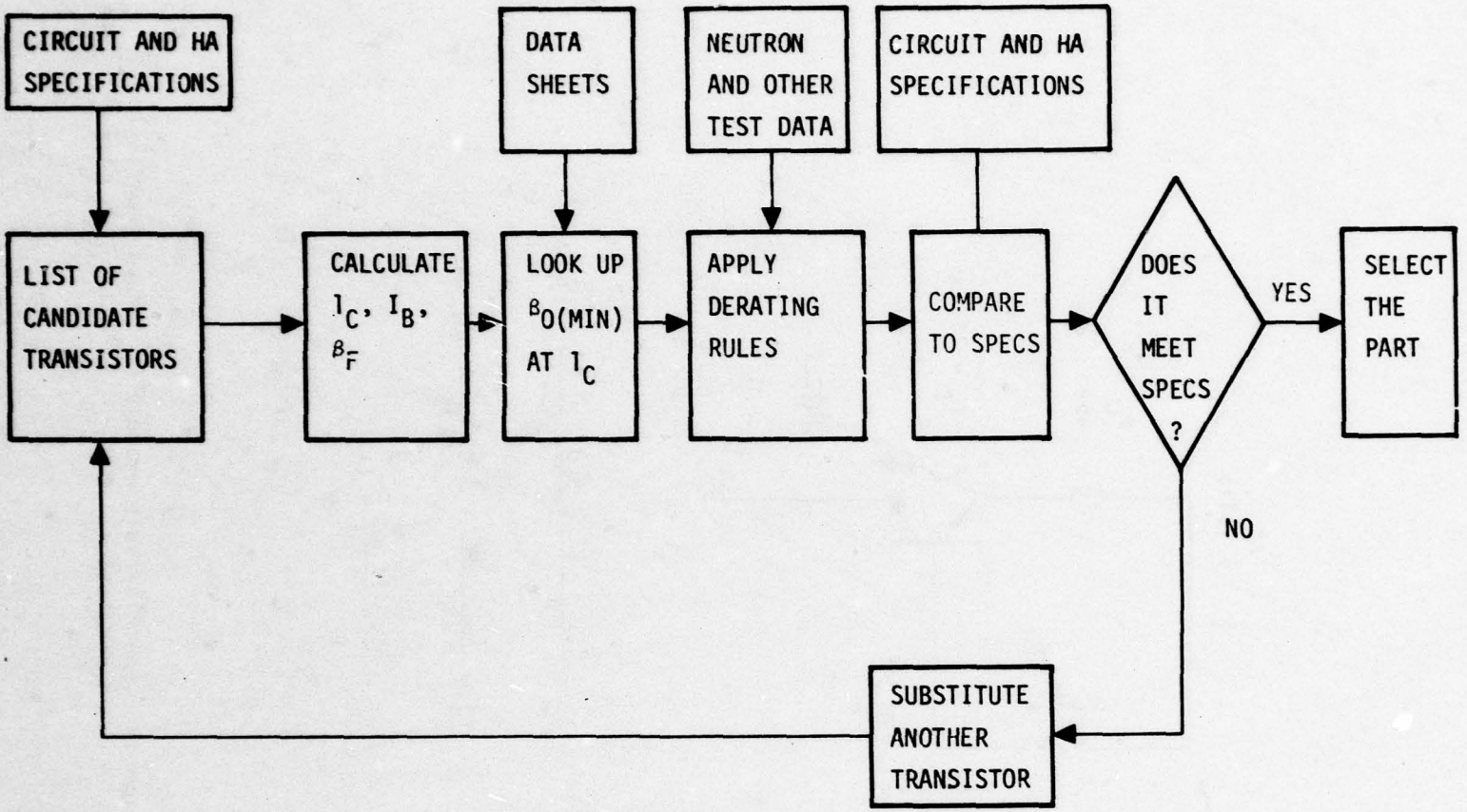


$$I_C = \frac{V_{CC} - V_{CE}}{R_L} = \frac{5.0 - 0.03}{454} = 11 \text{ mA}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_N} = \frac{5.0 - 0.7}{4.3K} = 1 \text{ mA}$$

$$\beta_F = \frac{I_C}{I_B} = \frac{11 \text{ mA}}{1 \text{ mA}} = 11 \quad .$$

Figure 14. Logic circuit example of forced beta (β_F) calculation.



RT-16449

Figure 15. User part selection where $V_{CE(SAT)}$ is the important parameter (switching application).

PS STEP 2: DETERMINE COLLECTOR CURRENT FOR DEVICE

The collector current was calculated in figure 14 to be 11 mils.

PS STEP 3: DETERMINE MINIMUM DEVICE GAIN AND CIRCUIT FORCED β

The collector current is calculated in figure 14 to be 11 mils and the transistor minimum β is measured in the active region to be 75 for that collector current and a collector emitter voltage of 10 V. I_B is calculated in figure 14 to be 1 mil; therefore, the forced beta (which is the ratio of the collector to be base current) is 11.

PS STEP 4: APPLY DERATING RULES

The neutron fluence at which the device will come out of saturation is calculated by comparing the device beta to the forced beta. This occurs when the transistor beta is approximately equal to 2.5 times the forced beta. The forced beta must be calculated from the circuit. This was accomplished in Step 3. The degraded transistor beta is calculated from

$$\frac{1}{\beta_{\phi(MIN)}} = \frac{1}{\beta_{0(MIN)}} + [K_{B(MAX)}][\phi]$$

which is the same formula listed for the small-signal NPN transistors. Knowing $\beta_{0(MIN)}$ from the manufacturer's data sheet (75), the fluence (1×10^{13}), and the neutron damage factor maximum (which is determined from PS Step 4 in section 4.5.1 to be 4.50×10^{-16}), the degraded β_ϕ can be calculated.

PS STEP 5: COMPARE DERATED PARAMETERS TO SYSTEM SPECIFICATION

At the 1x system specification level of 1×10^{13} neutrons/cm^2, the derating rule on β_0 yields a degraded β of 56. This is above the required beta of (11)(2.5) or 28 so the device can be used in the system and will not come out of saturation at the 1x level.

PS STEP 6: SELECT PART

Since the derating rule on β_ϕ shows that the device will function in the circuit at the 1x level, the 2N2222 is selected for use in the circuit.

Although we have a qualified part, suppose that the base drive of the circuit in figure 14 were reduced to the point where the circuit forced beta rose to 62. In this case the 2N2222 cannot be used since the degraded beta is less than the forced beta and the device would come out of saturation. In such a case, transistor substitution would need to be made. As in the case of the small-signal transistor, the simplest approach would be to search a data bank for a similar NPN transistor with a higher $\beta_{\phi(MIN)}$ and a lower neutron damage factor. As a guide, a device with a higher f_T value can be used since this is an indication of a harder transistor.

PS STEP 7: DETERMINE HA PROCUREMENT CATEGORY

The first step is to determine the worst-case failure criteria dictated by the circuit for neutrons. The degraded β must be equal to or greater than 2.5 times the forced β of the circuit or about 28. From PS Step 7, the degraded β at 10x is 17, which is below the 2.5 overdrive-calculated minimum value of 28, so the part is Category 1 for HA purposes.

4.6.2 HA Procedure

HA STEP 1: PROCUREMENT

Since the 2N2222 has been determined to be a Category 1 part, the HA procurement specifications follow the same specification listed in section 4.5.2 for the small-signal applications.

HA STEP 2: USER ELECTRICAL SCREENS

The HA electrical screens are the same as those listed in section 4.5.2.

HA STEP 3: USER RADIATION QUALITY-CONFORMANCE TESTS

The HA radiation tests are the same as those listed in Section 4.5.2.

5. HA CONTROLS FOR SILICON ZENER DIODES

5.1 Effects of Neutron Radiation on Zener Diodes

Voltage-reference (zener) diodes are pn junction devices operated in the reverse direction with sufficient bias to cause avalanche or zener breakdown. The desired property of the voltage reference diode is that very little current flows until the specified breakdown voltage. At that voltage, the zener or avalanche processes should allow large current flows so that the voltage drop across the diode remains essentially constant over many decades of current. This kind of diode can be used as a voltage reference element since the voltage across it is independent of the current through it, as long as the voltage remains above the breakdown voltage of the diode. For avalanche breakdown diodes, the breakdown voltage is a function of the impurity doping levels and increases with neutron radiation. "Zener diodes" above 7 to 8 V exhibit avalanche breakdown.

Zener breakdown is similar to avalanche breakdown except that the breakdown results from band-to-band tunneling. In this mechanism, carriers tunnel from the conduction band of the heavily doped n-region across the forbidden gap to the valence band of the heavily doped p-region. Diodes operating in zener breakdown exhibit relatively low breakdown voltages (less than about 6 V) with a breakdown characteristic somewhat softer than those diodes which are avalanching. Increased traps in the forbidden gap provide additional sites to which carriers can tunnel. Consequently, voltage reference diodes based on zener breakdown show a <u>decrease</u> in the breakdown voltage with neutron fluence.[11]

The high doping levels found in standard zener diodes make these types of diodes inherently radiation resistant. Typically, for a silicon reference diode, a 1 % change in the breakdown voltage is not reached until neutron fluences exceed 1×10^{14} n/cm^2.

---

[11] R. P. Donovan et al, A Survey of the Vulnerability of Contemporary Semiconductor Components to Nuclear Radiation, Air Force Avionics Laboratory TR-74-61 (June 1974).

While standard zener diodes are inherently radiation resistant, this is not the case in temperature-compensated zener reference diodes.[12] To achieve temperature compensation two diodes are employed in series, one forward biased and one reverse biased. This is done so that the forward bias pn junction, which has a negative temperature coefficient, can be utilized to compensate for the positive temperature coefficient of the reverse bias junction. It is normally the forward bias diode which presents the problem because the characteristics of the forward bias pn junction changes significantly with fast neutron dosage and hence makes the composite sensitive to radiation.

One technique to achieve temperature compensations and radiation hardening is to make use of the fact that low forward current operation of the forward bias diode decreases with neutron fluence while the avalanche breakdown voltage of the reverse bias junction increases. Thus the effects compensate each other which results in a radiation-hardened temperature-compensated unit.

Since reference diodes do not exceed a 1 % variation in their breakdown voltages below fluences of 10^{14} n/cm^2, they are not often considered in survivability/vulnerability analysis because other devices in the system usually have lower failure thresholds.

5.2 HA Controls for Supplier- and User-Qualified Parts

Temperature-compensated silicon reference diodes are of interest because they are more sensitive to neutron damage and are more likely to be found in critical circuit applications. Process controls on the doping levels may be useful for HA.

Because of lack of experimental data and adequate theory in relating neutron displacement damage to small changes in the breakdown voltage and reverse current, it is difficult to say which parameters would be useful for screening purposes. A screen on the zener voltage and the reverse current is usually carried out from a nonradiation reliability standpoint and may be useful for HA purposes. For quality-conformance tests, a lot sample radiation test on the change in the zener voltage may be useful because it is usually the parameter of interest to the design engineer. Thus, a supplier procurement

specification for displacement effects for temperature-compensated silicon reference zener diode awaits more experimental data or the development of an adequate model.

6. HA CONTROLS FOR TTL DIGITAL INTEGRATED CIRCUITS

6.1 Effects of Neutron Radiation on TTL 54/74 NAND GATES

Transistor/transistor logic (TTL or T^2L) is the most popular form of bipolar IC digital logic. In the 54/74 series, TTL devices come in five different versions: (1) the standard version (54/74), (2) the low-power version (54/74L), (3) the high-speed version (54/74H), (4) the Schottky version (54/74S), and (5) the low-power Schottky version (54/74S). A 54/74 schematic showing the input/output differences between families of TTL circuits is shown in figure 16.[13]

This section is limited to standard and low-power TTL logic. A circuit schematic of a typical TTL low-power logic gate is shown in figure 17.[14] This gate operates from a single 5-V power supply and had typical logic levels of 0.2 V for the binary 0 (low) and 3.4 V for binary 1 (high). The circuit consists of three basic sections, a multiple emitter input transistor Q1, a phase splitter transistor Q2, and a totem pole output circuit consisting of transistors Q3 and Q4. The multiple emitter-base junctions of transistor Q1 along with R1 form a diode gate. The primary advantage of this arrangement over individual diodes is that it allows higher speed operation. The phase splitter transistor Q2 provides complementary drive signals for the two output transistors Q3 and Q4. Transistor Q3 is a shunt transistor switch while Q4 serves as an active load resistor for Q3 (Q4 serves as an active "pull-up resistor" for Q3). Current to any shunt load on the output of the TTL logic gate is supplied by transistor Q4. This arrangement provides a lower output impedance in the high output state (when compared to a resistor) and therefore a higher speed operation can be obtained.

Referring to figure 16, the operation of the typical TTL logic gate can be described as follows. Note that the base-collector junction of Q1, the emitter-base junction of Q2, and the emitter-base of junction Q3 form a

---

[13] Texas Instruments, The TTL Data Book, Second Edition (1976).

[14] Allan H. Johnston and Robert L. Skavland, Terminal Measurement for Hardness Assurance in TTL Devices, IEEE Trans. Nucl. Sci. NS-22 (December 1975), 2303.

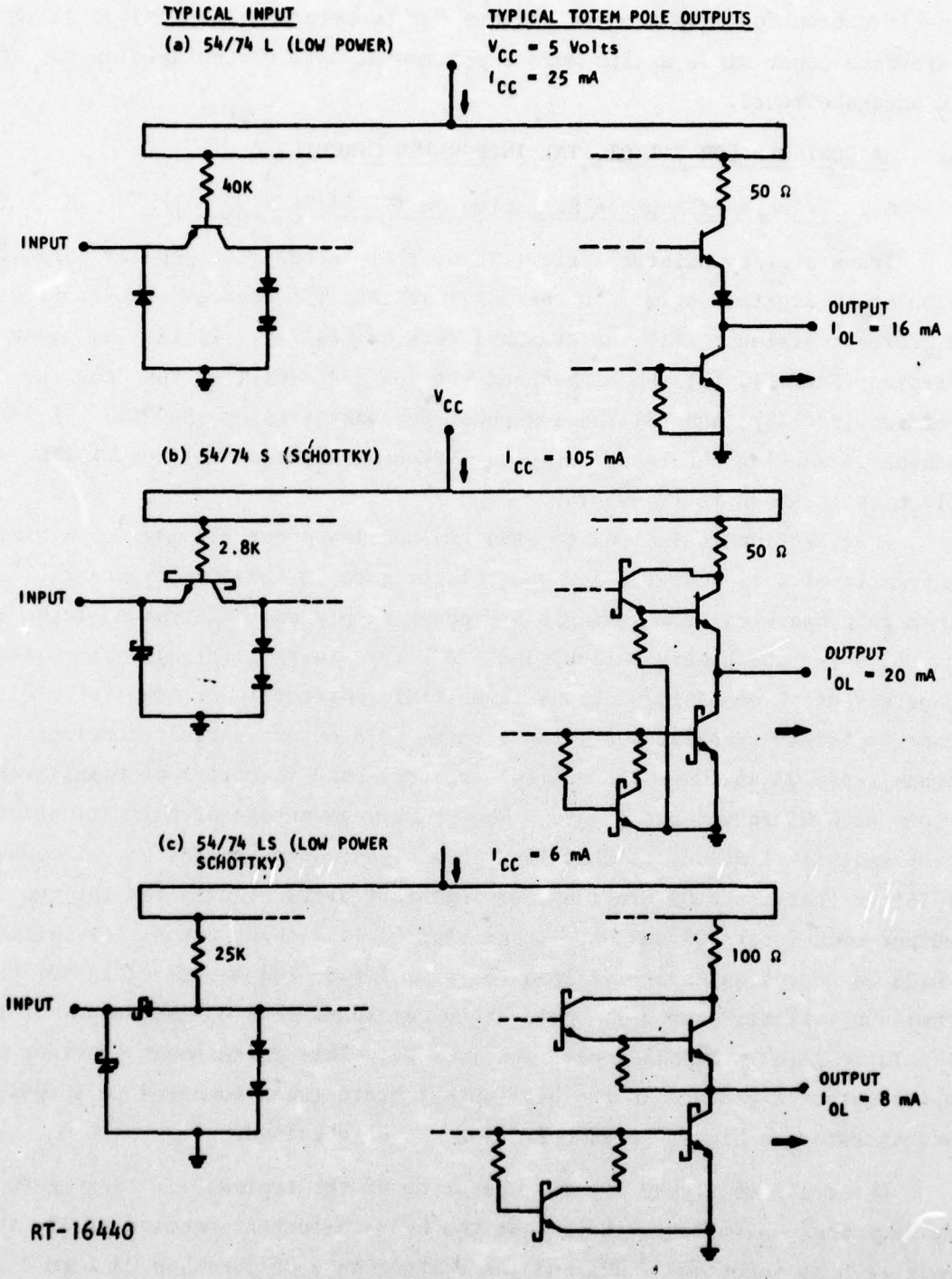


Figure 16. 54/74 family input-output comparison.

RT-16441

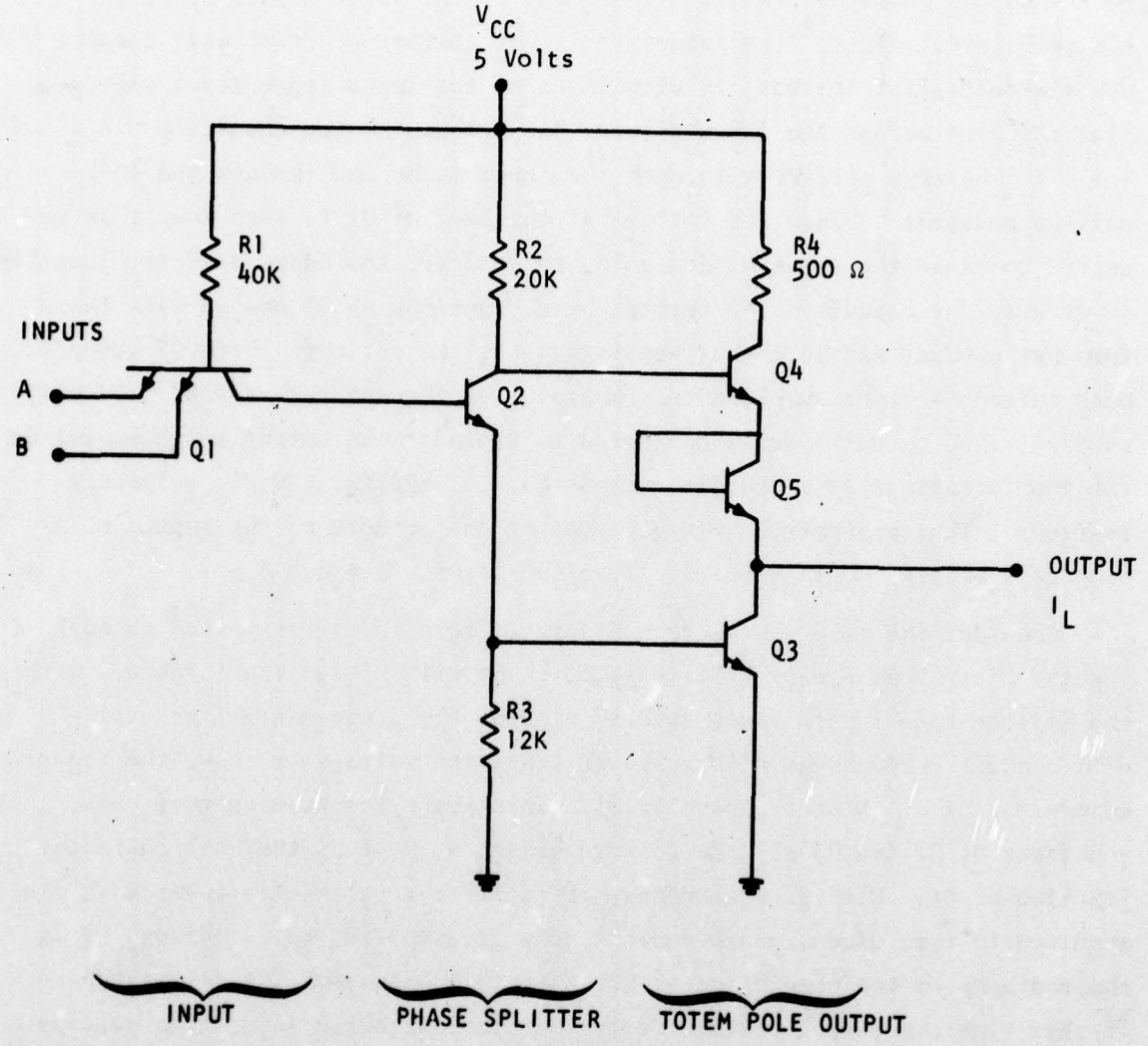


Figure 17. TTL 54L00 logic gate

three-diode series string. Since a pn junction silicon diode requires approximately 0.7 V across it before it conducts, the voltage at the base of Q1 must be greater than 2.1 V (3 x 0.7 - 2.1) so that all three diodes can be turned on. Consider the case where one of the logic inputs is at its binary 0 level. If so, the associated input emitter junction will conduct and the voltage at the base of 01 will be at the input logic level voltage plus the drop across the input emitter-base diode, or approximately 0.4 $\pm$ 0.7 = 1.1 V. Current will flow through the input diode and through the 40-k pull-up resistor. Since the voltage at the base of Q1 is less than that required to cause the three diodes going to conduct, the base-collector junction of Q1 will not conduct. The emitter-base junctions of Q2 and Q3 will therefore not conduct and so these transistors will be cut off. With Q2 cut off, base current will be supplied to transistor Q4 through resistor R2. Q4 will conduct if an output load is connected to ground. The output voltage will be the supply voltage less the drop across Q5, Q4, and the 500 phm collector resistor. Thus a binary 0 voltage level at one or more of the inputs will produce a binary 1 output voltage level of between 2.4 and 3.6 V.

Consider the case now where a binary 1 logic level is applied to both inputs. A typical binary 1 logic level input will be 2.4 V or higher. With the emitter-base input diodes reverse biased, the diode equivalent string will conduct through the 40-k resistor since the voltage is above the required minimum of 2.1 V at the base of Q1. This means that the emitter-base junctions of Q2 and Q3 will be forward biased as well as the base collector junction of Q1. With Q2 conducting, its collector voltage is lower than that required to turn Q4 on. Base current normally supplied to Q4 through Q2 is shunted away by the conduction of Q2. With Q2 conducting, Q3 will saturate. At this time the output voltage is the emitter-collector saturation voltage of Q3 which will be about 0.4 V or less. Thus, with binary 1 on both inputs the output will be binary 0.

In summary, standard TTL gates have a current sinking type of logic. They have a typical fan out of 10, logic levels of +0.2 V for a binary 0, plus 3.3 V for a binary 1, a power dissipation of 10 mW, and a propagation delay of 10 ns (54/74); they require a supply voltage of +5 V, ±10 %.

In addition to the standard TTL IC's, radiation-hardened versions are

available. The radiation-hardened versions employ dielectric isolation, thin-film resistors, small transistor geometries, shallow-based diffusions, heavy gold doping, minimum collector thickness and resistivity, and aluminum metalization in their technologies to harden the circuit against gamma and neutron irradiation.[13] The Texas Instruments series of radiation-hardened TTL IC's are designated by the RSN prefix. They are available in the 00 version (quad 2 input), the 04 version (a hex inverter), the 10 version (a triple 3-input device), and the 20 version (a dual 4-input gate). They are also available in the S series which means that they will meet specifications over the full military temperature range of -55°C to +125°C

Monolithic integrated bipolar TTL 54/74, 54/74H, and 54/74L circuits consist of NPN transistors and resistors (see figure 17). Displacement damage decreases transistor gain by lifetime degradation. The transistor gain degradation is the most sensitive parameter to neutron damage and therefore the most important parameter for this application.

Satisfactory performance of TTL logic depends upon the driving capability of the output transistors. As the gain of the output transistors decreases because of displacement damage so does the output current capability of the logic gate. The major effect of this is the reduction in the low-level output current (I_{OL}) which reduces the fanout of the circuit. The primary parameter in determining I_{OL} is the gain of the output transistor. Although no simple analytical expression exists to relate I_{OL} to h_{FE} of the output transistor, I_{OL} is approximately proportional to the h_{FE} of the output transistor. Knowing the gain degradation characteristics of the output transistor therefore provides a reasonably good prediction of logic gate performance.[15]

Several techniques have been proposed for TTL circuits relating various electrical screens to the prediction of neutron effects, but limitations exist on all of them as can be seen in table 6. None of the techniques appear to provide effective neutron response prediction information, such as was developed earlier for transistors, without making some modification

---

[13] Texas Instruments, The TTL Data Book, Second Edition (1976).

[15] M. Simons et al., Integrated Circuits for Radiation-Hardened Systems: A State-of-the-Art Review, Air Force Avionics Laboratory-TR-76-194 (January 1977).

TABLE VI. CANDIDATE TTL SCREENING AND QUALITY CONFORMANCE PARAMETERS

Parameter	Advantages	Limitations
I_{SK} (output sink current)	(1) Gain margin of output transistor can be established	(1) V_{BE} and $V_{CE(SAT)}$ variation not included
	(2) I_{SK} is easily measured	(2) Gain measured at fixed base current (collector current will vary)
	(3) I_{SK} degrades in a manner similar to h_{FE} of individual transistor	(3) Resistor ratio process variation not included
V_{OH} (terminal V_{BE} measurement reference of Johnston & Skavland*)	(1) A dc measurement	(1) Circuit design needs to be fixed
	(2) Applicable to most TTL devices	(2) Transistor geometries need to be fixed
	(3) No special metallization patterns required	(3) Leakage currents not included
	(4) A good screening parameter	
TPLH and TPHL	(1) f_T of the phase-slitter and output transistors can be estimated	(1) Switching time tends to be dominated by the output load capacitance
		(2) Low correlation with neutron damage
B.O.T. (breakout transistor)	(1) High correlation between V_{BE} at a fixed I_C and neutron damage	(1) Assumes homogenity in f_T across the wafer
	(2) Useful for more complex circuits	(2) f_T measurements are not easily made
		(3) Requires special metallization pattern
V_{OL}		(1) Changes in this parameter are small so measurements must be very accurate

*Allan H. Johnston and Robert L. Skavland, Terminal Measurements for Hardness Assurance in TTL Devices, IEEE Trans. Nucl. Sci. NS-22 (December 1975), 2303.

to the structure of the device for extra access to each critical element.

The output sink current (I_{SK}) is related to the output transistor gain and can be measured using existing terminal parameters. The sink current is measured with the device in the low state by forcing sufficient current into the output of the device to drive the transistor out of saturation. The sink current is then limited by the gain of the output transistor, and because the base drive of the transistordepends upon the resistor values V_{BE} and $V_{CE(SAT)}$ of the internal transistors, the base current is essentially constant. This approach willyield the neutron damage factor of the output transistor; however, it has several limitations which are of second-order importance. These limitations include the fact that circuit variation in V_{BE} and $V_{CE(SAT)}$ are not included, resistor values are dependent on process variation, and the gain measurement is made at a fixed base current. Since I_{SK} is made under conditions of constant base current, collector current can vary between units because of the variability of transistor gain. While this variation is not great, it can lead to difficulty because of the dependence of h_{FE} and K_D on collector current.

Johnston and Skavland[14] propose a terminal (V_{OH}) measurement technique that uses the difference between the power supply voltage and the output high (modified input conditions) volatge to provide an effective screening parameter for the neutron response of ITL IC's. The requirements on this technique are that the chip circuit design and internal transistor geometry be known and fixed. Therefore, while this technique would not be useful for general circuit evaluation because it requires the internal structure to be known it would be useful for devices which have configuration and process controls, such as those found in integrated circuits prepared for supplier level 2 qualification.

Changes in the switching times (TPLH and TPHL) of TTL devices after neutron exposure can also be related to transistor h_{FE} degradation, however the behavior of these two parameters is strongly nonlinear with neutron fluence. TLPH is the propagation delay time, low to high level, and is

---

[14]Allan H. Johnston and Robert L. Skavland, Terminal Measurements for Hardness Assurance in TTL Devices, IEEE Trams. Nucl. Sci. NS-22 (December 1975), 2303.

defined as the time between the specified reference points in the input and output voltage waveforms with the output changing from the defined low level to the defined high level. The TPHL is the propagation delay time, high- to low-level output. Switching times can yield an estimation of the f_T of the phase splitter and output transistors; however, low correlation with neutron damage[16] reduces the effectiveness of this parameter as an HA screen.

Another approach to the HA problem is the use of devices with special leads to allow direct access to the base of the output transistor.[17] However, variations in transistors across a wafer may be severe enough that the output transistor may not accurately predict the worst-case element degradation for anything larger than a simple small-scale integration IC. This technique, however, may be theonly option available for complex IC's. Breakout transistors could be used, but care must be taken so that the transistor selected has the lowest gain-bandwidth product and the largest area of any element in the device itself.

The output low-level voltage (V_{OL}) degrades nonlinearly with neutron fluence. The problem of predicting post-irradiation V_{OL} is analogous to the $V_{CE(SAT)}$ problem of discrete transistors.

It must be remembered that these candidate screen and quality-conformance parameters are to be used only for Category 1 parts which must survive a high radiation requirement. Typical failure levels for TTL circuits range from 10^{14} to 10^{15} n/cm^2, so these devices are relatively hard to neutron radiation Thus, systems with moderate nuetron requirements will probably not need to apply HA controls for TTL parts because they will be Category 2 parts in most cases.

6.2 HA Controls for Supplier-Qualified Parts

Of all the candidate existing-terminal screens listed in table 6, I_{SK} is recommended as the best. Thus it is listed as a screen in the supplier

---

[16] Allan H. Johnston and Robert L. Skavland, Neutron Hardness Assurance Techniques for TTL Integrated Circuits, IEEE Trans. Nucl. Sci. NS-21 (December 1974), 393.

[17] I. Arimura, A Study of Electronics Radiation Hardness Assurance Techniques, Air Force Weapons Laboratory-TR-73-134 (January 1974).

procurement specification of table 7. For the screen to be effective, process (including configuration) controls must be applied. Base sheet resistivity (base doping) and base width of the constituent transistors needs to be specified and maintained by the manufacturer.

The output sink current (I_{SK}) is a good parameter for radiation tests because it is easily measured, it degrades in a manner similar to discrete devices, and other parameter degradation can be calculated from it.[14] A failure criteria of 3 mA is set because this is the minimum value required to meet worst-case switching and fanout of the device.[16]

6.3 HA Controls for User-Qualified Parts

The screen listed in table 8 (I_{SK}) requires process controls to be effective. Thus, the user should purchase a level 2 part from the supplier. A supplier level 2 part has been screened for I_{SK} (see table 7).

The output sink current (I_{SK}) is a good parameter for user radiation tests for the same reasons it was recommended for the supplier radiation tests. The user subjects 10 samples to a 1x neutron fluence and uses the statistics of section 1.5 on the K_D of the output transistor (calculated from I_{SK}) to compare the lot 80 % worst-case value to the specified value for quality level 2. For quality level 1 the 10-sample mean at 5x on K_D is compared to the specified value, and if the mean is below the specified value then the lot is of at least 99.9 % quality at 90 % confidence (table 8).

The validity of the mean-at-5x statement being 99.9 % quality follows the reasoning of Berger[7] and that in section 4 for transistors. The statement is valid for NPN transistors where h_{FE} degradation is the primary mode of failure, such as TTL logic. The assumptions implicit in the

---

[7] R. A. Berger, Hardness Assurance for Neutron-Induced Displacement Effects in Semiconductor Devices, IRT Report IRT 8166-004 (March 1978).

[14] Allan H. Johnston and Robert L. Skavland, Terminal Measurements for Hardness Assurance in TTL Devices, IEEE Trans. Nucl. Sci. NS-22 (December 1975), 2303.

[16] Allan H. Johnston and Robert L. Skavland, Neutron Hardness Assurance Techniques for TTL Integrated Circuits, IEEE Trans. Nucl. Sci. NS-21 (December 1975), 393.

TABLE VII. TTL SUPPLIER-QUALIFIED PART PROCUREMENT SPECIFICATION
EXAMPLE (54L00 LOW POWER GATE)

HA controls	Parameter	Test method	Test conditions	Control level failure criteria (S-2)	(S-2)	Units
Process controls	Base width	(1)	-	±10%	±10%	μm
	Base resistivity	(1)	-	±10%	±10%	cm^{-3}
	Configuration	-	-	-	-	-
Screens	I_{SK}	(3)	(3)	(1)	(1)	mA
Radiation[2] quality-conformance test	I_{SK}	(3)	(3)	-	(3)	mA

NOTES: (1) To be determined.
(2) Radiation tests are read and record on 10 samples.
(3) First draft document prepared for ASTM by IRT Corporation in February 1978.

TABLE VIII. TTL USER-QUALIFIED PART PROCUREMENT SPECIFICATION EXAMPLE
(54L00 LOW POWER GATE)

HA controls	Parameter	Test method	Test conditions	Quality Level Failure Criteria (S-2)	(S-1)	Units
Screens	I_{SK}	(1)	(1)	(2)	(2)	V
Radiation[3] quality-conformance test	I_{SK}	(1)	(1)	1x(80% K_D)	5x(50% K_D)	mA

NOTES: (1) First draft document prepared for ASTM by IRT Corporation in February 1978.
(2) To be determined.
(3) Radiation tests are read and recorded on 10 samples.

statement are (1) the K_D distribution is lognormal, (2) delta $1/h_{FE}$ is proportional to neutron fluence, and (3) the NPN log (K_D/f_T) mean and standard deviation data does not vary significantly from lot to lot. Since TTL logic uses NPN transistors and since I_{SK} is related to the h_{FE} of the output transistor, for first-order effects the I_{SK} parameter degradation can be considered to behave the same as the $\Delta 1/h_{FE}$ parameter of individual transistors.

6.4 HA Example Using SN54L00 Gate

In this example, it is assumed that the SN54L00 gate was chosen because it was the logic type needed and it was hard enough to meet the system neutron specification of 1×10^{14} n/cm^2. The succeeding steps, therefore, are for an HA category 1 part since 1×10^{14} n/cm^2 approaches the technology failure level.

HA STEP 1: PROCUREMENT

Since the HA screens and radiation quality conformance tests on a Category 1 TTL part require process controls, a supplier level 2 part should be purchased if available.

HA STEP 2: ELECTRICAL SCREEN

A supplier electrical screen on I_{SK} is suggested (table 7) elsewhere.[14]

HA STEP 3: USER RADIATION QUALITY-CONFORMANCE TEST

A user radiation quality-conformance test on I_{SK} at 1x and 5x fluences is recommended in table 8. In figure 17 for the SN54L00 gate, the output transistor gain h_{FEQ3} is given by

$$h_{FEQ3} = \frac{I_{SK}}{I_{BQ3}} \quad ,$$

---

[14] Allan H. Johnston and Robert L. Skavland, Terminal Measurements for Hardness Assurance in TTL Devices, IEEE Trans. Nucl. Sci. NS-22 (December 1975), 2303.

where

$$I_{BQ3} = I_1 + I_3 \cong \frac{V_{CC} - 3\,V_{BE}}{R_1} + \frac{V_{CC} - V_{CE(SAT)Q2} - V_{BE}}{R_2} - \frac{V_{BEQ3}}{R_3} \quad .$$

I_{SK} is measured with the input in the high state and with a voltage supply attached to the output and adjusted until the output voltage measured at the collector of Q3 is greater than $V_{CE(SAT)Q3}$ (greater than about 1 V). Since this drives Q3 out of saturation and the base current is held constant, I_{SK} (the current into the output terminal) is proportional to the output transistor (Q3) gain.

The damage factor can then be calculated using[16]

$$K_D = \Delta(1/h_{FEQ3})/\Phi \quad .$$

For the SN54L00, assume V_{CC} is 5 V, V_{BE} is 0.7 V, and $V_{CE(SAT)Q2}$ is 0.2 V. Then I_{BQ3} is approximately

$$I_{BQ3} \cong \frac{5 - 3(0.7)}{4 \times 10^3} + \frac{5 - 0.2 - 0.7}{2 \times 10^4} - \frac{0.7}{1.2 \times 10^4}$$

$$\cong \frac{5 - 0.9}{2 \times 10^4}$$

$$\cong 0.2 \text{ mA} \quad .$$

Assuming that the base current is constant at this value, the damage factor can be calculated from the previous equations. An example of the calculation is given in table 9 for 10 samples. The cumulative distribution of the data, together with the lot worst-case probability calculated from the methods of section 1.5, is plotted in figure 18. Future lots of SN54L00 units are accepted or rejected for user quality level 2 in a sample of 10 by the factor

$$\frac{m - 35.30}{s} \geq 1.4$$

for minimum lot quality of 80 %.

---

[16] Allan H. Johnston and Robert L. Skavland, Neutron Hardness Assurance Techniques for TTL Integrated Circuits, IEEE Trans. Nucl. Sci. NS-21 (December 1974), 393.

TABLE IX. CALCULATION OF OUTPUT TRANSISTOR DAMAGE FACTOR FROM I_{SK} MEASUREMENTS OF SN54L00 TTL GATE

Sample No.	I_{SK} (1) (mA)	$h_{FE\phi}$ (1)	$\Delta 1/h_{FE}$ (1)	K_D ($\times 10^{-16}$)	$\ell n K_D$	% Cumulative Distribution
1	3.68	18.4	0.021	2.10	-36.10	9.1
2	3.54	17.7	0.023	2.32	-36.00	18
3	3.46	17.3	0.024	2.44	-35.95	27
4	3.34	16.7	0.026	2.64	-35.87	36
5	3.30	16.5	0.027	2.72	-35.84	45
6	3.24	16.2	0.028	2.83	-35.80	54
7	3.16	15.8	0.030	2.98	-35.75	64
8	3.08	15.4	0.032	3.16	-35.69	73
9	2.98	14.9	0.034	3.39	-35.62	82
10	2.86	14.3	0.037	3.67	-35.54	91

(1) I_{SK}, $h_{FE\phi}$ and $\Delta 1/h_{FE}$ are the values after 1×10^{14} n/cm^2. The preirradiated I_{SK} was calculated to be 6 mA from an assumed preirradiated h_{FE} of 30 (the preirradiated values were not available).

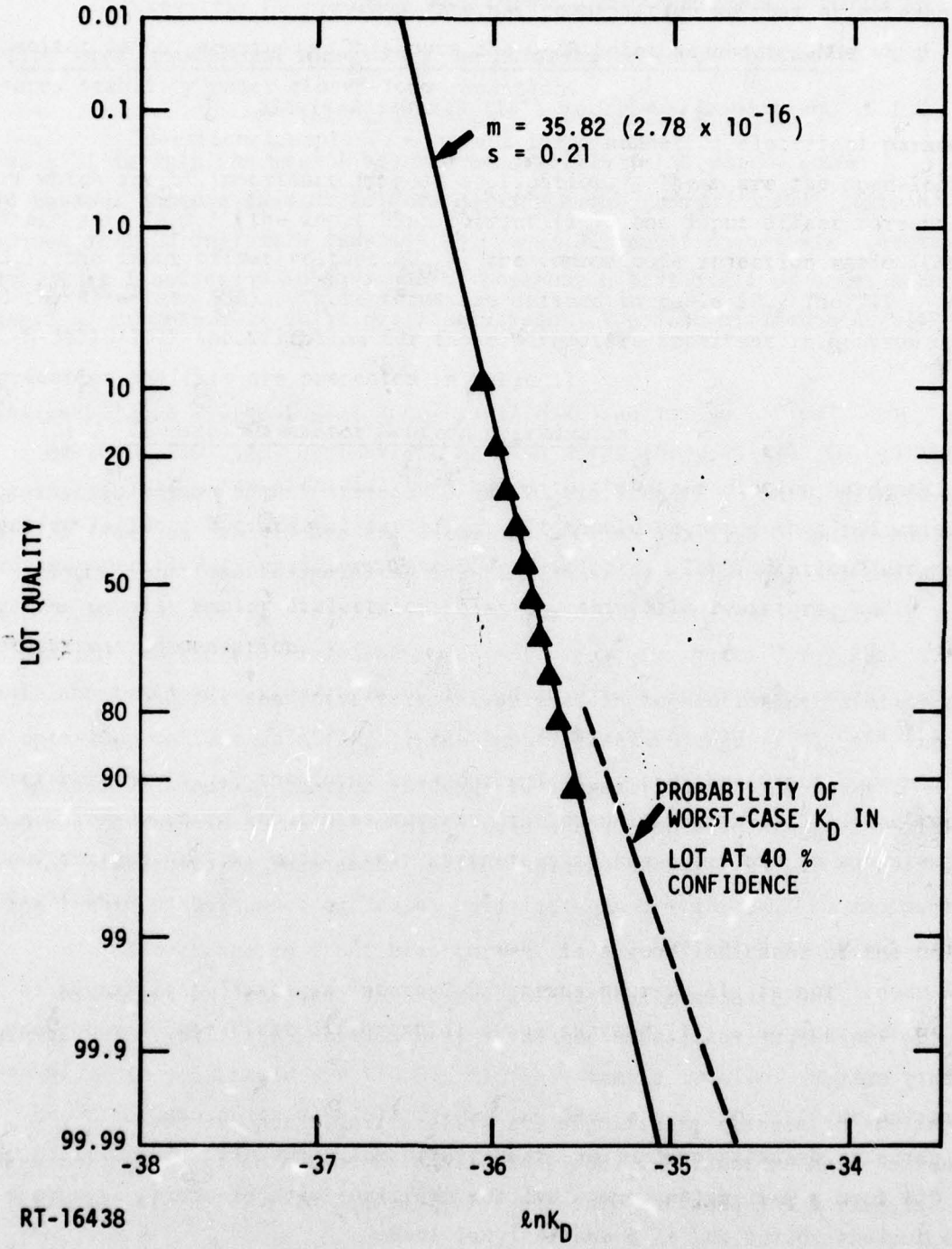


Figure 18. SN54L00 output transistor ℓnK_D cumulative statistics.

7. HA CONTROLS FOR OPERATIONAL AMPLIFIERS (741)

7.1 Effects of Neutron Radiation on Operational Amplifiers (Type 741)

7.1.1 Operational Amplifier (741) Circuit Analysis

One of the major differences between linear and digital IC's is the internal device current dependence on complex current sources instead of resistors. Since each linear IC type uses somewhat different current sources, it makes sense to limit this discussion to one type of operational amplifier, the 741. A schematic of the 741 operational amplifier is presented in figure 19.[18]

The 741 operational amplifier input stage employs a differential amplifier (Q7, Q8, Q9, Q10) which uses an active load (Q11, Q12, Q13) to develop high gain.[18] Transistors Q7 and Q8 operate in the common collector mode and Q9 and Q10 in the common base mode. Q9 and Q10 act as level shifters to isolate the input from V_{CC} and V_{EE}. The differential amplifier output comes from the collectors of Q10 and Q12. Transistors Q1, Q2, Q3, Q4, Q5, and Q6 are used for biasing purposes. The PNP transistors Q1, Q2, Q5, Q6, and Q10 are lateral PNP devices with an h_{FE} of about 4, while the NPN transistors are all high-gain (not "super-gain") devices.

Feedback stabilization of the bias current of the differential amplifier stage is provided by the bias current source comprising Q5 and Q6. Resistors R3 and R5 allow an external offset adjustment to compensate for differences in transistor characteristics (a pot is connected to pins 1 and 5 with the wiper connected to -15 Vdc).

The principle function of the output stage of the 741 is to provide low output resistance and large load current capability. The complementary emitter follower transistors Q16 and Q17 are biased for Class AB operation by Q15. Q17 has a vertical (substrate) PNP structure. Q18 and Q19 serve as overload protection, they are normally cut off. Transistors Q13 and Q14 form a Darlington common emitter amplifier with Q1 acting as both a bias current source and as a small-signal load.[18]

---

[18] D. J. Hamilton and W. G. Howard, Basic Integrated Circuit Engineering, McGraw-Hill (1975).

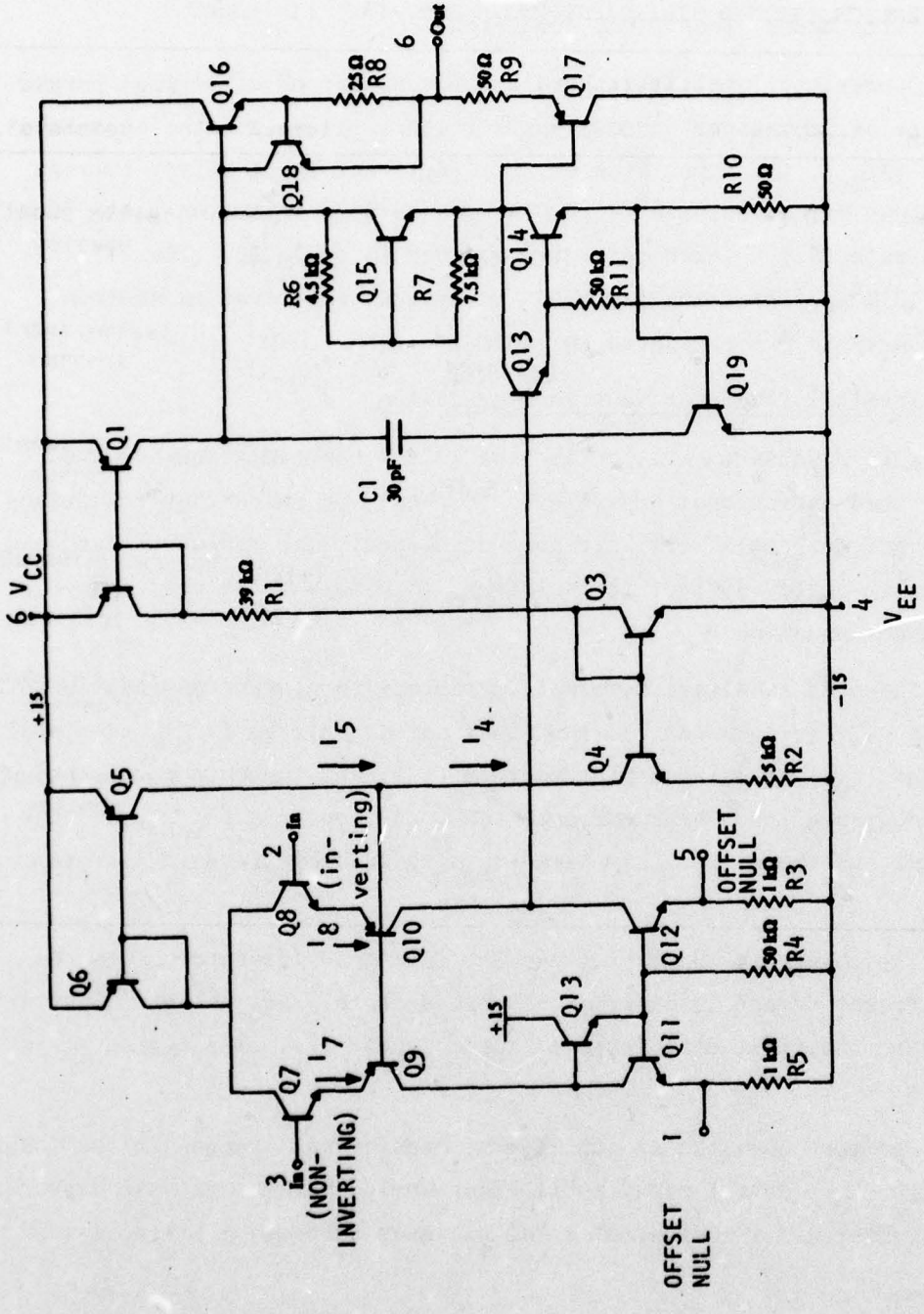


Figure 19. 741-type operational amplifier schematic.

Capacitor C1 provides internal compensation so that an external capacitor is not required. This puts the 0-dB point at about 1 MHz which insures stability under closed-loop condition.

Operational amplifiers have a large number of electrical parameters which are of importance in most applications. These are the open-loop voltage gain (A_{VOL}), the input bias current (I_B), the input offset current (I_{OS}), the input offset voltage (V_{OS}), the common mode rejection ratio (CMMR), and the slew rate (SR). These terms are defined in table 10. The 741 MIL-M-38510/101E specification for those parameters important in neutron degradation analysis are presented in table 11.

7.1.2 Terminal Parameter Neutron Degradation

This discussion will be limited to the non-radiation-hardened, junction-isolated operational amplifier. It should be noted that radiation-hardened operational amplifiers have been developed. The radiation-hardened versions usually employ dielectric isolation, thin-film resistors, and photocurrent compensation.

The most sensitive terminal parameters to neutron degradation are the open-loop voltage gain (A_{VOL}), the input offset voltage (V_{OS}), the input offset current (I_{OS}), the input bias current (I_B), and the output current. The neutron-degraded input bias current, the open-loop gain (A_{VOL}), and the output current are the most likely parameters to cause failure in a system application.

The change in input bias current is a good indicator of the onset of significant damage in internal NPN transistors. ΔI_B is not linear with fluence because the first differential stage current (I_I) also degrades with fluence.

For most operational amplifiers, significant changes in the input offset voltage (V_{OS}) do not occur until other device parameters have degraded. For example, after 2.3×10^{12} n/cm^2 a 741 has only suffered a 5 % rise in

---

[18] D. J. Hamilton and W. G. Howard, Basic Integrated Circuit Engineering, McGraw-Hill (1975).

TABLE X. OPERATIONAL AMPLIFIER DEFINITIONS

Term	Definition
Large Signal Voltage Gain (A_{VOL})	Ratio of maximum output voltage swing to change in input voltage required to drive output to this voltage.
Input Bias Current (I_B)	Average of two input currents at 0 output voltage.
Input Offset Current (I_{OS})	Difference in currents inot two input terminals with output at 0 V.
Input Offset Voltage (V_{OS})	That voltage which must be applied between input terminals to obtain 0 output voltage.
Common Mode Rejection Ratio (CMRR)	Ratio of change of input offset voltage to input common mode voltage change producing it (decibels).
Slew Rate (SR)	Maximum rate of change of output voltage under large-signal conditions.
Output Short Circuit Current ($I_{OS(+)}$)	Maximum output current available from amplifier with output shorted to ground or to either supply.
Supply Current (I_{CC})	Current required from power supply to operate amplifier with no load and zero output.

TABLE XI. 741-TYPE MIL-M-48510/101E SPECIFICATIONS

Parameter	Symbol	Test conditions (T_A = 25°C)	Minimum	Maximum	Units
Input offset voltage	V_{IO} (V_{OS})	R_S = 50 Ω 883B-4001	-3.0	+3.0	mV
Input offset current	I_{IO} (I_{OS})	883B-4001	-30	+30	nA
Input bias current	I_{IB} (I_B)	883B-4001	1	110	nA
Output short-circuit current	$I_{OS(+)}$	$+V_{CC}$ = 15 V	-60	-	mA
	$I_{OS(-)}$	883B-3011	-	60	mA
Supply current	I_{CC}	$+V_{CC}$ = ±15 V 883B-4005	-	3.8	mA
Open-loop voltage	Avs	$\pm V_{CC}$ = 20 V, R_L = 2K, 10K	50	-	V/mV
	(A_{VOL})	V_{OUT} = ±15 V, 883B-4004			

V_{OS} but a 300 % rise in I_B and a 65 % increase in I_{OS}.[19]

The output current can be an important determination of margin for neutron damage evaluation. How important it is depends on the configuration of the output state.[19,20]

The open-loop gain degrades with neutron fluence but it does not change in a smooth predictable way. In addition, the measurement and interpretation of the open-loop gain is not straightforward. The open-loop voltage gain must be carefully measured and defined if meaningful interpretations are required of the degradation of this parameter in irradiation environment. The best approach is to measure the transfer characteristic in a loaded and unloaded condition and define the gain in terms of the maximum input voltage required to drive the output voltage through a given range.[20] The reason for this is that many manufacturers specify a dc measurement for A_{VOL}, forcing the output from a negative to positive voltage with a fixed-load resistor. However, there are several problems with this definition which makes it unsuitable for evaluating irradiated devices, as is pointed out by Johnston.[20] These problems are

(1) Most modern operational amplifiers have a 3-dB corner frequency in the 1 to 10-Hz region before irradiation and thus it is important that the test time be sufficiently long to establish equilibrium.

(2) It is impossible to distinguish between small drifts in offset voltage and the small (10 to 15 mV) change in the dc input voltage which is expected for the dc gain measurement.

(3) The output stage has a significant effect on the open-loop gain. The gain is a function of the load conditions and there is a large difference in the gain between

---

[19] Allan H. Johnston, Application of Operational Amplifiers to Hardened Systems, IEEE Trans. Nucl. Sci. NS-24 (December 1977), 2071.

[20] Allan H. Johnston, Hand Analysis Techniques for Neutron Degradation of Operational Amplifiers, IEEE Trans. Nucl. Sci. NS-23 (December 1976), 1709.

loaded and unloaded conditions. The gain in the loaded condition is also very nonlinear which confuses the definition of gain and allows contradictory results.

For neutron radiation most operational amplifiers are useful up to about 10^{14} n/cm^2. They suffer a considerable loss in the open-loop gain at this radiation level, but are usable in conservative circuit design where the closed-loop gain is kept at about 100 or more. This assumes that the changes in input bias current and input offset current, both of which increase with neutron fluence, are acceptable.

7.1.3 Special Methods for HA Controls

In addition to examining the neutron sensitivity of existing device terminal parameters for possible HA controls, two special methods have been proposed: (1) special leads for the output transistor and (2) a high-frequency ac probe wafer measurement. In the latter method,[21] a commercially available high-frequency ac probe is used for making measurements on the elements of the integrated circuits on the wafer. This can be used as a 100-percent screen of the elements in an IC or on breakout transistors. It is used in the early stages of the manufacturer's process. Bascially, the technique measures the minority carrier delay time of each transistor element with a temporary metallization pattern. The temporary pattern is removed after the measurement and an operational one is applied. In this technique the silicon damage constant is assumed to be constant with current and the total minority delay time is used and obtained from S-parameter measurements. By applying this technique at the wafer stage, significant savings were realized[21] through eliminating IC's with poor radiation performance before the costly packaging stage. This was found to be especially true for higher reliability IC's and hybrids where the package level yield can be quite low.

Special leads attached to the output transistor have also been proposed as a possible HA tool.[17] Since the output transistor uses the same

---

[17] I. Arimura, A Study of Electronics Radiation Hardness Assurance Techiques, Air Force Weapons Laboratory-TR-73-134 (January 1974).

[21] R. A. Bailey et al., A Neutron Hardness Assurance Screen Based on High Frequency Probe Measurements, IEEE Trans. Nucl. Sci. NS-23 (December 1976), 2020.

process sequence for base doping and base width, an extra lead or two may provide the necessary parameters for worst-case predictions and comparisons of IC's. Also, since the output transistor has the largest area and thus the largest input capacitance it should have the largest composite damage constant. The problem with examining only the output transistor is that both PNP and NPN transistors are usually on the same monolithic chip and the PNP units have a different damage constant.

7.1.4 Operational Amplifier HA Considerations

It has been pointed out that several terminal operational amplifier parameters degrade with neutron fluence, but they do so in a non-predictable manner and hence are not good parameters for evaluating neutron damage except perhaps in special cases. In order to be effective, it has been suggested that an HA program must consider[19]

(1) internal operating margins,
(2) the damage factors of the internal transistors, and
(3) the gain of the internal transistors.

All three of the above HA factors depend on the internal currents in the device. The most important internal current is the first stage current I_I. This parameter should be controlled within established limits. For externally compensated operational amplifiers, I_I can be measured at the balance or strobe terminal (pin 1 in the LM108A). For internally compensated units such as the 741, the measurement cannot be made on the standard package; either a special lead needs to be brought out to the unused pin 8 on the package or I_I needs to be estimated from the slew rate.[19]

The input stage current of the 741 ($I_7 + I_8$ in figure 7.1) is derived from the collector of Q6. The Q5 collector current (I_5 in figure 7.1) also is equal to ($I_7 + I_8$), which in turn is approximately equal to I_4, the stabilized current. Thus any point which allows the monitoring of ($I_7 + I_8$) can be brought out to pin 8 for HA monitoring.

---

[19]Allan H. Johnston, Application of Operational Amplifiers to Hardened Systems, IEEE Trans. Nucl. Sci. NS-24 (December 1977), 2071.

There are four general types of bipolar transistors which can be encountered in commercial operational amplifier designs: (1) normal NPN transistors, (2) super-gain NPN transistors, (3) lateral PNP transistors, and (4) vertical (substrate) PNP transistors.[20] The sensitivity of these individual devices to neutron damage varies widely because of differences in topology, doping levels, and base width. Table 12 lists the relevant characteristics of the four transistor types while figure 20 gives a comparison of the structure.

The lateral PNP transistors in the 741 and other operational amplifiers have lower gain and suffer more neutron damage than other NPN and PNP constituent transistors. This is because the latent PNP transistor is a wide base device owing to masking tolerances and side-wall diffusion. Johnson[19] gives a mean lateral PNP damage factor of 3.5×10^{-4} and shows a tighter distribustion than the NPN transistors. The mean K_D for the worst lot for the NPN input transistor for 38510 versions of the 741 was 0.7×10^{-14} cm^2/n.[19]

Transistor Q17 in the 741 schematic in figure 19 is the only vertical (substrate) PNP transistor in the IC. It has a smaller base width than the lateral PNP devices and is thus less sensitive to neutron effects (but it is still more sensitive than NPN devices).

7.2 Proposed HA Controls for Supplier-Qualified Radiation Parts

Operational amplifier failure may occur because of severe neutron degradation of any one parameter, depending upon the application of the operational amplifier. Thus, it is difficult to fully anticipate the end usage of an operational amplifier so that cost-effective supplier HA controls can be implemented. For example, the open-loop gain degradation which can be accepted for an amplifier operated with a closed-loop gain of a thousand is

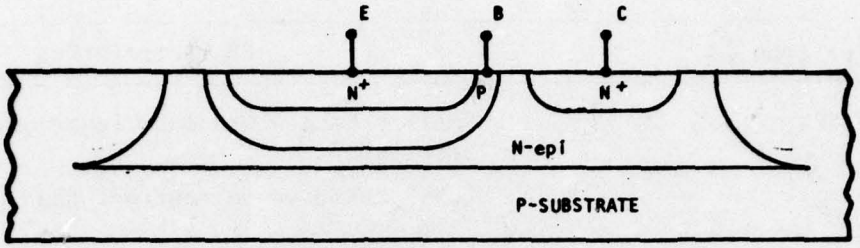
---

[19] Allan H. Johnston, Application of Operational Amplifiers to Hardened Systems, IEEE Trans. Nucl. Sci. NS-24 (December 1977), 2071.

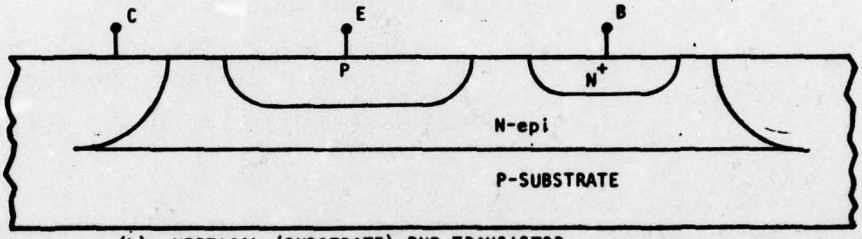
[20] Allan H. Johnston, Hand Analysis Techniques for Neutron Degradation of Operational Amplifiers, IEEE Trans. Nucl. Sci. NS-23 (December 1976), 1709.

TABLE XII. IC TECHNOLOGY COMPARISON

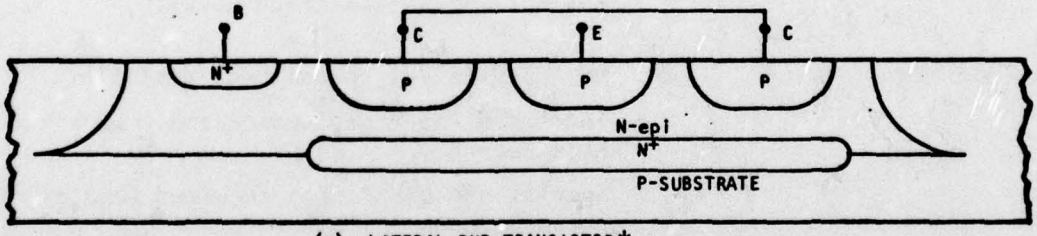
Transistor type	Characteristics
Standard NPN	1. Smaller base width and higher gain than PNP transistor.
	2. Less sensitive to neutrons than PNP units.
Vertical (substrate) PNP	1. Wider base widths than NPN units but smaller than lateral PNP.
	2. More sensitive to neutrons than NPN units.
	3. Low current gain ($\beta \sim 50$).
	4. Increased base resistance over NPN means lower onset of current crowding.
	5. Useful as emitter followers (Q17 in figure 20 for the 741).
Lateral PNP	1. Wide base device, hence low-frequency operation and severe neutron damage.
	2. Low current gain (maximum $\beta \sim 10$).
	3. Q1, Q2, Q5, Q9, and Q10 are lateral PNP devices in the 741 (Figure 20).
Super-gain NPN	1. Not used in 741 operational amplifier.
	2. Increases input resistance and lowers input bias current.
	3. Special circuit design required to prevent punch-through.
	4. Base width less than 0.1 μm and β greater than 2000.
	5. Requires an extra emitter diffusion.



(a) STANDARD NPN IC TRANSISTOR



(b) VERTICAL (SUBSTRATE) PNP TRANSISTOR



(c) LATERAL PNP TRANSISTOR*

RT-16444

*D. J. Hamilton and W. G. Howard, Basic Integrated Circuit Engineering, McGraw-Hill (1975).

Figure 20. A comparison of transistor cross sections.

much less than can be accepted for an amplifier operating with a closed-loop gain of only 10.

On the other hand, there are process controls that the supplier needs to impose. Transistor base width, base doping, and configuration controls need to be imposed. These process controls are listed in table 13.

Several HA screens have been proposed for the 741 operational amplifier to allow more control over the degraded distributions than the electrical parameters normally specified. These include

(1) measurement of the first stage bias current (I_I) with a screen to discard devices with abnormally low or high values of bias current,[19]

(2) specification and measurement of the open-loop voltage gain (A_{VOL}) with a screen to discard devices with abnormally low values, since this correlates moderately well with the post-irradiation ΔA_{VOL},[17] and since none of these screens has been proven to be cost-effective as yet none are recommended at the present time.

Radiation quality-conformance tests need to be made on those parameters which are of most importance to design engineers in the typeical application of 741-type operational amplifiers in a neutron environment. These include the input bias current (I_B), the output short-circuit current (I_{OSC}), and the open-loop voltage gain (A_{VOL}). These are listed in table 13.

7.3 Proposed HA Controls for User-Qualified Radiation Parts

The user screens (table 14) follow the supplier screens of table 13 in that none have been determined to be really cost-effective at the present time.

---

[17] I. Arimura, A Study of Electronics Radiation Hardness Assurance Techniques, Air Force Weapons Laboratory-TR-73-134 (January 1974).

[19] Allan H. Johnston, Application of Operational Amplifiers to Hardened Systems, IEEE Trans. Nucl. Sci. NS-24 (December 1977), 2071.

TABLE XIII. OPERATIONAL AMPLIFIER SUPPLIER-QUALIFIED PART PROCUREMENT SPECIFICATION EXAMPLE (741)

HA controls	Parameter	Test Method	Test Conditions	Control level failure criteria (S-2)	Control level failure criteria (S-1)	Units
Process controls	Base width	(1)	-	±10%	±10%	μm
	Base doping	(1)	-	±10%	±10%	cm^{-3}
	Configuration	-	-	-	-	-
Radiation[2] quality-conformance test	Input bias current (I_B)	883B-4001	-	-	(1)	nA
	Output short circuit current (I_{OSC})	883B-3011	V_{CC} = 15 V	-	(1)	mA
	Gain (A_{VOL})	883B-4004	(3)	-	(1)	V/mV

NOTES: (1) To be determined.

(2) Radiation tests are read and recorded on 10 samples at 1×10^{12}, 1×10^{13}, 1×10^{14} n/cm^2.

(3) V_{CC} = 20 V, V_{OUT} = 15 V, R_L = 2k.

TABLE XIV. OPERATIONAL AMPLIFIER USER-QUALIFIED PART PROCUREMENT SPECIFICATION EXAMPLE (741)

HA controls	Parameter	Test methods	Test conditions	Quality level failure criteria (S-2)	(S-1)	Units
Radiation[1] quality-conformance test	Input bias current (I_B)	883B-4001	Determined by the circuit	1x(80%)	5x(80%)	mA
	Output short-circuit current (I_{OSC})	883B-3011				
	Gain (A_{VOL})	883B-4004				V/mV

Note: (1) Radiation tests are read and recorded on 10 samples.

User radiation quality-conformance tests would be done on that parameter which is deemed to be most important inthe intended application of the operational amplifier. For example, if open-loop voltage gain is the primary parameter for concern in the intended application and the other parameters are of lesser importance, then a lot quality-conformance test on the open-loop voltage gain amplitude should be employed.

User level 2 criteria are set at 80% (at 90 % confidence) at 1x fluence on the low worst-case expectation. User level 1 criteria (greater than 80%) are set at 80 % (at 90 % confidence) at the 5x fluence.

7.4 HA Example Using 741 Operational Amplifier

In this example it is assumed that the 741 operational amplifier was chosen for the circuit because it met electrical and radiation (3×10^{13} n/cm^2) specifications. The radiation specification of 3×10^{13} n/cm^2 is high for the 741, so the device has been placed in an HA procurement category 1 which requires screens and radiation quality-conformance testing. Analysis of the circuit in which the 741 is to be used shows the critical parameter to be the open-loop gain, A_{VOL}. The failure criteria is 2 V/mV at 3×10^{13} n/cm^2 with a lot quality of 80 % desired.

HA STEP 1: PROCUREMENT

Since category 1 parts require screens and process controls, a supplier level 2 part should be purchased.

HA STEP 2: ELECTRICAL SCREEN

No electrical screens for supplier level 2 parts are recommended.

HA STEP 3: USER RADIATION QUALITY CONFORMANCE TEST

Since A_{VOL} is the sensitive parameter, a radiation test is carried out at 1x (3×10^{13} n/cm^2) on 10 samples. The data on

$$\ell n \left[1/A_{VOL(PRE)} - 1/A_{VOL(POST)} \right]$$

is plotted on normal probability paper (figure 21). The limit L_σ can be calculated at the 80 % point on 10 samples using the method of section 1.5 to be

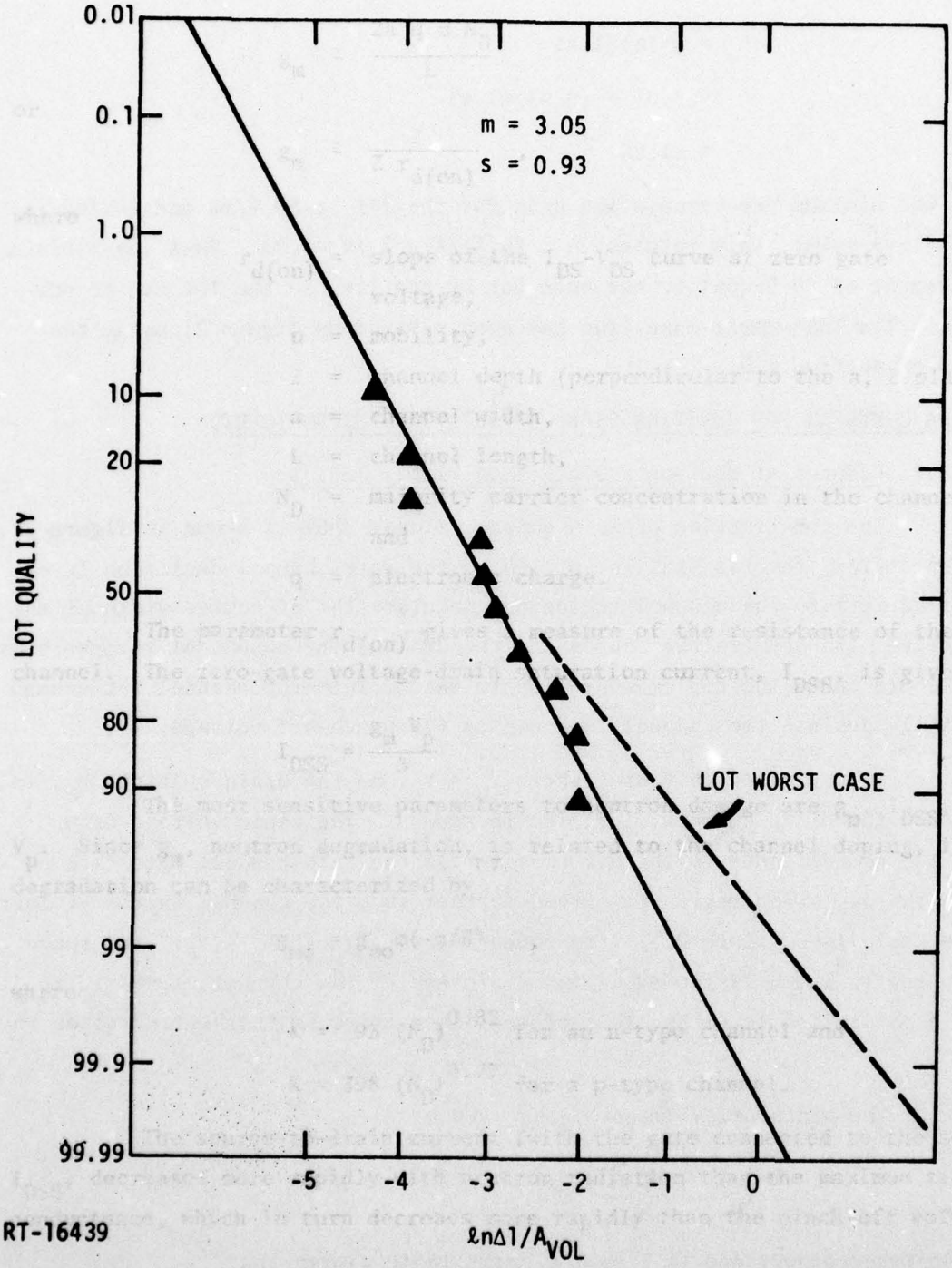


Figure 21. Type 741 open-loop gain degradation ($\Delta I/A_{VOL}$) at 3×10^{13} n/cm^2.

$$L_\sigma = m+(s)(1.4)$$

$$= 3.05 + (0.93)(1.4)$$

$$= -1.75 \quad .$$

Since the minimum pre-irradiation gain for the 741 is 50 V/mV and 2 V/mV is the failure point, this results in a $\ln[\Delta 1/A_{VOL}]$ of -0.73. Thus the minimum requirement of 80 % quality has been met by the lot, so the lot can be purchased. The lost worst-case line has been plotted on figure 21 using the method of section 1.5.

8. HA CONTROLS FOR JUNCTION FIELD EFFECT TRANSISTORS (JFET)

8.1 Effects of Neutron Radiation on Planar JFET's

The construction of an N-channel planar JFET is shown in figure 22. In this device, reverse bias is applied to the gate-channel depletion layer to extend it into the channel region and modulate the effective width of the conductive path between the source and the drain. The amount of reverse bias which would cause the depletion region to extend into the channel far enough to totally deplete the channel is known as the pinch-off voltage, V_p.

At any given gate bias where $V_G < V_p$, as the drain voltage, V_D, is increased the drain current, I_D, also increases. The ohmic voltage drop along the channel adds to the net bias across the gate-channel interface and causes the depletion region to extend further into the channel in the vicinity of the drain (see figure 22). Consequently, when $V_D \geq (V_p - V_G)$, the space charge region which is formed at the drain end of the channel causes I_D to reach a saturation level and thus become insensitive to further increases in V_D.

The pinch-off voltage V_p is given by

$$V_p = \frac{a\, N_D\, a^2}{2e}$$

and the transconductance (g_m) by the approximate expression,[17]

---

[17] I. Arimura, A Study of Electronics Radiation Hardness Assurance Techniques, Air Force Weapons Laboratory-TR-73-134 (January 1974).

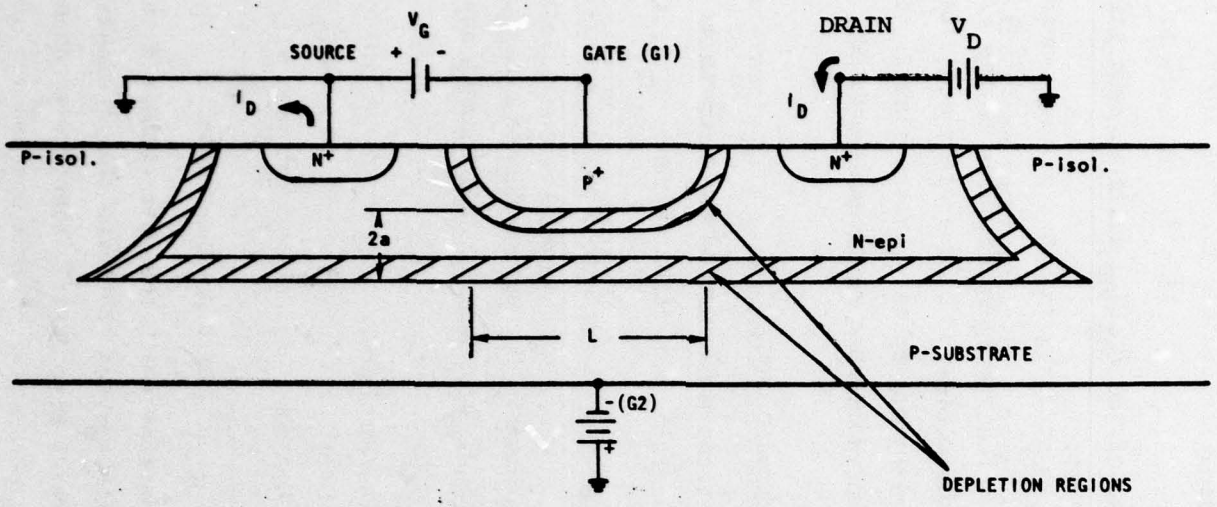


Figure 22. N-channel JFET cross section

$$g_m \cong \frac{2a\ q\ u\ N_D}{L}$$

or

$$g_m \cong \frac{2}{Z\ r_{d(on)}} \quad ,$$

where

$r_{d(on)}$ = slope of the I_{DS}-V_{DS} curve at zero gate voltage,

u = mobility,

Z = channel depth (perpendicular to the a, L plane),

a = channel width,

L = channel length,

N_D = majority carrier concentration in the channel, and

q = electronic charge.

The parameter $r_{d(on)}$ gives a measure of the resistance of the channel. The zero-gate voltage-drain saturation current, I_{DSS}, is given by

$$I_{DSS} = \frac{g_m\ V_p}{3} \quad .$$

The most sensitive parameters to neutron damage are g_m, I_{DSS}, and V_p. Since g_m, neutron degradation,[17] is related to the channel doping, its degradation can be characterized by

$$g_{m\phi} = g_{mo} e(-\phi/K) \quad ,$$

where

$K = 93\ (N_D)^{0.82}$ for an n-type channel and

$K = 398\ (N_D)^{0.77}$ for a p-type channel.

The source-to-drain current (with the gate connected to the source) I_{DSS}, decreases more rapidly with neutron radiation than the maximum transconductance, which in turn decreaes more rapidly than the pinch-off voltage.[11]

---

[11] R. P. Donovan et al., A Survey of the Vulnerability of Contemporary Semiconductor Components to Nuclear Radiation, Air Force Avionics Laboratory TR-74-61 (June 1974).

[17] I. Arimura, A Study of Electronics Radiation Hardness Assurance Techniques, Air Force Weapons Laboratory-TR-73-134 (January 1974).

Calculated and experimental decreases of these three parameters with neutron fluence leads to the selection of I_{DSS} as the most sensitive electrical parameter for neutron effects.

The effect of neutrons on JFET's is to induce carrier removal in the neutron channel region and to induce channel modulation because of traps in the gate depletion region. This leads to observed lower values for the zero-gate voltage-drain current (I_{DSS}), the maximum transconductance (g_m), and the pinch-off voltage (V_p). Large dopant concentrations make the carrier removal less significant. Since the dopant levels are usually in the 10^{16} atoms/cm range for planar structures, fluences of less than 10^{14} n/cm^2 would cause less than a 1 % change in the carrier concentration. For heavily doped channels (about 3 x 10^{16} cm^2), N-channel JFET's will suffer a 50 % degradation in the source to drain current at about a fluence of 2 x 10^{15} n/cm^2.[11] Lighter doped channels will fail at a lower fluence and higher doped channels at a higher fluence.

Neutron-induced damage data for P-channel JFET's is less plentiful because P-channel JFET's are less plentiful. Their lower carrier mobility produces lower transconductance than the N-channel JFET's, but their radiation sensitivity should be only slightly inferior to the N-channel units.

8.2 HA Controls for Supplier-Qualified Parts

Various authors[5,11,17] have identified the following candidate screens: BV_{GSS} (the gate-to-source breakdown voltage), $r_{d(on)}$ (the slope of the I_{DSS}-V_{DS} curve at zero gate voltage), and g_{mo} (the pre-irradiated transconductance).

Since g_m, I_{DSS}, and V_p are all related to channel doping and channel configuration, process controls on the channel doping and configuration need to be imposed for meaningful statistics.

---

[5] A. R. Hart et al., Parameter Sensitivities for Hardness Assurance: Displacement Effects in Bipolar Transistors, Final Report, Mission Research Corporation Report MRC/SD-R-20 (December 1977).

[11] R. P. Donovan et al., A Survey of the Vulnerability of Contemporary Semiconductor Components to Nuclear Radiation, Air Force Avionics Laboratory TR-74-61 (June 1974).

[17] I. Arimura, A Study of Electronics Radiation Hardness Assurance Techniques, Air Force Weapons Laboratory-TR-73-134 (January 1974).

AD-A065 161 IRT CORP SAN DIEGO CALIF F/G 18/6
HARDNESS ASSURANCE GUIDELINES FOR DISPLACEMENT EFFECTS FOR BIPO--ETC(U)
MAY 78 R A BERGER DAAG39-77-C-0135
UNCLASSIFIED IRT-8166-003 HDL-CR-78-135-1 NL

2 OF 2
AD
AD65131





END
DATE
FILMED
4-79
DDC

Although I_{DSS} is the most sensitive parameter to neutron degradation, radiation data on this parameter is not recommended because JFET's are not a problem in moderate neutron environments.

An example supplier procurement specification for the N-channel 2N4220 JFET is given in table 15.

8.3 Proposed HA Controls for User-Qualified Parts

Channel doping and configuration must be maintained for meaningful statistics, therefore supplier level 2 parts should be specified if available.

Radiation tests should be made on those parameters which have been determined by circuit analysis to be the most important in the intended application. The most important parameters for neutron effects are usually I_{DSS} and g_m.

An example of a user procurement specification for the N-channel 2N4220 JFET is given in table 16.

9. SUMMARY

The *objective* of the contract was to provide an effective means of purchasing semiconductor devices whose neutron-induced response is within known and acceptable limits. The *scope* of the contract was limited to those procedures for the neutron environment for bipolar transistors, zener diodes, TTL (54/74) series digital IC's, 741-type operational amplifiers, and JFET's. The objective was met by imposing two levels of HA controls on both the supplier and the user. These control and quality levels are summarized in table 17 for the supplier and in table 18 for the user. Notice that for the supplier the levels are called control levels, whereas for the user they are quality levels. For the supplier the difference between levels 1 and 2 is the number of HA controls to which the part is subjected in order to be qualified (control level 2 requires screens and process controls, and radiation tests in an inspection lot are added to achieve level 1). For the user the difference between the quality levels is the difference between the quality of the lot, with 80 % lot quality considered to be the breakpoint. The reason for choosing the 80 % lot quality point is based upon the restriction of the sample size to 10 devices. A sample of 10 devices will yield

TABLE XV. JFET SUPPLIER-QUALIFIED PART PROCUREMENT SPECIFICATION EXAMPLE (2N4220)

HA controls	Parameter	Test method	Test conditions	Control level failure criteria (S-2)	Control level failure criteria (S-1)	Units
Process controls	Channel doping	(1)	-	±10%	±10%	cm^{-3}
	Configuration	-	-	-	-	-
Radiation[2] quality-conformance test	I_{DSS}	750B-3413	V_{DS} = 15V, V_{GS} = 0	-	(2)	mA

Notes: (1) To be determined.

(2) Radiation tests are not recommended at the supplier level.

TABLE XVI. JFET USER-QUALIFIED PART PROCUREMENT SPECIFICATION
EXAMPLE (2N4220)

HA controls	Parameter	Test method	Test conditions	Quality level failure criteria (S-2)	(S-1)	Units
Radiation quality-conformance test (1)	I_{DSS}	-	(2)	1x(80%)	5x(80%)	mA
	g_m		(2)			μ mhos

NOTES: (1) Radiation tests are read and recorded on 10 samples.
(2) Determined by the circuit application.

80 % lot quality without extrapolating the statistics to some unknown point.

9.1 Supplier Control Levels

Table 17 is a summary of supplier control levels. The supplier is defined to be the manufacturer, testing contractor, or any other organization which qualifies parts for more than one specific system application. This means that the supplier must specify all those parameters which may be used by various systems in many different applications. *The philosophy of the supplier controls is not to put tight tolerance limits on the manufacturer so that a significant number of parts would be rejected, but merely to call for the specification and maintenance of any important neutron-sensitive parameter so that lot-to-lot variability is reduced.*

For transistors, supplier HA process controls are required on the base width, the sheet resistivity, and the configuration. Two screens have been identified for HA controls which will reduce the radiation response variability. These screens are the minimum pre-irradiated common emitter current gain and the minimum gain bandwidth product. These screens are applied at supplier control levels 2 and 1. Note that the minimum h_{FEO} is already a screen for transistors.

The parameter required for the transistor radiation test is $\Delta(1/h_{FE})$, from which K_D can be calculated. This test is performed on ten samples to give reasonable statistics at 20%, 50%, and 80% degradation in $1/h_{FE}$.

No effective HA controls have been identified for temperature-compensated silicon reference: a discussion of these devices appears in section 5 of this document but they do not appear in tables 17. Non-temperature-compensated reference diodes are inherently hard to neutron radiation: units are available which exhibit only a 1 % change in the zener voltage at fluences of 1×10^{14} n/cm^2.[11]

For TTL's the base width, base doping, and configuration are process controls which need to be imposed. TTL's are inherently hard to

[11] R. P. Donovan et al., A Survey of the Vulnerability of Contemporary Semiconductor Components to Nuclear Radiation, Air Force Avionics Laboratory TR-74-61 (June 1974).

TABLE XVII. SUMMARY OF SUPPLIER HA CONTROL LEVELS

Category	Parameter	Type of HA control	Supplier control level S-2	Supplier control level S-1
Transistors	Maximum base width and base doping	P	±10%	±10%
	Configuration	P	TBS	TBS
	Minimum h_{FEO}	S	SS	SS
	Minimum f_T	S	SS	SS
	Maximum $\Delta(1/h_{FE})$	RT	-	TBS
TTL (54/74)	Base width and base doping	P	±10%	±10%
	Configuration	P	TBS	TBS
	I_{SK}	S	TBS	TBS
	I_{SK}	RT	-	TBS
Operational amplifiers	Base width and base doping	P	±10%	±10%
	Configuration	P	TBS	TBS
	Input bias current (I_B)	RT	-	TBS
	Output short-circuit current (I_{OSC})	RT	-	TBS
	Gain (A_{VOL})	RT	-	TBS
JFET	Channel doping and configuration	P	TBS	TBS

NOTES: TBS: To be specified and maintained by the manufacturers for each part type.

SS: Specification sheet value.

RT: Radiation test on 10 samples at 10^{12}, 10^{13}, 10^{14} (Read and Record).

P: Process controls

S: Screens

neutrons and no significant degradation occurs up to 10^{14} n/cm^2.

Operational amplifiers are not hard to the neutron environment and because of the variability encountered in these devices it is hard to specify effective screens. The open-loop gain and the input differential-stage bias current have been identified as screens which can reduce the variability of the radiation parameters of interest, but none of these screens are recommended until more data is accumulated on their effectiveness. The radiation parameters of interest are the input bias current, the output short-circuit current, and the open-loop gain.

For JFET's the process controls of interest are the channel doping and the channel configuration. Several screens have been identified as exercising some degree of control over the variability of the radiation response of the device, but none have been selected as being cost-effective. The drain-to-source saturated current is the most sensitive parameter to the neutron effects and hence is a good measure of where the device starts to go out of specification. JFET;s are inherently hard to neutron radiation with significant source-to-drain current degradation not occurring until 1 x 10^{15} n/cm^2.

9.2 User Quality Levels

The user is defined to be the organization which qualifies parts for one specific system application. The user has the advantage over the supplier of knowing (1) the application of the part to be qualified, and (2) the specification fluence. Thus the number of tests and the choice of parameters for those tests may be reduced.

The user procedure is to go through the specific system application and try to substitute parts or do other procedures so that the design margin is greater than 10. The design margin is defined to be the ratio of the degraded parameter to the failure level. If the design margin is greater than 10, this means that variations in part response to neutrons are small enough so that the design margin will not be exceeded and therefore the part will perform in the circuit as required. Thus the user does not need to have any HA controls (the part is a category 2 part). For systems with only moderate neutron environments (10^{12} n/cm^2 or less) design margins of 10 are common. For those few cases where the design margin cannot be made greater than 10,

we have what is flagged or defined to be a HA category 1 part. The flagging of the part with this designation merely means that HA controls in the form of screens and radiation quality-conformance tests must be applied to the procurement specification of the device. When these two HA controls are applied, the result is a user level 2 or a user level 1 part depending upon the statistics of the lot. A level 2 is for a quality of 80 % or 90 % confidence, level 1 is quality greater than 80 % at 90 % confidence.

Table 18 is a summary of the user HA specifications. Transistor radiation quality-conformance tests are done for the user quality level 2 at the 1x fluence specification and the lot 80 % point is calculated from statistics on the damage factor. To achieve lot quality above 80 % (user level 1), a radiation test at 5x is done and the mean of that data for the parameter $\Delta(1/h_{FE})$ will be the 99.9 % lot quality level.

For TTL's, operational amplifiers, and JFET's, the user HA control parameters generally follow those of the supplier. The supplier and user screens in all cases are identical. The radiation tests for user level 2 are done on the circuit-defined parameters of interest with 80 % lot quality calculated at 1x using the statistical method discussed in section 1.5 of this document. The radiation tests for user level 1 for TTL units are done at the 5x level using the mean of the sample data to determine the 99.9 % lot quality criterion. The radiation tests for user level 1 for operational amplifiers and JFET's are done at 5x on the radiation parameters of interest to achieve lot quality above 80 % (also using the statistics developed in section 1.5 of this document).

The method by which the user test at the 1x (80 % quality level) and at the 5x fluence levels is done is to use a radiation lot-sample test and an appropriate sample plan. These radiation tests are performed on a random sample of 10 devices from an inspection lot to place confidence limits on the device population. The statistical method is a variable sampling plan which uses one-sided tolerance limit factors for a normal distribution to identify the worst-case values for the device population.

TABLE XVIII. SUMMARY OF USER HA QUALITY LEVELS

Category	Parameter	Type of HA control	U-2 (Minimum 80% lot quality)	U-1 (Lot quality above 80%)
Transistor	Minimum h_{FEO}	S	SS	SS
	Minimum f_T	S	SS	SS
	$\Delta(1/h_{FE})$, K_D	RQCT	1x(80%,K_D) → 80%	5x(50%,$\Delta 1/h_{FE}$) → 99.9%
TTL (54/74)	I_{SK}	S	TBD	TBD
	I_{SK}	RQCT	1x(80%) → 80%	5x(50%) → 99.9%
Operational Amplifiers	Input bias current (I_B)	RQCT	1x(80%) → 80% on parameters of interest	5x(80%) → >80% on parameters of interest
	Output short-circuit current (I_{OSC})	RQCT		
	Gain (A_{VOL})	RQCT		
JFET	Drain-source current (I_{DSS})	RQCT	1x(80%) → 80% on parameters of interest	5x(80%) → 80% on parameters of interest
	Transconductance (g_m)	RQCT		

NOTES: TBD: To be determined.
SS: Specification sheet value.
RQCT: Radiation quality-conformance test on 10 samples.
S: Screens.

Glossary of Terms

Design margin	The difference between the predicted failure level of an item and the specification level.
Hardness assessment	Determination of system vulnerability to nuclear environments.
Hardness assurance (systems)	Procedures applied during the production phase to insure the production line end product is in accord with the hardened design and in compliance withe the nuclear specifications.
Hardness dedicated (items)	Those items dedicated to achieving the required hardness and which generally serve no other purpose.
Hardness maintenance	Procedures applied during the operational phase to insure that the system's operational procedures, maintenance requirements, and aging characteristics do not degrade the system's operational capability below mission completion levels.
Hardness surveillance	Periodic test and inspection requirements performed during the operational phase to verify the adequacy of the hardness maintenance program.
Hardness validation	Verification of system survivability in a nuclear environment.
Hi-Rel	A term which describes piece-parts and manufacturing processes in which the yield is high and the manufacturing process is "perfected" or "mature." The term generally applies to military approved manufacturer's high-reliability standard.
Supplier	Manufacturer or other organization which qualifies parts for more than one system.
Survivability	The capability of a system to withstand an unnatural hostile environment (man-made) and not suffer abortive impairment of its ability to accomplish its designated mission.
S/V relationship	When the level of hardness of a system is less than the specified nuclear environment, the system is vulnerable in that environment. However, the system will still be survivable if those environmental effects do not impair its performance to the extent that they prevent mission completion.
User	The organization which qualifies parts for one specific system applications.

Vulnerability	The characteristics of a system which causes it to suffer finite degradation in its capability to perform its designated mission as a result of having been subjected to a hostile environment.

LITERATURE CITED

1. R. Patrick and J. Ferry, Nuclear Hardness Assurance Guidelines for Systems With Moderate Requirements, Air Force Avionics Laboratory, (September 1976).

2. G. C. Messenger and E. L. Steele, Statistical Modeling of Semiconductor Devies for the TREE Environment, IEEE Trans. Nucl. Sci. NS-15 (December 1968), 133.

3. J. R. King, Probability Charts for Decision Making, Industrial Press (1962).

4. A. J. Duncan, Quality Control and Industrial Statistics, R. D. Irwin, Inc. (1959).

5. A. R. Hart, et al., Parameter Sensitivities for Hardness Assurance: Displacement Effects in Bipolar Transistors, Final Report, Mission Research Corporation Report MRC/SD-R-20 (December 1977).

6. G. C. Messenger, Hardness Assurance Consideration for the Neutron Environment, IEEE Trans. Nucl. Sci. NS-22, (December 1975), 2308

7. R. A. Berger, Hardness Assurance for Neutron-Induced Displacement Effects in Semiconductor Devices, IRT Report IRT 8166-004 (March 1978).

8. J. W. Downs, Relative Hardness of Bipolar Transistors to Tactical Levels of Neutron Irradiation (Naval Surface Weapons Center/WOL/TR-75-126 (October 1975).

9. D. R. Alexander et al., Hardening Options For Neutron Effects - An Approach For Tactical Systems, IEEE Trans. Nucl. Sci. NS-23 (December 1976), 1691.

10. Motorola Corporation, Switching Transistor Handbook (1963).

11. R. P. Donovan et al., A Survey of the Vulnerability of Contemporary Semiconductor Components to Nuclear Radiation, Air Force Avionics Laboratory TR-74-61 (June 1974).

12. Motorola Semiconductor Data Library, Series A, 3 (1974).

13. Texas Instruments, The TTL Data Book, Second Edition (1976).

14. Allan H. Johnston and Robert L. Skavland, Terminal Measurement for Hardness Assurance in TTL Devices, IEEE Trans. Nucl. Sci. NS-22, (December 1974), 2303.

15. M. Simons et al., Integrated Circuits for Radiation-Hardened Systems: A State-of-the-Art Review, Air Force Avionics Laboratory TR-76-194 (January 1977).

16. Allan H. Johnston and Robert L. Skavland, Neutron Hardness Assurance Techniques for TTL Integrated Circuits, IEEE Trans. Nucl. Sci. NS-21 (December 1974), 393.

17. I. Arimura, A Study of Electronics Radiation Hardness Assurance Techniques, Air Force Weapons Laboratory TR-73-134 (January 1974.)

18. D. J. Hamilton and W. G. Howard, Basic Integrated Circuit Engineering, McGraw-Hill (1975).

19. Allan H. Johnston, Application of Operational Amplifiers to Hardened Systems, IEEE Trans. Nucl. Sci. NS-24 (December 1977), 2071.

20. Allan H. Johnston, Hand Analysis Techniques for Neutron Degradation of Operational Amplifiers, IEEE Trans. Nucl. Sci. NS-23, (December 1976), 1709.

21. R. A. Bailey et al., A Neutron Hardness Assurance Screen Based on High Frequency Probe Measurements, IEEE Trans. Nucl. Sci. NS-23, (December 1976), 2020.

APPENDIX A
STANDARDS

In this appendix the uniform test methods for neutron hardness assurance are summarized. The applicable ASTM documents are listed in table A-1, the MIL-STD 883B test methods in table A-2, the MIL-STD 750B test methods in table A-3, and the parameters for which no standards exist in Table A-4.

The American Society for Testing and Materials (ASTM) is an organization devoted to the promotion of standardization. The Defense Material Specifications and Standards Office (DMSSO) administers the Defense Standardization Program, which encompasses the development, application, and maintenance of Department of Defense (DoD) standards (MIL-STD's). MIL-STD's are specifications and procedures which must be complied with by all DoD organization and contracting agencies.[1]

The interaction between the ASTM and the DoD is changing. At one time the DoD probably purchased better than 50 % of U.S. high technology electronic parts.[1] As a consequence it was logical for the DoD to write the specifications at that time. Now, however, the market percentage has shrunk to below 50 %, so it is in the best interests of the DoD to take advantage of ASTM standards that exist or that will be developed. Thus DoD instruction 4120.20[2] includes the following provision:

> "It is desired that non-Government specifications and standards be adopted and used in lieu of the development and promulgation of a new document when there is no substantial or demonstrable advantage to the Department of Defense in the development of a new document. . ."

As a result the DoD has already adopted more than 500 ASTM standards with an even larger number of existing standards currently under consideration for adoption.

---

[1] *L. Fox, "DoD and ASTM," ASTM Standardization News, January 1978.*

[2] *DoD Instruction 4120.20, "Development and Use of Non-Government Specifications and Standards," December 1976.*

Table A-1

ASTM DOCUMENTS*

TEMPORARY STANDARD NUMBERS	
F466-76T	Method of Test for Determining the Small-Signal Scattering Parameters of Low-Power Transistors in the 0.2 to 2 GHz Range (June 1977).
F528-77T	Method of Measurement of Common Emitter dc Current Gain of Junction Transistors (June 1977).
EXX1	Method for Irradiating a Standard Set of Neutron Threshold Activation Foils for Radiation Hardness Testing (June 1977)
EXX2	Method for Measuring Neutron Activated Foils for Radiation Hardness Testing (June 1977).
EXX3	Methods for Using SAND II for Unfolding Neutron Spectra for Radiation Hardness Testing (June 1977).
EXX4	Recommended Practice for Characterizing Neutron Spectra in Terms of 1 MeV Equivalent Fluence for Radiation Damage in Silicon (June 1977).
EXX5	Recommended Practice for Measuring the Relative 1 MeV Silicon Equivalent Fluence with Fast Neutron Monitors (June 1977).
DRAFT DOCUMENTS	
11B11	Method of Test for Small-Signal Common-Emitter Current Gain of Transistors (Out for Letter Ballot, February (1978).
TEMPORARY STANDARD NUMBERS	
11A22	Method of Test for Transistor Collector-Emitter Saturation Voltage (round-robin started, February 1978).
--	Method of Test for Sink Current (first draft submitted February 1978).

*The ASTM document numbers listed here are all temporary numbers which will change when the final standard is issued.

Table A-2

RELEVANT NEUTRON HARDNESS ASSURANCE TEST METHODS OF MILITARY STANDARD 883B, TEST METHODS AND PROCEDURES FOR MICROELECTRONICS (AUGUST 1977)

METHOD NUMBER	TITLE
1017	Neutron Irradiation
4001	Input Offset Voltage and Current and Bias Current
4002	Phase Margin and Slew Rate
4004	Open Loop Performance (needs more notes added – see Section 7.1.2)

Table A-3

RELEVANT NEUTRON HARDNESS ASSURANCE TEST METHODS OF MILITARY STANDARD 750B, TEST METHODS FOR SEMICONDUCTOR DEVICES (FEBRUARY 1970)

METHOD NUMBER	TITLE
3071	Saturation Voltage and Resistance
3076.1	Forward Current Transfer Ratio
3301	Small-Signal Short-Circuit Forward-Current Transfer-Ratio Cutoff Frequency
3413	Drain Current
3423	Small Signal Drain-to-Source "ON" State Resistance

Table A-4

NEUTRON HARDNESS ASSURANCE PARAMETERS

FOR WHICH NO STANDARDS EXIST

DIGITAL IC
$V_{OH'}$, the modified V_{OH} measurement of Reference 14
I_{SK}, the sink current (the ASTM has a first draft)
LINEAR IC
I_{EE}, the power supply current
I_I, the input differential stage bias current
I_{OSC}, the output short circuit current
Method 4004, 883B, needs to have the cautionary notes of Section added

ASTM documents can be obtained from the ASTM, 1916 Race Street, Philadelphia, PA 19103. Military Standards and NASA documents can be obtained from the Superintendent of Documents, Government Printing Office, Washington, DC 20402.

APPENDIX B
CERTIFICATION REQUIREMENTS FOR BIPOLAR DEVICES FOR NEUTRON HARDNESS ASSURANCE

B-1 SCOPE

The final version of this appendix is intended as an appendix to MIL-STD-976, Certification Requirements for JAN Microcircuits (August 1977), and conforms to the definitions and general requirements therein. This appendix identifies those special certification requirements necessary for effective process controls in a neutron hardness assurance plan.

B-2 REFERENCED DOCUMENTS

In addition to those documents referenced in MIL-STD-976, the following apply:

Neutron Test Procedures, MIL-STD-883B, Method No. 1017.
ASTM Methods and Recommended Practices for Neutron Testing: EXX1 through EXX5.

B-3 DEFINITIONS

All needed definitions are contained in MIL-STD-976.

B-4 GENERAL REQUIREMENTS

The general requirements conform to MIL-STD-976.

B-5 DETAIL REQUIREMENTS

In addition to Sections 4 and 5 of MIL-STD-976, the manufacturer shall document, control, and meet the following requirements.

B-5.1 Neutron Radiation Tests

B-5.1.1 Certification of Radiation Test Facilities

Documents shall be maintained which specify the calibration techniques and test methods of the radiation facility. This will include the neutron dosimetry techniques, neutron fluence levels, pulse lengths, method for characterizing neutron spectra, and other information relative to radiation tests.

B-5.1.2 Neutron Radiation Tests

For each test, a radiation test report will be filed, giving the device serial numbers, pre-irradiation and post-irradiation data, irradiation levels, dosimetry, neutron-to-gamma ratio at the test position, and other related information.

B-5.2 Line Requirements

Process controls shall meet the requirements of the detail specification for each device. Those process-related parameters which have been identified as sensitive to device neutron degradation are

transistor base width,
transistor base doping profile, and
configuration.

Tolerances will need to be specified for each of the above parameters for each device type after a mature line has been characterized.

DISTRIBUTION LIST

Defense Documentation Center
ATTN: DDC-TCA (12 copies)

Harry Diamond Laboratories
Adelphi, Maryland 20783
ATTN: Harvey Eisen
Branch 280 (50 copies)

ATTN: Library (3 copies)

ATTN: Editorial
Committee
(Chairman)
Branch 013 (1 copy)

ATTN: Branch 041
(Record Copy) (1 copy)

IRT Corporation
P. O. Box 80817
San Diego California 92138
ATTN: R. Berger (2 copies)

J. Azarewicz (2 copies)

B. Passenheim (2 copies)

IRT Library (2 copies)

Publications
Department (1 copy)